AUDIO/VIDEO
REFERENCE MANUAL

1992

ADCs
DACs
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ANALOG DEVICES

AUDIO/VIDEO
REFERENCE MANUAL

OP AMPS • AUDIO ADCs • VIDEO ADCs •
AUDIO DACs • VIDEO DACs • SPECIAL FUNCTION AUDIO •
SPECIAL FUNCTION VIDEO • DSP • APPLICATION NOTES

ANALOG DEVICES

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Sweden:
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General Information
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Since its founding in 1965, Analog Devices has dedicated itself to the design, manufacture and marketing of products used in real-world signal processing applications. Our product universe includes data converters, operational amplifiers, digital signal processors, special function devices and application specific ICs that combine these functions on a single chip.

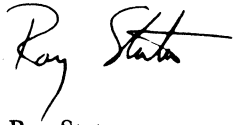
Analog's core strengths are its analog circuit design expertise and state-of-the-art linear and mixed-signal semiconductor process technology, which have led to a long list of technically innovative products. These strengths are supported by a number of manufacturing locations around the world and by a technical sales force trained and ready to serve your needs.

The decade of the '90s offers many exciting opportunities for linear and mixed-signal ICs for a wide range of emerging applications in computer peripherals, telecommunications equipment and consumer products, including the automotive market. Many of these involve processing audio and/or video information, which has become an increasingly significant part of Analog's business in recent years, and which was enhanced last year by the acquisition of Precision Monolithics.

Among other successes, our efforts to provide technically innovative and economically practical products for audio and video signal processing applications have resulted in Analog becoming a leading supplier of both D/A converters used in compact disc players and RAM-DACs used in VGA displays. And our monolithic SSM-2125 Dolby Pro-Logic Surround Sound Decoder has been recognized as the best integrated solution available for implementing this function in consumer electronics products.

This first edition of our *Audio/Video Reference Manual* is a clear sign of our commitment to continue developing and marketing high performance integrated circuits for a wide range of audio and video signal processing applications in professional, consumer, automotive, medical, military and industrial applications. Here you will find data sheets containing complete specifications and applications information on 103 product families, as well as 40 application notes to assist you in your product development efforts.

The products described in this reference guide represent integrated solutions that offer higher performance, increased reliability and lower overall cost, and as a consequence, will help you design products that make your company more competitive in its markets. We look forward to serving your needs for these types of products for many years to come.



Ray Stata
Chairman of the Board
Chief Executive Officer
Analog Devices

Introduction

Analog Devices designs, manufactures and sells worldwide sophisticated electronic components and subsystems for use in real-world signal processing. More than six hundred standard products are produced in manufacturing facilities located throughout the world. These facilities encompass all relevant technologies, including several embodiments of CMOS, BiMOS, bipolar and hybrid integrated circuits, each optimized for specific attributes—and assembled products in the form of potted modules, printed-circuit boards and instrument packages.

State-of-the-art technologies (including surface micromachining) have been utilized (and in many cases invented) to provide timely, reliable, easy-to-use advanced designs at realistic prices. Our popular IC products are available in both conventional and surface-mount packages (SOIC, LCC, PLCC), and many of our assembled products employ surface-mount technology to reduce manufacturing costs and overall size. A quarter-century of successful applications experience and continuing vertical integration insure that these products are oriented to user needs. The ongoing application of today's state-of-the-art and the invention of tomorrow's state-of-the-art processes strengthen the leadership position of Analog Devices in standard data-acquisition and signal-processing products and make us a strong contender in high performance mixed-signal ASICs.

MAJOR PROGRESS

Audio electronic components are an important subset of products for equipment designers instrumenting the multimedia interface between information in electronic form and human communication capabilities (particularly sight, speech, hearing, and the audible and visual arts).

The *Audio Handbook*, published by Precision Monolithics, Inc. —which was acquired by and became a Division of Analog Devices in 1990—described many of our analog IC products for the audio equipment subset. However, we also manufacture many analog, digital, and mixed-signal products that are useful in the processing and display of video signals, as well as conversion products for professional and consumer audio equipment. It appeared to make good sense in this new edition to expand the publication's concept to include all products—including many new ones—designed for the multimedia interface.

Important products described here that we have introduced for this industry include:

- the AD9020/9060 families of 10-bit "flash" converters that provide interfacing for both conventional and HDTV digital video systems
- the ADSP-2105 and ADSP-21020 fixed- and floating-point digital signal processors for high speed implementation of computational algorithms
- the ADV7141/46/48 CEG/DAC™ family of monolithic RAM-DACs, designed to eliminate "jaggies" and improve color resolution in VGA displays at low cost
- the AD712 family of low-noise-and-distortion op amps for audio preamplification
- the AD847 op amp for video line driving and other high speed applications
- the AD1879 dual-channel 18-bit ADC and the AD1865 dual-channel DAC for stereo applications
- the DAC-8840 and DAC-8841 TrimDACs™ for digitally controlled circuit parameter adjustment
- the SSM-2018 voltage-controlled amplifier, for audio panning, equalization, remote volume control, and compressor/limiter applications—using patented Operational Voltage-Controlled-Element (OVCE) architecture
- the SSM-2125 Dolby* Pro-Logic Surround Sound Matrix Decoder, a low cost chip that gives home-entertainment system manufacturers a practical way to bring the benefits of theater-type sound to consumers
- the SSM-2142 and SSM-2141 balanced line driver and line receiver for transporting analog signals with minimal signal degradation

Many more could have been added to this list.

AUDIO/VIDEO REFERENCE MANUAL

The *Audio/Video Reference Manual* is one of a set of books cataloguing Analog Devices products. It is accompanied by the *Linear Products Databook* and the two-volume *Data Converter Reference Manual*.

This volume provides comprehensive technical data and application notes on 103 Analog Devices product families designed for incorporation in professional and consumer audio, video, imaging, and multimedia equipment. Included are the following:

- comprehensive data sheets and package information
- selection guides for finding products rapidly
- a set of 40 application notes
- ordering guide, publications list, and worldwide sales directory
- indexes:
  —application notes, by topic and by part numbers
  —all Analog Devices products, listed alphanumerically by part number and keyed to catalog location.

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TECHNICAL SUPPORT

Our extensive technical literature discusses the technology and applications of products for real-world signal processing. Besides tutorial material and comprehensive data sheets, including a large number in our Databooks, we offer Application Notes, Application Guides, Technical Handbooks (at reasonable prices), and several free serial publications; for example, *Analog Productlog* provides brief information on new products being introduced, and *Analog Dialogue*, our technical magazine, provides in-depth discussions of new developments in analog and digital circuit technology as applied to data acquisition, signal processing, control, and test. *DSPatch*™ is a quarterly newsletter that brings its readers up-to-date applications information on our DSP products and the general field of digital signal processing. We maintain a mailing list of engineers, scientists, and technicians with a serious interest in our products. In addition to Databook catalogs—and general short-form selection guides—we also publish several short-form catalogs on specific product families. You will find typical publications described on pages 13-4 to 13-7 at the back of the book.

SALES AND SERVICE

Backing up our design and manufacturing capabilities and our extensive array of publications, is a network of distributors, plus sales offices and representatives throughout the United States and most of the world, staffed by experienced sales and applications engineers. Our Worldwide Sales Directory, as of the publication date, appears on pages 13-8 and 13-9 at the back of the book.

RELIABILITY

The manufacture of reliable products is a key objective at Analog Devices. The primary focus is the companywide Quality Improvement Process (QIP). In addition, we maintain facilities that have been qualified under such standards as MIL-M-38510 (Class B and Class S) for ICs in the U.S. and MIL-STD-1772 for hybrids. Many of our products—both proprietary and second-source—have qualified for JAN part numbers; others are in the process. A larger number of products—including many of the newer ones just starting the JAN qualification process—are specifically characterized on Standard Military Drawings (SMDs). Most of our ICs are available in versions that comply with MIL-STD-883C Class B, and many also comply with Class S. We publish a *Military Products Databook* for designers who specify ICs and hybrids for military contracts. The 1990 issue consists of two volumes with data on 343 product families; the 120 entries in the second of those volumes describe qualified products manufactured by our PMI Division. A newsletter, *Analog Briefings*®, provides current information about the status of reliability at ADI.

Our PLUS program makes available standard devices (commercial and industrial grades, plastic or ceramic packaging) for *any* user with demanding application environments, at a small premium. Subjected to stringent screening, similar to MIL-STD-883 test methods, these devices are suffixed "/+" and are available from stock.

PRICES

Accurate, up-to-date prices are an important consideration in making a choice among the many available product families. Since prices are subject to change, current price lists and/or quotations are available upon request from our sales offices and distributors.

How to Use This Book

THIS IS THE ANALOG DEVICES AUDIO/VIDEO REFERENCE MANUAL

It contains Data Sheets, Selection Guides and Application Notes on IC products for audio and video equipment design.

It is one member of a four-volume set of reference manuals on Linear, Converter and Audio/Video products from Analog Devices, Inc., in IC, hybrid and assembled form for measurement, control and real-world signal processing.

IF YOU KNOW THE MODEL NUMBER

Turn to the product index at the back of the book and look up the model number. You will find the location of any product catalogued in this volume or those listed below, with the Volume-Section-Page location of any data sheet in this volume.

IF YOU DON'T KNOW THE MODEL NUMBER

Find your functional group in the list on the opposite page. Turn directly to the appropriate Section. You will find a functional Selection Guide at the beginning of the Section. The Selection Guides will help you find the products that are the closest to satisfying your need. Use them to compare all products in the category by salient criteria. A comprehensive Table of Contents (of this volume) is provided for your convenience on pages 1–7 through 1–10.

IF YOU CAN'T FIND IT HERE . . . ASK!

If it's not an audio/video product, it's probably in one of the two companion reference manuals, the *Linear Products Databook* or the *Data Converter Reference Manual*. If you don't already own these volumes, you can have them FREE by getting in touch with Analog Devices or the nearest sales office, or by phoning 1-800-262-5643 (U.S.A. only) or (617) 329-4700, Ext. 3392.

See the Worldwide Sales Directory on pages 13–8 and 13–9 at the back of this volume for our sales office phone numbers.

Contents of Other Reference Manuals

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Selection Guide
Operational Amplifiers

Video Amplifiers

Model	SR V/μs typ	ΔP deg typ	ΔG % typ	Settling Time ns to % typ	BW at A_{CL} Min MHz typ	A_{CL} V/V min	V_{OS} mV max	Input Bias Current μA max	Voltage Noise nV/√Hz @ 10 kHz	I_{OUT} mA min	Supply Range ±Volts	Supply Current mA typ	Spice Model Avail.	Page	Comments
AD811	2500	0.01	0.01	65–0.01	120	1	3	10	2	100	4.5 to 18	16.5	X	2-41	Best Video Specifications Flatness = 0.1 dB to 35 MHz
AD844	2000	0.025	0.008	100–0.1	60	−1	0.15	0.25	2	20	4.5 to 18	6.5		2-101	Constant 10 ns Rise Time for Any Pulse
OP160	1300	0.04	0.04	75–0.1	90	1	5	20	5.5	35	4 to 15	6.5	X	2-225	Disable Mode for Low Power Applications
OP260	1000	0.067	0.02	250–0.1	90	1	3.5	8	5.5	35	4 to 15	9	X	2-267	Dual OP160; Only Dual Transimpedance
AD5539	600	0.1	0.04	12–1	220	2	3	13	6	15	4.5 to 10	14		2-153	Improved Replacement for Industry Standard
AD846	450	0.03	0.01	110–0.01	80	−1	0.075	0.25	2	20	5 to 18	5	X	2-121	Highest DC Precision High Speed Amplifier
AD840	400	0.04	0.025	100–0.01	40	10	0.3	5	4	50	5 to 18	10.5	X	2-65	Fast Settling Time; Gain > 10
AD842	375	0.035	0.015	100–0.01	40	2	1	5	9	100	5 to 18	13		2-81	High Current Output; Gain > 2
AD841	300	0.02	0.03	110–0.01	40	1	1	5	13	50	5 to 18	11		2-73	Fast Settling Time and Unity Gain Stable
AD847	300	0.2	0.04	120–0.1	50	1	1	5	15	20	4.5 to 18	5.3	X	2-133	General Purpose, Low Power, Unity Gain
AD827	300	0.2	0.04	120–0.1	50	1	2	7	15	20	4.5 to 18	10	X	2-45	Dual AD847
AD829	300	0.04	0.02	90–0.1	50	1	0.5	7	2	20	4.5 to 18	5	X	2-53	Low Noise and High Speed
AD848	300	0.08	0.07	100–0.1	35	5	1	5	5	20	4.5 to 18	5.1	X	2-145	General Purpose, Low Power, Gain > 5
AD849	300	0.04	0.08	80–0.1	30	25	0.75	5	3	20	4.5 to 18	5.1		2-145	General Purpose, Low Power Preamplifier
AD843	250	0.025	0.025	135–0.01	34	1	1	0.001	19	50	4.5 to 18	12		2-89	High Performance, Replaces LH0032
OP64	170	0.018	0.045	100–0.1	16	5	1	1	8	50	5 to 18	6.2	X	2-211	Stable for Gains > 5
AD845	100	0.025	0.04	350–0.01	16	1	0.25	0.001	18	25	4.75 to 18	10		2-113	General Purpose. Unity Gain Stable

Selection Guide
Operational Amplifiers

Audio Amplifiers
Single Op Amps

Model	Voltage Noise @ 1 kHz nV/√Hz typ	SR V/μs typ	GBW MHz typ	Supply Current mA max	V_{OUT} Volts min	Page	Comments
AD829	2	300	750	6.8	±10, R_L = 500 Ω	2-53	Ideal High Gain, Low Noise Input Device
AD846	2	450	80	6.5	±10, R_L = 500 Ω	2-121	Current Feedback
AD844	2	2000	60	7.5	±10, R_L = 500 Ω	2-101	Low Noise, Highest Slew Rate
OP27	3	2.8	8	4.67	±10, R_L = 600 Ω	2-169	Low Cost, Precision
OP37	3	17	63	4.67	±10, R_L = 600 Ω	2-181	$A_{VCL} \geq 5$, Low Cost
OP61	3.4	40	200	8	±11, R_L = 500 Ω	2-193	$A_{VCL} \geq 10$
SSM2134	3.5	13	10	6.5	±12, R_L = 600 Ω	2-325	Improved 5532
OP160	5.5	1300	90	8	±11, R_L = 500 Ω	2-225	Current Feedback
OP64	8	170	80	8	±10, R_L = 200 Ω	2-211	$A_{VCL} \geq 5$, High Output Current
SSM2131	13	50	10	6.5	±11.5, R_L = 1000 Ω	2-315	Ultralow Distortion
AD711	18	20	4	2.8	+13/−12.5, R_L = 2000 Ω	2-5	Precision BiFET
AD843	19	250	34	13	±10, R_L = 500 Ω	2-89	Low Bias Current, Fast Settling
AD845	25	100	16	12	±12.5, R_L = 500 Ω	2-113	Low Bias Current, Faster Settling

Dual Op Amps

Model	Voltage Noise @ 1 kHz nV/√Hz typ	SR V/μs typ	GBW MHz typ	Supply Current mA/Amp max	V_{OUT} Volts min	Page	Comments
SSM2139	3.6	11	30	3.25	±12, R_L = 2000 Ω	2-331	$A_{VCL} \geq 3$
OP275	5	20	8	2	±13, R_L = 600 Ω	2-297	Ultralow Distortion
OP260	6	1000	90	5.25	±12, R_L = 1000 Ω	2-267	Current Feedback
OP271	7.6	8.5	5	3.25	±12, R_L = 2000 Ω	2-287	Precision
OP249	17	22	4.7	3.5	±12, R_L = 2000 Ω	2-249	Low Power, Low Distortion
AD712	18	20	4	2.8	+13 −12.5, R_L = 2000 Ω	2-17	Low Cost, Dual AD711

Quad Op Amps

Model	Voltage Noise @ 1 kHz nV/√Hz typ	SR V/μs typ	GBW MHz typ	Supply Current mA/Amp max	V_{OUT} Volts min	Page	Comments
OP471	6.5	8	6.5	2.75	±12, R_L = 2000 Ω	2-299	Precision
AD713	18	20	4	3	+13/−12.5, R_L = 2000 Ω	2-29	Quad AD711

Audio Analog-to-Digital Converters

Model	Res Bits	Converter Type	Channels	SNR 0 dB–dB typ	THD+N % typ	Input Architecture	Input Range Volts	Supplies Volts	Power mW typ	Pins	Page
AD1876	16	Sampling	Single	No Spec	90[1]	Single-ended	±3 V	±5, ±12	235	16	3-3
AD1879	18	ΣΔ	Dual	103	98	Differential	±3 V	±5	1100	28	3-17
AD1878	16	ΣΔ	Dual	98	98	Differential	±3 V	±5	1100	28	3-15
AD1885	16	ΣΔ	Dual	85	85	Differential	±3 V	±5	500	28	3-19

[1]–0.05 dB Input, A-Weighted Filter

Video Analog-to-Digital Converters

Model	Res Bits	Sample Rate (MSPS)	Input Bandwidth MHz, –3 dB	Power Dissipation W	Page	Comments
AD9048	8	35	15	0.55	4-31	
					4-31	
					4-31	
					4-31	
AD773	10	18	100	1.3	4-3	On-Board Track and Hold, Evaluation PCB
AD9020	10	60	175	2.8	4-19	Evaluation PCB
					4-19	
AD9060	10	75	175	2.8	4-39	Evaluation PCB
					4-39	

Selection Guide

Audio Digital-to-Analog Converters

Model	Res Bits	Channels	SNR 0 dB–dB typ	THD+N % typ	Supplies Volts	Power mW typ	Pins	Page
AD1851	16	Single	110	0.003	±5	100	16	5-13
AD1856	16	Single	No Spec	0.002	±5 to ±12	110	16	5-3
AD1860	18	Single	No Spec	0.002	±5 to ±12	110	16	5-21
AD1861	18	Single	110	0.003	±5	100	16	5-3
AD1862	20	Single	119	0.0012	±5 to ±12	288	16	5-33
AD1864	18	Dual	108	0.0017	±5 to ±12	225	24 / 28	5-43
AD1865	18	Dual	110	0.0017	±5	225	24 / 28	5-55
AD1866	16	Dual	95	0.005	5	45	16	5-65
AD1868	18	Dual	97.5	0.004	5	50	16	5-67

Video Digital-to-Analog Converters

Model	Clock Rate MHZ	D/A Converter Organization	RAM (Color Palette) Size	Overlays	Page	Comments
ADV471	35, 50, 66, 80	Triple 6-Bit	256 × 18	15 × 18	6-19	ADV478 Pin-Compatible
ADV476	35, 40, 50, 66, 80, 100	Triple 6-Bit	256 × 18		6-9	Triple 6-Bit RAM-DAC
ADV7141	35, 50, 66	Triple 6-Bit	256 × 18		6-49	CEG – Effective 24-Bit True Color
ADV7146	35, 50, 66	Triple 6-Bit	256 × 18		6-49	CEG – Effective 24-Bit True Color
ADV453	40	Triple 8-Bit	256 × 24	3 × 24	6-3	Triple 8-Bit RAM-DAC
ADV478	35, 50, 66, 80, 100	Triple 8-Bit	245 × 24	15 × 24	6-19	Triple 8-Bit RAM-DAC
ADV7148	35, 50, 66	Triple 8-Bit	256 × 24		6-49	CEG – Effective 24-Bit True Color
ADV7120	35, 50, 80	Triple 8-Bit			6-31	True Color DAC
ADV7121	35, 50, 80	Triple 10-Bit			6-37	True Color DAC
ADV7122	35, 50, 80	Triple 10-Bit			6-37	True Color DAC

Special Function Audio Products

Audio Preamplifiers (All Values Typical)

Model	Input Voltage Noise nV/√Hz, G = 1000	THD+N %, G = 1000, f = 1 kHz	Slew Rate V/μs	Gain Bandwidth MHz, G = 1000	CMRR dB, G = 1000 f = 60 Hz	Page	Comments
SSM-2015	1.3	0.007	8	0.7	100	7-59	Programmable Input Stage for Noise vs. Source Impedance Optimization
SSM-2016	0.8	0.009	10	0.55	100	7-65	±9 V to ±36 V Operation
SSM-2017	0.95	0.012	17	1	112	7-73	Only One External Component Required
						7-73	

Volume Control

Voltage Controlled Amplifiers (All Values Typical)

Model	# Channels	Audio Dynamic Range dB	THD+N %, @ 1 kHz G = 1	Gain/Atten Range dB	Gain Bandwidth MHz	Gain Core Class	Page	Comments
SSM-2013	1	106	0.004	115	0.8	A	7-51	Includes Mute Function
SSM-2014		Discontinued – Specify Pin-Compatible Upgrade SSM-2018						
SSM-2018	1	117[1]	0.006[2]	140	10	A/AB	7-81	Programmable Gain Core Class
							7-81	
SSM-2024	4	82	0.05			A	7-93	Lowest Cost Per VCA
SSM-2120/2	2	100	0.005	140	0.25	A	7-111	SSM-2120 Contains Two Level
							7-111	Detection Side Chains On-Chip
AD600	2	98		40	3980	A	7-5	32 dB/V Scale Factor
							7-5	
AD602	2	108		40	1258	A	7-5	32 dB/V Scale Factor
							7-5	

LogDACs

Model	# Channels	Step Resolution dB	Attenuation Range dB	Page	Comments
AD7111	1	0.375	89.6	7-9	8-Bit Control Input
AD7118	1	1.5	88.5	7-15	6-Bit Control Input

[1]Class AB
[3]Trimmed, Class AB

Selection Guide
Special Function Audio Products

Dolby* Pro-Logic Decoders** (All Values Typical Unless Otherwise Noted)

Model	Audio Dynamic Range dB	THD+N %, @ 1 kHz, 0 dBd = 500 mV rms	Min Channel Separation dB C_{IN} to L, R_{OUT}	Min Channel Separation dB All Other Channels	Page	Comments
SSM-2125	103	0.02	35	25	7-123	Autobalance, Noise Sequencer On-Chip
SSM-2126	103	0.02	25	25	7-123	Autobalance, Noise Sequencer On-Chip

Audio Line Driver and Receivers (All Values Typical)

Balanced Line Driver

Model	Audio Dynamic Range dB	THD+N %, @ 1 kHz V_{IN} = 10 V rms	Output CMRR dB, f = 1 kHz	Slew Rate V/μs	Page	Comments
SSM-2142	116	0.006	−45	15	7-139	No External Components Required, Drives Difficult Loads

Differential Line Receivers

Model	Audio Dynamic Range dB	THD+N %, @ 1 kHz, 10 V rms	Input CMRR dB, f = 60 Hz	Slew Rate V/μs	Gain	Page	Comments
SSM-2141	126	0.001	100	9.5	1	7-133	No External Components Required
SSM-2143	128	0.0008	90	10	1/2 or 2	7-145	No External Components Required

Audio Switches (All Values Typical)

Model	# Switches	Noise Voltage $nV\sqrt{Hz}$	THD+N % @ 1 kHz	OFF Isolation dB 20 Hz to 20 kHz	Charge Injection pC	Page	Comments
SSM-2402	2	1	0.003	120	50	7-167	Handles +24 dBu Signals (20 V supplies)
SSM-2404	4	0.8	0.0009	100	35	7-181	Lowest Cost-Per-Switch
SSM-2412	2	1	0.003	120	150	7-167	Faster Version of SSM-2402 (t_{ON} = 4 ms)

Matched Transistors

Model	Type	Voltage Noise Max $nV/\sqrt{Hz}$, f = 1 kHz	Hfe Min	Δhfe Max %, Ic = 1 mA	Unity Gain Bandwidth MHz, I_C = 10 mA (typ)	Voltage Offset Max μV	Page	Comments
SSM-2210	Dual NPN	1	300	5	200	200	7-147	Low Cost
SSM-2220	Dual PNP	1	80	6	180	200	7-159	Low Cost
MAT-04	Quad NPN	2.5	400	2	300	200	7-21	Low Cost

Other Special Function Audio Products

Model	Page	Comments
PKD-01	7-33	Monolithic Peak Detector
SSM-2110	7-99	RMS-to-DC Converter

*Dolby is a registered trademark of Dolby Laboratories Licensing Corporation, San Francisco, CA.
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Selection Guide
Special Function Video Products

CRT Geometry Correction Selection Guide

Model	Bandwidth MHz	Slew Rate	Peak Signal Amplitude V_P, I_P	Power Supplies Volts	Page	Comments
AD539	60		±1 mA Out, ±2 V In	±5 to ±15	8-3	2 CH, Current Output
AD633	1	20 V/μs	±10 V	±8.5 to ±15	8-11	V_{OUT}
AD734	10	450 V/μs	±10 V	±8.5 to ±15	8-21	V_{OUT}
AD834	500		±4 mA Out, ±1 V In	±5	8-33	Current Output
DAC8408	1	1 mA/μs	±1 mA Out, ±10 V In	+5	8-49	4 CH, I_{OUT}, Parallel Data In
DAC8800	DC		V_{SS} to $V_{DD}-4$ V	$(V_{DD}-V_{SS})<18$	8-63	8 CH, 10 kΩ, R_{OUT}, Serial Data In
DAC8840	1	1.3 V/μs	±3 V	V_{DD} = +5, V_{SS} = −5	8-77	8 CH, V_{OUT}, Serial Data In
DAC8841	1	1.3 V/μs	0 V to +3 V	V_{DD} = +5, V_{SS} = −5	8-87	8 CH, V_{OUT}, Serial Data In

Other Special Function Video Products

Model	Page	Comments
AD720	8-19	RGB to NTSC and PAL Converter
AD9300	8-41	4 × 1 Video Multiplexer

Digital Signal Processing Products

DSP Processor Key Feature Summary

Model	Instruction Cycle Time ns	Off-Chip Harvard Arch	Internal Program Memory RAM	Internal Data Memory RAM	Internal Program Cache Word	Program Memory Boot	Serial Ports	Programmable Timer	Ext Interrupts	Low Power Modes	Pin Count	Page
ADSP2100A	80	\			16 × 24				4		100	9-13
ADSP-2101	60		2K × 24	1K × 16		\	2	\	3	1	68	9-17
ADSP-2105	100		1K × 24	0.5K × 16		\	1	\	3	1	68	9-23
ADSP-2111	60		2K × 24	1K × 16		\	2	\	3	1	100	9-29
32/40-Bit Floating Point												
ADSP-21020	40	\			32 × 48				4	1	223	9-33

Product Assurance

PRODUCT ASSURANCE OVERVIEW

Introduction

Analog Devices has long been a leader in its innovations of analog integrated circuit design, processing, and testing. Of equal importance to innovation is its commitment to continuous improvement of quality, reliability and excellence in service. Achieving, and continuously striving to improve the quality and reliability have led to Analog's success as a world-recognized, leading supplier of analog integrated circuits.

Product Assurance Philosophy

Product Assurance's role within Analog Devices is many faceted. All of the traditional roles of Product Assurance are maintained, including Military Programs management, QA/Reliability conformance inspections, specification control, auditing, failure analysis, corrective action, calibration systems, as well as many other functions. In addition, Analog's Product Assurance departments maintain an active role in servicing internal operational entities' requirements as well as our customers' needs. This is accomplished through various programs aimed at improving product quality, reliability and service.

Continuous Improvement and Statistical Process Control Programs

Fundamental to our beliefs about manufacturing success is that quality and reliability are not inspected into the process as was the historical methodology, but instead built into the process from the outset. In order to be successful at consistently providing excellence in all areas, it is essential that the processes be measured, understood, and have controlled variance. Keeping this in mind, ADI has been aggressively pursuing statistical process control.

ADI is engaged in continuous improvement as an integral portion of our cultural development. The overall intent of this process has been to create an environment in which each employee is trained and is empowered to change and to improve the process. Essential to this environment are the absence of fear and an active encouragement to take risks to improve.

All manufacturing and related service personnel are trained in the concepts of problem solving and statistical process control (SPC) techniques. SPC training is also an orientation requirement for all new employees.

Quality improvement teams are continually being formed, as opportunities to improve and to implement change are identified. These groups have addressed many issues and have had a dramatic effect on ADI's manufacturing and administrative processes. These teams have typically crossed departmental and functional lines, as the effects of change or the type of problem could not be solved without cooperation and resultant expanded knowledge bases.

PRODUCT RELIABILITY

Reliability Assurance Programs

Reliability assurance programs at Analog Devices are designed to encompass all aspects necessary to achieve and to improve product performance and lifetimes. We recognize that reliability cannot be tested or screened in if the aggressive goals set by both our customers as well as ourselves are to be met.

The major areas of focus within Analog Devices include:

Design For Manufacturability (Design for Success). Product and process designs focus on achieving product performance and "building-in reliability." Causes for degraded reliability performance must be well understood and controlled. Reliability design rules, updated frequently as experience grows and the industry matures, are essential to improving product performance.

Process Capability. A new or an established process must not only be capable of meeting specification limits but must also exhibit a sufficient safety margin to ensure continued performance over the product life.

Manufacturing Process Control. Of utmost importance is the control of the manufacturing environment under which product is fabricated, assembled, tested or stored. Temperature, humidity, particulate, ionic contamination and equipment interactions must be well understood and controlled.

Process Monitoring. 100% inspections or sampling points of key parameters with appropriate controls on output are utilized throughout the manufacturing process. These include the following as listed in order of timeliness of information feedback:

In-line or in-situ measurements utilizing SPC.
Process step specific.
Wafer ship measurements.
Wafer level testing; i.e., sort, wafer level stress testing.
Die visual quality.
Final electrical testing after assembly.
Reliability stress testing of customer-ready finished goods.
Customer feedback.

Program Goal

Our goal is to provide our customers with the highest level of reliability performance obtainable. It is a program which is, by its nature at Analog Devices, an integral part of all new products and process introductions, as well as all changes made within the products, processes or facilities for which it measures.

Reliability Qualification Program

Analog Devices maintains a reliability qualification program that includes extensive use of accelerated stress testing. The program's intent is not only to meet the requirements of the military programs but also to provide products in plastic which, at minimum, meet or exceed world-class standards of excellence. All new processes and facilities are qualified. Any changes to existing qualified processes are also qualified as appropriate (see Process Change Notification section).

Reliability Monitor/Audit Program
Periodic monitoring of all fabrication and assembly locations is performed. The monitoring program uses highly accelerated stress testing in order to monitor our various processes. The program is geared to fabrication process and packaging families.

Process Change Notification System
Analog Devices has a standard procedure and criteria for classifying and controlling changes to our processes, packages, materials, facilities and manufacturing techniques. This system includes technical reviews of proposed changes, qualification plans including all considerations of MIL-M-38510, customer specification, as well as ADI's internal qualification requirements. Included in this program is a system to notify customers of the proposed changes in a timely fashion.

Reliability Definitions and Theory

Reliability The probability that a device or system will perform a required function satisfactorily or without failure (within specification limits) under stated conditions for a stated period of time. Reliability is described as a mathematical expression of probability.

Hazard Rate The instantaneous rate of failure for units of the population that have survived to a given time.

Failure Usually involves the degradation in performance to specified parameters which are typically electrically measurable.

Semiconductor failure patterns follow that of long-life devices and are typically described by the so-called "Bathtub Curve," named for its shape, as shown in Figure 1. There are three distinct regions on this curve: Early Life, Constant Failure Rate Life, and Wear-Out.

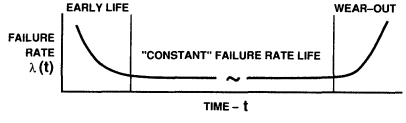

Figure 1. Semiconductor Failure Rate "Bathtub Curve"

Early Life Sometimes called infant mortality, early or initial failure time. This region may exhibit a high initial failure rate compared to the remaining population, typically because of defects from the manufacturing or assembly process. To a user the failures can also exhibit themselves due to debugging or misuse. Refer to Table I. Early failure rate reduction programs are in place throughout Analog Devices.

Table I. Early Life Failure Mechanisms (Infant Mortality)

Failure Mechanism	Defect	Stress Factors
Oxide ruptures	Thin or defective oxide (masking and oxidation)	System electrical noise/transients. System power interruptions. Inductive loading.
Open wire bonds	Assembly defects	Ultrasonic exposure during printed circuit board assembly. Excessive burn-in temperatures.
Lifted die bonds	Assembly defects	Excessive burn-in temperatures.
Fused die metallization		System electrical noise/transients. System power interruptions. Inductive loading.
Shorts	Inadequate spacing between adjacent traces.	
Opens	Inadequate trace width (masking and evaporation)	
Corrosion of wire bonds and/or die metallization	Seal leaks (defective encapsulation); poor lead frame/plastic adhesion at interface	Handling damage. Excessive solder heat during printed circuit board assembly. Ionic contamination.

Constant Failure Rate Region Also called the intrinsic or accidental failure time and is considered the useful life region of the product. This region is a mixture of any of the remaining manufacturing defects which require longer times to fail as well as the failures from the main distribution of the product.

Wear-out Region Alternately referred to as the degradation period. The failure rate continuously increases with time. Under typical use conditions, silicon semiconductor devices will never approach this region relative to system life expectancies (see Table II).

Table II. Wearout Failure Mechanisms

Failure Mechanism	Defect Observed	Contributing Factors
Electromigration	Voids, open circuits, hillock or metal accumulation.	Grain boundary diffusion. Grain size and distribution. Fiber texture.
Slow Trapping charge injection	Electrical degradation	Structural defects related to the oxidation process. Metallic impurities. Bond breaking processes.
Charge Accumulation mobile ions	Electrical degradation	Alkali ions—sodium, potassium and lithium in the oxide. Other negative ions/ heavy metals.
Intermetallic Growth in Al-Au wire bonds	Highly resistive bonds. Open circuit at bond. Bond lift failures.	Kirkendahl Voiding. Diffusion of Al into Au.
Wire and Wire Bond Failures during thermal cycling	Open/intermittent circuits. Short circuits.	A fatigue mechanism. Thermal mismatch. Stress induced wire creep. Intermetallics. Wire Length not optimized Too taut—breakage Too long —sag.

Life Distributions

Time-to-failure data is analyzed in order to predict the future reliability of the product. Four life distributions are typically used in the analysis of silicon semiconductor reliability.

1. Normal Distribution Function—Describe the wear-out region where there exists a monotonically increasing failure rate with respect to time.
2. Lognormal Distribution Function—The natural logarithm of the failure time is distributed normally. Extensive use of this distribution occurs, as it can be used to fit many different kinds of data.
3. Weibull Distribution Function—In this case the hazard rate varies as a power of device age. The failure-rate curve does not start at zero as is the case of the lognormal distribution.
4. Exponential Distribution Function—This distribution is used when the failure rate is constant. Failures occur randomly and are characteristic of the constant failure rate region of the "Bathtub Curve."

Accelerated Life Stress Testing

It is possible to evaluate the early life reliability levels from short-term burn-ins, customer system burn-ins, and early failure rates in the field. It is not practical, however, to evaluate the useful life or wear-out failure rates from these same sources. The amount of time necessary to obtain statistically significant data far exceeds the useful life of most systems. Obtaining data about the life of a semiconductor beyond the infant stage requires a higher than normal stress level to be applied to the device. In practice, a sample of devices of sufficient quantity to statistically represent the population is subjected to stress levels from various types of environmental stimuli to evaluate these failure levels and mechanisms. This type of testing is known as accelerated stress testing.

The time and temperature dependences of most semiconductor failure mechanisms over the life of a product have been studied and quantified. The established relationship between time, temperature, and particular failure mechanisms has been demonstrated to be a log-normal function capable of being represented by the "Arrhenius" model that includes the effects of temperature and activation energy of the failure mechanisms. It is possible, by using the model, to characterize failure modes from accelerated stress testing, and then to predict reliability levels at normal, nonaccelerated conditions.

As applied to accelerated life testing of semiconductors, the Arrhenius model assumes that the degradation of a performance parameter is linear with respect to time, with the mean time between failures (MTBF) as a function of the temperature stress. The temperature dependence is taken to be the exponential function that defines the probability of occurrence, resulting in the following formula for defining the lifetime or MTBF at a given temperature stress level:

$$t_1 = t_2 \exp[E_a/k(1/T_1 - 1/T_2)]$$

where:

t_1 = MTBF at junction temperature T_1
t_2 = MFBF at junction temperature T_2
T_X = junction temperature in °K
E_a = thermal activation energy in electron volts (eV)
k = Boltzman's constant (8.617×10^{-5} eV/°K

The activation energy in this formula is the mean E_a for all of the failure mechanisms of the particular product line for which the calculation is being done. These activation energies are established by the examination of failures from stress testing. See Table III.

Table III. Time-Dependent Failure Mechanisms in Silicon Semiconductor Devices[1]

Device Association	Failure Mechanism	Relevant Factors	Acceleration Factors	Acceleration (E_a eV = Apparent Activation Energy)
Silicon Oxide and Silicon-Silicon Oxide Interface	Surface Charge Accumulation	Mobile ions V, T	T	E_a = 1.0 – 1.5 eV depends on ion density
	Dielectric Breakdown	EF, T	EF, T	E_a = 0.2 – 1.0 eV, EF, (T) = 1 – 4.4
	Charge Injection	EF, T, Q_f	EF, T	E_a = 1.3 eV (slow trapping) E_a = −1 eV (hot electron ejection)
Metallization	Electromigration	T, J, A, Gradients of T and J, Grain Size	T, J	E_a = 0.5 – 1.2 eV J, (T) = 1–4
	Corrosion (chemical, galvanic, electrolytic)	Contamination H, V, T	H, V, T	Strong H effect E_a = 0.3 – 1.1 eV (for electrolysis) V may have thresholds
	Contact Degradation	T, Metals, Impurities	Varied	
Bonds and Other Mechanical Interfaces	Intermetallic Growth	T, Impurities, Bond Strength	T	Al – Au: E_a = 1.0 – 1.05 eV
	Fatigue	Bond Strength, Temperature Cycling	Temperature extremes in cycling	
Hermeticity	Seal Leaks	Pressure Differential, Atmosphere	Pressure	

NOTE
V-voltage, T-temperature; EF-electric field; J-current density; A-area; H-humidity; Q_f-charge
[1]D. S. Peck, "Practical Applications of Accelerated Testing—Introduction," Reliability Physics, 13th Annual Proceedings, 1975, pp. 253—254.

Reliability Testing

Standards Conformance. Test methods to confirm the reliability of Analog Devices product are detailed below, and are determined primarily through conformance to the various industry standards. These include MIL-STD, JEDEC, IEC, JIS, and EIAJ.

1. MIL-STD – U.S. Military Standards:
   MIL-STD-750 Test Methods for Semiconductor Devices
   MIL-STD-202 Test Methods for Electronics and Electrical Component
   MIL-STD-883 Test Methods and Procedures for Microelectronics
2. JEDEC
3. JIS – Japanese Industrial Standards:
   JIS-C-7022 Environmental Testing Methods and Endurance Testing Methods for Semiconductor Integrated Circuits.
4. IEC Standard:
   Publication 68 Basic Environmental Testing Procedures.
5. EIAJ Standard:
   IC-121 Test Methods for Reliability of Integrated Circuits.

Methods

High Temperature Operating Life Test (HTOL). The operating life test demonstrates the quality or reliability of devices subjected to the specified conditions over an extended time period. HTOL stressing applies a static DC bias at an elevated ambient temperature. This bias is maintained throughout the duration of the test as well as during cool-down from elevated temperature after stress. HTOL testing is particularly useful because it provides a means of accelerated time-to-failure of temperature sensitive failure mechanisms.

High Temperature Storage Life Test (HTSL). High temperature storage life testing is performed in order to demonstrate the quality or reliability of devices subjected to elevated temperature storage conditions without electrical bias.

Thermal Shock (TMSK). Thermal shock testing demonstrates the quality or reliability of devices exposed to extreme changes in temperature, especially to alternating extremes. The change in temperature is quite rapid as the heat transfer is by conduction and the transfer time from one temperature extreme to another in minimal (<10 sec.). Thermal shock testing induces mechanical stresses caused by thermal expansion and contraction. These stresses can be extreme, especially in plastic molded devices where large differences in the thermal coefficients of expansion between the die, leadframe and plastic material can exist. This is especially critical for large dies where the stress can be too severe and will induce failures that would not be

expected in a real application. As a result of the permanent changes in electrical and mechanical characteristics and/or physical damage that may result from thermal shock, any tests in which the duration is greater than ten cycles shall be considered destructive.

Temperature Cycle (TMCL). Temperature cycle testing is performed to demonstrate the quality or reliability of devices exposed to the extremes of high and low temperatures, and especially to alternating extremes. TMCL testing more closely relates to actual use conditions as the temperature change of the device is due to convection and, therefore, is at a slower rate than thermal shock. This slower rate of change will more closely simulate such use conditions as the transfer to or from heated storage in cold climates, or where ambient temperature is relatively mild but heats up greatly as the system is operating. This is a very good test to measure the overall die-to-package compatibility.

Temperature and Humidity Life (THB). Temperature and humidity life testing demonstrates the quality or reliability of devices exposed to the combination of high temperature and high humidity, with an applied voltage bias. Maximum bias voltage levels are desired as this bias accelerates any electrolysis of the device metalization as well as increasing ion mobility. At the same time, device power dissipation is desired to be minimized as any localized heating at die level will tend to lower the humidity level at the die surface and lessen the electrolysis potential. In certain cases, power cycling must be used in order to permit moisture accumulation on die surface during the "power-off" periods.

Autoclave/Pressure Pot (PTH). Autoclave testing evaluates the quality and reliability of devices exposed to a saturated humidity and high temperature environment under pressure. This test is performed without bias, and therefore, once equilibrium is reached, the die temperature and relative humidity will be the same as the external environment. PTH conditions, although not typical of actual operating environments, are very effective at evaluating the moisture resistance of a device/package combination in a relatively short period of time.

Biased Pressure Pot (HAST). Biased pressure pot testing evaluates the quality and reliability of devices under bias subjected to a humid, high temperature environment under pressure. This test can be considered an acceleration of the THB test due to the elevated temperature and steam environment which is under pressure. Biasing guidelines are the same as for THB testing, with an additional consideration: because of the elevated temperature, certain high power devices will dissipate sufficient power to elevate the die temperature above the glassivation temperature of the plastic molding compound. This could occur even though power cycling techniques are employed. This condition is not desired as abnormal conditions not related to real operating conditions could exist, resulting in anomalous failure mechanisms.

Resistance to Solder Heat (RTSH). Resistance to solder heat evaluates the ability of a product/package to withstand the worst-case heat cycles that could be encountered during normal printed circuit board assembly.

QUALITY ASSURANCE

Vendor Assurance Programs

Analog maintains an active program with its vendors to ensure that the highest standards of quality are met. The program focuses on many key areas including vendor qualification and certifications, periodic vendor audits, rigorous incoming inspection of fit, form, and function, as well as tracking the vendor performance over time.

Analog Devices has established minimum standards of performance for our vendors, who are audited for compliance to minimum standards. We then rate each vendor on the quality and delivery of incoming material. It is through this program that we can assess and then purchase material based upon cost-of-ownership. This contrasts to buying strictly on purchase price, as the purchase price alone does not completely reflect the total cost. Another benefit of our vendor quality program is that we have the necessary information to work in partnership with our vendors to continuously evaluate and improve the quality of incoming product.

Incoming Quality Assurance (IQA)

Analog Devices' IQA organization performs detailed inspections of vendor quality performance. Conformance to specification is directly measured to ensure compliance with the specified requirements. When a failure to meet the requirements is discovered, a corrective action from the vendor is required. Extensive follow-up is done to ensure future and continued compliance.

Vendor Audits

Analog Devices performs periodic audits of all of its manufacturing-related vendors. ADI performs these audits to assess compliance to MIL-Q-9858 and MIL-I-45208. Corrective action requests are issued with deadlines for compliance appropriate to the noncompliance. These audits are also used to discuss both open and closed quality, reliability, and service issues. Through this extensive interaction, ADI has been able to continuously improve the quality and reliability of incoming materials.

QUALITY CONTROL SYSTEMS

Corrective Action

An active, internal, closed loop-corrective action system has been utilized for many years both to communicate deficiencies as well as to provide traceability of corrective actions. This system has been a key element of process audits and customer return issues. The program has been very effective in correcting deficiencies in a timely manner.

Traceability and Record Retention

Traceability after shipment is maintained through actual marking of devices with lot identifiers. This information will provide traceability through assembly and wafer fabrication for all devices. This traceability allows for very good control of products as well as for direct correlation of products to time of process, machines, processes, and other pertinent related items.

Control of Nonconforming Material
Whenever nonconforming material is found, it is put under control for disposition. This holding of material is done at all stages in the process from incoming inspection through all inventory locations. Response to hold requests, whenever necessary, is quick and complete.

Process Audits – Fab, Assembly, and Test
In addition to auditing our venders, ADI has an ongoing internal process auditing group. This group audits all of Analog's manufacturing areas to ensure compliance to specification. In addition, selected service areas are audited where appropriate. Dedicated process auditors perform verifications in wafer fabrication, assembly and test. All types of critiques are used to review compliance, and the results are reviewed with appropriate supervisors and managers. The criticality of all deficient items is assessed and appropriate action is taken. Periodic reports are also issued to all levels of management.

Quality Conformance Inspections (QCI)
In-process QCI is employed throughout the manufacturing process to verify compliance to specification. All QCI is performed to specification and results are tracked and reported as appropriate. The QCI inspections include both very traditional and innovative methods to measure and to control product conformance. These inspections provide very valuable information about the processes they measure. Analog Devices uses these inspections and the results obtained to enhance, where appropriate, our statistical process control program.

Average Outgoing Quality (AOQL)
At the end of manufacturing processing, just prior to moving product into finished goods inventory, product is sampled for electrical, visual/mechanical and hermeticity to determine compliance to the requirements. The sampling and results include all products released to production and, therefore, include all new products and packages. These performance levels are tracked in very precise detail. Results of this inspection determine ADI's reported AOQ.

Added to this very extensive sampling program are quality improvement teams to address the findings. These teams meet on an ongoing basis to review the results, to determine root causes and to correct the processes as appropriate.

CUSTOMER SERVICE

Regional Customer Service Centers
Responsiveness to customer problems is a key factor in maintaining a leadership position in today's semiconductor marketplace. In order to improve support to Analog Devices' customers, five Regional Customer Service Centers have been established worldwide. These locations are strategically located within direct reach of our customers without having time zone logistics issues. Two centers are established in Asia (Japan/Taiwan), two are in the USA (Boston, MA/Santa Clara, CA), and one is in Europe (Ireland). These centers will provide Engineering Support to customers in the areas of failure analysis, problem resolution and reliability information.

The goals established for the Regional Customer Service Centers include the following:

- Assume regional failure analysis responsibility for all ADI monolithic products.
- Provide rapid response to customer perceived problems through correlation, failure analysis results and failure analysis.
- Minimize the impact of a field performance problem by immediate, on-site interaction with the customer.
- Provide to ADI a "voice of the customer" for field performance information.
- Improve customer satisfaction and become a competitive tool for ADI.
- Maintain the technical expertise required to meet customer and factory needs.
- Provide a single point of contact for all quality and failure analysis issues.

Customer Returns
The customer returns processing area, as well as evaluations of returned material, is administered by the Quality Assurance Engineering organization. QA Engineering receives the returned material, and also controls it until disposition. All customer returns are reviewed, verified, and/or failure analyzed as appropriate. Formal reports of findings are issued and appropriate actions are taken.

Periodic reports are issued to all levels of management and engineering. The reports provide details of any returned material as well as trend information to highlight appropriate areas for action.

The extensive evaluations of customer returns have, over time, been one of the more valuable feedbacks from the customer to ADI's internal systems. By directly working with both ADI's engineering and the customer, Analog has been able to supply its customers with the highest level of quality. Consistent processing and delivery of quality product that meets the customer's expectations are direct results of close working relationships.

Failure Analysis
Analog maintains a full service analytical laboratory staffed with professional engineers and technicians who analyze failures. The purpose of the laboratory is to provide, through detailed analysis, timely and effective feedback to customers on the quality and reliability of Analog's product. The analysis will involve the identification of the failure modes and mechanisms and probable failure causes. A complete written report is then supplied to the customer describing in detail the exact steps taken during the analysis and any conclusions drawn from the analysis. Where necessary, corrective actions are initiated based on the results and conclusions of the analysis. Thus, the results of analysis performed are fed back into the manufacturing process to continually improve the quality and reliability of Analog's product.

A flow of how Analog handles customer failure analysis is shown in Figure 2. Figure 3 shows a failure analysis approach diagram and Figure 4 shows a generalized failure analysis flow diagram.

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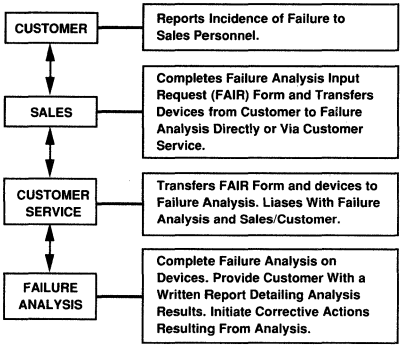


Figure 2. Failure Handling Procedure

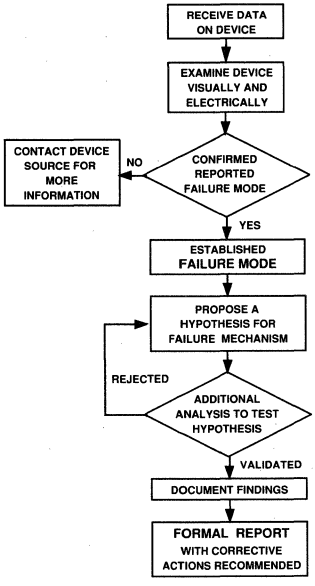


Figure 3. Failure Analysis Approach Flow Diagram

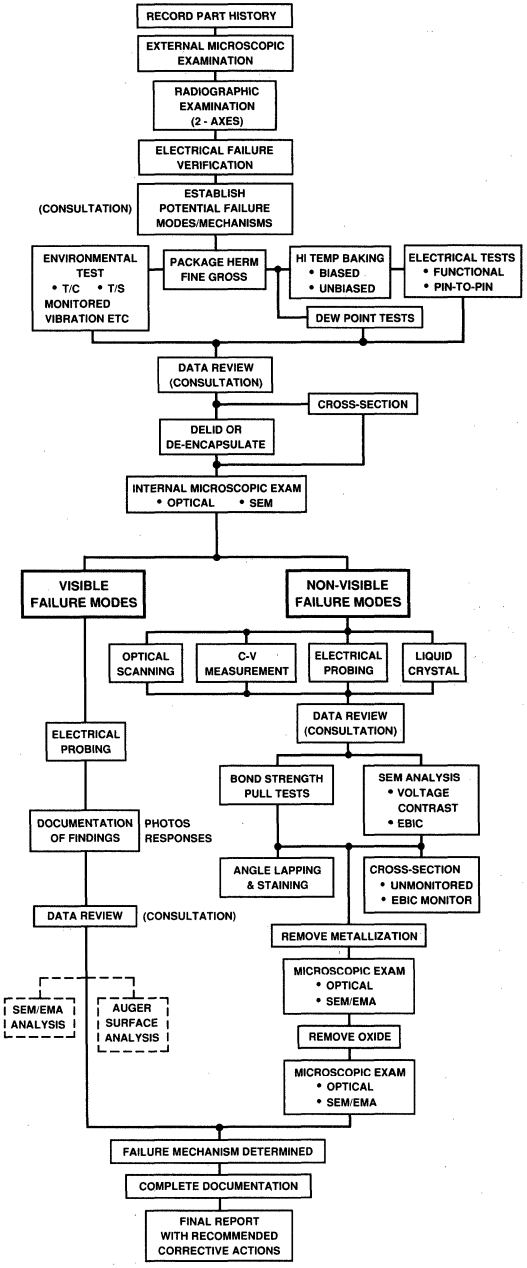


Figure 4. Generalized Failure Analysis Flow

Table IV. Failure Modes

Failure Mode	Definition	Effect on Device or IC
1. Internal Short	Short Circuit between Metallized Leads or Across Junction.	Short Circuit or Circuit Malfunction.
2. Internal Open	Open Circuit in the Metallization or Wire Bond	Open Circuit
3. Parametric Variation	Variation in Gain or Other Electrical Parameter	Marginal Performance, Temperature Sensitivity, or No Effect
4. Junction Leakage	Leakage Current Across P–N Junctions.	Effects Range from None to Malfunctions.
5. Threshold Shift	Shift in Turn-on Voltage.	Random Logic Malfunction
6. Seal Integrity	Ingress of Ambient Air, Moisture and/or Contaminants.	Effects Range from Degradation to Complete Malfunction.

Following are definitions used in ADI failure analysis:

Failure mode — the characteristic of a device for which the device has been characterized a failure, i.e., deviation from a specification or desired performance. A summary of failure modes is given in Table IV.

Failure mechanism — a physical process which leads to failure. The "physics of failure."

Ionic contamination — ionic species in the passivation layers can cause permanent or temporary threshold voltage shifts of the silicon surface below. This may cause leakage (channeling) between device elements resulting in nonfunctionality.

Electromigration — at high current densities atoms of the conductor material are swept along due to the momentum of the electron "wind." This creates a depletion of conductor material upwind and an accumulation downwind. Electromigration can cause open circuits or short circuits between closely spaced conductor lines.

Intermetallics — in the microdimensions of integrated circuits, the interactions between dissimilar metals cannot be ignored. These intermetallics can have radically different physical, chemical and electrical properties from those of the individual elements or compounds.

Radiation — the ionizing effects of radiation can generate electron-hole pairs. Recombination of these electron-hole pairs can result in latch-up, shorting paths, pin junction breakdown and excessive leakage. Robustness to these radiation effects is particularly important for semiconductors intended for space or military applications.

Mechanical — thermal cycling or power cycling can lead to device failure due to the differences in the coefficients of thermal expansion of the materials used in semiconductor manufacture. Coefficients of thermal expansion can range from 2 to over 40 ppm/°C. Fatigue of bond wires can occur during ultrasonic cleaning due to a high cycle fatigue mechanism. This happens in hermetic packages that are ultrasonically cleaned in a tank whose resonant frequency matches those of the bond wires.

Electrostatic discharge (ESD) and electrical overstress (EOS) — these are probably two of the most frequently identified failure mechanisms. ESD, created by the exchange of charge between two dissimilar materials, can cause pin junction damage as well as rupture of dielectrics. Although it generally has a short pulse width, the voltage and current transients generated can be extremely large. EOS is characterized by excessive voltages or currents that tend to be sustained for a much longer period than ESD pulses. It will cause conductor or wire bond burn-out as well as pin junction damage.

Corrosion — package environment, package moisture content, glassivation/passivation integrity, presence of ionic species and electrical bias conditions can all contribute to corrosion. Corrosion occurs when two or more electrodes are present in an electrolyte (typically moisture) along with some ionic species (contamination).

Figure 5 shows a summary of identified failure mechanisms from 1983 to 1990.

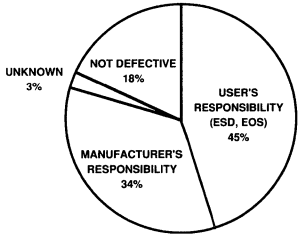


Figure 5. Identified Failure Mechanisms (1983–1990)

Operational Amplifiers
Contents

Selection Guide
Operational Amplifiers

Video Amplifiers

Model	SR V/μs typ	ΔP deg typ	ΔG % typ	Settling Time ns to % typ	BW at A_{CL} Min MHz typ	A_{CL} V/V min	V_{OS} mV max	Input Bias Current μA max	Voltage Noise nV/√Hz @ 10 kHz	I_{OUT} mA min	Supply Range ±Volts	Supply Current mA typ	Spice Model Avail.	Page	Comments
AD811	2500	0.01	0.01	65–0.01	120	1	3	10	2	100	4.5 to 18	16.5	X	2-41	Best Video Specifications Flatness = 0.1 dB to 35 MHz
AD844	2000	0.025	0.008	100–0.1	60	−1	0.15	0.25	2	20	4.5 to 18	6.5		2-101	Constant 10 ns Rise Time for Any Pulse
OP160	1300	0.04	0.04	75–0.1	90	1	5	20	5.5	35	4 to 15	6.5	X	2-225	Disable Mode for Low Power Applications
OP260	1000	0.067	0.02	250–0.1	90	1	3.5	8	5.5	35	4 to 15	9	X	2-267	Dual OP160; Only Dual Transimpedance
AD5539	600	0.1	0.04	12–1	220	2	3	13	6	15	4.5 to 10	14		2-153	Improved Replacement for Industry Standard
AD846	450	0.03	0.01	110–0.01	80	−1	0.075	0.25	2	20	5 to 18	5	X	2-121	Highest DC Precision High Speed Amplifier
AD840	400	0.04	0.025	100–0.01	40	10	0.3	5	4	50	5 to 18	10.5	X	2-65	Fast Settling Time; Gain > 10
AD842	375	0.035	0.015	100–0.01	40	2	1	5	9	100	5 to 18	13		2-81	High Current Output; Gain > 2
AD841	300	0.02	0.03	110–0.01	40	1	1	5	13	50	5 to 18	11		2-73	Fast Settling Time and Unity Gain Stable
AD847	300	0.2	0.04	120–0.1	50	1	1	5	15	20	4.5 to 18	5.3	X	2-133	General Purpose, Low Power, Unity Gain
AD827	300	0.2	0.04	120–0.1	50	1	2	7	15	20	4.5 to 18	10	X	2-45	Dual AD847
AD829	300	0.04	0.02	90–0.1	50	1	0.5	7	2	20	4.5 to 18	5	X	2-53	Low Noise and High Speed
AD848	300	0.08	0.07	100–0.1	35	5	1	5	5	20	4.5 to 18	5.1	X	2-145	General Purpose, Low Power, Gain > 5
AD849	300	0.04	0.08	80–0.1	30	25	0.75	5	3	20	4.5 to 18	5.1		2-145	General Purpose, Low Power Preamplifier
AD843	250	0.025	0.025	135–0.01	34	1	1	0.001	19	50	4.5 to 18	12		2-89	High Performance, Replaces LH0032
OP64	170	0.018	0.045	100–0.1	16	5	1	1	8	50	5 to 18	6.2	X	2-211	Stable for Gains > 5
AD845	100	0.025	0.04	350–0.01	16	1	0.25	0.001	18	25	4.75 to 18	10		2-113	General Purpose. Unity Gain Stable

Audio Amplifiers

Single Op Amps

Model	Voltage Noise @ 1 kHz nV/√Hz typ	SR V/μs typ	GBW MHz typ	Supply Current mA max	V_{OUT} Volts min	Page	Comments
AD829	2	300	750	6.8	±10, R_L = 500 Ω	2-53	Ideal High Gain, Low Noise Input Device
AD846	2	450	80	6.5	±10, R_L = 500 Ω	2-121	Current Feedback
AD844	2	2000	60	7.5	±10, R_L = 500 Ω	2-101	Low Noise, Highest Slew Rate
OP27	3	2.8	8	4.67	±10, R_L = 600 Ω	2-169	Low Cost, Precision
OP37	3	17	63	4.67	±10, R_L = 600 Ω	2-181	$A_{VCL} \geq 5$, Low Cost
OP61	3.4	40	200	8	±11, R_L = 500 Ω	2-193	$A_{VCL} \geq 10$
SSM2134	3.5	13	10	6.5	±12, R_L = 600 Ω	2-325	Improved 5532
OP160	5.5	1300	90	8	±11, R_L = 500 Ω	2-225	Current Feedback
OP64	8	170	80	8	±10, R_L = 200 Ω	2-211	$A_{VCL} \geq 5$, High Output Current
SSM2131	13	50	10	6.5	±11.5, R_L = 1000 Ω	2-315	Ultralow Distortion
AD711	18	20	4	2.8	+13/−12.5, R_L = 2000 Ω	2-5	Precision BiFET
AD843	19	250	34	13	±10, R_L = 500 Ω	2-89	Low Bias Current, Fast Settling
AD845	25	100	16	12	±12.5, R_L = 500 Ω	2-113	Low Bias Current, Faster Settling

Dual Op Amps

Model	Voltage Noise @ 1 kHz nV/√Hz typ	SR V/μs typ	GBW MHz typ	Supply Current mA/Amp max	V_{OUT} Volts min	Page	Comments
SSM2139	3.6	11	30	3.25	±12, R_L = 2000 Ω	2-331	$A_{VCL} \geq 3$
OP275	5	20	8	2	±13, R_L = 600 Ω	2-297	Ultralow Distortion
OP260	6	1000	90	5.25	±12, R_L = 1000 Ω	2-267	Current Feedback
OP271	7.6	8.5	5	3.25	±12, R_L = 2000 Ω	2-287	Precision
OP249	17	22	4.7	3.5	±12, R_L = 2000 Ω	2-249	Low Power, Low Distortion
AD712	18	20	4	2.8	+13 −12.5, R_L = 2000 Ω	2-17	Low Cost, Dual AD711

Quad Op Amps

Model	Voltage Noise @ 1 kHz nV/√Hz typ	SR V/μs typ	GBW MHz typ	Supply Current mA/Amp max	V_{OUT} Volts min	Page	Comments
OP471	6.5	8	6.5	2.75	±12, R_L = 2000 Ω	2-299	Precision
AD713	18	20	4	3	+13/−12.5, R_L = 2000 Ω	2-29	Quad AD711

ANALOG DEVICES

Precision, Low Cost, High Speed BiFET Op Amp

AD711

FEATURES

Enhanced Replacement for LF411 and TL081
AC PERFORMANCE:
- **Settles to ±0.01% in 1μs**
- **16V/μs min Slew Rate (AD711J)**
- **3MHz min Unity Gain Bandwidth (AD711J)**

DC PERFORMANCE:
- **0.25mV max Offset Voltage: (AD711C)**
- **3μV/°C max Drift: (AD711C)**
- **200V/mV min Open-Loop Gain (AD711K)**
- **4μV p–p max Noise, 0.1Hz to 10Hz (AD711C)**

Available in Plastic Mini-DIP, Plastic SO, Hermetic Cerdip, and Hermetic Metal Can Packages
MIL-STD-883B Parts Available
Available in Tape and Reel in Accordance with EIA-481A Standard
Surface Mount (SOIC)
Dual Version: AD712
Quad Version: AD713

PRODUCT DESCRIPTION

The AD711 is a high speed, precision monolithic operational amplifier offering high performance at very modest prices. Its very low offset voltage and offset voltage drift are the results of advanced laser wafer trimming technology. These performance benefits allow the user to easily upgrade existing designs that use older precision BiFETs and, in many cases, bipolar op amps.

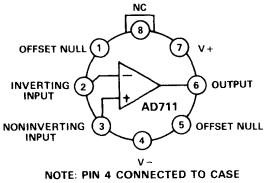
The superior ac and dc performance of this op amp makes it suitable for active filter applications. With a slew rate of 16V/μs and a settling time of 1μs to ±0.01%, the AD711 is ideal as a buffer for 12-bit D/A and A/D Converters and as a high-speed integrator. The settling time is unmatched by any similar IC amplifier.

The combination of excellent noise performance and low input current also make the AD711 useful for photo diode preamps. Common-mode rejection of 88dB and open loop gain of 400V/mV ensure 12-bit performance even in high-speed unity gain buffer circuits.

The AD711 is pinned out in a standard op amp configuration and is available in seven performance grades. The AD711J and AD711K are rated over the commercial temperature range of 0 to +70°C. The AD711A, AD711B and AD711C are rated over the industrial temperature range of −40°C to +85°C. The AD711S and AD711T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

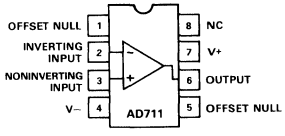
CONNECTION DIAGRAMS

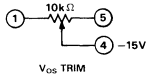
TO-99 (H) Package



NOTE: PIN 4 CONNECTED TO CASE
NC = NO CONNECT

Plastic Mini-DIP (N) Package
Plastic Small Outline (R) and Cerdip (Q) Package





Extended reliability PLUS screening is available, specified over the commercial and industrial temperature ranges. PLUS screening includes 168-hour burn-in, as well as other environmental and physical tests.

The AD711 is available in an 8-pin plastic mini-DIP, small outline, cerdip, TO-99 metal can or in chip form.

PRODUCT HIGHLIGHTS

1. The AD711 offers excellent overall performance at very competitive prices.
2. Analog Devices' advanced processing technology and with 100% testing guarantees a low input offset voltage (0.25mV max, C grade, 2mV max, J grade). Input offset voltage is specified in the warmed-up condition. Analog Devices' laser wafer drift trimming process reduces input offset voltage drifts to 3μV/°C max on the AD711C.
3. Along with precision dc performance, the AD711 offers excellent dynamic response. It settles to ±0.01% in 1μs and has a 100% tested minimum slew rate of 16V/μs. Thus this device is ideal for applications such as DAC and ADC buffers which require a combination of superior ac and dc performance.
4. The AD711 has a guaranteed and tested maximum voltage noise of 4μV p-p, 0.1 to 10Hz (AD711C).
5. Analog Devices' well-matched, ion-implanted JFETs ensure a guaranteed input bias current (at either input) of 25pA max (AD711C) and an input offset current of 10pA max (AD711C). Both input bias current and input offset current are guaranteed in the warmed-up condition.

AD711—SPECIFICATIONS (@ +25°C and V_S = ±15V dc, unless otherwise noted)

Model	AD711J/A/S Min	AD711J/A/S Typ	AD711J/A/S Max	AD711K/B/T Min	AD711K/B/T Typ	AD711K/B/T Max	AD711C Min	AD711C Typ	AD711C Max	Units
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0.3	**2/1/1**		0.2	**0.5**		0.1	**0.25**	mV
T_{min} to T_{max}			3/2/2			**1.0**			**0.45**	mV
vs. Temp.		7	20/20/**20**		5	**10**		2	**3**	μV/°C
vs. Supply	**76**	95		**80**	100		**86**	110		dB
vs. Supply, T_{min} to T_{max}	76/76/**76**			**80**			**86**			dB
Long Term Offset Stability		15			15			15		μV/month
INPUT BIAS CURRENT[2]										
Either Input, V_{CM} = 0		15	**50**		15	**50**		15	**25**	pA
Either Input at T_{max},			1.1/3.2/51			1.1/3.2/51			1.6	nA
V_{CM} = 0 (70°C/85°C/125°C)										
Either Input, V_{CM} = +10V		20	**100**		20	**100**		20	**50**	pA
Offset Current, V_{CM} = 0		10	**25**		5	**25**		5	**10**	pA
Offset Current at T_{max}										
(70°C/85°C/125°C)			0.57/1.6/26			0.57/1.6/26			0.65	nA
FREQUENCY RESPONSE										
Unity Gain, Small Signal	3.0	4		3.4	4		3.4	4		MHz
Full Power Response		200			200			200		kHz
Slew Rate, Unity Gain	**16**	20		**18**	20		**18**	20		V/μs
Settling Time to 0.01%[3]		1	1.2		1	1.2		1	1.2	μs
Total Harmonic Distortion										
f = 1kHz										
$R_L \geq 2k\Omega$, V_O = 3V RMS		0.0003			0.0003			0.0003		%
INPUT IMPEDANCE										
Differential		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω‖pF
Common-Mode		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω‖pF
INPUT VOLTAGE RANGE										
Differential[4]		±20			±20			±20		V
Common-Mode Voltage		+14.5, −11.5			+14.5, −11.5			+14.5, −11.5		
Over Max Operating Range[5]	$-V_S+4V$		$+V_S-2V$	$-V_S+4V$		$+V_S-2V$	$-V_S+4V$		$+V_S-2V$	V
Common-Mode Rejection Ratio										
V_{CM} = ±10V	**76**	88		**80**	88		**86**	94		dB
T_{min} to T_{max}	76/76/**76**	84		**80**	84		**86**	90		dB
V_{CM} = ±11V	**70**	84		**76**	84		**76**	90		dB
T_{min} to T_{max}	70/70/**70**	80		**74**	80		**74**	84		dB
INPUT VOLTAGE NOISE										
Voltage 0.1Hz to 10Hz		2			2			2	**4.0**	μV_{p-p}
f = 10Hz		45			45			45		$nV/\sqrt{Hz}$
f = 100Hz		22			22			22		$nV/\sqrt{Hz}$
f = 1kHz		18			18			18		$nV/\sqrt{Hz}$
f = 10kHz		16			16			16		$nV/\sqrt{Hz}$
INPUT CURRENT NOISE										
f = 1kHz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
OPEN LOOP GAIN[6]										
V_O = ±10V, $R_L \geq 2k\Omega$	**150**	400		**200**	400		**200**	400		V/mV
V_O = ±10V, $R_L \geq 2k\Omega$,										
T_{min} to T_{max}	100/100/**100**			**100**			**100**			V/mV
OUTPUT CHARACTERISTICS										
Voltage @ $R_L \geq 2k\Omega$	**+13, −12.5**	+13.9, −13.3		**+13, −12.5**	+13.9, −13.3		**+13, −12.5**	+13.9, −13.3		V
Voltage @ $R_L \geq 2k\Omega$,										
T_{min} to T_{max}	±12/±12/**±12**	+13.8, −13.1		**±12**	+13.8, −13.1		**±12**	+13.8, −13.1		V
Short-Circuit Current		25			25			25		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current		2.5	**3.4**		2.5	**3.0**		2.5	**2.8**	mA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0 to +70°C)		AD711J			AD711K					
Industrial (−40°C to +85°C)		AD711A			AD711B			AD711C		
Military (−55°C to +125°C)		AD711S			AD711T					
PACKAGE OPTIONS[7]										
Plastic (N-8)		AD711JN			AD711KN					
SOIC (R-8)		AD711JR			AD711KR					
Cerdip (Q-8)		AD711AQ, AD711SQ			AD711BQ, AD711TQ			AD711CQ		
TO-99 (H-08A)		AD711AH, AD711SH			AD711BH, AD711TH			AD711CH		
Tape and Reel		AD711JR-REEL			AD711KR-REEL					
J, K and S Chips Available										
TRANSISTOR COUNT		30			30			30		

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25°C$.
[2]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A = +25°C$. For higher temperature, the current doubles every 10°C.
[3]Refer to Figure 29.
[4]Defined as voltage between inputs, such that neither exceeds ±10V from ground.
[5]Typically exceeding −14.1V negative common-mode voltage on either input results in an output phase reversal.
[6]Open-Loop Gain is specified with V_{OS} both nulled and unnulled.
[7]H = Metal Can; N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

Specifications subject to change without notice.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

2

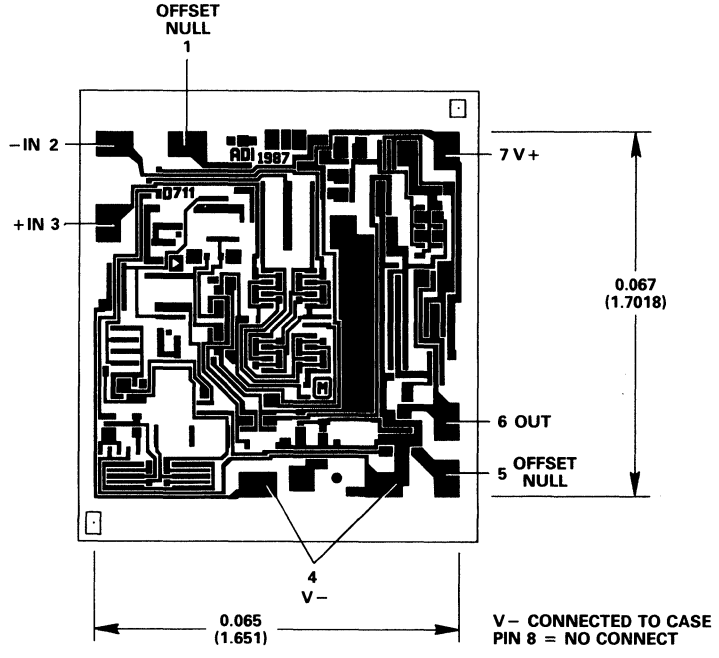
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18V
Internal Power Dissipation[2]	500mW
Input Voltage[3]	±18V
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range Q, H	−65°C to +150°C
Storage Temperature Range N	−65°C to +125°C
Operating Temperature Range	
AD711J/K	0 to +70°C
AD711A/B/C	−40°C to +85°C
AD711S/T	−55°C to +125°C
Lead Temperature Range (Soldering 60 seconds)	300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal Characteristics
8-Pin Plastic Package: $\theta_{JC} = 33°C/W$, $\theta_{JA} = 100°C/W$
8-Pin Cerdip Package: $\theta_{JC} = 22°C/W$, $\theta_{JA} = 110°C/W$
8-Pin Metal Can Package: $\theta_{JC} = 65°C/W$, $\theta_{JA} = 150°C/W$
[3]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

METALLIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



AD711—Typical Characteristics

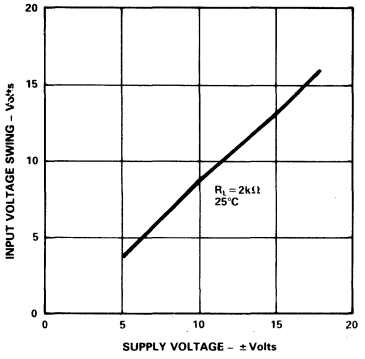


Figure 1. Input Voltage Swing vs. Supply Voltage

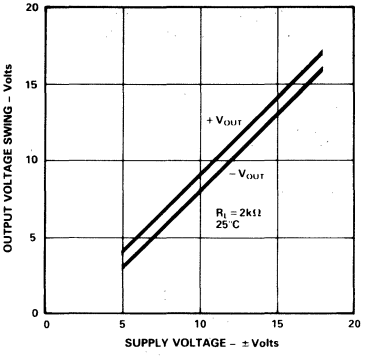


Figure 2. Output Voltage Swing vs. Supply Voltage

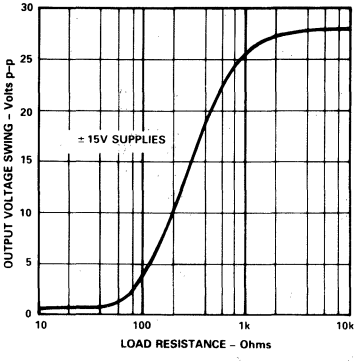


Figure 3. Output Voltage Swing vs. Load Resistance

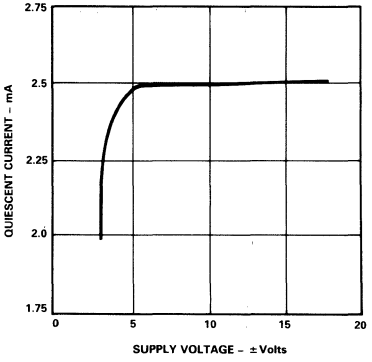


Figure 4. Quiescent Current vs. Supply Voltage

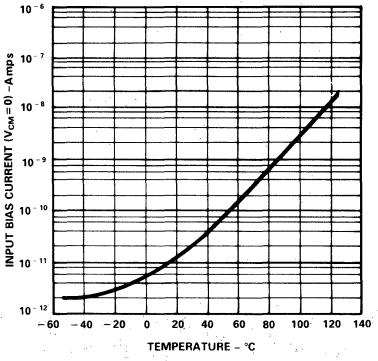


Figure 5. Input Bias Current vs. Temperature

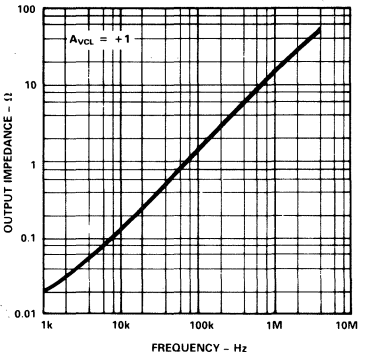


Figure 6. Output Impedance vs. Frequency

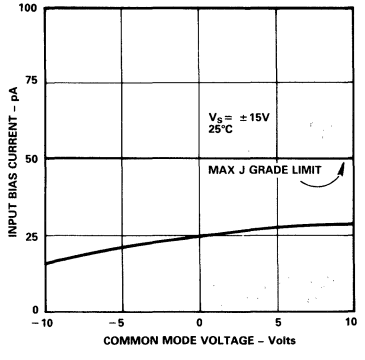


Figure 7. Input Bias Current vs. Common Mode Voltage

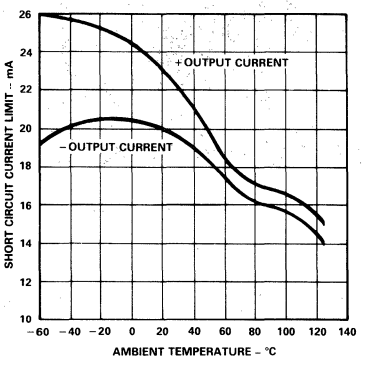


Figure 8. Short Circuit Current Limit vs. Temperature

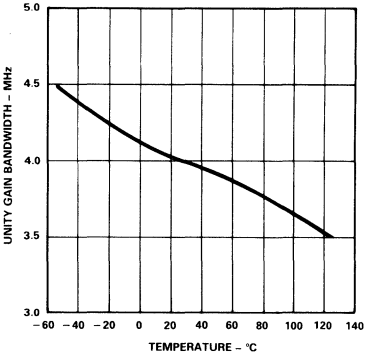


Figure 9. Unity Gain Bandwidth vs. Temperature

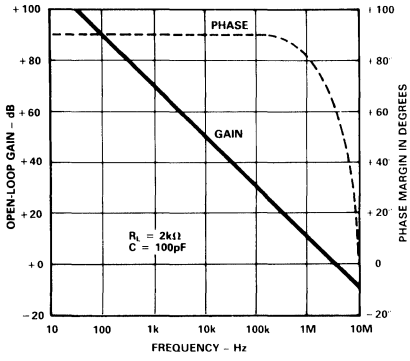


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

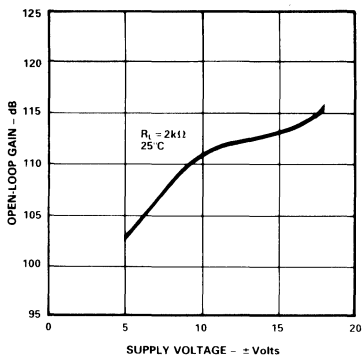


Figure 11. Open-Loop Gain vs. Supply Voltage

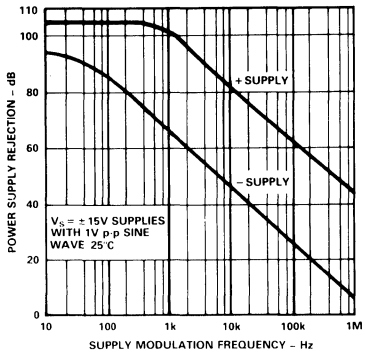


Figure 12. Power Supply Rejection vs. Frequency

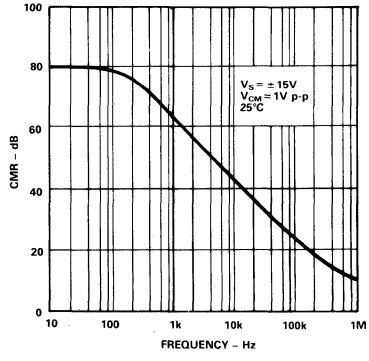


Figure 13. Common Mode Rejection vs. Frequency

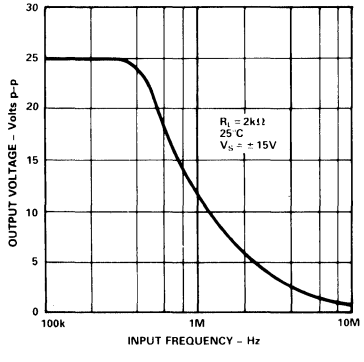


Figure 14. Large Signal Frequency Response

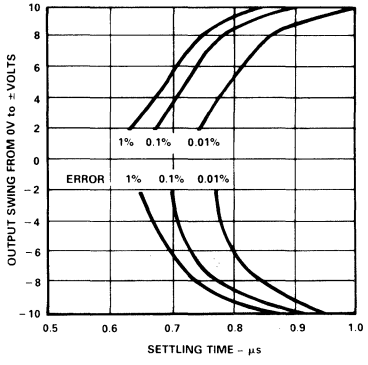


Figure 15. Output Swing and Error vs. Settling Time

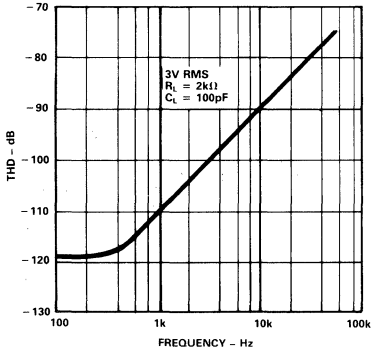


Figure 16. Total Harmonic Distortion vs. Frequency

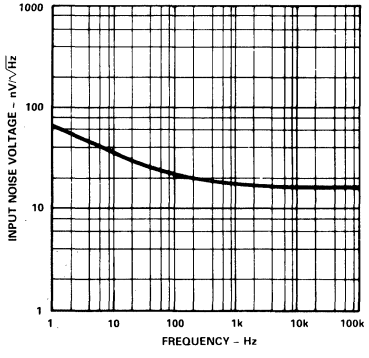


Figure 17. Input Noise Voltage Spectral Density

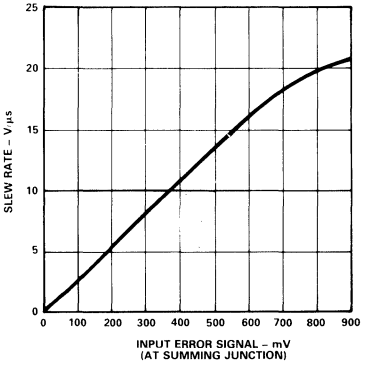


Figure 18. Slew Rate vs. Input Error Signal

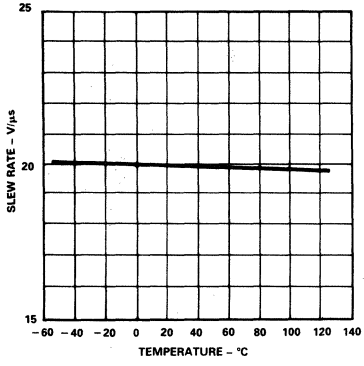


Figure 19. Slew Rate vs. Temperature

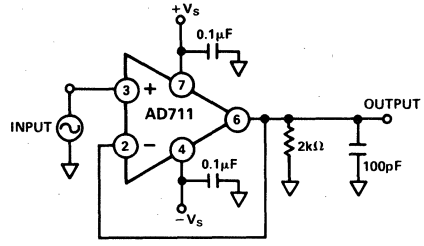


Figure 20. T.H.D. Test Circuit

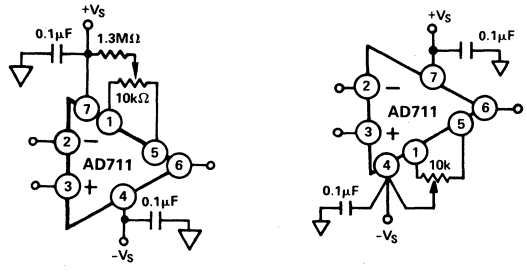


Figure 21. Offset Null Configurations

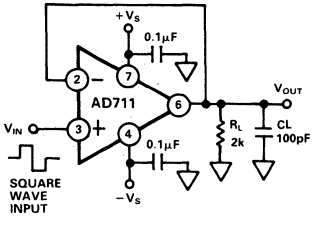


Figure 22a. Unity Gain Follower

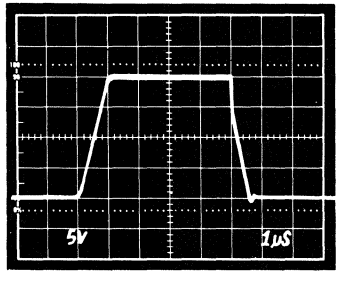


Figure 22b. Unity Gain Follower Pulse Response (Large Signal)

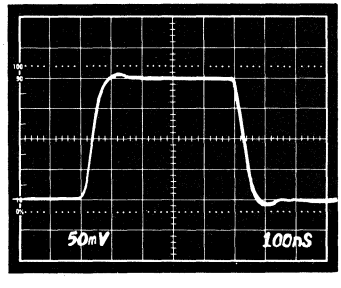


Figure 22c. Unity Gain Follower Pulse Response (Small Signal)

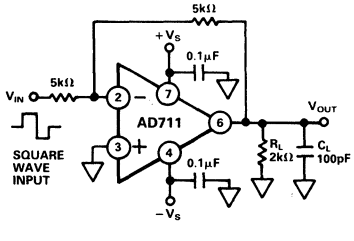


Figure 23a. Unity Gain Inverter

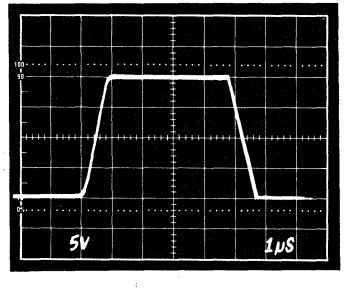


Figure 23b. Unity Gain Inverter Pulse Response (Large Signal)

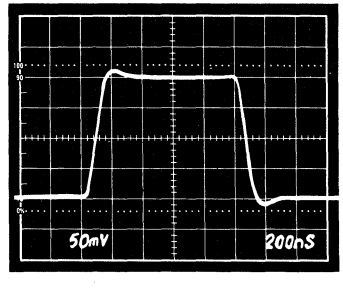


Figure 23c. Unity Gain Inverter Pulse Response (Small Signal)

OPTIMIZING SETTLING TIME

Most bipolar high-speed D/A converters have curent outputs; therefore, for most applications, an external op amp is required for current-to-voltage conversion. The settling time of the converter/op amp combination depends on the settling time of the DAC and output amplifier. A good approximation is:

$$t_s \text{ Total} = \sqrt{(t_s \text{ DAC})^2 + (t_s \text{ AMP})^2}$$

The settling time of an op amp DAC buffer will vary with the noise gain of the circuit, the DAC output capacitance, and with the amount of external compensation capacitance across the DAC output scaling resistor.

Settling time for a bipolar DAC is typically 100 to 500ns. Previously, conventional op amps have required much longer settling times than have typical state-of-the-art DACs; therefore, the amplifier settling time has been the major limitation to a high-speed voltage-output D-to-A function. The introduction of the AD711/712 family of op amps with their 1μs (to ±0.01% of final value) settling time now permits the full high-speed capabilities of most modern DACs to be realized.

In addition to a significant improvement in settling time, the low offset voltage, low offset voltage drift, and high open-loop gain of the AD711 family assures 12-bit accuracy over the full operating temperature range.

The excellent high-speed performance of the AD711 is shown in the oscilloscope photos of Figure 25. Measurements were taken using a low input capacitance amplifier connected directly to the summing junction of the AD711 – both photos show the worst case situation: a full-scale input transition. The DAC's 4kΩ [10kΩ‖8kΩ = 4.4kΩ] output impedance together with a 10kΩ feedback resistor produce an op amp noise gain of 3.25. The current output from the DAC produces a 10V step at the op amp output (0 to −10V Figure 25a, −10V to 0V Figure 25b.)

Therefore, with an ideal op amp, settling to ±1/2LSB (±0.01%) requires that 375μV or less appears at the summing junction. This means that the error between the input and output (that voltage which appears at the AD711 summing junction) must be less than 375μV. As shown in Figure 25, the total settling time for the AD711/AD565 combination is 1.2 microseconds.

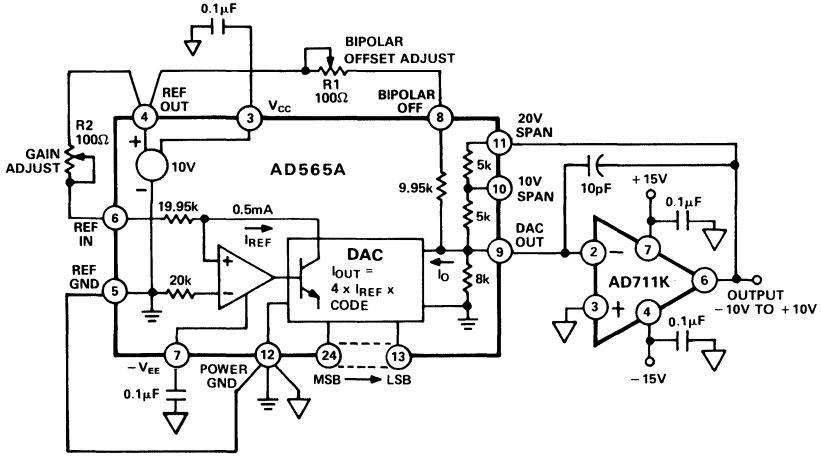
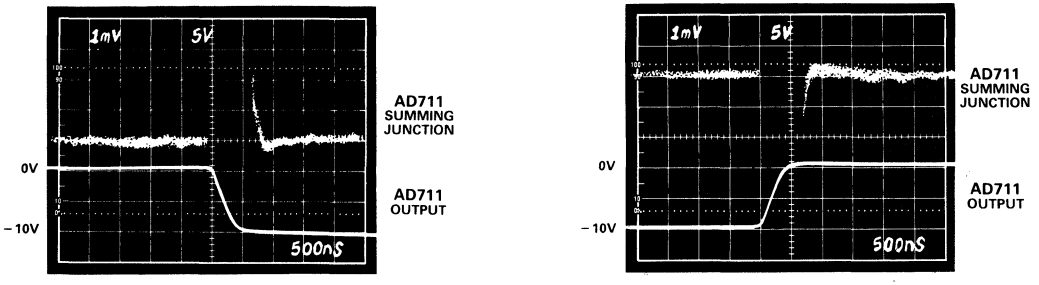


Figure 24. ±10V Voltage Output Bipolar DAC



a. (Full-Scale Negative Transition)

b. (Full-Scale Positive Transition)

Figure 25. Settling Characteristics for AD711 with AD565A

OP AMP SETTLING TIME – A MATHEMATICAL MODEL

The design of the AD711 gives careful attention to optimizing individual circuit components; in addition, a careful tradeoff was made: the gain bandwidth product (4MHz) and slew rate (20V/μs) were chosen to be high enough to provide very fast settling time but not too high to cause a significant reduction in phase margin (and therefore stability). Thus designed, the AD711 settles to ±0.01%, with a 10V output step, in under 1μs, while retaining the ability to drive a 250pF load capacitance when operating as a unity gain follower.

If an op amp is modeled as an ideal integrator with a unity gain crossover frequency of $\omega_O/2\pi$, Equation 1 will accurately describe the small signal behavior of the circuit of Figure 26a, consisting of an op amp connected as an I-to-V converter at the output of a bipolar or CMOS DAC. This equation would completely describe the output of the system if not for the op amp's finite slew rate and other nonlinear effects.

Equation 1.

$$\frac{V_O}{I_{IN}} = \frac{-R}{\frac{R(C_f + C_X)}{\omega_o} s^2 + \left(\frac{G_N}{\omega_o} + RC_f\right) s + 1}$$

where $\frac{\omega_o}{2\pi}$ = op amp's unity gain frequency

G_N = "noise" gain of circuit $\left(1 + \frac{R}{R_O}\right)$

This equation may then be solved for C_f:

Equation 2.

$$C_f = \frac{2 - G_N}{R\omega_o} + \frac{2\sqrt{RC_X\omega_o + (1-G_N)}}{R\omega_o}$$

In these equations, capacitor C_X is the total capacitance appearing at the inverting terminal of the op amp. When modeling a DAC buffer application, the Norton equivalent circuit of Figure 26a can be used directly; capacitance C_X is the total capacitance of the output of the DAC plus the input capacitance of the op amp (since the two are in parallel).

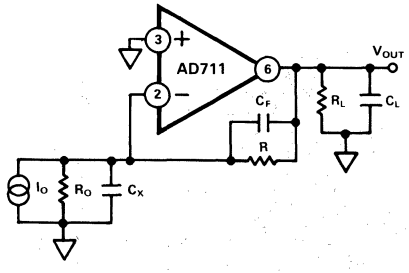


Figure 26a. Simplified Model of the AD711 Used as a Current-Out DAC Buffer

When R_O and I_O are replaced with their Thevenin V_{IN} and R_{IN} equivalents, the general purpose inverting amplifier of Figure 26b is created. Note that when using this general model, capacitance C_X is EITHER the input capacitance of the op amp if a simple inverting op amp is being simulated OR it is the combined capacitance of the DAC output and the op amp input if the DAC buffer is being modeled.

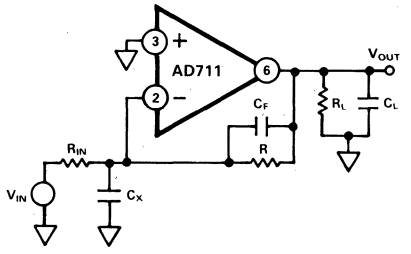


Figure 26b. Simplified Model of the AD711 Used as an Inverter

In either case, the capacitance C_X causes the system to go from a one-pole to a two-pole response; this additional pole increases settling time by introducing peaking or ringing in the op amp output. Since the value of C_X can be estimated with reasonable accuracy, Equation 2 can be used to choose a small capacitor, C_F, to cancel the input pole and optimize amplifier response. Figure 27 is a graphical solution of Equation 2 for the AD711 with R = 4kΩ.

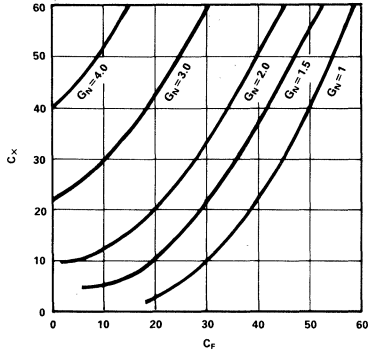


Figure 27. Value of Capacitor C_F vs. Value of C_X

The photos of Figures 28a and 28b show the dynamic response of the AD711 in the settling test circuit of Figure 29.

The input of the settling time fixture is driven by a flat-top pulse generator. The error signal output from the false summing node of A1 is clamped, amplified by A2 and then clamped again. The error signal is thus clamped twice: once to prevent overloading amplifier A2 and then a second time to avoid overloading the oscilloscope preamp. The Tektronix oscilloscope preamp type 7A26 was carefully chosen because it does not overload with these input levels. Amplifier A2 needs to be a very high speed FET-input op amp; it provides a gain of 10, amplifying the error signal output of A1.

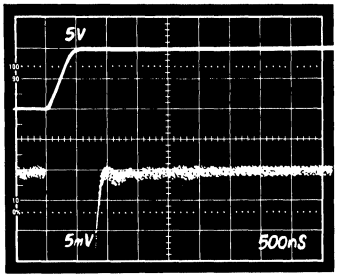


Figure 28a. Settling Characteristics 0 to +10V Step
Upper Trace: Output of AD711 Under Test (5V/Div)
Lower Trace: Amplified Error Voltage (0.01%/Div)

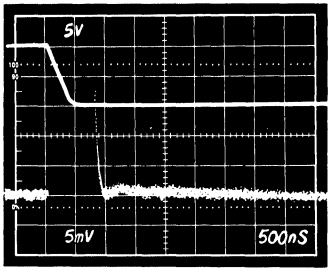


Figure 28b. Settling Characteristics 0 to −10V Step
Upper Trace: Output of AD711 Under Test (5V/Div)
Lower Trace: Amplified Error Voltage (0.01%/Div)

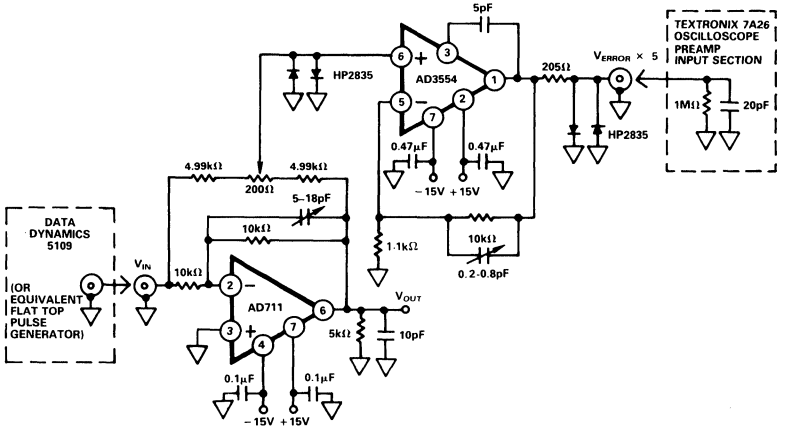
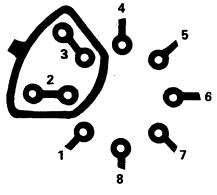


Figure 29. Settling Time Test Circuit

GUARDING

The low input bias current (15pA) and low noise characteristics of the AD711 BiFET op amp make it suitable for electrometer applications such as photo diode preamplifiers and picoampere current-to-voltage converters. The use of a guarding technique such as that shown in Figure 30, in printed circuit board layout and construction is critical to minimize leakage currents. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on the printed circuit board.

TO-99 (H) Package



Plastic DIP (N) Package and Cerdip (Q) Package

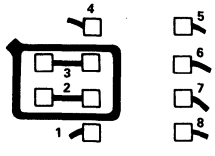


Figure 30. Board Layout for Guarding Inputs

D/A CONVERTER APPLICATIONS

The AD711 is an excellent output amplifier for CMOS DACs. It can be used to perform both 2 quadrant and 4 quadrant operation. The output impedance of a DAC using an inverted R-2R ladder approaches R for codes containing many 1s, 3R for codes containing a single 1, and for codes containing all zero, the output impedance is infinite.

For example, the output resistance of the AD7545 will modulate between 11kΩ and 33kΩ. Therefore, with the DAC's internal feedback resistance of 11kΩ, the noise gain will vary from 2 to 4/3. This changing noise gain modulates the effect of the input offset voltage of the amplifier, resulting in nonlinear DAC-amplifier performance.

The AD711K with guaranteed 500μV offset voltage minimizes this effect to achieve 12-bit performance.

Figures 31 and 32 show the AD711 and AD7545 (12-bit CMOS DAC) configured for unipolar binary (2-quadrant multiplication) or bipolar (4-quadrant multiplication) operation. Capacitor C1 provides phase compensation to reduce overshoot and ringing.

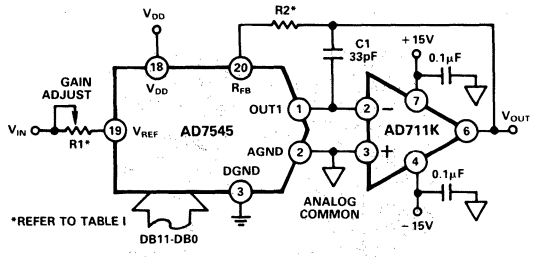


Figure 31. Unipolar Binary Operation

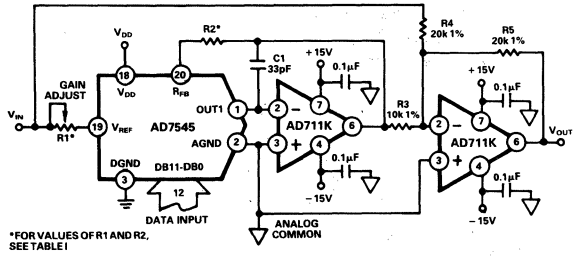


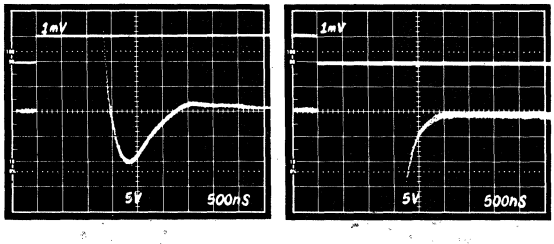
Figure 32. Bipolar Operation

R1 and R2 calibrate the zero offset and gain error of the DAC. Specific values for these resistors depend upon the grade of AD7545 and are shown below.

TRIM RESISTOR	JN/AQ/SD	KN/BQ/TD	LN/CQ/UD	GLN/GCQ/GUD
R1	500Ω	200Ω	100Ω	20Ω
R2	150Ω	68Ω	33Ω	6.8Ω

Table I. Recommended Trim Resistor Values vs. Grades of the AD7545 for V_{DD} = +5V

Figures 33a and 33b show the settling time characteristics of the AD711 when used as a DAC output buffer for the AD7545.



a. Full-Scale Positive Transition

b. Full-Scale Negative Transition

Figure 33. Settling Characteristics for AD711 with AD7545

NOISE CHARACTERISTICS

The random nature of noise, particularly in the 1/f region, makes it difficult to specify in practical terms. At the same time, designers of precision instrumentation require certain guaranteed maximum noise levels to realize the full accuracy of their equipment.

The AD711C grade is specified at a maximum level of 4.0μV p-p, in a 0.1 to 10Hz bandwidth. Each AD711C receives a 100% noise test for two 10-second intervals; devices with any excursion in excess of 4.0μV are rejected. The screened lot is then submitted to Quality Control for verification on an AQL basis.

All other grades of the AD711 are sample-tested on an AQL basis to a limit of 6μV p-p, 0.1 to 10Hz.

DRIVING THE ANALOG INPUT OF AN A/D CONVERTER

An op amp driving the analog input of an A/D converter, such as that shown in Figure 34, must be capable of maintaining a constant output voltage under dynamically changing load conditions. In successive-approximation converters, the input current is compared to a series of switched trial currents. The comparison point is diode clamped but may deviate several hundred millivolts resulting in high frequency modulation of A/D input current. The output impedance of a feedback amplifier is made artificially low by the loop gain. At high frequencies, where the loop gain is low, the amplifier output impedance can approach its open loop value. Most IC amplifiers exhibit a minimum open loop output impedance of 25Ω due to current limiting resistors. A few hundred microamps reflected from the change in converter

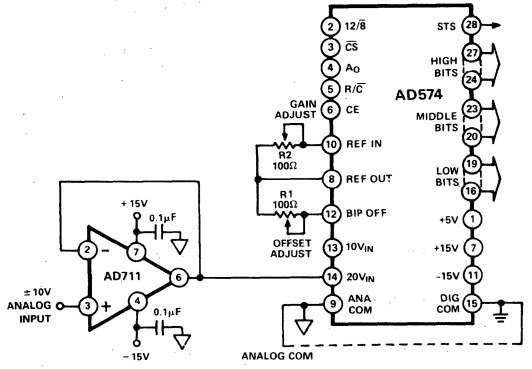
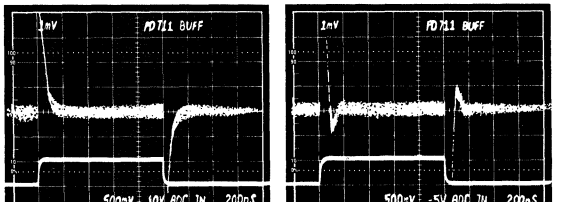


Figure 34. AD711 as ADC Unity Gain Buffer



a. Source Current = 2mA

b. Sink Current = 1mA

Figure 35. ADC Input Unity Gain Buffer Recovery Times

loading can introduce errors in instantaneous input voltage. If the A/D conversion speed is not excessive and the bandwidth of the amplifier is sufficient, the amplifier's output will return to the nominal value before the converter makes its comparison. However, many amplifiers have relatively narrow bandwidth yielding slow recovery from output transients. The AD711 is ideally suited to drive high speed A/D converters since it offers both wide bandwidth and high open-loop gain.

DRIVING A LARGE CAPACITIVE LOAD

The circuit in Figure 36 employs a 100Ω isolation resistor which enables the amplifier to drive capacitive loads exceeding 1500pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 100Ω series resistor and the load capacitance, C_L. Figure 37 shows a typical transient response for this connection.

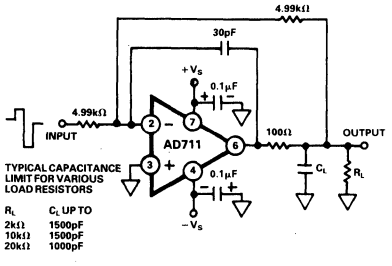


Figure 36. Circuit for Driving a Large Capacitive Load

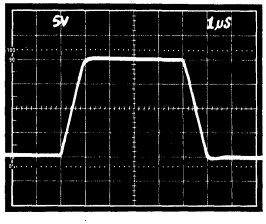


Figure 37. Transient Response R_L = 2kΩ, C_L =500pF

ACTIVE FILTER APPLICATIONS

In active filter applications using op amps, the dc accuracy of the amplifier is critical to optimal filter performance. The amplifier's offset voltage and bias current contribute to output error. Offset voltage will be passed by the filter and may be amplified to produce excessive output offset. For low frequency applications requiring large value input resistors, bias currents flowing through these resistors will also generate an offset voltage.

In addition, at higher frequencies, an op amp's dynamics must be carefully considered. Here, slew rate, bandwidth, and open-loop gain play a major role in op amp selection. The slew rate must be fast as well as symmetrical to minimize distortion. The amplifier's bandwidth in conjunction with the filter's gain will dictate the frequency response of the filter.

The use of a high performance amplifier such as the AD711 will minimize both dc and ac errors in all active filter applications.

SECOND ORDER LOW PASS FILTER

Figure 38 depicts the AD711 configured as a second order Butterworth low pass filter. With the values as shown, the corner frequency will be 20kHz; however, the wide bandwidth of the AD711 permits a corner frequency as high as several hundred kilohertz. Equations for component selection are shown below.

$$R1 = R2 = \text{user selected (typical values: } 10k\Omega - 100k\Omega)$$

$$C1 = \frac{1.414}{(2\pi)\,(f_{cutoff})\,(R1)}, \quad C2 = \frac{0.707}{(2\pi)\,(f_{cutoff})\,(R1)}$$

Where C1 and C2 are in farads.

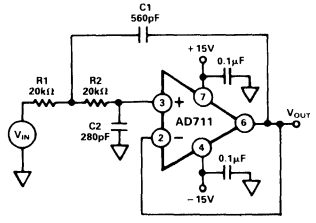


Figure 38. Second Order Low Pass Filter

An important property of filters is their out-of-band rejection. The simple 20kHz low pass filter shown in Figure 38, might be used to condition a signal contaminated with clock pulses or sampling glitches which have considerable energy content at high frequencies.

The low output impedance and high bandwidth of the AD711 minimize high frequency feedthrough as shown in Figure 39.

The upper trace is that of another low cost BiFET op amp showing 17dB more feedthrough at 5MHz.

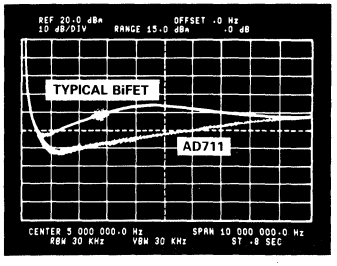


Figure 39.

9 POLE CHEBYCHEV FILTER

Figure 40 shows the AD711 and its dual counterpart, the AD712, as a 9 pole Chebychev filter using active frequency dependent negative resistors (FDNR). With a cutoff frequency of 50kHz and better than 90dB rejection, it may be used as an anti-aliasing filter for a 12-bit Data Acquisition System with 100kHz throughput.

As shown in Figure 40, the filter is comprised of four FDNRs (A, B, C, D) having values of 4.9395×10^{-15} and 5.9276×10^{-15} farad-seconds. Each FDNR active network provides a two-pole response; for a total of 8 poles. The 9th pole consists of a 0.001μF capacitor and a 124kΩ resistor at Pin 3 of amplifier A2. Figure 41 depicts the circuits for each FDNR with the proper selection of R. To achieve optimal performance, the 0.001μF capacitors must be selected for 1% or better matching and all resistors should have 1% or better tolerance.

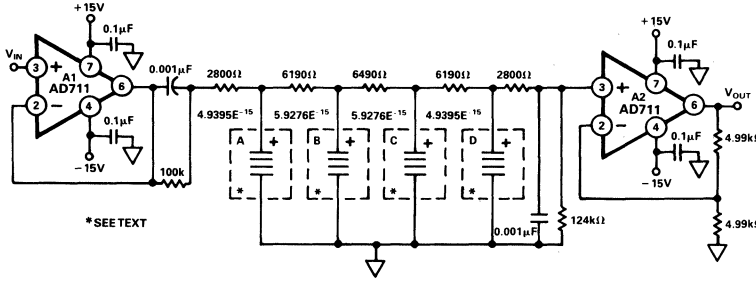


Figure 40. 9 Pole Chebychev Filter

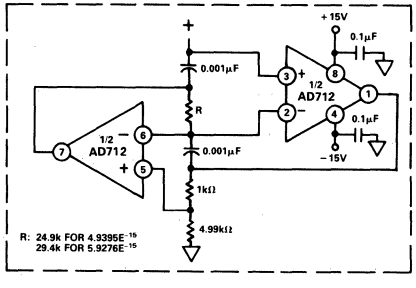


Figure 41. FDNR for 9 Pole Chebychev Filter

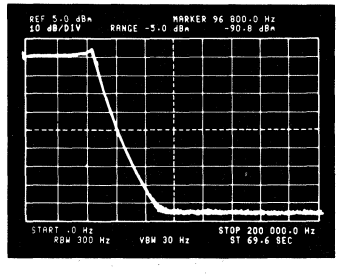


Figure 42. High Frequency Response for 9 Pole Chebychev Filter

ANALOG DEVICES

Dual Precision, Low Cost, High Speed, BiFET Op Amp

AD712

FEATURES

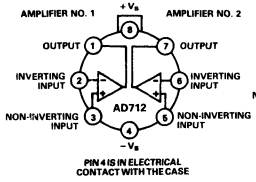
Enhanced Replacement for LF412 and TL082
AC PERFORMANCE:
- **Settles to ±0.01% in 1μs**
- **16V/μs min Slew Rate (AD712J)**
- **3MHz min Unity Gain Bandwidth (AD712J)**

DC PERFORMANCE:
- **0.30mV max Offset Voltage: (AD712C)**
- **5μV/°C max Drift: (AD712C)**
- **200V/mV min Open Loop Gain (AD712K)**
- **4μV p–p max Noise, 0.1Hz to 10Hz (AD712C)**

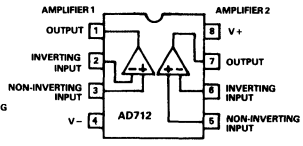
Surface Mount Available in Tape and Reel in Accordance with EIA-481A Standard
MIL-STD-883B Parts Available
Single Version Available: AD711
Quad Version: AD713
Available in Plastic Mini-DIP, Plastic SOIC, Hermetic Cerdip, Hermetic Metal Can Packages and Chip Form

FUNCTIONAL BLOCK DIAGRAMS

TO-99 (H) Package



Plastic Mini-DIP (N) Package, Cerdip (Q) Package and SOIC (R) Package



PRODUCT DESCRIPTION

The AD712 is a high speed, precision monolithic operational amplifier offering high performance at very modest prices. Its very low offset voltage and offset voltage drift are results of advanced laser wafer trimming technology. These performance benefits allow the user to easily upgrade existing designs that use older precision BiFETs and, in many cases, bipolar op amps.

The superior ac and dc performance of this op amp makes it suitable for active filter applications. With a slew rate of 16V/μs and a settling time of 1μs to ±0.01%, the AD712 is ideal as a buffer for 12-bit D/A and A/D Converters and as a high-speed integrator. The settling time is unmatched by any similar IC amplifier.

The combination of excellent noise performance and low input current also make the AD712 useful for photo diode preamps. Common-mode rejection of 88dB and open loop gain of 400V/mV ensure 12-bit performance even in high-speed unity gain buffer circuits.

The AD712 is pinned out in a standard op amp configuration and is available in seven performance grades. The AD712J and AD712K are rated over the commercial temperature range of 0 to +70°C. The AD712A, AD712B and AD712C are rated over the industrial temperature range of −40°C to +85°C. The AD712S and AD712T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available, specified over the commercial and industrial temperature ranges. PLUS screening includes 168-hour burn-in, as well as other environmental and physical tests.

The AD712 is available in an 8-pin plastic mini-DIP, cerdip, TO-99 metal can, or chip form.

PRODUCT HIGHLIGHTS

1. The AD712 offers excellent overall performance at very competitive prices.
2. Analog Devices' advanced processing technology and with 100% testing guarantees a low input offset voltage (0.3mV max, C grade, 3mV max, J grade). Input offset voltage is specified in the warmed-up condition. Analog Devices' laser wafer drift trimming process reduces input offset voltage drifts to 5μV/°C max on the AD712C.
3. Along with precision dc performance, the AD712 offers excellent dynamic response. It settles to ±0.01% in 1μs and has a 100% tested minimum slew rate of 16V/μs. Thus this device is ideal for applications such as DAC and ADC buffers which require a combination of superior ac and dc performance.
4. The AD712 has a guaranteed and tested maximum voltage noise of 4μV p–p, 0.1 to 10Hz (AD712C).
5. Analog Devices' well-matched, ion-implanted JFETs ensure a guaranteed input bias current (at either input) of 50pA max (AD712C) and an input offset current of 10pA max (AD712C). Both input bias current and input offset current are guaranteed in the warmed-up condition.

AD712—SPECIFICATIONS (@ +25°C and V_S = ±15V dc, unless otherwise noted)

Model	AD712J/A/S			AD712K/B/T			AD712C			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0.3	**3/1/1**		0.2	**1/0.7/0.7**		0.1	**0.30**	mV
T_{min} to T_{max}			**4/2/2**			**2/1.5/1.5**			**0.60**	mV
vs. Temp.		7	**20/20/20**		7	**10**		3	**5**	µV/°C
vs. Supply	**76**	95		**80**	100		**86**	110		dB
vs. Supply, T_{min} to T_{max}	76/76/**76**			**80**			**86**			dB
Long-Term Offset Stability		15			15			15		µV/month
INPUT BIAS CURRENT[2]										
Either Input, V_{CM} = 0		25	**75**		20	**75**		20	**50**	pA
Either Input at T_{max},										
V_{CM} = 0 (70°C/85°C/125°C)		0.6/1.6/26	1.7/4.8/**77**		0.5/1.3/20	1.7/4.8/**77**		1.3	3.2	nA
Either Input, V_{CM} = +10V			**100**			**100**			**75**	pA
Offset Current, V_{CM} = 0		10	**25**		5	**25**		5	**10**	pA
Offset Current at T_{max}										
(70°C/85°C/125°C)		0.3/0.7/11	0.6/1.6/**26**		0.1/0.3/5	0.6/1.6/**26**		0.3	0.7	nA
MATCHING CHARACTERISTICS[3]										
Input Offset Voltage			**3/1/1**			**1/0.7/0.7**			**0.3**	mV
Input Offset Voltage T_{min} to T_{max}			4/2/2			**2/1.5/1.5**			**0.6**	mV
Input Offset Voltage vs. Temp			**20/20/20**			**10**			5	µV/°C
Input Bias Current			**25**			**25**			**10**	pA
Crosstalk[4] @ 1kHz		120			120			120		dB
@ 100kHz		90			90			90		dB
FREQUENCY RESPONSE										
Unity Gain, Small Signal	3.0	4		3.4	4		3.4	4		MHz
Full Power Response		200			200			200		kHz
Slew Rate, Unity Gain	**16**	20		**18**	20		**18**	20		V/µs
Settling Time to 0.01%[5]		1	1.2		1	1.2		1	1.2	µs
Total Harmonic Distortion										
f = 1kHz, $R_L \geq 2k\Omega$, V_O = 3V rms		0.0003			0.0003			0.0003		%
INPUT IMPEDANCE										
Differential		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω‖pF
Common Mode		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω‖pF
INPUT VOLTAGE RANGE										
Differential[6]		±20			±20			±20		V
Common-Mode Voltage										
Over Max Operating Range[7]	$-V_S+4V$	+14.5, −11.5	$+V_S-2V$	$-V_S+4V$	+14.5, −11.5	$+V_S-2V$	$-V_S+4V$	+14.5, −11.5	$+V_S-2V$	V
Common-Mode Rejection Ratio										
V_{CM} = ±10V	**76**	88		**80**	88		**86**	94		dB
T_{min} to T_{max}	76/76/**76**	84		**80**	84		**86**	90		dB
V_{CM} = ±11V	**70**	84		**76**	84		**76**	90		dB
T_{min} to T_{max}	70/70/**70**	80		**74**	80		**74**	84		dB
INPUT VOLTAGE NOISE										
Voltage 0.1Hz to 10Hz		2			2			2	**4**	µV p-p
f = 10Hz		45			45			45		nV/√Hz
f = 100Hz		22			22			22		nV/√Hz
f = 1kHz		18			18			18		nV/√Hz
f = 10kHz		16			16			16		nV/√Hz
INPUT CURRENT NOISE										
f = 1kHz		0.01			0.01			0.01		pA/√Hz
OPEN LOOP GAIN										
V_O = ±10V, $R_L \geq 2k\Omega$	**150**	400		**200**	400		**200**	400		V/mV
T_{min} to T_{max}, $R_L \geq 2k\Omega$	100/100/**100**			**100**			**100**			V/mV
OUTPUT CHARACTERISTICS										
Voltage @ $R_L \geq 2k\Omega$	**+13, −12.5**	+13.9, −13.3		**+13, −12.5**	+13.9, −13.3		**+13, −12.5**	+13.9, −13.3		V
T_{min} to T_{max}	±12, ±12, **±12**	+13.8, −13.1		**±12**	+13.8, −13.1		**±12**	+13.8, −13.1		V
Short Circuit Current		25			25			25		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current,										
Both Amplifiers		5	**6.8**		5	**6.0**		5	**5.6**	mA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0 to +70°C)		AD712J			AD712K					
Industrial (−40°C to +85°C)		AD712A			AD712B			AD712C		
Military (−55°C to +125°C)		AD712S			AD712T					
PACKAGE OPTIONS[8]										
SOIC (R-8)		AD712JR								
Plastic (N-8)		AD712JN			AD712KN					
Cerdip (Q-8)		AD712AQ, AD712SQ			AD712BQ, AD712TQ			AD712CQ		
TO-99 (H-08A)		AD712AH, AD712SH			AD712BH, AD712TH			AD712CH		
Tape and Reel		AD712JR								
A, J and S Grade Chips Available										

NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25°C$.
[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A = +25°C$. For higher temperature, the current doubles every 10°C.
[3]Matching is defined as the difference between parameters of the two amplifiers.
[4]Refer to Figure 21.
[5]Refer to Figure 29.
[6]Defined as voltage between inputs, such that neither exceeds ±10V from ground.
[7]Typically exceeding −14.1V negative common-mode voltage on either input results in an output phase reversal.
[8]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

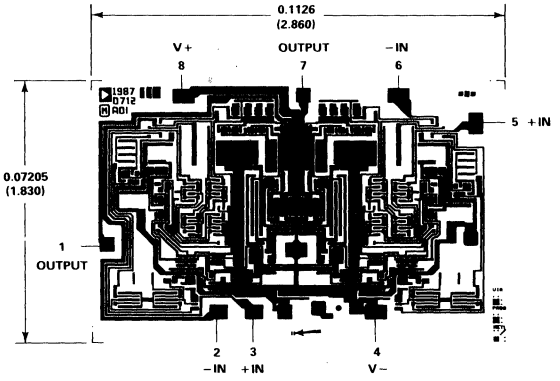
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18V
Internal Power Dissipation[2]	500mW
Input Voltage[3]	±18V
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range Q, H	−65°C to +150°C
Storage Temperature Range N	−65°C to +125°C
Operating Temperature Range	
AD712J/K	0 to +70°C
AD712A/B/C	−40°C to +85°C
AD712S/T	−55°C to +125°C
Lead Temperature Range (Soldering 60 seconds)	300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal Characteristics:
8-Pin Plastic Package: $\theta_{JA} = 165°C/W$.
8-Pin Cerdip Package: $\theta_{JC} = 22°C/W$, $\theta_{JA} = 110°C/W$.
8-Pin Metal Can Package: $\theta_{JC} = 65°C/W$, $\theta_{JA} = 150°C/W$.
[3]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



AD712—Typical Characteristics

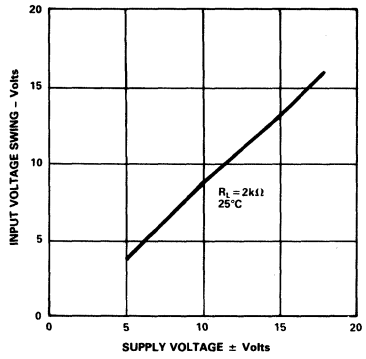


Figure 1. Input Voltage Swing vs. Supply Voltage

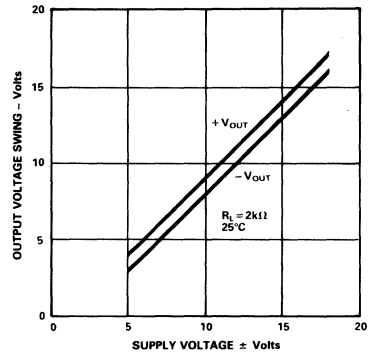


Figure 2. Output Voltage Swing vs. Supply Voltage

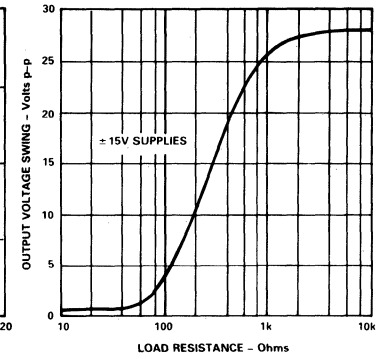


Figure 3. Output Voltage Swing vs. Load Resistance

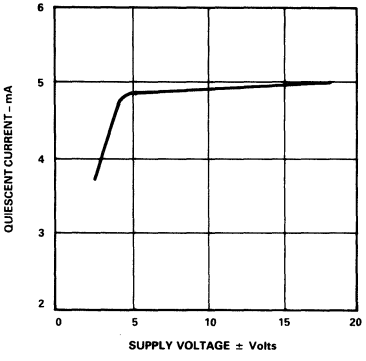


Figure 4. Quiescent Current vs. Supply Voltage

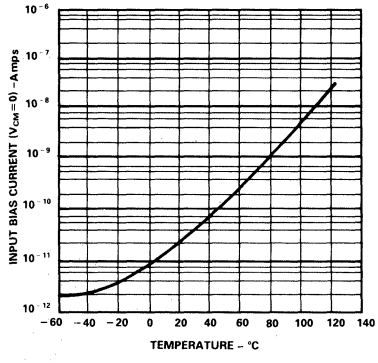


Figure 5. Input Bias Current vs. Temperature

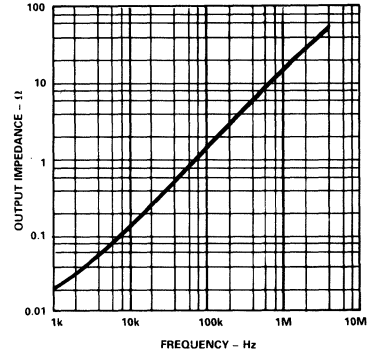


Figure 6. Output Impedance vs. Frequency

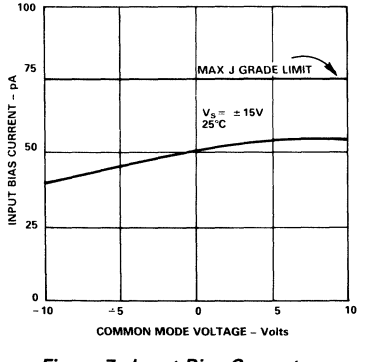


Figure 7. Input Bias Current vs. Common Mode Voltage

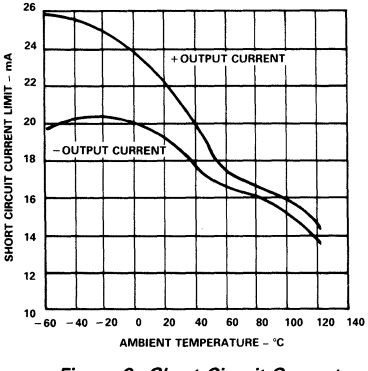


Figure 8. Short Circuit Current Limit vs. Temperature

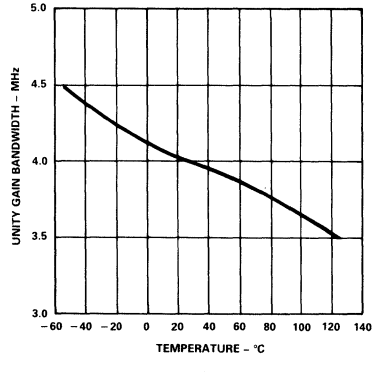


Figure 9. Unity Gain Bandwidth vs.Temperature

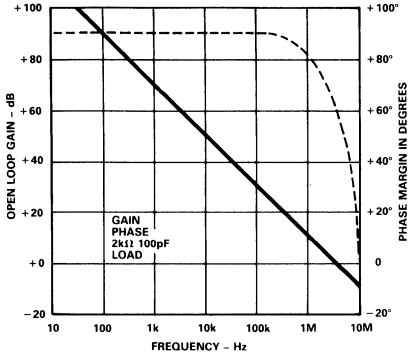


Figure 10. Open Loop Gain and Phase Margin vs. Frequency

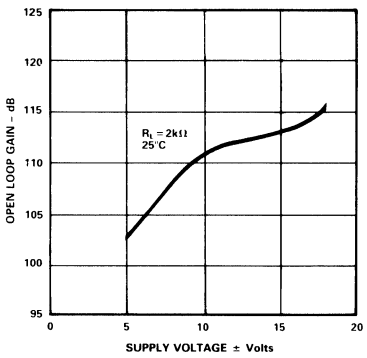


Figure 11. Open Loop Gain vs. Supply Voltage

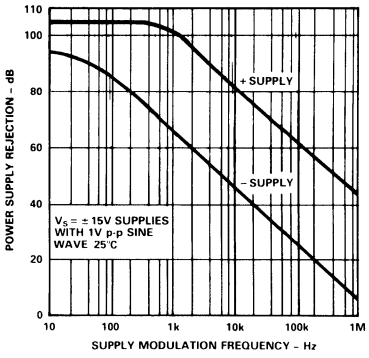


Figure 12. Power Supply Rejection vs. Frequency

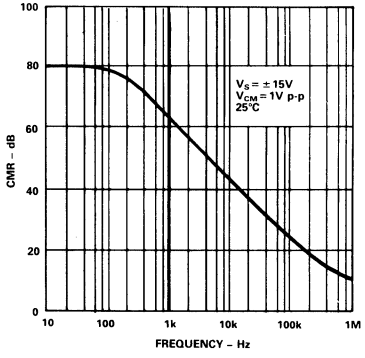


Figure 13. Common Mode Rejection vs. Frequency

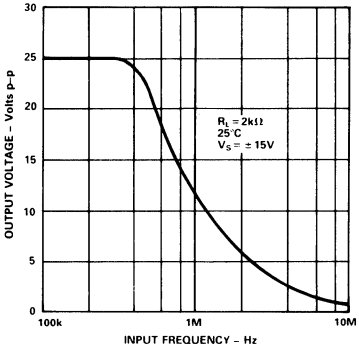


Figure 14. Large Signal Frequency Response

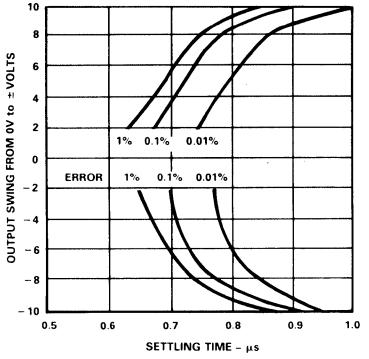


Figure 15. Output Swing and Error vs. Settling Time

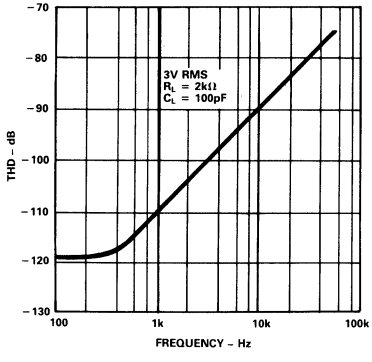


Figure 16. Total Harmonic Distortion vs. Frequency

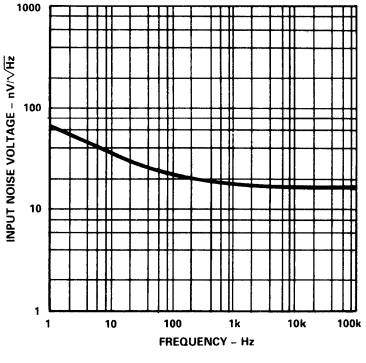


Figure 17. Input Noise Voltage Spectral Density

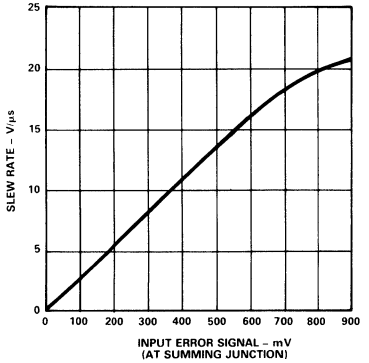


Figure 18. Slew Rate vs. Input Error Signal

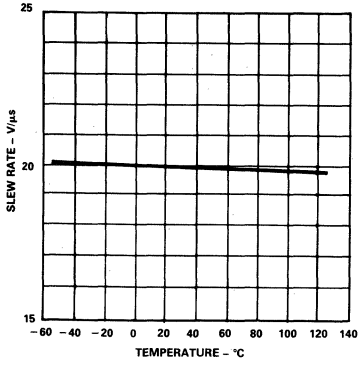


Figure 19. Slew Rate vs. Temperature

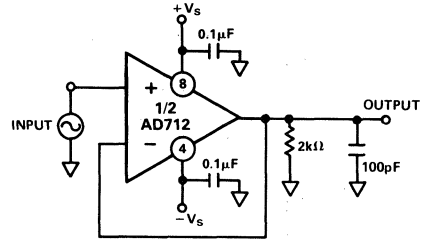


Figure 20. T.H.D. Test Circuit

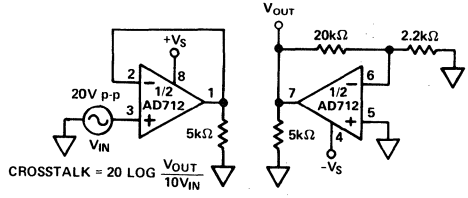


Figure 21. Crosstalk Test Circuit

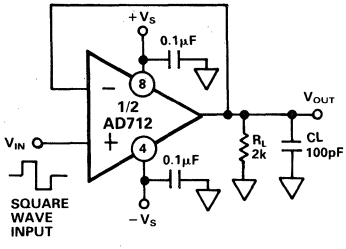


Figure 22a. Unity Gain Follower

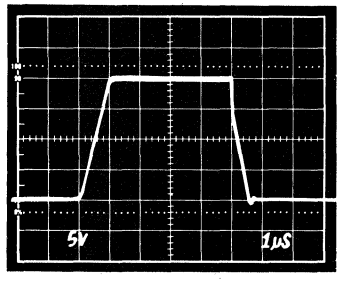


Figure 22b. Unity Gain Follower Pulse Response (Large Signal)

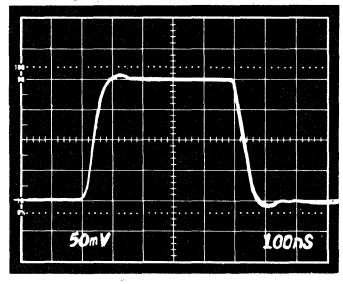


Figure 22c. Unity Gain Follower Pulse Response (Small Signal)

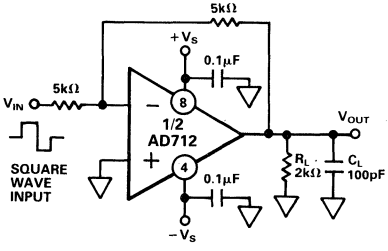


Figure 23a. Unity Gain Inverter

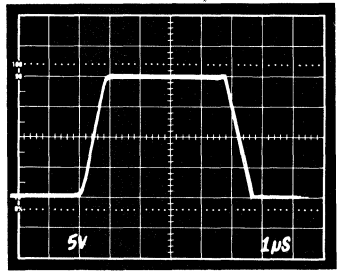


Figure 23b. Unity Gain Inverter Pulse Response (Large Signal)

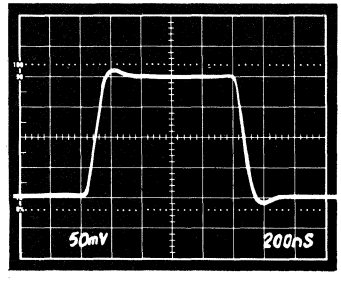


Figure 23c. Unity Gain Inverter Pulse Response (Small Signal)

OPTIMIZING SETTLING TIME

Most bipolar high-speed D/A converters have curent outputs; therefore, for most applications, an external op amp is required for current-to-voltage conversion. The settling time of the converter/op amp combination depends on the settling time of the DAC and output amplifier. A good approximation is:

$$t_s \text{ Total} = \sqrt{(t_s \text{ DAC})^2 + (t_s \text{ AMP})^2}$$

The settling time of an op amp DAC buffer will vary with the noise gain of the circuit, the DAC output capacitance, and with the amount of external compensation capacitance across the DAC output scaling resistor.

Settling time for a bipolar DAC is typically 100 to 500ns. Previously, conventional op amps have required much longer settling times than have typical state-of-the-art DACs; therefore, the amplifier settling time has been the major limitation to a high-speed voltage-output D-to-A function. The introduction of the AD711/712 family of op amps with their 1μs (to ±0.01% of final value) settling time now permits the full high-speed capabilities of most modern DACs to be realized.

In addition to a significant improvement in settling time, the low offset voltage, low offset voltage drift, and high open-loop gain of the AD711/AD712 family assures 12-bit accuracy over the full operating temperature range.

The excellent high-speed performance of the AD712 is shown in the oscilloscope photos of Figure 25. Measurements were taken using a low input capacitance amplifier connected directly to the summing junction of the AD712 – both photos show the worst case situation: a full-scale input transition. The DAC's 4kΩ [10kΩ‖8kΩ = 4.4kΩ] output impedance together with a 10kΩ feedback resistor produce an op amp noise gain of 3.25. The current output from the DAC produces a 10V step at the op amp output (0 to −10V Figure 25a, −10V to 0V Figure 25b.)

Therefore, with an ideal op amp, settling to ±1/2LSB (±0.01%) requires that 375μV or less appears at the summing junction. This means that the error between the input and output (that voltage which appears at the AD712 summing junction) must be less than 375μV. As shown in Figure 25, the total settling time for the AD712/AD565 combination is 1.2 microseconds.

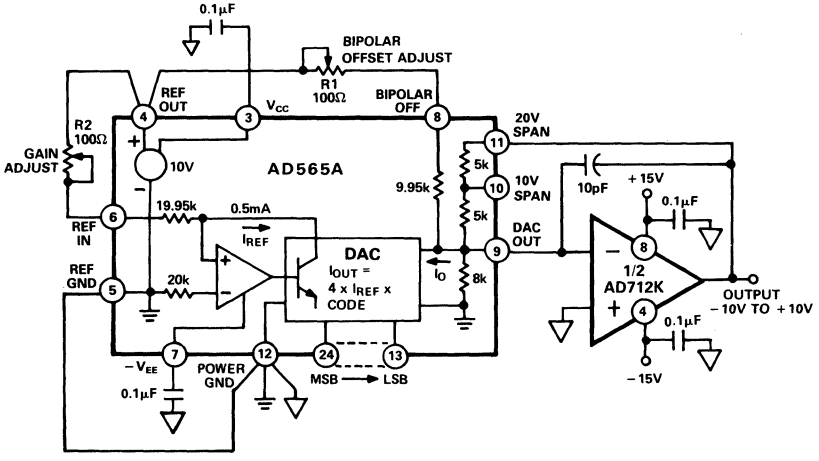
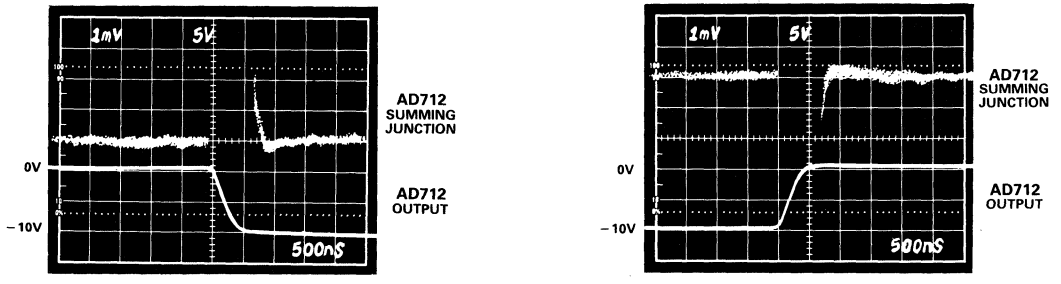


Figure 24. ±10V Voltage Output Bipolar DAC



a. (Full-Scale Negative Transition)

b. (Full-Scale Positive Transition)

Figure 25. Settling Characteristics for AD712 with AD565A

OP AMP SETTLING TIME – A MATHEMATICAL MODEL

The design of the AD712 gives careful attention to optimizing individual circuit components; in addition, a careful tradeoff was made: the gain bandwidth product (4MHz) and slew rate (20V/μs) were chosen to be high enough to provide very fast settling time but not too high to cause a significant reduction in phase margin (and therefore stability). Thus designed, the AD712 settles to ±0.01%, with a 10V output step, in under 1μs, while retaining the ability to drive a 250pF load capacitance when operating as a unity gain follower.

If an op amp is modeled as an ideal integrator with a unity gain crossover frequency of $\omega_O/2\pi$, Equation 1 will accurately describe the small signal behavior of the circuit of Figure 26a, consisting of an op amp connected as an I-to-V converter at the output of a bipolar or CMOS DAC. This equation would completely describe the output of the system if not for the op amp's finite slew rate and other nonlinear effects.

Equation 1.

$$\frac{V_O}{I_{IN}} = \frac{-R}{\frac{R(C_f + C_X)}{\omega_o} s^2 + \left(\frac{G_N}{\omega_o} + RC_f\right) s + 1}$$

where $\frac{\omega_o}{2\pi}$ = op amp's unity gain frequency

G_N = "noise" gain of circuit $\left(1 + \frac{R}{R_O}\right)$

This equation may then be solved for C_f:

Equation 2.

$$C_f = \frac{2 - G_N}{R\omega_o} + \frac{2\sqrt{RC_X\omega_o + (1 - G_N)}}{R\omega_o}$$

In these equations, capacitor C_X is the total capacitance appearing at the inverting terminal of the op amp. When modeling a DAC buffer application, the Norton equivalent circuit of Figure 26a can be used directly; capacitance C_X is the total capacitance of the output of the DAC plus the input capacitance of the op amp (since the two are in parallel).

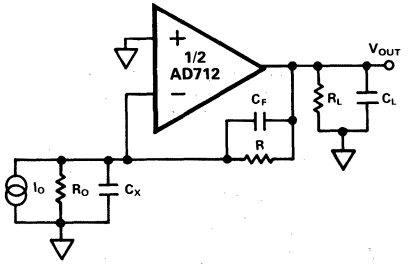


Figure 26a. Simplified Model of the AD712 Used as a Current-Out DAC Buffer

When R_O and I_O are replaced with their Thevenin V_{IN} and R_{IN} equivalents, the general purpose inverting amplifier of Figure 26b is created. Note that when using this general model, capacitance C_X is EITHER the input capacitance of the op amp if a simple inverting op amp is being simulated OR it is the combined capacitance of the DAC output and the op amp input if the DAC buffer is being modeled.

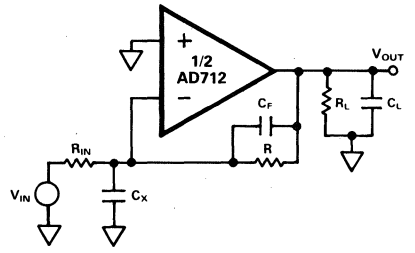


Figure 26b. Simplified Model of the AD712 Used as an Inverter

In either case, the capacitance C_X causes the system to go from a one-pole to a two-pole response; this additional pole increases settling time by introducing peaking or ringing in the op amp output. Since the value of C_X can be estimated with reasonable accuracy, Equation 2 can be used to choose a small capacitor, C_F, to cancel the input pole and optimize amplifier response. Figure 27 is a graphical solution of Equation 2 for the AD712 with R = 4kΩ.

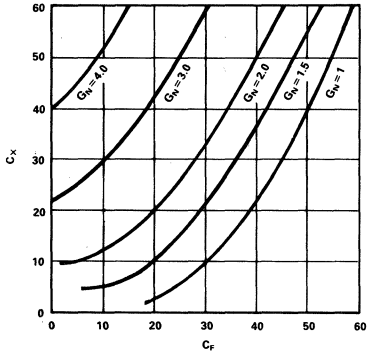


Figure 27. Value of Capacitor C_F vs. Value of C_X

The photos of Figures 28a and 28b show the dynamic response of the AD712 in the settling test circuit of Figure 29.

The input of the settling time fixture is driven by a flat-top pulse generator. The error signal output from the false summing node of A1 is clamped, amplified by A2 and then clamped again. The error signal is thus clamped twice: once to prevent overloading amplifier A2 and then a second time to avoid overloading the oscilloscope preamp. The Tektronix oscilloscope preamp type 7A26 was carefully chosen because it does not overload with these input levels. Amplifier A2 needs to be a very high-speed, FET-input op amp; it provides a gain of 10, amplifying the error signal output of A1.

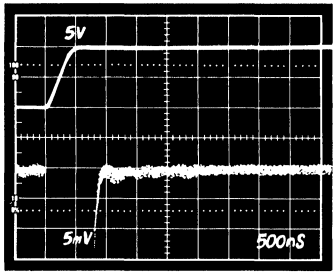


Figure 28a. Settling Characteristics 0 to +10V Step
Upper Trace: Output of AD712 Under Test (5V/Div)
Lower Trace: Amplified Error Voltage (0.01%/Div)

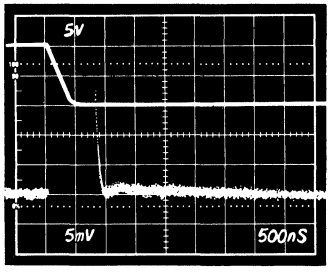


Figure 28b. Settling Characteristics 0 to −10V Step
Upper Trace: Output of AD712 Under Test (5V/Div)
Lower Trace: Amplified Error Voltage (0.01%/Div)

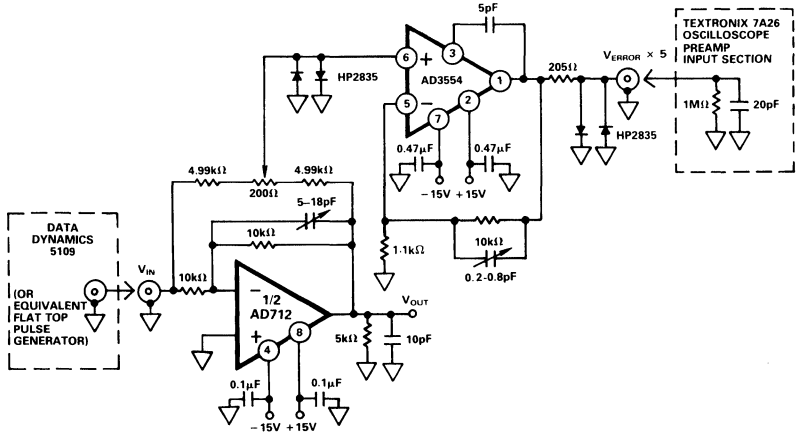


Figure 29. Settling Time Test Circuit

GUARDING

The low input bias current (15pA) and low noise characteristics of the AD712 BiFET op amp make it suitable for electrometer applications such as photo diode preamplifiers and picoampere current-to-voltage converters. The use of a guarding technique such as that shown in Figure 30, in printed circuit board layout and construction is critical to minimize leakage currents. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on the printed circuit board.

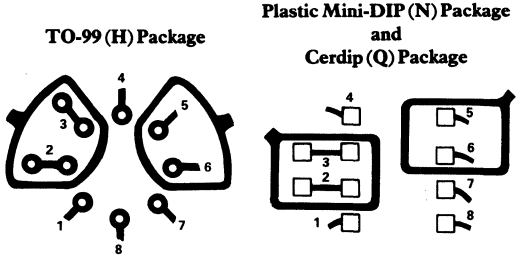


Figure 30. Board Layout for Guarding Inputs

D/A CONVERTER APPLICATIONS

The AD712 is an excellent output amplifier for CMOS DACs. It can be used to perform both 2 quadrant and 4 quadrant operation. The output impedance of a DAC using an inverted R-2R ladder approaches R for codes containing many 1s, 3R for codes containing a single 1, and for codes containing all zero, the output impedance is infinite.

For example, the output resistance of the AD7545 will modulate between 11kΩ and 33kΩ. Therefore, with the DAC's internal feedback resistance of 11kΩ, the noise gain will vary from 2 to 4/3. This changing noise gain modulates the effect of the input offset voltage of the amplifier, resulting in nonlinear DAC-amplifier performance.

The AD712K with guaranteed 700μV offset voltage minimizes this effect to achieve 12-bit performance.

Figures 31 and 32 show the AD712 and AD7545 (12-bit CMOS DAC) configured for unipolar binary (2-quadrant multiplication) or bipolar (4-quadrant multiplication) operation. Capacitor C1 provides phase compensation to reduce overshoot and ringing.

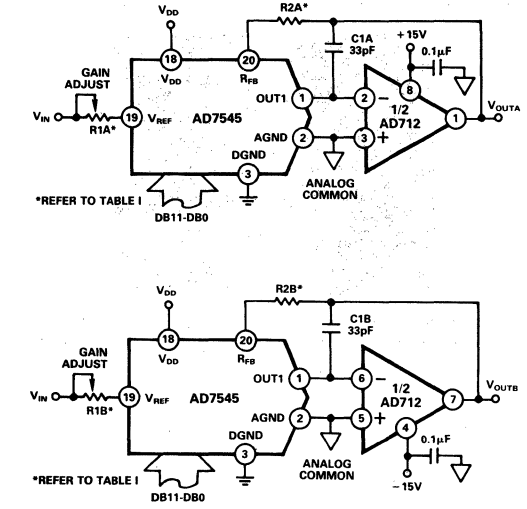


Figure 31. Unipolar Binary Operation

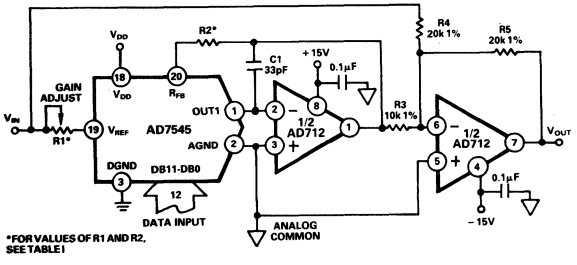


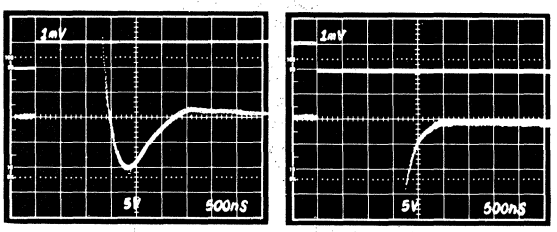
Figure 32. Bipolar Operation

R1 and R2 calibrate the zero offset and gain error of the DAC. Specific values for these resistors depend upon the grade of AD7545 and are shown below.

TRIM RESISTOR	JN/AQ/SD	KN/BQ/TD	LN/CQ/UD	GLN/GCQ/GUD
R1	500Ω	200Ω	100Ω	20Ω
R2	150Ω	68Ω	33Ω	6.8Ω

Table I. Recommended Trim Resistor Values vs. Grades of the AD7545 for $V_{DD} = +5V$

Figures 33a and 33b show the settling time characteristics of the AD712 when used as a DAC output buffer for the AD7545.



a. Full-Scale Positive Transition

b. Full-Scale Negative Transition

Figure 33. Settling Characteristics for AD712 with AD7545

NOISE CHARACTERISTICS

The random nature of noise, particularly in the l/f region, makes it difficult to specify in practical terms. At the same time, designers of precision instrumentation require certain guaranteed maximum noise levels to realize the full accuracy of their equipment.

The AD712C grade is specified at a maximum level of 4.0μV p-p, in a 0.1 to 10Hz bandwidth. Each AD712C receives a 100% noise test for two 10-second intervals; devices with any excursion in excess of 4.0μV are rejected. The screened lot is then submitted to Quality Control for verification on an AQL basis.

All other grades of the AD712 are sample-tested on an AQL basis to a limit of 6μV p-p, 0.1 to 10Hz.

DRIVING THE ANALOG INPUT OF AN A/D CONVERTER

An op amp driving the analog input of an A/D converter, such as that shown in Figure 34, must be capable of maintaining a constant output voltage under dynamically changing load conditions. In successive-approximation converters, the input current is compared to a series of switched trial currents. The comparison point is diode clamped but may deviate several hundred millivolts resulting in high frequency modulation of A/D input current. The output impedance of a feedback amplifier is made artificially low by the loop gain. At high frequencies, where the loop gain is low, the amplifier output impedance can approach its open loop value. Most IC amplifiers exhibit a minimum open loop output impedance of 25Ω due to current limiting resistors. A

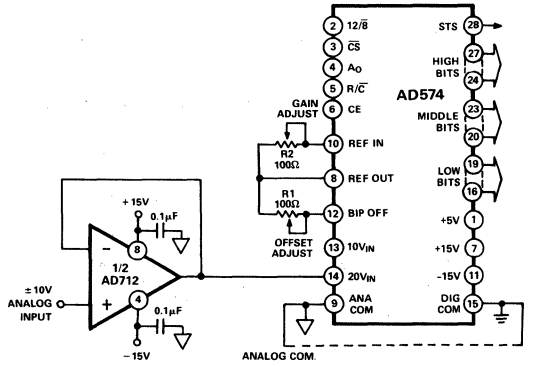
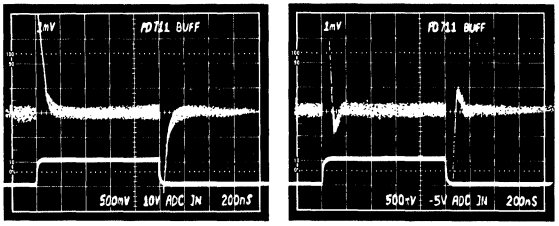


Figure 34. AD712 as ADC Unity Gain Buffer



a. Source Current = 2mA *b. Sink Current = 1mA*

Figure 35. ADC Input Unity Gain Buffer Recovery Times

few hundred microamps reflected from the change in converter loading can introduce errors in instantaneous input voltage. If the A/D conversion speed is not excessive and the bandwidth of the amplifier is sufficient, the amplifier's output will return to the nominal value before the converter makes its comparison. However, many amplifiers have relatively narrow bandwidth yielding slow recovery from output transients. The AD712 is ideally suited to drive high-speed A/D converters since it offers both wide bandwidth and high open-loop gain.

DRIVING A LARGE CAPACITIVE LOAD

The circuit in Figure 36 employs a 100Ω isolation resistor which enables the amplifier to drive capacitive loads exceeding 1500pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 100Ω series resistor and the load capacitance, C_L. Figure 37 shows a typical transient response for this connection.

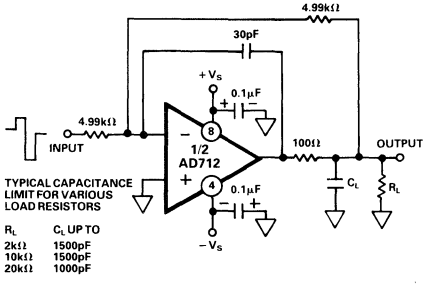


Figure 36. Circuit for Driving a Large Capacitive Load

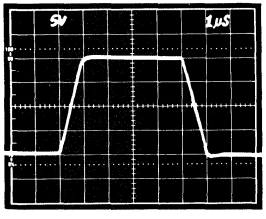


Figure 37. Transient Response R_L = 2kΩ, C_L =500pF

ACTIVE FILTER APPLICATIONS

In active filter applications using op amps, the dc accuracy of the amplifier is critical to optimal filter performance. The amplifier's offset voltage and bias current contribute to output error. Offset voltage will be passed by the filter and may be amplified to produce excessive output offset. For low frequency applications requiring large value input resistors, bias currents flowing through these resistors will also generate an offset voltage.

In addition, at higher frequencies, an op amp's dynamics must be carefully considered. Here, slew rate, bandwidth, and open-loop gain play a major role in op amp selection. The slew rate must be fast as well as symmetrical to minimize distortion. The amplifier's bandwidth in conjunction with the filter's gain will dictate the frequency response of the filter.

The use of a high performance amplifier such as the AD712 will minimize both dc and ac errors in all active filter applications.

SECOND ORDER LOW PASS FILTER

Figure 38 depicts the AD712 configured as a second order Butterworth low pass filter. With the values as shown, the corner frequency will be 20kHz; however, the wide bandwidth of the AD712 permits a corner frequency as high as several hundred kilohertz. Equations for component selection are shown below.

$$R1 = R2 = \text{user selected (typical values: } 10k\Omega - 100k\Omega)$$

$$C1 \text{ (in farads)} = \frac{1.414}{(2\pi)\,(f_{cutoff})\,(R1)} \qquad C2 = \frac{0.707}{(2\pi)\,(f_{cutoff})\,(R1)}$$

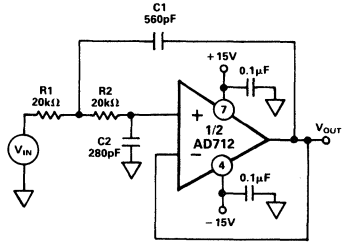


Figure 38. Second Order Low Pass Filter

An important property of filters is their out-of-band rejection. The simple 20kHz low pass filter shown in Figure 38, might be used to condition a signal contaminated with clock pulses or sampling glitches which have considerable energy content at high frequencies.

The low output impedance and high bandwidth of the AD712 minimize high frequency feedthrough as shown in Figure 39.

The upper trace is that of another low-cost BiFET op amp showing 17dB more feedthrough at 5MHz.

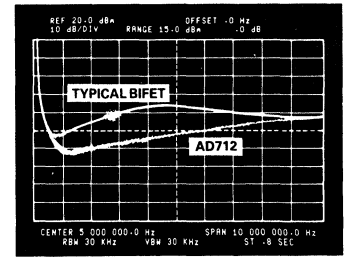


Figure 39.

9-POLE CHEBYCHEV FILTER

Figure 40 shows the AD712 and its single counterpart, the AD711, as a 9-pole Chebychev filter using active frequency dependent negative resistors (FDNR). With a cutoff frequency of 50kHz and better than 90dB rejection, it may be used as an antialiasing filter for a 12-bit Data Acquisition System with 100kHz throughput.

As shown in Figure 40, the filter is comprised of four FDNRs (A, B, C, D) having values of 4.9395×10^{-15} and 5.9276×10^{-15} farad-seconds. Each FDNR active network provides a two-pole response; for a total of 8 poles. The 9th pole consists of a 0.001μF capacitor and a 124kΩ resistor at Pin 3 of amplifier A2. Figure 41 depicts the circuits for each FDNR with the proper selection of R. To achieve optimal performance, the 0.001μF capacitors must be selected for 1% or better matching and all resistors should have 1% or better tolerance.

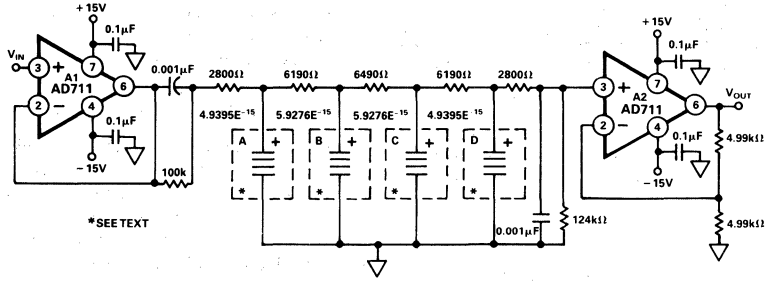


Figure 40. 9-Pole Chebychev Filter

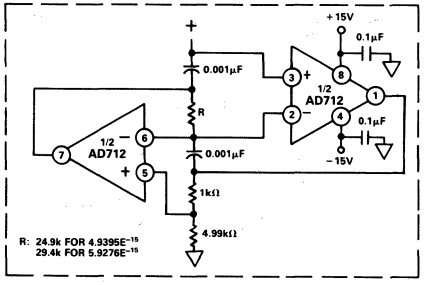


Figure 41. FDNR for 9-Pole Chebychev Filter

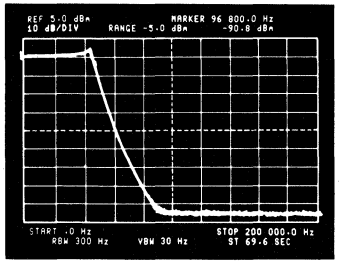


Figure 42. High Frequency Response for 9-Pole Chebychev Filter

Quad Precision, Low Cost, High Speed BiFET Op Amp

AD713

FEATURES

Enhanced Replacement for LF347 and TL084

AC PERFORMANCE

- **1μs Settling to 0.01% for 10V Step**
- **20V/μs Slew Rate**
- **0.0003% Total Harmonic Distortion (THD)**
- **4MHz Unity Gain Bandwidth**

DC PERFORMANCE

- **0.5mV max Offset Voltage (AD713K)**
- **20μV/°C max Drift (AD713K)**
- **200V/mV min Open Loop Gain (AD713K)**
- **2μV p–p typ Noise, 0.1Hz to 10Hz**

True 14-Bit Accuracy

Single Version: AD711, Dual Version: AD712

Available in 16-Pin SOIC, 14-Pin Plastic DIP and Hermetic Cerdip Packages and Chip Form

MIL-STD-883B Processing Available

APPLICATIONS

Active Filters

Quad Output Buffers for 12- and 14-Bit DACs

Input Buffers for Precision ADCs

Photo Diode Preamplifier Applications

PRODUCT DESCRIPTION

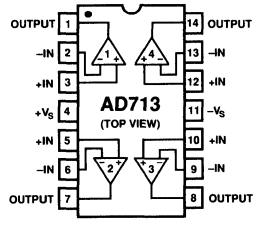
The AD713 is a quad operational amplifier, consisting of four AD711 BiFET op amps. These precision monolithic op amps offer excellent dc characteristics plus rapid settling times, high slew rates, and ample bandwidths. In addition, the AD713 provides the close matching ac and dc characteristics inherent to amplifiers sharing the same monolithic die.

The single-pole response of the AD713 provides fast settling: 1μs to 0.01%. This feature, combined with its high dc precision, makes it suitable for use as a buffer amplifier for 12- or 14-bit DACs and ADCs. It is also an excellent choice for use in active filters in 12-, 14- and 16-bit data acquisition systems. Furthermore, the AD713's low total harmonic distortion (THD) level of 0.0003% and very close matching ac characteristics make it an ideal amplifier for many demanding audio applications.

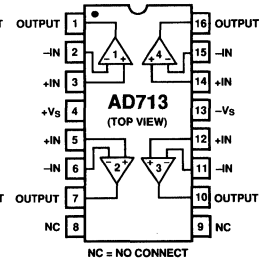
The AD713 is internally compensated for stable operation at unity gain and is available in seven performance grades. The AD713J and AD713K are rated over the commercial temperature range of 0 to +70°C. The AD713A and AD713B are rated over the industrial temperature of −40°C to +85°C. The AD713S and AD713T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

CONNECTION DIAGRAMS

Plastic (N) and Cerdip (Q) Packages



SOIC (R) Package



The AD713 is offered in a 16-pin SOIC, 14-pin plastic DIP and hermetic cerdip package, or in chip form.

PRODUCT HIGHLIGHTS

1. The AD713 is a high speed BiFET op amp that offers excellent performance at competitive prices. It upgrades the performance of circuits using op amps such as the TL074/TL084, LT1058, LF347 and OPA404.
2. Slew rate is 100% tested for a guaranteed minimum of 16V/μs (J, A and S Grades).
3. The combination of Analog Devices' advanced processing technology, laser wafer drift trimming and well-matched ion-implanted JFETs provides outstanding dc precision. Input offset voltage, input bias current and input offset current are specified in the warmed-up condition and are 100% tested.
4. Very close matching of ac characteristics between the four amplifiers makes the AD713 ideal for high quality active filter applications.

AD713—SPECIFICATIONS (@ +25°C and ±15V dc, unless otherwise noted)

Model	Conditions	AD713J/A/S Min	AD713J/A/S Typ	AD713J/A/S Max	AD713K/B/T Min	AD713K/B/T Typ	AD713K/B/T Max	Units
INPUT OFFSET VOLTAGE[1]								
Initial Offset			0.3	**1.5**		0.2	**0.5**	mV
Offset	T_{min} to T_{max}		0.5	2/2/2		0.4	**0.7/0.7/1.0**	mV
vs. Temp.			5			5	20/**20**/**15**	µV/°C
vs. Supply		**78**	95		**84**	100		dB
vs. Supply	T_{min} to T_{max}	76/76/**76**	95		**84**	100		dB
Long-Term Stability			15			15		µV/month
INPUT BIAS CURRENT[2]								
Either Input	V_{CM}=0V		40	**150**		40	**75**	pA
Either Input @ T_{max} = 70°C/85°C/125°C	V_{CM}=0V			3.4/9.6/154			1.7/4.8/77	nA
Either Input	V_{CM}=+10V		55	200		55	**120**	pA
Offset Current	V_{CM}=0V		10	**75**		10	**35**	pA
Offset Current @ T_{max} = 70°C/85°C/125°C	V_{CM}=0V			1.7/4.8/77			0.8/2.2/36	nA
MATCHING CHARACTERISTICS								
Input Offset Voltage			0.5	**1.8**		0.4	**0.8**	mV
Input Offset Voltage	T_{min} to T_{max}		0.7	2.3/2.3/**2.3**		0.6	**1.0/1.0/1.3**	mV
Input Offset Voltage Drift			8			6	25	µV/°C
Input Bias Current			10	**100**		10	**35**	pA
Crosstalk (See Figure 20)	@ 1kHz			−130			−130	dB
	@ 100kHz			−95			−95	dB
FREQUENCY RESPONSE								
Gain BW, Small Signal	G=−1	3	4		3.4	4		MHz
Full Power Response	V_O=20V p-p		200			200		kHz
Slew Rate, Unity Gain	G=−1	**16**	20		**18**	20		V/µs
Settling Time to 0.01%	G=−1 (Fig. 23)		1	1.2		1	1.2	µs
Total Harmonic Distortion (See Figures 16 and 30)	f=1kHz Rl≥2kΩ V_O=3V rms		0.0003			0.0003		%
INPUT IMPEDANCE								
Differential			$3\times10^{12}\|\|5.5$			$3\times10^{12}\|\|5.5$		Ω||pF
Common Mode			$3\times10^{12}\|\|5.5$			$3\times10^{12}\|\|5.5$		Ω||pF
INPUT VOLTAGE RANGE								
Differential[3]			±20			±20		V
Common-Mode Voltage[4]			+14.5,−11.5			+14.5,−11.5		V
T_{min} to T_{max}		−11		+13	**−11**		+13	V
Common-Mode Rejection Ratio	V_{CM}=±10V	**78**	88		**84**	94		dB
	T_{min} to T_{max}	76/76/**76**	84		**82**	90		dB
	V_{CM}=±11V	**72**	84		**78**	90		dB
	T_{min} to T_{max}	70/70/**70**	80		**74**	84		dB
INPUT VOLTAGE NOISE	Noise 0.1 to 10Hz		2			2		µV p-p
	f=10Hz		45			45		nV/$\sqrt{Hz}$
	f=100Hz		22			22		nV/$\sqrt{Hz}$
	f=1kHz		18			18		nV/$\sqrt{Hz}$
	f=10kHz		16			16		nV/$\sqrt{Hz}$
INPUT CURRENT NOISE	f=1kHz		0.01			0.01		pA/$\sqrt{Hz}$
OPEN LOOP GAIN	V_O=±10V							
	R_{LOAD}≥2kΩ	**150**	400		**200**	400		V/mV
	T_{min} to T_{max}	100/100/**100**			**100**			V/mV
OUTPUT CHARACTERISTICS								
Voltage	R_{LOAD}≥2kΩ	**+13,−12.5**	+13.9,−13.3		**+13,−12.5**	+13.9,−13.3		V
	T_{min} to T_{max}	±12/±12/**±12**	+13.8,−13.1		**±12**	+13.8,−13.1		V
Current	Short Circuit		25			25		mA

Model	Conditions	AD713J/A/S Min	AD713J/A/S Typ	AD713J/A/S Max	AD713K/B/T Min	AD713K/B/T Typ	AD713K/B/T Max	Units
POWER SUPPLY								
Rated Performance			±15			±15		V
Operating Range		±4.5		±18	±4.5		±18	V
Quiescent Current			10.0	13.5		10.0	12.0	mA
TRANSISTOR COUNT	# of Transistors		120			120		

NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Bias Current Specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.
[3]Defined as voltage between inputs, such that neither exceeds ±10V from ground.
[4]Typically exceeding −14.1V negative common-mode voltage on either input results in an output phase reversal.

Specifications subject to change without notice.
All min and max specifications are guaranteed.
Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

2

ABSOLUTE MAXIMUM RATINGS[1, 2]

Supply Voltage . . . . . ±18V
Internal Power Dissipation[2]
Input Voltage[3] . . . . . ±18V
Output Short Circuit Duration
(For One Amplifier) . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range Q . . . . . −65°C to +150°C
Storage Temperature Range N . . . . . −65°C to +125°C
Operating Temperature Range
AD713J/K . . . . . 0 to +70°C
AD713A/B . . . . . −40°C to +85°C
AD713S/T . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal characteristics:
14-pin plastic package: θ_{JA} = 100°C/W, θ_{JC} = 30°C/W
14-pin cerdip package: θ_{JA} = 110°C/W; θ_{JC} = 30°C/W.
[3]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

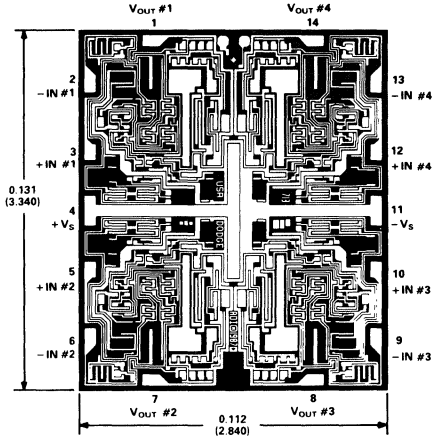
ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
AD713JN	Commercial 0°C to +70°C	14-Pin Plastic Mini-DIP	N-14
AD713JR	Commercial 0°C to +70°C	16-Pin Plastic SOIC	R-16
AD713KN	Commercial 0°C to +70°C	14-Pin Plastic Mini-DIP	N-14
AD713AQ	Industrial −40°C to +85°C	14-Pin Cerdip	Q-14
AD713BQ	Industrial −40°C to +85°C	14-Pin Cerdip	Q-14
AD713SQ	Military −55°C to +125°C	14-Pin Cerdip	Q-14
AD713SQ/883B	Military −55°C to +125°C	14-Pin Cerdip	Q-14
AD713TQ	Military −55°C to +125°C	14-Pin Cerdip	Q-14
AD713TQ/883B	Military −55°C to +125°C	14-Pin Cerdip	Q-14

NOTES
[1]"J" and "S" grade chips are also available.
[2]N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



AD713—Typical Characteristics

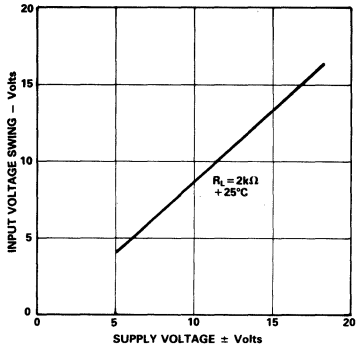


Figure 1. Input Voltage Swing vs. Supply Voltage

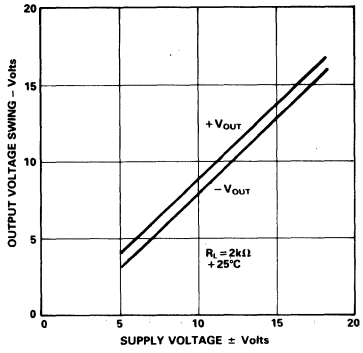


Figure 2. Output Voltage Swing vs. Supply Voltage

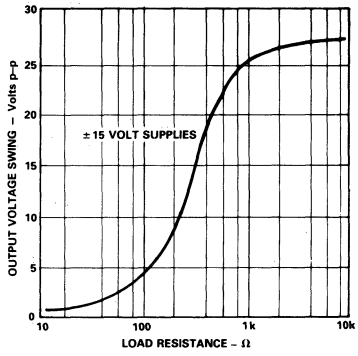


Figure 3. Output Voltage Swing vs. Load Resistance

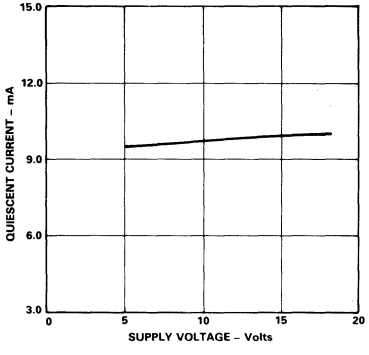


Figure 4. Quiescent Current vs. Supply Voltage

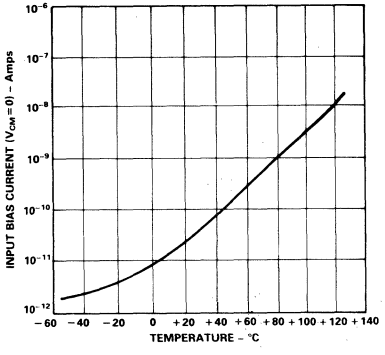


Figure 5. Input Bias Current vs. Temperature

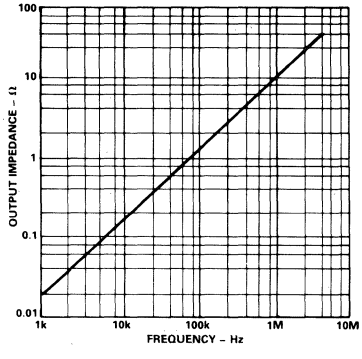


Figure 6. Output Impedance vs. Frequency, G = 1

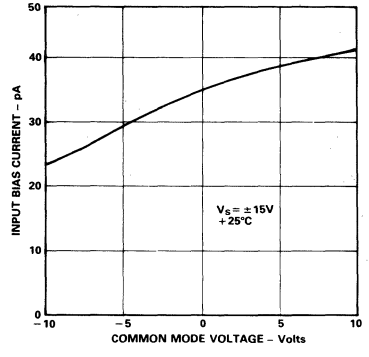


Figure 7. Input Bias Current vs. Common Mode Voltage

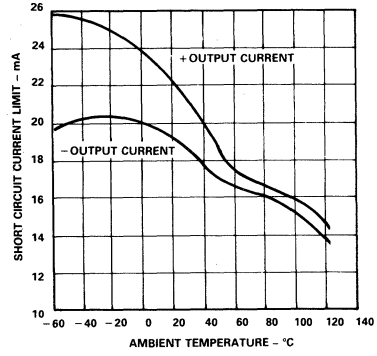


Figure 8. Short Circuit Current Limit vs. Temperature

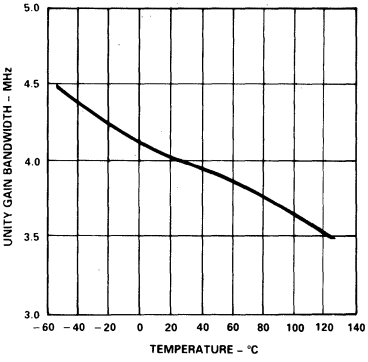


Figure 9. Gain Bandwidth Product vs. Temperature

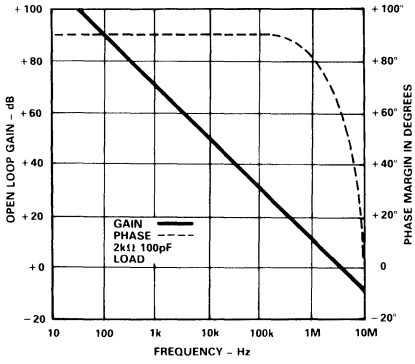


Figure 10. Open Loop Gain and Phase Margin vs. Frequency

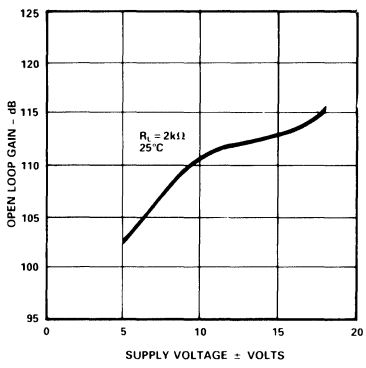


Figure 11. Open Loop Gain vs. Supply Voltage

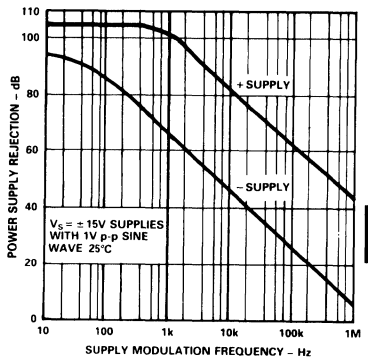


Figure 12. Power Supply Rejection vs. Frequency

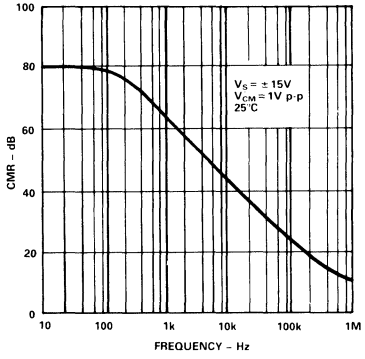


Figure 13. Common Mode Rejection vs. Frequency

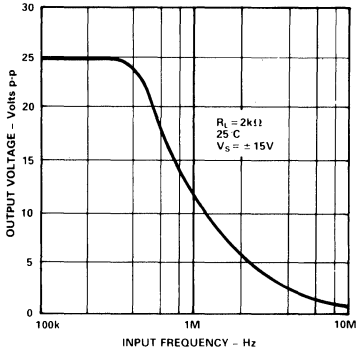


Figure 14. Large Signal Frequency Response

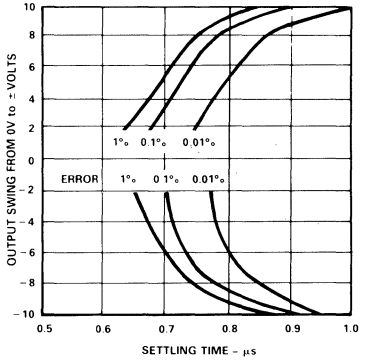


Figure 15. Output Swing and Error vs. Settling Time

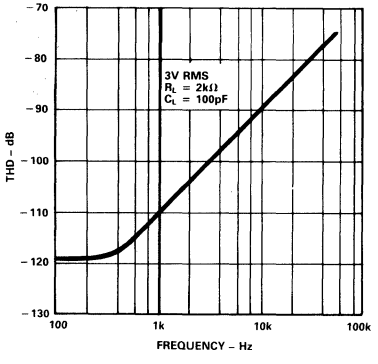


Figure 16. Total Harmonic Distortion vs. Frequency

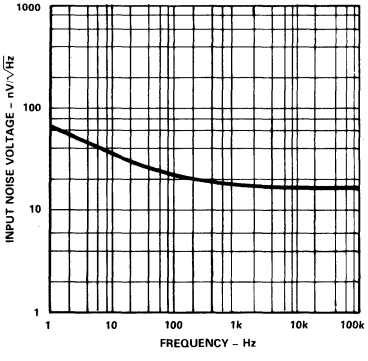


Figure 17. Input Noise Voltage Spectral Density

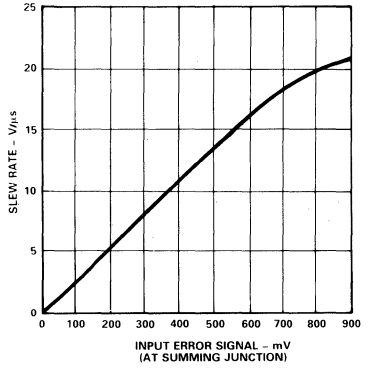
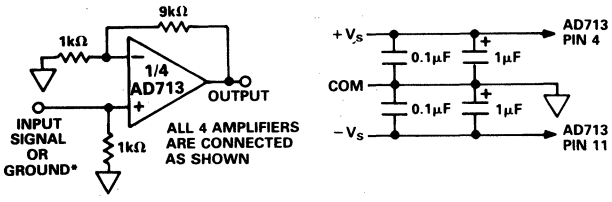


Figure 18. Slew Rate vs. Input Error Signal



*THE SIGNAL INPUT (1kHz SINEWAVE, 2V p-p) IS APPLIED TO ONE AMPLIFIER AT A TIME. THE OUTPUTS OF THE OTHER THREE AMPLIFIERS ARE THEN MEASURED FOR CROSSTALK.

Figure 19. Crosstalk Test Circuit

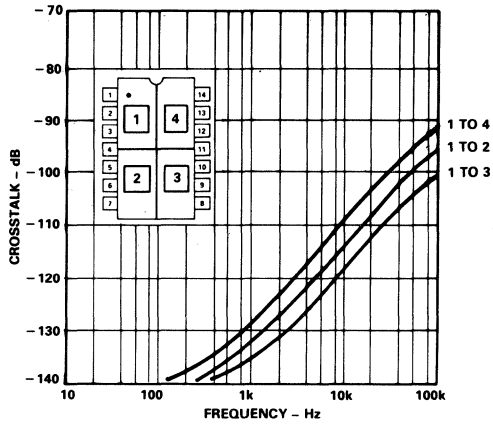


Figure 20. Crosstalk vs. Frequency

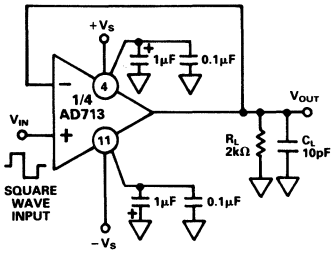


Figure 21a. Unity Gain Follower

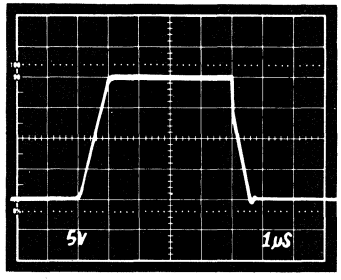


Figure 21b. Unity Gain Follower Large Signal Pulse Response

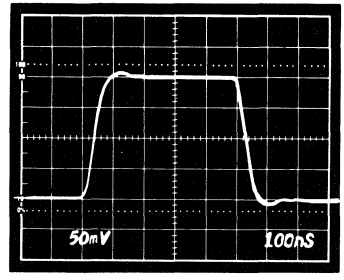


Figure 21c. Unity Gain Follower Small Signal Pulse Response

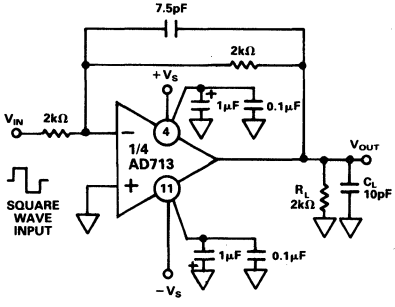


Figure 22a. Unity Gain Inverter

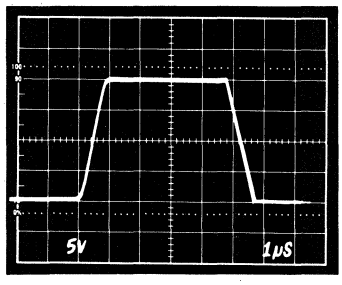


Figure 22b. Unity Gain Inverter Large Signal Pulse Response

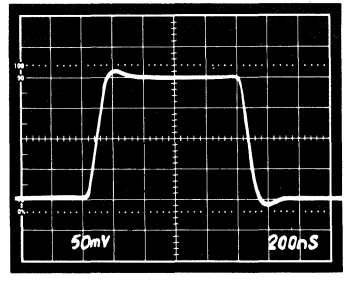


Figure 22c. Unity Gain Inverter Small Signal Pulse Response

MEASURING AD713 SETTLING TIME

The photos of Figures 24 and 25 show the dynamic response of the AD713 while operating in the settling time test circuit of Figure 23. The input of the settling time fixture is driven by a flat-top pulse generator. The error signal output from the false summing node of A1, the AD713 under test, is clamped, amplified by op amp A2 and then clamped again.

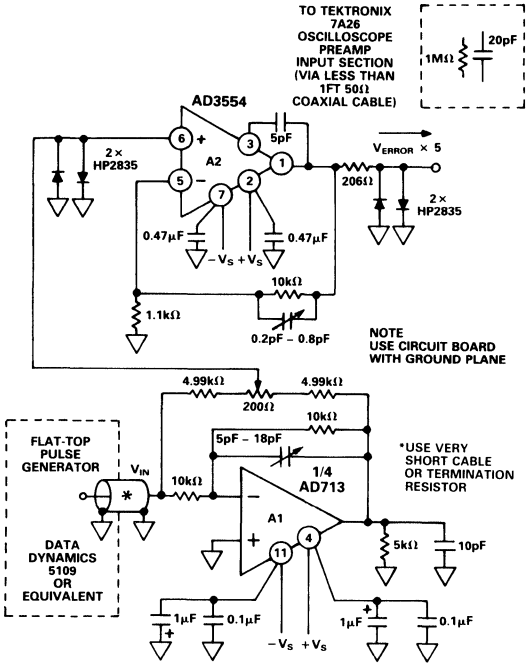


Figure 23. Settling Time Test Circuit

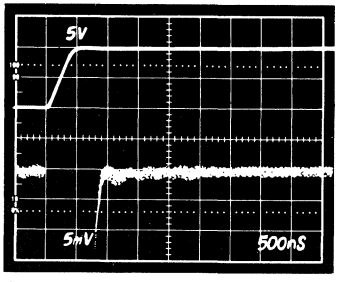


Figure 24. Settling Characteristics 0 to +10V Step. Upper Trace: Output of AD713 Under Test (5V/div). Lower Trace: Amplified Error Voltage (0.01%/div)

The error signal is thus clamped twice: once to prevent overloading amplifier A2 and then a second time to avoid overloading the oscilloscope preamp. A Tektronix oscilloscope preamp type 7A26 was carefully chosen because it recovers from the approximately 0.4 volt overload quickly enough to allow accurate measurement of the AD713's 1μs settling time. Amplifier A2 is a very high speed FET input op amp; it provides a voltage gain of 10, amplifying the error signal output of the AD713 under test (providing an overall gain of 5).

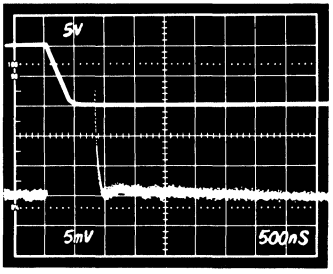


Figure 25. Settling Characteristics to −10V Step. Upper Trace: Output of AD713 Under Test (5V/div). Lower Trace: Amplified Error Voltage (0.01%/div)

POWER SUPPLY BYPASSING

The power supply connections to the AD713 must maintain a low impedance to ground over a bandwidth of 4MHz or more. This is especially important when driving a significant resistive or capacitive load, since all current delivered to the load comes from the power supplies. Multiple high quality bypass capacitors are recommended for each power supply line in any critical application. A 0.1μF ceramic and a 1μF electrolytic capacitor as shown in Figure 26 placed as close as possible to the amplifier (with short lead lengths to power supply common) will assure adequate high frequency bypassing in most applications. A minimum bypass capacitance of 0.1μF should be used for any application.

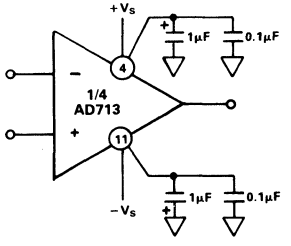


Figure 26. Recommended Power Supply Bypassing

A HIGH SPEED INSTRUMENTATION AMPLIFIER CIRCUIT

The instrumentation amplifier circuit shown in Figure 27 can provide a range of gains from unity up to 1000 and higher using only a single AD713. The circuit bandwidth is 1.2MHz at a gain of 1 and 250kHz at a gain of 10; settling time for the entire circuit is less than 5μs to within 0.01% for a 10 volt step, (G = 10). Other uses for amplifier A4 include an active data guard and an active sense input.

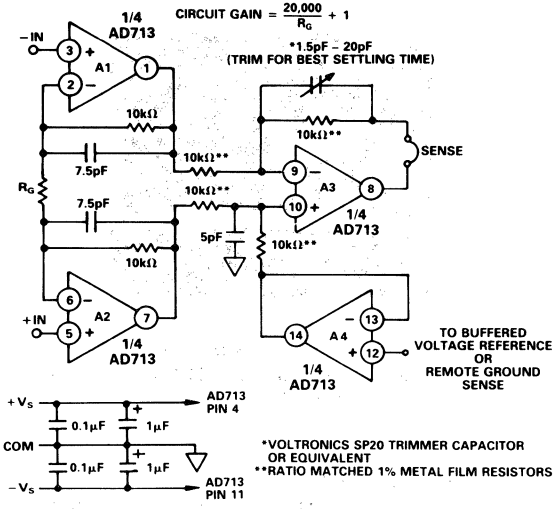


Figure 27. A High Speed Instrumentation Amplifier Circuit

Table I provides a performance summary for this circuit. The photo of Figure 28 shows the pulse response of this circuit for a gain of 10.

Gain	R_G	Bandwidth	T Settle (0.01%)
1	NC	1.2MHz	2μs
2	20kΩ	1.0MHz	2μs
10	4.04kΩ	0.25MHz	5μs

Table I. Performance Summary for the High Speed Instrumentation Amplifier Circuit

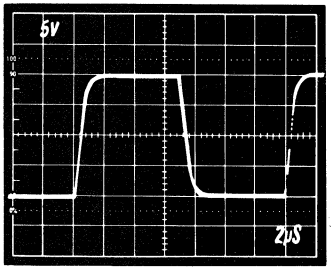


Figure 28. The Pulse Response of the High Speed Instrumentation Amplifier. Gain = 10

A HIGH SPEED FOUR OP AMP CASCADED AMPLIFIER CIRCUIT

Figure 29 shows how the four amplifiers of the AD713 may be connected in cascade to form a high gain, high bandwidth amplifier. This gain of 100 amplifier has a −3dB bandwidth greater than 600kHz.

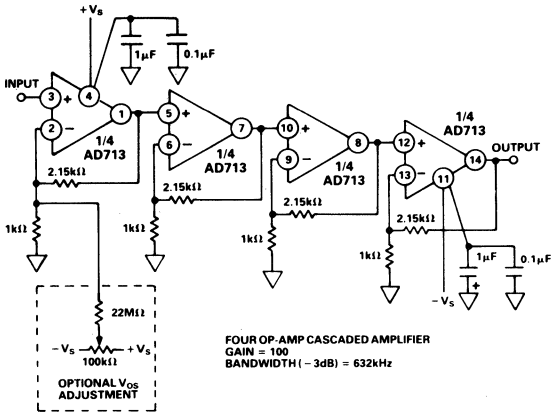


Figure 29. A High Speed Four Op Amp Cascaded Amplifier Circuit

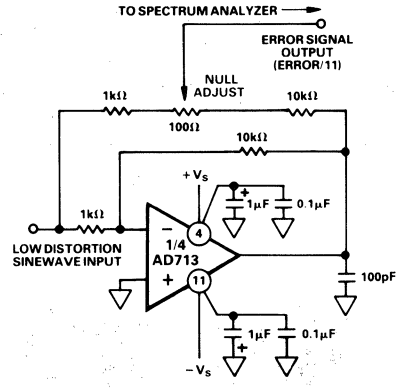


Figure 30. THD Test Circuit

HIGH SPEED OP AMP APPLICATIONS AND TECHNIQUES

DAC Buffers (I-to-V Converters)

The wide input dynamic range of JFET amplifiers makes them ideal for use in both waveform reconstruction and digital-audio-DAC applications. The AD713, in conjunction with the AD1860 DAC, can achieve 0.0016% THD (here at a 4fs or a 176.4kHz update rate) without requiring the use of a deglitcher. Just such a circuit is shown in Figure 31. The 470pF feedback capacitor used with IC2a, along with op amp IC2b and its associated components, together form a 3-pole low-pass filter. Each or all of these poles can be tailored for the desired attenuation and phase characteristics required for a particular application. In this application, one half of an AD713 serves each channel in a two-channel stereo system.

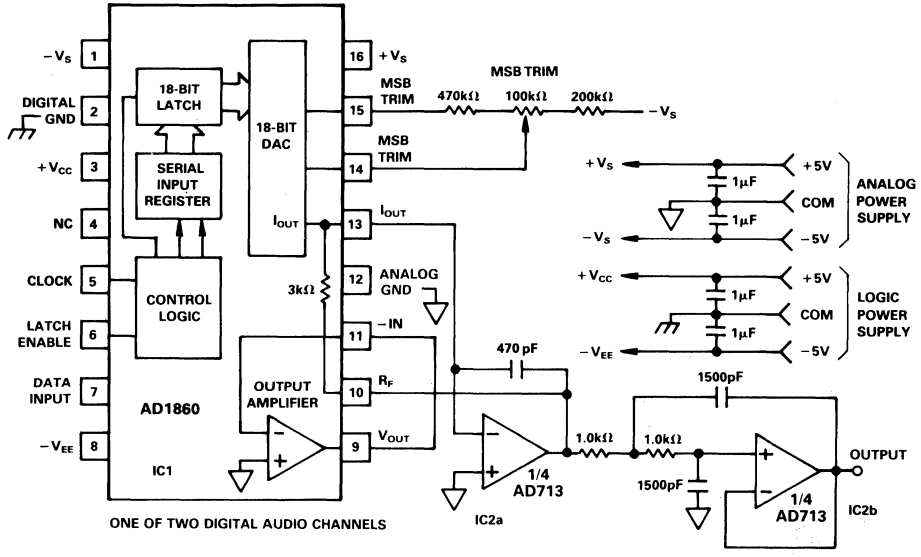


Figure 31. A D/A Converter Circuit for Digital Audio

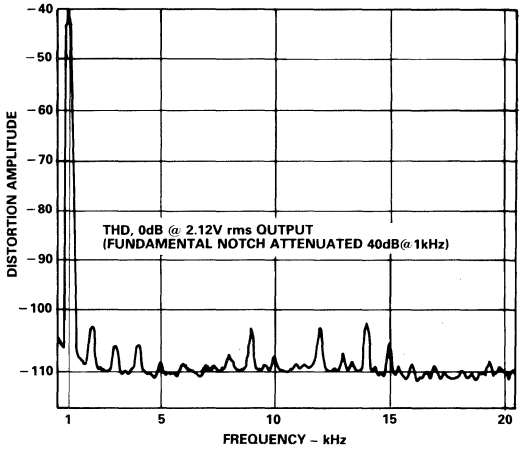


Figure 32. Harmonic Distortion vs. Frequency for the Digital Audio Circuit of Figure 31

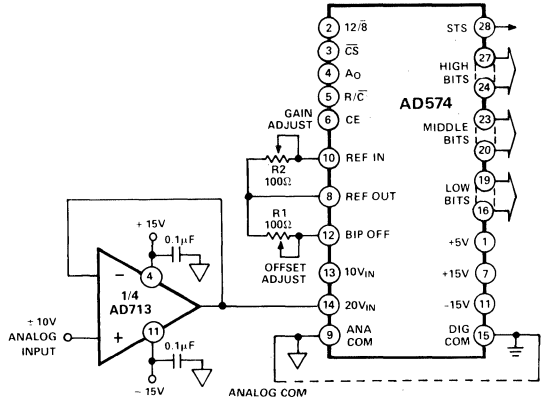


Figure 33. The AD713 as an ADC Buffer

Driving the Analog Input of an A/D Converter

An op amp driving the analog input of an A/D converter, such as that shown in Figure 33, must be capable of maintaining a constant output voltage under dynamically changing load conditions. In successive approximation converters, the input current is compared to a series of switched trial currents. The comparison point is diode clamped but may vary by several hundred millivolts, resulting in high frequency modulation of the A/D input current. The output impedance of a feedback amplifier is made artificially low by its loop gain. At high frequencies, where the loop gain is low, the amplifier output impedance can approach its open loop value.

Most IC amplifiers exhibit a minimum open loop output impedance of 25Ω, due to current limiting resistors. A few hundred microamps reflected from the change in converter loading can introduce errors in instantaneous input voltage. If the A/D conversion speed is not excessive and the bandwidth of the amplifier is sufficient, the amplifier's output will return to the nominal value before the converter makes its comparison. However, many amplifiers have relatively narrow bandwidths, yielding slow recovery from output transients. The AD713 is ideally suited as a driver for A/D converters since it offers both a wide bandwidth and a high open loop gain.

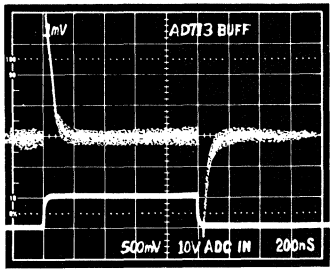


Figure 34. Buffer Recovery Time Source Current = 2mA

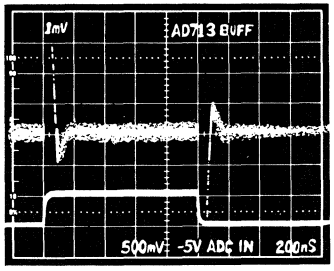


Figure 35. Buffer Recovery Time Sink Current = 1mA

Driving A Large Capacitive Load

The circuit of Figure 36 employs a 100Ω isolation resistor which enables the amplifier to drive capacitive loads exceeding 1500pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 100Ω series resistor and the load capacitance, Cl. Figure 37 shows a typical transient response for this connection.

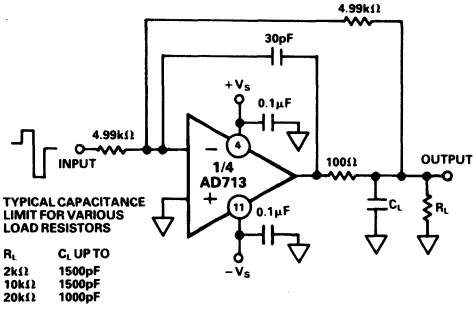


Figure 36. Circuit for Driving a Large Capacitance Load

Trim Resistor	JN/AQ/ SD	KN/BQ/ TD	LN/CQ/ UD	GLN/GCQ/ GUD
R1	500Ω	200Ω	100Ω	20Ω
R2	150Ω	68Ω	33Ω	6.8Ω

Table II. Recommended Trim Resistor Values vs. Grades for AD7545 for V_D = +5V

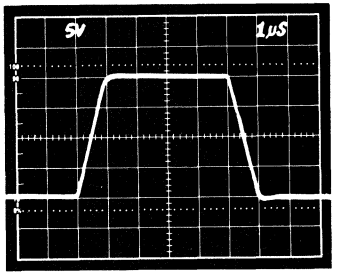


Figure 37. Transient Response, R_L = 2kΩ, C_L = 500pF

CMOS DAC APPLICATIONS

The AD713 is an excellent output amplifier for CMOS DACs. It can be used to perform both 2 and 4 quadrant operation. The output impedance of a DAC using an inverted R-2R ladder approaches R for codes containing many "1"s, 3R for codes containing a single "1" and infinity for codes containing all zeros.

For example, the output resistance of the AD7545 will modulate between 11kΩ and 33kΩ. Therefore, with the DAC's internal feedback resistance of 11kΩ , the noise gain will vary from 2 to 4/3. This changing noise gain modulates the effect of the input offset voltage of the amplifier, resulting in nonlinear DAC-amplifier performance. The AD713, with its guaranteed 1.5mV input offset voltage, minimizes this effect achieving 12-bit performance.

Figures 38 and 39 show the AD713 and a 12-bit CMOS DAC, the AD7545, configured for either a unipolar binary (2-quadrant multiplication) or bipolar (4-quadrant multiplication) operation. Capacitor C1 provides phase compensation which reduces overshoot and ringing.

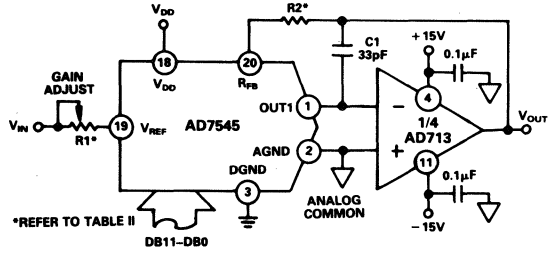


Figure 38. Unipolar Binary Operation

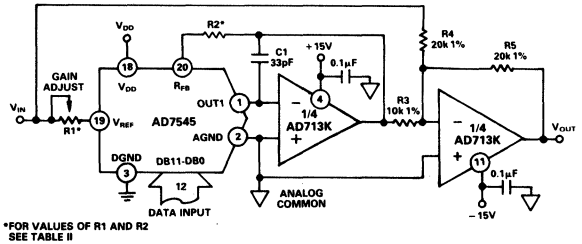
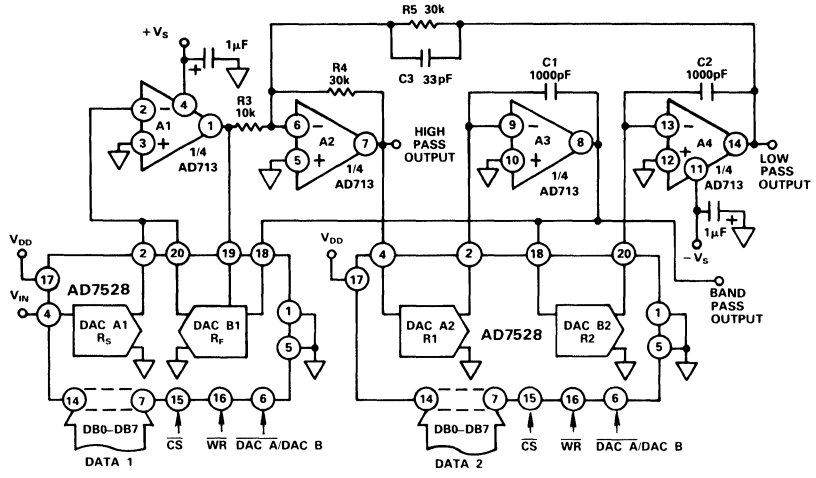


Figure 39. Bipolar Operation



CIRCUIT EQUATIONS

$C_1 = C_2$, $R_1 = R_2$, $R_4 = R_5$

$$f_C = \frac{1}{2\pi R_1 C_1}$$

$$Q = \frac{R_3}{R_4} \cdot \frac{R_F}{R_{FBB1}}$$

$$A_O = -\frac{R_F}{R_S}$$

Note:
DAC equivalent resistance equals
256 × (DAC Ladder resistance) / DAC Digital Code

Figure 40. A Programmable State Variable Filter Circuit

FILTER APPLICATIONS

A Programmable State Variable Filter

For the state variable or universal filter configuration of Figure 40 to function properly, DACs A1 and B1 need to control the gain and Q of the filter characteristic, while DACs A2 and B2 must accurately track for the simple expression of f_C to be true. This is readily accomplished using two AD7528 DACs and one AD713 quad op amp. Capacitor C3 compensates for the effects of op amp gain-bandwidth limitations.

This filter provides low pass, high pass and band pass outputs and is ideally suited for applications where microprocessor control of filter parameters is required. The programmable range for component values shown is f_C = 0 to 15kHz and Q = 0.3 to 4.5.

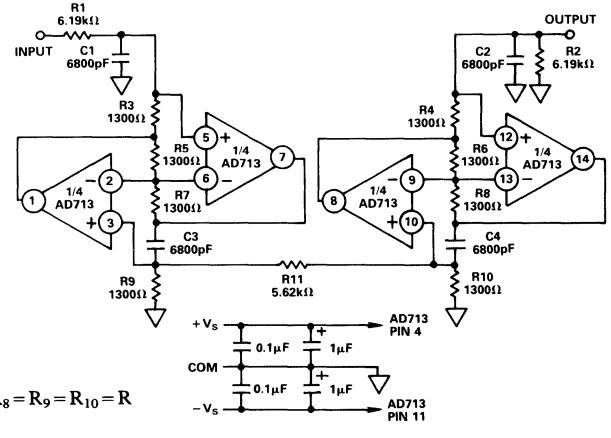
GIC and FDNR FILTER APPLICATIONS

The closely matched and uniform ac characteristics of the AD713 make it ideal for use in GIC (gyrator) and FDNR (frequency dependent negative resistor) filter applications. Figures 41 and 43 show the AD713 used in two typical active filters. The first shows a single AD713 simulating two coupled inductors configured as a one-third octave bandpass filter. A single section of this filter meets ANSI class II specifications and handles a 7.07V rms signal with <0.002% THD (20Hz-20kHz).

Figure 43 shows a 7-pole antialiasing filter for a 2× oversampling (88.2kHz) digital audio application. This filter has <0.05 dB pass band ripple and 19.8 ±0.3µs delay, dc-20kHz and will handle a 5V rms signal (V_S = ±15V) with no overload at any internal nodes.

The filter of Figure 41 can be scaled for any center frequency by using the formula:

$$f_C = \frac{1.11}{2\pi RC}$$



$$f_c = \frac{1.11}{2\pi RC}$$

$C_1 = C_2 = C_3 = C_4 = C$

$R_1 = R_2 = 4.76R$

$R_{11} = 4.32R$

$R_3 = R_4 = R_5 = R_6 = R_7 = R_8 = R_9 = R_{10} = R$

Figure 41. A 1/3 Octave Filter Circuit

where all resistors and capacitors scale equally. Resistors R3—R8 should not be greater than 2kΩ in value, to prevent parasitic oscillations caused by the amplifier's input capacitance.

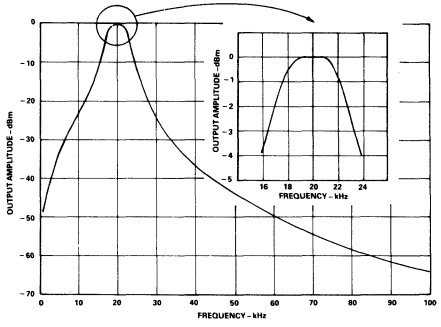


Figure 42. Output Amplitude vs. Frequency of 1/3 Octave Filter

If this is not practical, small lead capacitances (10-20pF) should be added across R5 and R6. Figures 42 and 44 show the output amplitude vs. frequency of these filters.

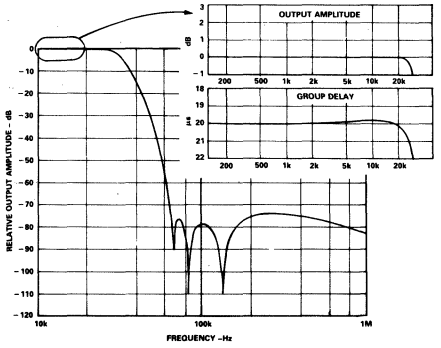


Figure 44. Relative Output Amplitude vs. Frequency of Antialiasing Filter

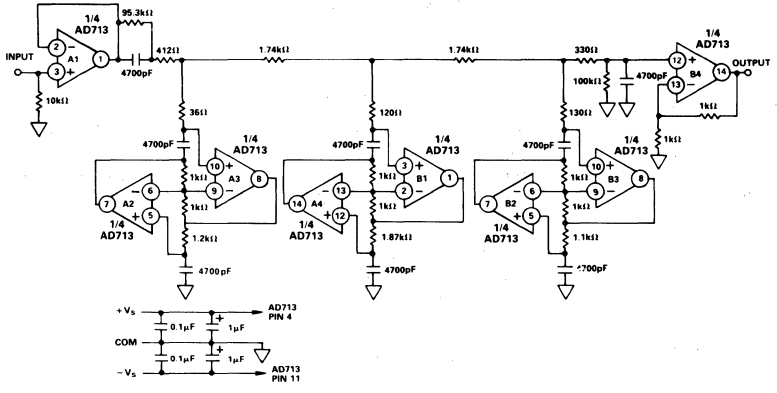


Figure 43. An Antialiasing Filter

ANALOG DEVICES

High Performance Video Op Amp

AD811

FEATURES

High Speed
- 140 MHz Bandwidth (3 dB, G = +1)
- 120 MHz Bandwidth (3 dB, G = +2)
- 35 MHz Bandwidth (0.1 dB, G = +2)
- 2500 V/μs Slew Rate
- 25 ns Settling Time to 0.1% (For a 2 V Step)
- 65 ns Settling Time to 0.01% (For a 10 V Step)

Excellent Video Performance (R_L = 150 Ω)
- 0.01% Differential Gain, 0.01° Differential Phase
- Voltage Noise of 1.9 nV/√Hz

Low Distortion: THD = −74 dB @ 10 MHz

Excellent DC Precision
- 3 mV max Input Offset Voltage

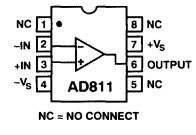
Flexible Operation
- Specified for ±5 V and ±15 V Operation
- ±2.3 V Output Swing into a 75 Ω Load (V_S = ±5 V)

APPLICATIONS

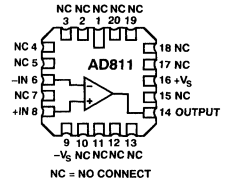
Video Crosspoint Switchers, Multimedia Broadcast Systems
HDTV Compatible Systems
Video Line Drivers, Distribution Amplifiers
ADC/DAC Buffers
DC Restoration Circuits
Medical—Ultrasound, PET, Gamma & Counter Applications

CONNECTION DIAGRAMS

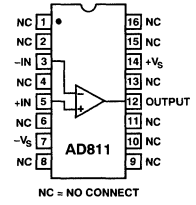
8-Pin Plastic (N-8) and Cerdip (Q-8) Packages



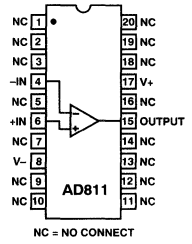
20-Pin LCC (E-20A) Package



16-Pin SOIC (R-16) Package



20-Pin SOIC (R-20) Package

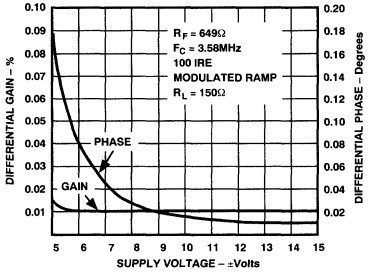


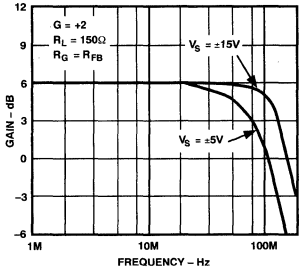
PRODUCT DESCRIPTION

The AD811 is a wideband current-feedback operational amplifier, optimized for broadcast quality video systems. The −3 dB bandwidth of 120 MHz at a gain of +2 and differential gain and phase of 0.01% and 0.01° (R_L = 150 Ω) make the AD811 an excellent choice for all video systems. The AD811 is designed to meet a stringent 0.1 dB gain flatness specification to a bandwidth of 35 MHz (G = +2) in addition to the low differential gain and phase errors. This performance is achieved whether driving one or two back terminated 75 Ω cables, with a low power supply current of 16.5 mA. Furthermore, the AD811 is specified over a power supply range of ±4.5 V to ±18 V.

The AD811 is also excellent for pulsed applications where transient response is critical. It can achieve a maximum slew rate of greater than 2500 V/μs with a settling time of less than 25 ns to 0.1% on a 2 volt step and 65 ns to 0.01% on a 10 volt step.

The AD811 is ideal as an ADC or DAC buffer in data acquisition systems due to its low distortion up to 10 MHz and its wide unity gain bandwidth. Because the AD811 is a current feedback amplifier, this bandwidth can be maintained over a wide range of gains. The AD811 also offers low voltage and current noise of 1.9 nV/√Hz and 20 pA/√Hz, respectively, and excellent dc accuracy for wide dynamic range applications.





This is an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

AD811—SPECIFICATIONS (@ T_A = +25°C and V_S = ±15 V dc, R_{LOAD} = 150 Ω unless otherwise noted)

Model	Conditions	V_S	AD811A Min	AD811A Typ	AD811A Max	AD811S[1] Min	AD811S[1] Typ	AD811S[1] Max	Units
DYNAMIC PERFORMANCE									
Small Signal Bandwidth (No Peaking)									
−3 dB									
G = +1	R_{FB} = 562 Ω	±15 V		140			140		MHz
G = +2	R_{FB} = 649 Ω	±15 V		120			120		MHz
G = +2	R_{FB} = 562 Ω	±5 V		80			80		MHz
G = +10	R_{FB} = 511 Ω	±15 V		100			100		MHz
0.1 dB Flat									
G = +2	R_{FB} = 562 Ω	±5 V		25			25		MHz
	R_{FB} = 649 Ω	±15 V		35			35		MHz
Full Power Bandwidth[2]	V_{OUT} = 20 V p–p	±15 V		40			40		MHz
Slew Rate	V_{OUT} = 4 V p–p	±5 V		400			400		V/μs
	V_{OUT} = 20 V p–p	±15 V		2500			2500		V/μs
Settling Time to 0.1%	10 V Step, A_V = −1	±15 V		50			50		ns
Settling Time to 0.01%				65			65		ns
Settling Time to 0.1%	2 V Step, A_V = −1	±5 V		25			25		ns
Rise Time, Fall Time	R_{FB} = 649, A_V = +2	±15 V		3.5			3.5		ns
Differential Gain	f = 3.58 MHz	±15 V		0.01			0.01		%
Differential Phase	f = 3.58 MHz	±15 V		0.01			0.01		Degree
THD @ f_C = 10 MHz	V_{OUT} = 2 V p–p, A_V = +2	±15 V		−74			−74		dBc
Third Order Intercept[3]	@ f_C = 10 MHz	±5 V		36			36		dBm
		±15 V		43			43		dBm
INPUT OFFSET VOLTAGE		±5 V, ±15 V		0.5	3		0.5	3	mV
	T_{MIN} to T_{MAX}				5			5	mV
Offset Voltage Drift				5			5		μV/°C
INPUT BIAS CURRENT									
−Input		±5 V, ±15 V		2	5		2	5	μA
	T_{MIN} to T_{MAX}				15			30	μA
+Input		±5 V, ±15 V		2	10		2	10	μA
	T_{MIN} to T_{MAX}				20			25	μA
TRANSRESISTANCE	T_{MIN}–T_{MAX}								
	V_{OUT} = ±10 V								
	R_L = ∞	±15 V	0.75	1.5		0.75	1.5		MΩ
	R_L = 200 Ω	±15 V	0.5	0.75		0.5	0.75		MΩ
	V_{OUT} = ±2.5 V								
	R_L = 150 Ω	±5 V	0.25	0.4		0.125	0.4		MΩ
COMMON-MODE REJECTION									
V_{OS} (vs. Common Mode)									
T_{MIN}–T_{MAX}	V_{CM} = ±2.5	±5 V	56	60		50	60		dB
T_{MIN}–T_{MAX}	V_{CM} = ±10 V	±15 V	60	66		56	66		dB
Input Current (vs. Common Mode)	T_{MIN}–T_{MAX}			1	3		1	3	μA/V
POWER SUPPLY REJECTION	V_S = ±4.5 V to ±18 V								
V_{OS}	T_{MIN}–T_{MAX}		60	70		60	70		dB
+Input Current	T_{MIN}–T_{MAX}			0.3	2		0.3	2	μA/V
−Input Current	T_{MIN}–T_{MAX}			0.4	2		0.4	2	μA/V
INPUT VOLTAGE NOISE	f = 1 kHz			1.9			1.9		nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz			20			20		pA/√Hz
OUTPUT CHARACTERISTICS									
Voltage Swing, Useful Operating Range[4]		±5 V		±2.9			±2.9		V
		±15 V		±12			±12		V
Output Current	T_J = +25°C			100			100		mA
Short-Circuit Current				150			150		mA
Output Resistance	(Open Loop @ 5 MHz)			11			11		Ω
INPUT CHARACTERISTICS									
+Input Resistance				1.5			1.5		MΩ
−Input Resistance				14			14		Ω
Input Capacitance	+Input			7.5			7.5		pF
Common-Mode Voltage Range		±5 V		±3			±3		V
		±15 V		±13			±13		V
POWER SUPPLY									
Operating Range			±4.5		±18	±4.5		±18	V
Quiescent Current		±5 V		14.5	16.0		14.5	16.0	mA
		±15 V		16.5	18.0		16.5	18.0	mA
TRANSISTOR COUNT	# of Transistors			40			40		

NOTES

[1]See Analog Devices' military data sheet for 883B tested specifications.

[2]FPBW = slew rate/(2 π V_{PEAK})

[3]Output power level, tested at a closed loop gain of two.

[4]Useful operating range is defined as the output voltage at which linearity begins to degrade.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . Observe Derating Curves
Output Short Circuit Duration . . . . . Observe Derating Curves
Common-Mode Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N) . . . . . −65°C to +125°C
Storage Temperature Range (R) . . . . . −65°C to +125°C
Operating Temperature Range
AD811A . . . . . −40°C to +85°C
AD811S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]8-Pin Plastic Package: θ_{JA} = 90°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt
16-Pin SOIC Package: θ_{JA} = 85°C/Watt
20-Pin SOIC Package: θ_{JA} = 80°C/Watt
20-Pin LCC Package: θ_{JA} = 70°C/Watt

ORDERING GUIDE

Model	Temperature Range	Package*
AD811AN	−40°C to +85°C	N-8
AD811AR-16	−40°C to +85°C	R-16
AD811AR-20	−40°C to +85°C	R-20
AD811SQ/883B	−55°C to +125°C	Q-8
AD811SE/883B	−55°C to +125°C	E-20A
AD811ACHIPS	−40°C to +85°C	Die
AD811SCHIPS	−55°C to +125°C	Die

*E = Ceramic Leadless Chip Carrier; N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD811 is limited by the associated rise in junction temperature. For the plastic packages, the maximum safe junction temperature is 145°C. For the cerdip and LCC packages, the maximum junction temperature is 175°C. If these maximums are exceeded momentarily, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the device in the "overheated" condition for an extended period can result in device burnout. To ensure proper operation, it is important to observe the derating curves in Figures 17 and 18.

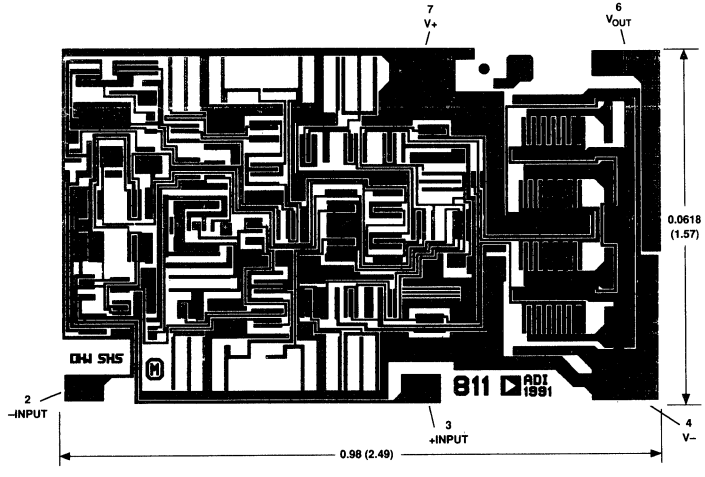
While the AD811 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions. One important example is when the amplifier is driving a reverse terminated 75 Ω cable and the cable's far end is shorted to a power supply. With power supplies of ±12 volts (or less) at an ambient temperature of +25°C or less, if the cable is shorted to a supply rail, then the amplifier will not be destroyed, even if this condition persists for an extended period.

ESD SUSCEPTIBILITY

An ESD classification per method 3015.6 of MIL-STD-883C has been performed on the AD811, which is a Class 2 device. Using an IMCS 5000 automated ESD tester, all pins will pass at voltages up to and including 3,000 volts.

METALIZATION PHOTOGRAPH

Contact Factory for Latest Dimensions.
Dimensions Shown in Inches and (mm).



AD811—Typical Characteristics

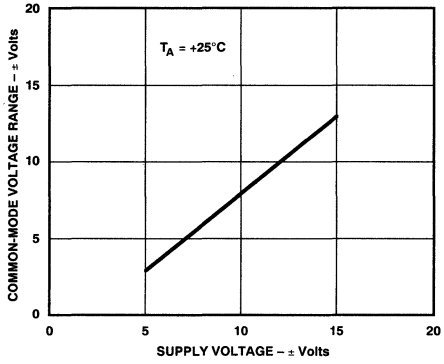


Figure 1. Input Common-Mode Voltage Range vs. Supply

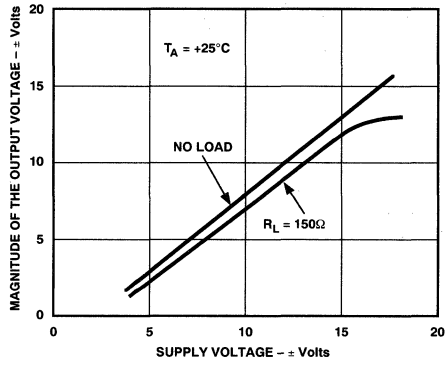


Figure 2. Output Voltage Swing vs. Supply

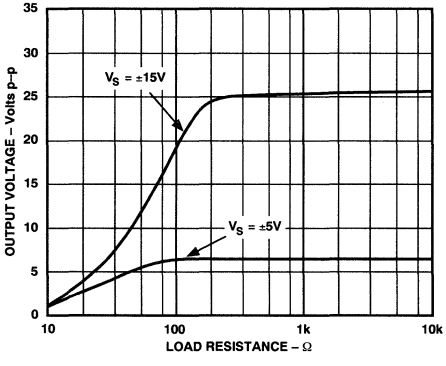


Figure 3. Output Voltage Swing vs. Resistive Load

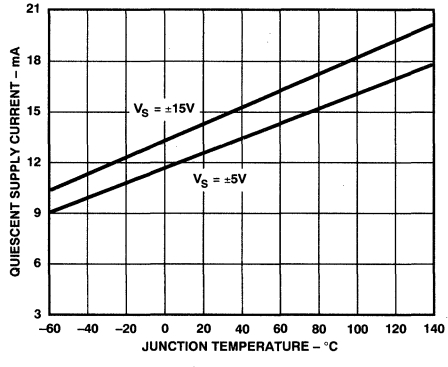


Figure 4. Quiescent Supply Current vs. Junction Temperature

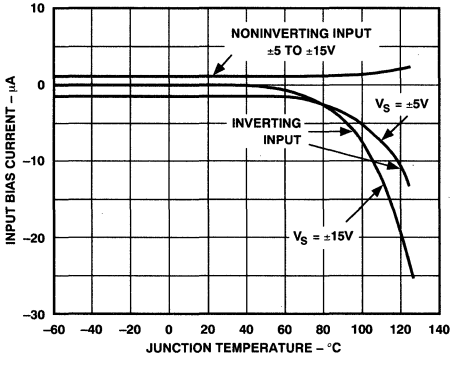


Figure 5. Input Bias Current vs. Junction Temperature

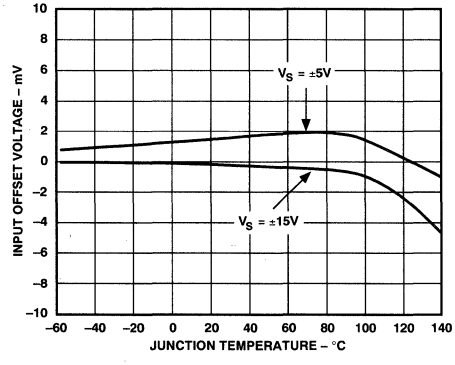


Figure 6. Input Offset Voltage vs. Junction Temperature

High Speed, Low Power Dual Op Amp

AD827

FEATURES

HIGH SPEED
50 MHz Unity Gain Stable Operation
300 V/μs Slew Rate
120 ns Settling Time
Drives Unlimited Capacitive Loads

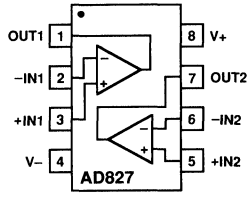
EXCELLENT VIDEO PERFORMANCE
0.04% Differential Gain @ 4.4 MHz
0.19° Differential Phase @ 4.4 MHz

GOOD DC PERFORMANCE
2 mV max Input Offset Voltage
15 μV/°C Input Offset Voltage Drift

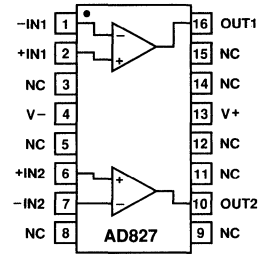
LOW POWER
Only 10 mA Total Supply Current for Both Amplifiers
±5 V to ±15 V Supplies

CONNECTION DIAGRAMS

8-Pin Plastic (N) and Cerdip (Q) Packages



16-Pin Small Outline (R) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD827 is a dual version of Analog Devices' industry-standard AD847 op amp. Like the AD847, it provides high speed, low power performance at low cost. The AD827 achieves a 300 V/μs slew rate and 50 MHz unity-gain bandwidth while consuming only 100 mW when operating from ±5 volt power supplies. Performance is specified for operation using ±5 V to ±15 V power supplies.

The AD827 offers an open-loop gain of 3,500 V/V into 500 Ω loads. It also features a low input voltage noise of 15 nV/$\sqrt{\text{Hz}}$, and a low input offset voltage of 2 mV maximum. Common-mode rejection ratio is a minimum of 80 dB. Power supply rejection ratio is maintained at better than 20 dB with input frequencies as high as 1 MHz, thus minimizing noise feedthrough from switching power supplies.

The AD827 is also ideal for use in demanding video applications, driving coaxial cables with less than 0.04% differential gain and 0.19° differential phase errors for 643 mV p–p into a 75 Ω reverse terminated cable.

The AD827 is also useful in multichannel, high speed data conversion systems where its fast (120 ns to 0.1%) settling time is of importance. In such applications, the AD827 serves as an input buffer for 8-bit to 10-bit A/D converters and as an output amplifier for high speed D/A converters.

APPLICATION HIGHLIGHTS

1. Performance is fully specified for operation using ±5 V to ±15 V supplies.
2. A 0.04% differential gain and 0.19° differential phase error at the 4.4 MHz color subcarrier frequency, together with its low cost, make it ideal for many video applications.
3. The AD827 can drive unlimited capacitive loads, while its 30 mA output current allows 50 Ω and 75 Ω reverse-terminated loads to be driven.
4. The AD827's 50 MHz unity-gain bandwidth makes it an ideal candidate for multistage active filters.
5. The AD827 is available in 8-pin plastic mini-DIP, cerdip, and 16-pin SOIC packages. Chips and MIL-STD-883B processing are also available.

AD827—SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Model	Conditions	V_S	AD827J Min	AD827J Typ	AD827J Max	AD827A/S Min	AD827A/S Typ	AD827A/S Max	Units
DC PERFORMANCE									
Input Offset Voltage[1]		±5 V		0.5	2		0.3	2	mV
	T_{min} to T_{max}				3.5			4	mV
		±15 V			4			4	mV
	T_{min} to T_{max}				6			6	mV
Offset Voltage Drift		±5 V to ±15 V		15			15		µV/°C
Input Bias Current		±5 V to ±15 V		3.3	7		3.3	7	µA
	T_{min} to T_{max}				8.2			9.5	µA
Input Offset Current		±5 V to ±15 V		50	300		50	300	nA
	T_{min} to T_{max}				400			400	nA
Offset Current Drift		±5 V to ±15 V		0.5			0.5		nA/°C
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V	±5 V	78	95		80	95		dB
	V_{CM} = ±12 V	±15 V	78	95		80	95		dB
	T_{min} to T_{max}	±5 V to ±15 V	75			75			dB
Power Supply Rejection Ratio		±5 V to ±15 V	75	86		75	86		dB
	T_{min} to T_{max}		72			72			dB
Open-Loop Gain									
	V_O = ±2.5 V	±5 V							
	R_{LOAD} = 500 Ω		2	3.5		2	3.5		V/mV
	T_{min} to T_{max}		1			1			V/mV
	R_{LOAD} = 150 Ω			1.6			1.6		V/mV
	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 1 kΩ		3	5.5		3	5.5		V/mV
	T_{min} to T_{max}		1.5			1.5			V/mV
MATCHING CHARACTERISTICS									
Input Offset Voltage		±5 V		0.4			0.2		mV
Crosstalk	f = 5 MHz	±5 V		85			85		dB
DYNAMIC PERFORMANCE									
Unity-Gain Bandwidth		±5 V		35			35		MHz
		±15 V		50			50		MHz
Full Power Bandwidth[2]	V_O = 5 V p-p,								
	R_{LOAD} = 500 Ω	±5 V		12.7			12.7		MHz
	V_O = 20 V p-p,								
	R_{LOAD} = 1 kΩ	±15 V		4.7			4.7		MHz
Slew Rate[3]	R_{LOAD} = 500 Ω	±5 V		200			200		V/µs
	R_{LOAD} = 1 kΩ	±15 V		300			300		V/µs
Settling Time to 0.1%	A_V = −1								
	−2.5 V to +2.5 V	±5 V		65			65		ns
	−5 V to +5 V	±15 V		120			120		ns
Phase Margin	C_{LOAD} = 10 pF	±15 V							
	R_{LOAD} = 1 kΩ			50			50		Degrees
Differential Gain Error	f = 4.4 MHz	±15 V		0.04			0.04		%
Differential Phase Error	f = 4.4 MHz	±15 V		0.19			0.19		Degrees
Input Voltage Noise	f = 10 kHz	±15 V		15			15		nV/√Hz
Input Current Noise	f = 10 kHz	±15 V		1.5			1.5		pA/√Hz
Input Common-Mode Voltage Range		±5 V		+4.3			+4.3		V
				−3.4			−3.4		V
		±15 V		+14.3			+14.3		V
				−13.4			−13.4		V
Output Voltage Swing	R_{LOAD} = 500 Ω	±5 V	3.0	3.6		3.0	3.6		±V
	R_{LOAD} = 150 Ω	±5 V	2.5	3.0		2.5	3.0		±V
	R_{LOAD} = 1 kΩ	±15 V	12	13.3		12	13.3		±V
	R_{LOAD} = 500 Ω	±15 V	10	12.2		10	12.2		±V
Short-Circuit Current Limit		±5 V to ±15 V		32			32		mA
INPUT CHARACTERISTICS									
Input Resistance				300			300		kΩ
Input Capacitance				1.5			1.5		pF
OUTPUT RESISTANCE	Open Loop			15			15		Ω

Model	Conditions	V_S	AD827J Min	AD827J Typ	AD827J Max	AD827A/S Min	AD827A/S Typ	AD827A/S Max	Units
POWER SUPPLY									
Operating Range			±4.5		±18	±4.5		±18	V
Quiescent Current		±5 V		10	13		10	13	mA
	T_{min} to T_{max}				16			16.5/17.5	mA
		±15 V		10.5	13.5		10.5	13.5	mA
	T_{min} to T_{max}				16.5			17/18	mA
TRANSISTOR COUNT				92			92		

NOTES
[1]Offset voltage for the AD827 is guaranteed after power is applied and the device is fully warmed up. All other specifications are measured using high speed test equipment, approximately 1 second after power is applied.
[2]Full Power Bandwidth = Slew Rate/2π V_{PEAK}.
[3]Gain = +1, rising edge.

All min and max specifications are guaranteed.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) Package (Derate at 10 mW/°C) . . . . . 1.5 W
Cerdip (Q) Package (Derate at 8.7 mW/°C) . . . . . 1.3 W
Small Outline (R) Package (Derate at 10 mW/°C) . . . . 1.5 W
Input Common Mode Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . 6 V
Output Short Circuit Duration[3] . . . . . Indefinite
Storage Temperature Range N, R . . . . . −65°C to +125°C
Storage Temperature Range Q . . . . . −65°C to +150°C
Operating Temperature Range
AD827J . . . . . 0 to +70°C
AD827A . . . . . −40°C to +85°C
AD827S . . . . . −55°C to +125°C
Lead Temperature Range
(Soldering to 60 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C. Thermal Characteristics:
Mini-DIP: θ_{JA} = 100°C/Watt, θ_{JC} = 33°C/Watt
Cerdip: θ_{JA} = 110°C/Watt, θ_{JC} = 30°C/Watt
16-Pin Small Outline Package: θ_{JA} = 100°C/Watt
[3]Indefinite short circuit duration is only permissible as long as the absolute maximum power rating is not exceeded.

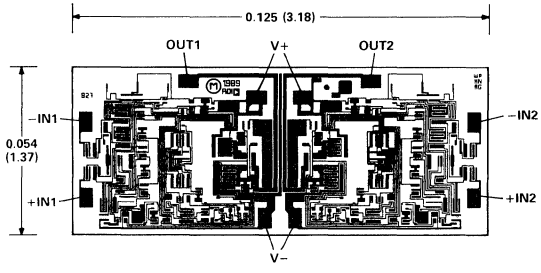
ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
AD827JN	0 to +70°C	N-8
AD827JR	0 to +70°C	R-16
AD827AQ	−40°C to +85°C	Q-8
AD827SQ	−55°C to +125°C	Q-8
AD827SQ/883B	−55°C to +125°C	Q-8

NOTES
[1]"J" and"S" chips also available.
[2]N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).
Substrate is connected to V+.



AD827—Typical Characteristics (@ +25°C & ±15 V, unless otherwise noted)

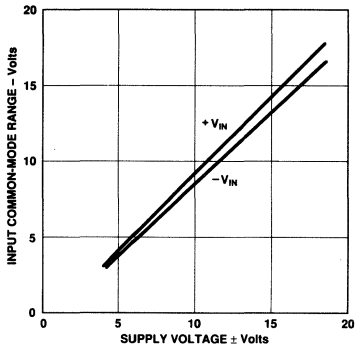


Figure 1. Input Common-Mode Range vs. Supply Voltage

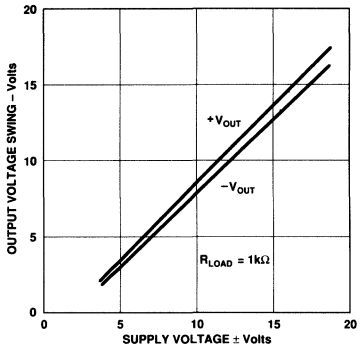


Figure 2. Output Voltage Swing vs. Supply Voltage

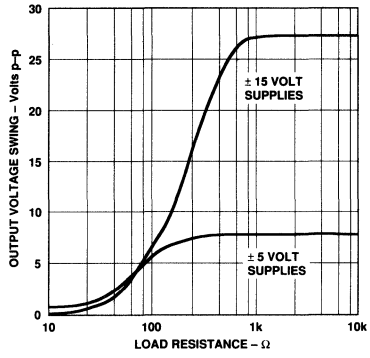


Figure 3. Output Voltage Swing vs. Load Resistance

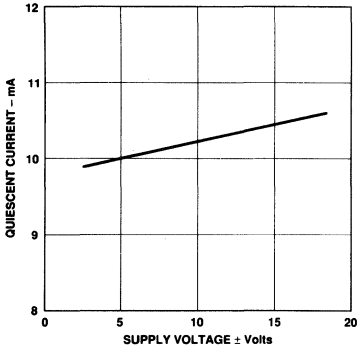


Figure 4. Quiescent Current vs. Supply Voltage

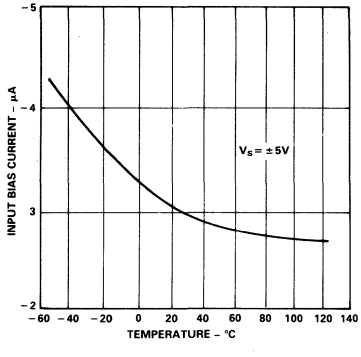


Figure 5. Input Bias Current vs. Temperature

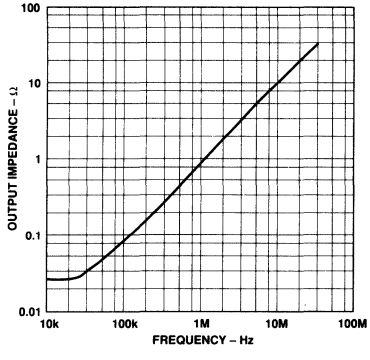


Figure 6. Closed-Loop Output Impedance vs. Frequency, Gain = +1

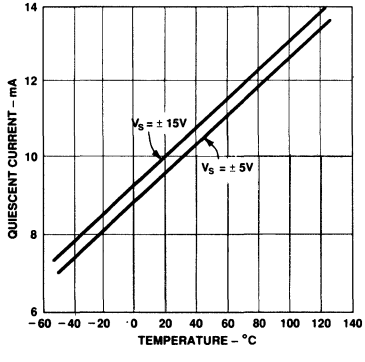


Figure 7. Quiescent Current vs. Temperature

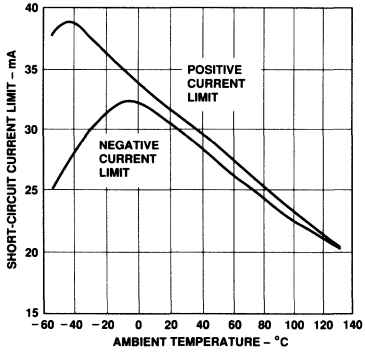


Figure 8. Short-Circuit Current Limit vs. Temperature

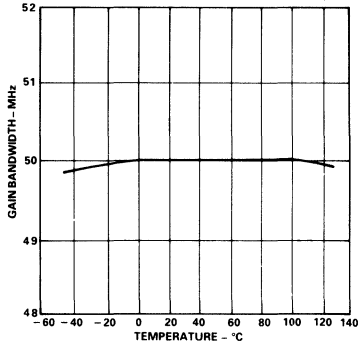


Figure 9. Gain Bandwidth vs. Temperature

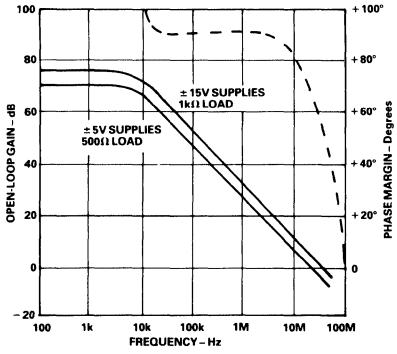


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

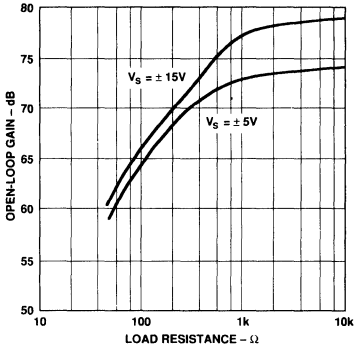


Figure 11. Open-Loop Gain vs. Load Resistance

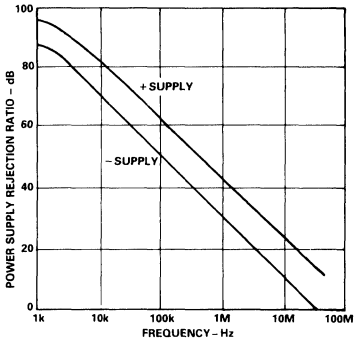


Figure 12. Power Supply Rejection Ratio vs. Frequency

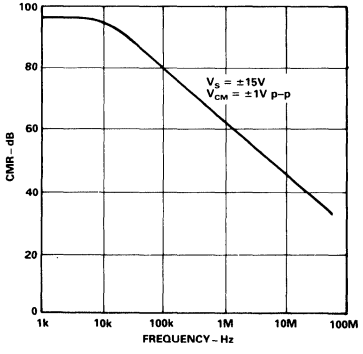


Figure 13. Common-Mode Rejection Ratio vs. Frequency

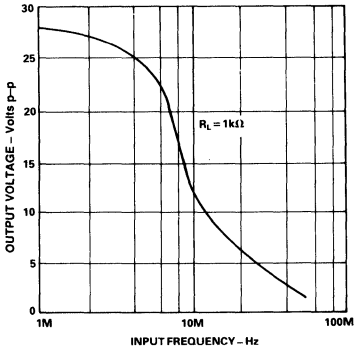


Figure 14. Large Signal Frequency Response

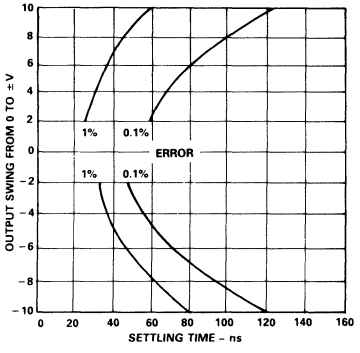


Figure 15. Output Swing and Error vs. Settling Time

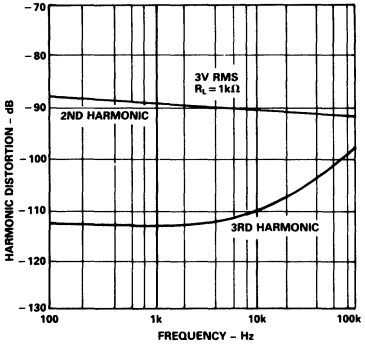


Figure 16. Harmonic Distortion vs. Frequency

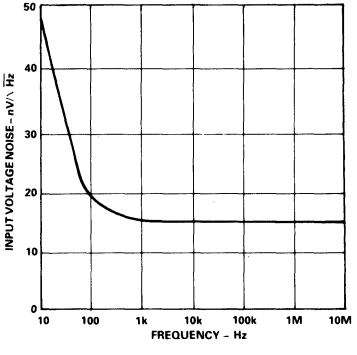


Figure 17. Input Voltage Noise Spectral Density

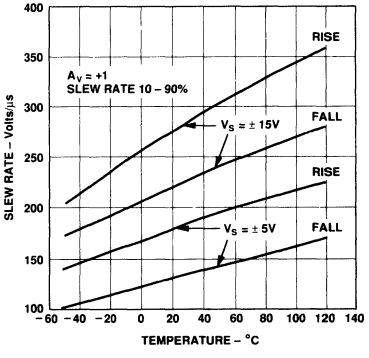


Figure 18. Slew Rate vs. Temperature

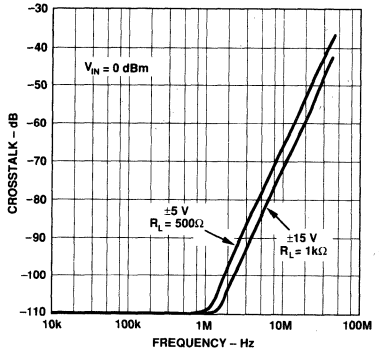


Figure 19. Crosstalk vs. Frequency

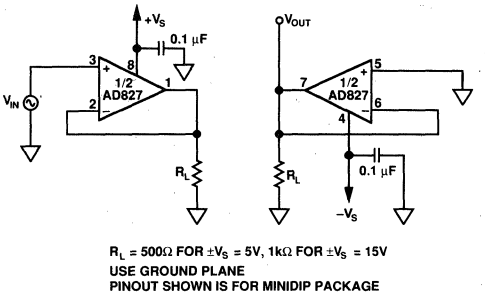


Figure 20. Crosstalk Test Circuit

INPUT PROTECTION PRECAUTIONS

An input resistor (resistor R_{IN} of Figure 21a) is recommended in circuits where the input common-mode voltage to the AD827 may exceed (on a transient basis) the positive supply voltage. This resistor provides protection for the input transistors by limiting the maximum current that can be forced into their bases.

For high performance circuits, it is recommended that a second resistor (R_B in Figures 21a and 22a) be used to reduce bias-current errors by matching the impedance at each input. This resistor reduces the error caused by offset voltages by more than an order of magnitude.

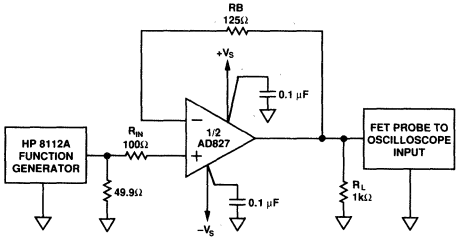


Figure 21a. Follower Connection

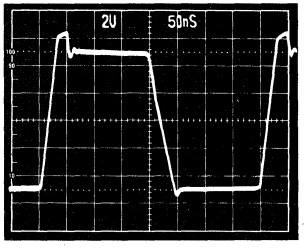


Figure 21b. Follower Large Signal Pulse Response

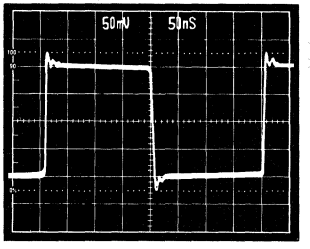


Figure 21c. Follower Small Signal Pulse Response

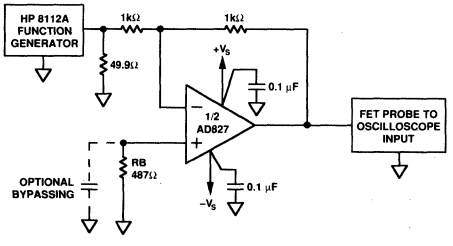


Figure 22a. Inverter Connection

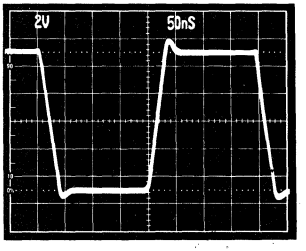


Figure 22b. Inverter Large Signal Pulse Response

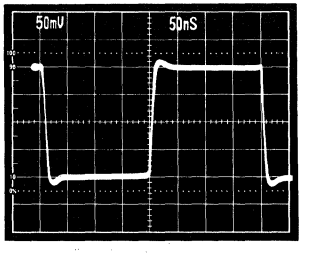


Figure 22c. Inverter Small Signal Pulse Response

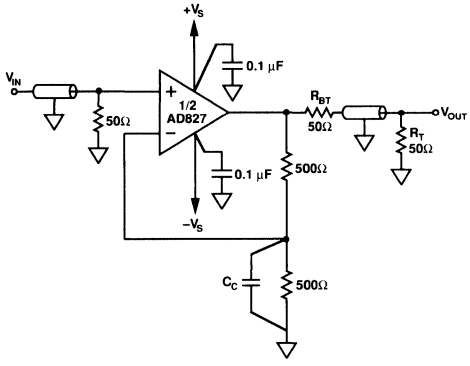


Figure 23. A Video Line Driver

VIDEO LINE DRIVER

The AD827 functions very well as a low cost, high speed line driver for either terminated or unterminated cables. Figure 23 shows the AD827 driving a doubly terminated cable in a follower configuration.

The termination resistor, R_T, (when equal to the cable's characteristic impedance) minimizes reflections from the far end of the cable. While operating from ±5 V supplies, the AD827 maintains a typical slew rate of 200 V/µs, which means it can drive a ±1 V, 30 MHz signal into a terminated cable.

Video Line Driver Performance Summary

V_{IN}*	V_{SUPPLY}	C_C	−3 dB B_W	Overshoot
0 dB or ±500 mV Step	±15	20 pF	23 MHz	4%
0 dB or ±500 mV Step	±15	15 pF	21 MHz	0%
0 dB or ±500 mV Step	±15	0 pF	13 MHz	0%
0 dB or ±500 mV Step	±5	20 pF	18 MHz	2%
0 dB or ±500 mV Step	±5	15 pF	16 MHz	0%
0 dB or ±500 mV Step	±5	0 pF	11 MHz	0%

NOTE
*−3 dB bandwidth numbers are for the 0 dBm signal input. Overshoot numbers are the percent overshoot of the 1 Volt step input.

Table I. Video Line Driver Performance Chart

A back-termination resistor (R_{BT}, also equal to the characteristic impedance of the cable) may be placed between the AD827 output and the cable input, in order to damp any reflected signals caused by a mismatch between R_T and the cable's characteristic impedance. This will result in a flatter frequency response, although this requires that the op amp supply ±2 V to the output in order to achieve a ±1 V swing at resistor R_T.

A HIGH SPEED 3 OP AMP INSTRUMENTATION AMPLIFIER CIRCUIT

The instrumentation amplifier circuit shown in Figure 24 can provide a range of gains. The chart of Table II details performance.

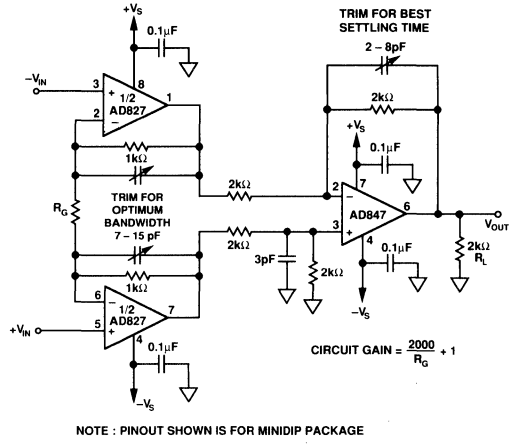


Figure 24. A High Bandwidth Three Op Amp Instrumentation Amplifier

Gain	R_G	Small Signal Bandwidth @ 1 V p–p Output
1	Open	16.1 MHz
2	2 k	14.7 MHz
10	226 Ω	4.9 MHz
100	20 Ω	660 kHz

Table II. Performance Specifications for the Three Op Amp Instrumentation Amplifier

A TWO-CHIP VOLTAGE-CONTROLLED AMPLIFIER (VCA) WITH EXPONENTIAL RESPONSE

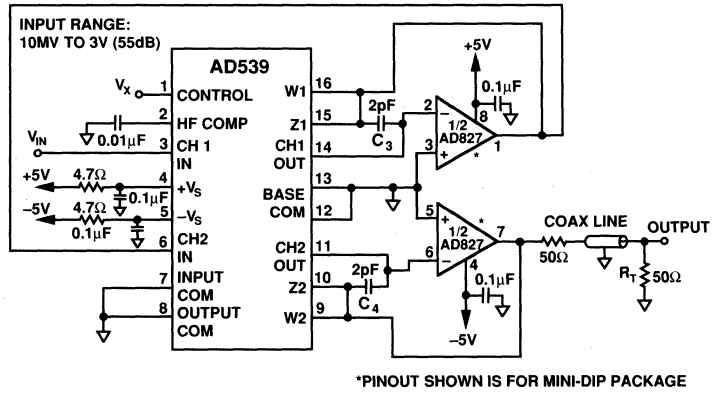
Voltage-controlled amplifiers are often used as building blocks in automatic gain control systems. Figure 25 shows a two-chip VCA built using the AD827 and the AD539, a dual, current-output multiplier. As configured, the circuit has its two multipliers connected in series. They could also be placed in parallel with an increase in bandwidth and a reduction in gain. The gain of the circuit is controlled by V_X, which can range from 0 to 3 V dc. Measurements show that this circuit easily supplies 2 V p–p into a 100 Ω load while operating from ±5 V supplies. The overall bandwidth of the circuit is approximately 7 MHz with 0.5 dB of peaking.

Each half of the AD827 serves as an I/V converter and converts the output current of one of the two multipliers in the AD539 into an output voltage. Each of the AD539's two multipliers contains two internal 6 kΩ feedback resistors; one is connected between the CH1 output and Z1, the other between the CH1 output and W1. Likewise, in the CH2 multiplier, one of the feedback resistors is connected between CH2 and Z2 and the other is connected between CH2 and Z2. In Figure 25, Z1 and W1 are tied together, as are Z2 and W2, providing a 3 kΩ feedback resistor for the op amp. The 2 pF capacitors connected between the AD539's W1 and CH1 and W2 and CH2 pins are in parallel with the feedback resistors and thus reduce peaking in the VCA's frequency response. Increasing the values of C3 and C4 can further reduce the peaking at the expense of reduced bandwidth. The 1.25 mA full-scale output current of the AD539 and the 3 kΩ feedback resistor set the full-scale output voltage of each multiplier at 3.25 V p–p.

Current limiting in the AD827 (typically 30 mA) limits the output voltage in this application to about 3 V p–p across a 100 Ω load. Driving a 50 Ω reverse-terminated load divides this value by two, limiting the maximum signal delivered to a 50 Ω load to about 1.5 V p–p, which suffices for video signal levels. The dynamic range of this circuit is approximately 55 dB and is primarily limited by feedthrough at low input levels and by the maximum output voltage at high levels.

Guidelines for Grounding and Bypassing

When designing practical high frequency circuits using the AD827, some special precautions are in order. Both short interconnection leads and a large ground plane are needed whenever possible to provide low resistance, low inductance circuit paths. One should remember to minimize the effects of capacitive coupling between circuits. Furthermore, IC sockets should be avoided. Feedback resistors should be of a low enough value that the time constant formed with stray circuit capacitances at the amplifier summing junction will not limit circuit performance. As a rule of thumb, use feedback resistor values that are less than 5 kΩ. If a larger resistor value is necessary, a small (<10 pF) feedback capacitor in parallel with the feedback resistor may be used. The use of 0.1 μF ceramic disc capacitors is recommended for bypassing the op amp's power supply leads.



$$V_{OUT} \text{ AT TERMINATION RESISTOR, } R_T = \frac{V_X^2 V_{IN}}{8V_2}$$

$$V_{OUT} \text{ AT PIN 8 OF AD827} = \frac{V_X^2 V_{IN}}{4V^2}$$

Figure 25. A Wide Range Voltage-Controlled Amplifier Circuit

ANALOG DEVICES

High Speed, Low Noise Video Op Amp

AD829

FEATURES

High Speed
- 120 MHz Bandwidth, Gain = −1
- 230 V/μs Slew Rate
- 90 ns Settling Time to 0.1%

Ideal for Video Applications
- 0.02% Differential Gain
- 0.04° Differential Phase

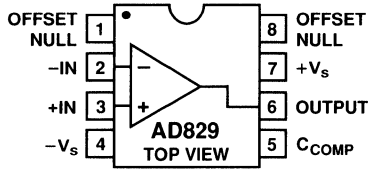
Low Noise
- 2 nV/$\sqrt{Hz}$ Input Voltage Noise
- 1.5 pA/$\sqrt{Hz}$ Input Current Noise

Excellent DC Precision
- 1 mV max Input Offset Voltage (Over Temp)
- 0.3 μV/°C Input Offset Drift

Flexible Operation
- Specified for ±5 V to ±15 V Operation
- ±3 V Output Swing into a 150 Ω Load
- External Compensation for Gains 1 to 20
- 5 mA Supply Current

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N),
Cerdip (Q) and SOIC (R) Packages



PRODUCT DESCRIPTION

The AD829 is a low noise (2 nV/$\sqrt{Hz}$), high speed op amp with custom compensation that provides the user with gains from ±1 to ±20 while maintaining a bandwidth greater than 50 MHz. The AD829's 0.04° differential phase and 0.02% differential gain performance at 3.58 MHz and 4.43 MHz, driving reverse-terminated 50 Ω or 75 Ω cables, makes it ideally suited for professional video applications. The AD829 achieves its 230 V/μs uncompensated slew rate and 750 MHz gain bandwidth product while requiring only 5 mA of current from the power supplies.

The AD829's external compensation pin gives it exceptional versatility. For example, compensation can be selected to optimize the bandwidth for a given load and power supply voltage. As a gain-of-two line driver, the −3 dB bandwidth can be increased to 95 MHz at the expense of 1 dB of peaking. In addition, the AD829's output can also be clamped at its external compensation pin.

The AD829 has excellent dc performance. It offers a minimum open-loop gain of 30 V/mV into loads as low as 500 Ω, low input voltage noise of 2 nV/$\sqrt{Hz}$, and a low input offset voltage of 1 mV maximum. Common-mode rejection and power supply rejection ratios are both 120 dB.

The AD829 is also useful in multichannel, high speed data conversion where its fast (90 ns to 0.1%) settling time is of importance. In such applications, the AD829 serves as an input buffer for 8-to-10-bit A/D converters and as an output I/V converter for high speed D/A converters.

The AD829 provides many of the same advantages that a transimpedance amplifier offers, while operating as a traditional voltage feedback amplifier. A bandwidth greater than 50 MHz can be maintained for a range of gains by changing the external compensation capacitor. The AD829 and the transimpedance amplifier are both unity gain stable and provide similar voltage noise performance (2 nV/$\sqrt{Hz}$). However, the current noise of the AD829 (1.5 pA/$\sqrt{Hz}$) is less than 10% of the noise of transimpedance amps. Furthermore, the inputs of the AD829 are symmetrical.

PRODUCT HIGHLIGHTS

1. Input voltage noise of 2 nV/$\sqrt{Hz}$, current noise of 1.5 pA/$\sqrt{Hz}$ and 50 MHz bandwidth, for gains of 1 to 20, make the AD829 an ideal preamp.
2. Differential phase error of 0.04° and a 0.02% differential gain error, at the 3.58 MHz NTSC and 4.43 MHz PAL and SECAM color subcarrier frequencies, make it an outstanding video performer for driving reverse-terminated 50 Ω and 75 Ω cables to ±1 V (at their terminated end).
3. The AD829 can drive heavy capacitive loads.
4. Performance is fully specified for operation from ±5 V to ±15 V supplies.
5. Available in plastic, cerdip, and small outline packages. Chips and MIL-STD-883B parts are also available.

AD829—SPECIFICATIONS (@ T_A = +25°C and V_S = ±15 V dc, unless otherwise noted)

Model	Conditions	V_S	AD829J Min	AD829J Typ	AD829J Max	AD829 A/S Min	AD829 A/S Typ	AD829 A/S Max	Units
INPUT OFFSET VOLTAGE		±5 V, ±15 V		0.2	1		0.1	0.5	mV
	T_{min} to T_{max}				1			0.5	mV
Offset Voltage Drift		±5 V, ±15 V		0.3			0.3		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	7		3.3	7	µA
	T_{min} to T_{max}				8.2			9.5	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		50	500		50	500	nA
	T_{min} to T_{max}				500			500	nA
Offset Current Drift		±5 V, ±15 V		0.5			0.5		nA/°C
OPEN-LOOP GAIN	V_O = ±2.5 V	±5 V							
	R_{LOAD} = 500 Ω		30	65		30	65		V/mV
	T_{min} to T_{max}		20			20			V/mV
	R_{LOAD} = 150 Ω			40			40		V/mV
	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 1 kΩ		50	100		50	100		V/mV
	T_{min} to T_{max}		20			20			V/mV
	R_{LOAD} = 500 Ω			85			85		V/mV
DYNAMIC PERFORMANCE									
Gain Bandwidth Product		±5 V		600			600		MHz
		±15 V		750			750		MHz
Full Power Bandwidth[1, 2]	V_O = 2 V p–p								
	R_{LOAD} = 500 Ω	±5 V		25			25		MHz
	V_O = 20 V p–p								
	R_{LOAD} = 1 kΩ	±15 V		3.6			3.6		MHz
Slew Rate[2]	R_{LOAD} = 500 Ω	±5 V		150			150		V/µs
	R_{LOAD} = 1 kΩ	±15 V		230			230		V/µs
Settling Time to 0.1%	A_V = −19								
	−2.5 V to +2.5 V	±5 V		65			65		ns
	10 V Step	±15 V		90			90		ns
Phase Margin[2]	C_{LOAD} = 10 pF	±15 V							
	R_{LOAD} = 1 kΩ			60			60		Degrees
DIFFERENTIAL GAIN ERROR[3]	R_{LOAD} = 100 Ω	±15 V							
	C_{COMP} = 30 pF			0.02			0.02		%
DIFFERENTIAL PHASE ERROR[3]	R_{LOAD} = 100 Ω	±15 V							
	C_{COMP} = 30 pF			0.04			0.04		Degrees
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5 V	100	120		100	120		dB
	V_{CM} = ±12 V	±15 V	100	120		100	120		dB
	T_{min} to T_{max}		96			96			dB
POWER SUPPLY REJECTION	V_S = ±4.5 V to ±18 V		98	120		98	120		dB
	T_{min} to T_{max}		94			94			dB
INPUT VOLTAGE NOISE	f = 1 kHz	±15 V		2			2		nV/$\sqrt{Hz}$
INPUT CURRENT NOISE	f = 1 kHz	±15 V		1.5			1.5		pA/$\sqrt{Hz}$
INPUT COMMON-MODE VOLTAGE RANGE		±5 V		+4.3			+4.3		V
				−3.8			−3.8		V
		±15 V		+14.3			+14.3		V
				−13.8			−13.8		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	3.0	3.6		3.0	3.6		±V
	R_{LOAD} = 150 Ω	±5 V	2.5	3.0		2.5	3.0		±V
	R_{LOAD} = 50 Ω	±5 V		1.4			1.4		±V
	R_{LOAD} = 1 kΩ	±15 V	12	13.3		12	13.3		±V
	R_{LOAD} = 500 Ω	±15 V	10	12.2		10	12.2		±V
Short Circuit Current		±5 V, ±15 V		32			32		mA
INPUT CHARACTERISTICS									
Input Resistance (Differential)				13			13		kΩ
Input Capacitance (Differential)[4]				5			5		pF
Input Capacitance (Common Mode)				1.5			1.5		pF
CLOSED-LOOP OUTPUT RESISTANCE	A_V = +1, f = 1 kHz			2			2		MΩ

Model	Conditions	V_S	AD829J Min	AD829J Typ	AD829J Max	AD829 A/S Min	AD829 A/S Typ	AD829 A/S Max	Units
POWER SUPPLY									
Operating Range			±4.5		±18		±4.5	±18	V
Quiescent Current		±5 V		5	6.5		5	6.5	mA
	T_{min} to T_{max}				8.0			8.2/8.7	mA
		±15 V		5.3	6.8		5.3	6.8	mA
	T_{min} to T_{max}				8.3			8.5/9.0	mA
TRANSISTOR COUNT	Number of Transistors			46			46		

NOTES
[1]Full Power Bandwidth = Slew Rate/2 π V_{PEAK}.
[2]Tested at Gain = +20, C_{COMP} = 0 pF.
[3]3.58 MHz (NTSC) and 4.43 MHz (PAL & SECAM).
[4]Differential input capacitance consists of 1.5 pF package capacitance plus 3.5 pF from the input differential pair.
Specifications subject to change without notice.

2

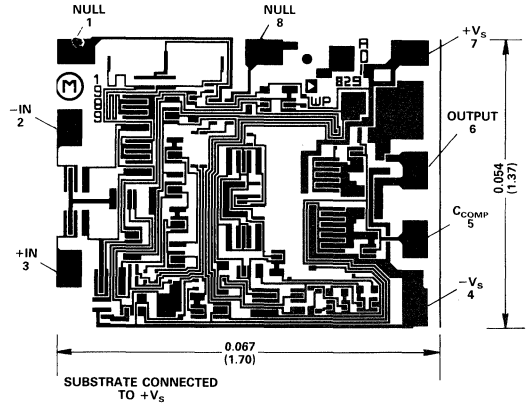
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) . . . . . 1.3 Watts
Small Outline (R) . . . . . 0.9 Watts
Cerdip (Q) . . . . . 1.3 Watts
Input Voltage . . . . . ±Vs
Differential Input Voltage[3] . . . . . ±6 Volts
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range Q . . . . . −65°C to +150°C
Storage Temperature Range N, R . . . . . −65°C to +125°C
Operating Temperature Range
AD829J . . . . . 0 to +70°C
AD829A . . . . . −40°C to +85°C
AD829S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C.
Thermal characteristics:
8-pin plastic package: θ_{JA} = 100°C/watt (derate at 8.7 mW/°C)
8-pin cerdip package: θ_{JA} = 110°C/watt (derate at 8.7 mW/°C)
8-pin small outline package: θ_{JA} = 155°C/watt (derate at 6 mW/°C).
[3]If the differential voltage exceeds 6 volts, external series protection resistors should be added to limit the input current.

METALIZATION PHOTO

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options[1, 2]
AD829JN	0 to +70°C	8-Pin Plastic Mini-DIP	N-8
AD829JR[3]	0 to +70°C	8-Pin Plastic SOIC	R-8
AD829AQ	−40°C to +85°C	8-Pin Cerdip	Q-8
AD829SQ	−55°C to +125°C	8-Pin Cerdip	Q-8
AD829SQ/883B	−55°C to +125°C	8-Pin Cerdip	Q-8

NOTES
[1]N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.
[2]J grade chips also available.
[3]Available in tape and reel packaging.

AD829—Typical Performance Characteristics

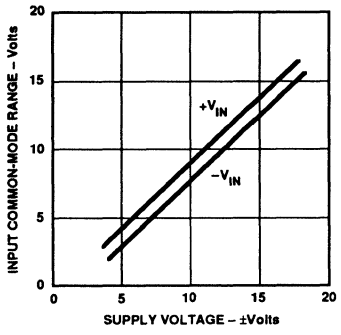


Figure 1. Input Common-Mode Range vs. Supply Voltage

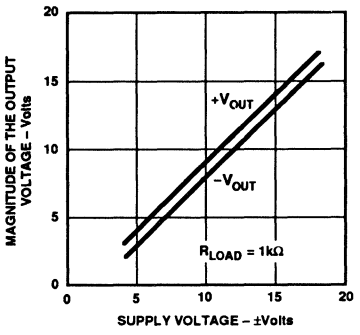


Figure 2. Output Voltage Swing vs. Supply Voltage

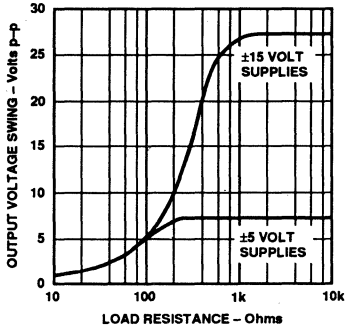


Figure 3. Output Voltage Swing vs. Resistive Load

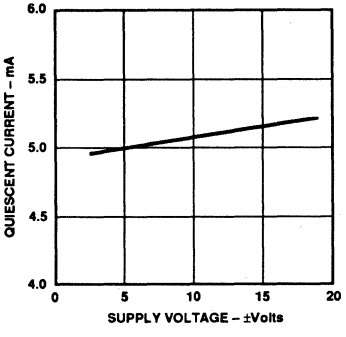


Figure 4. Quiescent Current vs. Supply Voltage

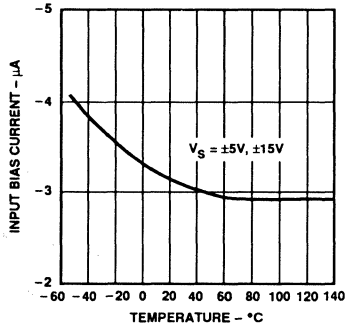


Figure 5. Input Bias Current vs. Temperature

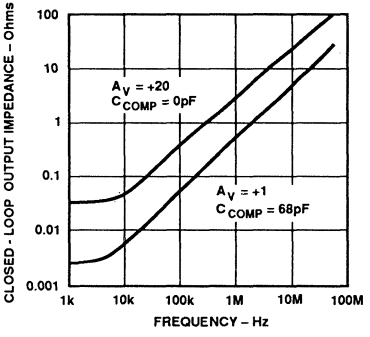


Figure 6. Closed-Loop Output Impedance vs. Frequency

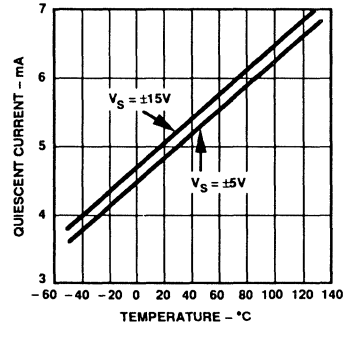


Figure 7. Quiescent Current vs. Temperature

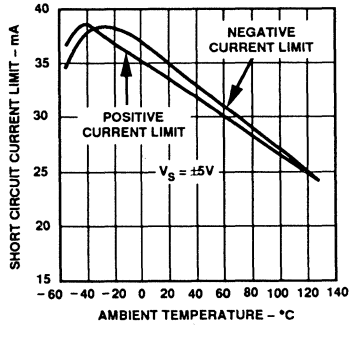


Figure 8. Short Circuit Current Limit vs. Temperature

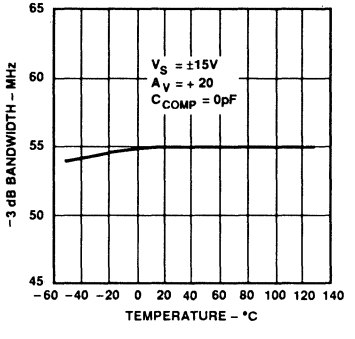


Figure 9. –3 dB Bandwidth vs. Temperature

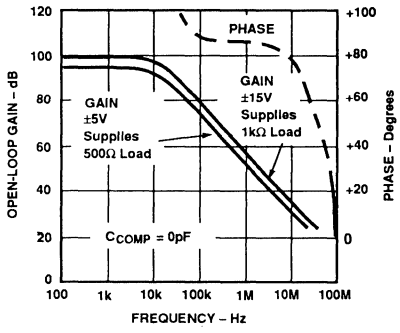


Figure 10. Open-Loop Gain & Phase Margin vs. Frequency

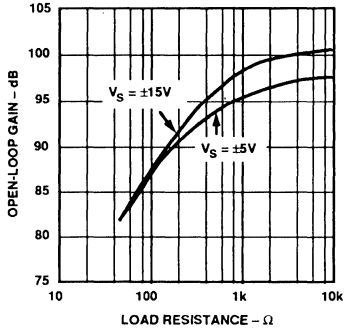


Figure 11. Open-Loop Gain vs. Resistive Load

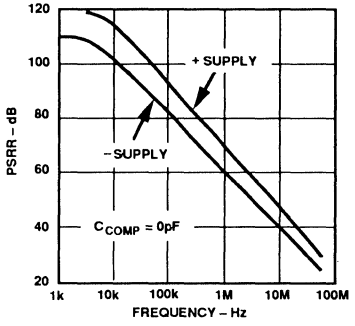


Figure 12. Power Supply Rejection Ratio (PSRR) vs. Frequency

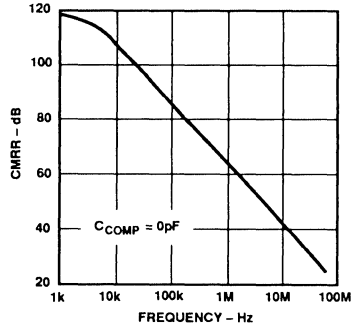


Figure 13. Common-Mode Rejection Ratio vs. Frequency

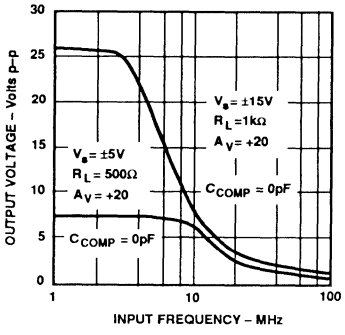


Figure 14. Large Signal Frequency Response

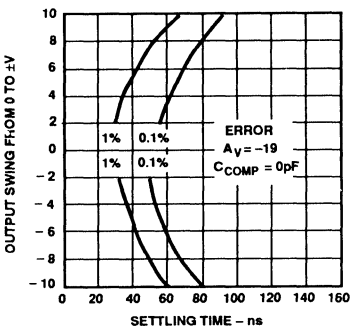


Figure 15. Output Swing & Error vs. Settling Time

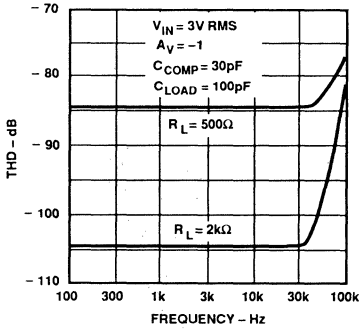


Figure 16. Total Harmonic Distortion (THD) vs. Frequency

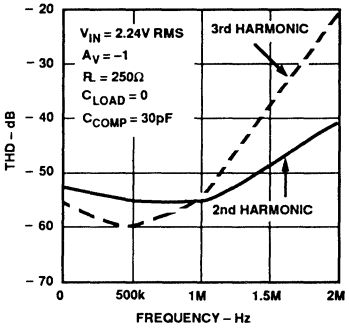


Figure 17. 2nd & 3rd Harmonic Distortion vs. Frequency

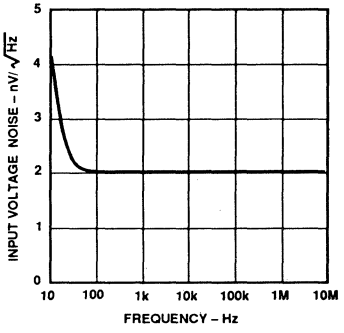


Figure 18. Input Voltage Noise Spectral Density

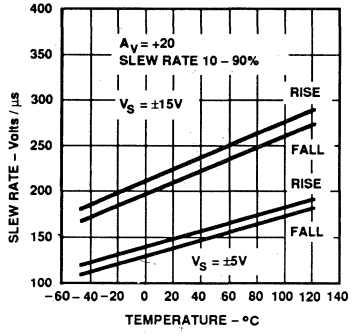


Figure 19. Slew Rate vs. Temperature

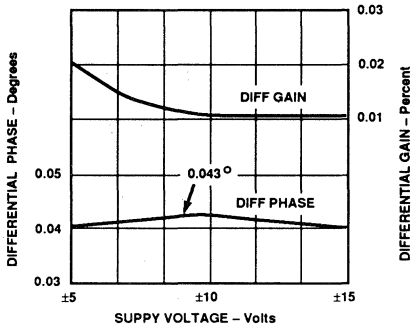


Figure 20. Differential Gain & Phase vs. Supply

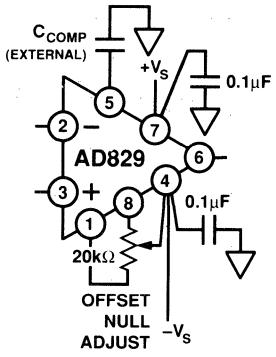


Figure 21. Offset Null and External Shunt Compensation Connections

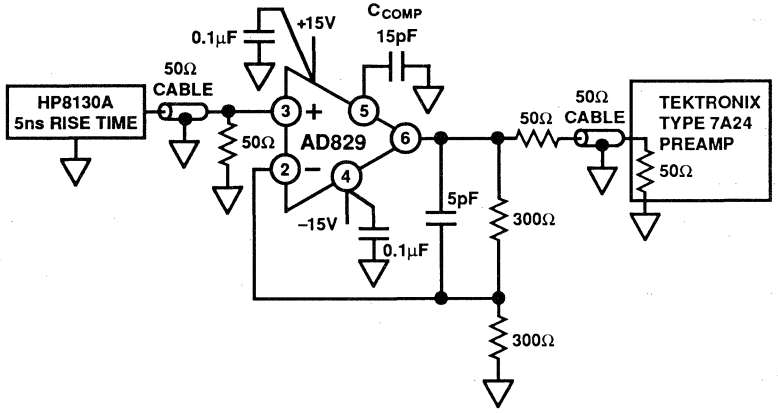


Figure 22a. Follower Connection. Gain = +2

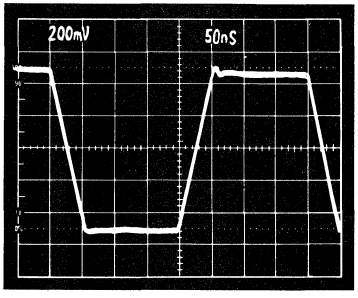


Figure 22b. Gain of 2 Follower Large Signal Pulse Response

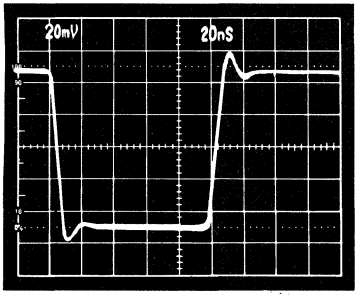


Figure 22c. Gain of 2 Follower Small Signal Pulse Response

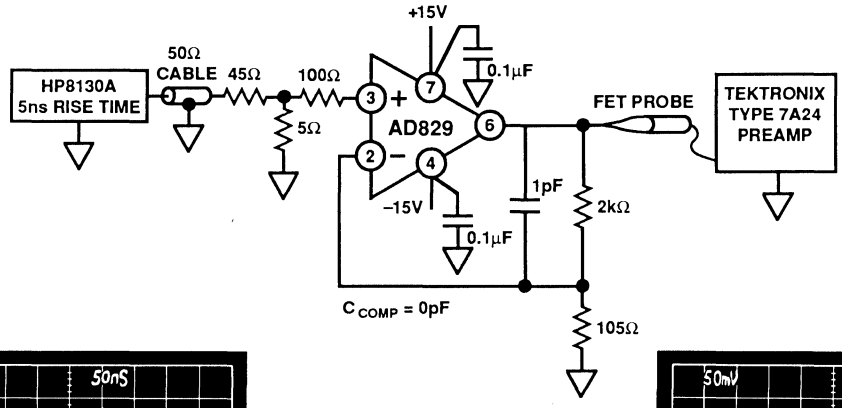


Figure 23a. Follower Connection. Gain = +20

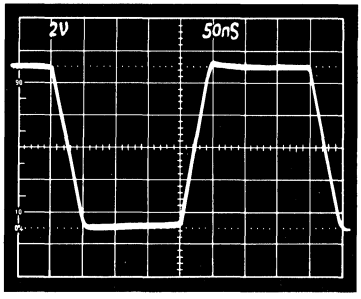


Figure 23b. Gain of 20 Follower Large Signal Pulse Response

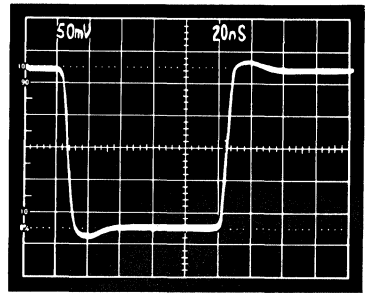


Figure 23c. Gain of 20 Follower Small Signal Pulse Response

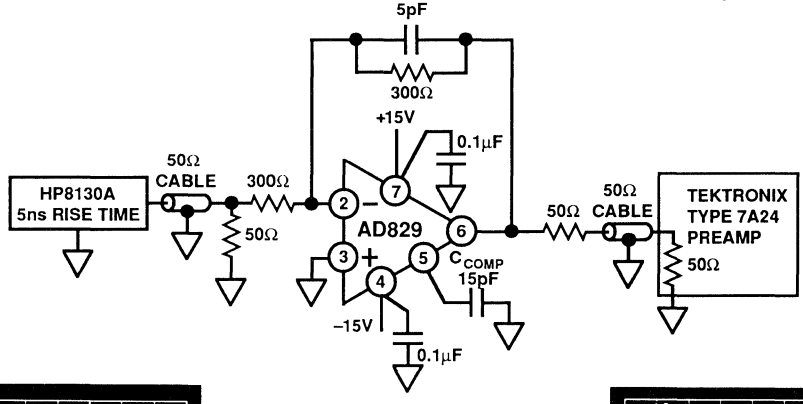


Figure 24a. Unity Gain Inverter Connection

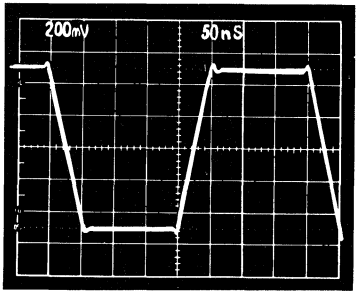


Figure 24b. Unity Gain Inverter Large Signal Pulse Response

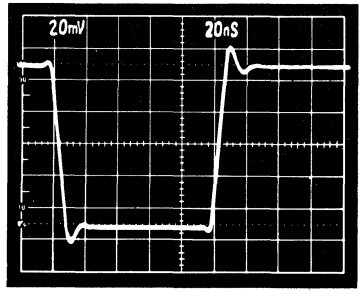


Figure 24c. Unity Gain Inverter Small Signal Pulse Response

THEORY OF OPERATION

The AD829 is fabricated on Analog Devices' proprietary complementary bipolar (CB) process which provides PNP and NPN transistors with similar f_Ts of 600 MHz. As shown in Figure 25, the AD829 input stage consists of an NPN differential pair in which each transistor operates at 600 μA collector current. This gives the input devices a high transconductance and hence gives the AD829 a low noise figure of 2 nV/$\sqrt{Hz}$ @ 1 kHz.

The input stage drives a folded cascode which consists of a fast pair of PNP transistors. These PNPs then drive a current mirror which provides a differential-input to single-ended-output conversion. The high speed PNPs are also used in the current-amplifying output stage which provides high current gain of 40,000. Even under conditions of heavy loading, the high f_Ts of the NPN & PNPs, produced using the CB process, permit cascading two stages of emitter followers while still maintaining 60° of phase margin at closed-loop bandwidths greater than 50 MHz.

Two stages of complementary emitter followers also effectively buffer the high impedance compensation node (at the C_{COMP} pin) from the output so that the AD829 can maintain a high dc open-loop gain, even into low load impedances: 92 dB into a 150 Ω load, 100 dB into a 1 kΩ load. Laser trimming and PTAT biasing assure low offset voltage and low offset voltage drift enabling the user to eliminate ac coupling in many applications.

For added flexibility, the AD829 provides access to the internal frequency compensation node. This allows the user to customize frequency response characteristics for a particular application.

Unity gain stability requires a compensation capacitance of 68 pF (Pin 5 to ground) which will yield a small signal bandwidth of 66 MHz and slew rate of 16 V/μs. The slew rate and gain bandwidth product will vary inversely with compensation capacitance. Table I and the graph of Figure 28 show the optimum compensation capacitance and the resulting slew rate for a desired noise gain. For gains between 1 and 20, C_{COMP} can be chosen to keep the small signal bandwidth relatively constant. The minimum gain which will still provide stability also depends on the value of external compensation capacitance.

An RC network in the output stage (Figure 25) completely removes the effect of capacitive loading when the amplifier is compensated for closed-loop gains of 10 or higher. At low frequencies, and with low capacitive loads, the gain from the compensation node to the output is very close to unity. In this case, C is bootstrapped and does not contribute to the compensation capacitance of the device. As the capacitive load is increased, a pole is formed with the output impedance of the output stage– this reduces the gain, and subsequently, C is incompletely bootstrapped. Therefore, some fraction of C contributes to the compensation capacitance, and the unity gain bandwidth falls. As the load capacitance is further increased, the bandwidth continues to fall, and the amplifier remains stable.

Externally Compensating the AD829

The AD829 is stable with no external compensation for noise gains greater than 20. For lower gains, there are two methods of frequency compensating the amplifier to achieve closed-loop stability; these are the shunt and current feedback compensation methods.

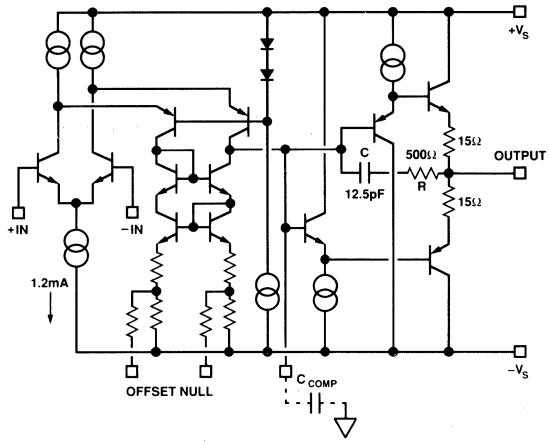


Figure 25. AD829 Simplified Schematic

Shunt Compensation

Figures 26 & 27 show that the first method, shunt compensation, has an external compensation capacitor, C_{COMP}, connected between the compensation pin and ground. This external capacitor is tied in parallel with approximately 3 pF of internal capacitance at the compensation node. In addition, a small capacitance, C_{LEAD}, in parallel with resistor R_2, compensates for the capacitance at the amplifier's inverting input.

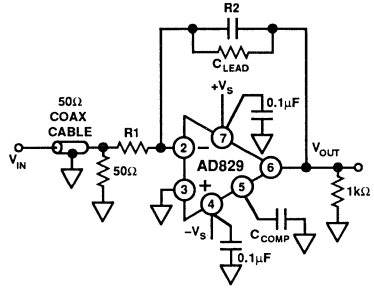


Figure 26. Inverting Amplifier Connection Using External Shunt Compensation

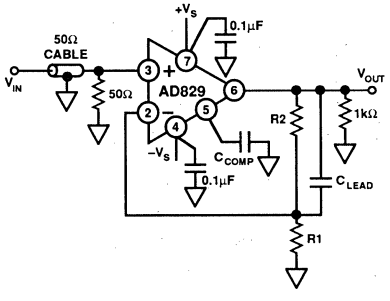


Figure 27. Noninverting Amplifier Connection Using External Shunt Compensation

Follower Gain	Inverter Gain	R1 Ω	R2 Ω	C_L pF	C_{COMP} pF	Slew Rate V/μs	−3 dB Small Signal Bandwidth – MHz
1		Open	100	0	68	16	66
2	−1	1k	1k	5	25	38	71
5	−4	511	2.0k	1	7	90	76
10	−9	226	2.05k	0	3	130	65
20	−19	105	2k	0	0	230	55
25	−24	105	2.49	0	0	230	39
100	−101	20	2k	0	0	230	7.5

Table I. Component Selection for Shunt Compensation

Table I gives recommended C_{COMP} and C_{LEAD} values along with the corresponding slew rates and bandwidth. The capacitor values given were selected to provide a small signal frequency response with less than 1 dB of peaking and less than 10% overshoot. For this table, supply voltages of ±15 volts should be used. Figure 28 is a graphical extension of the table which shows the slew rate/gain trade-off for lower closed-loop gains, when using the shunt compensation scheme.

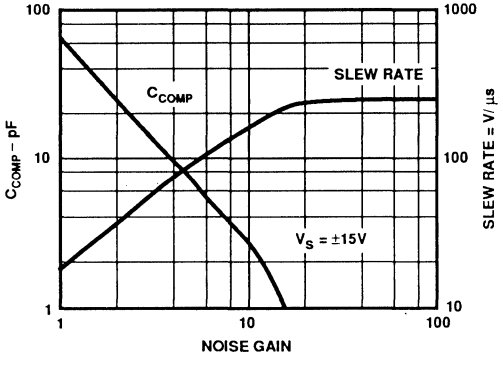


Figure 28. Value of C_{COMP} & Slew Rate vs. Noise Gain

Current Feedback Compensation

Bipolar nondegenerated amplifiers which are single pole and internally compensated have their bandwidths defined as:

$$f_T = \frac{1}{2\pi r_e C_{COMP}} = \frac{I}{2\pi \frac{kT}{q} C_{COMP}}$$

where:

f_T is the unity gain bandwidth of the amplifier
I is the collector current of the input transistor
C_{COMP} is the compensation capacitance
r_e is the inverse of the transconductance of the input transistors
kT/q is approximately equal to 26 mV @ 27°C.

Since both f_T and slew rate are functions of the same variables, the dynamic behavior of an amplifier is limited. Since:

$$Slew\ Rate = \frac{2I}{C_{COMP}}$$

then:

$$\frac{Slew\ Rate}{f_T} = 4\pi \frac{kT}{q}$$

This shows that the slew rate will be only 0.314 V/μs for every MHz of bandwidth. The only way to increase slew rate is to increase the f_T and that is difficult, due to process limitations. Unfortunately, an amplifier with a bandwidth of 10 MHz can only slew at 3.1 V/μs, which is barely enough to provide a full power bandwidth of 50 kHz.

The AD829 is especially suited to a new form of compensation which allows for the enhancement of both the full power bandwidth and slew rate of the amplifier. The voltage gain from the inverting input pin to the compensation pin is large; therefore, if a capacitance is inserted between these pins, the amplifier's bandwidth becomes a function of its feedback resistor and this capacitance. The slew rate of the amplifier is now a function of its internal bias (2I) and this compensation capacitance.

Since the closed-loop bandwidth is a function of R_F and C_{COMP} (Figure 29), it is independent of the amplifier closed-loop gain, as shown in Figure 31. To preserve stability, the time constant of R_F and C_{COMP} needs to provide a bandwidth of less than 65 MHz. For example, with C_{COMP} = 15 pF and R_F = 1 kΩ, the small signal bandwidth of the AD829 is 10 MHz, while Figure 30 shows that the slew rate is in excess of 60 V/μs. As can be seen in Figure 31, the closed-loop bandwidth is constant for gains of −1 to −4, a property of current feedback amplifiers.

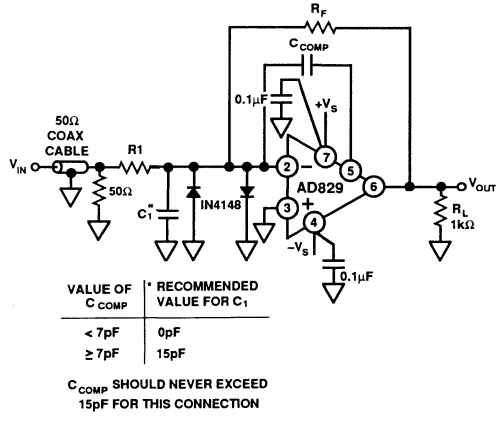


Figure 29. Inverting Amplifier Connection Using Current Feedback Compensation

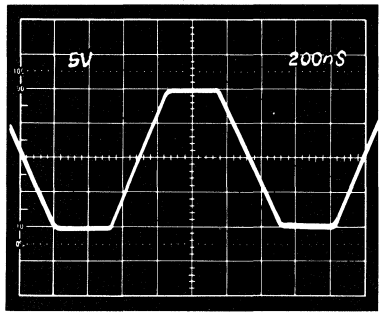


Figure 30. Large Signal Pulse Response of Inverting Amplifier Using Current Feedback Compensation. C_{COMP} = 15 pF, C_1 = 15pF, R_F = 1kΩ, R_1 = 1 kΩ

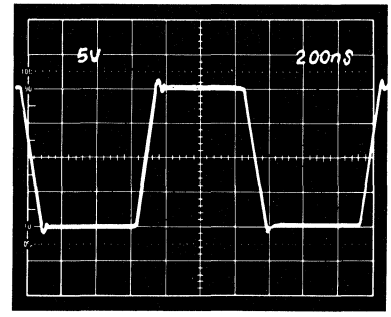


Figure 32. Large Signal Pulse Response of the Inverting Amplifier Using Current Feedback Compensation. C_{COMP} = 1 pF, R_F = 3 kΩ, R_1 = 3 kΩ

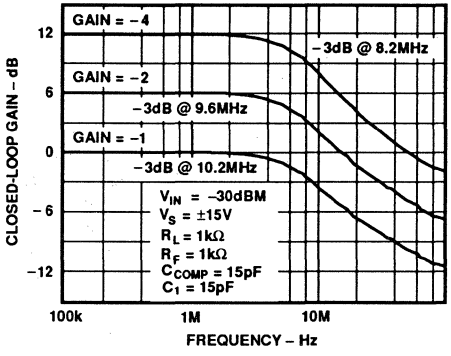


Figure 31. Closed-Loop Gain vs. Frequency for the Circuit of Figure 29

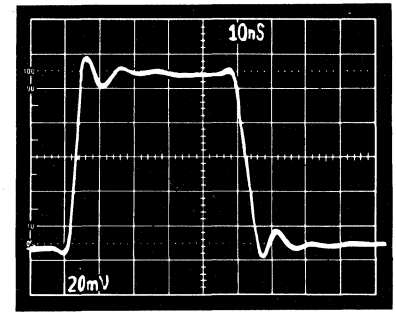


Figure 33. Small Signal Pulse Response of Inverting Amplifier Using Current Feedback Compensation. C_{COMP} = 4 pF, R_F = 1 kΩ, R_1 = 1 kΩ

Figure 32 is an oscilloscope photo of the pulse response of a unity gain inverter which has been configured to provide a small signal bandwidth of 53 MHz and a subsequent slew rate of 180 V/μs; resistor R_F = 3 kΩ, capacitor C_{COMP} = 1 pF. Figure 33 shows the excellent pulse response as a unity gain inverter, this time using component values of: R_F = 1 kΩ and C_{COMP} = 4 pF.

Figures 34 and 35 show the closed-loop frequency response of the AD829 for different closed-loop gains and for different supply voltages.

If a noninverting amplifier configuration using current feedback compensation is desired, the circuit of Figure 36 is recommended. This circuit doubles the slew rate compared to the shunt compensated noninverting amplifier of Figure 27 at the expense of gain flatness. Nonetheless, this circuit delivers 95 MHz bandwidth with ±1 dB flatness into a back terminated cable, with a differential gain error of only 0.01%, and a differential phase error of only 0.015° at 4.43 MHz.

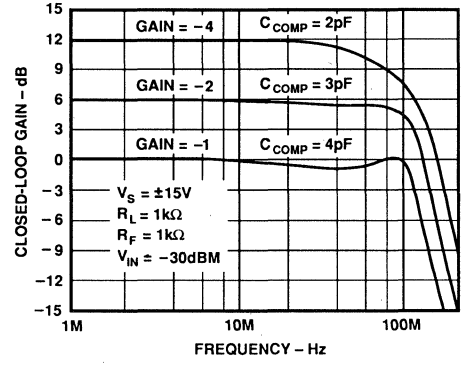


Figure 34. Closed-Loop Frequency Response for the Inverting Amplifier Using Current Feedback Compensation

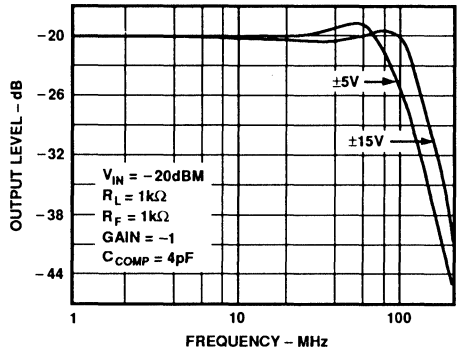


Figure 35. Closed-Loop Frequency Response vs. Supply for the Inverting Amplifier Using Current Feedback Compensation

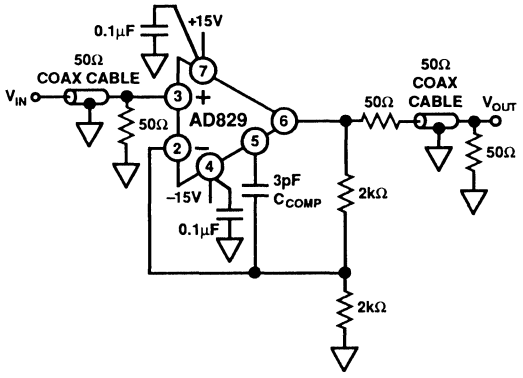


Figure 36. Noninverting Amplifier Connection Using Current Feedback Compensation

A Low Error Video Line Driver

The buffer circuit shown in Figure 37 will drive a back-terminated 75 Ω video line to standard video levels (1 V p–p) with 0.1 dB gain flatness to 30 MHz with only 0.04° and 0.02% differential phase and gain at the 4.43 MHz PAL color subcarrier frequency. This level of performance, which meets the requirements for high definition video displays and test equipment, is achieved using only 5 mA quiescent current.

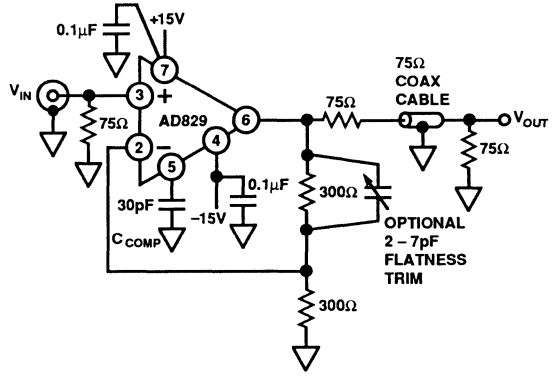


Figure 37. A Video Line Driver with a Flatness over Frequency Adjustment

ANALOG DEVICES

Wideband, Fast Settling Op Amp

AD840

FEATURES

Wideband AC Performance
- Gain Bandwidth Product: 400 MHz (Gain ≥ 10)
- Fast Settling: 100 ns to 0.01% for a 10 V Step
- Slew Rate: 400 V/μs
- Stable at Gains of 10 or Greater
- Full Power Bandwidth: 6.4 MHz for 20 V p–p into a 500 Ω Load

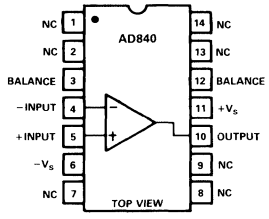
Precision DC Performance
- Input Offset Voltage: 0.3 mV max
- Input Offset Drift: 3 μV/°C typ
- Input Voltage Noise: 4 nV/√Hz
- Open-Loop Gain: 130 V/mV into a 1 kΩ Load
- Output Current: 50 mA min
- Supply Current: 12 mA max

APPLICATIONS

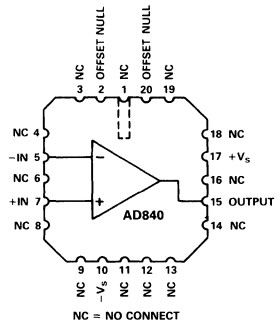
Video and Pulse Amplifiers
DAC and ADC Buffers
Line Drivers
Available in 14-Pin Plastic DIP, Hermetic Cerdip and 20-Pin LCC Packages and in Chip Form
MIL-STD-883B Processing Available

CONNECTION DIAGRAMS

Plastic DIP (N) Package and Cerdip (Q) Package



LCC (E) Package



PRODUCT DESCRIPTION

The AD840 is a member of the Analog Devices' family of wide bandwidth operational amplifiers. This high speed/high precision family includes, among others, the AD841, which is unity-gain stable, and the AD842, which is stable at a gain of two or greater and has 100 mA minimum output current drive. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to its 400 MHz gain bandwidth product, the AD840 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in 100 ns for a 10 volt step.

The AD840 remains stable over its full operating temperature range at closed-loop gains of 10 or greater. It also offers a low quiescent current of 12 mA maximum, a minimum output current drive capability of 50 mA, a low input voltage noise of 4 nV/√Hz and a low input offset voltage of 0.3 mV maximum (AD840K).

The 400 V/μs slew rate of the AD840, along with its 400 MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is ideally suited for use in high frequency signal conditioning circuits and wide bandwidth active filters. The extremely rapid settling time of the AD840 makes it the preferred choice for data acquisition applications which require 12-bit accuracy. The AD840 is also appropriate for other applications such as high speed DAC and ADC buffer amplifiers and other wide bandwidth circuitry.

APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD840 make it ideal for DAC and ADC buffers, line drivers and all types of video instrumentation circuitry.
2. The AD840 is truly a precision amplifier. It offers 12-bit accuracy to 0.01% or better and wide bandwidth, performance previously available only in hybrids.
3. The AD840's thermally balanced layout and the high speed of the CB process allow the AD840 to settle to 0.01% in 100 ns without the long "tails" that occur with other fast op amps.
4. Laser wafer trimming reduces the input offset voltage to 0.3 mV max on the K grade, thus eliminating the need for external offset nulling in many applications. Offset null pins are provided for additional versatility.
5. Full differential inputs provide outstanding performance in all standard high frequency op amp applications where circuit gain will be 10 or greater.
6. The AD840 is an enhanced replacement for the HA2540.

AD840—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD840J Min	AD840J Typ	AD840J Max	AD840K Min	AD840K Typ	AD840K Max	AD840S Min	AD840S Typ	AD840S Max	Units
INPUT OFFSET VOLTAGE[1]			0.2	**1**		0.1	**0.3**		0.2	**1**	mV
	T_{min} – T_{max}			1.5			**0.7**			2	mV
Offset Drift			5			3			5		μV/°C
INPUT BIAS CURRENT			3.5	**8**		3.5	**5**		3.5	**8**	μA
	T_{min} – T_{max}			10			**6**			12	μA
INPUT OFFSET CURRENT			0.1	**0.4**		0.1	**0.2**		0.1	**0.4**	μA
	T_{min} – T_{max}			0.5			**0.3**			0.6	μA
INPUT CHARACTERISTICS	Differential Mode										
Input Resistance			30			30			30		kΩ
Input Capacitance			2			2			2		pF
INPUT VOLTAGE RANGE											
Common Mode		**±10**	12		**±10**	12		±10	12		V
Common-Mode Rejection	V_{CM} = ±10 V	**90**	110		**106**	115		**90**	110		dB
	T_{min} – T_{max}	85			**90**			85			dB
INPUT VOLTAGE NOISE	f = 1 kHz		4			4			4		nV/√Hz
Wideband Noise	10 Hz to 10 MHz		10			10			10		μV rms
OPEN LOOP GAIN	V_O = ±10 V										
	R_{LOAD} = 1 kΩ	**100**	130		**100**	130		**100**	130		V/mV
	T_{min} – T_{max}	50	80		**75**	100		**50**	80		V/mV
	R_{LOAD} = 500 Ω	**75**			**100**			75			V/mV
	T_{min} – T_{max}	50			75			50			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} ≥ 500 Ω										
	T_{min} – T_{max}	**±10**			**±10**			**±10**			V
Current	V_{OUT} = ±10 V	**50**			**50**			**50**			mA
Output Resistance	Open Loop		15			15			15		Ω
FREQUENCY RESPONSE											
Gain Bandwidth Product	V_{OUT} = 90 mV p–p										
	A_V = –10		400			400			400		MHz
Full Power Bandwidth[2]	V_O = 20 V p–p										
	R_{LOAD} ≥ 500 Ω	5.5	6.4		5.5	6.4		5.5	6.4		MHz
Rise Time	A_V = –10		10			10			10		ns
Overshoot[3]	A_V = –10		20			20			20		%
Slew Rate[3]	A_V = –10	350	400		350	400		350	400		V/μs
Settling Time[3] –10 V Step	A_V = –10										
	to 0.1%		80			80			80		ns
	to 0.01%		100			100			100		ns
OVERDRIVE RECOVERY	–Overdrive		190			190			190		ns
	+Overdrive		350			350			350		ns
DIFFERENTIAL GAIN	f = 4.4 MHz		0.025			0.025			0.025		%
DIFFERENTIAL PHASE	f = 4.4 MHz		0.04			0.04			0.04		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±5		**±18**	±5		**±18**	±5		**±18**	V
Quiescent Current			10.5	**12**		10.5	**12**		10.5	**12**	mA
	T_{min} – T_{max}			14			**14**			**16**	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±18 V	**90**	100		**94**	100		**90**	100		dB
	T_{min} – T_{max}	80			**86**			**80**			dB
TEMPERATURE RANGE											
Rated Performance[4]		**0**		**+75**	0		**+75**	–55		**+125**	°C
TRANSISTOR COUNT	# of Transistors		72			72			72		

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.
[2]Full power bandwidth = slew rate/2π V_{PEAK}.
[3]Refer to Figures 22 and 23.
[4]"S" grade T_{min}–T_{max} specifications are tested with automatic test equipment at T_A = −55°C and T_A = +125°C.
All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) . . . . . 1.5 W
Cerdip (Q) . . . . . 1.3 W
LCC (E) . . . . . 1.0 W
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Storage Temperature Range
Q, E . . . . . −65°C to +150°C
N . . . . . −65°C to +125°C
Junction Temperature (T_J) . . . . . +175°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C.

Thermal Characteristics:

	θ_{JC}	θ_{JA}	Derate at
Cerdip Package	30°C/W	110°C/W	8.7 mW/°C
Plastic Package	30°C/W	100°C/W	10 mW/°C
LCC Package	35°C/W	150°C/W	6.7 mW/°C

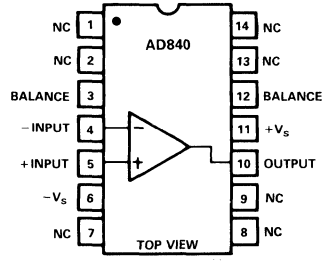
Recommended Heat Sink:
Aavid Engineering© #602B

ORDERING GUIDE

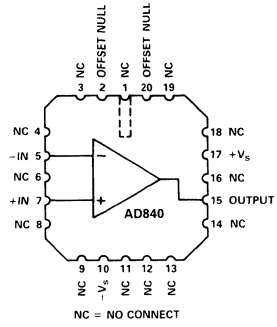
Model[1]	Package Options[2]
AD840JN	N-14
AD840KN	N-14
AD840JQ	Q-14
AD840KQ	Q-14
AD840SQ	Q-14
AD840SQ-883B	Q-14
AD840SE-883B	E-20A

NOTES
[1]J and S Grade Chips also available.
[2]N = Plastic DIP; Q = Cerdip; E = LCC (Leadless Ceramic Chip Carrier). For outline information see Package Information section.

Plastic DIP (N) Package and Cerdip (Q) Package



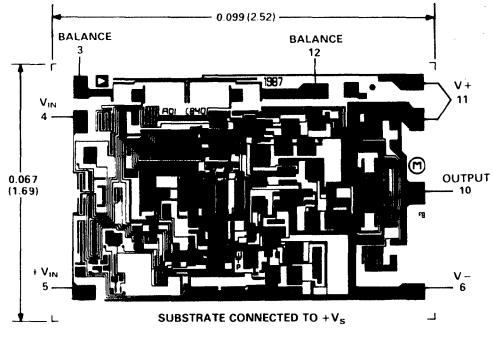
LCC (E) Package



AD840 Connection Diagrams

METALIZATION PHOTOGRAPHY

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



AD840—Typical Characteristics (at +25°C and V_S = ±15 V, unless otherwise noted)

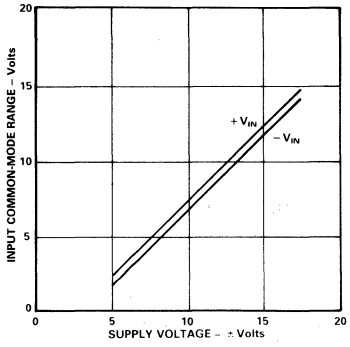


Figure 1. Input Common-Mode Range vs. Supply Voltage

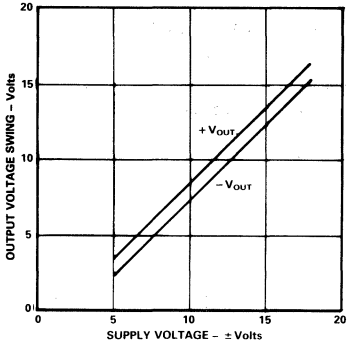


Figure 2. Output Voltage Swing vs. Supply Voltage

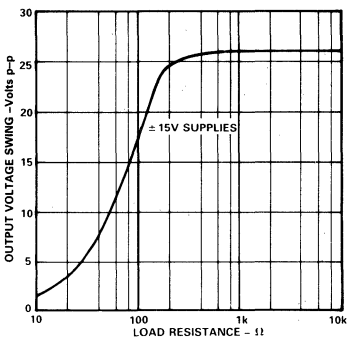


Figure 3. Output Voltage Swing vs. Load Resistance

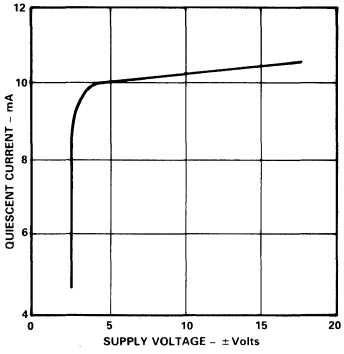


Figure 4. Quiescent Current vs. Supply Voltage

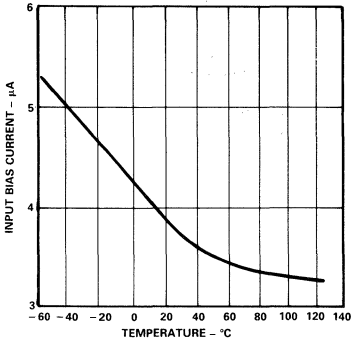


Figure 5. Input Bias Current vs. Temperature

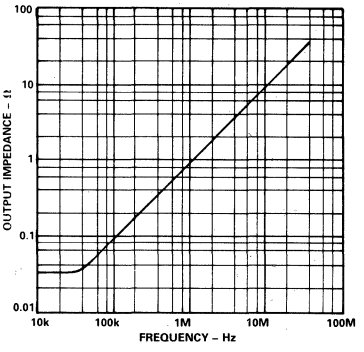


Figure 6. Output Impedance vs. Frequency

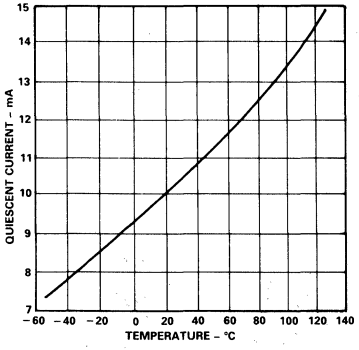


Figure 7. Quiescent Current vs. Temperature

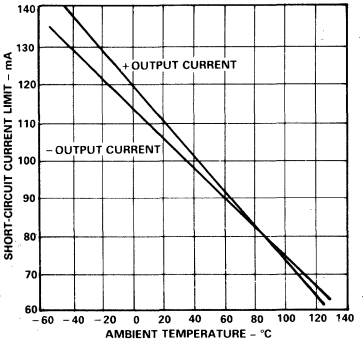


Figure 8. Short-Circuit Current Limit vs. Temperature

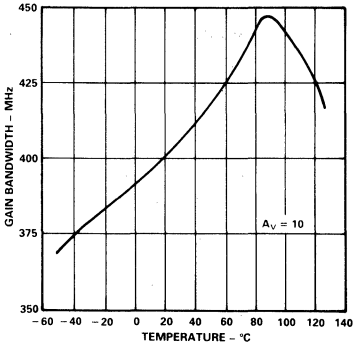


Figure 9. Gain Bandwidth Product vs. Temperature

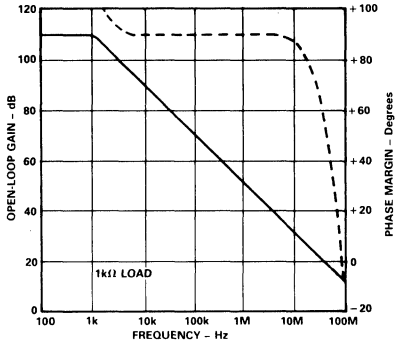


Figure 10. Open-Loop Gain and Phase Margin Phase vs. Frequency

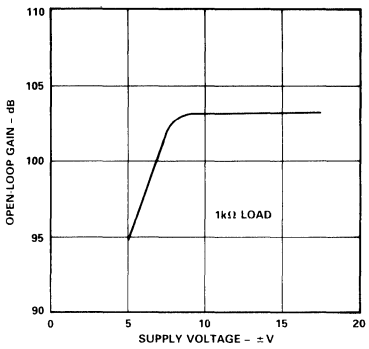


Figure 11. Open-Loop Gain vs. Supply Voltage

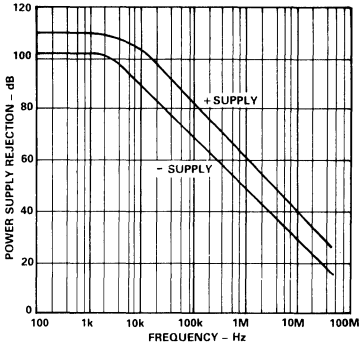


Figure 12. Power Supply Rejection vs. Frequency

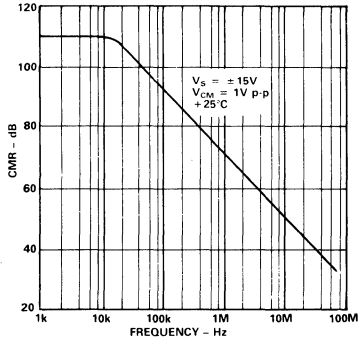


Figure 13. Common-Mode Rejection vs. Frequency

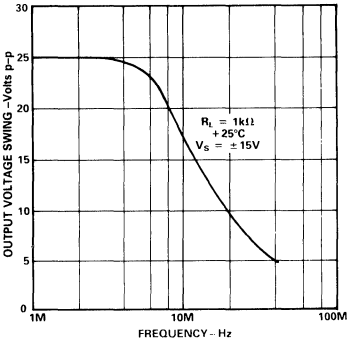


Figure 14. Large Signal Frequency Response

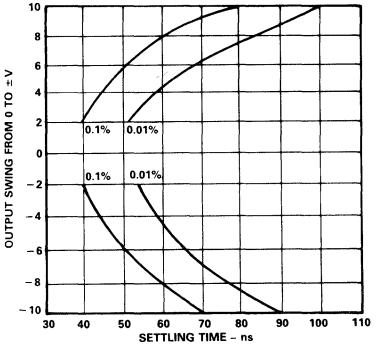


Figure 15. Output Swing and Error vs. Settling Time

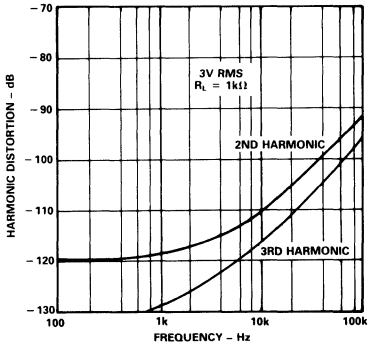


Figure 16. Harmonic Distortion vs. Frequency

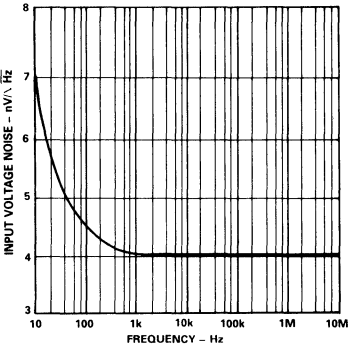


Figure 17. Input Voltage Noise Spectral Density

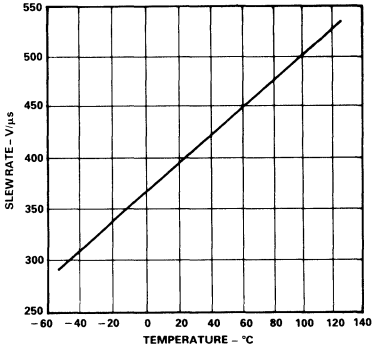


Figure 18. Slew Rate vs. Temperature

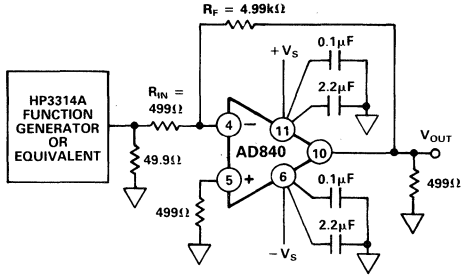


Figure 19a. Inverting Amplifier Configuration (DIP Pinout)

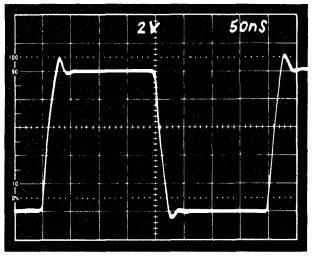


Figure 19b. Inverter Large Signal Pulse Response

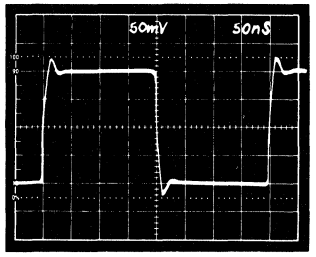


Figure 19c. Inverter Small Signal Pulse Response

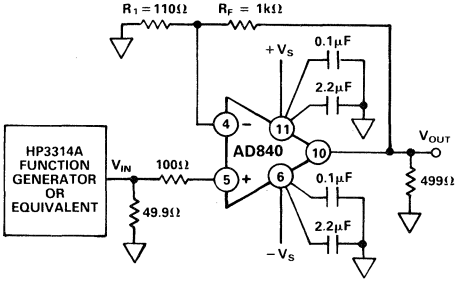


Figure 20a. Noninverting Amplifier Configuration (DIP Pinout)

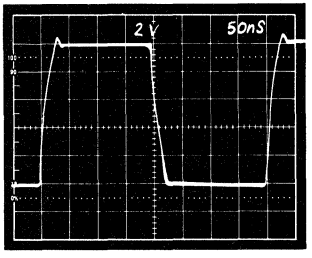


Figure 20b. Noninverting Large Signal Pulse Response

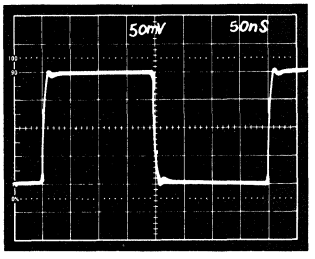


Figure 20c. Noninverting Small Signal Pulse Response

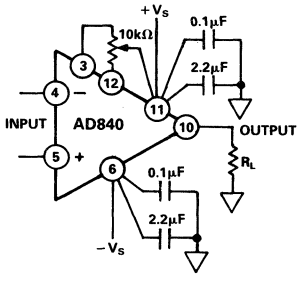


Figure 21. Offset Nulling (DIP Pinout)

OFFSET NULLING

The input offset voltage of the AD840 is very low for a high speed op amp, but if additional nulling is required, the circuit shown in Figure 21 çan be used.

AD840 SETTLING TIME

Figures 22 and 24 show the settling performance of the AD840 in the test circuit shown in Figure 23.

Settling time is defined as:

> The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

This definition encompasses the major components which comprise settling time. They include (1) propagation delay through the amplifier; (2) slewing time to approach the final output value; (3) the time of recovery from the overload associated with slewing; and (4) linear settling to within the specified error band.

Expressed in these terms, the measurement of settling time is obviously a challenge and needs to be done accurately to assure the user that the amplifier is worth consideration for the application.

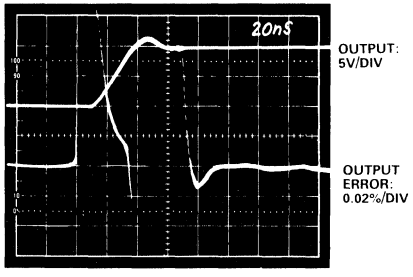


Figure 22. AD840 0.01% Settling Time

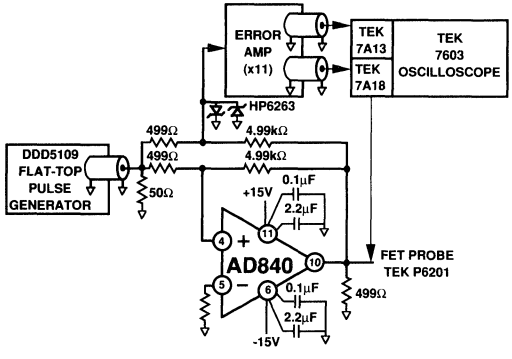


Figure 23. Settling Time Test Circuit

Figure 23 shows how measurement of the AD840's 0.01% settling in 100 ns was accomplished by amplifying the error signal from a false summing junction with a very high speed proprietary hybrid error amplifier specially designed to enable testing of small settling errors. The device under test was driving a 420 Ω load. The input to the error amp is clamped in order to avoid possible problems associated with the overdrive recovery of the oscilloscope input amplifier. The error amp amplifies the error from the false summing junction by 11, and it contains a gain vernier to fine trim the gain.

Figure 24 shows the "long-term" stability of the settling characteristics of the AD840 output after a 10 V step. There is no evidence of settling tails after the initial transient recovery time. The use of a junction isolated process, together with careful layout, avoids these problems by minimizing the effects of transistor isolation capacitance discharge and thermally induced shifts in circuit operating points. These problems do not occur even under high output current conditions.

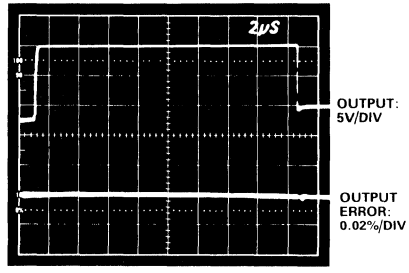


Figure 24. AD840 Settling Demonstrating No Settling Tails

GROUNDING AND BYPASSING

In designing practical circuits with the AD840, the user must remember that whenever high frequencies are involved, some special precautions are in order. Circuits must be built with short interconnect leads. Large ground planes should be used whenever possible to provide a low resistance, low inductance circuit path, as well as minimizing the effects of high frequency coupling. Sockets should be avoided, because the increased inter-lead capacitance can degrade bandwidth.

Feedback resistors should be of low enough value to assure that the time constant formed with the circuit capacitances will not limit the amplifier performance. Resistor values of less than 5 kΩ are recommended. If a larger resistor must be used, a small (±10 pF) feedback capacitor in connected parallel with the feedback resistor, R_F, may be used to compensate for these stray capacitances and optimize the dynamic performance of the amplifier in the particular application.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. A 2.2 μF capacitor in parallel with a 0.1 μF ceramic disk capacitor is recommended.

CAPACITIVE LOAD DRIVING ABILITY

Like all wideband amplifiers, the AD840 is sensitive to capacitive loading. The AD840 is designed to drive capacitive loads of up to 20 pF without degradation of its rated performance. Capacitive loads of greater than 20 pF will decrease the dynamic performance of the part although instability should not occur unless the load exceeds 100 pF. A resistor in series with the output can be used to decouple larger capacitive loads.

USING A HEAT SINK

The AD840 draws less quiescent power than most high speed amplifiers and is specified for operation without a heat sink. However, when driving low impedance loads the current to the load can be 4 to 5 times the quiescent current. This will create a noticeable temperature rise. Improved performance can be achieved by using a small heat sink such as the Aavid Engineering #602B.

HIGH SPEED DAC BUFFER CIRCUIT

The AD840's 100 ns settling time to 0.01% for a 10 V step makes it well suited as an output buffer for high speed D/A converters. Figure 25 shows the connections for producing a 0 to +10.24 V output swing from the AD568 35 ns DAC. With the AD568 in unbuffered voltage output mode, the AD840 is placed in noninverting configuration. As a result of the 1 kΩ span resistor provided internally in the AD568, the noise gain of this topology is 10. Only 5 pF is required across the feedback (span) resistor to optimize settling.

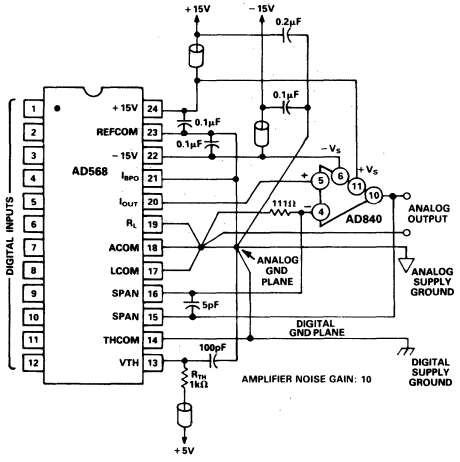


Figure 25. 0 to +10.24 V DAC Output Buffer

OVERDRIVE RECOVERY

Figure 26 shows the overdrive recovery capability of the AD840. Typical recovery time is 190 ns from negative overdrive and 350 ns from positive overdrive.

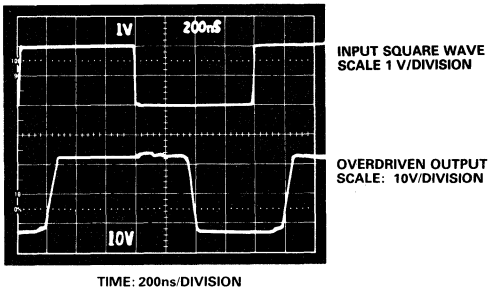


Figure 26. Overdrive Recovery

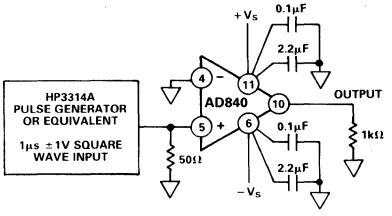


Figure 27. Overdrive Recovery Test Circuit

ANALOG DEVICES

Wideband, Unity-Gain Stable, Fast Settling Op Amp

AD841

FEATURES

AC PERFORMANCE

Unity-Gain Bandwidth: 40 MHz
Fast Settling: 110 ns to 0.01%
Slew Rate: 300 V/μs
Full Power Bandwidth: 4.7 MHz for 20 V p-p into a 500 Ω Load

DC PERFORMANCE

Input Offset Voltage: 1 mV max
Input Voltage Noise: 13 nV/$\sqrt{Hz}$ typ
Open-Loop Gain: 45V/mV into a 1 kΩ Load
Output Current: 50 mA min
Supply Current: 12 mA max

APPLICATIONS

High Speed Signal Conditioning
Video and Pulse Amplifiers
Data Acquisition Systems
Line Drivers
Active Filters
Available in 14-Pin Plastic DIP and Hermetic Cerdip, 12-Pin TO-8 Metal Can and 20-Pin LCC Packages and in Chip Form
Chips and MIL-STD-883B Parts Available

PRODUCT DESCRIPTION

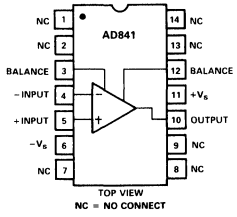
The AD841 is a member of the Analog Devices family of wide bandwidth operational amplifiers. This high speed/high precision family includes, among others, the AD840, which is stable at a gain of 10 or greater, and the AD842, which is stable at a gain of two or greater and has 100 mA minimum output current drive. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to its 40 MHz unity-gain bandwidth product, the AD841 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in 110 ns for a 10 volt step.

Unlike many high frequency amplifiers, the AD841 requires no external compensation. It remains stable over its full operating temperature range. It also offers a low quiescent current of 12 mA maximum, a minimum output current drive capablity of 50 mA, a low input voltage noise of 13 nV/$\sqrt{Hz}$ and low input offset voltage of 1 mV maximum.

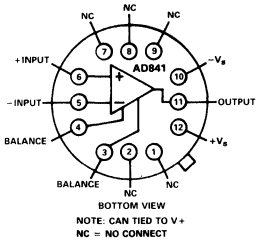
The 300 V/μs slew rate of the AD841, along with its 40 MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is well suited for use in high frequency signal conditioning circuits and wide bandwidth active filters. The extremely rapid settling time of the

CONNECTION DIAGRAMS

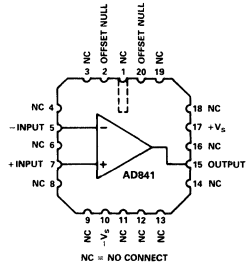
Plastic DIP (N) Package and Cerdip (Q) Package



TO-8 (H) Package



LCC (E) Package



AD841 makes it the preferred choice for data acquisition applications which require 12-bit accuracy. The AD841 is also appropriate for other applications such as high speed DAC and ADC buffer amplifiers and other wide bandwidth circuitry.

APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD841 make it ideal for DAC and ADC buffers, and all types of video instrumentation circuitry.
2. The AD841 is a precision amplifier. It offers accuracy to 0.01% or better and wide bandwidth performance previously available only in hybrids.
3. The AD841's thermally balanced layout and the speed of the CB process allow the AD841 to settle to 0.01% in 110 ns without the long "tails" that occur with other fast op amps.
4. Laser wafer trimming reduces the input offset voltage to 1 mV max on the K grade, thus eliminating the need for external offset nulling in many applications. Offset null pins are provided for additional versatility.
5. The AD841 is an enhanced replacement for the HA2541.

AD841—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD841J Min	AD841J Typ	AD841J Max	AD841K Min	AD841K Typ	AD841K Max	AD841S Min	AD841S Typ	AD841S Max	Units
INPUT OFFSET VOLTAGE[1]			0.8	**2.0**		0.5	**1.0**		0.5	**2.0**	mV
	T_{min}–T_{max}			5.0			**3.3**			5.5	mV
Offset Drift			35			35			35		μV/°C
INPUT BIAS CURRENT			3.5	**8**		3.5	**5**		3.5	**8**	μA
	T_{min}–T_{max}			10			**6**			**12**	μA
Input Offset Current			0.1	**0.4**		0.1	**0.2**		0.1	**0.4**	μA
	T_{min}–T_{max}			0.5			**0.3**			**0.6**	μA
INPUT CHARACTERISTICS	Differential Mode										
Input Resistance			200			200			200		kΩ
Input Capacitance			2			2			2		pF
INPUT VOLTAGE RANGE											
Common Mode		**± 10**	12		**±10**	12		**±10**	12		V
Common Mode Rejection	V_{CM} = ±10 V	**86**	100		**103**	109		**86**	100		dB
	T_{min}–T_{max}	80			**100**			80			dB
INPUT VOLTAGE NOISE	f = 1 kHz		15			15			15		nV/$\sqrt{Hz}$
Wideband Noise	10 Hz to 10 MHz		47			47			47		μV rms
OPEN-LOOP GAIN	V_O = ±10 V										
	R_{LOAD}≥500 Ω	**25**	45		**25**	45		**25**	45		V/mV
	T_{min}–T_{max}	12			**20**			**12**			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}≥500 Ω										
	T_{min}–T_{max}	±10			**±10**			**±10**			V
Current	V_{OUT} = ±10 V	**50**			**50**			**50**			mA
OUTPUT RESISTANCE	Open Loop		5			5			5		Ω
FREQUENCY RESPONSE											
Unity Gain Bandwidth	V_{OUT} = 90 mV p–p		40			40			40		MHz
Full Power Bandwidth[2]	V_O = 20 V p–p										
	R_{LOAD}≥500 Ω	3.1	4.7		3.1	4.7		3.1	4.7		MHz
Rise Time[3]	A_V = −1		10			10			10		ns
Overshoot[3]	A_V = −1		10			10			10		%
Slew Rate[3]	A_V = −1	200	300		200	300		200	300		V/μs
Settling Time – 10 V Step	A_V = −1										
	to 0.1%		90			90			90		ns
	to 0.01%		110			110			110		ns
OVERDRIVE RECOVERY	−Overdrive		200			200			200		ns
	+Overdrive		700			700			700		ns
DIFFERENTIAL GAIN	f = 4.4 MHz		0.03			0.03			0.03		%
Differential Phase	f = 4.4 MHz		0.022			0.022			0.022		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±5**		**±18**	±5		**±18**	±5		**±18**	V
Quiescent Current			11	**12**		11	**12**		11	**12**	mA
	T_{min}–T_{max}			14			**14**			**16**	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±18 V	**86**	100		**90**	100		**86**	100		dB
	T_{min}–T_{max}	80			**86**			**80**			dB
TEMPERATURE RANGE											
Rated Performance[4]		0		+75	0		+75	−55		+125	°C
PACKAGE OPTIONS[5]											
LCC (E-20A)[6]								AD841SE, AD841SE/883B			
Cerdip (Q-14)		AD841JQ			AD841KQ			AD841SQ, AD841SQ/883B			
Plastic (N-14)		AD841JN			AD841KN						
TO-8 (H-12)		AD841JH			AD841KH			AD841SH, AD841SH/883B			
J and S Grade Chips Also Available		AD841J CHIP						AD841S CHIP			

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.

[2]Full power bandwidth = Slew Rate/2π V_{PEAK}.

[3]Refer to Figure 19.

[4]"S" grade T_{min} and T_{max} specifications are tested with automatic test equipment at T_A = −55°C and T_A = +125°C.

[5]For outline information see Package Information section.

[6]Contact factory for availability.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
TO-8 (H) . . . . . 1.4 W
Plastic (N) . . . . . 1.5 W
Cerdip (Q) . . . . . 1.3 W
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Storage Temperature Range
Q, H, E . . . . . −65°C to +150°C
N . . . . . −65°C to +125°C
Junction Temperature . . . . . +175°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C.

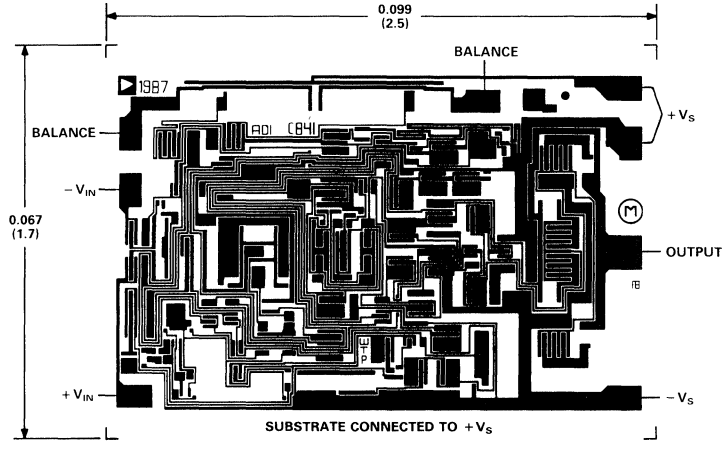
Thermal Characteristics:

	θ_{JC}	θ_{JA}	θ_{SA}	
Cerdip Package	35°C/W	110°C/W	38°C/W	Recommended Heat Sink:
TO-8 Package	30°C/W	100°C/W	37°C/W	Aavid Engineering ©#602B
Plastic Package	30°C/W	100°C/W		
LCC Package	35°C/W	150°C/W		

2

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



AD841—Typical Characteristics (at +25°C and V_S = ±15 V, unless otherwise noted.

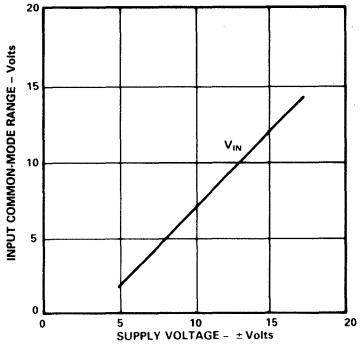


Figure 1. Input Common-Mode Range vs. Supply Voltage

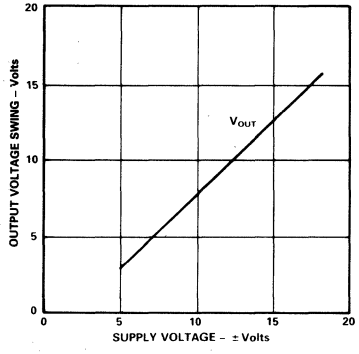


Figure 2. Output Voltage Swing vs. Supply Voltage

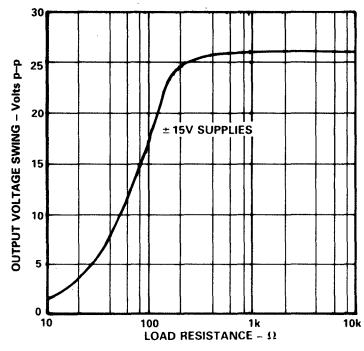


Figure 3. Output Voltage Swing vs. Load Resistance

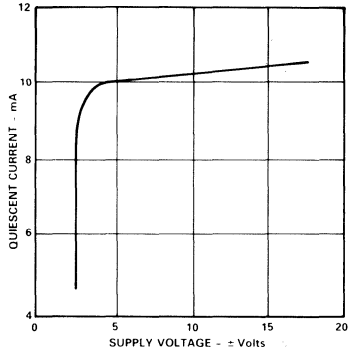


Figure 4. Quiescent Current vs. Supply Voltage

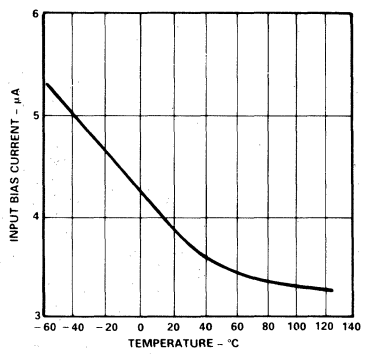


Figure 5. Input Bias Current vs. Temperature

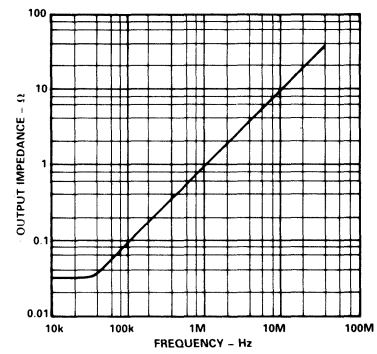


Figure 6. Output Impedance vs. Frequency

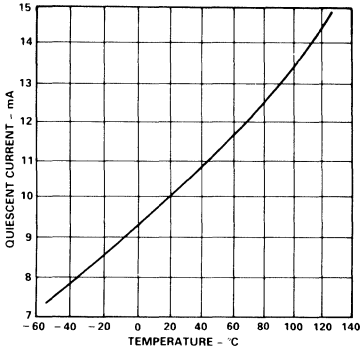


Figure 7. Quiescent Current vs. Temperature

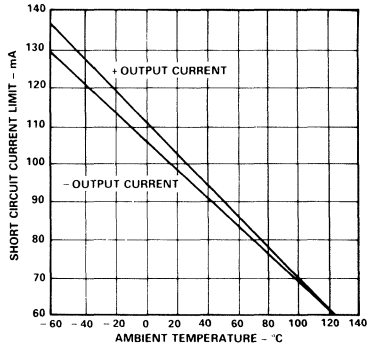


Figure 8. Short-Circuit Current Limit vs. Temperature

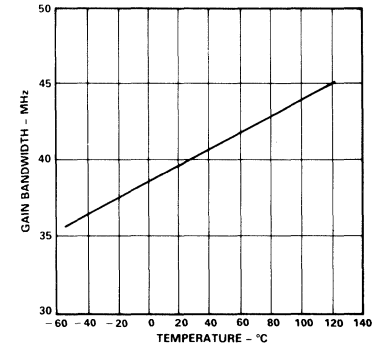


Figure 9. Gain Bandwidth Product vs. Temperature

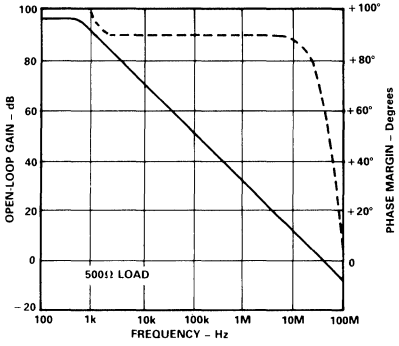


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

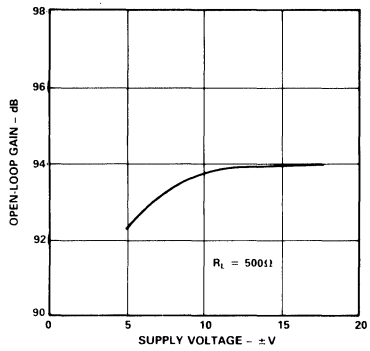


Figure 11. Open-Loop Gain vs. Supply Voltage

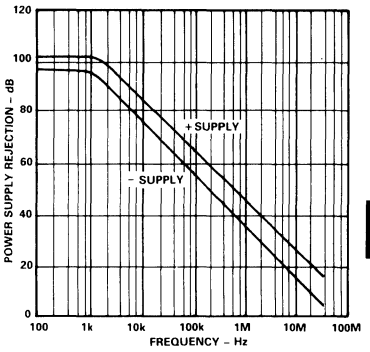


Figure 12. Power Supply Rejection vs. Frequency

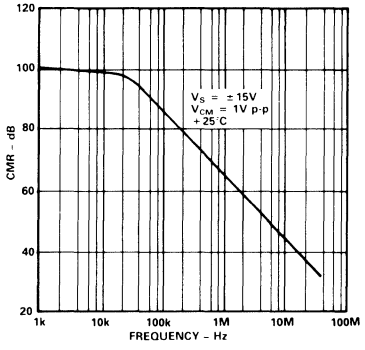


Figure 13. Common-Mode Rejection vs. Frequency

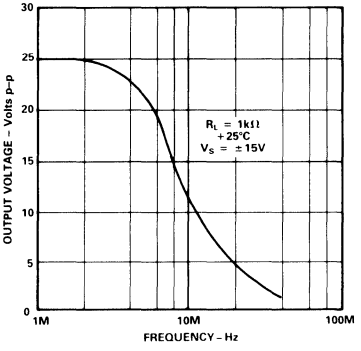


Figure 14. Large Signal Frequency Response

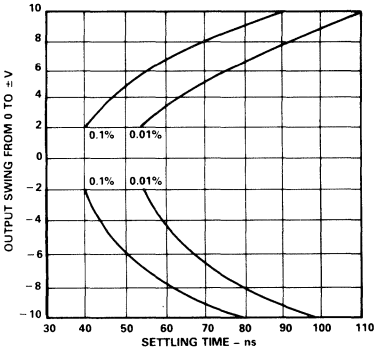


Figure 15. Output Swing and Error vs. Settling Time

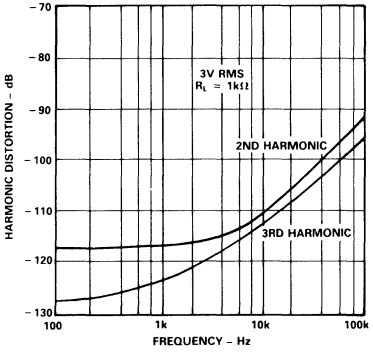


Figure 16. Harmonic Distortion vs. Frequency

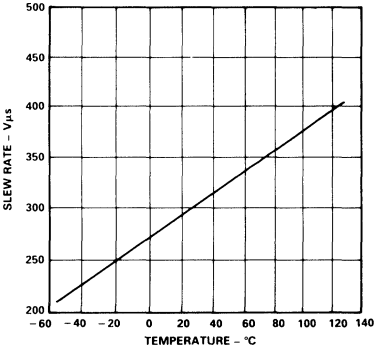


Figure 17. Slew Rate vs. Temperature

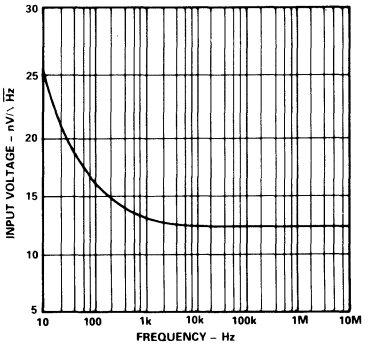


Figure 18. Input Noise Voltage Spectral Density

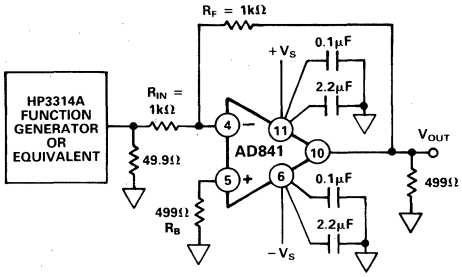


Figure 19a. Inverting Amplifier Configuration (DIP Pinout)

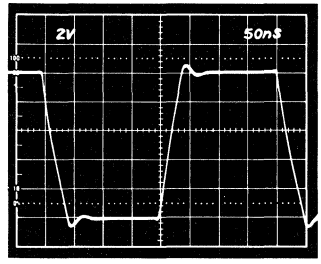


Figure 19b. Inverter Large Signal Pulse Response

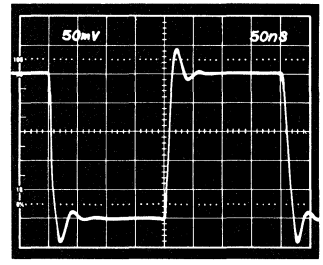


Figure 19c. Inverter Small Signal Pulse Response

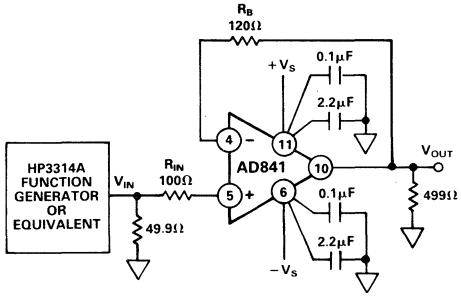


Figure 20a. Unity-Gain Buffer Amplifier Configuration (DIP Pinout)

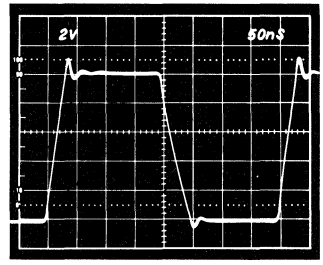


Figure 20b. Buffer Large Signal Pulse Response

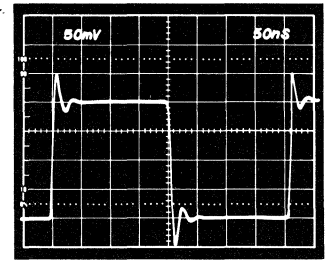


Figure 20c. Buffer Small Signal Pulse Response

OFFSET NULLING

The input offset voltage of the AD841 is very low for a high speed op amp, but if additional nulling is required, the circuit shown in Figure 21 can be used.

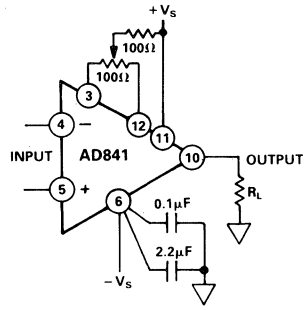


Figure 21. Offset Nulling (DIP Pinout)

INPUT CONSIDERATIONS

An input resistor (R_{IN} in Figure 20) is recommended in circuits where the input to the AD841 will be subjected to transient or continuous overload voltages exceeding the ±6 V maximum differential limit. This resistor provides protection for the input transistors by limiting the maximum current that can be forced into the input.

For high performance circuits it is recommended that a resistor (R_B in Figures 19 and 20) be used to reduce bias current errors by matching the impedance at each input. The output voltage error caused by the offset current is more than an order of magnitude less than the error present if the bias current error is not removed.

AD841 SETTLING TIME

Figures 22 and 24 show the settling performance of the AD841 in the test circuit shown in Figure 23.

Settling time is defined as:

> The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

This definition encompasses the major components which comprise settling time. They include (1) propagation delay through the amplifier; (2) slewing time to approach the final output value; (3) the time of recovery from the overload associated with slewing and (4) linear settling to within the specified error band.

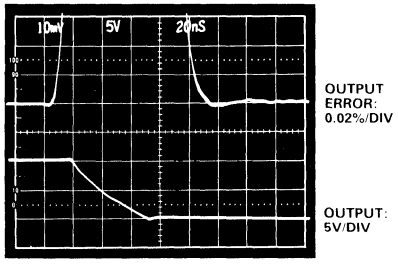


Figure 22. AD841 0.01% Settling Time

Expressed in these terms, the measurement of settling time is obviously a challenge and needs to be done accurately to assure the user that the amplifier is worth consideration for the application.

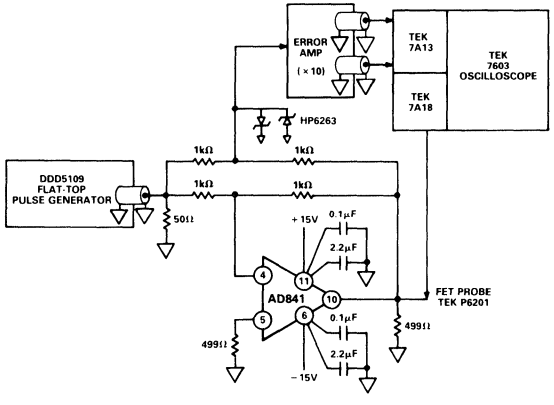


Figure 23. Settling Time Test Circuit

Measurement of the AD841's 0.01% settling in 110 ns was accomplished by amplifying the error signal from a false summing junction with a very high speed proprietary hybrid error amplifier specially designed to enable testing of small settling errors. The device under test was driving a 500 Ω load. The input to the error amp is clamped in order to avoid possible problems associated with the overdrive recovery of the oscilloscope input amplifier. The error amp gains the error from the false summing junction by 10, and it contains a gain vernier to fine trim the gain.

Figure 24 shows the "long term" stability of the settling characteristics of the AD841 output after a 10 V step. There is no evidence of settling tails after the initial transient recovery time. The use of a junction isolated process, together with careful layout, avoids these problems by minimizing the effects of transistor isolation capacitance discharge and thermally induced shifts in circuit operating points. These problems do not occur even under high output current conditions.

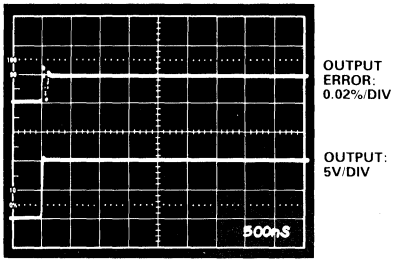


Figure 24. AD841 Settling Demonstrating No Settling Tails

GROUNDING AND BYPASSING

In designing practical circuits with the AD841, the user must remember that whenever high frequencies are involved, some special precautions are in order. Circuits must be built with short interconnect leads. Large ground planes should be used whenever possible to provide a low resistance, low inductance circuit path, as well as minimizing the effects of high frequency coupling. Sockets should be avoided because the increased interlead capacitance can degrade bandwidth.

Feedback resistors should be of low enough value to assure that the time constant formed with the circuit capacitances will not limit the amplifier performance. Resistor values of less than 5 kΩ are recommended. If a larger resistor must be used, a small (<10 pF) feedback capacitor in parallel with the feedback resistor, R_F, may be used to compensate for these stray capacitances and optimize the dynamic performance of the amplifier in the particular application.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. A 2.2 μF capacitor in parallel with a 0.1 μF ceramic disk capacitor is recommended.

CAPACITIVE LOAD DRIVING ABILITY

Like all wideband amplifiers, the AD841 is sensitive to capacitive loading. The AD841 is designed to drive capacitive loads of up to 20 pF without degradation of its rated performance. Capacitive loads of greater than 20 pF will decrease the dynamic performance of the part although instability should not occur unless the load exceeds 100 pF (for a unity-gain follower). A resistor in series with the output can be used to decouple larger capacitive loads.

Figure 25 shows a typical configuration for driving a large capacitive load. The 51 Ω output resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 51 Ω resistor and the load capacitance, C_L.

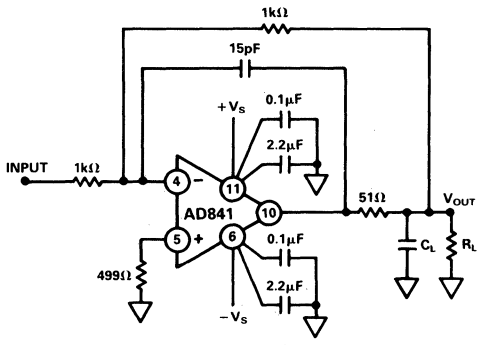


Figure 25. Circuit for Driving a Large Capacitive Load

USING A HEAT SINK

The AD841 draws less quiescent power than most precision high speed amplifiers and is specified for operation without a heat sink. However, when driving low impedance loads, the current to the load can be 4 to 5 times the quiescent current. This will create a noticeable temperature rise. Improved performance can be achieved by using a small heat sink such as the Aavid Engineering #602B.

TERMINATED LINE DRIVER

The AD841 functions very well as a high speed line driver of either terminated or unterminated cables. Figure 26 shows the AD841 driving a doubly terminated cable in a follower configuration. The AD841 maintains a typical slew rate of 300 V/μs, which means it can drive a ±10 V, 4.7 MHz signal or a ±3 V, 15.9 MHz signal.

The termination resistor, R_T, (when equal to the characteristic impedance of the cable) minimizes reflections from the far end of the cable. A back-termination resistor (R_{BT}, also equal to the characteristic impedance of the cable) may be placed between the AD841 output and the cable in order to damp any stray signals caused by a mismatch between R_T and the cable's characteristic impedance.This will result in a "cleaner" signal, but since 1/2 the output voltage will be dropped across R_{BT}, the op amp must supply double the output signal required if there is no back termination. Therefore the full power bandwidth is cut in half.

If termination is not used, cables appear as capacitive loads. If this capacitive load is large, it should be decoupled from the AD841 by a resistor in series with the output (see above: Driving a Capacitive Load).

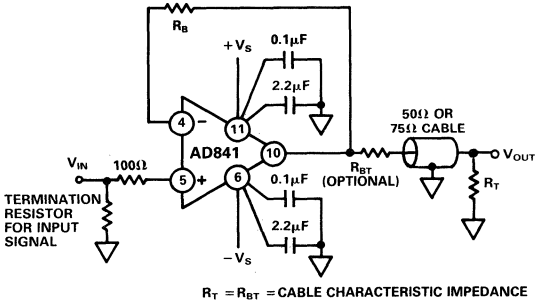


Figure 26. Line Driver Configuration

OVERDRIVE RECOVERY

Figure 27 shows the overdrive recovery capability of the AD841. Typical recovery time is 200 ns from negative overdrive and 700 ns from positive overdrive.

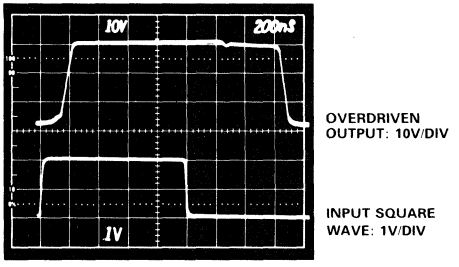


Figure 27. Overdrive Recovery

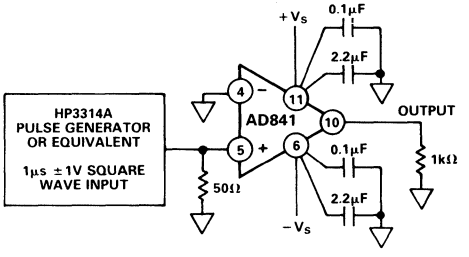


Figure 28. Overdrive Recovery Test Circuit

Wideband, High Output Current, Fast Settling Op Amp

AD842

FEATURES

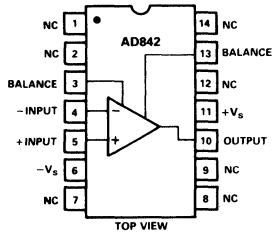
AC PERFORMANCE
- Gain Bandwidth Product: 80 MHz (Gain = 2)
- Fast Settling: 100 ns to 0.01% for a 10 V Step
- Slew Rate: 375 V/μs
- Stable at Gains of 2 or Greater
- Full Power Bandwidth: 6.0 MHz for 20 V p–p

DC PERFORMANCE
- Input Offset Voltage: 1 mV max
- Input Offset Drift: 14 μV/°C
- Input Voltage Noise: 9 nV/$\sqrt{Hz}$ typ
- Open-Loop Gain: 90 V/mV into a 500 Ω Load
- Output Current: 100 mA min
- Quiescent Supply Current: 14 mA max

APPLICATIONS
- Line Drivers
- DAC and ADC Buffers
- Video and Pulse Amplifiers
- Available in Plastic DIP Hermetic Metal Can, Hermetic Cerdip and LCC Packages and in Chip Form
- MIL-STD-883B Parts Available

CONNECTION DIAGRAMS

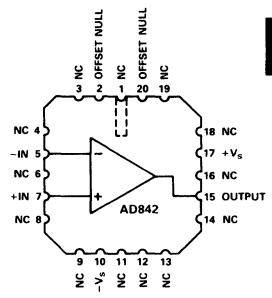
Plastic DIP (N) Package and Cerdip (Q) Package



TOP VIEW

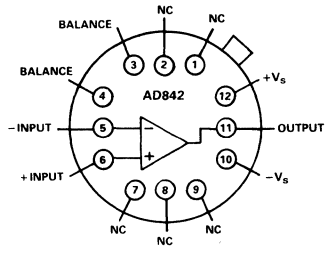
NC = NO CONNECT

LCC (E) Package



NC = NO CONNECT

TO-8 (H) Package



TOP VIEW

NOTE: CAN TIED TO V+
NC = NO CONNECT

PRODUCT DESCRIPTION

The AD842 is a member of the Analog Devices family of wide bandwidth operational amplifiers. This family includes, among others, the AD840 which is stable at a gain of 10 or greater and the AD841 which is unity-gain stable. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to its 80 MHz gain bandwidth, the AD842 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in less than 100 ns for a 10 volt step.

The AD842 also offers a low quiescent current of 13 mA, a high output current drive capability (100 mA minimum), a low input voltage noise of 9 nV$\sqrt{Hz}$ and a low input offset voltage (1 mV maximum).

The 375 V/μs slew rate of the AD842, along with its 80 MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is ideally suited for use in high frequency signal conditioning circuits and wide bandwidth active filters. The extremely rapid settling time of the AD842 makes this amplifier the preferred choice for data acquisition applications which require 12-bit accuracy. The AD842 is also appropriate for other applications such as high speed DAC and ADC buffer amplifiers and other wide bandwidth circuitry.

APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD842 make it ideal for DAC and ADC buffers amplifiers, lines drivers and all types of video instrumentation circuitry.
2. The AD842 is a precision amplifier. It offers accuracy to 0.01% or better and wide bandwidth; performance previously available only in hybrids.
3. Laser-wafer trimming reduces the input offset voltage of 1 mV max, thus eliminating the need for external offset nulling in many applications.
4. Full differential inputs provide outstanding performance in all standard high frequency op amp applications where the circuit gain will be 2 or greater.
5. The AD842 is an enhanced replacement for the HA2542.

AD842—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD842J Min	AD842J Typ	AD842J Max	AD842K Min	AD842K Typ	AD842K Max	AD842S Min	AD842S Typ	AD842S Max	Units
INPUT OFFSET VOLTAGE[1]			0.5	**1.5**		0.3	**1.0**		0.5	1.5	mV
	T_{min}–T_{max}			2.5			**1.5**			3.5	mV
Offset Drift			14			14			14		μV/°C
INPUT BIAS CURRENT			4.2	**8**		3.5	**5**		4.2	**8**	μA
	T_{min}–T_{max}			10			**6**			**12**	μA
Input Offset Current			0.1	**0.4**		0.05	**0.2**		0.1	**0.4**	μA
	T_{min}–T_{max}			0.5			**0.3**			**0.6**	μA
INPUT CHARACTERISTICS											
Input Resistance	Differential Mode		100			100			100		kΩ
Input Capacitance			2.0			2.0			2.0		pF
INPUT VOLTAGE RANGE											
Common Mode		**± 10**			**±10**			**±10**			V
Common-Mode Rejection	V_{CM} = ±10 V	**86**	115		**90**	115		**86**	115		dB
	T_{min}–T_{max}	80			**86**			**80**			dB
INPUT VOLTAGE NOISE	f = 1 kHz		9			9			9		nV/√Hz
Wideband Noise	10 Hz to 10 MHz		28			28			28		μV rms
OPEN-LOOP GAIN	V_O = ±10 V										
	R_{LOAD}≥500 Ω	**40**	90		**50**	90		**40**	90		V/mV
	T_{min}–T_{max}	20			**25**			**20**			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}≥500 Ω	**± 10**			**±10**			**±10**			V
Current	V_{OUT} = ±10 V	**100**			**100**			**100**			mA
	Open Loop		5			5			5		Ω
FREQUENCY RESPONSE											
Gain Bandwidth Product	V_{OUT} = 90 mV		80			80			80		MHz
Full Power Bandwidth[2]	V_O = 20 V p–p										
	R_{LOAD}≥500 Ω	4.7	6		4.7	6		4.7	6		MHz
Rise Time[3]	A_{VCL} = −2		10			10			10		ns
Overshoot[3]	A_{VCL} = −2		20			20			20		%
Slew Rate[3]	A_{VCL} = −2	300	375		300	375		300	375		V/μs
Settling Time[3]	10 V Step										
	to 0.1%		80			80			80		ns
	to 0.01%		100			100			100		ns
Differential Gain	f = 4.4 MHz		0.015			0.015			0.015		%
Differential Phase	f = 4.4 MHz		0.035			0.035			0.035		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±5**		**±18**	**±5**		**±18**	**±5**		**±18**	V
Quiescent Current			13	**14**		13	**14**		13	**14**	mA
	T_{min}–T_{max}			16			**16**			**19**	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±15 V	**86**	100		**90**	105		**86**	100		dB
	T_{min}–T_{max}	80			**86**			**80**			dB
TEMPERATURE RANGE											
Rated Performance[4]		0		+75	0		+75	−55		+125	°C
PACKAGE OPTIONS[5]											
Plastic (N-14)			AD842JN			AD842KN					
Cerdip (Q-14)			AD842JQ			AD842KQ			AD842SQ, AD842SQ/883B		
TO-8 (H-12A)			AD842JH			AD842KH			AD842SH		
LCC[6] (E-20A)									AD842SE		
J and S Grade Chips Also Available											

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.
[2]FPBW Slew Rate/2π V_{PEAK}.
[3]Refer to Figures 22 and 23.
[4]"S" grade T_{min} and T_{max} specifications are tested with automatic test equipment at T_A = −55°C and T_A = +125°C.
[5]For outline information see Package Information section.
[6]Contact factory for availability.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) . . . . . 1.5 W
Cerdip (Q) . . . . . 1.1 W
TO-8 . . . . . 1.3 W
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Storage Temperature Range
Q, H . . . . . −65°C to +150°C
N . . . . . −65°C to +125°C
Junction Temperature . . . . . +175°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTE
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_J does not exceed +150°C at an ambient temperature of +25°C.

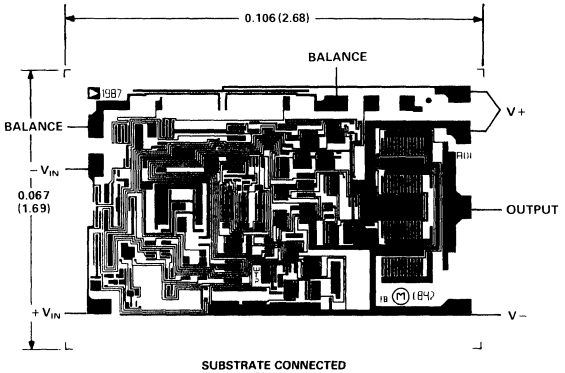
Thermal Characteristics:

	θ_{JC}	θ_{JA}	θ_{SA}
Plastic Package	30°C/W	100°C/W	
Cerdip Package	30°C/W	110°C/W	38°C/W
TO-8 Package	30°C/W	100°C/W	27°C/W

Recommended heat sink: Aavid Engineering© #602B

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



SUBSTRATE CONNECTED TO $+V_S$

2

AD842—Typical Characteristics (at +25°C and V_S = ±15 V, unless otherwise noted.)

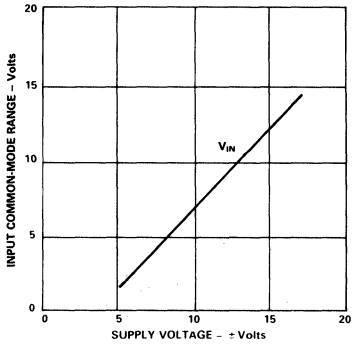


Figure 1. Input Common-Mode Range vs. Supply Voltage

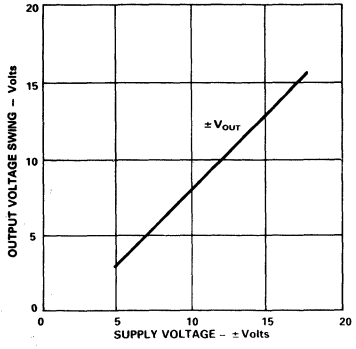


Figure 2. Output Voltage Swing vs. Supply Voltage

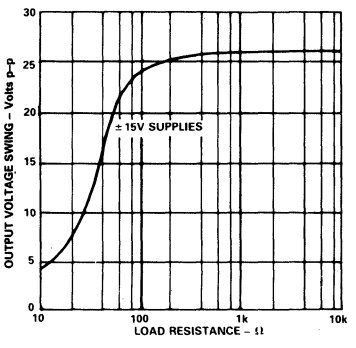


Figure 3. Output Voltage Swing vs. Load Resistance

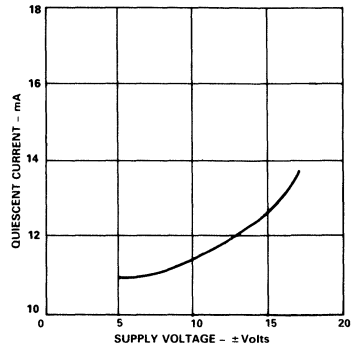


Figure 4. Quiescent Current vs. Supply Voltage

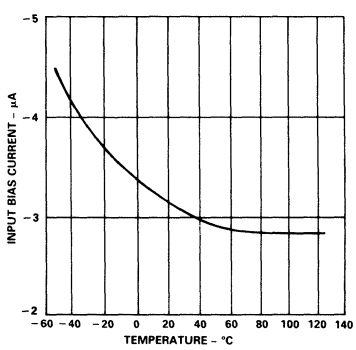


Figure 5. Input Bias Current vs. Temperature

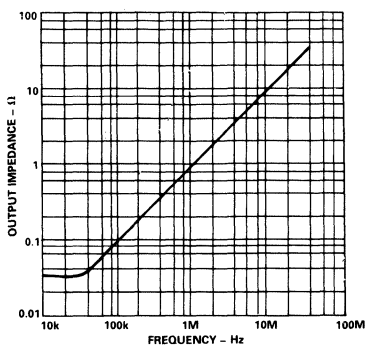


Figure 6. Output Impedance vs. Frequency

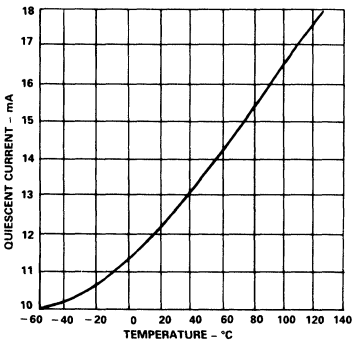


Figure 7. Quiescent Current vs. Temperature

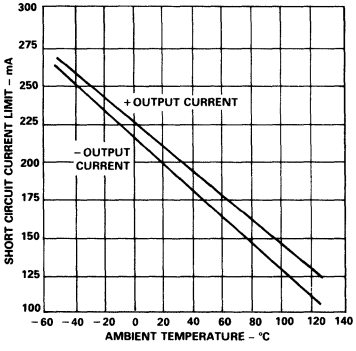


Figure 8. Short-Circuit Current Limit vs. Temperature

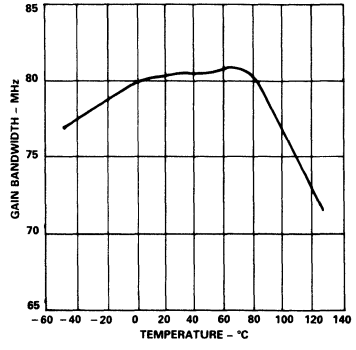


Figure 9. Gain Bandwidth Product vs. Temperature

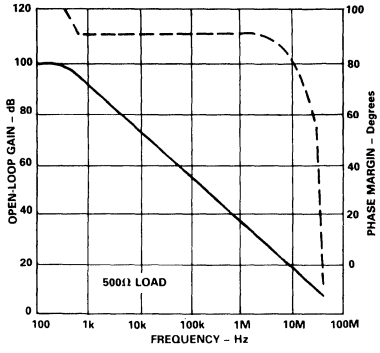


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

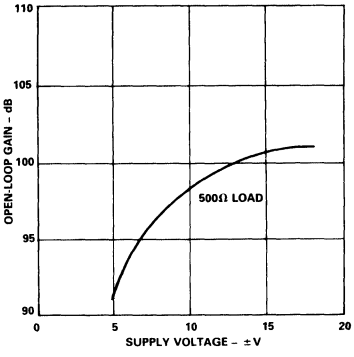


Figure 11. Open-Loop Gain vs. Supply Voltage

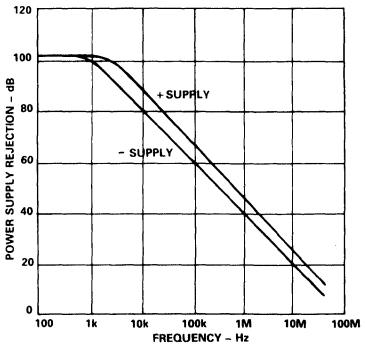


Figure 12. Power Supply Rejection vs. Frequency

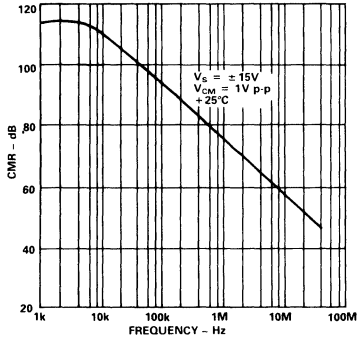


Figure 13. Common-Mode Rejection vs. Frequency

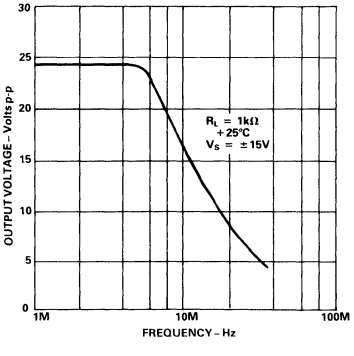


Figure 14. Large Signal Frequency Response

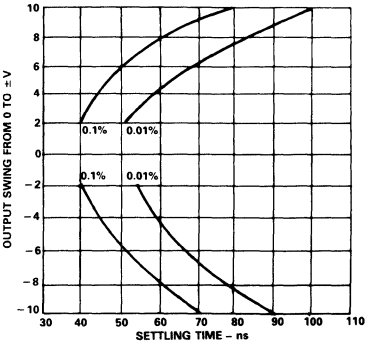


Figure 15. Output Swing and Error vs. Settling Time

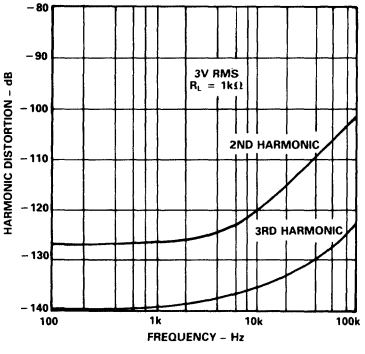


Figure 16. Harmonic Distortion vs. Frequency

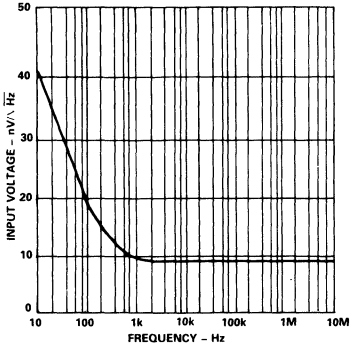


Figure 17. Input Voltage vs. Frequency

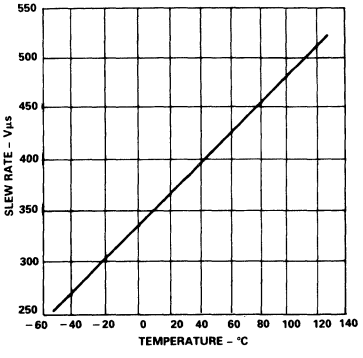


Figure 18. Slew Rate vs. Temperature

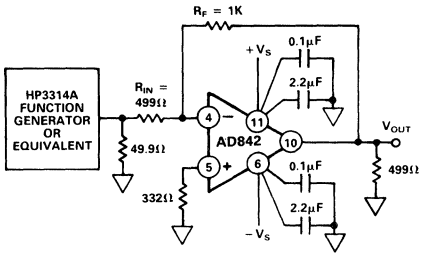


Figure 19a. Inverting Amplifier Configuration (DIP Pinout)

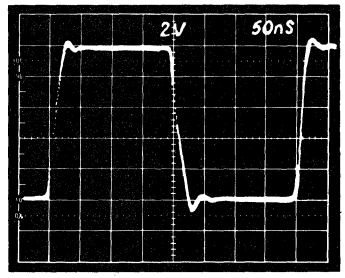


Figure 19b. Inverter Large Signal Pulse Response

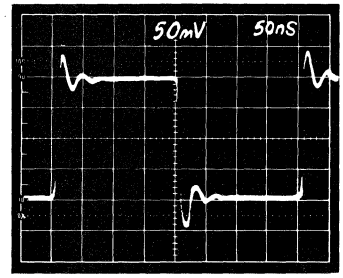


Figure 19c. Inverter Small Signal Pulse Response

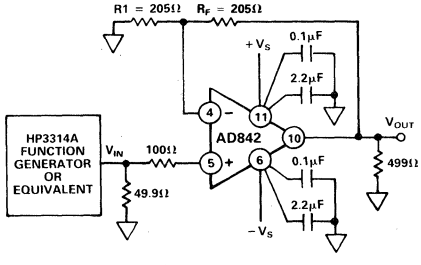


Figure 20a. Noninverting Amplifier Configuration (DIP Pinout)

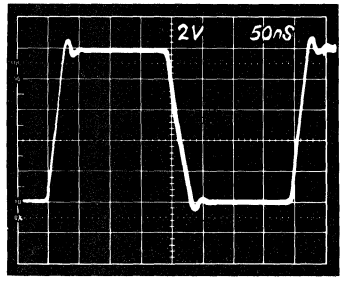


Figure 20b. Noninverting Large Signal Pulse Response

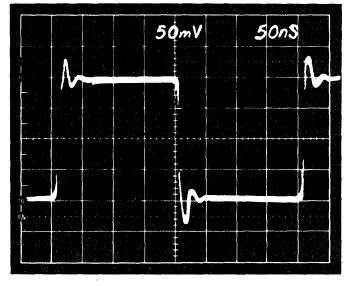


Figure 20c. Noninverting Small Signal Pulse Response

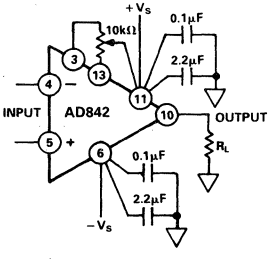


Figure 21. Offset Nulling (DIP Pinout)

OFFSET NULLING

The input offset voltage of the AD842 is very low for a high speed op amp, but if additional nulling is required, the circuit shown in Figure 21 can be used.

AD842 SETTLING TIME

Figures 22 and 24 show the settling performance of the AD842 in the test circuit shown in Figure 23.

Settling time is defined as:

> The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

This definition encompasses the major components which comprise settling time. They include: (1) propagation delay through the amplifier; (2) slewing time to approach the final output value; (3) the time of recovery from the overload associated with slewing; and (4) linear settling to within the specified error band.

Expressed in these terms, the measurement of settling time is obviously a challenge and needs to be done accurately to assure the user that the amplifier is worth consideration for the application.

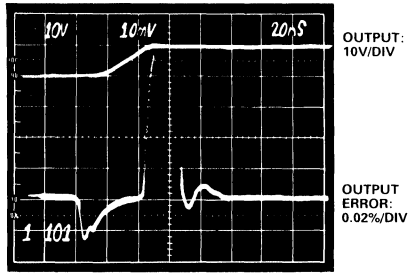


Figure 22. AD842 0.01% Settling Time

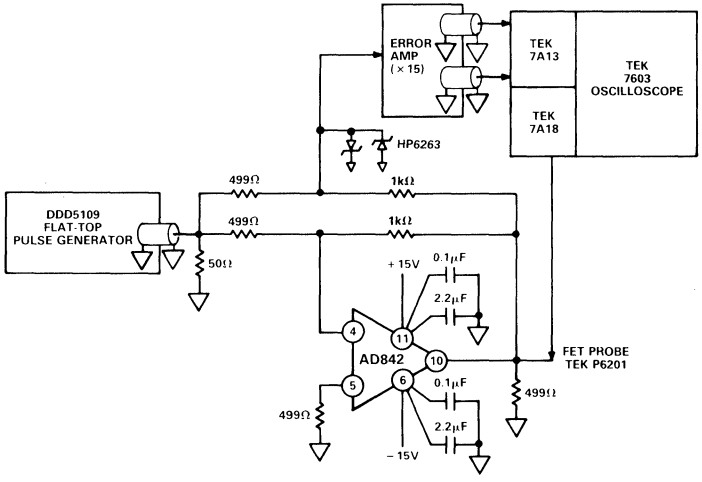


Figure 23. Settling Time Test Circuit

Figure 23 shows how measurement of the AD842's 0.01% settling in 100 ns was accomplished by amplifying the error signal from a false summing junction with a very high-speed proprietary hybrid error amplifier specially designed to enable testing of small settling errors. The device under test was driving a 300 Ω load. The input to the error amp is clamped in order to avoid possible problems associated with the overdrive recovery of the oscilloscope input amplifier. The error amp gains the error from the false summing junction by 15, and it contains a gain vernier to fine trim the gain.

Figure 24 shows the "long term" stability of the settling characteristics of the AD842 output after a 10 V step. There is no evidence of settling tails after the initial transient recovery time. The use of a junction isolated process, together with careful layout, avoids these problems by minimizing the effects of transistor isolation capacitance discharge and thermally induced shifts in circuit operating points. These problems do not occur even under high output current conditions.

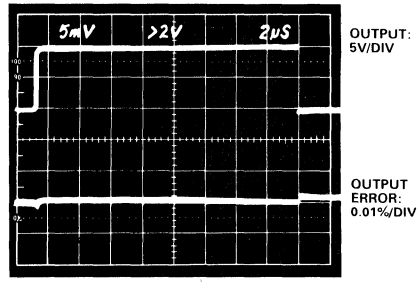


Figure 24. AD842 Settling Demonstrating No Settling Tails

GROUNDING AND BYPASSING

In designing practical circuits with the AD842, the user must remember that whenever high frequencies are involved, some special precautions are in order. Circuits must be built with short interconnect leads. Large ground planes should be used whenever possible to provide a low resistance, low inductance circuit path, as well as minimizing the effects of high frequency coupling. Sockets should be avoided because the increased interlead capacitance can degrade bandwidth.

Feedback resistors should be of low enough value to assure that the time constant formed with the circuit capacitances will not limit the amplifier performance. Resistor values of less than 5 kΩ are recommended. If a larger resistor must be used, a small (<10 pF) feedback capacitor connected in parallel with the feedback resistor, R_F, may be used to compensate for these stray capacitances and optimize the dynamic performance of the amplifier in the particular application.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. A 2.2 μF capacitor in parallel with a 0.1 μF ceramic disk capacitor is recommended.

CAPACITIVE LOAD DRIVING ABILITY

Like all wideband amplifiers, the AD842 is sensitive to capacitive loading. The AD842 is designed to drive capacitive loads of up to 20 pF without degradation of its rated performance. Capacitive loads of greater than 20 pF will decrease the dynamic performance of the part although instability should not occur unless the load exceeds 100 pF.

USING A HEAT SINK

The AD842 draws less quiescent power than most precision high speed amplifiers and is specified for operation without a heat sink. However, when driving low impedance loads, the current to the load can be 10 times the quiescent current. This will create a noticeable temperature rise. Improved performance can be achieved by using a small heat sink such as the Aavid Engineering #602B.

TERMINATED LINE DRIVER

The AD842 is optimized for high speed line driver applications. Figure 25 shows the AD842 driving a doubly terminated cable in a gain-of-2 follower configuration. The AD842 maintains a typical slew rate of 375 V/μs, which means it can drive a ±10 V, 6.0 MHz signal or a ±3 V, 19.9 MHz signal.

The termination resistor, R_T, (when equal to the characteristic impedance of the cable) minimizes reflections from the far end of the cable. A back-termination resistor (R_{BT}, also equal to the characteristic impedance of the cable) may be placed between the AD842 output and the cable in order to damp any stray signals caused by a mismatch between R_T and the cable's characteristic impedance. This will result in a "cleaner" signal. With this circuit, the voltage on the line equals V_{IN} because one half of V_{OUT} is dropped across R_{BT}.

The AD842 has ±100 mA minimum output current and, therefore, can drive ±5 V into a 50 Ω cable.

The feedback resistors, R_1 and R_2, must be chosen carefully. Large value resistors are desirable in order to limit the amount of current drawn from the amplifier output. But large resistors can cause amplifier instability because the parallel resistance $R_1 \| R_2$ combines with the input capacitance (typically 2–5 pF) to create an additional pole. Also, the voltage noise of the AD842 is equivalent to a 5 kΩ resistor, so large resistors can significantly increase the system noise. Resistor values of 1 kΩ or 2 kΩ are recommended.

If termination is not used, cables appear as capacitive loads and can be decoupled from the AD842 by a resistor in series with the output.

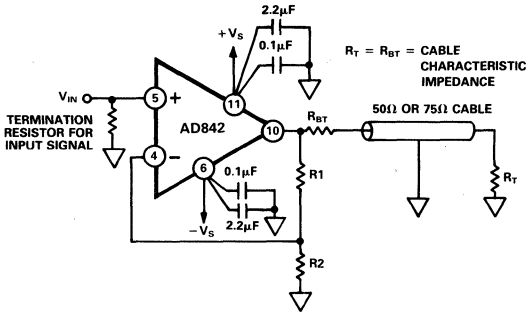


Figure 25. Line Driver Configuration

OVERDRIVE RECOVERY

Figure 26 shows the overdrive recovery capability of the AD842. Typical recovery time is 80 ns from negative overdrive and 400 ns from positive overdrive.

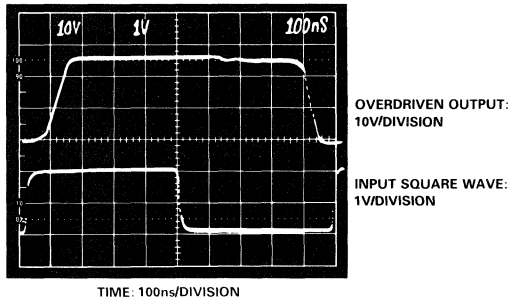


Figure 26. Overdrive Recovery

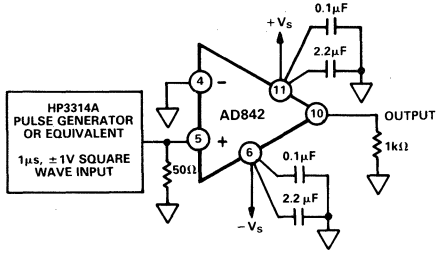


Figure 27. Overdrive Recovery Test Circuit

34 MHz, CBFET Fast Settling Op Amp

AD843

FEATURES

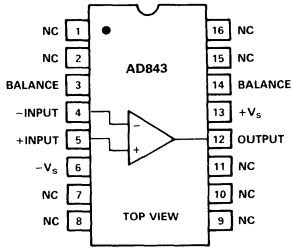
AC PERFORMANCE
- Unity Gain Bandwidth: 34 MHz
- Fast Settling: 135 ns to 0.01%
- Slew Rate: 250 V/μs
- Stable at Gains of 1 or Greater
- Full Power Bandwidth: 3.9 MHz

DC PERFORMANCE
- Input Offset Voltage: 1 mV max (AD843K/B)
- Input Bias Current: 0.6 nA typ
- Input Voltage Noise: 19 nV/$\sqrt{Hz}$
- Open Loop Gain: 30 V/mV into a 500 Ω Load
- Output Current: 50 mA min
- Supply Current: 13 mA max
- Available in 8-Pin Plastic Mini-DIP & Cerdip Packages, 20-Pin LCC and 12-Pin Hermetic Metal Cans
- Chips and MIL-STD-883B Parts Also Available

APPLICATIONS
- High Speed Sample-and-Hold Amplifiers
- High Bandwidth Active Filters
- High Speed Integrators
- High Frequency Signal Conditioning

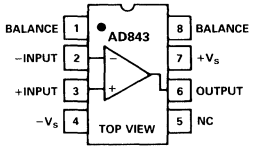
CONNECTION DIAGRAMS

16-Pin SOIC Package



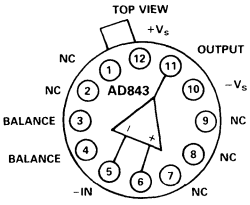
NC = NO CONNECT

Plastic (N) and Cerdip (Q) Package



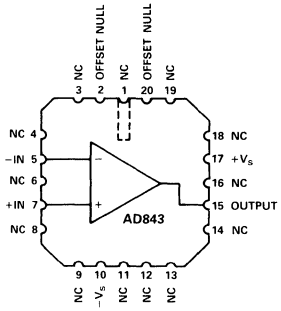
NC = NO CONNECT

TO-8 (H) Package



NOTE: CAN TIED TO V+
NC = NO CONNECT

LCC (E) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD843 is a fast settling, 34 MHz, CBFET input op amp. The AD843 combines the low (0.6 nA) input bias currents characteristic of a FET input amplifier while still providing a 34 MHz bandwidth and a 135 ns settling time (to within 0.01% of final value for a 10 volt step). The AD843 is a member of the Analog Devices' family of wide bandwidth operational amplifiers. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp.

The 250 V/μs slew rate and 0.6 nA input bias current of the AD843 ensure excellent performance in high speed sample-and-hold applications and in high speed integrators. This amplifier is also ideally suited for high bandwidth active filters and high frequency signal conditioning circuits.

Unlike many high frequency amplifiers, the AD843 requires no external compensation and it remains stable over its full operating temperature range. It is available in five performance grades: the AD843J and AD843K are rated over the commercial temperature range of 0°C to +70°C. The AD843A and AD843B are rated over the industrial temperature range of −40°C to +85°C. The AD843S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

The AD843 is offered in either 8-pin plastic DIP or hermetic cerdip packages, in 16-pin SOIC, or in a 12-pin metal can. Chips are also available.

PRODUCT HIGHLIGHTS

1. The high slew rate, fast settling time and low input bias current of the AD843 make it the ideal amplifier for 12-bit D/A and A/D buffers, for high speed sample-and-hold amplifiers and for high speed integrator circuits. The AD843 can replace many FET input hybrid amplifiers such as the LH0032, LH4104 and OPA600.
2. Fully differential inputs provide outstanding performance in all standard high frequency op amp applications such as signal conditioning and active filters.
3. Laser wafer trimming reduces the input offset voltage to 1 mV max (AD843K and AD843B).
4. Although external offset nulling is unnecessary in many applications, offset null pins are provided.
5. The AD843 does not require external compensation at closed loop gains of 1 or greater.

AD843—SPECIFICATIONS (@ T_A +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD843J/A Min	AD843J/A Typ	AD843J/A Max	AD843K/B Min	AD843K/B Typ	AD843K/B Max	AD843S Min	AD843S Typ	AD843S Max	Units
INPUT OFFSET VOLTAGE[1]			1.0	**2.0**		0.5	**1.0**		1.0	**2.0**	mV
	T_{min}–T_{max}		1.7	4.0		1.2	**2.0**		3.0	**4.5**	mV
Offset Drift			12			12	35		12		µV/°C
INPUT BIAS CURRENT	Initial (T_J = +25°C)		50			40			50		pA
	Warmed-Up[1]		0.8	**2.5**		0.6	**1.0**		0.8	**2.5**	nA
	T_{min}–T_{max}			60/160			23/65			2600	nA
INPUT OFFSET CURRENT	Initial (T_J = +25°C)		30			20			30		pA
	Warmed-Up[1]		0.25	**1.0**		0.2	**0.4**		0.25	**1.0**	nA
	T_{min}–T_{max}			23/64			9/26			1025	nA
INPUT CHARACTERISTICS											
Input Resistance			10^{10}			10^{10}			10^{10}		Ω
Input Capacitance			6			6			6		pF
INPUT VOLTAGE RANGE											
Common Mode		**±10**	+12, −13		**±10**	+12, −13		**±10**	+12, −13		V
COMMON MODE REJECTION	V_{CM} = ±10 V	**60**	72		**70**	76		**60**	72		dB
	T_{min}–T_{max}	60	72		**68**	76		**60**	72		dB
INPUT VOLTAGE NOISE	f = 10 kHz		19			19			19		nV/√Hz
Wideband Noise	10 Hz to 10 MHz		60			60			60		µV rms
OPEN LOOP GAIN	V_O = ±10 V										
	R_{LOAD}≥500 Ω	**15**	25		**20**	30		**15**	30		V/mV
	T_{min}–T_{max}	10	20		**10**	25		**10**	25		V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}≥500 Ω	**±10**	+11.5, −12.6		**±10**	+11.5, −12.6		**±10**	+11.5, −12.6		V
Current	V_{OUT} = ±10 V	**50**			**50**			**50**			mA
Output Resistance	Open Loop		12			12			12		Ω
FREQUENCY RESPONSE											
Unity Gain Bandwidth	V_{OUT} = 90 mV p–p		34			34			34		MHz
Full Power Bandwidth[2]	V_O = 20 V p–p										
	Rl≥500 Ω	2.5	3.9		2.5	3.9		2.5	3.9		MHz
Rise Time	A_{VCL} = −1		10			10			10		ns
Overshoot	A_{VCL} = −1		15			15			15		%
Slew Rate	A_{VCL} = −1	160	250		160	250		160	250		V/µs
Settling Time	10 V Step										
	A_{VCL} = −1										
	to 0.1%		95			95			95		ns
	to 0.01%		135			135			135		ns
Overdrive Recovery	−Overdrive		200			200			200		ns
	+Overdrive		700			700			700		ns
Differential Gain	f = 4.4 MHz		0.025			0.025			0.025		%
Differential Phase	f = 4.4 MHz		0.025			0.025			0.025		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current			12	**13**		12	**13**		12	**13**	mA
	T_{min}–T_{max}		12.3	14		12.3	**14**		12.5	**16**	mA
Rejection Ratio	±5 V to ±18 V	**65**	76		**70**	80		**65**	76		dB
Rejection Ratio	T_{min}–T_{max}	62	76		**68**	80		**62**	76		dB
TEMPERATURE RANGE											
Operating, Rated Performance											
Commercial (0 to +70°C)			AD843J			AD843K					
Industrial (−40°C to +85°C)			AD843A			AD843B					
Military (−55°C to +125°C)[3]									AD843S		
PACKAGE OPTIONS[4]											
Plastic (N)			AD843JN			AD843KN					
Cerdip (Q)			AD843AQ			AD843BQ			AD843SQ, AD843SQ/883B		
Metal Can (H)						AD843BH			AD843SH		
LCC (E)[5]									AD843SE, AD843SE/883B		
SOIC (R)			AD843JR								

NOTES
[1]Specifications are guaranteed after 5 minutes at $T_A = +25°C$.
[2]Full power bandwidth = Slew Rate/2 πV peak.
[3]All "S" grade T_{min}–T_{max} specifications are tested with automatic test equipment at $T_A = -55°C$ and $T_A = +125°C$.
[4]For outline information see Package Information section.
[5]Contact factory for availability.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed although only those shown in **boldface** are tested on all production units.

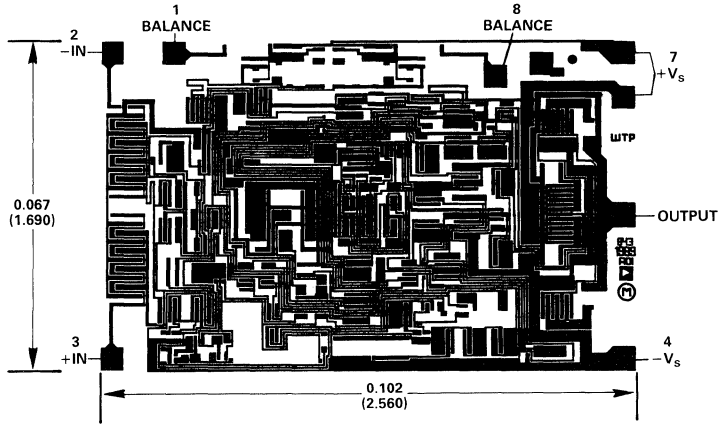
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
  Plastic Package . . . . . 1.50 Watts
  Cerdip Package . . . . . 1.35 Watts
  12-Pin Header Package . . . . . 1.80 Watts
  20-Pin LCC Package . . . . . 1.0 Watt
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (N, R) . . . . . −65°C to +150°C
Storage Temperature Range (Q, H) . . . . . −65°C to +125°C
Operating Temperature Range
  AD843J/K . . . . . 0 to +70°C
  AD843A/B . . . . . −40°C to +85°C
  AD843S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: $\theta_{JA} = 100°C/Watt$
8-Pin Cerdip Package: $\theta_{JA} = 110°C/Watt$
12-Pin Header Package: $\theta_{JA} = 80°C/Watt$
20-Pin LCC Package: $Q_{JA} = 150°C/Watt$

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



AD843—Typical Characteristics

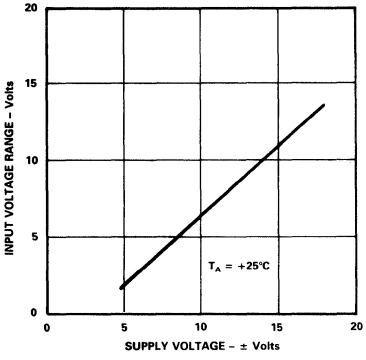


Figure 1. Input Voltage Range vs. Supply Voltage

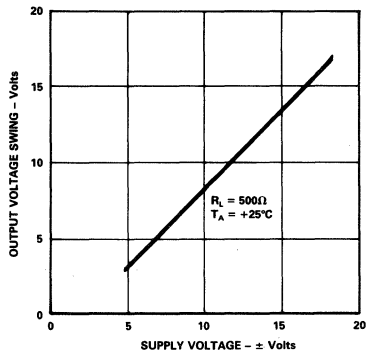


Figure 2. Output Voltage Swing vs. Supply Voltage

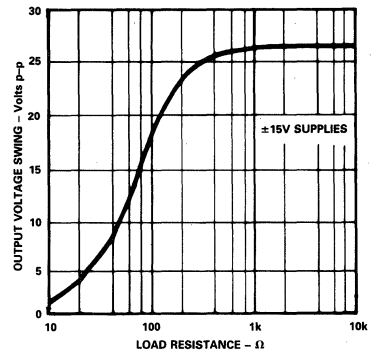


Figure 3. Output Voltage Swing vs. Load Resistance

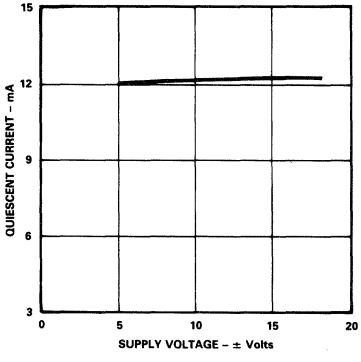


Figure 4. Quiescent Current vs. Supply Voltage

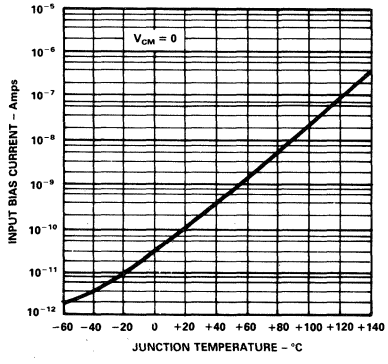


Figure 5. Input Bias Current vs. Junction Temperature

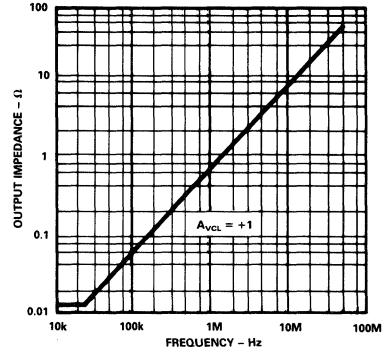


Figure 6. Output Impedance vs. Frequency

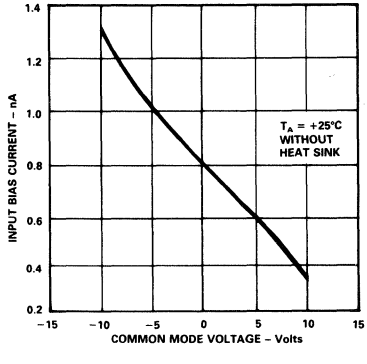


Figure 7. Input Bias Current vs. Common Mode Voltage

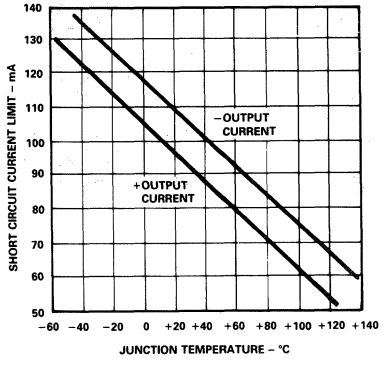


Figure 8. Short Circuit Current Limit vs. Junction Temperature (T_J)

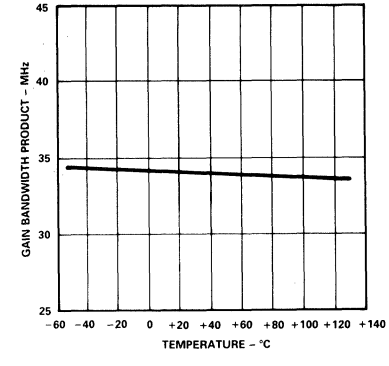


Figure 9. Gain Bandwidth Product vs. Temperature

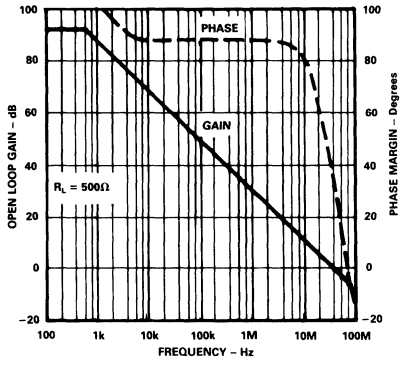


Figure 10. Open Loop Gain and Phase Margin vs. Frequency

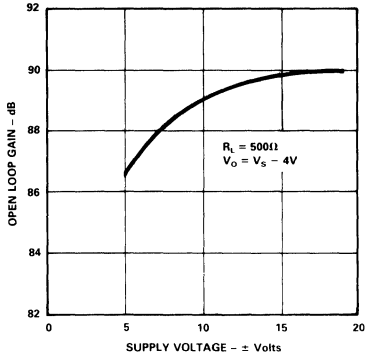


Figure 11. Open Loop Gain vs. Supply Voltage

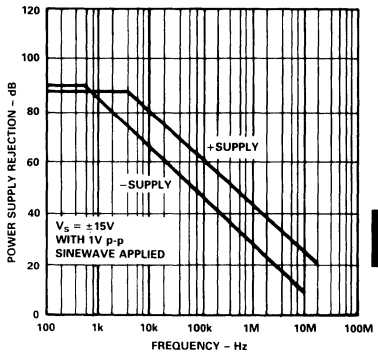


Figure 12. Power Supply Rejection vs. Frequency

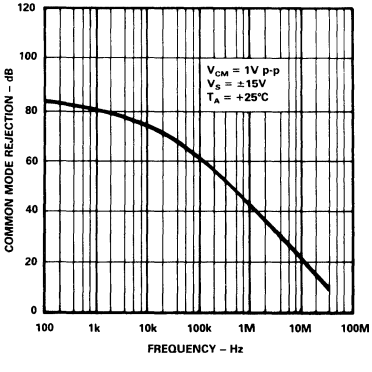


Figure 13. Common Mode Rejection vs. Frequency

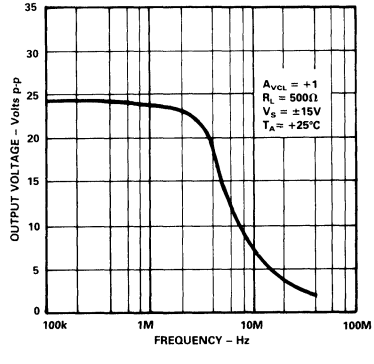


Figure 14. Large Signal Frequency Response

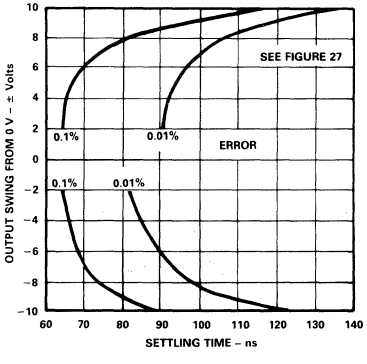


Figure 15. Output Swing and Error vs. Settling Time

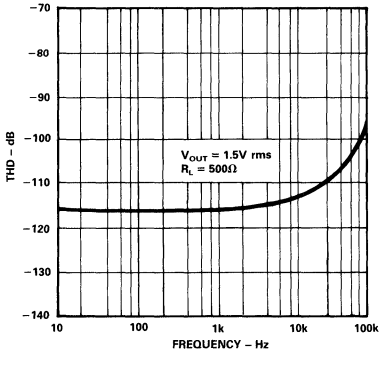


Figure 16. Harmonic Distortion vs. Frequency

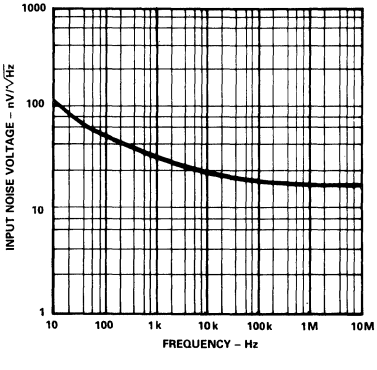


Figure 17. Input Noise Voltage Spectral Density

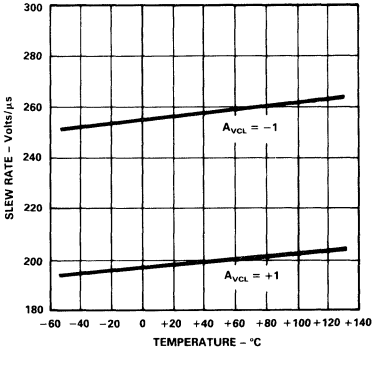


Figure 18. Slew Rate vs. Temperature

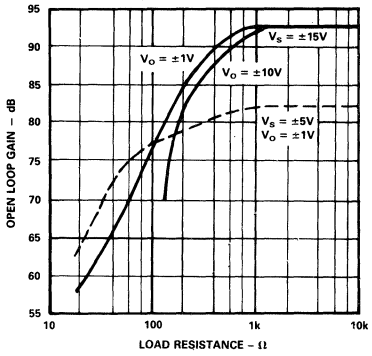


Figure 19. Open Loop Gain vs. Resistive Load

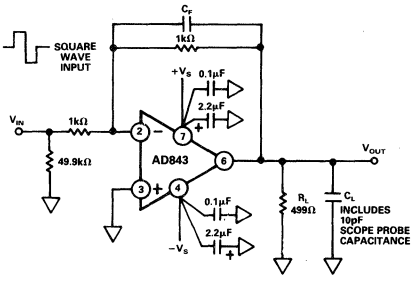


Figure 20a. Inverting Amplifier Connection

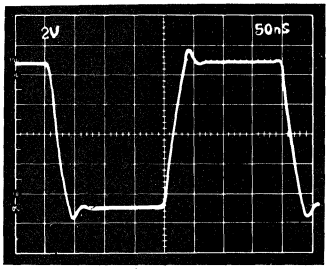


Figure 20b. Inverter Large Signal Pulse Response. C_F = 0, C_L = 10 pF

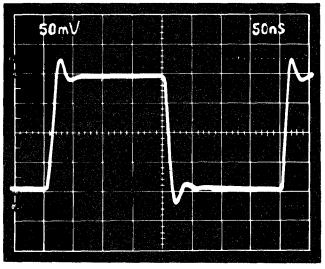


Figure 20c. Inverter Small Signal Pulse Response. C_F = 0, C_L = 10 pF

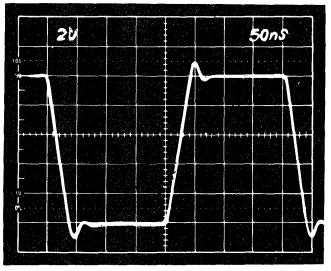


Figure 20d. Inverter Large Signal Pulse Response. C_F = 5 pF, C_L = 110 pF

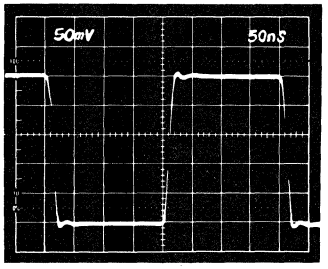


Figure 20e. Inverter Small Signal Pulse Response. C_F = 5 pF, C_L = 110 pF

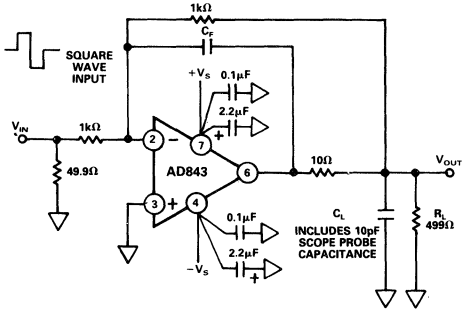


Figure 21a. Unity Gain Inverter Circuit for Driving Capacitive Loads

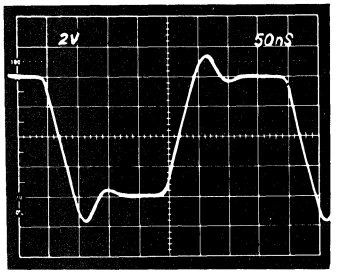


Figure 21b. Inverter Cap Load Large Signal Pulse Response. C_F = 15 pF, C_L = 410 pF

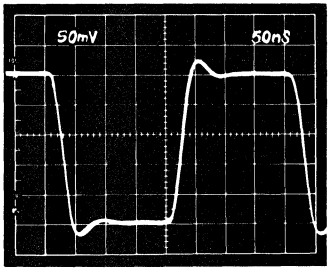


Figure 21c. Inverter Cap Load Small Signal Pulse Response. C_F = 15 pF, C_L = 410 pF

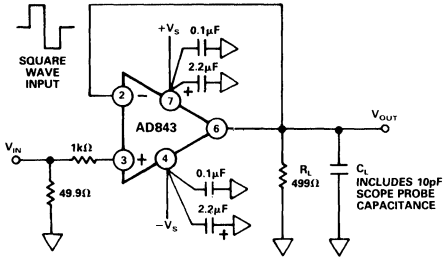


Figure 22a. Unity Gain Buffer Amplifier

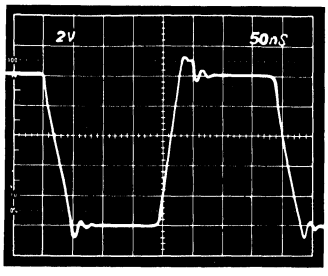


Figure 22b. Buffer Large Signal Pulse Response. C_L = 10 pF

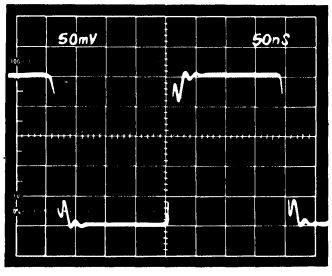


Figure 22c. Buffer Small Signal Pulse Response. C_L = 10 pF

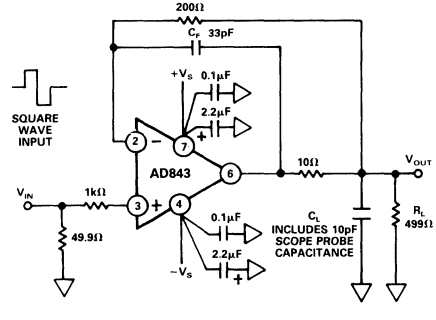


Figure 23a. Unity Gain Buffer Circuit for Driving Capacitive Loads

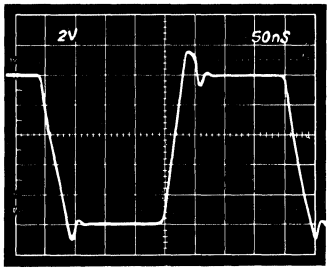


Figure 23b. Buffer Cap Load Large Signal Pulse Response. C_F = 33 pF, C_L = 10 pF

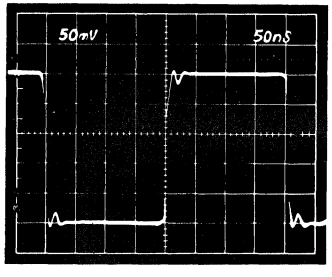


Figure 23c. Buffer Cap Load Small Signal Pulse Response. C_F = 33 pF, C_L = 10 pF

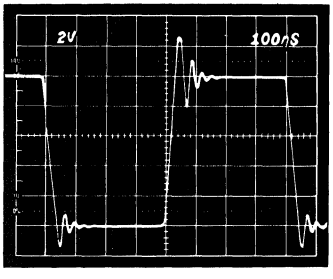


Figure 23d. Buffer Cap Load Large Signal Pulse Response. C_F = 33 pF, C_L = 110 pF

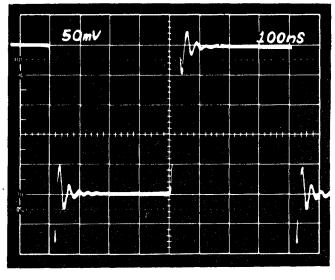


Figure 23e. Buffer Cap Load Small Signal Pulse Response. C_F = 33 pF, C_L = 110 pF

DRIVING CAPACITIVE LOADS

Like most high bandwidth amplifiers, the AD843 is sensitive to capacitive loading. Although it will drive capacitive loads up to 20 pF without degradation of its rated performance, both an increased capacitive load drive capability and a "cleaner" (non-ringing) pulse response can be obtained from the AD843 by using the circuits illustrated in Figures 20 to 23. The addition of a 5 pF feedback capacitor to the unity gain inverter connection (Figure 20a) substantially reduces the circuit's overshoot, even when it is driving a 110 pF load. This can be seen by comparing the waveforms of Figures 20b through 20e. To drive capacitive loads greater than 100 pF, the load should be decoupled from the amplifier's output by a 10 Ω resistor and the feedback capacitor, C_F, should be connected directly between the amplifier's output and its inverting input (Figure 21a). When using a 15 pF feedback capacitor, this circuit can drive 400 pF with less than 20% overshoot, as illustrated in Figures 21b and 21c. Increasing capacitor C_F to 47 pF also increases the capacitance drive capability to 1000 pF, at the expense of a 10:1 reduction in bandwidth compared with the simple unity gain inverter circuit of Figure 20a.

Unity gain voltage followers (buffers) are more sensitive to capacitive loads than are inverting amplifiers because there is no attenuation of the feedback signal. The AD843 can drive 10 pF to 20 pF when connected in the basic unity gain buffer circuit of Figure 22a.

The 1 kΩ resistor in series with the AD843's noninverting input serves two functions: first, together with the amplifier's input capacitance, it forms a low pass filter which slows down the actual signal seen by the AD843. This helps reduce ringing on the amplifier's output voltage. The resistor's second function is to limit the current into the amplifier when the differential input voltage exceeds the total supply voltage.

The AD843 will deliver a much "cleaner" pulse response when connected in the somewhat more elaborate follower circuit of Figure 23a. Note the reduced overshoot in Figure 23b and 23c as compared to Figure 22b and 22c.

For maximum bandwidth, in most applications, input and feedback resistors used with the AD843 should have resistance values equal to or less than 1.5 kΩ. Even with these low resistance values, the resultant RC time constant formed between them and stray circuit capacitances is large enough to cause peaking in the amplifier's response. Adding a small capacitor, C_F, as shown in Figures 20a to 23a will reduce this peaking and flatten the overall frequency response. C_F will normally be less than 10 pF in value.

The AD843 can drive resistive loads over the range of 500 Ω to ∞ with no change in dynamic response. While a 499 Ω load was used in the circuits of Figures 20–23, the performance of these circuits will be essentially the same even if this load is removed or changed to some other value, such as 2 kΩ.

To obtain the "cleanest" possible transient response when driving heavy capacitive loads, be sure to connect bypass capacitors directly between the power supply pins of the AD843 and ground as outlined in "grounding and bypassing."

GROUNDING AND BYPASSING

In designing practical circuits using the AD843, the user must keep in mind that some special precautions are needed when dealing with high frequency signals. Circuits must be wired using short interconnect leads. Ground planes should be used whenever possible to provide both a low resistance, low inductance circuit path and to minimize the effects of high frequency coupling. IC sockets should be avoided, since their increased interlead capacitance can degrade the bandwidth of the device.

Power supply leads should be bypassed to ground as close as possible to the pins of the amplifier. Again, the component leads should be kept very short. As shown in Figure 24, a parallel combination of a 2.2 μF tantalum and a 0.1 μF ceramic disc capacitor is recommended.

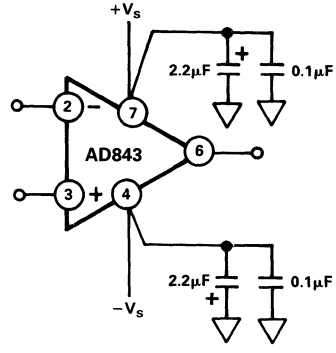
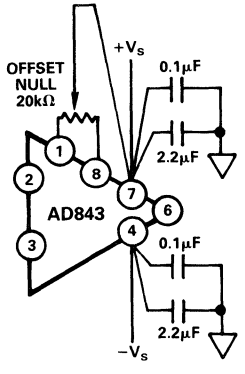


Figure 24. Recommended Power Supply Bypassing for the AD843 (DIP Pinout)

USING A HEAT SINK

The AD843 consumes less quiescent power than most precision high speed amplifiers and is specified to operate without using a heat sink. However, when driving low impedance loads, the current applied to the load can be 4 to 5 times greater than the quiescent current. This will produce a noticeable temperature rise, which will increase input bias currents. The use of a small heat sink, such as the Mouser Electronics #33HS008 is recommended.



Offset Null Configuration (DIP Pinout)

SAMPLE-AND-HOLD AMPLIFIER CIRCUITS

A Fast Switching Sample & Hold Circuit

A sample-and-hold circuit possessing short acquisition time and low aperture delay can be built using an AD843 and discrete JFET switches. The circuit of Figure 25 employs five n-channel JFETs (with turn-on times of 35 ns) and an AD843 op amp (which can settle to 0.01% in 135 ns). The circuit has an aperture delay time of 50 ns and an acquisition time of 1 μs or less.

This circuit is based on a noninverting open loop architecture, using a differential hold capacitor to reduce the effects of pedestal error. The charge that is removed from CH1 by Q2 and Q3 is offset by the charge removed from CH2 by Q4 and Q5. This circuit can tolerate low hold capacitor values (approximately 100 pF), which improve acquisition time, due to the small gate-to-drain capacitance of the discrete JFETs. Although pedestal error will vary with input signal level, making trimming more difficult, the circuit has the advantages of high bandwidth and short acquisition times. In addition, it will exhibit some nonlinearity because both amplifiers are operating with a common mode input. Amplifier A2, however, contributes less than 0.025% linearity error, due to its 72 dB common mode rejection ratio.

To make sure the circuit accommodates a wide ±10 V input range, the gates of the JFETs must be connected to a potential near the −15 V supply. The level-shift circuitry (diode D3, PNP transistor Q7, and NPN transistor Q6) shifts the TTL-level S/H command to provide for an adequate pinch-off voltage for the JFET switches over the full input voltage range.

The JFETs Q2, Q3, Q4 and Q5 across the two hold capacitors ensure signal acquisition for all conditions of V_{IN} and V_{OUT} when the circuit switches from the sample to the hold mode. Transistor Q1 provides an extra stage of isolation between the output of amplifier A1 and the hold capacitor CH1.

When selecting capacitors for use in a sample-and-hold circuit, the designer should choose those types with low dielectric absorption and low temperature coefficients. Silvered-mica capacitors exhibit low (0 to 100 ppm/°C) temperature coefficients and will still work in temperatures exceeding 200°C. It is also recommend that the user test the chosen capacitor to insure that its value closely matches that printed on it since not all capacitors are fully tested by their manufacturers for absolute tolerance.

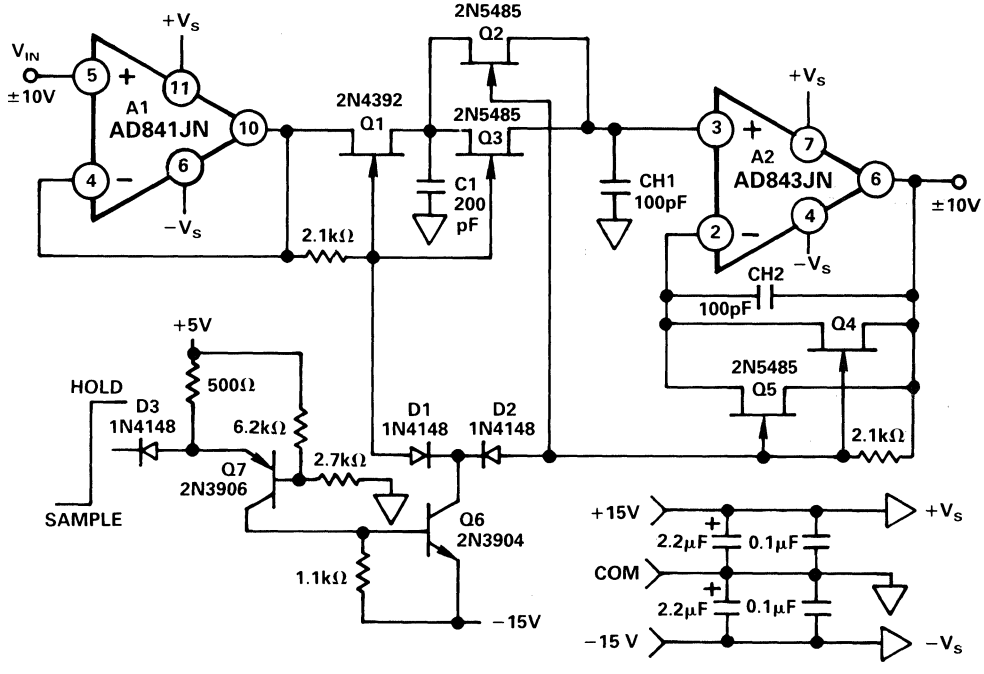


Figure 25. A Fast Switching Sample-and-Hold Amplifier

A PING-PONG S/H AMPLIFIER

For improved throughput over the circuit of Figure 25, a "ping-pong" architecture may be used. A ping-pong circuit overcomes some of the problems associated with high speed S/H amplifiers by allowing the use of a larger hold capacitor for a given sample rate: this will reduce the associated feedthrough, droop and pedestal errors.

Figure 26 illustrates a simple, four-chip ping-pong sample-and-hold amplifier circuit. This design increases throughput by using one channel to acquire a new sample while another channel holds the previous sample. Instead of having to reacquire the signal when switching from hold to sample mode, it alternately connects the outputs from Channel 1 or from Channel 2 to the A/D converter. In this case, the throughput is the slew rate and settling time of the output amplifiers, A2 and A3.

A high speed CB amplifier, A1, follows the input signal. U1, a dual wide-band "T" switch, connects the input buffer amp to one of the two output amplifiers while selecting the complementary amplifier to drive the A/D input. For example, when "select" is at logic high, A1 drives CH1, A2 tracks the input signal and the output of A3 is connected to the input of the A/D converter. At the same time, A3 holds an analog value and its output is connected to the input of the A/D converter. When the select command goes to logic LOW, the two output amplifiers alternate functions.

Since the input to the A/D converter is the alternated "held" outputs from A1 and A2, the offset voltage mismatch of the two amplifiers will show up as nonlinearity and, therefore, distortion in the output signal. To minimize this, potentiometers can be used to adjust the offsets of the output amplifiers until they are equal. Alternatively, an autocalibration circuit using two D/A converters can be employed. This can also be used to calibrate-out the effects of offset voltage drift over temperature.

The switch choice, for U1, is critical in this type of design. The DG542 utilizes "T" switching techniques on each channel for exceptionally low crosstalk and for high isolation. The part further improves these specifications by using ground pins between the signal pins. With an input frequency of 5 MHz, crosstalk and isolation are −85 dB and −75 dB, respectively. A limitation of this switch is that it operates from a maximum −5 V negative supply, making bipolar operation more difficult. It is recommended that amplifiers A1, A2 and A3 operate from the same −5 V supply to minimize any potential latch-up problems.

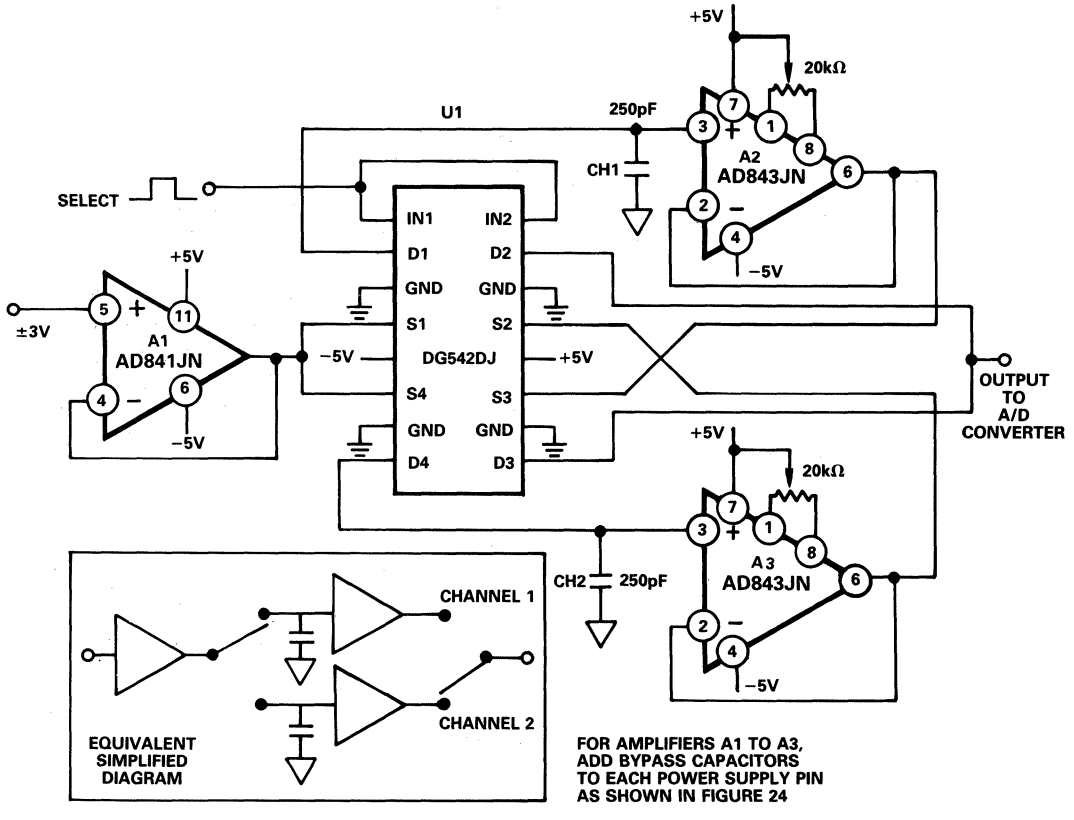


Figure 26. A Ping-Pong Sample-and-Hold Amplifier

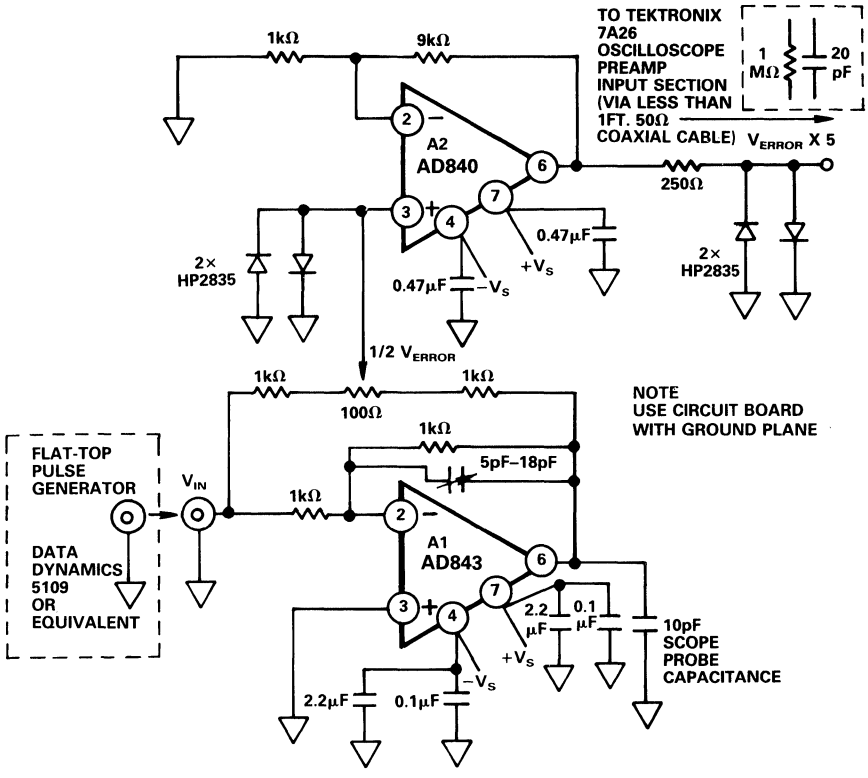


Figure 27. Settling Time Test Circuit

MEASURING AD843 SETTLING TIME

Figure 28 shows the dynamic response of the AD843 while operating in the settling time test circuit of Figure 27. The input of the settling time fixture is driven by a flat-top pulse generator. The error signal output from A1, the AD843 under test, is amplified by op amp A2 and then clamped by two high speed Schottky diodes.

The error signal is clamped to prevent it from greatly overloading the oscilloscope preamp. A Tektronix oscilloscope preamp type 7A26 was chosen because it will recover from the approximately 0.4 volt overload, quickly enough to allow accurate measurement of the AD843's 135 ns settling time. Amplifier A2 is a very high speed op amp; it provides a voltage gain of 10, providing a total gain of 5 from the error signal to the oscilloscope input.

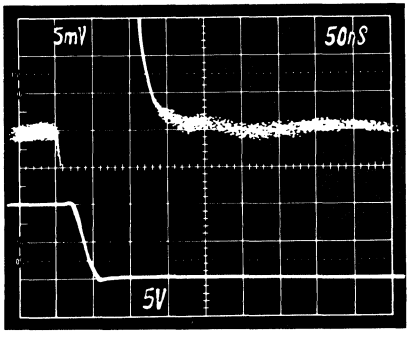


Figure 28. Settling Characteristics: +10 V to 0 V Step. Upper Trace: Amplified Error Voltage (0.01%/Div) Lower Trace: Output of AD843 Under Test (5 V/Div)

AD843—Applications Circuit

A FAST PEAK DETECTOR CIRCUIT

The peak detector circuit of Figure 29, can accurately capture the amplitude of input pulses as narrow as 200 ns and can hold their value with a droop rate of less than 20 μV/μs. This circuit will capture the peak value of positive polarity waveforms; to detect negative peaks, simply reverse the polarity of the two diodes.

The high bandwidth and 200 V/μs slew rate of amplifier A2, an AD843, allows the detector's output to "keep up" with its input thus minimizing overshoot. The low (<1 nA) input current of the AD843 ensures that the droop rate is limited only by the reverse leakage of diode D2, which is typically <10 nA for the type shown. The low droop rate is apparent in Figure 30. The detector's output (top trace) loses slightly over a volt of the 8 volt peak input value (bottom trace) in 75 ms, or a rate of approximately 16 μV/μs

Amplifier A1, an AD847, can drive 680 pF hold capacitor, C_P, fast enough to "catch-up" with the next peak in 100 ns and still settle to the new value in 250 ns, as illustrated in Figure 31. *Reducing* the value of capacitor C_P to 100 pF will maximize the speed of this circuit at the expense of increased overshoot and droop. Since the AD847 can drive an arbitrarily large value of capacitance, C_P can be *increased* to reduce droop, at the expense of response time.

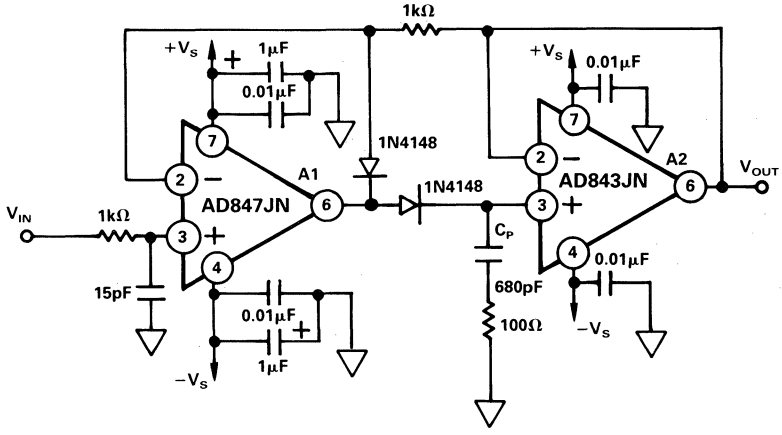
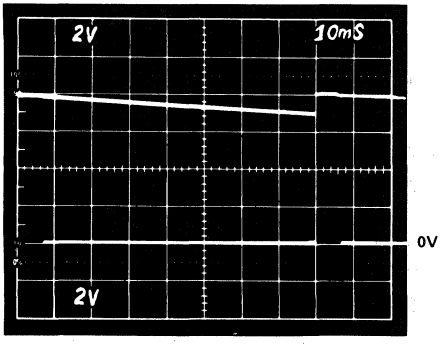


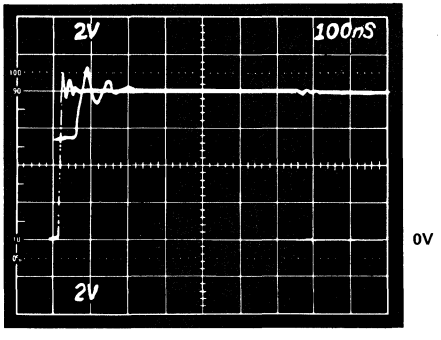
Figure 29. A Fast Peak Detector Circuit



TOP TRACE: PEAK DETECTOR OUTPUT

BOTTOM TRACE: INPUT, 8V PEAK @ 125Hz

Figure 30. Peak Detector Response to 125 Hz Pulse Train



TOP TRACE: PEAK DETECTOR OUTPUT, 8V

BOTTOM TRACE: INPUT VOLTAGE, 8V PEAK, 650ns PULSE WIDTH

Figure 31. Peak Capture Time

60MHz, 2000V/μs Monolithic Op Amp

AD844

FEATURES

Wide Bandwidth: 60MHz at Gain of −1
33MHz at Gain of −10
Very High Output Slew Rate: Up to 2000V/μs
20MHz Full Power Bandwidth, 20V pk-pk, R_L=500Ω
Fast Settling: 100ns to 0.1% (10V Step)
Differential Gain Error: 0.03% at 4.4MHz
Differential Phase Error: 0.15° at 4.4MHz
High Output Drive: ±50mA into 50Ω Load
Low Offset Voltage: 150μV max (B Grade)
Low Quiescent Current: 6.5mA

APPLICATIONS

Flash ADC Input Amplifiers
High Speed Current DAC Interfaces
Video Buffers and Cable Drivers
Pulse Amplifiers

PRODUCT DESCRIPTION

The AD844 is a high speed monolithic operational amplifier fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. It combines high bandwidth and very fast large signal response with excellent dc performance. Although optimized for use in current to voltage applications and as an inverting mode amplifier, it is also suitable for use in many non-inverting applications.

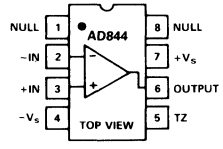
The AD844 can be used in place of traditional op amps, but its current feedback architecture results in much better ac performance, high linearity and an exceptionally clean pulse response.

This type of op amp provides a closed-loop bandwidth which is determined primarily by the feedback resistor and is almost independent of the closed-loop gain. The AD844 is free from the slew rate limitations inherent in traditional op amps and other current-feedback op amps. Peak output rate of change can be over 2000V/μs for a full 20V output step. Settling time is typically 100ns to 0.1%, and essentially independent of gain. The AD844 can drive 50Ω loads to ±2.5V with low distortion and is short circuit protected to 80mA.

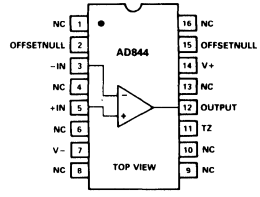
The AD844 is available in four performance grades and three package options. In the 16-pin SOIC (R) package, the AD844J is specified for the commercial temperature range of 0 to +70°C. The AD844A and AD844B are specified for the industrial temperature range of −40°C to +85°C and are available in the cerdip (Q) package. The AD844A is also available in an 8-pin plastic mini-DIP (N). The AD844S is specified over the military temperature range of −55°C to +125°C and is available in the cerdip (Q) package. "A" and "S" grade chips and devices processed to MIL-STD-883B, REV. C are also available.

CONNECTION DIAGRAM

8-Pin Plastic (N), and Cerdip (Q) Packages



16-Pin SOIC (R) Package



PRODUCT HIGHLIGHTS

1. The AD844 is a versatile, low cost component providing an excellent combination of ac and dc performance. It may be used as an alternative to the EL2020 and CLC400/1.
2. It is essentially free from slew rate limitations. Rise and fall times are essentially independent of output level.
3. The AD844 can be operated from ±4.5V to ±18V power supplies and is capable of driving loads down to 50Ω, as well as driving very large capacitive loads using an external network.
4. The offset voltage and input bias currents of the AD844 are laser trimmed to minimize dc errors; V_{OS} drift is typically 1μV/°C and bias current drift is typically 9nA/°C.
5. The AD844 exhibits excellent differential gain and differential phase characteristics, making it suitable for a variety of video applications with bandwidths up to 60MHz.
6. The AD844 combines low distortion, low noise and low drift with wide bandwidth, making it outstanding as an input amplifier for flash A/D converters.

AD844—SPECIFICATIONS (@ T_A=+25°C and V_S=±15V dc, unless otherwise noted)

Model	Conditions	AD844J/A Min	AD844J/A Typ	AD844J/A Max	AD844B Min	AD844B Typ	AD844B Max	AD844S Min	AD844S Typ	AD844S Max	Units
INPUT OFFSET VOLTAGE[1]			50	**300**		50	**150**		50	**300**	μV
T_{min}–T_{max}			75	500		75	**200**		125	**500**	μV
vs. Temperature			1			1	5		1	5	μV/°C
vs. Supply	5V–18V										
Initial			4	**20**		4	**10**		4	**20**	μV/V
T_{min}–T_{max}			4			4	**10**		4	**20**	μV/V
vs. Common Mode	V_{CM}=±10V										
Initial			10	**35**		10	**20**		10	**35**	μV/V
T_{min}–T_{max}			10			10	**20**		10	**35**	μV/V
INPUT BIAS CURRENT											
–Input Bias Current[1]			200	**450**		150	**250**		200	**450**	nA
T_{min}–T_{max}			800	1500		750	**1100**		1900	**2500**	nA
vs. Temperature			9			9	15		20	30	nA/°C
vs. Supply	5V–18V										
Initial			175	**250**		175	**200**		175	**250**	nA/V
T_{min}–T_{max}			220			220	**240**		220	**300**	nA/V
vs. Common Mode	V_{CM}=±10V										
Initial			90	**160**		90	**110**		90	**160**	nA/V
T_{min}–T_{max}			110			110	**150**		120	**200**	nA/V
+Input Bias Current[1]			150	**400**		100	**200**		100	**400**	nA
T_{min}–T_{max}			350	700		300	**500**		800	**1300**	nA
vs. Temperature			3			3	7		7	15	nA/°C
vs. Supply	5V–18V										
Initial			80	**150**		80	**100**		80	**150**	nA/V
T_{min}–T_{max}			100			100	**120**		120	**200**	nA/V
vs. Common Mode	V_{CM}=±10V										
Initial			90	**150**		90	**120**		90	**150**	nA/V
T_{min}–T_{max}			130			130	**190**		140	**200**	nA/V
INPUT CHARACTERISTICS											
Input Resistance											
–Input			50	65		50	65		50	65	Ω
+Input		7	10		7	10		7	10		MΩ
Input Capacitance											
–Input			2			2			2		pF
+Input			2			2			2		pF
Input Voltage Range											
Common Mode		±10			±10			±10			V
INPUT VOLTAGE NOISE	f≥1kHz		2			2			2		nV/√Hz
INPUT CURRENT NOISE											
–Input	f≥1kHz		10			10			10		pA/√Hz
+Input	f≥1kHz		12			12			12		pA/√Hz
OPEN LOOP TRANSRESISTANCE	V_{OUT}=±10V										
	R_{LOAD}=500Ω	**2.2**	3.0		**2.8**	3.0		**2.2**	3.0		MΩ
T_{min}–T_{max}		1.3	2.0		**1.6**	2.0		**1.3**	1.6		MΩ
Transcapacitance			4.5			4.5			4.5		pF
DIFFERENTIAL GAIN ERROR[2]	f=4.4MHz		0.03			0.03			0.03		%
DIFFERENTIAL PHASE ERROR[2]	f=4.4MHz		0.15			0.15			0.15		Degree
FREQUENCY RESPONSE											
Small Signal Bandwidth											
[3]Gain=–1			60			60			60		MHz
[4]Gain=–10			33			33			33		MHz
TOTAL HARMOMIC DISTORTION	f=100kHz, 2V rms[5]		0.005			0.005			0.005		%
SETTLING TIME											
10V Output Step	±15V Supplies										
Gain=–1, to 0.1%[5]			100			100			100		ns
Gain=–10, to 0.1%[6]			100			100			100		ns
2V Output Step	±5V Supplies										
Gain=–1, to 0.1%[5]			110			110			110		ns
Gain=–10, to 0.1%[6]			100			100			100		ns

Model	Conditions	AD844J/A Min	AD844J/A Typ	AD844J/A Max	AD844B Min	AD844B Typ	AD844B Max	AD844S Min	AD844S Typ	AD844S Max	Units
OUTPUT SLEW RATE	Overdriven Input	1200	2000		1200	2000		1200	2000		V/μs
FULL POWER BANDWIDTH											
V_{OUT}=20V p-p[5]	V_S=±15V		20			20			20		MHz
V_{OUT}=2V p-p[5]	V_S=±5V THD=3%		20			20			20		MHz
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}=500Ω	**10**	11		**10**	11		**10**	11		±V
Short Circuit Current			80			80			80		mA
T_{min}–T_{max}			60			60			60		mA
Output Resistance	Open Loop		15			15			15		Ω
POWER SUPPLY											
Operating Range		±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current			6.5	7.5		6.5	7.5		6.5	7.5	mA
T_{min}–T_{max}			7.5	8.5		7.5	**8.5**		8.5	**9.5**	mA

NOTES
[1]Rated performance after a 5 minute warmup at T_A=25°C.
[2]Input signal 285mV p-p carrier (40 IRE) riding on 0 to 642mV (90 IRE) ramp. R_L=100Ω; R1, R2=300Ω.
[3]Input signal 0dBm, C_L=10pF, R_L=500Ω, R1=500Ω, R2=500Ω in Figure 26.
[4]Input signal 0dBm, C_L=10pF, R_L=500Ω, R1=500Ω, R2=50Ω in Figure 26.
[5]C_L=10pF, R_L=500Ω, R1=1kΩ, R2=1kΩ in Figure 26.
[6]C_L=10pF, R_L=500Ω, R1=500Ω, R2=50Ω in Figure 26.

Specifications subject to change without notice. All min and max specifications are guaranteed.
Specifications shown in **boldface** are tested on all production units at final electrical test.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18V
Power Dissipation[2] 1.1W
Output Short Circuit Duration . . . . . Indefinite
Common Mode Input Voltage . . . . . ±V_S
Differential Input Voltage 6V
Inverting Input Current
Continuous 5mA
Transient 10mA
Storage Temperature Range Q . . . . . −65°C to +150°C
N, R . . . . . −65°C to +125°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA}= 100°C/Watt
8-Pin Cerdip Package: θ_{JA}=110°C/Watt
16-Pin SOIC Package: θ_{JA}=100°C/Watt

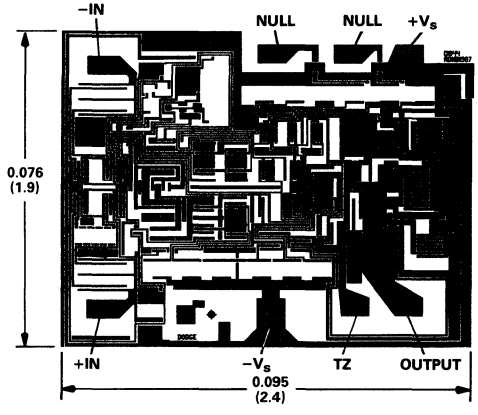
ORDERING GUIDE[1]

Model[1]	Temperature Range	Package Option[2]
AD844JR	0°C to +70°C	R-16
AD844AN	−40°C to +85°C	N-8
AD844AQ	−40°C to +85°C	Q-8
AD844BQ	−40°C to +85°C	Q-8
AD844SQ	−55°C to +125°C	Q-8
AD844SQ/883B	−55°C to +125°C	Q-8

NOTES
S[1]"A" and "S" grade chips are also available.
[2]N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



SUBSTRATE CONNECTED TO +V_S

AD844–Typical Characteristics (T_A = +25°C and V_S = ±15V unless otherwise noted)

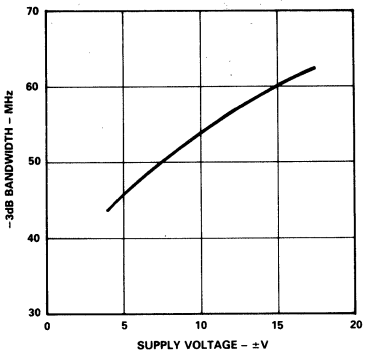


Figure 1. −3dB Bandwidth vs. Supply Voltage R1 = R2 = 500Ω

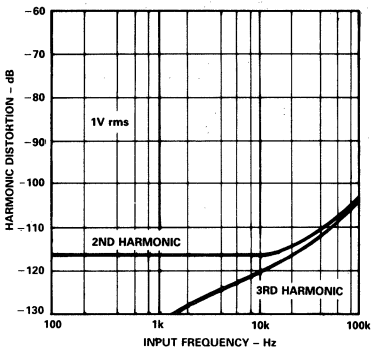


Figure 2. Harmonic Distortion vs. Frequency, R1 = R2 = 1kΩ

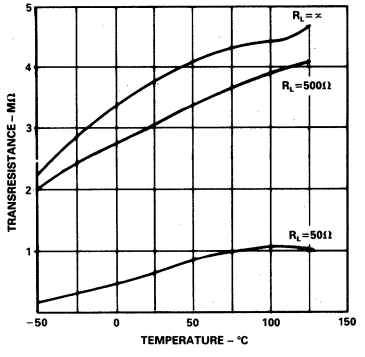


Figure 3. Transresistance vs. Temperature

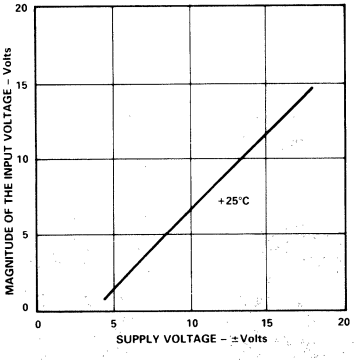


Figure 4. Noninverting Input Voltage Swing vs. Supply Voltage

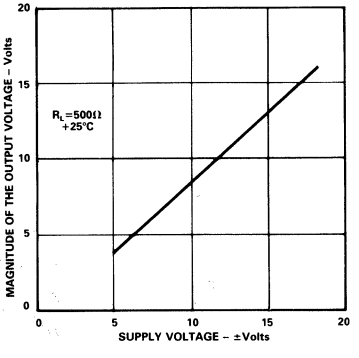


Figure 5. Output Voltage Swing vs. Supply Voltage

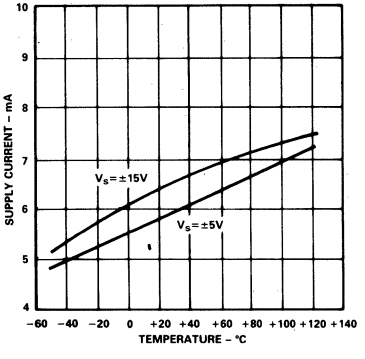


Figure 6. Quiescent Supply Current vs. Temperature and Supply Voltage

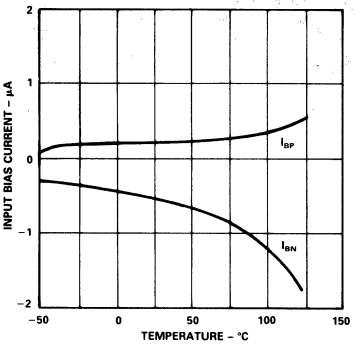


Figure 7. Inverting Input Bias Current (I_{BN}) and Noninverting Input Bias Current (I_{BP}) vs. Temperature

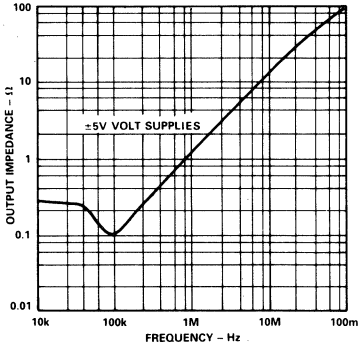


Figure 8. Output Impedance vs. Frequency, Gain = −1, R1 = R2 = 1kΩ

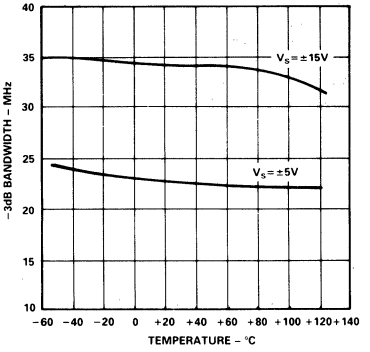


Figure 9. −3dB Bandwidth vs. Temperature, Gain = −1, R1 = R2 = 1kΩ

Inverting Gain of 1 AC Characteristics

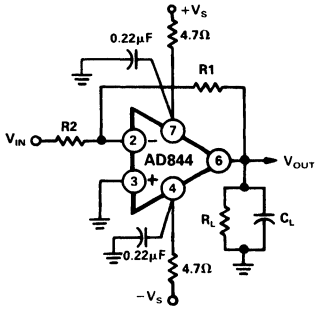


Figure 10. Inverting Amplifier, Gain of −1 (R1=R2)

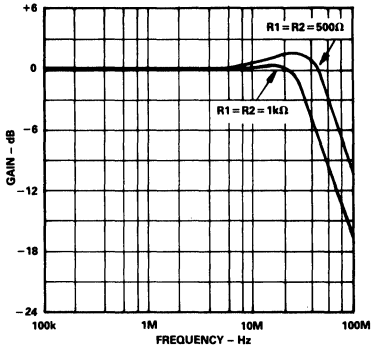


Figure 11. Gain vs. Frequency for Gain = −1, R_L = 500Ω, C_L = 0pF

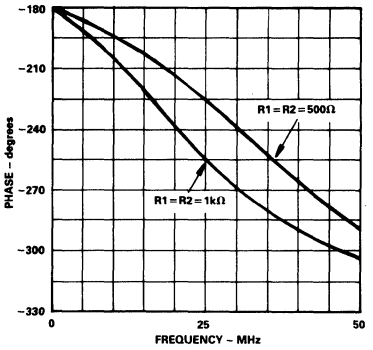


Figure 12. Phase vs. Frequency Gain = −1, R_L = 500Ω, C_L = 0pF

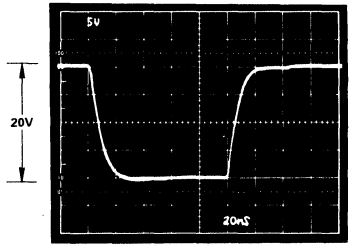


Figure 13. Large Signal Pulse Response, Gain = −1, R1 = R2 = 1kΩ

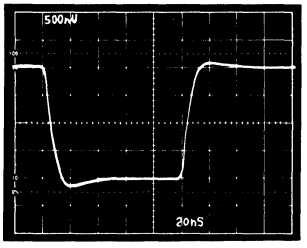


Figure 14. Small Signal Pulse Response, Gain = −1, R1 = R2 = 1kΩ

Inverting Gain of 10 AC Characteristics

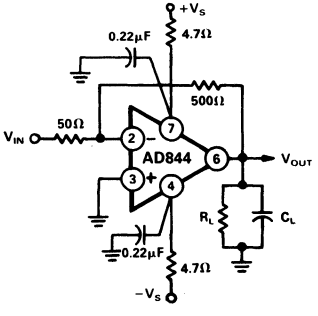


Figure 15. Gain of −10 Amplifier

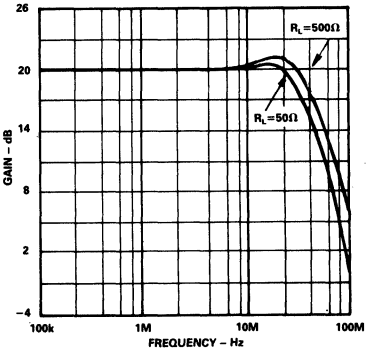


Figure 16. Gain vs. Frequency, Gain = −10

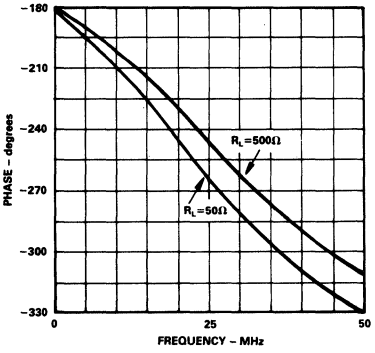


Figure 17. Phase vs. Frequency, Gain = −10

Inverting Gain of 10 Pulse Response

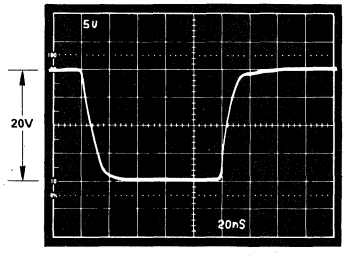


Figure 18. Large Signal Pulse Response, Gain=−10, R_L=500Ω

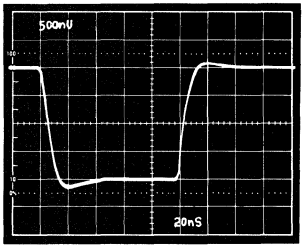


Figure 19. Small Signal Pulse Response, Gain=−10, R_L=500Ω

Noninverting Gain of 10 AC Characteristics

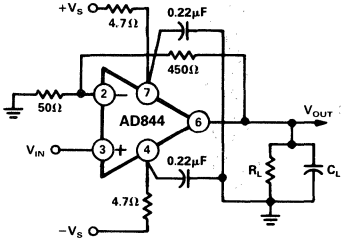


Figure 20. Noninverting Gain of +10 Amplifier

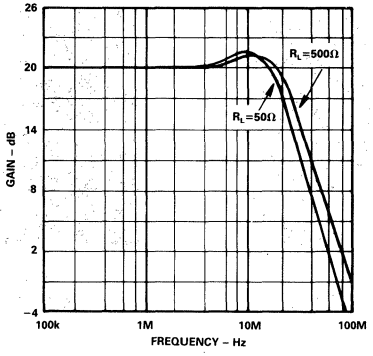


Figure 21. Gain vs. Frequency, Gain=+10

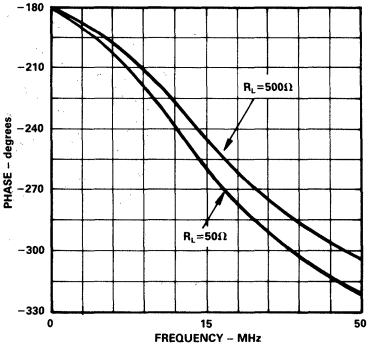


Figure 22. Phase vs. Frequency, Gain=+10

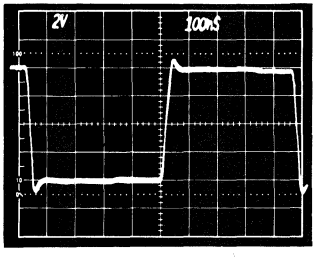


Figure 23. Noninverting Amplifier Large Signal Pulse Response, Gain=+10, R_L=500Ω

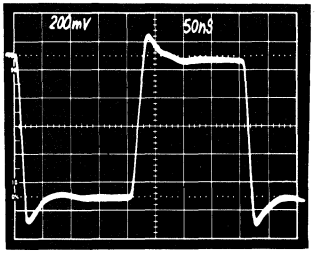


Figure 24. Small Signal Pulse Response, Gain=+10, R_L=500Ω

UNDERSTANDING THE AD844

The AD844 can be used in ways similar to a conventional op amp while providing performance advantages in wideband applications. However, there are important differences in the internal structure which need to be understood in order to optimize the performance of the AD844 op amp.

Open Loop Behavior

Figure 25 shows a current feedback amplifier reduced to essentials. Sources of fixed dc errors such as the inverting node bias current and the offset voltage are excluded from this model and are discussed later. The most important parameter limiting the dc gain is the transresistance, Rt, which is ideally infinite. A finite value of Rt is analogous to the finite open loop voltage gain in a conventional op amp.

The current applied to the inverting input node is replicated by the current conveyor so as to flow in resistor Rt. The voltage developed across Rt is buffered by the unity gain voltage follower. Voltage gain is the ratio Rt/ R_{IN}. With typical values of Rt=3MΩ and R_{IN}=50Ω, the voltage gain is about 60,000. The open loop current gain is another measure of gain and is determined by the beta product of the transistors in the voltage follower stage (see Figure 28); it is typically 40,000.

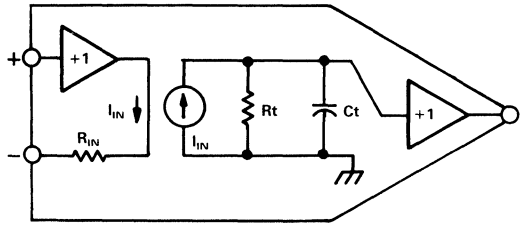


Figure 25. Equivalent Schematic

The important parameters defining ac behavior are the transcapacitance, Ct, and the external feedback resistor (not shown). The time constant formed by these components is analogous to the dominant pole of a conventional op amp, and thus cannot be reduced below a critical value if the closed loop system is to be stable. In practice, Ct is held to as low a value as possible (typically 4.5pF) so that the feedback resistor can be maximized while maintaining a fast response. The finite R_{IN} also affects the closed loop response in some applications as will be shown.

The open loop ac gain is also best understood in terms of the transimpedance rather than as an open loop voltage gain. The open loop pole is formed by Rt in parallel with Ct. Since Ct is typically 4.5pF, the open loop corner frequency occurs at about 12kHz. However, this parameter is of little value in determining the closed loop response.

Response as an Inverting Amplifier

Figure 26 shows the connections for an inverting amplifier. Unlike a conventional amplifier the transient response and the small signal bandwidth are determined primarily by the value of the external feedback resistor, R1, rather than by the ratio of R1/R2 as is customarily the case in an op amp application. This is a direct result of the low impedance at the inverting input. As with conventional op amps, the closed loop gain is −R1/R2.

The closed loop transresistance is simply the parallel sum of R1 and Rt. Since R1 will generally be in the range 500Ω to 2kΩ and Rt is about 3MΩ the closed loop transresistance will be only 0.02% to 0.07% lower than R1. This small error will often be less than the resistor tolerance.

When R1 is fairly large (above 5kΩ) but still much less than Rt, the closed loop HF response is dominated by the time constant R1Ct. Under such conditions the AD844 is over-damped and will provide only a fraction of its bandwidth potential. Because of the absence of slew rate limitations under these conditions, the circuit will exhibit a simple single pole response even under large signal conditions.

In Figure 26, R3 is used to properly terminate the input if desired. R3 in parallel with R2 gives the terminated resistance. As R1 is lowered, the signal bandwidth increases, but the time constant R1Ct becomes comparable to higher order poles in the closed loop response. Therefore, the closed loop response becomes complex, and the pulse response shows overshoot. When R2 is much larger than the input resistance, R_{IN}, at Pin 2, most of the feedback current in R1 is delivered to this input; but as R2 becomes comparable to R_{IN}, less of the feedback is absorbed at Pin 2, resulting in a more heavily damped response. Consequently, for low values of R2 it is possible to lower R1 without causing instability in the closed loop response. Table I lists combinations of R1 and R2 and the resulting frequency response for the circuit of Figure 26. Figure 13 shows the very clean and fast ±10V pulse response of the AD844.

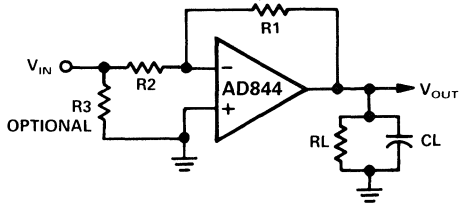


Figure 26. Inverting Amplifier

Gain	R1	R2	BW (MHz)	GBW (MHz)
−1	1kΩ	1kΩ	35	35
−1	500Ω	500Ω	60	60
−2	2kΩ	1kΩ	15	30
−2	1kΩ	500Ω	30	60
−5	5kΩ	1kΩ	5.2	26
−5	500Ω	100Ω	49	245
−10	1kΩ	100Ω	23	230
−10	500Ω	50Ω	33	330
−20	1kΩ	50Ω	21	420
−100	5kΩ	50Ω	3.2	320
+100	5kΩ	50Ω	9	900

Table I.

Response as an I-V Converter

The AD844 works well as the active element in an operational current to voltage converter, used in conjunction with an external scaling resistor, R1, in Figure 27. This analysis includes the stray capacitance, C_S, of the current source, which might be a high speed DAC. Using a conventional op amp, this capacitance forms a "nuisance pole" with R1 which destabilizes the closed loop response of the system. Most op amps are internally compensated for the fastest response at unity gain, so the pole due to R1 and C_S reduces the already narrow phase margin of the system. For example, if R1 were 2.5kΩ a C_S of 15pF would place this pole at a frequency of about 4MHz, well within the response range of even a medium speed operational amplifier. In a current feedback amp this nuisance pole is no longer determined by R1 but by the input resistance, R_{IN}. Since this is about 50Ω for the AD844, the same 15pF forms a pole 212MHz and causes little trouble. It can be shown that the response of this system is:

$$V_{OUT} = -Isig \frac{K\,R1}{(1+sTd)(1+sTn)}$$

where K is a factor very close to unity and represents the finite dc gain of the amplifier, Td is the dominant pole and Tn is the nuisance pole:

$$K = \frac{Rt}{Rt+R1}$$

$$Td = KR1Ct$$

$$Tn = R_{IN}C_S \qquad \text{(assuming } R_{IN} << R1\text{)}$$

Using typical values of R1=1kΩ and Rt=3MΩ, K is 0.9997; in other words, the "gain error" is only 0.03%. This is much less than the scaling error of virtually all DACs and can be absorbed, if necessary, by the trim needed in a precise system.

In the AD844, Rt is fairly stable with temperature and supply voltages, and consequently the effect of finite "gain" is negligible unless high value feedback resistors are used. Since that would result in slower response times than are possible, the relatively low value of Rt in the AD844 will rarely be a significant source of error.

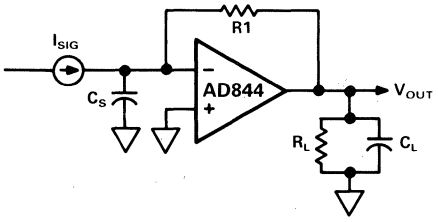


Figure 27. Current to Voltage Converter

Circuit Description of the AD844

A simplified schematic is shown in Figure 28. The AD844 differs from a conventional op amp in that the signal inputs have radically different impedance. The noninverting input (Pin 3) presents the usual high impedance. The voltage on this input is transferred to the inverting input (Pin 2) with a low offset voltage, ensured by the close matching of like polarity transistors

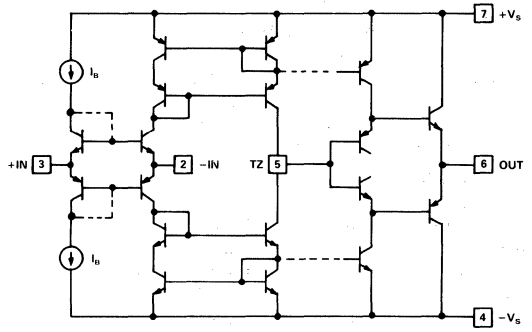


Figure 28. Simplified Schematic

operating under essentially identical bias conditions. Laser trimming nulls the residual offset voltage, down to a few tens of microvolts. The inverting input is the common emitter node of a complementary pair of grounded base stages and behaves as a current summing node. In an ideal current feedback op amp the input resistance would be zero. In the AD844 it is about 50Ω.

A current applied to the inverting input is transferred to a complementary pair of unity-gain current mirrors which deliver the same current to an internal node (Pin 5) at which the full output voltage is generated. The unity-gain complementary voltage follower then buffers this voltage and provides the load driving power. This buffer is designed to drive low impedance loads such as terminated cables, and can deliver ±50mA into a 50Ω load while maintaining low distortion, even when operating at supply voltages of only ±6V. Current limiting (not shown) ensures safe operation under short circuited conditions.

It is important to understand that the low input impedance at the inverting input is locally generated, and does not depend on feedback. This is very different from the "virtual ground" of a conventional operational amplifier used in the current summing mode which is essentially an open circuit until the loop settles. In the AD844, transient current at the input does not cause voltage spikes at the summing node while the amplifier is settling. Furthermore, all of the transient current is delivered to the slewing (TZ) node (Pin 5) via a short signal path (the grounded base stages and the wideband current mirrors).

The current available to charge the capacitance (about 4.5pF) at TZ node, *is always proportional to the input error current*, and the slew rate limitations associated with the large signal response of op amps do not occur. For this reason, the rise and fall times are almost independent of signal level. In practice, the input current will eventually cause the mirrors to saturate. When using ±15V supplies, this occurs at about 10mA (or ±2200V/μs). Since signal currents are rarely this large, classical "slew rate" limitations are absent.

This inherent advantage would be lost if the voltage follower used to buffer the output were to have slew rate limitations. The AD844 has been designed to avoid this problem, and as a result the output buffer exhibits a clean large signal transient response, free from anomalous effects arising from internal saturation.

Response as a Noninverting Amplifier

Since current feedback amplifiers are asymmetrical with regard to their two inputs, performance will differ markedly in noninverting and inverting modes. In noninverting modes, the large signal high speed behavior of the AD844 deteriorates at low gains because the biasing circuitry for the input system (not shown in Figure 28) is not designed to provide high input voltage slew rates.

However, good results can be obtained with some care. The noninverting input will not tolerate a large transient input; it must be kept below ±1V for best results. Consequently this mode is better suited to high gain applications (greater than ×10). Figure 20 shows a noninverting amplifier with a gain of 10 and a bandwidth of 30MHz. The transient response is shown in Figures 23 and 24. To increase the bandwidth at higher gains, a capacitor can be added across R2 whose value is approximately the ratio of R1 and R2 times Ct.

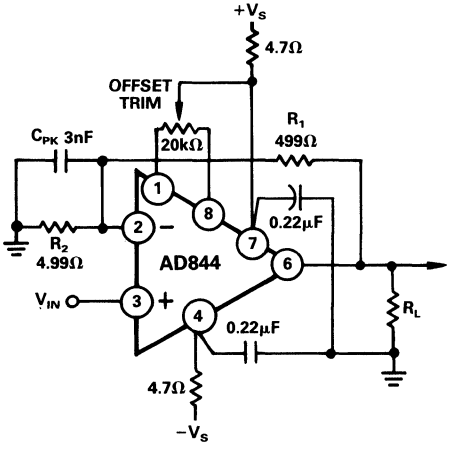


Figure 29. Noninverting Amplifier Gain=100, Optional Offset Trim Is Shown

Noninverting Gain of 100

The AD844 provides very clean pulse response at high noninverting gains. Figure 29 shows a typical configuration providing a gain of 100 with high input resistance. The feedback resistor is kept as low as practicable to maximize bandwidth, and a peaking capacitor (C_{PK}) can optionally be added to further extend the bandwidth. Figure 30 shows the small signal response with C_{PK} = 3nF, R_L = 500Ω and supply voltages of either ±5V or ±15V. *Gain bandwidth products of up to 900MHz can be achieved in this way.*

The offset voltage of the AD844 is laser trimmed to the 50μV level and exhibits very low drift. In practice, there is an additional offset term due to the bias current at the inverting input (I_{BN}) which flows in the feedback resistor (R1). This can optionally be nulled by the trimming potentiometer shown in Figure 29.

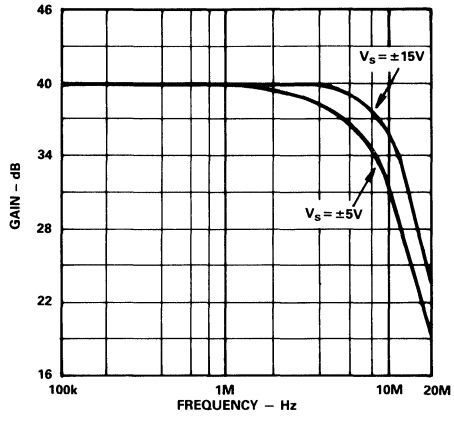


Figure 30. AC Response for Gain = 100, Configuration Shown in Figure 29

USING THE AD844

Board Layout

As with all high frequency circuits considerable care must be used in the layout of the components surrounding the AD844. A ground plane, to which the power supply decoupling capacitors are connected by the shortest possible leads, is essential to achieving clean pulse response. Even a continuous ground plane will exhibit finite voltage drops between points on the plane, and this must be kept in mind in selecting the grounding points. Generally speaking, decoupling capacitors should be taken to a point close to the load (or output connector) since the load currents flow in these capacitors at high frequencies. The +In and −In circuits (for example, a termination resistor and Pin 3) must be taken to a common point on the ground plane close to the amplifier package.

Use low impedance capacitors (AVX SR305C224KAA or equivalent) of 0.22μF wherever ac coupling is required. Include either ferrite beads and/or a small series resistance (approximately 4.7Ω) in each supply line.

Input Impedance

At low frequencies, negative feedback keeps the resistance at the inverting input close to zero. As the frequency increases, the impedance looking into this input will increase from near zero to the open loop input resistance, due to bandwidth limitations, making the input seem inductive. If it is desired to keep the input impedance flatter, a series RC network can be inserted across the input. The resistor is chosen so that the parallel sum of it and R2 equals the desired termination resistance. The capacitance is set so that the pole determined by this RC network is about half the bandwidth of the op amp. This network is not important if the input resistor is much larger than the termination used, or if frequencies are relatively low. In some cases, the small peaking that occurs without the network can be of use in extending the −3dB bandwidth.

Driving Large Capacitive Loads

Capacitive drive capability is 100pF without an external network. With the addition of the network shown in Figure 31, the capacitive drive can be extended to over 10,000pF, limited by internal power dissipation. With capacitive loads, the output speed becomes a function of the overdriven output current limit. Since this is roughly ±100mA, under these conditions, the maximum slew rate into a 1000pF load is ±100V/μs. Figure 32 shows the transient response of an inverting amplifier (R1=R2=1kΩ) using the feed forward network shown in Figure 31, driving a load of 1000pF.

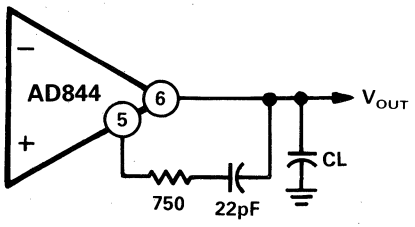


Figure 31. Feed Forward Network for Large Capacitive Loads

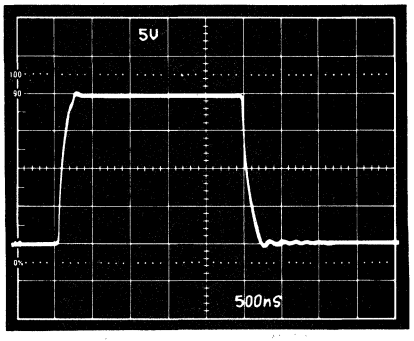


Figure 32. Driving 1000pF CL with Feed Forward Network of Figure 31

Settling Time

Settling time is measured with the circuit of Figure 33. This circuit employs a false summing node, clamped by the two Schottky diodes, to create the error signal and limit the input signal to the oscilloscope. For measuring settling time, the ratio of R6/R5 is equal to R1/R2. For unity gain, R6=R5=1kΩ, and R_L=500Ω. For the gain of −10, R5=50Ω, R6=500Ω and R_L was not used since the summing network loads the output with approximately 275Ω. Using this network in a unity-gain configuration, settling time is 100ns to 0.1% for a −5V to +5V step with C_L=10pF.

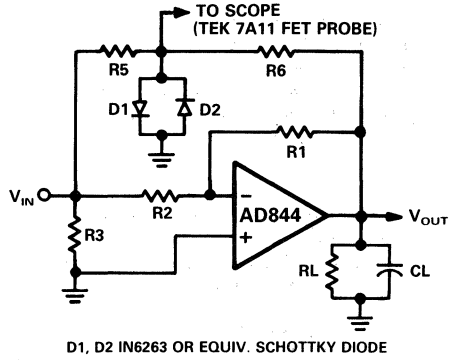


Figure 33. Settling Time Test Fixture

DC Error Calculation

Figure 34 shows a model of the dc error and noise sources for the AD844. The inverting input bias current, I_{BN}, flows in the feedback resistor. I_{BP}, the noninverting input bias current, flows in the resistance at Pin 3 (R_P), and the resulting voltage (plus any offset voltage) will appear at the inverting input. The total error, V_O, at the output is:

$$V_O=(I_{BP}\,R_P+V_{OS}+I_{BN}\,R_{IN})\left(1+\frac{R1}{R2}\right)+I_{BN}\,R1$$

Since I_{BN} and I_{BP} are unrelated both in sign and magnitude, inserting a resistor in series with the noninverting input will not necessarily reduce dc error and may actually increase it.

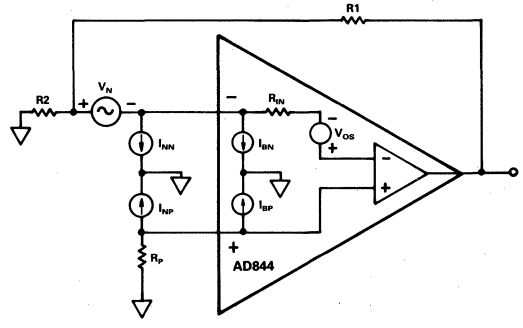


Figure 34. Offset Voltage and Noise Model for the AD844

Noise

Noise sources can be modeled in a manner similar to the dc bias currents, but the noise sources are Inn, Inp, Vn, and the amplifier-induced noise at the output, V_{ON}, is:

$$V_{ON}=\sqrt{((\text{Inp}\,R_P)^2+\text{Vn}^2)\left(1+\frac{R1}{R2}\right)^2+(\text{Inn}\,R1)^2}$$

Overall noise can be reduced by keeping all resistor values to a minimum. With typical numbers, R1=R2=1k, R_P=0, Vn=2nV/√Hz, Inp=10pA/√Hz, Inn=12pA/√Hz, V_{ON} calculates to 12nV/√Hz. The current noise is dominant in this case, as it will be in most low gain applications.

Video Cable Driver Using ±5 Volt Supplies

The AD844 can be used to drive low impedance cables. Using ±5V supplies, a 100Ω load can be driven to ±2.5V with low distortion. Figure 35a shows an illustrative application which provides a noninverting gain of 2, allowing the cable to be reverse-terminated while delivering an overall gain of +1 to the load. The −3dB bandwidth of this circuit is typically 30MHz. Figure 35b shows a differential gain and phase test setup. In video applications, differential-phase and differential-gain characteristics are often important. Figure 35c shows the variation in phase as the load voltage varies. Figure 35d shows the gain variation.

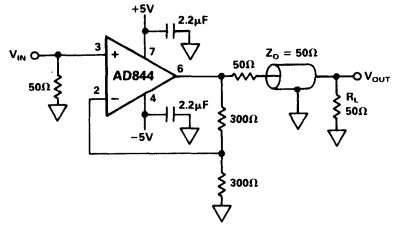


Figure 35a. The AD844 as a Cable Driver

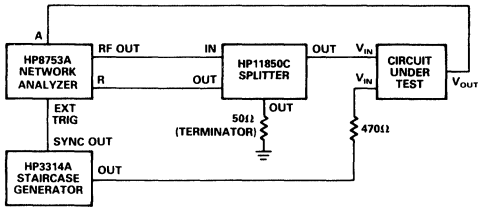


Figure 35b. Differential Gain/Phase Test Setup

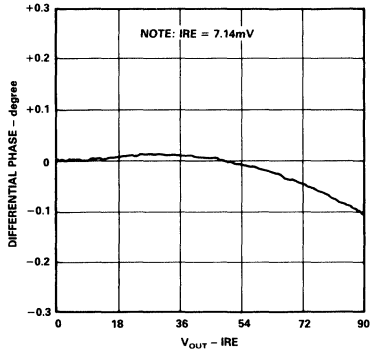


Figure 35c. Differential Phase for the Circuit of Figure 35a

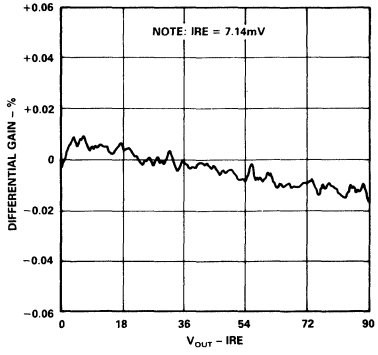


Figure 35d. Differential Gain for the Circuit of Figure 35a

High Speed DAC Buffer

The AD844 performs very well in applications requiring current-to-voltage conversion. Figure 36 shows connections for use with the AD568 current output DAC. In this application the bipolar offset is used so that the full scale current is ±5.12mA, which generates an output of ±5.12V using the 1kΩ application resistor on the AD568. Figure 37 shows the full scale transient response. Care is needed in power supply decoupling and grounding techniques to achieve the full 12-bit accuracy and realize the fast settling capabilities of the system. The unmarked capacitors in this figure are 0.1μF ceramic (for example, AVX Type SR305C104KAA), and the ferrite inductors should be about 2.5μH (for example, Fair-Rite Type 2743002122). The AD568 data sheet should be consulted for more complete details about its use.

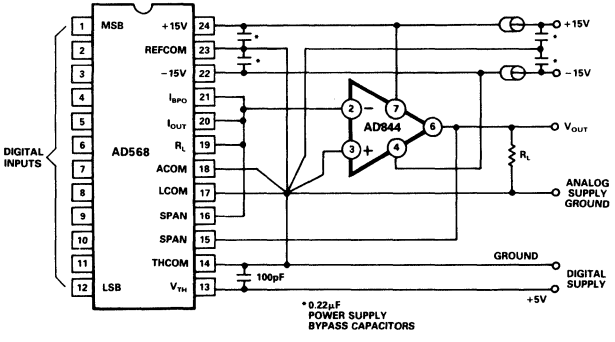


Figure 36. High Speed DAC Amplifier

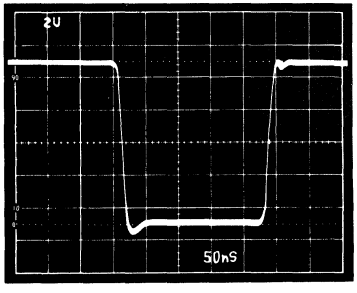


Figure 37. DAC Amplifier Full-Scale Transient Response

20MHz Variable Gain Amplifier

The AD844 is an excellent choice as an output amplifier for the AD539 multiplier, in all of its connection modes. (See AD539 data sheet for full details.) Figure 38 shows a simple multiplier providing the output:

$$V_W = -\frac{V_X V_Y}{2V}$$

where V_X is the "gain control" input, a positive voltage of from 0 to +3.2V (max) and V_Y is the "signal voltage", nominally ±2V FS but capable of operation up to ±4.2V. The peak output in this configuration is thus ±6.7V. Using all four of the internal application resistors provided on the AD539 in parallel results in a feedback resistance of 1.5kΩ, at which value the bandwidth of the AD844 is about 22MHz, and is essentially independent of V_X. The gain at V_X=3.16V is +4dB.

Figure 39 shows the small signal response for a 50dB gain control range (V_X=+10mV to +3.16V). At small values of V_X, capacitive feedthrough on the PC board becomes troublesome, and very careful layout techniques are needed to minimize this problem. A ground strip between the pins of the AD539 will be helpful in this regard. Figure 40 shows the response to a 2V pulse on V_Y for V_X=+1V, +2V and +3V. For these results, a load resistor of 500Ω was used and the supplies were ±9V. The multiplier will operate from supplies between ±4.5V and ±16.5V.

Disconnecting Pins 9 and 16 on the AD539 alters the denominator in the above expression to 1V, and the bandwidth will be approximately 10MHz, with a maximum gain of 10dB. Using only Pin 9 or Pin 16 results in a denominator of 0.5V, a bandwidth of 5MHz and a maximum gain of 16dB.

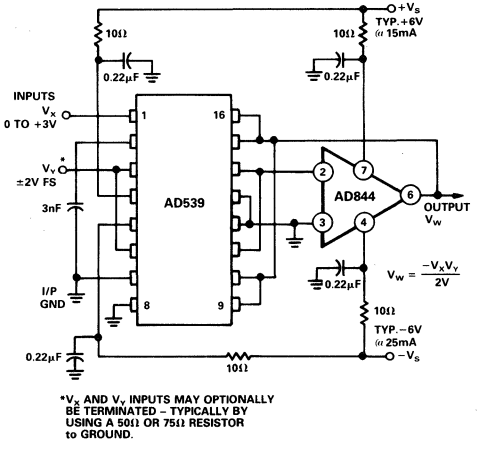


Figure 38. 20MHz VGA Using the AD539

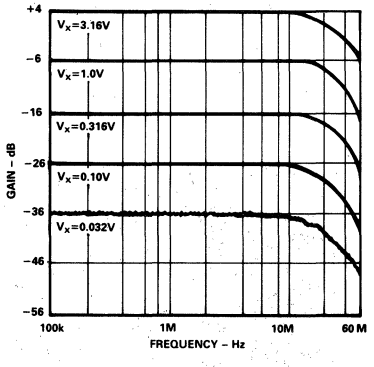


Figure 39. VGA AC Response

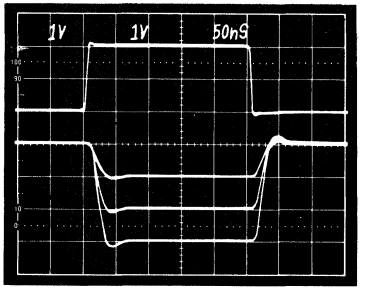


Figure 40. VGA Transient Response with V_X=1V, 2V, and 3V

ANALOG DEVICES

Precision 16 MHz CBFET Op Amp

AD845

FEATURES

Replaces Hybrid Amplifiers in Many Applications

AC PERFORMANCE:

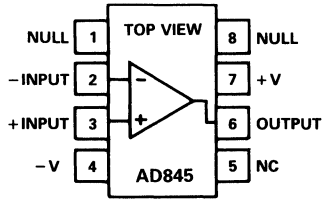
Settles to 0.01% in 350 ns
100 V/μs Slew Rate
12.8 MHz min Unity-Gain Bandwidth
1.75 MHz Full-Power Bandwidth at 20 V p–p

DC PERFORMANCE:

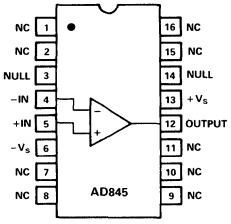
0.25 mV max Input Offset Voltage
5 μV/°C max Offset Voltage Drift
0.5 nA Input Bias Current
250 V/mV min Open-Loop Gain
4 μV p–p max Voltage Noise, 0.1 Hz to 10 Hz
94 dB min CMRR
Available in Plastic Mini-DIP, Hermetic Cerdip and SOIC Packages

CONNECTION DIAGRAM

Plastic Mini-DIP (N) Package and Cerdip (Q) Package



16-Pin SOIC (R) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD845 is a fast, precise, N channel JFET input, monolithic operational amplifier. It is fabricated using Analog Devices' complementary bipolar (CB) process. Advanced laser-wafer trimming technology enables the very low input offset voltage and offset voltage drift performance to be realized. This precision, when coupled with a slew rate of 100 V/μs, a stable unity-gain bandwidth of 16 MHz, and a settling time of 350 ns 0.01%—while driving a parallel load of 100 pF and 500 Ω—represents a combination of features unmatched by any FET input IC amplifier. The AD845 can easily be used to upgrade many existing designs which use BiFET or FET input hybrid amplifiers and, in some cases, those which use bipolar input op amps.

The AD845 is ideal for use in applications such as active filters, high speed integrators, photo diode preamps, sample-and-hold amplifiers, log amplifiers, and in buffering A/D and D/A converters. The 250 μV max input offset voltage makes offset nulling unnecessary in many applications. The common-mode rejection ratio of 110 dB over a ±10 V input voltage range represents exceptional performance for a JFET input high speed op amp. This, together with a minimum open-loop gain of 250 V/mV ensures that 12-bit performance is achieved, even in unity-gain buffer circuits.

The AD845 conforms to the standard op amp pinout except that offset nulling is to V+. The AD845J and AD845K grade devices are available specified to operate over the commercial 0 to +70°C temperature range. AD845A and AD845B devices are specified for operation over the −40°C to +85°C industrial temperature range. The AD845S is specified to operate over the full military temperature range of −55°C to +125°C. Both the industrial and military versions are available in 8-pin cerdip packages. The commercial version is available in an 8-pin plastic mini-DIP and 16-pin SOIC. "J" and "S" grade chips are also available.

PRODUCT HIGHLIGHTS

1. The high slew rate, fast settling time, and dc precision of the AD845 make it ideal for high speed applications requiring 12-bit accuracy.
2. The performance of circuits using the LF400, OP-42, OP-44, OP-16, OP-17, HA2520/2/5, HA2620/2/5, 3550, OPA605, and LH0062 can be upgraded in most cases.
3. The AD845 is unity-gain stable and internally compensated.
4. The AD845 is specified while driving 100 pF/500 Ω loads.

AD845—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD845J/A Min	AD845J/A Typ	AD845J/A Max	AD845K/B Min	AD845K/B Typ	AD845K/B Max	AD845S Min	AD845S Typ	AD845S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0.7	**1.5**		0.1	**0.25**		0.25	**1.0**	mV
	T_{min}–T_{max}			2.5			**0.4**			2.0	mV
Offset Drift				20		1.5	**5.0**			**10**	μV/°C
INPUT BIAS CURRENT[2]											
Initial	V_{CM} = 0 V		0.75	**2**		0.5	**1**		0.75	**2**	nA
	T_{min}–T_{max}			45/75			**18/38**			**500**	nA
INPUT OFFSET CURRENT											
Initial	V_{CM} = 0 V		25	**300**		15	**100**		25	**300**	pA
	T_{min}–T_{max}			3/6.5			**1.2/2.6**			**20**	nA
INPUT CHARACTERISTICS											
Input Resistance			10^{11}			10^{11}			10^{11}		kΩ
Input Capacitance			4.0			4.0			4.0		pF
INPUT VOLTAGE RANGE											
Differential			±20			±20			±20		V
Common Mode		**±10**	+ 10.5/−13		**+10**	+10.5/−13		**±10**	+10.5/−13		V
Common-Mode Rejection	V_{CM} = ±10 V	**86**	110		**94**	113		**86**	110		dB
INPUT VOLTAGE NOISE	0.1 to 10 Hz		4			4			4		μV p–p
	f = 10 Hz		80			80			80		nV/√Hz
	f = 100 Hz		60			60			60		nV/√Hz
	f = 1 kHz		25			25			25		nV/√Hz
	f = 10 kHz		18			18			18		nV/√Hz
	f = 100 kHz		12			12			12		nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz		0.1			0.1			0.1		pA/√Hz
OPEN-LOOP GAIN	V_O = ±10 V										
	R_{LOAD}≥2 kΩ	**200**	500		**250**	500		**200**	500		V/mV
	R_{LOAD}≥500 Ω	**100**	250		**125**	250		**100**	250		V/mV
	T_{min}–T_{max}	70			75			50			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}≥500 Ω	**±12.5**			**±12.5**			**±12.5**			V
Current	Short Circuit		50			50			50		mA
Output Resistance	Open Loop		5			5			5		Ω
FREQUENCY RESPONSE											
Small Signal	Unity Gain	12.8	16		13.6	16		13.6	16		MHz
Full Power Bandwidth[3]	V_O = ±10 V										
	R_{LOAD} = 500 Ω		1.75			1.75			1.75		MHz
Rise Time			20			20			20		ns
Overshoot			20			20			20		%
Slew Rate		**80**	100		**94**	100		**94**	100		V/μs
Settling Time	10 V Step										
	C_{LOAD} = 100 pF										ns
	R_{LOAD} = 500 Ω										ns
	to 0.01%		350			350	500		350	500	ns
	to 0.1%		250			250			250		ns
DIFFERENTIAL GAIN	f = 4.4 MHz		0.04			0.04			0.04		%
DIFFERENTIAL PHASE	f = 4.4 MHz		0.02			0.02			0.02		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±4.75**		**±18**	**±4.75**		**±18**	**±4.75**		**±18**	V
Rejection Ratio	V_S = ±5 to ±15 V	**88**	110		**95**	113		**88**	110		dB
Quiescent Current	T_{min} to T_{max}		10	12		10	**12**		10	**12**	mA

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C.

[3]FPBW=slew rate/2π V peak.

[4]"S" grade T_{min}-T_{max} are tested with automatic test equipment at T_A = −55°C and T_A = +125°C.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from these tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

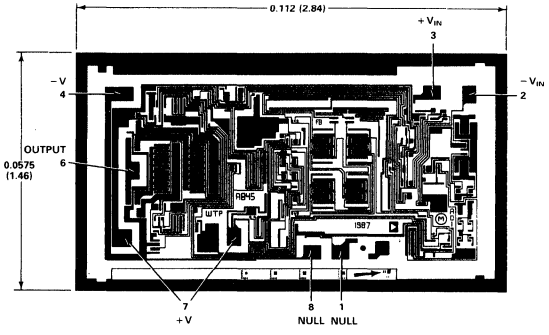
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic Mini-DIP . . . . . 1.6 Watts
Cerdip . . . . . 1.4 Watts
Input Voltage . . . . . $\pm V_S$
Output Short-Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range
Q . . . . . −65°C to +150°C
N, R . . . . . −65°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Mini-DIP package: θ_{JA} = 100°C/watt; cerdip package: θ_{JA} = 110°C/watt.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
AD845JN	0°C to +70°C	N-8
AD845KN	0°C to +70°C	N-8
AD845JR[3]	0°C to +70°C	R-8
AD845AQ	−40°C to +85°C	Q-8
AD845BQ	−40°C to +85°C	Q-8
AD845SQ	−55°C to +125°C	Q-8
AD845SQ/883B	−55°C to +125°C	Q-8

NOTES
[1]"J" and "S" grade chips are also available.
[2]N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.
[3]Available in tape and reel packaging.

2

AD845—Typical Characteristics

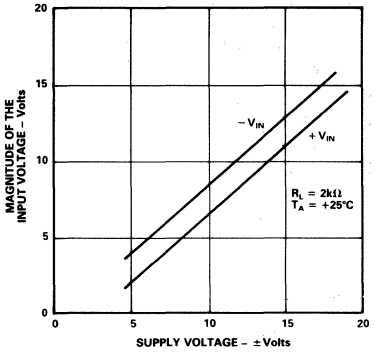


Figure 1. Input Voltage Swing vs. Supply Voltage

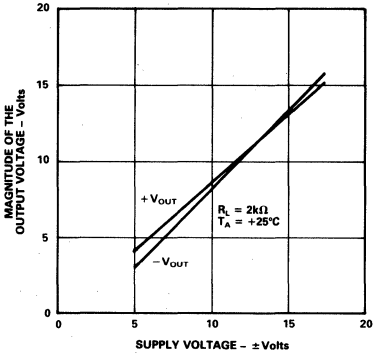


Figure 2. Output Voltage Swing vs. Supply Voltage

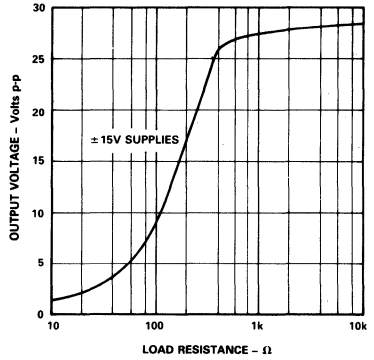


Figure 3. Output Voltage Swing vs. Resistive Load

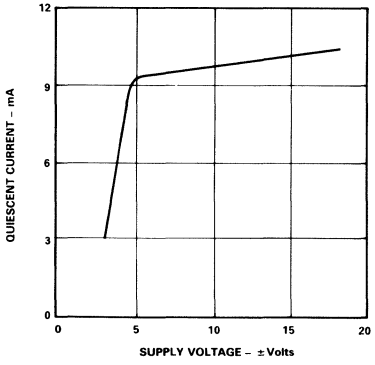


Figure 4. Quiescent Current vs. Supply Voltage

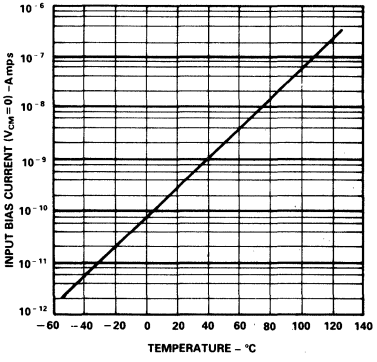


Figure 5. Input Bias Current vs. Temperature

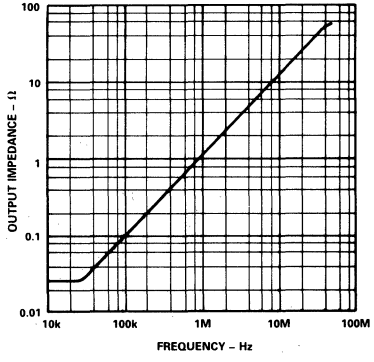


Figure 6. Magnitude of Output Impedance vs. Frequency

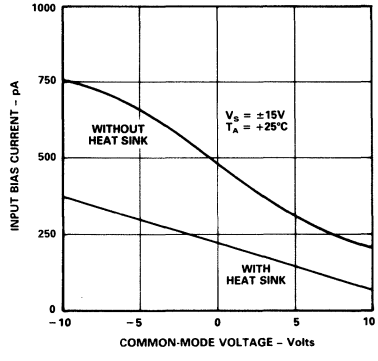


Figure 7. Input Bias Current vs. Common-Mode Voltage

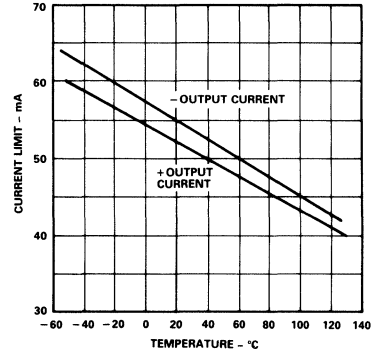


Figure 8. Short-Circuit Current Limit vs. Temperature

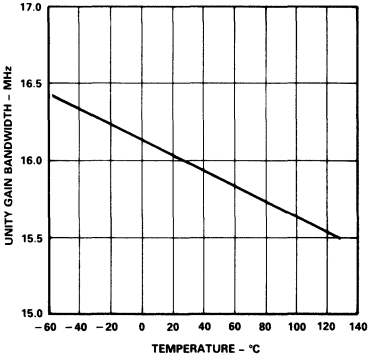


Figure 9. Unity-Gain Bandwidth vs. Temperature

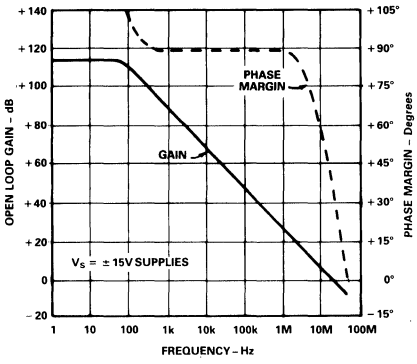


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

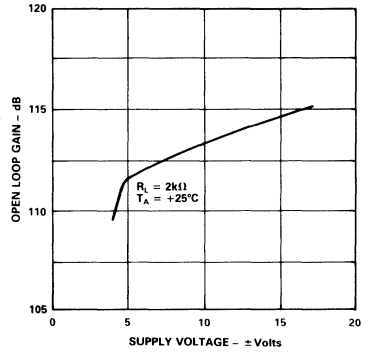


Figure 11. Open-Loop Gain vs. Supply Voltage

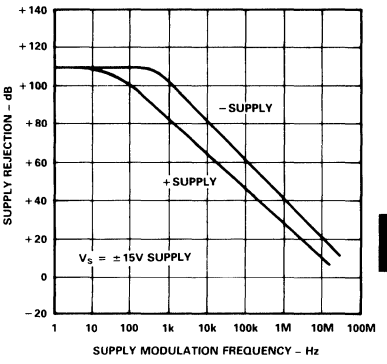


Figure 12. Power Supply Rejection vs. Frequency

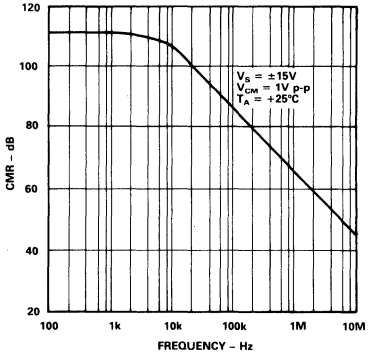


Figure 13. Common-Mode Rejection vs. Frequency

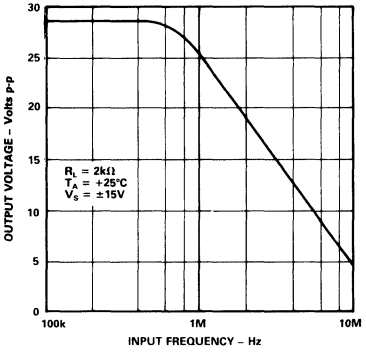


Figure 14. Large Signal Frequency Response

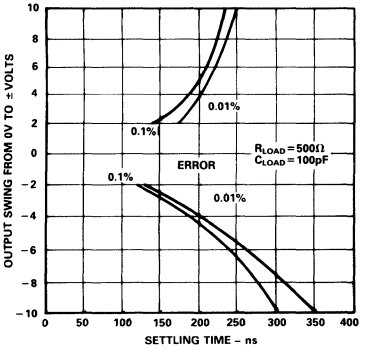


Figure 15. Output Swing and Error vs. Settling Time

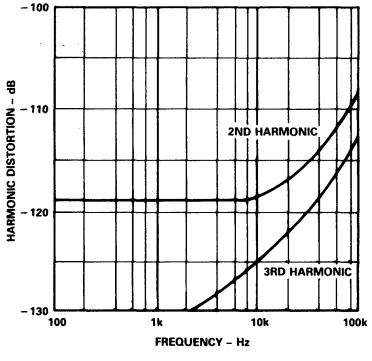


Figure 16. Harmonic Distortion vs. Frequency

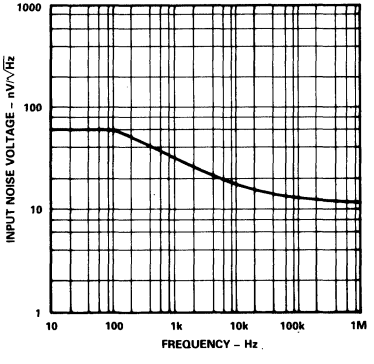


Figure 17. Input Noise Voltage Spectral Density

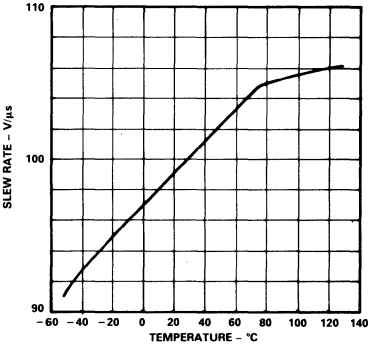


Figure 18. Slew Rate vs. Temperature

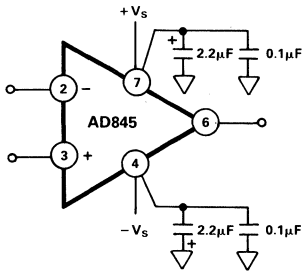


Figure 19. Recommended Power Supply Bypassing

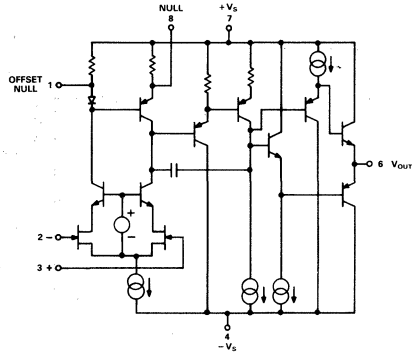


Figure 20. AD845 Simplified Schematic

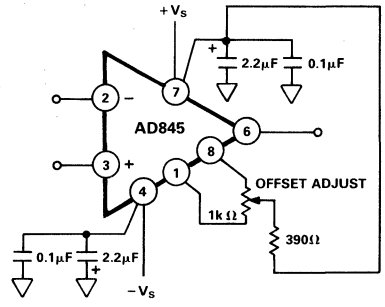


Figure 21. Offset Null Configuration

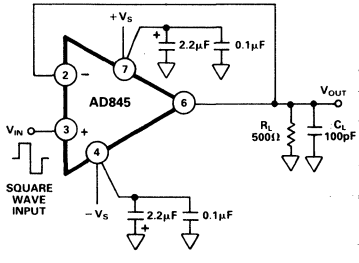


Figure 22a. Unity-Gain Follower

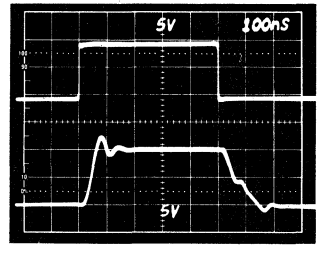


Figure 22b. Unity-Gain Follower Large Signal Pulse Response

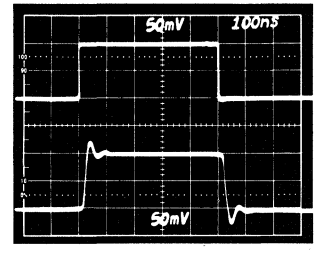


Figure 22c. Unity-Gain Follower Small Signal Pulse Response

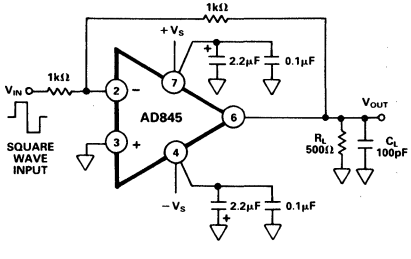


Figure 23a. Unity-Gain Inverter

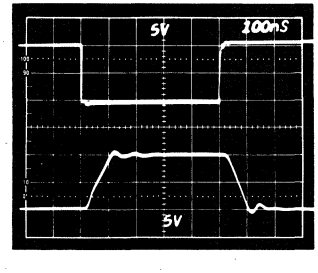


Figure 23b. Unity-Gain Inverter Large Signal Pulse Response

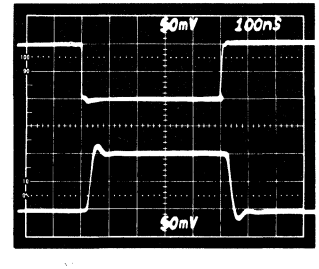


Figure 23c. Unity-Gain Inverter Small Signal Pulse Response

MEASURING AD845 SETTLING TIME

The Figure 24 shows the AD845 settling time performance. This measurement was accomplished by driving the amplifier in the unity-gain inverting mode with a fast pulse generator. The input summing junction was measured using false nulling techniques.

Settling time is defined as:

> The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

Components of settling time include:

1. Propagation time through the amplifier
2. Slewing time to approach the final output value
3. Recovery time from overload associated with the slewing
4. Linear settling to within a specified error band.

These individual components can easily be seen in Figure 24. Settling time is extremely important in high speed applications where the current output of a DAC must be converted to a voltage. When driving a 500 Ω load in parallel with a 100 pF capacitor, the AD845 settles to 0.1% in 250 ns and to 0.01% in 310 ns.

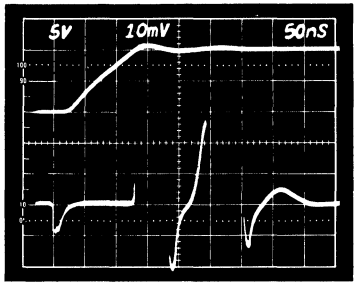


Figure 24. Settling Characteristics 0 to 10 V Step
Upper Trace: Output of AD845 Under Test (5 V/Div)
Lower Trace: Error Voltage (1 mV/Div)

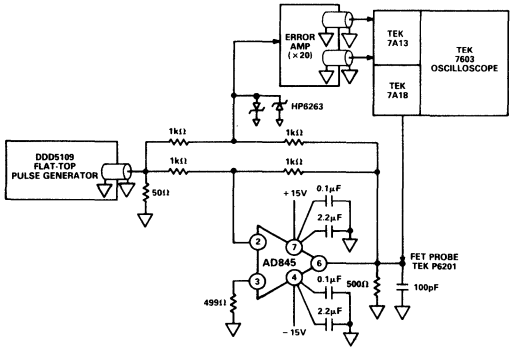


Figure 25. Settling Time Test Circuit

A HIGH SPEED INSTRUMENTATION AMP

The three op amp instrumentation amplifier circuit shown in Figure 26 can provide a range of gains from unity up to 1000 and higher. The instrumentation amplifier configuration features high common-mode rejection, balanced differential inputs and stable, accurately defined gain. Low input bias currents and fast settling are achieved with the FET input AD845.

Most monolithic instrumentation amplifiers do not have the high frequency performance of the circuit in Figure 26. The circuit bandwidth is 10.9 MHz at a gain of 1 and 8.8 MHz at a gain of 10; settling time for the entire circuit is 900 ns to 0.01% for a 10 V step (Gain = 10).

The capacitors employed in this circuit greatly improve the amplifier's settling time and phase margin.

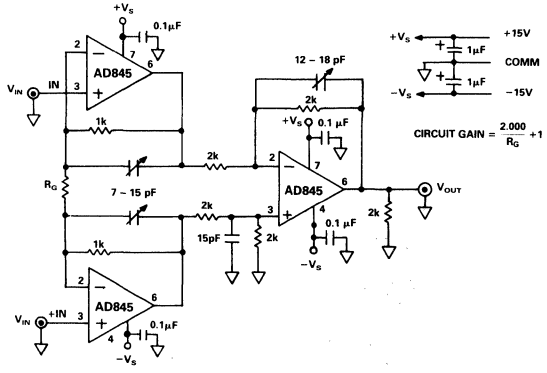


Figure 26. High Performance, High Speed Instrumentation Amplifier

3 OP-AMP IN-AMP

Gain	RG	Small Signal Bandwidth	Settling Time to 0.01%
1	Open	10.9 mHz	500 ns
2	2k	8.8 mHz	500 ns
10	226Ω	2.6 mHz	900 ns
100	20Ω	290 kHz	7.5 μs

Note: Resistors around the amplifiers' input pins need to be small enough in value so that the RC time constant they form, with stray circuit capacitance, does not reduce circuit bandwidth.

Table I. Performance Summary for the Three Op Amp Instrumentation Amplifier Circuit

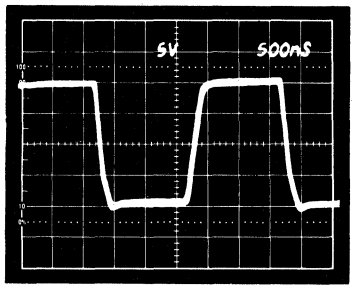


Figure 27. The Pulse Response of the Three Op Amp Instrumentation Amplifier. Gain = 1, Horizontal Scale: 0.5 ms/Div; Vertical Scale: 5 V/Div

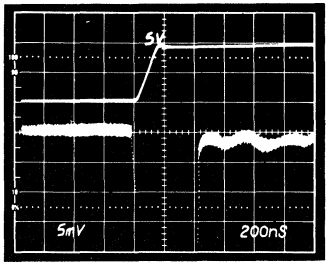


Figure 28a. Settling Time of the Three Op Amp Instrumentation Amplifier. Horizontal Scale:200 ns/Div; Vertical Scale, Positive Pulse Input: 5 V/Div; Output Settling: 1 mV/Div

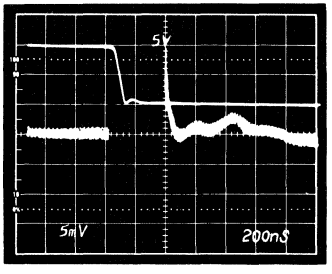


Figure 28b. Settling Time of the Three Op Amp Instrumentation Amplifier. Horizontal Scale: 200 ns/Div; Vertical Scale, Negative Pulse Input: 5 V/Div; Output Settling: 1 mV/Div

DRIVING THE ANALOG INPUT OF AN A/D CONVERTER

An op amp driving the analog input of an A/D converter, such as that shown in Figure 29, must be capable of maintaining a constant output voltage under dynamically changing load conditions. In successive-approximation converters, the input current is compared to a series of switched trial currents. The comparison point is diode clamped but may deviate several hundred millivolts resulting in high frequency modulation of A/D input current. The output impedance of a feedback amplifier is made artificially low by the loop gain. At high frequencies, where the loop gain is low, the amplifier output impedance can approach its open-loop value. Most IC amplifiers exhibit a minimum open-loop output impedance of 25 Ω due to current limiting resistors. A few hundred microamps reflected from the change in converter loading can introduce errors in instantaneous input voltage. If the A/D conversion speed is not excessive and the bandwidth of the amplifier is sufficient, the amplifier's output will return to the nominal value before the converter makes its comparison. However, many amplifiers have relatively narrow bandwidth yielding slow recovery from output transients. The AD845 is ideally suited to drive high resolution A/D converters with 5 μs on longer conversion times since it offers both wide bandwidth and high open-loop gain.

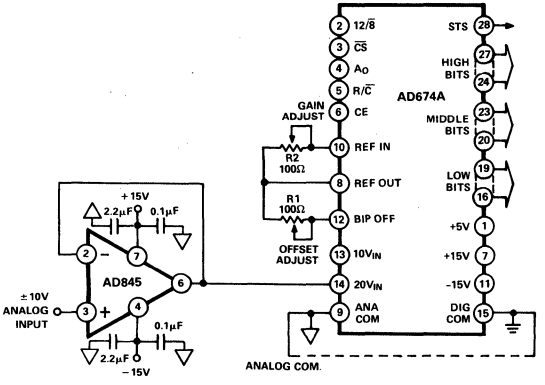


Figure 29. AD845 As ADC Unity Gain Buffer

ANALOG DEVICES

450 V/μs, Precision, Current-Feedback Op Amp

AD846

FEATURES

AC PERFORMANCE
- Small Signal Bandwidth: 80 MHz (A_V = −1)
- Slew Rate: 450 V/μs
- Full Power Bandwidth: 6.8 MHz at 20 V p-p, R_L = 500 Ω
- Fast Settling: for 10 V Step: 110 ns to 0.01%, 80 ns to 0.1%
- Differential Gain: <0.01% @ 4.4 MHz
- Differential Phase: <0.028° @ 4.4 MHz
- Total Harmonic Distortion (THD): 0.0005% @ 100 kHz
- Open-Loop Transimpedance: 200 MΩ
- Input Voltage Noise: 2 nV/√Hz

DC PERFORMANCE
- Input Offset Voltage: 75 μV max (B Grade)
- Input Offset Drift: 3.5 μV/°C max (B Grade)
- Quiescent Supply Current: 6.5 mA max

APPLICATIONS
- High Speed DAC Buffers
- Multiflash ADC Error Amplifiers
- Flash ADC Buffers
- Coaxial Cable Drivers
- High Performance Audio Circuitry
- Available in Plastic Mini-DIP, Hermetic Cerdip, and Hermetic Metal Can Packages
- MIL-STD-883B Parts Available

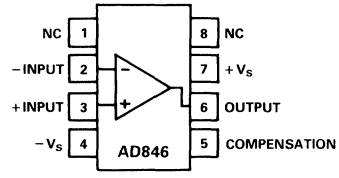
PRODUCT DESCRIPTION

The AD846 is a monolithic, very high speed operational amplifier offering high performance. Although technically classed as a current-feedback or transimpedance amplifier, it may be used in much the same way as traditional op amps while providing significant performance benefits. Employing Analog Devices' junction isolated complementary bipolar (CB) process, the AD846 achieves true "12-bit" (0.01%) precision on critical ac and dc parameters, a level of performance unmatched by amplifiers fabricated using either the dielectrically isolated (DI) or other bipolar processes.

The AD846 offers significant advantages over conventional high speed operational amplifiers. It maintains a nearly constant bandwidth and settling time to 0.01% over a wide range of closed-loop gains. This makes the AD846 ideal for amplifying the residue in multiple-pass analog-to-digital converters.

CONNECTION DIAGRAM

Plastic Mini-DIP (N) Package
and
Cerdip (Q) Package
Top View



NC = NO CONNECT

Other advantages include: low input errors and high open-loop transresistance (200 MΩ) into a 500 Ω load, ensuring true 12-bit dc accuracy for closed-loop gains from −1 to gains greater than −100. This combination of ac and dc performance makes the AD846 an excellent choice for buffering precision high speed DACs and flash ADCs.

The AD846 is available in three performance grades. The AD846A and AD846B are rated over the industrial temperature range of −40°C to +85°C. The AD846S is rated over the full military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev C.

Extended reliability PLUS screening is available specified over the commercial temperature range. PLUS screening includes 168 hour burn-in as well as other environmental and physical tests. The AD846 is available in two types of 8-pin package: plastic mini-DIP and hermetic cerdip. "A" and "S" grade chips are also available.

PRODUCT HIGHLIGHTS

1. The AD846 achieves settling times of 110 ns to 0.01% for gains of −1 to −10, with a 450 V/μs slew rate, while consuming only 5 mA of supply current.
2. For closed-loop gains of −1 to −100, the high speed performance of the AD846 is achieved without sacrificing full 12-bit dc precision.
3. The AD846 is well suited to line driver and video buffer applications where the properties of low distortion and high slew rate are required.

AD846—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD846A Min	AD846A Typ	AD846A Max	AD846B Min	AD846B Typ	AD846B Max	AD846S Min	AD846S Typ	AD846S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial			25	**200**		25	**75**		25	**200**	μV
T_{min}–T_{max}			50	350		50	**125**		100	**350**	μV
vs. Temperature			0.8	5		0.8	3.5		1	5.5	μV/°C
vs. Supply (PSRR)	5 V–18 V[2]										
Initial		**110**	125		**120**	125		**110**	125		dB
T_{min}–T_{max}		110	120		**116**	120		**94**	116		dB
vs. Common Mode (CMRR)	V_{CM} = ±10 V										
Initial		**110**	125		**120**	125		**110**	125		dB
T_{min}–T_{max}		110	120		**116**	120		**94**	116		dB
INPUT BIAS CURRENT[3]											
–Input Bias Current											
Initial			150	**450**		100	**250**		150	**450**	nA
T_{min}–T_{max}			450	1200		400	**750**		1000	**1500**	nA
vs. Temperature			6	20		6	**17**		9	20	nA/°C
vs. Supply	5 V–18 V[2]										
Initial			9	**15**		9	**10**		9	**15**	nA/V
T_{min}–T_{max}			11	20		11	**15**		11	**25**	nA/V
vs. Common Mode	V_{CM} = ±10 V										
Initial			5	**10**		3	**5**		5	**10**	nA/V
T_{min}–T_{max}			5	15		3	7		5	**20**	nA/V
+Input Bias Current											
Initial			3	**15**		3	**5**		3	**15**	μA
T_{min}–T_{max}			4	20		4	7		5	**20**	μA
vs. Temperature			15	80		15	45		15	80	nA/°C
vs. Supply	5 V–18 V[2]										
Initial			5	**15**		5	**10**		5	**15**	nA/V
T_{min}–T_{max}			5	20		5	**15**		5	**20**	nA/V
vs. Common Mode	V_{CM} = ±10 V										
Initial			5	**15**		3	**10**		5	**15**	nA/V
T_{min}–T_{max}			5	15		3	**10**		5	**20**	nA/V
INPUT CHARACTERISTICS											
Input Resistance											
–Input			50			50			50		Ω
+Input			10			10			10		kΩ
Input Capacitance											
–Input			2			2			2		pF
+Input			2			2			2		pF
INPUT VOLTAGE RANGE											
Common Mode		±10			±10			±10			V
INPUT VOLTAGE NOISE	F = 1 kHz		2			2			2		nV/√Hz
Input Current Noise											
–Input	1 kHz		20			20			20		pA/√Hz
+Input	1 kHz		6			6			6		pA/√Hz
OPEN LOOP TRANSRESISTANCE	V_{OUT} = ±10 V										
	R_{LOAD} = 500 Ω	**100**	200		**150**	200		**100**	200		MΩ
	T_{min}–T_{max}	50			75			**50**			MΩ
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} = 500 Ω	**±10**			**±10**			**±10**			V
Current	Short Circuit		65			65			65		mA
Output Resistance	Open Loop		16			16			16		Ω
FREQUENCY RESPONSE											
Small Signal Bandwidth	A_V = −1 R_F = 1k		80			80			80		MHz
(−3dB)	A_V = −10 R_F = 875 Ω		31			31			31		MHz
	A_V = −30 R_F = 875 Ω		15			15			15		MHz
Full Power Bandwidth[4]	V_{OUT} = 20 V p-p										
	R_I = 500 Ω		6.8			6.8			6.8		MHz
Rise Time	A_V = −1		10			10			10		ns
Overshoot	A_V = −1		20			20			20		%
Slew Rate	A_V = −1		450			450			450		V/μs
Settling Time											
10 V Step, A_V = −1	to 0.1%		80			80			80		ns
	to 0.01%		110			110			110		ns
TOTAL HARMONIC DISTORTION[5]	F = 100 kHz		0.0005			0.0005			0.0005		%

Model	Conditions	AD846A Min	AD846A Typ	AD846A Max	AD846B Min	AD846B Typ	AD846B Max	AD846S Min	AD846S Typ	AD846S Max	Units
DIFFERENTIAL GAIN	F = 4.4 MHz, R_L = 100 Ω		0.01			0.01			0.01		%
DIFFERENTIAL PHASE	F = 4.4 MHz, R_L = 100 Ω		0.028			0.028			0.028		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±5		**±18**	**±5**		**±18**	**±5**		**±18**	V
Quiescent Current	T_{min}–T_{max}		5	**6.5**		5	**6.5**		5	7	mA
TRANSISTOR COUNT			72			72			72		

NOTES
[1]Input Offset Voltage Specifications are guaranteed after 5 minutes at T_A = +25°C.
[2]Test Conditions: $+V_S$ = 15 V, $-V_S$ = 5 V to 18 V and $+V_S$ = 5 V to 18 V, $-V_S$ = 15 V.
[3]Bias Current Specifications are guaranteed maximum after 5 minutes at T_A = +25°C.
[4]FPBW = Slew Rate/2 π V_{PEAK}.
[5]Total Harmonic Distortion.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
  Plastic Package . . . . . 1.5 W
  Cerdip Package . . . . . 1.3 W
Common-Mode Input Voltage, Max Safe . . . . . $|V_S|$ −3 V
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . ±1 V
Continuous Input Current
  Inverting or Noninverting . . . . . 2.0 mA
Storage Temperature Range Q . . . . . −65°C to +150°C
Storage Temperature Range N . . . . . −65°C to +125°C
Operating Temperature Range
  AD846A/B . . . . . −40°C to +85°C
  AD846S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C, derate cerdip (Q) package at 8.7 mW/°C and plastic (N) package at 10 mW/°C.
Plastic Package: θ_{JA} = 100°C/Watt, θ_{JC} =33°C/W.
Cerdip Package: θ_{JA} = 110°C/Watt, θ_{JC} = 30°C/W.

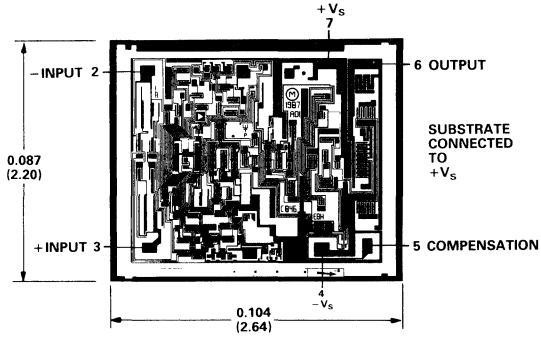
ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
AD846AN	−40°C to +85°C	N-8
AD846BN	−40°C to +85°C	N-8
AD846AQ	−40°C to +85°C	Q-8
AD846BQ	−40°C to +85°C	Q-8
AD846SQ	−55°C to +125°C	Q-8
AD846SQ/883B	−55°C to +125°C	Q-8

NOTES
[1]"A" and "S" grade chips are also available.
[2]N = Plastic DIP Package; Q = Cerdip Package. For outline information see Package Information section.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Consult factory for latest dimensions.



AD846 — Typical Characteristics

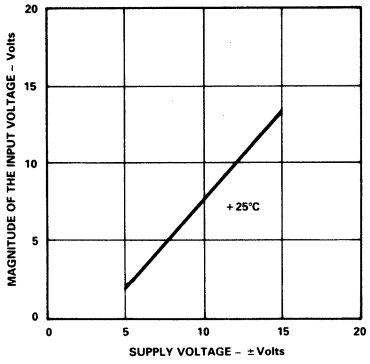


Figure 1. Input Voltage Swing vs. Supply

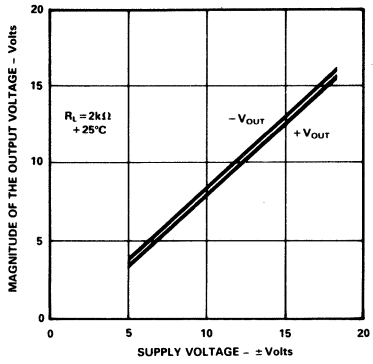


Figure 2. Output Voltage Swing vs. Supply

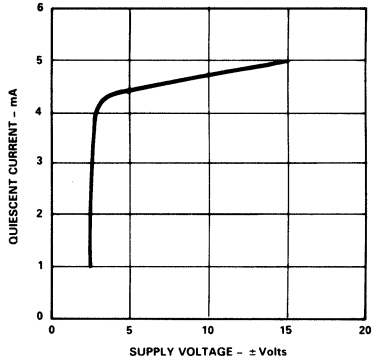


Figure 3. Quiescent Current vs. Supply Voltage

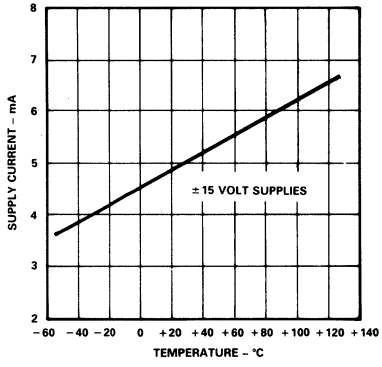


Figure 4. Quiescent Supply Current vs. Temperature

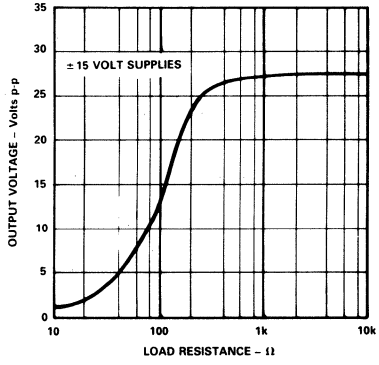


Figure 5. Output Voltage Swing vs. Resistive Load

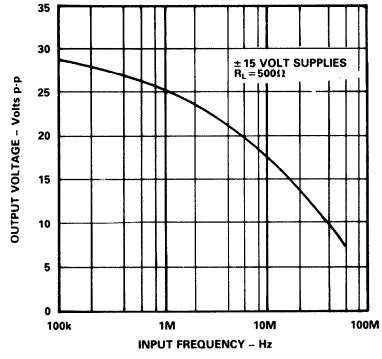


Figure 6. Large Signal Frequency Response

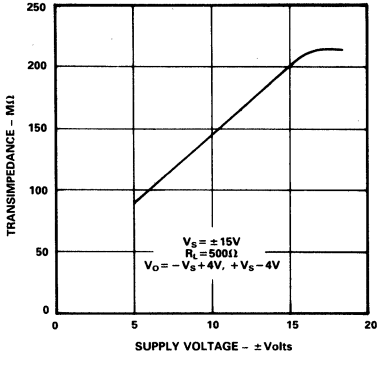


Figure 7. Open-Loop Transimpedance vs. Supply

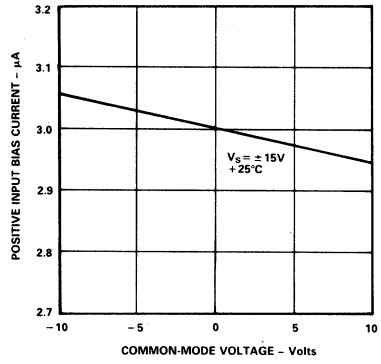


Figure 8. Positive Input Bias Current vs. Common-Mode Voltage

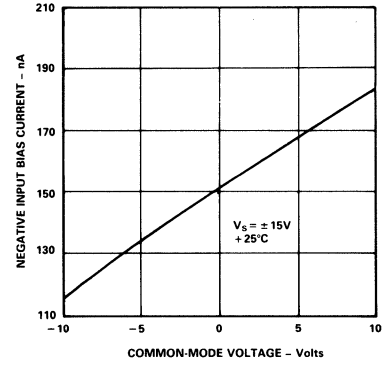


Figure 9. Negative Input Bias Current vs. Common-Mode Voltage

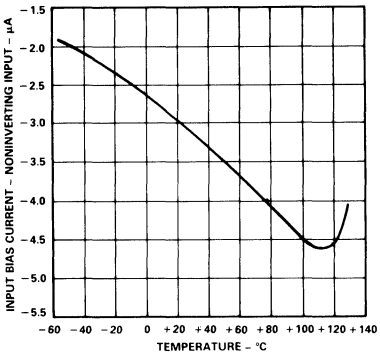


Figure 10. Positive Input Bias Current vs. Temperature

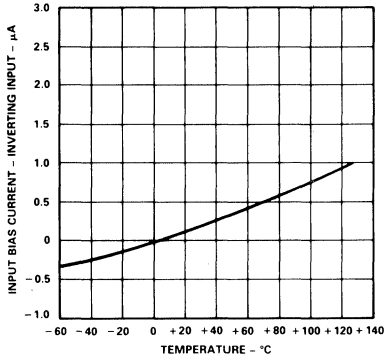


Figure 11. Negative Input Bias Current vs. Temperature

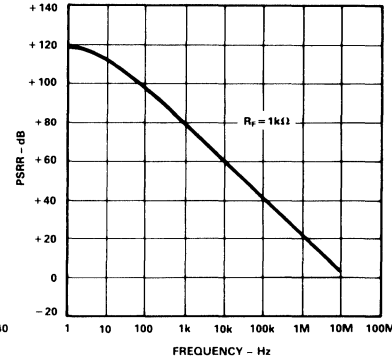


Figure 12. Power Supply Rejection vs. Frequency

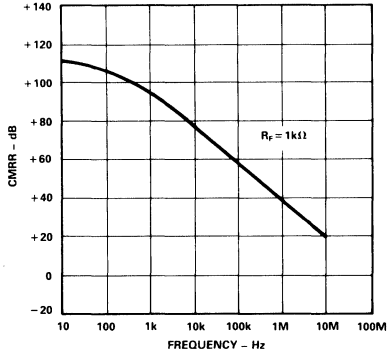


Figure 13. Common-Mode Rejection vs. Frequency

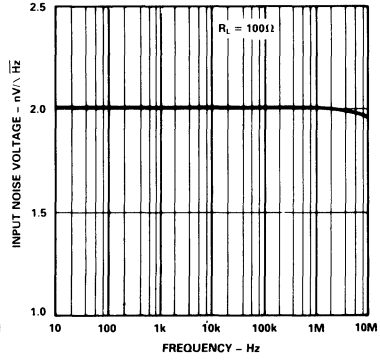


Figure 14. Input Noise Voltage Spectral Density

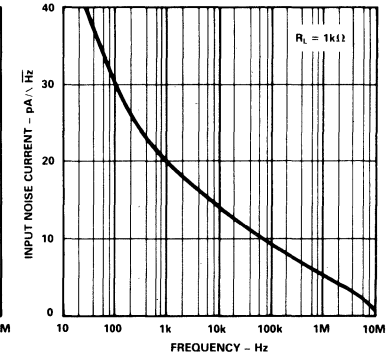


Figure 15. Inverting Input Noise Current Spectral Density

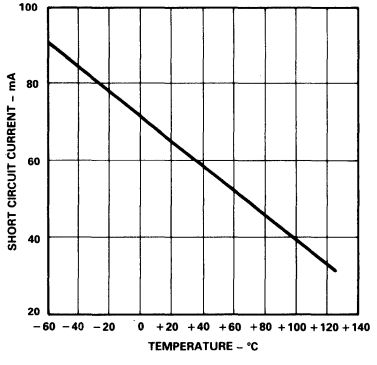


Figure 16. Short Circuit Current Limit vs. Temperature

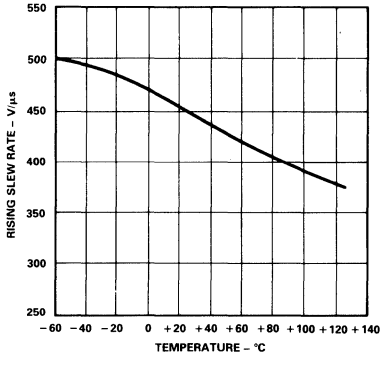


Figure 17. Slew Rate vs. Temperature

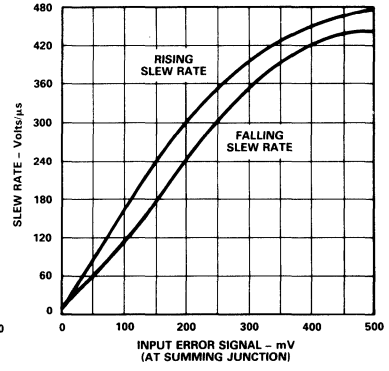


Figure 18. Slew Rate vs. Input Error Signal

AD846—Typical Characteristics, Inverting Gain of 1

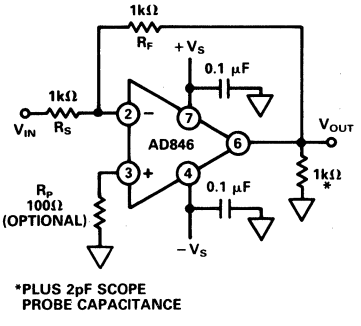


Figure 19a. Inverting Amplifier, Gain of 1

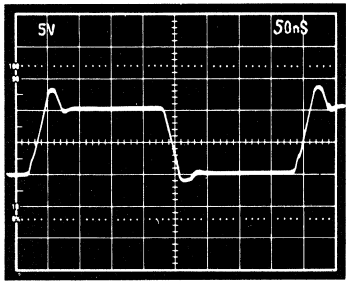


Figure 19b. Large Signal Pulse Response, Gain of −1

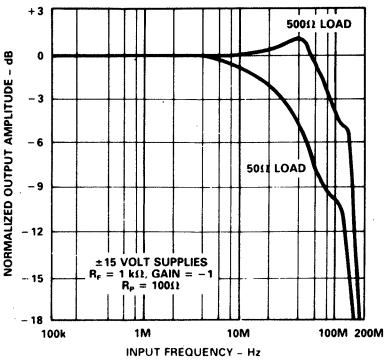


Figure 20. Normalized Output Amplitude vs. Frequency vs. Load

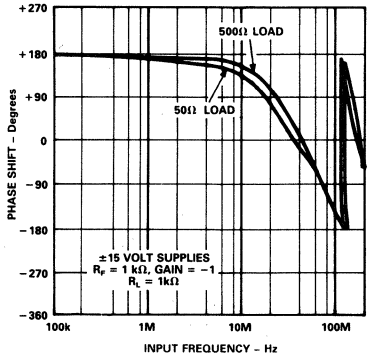


Figure 21. Phase Shift vs. Frequency

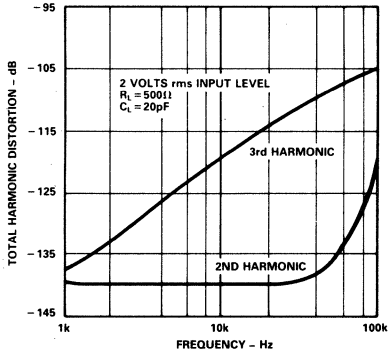


Figure 22. Total Harmonic Distortion vs. Frequency

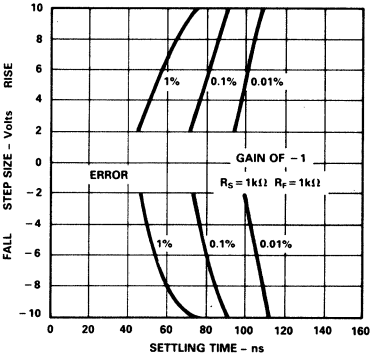


Figure 23. Settling Time vs. Step Size

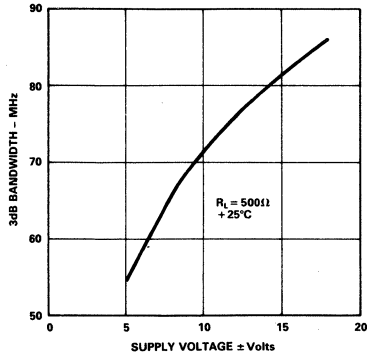


Figure 24. 3 dB Bandwidth vs. Supply Voltage

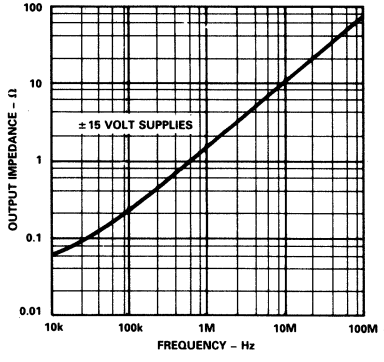


Figure 25. Output Impedance vs. Frequency

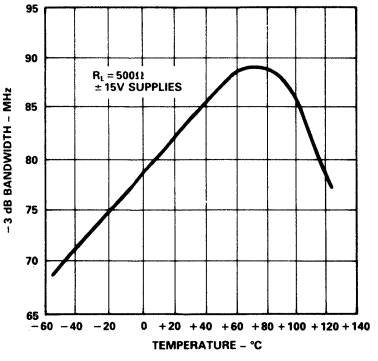


Figure 26. 3 dB Bandwidth vs. Temperature

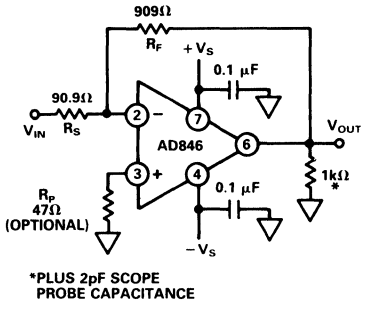


Figure 27a. Inverting Amplifier, Gain of 10

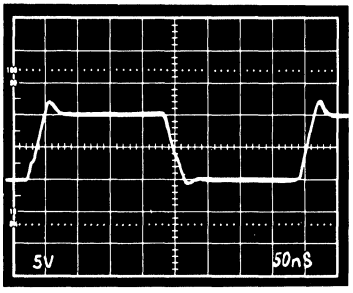


Figure 27b. Large Signal Pulse Response, Gain of 10

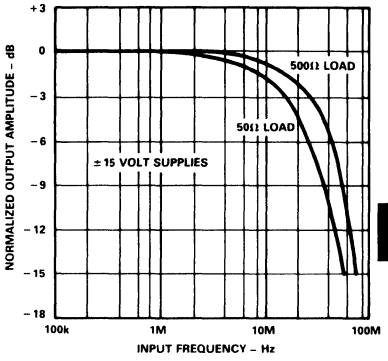


Figure 28. Normalized Output Amplitude vs. Frequency vs. Load

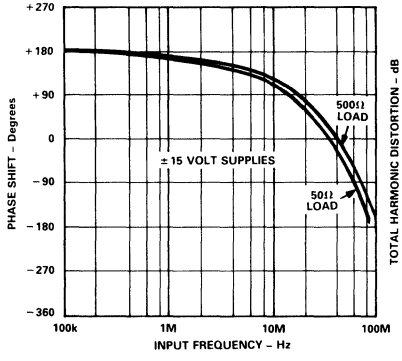


Figure 29. Phase vs. Frequency vs. Load

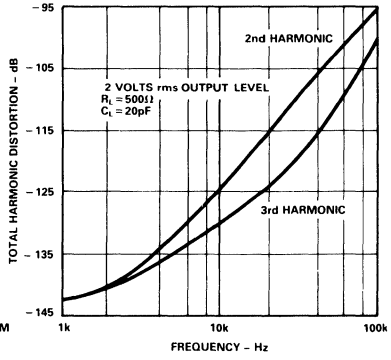


Figure 30. Harmonic Distortion vs. Frequency

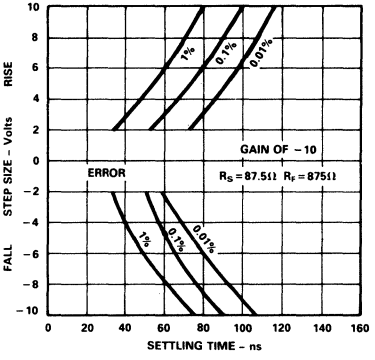


Figure 31. Settling Time vs. Step Size

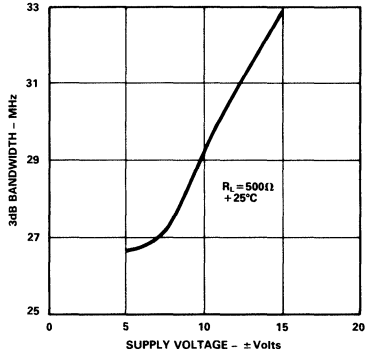


Figure 32. 3 dB Bandwidth vs. Supply Voltage

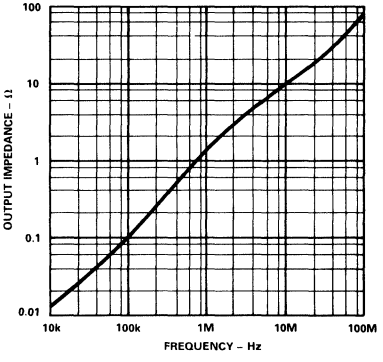


Figure 33. Output Impedance vs. Frequency

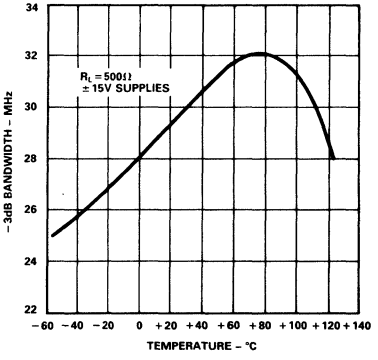


Figure 34. 3 dB Bandwidth vs. Temperature

Applying the AD846

POWER SUPPLY CONSIDERATIONS

The power supply connections to the AD846 must maintain a low impedance to ground over a bandwidth of 40 MHz or more. This is especially important when driving a significant resistive or capacitive load, since all current delivered to the load comes from the power supplies. Multiple high quality bypass capacitors are recommended for each power supply line in any critical application. A 0.1 μF ceramic and a 2.2 μF electrolytic capacitor as shown in Figure 35 placed as close as possible to the amplifier (with short lead lengths to power supply common) will assure adequate high frequency bypassing, in most applications. A minimum bypass capacitance of 0.1 μF should be used for any application.

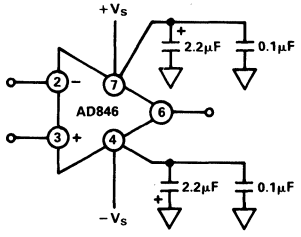


Figure 35. Recommended Power Supply Bypassing

THEORY OF OPERATION

The AD846 differs from conventional operational amplifiers in that it is a transimpedance device rather than a conventional voltage amplifier. Figure 36 is a simplified schematic of the AD846. The input stage consists of a pair of transistors, Q1 and Q2, which are biased by two diode-connected transistors, Q3 and Q4. Transistors Q1 and Q2 have their emitters connected together, and this common point functions as the inverting input of the amplifier. Correspondingly, the common connection of the two biasing diodes acts as the noninverting input.

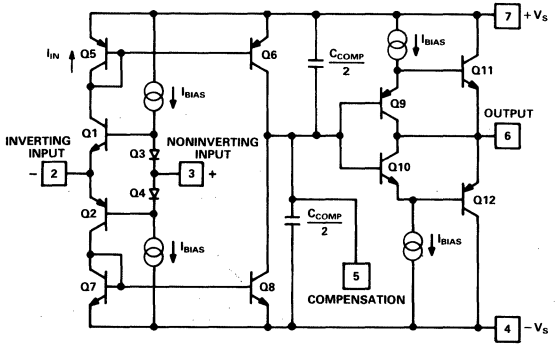


Figure 36. AD846 Simplified Schematic

When operated as a closed-loop amplifier, feedback error current, I_{IN}, flows into the inverting input terminal and is conveyed via current mirrors (transistors Q5, Q6, Q7, and Q8) to the compensation capacitor, C_{COMP}. The voltage developed across C_{COMP} is buffered by the output stage, consisting of transistors Q9–Q12.

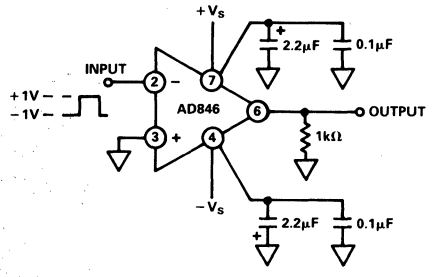


Figure 37. Overload Recovery Test Circuit

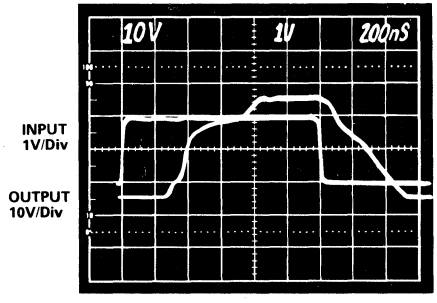


Figure 38. Overload Recovery Time Photo

Because the input error signal developed is in the form of a current, not a voltage, the AD846 differs from conventional operational amplifiers. This also means that, unlike most operational amplifiers which rely on negative feedback to produce a "virtual ground" at the inverting input terminal, this terminal explicitly has a low impedance.

A unique circuit approach allows the AD846 to realize an open-loop transimpedance of close to 200 MΩ. This is nearly three orders of magnitude greater than that of any other operational transimpedance amplifier and results in extremely high levels of dc precision.

As an example, the output voltage gain error is approximately equal to the value of the feedback resistor divided by the value of the open-loop transimpedance of the amplifier. That is, when using a 1 kΩ feedback resistor, this error is one part in 200,000. For a transimpedance amplifier with 1 MΩ transimpedance, this error is only one part in 1000; such an amplifier would barely be able to achieve 10-bit precision.

Figure 39 is a simplified three-terminal model for the AD846. Figure 40 is a simplified three-terminal model for a conventional voltage op amp. The action of current feedback serves to modify the behavior of the amplifier under closed-loop conditions. The feedback resistor, R_F, is somewhat analogous to the input stage transconductance of a conventional voltage amplifier; and therefore, if the value of R_F is held constant, the closed-loop bandwidth also remains virtually constant, independent of closed-loop voltage gain.

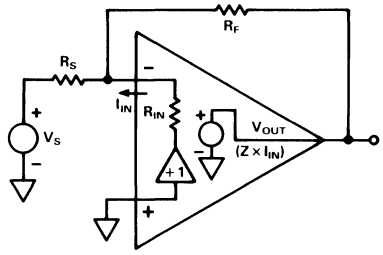


Figure 39. AD846 Three-Terminal Model

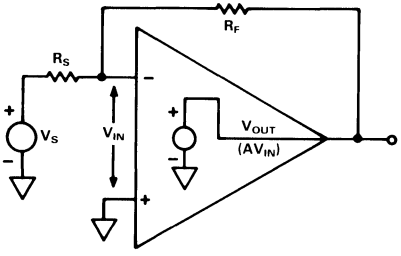


Figure 40. Op Amp Three-Terminal Model

A more detailed examination of the closed-loop transfer function of the AD846 results in the following equation:

$$\text{Closed-Loop Gain } G(s) = \frac{\frac{-R_F}{R_S}}{\left(1 + C_{COMP}\left[R_F + \left(1 + \frac{R_F}{R_S}\right)R_{IN}\right] s\right)}$$

Compare this to the equation for a conventional op amp:

$$\text{Closed-Loop Gain } G(s) = \frac{\frac{-R_F}{R_S}}{\left(1 + \frac{C_{COMP}}{g_M}\left(1 + \frac{R_F}{R_S}\right) s\right)}$$

where: C_{COMP} is the internal compensation capacitor of the amplifier; g_M is the input stage transconductance of the amplifier.

In the case of the voltage amplifier, the closed-loop bandwidth decreases directly with increasing values of $(1 + R_F/R_S)$, the closed-loop gain. However, for the transimpedance amplifier, the situation is different. At low gains, where $(1 + R_F/R_S)\ R_{IN}$ is small compared to R_F, the closed-loop bandwidth is controlled by the internal compensation capacitance of 7 pF and the value of R_F, and not by the closed-loop gain. At higher gains, where $(1 + R_F/R_S)\ R_{IN}$ is much larger than R_F, the behavior is that of a conventional operational amplifier in which the input stage transconductance is equal to the inverting terminal input impedance of the transimpedance amplifier (R_{IN} = 50 Ω).

A simple equation can, therefore, be used to determine the bandwidth of an amplifier employing the AD846 in the inverting configuration.

$$3\ dB\ Bandwidth = \frac{23}{R_F + 0.05\ (1 + G)}$$

where: The 3 dB bandwidth is in MHz
G is the closed-loop inverting gain of the AD846
R_F is the feedback resistance in kΩ.

NOTE: This equation applies only for values of R_F between 10 kΩ and 100 kΩ, and for R_{LOAD} greater than 500 Ω. For R_F = 1 kΩ the bandwidth should be estimated from Figure 41.

Figure 41 illustrates the closed-loop voltage gain vs. frequency of the AD846 for various values of feedback resistor. For comparison purposes, the characteristic of a conventional amplifier having an 80 MHz unity gain bandwidth is also shown.

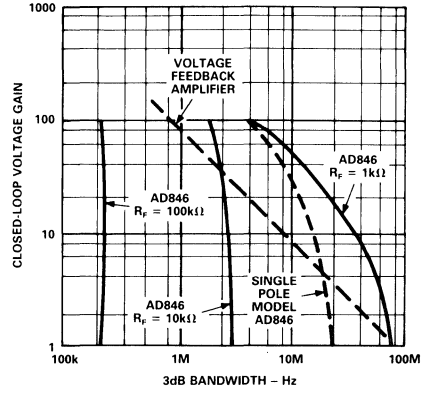


Figure 41. Closed-Loop Voltage Gain vs. Bandwidth for Various Values of R_F

For the case where R_F = 1 kΩ and R_S = 100 Ω (closed-loop gain of −10), the closed-loop bandwidth is approximately 28 MHz. It should also be noted that the use of a capacitor to shunt R_F, a normal practice for stabilizing conventional op amps, will cause this amplifier to become unstable because the closed-loop bandwidth will increase beyond the stable operating frequency.

A similar approach can be taken to calculate the noise performance of the amplifier. A simplified noise model is shown in Figure 42.

The equivalent mean-square output noise voltage spectral density will equal:

$$V_{ON}^2 = (R_F\ I_{NN})^2 + \left(1 + \frac{R_F}{R_S}\right)^2 [V_N^2 + (R_P\ I_{NP})^2 + 4\ kT\ R_P] + 4\ kT\ R_F\left(\frac{R_F}{R_S} + 1\right)$$

Where:

R_P is the external resistance placed in series with the noninverting input
R_F is the feedback resistor
R_S is the source resistor
I_{NN} is the noise current in the inverting input
I_{NP} is the noise current in the noninverting input
V_N is the input noise voltage.

Typical values for these parameters (@ 1 kHz) in pA/$\sqrt{\text{Hz}}$ are: I_{NN} = 20, I_{PN} = 6, V_N = 2.

Or, referring to the signal input, the equivalent mean-square input voltage noise is:

$$V_{IN}^2 = (R_F I_{NN})^2 + \left(1 + \frac{R_S}{R_F}\right)^2 [V_N^2 + (R_P I_{NP})^2 + 4\,kT\,R_P]$$

$$+ 4\,kT\,R_S\left(1 + \frac{R_S}{R_F}\right)$$

Resistor R_P is required for both inverting and noninverting (follower) operation, to insure stable operation. The amplifier's noninverting input current (flowing through R_P of 100 Ω) will typically add less than 300 μV to the AD846's input offset voltage. This can be trimmed-out using the optional network shown in Figure 44. The following table gives recommended values for R_P.

Supply Voltage	Gain (R_F/R_S)	Recommended Value for R_P
6 V to 15 V	1–10	100 Ω
6 V to 15 V	10–20	47 Ω
6 V to 15 V	20–200	0 Ω
5 V	1–10	47 Ω
5 V	10–200	0 Ω

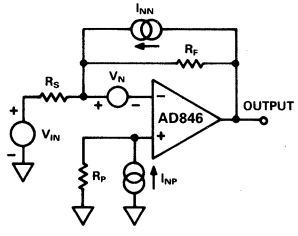


Figure 42. Op Amp Simplified Noise Model

NONINVERTING GAIN OPERATION

The AD846 can be used as a noninverting amplifier or voltage follower, operating at gains between 1 and 200. A minimum value of R_F equal to 1 kΩ should be employed. For low gains (1 to 2), the input signal should be applied to the AD846's noninverting input through a 100 Ω series resistor; this will help reduce peaking. The best transient response will occur when the amplifier's output level is below 5 V peak to peak.

At closed-loop gains of 3 or more, the input resistor is not required unless peak signals greater than 3 V will be applied. The amplifier's bandwidth can be determined by using the inverting amplifier's bandwidth equation or from Figure 41. For example, at a gain of +10 (R_F = 1 kΩ, R_S = 100 Ω) the bandwidth of the AD846 will be approximately 33 MHz; at a gain of +100, (R_F = 1 kΩ, R_S = 10 Ω) it will be 4 MHz. At gains of 3 or greater, a small capacitor (2 pF–5 pF) connected across the feedback resistor will help reduce overshoot; but when operating at noninverting gains below 3, this same capacitance will cause instability.

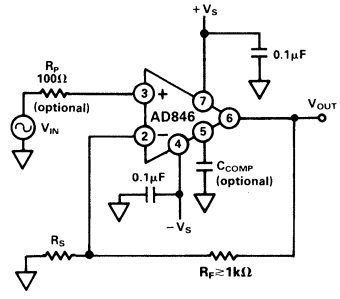


Figure 43. AD846 Noninverting Amplifier Configuration

USING THE COMPENSATION PIN OF THE AD846

Additional compensation may be provided for the AD846 by applying an external capacitance between Pin 5 and analog ground (Figure 44). The nominal value of the AD846's internal compensation capacitor is 7 pF. For a given value of feedback resistance (R_F), any added external capacitance reduces the amplifier's slew rate and bandwidth proportionally.

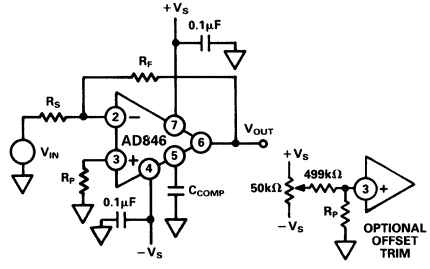


Figure 44. AD846 Inverting Amplifier Showing External Compensation Connection, R_P and Optional V_{OS} Trim

In addition to providing for external compensation, Pin 5 may be used to clamp the output of the amplifier, as shown in Figure 45. The output can be clamped anywhere within the output range (approximately ±10 V) of the amplifier. The input should also be clamped as a precaution against damaging the amplifier's input transistors.

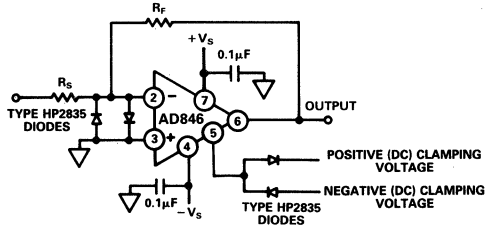


Figure 45. AD846 Used as a Clamped Amplifier

This compensation node may also be used as an additional output terminal as in the precision transconductance amplifier application of Figure 46.

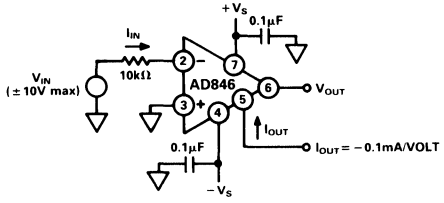


Figure 46. A Precision Transconductance Amplifier

The AD846 can be used in either the inverting transconductance mode as shown in Figure 46, or in a noninverting mode with R_S grounded and V_{IN} applied to the noninverting terminal. The current output is essentially constant over a compliance range of ±10 V at the compensation node. The output current (from Pin 5) is limited to about ±1 mA due to internal saturation. Under these circumstances the normal output pin provides a buffered version of the compensation node output voltage. Output load impedance of 500 Ω or greater will not affect the accuracy of the transconductance conversion.

THE AD846 IN A 2 MHz, 12-BIT SUBRANGING A/D CONVERTER CIRCUIT

The combination of fast settling times at high gains and low dc errors make the AD846 ideal for use as an error amplifier in high speed, 12-bit subranging A-D applications. In the circuit of Figure 47, an AD842 serves as an input amplifier. First pass conversion is accomplished, in a straightforward manner, determining the top 7 bits. The latch then holds these top 7 bits which are applied to a 7 bit, 12-bit accurate DAC and also to the highest 7 bits of the adder (note that a sample-and-hold should be used ahead of this converter to minimize errors due to its 500 ns acquisition time). In the second pass, the input switches S1 and S2 and S3 are set to state 2. The DAC output is then subtracted from the input signal and the resulting difference is then amplified by an AD846 gain of 32 follower. This gain, together with a 1/64th scale offset, insures a unipolar residue which can be converted by the flash A-D. Conversion is accomplished via switches S1, S2 and S3 in state 1. Switch S1 connects the input signal of the AD846 residue amplifier to ground which minimized overload recovery time.

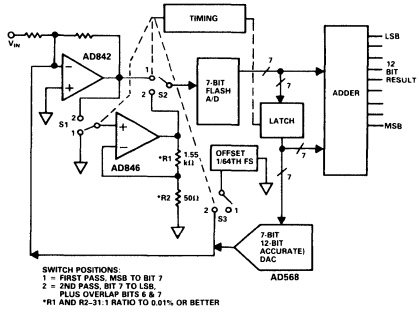


Figure 47. Block Diagram of a 2 MHz, 12-Bit Subranging A/D Converter

THE AD846 AS AN OPEN-LOOP LEVEL SHIFTER

The AD846 can also be used for open-loop level shifting. As shown in Figure 48, resistor R_S is used to develop an input current which is proportional to the input voltage, V_{IN}. This current flows from the compensation node (Pin 5) developing a voltage across resistor R_C (R_C is equal in value to resistor R_S) which, rather than being grounded, has one end tied to reference voltage V2. The voltage appearing at Pin 5 is, therefore, voltage V_{IN} plus voltage V2 and will directly follow changes in V_{IN}. By scaling resistor R_C, a level shift with voltage gain can be produced.

In addition, the normal voltage output at Pin 6 is approximately equal to the voltage at Pin 5 thus providing a low impedance, buffered output for the level shifter.

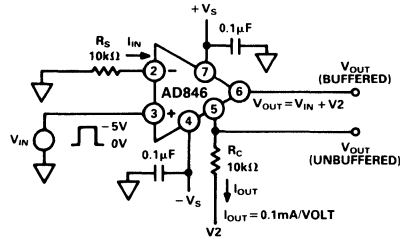


Figure 48. AD846 Connected as a Level Shift Amplifier

THE AD846 AS A HIGH SPEED DAC BUFFER

The AD846 will enable the AD568 12-bit DAC to develop a 10 V output step which settles to within 0.025 percent of its final value in about 100 ns. This AD846/AD568 combination is shown in the circuit of Figure 49. Correct power supply decoupling is essential: a 2.2 μF tantalum capacitor connected in parallel with a 0.1 μF to 0.01 μF ceramic disc capacitor is usually sufficient. These should be placed as close to the power supply pins as possible. Also, a ground plane should be employed; this ensure that there is a low impedance signal path to ground which allows the fastest possible output settling. In 12-bit systems with the AD846 operating at gains of 10 or less, inadequate supply decoupling can cause the output settling to degrade from 100 ns to as much as 300 ns, with a 10 V output step applied.

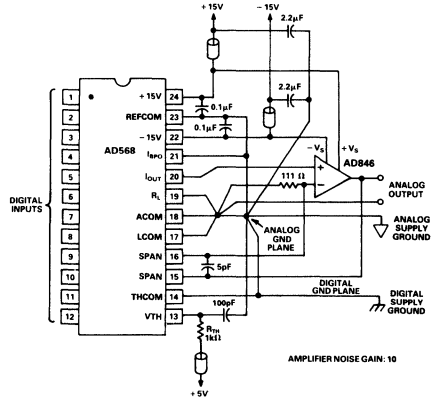


Figure 49. The AD846 Serving as a DAC Buffer

High Speed, Low Power Monolithic Op Amp

AD847

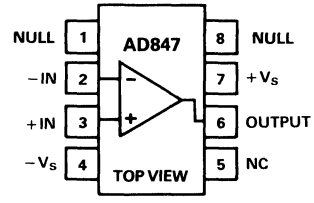
FEATURES
50 MHz Unity Gain Bandwidth
4.8 mA Supply Current
300 V/μs Slew Rate
65 ns Settling Time to 0.1% for a 10 V Step
0.04% Differential Gain
0.19° Differential Phase
Drives Capacitive Loads

DC Performance
5.5 V/mV Open-Loop Gain into a 1 kΩ Load
1 mV max Input Offset Voltage

Performance Specified for ±5 V and ±15 V Operation
Available in Plastic, Hermetic Cerdip and Small Outline Packages; Chips and MIL-STD-883B Processing Available
Available in Tape and Reel in Accordance with EIA-481A Standard
Dual Version Available: AD827

APPLICATIONS
Unity Gain Buffer
Cable Drivers
8- and 10-Bit Data Acquisition Systems
Video and RF Amplification
Signal Generators

CONNECTION DIAGRAM



NC = NO CONNECT

Plastic DIP (N), Small Outline (R) and Cerdip (Q) Packages

PRODUCT DESCRIPTION

The AD847 is a high speed, low power monolithic operational amplifier. The AD847 achieves its combination of fast ac and good dc performance by utilizing Analog Devices' junction isolated complementary bipolar (CB) process. This process enables the AD847 to achieve its high speed while only requiring 4.8 mA of current from the power supplies.

The AD847 is a member of Analog Devices' family of high speed op amps. This family includes, among others, the AD848, which is stable at a gain of five or greater, and the AD849, which offers 725 MHz of gain bandwidth at gains of 25 or greater. For more demanding applications, the AD840, AD841 and AD842 offer even greater precision and greater output current drive.

The AD847 also has good dc performance. When operating with ±5 V supplies, it offers an open loop gain of 3,500 V/V (with a 500 Ω load) and low input offset voltage of 1 mV maximum. Common-mode rejection is a minimum of 80 dB. Output voltage swing is ±3 V even into loads as low as 150 Ω.

APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD847 make it ideal for all types of video instrumentation circuitry, fast DAC and flash ADC buffers, and line drivers.
2. As a buffer, the AD847 offers a full-power bandwidth of 30 MHz (for 2 V p-p with V_S = ±5 V) making it outstanding as an input buffer for flash A/D converters.
3. In order to meet the needs of both video and data acquisition applications, the AD847 is optimized and tested for ±5 V and ±15 V power supply operation.
4. The low power and small outline packaging of the AD847 make it very well suited for high density applications such as multiple pole active filters.
5. The AD847 is internally compensated for unity gain operation and remains stable when driving any capacitive load.
6. Laser wafer trimming reduces the input offset voltage to less than 1 mV maximum on all AD847 grades, thus eliminating the need for external offset nulling in many applications.
7. The AD847 is an enhanced replacement for the LM6161 series and can function as a pin for pin replacement for many high speed amplifiers such as the HA2544, HA2520/2/5 and the EL2020.

AD847—SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Model	Conditions	V_S	AD847J Min	AD847J Typ	AD847J Max	AD847AR Min	AD847AR Typ	AD847AR Max	Units
INPUT OFFSET VOLTAGE[1]		±5 V		0.5	**1**		0.5	**1**	mV
	T_{MIN} to T_{MAX}				3.5			4	mV
Offset Drift				15			15		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	**6.6**		3.3	**6.6**	µA
	T_{MIN} to T_{MAX}				7.2			10	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		50	**300**		50	**300**	nA
	T_{MIN} to T_{MAX}				400			500	nA
Offset Current Drift				0.3			0.3		nA/°C
OPEN-LOOP GAIN	V_O = ±2.5 V	±5 V							
	R_{LOAD} = 500 Ω		**2**	3.5		**2**	3.5		V/mV
	T_{MIN} to T_{MAX}		1			1			V/mV
	R_{LOAD} = 150 Ω			1.6			1.6		V/mV
	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 1 kΩ		**3**	5.5		**3**	5.5		V/mV
	T_{MIN} to T_{MAX}		1.5			1.5			V/mV
DYNAMIC PERFORMANCE									
Unity Gain Bandwidth		±5 V		35			35		MHz
		±15 V		50			50		MHz
Full Power Bandwidth[2]	V_O = 5 V p-p								
	R_L = 500 Ω,	±5 V		12.7			12.7		MHz
	V_O = 20 V p-p,								
	R_L = 1 kΩ	±15 V		4.7			4.7		MHz
Slew Rate[3]	R_{LOAD} = 1kΩ	±5 V		200			200		V/µs
		±15 V	225	300		225	300		V/µs
Settling Time to 0.1%	−2.5 V to +2.5 V	±5 V		65			65		ns
	10 V Step, A_V = −1	±15 V		65			65		ns
to 0.01%	−2.5 V to +2.5 V	±5 V		140			140		ns
	10 V Step, A_V = −1	±15 V		120			120		ns
Phase Margin	C_{LOAD} = 10 pF	±15 V							
	R_{LOAD} = 1 kΩ			50			50		Degree
Differential Gain	f ≈ 4.4 MHz	±15 V		0.04			0.04		%
Differential Phase	f ≈ 4.4 MHz	±15 V		0.19			0.19		Degree
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5 V	**78**	95		**78**	95		dB
	V_{CM} = ±12 V	±15 V	**78**	95		**78**	95		dB
	R_{IN} = 100 Ω (See Figure 20)								
	T_{MIN} to T_{MAX}		75			75			dB
POWER SUPPLY REJECTION	V_S = ±5 V to ±15 V		**75**	86		**75**	86		dB
	T_{MIN} to T_{MAX}		72			72			dB
INPUT VOLTAGE NOISE	f = 10 kHz	±15 V		15			15		nV/√Hz
INPUT CURRENT NOISE	f = 10 kHz	±15 V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5 V		+4.3			+4.3		V
				−3.4			−3.4		V
		±15 V		+14.3			+14.3		V
				−13.4			−13.4		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	**3.0**	3.6		**3.0**	3.6		±V
	R_{LOAD} = 150 Ω	±5 V	**2.5**	3		**2.5**	3		±V
	R_{LOAD} = 1 kΩ	±15 V	**12**			**12**			±V
	R_{LOAD} = 500 Ω	±15 V	**10**			**10**			±V
Short-Circuit Current		±15 V		32			32		mA
INPUT RESISTANCE				300			300		kΩ
INPUT CAPACITANCE				1.5			1.5		pF
OUTPUT RESISTANCE	Open Loop			15			15		Ω
POWER SUPPLY									
Operating Range			**± 4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current		±5 V		4.8	**6.0**		4.8	**6.0**	mA
	T_{MIN} to T_{MAX}				7.3			7.3	mA
		±15 V		5.3	**6.3**		5.3	**6.3**	mA
	T_{MIN} to T_{MAX}				7.6			7.6	mA

NOTES
[1]Input Offset Voltage Specifications are guaranteed after 5 minutes at T_A = +25°C.
[2]Full Power Bandwidth = Slew Rate/2π V_{PEAK}.
[3]Slew Rate is measured on rising edge.

All min and max specifications are guaranteed. Specifications in **boldface** are 100% tested at final electrical test.
Specifications subject to change without notice.

Model	Conditions	V_S	AD847AQ Min	AD847AQ Typ	AD847AQ Max	AD847S Min	AD847S Typ	AD847S Max	Units
INPUT OFFSET VOLTAGE[1]		±5 V		0.5	1		0.5	1	mV
	T_{MIN} to T_{MAX}				4			4	mV
Offset Drift				15			15		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	5		3.3	5	µA
	T_{MIN} to T_{MAX}				7.5			7.5	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		50	300		50	300	nA
	T_{MIN} to T_{MAX}				400			400	nA
Offset Current Drift				0.3			0.3		nA/°C
OPEN LOOP GAIN	V_O = ±2.5 V	±5 V							
	R_{LOAD}= 500 Ω		2	3.5		2	3.5		V/mV
	T_{MIN} to T_{MAX}		1			1			V/mV
	R_{LOAD} = 150 Ω			1.6			1.6		V/mV
	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 1 kΩ		3	5.5		3	5.5		V/mV
	T_{MIN} to T_{MAX}		1.5			1.5			V/mV
DYNAMIC PERFORMANCE									
Unity Gain Bandwidth		±5 V		35			35		MHz
		±15 V		50			50		MHz
Full Power Bandwidth[2]	V_O = 5 V p-p								
	R_L = 500 Ω,	±5 V		12.7			12.7		MHz
	V_O = 20 V p-p,								
	R_L = 1 kΩ	±15 V		4.7			4.7		MHz
Slew Rate[3]	R_{LOAD} = 1kΩ	±5 V		200			200		V/µs
		±15 V	225	300		225	300		V/µs
Settling Time to 0.1%	−2.5 V to +2.5 V	±5 V		65			65		ns
	10 V Step, A_V = −1	±15 V		65			65		ns
to 0.01%	−2.5 V to +2.5 V	±5 V		140			140		ns
	10 V Step, A_V = −1	±15 V		120			120		ns
Phase Margin	C_{LOAD} = 10 pF	±15 V							
	R_{LOAD} = 1 kΩ			50			50		Degree
Differential Gain	f ≈ 4.4 MHz	±15 V		0.04			0.04		%
Differential Phase	f ≈ 4.4 MHz	±15 V		0.19			0.19		Degree
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5 V	80	95		80	95		dB
	V_{CM} = ±12 V	±15 V	80	95		80	95		dB
	R_{IN} = 100 Ω (See Figure 20)								
	T_{MIN} to T_{MAX}		75			75			dB
POWER SUPPLY REJECTION	V_S = ±5 V to ±15 V		75	86		75	86		dB
	T_{MIN} to T_{MAX}		72			72			dB
INPUT VOLTAGE NOISE	f = 10 kHz	±15 V		15			15		nV/√Hz
INPUT CURRENT NOISE	f = 10 kHz	±15 V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5 V		+4.3			+4.3		V
				−3.4			−3.4		V
		±15 V		+14.3			+14.3		V
				−13.4			−13.4		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	3.0	3.6		3.0	3.6		±V
	R_{LOAD} = 150 Ω	±5 V	2.5	3		2.5	3		±V
	R_{LOAD} = 1 kΩ	±15 V	12			12			±V
	R_{LOAD} = 500 Ω	±15 V	10			10			±V
Short-Circuit Current		±15 V		32			32		mA
INPUT RESISTANCE				300			300		kΩ
INPUT CAPACITANCE				1.5			1.5		pF
OUTPUT RESISTANCE	Open Loop			15			15		Ω
POWER SUPPLY									
Operating Range			± 4.5		±18	±4.5		±18	V
Quiescent Current		±5 V		4.8	5.7		4.8	5.7	mA
	T_{MIN} to T_{MAX}				7.0			7.8	mA
		±15 V		5.3	6.3		5.3	6.3	mA
	T_{MIN} to T_{MAX}				7.6			8.4	mA

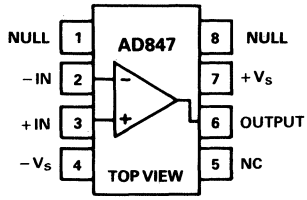
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) . . . . . 1.2 Watts
Small Outline (R) . . . . . 0.8 Watts
Cerdip (Q) . . . . . 1.1 Watts
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Storage Temperature Range Q . . . . . −65°C to +150°C
N, R . . . . . −65°C to +125°C
Junction Temperature . . . . . 175°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Mini-DIP Package: θ_{JA} = 100°C/Watt; θ_{JC} = 33°C/Watt
Cerdip Package: θ_{JA} = 110°C/Watt; θ_{JC} = 30°C/Watt
Small Outline Package: θ_{JA} = 155°C/Watt; θ_{JC} = 33°C/Watt

CONNECTION DIAGRAM

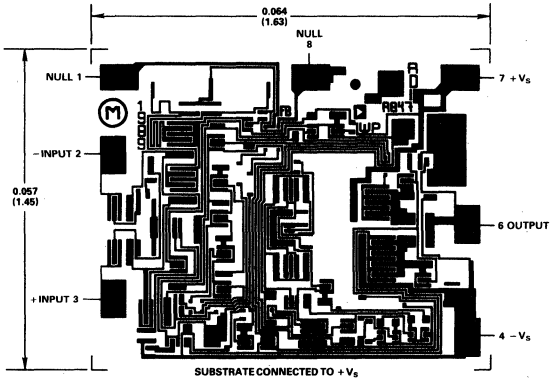
Plastic DIP (N), Small Outline (R) and Cerdip (Q) Packages



NC = NO CONNECT

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



ORDERING GUIDE

Model[1]	Gain Bandwidth MHz	Minimum Stable Gain	Maximum Offset Voltage mV	Temperature Range – °C	Package Description	Package Option[2]
AD847JN	50	1	1	0 to +70	Plastic	N-8
AD847JR	50	1	1	0 to +70	SOIC	R-8
AD847AQ	50	1	1	−40 to +85	Cerdip	Q-8
AD847AR[3]	50	1	1	−40 to +85	SOIC	R-8
AD847SQ	50	1	1	−55 to +125	Cerdip	Q-8
AD847SQ/883B	50	1	1	−55 to +125	Cerdip	Q-8
AD848J/A/S	175	5	1	See AD848 Data Sheet		
AD849J/A/S	725	25	1	See AD849 Data Sheet		

NOTES
[1]AD847 also available in J and S grade chips, and AD847JR is available in tape and reel.
[2]N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.
[3]Contact sales office for detailed information.

Typical Characteristics (@ +25°C and V_S = ±25°C and V_S = ±15 V, unless otherwise noted)

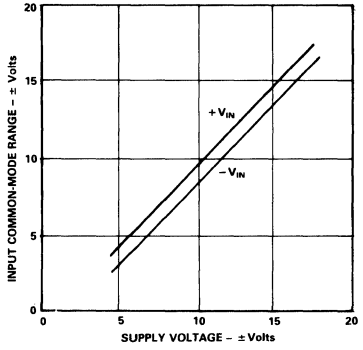


Figure 1. Input Common-Mode Range vs. Supply Voltage

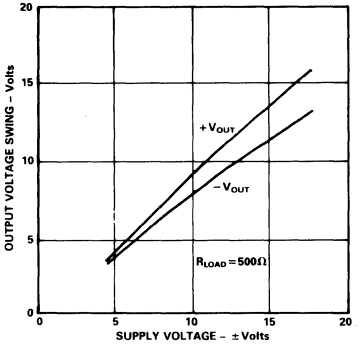


Figure 2. Output Voltage Swing vs. Supply Voltage

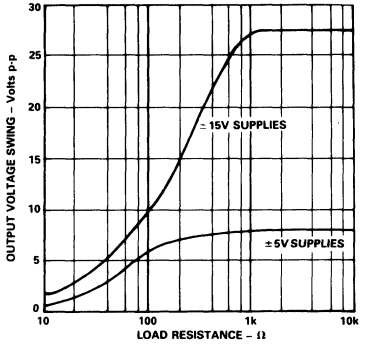


Figure 3. Output Voltage Swing vs. Load Resistance

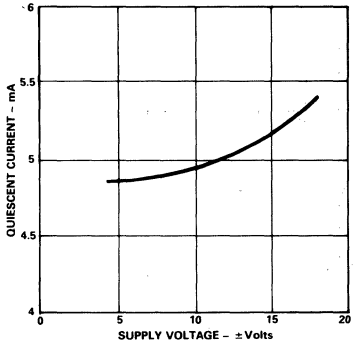


Figure 4. Quiescent Current vs. Supply Voltage

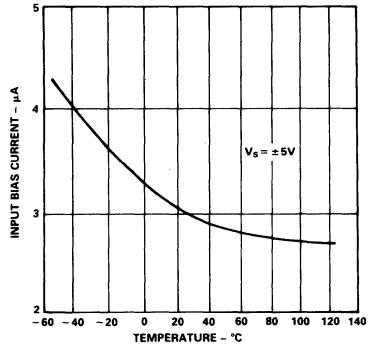


Figure 5. Input Bias Current vs. Temperature

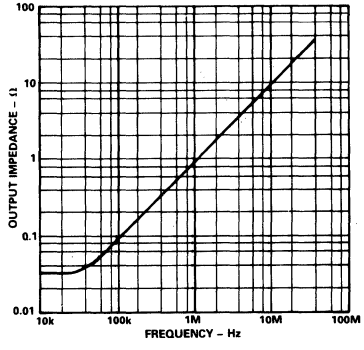


Figure 6. Output Impedance vs. Frequency

AD847 — Typical Characteristics (@ +25°C and V_S = ±25°C and V_S = ±15 V, unless otherwise noted)

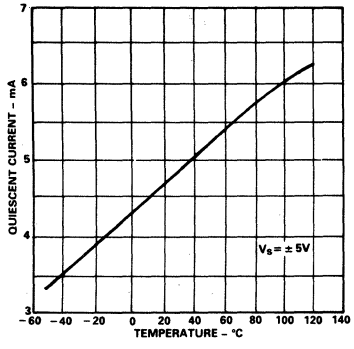


Figure 7. Quiescent Current vs. Temperature

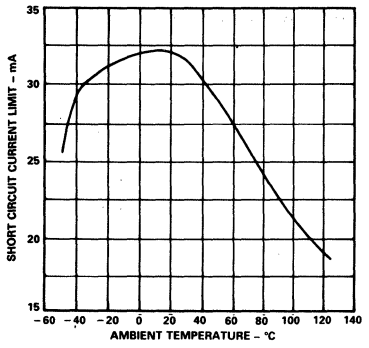


Figure 8. Short-Circuit Current Limit vs. Temperature

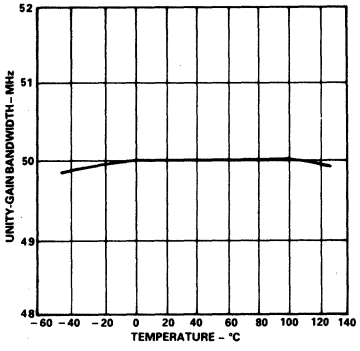


Figure 9. Gain Bandwidth Product vs. Temperature

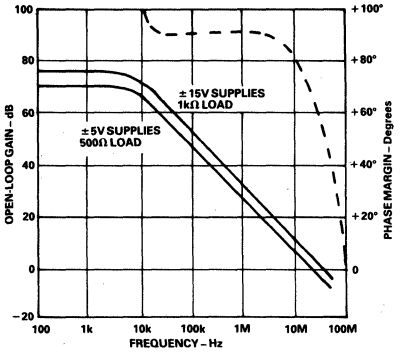


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

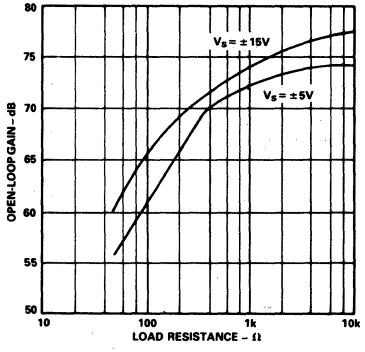


Figure 11. Open-Loop Gain vs. Load Resistance

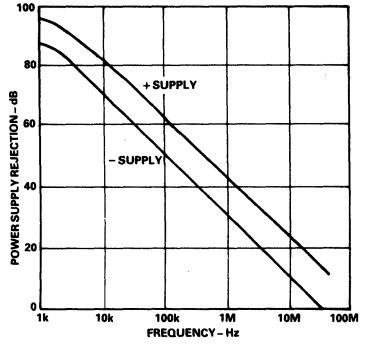


Figure 12. Power Supply Rejection vs. Frequency

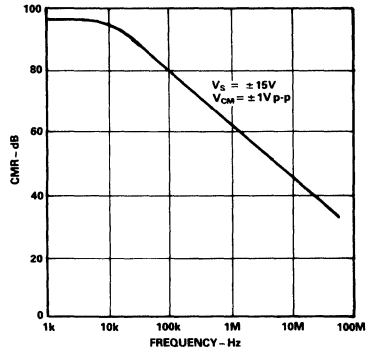


Figure 13. Common Mode Rejection vs. Frequency

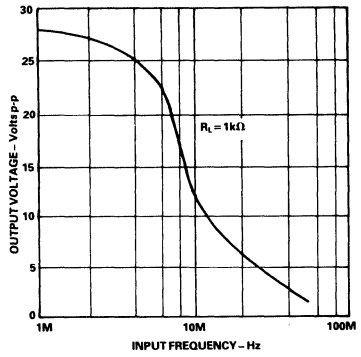


Figure 14. Large Signal Frequency Response

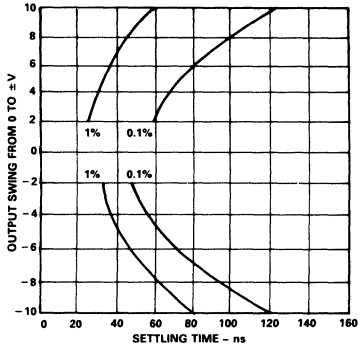


Figure 15. Output Swing and Error vs. Settling Time

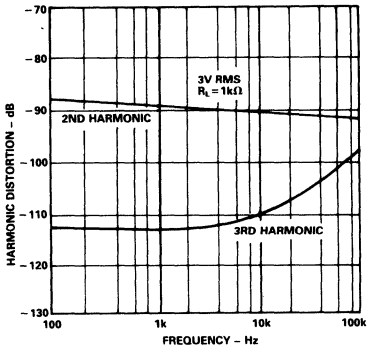


Figure 16. Harmonic Distortion vs. Frequency

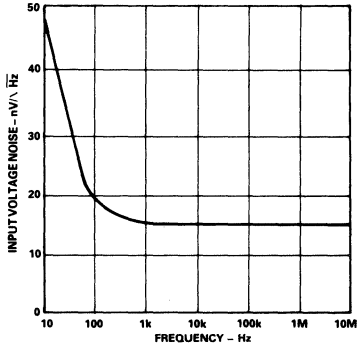


Figure 17. Input Voltage Noise Spectral Density

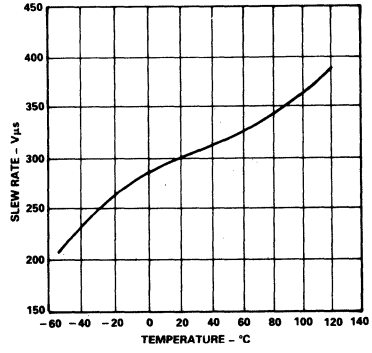


Figure 18. Slew Rate vs. Temperature

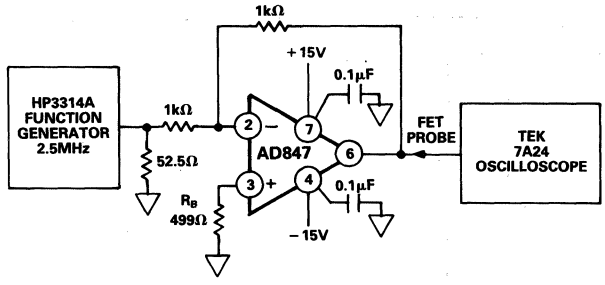


Figure 19. Inverting Amplifier Configuration

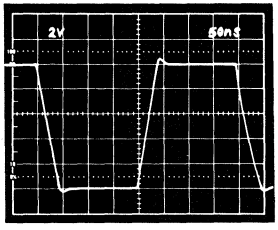


Figure 19a. Inverter Large Signal Pulse Response

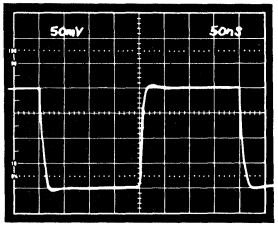


Figure 19b. Inverter Small Signal Pulse Response

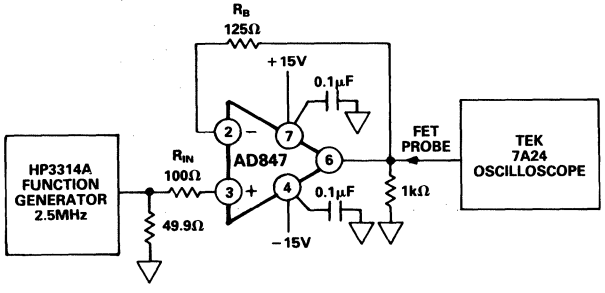


Figure 20. Noninverting Amplifier Configuration

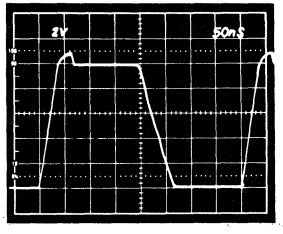


Figure 20a. Noninverting Large Signal Pulse Response

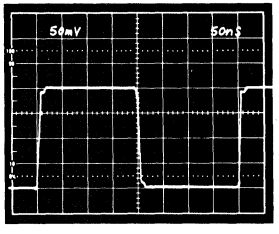


Figure 20b. Noninverting Small Signal Pulse Response

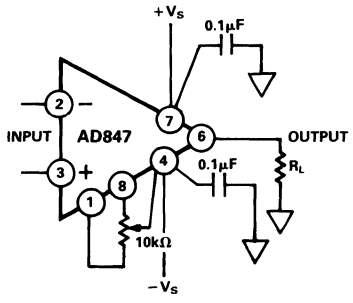


Figure 21. Offset Nulling

OFFSET NULLING

The input offset voltage of the AD847 is very low for a high speed op amp, but if additional nulling is required, the circuit shown in Figure 21 can be used.

INPUT CONSIDERATIONS

An input resistor (R_{IN} in Figure 20) is required in circuits where the input to the AD847 will be subjected to transient or continuous overload voltages exceeding the ±6 V maximum differential limit. This resistor provides protection for the input transistors by limiting the maximum current that can be forced into their bases.

For high performance circuits it is recommended that a resistor (R_B in Figures 19 and 20) be used to reduce bias current errors by matching the impedance at each input. The offset voltage error caused by the offset current is more than an order of magnitude less.

THEORY OF OPERATION

The AD847 is fabricated on Analog Devices' proprietary complementary bipolar (CB) process which enables the construction of pnp and npn transistors with similar f_Ts in the 600 MHz to 800 MHz region. The AD847 circuit (Figure 22) includes an npn input stage followed by fast pnps in the folded cascade intermediate gain stage. The CB pnps are also used in the current amplifying output stage. The internal compensation capacitance that makes the AD847 unity gain stable is provided by the junction capacitances of transistors in the gain stage.

The capacitor, C_F, in the output stage mitigates the effect of capacitive loads. At low frequencies and with low capacitive loads, the gain from the compensation node to the output is very close to unity. In this case C_F is bootstrapped and does not contribute to the compensation capacitance of the part. As the capacitive load is increased, a pole is formed with the output impedance of the output stage. This reduces the gain, and therefore, C_F is incompletely bootstrapped. Some fraction of C_F contributes to the compensation capacitance, and the unity gain bandwidth falls. As the load capacitance is increased, the bandwidth continues to fall, and the amplifier remains stable.

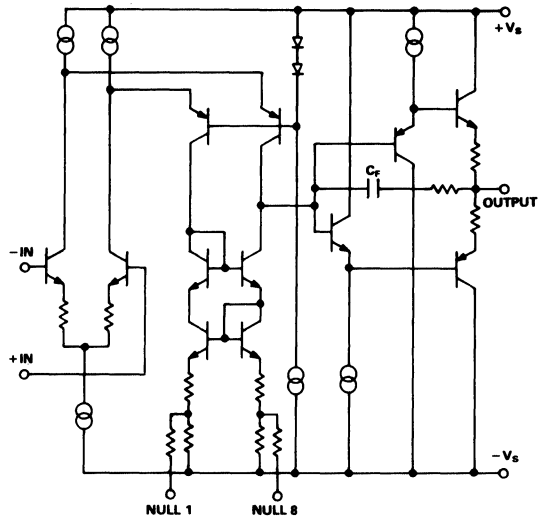


Figure 22. AD847 Simplified Schematic

GROUNDING AND BYPASSING

In designing practical circuits with the AD847, the user must remember that whenever high frequencies are involved, some special precautions are in order. Circuits must be built with short interconnect leads. A large ground plane should be used whenever possible to provide a low resistance, low inductance circuit path, as well as minimizing the effects of high frequency coupling. Sockets should be avoided because the increased interlead capacitance can degrade bandwidth.

Feedback resistors should be of low enough value to assure that the time constant formed with the capacitances at the amplifier summing junction will not limit the amplifier performance. Resistor values of less than 5 kΩ are recommended. If a larger resistor must be used, a small (<10 pF) feedback capacitor in parallel with the feedback resistor, R_F, may be used to compensate for the input capacitances and optimize the dynamic performance of the amplifier.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. 0.1 μF ceramic disc capacitors are recommended.

VIDEO LINE DRIVER

The AD847 functions very well as a low cost, high speed line driver for either terminated or unterminated cables. Figure 23 shows the AD847 driving a doubly terminated cable in a follower configuration.

The termination resistor, R_T, (when equal to the cable's characteristic impedance) minimizes reflections from the far end of the cable. While operating from ±5 V supplies, the AD847 maintains a typical slew rate of 200 V/μs, which means it can drive a ±1 V, 30 MHz signal into a terminated cable.

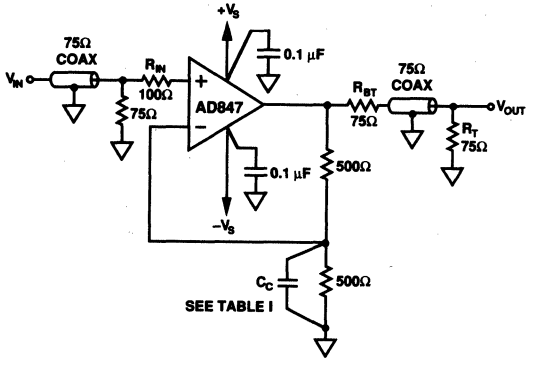


Figure 23. Video Line Driver

Table I. Video Line Driver Performance Chart

V_{IN}*	V_{SUPPLY}	C_C	−3 dB B_W	Overshoot
0 dB or ±500 mV Step	±15	20 pF	23 MHz	4%
0 dB or ±500 mV Step	±15	15 pF	21 MHz	0%
0 dB or ±500 mV Step	±15	0 pF	13 MHz	0%
0 dB or ±500 mV Step	±5	20 pF	18 MHz	2%
0 dB or ±500 mV Step	±5	15 pF	16 MHz	0%
0 dB or ±500 mV Step	±5	0 pF	11 MHz	0%

NOTE
*−3 dB bandwidth numbers are for the 0 dBm signal input. Overshoot numbers are the percent overshoot of the 1 volt step input.

A back-termination resistor (R_{BT}, also equal to the characteristic impedance of the cable) may be placed between the AD847 output and the cable input, in order to damp any reflected signals caused by a mismatch between R_T and the cable's characteristic impedance. This will result in a flatter frequency response, although this requires that the op amp supply ±2 V to the output in order to achieve a −1 V swing at resistor R_T.

Figure 24 shows the AD847 driving 100 pF and 1000 pF loads.

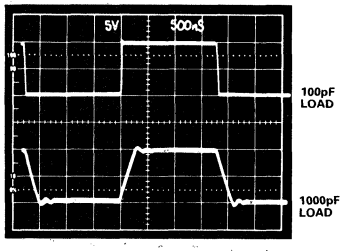


Figure 24. AD847 Driving Capacitive Loads

FLASH ADC INPUT BUFFER

The 35 MHz unity gain bandwidth of the AD847 when operated with ±5 V supplies makes it an excellent choice for buffering the input of high speed flash A/D converters, such as the AD9048.

Figure 25 shows the AD847 as a unity inverter for the input to the AD9048.

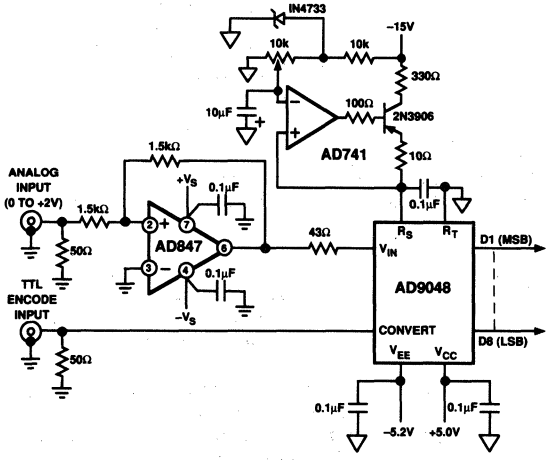


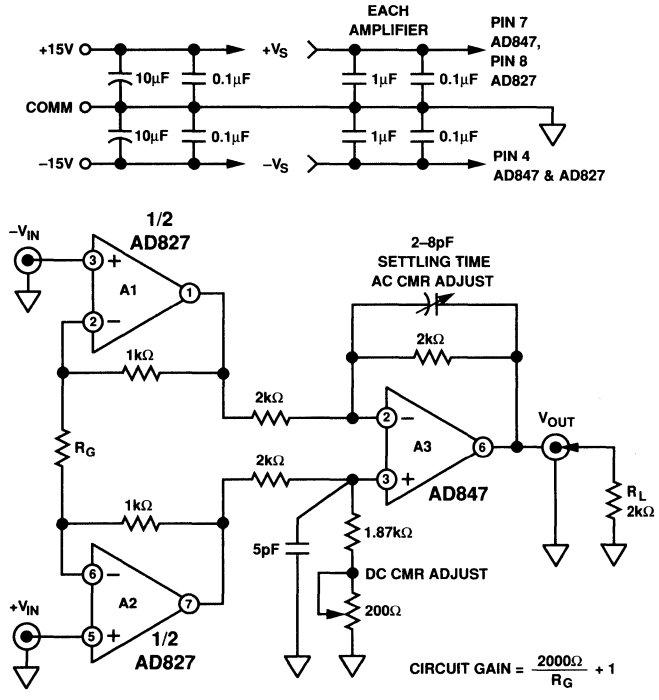
Figure 25. Flash ADC Input Buffer

A High Speed, Three Op-Amp In-Amp

The circuit of Figure 26 lends itself well to CCD imaging and other video speed applications. It uses two high speed CB process op-amps: Amplifier A3, the output amplifier, is an AD847. The input amplifier (A1 and A2) is an AD827, which is a dual version of the AD847. This circuit has the optional flexibility of both dc and ac trims for common-mode rejection, plus the ability to adjust for minimum settling time.

Input Frequency	CMRR
100 Hz	88.3 dB
1 kHz	87.4 dB
10 kHz	86.2 dB
100 kHz	67.4 dB
1 MHz	47.1 dB
10 MHz	26.4 dB

2



Bandwidth, Settling Time and Total Harmonic Distortion vs. Gain

Gain	R_G	C_{ADJ} (pF)	Small Signal Bandwidth	Settling Time to 0.1%	THD+Noise Below Input Level @ 10 kHz
1	Open	2–8	16.1 MHz	200 ns	82 dB
2	2 kΩ	2–8	14.7 MHz	200 ns	82 dB
10	226 Ω	2–8	4.5 MHz	370 ns	81 dB
100	200 Ω	2–8	660 kHz	2.5 μs	71 dB

Figure 26. A High Speed In-Amp Circuit for Data Acquistion

HIGH SPEED DAC BUFFER

The wide bandwidth and fast settling time of the AD847 makes it a very good output buffer for high speed current-output D/A converters like the ADDAC-08. Figure 28 shows the ADDAC-08 with the AD847 as the current to voltage converter. In this unipolar configuration the output swing ranges from 0.00 V to +9.96 V.

Figure 27 shows the full scale settling time of this circuit when the digital codes are changed from all 1s to all 0s. For the +9.96 V to 0.00 V output change shown 1 LSB = 40 mV the overall settling time of the circuit is 140 ns.

The variable feedback capacitor, C_F, is used to optimize the settling time of the circuit by compensating for the additional pole created by R_F and the stray capacitance at the inverting input pin. A −10.0 V to +9.92 V bipolar output is achievable by connecting a 10 kΩ resistor between the AD587 output and the AD847 input and replacing R_F with a 10 kΩ resistor.

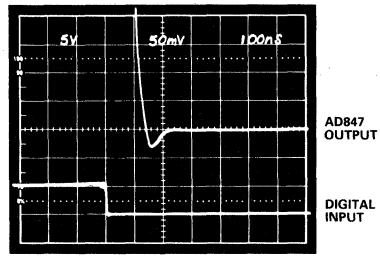


Figure 27. Settling Time for AD DAC-08 and AD847 Combination

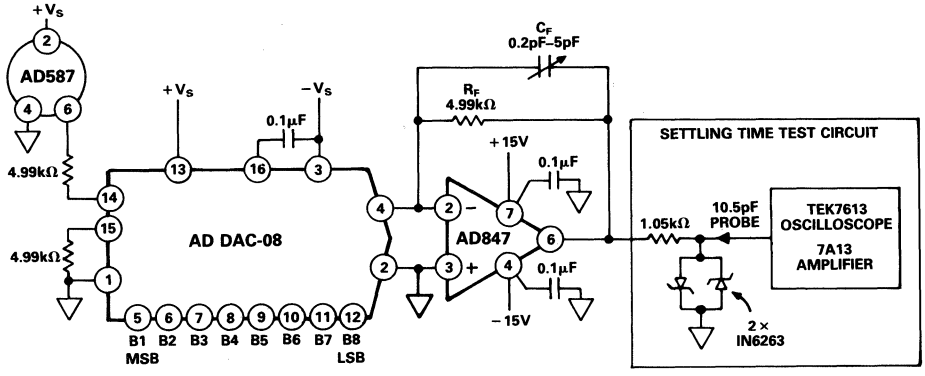


Figure 28. High Speed DAC Buffer

High Speed, Low Power Monolithic Op Amps

AD848/AD849

FEATURES
725MHz Gain Bandwidth – AD849
175MHz Gain Bandwidth – AD848
4.8mA Supply Current
300V/μs Slew Rate
80ns Settling Time to 0.1% for a 10V Step – AD849
Differential Gain: AD848 = 0.07%, AD849 = 0.08%
Differential Phase: AD848 = 0.08°, AD849 = 0.04°
Drives Capacitive Loads

DC PERFORMANCE
3nV/$\sqrt{Hz}$ Input Voltage Noise – AD849
85V/mV Open Loop Gain into a 1kΩ Load – AD849
1mV max Input Offset Voltage
Performance Specified for ±5V and ±15V Operation
Available in Plastic, Hermetic Cerdip and Small Outline Packages. Chips and MIL-STD-883B Parts Available. Tape and Reel Also Available

APPLICATIONS
Cable Drivers
8- and 10-Bit Data Acquisition Systems
Video and R_F Amplification
Signal Generators

PRODUCT DESCRIPTION

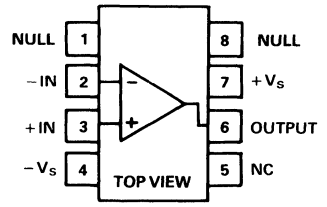
The AD848 and AD849 are high speed, low power monolithic operational amplifiers. The AD848 is internally compensated so that it is stable for closed loop gains of 5 or greater. The AD849 is fully decompensated and is stable at gains greater than 24. The AD848 and AD849 achieve their combination of fast ac and good dc performance by utilizing Analog Devices' junction isolated complementary bipolar (CB) process. This process enables these op amps to achieve their high speed while only requiring 4.8mA of current from the power supplies.

The AD848 and AD849 are members of Analog Devices' family of high speed op amps. This family includes, among others, the AD847 which is unity gain stable, with a gain bandwidth of 50MHz. For more demanding applications, the AD840, AD841 and AD842 offer even greater precision and greater output current drive.

The AD848 and AD849 have good dc performance. When operating with ±5V supplies, they offer open loop gains of 13V/mV (AD848 with a 500Ω load) and low input offset voltage of 1mV maximum. Common-mode rejection is a minimum of 92dB. Output voltage swing is ±3V even into loads as low as 150Ω.

CONNECTION DIAGRAM
AD848 and AD849

Plastic (N), Small Outline (R) and Cerdip (Q) Packages



NC = NO CONNECT

APPLICATIONS HIGHLIGHTS

1. The high slew rate and fast settling time of the AD848 and AD849 make them ideal for video instrumentation circuitry, low noise preamps and line drivers.
2. In order to meet the needs of both video and data acquisition applications, the AD848 and AD849 are optimized and tested for ±5V and ±15V power supply operation.
3. Both amplifiers offer full power bandwidth greater than 20MHz (for 2V p-p with ±5V supplies).
4. The AD848 and AD849 remain stable when driving any capacitive load.
5. Laser wafer trimming reduces the input offset voltage to 1mV maximum on all grades, thus eliminating the need for external offset nulling in many applications.
6. The AD848 is an enhanced replacement for the LM6164 series and can function as a pin-for-pin replacement for many high speed amplifiers such as the HA2520/2/5 and EL2020 in applications where the gain is 5 or greater.

AD848/AD849—SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Model	Conditions	V_S	AD848J Min	AD848J Typ	AD848J Max	AD848A/S Min	AD848A/S Typ	AD848A/S Max	Units
INPUT OFFSET VOLTAGE[1]		±5V		0.2	**1**		0.2	**1**	mV
		±15V		0.5	**2.3**		0.5	**2.3**	mV
	T_{min} to T_{max}	±5V			1.5			**2**	mV
		±15V			3.0			**3.5**	mV
Offset Drift		±5V, ±15V		7			7		µV/°C
INPUT BIAS CURRENT		±5V, ±15V		3.3	**6.6**		3.3	**6.6/5**	µA
	T_{min} to T_{max}	±5V, ±15V			7.2			**7.5**	µA
INPUT OFFSET CURRENT		±5V, ±15V		50	**300**		50	**300**	nA
	T_{min} to T_{max}	±5V, ±15V			400			**400**	nA
Offset Current Drift		±5V, ±15V		0.3			0.3		nA/°C
OPEN LOOP GAIN	V_O = ±2.5V	±5V							
	R_{LOAD} = 500Ω		**9**	13		**9**	13		V/mV
	T_{min} to T_{max}		7			**7/5**			V/mV
	R_{LOAD} = 150Ω			8			8		V/mV
	V_{OUT} = ±10V	±15V							
	R_{LOAD} = 1kΩ		**12**	20		**12**	20		V/mV
	T_{min} to T_{max}		8			**8/6**			V/mV
DYNAMIC PERFORMANCE									
Gain Bandwidth	A_{VCL} ≥ 5	±5V		125			125		MHz
		±15V		175			175		MHz
Full Power Bandwidth[2]	V_O = 2V p-p,								
	R_L = 500Ω	±5V		24			24		MHz
	V_O = 20V p-p,								
	R_L = 1kΩ	±15V		4.7			4.7		MHz
Slew Rate		±5V		200			200		V/µs
	R_{LOAD} = 1kΩ	±15V	225	300		225	300		V/µs
Settling Time to 0.1%	−2.5V to +2.5V	±5V		65			65		ns
	10V Step, A_V = −4	±15V		100			100		ns
Phase Margin	C_{LOAD} = 10pF	±15V							
	R_{LOAD} = 1kΩ			60			60		Degrees
DIFFERENTIAL GAIN	f = 4.4MHz	±15V		0.07			0.07		%
DIFFERENTIAL PHASE	f = 4.4MHz	±15V		0.08			0.08		Degree
COMMON-MODE REJECTION	V_{CM} = ±2.5V	±5V	**92**	105		**92**	105		dB
	V_{CM} = ±12V	±15V	**92**	105		**92**	105		dB
	T_{min} to T_{max}		88			**88**			dB
POWER SUPPLY REJECTION	V_S = ±4.5V to ±18V		**85**	98		**85**	98		dB
	T_{min} to T_{max}		80			**80**			dB
INPUT VOLTAGE NOISE	f = 10kHz	±15V		5			5		nV/√Hz
INPUT CURRENT NOISE	f = 10kHz	±15V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5V		+4.3			+4.3		V
				−3.4			−3.4		V
		±15V		+14.3			+14.3		V
				−13.4			−13.4		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500Ω	±5V	**3.0**	3.6		**3.0**	3.6		±V
	R_{LOAD} = 150Ω	±5V	**2.5**	3		**2.5**	3		±V
	R_{LOAD} = 50Ω	±5V		1.4			1.4		±V
	R_{LOAD} = 1kΩ	±15V	**12**			**12**			±V
	R_{LOAD} = 500Ω	±15V	**10**			**10**			±V
SHORT CIRCUIT CURRENT		±15V		32			32		mA
INPUT RESISTANCE				70			70		kΩ
INPUT CAPACITANCE				1.5			1.5		pF
OUTPUT RESISTANCE	Open Loop			15			15		Ω
POWER SUPPLY									
Operating Range			**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current		±5V		4.8	**6.0**		4.8	**6.0**	mA
	T_{min} to T_{max}				7.4			**7.4/8.3**	mA
		±15V		5.1	**6.8**		5.1	**6.8**	mA
	T_{min} to T_{max}				8.0			**8.0/9.0**	mA

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.

[2]Full power bandwidth = slew rate/2π V_{PEAK}. Refer to Figure 1.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. All others are guaranteed but not necessarily tested.

Specifications subject to change without notice.

Model	Conditions	V_S	AD849J Min	AD849J Typ	AD849J Max	AD849A/S Min	AD849A/S Typ	AD849A/S Max	Units
INPUT OFFSET VOLTAGE[1]		±5V		0.3	**1**		0.1	**0.75**	mV
		±15V		0.3	**1**		0.1	**0.75**	mV
	T_{min} to T_{max}	±5V			1.3			**1.0**	mV
		±15V			1.3			**1.0**	mV
Offset Drift		±5V, ±15V		2			2		µV/°C
INPUT BIAS CURRENT		±5V, ±15V		3.3	**6.6**		3.3	**6.6/5**	µA
	T_{min} to T_{max}	±5V, ±15V			7.2			**7.5**	µA
INPUT OFFSET CURRENT		±5V, ±15V		50	**300**		50	**300**	nA
	T_{min} to T_{max}	±5V, ±15V			400			**400**	nA
Offset Current Drift		±5V, ±15V		0.3			0.3		nA/°C
OPEN LOOP GAIN	V_O = ±2.5V	±5V							
	R_{LOAD} = 500Ω		**30**	50		**30**	50		V/mV
	T_{min} to T_{max}		20			**20/15**			V/mV
	R_{LOAD} = 150Ω			32			32		V/mV
	V_{OUT} = ±10V	±15V							
	R_{LOAD} = 1kΩ		**45**	85		**45**	85		V/mV
	T_{min} to T_{max}		30			**30/25**			V/mV
DYNAMIC PERFORMANCE									
Gain Bandwidth	A_{VCL} ≥ 25	±5V		520			520		MHz
		±15V		725			725		MHz
Full Power Bandwidth[2]	V_O = 2V p-p,								
	R_L = 500Ω	±5V		20			20		MHz
	V_O = 20V p-p,								
	R_L = 1kΩ	±15V		4.7			4.7		MHz
Slew Rate		±5V		200			200		V/µs
	R_{LOAD} = 1kΩ	±15V	225	300		225	300		V/µs
Settling Time to 0.1%	−2.5V to +2.5V	±5V		65			65		ns
	10V Step, A_V = −24	±15V		80			80		ns
Phase Margin	C_{LOAD} = 10pF	±15V							
	R_{LOAD} = 1kΩ			60			60		Degrees
DIFFERENTIAL GAIN	f = 4.4MHz	±15V		0.08			0.08		%
DIFFERENTIAL PHASE	f = 4.4MHz	±15V		0.04			0.04		Degree
COMMON-MODE REJECTION	V_{CM} = ±2.5V	±5V	**100**	115		**100**	115		dB
	V_{CM} = ±12V	±15V	**100**	115		**100**	115		dB
	T_{min} to T_{max}		**96**			**96**			dB
POWER SUPPLY REJECTION	V_S = ±4.5V to ±18V		**98**	120		**98**	120		dB
	T_{min} to T_{max}		94			**94**			dB
INPUT VOLTAGE NOISE	f = 10kHz	±15V		3			3		nV/√Hz
INPUT CURRENT NOISE	f = 10kHz	±15V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5V		+4.3			+4.3		V
				−3.4			−3.4		V
		±15V		+14.3			+14.3		V
				−13.4			−13.4		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500Ω	±5V	**3.0**	3.6		**3.0**	3.6		±V
	R_{LOAD} = 150Ω	±5V	**2.5**	3		**2.5**	3		±V
	R_{LOAD} = 50Ω	±5V		1.4			1.4		±V
	R_{LOAD} = 1kΩ	±15V	**12**			**12**			±V
	R_{LOAD} = 500Ω	±15V	**10**			**10**			±V
SHORT CIRCUIT CURRENT		±15V		32			32		mA
INPUT RESISTANCE				25			25		kΩ
INPUT CAPACITANCE				1.5			1.5		pF
OUTPUT RESISTANCE	Open Loop			15			15		Ω
POWER SUPPLY									
Operating Range			**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current		±5V		4.8	**6.0**		4.8	**6.0**	mA
	T_{min} to T_{max}				7.4			**7.4/8.3**	mA
		±15V		5.1	**6.8**		5.1	**6.8**	mA
	T_{min} to T_{max}				8.0			**8.0/9.0**	mA

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.

[2]Full power bandwidth = slew rate/2π V_{PEAK}. Refer to Figure 2.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. All others are guaranteed but not necessarily tested.

Specifications subject to change without notice.

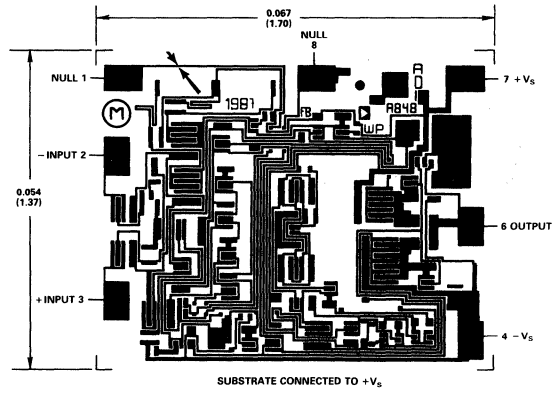
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18V
Internal Power Dissipation[2]
Plastic (N) . . . . . 1.1 Watts
Small Outline (R) . . . . . 0.9 Watts
Cerdip (Q) . . . . . 1.1 Watts
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . +6V
Storage Temperature Range Q . . . . . −65°C to +150°C
N, R . . . . . −65°C to +125°C
Junction Temperature . . . . . +175°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Mini-DIP Package: $\theta_{JA} = 110°C$ Watt.
Cerdip Package: $\theta_{JA} = 110°C$ Watt.
Small Outline Package: $\theta_{JA} = 155°C$ Watt.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions. (AD848 and AD849 are identical except for the part number in the upper right.)
Dimensions shown in inches and (mm).



ORDERING GUIDE

Model	Gain Bandwidth MHz	Min Stable Gain	Max Offset Voltage mV	Temperature Range – °C	Package Option[1, 2]
AD848JN	175	5	1	0 to +70	N-8
AD848JR	175	5	1	0 to +70	R-8
AD848AQ	175	5	1	−40 to +85	Q-8
AD848SQ	175	5	1	−55 to +125	Q-8
AD848SQ/883B	175	5	1	−55 to +125	Q-8
AD849JN	725	25	1	0 to +70	N-8
AD849JR	725	25	1	0 to +70	R-8
AD849AQ	725	25	0.75	−40 to +85	Q-8
AD849SQ	725	25	0.75	−55 to +125	Q-8
AD849SQ/883B	725	25	0.75	−55 to +125	Q-8
AD847J/A/S	50	1	1	See AD847 Data Sheet	

NOTES
[1]Plastic SOIC (R) available in tape and reel. AD848 available in S grade chips. AD849 available in J and S grade chips.
[2]N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

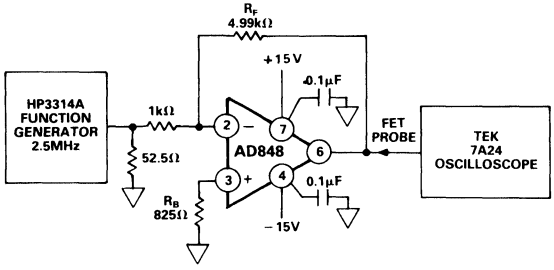


Figure 1. AD848 Inverting Amplifier Configuration

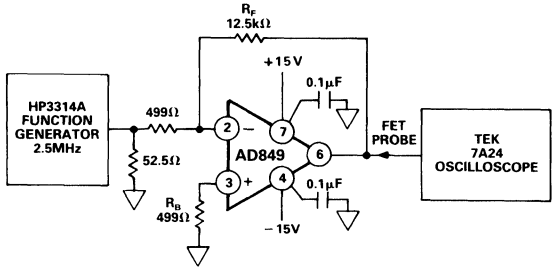


Figure 2. AD849 Inverting Amplifier Configuration

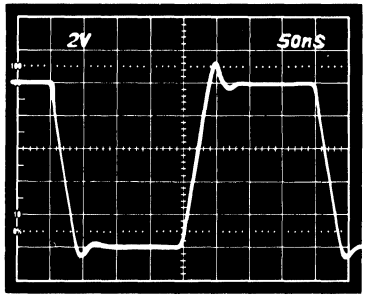


Figure 1a. AD848 Large Signal Pulse Response

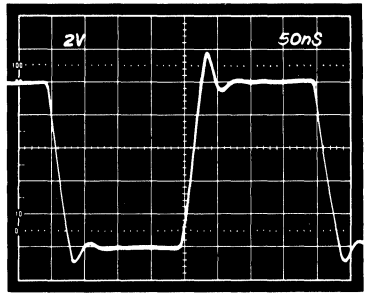


Figure 2a. AD849 Large Signal Pulse Response

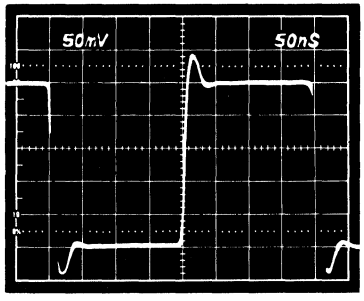


Figure 1b. AD848 Small Signal Pulse Response

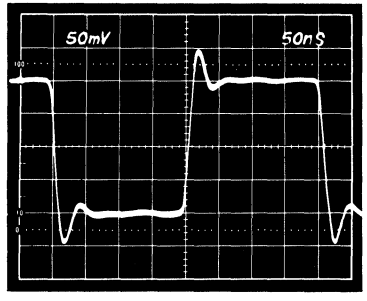


Figure 2b. AD849 Small Signal Pulse Response

OFFSET NULLING

The input voltage of the AD848 and AD849 are very low for high speed op amps, but if additional nulling is required, the circuit shown in Figure 3 can be used.

For high performance circuits it is recommended that a resistor (R_B in Figures 1 and 2) be used to reduce bias current errors by matching the impedance at each input. The offset voltage error caused by the input currents is decreased by more than an order of magnitude.

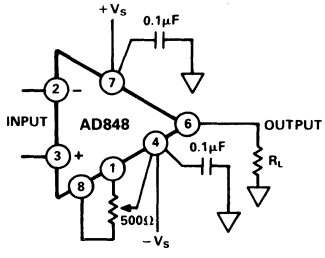


Figure 3. Offset Nulling

AD848/AD849—Typical Characteristics (@ +25°C and $V_S = \pm 15V$, unless otherwise noted)

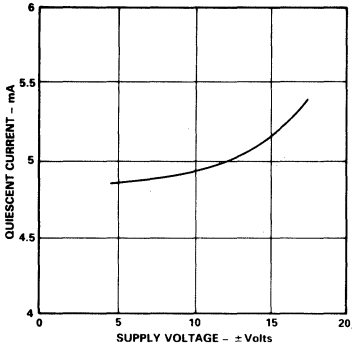


Figure 4. Quiescent Current vs. Supply Voltage (AD848 and AD849)

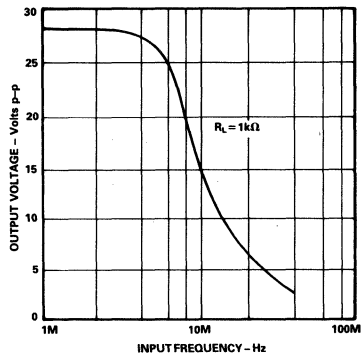


Figure 5. Large Signal Frequency Response (AD848 and AD849)

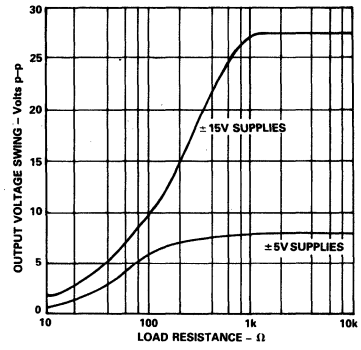


Figure 6. Output Voltage Swing vs. Load Resistance (AD848 and AD849)

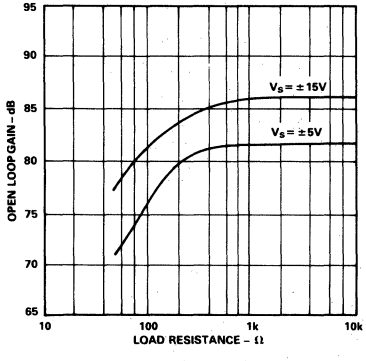


Figure 7. Open Loop Gain vs. Load Resistance (AD848)

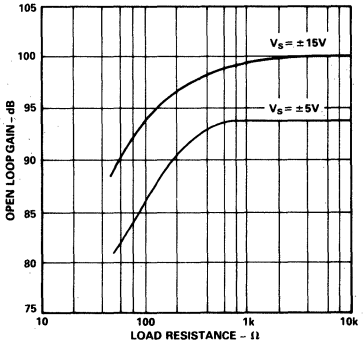


Figure 8. Open Loop Gain vs. Load Resistance (AD849)

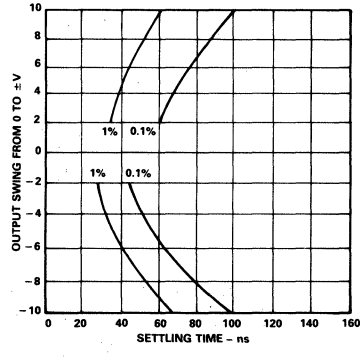


Figure 9. Output Swing and Error vs. Settling Time (AD848)

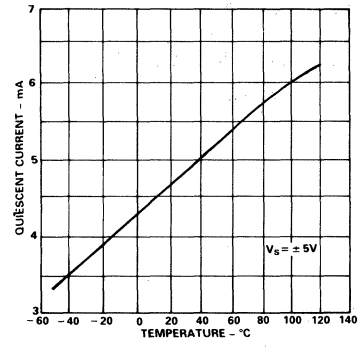


Figure 10. Quiescent Current vs. Temperature (AD848 and AD849)

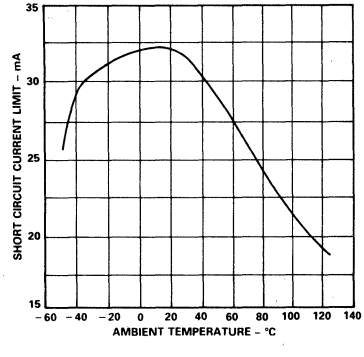


Figure 11. Short Circuit Current Limit vs. Temperature (AD848 and AD849)

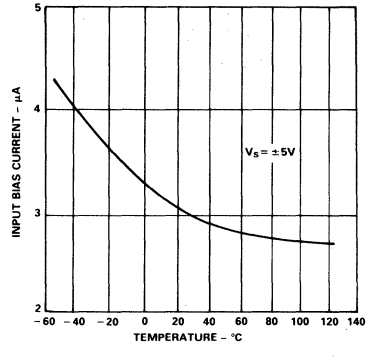


Figure 12. Input Bias Current vs. Temperature (AD848 and AD849)

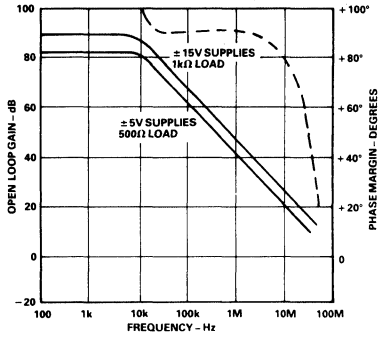


Figure 13. Open Loop Gain and Phase Margin vs. Frequency (AD848)

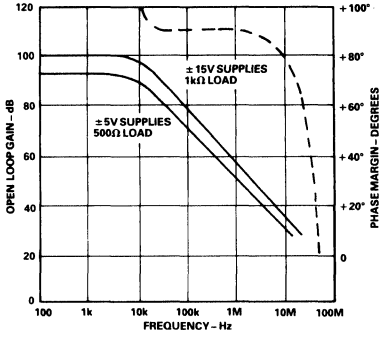


Figure 14. Open Loop Gain and Phase Margin vs. Frequency (AD849)

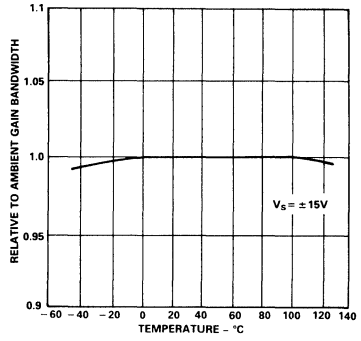


Figure 15. Normalized Gain Bandwidth Product vs. Temperature (AD848 and AD849)

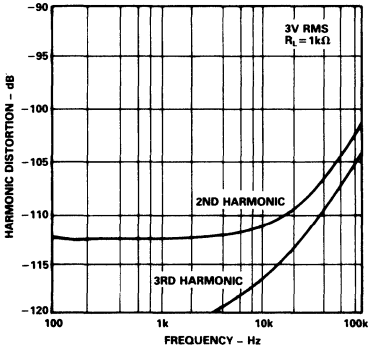


Figure 16. Harmonic Distortion vs. Frequency (AD848)

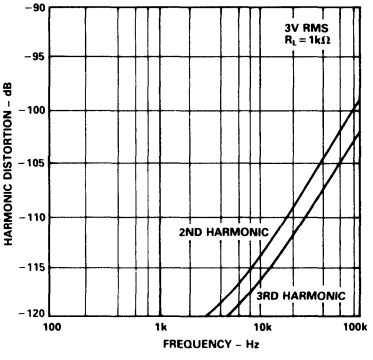


Figure 17. Harmonic Distortion vs. Frequency (AD849)

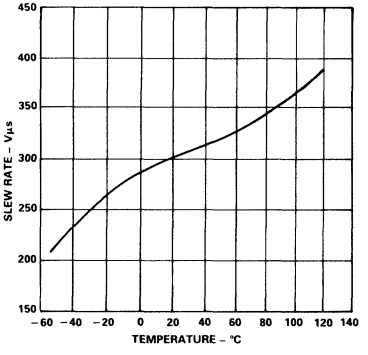


Figure 18. Slew Rate vs. Temperature (AD848 and AD849)

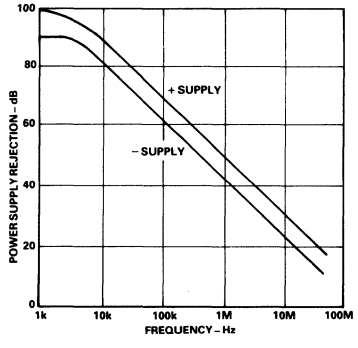


Figure 19. Power Supply Rejection vs. Frequency (AD848)

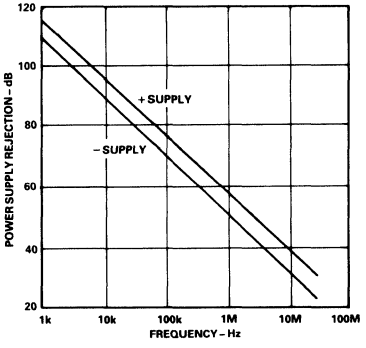


Figure 20. Power Supply Rejection vs. Frequency (AD849)

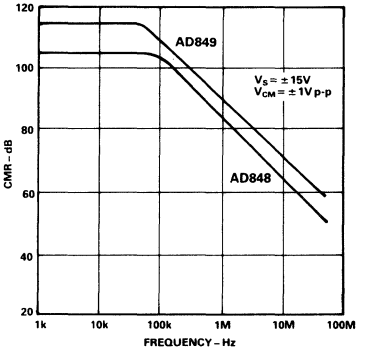


Figure 21. Common-Mode Rejection vs. Frequency

GROUNDING AND BYPASSING

In designing practical circuits with the AD848 or AD849, the user must remember that whenever high frequencies are involved, some special precautions are in order. Circuits must be built with short interconnect leads. A large ground plane should be used whenever possible to provide a low resistance, low inductance circuit path, as well as minimizing the effects of high frequency coupling. Sockets should be avoided because the increased interlead capacitance can degrade bandwidth.

Feedback resistors should be of low enough value to assure that the time constant formed with the capacitances at the amplifier summing junction will not limit the amplifier performance. Resistor values of less than 5kΩ are recommended. If a larger resistor must be used, a small (<10pF) feedback capacitor in parallel with the feedback resistor, R_F, may be used to compensate for the input capacitances and optimize the dynamic performance of the amplifier.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. 0.1μF ceramic disc capacitors are recommended.

VIDEO LINE DRIVER

The AD848 functions very well as a low cost, high speed line driver of either terminated or unterminated cables. Figure 22 shows the AD848 driving a doubly terminated cable.

The termination resistor, R_T, (when equal to the characteristic impedance of the cable) minimizes reflections from the far end of the cable. While operating off ±5V supplies, the AD848 maintains a typical slew rate of 200V/μs, which means it can drive a ±1V, 24MHz signal on the terminated cable.

A back-termination resistor (R_{BT}, also equal to the characteristic impedance of the cable) may be placed between the AD848 output and the cable in order to damp any reflected signals caused by a mismatch between R_T and the cable's characteristic impedance. This will result in a "cleaner" signal, although it requires that the op amp supply ±2V to the output in order to achieve a ±1V swing at the line.

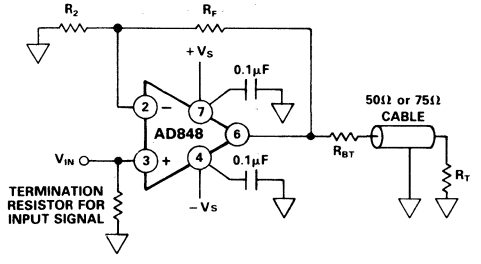


Figure 22. Video Line Driver

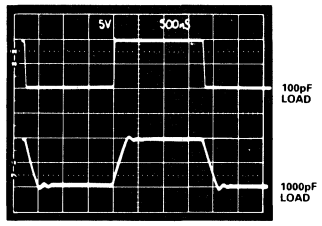


Figure 23. AD848 Driving a Capacitive Load

Often termination is not used, either because signal integrity requirements are low or because too many high frequency signals returned to ground contaminate the ground plane. Unterminated cables appear as capacitive loads. Since the AD848 and AD849 are stable into any capacitive load, the op amp will not oscillate if the cable is not terminated; however pulse integrity will be degraded. Figure 23 shows the AD848 driving both 100pF and 1000pF loads.

LOW NOISE PRE-AMP

The input voltage noise spectral densities of the AD848 and the AD849 are shown in Figure 24. The low wideband noise and high gain bandwidths of these devices makes them well suited as pre-amps for high frequency systems.

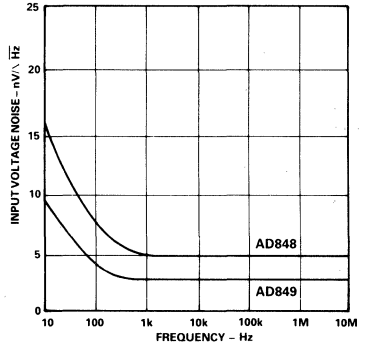


Figure 24. Input Voltage Noise Spectral Density

Input voltage noise will be the dominant source of noise at the output in most applications. Other noise sources can be minimized by keeping resistor values as small as possible.

ANALOG DEVICES

Ultrahigh Frequency Operational Amplifier

AD5539

FEATURES

Improved Replacement for Signetics SE/NE5539

AC PERFORMANCE

- **Gain Bandwidth Product: 1.4 GHz typ**
- **Unity Gain Bandwidth: 220 MHz typ**
- **High Slew Rate: 600 V/μs typ**
- **Full Power Response: 82 MHz typ**
- **Open-Loop Gain: 47 dB min, 52 dB typ**

DC PERFORMANCE

- **All Guaranteed DC Specifications Are 100% Tested For Each Device Over Its Full Temperature Range – For All Grades and Packages**
- **V_{OS}: 5 mV max Over Full Temperature Range (AD5539J)**
- **I_B: 20 μA max (AD5539J)**
- **CMRR: 70 dB min, 85 dB typ**
- **PSRR: 100 μV/V typ**
- **MIL-STD-883B Parts Available**

PRODUCT DESCRIPTION

The AD5539 is an ultrahigh frequency operational amplifier designed specifically for use in video circuits and RF amplifiers. Requiring no external compensation for gains greater than 5, it may be operated at lower gains with the addition of external compensation.

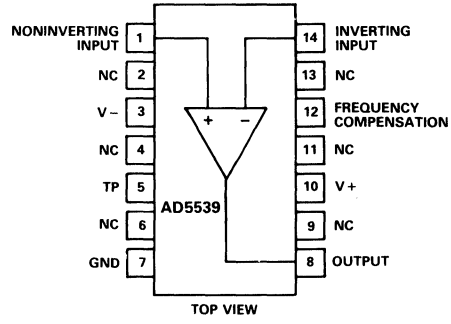
As a superior replacement for the Signetics NE/SE5539, each AD5539 is 100% dc tested to meet all of its guaranteed dc specifications over the full temperature range of the device.

The high slew rate and wide bandwidth of the AD5539 provide low cost solutions to many otherwise complex and expensive high frequency circuit design problems.

The AD5539 is available specified to operate over either the commercial (AD5539JN/JQ) or military (AD5539SQ) temperature range. The commercial grade is available either in 14-pin plastic or cerdip packages. The military version is supplied in the cerdip package. Chip versions are also available.

CONNECTION DIAGRAM

Plastic DIP (N) Package
or Cerdip (Q) Package



TOP VIEW

PRODUCT HIGHLIGHTS

1. All guaranteed dc specifications are 100% tested.
2. The AD5539 drives 50 Ω and 75 Ω loads directly.
3. Input voltage noise is less than 4 $nV\sqrt{Hz}$.
4. Low cost RF and video speed performance.
5. ±2 volt output range into a 150 Ω load.
6. Low cost.
7. Chips available.

AD5539—SPECIFICATIONS (@ +25°C and V_S = ±8 V dc, unless otherwise noted)

Parameter	AD5539J Min	AD5539J Typ	AD5539J Max	AD5539S Min	AD5539S Typ	AD5539S Max	Units
INPUT OFFSET VOLTAGE							
Initial Offset[1]		2	5		2	3	mV
T_{min} to T_{max}			6			5	mV
INPUT OFFSET CURRENT							
Initial Offset[2]		0.1	2		0.1	1	μA
T_{min} to T_{max}			5			3	μA
INPUT BIAS CURRENT							
Initial[2]							
V_{CM} = 0		6	20		6	13	μA
Either Input							
T_{min} to T_{max}			40			25	μA
FREQUENCY RESPONSE							
R_L = 150 Ω[3]							
Small Signal Bandwidth		220			220		MHz
A_{CL} = 2[4]							
Gain Bandwidth Product		1400			1400		MHz
A_{CL} = 26 dB							
Full Power Response							
A_{CL} = 2[4]		68			68		MHz
A_{CL} = 7		82			82		MHz
A_{CL} = 20		65			65		MHz
Settling Time (1%)		12			12		ns
Slew Rate		600			600		V/μs
Large Signal Propagation Delay		4			4		ns
Total Harmonic Distortion							
R_L = ∞		0.010			0.010		%
R_L = 100 Ω[3]		0.016			0.016		%
V_{OUT} = 2 V p–p							
A_{CL} = 7, f = 1 kHz							
INPUT IMPEDANCE		100			100		kΩ
OUTPUT IMPEDANCE (f <10 MHz)		2			2		Ω
INPUT VOLTAGE RANGE							
Differential[5]							
(Max Nondestructive)		250			250		mV
Common-Mode Voltage							
(Max Nondestructive)		2.5			2.5		V
Common-Mode Rejection Ratio							
ΔV_{CM} = 1.7 V							
R_S = 100 Ω	70	85		70	85		dB
T_{min} to T_{max}	60			60			dB
INPUT VOLTAGE NOISE							
Wideband RMS Noise (RTI)		5			5		μV
BW = 5 MHz; R_S = 50 Ω							
Spot Noise		4			4		$nV\sqrt{Hz}$
F = 1 kHz; R_S = 50 Ω							
OPEN-LOOP GAIN							
V_O = +2.3 V, −1.7 V							
R_L = 150 Ω[3]	47	52	58	47	52	58	dB
R_L = 2 kΩ	47		58	48		57	dB
T_{min} to T_{max} $-R_L$ = 2 kΩ	43		63	46		60	dB

Parameter	AD5539J Min	AD5539J Typ	AD5539J Max	AD5539S Min	AD5539S Typ	AD5539S Max	Units
OUTPUT CHARACTERISTICS							
Positive Output Swing							
R_L = 150 Ω[3]	+2.3	+2.8		+2.3	+2.8		V
R_L = 2 kΩ	+2.3	+3.3		+2.5	+3.3		V
T_{min} to T_{max} with							
R_L = 2 kΩ	+2.3			+2.3			V
Negative Output Swing							
R_L = 150 Ω[3]		−2.2	**−1.7**		−2.2	**−1.7**	V
R_L = 2 kΩ		−2.9	**−1.7**		−2.9	**−2.0**	V
T_{min} to T_{max} with							
R_L = 2 kΩ			**−1.5**			**−1.5**	V
POWER SUPPLY (No Load, No Resistor to $-V_S$)							
Rated Performance		±8			±8		V
Operating Range	**±4.5**		**±10**	**±4.5**		**±10**	V
Quiescent Current							
Initial I_{CC}+		14	**18**		14	**17**	mA
T_{min} to T_{max}			**20**			**18**	mA
Initial I_{CC}−		11	**15**		11	**14**	mA
T_{min} to T_{max}			**17**			**15**	mA
PSRR							
Initial		100	**1000**		100	**1000**	μV/V
T_{min} to T_{max}			**2000**			**2000**	μV/V
TEMPERATURE RANGE							
Operating,							
Rated Performance							
Commercial (0 to +70°C)	AD5539JN, AD5539JQ						
Military (−55°C to +125°C)				AD5539SQ			
PACKAGE OPTIONS[6]							
Plastic (N-14)	AD5539JN						
Cerdip (Q-14)	AD5539JQ			AD5539SQ, AD5539SQ/883B			
J and S Grade Chips Available							

NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C.
[3]R_X = 470 Ω to $-V_S$.
[4]Externally compensated.
[5]Defined as voltage between inputs, such that neither exceeds +2.5 V, −5.0 V from ground.
[6]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

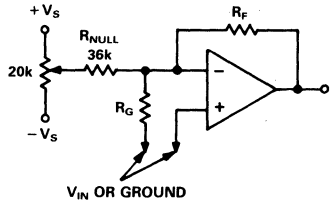
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±10V
Internal Power Dissipation	550mW
Input Voltage	+2.5V, −5.0V
Differential Input Voltage	0.25V
Storage Temperature Range Q	−65°C to +150°C
Storage Temperature Range N	−65°C to +125°C
Operating Temperature Range	
AD5539JN	0 to +70°C
AD5539JQ	0 to +70°C
AD5539SQ	−55°C to +125°C
Lead Temperature Range (Soldering 60 seconds)	300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OFFSET NULL CONFIGURATION



OUTPUT NULL RANGE = $+V_S\left(\frac{R_F}{R_{NULL}}\right)$ TO $-V_S\left(\frac{R_F}{R_{NULL}}\right)$

OFFSET NULL CONFIGURATION

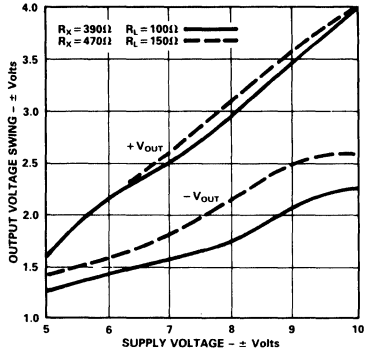


Figure 1. Output Voltage Swing vs. Supply Voltage

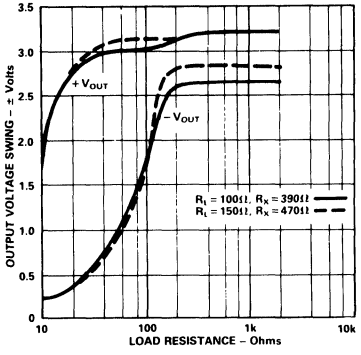


Figure 2. Output Voltage Swing vs. Load Resistance

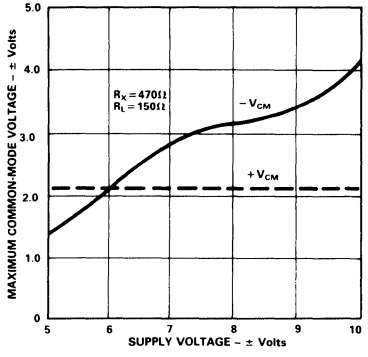


Figure 3. Maximum Common-Mode Voltage vs. Supply Voltage

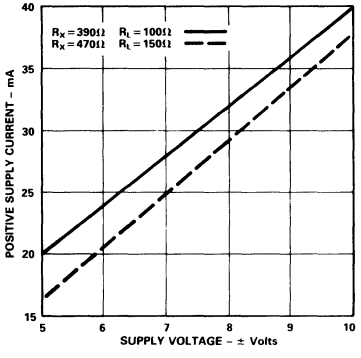


Figure 4. Positive Supply Current vs. Supply Voltage

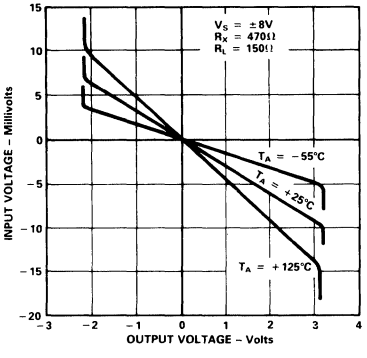


Figure 5. Input Voltage vs. Output Voltage for Various Temperatures

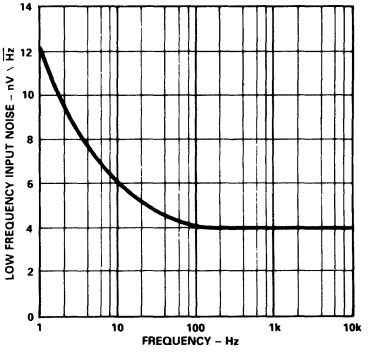


Figure 6. Low Frequency Input Noise vs. Frequency

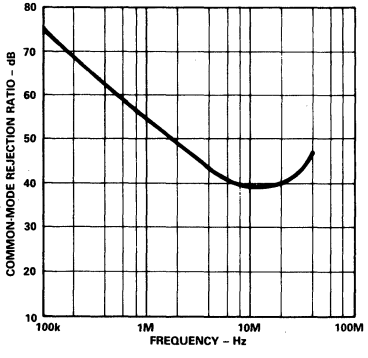


Figure 7. Common-Mode Rejection Ratio vs. Frequency

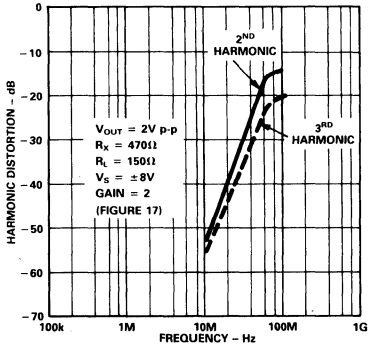


Figure 8. Harmonic Distortion vs. Frequency – Low Gain

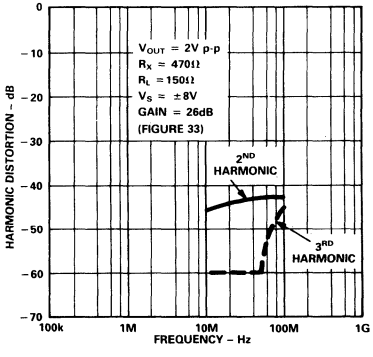


Figure 9. Harmonic Distortion vs. Frequency – High Gain

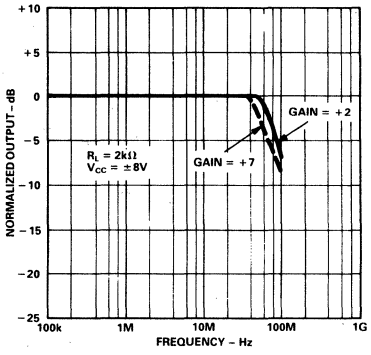


Figure 10. Full Power Response

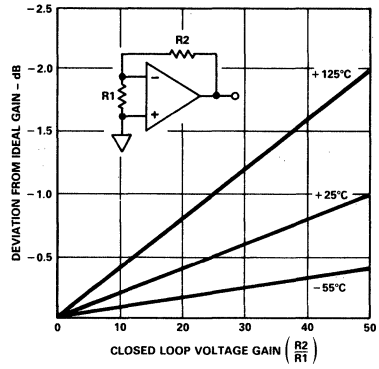


Figure 11. Deviation from Ideal Gain vs. Closed-Loop Voltage Gain

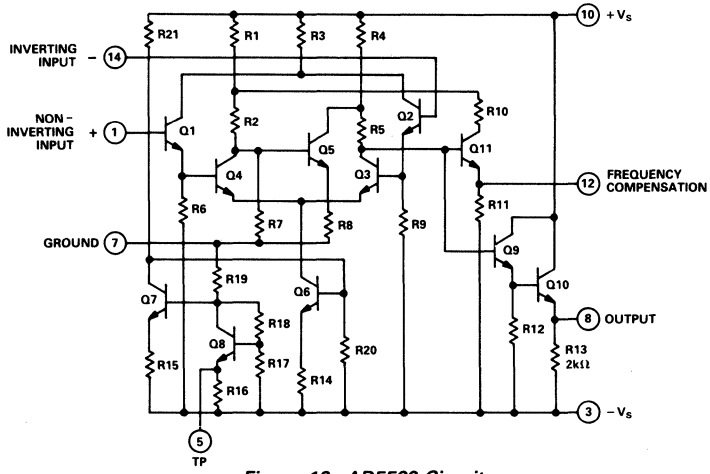


Figure 12. AD5539 Circuit

FUNCTIONAL DESCRIPTION

The AD5539 is a two-stage, very high frequency amplifier. Darlington input transistors Q1, Q4 –Q2, Q3 form the first stage — a differential gain amplifier with a voltage gain of approximately 50. The second stage, Q5, is a single-ended amplifier whose input is derived from one phase of the differential amplifier output; the other phase of the differential output is then summed with the output of Q5. The all NPN design of the AD5539 is configured such that the emitter of Q5 is returned, via a small résistor to ground; this eliminates the need for separate level shifting circuitry.

The output stage, consisting of transistors Q9 and Q10, is a Darlington voltage follower with a resistive pull-down. The bias section, consisting of transistors Q6, Q7 and Q8, provides a stable emitter current for the input section, compensating for temperature and power supply variations.

SOME GENERAL PRINCIPLES OF HIGH FREQUENCY CIRCUIT DESIGN

In designing practical circuits with the AD5539, the user must remember that whenever very high frequencies are involved, some special precautions are in order. All real-world applications circuits must be built using proper RF techniques: the use of short interconnect leads, adequate shielding, groundplanes, and very low profile IC sockets. In addition, very careful bypassing of power supply leads is a must.

Low-impedance transmission line is frequently used to carry signals at RF frequencies: 50 Ω line for telecommunications purposes and 75 Ω for video applications. The AD5539 offers a relatively low output impedance; therefore, some consideration must be given to impedance matching. A common matching technique involves simply placing a resistor in series with the amplifier output that is equal to the characteristic impedance of the transmission line. This provides a good match (although at a loss of 6 dB), adequate for many applications.

All of the circuits here were built and tested in a 50 Ω system. Care should be taken in adapting these circuits for each particular use. Any system which has been properly matched and terminated in its characteristic impedance should have the same small signal frequency response as those shown in this data sheet.

APPLYING THE AD5539

The AD5539 is stable for closed-loop gains of 4 or more as an inverter and at (noise) gains of 5 or greater as a voltage follower. This means that whenever the AD5539 is operated at noise gains below 5, external frequency compensation must be used to insure stable operation.

The following sections outline specific compensation circuits which permit stable operation of the AD5539 down to follower (noise) gains of 3 (inverting gains of 2) with corresponding −3 dB bandwidths up to 390 MHz. External compensation is achieved by modifying the frequency response to the AD5539's external feedback network (i.e., by adding lead-lag compensation) so that the amplifier operates at a noise gain of 5 (or more) at frequencies over 44 MHz, independent of signal gain.

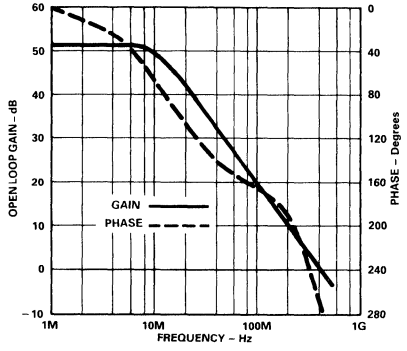


Figure 13. Small Signal Open-Loop Gain and Phase vs. Frequency

GENERAL PRINCIPLES OF LEAD AND LAG COMPENSATION

The AD5539 has its first pole or breakpoint in its open-loop frequency response at about 10 MHz (see Figure 13). At frequencies beyond 100 MHz, phase shift increases such that the output lags the input by 180° — well before the unity gain crossover frequency. Therefore, severe peaking (and possible oscillation) will result if the AD5539 is operated at noise gains below 5, unless external compensation is employed. Figure 14 shows the uncompensated closed-loop frequency response of the AD5539 when operating at a noise gain of 7. Under these conditions, excess phase shift causes nearly 10 dB of peaking at 150 MHz.

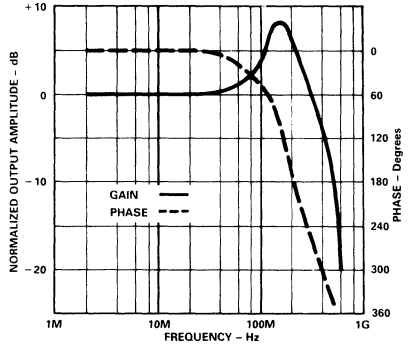


Figure 14. AD5539 Uncompensated Response, Closed-Loop Gain = 7

Figure 15 illustrates the use of both lead and lag compensation to permit stable low-gain operation. The AD5539 is shown connected as an inverting amplifier with the required external components added to provide stability and improve high frequency response. The stray capacitance between the amplifier summing junction and ground, C_X, represents whatever capacitance is associated with the particular type of op amp package used plus the stray wiring capacitance at the summing junction.

Evaluating the lead capacitance first (ignoring R_{LAG} and C_{LAG} for now): the feedback network, consisting of R2 and C_{LEAD}, has a pole frequency equal to:

$$F_A = \frac{1}{2\pi\,(C_{LEAD} + C_X)\,(R1 \parallel R2)} \quad (1)$$

and a zero frequency equal to:

$$F_B = \frac{1}{2\pi\,(R1 \times C_{LEAD})} \quad (2)$$

Usually, frequency F_A is made equal to F_B; that is, $(R1C_X) = (R2\ C_{LEAD})$, in a manner similar to the compensation used for an attenuator or scope probe. However, if the pole frequency, F_A, will lie above the unity gain crossover frequency (440 MHz), then the optimum location of F_B will be near the

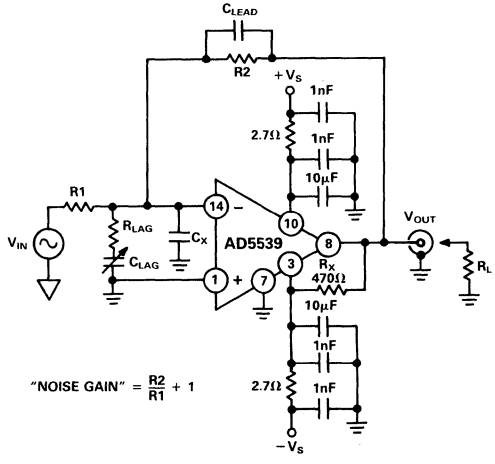


Figure 15. Inverting Amplifier Model Showing Both Lead and Lag Compensation

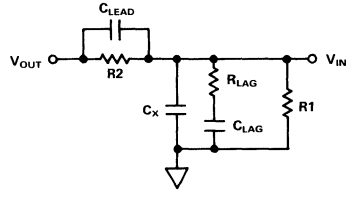


Figure 16. A Model of the Feedback Network of the Inverting Amplifier

crossover frequency. Both of these circuit techniques add a large amount of leading phase shift at the crossover frequency, greatly aiding stability.

The lag network (R_{LAG}, C_{LAG}) increases the feedback attenuation, i.e., the amplifier operates at a higher noise gain, above some frequency, typically one-tenth of the crossover frequency. As an example, to achieve a noise gain of 5 at frequencies above 44 MHz, for the circuit of Figure 15, would require a network of:

$$R_{LAG} = \frac{R1}{(4R1/R2) - 1} \quad (3)$$

and . . .

$$C_{LAG} = \frac{1}{2\pi\, R_{LAG}\, (44 \times 10^6)} \quad (4)$$

It is worth noting that an R_{LAG} resistor may be used alone, to increase the noise gain above 5 at all frequencies. However, this approach has the disadvantage of also increasing the dc offset and low frequency noise errors by an amount equal to the increase in gain, in this case, by a factor of 5.

SOME PRACTICAL CIRCUITS

The preceding general principles may now be applied to some actual circuits.

A General Purpose Inverter Circuit

Figure 17 is a general purpose inverter circuit operating at a gain of −2.

For this circuit, the total capacitance at the inverting input is approximately 3 pF; therefore, C_{LEAD} from Equations 1 and 2 needs to be approximately 1.5 pF. As shown in Figure 17, a small trimmer is used to optimize the frequency response of this circuit. Without a lag compensation network, the noise gain of the circuit is 3.0 and, as shown in Figure 18, the output amplitude remains within ±0.5 dB to 170 MHz and the −3 dB bandwidth is 200 MHz.

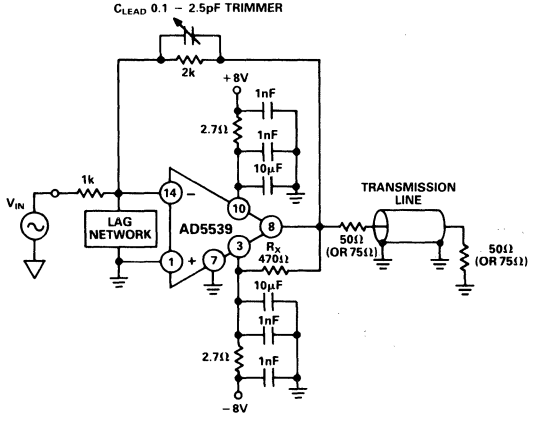


Figure 17. A General Purpose Inverter Circuit

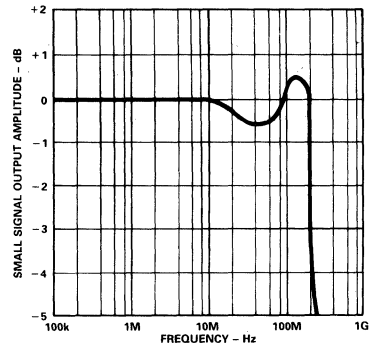


Figure 18. Response of the (Figure 17) Inverter Circuit without a Lag Compensation Network

A lag network (Figure 15) can be added to improve the response of this circuit even further as shown in Figures 19 and 20. In almost all cases, it is imperative to make capacitor C_{LEAD} adjustable; in some cases, C_{LAG} must also be variable. Otherwise, component and circuit capacitance variations will dominate circuit performance.

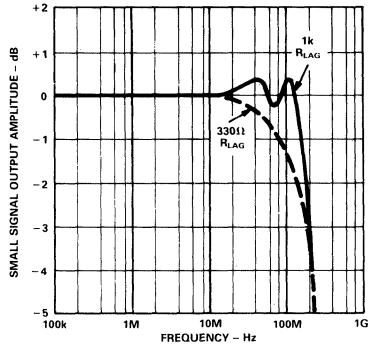


Figure 19. Response of the (Figure 17) Inverter Circuit with an R_{LAG} Compensation Network Employed

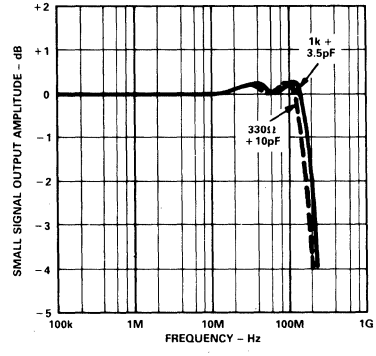


Figure 20. Response of the (Figure 17) Inverter Circuit with an R_{LAG} and a C_{LAG} Compensation Network Employed

Figures 21 and 22 show the small and large signal pulse responses of the general purpose inverter circuit of Figure 17, with C_{LEAD}=1.5 pF, R_{LAG}=330 Ω and C_{LAG}=3.5 pF.

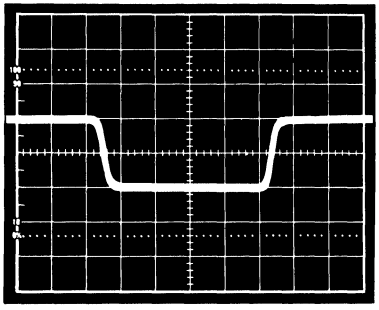


Figure 21. Small Signal Pulse Response of the (Figure 17) Inverter Circuit; Vertical Scale: 50 mV/div; Horizontal Scale: 5 ns/div

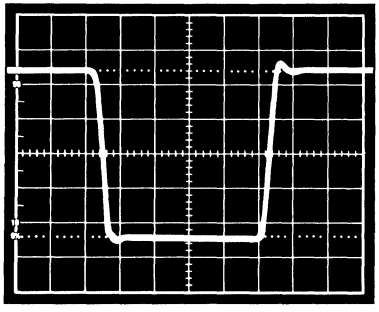


Figure 22. Large Signai Response of the (Figure 17) Inverter Circuit; Vertical Scale: 200 mV/div, Horizontal Scale: 5 ns/div

A C_{LEAD} capacitor may be used to limit the circuit bandwidth and to achieve a single pole response free of overshoot

$$\left(-3\ dB\ frequency = \frac{1}{2\pi\ R2\ C_{LEAD}}\right)$$

If this option is selected, it is recommended that a C_{LEAD} be connected between Pin 12 and the summing junction, as shown in Figure 23. Pin 12 provides a separately buffered version of the output signal. Connecting the lead capacitor here avoids the excess output-stage phase shift and subsequent oscillation problems (at approx. 350 MHz) which would otherwise occur when using the circuit of Figure 17 with a C_{LEAD} of more than about 2 pF.

Figure 24 shows the response of the circuit of Figure 23 for each connection of C_{LEAD}. Lag components may also be added to this circuit to further tailor its response, but, in this case, the results will be slightly less satisfactory than connecting C_{LEAD} directly to the output, as was done in Figure 17.

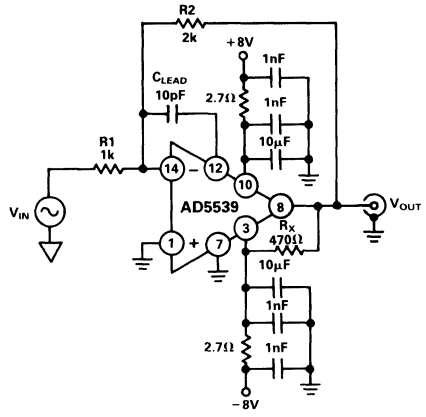


Figure 23. A Gain of 2 Inverter Circuit with the C_{LEAD} Capacitor Connected to Pin 12

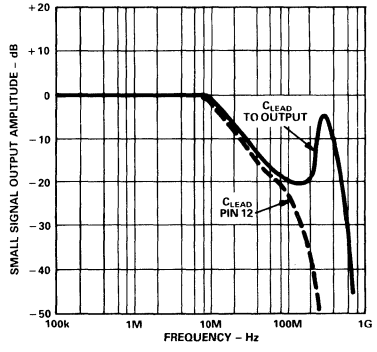


Figure 24. Response of the Circuit of Figure 23 with C_{LEAD} = 10 pF

A General Purpose Voltage Follower Circuit

Noninverting (voltage follower) circuits pose an additional complication, in that when a lag network is used, the source impedance will affect the noise gain. In addition, the slightly greater bandwidth of the noninverting configuration makes any excess phase shift due to the output stage more of a problem.

For example, a gain of 3 noninverting circuit with C_{LEAD} connected normally (across the feedback resistor — Figure 25) will require a source resistance of 200 Ω or greater to prevent UHF oscillation; the extra source resistance provides some damping as well as increasing the noise gain. The frequency response plot of Figure 26 shows that the highest −3 dB frequency of all the applications circuits can be achieved using this connection, unfortunately, at the expense of a noise gain of 14.2.

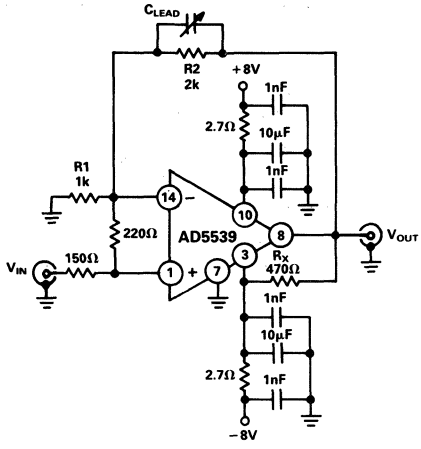


Figure 25. A Gain of 3 Follower with Both Lead and Lag Compensation

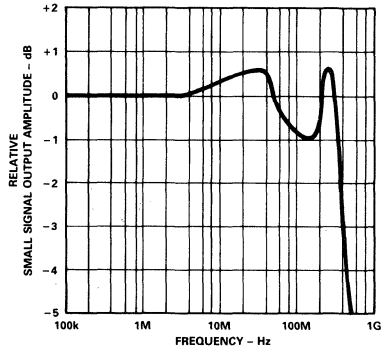


Figure 26. Response of the Gain of 3 Follower Circuit

Adding a lag capacitor (Figure 27) will greatly reduce the mid-band and low frequency noise gain of the circuit while sacrificing only a small amount of bandwidth as shown in Figure 28.

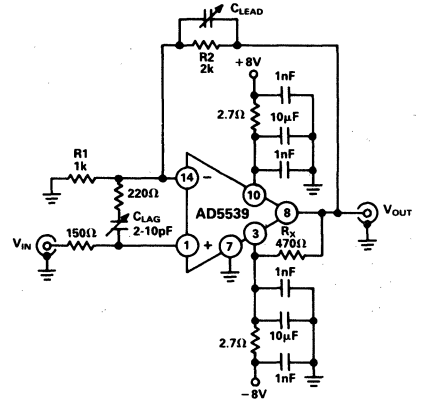


Figure 27. A Gain of 3 Follower Circuit with Both C_{LEAD} and R_{LAG} Compensation

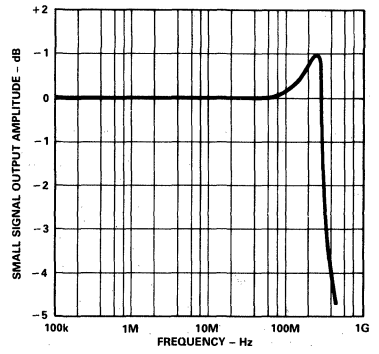


Figure 28. Response of the Gain of 3 Follower with C_{LEAD}, C_{LAG} and R_{LAG}

These same principles may be applied when capacitor C_{LEAD} is connected to Pin 12 (Figure 29). Figure 30 shows the bandwidth of the gain of 3 amplifier for various values of R_{LAG}. It can be seen from these response plots that a high noise gain is still needed to achieve a reasonably flat response (the smaller the

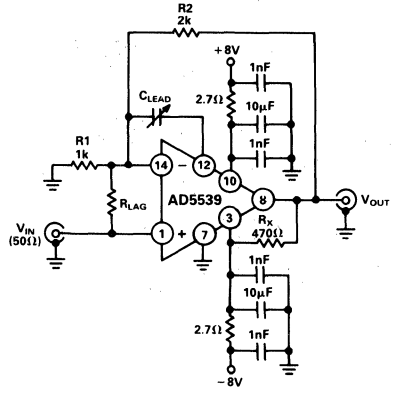


Figure 29. A Gain of 3 Follower Circuit with C_{LEAD} Compensation Connected to Pin 12

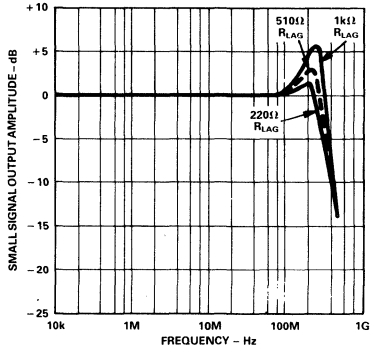


Figure 30. Response of the Gain of 3 Follower Circuit with C_{LEAD} Connected to Pin 12

value of R_{LAG}, the higher the noise gain). For example, with a 220 Ω R_{LAG} and a 50 Ω source resistance, the noise gain will be 12.8, because the source resistance affects the noise gain.

Figures 31 and 32 show the small and large signal responses of the circuit of Figure 29.

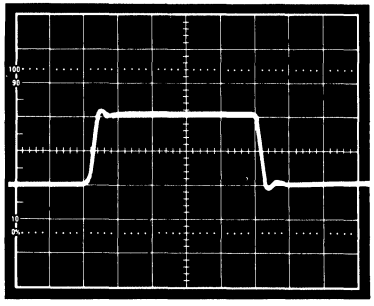


Figure 31. The Small-Signal Pulse Response of the Gain of 3 Follower Circuit with R_{LAG} and C_{LEAD} Compensation to Pin 12; Vertical Scale: 50 mV/div; Horizontal Scale: 5 ns/div

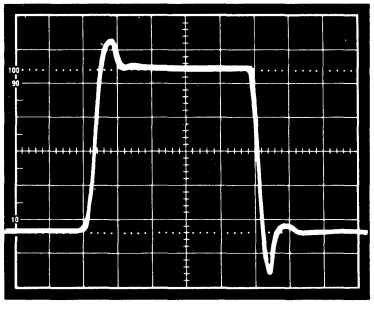


Figure 32. The Large-Signal Pulse Response of the Gain of 3 Follower Circuit with R_{LAG} and C_{LEAD} Compensation to Pin 12; Vertical Scale: 200 mV/div; Horizontal Scale: 5 ns/div

A Video Amplifier Circuit with 20 dB Gain (Terminated)

High gain applications (14 dB and up) require only a small lead capacitance to obtain flat response. The 26 dB (20 dB terminated) video amplifier circuit of Figure 33 has the response shown in Figure 34 using only approximately 0.5–1 pF lead capacitance. Again, a small C_{LEAD} can be connected, either to the output or to Pin 12 with very little difference in response.

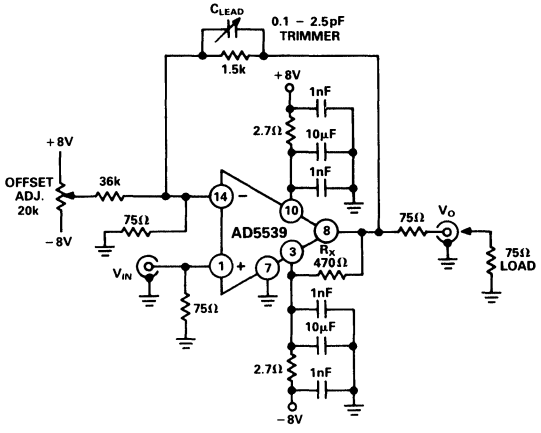


Figure 33. A 20 dB Gain Video Amplifier for 75 Ω Systems

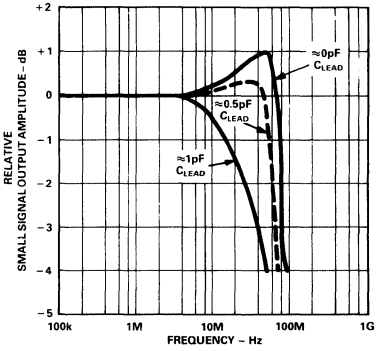


Figure 34. Response of the 20 dB Video Amplifier

In color video applications, the quality of differential gain and differential phase response is very important. Figures 35 and 36 show a circuit and test setup to measure the AD5539's response to a modulated ramp signal (0–90 IRE p–p ramp, 40 IRE p–p modulation, 4.4 MHz).

Figures 37 and 38 show the differential gain and phase response.

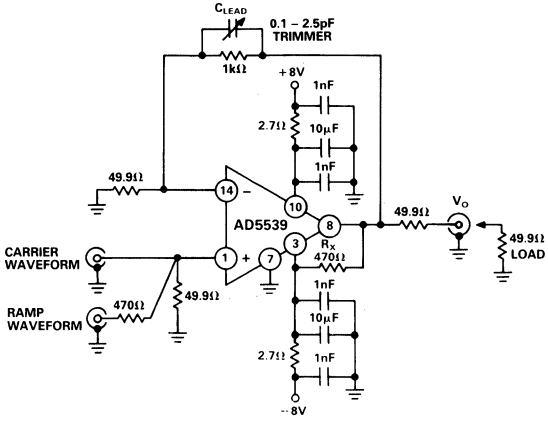


Figure 35. Differential Gain and Phase Measurement Circuit

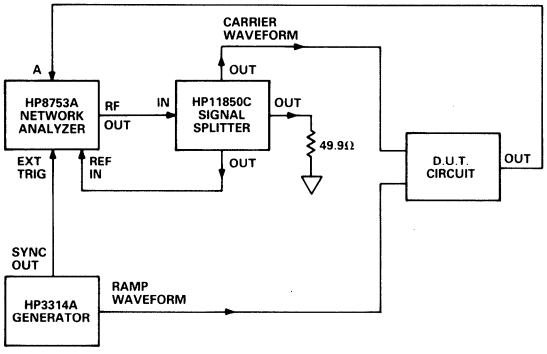


Figure 36. Differential Gain and Phase Test Setup

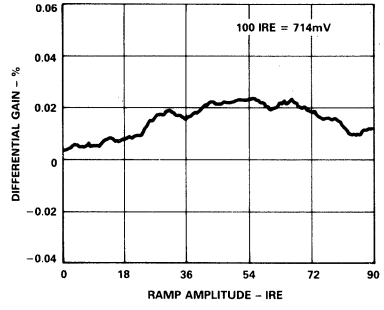


Figure 37. Differential Gain vs. Ramp Amplitude

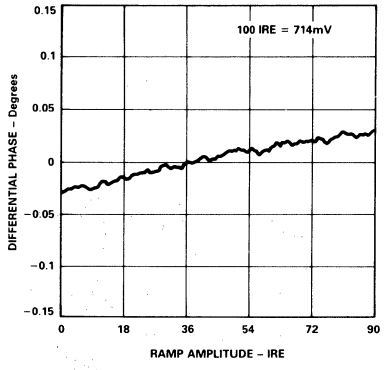


Figure 38. Differential Phase vs. Ramp Amplitude

MEASURING AD5539 SETTLING TIME

Measuring the very rapid settling times associated with AD5539 can be a real problem for the designer; proper component layout must be used and appropriate test equipment selected. In addition, both cable dispersion (a function of cable losses) and the quality of termination (SWR) directly affect the measurement. The circuit of Figure 39 was used to make a "brute force" AD5539 settling time measurement. The fixture containing the circuit was connected directly — using a male BNC connector (but no cable) — onto the front of a 50 Ω input oscilloscope preamp. A digital mainframe was then used to capture, average, and expand the error signal. Most of the small-scale waveform aberrations shown on the figure were caused by the oscilloscope itself, especially the glitch at 15 ns. The pulse source used for this measurement was an EH-SPG2000 pulse generator set for a 1 ns rise-time; it was coupled directly to the circuit using 18″ of microwave 50 Ω hard line.

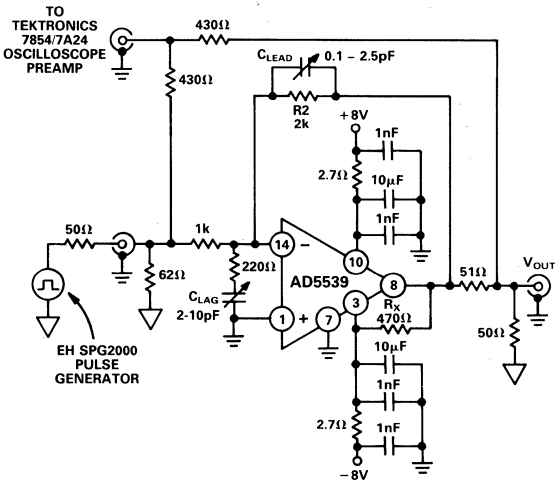


Figure 39. AD5539 Settling Time Test Circuit

APPLICATIONS SUMMARY CHART

	R1	R2[1]	R_{LAG}	C_{LAG}[2]	C_{LEAD}[2]	GAIN	GAIN FLATNESS (TRIMMED)	3 dB BANDWIDTH
Gain = −1 to −5 Circuit of Fig. 17	$\frac{R2}{G}$	2 k	$\leqq \frac{R1}{4\frac{R1}{R2} - 1}$	$\geqq \frac{1}{2\pi (44 \times 10^6) R_{LAG}}$	$\approx \frac{3\text{ pF}}{G}$	−2	±0.2 dB	200 MHz
Gain = −1 to −5 Circuit of Fig. 23	$\frac{R2}{G}$	2 k	$\leqq \frac{R1}{4\frac{R1}{R2} - 1}$	$\geqq \frac{1}{2\pi (44 \times 10^6) R_{LAG}}$	$\approx \frac{3\text{ pF}}{G}$	−2	±1 dB	180 MHz
Gain = −2 to +5[3] Circuit of Fig. 27	$\frac{R2}{G-1}$	2 k	$\leqq \frac{R1}{10\frac{R1}{R2} - 1}$	$\geqq \frac{1}{2\pi (44 \times 10^6) R_{LAG}}$	$\approx \frac{3\text{ pF}}{G-1}$	+3	±1 dB	390 MHz
Gain = +2 to +5[4] Circuit of Fig. 29	$\frac{R2}{G-1}$	2 k	$\leqq \frac{R1}{10\frac{R1}{R2} - 1}$	NA	$\approx \frac{3\text{ pF}}{G-1}$	+3	±0.5 dB	340 MHz
Gain < −5	$\frac{R2}{G}$	1.5 k	NA	NA	Trimmer[5]	−20	±0.2 dB	80 MHz
Gain >+5	$\frac{R}{G-1}$	1.5 k	NA	NA	Trimmer[5]	+20	±0.2 dB	80 MHz

NOTES
G=Gain NA=Not Applicable
[1]Values given for specific results summarized here—applications can be adapted for values different than those specified.
[2]It is recommended that C_{LEAD} and C_{LAG} be trimmers covering a range that includes the computed value above.
[3]$R_{SOURCE} \geq 200\ \Omega$.
[4]$R_{SOURCE} \geq 50\ \Omega$.
[5]Use Voltronics CPA2 0.1–2.5 pF Teflon Trimmer Capacitor (or equivalent).

The photos of Figures 40 and 41 demonstrate how the AD5539 easily settles to 1% (1 mV) in less than 12 ns; settling to 0.1% (100 μV) requires less than 25 ns.

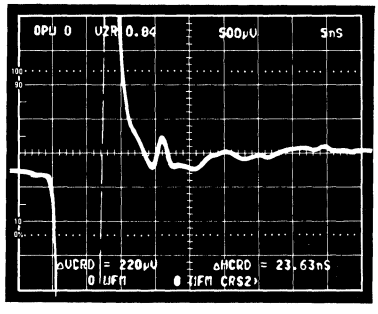


Figure 40. Error Signal from AD5539 Settling Time Test Circuit – Falling Edge. Vertical Scale: 5 ns/div.; Horizontal Scale: 500 μV/div

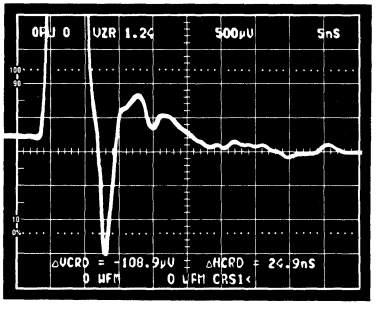


Figure 41. Error Signal from AD5539 Settling Time Test Circuit – Rising Edge. Vertical Scale: 5 ns/div.; Horizontal Scale: 500 μV/div

Figure 42 shows the oscilloscope response of the generator alone, set up to simulate the ideal test circuit error signal (Figure 43).

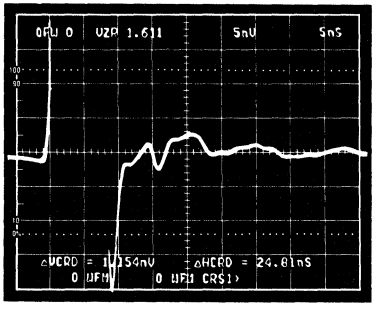


Figure 42. The Oscilloscope Response Alone Directly Driven by the Test Generator. Vertical Scale: 5 ns/div.; Horizontal Scale: 500 μV/div

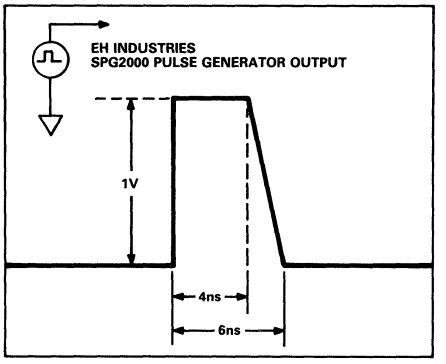


Figure 43. A Simulated Ideal Test Circuit Error Signal

A 50 MHz VOLTAGE-CONTROLLED AMPLIFIER

Figure 44 is a circuit for a 50 MHz voltage-controlled amplifier (VCA) suitable for use in high quality video-speed applications. This circuit uses the AD5539 as an output amplifier for the AD539, a high bandwidth multiplier. The outputs from the two signal channels of the AD539 are applied to the op amp in a subtracting configuration. This connection has two main advantages: first, it results in better rejection of the control voltage, particularly when over-driven (V_X<0 or V_X>3.3 V). Secondly, it provides a choice of either noninverting or inverting responses, using either input V_{Y1} or V_{Y2}, respectively. In this circuit, the output of the op amp will equal:

$$V_{OUT} = \frac{V_X (V_{Y1} - V_{Y2})}{2V} \text{ for } V_X > 0$$

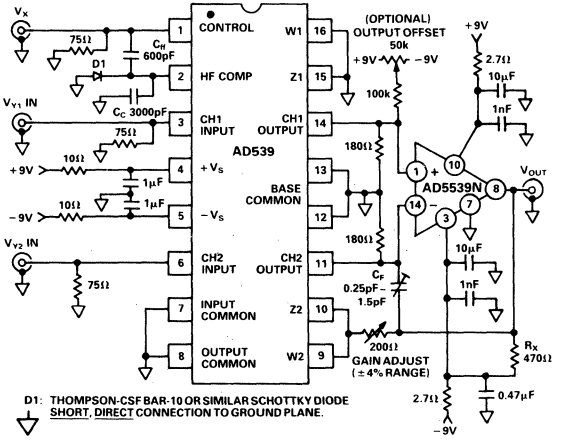


Figure 44. A Wide Bandwidth Voltage-Controlled Amplifier

Hence, the gain is unity at V_X = +2 V. Since V_X can overrange to +3.3 V, the maximum gain in this configuration is about 4.3 dB. (Note: If Pin 9 of the AD539 is grounded, rather than connected to the output of the 5539N, the maximum gain becomes 10 dB.)

The bandwidth of this circuit is over 50 MHz at full gain, and is not substantially affected at lower gains. Of course, when V_X is zero (or slightly negative, to override the residual input offset) there is still a small amount of capacitive feedthrough at high frequencies; therefore, extreme care is needed in laying out the PC board to minimize this effect. Also, for small values of V_X, the combination of this feedthrough with the multiplier output can cause a dip in the response where they are out of phase. Figure 45 shows the ac response from the noninverting input, with the response from the inverting input, V_{Y2}, essentially identical. Test conditions: V_{Y1} = 0.5 V rms for values of V_X from +10 mV to +3.16 V; this is with a 75 Ω load on the output. The feedthrough at V_X = −10 mV is also shown.

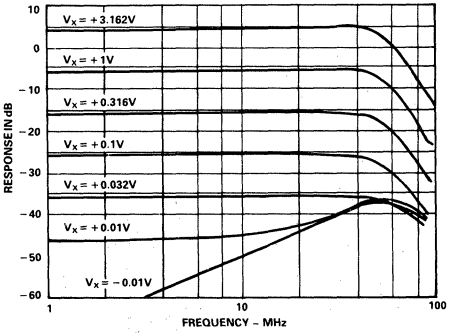


Figure 45. AC Response of the VCA at Different Gains V_Y = 0.5 V RMS

The transient response of the signal channel at V_X = +2 V, V_Y = V_{OUT} = + or −1 V is shown in Figure 46; with the VCA driving a 75 Ω load. The rise and fall times are both approximately 7 ns.

A few final circuit details: in general, the control amplifier compensation capacitor for Pin 2, C_C, must have a minimum value of 3000 pF (3 nF) to provide both circuit stability and maximum control bandwidth. However, if the *maximum* control bandwidth is not needed, then it is advisable to use a larger value of C_C, with typical values between 0.01 and 0.1 μF. Like many aspects of design, the value of C_C will be a tradeoff: higher values of C_C will lower the high frequency distortion, reduce the high frequency crosstalk and improve the signal channel phase response. Conversely, lower values of C_C will provide a higher control channel bandwidth at the expense of degraded linearity in the output response when amplitude modulating a carrier signal.

The control channel bandwidth will vary in inverse proportion to the value of C_C, providing a typical bandwidth of 2 MHz with a C_C of 0.01 μF and a V_X voltage of +1.7 volts.

Both the bandwidth and pulse response of the control channel can be further increased by using a feedforward capacitor, C_{ff}, with a value between 5 and 20 percent of C_C. C_{ff} should be carefully adjusted to give the best pulse response for a particular step input applied to the control channel. Note that since C_{ff} is connected between a linear control input (Pin 1) and a logarithmic node, the settling time of the control channel with a pulse input will vary with different control input step levels.

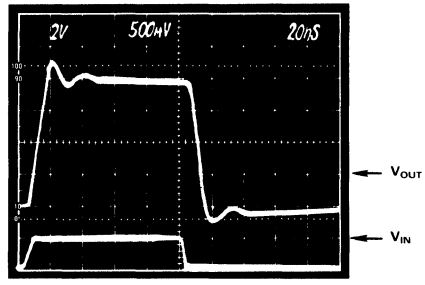


Figure 46. Transient Response of the Voltage-Controlled Amplifier V_X = +2 Volts, V_Y = ±1 Volt

Diode D1 clamps the logarithmic control node at Pin 2 of the AD539, (preventing this point from going too negative); this diode helps decrease the circuit recovery time when the control input goes below ground potential.

THE AD539/5539 COMBINATION AS A FAST, LOW FEEDTHROUGH, VIDEO SWITCH

Figure 47 shows how the AD539/5539 combination can be used to create a fast video speed switch suitable for many high fre-

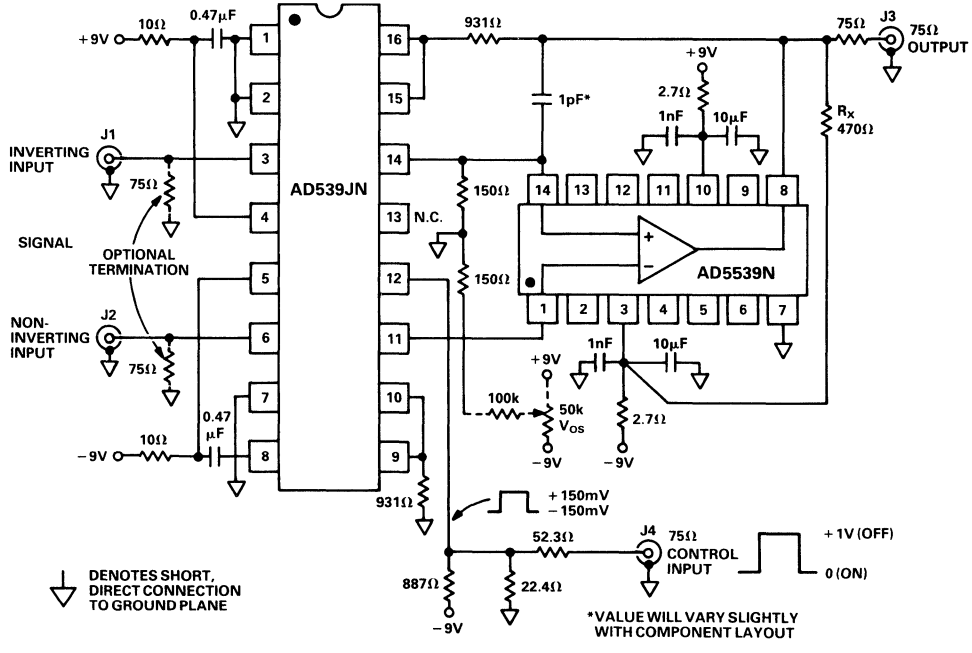


Figure 47. An Analog Multiplier Video Switch

quency applications including color key switching. It features both inverting and noninverting inputs and can provide an output of ±1 V into a reverse-terminated 75 Ω load (or ±2 V into 150 Ω). An optional output offset adjustment is provided. The input range of the video switch is the same as the output range: ±1 V at either input generates ±1 V (noninverting) or ∓1 V (inverting) across the 75 Ω load. The circuit provides a gain of about 1, when "ON," or zero when "OFF."

The differential configuration uses both channels of the AD539 not only to provide alternative input phases, but also to eliminate the switching pedestal due to step changes in the output current as the AD539 is gated on or off.

Figure 49 shows the response to a pulse of 0 to +1 V on the signal channel. With the control input held at zero, the rise time is under 10 ns. The response from the inverting input is similar.

The differential-gain and differential-phase characteristics of this switch are compatible with video applications. The incremental gain changes less than 0.05 dB over a signal window of 0 to +1 V, with a phase variation of less than 0.5 degree at the subcarrier frequency of 3.58 MHz. The noise level of this circuit measured at the 75 Ω load is typically 200 μV in a 0 to 5 MHz bandwidth or approximately 100 nV per root hertz. The noise spectral density is essentially flat to 40 MHz.

The waveforms shown in Figures 48 and 49 were taken across a 75 Ω termination; in both photos, the signal of 0 to +1 V (in this case, an offset sine wave at 1 MHz) was applied to the noninverting input. In Figure 48, the envelope response shows the output being fully switched in about 50 ns. Note that the output is ON when the control input is zero (or more negative) and OFF for a control input of +1 V or more. There is very little control-signal breakthrough.

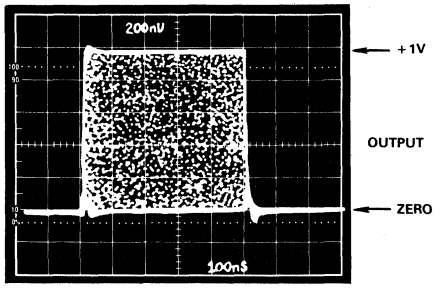


Figure 48. The Control Response of the Video Switcher

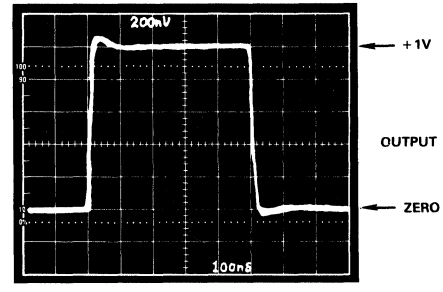


Figure 49. The Signal Response of the Video Switcher

ANALOG DEVICES

Low Noise Precision Operational Amplifier

OP-27

FEATURES

- **Low Noise** ..... **80nV$_{p-p}$ (0.1Hz to 10Hz)**
  ..... **3nV/$\sqrt{Hz}$**
- **Low Drift** ..... **0.2μV/°C**
- **High Speed** ..... **2.8V/μs Slew Rate**
  ..... **8MHz Gain Bandwidth**
- **Low V_{OS}** **10μV**
- **Excellent CMRR** ..... **126dB at V_{CM} of ±11V**
- **High Open-Loop Gain** ..... **1.8 Million**
- **Fits 725, OP-07, OP-05, AD510, AD517, 5534A sockets**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (µV)	PACKAGE TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
25	OP27AJ*	OP27AZ*	–	–	MIL
25	OP27EJ	OP27EZ	OP27EP	–	IND/COM
60	OP27BJ*	OP27BZ*	–	OP27BR/883	MIL
60	OP27FJ	OP27FZ	OP27FP	–	IND/COM
100	OP27CJ	OP27CZ	–	–	MIL
100	OP27GJ	OP27GZ	OP27GP	–	XIND
100	–	–	OP27GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

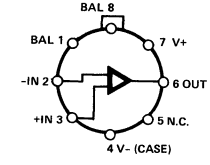
The OP-27 precision operational amplifier combines the low offset and drift of the OP-07 with both high-speed and low-noise. Offsets down to 25μV and drift of 0.6μV/°C maximum make the OP-27 ideal for precision instrumentation applications. Exceptionally low noise, e_n = 3.5nV/$\sqrt{Hz}$, at 10Hz, a low 1/f noise corner frequency of 2.7Hz, and high gain (1.8 million), allow accurate high-gain amplification of low-level signals. A gain-bandwidth product of 8MHz and a 2.8V/μsec slew rate provides excellent dynamic accuracy in high-speed data-acquisition systems.

A low input bias current of ±10nA is achieved by use of a bias-current-cancellation circuit. Over the military temperature range, this circuit typically holds I_B and I_{OS} to ±20nA and 15nA respectively.

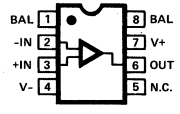
The output stage has good load driving capability. A guaranteed swing of ±10V into 600Ω and low output distortion make the OP-27 an excellent choice for professional audio applications.

PSRR and CMRR exceed 120dB. These characteristics, coupled with long-term drift of 0.2μV/month, allow the circuit designer to achieve performance levels previously attained only by discrete designs.

PIN CONNECTIONS



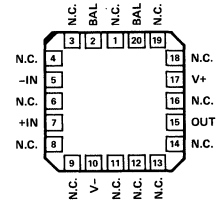
TO-99
(J-Suffix)



8-PIN HERMETIC DIP
(Z-Suffix)

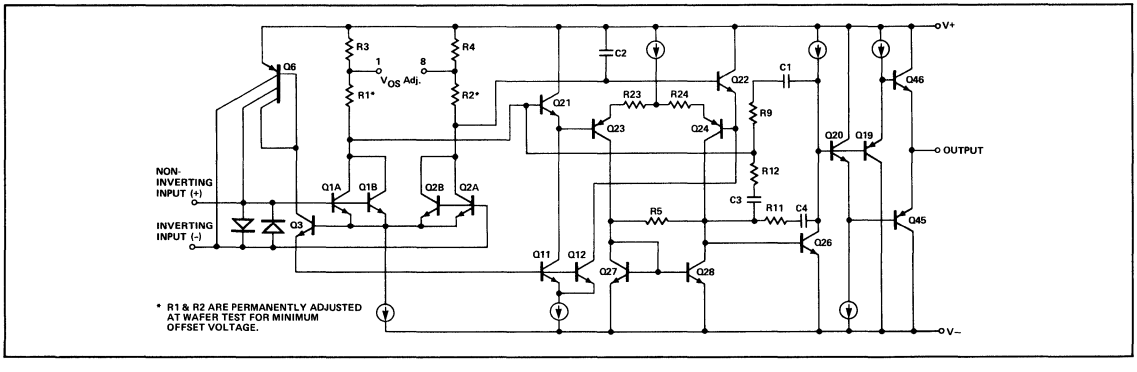
EPOXY MINI-DIP
(P-Suffix)

8-PIN SO
(S-Suffix)



OP-27BRC/883
LCC PACKAGE
(RC-Suffix)

SIMPLIFIED SCHEMATIC



OP-27

Low cost, high-volume production of OP-27 is achieved by using an on-chip zener-zap trimming network. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history.

The OP-27 provides excellent performance in low-noise high-accuracy amplification of low-level signals. Applications include stable integrators, precision summing amplifiers, precision voltage-threshold detectors, comparators, and professional audio circuits such as tape-head and microphone preamplifiers.

The OP-27 is a direct replacement for 725, OP-06, OP-07 and OP-05 amplifiers; 741 types may be directly replaced by removing the 741's nulling potentiometer.

ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage ..... ±22V
Input Voltage (Note 1) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Differential Input Voltage (Note 2) ..... ±0.7V
Differential Input Current (Note 2) ..... ±25mA
Storage Temperature Range ..... –65°C to +150°C

Operating Temperature Range
OP-27A, OP-27B, OP-27C (J, Z, RC)..... –55°C to +125°C
OP-27E, OP-27F (J, Z) ..... –25°C to +85°C
OP-27E, OP-27F (P) ..... 0°C to +70°C
OP-27G (P, S, J, Z) ..... –40°C to +85°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. The OP-27's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.
4. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-27A/E			OP-27B/F			OP-27C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	10	25	—	20	60	—	30	100	μV
Long-Term V_{OS} Stability	V_{OS}/Time	(Notes 2, 3)	—	0.2	1.0	—	0.3	1.5	—	0.4	2.0	μV/Mo
Input Offset Current	I_{OS}		—	7	35	—	9	50	—	12	75	nA
Input Bias Current	I_B		—	±10	±40	—	±12	±55	—	±15	±80	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Notes 3, 5)	—	0.08	0.18	—	0.08	0.18	—	0.09	0.25	μVp-p
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 3)	—	3.5	5.5	—	3.5	5.5	—	3.8	8.0	nV/√Hz
		f_O = 30Hz (Note 3)	—	3.1	4.5	—	3.1	4.5	—	3.3	5.6	
		f_O = 1000Hz (Note 3)	—	3.0	3.8	—	3.0	3.8	—	3.2	4.5	
Input Noise Current Density	i_n	f_O = 10Hz (Notes 3,6)	—	1.7	4.0	—	1.7	4.0	—	1.7	—	pA/√Hz
		f_O = 30Hz (Notes 3, 6)	—	1.0	2.3	—	1.0	2.3	—	1.0	—	
		f_O = 1000Hz (Notes 3, 6)	—	0.4	0.6	—	0.4	0.6	—	0.4	0.6	
Input Resistance — Differential-Mode	R_{IN}	(Note 7)	1.3	6	—	0.94	5	—	0.7	4	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	3	—	—	2.5	—	—	2	—	GΩ
Input Voltage Range	IVR		±11.0	±12.3	—	±11.0	±12.3	—	±11.0	±12.3	—	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±11V	114	126	—	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4V to ±18V	—	1	10	—	1	10	—	2	20	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	1000	1800	—	1000	1800	—	700	1500	—	V/mV
		$R_L \geq 600\Omega$, V_O = ±10V	800	1500	—	800	1500	—	600	1500	—	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±13.8	—	±12.0	±13.8	—	±11.5	±13.5	—	V
		$R_L \geq 600\Omega$	±10.0	±11.5	—	±10.0	±11.5	—	±10.0	±11.5	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 4)	1.7	2.8	—	1.7	2.8	—	1.7	2.8	—	V/μs

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-27A/E MIN	OP-27A/E TYP	OP-27A/E MAX	OP-27B/F MIN	OP-27B/F TYP	OP-27B/F MAX	OP-27C/G MIN	OP-27C/G TYP	OP-27C/G MAX	UNITS
Gain Bandwidth Prod.	GBW	(Note 4)	5.0	8.0	—	5.0	8.0	—	5.0	8.0	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	70	—	—	70	—	—	70	—	Ω
Power Consumption	P_d	V_O	—	90	140	—	90	140	—	100	170	mW
Offset Adjustment Range		$R_P = 10k\Omega$	—	±4.0	—	—	±4.0	—	—	±4.0	—	mV

NOTES:
1. Input offset voltage measurements are performed ~ 0.5 seconds after application of power. A/E grades guaranteed fully warmed-up.
2. Long-term input offset voltage stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV — refer to typical performance curve.
3. Sample tested.
4. Guaranteed by design.
5. See test circuit and frequency response curve for 0.1Hz to 10Hz tester.
6. See test circuit for current noise measurement.
7. Guaranteed by input bias current.

ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

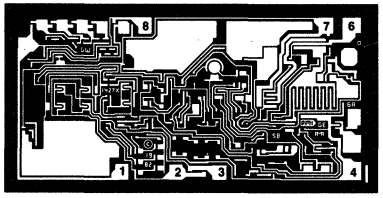
PARAMETER	SYMBOL	CONDITIONS	OP-27A MIN	OP-27A TYP	OP-27A MAX	OP-27B MIN	OP-27B TYP	OP-27B MAX	OP-27C MIN	OP-27C TYP	OP-27C MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	30	60	—	50	200	—	70	300	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2) (Note 3)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	μV/°C
Input Offset Current	I_{OS}		—	15	50	—	22	85	—	30	135	nA
Input Bias Current	I_B		—	±20	±60	—	±28	±95	—	±35	±150	nA
Input Voltage Range	IVR		±10.3	±11.5	—	±10.3	±11.5	—	±10.2	±11.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	108	122	—	100	119	—	94	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	16	—	2	20	—	4	51	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	600	1200	—	500	1000	—	300	800	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11.5	±13.5	—	±11.0	±13.2	—	±10.5	±13.0	—	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25°C \le T_A \le +85°C$ for OP-27J and OP-27Z, $0°C \le T_A \le +70°C$ for OP-27EP, FP and $-40°C \le T_A \le +85°C$ for OP-27GP, GS, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27E MIN	OP-27E TYP	OP-27E MAX	OP-27F MIN	OP-27F TYP	OP-27F MAX	OP-27G MIN	OP-27G TYP	OP-27G MAX	UNITS
Input Offset Voltage	V_{OS}		—	20	50	—	40	140	—	55	220	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2) (Note 3)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	μV/°C
Input Offset Current	I_{OS}		—	10	50	—	14	85	—	20	135	nA
Input Bias Current	I_B		—	±14	±60	—	±18	±95	—	±25	±150	nA
Input Voltage Range	IVR		±10.5	±11.8	—	±10.5	±11.8	—	±10.5	±11.8	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	110	124	—	102	121	—	96	118	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	15	—	2	16	—	2	32	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	750	1500	—	700	1300	—	450	1000	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11.7	±13.6	—	±11.4	±13.5	—	±11.0	±13.3	—	V

NOTES:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed-up.
2. The TCV_{OS} performance is within the specifications unnulled or when nulled with R_P = 8kΩ to 20kΩ. TCV_{OS} is 100% tested for A/E grades, sample tested for B/C/F/G grades.
3. Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.109 × 0.055 inch, 5995 sq. mils
(2.77 × 1.40mm, 3.88 sq. mm)

1. NULL
2. (–) INPUT
3. (+) INPUT
4. V–
6. OUTPUT
7. V+
8. NULL

For additional DICE ordering information, refer to 1990/91 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-27N, OP-27G, and OP-27GR devices; $T_A = 125°C$ for OP-27NT and OP-27GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27NT LIMIT	OP-27N LIMIT	OP-27GT LIMIT	OP-27G LIMIT	OP-27GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	60	35	200	60	100	μV MAX
Input Offset Current	I_{OS}		50	35	85	50	75	nA MAX
Input Bias Current	I_B		±60	±40	±95	±55	±80	nA MAX
Input Voltage Range	IVR		±10.3	±11	±10.3	±11	±11	V MIN
Common-Mode Rejection Ratio	CMRR	V_{CM} = IVR	108	114	100	106	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4V$ to $\pm 18V$	—	10	—	10	20	μV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 600\Omega$, $V_O = \pm 10V$	600 —	1000 800	500 —	1000 800	700 600	V/mV MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	±11.5 —	±12.0 ±10.0	±11.0 —	±12.0 ±10.0	±11.5 ±10.0	V MIN
Power Consumption	P_d	$V_O = 0$	—	140	—	140	170	mW MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

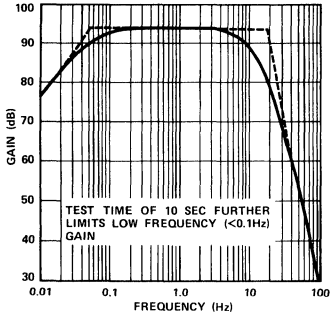
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27N TYPICAL	OP-27G TYPICAL	OP-27GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS} or TCV_{OSn}	Nulled or Unnulled R_P = 8kΩ to 20kΩ	0.2	0.3	0.4	μV/°C
Average Input Offset Current Drift	TCI_{OS}		80	130	180	pA/°C
Average Input Bias Current Drift	TCI_B		100	160	200	pA/°C
Input Noise Voltage Density	e_n	f_O = 10Hz f_O = 30Hz f_O = 1000Hz	3.5 3.1 3.0	3.5 3.1 3.0	3.8 3.3 3.2	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	f_O = 10Hz f_O = 30Hz f_O = 1000Hz	1.7 1.0 0.4	1.7 1.0 0.4	1.7 1.0 0.4	$pA/\sqrt{Hz}$
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	0.08	0.08	0.09	μVp-p
Slew Rate	SR	$R_L \geq 2k\Omega$	2.8	2.8	2.8	V/μs
Gain Bandwidth Product	GBW		8	8	8	MHz

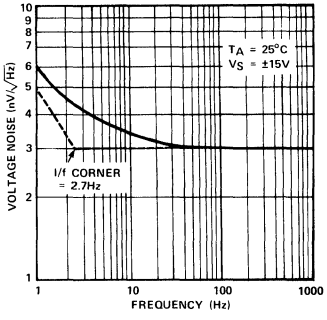
NOTE:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

TYPICAL PERFORMANCE CHARACTERISTICS

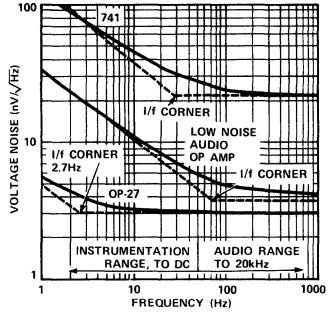
0.1Hz TO 10Hz$_{p-p}$ NOISE TESTER FREQUENCY RESPONSE



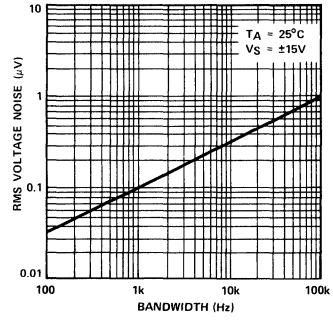
VOLTAGE NOISE DENSITY vs FREQUENCY



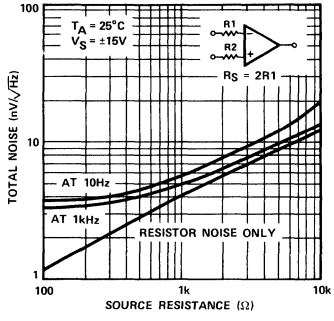
A COMPARISON OF OP AMP VOLTAGE NOISE SPECTRA



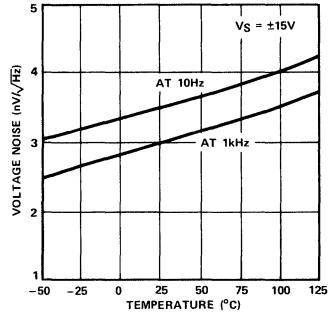
INPUT WIDEBAND VOLTAGE NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



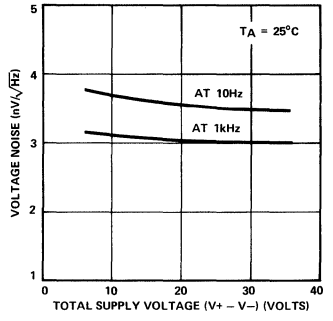
TOTAL NOISE vs SOURCE RESISTANCE



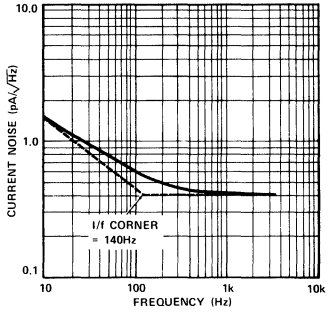
VOLTAGE NOISE DENSITY vs TEMPERATURE



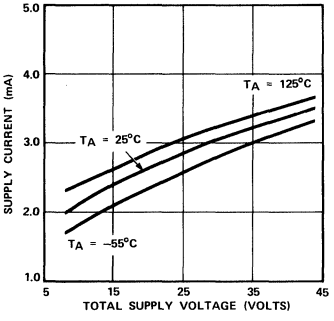
VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE



CURRENT NOISE DENSITY vs FREQUENCY

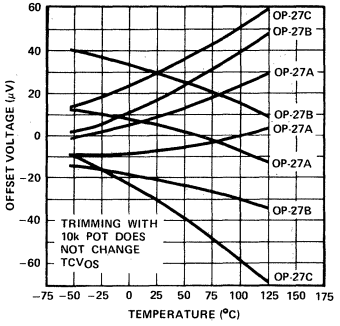


SUPPLY CURRENT vs SUPPLY VOLTAGE

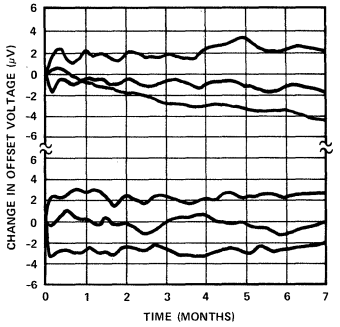


TYPICAL PERFORMANCE CHARACTERISTICS

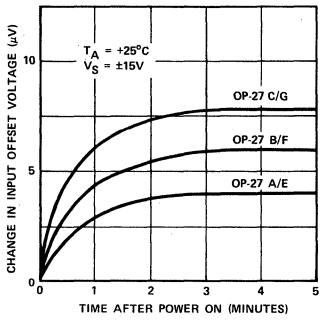
OFFSET VOLTAGE DRIFT OF EIGHT REPRESENTATIVE UNITS vs TEMPERATURE



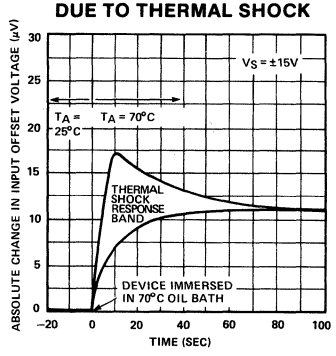
LONG-TERM OFFSET VOLTAGE DRIFT OF SIX REPRESENTATIVE UNITS



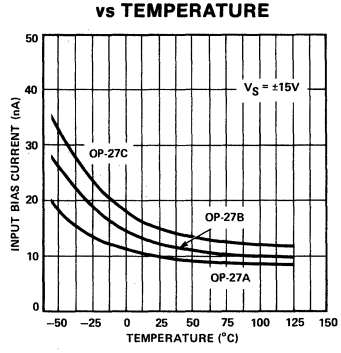
WARM-UP OFFSET VOLTAGE DRIFT



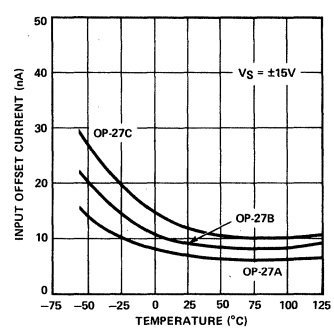
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



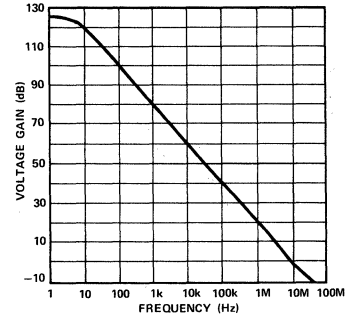
INPUT BIAS CURRENT vs TEMPERATURE



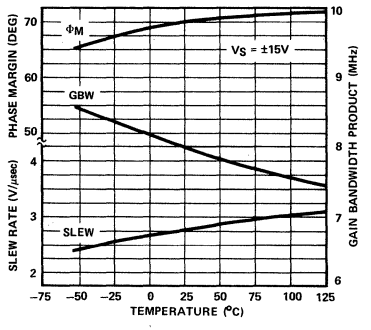
INPUT OFFSET CURRENT vs TEMPERATURE



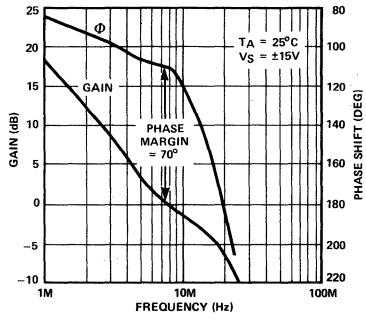
OPEN-LOOP GAIN vs FREQUENCY



SLEW RATE, GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE

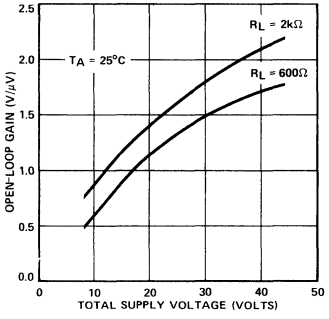


GAIN, PHASE SHIFT vs FREQUENCY

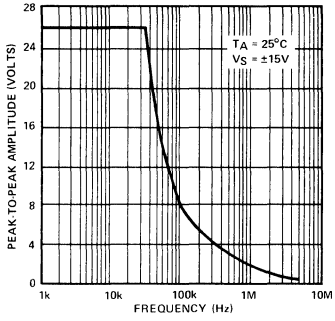


TYPICAL PERFORMANCE CHARACTERISTICS

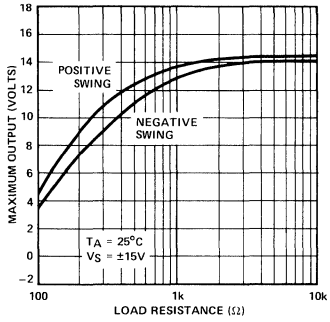
OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE



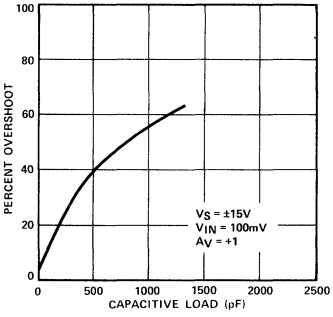
MAXIMUM OUTPUT SWING vs FREQUENCY



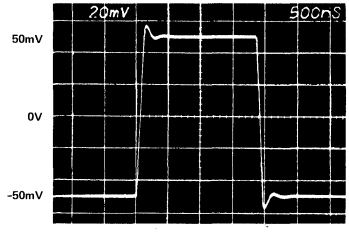
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD

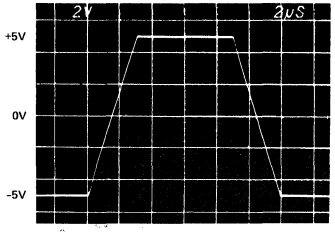


SMALL-SIGNAL TRANSIENT RESPONSE



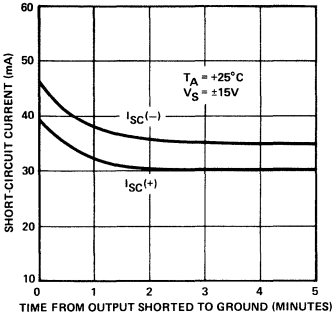
A_{VCL} = +1, C_L = 15pF
V_S = ±15V
T_A = 25°C

LARGE-SIGNAL TRANSIENT RESPONSE

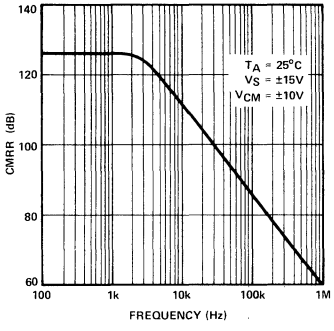


A_{VCL} = +1
V_S = ±15V
T_A = 25°C

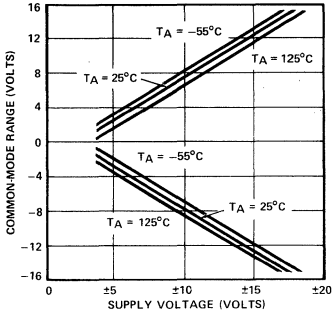
SHORT-CIRCUIT CURRENT vs TIME



CMRR vs FREQUENCY

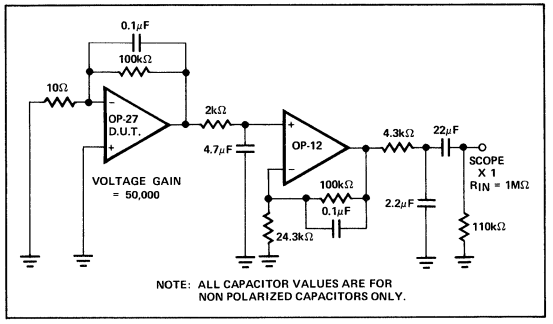


COMMON-MODE INPUT RANGE vs SUPPLY VOLTAGE

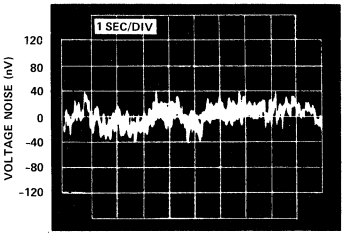


TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE NOISE TEST CIRCUIT (0.1Hz-TO-10Hz)



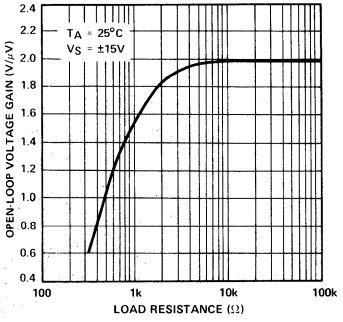
LOW-FREQUENCY NOISE



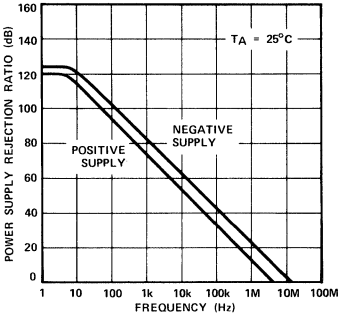
0.1Hz TO 10Hz PEAK-TO-PEAK NOISE

NOTE:
Observation time limited to 10 seconds.

OPEN-LOOP VOLTAGE GAIN vs LOAD RESISTANCE



PSRR vs FREQUENCY



APPLICATIONS INFORMATION

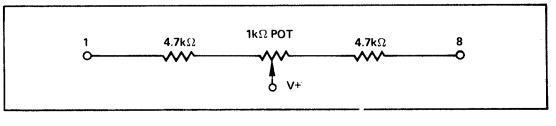
OP-27 Series units may be inserted directly into 725, OP-06, OP-07 and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, the OP-27 may be fitted to unnulled 741-type sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to ensure correct OP-27 operation. OP-27 offset voltage may be nulled to zero (or other desired setting) using a potentiometer (see Offset Nulling Circuit).

The OP-27 provides stable operation with load capacitances of up to 2000pF and ±10V swings; larger capacitances should be decoupled with a 50Ω resistor inside the feedback loop. The OP-27 is unity-gain stable.

Thermoelectric voltages generated by dissimilar metals at the input terminal contacts can degrade the drift performance. Best operation will be obtained when both input contacts are maintained at the same temperature.

OFFSET VOLTAGE ADJUSTMENT

The input offset voltage of the OP-27 is trimmed at wafer level. However, if further adjustment of V_{OS} is necessary, a 10kΩ trim potentiometer may be used. TCV_{OS} is not degraded (see Offset Nulling Circuit). Other potentiometer values from 1kΩ to 1MΩ can be used with a slight degradation (0.1 to 0.2μV/°C) of TCV_{OS}. Trimming to a value other than zero creates a drift of approximately (V_{OS}/300) μV/°C. For example, the change in TCV_{OS} will be 0.33μV/°C if V_{OS} is adjusted to 100μV. The offset-voltage adjustment range with a 10kΩ potentiometer is ±4mV. If smaller adjustment range is required, the nulling sensitivity can be reduced by using a smaller pot in conjuction with fixed resistors. For example, the network below will have a ±280μV adjustment range.



NOISE MEASUREMENTS

To measure the 80nV peak-to-peak noise specification of the OP-27 in the 0.1Hz to 10Hz range, the following precautions must be observed:

(1) The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage

typically changes 4μV due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.

(2) For similar reasons, the device has to be well-shielded from air currents. Shielding minimizes thermocouple effects.

(3) Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.

(4) The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve, the 0.1Hz corner is defined by only one zero. The test time of 10 seconds acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

(5) A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.

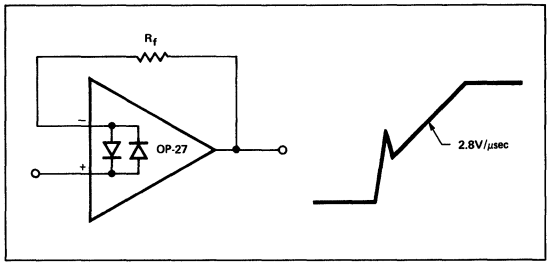
UNITY-GAIN BUFFER APPLICATIONS

When $R_f \leq 100\Omega$ and the input is driven with a fast, large signal pulse (>1V), the output waveform will look as shown in the pulsed operation diagram below.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at 10V); the amplifier will stay in its active mode and a smooth transition will occur.

When $R_f > 2k\Omega$, a pole will be created with R_f and the amplifier's input capacitance (8pF) that creates additional phase shift and reduces phase margin. A small capacitor (20 to 50pF) in parallel with R_f will eliminate this problem.

PULSED OPERATION



COMMENTS ON NOISE

The OP-27 is a very low-noise monolithic op amp. The outstanding input voltage noise characteristics of the OP-27 are achieved mainly by operating the input stage at a high quiescent current. The input bias and offset currents, which would normally increase, are held to reasonable values by the input-bias-current cancellation circuit. The OP-27A/E has I_B and I_{OS} of only ±40nA and 35nA respectively at 25°C. This is particularly important when the input has a high source-resistance. In addition, many audio amplifier designers prefer to use direct coupling. The high I_B, V_{OS}, TCV_{OS} of previous designs have made direct coupling difficult, if not impossible, to use.

Voltage noise is inversely proportional to the square-root of bias current, but current noise is proportional to the square-root of bias current. The OP-27's noise advantage disappears when high source-resistors are used. Figures 1, 2, and 3 compare OP-27 observed total noise with the noise performance of other devices in different circuit applications.

Total noise = $[(\text{Voltage noise})^2 + (\text{current noise} \times R_S)^2 + (\text{resistor noise})^2]^{1/2}$

Figure 1 shows noise-versus-source-resistance at 1000Hz. The same plot applies to wideband noise. To use this plot, just multiply the vertical scale by the square-root of the bandwidth.

NOISE vs SOURCE RESISTANCE (INCLUDING RESISTOR NOISE) AT 1000Hz.

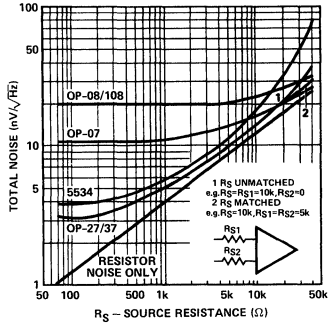


Figure 1

At $R_S < 1k\Omega$, the OP-27's low voltage noise is maintained. With $R_S > 1k\Omega$, total noise increases, but is dominated by the resistor noise rather than current or voltage noise. It is only beyond R_S of 20kΩ that current noise starts to dominate. The argument can be made that current noise is not important for applications with low-to-moderate source resistances. The crossover between the OP-27 and OP-07 and OP-08 noise occurs in the 15-to-40kΩ region.

Figure 2 shows the 0.1Hz-to-10Hz peak-to-peak noise. Here the picture is less favorable; resistor noise is negligible, current noise becomes important because it is inversely proportional to the square-root of frequency. The crossover with the OP-07 occurs in the 3-to-5kΩ range depending on whether balanced or unbalanced source resistors are used (at 3kΩ the I_B, I_{OS} error also can be three times the V_{OS} spec.).

PEAK-TO-PEAK NOISE (0.1 to 10Hz) vs SOURCE RESISTANCE (INCLUDES RESISTOR NOISE).

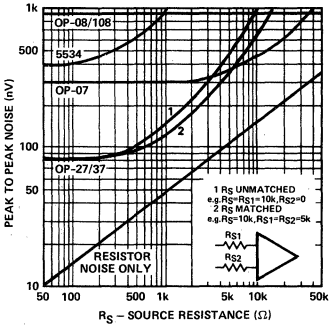


Figure 2

10Hz NOISE vs SOURCE RESISTANCE (INCLUDES RESISTOR NOISE).

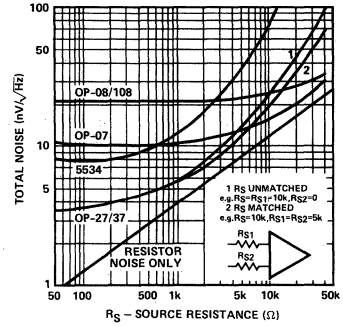


Figure 3

Therefore, for low-frequency applications, the OP-07 is better than the OP-27/37 when $R_S > 3k\Omega$. The only exception is when gain error is important. Figure 3 illustrates the 10Hz noise. As expected, the results are between the previous two figures.

For reference, typical source resistances of some signal sources are listed in Table 1.

Table 1

DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500Ω	Typically used in low-frequency applications.
Magnetic tapehead	<1500Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-27 I_B can be neglected.
Magnetic phonograph cartridges	<1500Ω	Similar need for low I_B in direct coupled applications. OP-27 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

OPEN-LOOP GAIN

FREQUENCY AT:	OP-07	OP-27	OP-37
3Hz	100dB	124dB	125dB
10Hz	100dB	120dB	125dB
30Hz	90dB	110dB	124dB

For further information regarding noise calculations, see "Minimization of Noise in Op-Amp Applications", Application Note AN-15.

AUDIO APPLICATIONS

The following applications information has been abstracted from a PMI article in the 12/20/80 issue of Electronic Design magazine and updated.

Figure 4 is an example of a phono pre-amplifier circuit using the OP-27 for A_1; R_1-R_2-C_1-C_2 form a very accurate RIAA network with standard component values. The popular method to accomplish RIAA phono equalization is to employ frequency-dependent feedback around a high-quality gain block. Properly chosen, an RC network can provide the three necessary time constants of 3180, 318, and 75μs.[1]

For initial equalization accuracy and stability, precision metal-film resistors and film capacitors of polystyrene or polypropylene are recommended since they have low voltage coefficients, dissipation factors, and dielectric absorption.[4] (High-K ceramic capacitors should be avoided here, though low-K ceramics—such as NPO types, which have excellent dissipation factors, and somewhat lower dielectric absorption—can be considered for small values.)

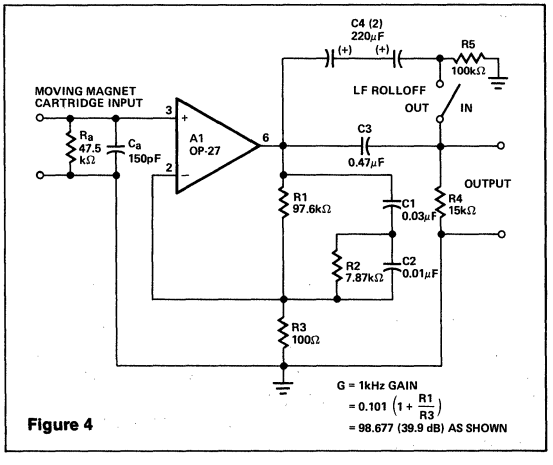


Figure 4

The OP-27 brings a 3.2nV/$\sqrt{Hz}$ voltage noise and 0.45 pA/$\sqrt{Hz}$ current noise to this circuit. To minimize noise from other sources, R_3 is set to a value of 100Ω, which generates a voltage noise of 1.3nV/$\sqrt{Hz}$. The noise increases the 3.2nV/$\sqrt{Hz}$ of the amplifier by only 0.7dB. With a 1kΩ source, the circuit noise measures 63dB below a 1mV reference level, unweighted, in a 20kHz noise bandwidth.

Gain (G) of the circuit at 1kHz can be calculated by the expression:

$$G = 0.101\ (1 + \frac{R_1}{R_3})$$

For the values shown, the gain is just under 100 (or 40dB). Lower gains can be accommodated by increasing R_3, but gains higher than 40dB will show more equalization errors because of the 8MHz gain-bandwidth of the OP-27.

This circuit is capable of very low distortion over its entire range, generally below 0.01% at levels up to 7V rms. At 3V output levels, it will produce less than 0.03% total harmonic distortion at frequencies up to 20kHz.

Capacitor C_3 and resistor R_4 form a simple −6dB-per-octave rumble filter, with a corner at 22Hz. As an option, the switch-selected shunt capacitor C_4, a nonpolarized electrolytic, bypasses the low-frequency rolloff. Placing the rumble filter's high-pass action after the preamp has the desirable result of discriminating against the RIAA-amplified low-frequency noise components and pickup-produced low-frequency disturbances.

A preamplifier for NAB tape playback is similar to an RIAA phono preamp, though more gain is typically demanded, along with equalization requiring a heavy low-frequency boost. The circuit in Fig. 4 can be readily modified for tape use, as shown by Fig. 5.

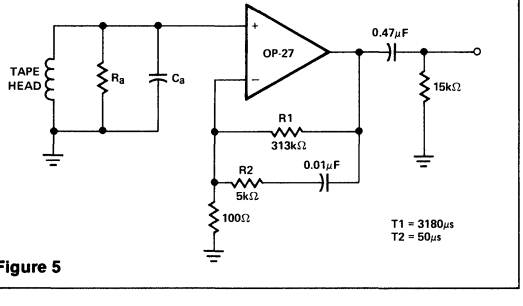


Figure 5

While the tape-equalization requirement has a flat high-frequency gain above 3kHz ($T_2 = 50\mu s$), the amplifier need not be stabilized for unity gain. The decompensated OP-37 provides a greater bandwidth and slew rate. For many applications, the idealized time constants shown may require trimming of R_1 and R_2 to optimize frequency response for nonideal tape-head performance and other factors.[5]

The network values of the configuration yield a 50dB gain at 1kHz, and the dc gain is greater than 70dB. Thus, the worst-case output offset is just over 500mV. A single 0.47μF output capacitor can block this level without affecting the dynamic range.

The tape head can be coupled directly to the amplifier input, since the worst-case bias current of 80nA with a 400mH, 100 μin. head (such as the PRB2H7K) will not be troublesome.

One potential tape-head problem is presented by amplifier bias-current transients which can magnetize a head. The OP-27 and OP-37 are free of bias-current transients upon power up or power down. However, it is always advantageous to control the speed of power supply rise and fall, to eliminate transients.

In addition, the dc resistance of the head should be carefully controlled, and preferably below 1kΩ. For this configuration, the bias-current-induced offset voltage can be greater than the 100μV maximum offset if the head resistance is not sufficiently controlled.

A simple, but effective, fixed-gain transformerless microphone preamp (Fig. 6) amplifies differential signals from low-impedance microphones by 50dB, and has an input impedance of 2kΩ. Because of the high working gain of the circuit, an OP-37 helps to preserve bandwidth, which will be 110kHz. As the OP-37 is a decompensated device (minimum stable gain of 5), a dummy resistor, R_p, may be necessary, if the microphone is to be unplugged. Otherwise the 100% feedback from the open input may cause the amplifier to oscillate.

Common-mode input-noise rejection will depend upon the match of the bridge-resistor ratios. Either close-tolerance (0.1%) types should be used, or R_4 should be trimmed for best CMRR. All resistors should be metal-film types for best stability and low noise.

Noise performance of this circuit is limited more by the input resistors R_1 and R_2 than by the op amp, as R_1 and R_2 each generate a 4nV/$\sqrt{Hz}$ noise, while the op amp generates a 3.2nV/$\sqrt{Hz}$ noise. The rms sum of these predominant noise sources will be about 6nV/$\sqrt{Hz}$, equivalent to 0.9μV in a 20kHz noise bandwidth, or nearly 61dB below a 1mV input signal. Measurements confirm this predicted performance.

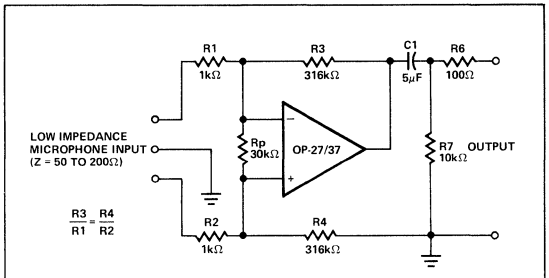


Figure 6

For applications demanding appreciably lower noise, a high-quality microphone-transformer-coupled preamp (Fig. 7) incorporates the internally-compensated OP-27. T_1 is a JE-115K-E 150Ω/15kΩ transformer which provides an optimum source resistance for the OP-27 device. The circuit has an overall gain of 40dB, the product of the transformer's voltage setup and the op amp's voltage gain.

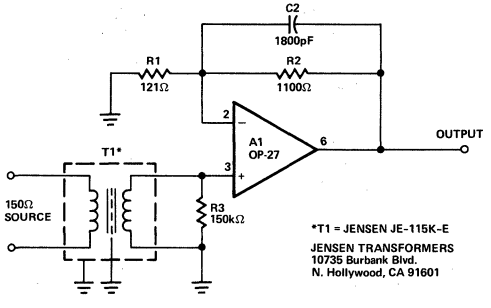


Figure 7

Gain may be trimmed to other levels, if desired, by adjusting R_2 or R_1. Because of the low offset voltage of the OP-27, the output offset of this circuit will be very low, 1.7mV or less, for a 40dB gain. The typical output blocking capacitor can be eliminated in such cases, but is desirable for higher gains to eliminate switching transients.

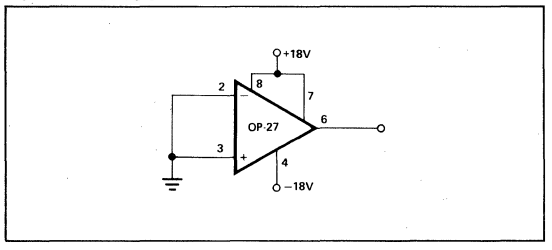
Capacitor C_2 and resistor R_2 form a 2μs time constant in this circuit, as recommended for optimum transient response by the transformer manufacturer. With C_2 in use, A_1 must have unity-gain stability. For situations where the 2μs time constant is not necessary, C_2 can be deleted, allowing the faster OP-37 to be employed.

Some comment on noise is appropriate to understand the capability of this circuit. A 150Ω resistor and R_1 and R_2 gain resistors connected to a noiseless amplifier will generate 220 nV of noise in a 20kHz bandwidth, or 73dB below a 1mV reference level. Any practical amplifier can only approach this noise level; it can never exceed it. With the OP-27 and T_1 specified, the additional noise degradation will be close to 3.6dB (or −69.5 referenced to 1mV).

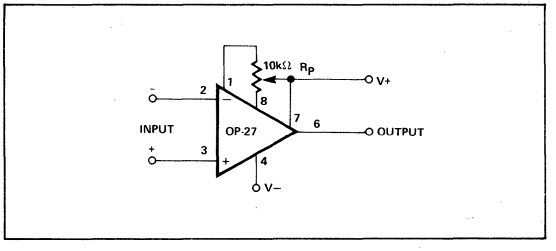
References

1. Lipshitz, S.P., "On RIAA Equalization Networks," *JAES*, Vol. 27, June 1979, p. 458-481.
2. Jung, W.G., *IC Op Amp Cookbook*, 2nd Ed., H.W. Sams and Company, 1980.
3. Jung, W.G., *Audio IC Op Amp Applications*, 2nd Ed., H.W. Sams and Company, 1978.
4. Jung, W.G., and Marsh, R.M., "Picking Capacitors," *Audio*, February & March, 1980.
5. Otala, M., "Feedback-Generated Phase Nonlinearity in Audio Amplifiers," London AES Convention, March 1980, preprint 1976.
6. Stout, D.F., and Kaufman, M., *Handbook of Operational Amplifier Circuit Design*, New York, McGraw Hill, 1976.

BURN-IN CIRCUIT



OFFSET NULLING CIRCUIT



ANALOG DEVICES

Low Noise Precision High Speed Operational Amplifier ($A_{VCL} \geq 5$)

OP-37

FEATURES

- **Low Noise ..... 80nV p-p (0.1Hz to 10Hz)**
  ..... 3nV/$\sqrt{Hz}$ at 1kHz
- **Low Drift ..... 0.2μV/°C**
- **High Speed ..... 17V/μs Slew Rate**
  ..... 63MHz Gain Bandwidth
- **Low Input Offset Voltage 10μV**
- **Excellent CMRR ... 126dB (Common-Voltage of ±11V)**
- **High Open-Loop Gain ..... 1.8 Million**
- **Replaces 725, OP-05, OP-06, OP-07, AD510, AD517, SE5534 in Gains >5**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (µV)	PACKAGE TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
25	OP37AJ*	OP37AZ*	–	–	MIL
25	OP37EJ	OP37EZ	OP37EP	–	IND/COM
60	OP37BJ*	OP37BZ*	–	OP37BRC/883	MIL
60	OP37FJ	OP37FZ	OP37FP	–	IND/COM
100	OP37CJ*	OP37CZ	–	–	MIL
100	OP37GJ	OP37GZ	OP37GP	–	XIND
100	–	–	OP37GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO package, contact your local sales office.

GENERAL DESCRIPTION

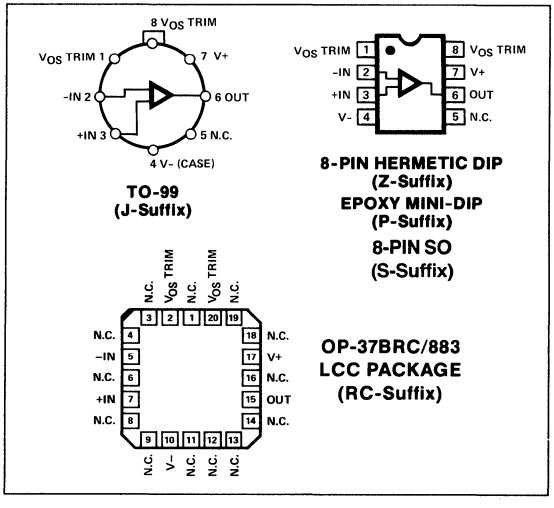
The OP-37 provides the same high performance as the OP-27, but the design is optimized for circuits with gains greater than five. This design change increases slew rate to 17V/μsec and gain-bandwidth product to 63MHz.

The OP-37 provides the low offset and drift of the OP-07 plus higher speed and lower noise. Offsets down to 25μV and drift of 0.6μV/°C maximum make the OP-37 ideal for precision instrumentation applications. Exceptionally low noise (e_n=3.5nV/$\sqrt{Hz}$ at 10Hz), a low 1/f noise corner frequency of 2.7Hz, and the high gain of 1.8 million, allow accurate high-gain amplification of low-level signals.

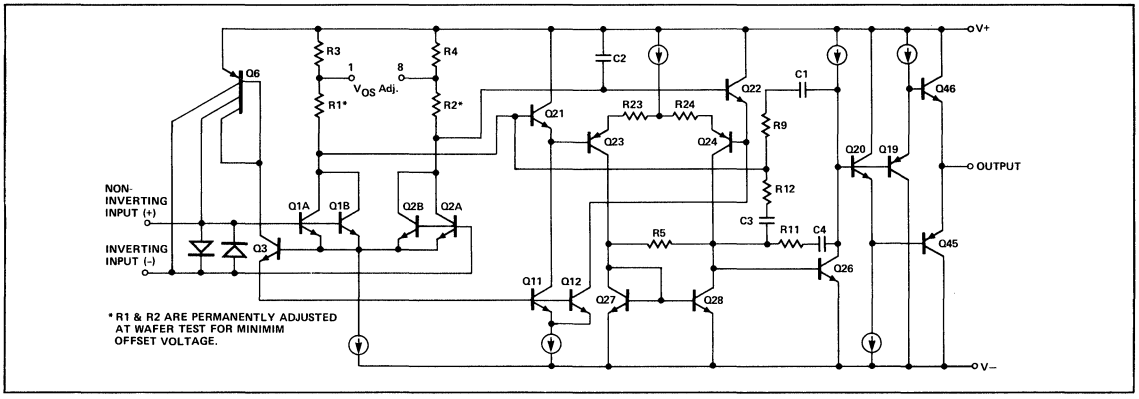
The low input bias current of ±10nA and offset current of 7nA are achieved by using a bias-current-cancellation circuit. Over the military temperature range this typically holds I_B and I_{OS} to ±20nA and 15nA respectively.

The output stage has good load driving capability. A guaranteed swing of ±10V into 600Ω and low output distortion make the OP-37 an excellent choice for professional audio applications.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



PSRR and CMRR exceed 120dB. These characteristics, coupled with long-term drift of 0.2μV/month, allow the circuit designer to achieve performance levels previously attained only by discrete designs.

Low-cost, high-volume production of the OP-37 is achieved by using on-chip zener-zap trimming. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history.

The OP-37 brings low-noise instrumentation-type performance to such diverse applications as microphone, tape-head, and RIAA phono preamplifiers, high-speed signal conditioning for data acquisition systems, and wide-bandwidth instrumentation.

ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage ..... ±22V
Internal Voltage (Note 1) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Differential Input Voltage (Note 2) ..... ±0.7V
Differential Input Current (Note 2) ..... ±25mA
Storage Temperature Range ..... –65°C to +150°C

Operating Temperature Range
OP-37A, OP-37B, OP-37C (J, Z, RC) ..... –55°C to +125°C
OP-37E, OP-37F (J, Z) ..... –25°C to +85°C
OP-37E, OP-37F (P) ..... 0°C to +70°C
OP-37G (P, S, J, Z) ..... –40°C to +85°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (NOTE 3)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC, TC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. The OP-37's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.
4. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-37A/E			OP-37B/F			OP-37C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	10	25	—	20	60	—	30	100	μV
Long-Term V_{OS} Stability	V_{OS}/Time	(Notes 2, 3)	—	0.2	1.0	—	0.3	1.5	—	0.4	2.0	μV/Mo
Input Offset Current	I_{OS}		—	7	35	—	9	50	—	12	75	nA
Input Bias Current	I_B		—	±10	±40	—	±12	±55	—	±15	±80	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Notes 3, 5)	—	0.08	0.18	—	0.08	0.18	—	0.09	0.25	μVp-p
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 3)	—	3.5	5.5	—	3.5	5.5	—	3.8	8.0	nV/√Hz
		f_O = 30Hz (Note 3)	—	3.1	4.5	—	3.1	4.5	—	3.3	5.6	
		f_O = 1000Hz (Note 3)	—	3.0	3.8	—	3.0	3.8	—	3.2	4.5	
Input Noise Current Density	i_n	f_O = 10Hz (Notes 3, 6)	—	1.7	4.0	—	1.7	4.0	—	1.7	—	pA/√Hz
		f_O = 30Hz (Notes 3, 6)	—	1.0	2.3	—	1.0	2.3	—	1.0	—	
		f_O = 1000Hz (Notes 3, 6)	—	0.4	0.6	—	0.4	0.6	—	0.4	0.6	
Input Resistance — Differential-Mode	R_{IN}	(Note 7)	1.3	6	—	0.94	5	—	0.7	4	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	3	—	—	2.5	—	—	2	—	GΩ
Input Voltage Range	IVR		±11.0	±12.3	—	±11.0	±12.3	—	±11.0	±12.3	—	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±11V	114	126	—	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSSR	V_S = ±4V to ±18V	—	1	10	—	1	10	—	2	20	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	1000	1800	—	1000	1800	—	700	1500	—	V/mV
		$R_L \geq 1k\Omega$, V_O = ±10V	800	1500	—	800	1500	—	400	1500	—	
		$R_L = 600\Omega$, V_O = ±1V, V_S = ±4V, (Note 4)	250	700	—	250	700	—	200	500	—	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±13.8	—	±12.0	±13.8	—	±11.5	±13.5	—	V
		$R_L \geq 600\Omega$	±10.0	±11.5	—	±10.0	±11.5	—	±10.0	±11.5	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 4)	11	17	—	11	17	—	11	17	—	V/μs
Gain Bandwidth Prod.	GBW	f_O = 10kHz (Note 4)	45	63	—	45	63	—	45	63	—	MHz
		f_O = 1MHz	—	40	—	—	40	—	—	40	—	

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-37A/E MIN	OP-37A/E TYP	OP-37A/E MAX	OP-37B/F MIN	OP-37B/F TYP	OP-37B/F MAX	OP-37C/G MIN	OP-37C/G TYP	OP-37C/G MAX	UNITS
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	70	—	—	70	—	—	70	—	Ω
Power Consumption	P_d	$V_O = 0$	—	90	140	—	90	140	—	100	170	mW
Offset Adjustment Range		$R_P = 10k\Omega$	—	±4.0	—	—	±4.0	—	—	±4.0	—	mV

NOTES:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed up.
2. Long-term input offset voltage stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV — refer to typical performance curve.
3. Sample tested.
4. Guaranteed by design.
5. See test circuit and frequency response curve for 0.1Hz to 10Hz tester.
6. See test circuit for current noise measurement.
7. Guaranteed by input bias current.

ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-37A MIN	OP-37A TYP	OP-37A MAX	OP-37B MIN	OP-37B TYP	OP-37B MAX	OP-37C MIN	OP-37C TYP	OP-37C MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	30	60	—	50	200	—	70	300	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2) (Note 3)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	μV/°C
Input Offset Current	I_{OS}		—	15	50	—	22	85	—	30	135	nA
Input Bias Current	I_B		—	±20	±60	—	±28	±95	—	±35	±150	nA
Input Voltage Range	IVR		±10.3	±11.5	—	±10.3	±11.5	—	±10.2	±11.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	108	122	—	100	119	—	94	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	16	—	2	20	—	4	51	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	600	1200	—	500	1000	—	300	800	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11.5	±13.5	—	±11.0	±13.2	—	±10.5	±13.0	—	V

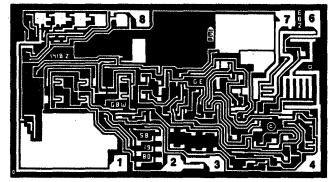
ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-25°C \le T_A \le +85°C$ for OP-37EJ/FJ and OP-37EZ/FZ, $0°C \le T_A \le +70°C$ for OP-37EP/FP and $-40°C \le T_A \le +85°$ for OP-37GP/GS/GJ/GZ, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-37E MIN	OP-37E TYP	OP-37E MAX	OP-37F MIN	OP-37F TYP	OP-37F MAX	OP-37G MIN	OP-37G TYP	OP-37G MAX	UNITS
Input Offset Voltage	V_{OS}		—	20	50	—	40	140	—	55	220	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2) (Note 3)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	μV/°C
Input Offset Current	I_{OS}		—	10	50	—	14	85	—	20	135	nA
Input Bias Current	I_B		—	±14	±60	—	±18	±95	—	±25	±150	nA
Input Voltage Range	IVR		±10.5	±11.8	—	±10.5	±11.8	—	±10.5	±11.8	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	110	124	—	102	121	—	96	118	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	15	—	2	16	—	2	32	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	750	1500	—	700	1300	—	450	1000	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11.7	±13.6	—	±11.4	±13.5	—	±11.0	±13.3	—	V

NOTES:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed up.
2. The TCV_{OS} performance is within the specifications unnulled or when nulled with $R_P = 8k\Omega$ to $20k\Omega$. TCV_{OS} is 100% tested for A/E grades, sample tested for B/C/F/G grades.
3. Guaranteed by design.

DICE CHARACTERISTICS

DIE SIZE 0.098 × 0.056 inch, 5488 sq. mils
(2.49 × 1.42 mm, 3.54 sq. mm)



1. NULL
2. (–) INPUT
3. (+) INPUT
4. V–
6. OUTPUT
7. V+
8. NULL

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-37N, OP-37G and OP-37GR devices; $T_A = 125°C$ for OP-37NT and OP-37GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-37NT LIMIT	OP-37N LIMIT	OP-37GT LIMIT	OP-37G LIMIT	OP-37GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	60	35	200	60	100	μV MAX
Input Offset Current	I_{OS}		50	35	85	50	75	nA MAX
Input Bias Current	I_B		±60	±40	±95	±55	±80	nA MAX
Input Voltage Range	IVR		±10.3	±11	±10.3	±11	±11	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11V$	108	114	100	106	100	dB MIN
Power Supply Rejection Ratio	PSRR	$T_A = 25°C$, $V_S = \pm 4V$ to $\pm 18V$ $T_A = 125°C$, $V_S = \pm 4.5V$ to $\pm 18V$	10 16	10 —	10 20	10 —	20 —	μV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 1k\Omega$, $V_O = \pm 10V$	600 —	1000 800	500 —	1000 800	700 —	V/mV MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	±11.5 —	±12.0 ±10.0	±11.0 —	±12.0 ±10.0	±11.5 ±10.0	V MIN
Power Consumption	P_d	$V_O = 0$	—	140	—	140	170	mW MAX

NOTES:
For 25° C characteristics of OP-37NT and OP-37GT devices, see OP-37N and OP-37G characteristics, respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot asembly and testing.

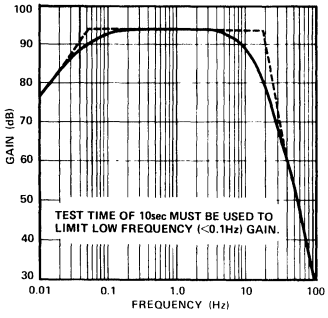
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-37NT TYPICAL	OP-37N TYPICAL	OP-37GT TYPICAL	OP-37G TYPICAL	OP-37GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS} or TCV_{OSn}	Nulled or Unnulled $R_P = 8k\Omega$ to $20k\Omega$	0.2	0.2	0.3	0.3	0.4	μV/°C
Average Input Offset Current Drift	TCI_{OS}		80	80	130	130	180	pA/°C
Average Input Bias Current Drift	TCI_B		100	100	160	160	200	pA/°C
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 30Hz$ $f_O = 1000Hz$	3.5 3.1 3.0	3.5 3.1 3.0	3.5 3.1 3.0	3.5 3.1 3.0	3.8 3.3 3.2	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	$f_O = 10Hz$ $f_O = 30Hz$ $f_O = 1000Hz$	1.7 1.0 0.4	1.7 1.0 0.4	1.7 1.0 0.4	1.7 1.0 0.4	1.7 1.0 0.4	$pA/\sqrt{Hz}$
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	0.08	0.08	0.08	0.08	0.09	μV_{P-P}
Slew Rate	SR	$R_L \geq 2k\Omega$	17	17	17	17	17	V/μs
Gain Bandwidth Product	GBW	$f_O = 10kHz$	63	63	63	63	63	MHz

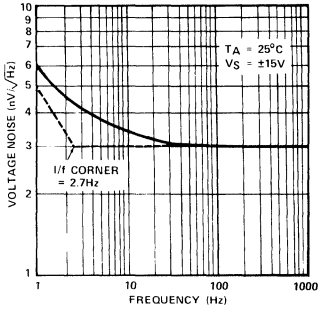
NOTE:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

TYPICAL PERFORMANCE CHARACTERISTICS

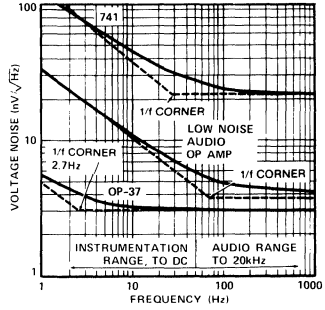
NOISE-TESTER FREQUENCY RESPONSE (0.1Hz TO 10Hz)



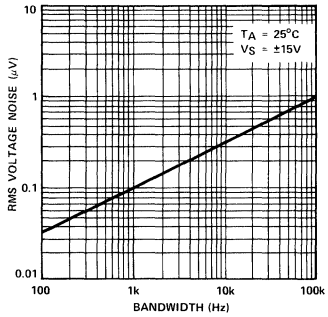
VOLTAGE NOISE DENSITY vs FREQUENCY



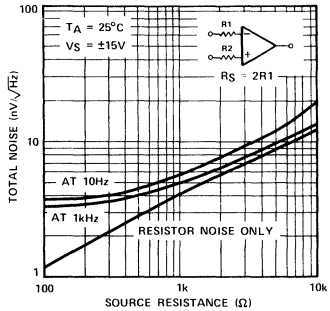
A COMPARISON OF OP AMP VOLTAGE NOISE SPECTRA



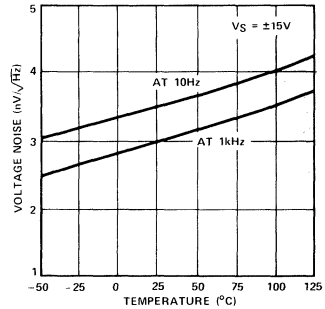
INPUT WIDEBAND VOLTAGE NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



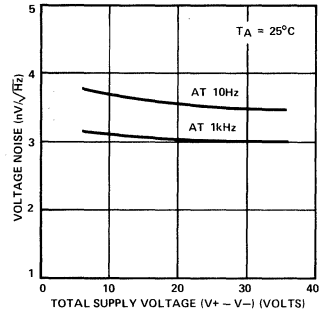
TOTAL NOISE vs SOURCE RESISTANCE



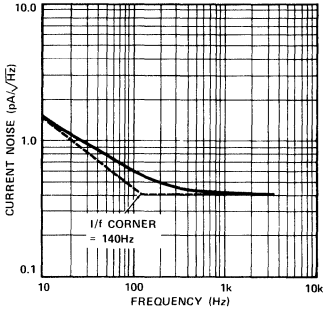
VOLTAGE NOISE DENSITY vs TEMPERATURE



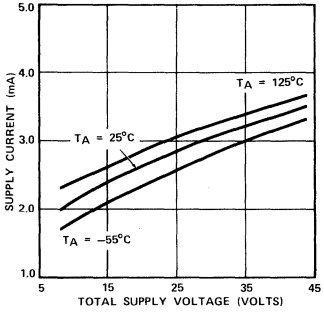
VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE



CURRENT NOISE DENSITY vs FREQUENCY

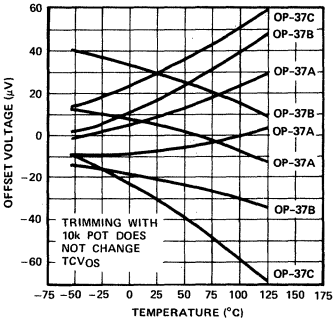


SUPPLY CURRENT vs SUPPLY VOLTAGE

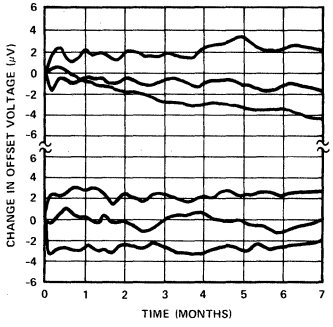


TYPICAL PERFORMANCE CHARACTERISTICS

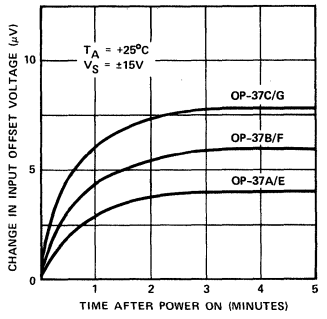
OFFSET VOLTAGE DRIFT OF EIGHT REPRESENTATIVE UNITS vs TEMPERATURE



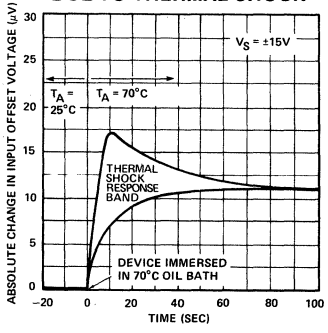
LONG-TERM OFFSET VOLTAGE DRIFT OF SIX REPRESENTATIVE UNITS



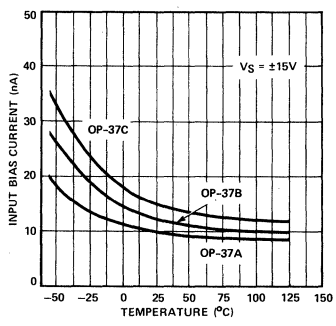
WARM-UP OFFSET VOLTAGE DRIFT



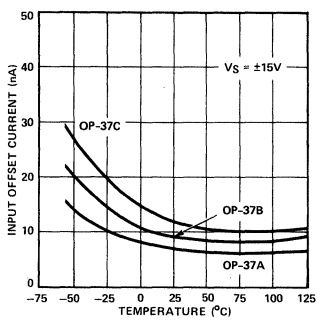
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



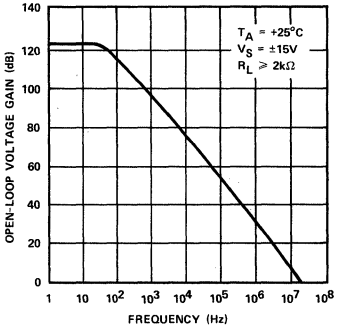
INPUT BIAS CURRENT vs TEMPERATURE



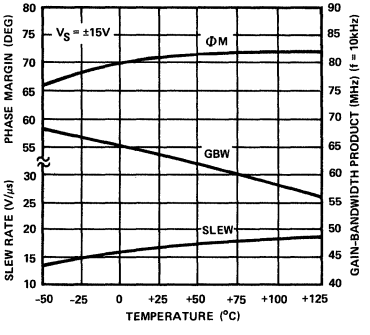
INPUT OFFSET CURRENT vs TEMPERATURE



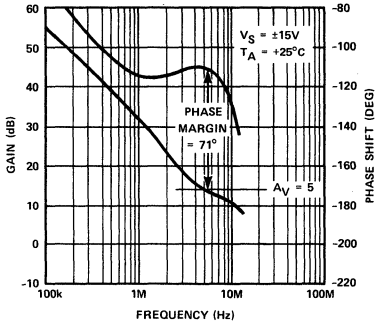
OPEN-LOOP GAIN vs FREQUENCY



SLEW RATE, GAIN BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE

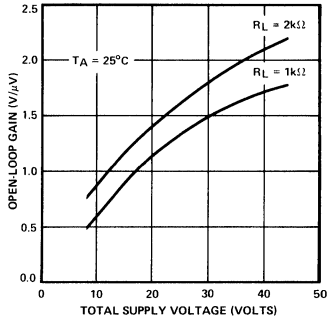


GAIN, PHASE SHIFT vs FREQUENCY

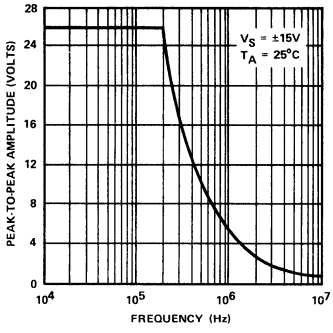


TYPICAL PERFORMANCE CHARACTERISTICS

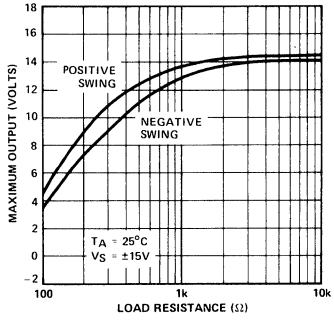
OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE



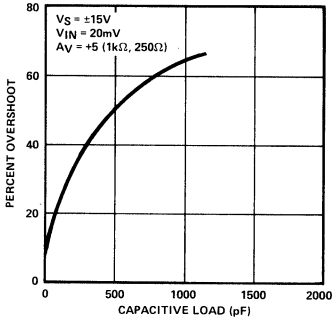
MAXIMUM OUTPUT SWING vs FREQUENCY



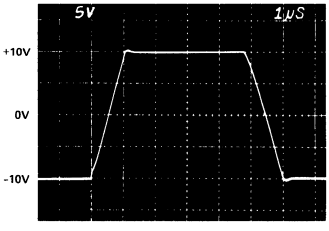
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD

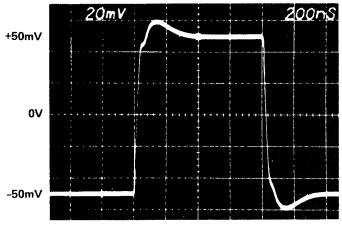


LARGE-SIGNAL TRANSIENT RESPONSE



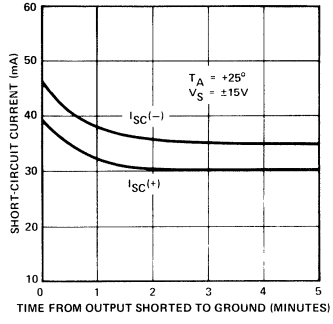
V_S = ±15V
A_V = +5 (1kΩ, 250Ω)
T_A = +25°C

SMALL-SIGNAL TRANSIENT RESPONSE

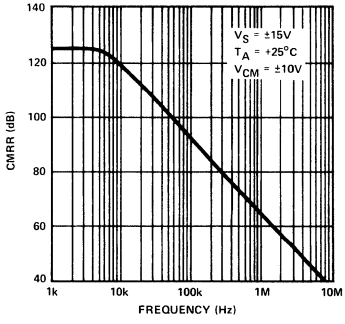


V_S = ±15V
A_V = +5 (1kΩ, 250Ω)
T_A = +25°C

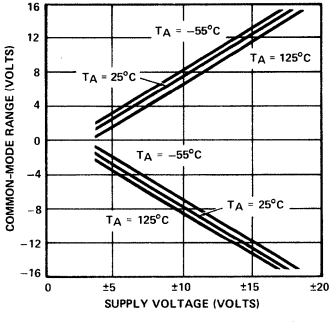
SHORT-CIRCUIT CURRENT vs TIME



CMRR vs FREQUENCY

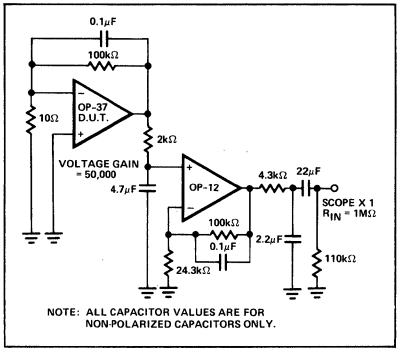


COMMON-MODE INPUT RANGE vs SUPPLY VOLTAGE

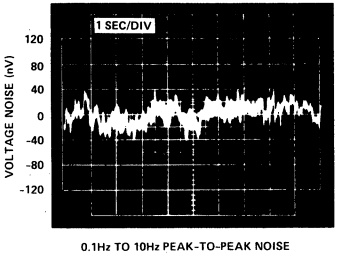


TYPICAL PERFORMANCE CHARACTERISTICS

NOISE TEST CIRCUIT (0.1Hz TO 10Hz)



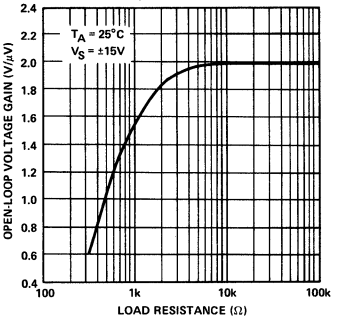
LOW-FREQUENCY NOISE



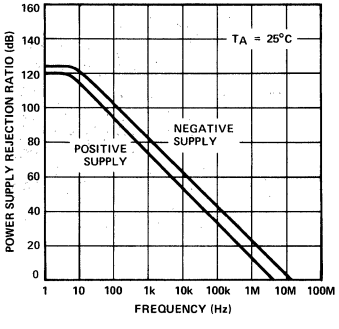
0.1Hz TO 10Hz PEAK-TO-PEAK NOISE

NOTE:
Observation time limited to 10 seconds.

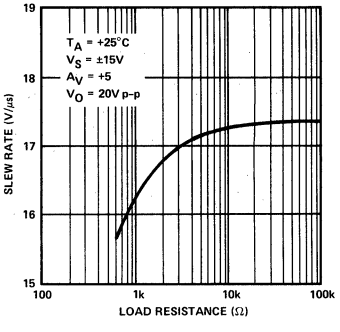
OPEN-LOOP VOLTAGE GAIN vs LOAD RESISTANCE



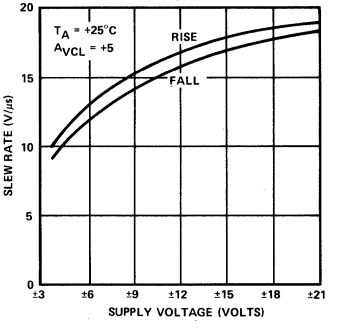
PSRR vs FREQUENCY



SLEW RATE vs LOAD



SLEW RATE vs SUPPLY VOLTAGE



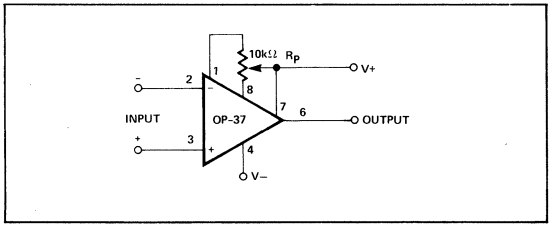
APPLICATIONS INFORMATION

OP-37 Series units may be inserted directly into 725, OP-06, OP-07, and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, the OP-37 may be fitted to unnulled 741-type sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to ensure correct OP-37 operation. OP-37 offset voltage may be nulled to zero (or other desired setting) using a potentiometer (see offset nulling circuit).

The OP-37 provides stable operation with load capacitances of up to 1000pF and ±10V swings; larger capacitances should be decoupled with a 50Ω resistor inside the feedback loop. Closed-loop gain must be at least five. For closed-loop gain between five to ten, the designer should consider both the OP-27 and the OP-37. For gains above ten, the OP-37 has a clear advantage over the unity-gain-stable OP-27.

Thermoelectric voltages generated by dissimilar metals at the input terminal contacts can degrade the drift performance. Best operation will be obtained when both input contacts are maintained at the same temperature.

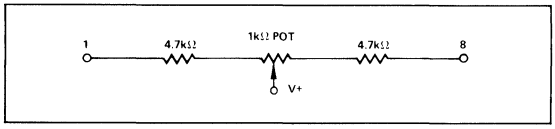
OFFSET NULLING CIRCUIT



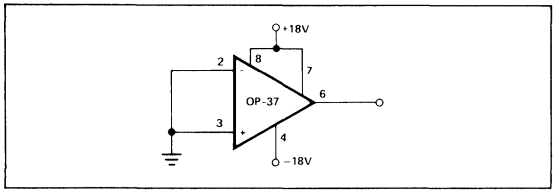
OFFSET VOLTAGE ADJUSTMENT

The input offset voltage of the OP-37 is trimmed at wafer level. However, if further adjustment of V_{OS} is necessary, a 10kΩ trim potentiometer may be used. TCV_{OS} is not degraded (see offset nulling circuit). Other potentiometer values from 1kΩ to 1MΩ can be used with a slight degradation (0.1 to 0.2μV/°C) of TCV_{OS}. Trimming to a value other than zero creates a drift of approximately (V_{OS}/300) μV/°C. For exam-

ple, the change in TCV_{OS} will be 0.33μV/° C if V_{OS} is adjusted to 100μV. The offset-voltage adjustment range with a 10kΩ potentiometer is ±4mV. If smaller adjustment range is required, the nulling sensitivity can be reduced by using a smaller pot in conjunction with fixed resistors. For example, the network below will have a ±280μV adjustment range.



BURN-IN CIRCUIT



NOISE MEASUREMENTS

To measure the 80nV peak-to-peak noise specification of the OP-37 in the 0.1Hz to 10Hz range, the following precautions must be observed:

(1) The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 4μV due to increasing chip temperature after power-up. In the 10 second measurement interval, these temperature-induced effects can exceed tens-of- nanovolts.

(2) For similar reasons, the device has to be well-shielded from air currents. Shielding minimizes thermocouple effects.

(3) Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.

(4) The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency response curve, the 0.1Hz corner is defined by only one zero. The test time of 10 seconds acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

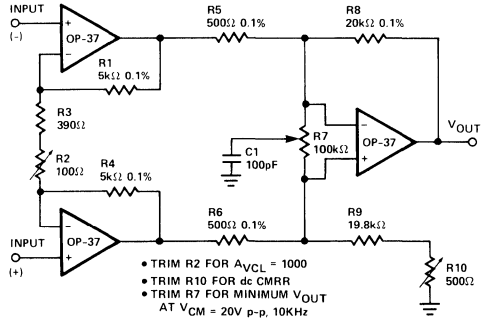
(5) A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.

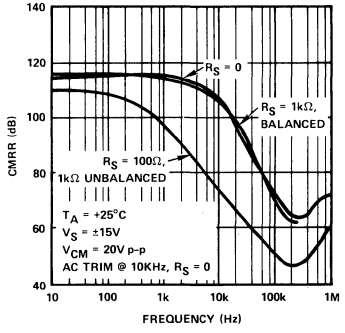
OPTIMIZING LINEARITY

Best linearity will be obtained by designing for the minimum output current required for the application. High gain and excellent linearity can be achieved by operating the op amp with a peak output current of less than ±10mA.

INSTRUMENTATION AMPLIFIER

A three-op-amp instrumentation amplifier provides high gain and wide bandwidth. The input noise of the circuit below is $4.9nV/\sqrt{Hz}$. The gain of the input stage is set at 25 and the gain of the second stage is 40; overall gain is 1000. The amplifier bandwidth of 800kHz is extraordinarily good for a precision instrumentation amplifier. Set to a gain of 1000, this yields a gain-bandwidth product of 800MHz. The full-power bandwidth for a $20V_{p-p}$ output is 250kHz. Potentiometer R7 provides quadrature trimming to optimize the instrumentation amplifier's AC common-mode rejection.





COMMENTS ON NOISE

The OP-37 is a very low-noise monolithic op amp. The outstanding input voltage noise characteristics of the OP-37 are achieved mainly by operating the input stage at a high quiescent current. The input bias and offset currents, which would normally increase, are held to reasonable values by the input-bias-current cancellation circuit. The OP-37A/E has I_B and I_{OS} of only ±40nA and 35nA respectively at 25° C. This is particularly important when the input has a high source-resistance. In addition, many audio amplifier designers

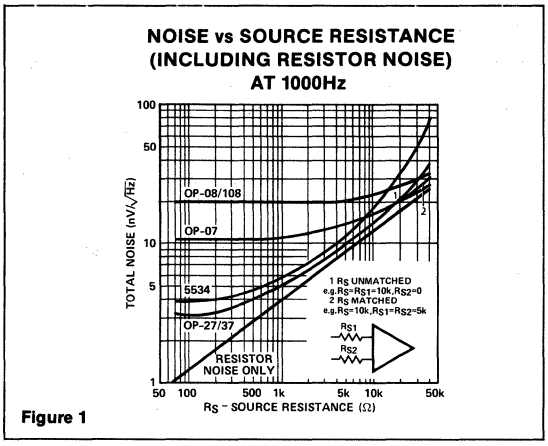


Figure 1

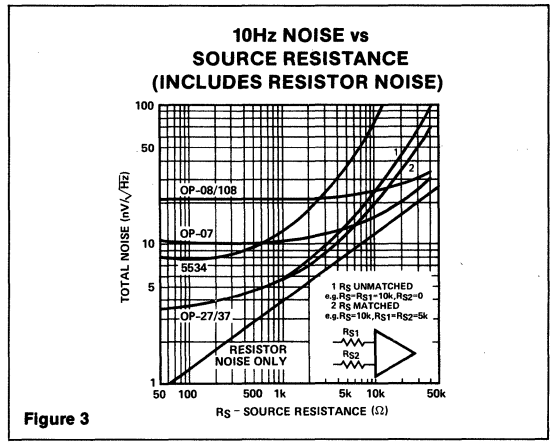


Figure 3

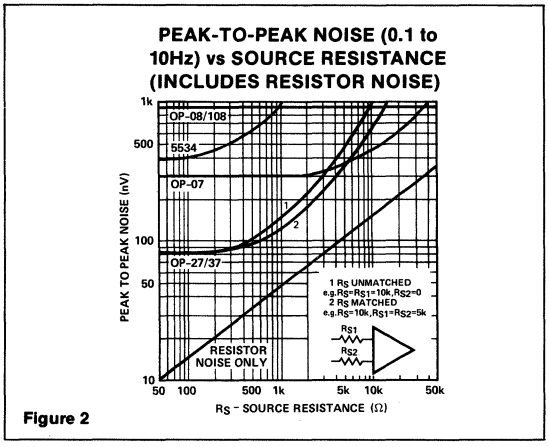


Figure 2

prefer to use direct coupling. The high I_B, TCV_{OS} of previous designs have made direct coupling difficult, if not impossible, to use.

Voltage noise is inversely proportional to the square-root of bias current, but current noise is proportional to the square-root of bias current. The OP-37's noise advantage disappears when high source-resistors are used. Figures 1, 2, and 3 compare OP-37 observed total noise with the noise performance of other devices in different circuit applications.

Total noise = $[(\text{Voltage noise})^2 + (\text{current noise} \times R_S)^2 + (\text{resistor noise}^2)]^{1/2}$

Figure 1 shows noise-versus-source-resistance at 1000Hz. The same plot applies to wideband noise. To use this plot, just multiply the vertical scale by the square-root of the bandwidth.

At R_S<1kΩ, the OP-37's low voltage noise is maintained. With R_S< 1kΩ, total noise increases, but is dominated by the resistor noise rather than current or voltage noise. It is only beyond R_S of 20kΩ that current noise starts to dominate. The argument can be made that current noise is not important for applications with low-to-moderate source resistances. The crossover between the OP-37 and OP-07 and OP-08 noise occurs in the 15-to-40kΩ region.

Figure 2 shows the 0.1Hz-to-10Hz peak-to-peak noise. Here the picture is less favorable; resistor noise is negligible, current noise becomes important because it is inversely proportional to the square-root of frequency. The crossover with the OP-07 occurs in the 3-to 5kΩ range depending on whether balanced or unbalanced source resistors are used (at 3kΩ the I_B, I_{OS} error also can be three times the V_{OS} spec.).

Therefore, for low-frequency applications, the OP-07 is better than the OP-27/37 when R_S > 3kΩ. The only exception is when gain error is important. Figure 3 illustrates the 10Hz noise. As expected, the results are between the previous two figures.

For reference, typical source resistances of some signal sources are listed in Table 1.

Table 1

DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500Ω	Typically used in low-frequency applications.
Magnetic tapehead	<1500Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-37 I_B can be neglected.
Magnetic phonograph cartridges	<1500Ω	Similar need for low I_B in direct coupled applications. OP-37 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

AUDIO APPLICATIONS

The following applications information has been abstracted from a PMI article in the 12/20/80 issue of Electronic Design magazine and updated.

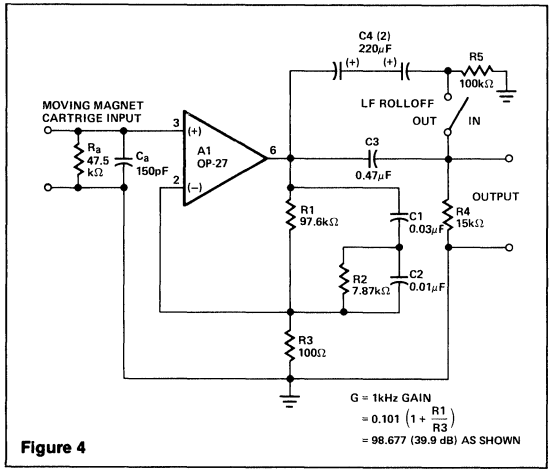


Figure 4

Figure 4 is an example of a phono pre-amplifier circuit using the OP-27 for A_1; R_1-R_2-C_1-C_2 form a very accurate RIAA network with standard component values. The popular method to accomplish RIAA phono equalization is to employ frequency-dependent feedback around a high-quality gain block. Properly chosen, an RC network can provide the three necessary time constants of 3180, 318, and 75μs.[1]

For initial equalization accuracy and stability, precision metal-film resistors and film capacitors of polystyrene or polypropylene are recommended since they have low voltage coefficients, dissipation factors, and dielectric absorption.[4] (High-K ceramic capacitors should be avoided here, though low-K ceramics—such as NPO types, which have excellent dissipation factors, and somewhat lower dielectric absorption — can be considered for small values or where space is at a premium.)

The OP-27 brings a $3.2nV/\sqrt{Hz}$ voltage noise and 0.45 $pA/\sqrt{Hz}$ current noise to this circuit. To minimize noise from other sources, R_3 is set to a value of 100Ω, which generates a voltage noise of $1.3nV/\sqrt{Hz}$. The noise increases the $3.2nV/\sqrt{Hz}$ of the amplifier by only 0.7dB. With a 1kΩ source, the circuit noise measures 63dB below a 1mV reference level, unweighted, in a 20kHz noise bandwidth.

Gain (G) of the circuit at 1kHz can be calculated by the expression:

$$G = 0.101\ (1 + \frac{R_1}{R_3})$$

For the values shown, the gain is just under 100 (or 40dB). Lower gains can be accommodated by increasing R_3, but gains higher than 40dB will show more equalization errors because of the 8MHz gain-bandwidth of the OP-27.

This circuit is capable of very low distortion over its entire range, generally below 0.01% at levels up to 7V rms. At 3V output levels, it will produce less than 0.03% total harmonic distortion at frequencies up to 20kHz.

Capacitor C_3 and resistor R_4 form a simple –6dB-per-octave rumble filter, with a corner at 22Hz. As an option, the switch-selected shunt capacitor C_4, a nonpolarized electrolytic, bypasses the low-frequency rolloff. Placing the rumble filter's high-pass action after the preamp has the desirable result of discriminating against the RIAA-amplified low-frequency noise components and pickup-produced low-frequency disturbances.

A preamplifier for NAB tape playback is similar to an RIAA phono preamp, though more gain is typically demanded, along with equalization requiring a heavy low-frequency boost. The circuit in Fig. 4 can be readily modified for tape use, as shown by Fig. 5.

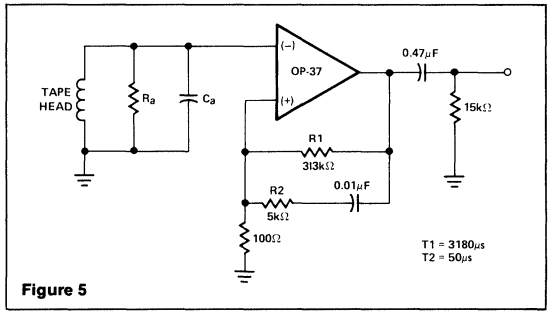


Figure 5

While the tape-equalization requirement has a flat high-frequency gain above 3kHz ($T_2 = 50\mu s$), the amplifier need not be stabilized for unity gain. The decompensated OP-37 provides a greater bandwidth and slew rate. For many applications, the idealized time constants shown may require trimming of R_1 and R_2 to optimize frequency response for nonideal tape-head performance and other factors.[5]

The network values of the configuration yield a 50dB gain at 1kHz, and the dc gain is greater than 70dB. Thus, the worst-case output offset is just over 500mV. A single 0.47μF output capacitor can block this level without affecting the dynamic range.

The tape head can be coupled directly to the amplifier input, since the worst-case bias current of 85nA with a 400mH, 100 μin. head (such as the PRB2H7K) will not be troublesome.

One potential tape-head problem is presented by amplifier bias-current transients which can magnetize a head. The OP-27 and OP-37 are free of bias-current transients upon power up or power down. However, it is always advantageous to control the speed of power supply rise and fall, to eliminate transients.

In addition, the dc resistance of the head should be carefully controlled, and preferably below 1kΩ. For this configuration, the bias-current-induced offset voltage can be greater than the 170μV maximum offset if the head resistance is not sufficiently controlled.

A simple, but effective, fixed-gain transformerless microphone preamp (Fig. 6) amplifies differential signals from low-impedance microphones by 50dB, and has an input impedance of 2kΩ. Because of the high working gain of the circuit, an OP-37 helps to preserve bandwidth, which will be 110kHz. As the OP-37 is a decompensated device (minimum stable gain of 5), a dummy resistor, R_p, may be necessary, if the microphone is to be unplugged. Otherwise the 100% feedback from the open input may cause the amplifier to oscillate.

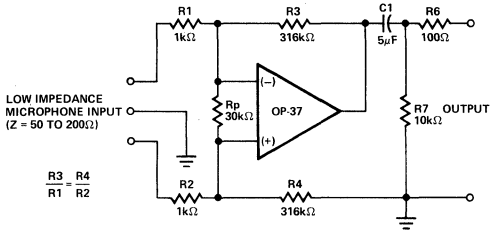


Figure 6

Common-mode input-noise rejection will depend upon the match of the bridge-resistor ratios. Either close-tolerance (0.1%) types should be used, or R_4 should be trimmed for best CMRR. All resistors should be metal-film types for best stability and low noise.

Noise performance of this circuit is limited more by the input resistors R_1 and R_2 than by the op amp, as R_1 and R_2 each generate a $4nV/\sqrt{Hz}$ noise, while the op amp generates a $3.2nV/\sqrt{Hz}$ noise. The rms sum of these predominant noise sources will be about $6nV/\sqrt{Hz}$, equivalent to 0.9μV in a 20kHz noise bandwidth, or nearly 61dB below a 1mV input signal. Measurements confirm this predicted performance.

For applications demanding appreciably lower noise, a high-quality microphone-transformer-coupled preamp (Fig. 7) incorporates the internally compensated OP-27. T_1 is a JE-115K-E 150Ω/15kΩ transformer which provides an optimum source resistance for the OP-27 device. The circuit has an overall gain of 40dB, the product of the transformer's voltage setup and the op amp's voltage gain.

Gain may be trimmed to other levels, if desired, by adjusting R_2 or R_1. Because of the low offset voltage of the OP-27, the output offset of this circuit will be very low, 1.7mV or less, for a

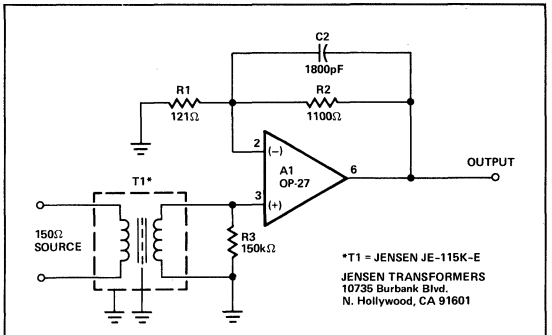


Figure 7

40dB gain. The typical output blocking capacitor can be eliminated in such cases, but is desirable for higher gains to eliminate switching transients.

Capacitor C_2 and resistor R_2 form a 2μs time constant in this circuit, as recommended for optimum transient response by the transformer manufacturer. With C_2 in use, A_1 must have unity-gain stability. For situations where the 2μs time constant is not necessary, C_2 can be deleted, allowing the faster OP-37 to be employed.

Some comment on noise is appropriate to understand the capability of this circuit. A 150Ω resistor and R_1 and R_2 gain resistors connected to a noiseless amplifier will generate 220 nV of noise in a 20kHz bandwidth, or 73dB below a 1mV reference level. Any practical amplifier can only approach this noise level; it can never exceed it. With the OP-27 and T_1 specified, the additional noise degradation will be close to 3.6dB (or −69.5 referenced to 1mV).

References

1. Lipshitz, S.P., "On RIAA Equalization Networks," *JAES*, Vol. 27, June 1979, p. 458-481.
2. Jung, W.G., *IC Op Amp Cookbook*, 2nd Ed., H.W. Sams and Company, 1980.
3. Jung, W.G., *Audio IC Op Amp Applications*, 2nd Ed., H.W. Sams and Company, 1978.
4. Jung, W.G., and Marsh, R.M., "Picking Capacitors," *Audio*, February & March, 1980.
5. Otala, M., "Feedback-Generated Phase Nonlinearity in Audio Amplifiers," London AES Convention, March 1980, preprint 1976.
6. Stout, D.F., and Kaufman, M., *Handbook of Operational Amplifier Circuit Design*, New York, McGraw Hill, 1976.

Wide-Bandwidth Precision Operational Amplifier ($A_V \geq 10$)

OP-61

FEATURES

- **High Gain-Bandwidth Product ..... 200MHz Typ**
- **Low Voltage Noise ..... 3.4nV/$\sqrt{Hz}$ @ 1kHz**
- **High Speed ..... 45V/μs Typ**
- **Fast Settling Time (0.01%) ..... 330ns Typ**
- **High Gain ..... 475V/mV Typ**
- **Low Offset Voltage ..... 100μV Typ**

APPLICATIONS

- **Low Noise Preamplifier**
- **Wideband Signal Conditioning**
- **Pulse/RF Amplifiers**
- **Wideband Instrumentation Amplifiers**
- **Active Filters**
- **Fast Summing Amplifiers**

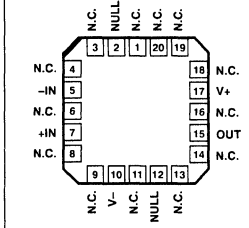
GENERAL DESCRIPTION

The OP-61 is a wide-bandwidth, precision operational amplifier designed to meet the requirements of fast, precision instrumentation systems. The OP-61's combination of DC accuracy with high bandwidth, fast slew rate and low noise, makes it unique among high-speed amplifiers. It is ideal for wideband systems requiring high signal-to-noise ratio, such as fast 12-16 bit data acquisition systems. The OP-61 maintains less than 3nV/$\sqrt{Hz}$ of input referred spot voltage noise over its closed-loop bandwidth.

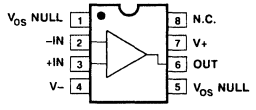
The OP-61 offers noise and gain performance similar to that of the industry standard OP-27/37 amplifiers, but maintains a much larger gain-bandwith product of 200MHz. With slew rate exceeding 45V/μs, and settling time for 12 bits (0.01%) typically 330ns, the OP-61 has excellent dynamic accuracy.

The OP-61 is an excellent upgrade for circuits using slower op amps such as the HA-5111, and the HA-5147. The OP-61 can also be used as a high-speed alternative to the HA-5101, HA-5127, HA-5137, OP-27, and OP-37 amplifiers, where closed-loop gains are greater than 10.

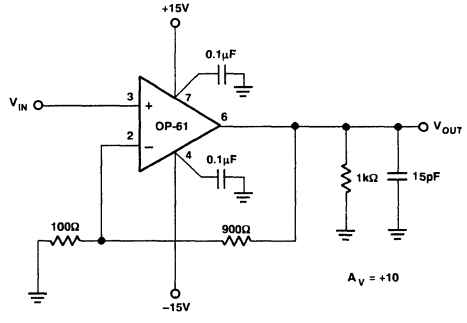
PIN CONNECTIONS

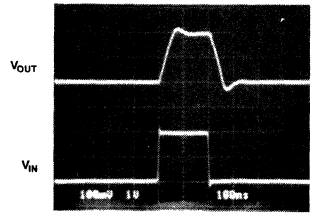


OP-61 ARC/883
20-CONTACT LCC
(RC-Suffix)



EPOXY MINI-DIP
(P-Suffix)
8-PIN CERDIP (Z-Suffix)
8-PIN SO (S-Suffix)





ORDERING INFORMATION †

PACKAGE			OPERATING TEMPERATURE RANGE
CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	
OP61AZ*	–	OP61ARC/883*	MIL
OP61FZ	OP61GP	–	XIND
–	OP61GS	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, and plastic DIP packages.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±18V
Differential Input Voltage ..... ±5.0V
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous

Storage Temperature Range
P, RC, S, Z Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_j) ..... 150°C
Operating Temperature Range
All A Grades ..... –55°C to +125°C
F & G Grades ..... –40°C to +85°C

PACKAGE TYPE	Θ_{jA} (Note 1)	Θ_{jC}	UNIT
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{jA} is specified for device soldered to printed circuit board for SOpackage.
2. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

			OP-61A			OP-61F			OP-61G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		–	100	500	–	150	750	–	200	1000	µV
Input Offset Current	I_{OS}	$V_{CM} = 0V$	–	30	150	–	40	200	–	40	200	nA
Input Bias Current	I_B	$V_{CM} = 0V$	–	130	500	–	200	600	–	200	600	nA
Input Noise Voltage Density	e_n	$f_O = 1000Hz$	–	3.4	–	–	3.4	–	–	3.4	–	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	$f_O = 10kHz$	–	1.7	–	–	1.7	–	–	1.7	–	$pA/\sqrt{Hz}$
Input Voltage Range	IVR	(Note 1)	±11.0	–	–	±11.0	–	–	±11.0	–	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm11V$	100	108	–	94	100	–	94	100	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm5V$ to ±18V	–	1.2	4.0	–	2.0	5.6	–	2.0	5.6	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$ $R_L = 2k\Omega$ $R_L = 1k\Omega$	225 200 150	475 400 340	– – –	175 150 120	425 350 300	– – –	175 150 120	425 350 300	– – –	V/mV
Output Voltage Swing	V_O	$R_L = 1k\Omega$ $R_L = 500\Omega$	±12.0 ±11.0	±13.2 ±12.8	– –	±12.0 ±11.0	±13.2 ±12.8	– –	±12.0 ±11.0	±13.2 ±12.8	– –	V
Slew Rate	SR	$R_L = 1k\Omega$ $C_L = 50pF$	40	45	–	35	45	–	35	45	–	V/µs
Gain Bandwidth Prod.	GBWP	$f_O = 1MHz$	–	200	–	–	200	–	–	200	–	MHz
SettlingTime	t_s	$A_V = -10$, 10V Step, 0.01%	–	300	–	–	330	–	–	330	–	ns
Supply Current	I_{SY}	No Load	–	6.1	7.5	–	6.1	7.5	–	6.1	7.5	mA

NOTES:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –55°C ≤ T_A ≤ +125°C, unless otherwise noted.

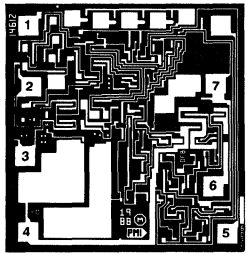
PARAMETER	SYMBOL	CONDITIONS	OP-61A MIN	OP-61A TYP	OP-61A MAX	UNITS
Input Offset Voltage	V_{OS}		–	200	1000	µV
Average Input Offset Drift	TCV_{OS}		–	1.0	5.0	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0V	–	70	400	nA
Input Bias Current	I_B	V_{CM} = 0V	–	180	800	nA
Input Voltage Range	IVR	(Note 1)	±11V	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	94	104	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±18V	–	2.0	5.6	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 10kΩ R_L = 2kΩ R_L = 1kΩ	175 150 120	400 340 260	– – –	V/mV
Output Voltage Swing	V_O	R_L ≥ 1kΩ R_L = 500Ω	±11.0 ±10.0	±13.0 ±12.7	– –	V
Supply Current	I_{SY}	No Load	–	6.5	8.0	mA

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –40°C ≤ T_A ≤ +85°C.

PARAMETER	SYMBOL	CONDITIONS	OP-61F MIN	OP-61F TYP	OP-61F MAX	OP-61G MIN	OP-61G TYP	OP-61G MAX	UNITS
Input Offset Voltage	V_{OS}		–	300	1250	–	400	1500	µV
Average Input Offset Drift	TCV_{OS}		–	3.0	7.0	–	3.0	7.0	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0V	–	125	500	–	125	500	nA
Input Bias Current	I_B	V_{CM} = 0V	–	250	900	–	250	900	nA
Input Voltage Range	IVR	(Note 1)	±11V	–	–	±11V	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	88	96	–	88	96	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±18V	–	4.0	10.0	–	4.0	10.0	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 10kΩ R_L = 2kΩ R_L = 1kΩ	150 120 100	350 300 240	– – –	150 120 100	350 300 240	– – –	V/mV
Output Voltage Swing	V_O	R_L = 1kΩ R_L = 500Ω	±11.0 ±10.0	±13.0 ±12.7	– –	±11.0 ±10.0	±13.0 ±12.7	– –	V
Supply Current	I_{SY}	No Load	–	6.4	8.0	–	6.4	8.0	mA

NOTES:
1. Guaranteed by CMR test.

DICE CHARACTERISTICS



DIE SIZE 0.064 x 0.068 inch, 4,352 sq. mils (1.63 x 1.73 mm, 2.81 sq. mm)

1. V_{OS} NULL
2. –IN
3. +IN
4. V–
5. V_{OS} NULL
6. OUT
7. V+

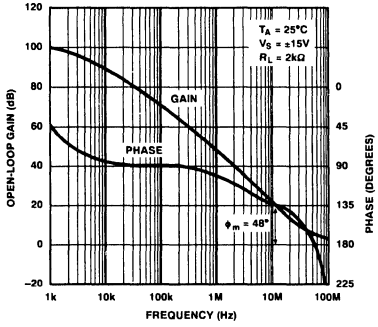
WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	OP-61GBC LIMITS	UNITS
Input Offset Voltage	V_{OS}		750	µV MAX
Input Offset Current	I_{OS}		200	nA MAX
Input Bias Current	I_B		600	nA MAX
Input Voltage Range	IVR		±11.0	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	94	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 18V$	5.6	µV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$ $R_L = 2k\Omega$ $R_L = 1k\Omega$	175 150 120	V/mV MIN
Output Voltage Swing	V_O	$R_L = 1k\Omega$ $R_L = 500\Omega$	±12.0 ±11.0	V MIN
Slew Rate	SR	$R_L = 1k\Omega$ $C_L = 50pF$	35	V/µs MIN
Supply Current	I_{SY}	No Load	7.5	mA MAX

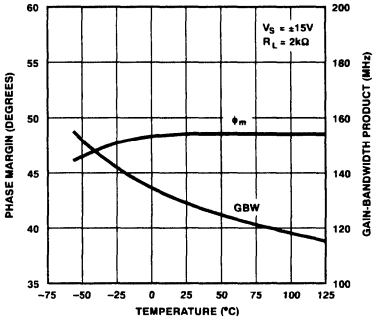
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

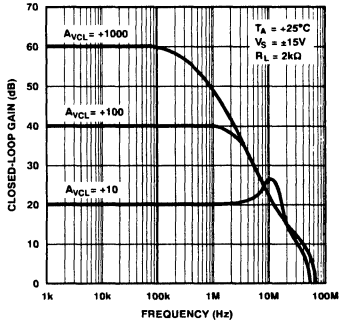
OPEN-LOOP GAIN, PHASE vs FREQUENCY



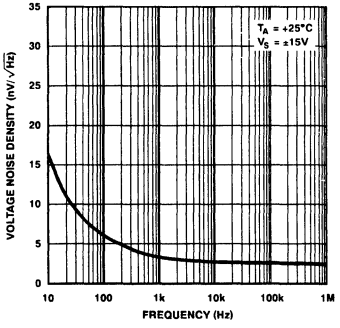
GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE



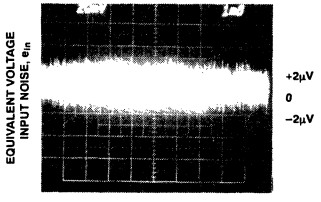
CLOSED-LOOP GAIN vs FREQUENCY



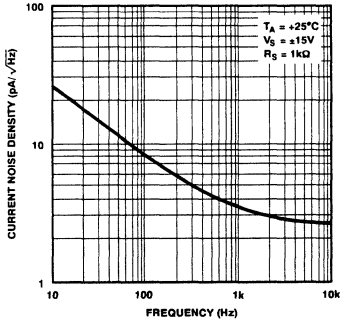
VOLTAGE NOISE DENSITY vs FREQUENCY



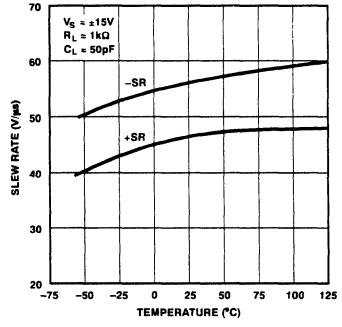
WIDEBAND PEAK-TO-PEAK VOLTAGE NOISE



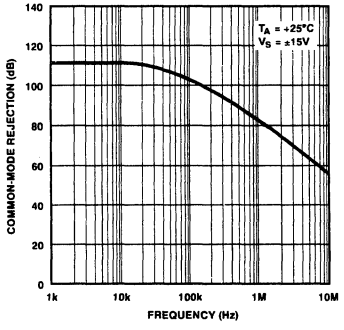
CURRENT NOISE DENSITY vs FREQUENCY



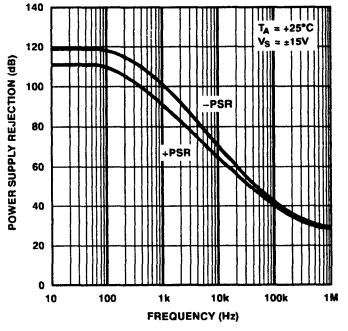
SLEW RATE vs TEMPERATURE



COMMON-MODE REJECTION vs FREQUENCY

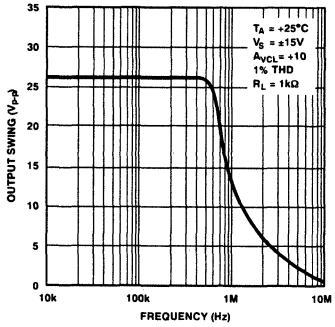


POWER SUPPLY REJECTION vs FREQUENCY

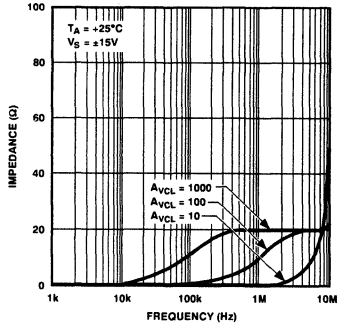


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

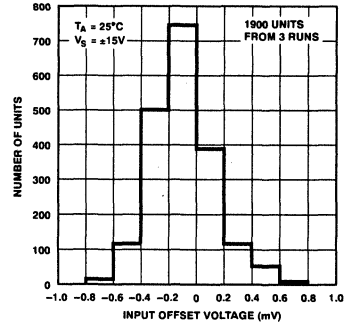
MAXIMUM OUTPUT SWING vs FREQUENCY



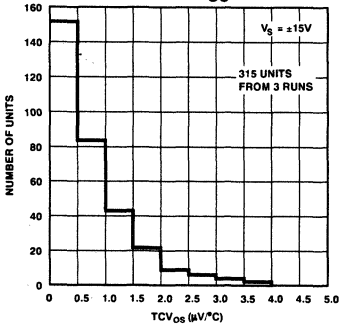
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



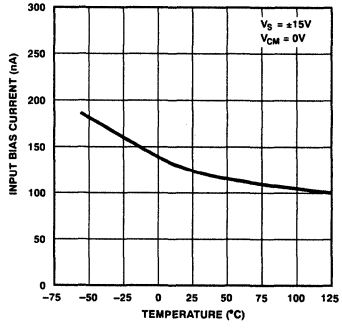
TYPICAL DISTRIBUTION OF INPUT OFFSET VOLTAGE



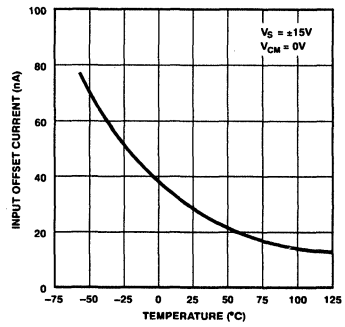
TYPICAL DISTRIBUTION OF TCV_{OS}



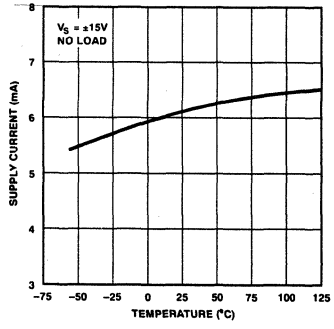
INPUT BIAS CURRENT vs TEMPERATURE



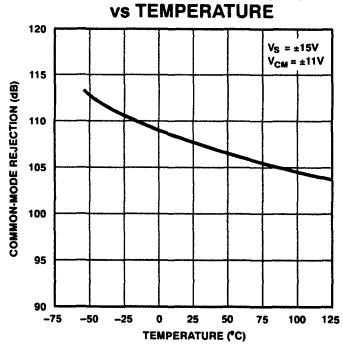
INPUT OFFSET CURRENT vs TEMPERATURE



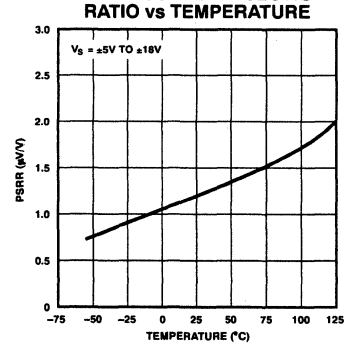
SUPPLY CURRENT vs TEMPERATURE



COMMON-MODE REJECTION vs TEMPERATURE

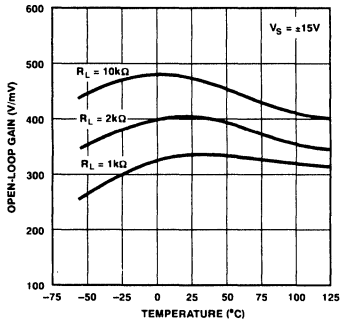


POWER SUPPLY REJECTION RATIO vs TEMPERATURE

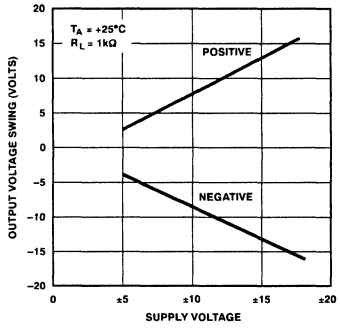


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

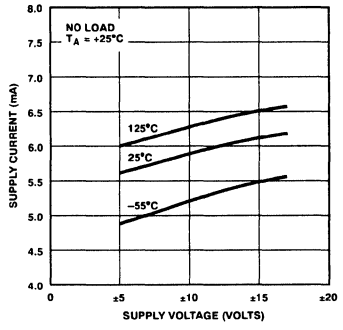
OPEN-LOOP GAIN vs TEMPERATURE



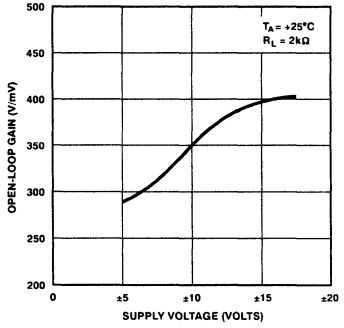
OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE



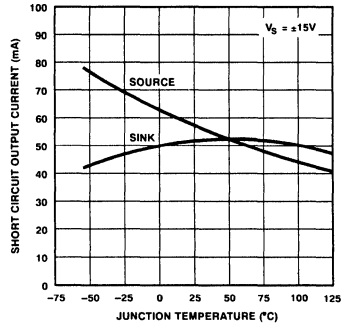
SUPPLY CURRENT vs SUPPLY VOLTAGE



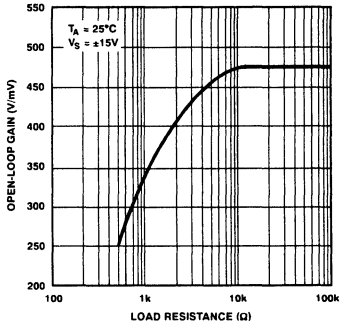
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



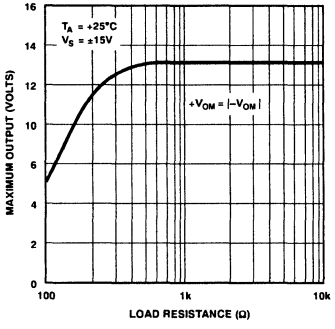
SHORT CIRCUIT OUTPUT CURRENT vs JUNCTION TEMPERATURE



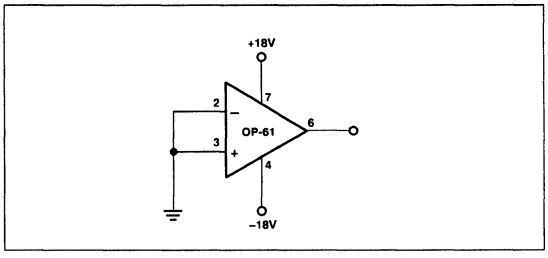
OPEN-LOOP GAIN vs LOAD RESISTANCE



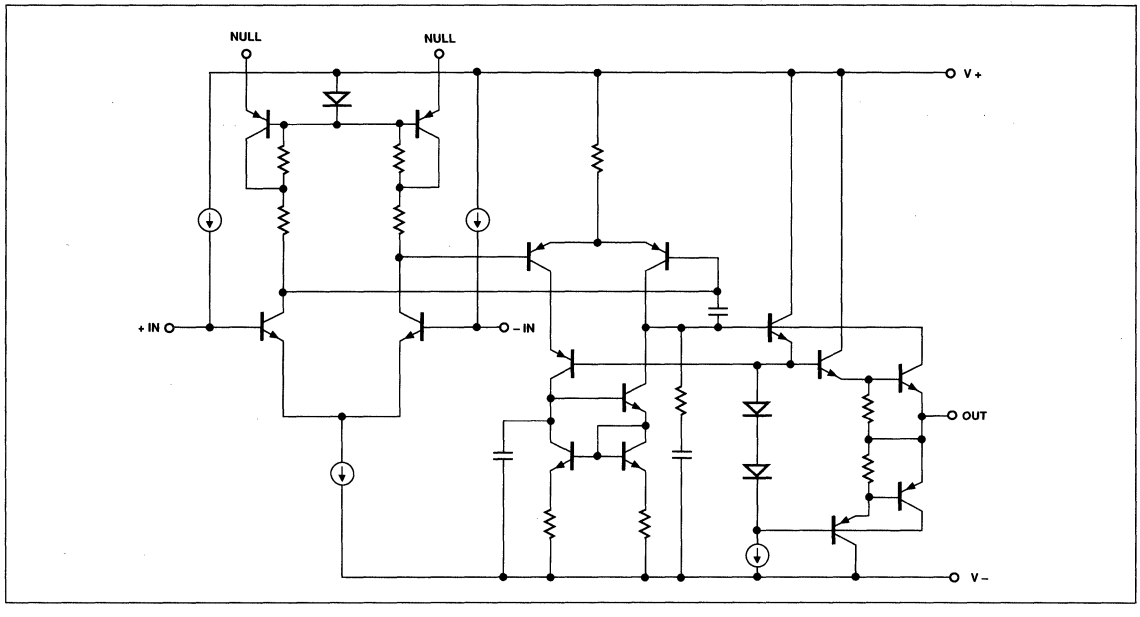
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



BURN-IN CIRCUIT



SIMPLIFIED SCHEMATIC



APPLICATIONS INFORMATION

The OP-61 combines high speed with a level of precision and noise performance normally only found with slower amplifiers. Data acquisition and instrumentation technology has progressed to where dynamic accuracy and high resolution are both maintained to a very high level. The OP-61 was specifically designed to meet the stringent requirements of these systems.

Signal-to-noise ratio degrades as input referred noise or bandwidth increases. The OP-61 has a very wide bandwidth, but its input noise is only $3nV/\sqrt{Hz}$. This makes the total noise generated over its closed-loop bandwidth considerably less than previously available wideband operational amplifiers.

The OP-61 provides stable operation in closed-loop gain configurations of 10 or more. Large load capacitances should be decoupled with a resistor placed inside the feedback loop (see Driving Large Capacitive Loads).

OFFSET VOLTAGE ADJUSTMENT

Offset voltage can be adjusted by a potentiometer of 10kΩ to 100kΩ resistance. This potentiometer should be connected between pins 1 and 5 with the wiper connected directly to the OP-61 V+ pin (see Figure 1). By connecting this line directly to the op amp V+ terminal, common impedance paths shared by both return currents and the null inputs will be avoided. Nulling inputs to any op amp are simply another set of sensitive differentially balanced inputs. Therefore, care must always be exercised in laying out signal paths by not placing the trimmer, or the nulling input lines, directly adjacent to high frequency signal lines.

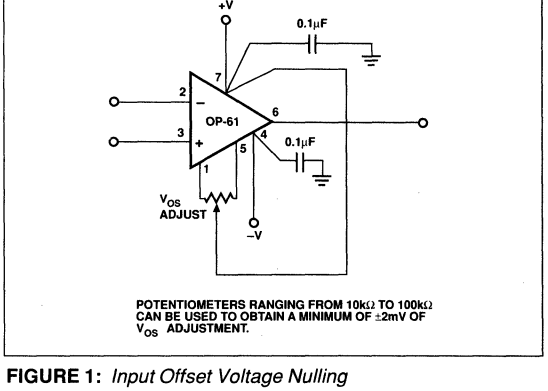


FIGURE 1: *Input Offset Voltage Nulling*

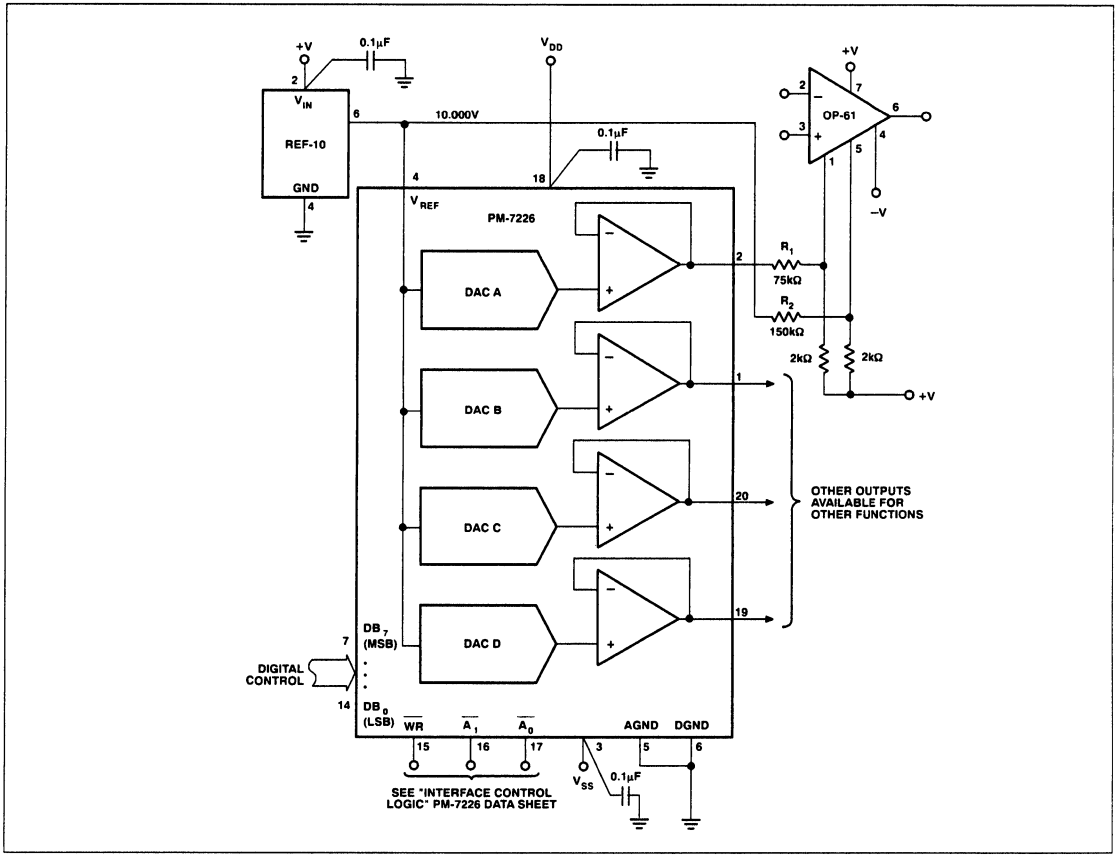


FIGURE 2: *Trimming OP-61 Voltage Offset with 0 to 10V Voltage Output, PM-7226 Quad D/A*

D/A converters can also be used for offset adjustments in systems that are microprocessor controlled. Figure 2 illustrates a PM-7226 quad, 8-bit D/A, used to null the OP-61's offset voltage. A stable fixed bias current is provided into pin 5 of the OP-61, from R_2, and a REF-10, +10V precision voltage reference. Current through R_1, from the D/A voltage output provides the programmed V_{OS} adjustment control. Symmetric control of the offset adjustment is effected since equal currents are sourced into R_1 and R_2 when the D/A is at half scale, binary input code = 10000000.

With the circuit components shown in Figure 2, the maximum V_{OS} adjustment range is ±500mV, referred to the input of the OP-61. Incremental adjustment range is approximately 2µV per bit, allowing V_{OS} to be trimmed to ±2µV.

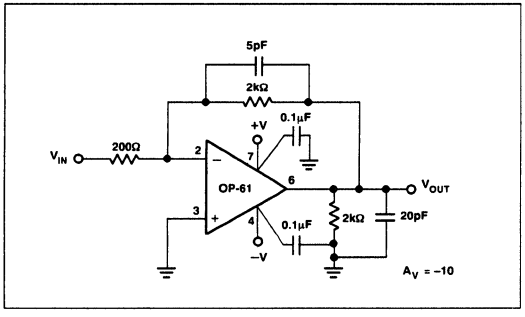


FIGURE 3: *Large- and Small-Signal Response Test Circuit*

TRANSIENT RESPONSE PERFORMANCE

Figures 4 and 5, respectively, show the small-signal and large-signal transient response of the OP-61 driving a 20pF load from the circuit in Figure 3. Both waveforms are symmetric and exhibit only minimal overshoot. The slew rate symmetry, apparent from the large-signal response, decreases the DC offsets that occur when processing input signals that extend outside the range of the OP-61's full-power bandwidth.

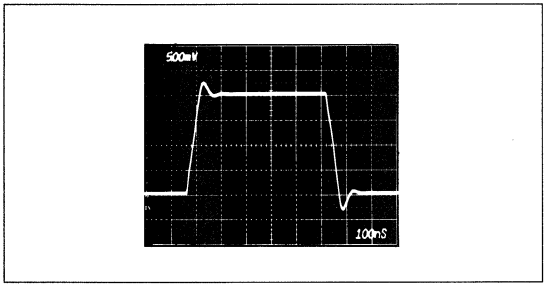


FIGURE 4: *Small-Signal Transient Response*

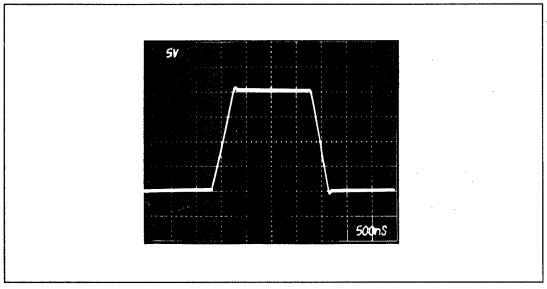


FIGURE 5: *Large-Signal Transient Response*

DRIVING CAPACITIVE LOADS

Direct capacitive loading will reduce the phase margin of any op amp. A pole is created by the combination of the op amp's output impedance and the capacitive load that induces phase lag and reduces stability. However, high-speed amplifiers can easily drive a capacitive load indirectly. This is shown in Figure 6. The OP-61 is driving a 1000pF capacitive load. R_1 and C_1 serve to counteract the loss of phase margin by feedforwarding a small amount of high frequency output signal back to the amplifier's inverting input,

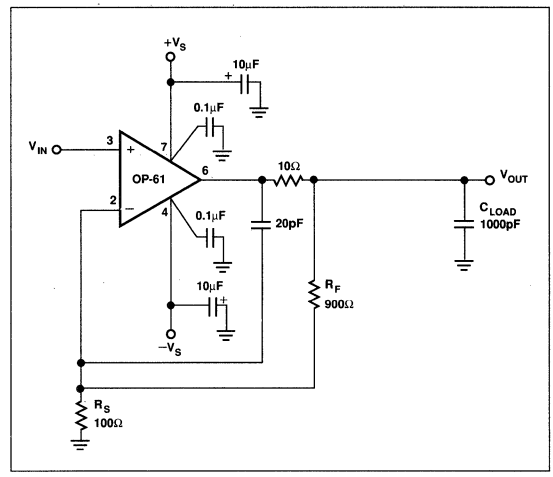


FIGURE 6: *OP-61 Noninverting Gain of 10 Amplifier, Compensated to Handle Large Capacitive Loads*

thereby preserving adequate phase margin. The resulting pulse response can be seen in Figure 7. Extra care may be required to ensure adequate decoupling by placing a 1µF to 10µF capacitor in parallel with the existing decoupling capacitor. Adequate decoupling ensures a low impedance path for high frequency energy transferred from the decoupling capacitors through the amplifier's output stage to a reactive load.

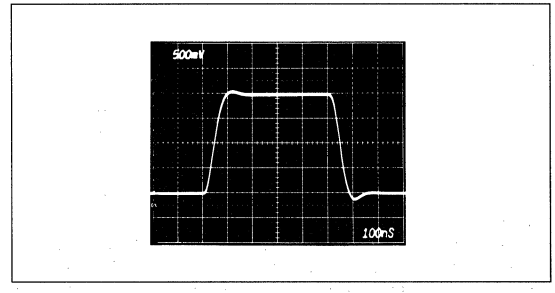


FIGURE 7: *Pulse Response of Compensated X10 Amplifier in Figure 6, V_{IN} = 100mV_{p-p}, V_{OUT} = 1V_{p-p}, Frequency of Square Wave = 1MHz, C_{LOAD} = 1000pF!*

DECOUPLING AND LAYOUT GUIDELINES

The OP-61 op amp is a superb choice for a wide range of precision high-speed, low noise amplifier applications. However, care must be exercized in both the design and layout of high-speed circuits in order for the specified performance to be realized.

Although the OP-61 has excellent power supply rejection over a wide bandwidth, the negative supply rejection is limited at high frequencies since the amplifier's internal integrator is biased via the negative supply line. This operation is typical performance for all monolithic op amps, and not unique to the OP-61. Since the negative supply rejection will approach zero for signals above the close-loop bandwidth, high-speed transients and wideband power supply noise, on the negative supply line, will result in spurious signals being directly added to the amplifier's output. Adequate power supply decoupling prevents this problem.

Generally, a 0.1μF tantalum decoupling capacitor, placed in close proximity across the amplifier's actual power supply pin and ground is recommended. This will satisfy most decoupling requirements, especially when the circuit is built on a low impedance ground plane. When a heavy copper clad ground plane is not used, it becomes especially important to confine the high frequency output load currents confined to as small a high-frequency signal path as possible, as suggested in Figure 8.

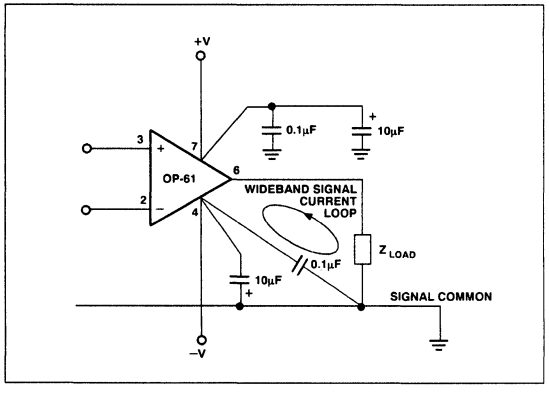


FIGURE 8: *Proper power supply bypassing is required to obtain optimum performance with the OP-61. Maintain as small wideband signal current path as possible. Where signal common is a low impedance ground plane, simply decouple 0.1μF to ground plane near the OP-61.*

Power management of complex systems sometimes results in a complex L-C network that has high frequency natural resonances that cause stability problems in circuits internal to the system. Resistors added in series to the supply lines can lower the Q of the undesired resonances, preventing oscillations on the supply lines. Resistors of 3 to 10 ohms work well and serve to ensure the stability of the OP-61 in such systems.

ADDITIONAL CAVEATS FOR HIGH-SPEED AMPLIFIERS INCLUDE:

1. Keep all leads as short as possible, using direct point-to-point wiring. Do not wire-wrap or use "plug-in" boards for prototyping circuits.
2. Op amp feedback networks should be placed in close proximity to the amplifiers inputs. This reduces stray capacitance that compromises stability margins.
3. Maintain low feedback and source resistance values. Impedance levels greater than several kilo-ohms may result in degrading the amplifier's overall bandwidth and stability.
4. The use of heavy ground planes reduces stray inductance, and provides a better return path for ground currents.
5. Decoupling capacitors must have short leads and be placed at the amplifier's supply pins. Use low equivalent series resistance (ESR) and low inductance chip capacitors wherever possible.
6. Evaluation of prototype circuits should be performed with a low input capacitance, X10 compensated oscilloscope probe. X1 uncompensated probes introduce excessive stray capacitance which alters circuit characteristics by introducing additional phase shifts.
7. Do not directly drive either large capacitive loads or coax cables with high-speed amplifiers (see DRIVING COAXIAL CABLES).
8. Watch out for parasitic capacitances at the +/– inputs to wideband noninverting op amp circuits. Since these nodes are not maintained at virtual ground as in the inverting amplifier configuration, parasitics may degrade bandwidth. Wideband noninverting amplifiers may require the ground plane trace removed from local proximity to the op amp's inputs.

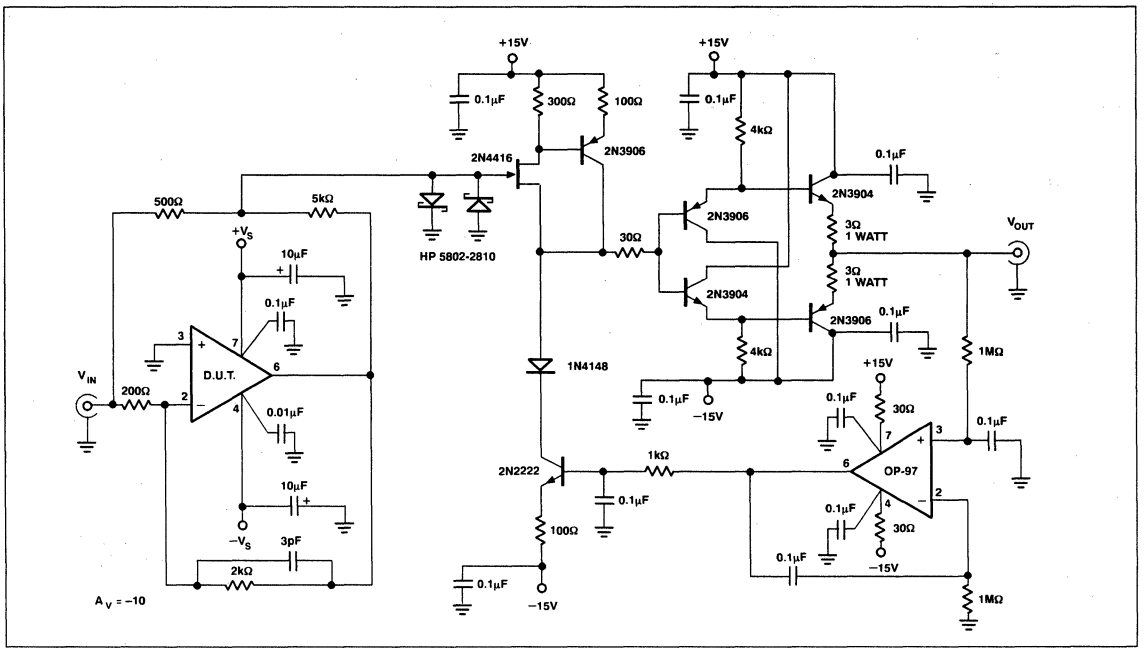


FIGURE 9: *High-Speed Settling Time Fixture (for 0.1 and 0.01%)*

SETTLING TIME

Settling time is the time between when the input signal begins to change and when the output permanently enters a prescribed error band. Figure 9 illustrates the artificial summing node test configuration, used to characterize the OP-61 settling time. The OP-61 is set in a gain of −10 with a 1.0V step input.The error bands on the output are 5mV and 0.5mV, respectively, for 0.1% and 0.01% accuracy.

The test circuit, built on a copper clad circuit board, has a FET input stage which maintains extremely low loading capacitance at the artificial sum node. Preceeding stages are complementary emitter follower stages, providing adequate drive current for a 50Ω oscilloscope input. The OP-97 establishes biasing for the input stage, and eliminates excessive offset voltage errors.

Figure 10 illustrates the OP-61's typical settling time of 330ns. Moreover, problems in settling response, such as thermal tails and long-term ringing are nonexistent. This performance of the OP-61 makes it a suberb choice for systems demanding both high sampling rates and high resolution.

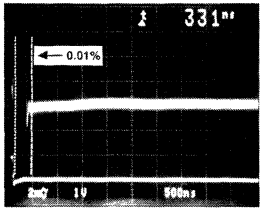


FIGURE 10: *Settling Characteristics of the OP-61 to 0.01%. No Thermal Settling Tail Appears as Part of the Settling Response.*

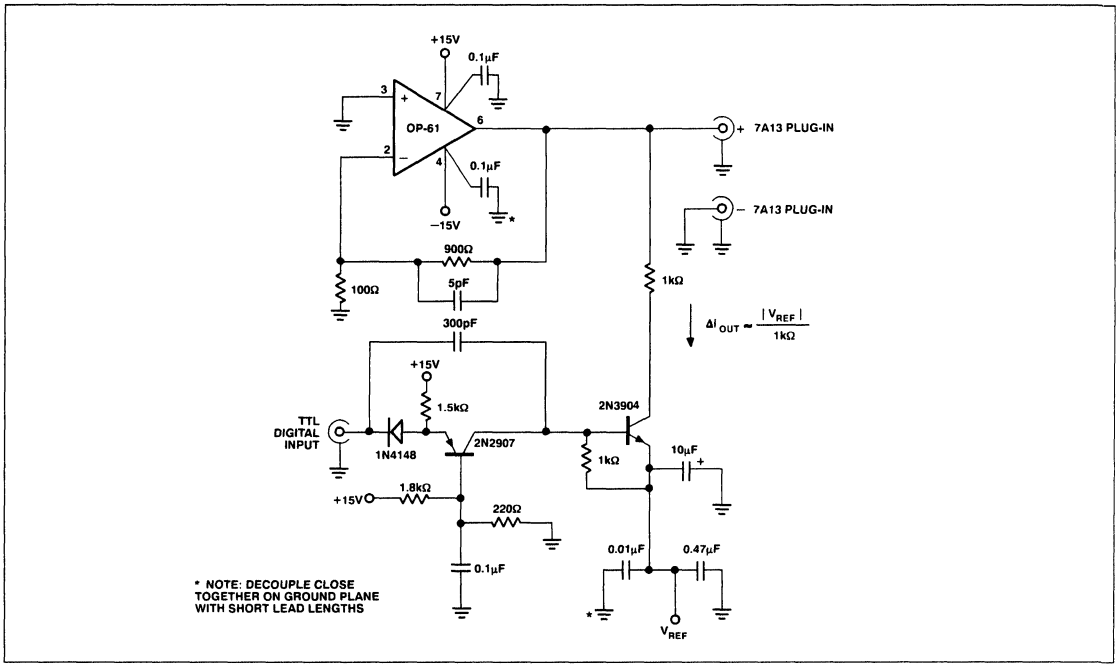


FIGURE 11: *Transient Output Impedance Test Fixture*

TRANSIENT OUTPUT IMPEDANCE

Settling characteristics of operational amplifiers also includes an amplifier's ability to recover, i.e., settle, from a transient current output load condition. An example of this includes an op amp driving the input from a SAR type A/D converter. Although the comparison point of the converter is usually diode clamped, the input swing of plus-and-minus a diode drop still gives rise to a significant modulation of input current. If the closed-loop output impedance is low enough and bandwidth of the amplifier is sufficiently large, the output will settle before the converter makes a comparison decision which will prevent linearity errors or missing codes.

Figure 11 shows a settling measurement circuit for evaluating recovery from an output current transient. An output disturbing current generator provides the transient change in output load current of 1mA. As seen in Figure 12, the OP-61 has extremely fast recovery of 180ns, (to 0.01%), for a 1mA load transient. The performance makes it an ideal amplifier for data acquisition systems.

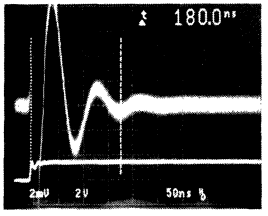


FIGURE 12: *OP-61's Extremely Fast Recovey Time from a 1mA Load Transient to 0.01%*

DRIVING COAXIAL CABLES

The OP-61 amplifier, and a BUF-03 unity-gain buffer, make an excellent drive circuit for 75Ω or 50Ω coaxial cables. To maintain optimum pulse response, and minimum reflections, op amp circuits driving coaxial cables should be terminated at both ends. Unterminated cables can appear as a resonant load to the amplifier, degrading stability margins. Also, since coaxial cables represent a significant capacitive load shunting the driving amplifier, it is not possible to drive them directly from the op amp's output (RG-58 coax. typically has 33pF/foot of capacitance).

Figure 13 illustrates an OP-61 noninverting, gain of 10, amplifier stage, driving a double-matched coaxial cable. Since the double-matching of the cable results in voltage gain loss of 6dB, the composite voltage gain of the entire circuit is 5, or 14dB.

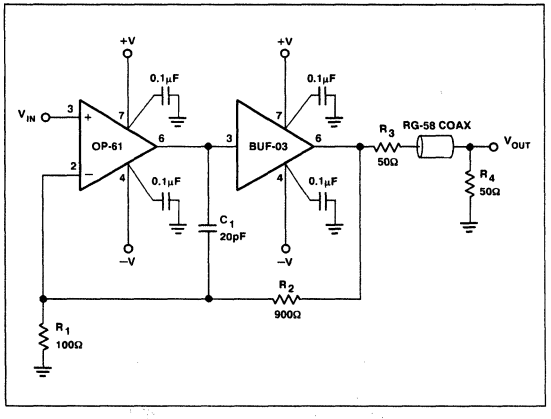


FIGURE 13: *OP-61 Noninverting Amplifier Driving Coaxial Cable, Composite Gain = 5 from V_{IN} to V_{OUT}. Adjust C_1 for Desired Pulse Response.*

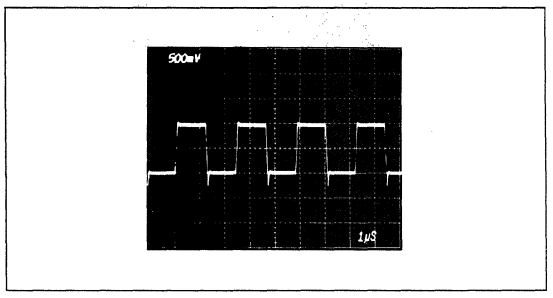


FIGURE 14: *Pulse Response from Amplifier Circuit in Figure 13, Driving 15 Ft. of RG-58 Coaxial Cable*

Resistors R_3 and R_4 serve to absorb reflections at both ends of the cable. The OP-61's wide bandwidth and fast symmetric slewing, results in a very clean pulse reponse, as can be seen in Figure 15. The BUF-03 serves to increase the output current capability to 70mA peak, and the ability to drive up to a 1µF capacitive load (or a longer cable). The value of C_1 may need to be slightly adjusted to provide an optimum value of phase lead, or pulse response. This capacitor serves to correct for the current buffers phase lag, internal to the OP-61's feedback loop.

NOISE MODEL AND DISCUSSION

The OP-61's exceptionally low voltage noise (e_n = 3.0nV/Hz, high open-loop gain, and wide bandwidth makes it ideal for accurately amplifying wideband low-level signals. Figure 15a shows the OP-61 cleanly amplifying a 5mV$_{p-p}$, 1MHz sine wave, with inverting gain of 100. Noise or limited bandwidth prevents most amplifiers from achieving this performance.

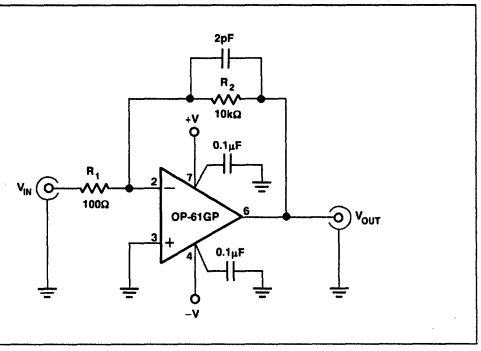


FIGURE 15a: *Example of Low Level Amplifier in an Inverting Configuration, Gain = V_{OUT}/V_{IN} = $-R_2/R_1$ = −100*

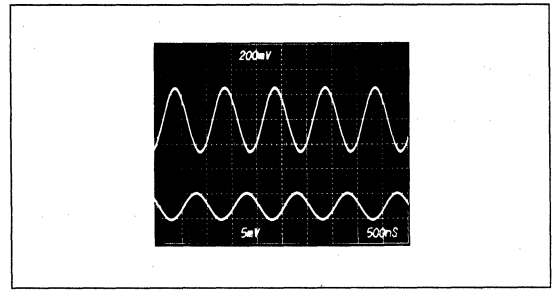


FIGURE 15b: *OP-61, Gain = −100.0, Wideband Amplifier, V_{IN} = 5mV$_{p-p}$ Signal at 1MHz, V_{OUT} = 500mV$_{p-p}$*

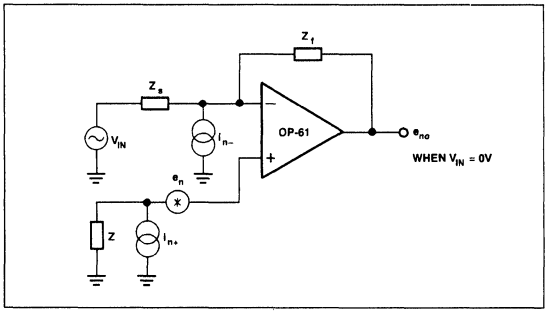


FIGURE 16: *Inverting Gain Configuration Noise Model for the OP-61*

The inverting amplifier model, seen in Figure 16, can be used to calculate the equivalent input noise, e_{ni}. e_{ni} is the voltage noise, modeled as part of the input signal. It represents all the current and voltage noise sources lumped into one equivalent input voltage.

Typical values for the OP-61 noise parameters are:

e_n = 3.4nV/$\sqrt{Hz}$ @ 1kHz

i_n = 1.7pA/$\sqrt{Hz}$ @ 10kHz

(where it is assumed that $i_n = i_n- = i_n+$).

It can be defined from the model in Figure 16:

e_{ni} = total input referred spot voltage noise (all noise contributions lumped into one equivalent voltage noise source).

e_n = spot voltage noise of OP-61

i_n = spot current noise of OP-61

Z_S = total input impedance

Z = impedance at OP-61 + input node

A_{VCL} = closed-loop gain for inverting amplifier

N.G. = $1 + |A_{VCL}|$ = noise gain for inverting amplifier

i_{ZS} = spot noise current generated by Z_s. If $Z_s = R_s$, then $i_{ZS} = i_{RS} = 0.129\sqrt{(1/R_S)}$ nV/$\sqrt{Hz}$.

e_{Zf} = spot voltage noise generated by Z_f. If $Z_f = R_f$, then $e_{Zf} = e_{Rf} = 0.129\sqrt{R_f}$ nV/$\sqrt{Hz}$.

Note: Equation is derived from Johnson noise relationship of resistor R:

$e_R = \sqrt{4kTR} = \sqrt{4kT}\sqrt{R} = 0.129\sqrt{R}$ nV/$\sqrt{Hz}$. R is in ohms.

The equivalent input voltage noise, referred to the output, can be found by adding all the noise sources in a sum-of-square fashion:

$$e_{no}^2 = e_n^2 (N.G.)^2 + i_n^2 |Z|^2 (N.G.)^2 + i_n^2 |Z_f|^2 + i_{ZS}^2 |Z_f|^2 + e_{Zf}^2$$

Referred back to the amplifiers input:

$$e_{ni} = \frac{e_{no}}{|A_{VCL}|} =$$

$$\frac{\sqrt{(e_n^2 (N.G.)^2 + i_n^2 |Z|^2 (N.G.)^2 + i_n^2 |Z_f|^2 + i_{ZS}^2 |Z_f|^2 + e_{Zf}^2)}}{|A_{VCL}|}$$

To capitalize on the low voltage performance of the OP-61, Z, Z_f and especially Z_S must be as low impedance as possible. With low impedance values of Z_f and Z_S:

$$e_{ni} \cong \frac{\sqrt{e_n^2 (1 + |A_{VCL}|)^2}}{|A_{VCL}|} \text{ or, } e_{ni} \cong \frac{e_n (N.G.)}{(N.G.) - 1}$$

All noise contributions are now easily modelled as a signal equivalent noise voltage source, e_{ni} (see Figure 17).

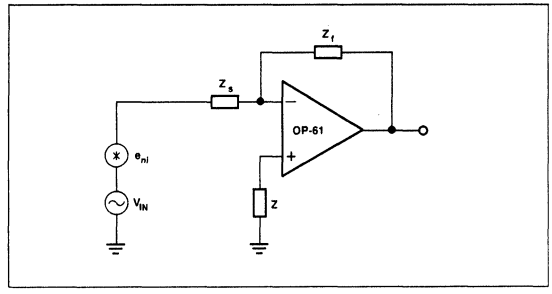


FIGURE 17: *Equivalent Noise Model, Where All Noise Contributions are Lumped Into e_{ni}*

OP-61 SPICE MACROMODEL

Figures 18 and 19 show the node and net list for a SPICE macromodel of the OP-61. The model is a simplified version of the actual device and simulates important DC parameters such as V_{OS}, I_{OS}, I_B, A_{VO}, CMR, V_O and I_{SY}. AC parameters such as slew rate, gain and phase reponse and CMR change with frequency are also simulated by the model.

The model uses typical parameters for the OP-61. The poles and zeros in the model were determined from the actual open and closed-loop gain and phase reponse of the OP-61. In this way the model presents an accurate AC representation of the actual device. The model assumes an ambient temperature of 25°C (see following pages).

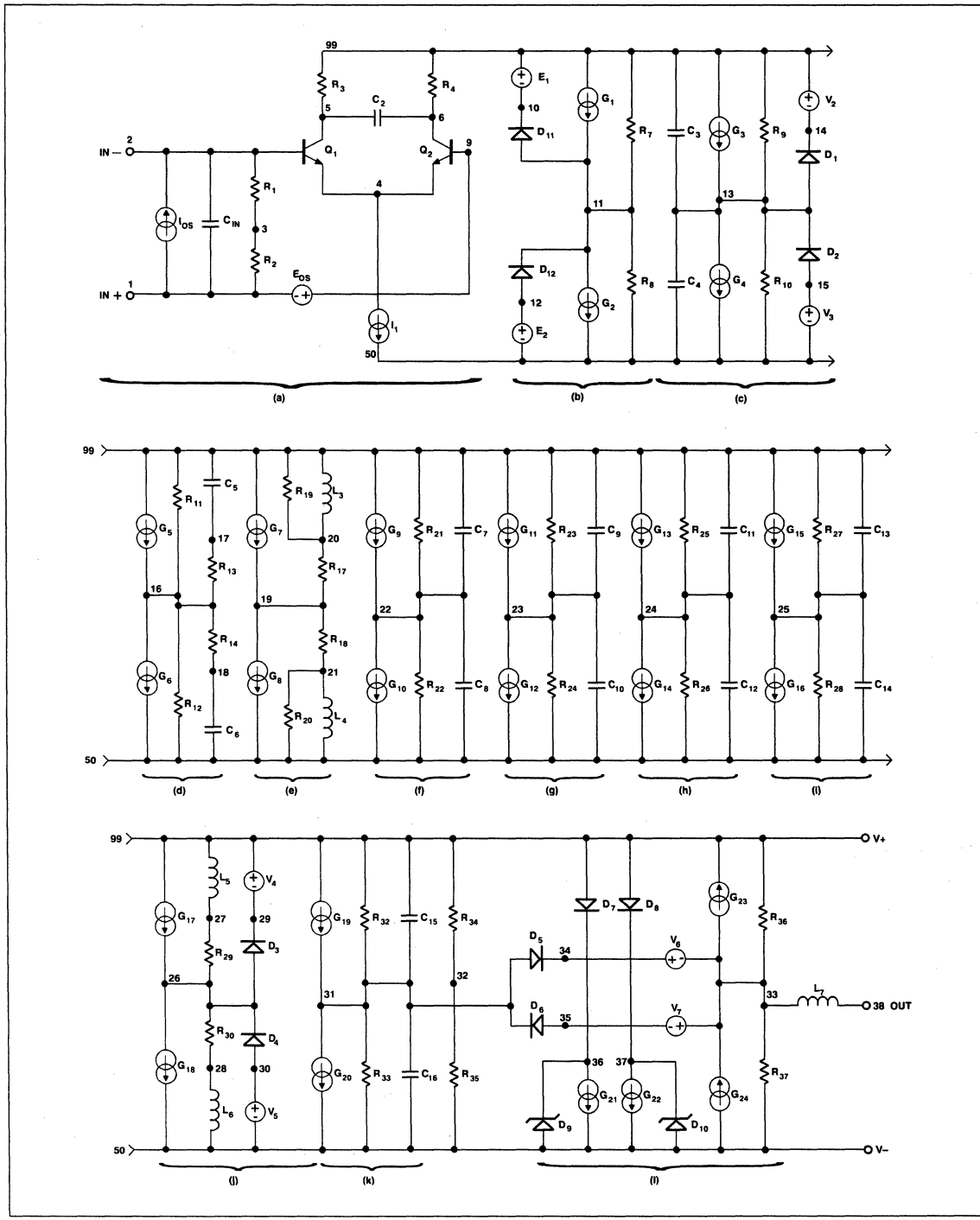


FIGURE 18: *OP-61 SPICE Macro-Model Schematic and Node List*

```
OP-61 MACROMODEL AND TEST CIRCUIT © ADI 1990
*
* subckt OP-61 1  2 38  99  50
*
* INPUT STAGE & POLE AT 300 MHz
*
r1   2   3        5E11
r2   1   3        5E11
r3   5   99       51.6
r4   6   99       51.6
cin  1   2        5E-12
c2   5   6        5.141E-12
i1   4   50       1E-3
ios  1   2        2E-7
eos  9   1        poly(1) 26 32 400E-6 1
q1   5   2   4    qx
q2   6   9   4    qx
*
* FIRST GAIN STAGE
*
r7   11  99       1E6
r8   11  50       1E6
d11  11  10       dx
d12  12  11       dx
g1   99  11       5 6 2E-4
g2   11  50       6 5 2E-4
e1   99  10       poly(1) 99 32 –4.4 1
e2   12  50       poly(1) 32 50 –4.4 1
*
* SECOND GAIN STAGE & POLE AT 2.5kHz
*
r9   13  99       5.1598E6
r10  13  50       5.1598E6
c3   13  99       12.338E-12
c4   13  50       12.338E-12
g3   99  13       poly(1) 11 32 4.24E-3 9.69E-5
g4   13  50       poly(1) 32 11 4.24E-3 9.69E-5
v2   99  14       2.3
v3   15  50       2.3
d1   13  14       dx
d2   15  13       dx
*
* POLE-ZERO PAIR AT 4MHz / 8MHz
*
r11  16  99       1E6
r12  16  50       1E6
r13  16  17       1E6
r14  16  18       1E6
c5   17  99       19.89E-15
c6   18  50       19.89E-15
g5   99  16       13 32 1E-6
g6   16  50       32 13 1E-6
*
* ZERO-POLE PAIR AT 85MHz / 300MHz
*
r17  19  20       1E6
r18  19  21       1E6
r19  20  99       2.529E6
r20  21  50       2.529E6
l3   20  99       1.342E-3
l4   21  50       1.342E-3
g7   99  19       16 32 1E-6
g8   19  50       32 16 1E-6
*
* POLE AT 40MHz
*
r21  22  99       1E6
r22  22  50       1E6
c7   22  99       3.979E-15
c8   22  50       3.979E-15
g9   99  22       19 32 1E-6
g10  22  50       32 19 1E-6
*
* POLE AT 200MHz
*
r23  23  99       1E6
r24  23  50       1E6
c9   23  99       .796E-15
c10  23  50       .796E-15
g11  99  23       22 32 1E-6
g12  23  50       32 22 1E-6
*
* POLE AT 200MHz
*
r25  24  99       1E6
26   24  50       1E6
c11  24  99       .796E-15
c12  24  50       .796E-15
g13  99  24       23 32 1E-6
g14  24  50       32 23 1E-6
*
* POLE AT 200MHz
*
r27  25  99       1E6
r28  25  50       1E6
c13  25  99       .796E-15
c14  25  50       .796E-15
g15  99  25       24 32  1E-6
g16  25  50       32 24 1E-6
*
* COMMON-MODE GAIN NETWORK WITH ZERO AT 40kHz
*
r29  26  27       1E6
r30  26  28       1E6
l5   27  99       3.979
l6   28  50       3.979
g17  99  26       33 32 1E-11
g18  26  50       32 33 1E-11
*
* POLE AT 300MHz
*
r32  31  99       1E6
r33  31  50       1E6
c15  31  99       .531E-15
c16  31  50       .531E-15
g19  99  31       25 32 1E-6
g20  31  50       32 25 1E-6
*
* OUTPUT STAGE
*
r34  32  99       20.0E3
r35  32  50       20.0E3
r36  33  99       30
r37  33  50       30
l7   33  38       1.65E-7
g21  36  50       31 33 33.3333333E-3
g22  37  50       33 31 33.3333333E-3
g23  33  99       99 31 33.3333333E-3
g24  50  33       31 50 33.3333333E-3
v6   34  33       .2
v7   33  35       .2
d5   31  34       dx
d6   35  31       dx
d7   99  36       dx
d8   99  37       dx
d9   50  36       dy
d10  50  37       dy
*
* MODELS USED
*
.model qx NPN(BF=1250)
.model dx  D(IS=1E-15)
.model dy  D(IS=1E-15  BV = 50)
```

FIGURE 19: *OP-61 SPICE Net List*

* PSpice is a registered trademark of MicroSim Corporation.
** HSPICE is a tradename of Meta-Software, Inc.

ANALOG DEVICES

High-Speed, Wide-Bandwidth Operational Amplifier ($A_{VCL} \geq 5$)

OP-64

FEATURES

- **High Slew Rate ..... 130V/μs Min**
- **Fast Settling Time (+10V, 0.1%) ..... 100ns Typ**
- **Gain-Bandwidth Product (A_{VCL} = +5) ..... 80MHz Typ**
- **Low Supply Current ..... 8mA Max**
- **Low Noise ..... 8nV/√Hz Typ**
- **Low Offset Voltage ..... 1mV Max**
- **High Output Current ..... ±80mA Typ**
- **Eliminates External Buffer**
- **Standard 8-Pin Packages**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC 8-PIN	HERMETIC LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
1.0	OP64AJ*	OP64AZ*	–	OP64ARC/883	MIL
1.0	OP64EJ	OP64EZ	–	–	XIND
2.0	OP64FJ	OP64FZ	–	–	XIND
2.5	–	–	OP64GP	–	XIND
2.5	–	–	OP64GS††	–	XIND

XIND = Extended Industrial Temperature Range, –40°C to +85°C

* For devices processed in total compliance to MIL-SDT-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-99 can packages.

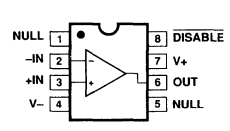
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The OP-64 is a high-performance monolithic operational amplifier that combines high speed and wide bandwidth with low power consumption. Advanced processing techniques have en-

Continued

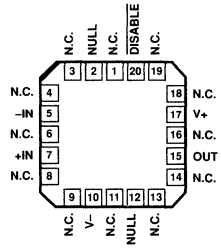
PIN CONNECTIONS



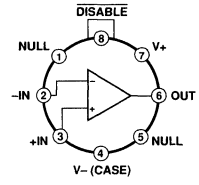
EPOXY MINI-DIP (P-Suffix)

8-PIN CERDIP (Z-Suffix)

EPOXY SO (S-Suffix)

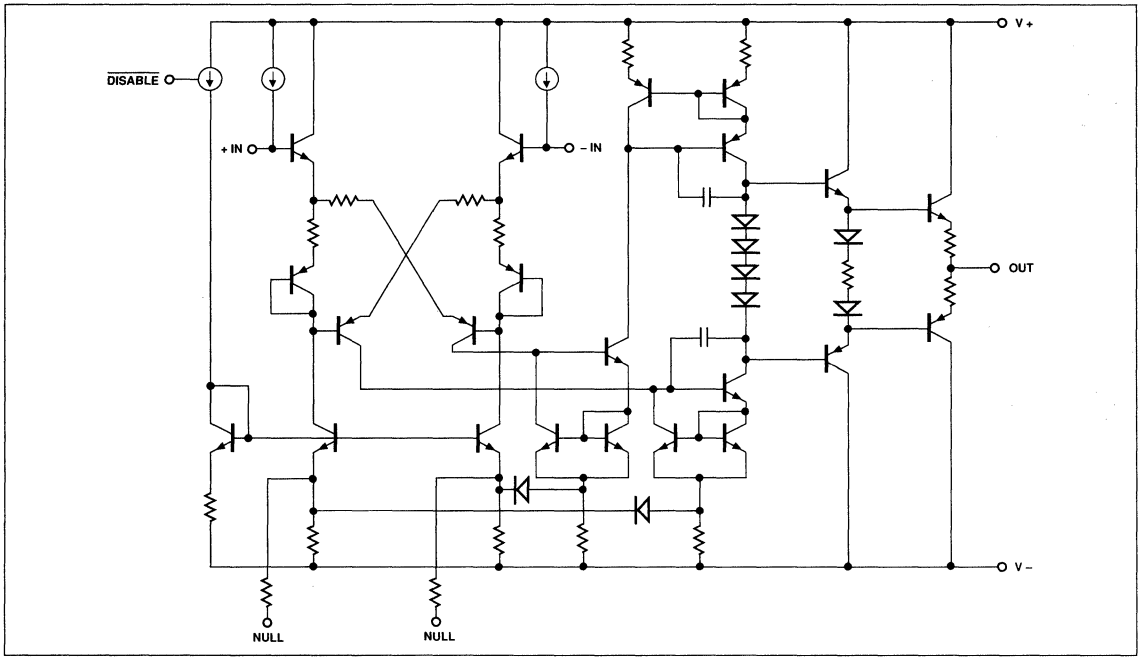


20-LEAD HERMETIC LCC (RC-Suffix)



TO-99 (J-Suffix)

SIMPLIFIED SCHEMATIC



GENERAL DESCRIPTION *Continued*

enabled PMI to make the OP-64 superior in cost and performance to many dielectrically-isolated and hybrid op amps.

Slew rate of the OP-64 is over 130V/µs. It is stable in gains of ≥5 and has a settling time of only 100ns to 0.1% with a 10V step input. However, unlike other high-speed op amps which have high supply requirements, the OP-64 needs less than 8mA of supply current. This enables the OP-64 to be packaged in space saving 8-pin packages. The OP-64 can deliver ±80mA of output current eliminating the need for a separate buffer amplifier in many applications. Noise of the OP-64 is only $8nV\sqrt{Hz}$, reducing system noise in wideband applications. In addition to its dynamic performance, the OP-64 adds DC precision with an input offset voltage of under 1mV.

The OP-64 is an ideal choice for RF, video and pulse amplifier applications and in new designs can replace the HA-5190/95 or EL-2190/95 with improved performance and reduced power consumption. Its high output current also suits the OP-64 for use in A/D or cable driver applications. The OP-64 includes a $\overline{\text{DISABLE}}$ pin which, when set low, shuts the amplifier off and reduces the supply current to 0.75mA.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Input Voltage ..... Supply Voltage
Differential Input Voltage 20V
$\overline{\text{DISABLE}}$ Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... 10 sec
Storage Temperature Range
(J, Z, RC) ..... –65°C to +175°C
(P, S) ..... –65°C to +150°C
Operating Temperature Range
OP-64A (J, Z, RC) ..... –55°C to +125°C
OP-64E, F (J, Z) ..... –40°C to +85°C
OP-64G (P, S) ..... –40°C to +85°C
Maximum Junction Temperature
OP-64A (J ,Z, RC) ..... +175°C
OP-64E, F (J, Z) ..... +175°C
OP-64G (P, S) ..... +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC, TC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

			OP-64A/E			OP-64F			OP-64G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Offset Voltage	V_{OS}		–	0.4	1	–	0.8	2	–	1.2	2.5	mV
Input Bias Current	I_B	V_{CM} = 0V	–	0.2	1	–	0.4	2	–	0.8	2.5	µA
Input Offset Current	I_{OS}	V_{CM} = 0V	–	0.1	1	–	0.3	2	–	0.6	2.5	µA
Input Voltage Range	IVR	(Note 1)	±11	–	–	±11	–	–	±11	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	90	100	–	84	94	–	84	94	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±5V to ±18V	–	5	17.8	–	15	31.6	–	15	31.6	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 2kΩ, V_O = ±10V R_L = 200Ω, V_O = ±5V	30 12.5	45 18	– –	20 10	35 16	– –	20 10	35 16	– –	V/mV
Output Voltage Swing	V_O	R_L = 2kΩ R_L = 200Ω	±11 ±10	±12.5 ±11.7	– –	±11 ±10	±12.5 ±11.7	– –	±11 ±10	±12.5 ±11.7	– –	V
Output Current	I_{OUT}		–	±80	–	–	±80	–	–	±80	–	mA
Supply Current	I_{SY}	No Load	–	6.2	8	–	6.2	8	–	6.2	8	mA

NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-64A/E MIN	OP-64A/E TYP	OP-64A/E MAX	OP-64F MIN	OP-64F TYP	OP-64F MAX	OP-64G MIN	OP-64G TYP	OP-64G MAX	UNITS
Disable Supply Current	$I_{SY\ \overline{DIS}}$	$\overline{DISABLE}$ = 0V Total for both supplies	–	0.75	1	–	0.75	1	–	0.75	1	mA
$\overline{DISABLE}$ Current	$I_{\overline{DIS}}$	$\overline{DISABLE}$ = 0V	–	0.5	–	–	0.5	–	–	0.5	–	mA
Slew Rate	SR	R_L = 2kΩ	130	170	–	130	170	–	130	170	–	V/µs
Full-Power Bandwidth	BW_p	(Note 2)	2	2.7	–	2	2.7	–	2	2.7	–	MHz
Gain-Bandwidth Product	GBWP	A_V = +5	–	80	–	–	80	–	–	80	–	MHz
Settling Time	t_s	10V Step 0.1%	–	100	–	–	100	–	–	100	–	ns
Phase Margin	$ø_m$	A_V = +5	–	57	–	–	57	–	–	57	–	degrees
Input Capacitance	C_{IN}		–	5	–	–	5	–	–	5	–	pF
Open-Loop Output Resistance	R_O		–	30	–	–	30	–	–	30	–	Ω
Voltage Noise Density	e_n	f_o = 10Hz f_o = 100Hz f_o = 1kHz f_o = 10kHz	– – – –	30 10 8 8	– – – –	– – – –	30 10 8 8	– – – –	– – – –	30 10 8 8	– – – –	nV/√Hz
Current Noise Density	i_n	f_o = 10kHz	–	7.5	–	–	7.5	–	–	7.5	–	pA/√Hz
External V_{OS} Trim Range	R_{pot} = 20kΩ		–	4	–	–	4	–	–	4	–	mV
Supply Voltage Range	V_S		±5	±15	±18	±5	±15	±18	±5	±15	±18	V

NOTES:
1. Guaranteed by CMR test.
2. Guaranteed by slew-rate test and formula $BW_p = SR/(2\pi 10V_{PEAK})$.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –40°C ≤ T_A ≤ +85°C for OP-64E/F/G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-64E MIN	OP-64E TYP	OP-64E MAX	OP-64F MIN	OP-64F TYP	OP-64F MAX	OP-64G MIN	OP-64G TYP	OP-64G MAX	UNITS
Offset Voltage	V_{OS}		–	0.5	1.5	–	1.0	3	–	1.5	3.5	mV
Input Bias Current	I_B	V_{CM} = 0V	–	0.3	2.5	–	0.5	3	–	1.5	3.5	µA
Input Offset Current	I_{OS}	V_{CM} = 0V	–	0.2	2.5	–	0.5	3	–	1.0	3.5	µA
Input Voltage Range	IVR	(Note 1)	±11	–	–	±11	–	–	±11	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11	86	100	–	80	94	–	80	94	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±5V to ±18V	–	5	31.6	–	15	50	–	15	50	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 2kΩ, V_O = ±10V R_L = 200Ω, V_O = ±5V	20 7.5	40 12	– –	15 5	35 10	– –	15 5	35 10	– –	V/mV
Output Voltage Swing	V_O	R_L = 2kΩ R_L = 200Ω	±11 ±10	±12.3 ±11.5	– –	±11 ±10	±12.3 ±11.5	– –	±11 ±10	±12.3 ±11.5	– –	V
Supply Current	I_{SY}	No Load	–	6.3	8.5	–	6.3	8.5	–	6.3	8.5	mA

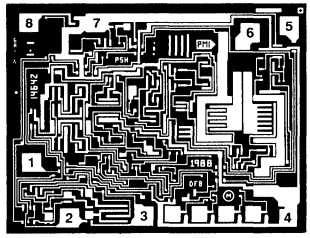
NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –55°C ≤ T_A ≤ +125°C for OP-64A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-64A MIN	OP-64A TYP	OP-64A MAX	UNITS
Offset Voltage	V_{OS}		–	0.4	2	mV
Input Bias Current	I_B	V_{CM} = 0V	–	0.35	2	µA
Input Offset Current	I_{OS}	V_{CM} = 0V	–	0.3	2	µA
Input Voltage Range	IVR	(Note 1)	±11	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11	86	100	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±5V to ±18V	–	8	31.6	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 2kΩ, V_O = ±10V R_L = 200Ω, V_O = ±5V	20 7.5	30 10	– –	V/mV
Output Voltage Swing	V_O	R_L = 2kΩ R_L = 200Ω	±11 ±7.5	±12 ±10	– –	V
Supply Current	I_{SY}	No Load	–	6.4	8.5	mA

NOTE:
1. Guaranteed by CMR test.

DICE CHARACTERISTICS



DIE SIZE 0.086 x 0.065 inch, 5,590 sq. mils
(2.18 x 1.65 mm, 3.60 sq. mm)

1. **NULL**
2. **–IN**
3. **+IN**
4. **V–**
5. **NULL**
6. **OUT**
7. **V+**
8. **$\overline{\text{DISABLE}}$**

2

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

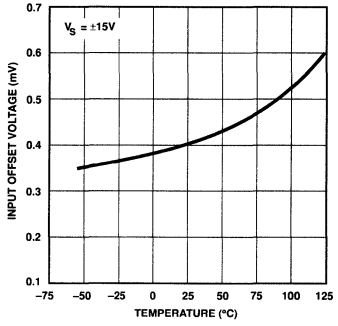
PARAMETER	SYMBOL	CONDITIONS	OP-64GBC LIMITS	UNITS
Offset Voltage	V_{OS}		2.5	mV MAX
Input Bias Current	I_B	$V_{CM} = 0V$	2.5	µA MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	2.5	µA MAX
Input Voltage Range	IVR	(Note 1)	±11	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	84	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 18V$	31.6	µV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 2k\Omega$, $V_O = \pm 10V$ $R_L = 200\Omega$, $V_O = \pm 5V$	20 10	V/mV MIN
Output Voltage Swing	V_O	$R_L = 2k\Omega$ $R_L = 200\Omega$	±11 ±10	V MIN
Slew Rate SR	$R_L = 2k\Omega$		120	V/µs MIN
Supply Current	I_{SY}	No Load	8	mA MAX

NOTES:
1. Guaranteed by CMR test.

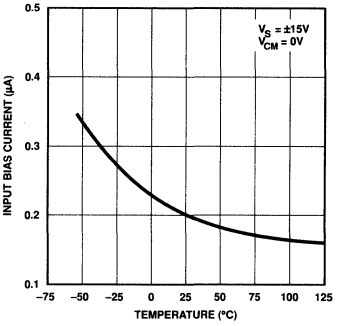
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

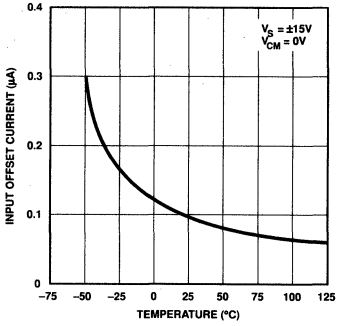
INPUT OFFSET VOLTAGE vs TEMPERATURE



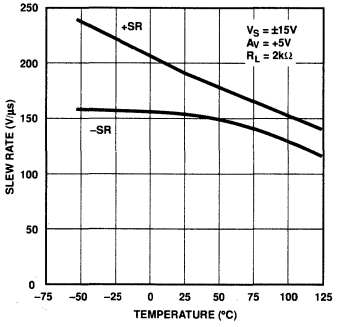
INPUT BIAS CURRENT vs TEMPERATURE



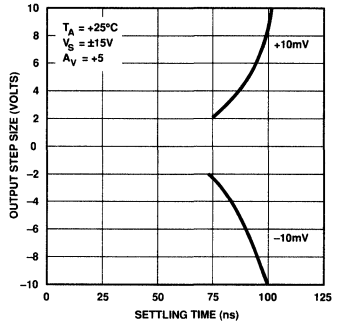
INPUT OFFSET CURRENT vs TEMPERATURE



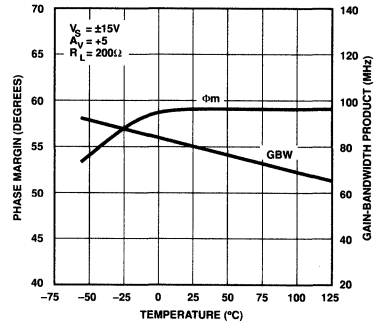
SLEW RATE vs TEMPERATURE



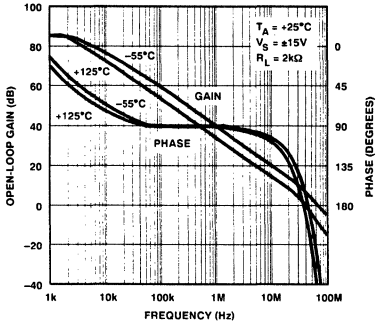
SETTLING TIME vs STEP SIZE



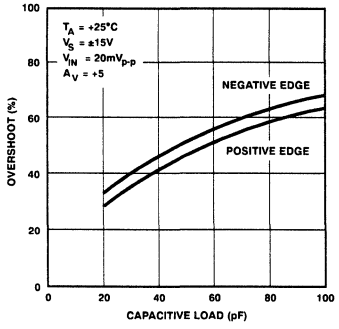
GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE



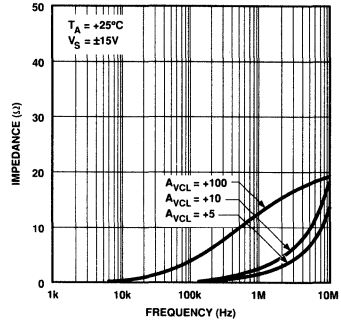
OPEN-LOOP GAIN, PHASE vs FREQUENCY



SMALL SIGNAL OVERSHOOT vs CAPACITIVE LOAD

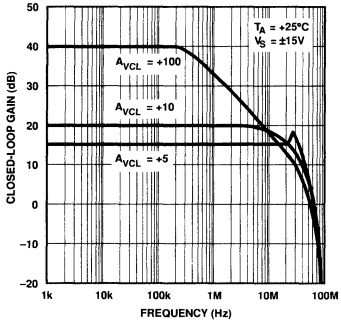


CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

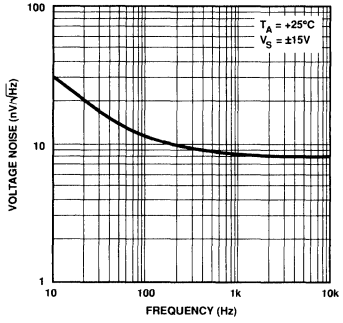


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

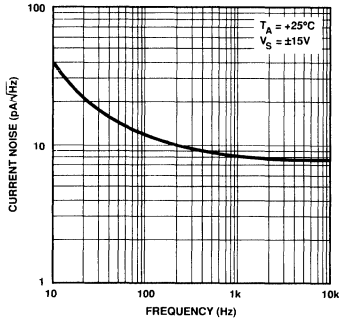
CLOSED-LOOP GAIN vs FREQUENCY



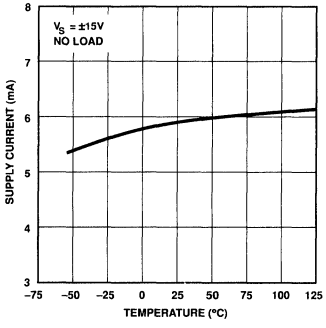
VOLTAGE NOISE DENSITY vs FREQUENCY



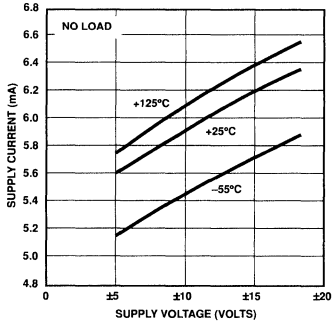
CURRENT NOISE DENSITY vs FREQUENCY



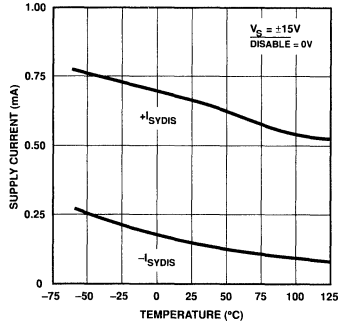
SUPPLY CURRENT vs TEMPERATURE



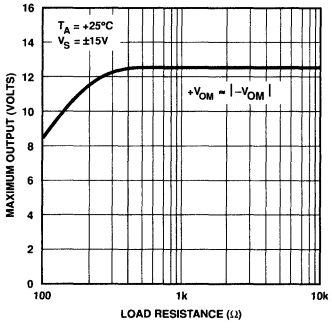
SUPPLY CURRENT vs SUPPLY VOLTAGE



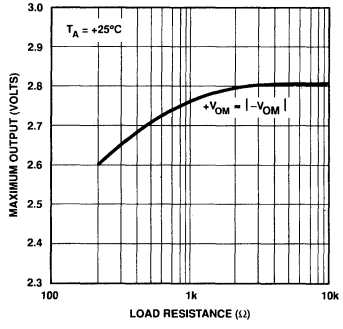
I_{SY} $\overline{\text{DISABLE}}$ vs TEMPERATURE



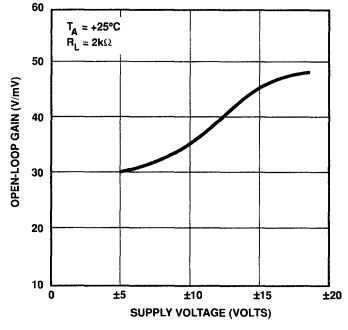
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE V_S = ±15V



MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE V_S = ±5V

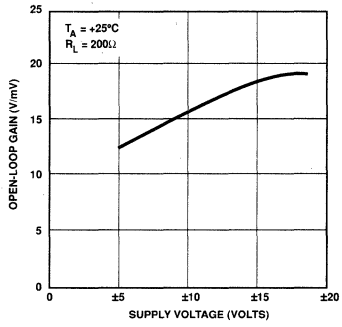


OPEN-LOOP GAIN vs SUPPLY VOLTAGE

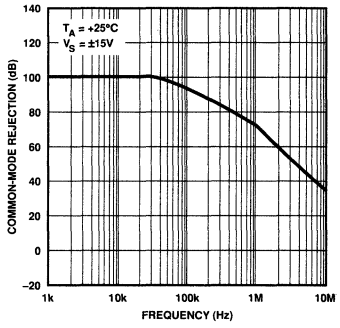


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

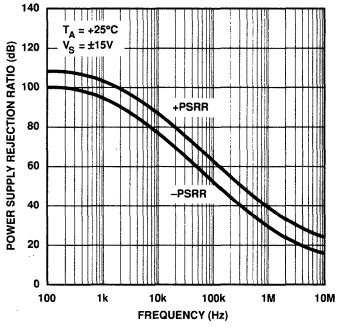
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



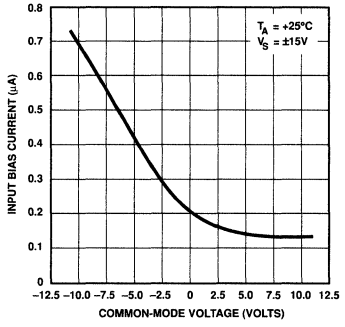
COMMON-MODE REJECTION vs FREQUENCY



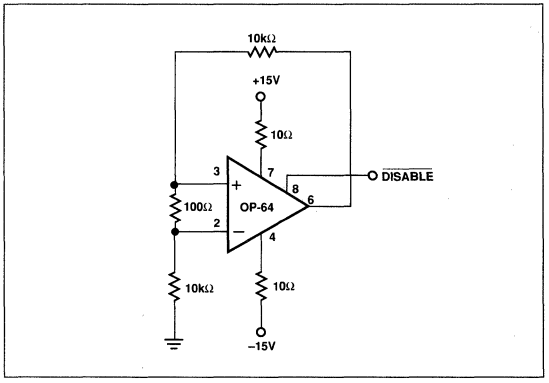
POWER SUPPLY REJECTION RATIO vs FREQUENCY



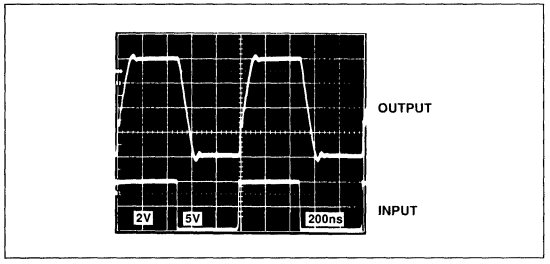
INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



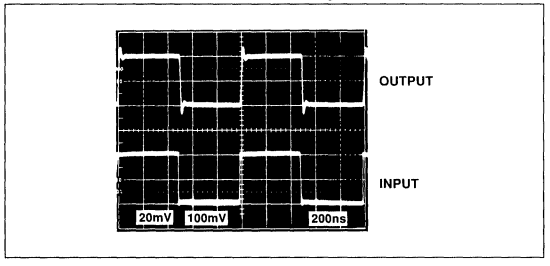
BURN-IN CIRCUIT



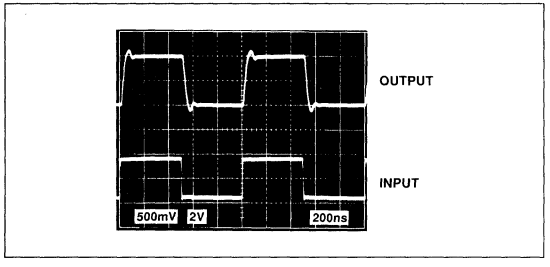
LARGE SIGNAL RESPONSE ($V_S = \pm 15V$)



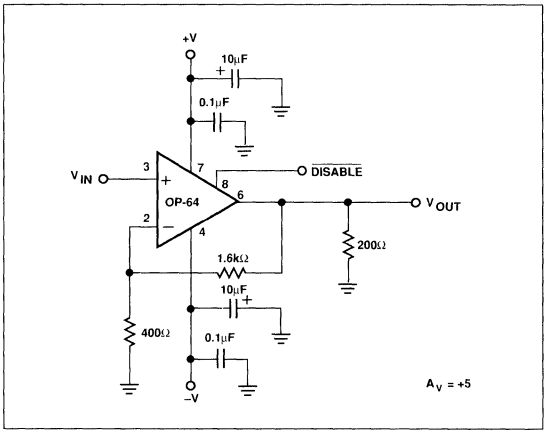
SMALL SIGNAL RESPONSE ($V_S = \pm 15V$)



LARGE SIGNAL RESPONSE ($V_S = \pm 5V$)



LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT



APPLICATIONS INFORMATION

POWER SUPPLY BYPASSING AND LAYOUT CONSIDERATIONS

Proper power supply bypassing is critical in all high-frequency circuit applications. For stable operation of the OP-64, the power supplies must maintain a low impedance-to-ground over an extremely wide bandwidth. This is most critical when driving a low resistance or large capacitance, since the current required to drive the load comes from the power supplies. A 10µF and 0.1µF ceramic bypass capacitor are recommended for each supply, as shown in Figure 1, and will provide adequate high-frequency bypassing in most applications. The bypass capacitors should be placed at the supply pins of the OP-64. As with all high frequency amplifiers, circuit layout is a critical factor in obtaining optimum performance from the OP-64. Proper high frequency layout reduces unwanted signal coupling in the circuit. When breadboarding a high frequency circuit, use direct point-to-point wiring, keeping all lead lengths as short as possible. Do not use wire-wrap boards or "plug-in" prototyping boards.

During PC board layout, keep all lead lengths and traces as short as possible to minimize inductance. The feedback and gain-setting resistors should be as close as possible to the inverting input to reduce stray capacitance at that point. To further reduce stray capacitance, remove the ground plane from the area around the inputs of the OP-64. Elsewhere, the use of a solid unbroken ground plane will insure a good high-frequency ground.

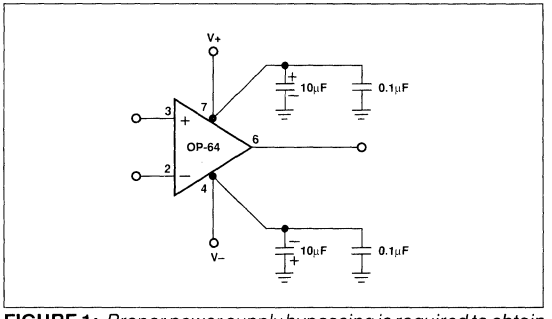


FIGURE 1: *Proper power supply bypassing is required to obtain optimum performance with the OP-64.*

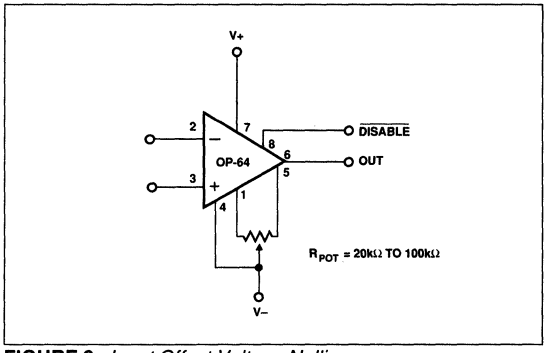


FIGURE 2: *Input Offset Voltage Nulling*

OFFSET VOLTAGE ADJUSTMENT

Offset voltage is adjusted with a 20kΩ potentiometer as shown in Figure 2. The potentiometer should be connected between pins 1 and 5 with its wiper connected to the V– supply. The typical trim range is ±4mV.

OP-64 $\overline{\text{DISABLE}}$ AMPLIFIER SHUTDOWN

Pin 8 of the OP-64, $\overline{\text{DISABLE}}$, is an amplifier shutdown control input. The OP-64 operates normally when Pin 8 is left floating. When greater than 250µA is drawn from the $\overline{\text{DISABLE}}$ pin, the OP-64 is disabled. The supply current drops to 1mA and the output impedance rises to 2kΩ. To draw current from the $\overline{\text{DISABLE}}$ pin, an open collector output logic gate or a discrete NPN transistor can be used as shown in Figure 3. An internal resistor

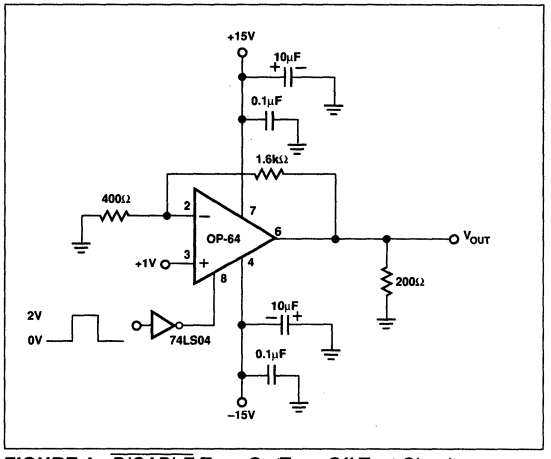


FIGURE 4: *$\overline{\text{DISABLE}}$ Turn-On/Turn-Off Test Circuit*

limits the $\overline{\text{DISABLE}}$ current to around 500µA if the $\overline{\text{DISABLE}}$ pin is grounded with the OP-64 powered by ±15V supplies. These logic interface methods have the added advantage of level shifting the TTL signal to whatever supply voltage is used to power the OP-64.

Figure 4 shows a test circuit for measuring the turn-on and turn-off times for the OP-64. The OP-64 is in a gain of 5 with a +1V DC input. As the input pulse to the 74LS04 rises its output falls,

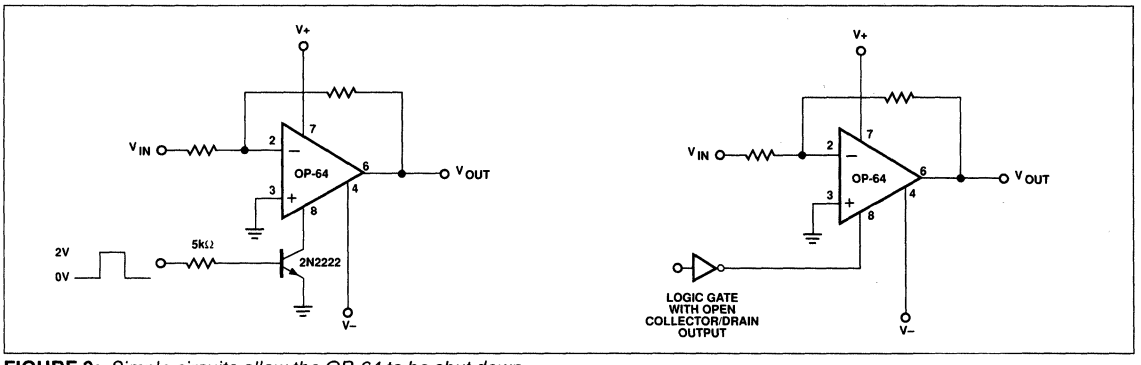


FIGURE 3: *Simple circuits allow the OP-64 to be shut down.*

drawing current from the $\overline{\text{DISABLE}}$ pin and disabling the amplifier. The output voltage delay is shown in Figure 5 and takes 500µs to reach ground due to the extra current supplied to the amplifier by the 10µF electrolytic bypass capacitors. The turn-on time is much quicker than the turn-off time. In this situation as the input to the 74LS04 falls its output rises, returning the OP-64 to normal operation. The amplifier's output turns on in 250ns.

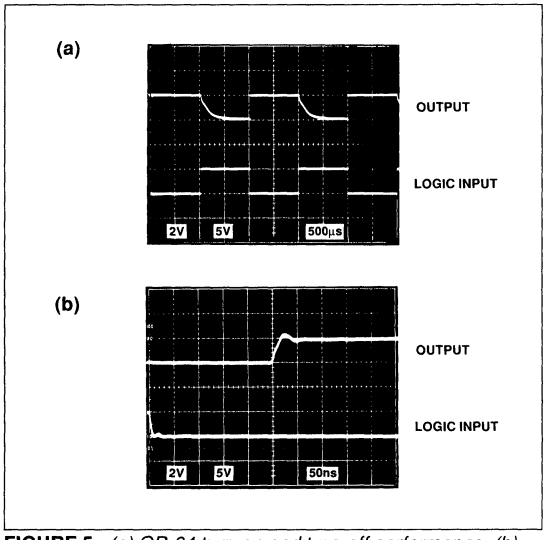


FIGURE 5: *(a) OP-64 turn-on and turn-off performance. (b) Expanded scale showing turn-on performance of the OP-64.*

OVERDRIVE RECOVERY

Figure 6 shows the overdrive recovery performance of the OP-64. Typical recovery time is 270ns from negative overdrive and 80ns from positive overdrive.

VIDEO AMPLIFIER/TERMINATED LINE DRIVER

The OP-64 can be used as a video amplifier/terminated line driver as shown in Figure 8. With its high output current capability, the OP-64 eliminates the need for an external buffer.

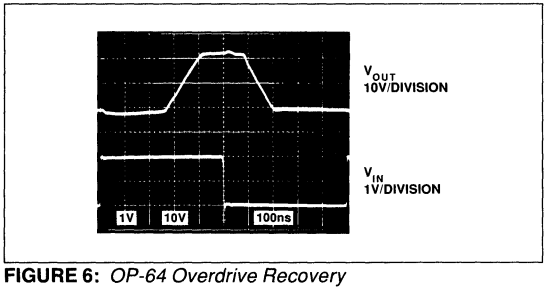


FIGURE 6: *OP-64 Overdrive Recovery*

The 75Ω cable termination resistor minimizes reflections from the end of the cable. The 75Ω series output resistor absorbs any reflections caused by a mismatch between the 75Ω termination resistor and the characteristic cable impedance. In this circuit the output voltage, V_{OUT}, is one-half of the OP-64's output voltage due to the divider formed by the 75Ω terminating resistors. The output voltage at the end of the terminated cable, V_{OUT}, spans –1V to +1V. The differential gain and phase for the video amplifier is summarized in Table1.

TABLE 1: Differential Gain and Phase of Video Amplifier/Line Driver

	Differential Gain		Differential Phase	
V_S	3.58MHz	5MHz	3.58MHz	5MHz
±15V	0.008dB	0.016dB	0.03°	0.03°
±12V	0.008dB	0.018dB	0.03°	0.03°

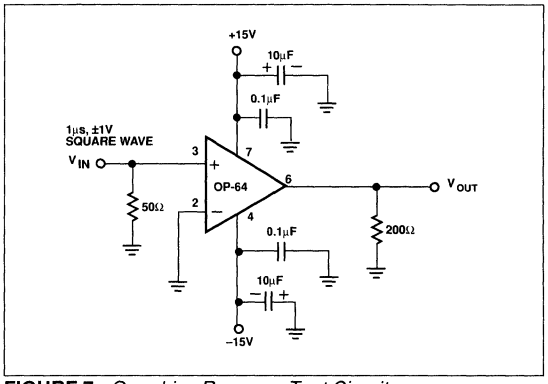


FIGURE 7: *Overdrive Recovery Test Circuit*

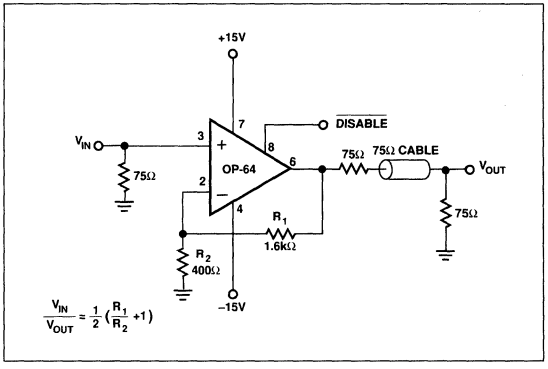


FIGURE 8: *Video Amplifier/Terminated Line Driver*

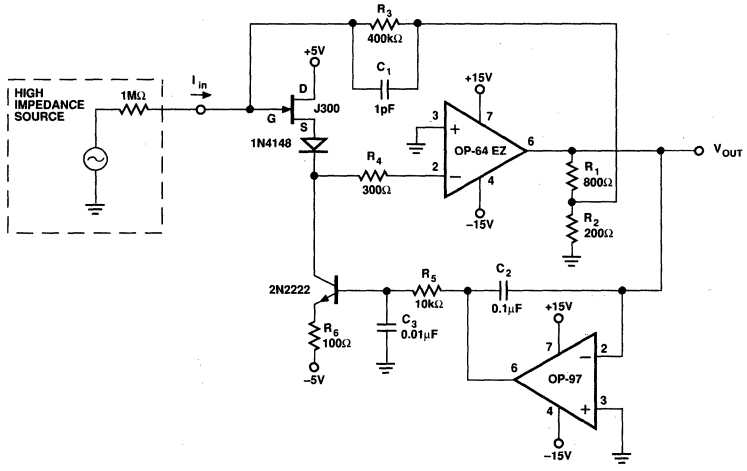


FIGURE 9: *Fast Transimpedance Amplifier*

FAST TRANSIMPEDANCE AMPLIFIER

The circuit shown in Figure 9 is a fast transimpedance amplifier designed to handle high speed signals from a high impedance source such as the output of a photomultiplier tube. The input current is amplified and converted to an output voltage by the transimpedance amplifier.

A JFET source-follower input is used to reduce the input bias current of the amplifier to 100 pA and lower the input current noise. Transimpedance of the amplifier is:

$$\frac{V_{OUT}}{I_{IN}} = \left(\frac{R_1}{R_2} + 1\right) R_3$$

and for the values shown equals

$$\frac{V_{OUT}}{I_{IN}} = \left(\frac{800\Omega}{200\Omega} + 1\right) 400k\Omega = 2V/\mu A$$

Figure 10 shows the output of the transimpedance amplifier when driven from a 1MΩ source impedance. The input signal of $10\mu A_{p-p}$ is converted into an output voltage of (10μA) 2V/μA = $20V_{p-p}$. Output slew rate is 100V/μs. The slew rate is limited by the combination of the capacitance of the JFET gate with the 1MΩ source impedance. For best performance, the stray input capacitance should be kept as small as possible. The OP-97 is used in an integrator loop to reduce the total amplifier offset voltage to under 25μV.

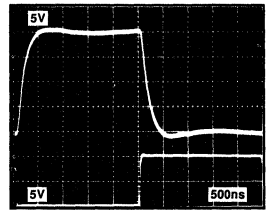


FIGURE 10: *Output of the Fast Transimpedance Amplifier*

OP-64 SPICE MACRO-MODEL

Figure 11 shows the node and net list for a SPICE macro-model of the OP-64. The model is a simplified version of the actual device and simulates important DC parameters such as V_{OS}, I_{OS}, I_B, A_{VO}, CMR, V_O and I_{SY}. AC parameters such as slew rate, gain and phase response and CMR change with frequency are also simulated by the model.

The model uses typical parameters for the OP-64. The poles and zeros in the model were determined from the actual open and closed-loop gain and phase response of the OP-64. In this way the model presents an accurate AC representation of the actual device. The model assumes an ambient temperature of 25°C (see following pages).

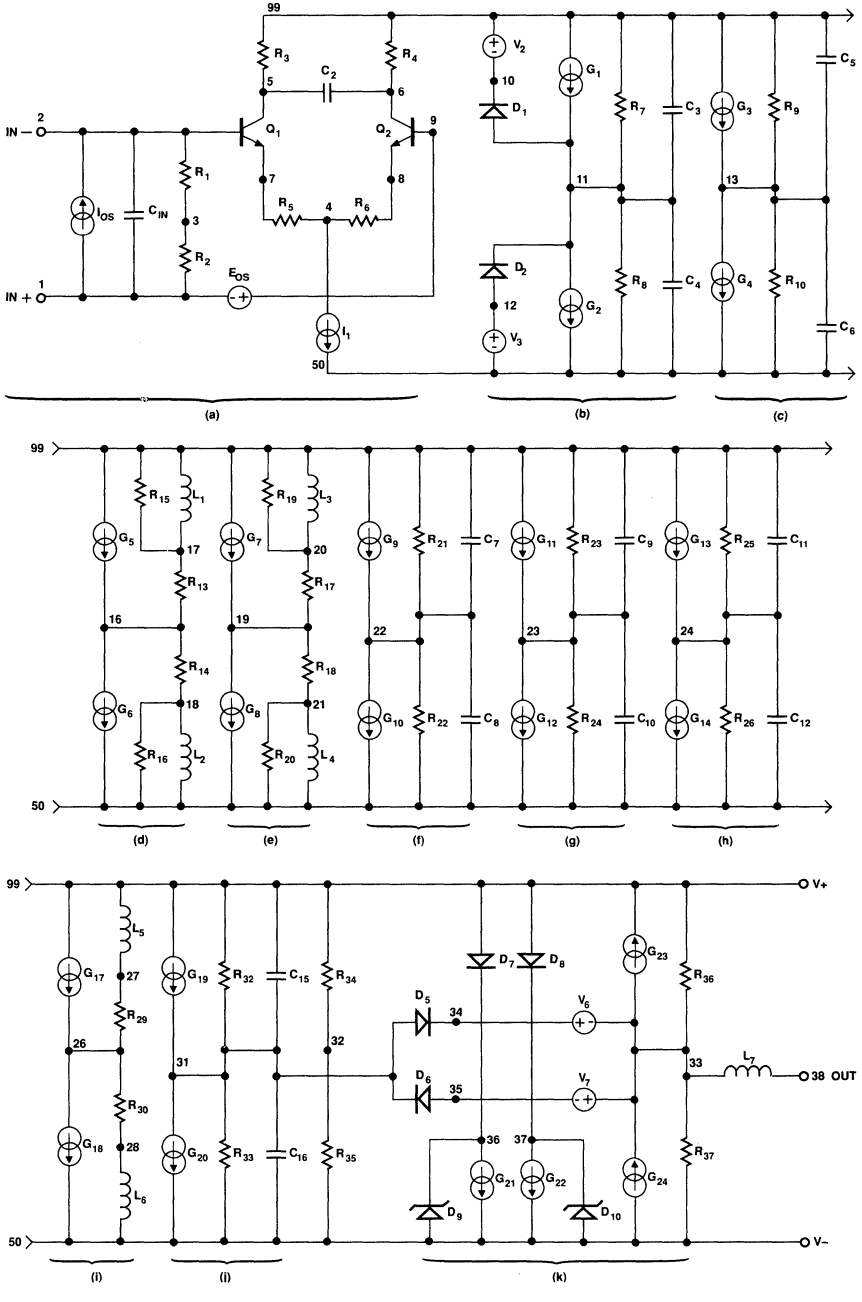


FIGURE 11a: *OP-64 SPICE Macro-Model Schematic and Node List*

* PSpice is a registered trademark of MicroSim Corporation.
** HSPICE is a tradename of Meta-Software, Inc.

```
OP-64 MACRO-MODEL © PMI 1989
*
* subckt OP-64 1  2 38  99  50
*
INPUT STAGE & POLE AT 39.8 MHz
*
r1   2   3        5E11
r2   1   3        5E11
r3   5   99       474.86
r4   6   99       474.86
r5   4   7        423.26
r6   4   8        423.26
cin  1   2        5E-12
c2   5   6        4.2106E-12
i1   4   50       1E-3
ios  1   2        1E-7
eos  9   1        poly(1) 26 32 4E-4 1
q1   5   2   7    qx
q2   6   9   8    qx
*
* SECOND STAGE & POLE AT 3.8 kHz
*
r7   11  99       7.1229E6
r8   11  50       7.1229E6
c3   11  99       5.88E-12
c4   11  50       5.88E-12
g1   99  11       poly(1) 5 6 4.31E-3 2.1059E-3
g2   11  50       poly(1) 6 5 4.31E-3 2.1059E-3
v2   99  10       2.25
v3   12  50       2.25
d1   11  10       dx
d2   12  11       dx
*
* POLE AT 39.8 MHz
*
r9   13  99       1E6
r10  13  50       1E6
c5   13  99       4E-15
c6   13  50       4E-15
g3   99  13       11 32 1E-6
g4   13  50       32 11 1E-6
*
* ZERO-POLE PAIR AT 26.5 MHz /159 MHz
*
r13  16  17       1E6
r14  16  18       1E6
r15  17  99       5E6
r16  18  50       5E6
l1   17  99       5.005E-3
l2   18  50       5.005E-3
g5   99  16       13 32 1E-6
g6   16  50       32 13 1E-6
*
* ZERO-POLE PAIR AT 31.8 MHz / 39.8 MHz
*
r17  19  20       1E6
r18  19  21       1E6
r19  20  99       2.5157E5
r20  21  50       2.5157E5
l3   20  99       1.006E-3
l4   21  50       1.006E-3
g7   99  19       16 32 1E-6
g8   19  50       32 16 1E-6
*
* POLE AT 100 MHz
*
r21  22  99       1E6
r22  22  50       1E6
c7   22  99       1.59E-15
c8   22  50       1.59E-15
g9   99  22       19 32 1E-6
g10  22  50       32 19 1E-6
*
*POLE AT 159 MHz
*
r23  23  99       1E6
r24  23  50       1E6
c9   23  99       1E-15
c10  23  50       1E-15
g11  99  23       22 32 1E-6
g12  23  50       32 22 1E-6
*
*POLE AT 159 MHz
*
r25  24  99       1E6
r26  24  50       1E6
c11  24  99       1E-15
c12  24  50       1E-15
g13  99  24       23 32 1E-6
g14  24  50       32 23 1E-6
*
*COMMON-MODE GAIN NETWORK WITH ZERO AT 20kHz
*
r29  26  27       1E6
r30  26  28       1E6
l5   27  99       7.9575
l6   28  50       7.9575
g17  99  26       33 32 1E-11
g18  26  50       32 33 1E-11
*
* POLE AT 159 MHz
*
r32  31  99       1E6
r33  31  50       1E6
c15  31  99       1E-15
c16  31  50       1E-15
g19  99  31       24 32 1E-6
g20  31  50       32 24 1E-6
*
* OUTPUT STAGE
*
r34  32  99       20.0E3
r35  32  50       20.0E3
r36  33  99       60
r37  33  50       60
l7   33  38       2.9E-7
g21  36  50       31  33   16.6666667E-3
g22  37  50       33  31   16.6666667E-3
g23  33  99       99  31   16.6666667E-3
g24  50  33       31  50   16.6666667E-3
v6   34  33       1.7
v7   33  35       1.7
d5   31  34       dx
d6   35  31       dx
d7   99  36       dx
d8   99  37       dx
d9   50  36       dy
d10  50  37       dy
*
* MODELS USED
*
.model qx NPN(BF=2500)
.model dx    D(IS=1E-15)
.model dy    D(IS=1E-15 BV=50)
.ends OP-64
```

FIGURE 11b: *OP-64 SPICE Net-List*

ANALOG DEVICES

High-Speed, Current Feedback Operational Amplifier

OP-160

FEATURES

- **Easy To Use – Drives Large Capacitive Loads**
- **Very High Slew Rate (A_V = +1) ..... 1300 V/µs Typ**
- **Bandwidth (A_V = +1) ..... 90MHz Typ**
- **Low Supply Current ..... 6.5mA Typ**
- **Bandwidth Independent of Gain**
- **Unity-Gain Stable**
- **Power Shutdown Pin**

APPLICATIONS

- **High-Speed Data Acquisition**
- **Communication Systems/RF Amplifiers**
- **Video Gain Block**
- **High-Speed Integrators**
- **Driving High-Speed ADCs**

ORDERING INFORMATION †

T_A = +25°C V_{IOS} MAX (mV)	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC 8-PIN	PACKAGE LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
5.0	OP160AZ*	—	OP160ARC/883	MIL
5.0	OP160FZ	OP160GP	—	XIND
5.0	—	OP160GS††	—	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on extended industrial temperature range parts in CerDIP and plastic packages.

†† For availability and burn-in information on SO package, contact your local sales office.

GENERAL DESCRIPTION

The OP-160 is an easy-to-use high-speed, current feedback op amp. Designed to handle large capacitive loads, the OP-160 resists unstable operation. The OP-160 combines PMI's high-speed complementary bipolar process with a current feedback topology for very high slew rate and wide bandwidth performance.

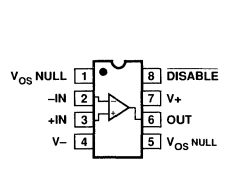
Slew rate of the OP-160 is typically 1300V/µs and is guaranteed to exceed 1000V/µs. In addition, the OP-160's current feedback design has the added advantage of nearly constant bandwidth versus gain. In a gain of +1 the –3dB bandwidth is 90MHz! The OP-160 also requires only 6.5mA of supply current, a considerable power savings over other high-speed amplifiers.

Applications using the OP-160 can be implemented with the same circuit assumptions utilized for conventional voltage feedback op amps. With its high speed and bandwidth, the OP-160 is ideal for a variety of applications including video amplifiers, RF amplifiers, and high-speed data acquisition systems.

The OP-160 is an easy-to-use alternative to the AD844, AD846, EL2020 and EL2030.

For applications requiring a high-speed, wide bandwidth dual amplifier, see the OP-260.

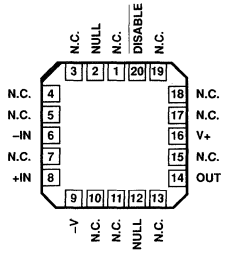
PIN CONNECTIONS



8-PIN EPOXY MINI-DIP (P-Suffix)

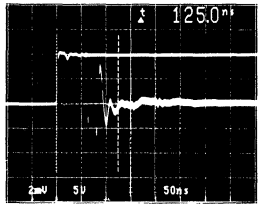
8-PIN CERDIP (Z-Suffix)

8-PIN SO (S-Suffix)



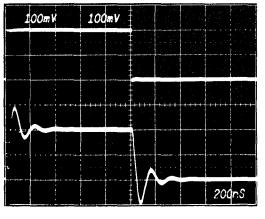
20-CONTACT LCC (RC-Suffix)

FAST SETTLING (0.01%)



A_V = –1, +10V STEP INPUT

DRIVES CAPACITIVE LOADS



A_V = +1, C_L = 1000pF

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Input Voltage ..... Supply Voltage
Differential Input Voltage ..... ±1V
Inverting Input Current ..... ±7mA Continuous
..... ±20mA Peak
Output Short-Circuit Duration ..... 10 sec
Operating Temperature Range
OP-160A (Z, RC) ..... –55°C to +125°C
OP-160A,F (Z) ..... –40°C to +85°C
OP-160G (P,S) ..... –40°C to +85°C
Storage Temperature (Z, RC) ..... –65°C to +175°C
(P, S) ..... –65°C to +150°C
Junction Temperature (Z, RC) ..... –65°C to +175°C
(P, S) ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $V_{CM} = 0V$, $R_F = 820\Omega$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		OP-160A/F MIN	OP-160A/F TYP	OP-160A/F MAX	OP-160G MIN	OP-160G TYP	OP-160G MAX	UNITS
Input Offset Voltage	V_{IOS}			–	2	5	–	2	5	mV
Input Bias Current	I_{B+} I_{B-}	Noninverting Input Inverting Input		– –	0.2 6	1 20	– –	0.4 10	1.5 30	µA
Input Bias Current Common-Mode Rejection Ratio	 $CMRRI_{B+}$ $CMRRI_{B-}$	$V_{CM} = \pm11V$ Noninverting Input Inverting Input		 – –	 40 30	 75 75	 – –	 50 40	 125 125	nA/V
Input Bias Current Power Supply Rejection Ratio	 $PSRRI_{B+}$ $PSRRI_{B-}$	$V_S = \pm9V$ to $\pm18V$ Noninverting Input Inverting Input		 – –	 1 20	 5 50	 – –	 1.5 25	 10 75	nA/V
Common-Mode Rejection	CMR	$V_{CM} = \pm11V$		60	65	–	60	65	–	dB
Power Supply Rejection	PSR	$V_S = \pm9V$ to $\pm18V$		74	80	–	74	80	–	dB
Open-Loop Transimpedance	R_T	$R_L = 500\Omega$ $V_O = \pm10V$		3	4	–	3	4	–	MΩ
Input Voltage Range	IVR	(Note 1)		±11	–	–	±11	–	–	V
Output Voltage Swing	V_O	$R_L = 500\Omega$		±11	–	–	±11	–	–	V
Output Current	I_O	$V_O = \pm10V$		±35	+60/–45	–	±35	+60/–45	–	mA
Supply Current	I_{SY}	No Load		–	6.5	8	–	6.5	8	mA
Slew Rate	SR	$A_V = +1$, $V_O = \pm10V$, $R_L = 500\Omega$, Test at $V_O = \pm5V$	All Grades	–	1300	–	–	1300	–	V/µs
		$A_V = +2$, $V_O = \pm10V$, $R_L = 500\Omega$, Test at $V_O = \pm5V$	OP-160A	1000	1300	–	–	–	–	
			OP-160F	800	1300	–	–	–	–	
			OP-160G	–	–	–	800	1300	–	

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $V_{CM} = 0V$, $R_F = 820\Omega$, $T_A = +25°C$, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS		OP-160A/F MIN	OP-160A/F TYP	OP-160A/F MAX	OP-160G MIN	OP-160G TYP	OP-160G MAX	UNITS
Rise Time	t_R	$A_V = +1$ $A_V = -1$	$V_O = \pm 100mV$	– –	4 6.4	– –	– –	4 6.4	– –	ns
–3dB Bandwidth	BW	–3dB Point $R_L = 500\Omega$	$A_V = -1$ $A_V = +1$ $A_V = +2$	– – –	55 90 65	– – –	– – –	55 90 65	– – –	MHz
Settling Time	t_s	$A_V = -1$, 10V Step 0.01% 0.1%		 – –	 125 75	 – –	 – –	 125 75	 – –	ns
Input Capacitance	C_{IN}	Noninverting Input		–	4	–	–	4	–	pF
Input Resistance	R_{IN}	Noninverting Input Inverting Input		– –	17 60	– –	– –	10 60	– –	MΩ Ω
Voltage Noise Density	e_n	$f = 1kHz$		–	5.5	–	–	5.5	–	$nV/\sqrt{Hz}$
Current Noise Density	i_n	$f = 1kHz$ Noninverting Input Inverting Input		 – –	 5 20	 – –	 – –	 5 20	 – –	$pA/\sqrt{Hz}$
Total Harmonic Distortion	THD	$f = 1kHz$, $A_V = +1$, $V_O = 2V_{RMS}$, $R_L = 500\Omega$		–	0.004	–	–	0.004	–	%
Differential Gain		$f = 3.58MHz$ $A_V = +1$, $R_L = 500\Omega$		–	0.04	–	–	0.04	–	%
Differential Phase		$f = 3.58MHz$ $A_V = +1$, $R_L = 500\Omega$		–	0.04	–	–	0.04	–	degrees
Disable Supply Current	$I_{SY\overline{DIS}}$	$\overline{DISABLE} = 0V$ No Load		–	2.3	–	–	2.3	–	mA

NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $V_{CM} = 0V$, $R_F = 820\Omega$, $-55°C \leq T_A \leq +125°C$, for the OP-160A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-160A MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{IOS}		–	3	8	mV
Average Input Offset Voltage Drift	TC_{VOS}		–	10	–	µV/°C
Input Bias Current	I_{B+} I_{B-}	Noninverting Input Inverting Input	– –	0.35 12	2 30	µA
Input Bias Current Common-Mode Rejection	 $CMRRI_{B+}$ $CMRRI_{B-}$	$V_{CM} = \pm 10V$ Noninverting Input Inverting Input	 – –	 55 45	 150 150	nA/V
Input Bias Current Power Supply Rejection Ratio	 $PSRRI_{B+}$ $PSRRI_{B-}$	$V_S = \pm 9V$ to $\pm 18V$ Noninverting Input Inverting Input	 – –	 2 40	 10 100	nA/V
Common-Mode Rejection	CMR	$V_{CM} = \pm 10V$	56	60	–	dB
Power Supply Rejection	PSR	$V_S = \pm 9V$ to $\pm 18V$	70	76	–	dB
Open-Loop Transimpedance	R_T	$R_L = 500\Omega$ $V_O = \pm 10V$	1.75	3	–	MΩ
Input Voltage Range	IVR	(Note 1)	±10	–	–	V
Output Voltage Swing	V_O	$R_L = 500\Omega$	±10	–	–	V
Supply Current	I_{SY}	No Load	–	6.75	9	mA

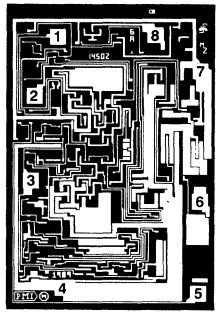
NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ $V_{CM} = 0V$, $R_F = 820\Omega$, $-40°C \le T_A \le +85°C$, for the OP-160F/G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-160F MIN	OP-160F TYP	OP-160F MAX	OP-160G MIN	OP-160G TYP	OP-160G MAX	UNITS
Input Offset Voltage	V_{IOS}		–	2.75	8	–	2.75	8	mV
Average Input Offset Voltage	TCV_{OS}		–	10	–	–	10	–	µV/°C
Input Bias Current	I_{B+} I_{B-}	Noninverting Input Inverting Input	– –	0.3 10	2 30	– –	0.5 15	3 40	µA
Input Bias Current Common-Mode Rejection Ratio		$V_{CM} = \pm 10V$							nA/V
	$CMRRI_{B+}$	Noninverting Input	–	45	150	–	55	250	
	$CMRRI_{B-}$	Inverting Input	–	35	150	–	45	250	
Input Bias Current Power Supply Rejection Ratio		$V_S = \pm 9V$ to $\pm 18V$							nA/V
	$PSRRI_{B+}$	Noninverting Input	–	1.5	10	–	2.5	20	
	$PSRRI_{B-}$	Inverting Input	–	30	100	–	3.5	150	
Common-Mode Rejection	CMR	$V_{CM} = \pm 10V$	56	62	–	56	62	–	dB
Power Supply Rejection	PSR	$V_S = \pm 9V$ to $\pm 18V$	70	80	–	70	80	–	dB
Open-Loop Transimpedance	R_T	$R_L = 500\Omega$ $V_O = \pm 10V$	1.75	3	–	1.75	3	–	MΩ
Input Voltage Range	IVR	(Note 1)	±10	–	–	±10	–	–	V
Output Voltage Swing	V_O	$R_L = 500\Omega$	±10	–	–	±10	–	–	V
Supply Current	I_{SY}	No Load, Both Amplifiers	–	6.75	9	–	6.75	9	mA

NOTE:
1. Guaranteed by CMR test.

DICE CHARACTERISTICS



DIE SIZE 0.071 x 0.099 inch, 7,029 sq. mils
(1.80 x 2.52 mm, 4.54 sq. mm)

1. V_{OS} NULL
2. –IN
3. +IN
4. V–
5. V_{OS} NULL
6. OUT
7. V+
8. $\overline{\text{DISABLE}}$

WAFER TEST LIMITS at $V_S = \pm 15V$, $V_{CM} = 0V$, $R_F = 820\Omega$, $T_A = +25°C$, unless otherwise noted.

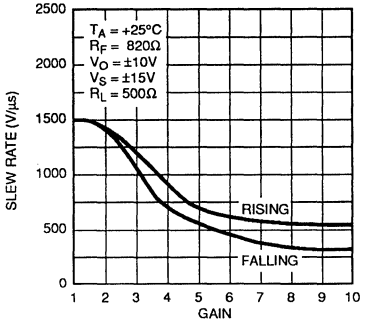
PARAMETER	SYMBOL	CONDITIONS	OP-160GBC LIMITS	UNITS
Input Offset Voltage	V_{IOS}		5	mV MAX
Input Bias Current	I_{B+} I_{B-}	Noninverting Input Inverting Input	1.5 30	µA MAX
Input Bias Current Common-Mode Rejection Ratio	 $CMRRI_{B+}$ $CMRRI_{B-}$	$V_{CM} = \pm 11V$ Noninverting Input Inverting Input	 125 125	nA/V MAX
Input Bias Current Power Supply Rejection Ratio	 $PSRRI_{B+}$ $PSRRI_{B-}$	$V_S = \pm 9V$ to $\pm 18V$ Noninverting Input Inverting Input	 10 75	nA/V MAX
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	60	dB MIN
Power Supply Rejection	PSR	$V_S = \pm 9V$ to $\pm 18V$	74	dB MIN
Open-Loop Transimpedance	R_T	$R_L = 500\Omega$ $V_O = \pm 10V$	3	MΩ MIN
Input Voltage Range	IVR		±11	V MIN
Output Voltage Swing	V_O	$R_L = 500\Omega$	±11	V MIN
Supply Current	I_{SY}	No Load	8	mA MAX

NOTES:
1. Guaranteed by CMR test.

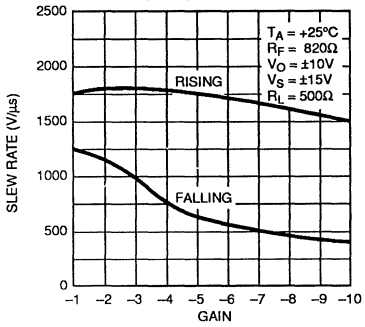
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

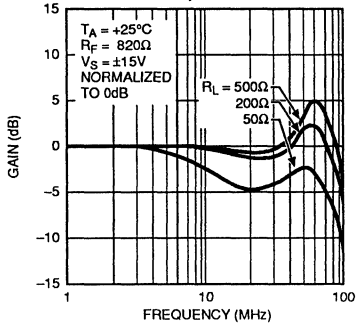
SLEW RATE vs NONINVERTING GAIN



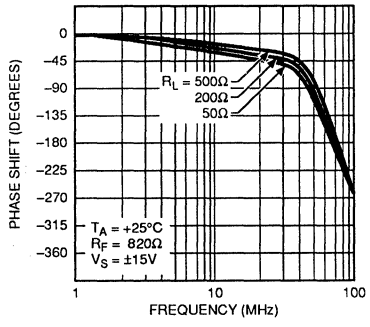
SLEW RATE vs INVERTING GAIN



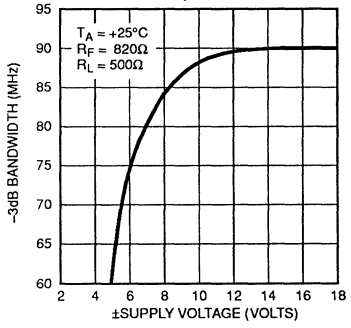
GAIN vs FREQUENCY A_V = +1



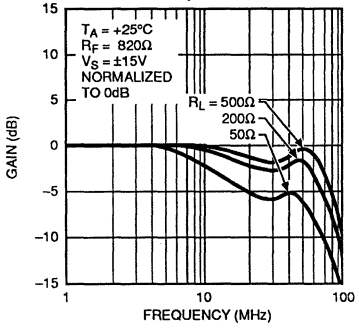
PHASE SHIFT vs FREQUENCY A_V = +1



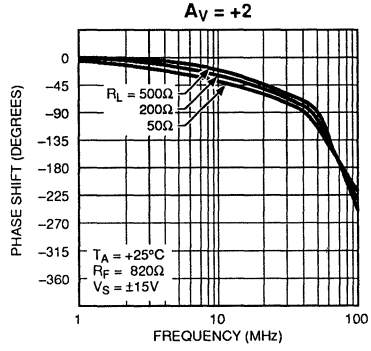
–3dB BANDWIDTH vs SUPPLY VOLTAGE A_V = +1



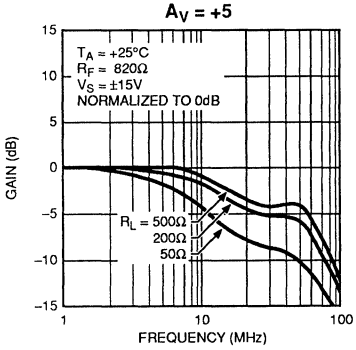
GAIN vs FREQUENCY A_V = +2



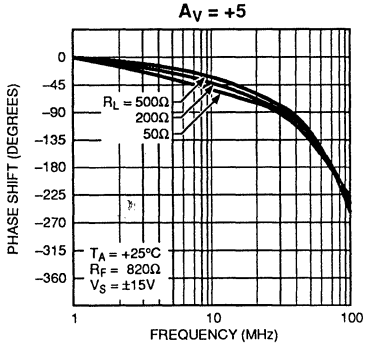
PHASE SHIFT vs FREQUENCY A_V = +2



GAIN vs FREQUENCY A_V = +5

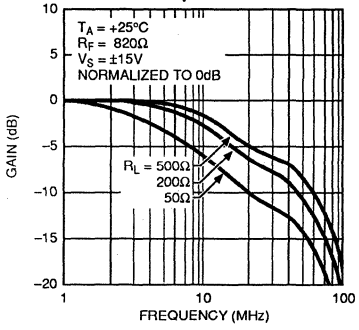


PHASE SHIFT vs FREQUENCY A_V = +5

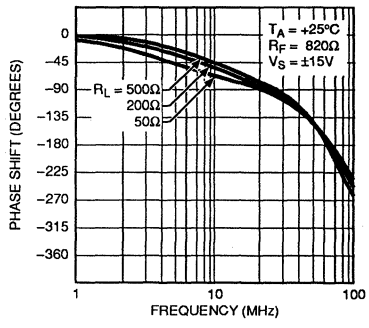


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

GAIN vs FREQUENCY
A_V = +10



PHASE SHIFT vs FREQUENCY
A_V = +10



GAIN vs FREQUENCY
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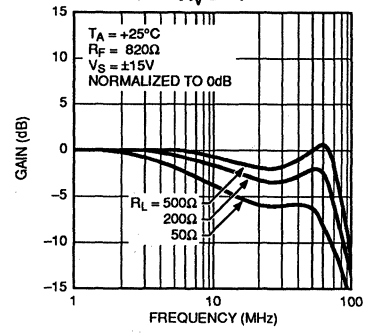

PHASE SHIFT vs FREQUENCY
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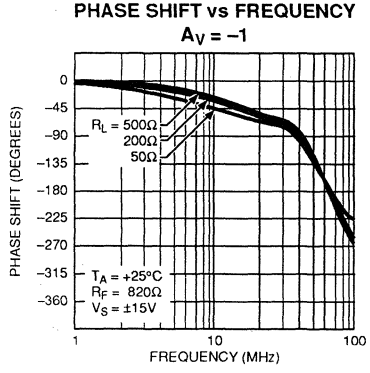

GAIN vs FREQUENCY
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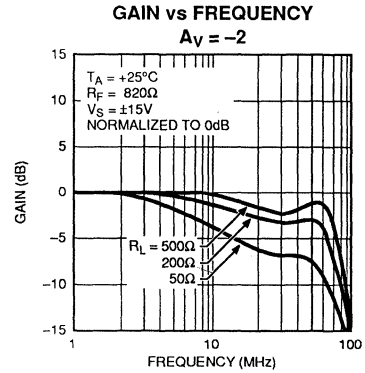
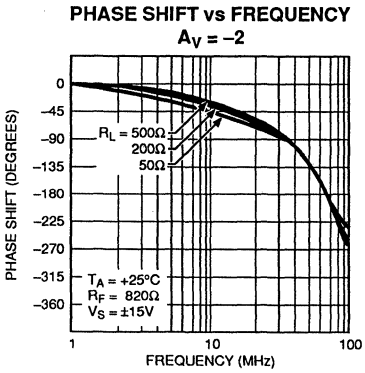


PHASE SHIFT vs FREQUENCY
A_V = –2



GAIN vs FREQUENCY
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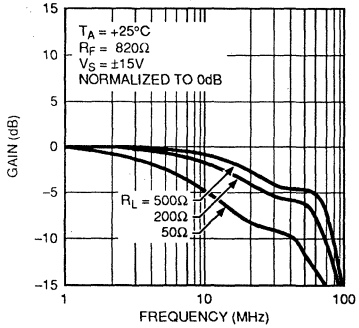
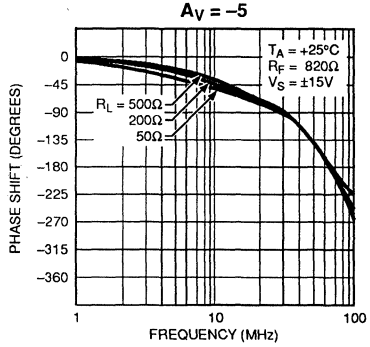
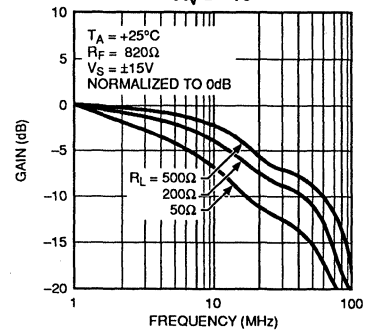


PHASE SHIFT vs FREQUENCY
A_V = –5



GAIN vs FREQUENCY
A_V = –10



TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

PHASE SHIFT vs FREQUENCY
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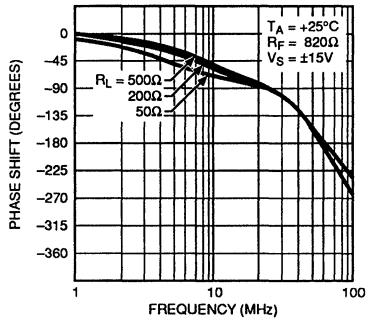
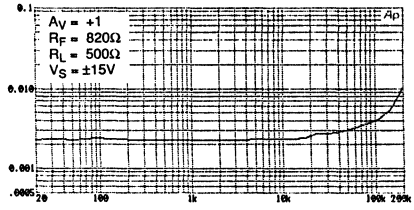
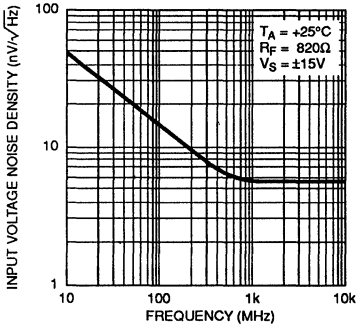


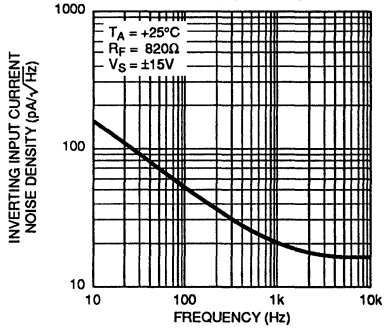
TOTAL HARMONIC DISTORTION vs FREQUENCY



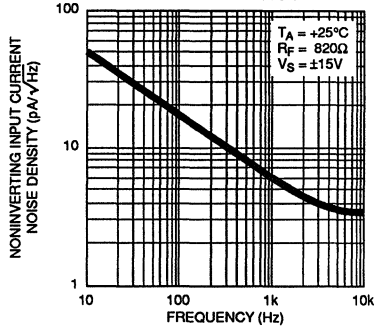
INPUT VOLTAGE NOISE DENSITY vs FREQUENCY



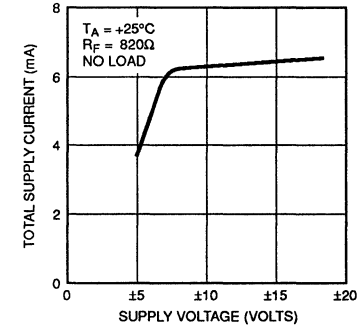
INVERTING INPUT CURRENT NOISE DENSITY vs FREQUENCY



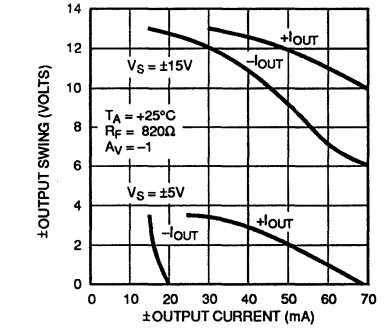
NONINVERTING INPUT CURRENT NOISE DENSITY vs FREQUENCY



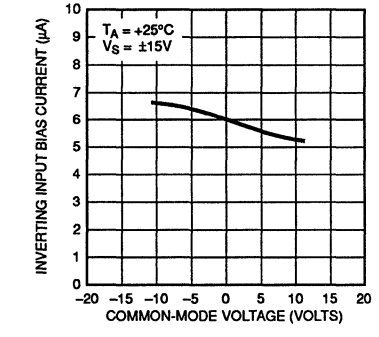
TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE



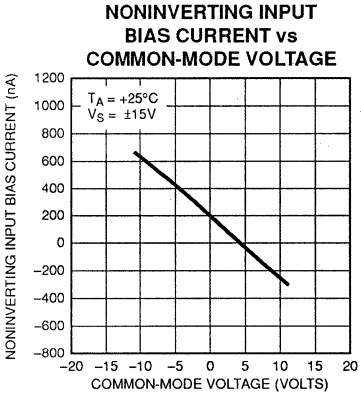
OUTPUT CURRENT vs OUTPUT SWING

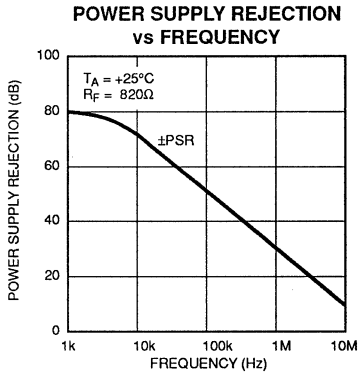


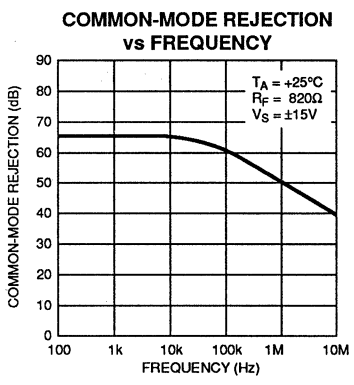
INVERTING INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



TYPICAL PERFORMANCE CHARACTERISTICS *Continued*







APPLICATIONS INFORMATION

CURRENT VERSUS VOLTAGE FEEDBACK AMPLIFIERS

The OP-160 employs a unique circuit topology that sets it apart from conventional op amps. By using a transimpedance amplifier configuration, the OP-160 provides substantial improvements in bandwidth and slew rate over voltage feedback op amps. Figure 1 compares models of these two different amplifier configurations.

A voltage feedback op amp multiplies the differential voltage at its inputs by its open-loop gain. The feedback loop forces the output to a voltage that, when divided by R_1 and R_2, equalizes the input voltages. Unlike a voltage feedback op amp, which has high impedance inputs, the current feedback amplifier has a high and a low impedance input. The current feedback amplifier's input stage consists of a unity-gain voltage buffer between the noninverting and inverting inputs. The inverting "input" is in reality a low impedance output. Current can flow into or out of the inverting input. A transimpedance stage follows the input buffer that converts the buffer output current into a linearly proportional amplifier output voltage.

The current feedback amplifier loop works in the following fashion (Figure 1b). As the noninverting input voltage rises, the inverting input follows and the buffer sources current through R_1.

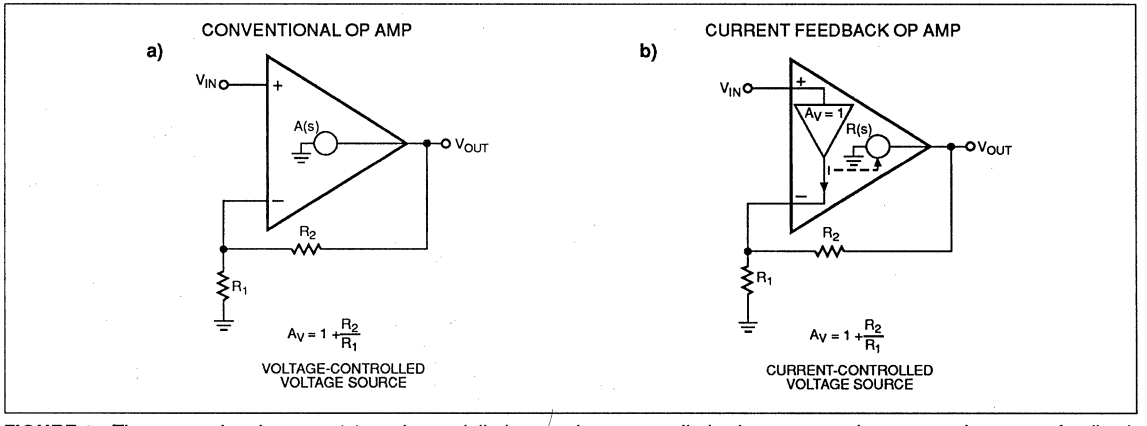


FIGURE 1: *The conventional op amp (a) can be modelled as a voltage-controlled voltage source. In contrast, the current feedback op amp (b), resembles a current-controlled voltage source.*

This current, multiplied by the transimpedance stage, causes the amplifier's output voltage to rise until the current flowing into R_2 from the amplifier's output equalizes the current through R_1, replacing the buffer's output current. At steady state, only a very small buffer output current must flow to sustain the proper output voltage. The ratio $(1 + R_2/R_1)$ determines the closed-loop gain of the circuit. The result is that when designing with current feedback amplifiers the familiar op amp assumptions can still be used for circuit analysis:

1. The voltage across the inputs equals zero.
2. The current into the inputs equals zero.

BANDWIDTH VERSUS GAIN

A unique feature of the current feedback amplifier design is that the closed-loop bandwidth remains relatively constant as a function of closed-loop gain. Voltage feedback op amps suffer from a bandwidth reduction as closed-loop gain increases, as quantified by the gain-bandwidth product (GBWP). This is illustrated in Figure 2 which shows the frequency response of the OP-160 for various closed-loop gains and the frequency response of a voltage feedback op amp with a gain-bandwidth product of 30MHz. The bandwidth of the OP-160 is much less dependent upon closed-loop gain than the voltage feedback op amp.

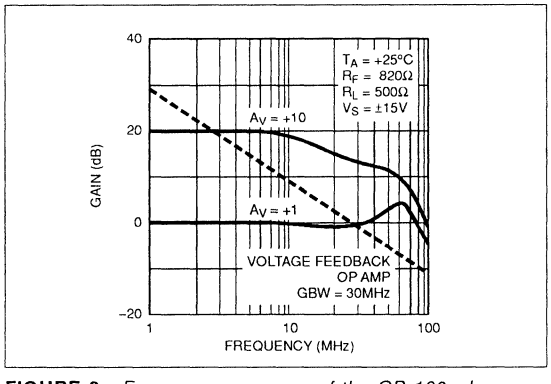


FIGURE 2: *Frequency response of the OP-160 when connected in various closed-loop gains with R_F = 820Ω and R_L = 100Ω. Note that the frequency response of the OP-160 does not follow the asymptotic roll-off characteristic of a voltage feedback op amp.*

FEEDBACK RESISTANCE AND BANDWIDTH

The closed-loop frequency response of the OP-160 shown in Figure 2 applies for a fixed feedback resistor of 820Ω. The frequency response of a current feedback amplifier is primarily dependent on the value of the feedback resistor value. The design of the OP-160 has been optimized for a feedback resistance of 820Ω. By holding the feedback resistor value constant, the –3dB frequency point will also remain constant within a moderate range of closed-loop gain.

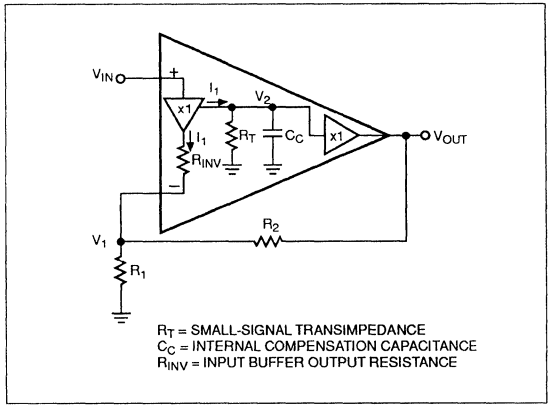


FIGURE 3: *Simple frequency response model of the current feedback amplifier.*

The model shown in Figure 3 can be used to determine the frequency response of a current feedback amplifier. With this model, the frequency response dependency on the value of the feedback resistance is easily seen.

From the model of Figure 3, nodal equations may be written for V_1 and V_2.

$$V_1 = \frac{V_{IN}\left(\frac{R_2}{R_{INV}}\right) + V_{OUT}}{1 + \frac{R_2}{R_1} + \frac{R_2}{R_{INV}}}$$

$$V_2 = \frac{R_T}{1 + sR_T C_C} I_1$$

where $I_1 = \frac{V_{IN} - V_1}{R_{INV}} = V_1\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{V_{OUT}}{R_2}$, and $V_{OUT} = V_2$

Combining these equations yields:

$$V_{OUT} = \left[\left(\frac{V_{IN}\left(\frac{R_2}{R_{INV}}\right) + V_{OUT}}{1 + \frac{R_2}{R_1} + \frac{R_2}{R_{INV}}}\right)\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{V_{OUT}}{R_2}\right] \frac{R_T}{1 + sR_T C_C}$$

If the transimpedance of the amplifier, R_T, is » R_2 and R_{INV}, then the transfer function may be simplified to:

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{1 + \frac{R_2}{R_1}}{1 + s\left[R_2 + \left(1 + \frac{R_2}{R_1}\right)R_{INV}\right] C_C}$$

The transfer function shows that the dominant closed-loop pole is mainly dependent on the value of the feedback resistance, R_2, and the internal compensation capacitor, C_C. For example, at unity gain, where R_1 is infinite, R_2 determines the –3dB frequency.

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{1}{1 + sR_2 C_C}$$

$$f_{-3dB} = \frac{1}{2\pi R_2 C_C}$$

where $R_2 \gg R_{INV}$

For higher gains, the –3dB frequency is determined by R_2 plus the output resistance of the buffer, R_{INV} (typically 60Ω), which is multiplied by the closed-loop gain. As the closed-loop gain increases, the multiplying effect on R_{INV} becomes dominant, causing the bandwidth to decrease. However, the closed-loop bandwidth of a current feedback amplifier still far exceeds that of a voltage feedback op amp for moderate values of gain.

Figure 4 shows the effect of the feedback resistance on the bandwidth of the OP-160 for various closed-loop gains.

SLEW RATE AND GAIN

The simplified schematic in Figure 5 shows the three stages of the OP-160. The input stage consists of a unity-gain emitter-follower amplifier. Q_5 and Q_6 form a class AB output stage at the inverting input which can source or sink current. The current flowing through the inverting input is sensed by the top current mirror, formed by Q_7, Q_9, and Q_{10}, or the bottom current mirror, formed by Q_8, Q_{11}, and Q_{12}. When the buffer sources current to a load, current flows out of the inverting input, increasing Q_5's collector current and causing more current to flow through Q_9

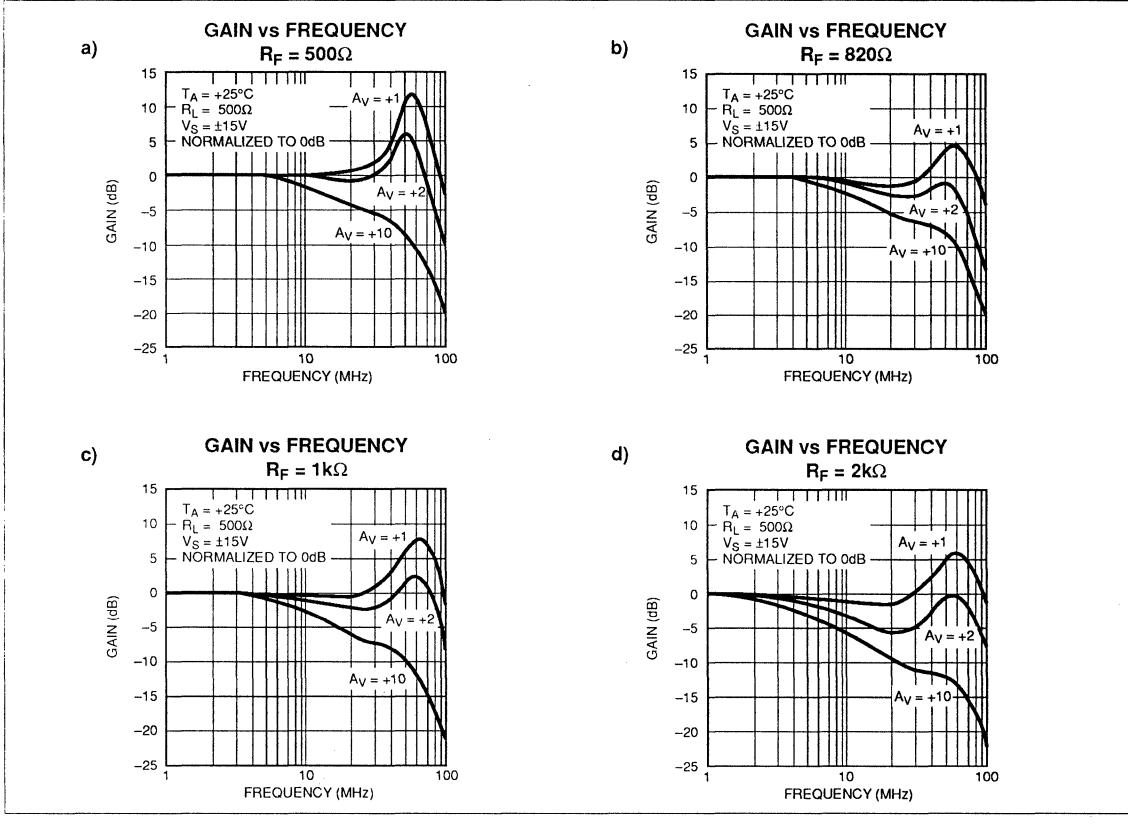


FIGURE 4: *Bandwidth will vary with feedback resistance. Peaking increases as the feedback resistance is decreased. R_F = 820Ω is the recommended value. All graphs are normalized to 0dB.*

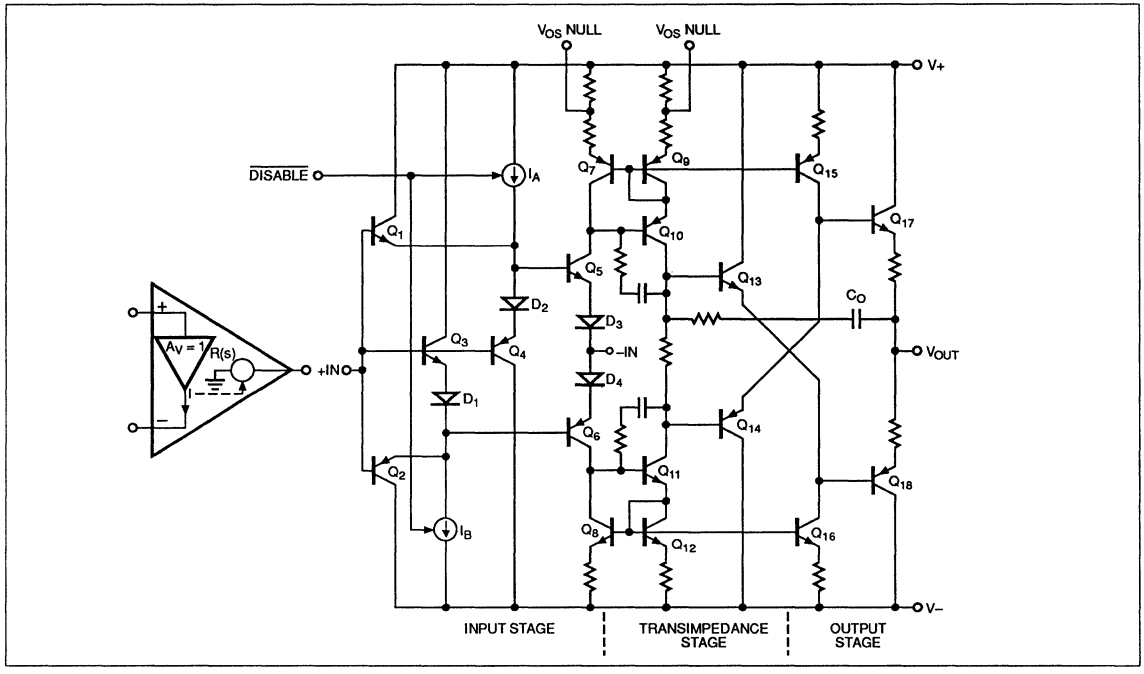


FIGURE 5: *Simplified schematic of the OP-160 showing the three stages of the amplifier.*

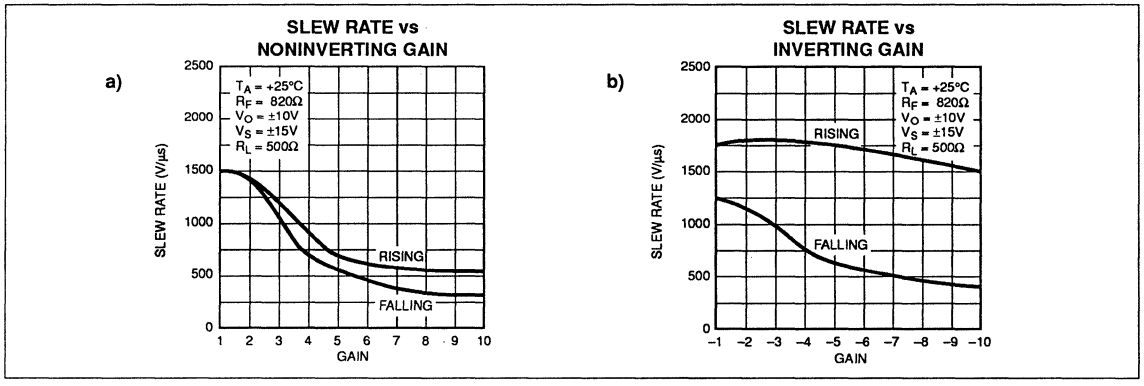


FIGURE 6: *Slew rate of the OP-160 in noninverting (a) and inverting (b) configurations.*

and Q_{15}. This increases the base drive to the output transistor Q_{17}. Simultaneously, the increased current in Q_9 drives Q_{13} which reduces base drive to the complementary output transistor Q_{18}. This push-pull action produces a very fast output slew rate. For a small voltage step, the OP-160's slew rate is dependent on the available current from the two current sources (I_A and I_B) that drive Q_5 and Q_6.

To increase the slew rate, transistors Q_1 and Q_2 have been added to boost the base drive to Q_5 and Q_6. In low gains, a large input step will turn on Q_1 or Q_2 increasing the slew rate dramatically as illustrated in Figure 6.

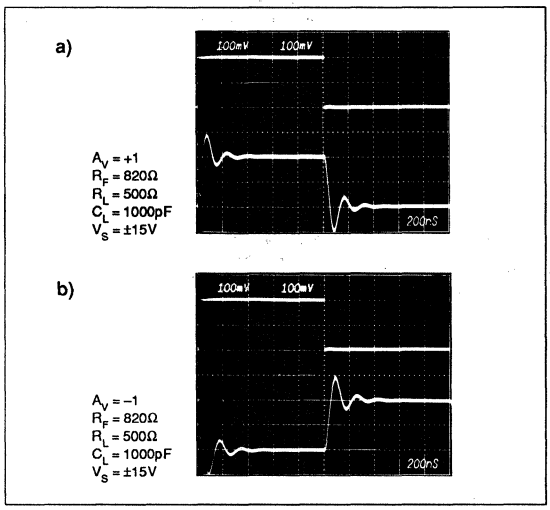


FIGURE 7: *The OP-160 remains stable when driving large capacitive loads.*

DRIVING CAPACITIVE LOADS

The OP-160 is capable of driving capacitive loads at high speed. Output stage compensation is used to reduce the effects of capacitive loading. With low capacitive loads, the gain from the compensation node to the output is unity and C_O does not contribute to the overall compensation. As the load capacitance is increased, a pole is formed with the output resistance of the amplifier. The gain is reduced and C_O begins to contribute to the overall compensation capacitance leading to a reduction in bandwidth. As the load capacitance is increased, the bandwidth is further reduced and the amplifier remains stable. Figure 7 shows the OP-160 in a gain of +1 and –1 driving a 1000pF load without any sign of oscillation. Table 1 shows the effects of capacitive load on the –3dB bandwidth for $A_V = -1$.

TABLE 1: –3dB Bandwidth vs. Capacitive Load; $A_V = -1$, $R_F = 820\Omega$, $R_L = 500\Omega$, $V_S = \pm 15V$.

CAPACITANCE (pF)	–3dB BANDWIDTH (MHz)
0	55
20	55
50	50
75	48
100	40
200	24
500	13
1000	9

AMPLIFIER NOISE PERFORMANCE

Simplified noise models of the OP-160 in the noninverting and inverting amplifier configurations are shown in Figure 8. All resistors are assumed to be noiseless.

For the noninverting amplifier, the equivalent input voltage noise, referred to the input, is:

$$E_N = \sqrt{(R_S\, i_{nn})^2 + e_n^2 + (R_2\, i_{ni})^2 / A_{VCL}}$$

where:

E_N = total input referred noise
e_n = amplifier voltage noise
i_{nn} = noninverting input current noise
i_{ni} = inverting input current noise
R_S = source resistance
A_{VCL} = closed loop gain = $1 + R_2/R_1$

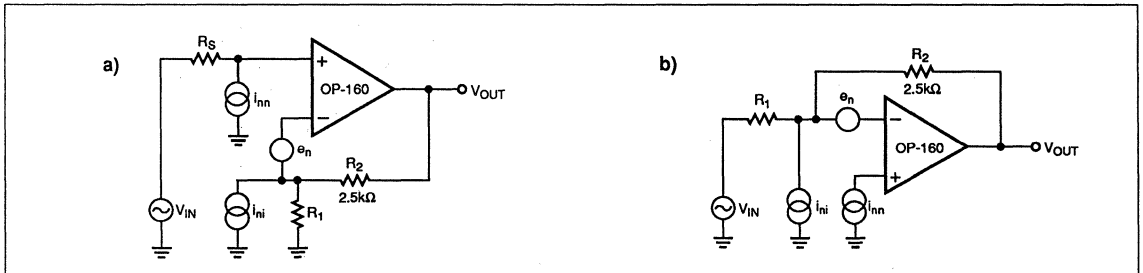


FIGURE 8: *Simplified noise models for the OP-160 in noninverting (a) and inverting (b) gain.*

For the inverting amplifier, the equivalent input voltage noise, referred to the input, is:

$$E_N = \sqrt{e_n^2 \left(\frac{1+|A_{VCL}|}{|A_{VCL}|}\right) + \frac{(R_2\, i_{ni})^2}{|A_{VCL}|}}$$

assuming $R_S \ll R_1$. A_{VCL} = closed-loop gain = $-R_2/R_1$.

Typical values @ 1kHz for the noise parameters of the OP-160 are:

e_n = 5.5nV/$\sqrt{Hz}$
i_{nn} = 5pA/$\sqrt{Hz}$
i_{ni} = 20pA/$\sqrt{Hz}$

SHORT-CIRCUIT PERFORMANCE

To avoid sacrificing bandwidth and slew rate performance the OP-160's output is **not** short-circuit protected. Do not short the amplifier's output to ground or to the supplies. Also, the buffer output current should not exceed a value of ±20mA peak or ±7mA continuous.

POWER SUPPLY BYPASSING AND LAYOUT CONSIDERATIONS

Proper power supply bypassing is critical in all high-frequency circuit applications. For stable operation of the OP-160, the power supplies must maintain a low impedance-to-ground over an extremely wide bandwidth. This is most critical when driving a low resistance or large capacitance, since the current required to drive the load comes from the power supplies. A 10µF and 0.1µF bypass capacitor are recommended for each supply, as shown in Figure 9, and will provide adequate high-frequency bypassing in most applications. The bypass capacitors should be placed at the supply pins of the OP-160. As with all high frequency amplifiers, circuit layout is a critical factor in obtaining optimum performance from the OP-160. Proper high-frequency layout reduces unwanted signal coupling in the circuit. When breadboarding a high-frequency circuit, use direct point-to-point wiring, keeping all lead lengths as short as possible. Do not use wire-wrap boards or "plug-in" prototyping boards.

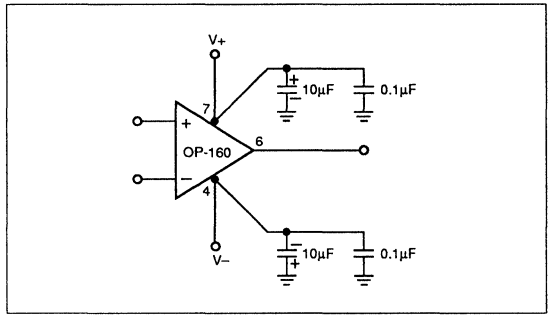


FIGURE 9: *Proper power supplying bypassing is required to obtain optimum performance with the OP-160.*

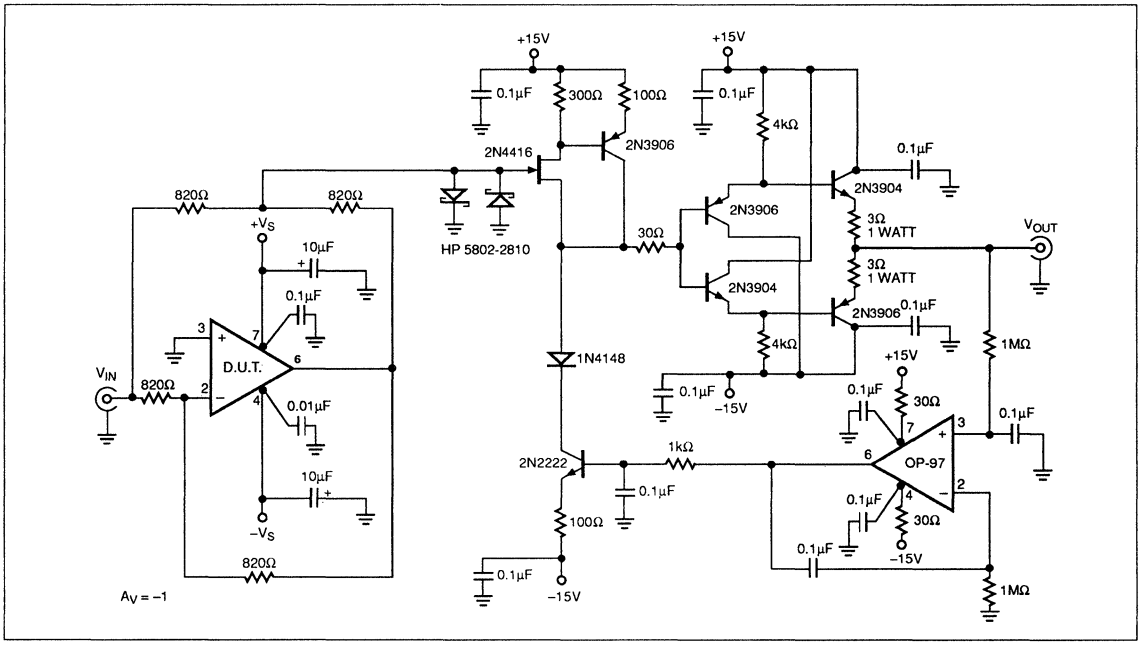


FIGURE 10: *High-Speed Settling Time Fixture (for 0.1 and 0.01%)*

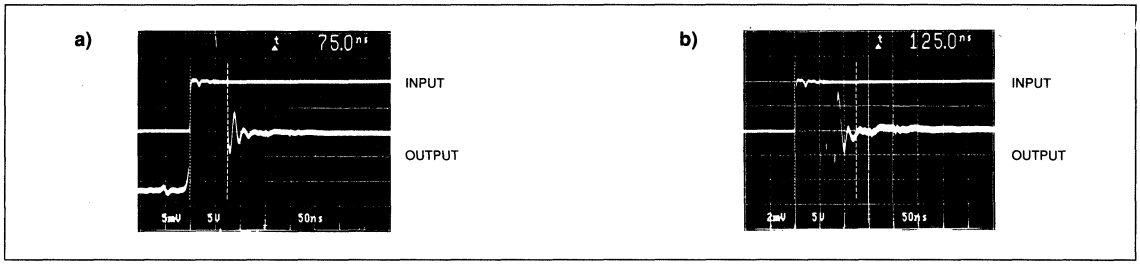


FIGURE 11: *Settling Time Performance of the OP-160 to 0.1% (a) and 0.01% (b) $A_V = -1$*

SETTLING TIME

Settling time is the time between when the input signal begins to change and when the output permanently enters a prescribed error band. Figure 10 illustrates the artificial summing node test configuration, used to characterize the OP-160 settling time. The OP-160 is set in a gain of –1 with a 10V step input. The error bands on the output are 5mV and 0.5mV, respectively, for 0.1% and 0.01% accuracy.

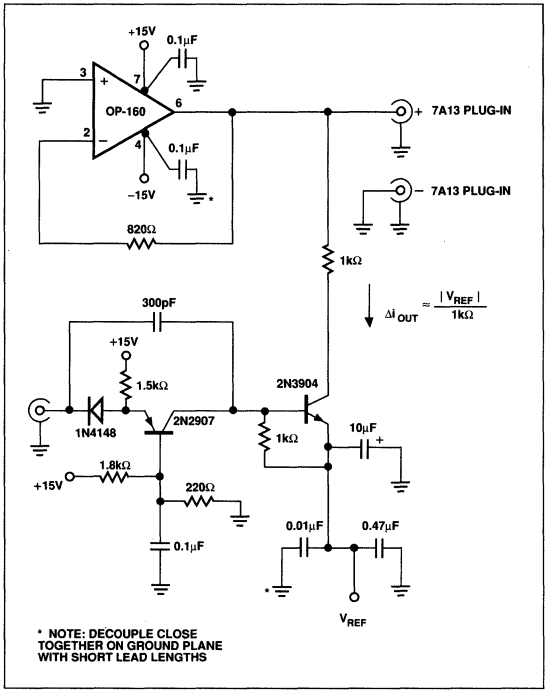


FIGURE 12: *Transient Output Impedance Test Fixture*

The test circuit, built on a copper clad circuit board, has a FET input stage which maintains extremely low loading capacitance at the artificial sum node. Preceding stages are complementary emitter follower stages, providing adequate drive current for a 50Ω oscilloscope input. The OP-97 establishes biasing for the input stage, and eliminates excessive offset voltage errors.

TRANSIENT OUTPUT IMPEDANCE

Settling characteristics of operational amplifiers also includes an amplifier's ability to recover, i.e., settle, from a transient current output load condition. An example of this includes an op amp driving the input from a SAR type A/D converter. Although the comparison point of the converter is usually diode clamped, the input swing of plus-and-minus a diode drop still gives rise to a significant modulation of input current. If the closed-loop output impedance is low enough and bandwidth of the amplifier is sufficiently large, the output will settle before the converter makes a comparison decision which will prevent linearity errors or missing codes.

Figure 12 shows a settling measurement circuit for evaluating recovery from an output current transient. An output disturbing current generator provides the transient change in output load current of 1mA. As seen in Figure 13, the OP-160 has extremely fast recovery of 80ns, (to 0.01%), for a 1mA load transient. The performance makes it an ideal amplifier for data acquisition systems.

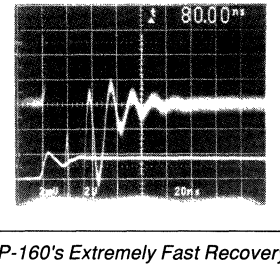


FIGURE 13: *OP-160's Extremely Fast Recovery Time from a 1mA Load Transient to 1mV (0.01%)*

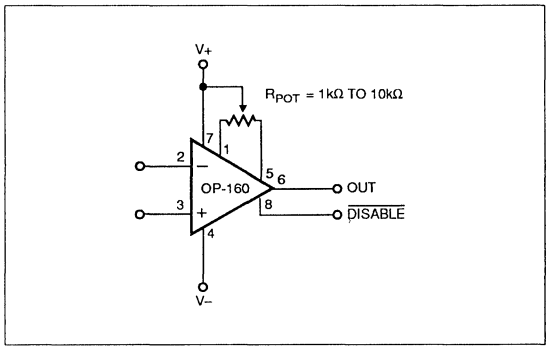


FIGURE 14: *Input Offset Voltage Nulling*

OFFSET VOLTAGE ADJUSTMENT

Offset voltage is adjusted with a 20kΩ potentiometer as shown in Figure 14. The potentiometer should be connected between pins 1 and 5 with its wiper connected to the V+ supply. The typical trim range is ±40mV.

DISABLE AMPLIFIER SHUTDOWN

Pin 8 of the OP-160, DISABLE, is an amplifier shutdown control input. The OP-160 operates normally when Pin 8 is left floating. When greater than 1000µA is drawn from the DISABLE pin, the OP-160 is disabled. To draw current from the DISABLE pin, an open collector output logic gate or a discrete NPN transistor can be used as shown in Figure 15. An internal resistor limits the DISABLE current to around 500µA if the DISABLE pin is grounded with the OP-160 powered by ±15V supplies. These logic interface methods have the added advantage of level shifting the TTL signal to whatever supply voltage is used to power the OP-160.

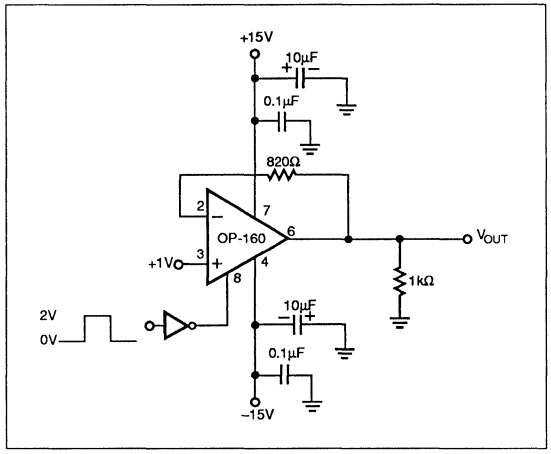


FIGURE 16: *DISABLE Turn-On/Turn-Off Test Circuit*

In the DISABLE mode, the OP-160 maintains 40dB of input-to-output isolation if the input signal remains below ±1.5V. Output resistance is very high, over 100kΩ, if the output is driven by signals of less than ±1.5V. Higher signals will be distorted.

Figure 16 shows a test circuit for measuring the turn-on and turn-off times for the OP-160. The OP-160 is in a gain of +1 with a +1V DC input. As the input pulse to the inverter rises its output falls, drawing current from the DISABLE pin and disabling the

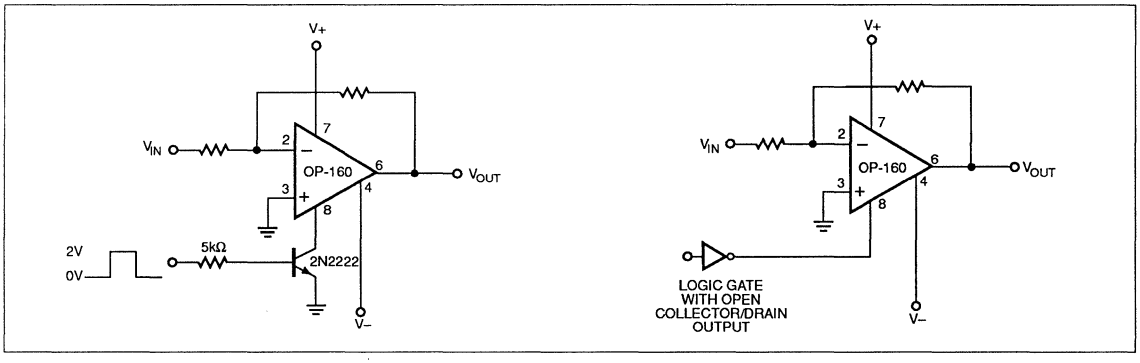


FIGURE 15: *Simple circuits allow the OP-160 to be shut down.*

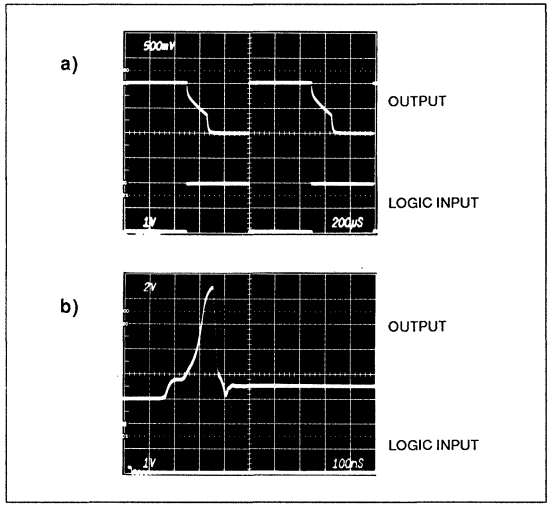


FIGURE 17: *(a) OP-160 turn-on and turn-off performance. (b) Expanded scale showing turn-on performance of the OP-160. Be aware of the high-frequency spike during turn-on.*

amplifier. The output voltage delay is shown in Figure 17 and takes 200µs to reach ground. The turn-on time is much quicker than the turn-off time. In this situation as the input to the inverter falls its output rises, returning the OP-160 to normal operation. The amplifier's output reaches its proper output voltage in 450ns.

OVERDRIVE RECOVERY

Figure 19 shows the overdrive recovery performance of the OP-160. Typical recovery time is 120ns from positive and negative overdrive.

APPLICATIONS

NONINVERTING AMPLIFIER

The OP-160 can be used as a voltage-follower or noninverting amplifier as shown in Figure 20. A current feedback amplifier in this configuration yields the same transfer function as a voltage feedback op amp:

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_2}{R_1}$$

Remember to use a 820Ω feedback resistor in voltage-follower applications.

In noninverting applications, stray capacitance at the inverting input of a current feedback amplifier will cause peaking which will increase as the closed-loop gain decreases. The gain setting resistor, R_1, is in parallel with this stray capacitance creating a zero in the

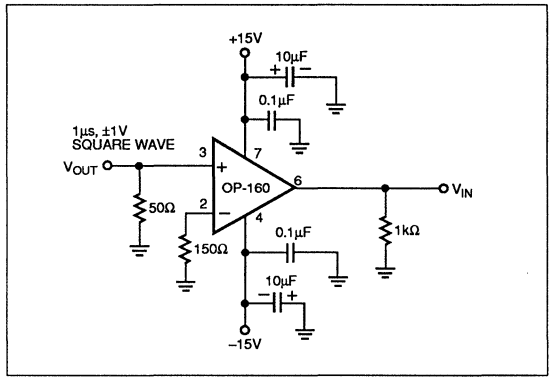


FIGURE 18: *Overdrive Recovery Test Circuit*

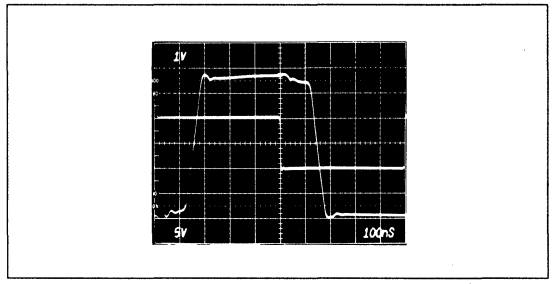


FIGURE 19: *The OP-160 recovers from both positive and negative overdrive in 120ns.*

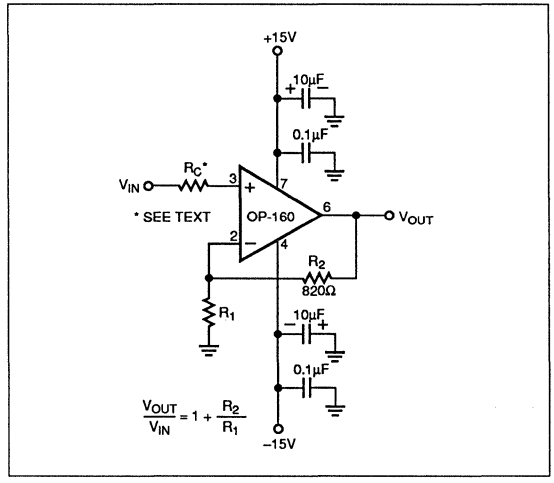


FIGURE 20: *The OP-160 as a voltage follower or noninverting amplifier.*

closed-loop response. For large noninverting gains, R_1 is small, creating a very high-frequency open-loop pole which has limited effect on the closed-loop response. As the noninverting gain is decreased, R_1 becomes larger and the stray zero becomes lower in frequency, having a much greater effect on the closed-loop response. To reduce peaking at low noninverting gains, place a series resistor, R_C, in series with the noninverting input as shown in Figure 20. This resistor combines with the stray capacitance at the noninverting input to form a low-pass filter that will reduce the peaking. The value of R_C should be determined experimentally in the actual PCB layout. Less peaking will occur in inverting gain configurations since the inverting input is a virtual ground which forces a constant voltage across the stray capacitance.

A common practice to stabilize voltage feedback op amps is to use a capacitor across the feedback resistance. This creates a zero in the voltage feedback amplifier response to offset the loss of phase margin due to a parasitic pole. In current feedback amplifiers, this technique will cause the amplifier to become unstable because the closed-loop bandwidth will increase beyond the stable operating frequency.

INVERTING AMPLIFIER

The OP-160 is also capable of operation as an inverting amplifier (see Figure 21). The transfer function of this circuit is identical to that using a voltage feedback op amp:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_2}{R_1}$$

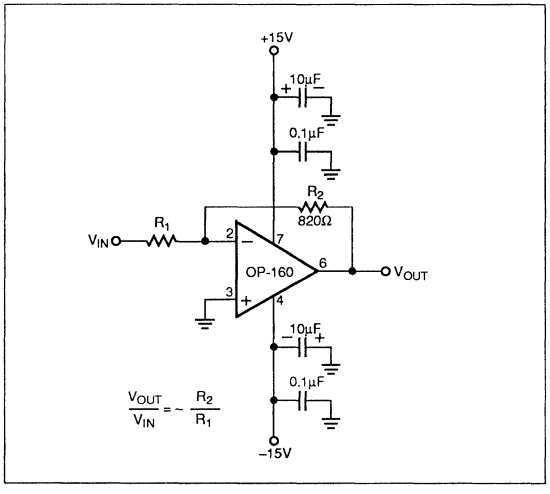


FIGURE 21: *The OP-160 as an inverting amplifier.*

USING CURRENT FEEDBACK OP AMPS IN INTEGRATOR APPLICATIONS

The small-signal model of a current feedback op amp shown earlier in Figure 3 assumes a non-varying value of feedback impedance. A non-varying feedback impedance ensures that the bandwidth of the amplifier does not extend beyond its 180° phase shift point and create unwanted oscillations. In integrator circuits, the feedback element is a capacitor whose impedance does vary with frequency. By definition then, integrator applications using current feedback amplifiers should be unstable. However, a simple trick, shown in Figure 22, enables high-speed, wide bandwidth current feedback op amps to be used in integrator applications.

Resistor R_F is placed between an artificial sum node and the inverting input of the amplifier. This resistor maintains a minimum value of feedback impedance over all frequencies. At high signal frequencies, the integrator capacitor, C_1, is a short circuit; the feedback impedance is equal to R_F only and the amplifier has maximum bandwidth. At low frequencies, C_1 adds to the overall feedback impedance. This lowers the amplifier's bandwidth but not enough to affect the integrator's performance.

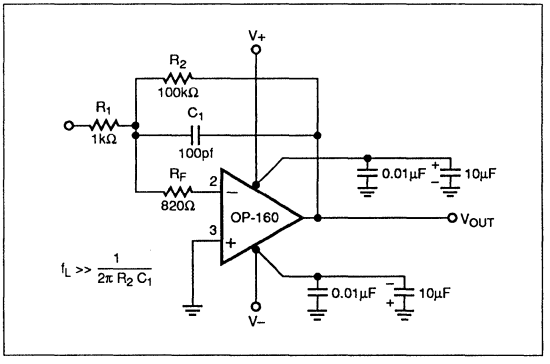


FIGURE 22: *An Integrator Using a Current Feedback Op Amp*

Figure 23 shows the gain and phase performance of the integrator. The integrator has the desired one-pole response for signal frequencies

$f_C >> 1/(2\pi R_2 C_1) \approx 16kHz.$

A more strenuous test of integrator performance is the pulse response. Ideally, this should be a linear ramp. The current feedback integrator's pulse response is exhibited in Figure 24. The response closely approximates the ideal linear ramp.

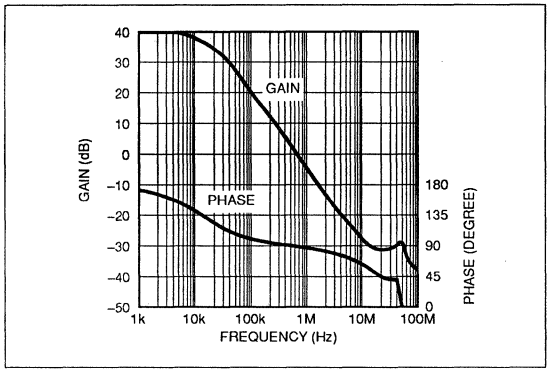


FIGURE 23: *Gain and phase response of the integrator shows a one-pole response.*

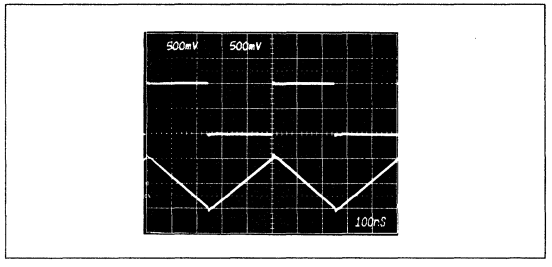


FIGURE 24: *Pulse response of the current feedback integrator. f = 2MHz.*

ACHIEVING FLAT GAIN RESPONSE WITH CURRENT FEEDBACK OP AMPS

In high-performance systems, flat gain response is often required. Current feedback op amps provide wide bandwidth performance but even these may not fulfill the gain flatness requirements of some systems.

Current feedback op amps exhibit both gain roll-off and peaking as shown in Figure 25. Peaking is primarily due to parasitic

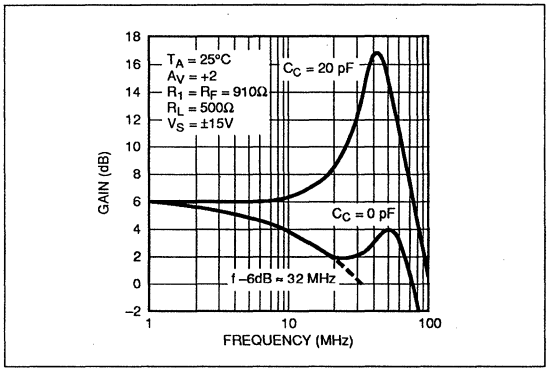


FIGURE 25: *Gain roll-off and peaking of current feedback amplifiers is dependent upon a number of factors including loading and parasitic capacitance.*

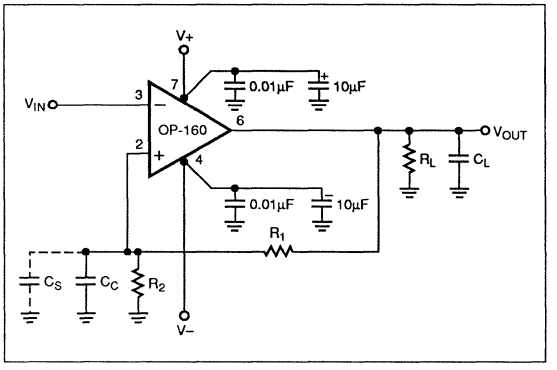


FIGURE 26: *A current feedback op amp configured for noninverting gain. Parasitic capacitances affecting gain are also shown.*

capacitance; gain roll-off is determined by the amount and type of load on the amplifier. Peaking is controlled by careful layout and circuit design; however, its cause can provide a method of improving gain flatness over a desired frequency range.

Consider the noninverting amplifier of Figure 26. The gain equals:

$$1 + \frac{R_2}{R_1 // Z_{(C_C // C_S)}},$$

and at low frequencies

$$A_V = 1 + \frac{R_2}{R_1} = 1 + \frac{910\Omega}{910\Omega} = 2$$

At higher frequencies the gain increases or peaks due to the effect of the parasitic capacitance, C_S, on the gain equation. Any capacitance at the inverting input will create a zero in the amplifier's response. This fact can be used to compensate for gain roll-off due to loading on the amplifier.

Begin by measuring or estimating the amplifier's –6dB point (this is the frequency at which the output signal is half its original amplitude). This can be easily determined from a network analyzer plot of the amplifier's frequency performance. From this the amount of capacitance, C_C, which will double the gain at the –6dB frequency and restore the original gain, can be determined.

From the –6dB frequency, C_C can be calculated:

$$C_C = C_S + \frac{1}{2\pi R_1 f_{-6dB}} + \frac{1}{2\pi R_2 f_{-6dB}}$$

for noninverting configuration, where C_S is the combination of the amplifier's input capacitance and the stray capacitance at the input.

In the example shown,

C_S = 9pF = OP-160 input capacitance (4pF) + stray capacitance (5pF)

$$C_S = 9pF + \frac{1}{2\pi(910\Omega)32MHz} + \frac{1}{2\pi(910\Omega)32MHz}$$

$\approx$ 20pF

Figure 27 is an expanded scale plot of the gain performance of the compensated amplifier at A_V = +2. Gain performance is flat to ±0.1dB out to beyond 9MHz. For low gains ($A_V \leq 5$) peaking will be increased. At higher gains, gain flatness can be significantly improved without gain peaking. Figure 28 depicts the OP-160 with A_V = +10. In this example $f_{-6dB} \approx 22$ MHz so,

$$C_S = 9pF + \frac{1}{2\pi(91\Omega)22MHz} + \frac{1}{2\pi(820\Omega)22MHz}$$

= 97pF

The nearest standard capacitor value is 100pF.

Gain performance is flat to 0.5dB to 30MHz and the amplifier's –3dB point is 38MHz. This gives the amplifier an effective gain-bandwidth of 380MHz! Compensating the OP-160 does not effect the pulse response as shown in Figure 29.

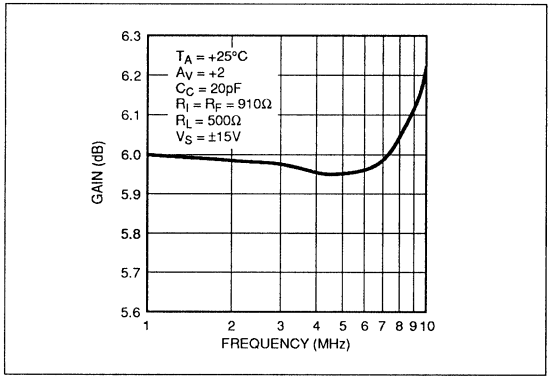


FIGURE 27: *Expanded Gain/Frequency Graph of the Compensated Amplifier, A_V = +2*

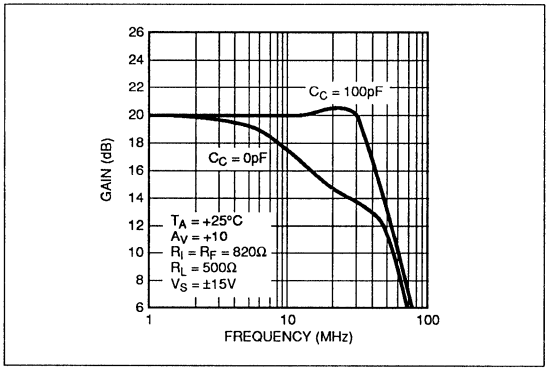


FIGURE 28: *Gain/frequency graph for the compensated amplifier, A_V = +10, showing the effect of the compensation capacitance, C_C, on gain flatness.*

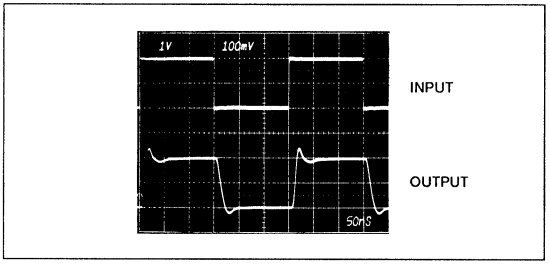


FIGURE 29: *Pulse Response of the OP-160 in a Gain of +10 Compensated for Gain Flatness*

OP-160 SPICE MACRO-MODEL

Figures 30 and 31 show the SPICE macro-model for the OP-160 high-speed, current feedback operational amplifier. This model was tested with, and is compatible with PSpice* and HSpice**. The schematic and net-list are included here so that the model can easily be used. This model uses a unique current feedback topology to accurately model both the AC and DC characteristics of the OP-160. In addition, this model can accommodate any number of poles and zeros to further shape the AC response.

The OP-160 SPICE macro-model uses four BJT transistors to create the input buffer as in the actual device. However, the rest of the model contains only ideal linear elements and ideal diodes to model the OP-160's behavior. Using only four transistors reduces simulation time and simplifies model development. It simulates important DC parameters such as V_{OS}, I_B, CMR, V_O and I_{SY}. AC parameters such as slew rate, open-loop transimpedance and phase response and CMR changes with frequency are also simulated by the model. In addition, the model includes the change in input bias current with varying common-mode and power supply voltages. Both output swing and supply current are accurately modelled.

One aspect of the OP-160's behavior is that slew rate varies with closed-loop gain. Slew rate of the basic model is set to the typical values for the OP-160 in a gain of +1. For other gains, the rising and falling slew rates can be adjusted by varying the values of V_1 and V_2 in the model. Slew rates for various gains can be determined from Figures 6a and 6b.

$$\text{Rising Slew Rate} = \frac{V_1 + 0.6V}{(1k\Omega)(5pF)}$$

$$\text{Falling Slew Rate} = \frac{V_2 + 0.6V}{(1k\Omega)(5pF)}$$

To keep the OP-160 model as simple as possible and thus save computer and development time, not all features of the op amp were modelled as listed below:

- PSR
- Crosstalk
- No limits on power supply voltages
- Maximum input voltage range
- Temperature effects (i.e., model parameters are assumed at 25°C)
- Input noise voltage and current sources
- Parameter variations for Monte Carlo analysis (i.e., all parameters are typical only)

These parameters are considered second-order effects and are not considered necessary for circuit simulation under normal operating conditions. However, users can easily add these functions as needed.

* PSpice is a registered trademark of MicroSim Corporation.
** HSPICE is a tradename of Meta-Software, Inc.

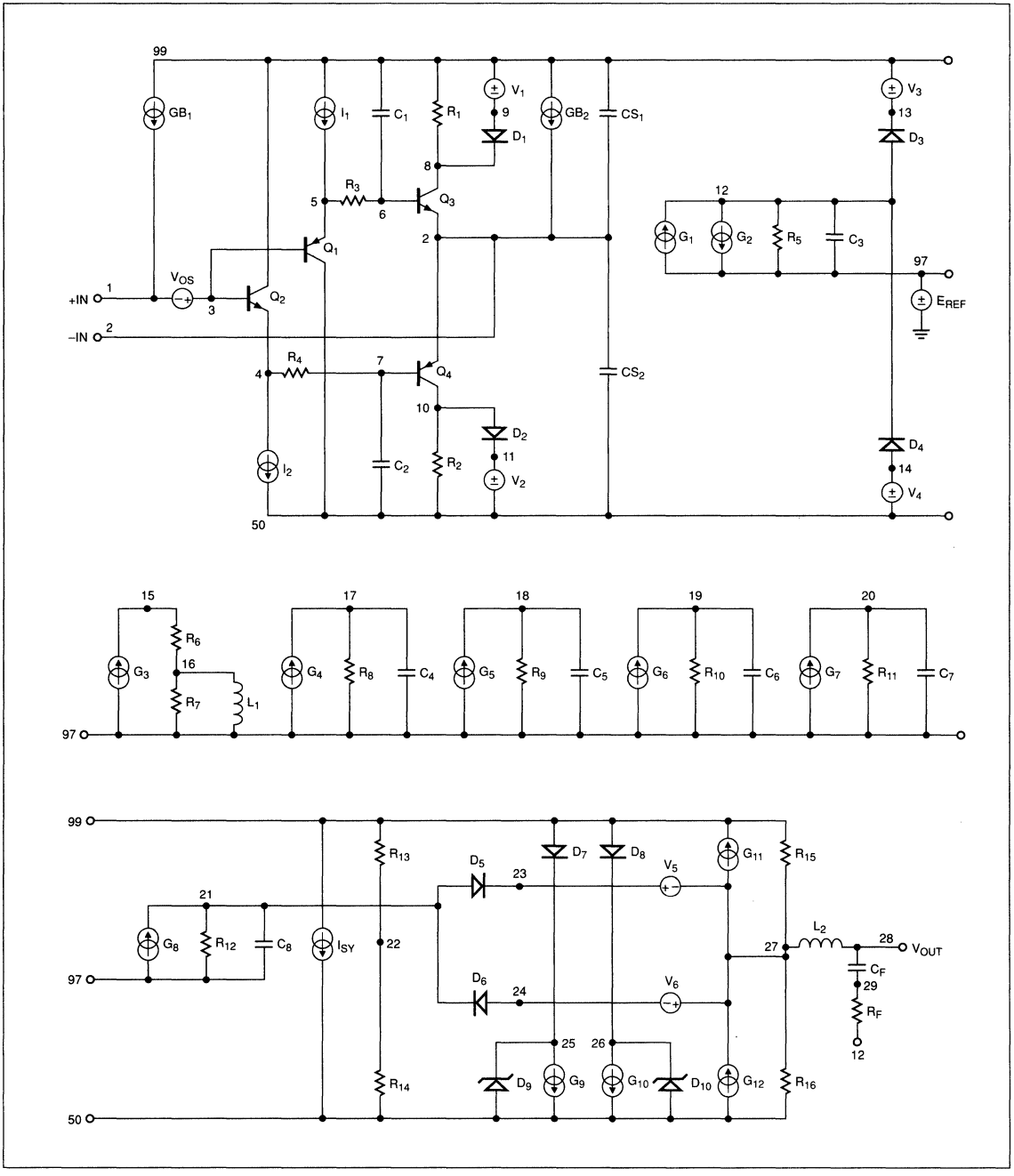


FIGURE 30: *OP-160 SPICE Model*

```
* OP-160 MACRO-MODEL © PMI 1990
*
* NODE ASSIGNMENTS
*                    NONINVERTING INPUT
*                    | INVERTING INPUT
*                    | | OUTPUT
*                    | | | POSITIVE SUPPLY
*                    | | | | NEGATIVE SUPPLY
*                    | | | | |
* SUBCKT OP-160  1  2  24  99  50
*
* INPUT STAGE
*
R1    99  8       1K
R2    10  50      1K
V1    99  9       9.4
D1    9   8       DX
V2    11  50      4.4
D2    10  11      DX
I1    99  5       125U
I2    4   50      125U
Q1    50  3   5   QP
Q2    99  3   4   QN
Q3    8   6   2   QN
Q4    10  7   2   QP
R3    5   6       143K
R4    4   7       143K
C1    99  6       0.0133P
C2    50  7       0.0133P
*
* INPUT ERROR SOURCES
*
GB1   99  1       POLY(1) 1  22  2E-7  4E-8
GB2   99  2       POLY(1) 1  22  6E-6  4E-8
VOS   3   1       1E-3
CS1   99  2       2.5E-12
CS2   50  2       2.5E-12
*
EREF  97  0       22  0  1
*
* GAIN STAGE & DOMINANT POLE
*
R5    12  97      5E6
C3    12  97      5P
G1    97  12      99  8  1E-3
G2    12  97      10 50  1E-3
V3    99  13      2.2
V4    14  50      2.2
D3    12  13      DX
D4    14  12      DX
CF    29  28      30P
RF    12  29      300
*
* ZERO/POLE PAIR AT 50MHZ/300MHZ
*
R6    15  16      1E6
L1    16  97      2.65E-3
R7    16  97      5E6
G3    97  15      12  22  1E-6
*
* POLE AT 300MHZ
*
R8    17  97      1E6
C4    17  97      0.531E-15
G4    97  17      15  22  1E-6
*
* POLE AT 300MHZ
*
R9    18  97      1E6
C5    18  97      0.531E-15
G5    97  18      17  22  1E-6
*
* POLE AT 500MHZ
*
R10   19  97      1E6
C6    19  97      0.318E-15
G6    97  19      18  22  1E-6
*
* POLE AT 500MHZ
*
R11   20  97      1E6
C7    20  97      0.318E-15
G7    97  20      19  22  1E-6
*
* POLE AT 500MHZ
*
R12   21  97      1E6
C8    21  97      0.318E-15
G8    97  21      20  22  1E-6
*
* OUTPUT STAGE
*
ISY   99  50      1.75E-3
R13   22  99      3.333E3
R14   22  50      3.333E3
R15   27  99      40
R16   27  50      40
L2    27  28      4E-8
G9    25  50      21  27  25E-3
G10   26  50      27  21  25E-3
G11   27  99      99  21  25E-3
G12   50  27      21  50  25E-3
V5    23  27      1.55
V6    27  24      1.55
D5    21  23      DX
D6    24  21      DX
D7    99  25      DX
D8    99  26      DX
D9    50  25      DY
D10   50  26      DY
*
* MODELS USED
*
.MODEL QN  NPN (BF=1E9 IS=1E-15 VAF=92)
.MODEL QP  PNP (BF=1E9 IS=1E-15 VAF=92)
.MODEL DX  D(IS=1E-15)
.MODEL DY  D(IS=1E-15 BV=50)
.ENDS OP-160
```

FIGURE 31: *OP-160 SPICE Net-List*

Dual, Precision JFET High Speed Operational Amplifier

OP-249

FEATURES

- **Fast Slew Rate ..... 22V/μs Typ**
- **Settling Time (0.01%) ..... 1.2μs Max**
- **Offset Voltage ..... 300μV Max**
- **High Open-Loop Gain ..... 1000V/mV Min**
- **Low Total Harmonic Distortion ..... 0.002% Typ**
- **Improved Replacement for AD712, LT1057, OP-215, TL072, and MC34082**
- **Available in Die Form**

APPLICATIONS

- **Output Amplifier for Fast D/As**
- **Signal Processing**
- **Instrumentation Amplifiers**
- **Fast Sample/Holds**
- **Active Filters**
- **Low Distortion Audio Amplifiers**
- **Input Buffer for A/D Converters**
- **Servo Controllers**

GENERAL DESCRIPTION

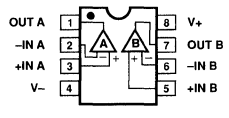
The OP-249 is a high-speed, precision dual JFET op amp, similar to the popular single op amp, the OP-42. The OP-249 outperforms available dual amplifiers by providing superior speed with excellent DC performance. Ultra-high open-loop gain (1kV/mV minimum), low offset voltage, and superb gain linearity, makes the OP-249 the industry's first true precision, dual high-speed amplifier.

With a slew rate of 22V/μs typical, and a fast settling time of less than 1.2μs maximum to 0.01%, the OP-249 is an ideal choice for high-speed bipolar D/A and A/D converter applications. The excellent DC performance of the OP-249 allows the full accuracy of high-resolution CMOS D/As to be realized.

Symmetrical slew rate, even when driving large loads, such as 600Ω, or 200pF of capacitance, and ultra-low distortion, make the OP-249 ideal for professional audio applications, active filters, high-speed integrators, servo systems, and buffer amplifiers.

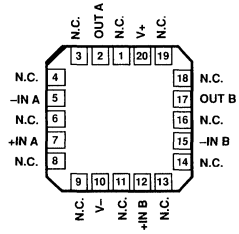
The OP-249 provides significant performance upgrades to the TL072, AD712, OP-215, MC34082 and the LT1057.

PIN CONNECTIONS

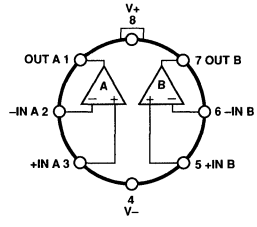


8-PIN CERDIP
(Z-Suffix)

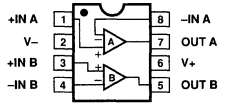
8-PIN EPOXY MINI-DIP
(P-Suffix)



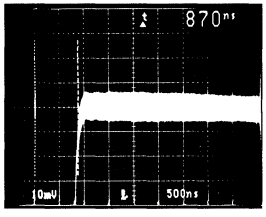
20-CONTACT LCC
(RC-Suffix)



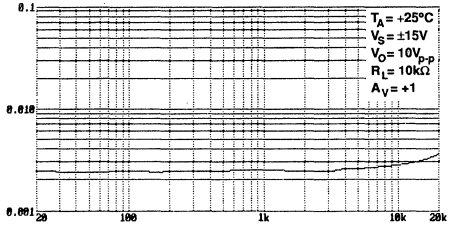
TO-99
(J-Suffix)



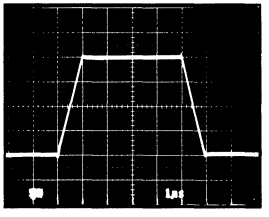
8-PIN SO
(S-Suffix)



FAST SETTLING
(0.01%)



LOW DISTORTION
A_V = +1, R_L = 10kΩ



EXCELLENT OUTPUT DRIVE
R_L = 600Ω

ORDERING INFORMATION †

PACKAGE				OPERATING TEMPERATURE RANGE
TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	
OP249AJ*	OP249AZ*	–	OP249ARC/883	MIL
OP249EJ	–	–	–	XIND
OP249FJ	OP249FZ	–	–	XIND
–	–	OP249GP	–	XIND
–	–	OP249GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see PMI's Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Input Voltage (Note 2) ..... ±18V
Differential Input Voltage (Note 2) 36V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to +175°C

Operating Temperature Range
OP-249A (J, Z, RC) ..... –55°C to +125°C
OP-249E,F (J, Z) ..... –40°C to +85°C
OP-249G (P, S) ..... –40°C to +85°C
Junction Temperature
OP-249 (J, Z, RC) ..... –65°C to +175°C
OP-249 (P, S) ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
TO-99 (J)	145	16	°C/W
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
8-Pin SO (S)	150	41	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

			OP-249A			OP-249E			OP-249F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Offset Voltage	V_{OS}		–	0.2	0.5	–	0.1	0.3	–	0.2	0.7	mV
Long Term Offset Voltage	V_{OS}	(Note 1)	–	–	0.8	–	–	0.6	–	–	1.0	mV
Offset Stability			–	1.5	–	–	1.5	–	–	1.5	–	µV/Month
Input Bias Current	I_B	V_{CM} = 0V, T_j = +25°C	–	30	75	–	20	50	–	30	75	pA
Input Offset Current	I_{OS}	V_{CM} = 0V, T_j = +25°C	–	6	25	–	4	15	–	6	25	pA
Input Voltage Range	IVR	(Note 2)	±11	+12.5 –12.5	–	±11	+12.5 –12.5	–	±11	+12.5 –12.5	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	80	90	–	86	95	–	80	90	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	–	12	31.6	–	9	31.6	–	12	50	µV/V
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 2kΩ	1000	1400	–	1000	1400	–	500	1200	–	V/mV
Output Voltage Swing	V_O	R_L = 2kΩ	±12.0	+12.5 –12.5	–	±12.0	+12.5 –12.5	–	±12.0	+12.5 –12.5	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±20	+36 –33	±50	±20	+36 –33	±50	±20	+36 –33	±50	mA
Supply Current	I_{SY}	No Load V_O = 0V	–	5.6	7.0	–	5.6	7.0	–	5.6	7.0	mA
Slew Rate	SR	R_L = 2kΩ, C_L = 50pF	18	22	–	18	22	–	18	22	–	V/µs
Gain-Bandwidth Product	GBW	(Note 4)	3.5	4.7	–	3.5	4.7	–	3.5	4.7	–	MHz
Settling Time	t_s	10V Step 0.01% (Note 3)	–	0.9	1.2	–	0.9	1.2	–	0.9	1.2	µs
Phase Margin	Θ_0	0dB Gain	–	55	–	–	55	–	–	55	–	Deg

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-249A MIN	OP-249A TYP	OP-249A MAX	OP-249E MIN	OP-249E TYP	OP-249E MAX	OP-249F MIN	OP-249F TYP	OP-249F MAX	UNITS
Differential Input Impedance	Z_{IN}		–	10^{12}||6	–	–	10^{12}||6	–	–	10^{12}||6	–	Ω||pF
Open-Loop Output Resistance	R_O		–	35	–	–	35	–	–	35	–	Ω
Voltage Noise	$e_{n\ p\text{-}p}$	0.1Hz to 10Hz	–	2	–	–	2	–	–	2	–	$\mu V_{p\text{-}p}$
Voltage Noise Density	e_n	f_O = 10Hz	–	75	–	–	75	–	–	75	–	nV/√Hz
		f_O = 100Hz	–	26	–	–	26	–	–	26	–	
		f_O = 1kHz	–	17	–	–	17	–	–	17	–	
		f_O = 10kHz	–	16	–	–	16	–	–	16	–	
Current Noise Density	i_n	f_O = 1kHz	–	0.003	–	–	0.003	–	–	0.003	–	pA/√Hz
Voltage Supply Range	V_S		±4.5	±15	±18	±4.5	±15	±18	±4.5	±15	±18	V

NOTES:
1 Long term offset voltage is guaranteed by a 1000 HR life test performed on 3 independent wafer lots at +125°C with a LTPD of 3.
2. Guaranteed by CMR test.
3. Settling-time is statistically tested.
4. Guaranteed by design and by inference from the slew rate measurement.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-249G MIN	OP-249G TYP	OP-249G MAX	UNITS
Offset Voltage	V_{OS}		–	0.4	2.0	mV
Input Bias Current	I_B	V_{CM} = 0V, T_j = +25°C	–	40	75	pA
Input Offset Current	I_{OS}	V_{CM} = 0V, T_j = +25°C	–	10	25	pA
Input Voltage Range	IVR	(Note 1)	±11	+12.5 –12.0	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	76	90	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	–	12	50	µV/V
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 2kΩ	500	1100	–	V/mV
Output Voltage Swing	V_O	R_L = 2kΩ	±12.0	+12.5 –12.5	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±20	+36 –33	±50	mA
Supply Current	I_{SY}	No Load V_O = 0V	–	5.6	7.0	mA
Slew Rate	SR	R_L = 2kΩ, C_L = 50pF	18	22	–	V/µs
Gain-Bandwidth Product	GBW		–	4.7	–	MHz
Settling Time	t_s	10V Step 0.01%	–	0.9	–	µs
Phase Margin	Θ_0	0dB Gain	–	55	–	Deg

NOTES:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-249G MIN	OP-249G TYP	OP-249G MAX	UNITS
Differential Input Impedance	Z_{IN}		–	10^{12}‖6	–	Ω‖pF
Open-Loop Output Resistance	R_O		–	35	–	Ω
Voltage Noise	$e_{n\ p\text{-}p}$	0.1Hz to 10Hz	–	2	–	$\mu V_{p\text{-}p}$
Voltage Noise Density	e_n	f_O = 10Hz	–	75	–	nV/√Hz
		f_O = 100Hz	–	26	–	
		f_O = 1kHz	–	17	–	
		f_O = 10kHz	–	16	–	
Current Noise Density	i_n	f_O = 1kHz	–	0.003	–	pA/√Hz
Voltage Supply Range	V_S		±4.5	±15	±18	V

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –40°C ≤ T_A ≤ +85°C for E/F grades, and –55°C ≤ T_A ≤ +125°C for A grade, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-249A MIN	OP-249A TYP	OP-249A MAX	OP-249E MIN	OP-249E TYP	OP-249E MAX	OP-249F MIN	OP-249F TYP	OP-249F MAX	UNITS
Offset Voltage	V_{OS}		–	0.12	1.0	–	0.1	0.5	–	0.5	1.1	mV
Offset Voltage Temperature Coefficient	TCV_{OS}		–	1	5	–	1	3	–	1.2	6	µV/°C
Input Bias Current	I_B	(Note 1)	–	4	20	–	0.25	3.0	–	0.3	4.0	nA
Input Offset Current	I_{OS}	(Note 1)	–	0.04	4	–	0.01	0.7	–	0.02	1.2	nA
Input Voltage Range	IVR	(Note 2)	±11	+12.5 –12.5	–	±11	+12.5 –12.5	–	±11	+12.5 –12.5	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	76	110	–	86	100	–	76	95	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	–	5	50	–	5	50	–	7	100	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 2kΩ V_O = ±10V	500	1400	–	750	1400	–	250	1200	–	V/mV
Output Voltage Swing	V_O	R_L = 2kΩ	±12.0	+12.5 –12.5	–	±12.0	+12.5 –12.5	–	±12.0	+12.5 –12.5	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±10	–	±60	±18	–	±60	±18	–	±60	mA
Supply Current	I_{SY}	No Load V_O = 0V	–	5.6	7.0	–	5.6	7.0	–	5.6	7.0	mA

NOTES:

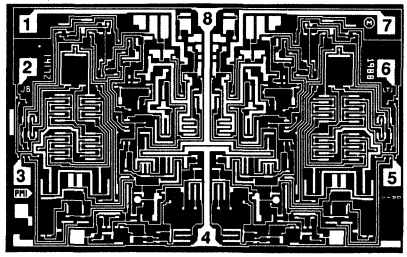
1. T_J = 85°C for E/F Grades; T_J = 125°C for A Grade.
2. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-40°C \leq T_A \leq +85°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-249G MIN	OP-249G TYP	OP-249G MAX	UNITS
Offset Voltage	V_{OS}		–	1.0	3.6	mV
Offset Voltage Temperature Coefficient	TCV_{OS}		–	6	25	µV/°C
Input Bias Current	I_B	(Note 1)	–	0.5	4.5	nA
Input Offset Current	I_{OS}	(Note 1)	–	0.04	1.5	nA
Input Voltage Range	IVR	(Note 2)	±11.0	+12.5 −12.5	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	76	95	–	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	–	10.0	100	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	250	1200	–	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	±12.0	+12.5 −12.5	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±18	–	±60	mA
Supply Current	I_{SY}	No Load $V_O = 0V$	–	5.6	7.0	mA

NOTES:
1. $T_j = 85°C$.
2. Guaranteed by CMR test.

DICE CHARACTERISTICS



DIE SIZE 0.072 x 0.112 inch, 8,064 sq. mils
(1.83 x 2.84 mm, 5.2 sq. mm)

1. OUT (A)
2. –IN (A)
3. +IN (A)
4. V–
5. +IN (B)
6. –IN (B)
7. OUT (B)
8. V+

WAFER TEST LIMITS at V_S = ±15V, T_j = +25°C, unless otherwise noted.

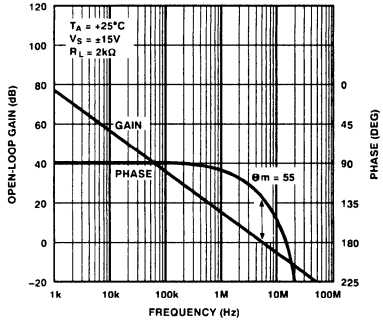
PARAMETER	SYMBOL	CONDITIONS	OP-249GBC LIMITS	UNITS
Offset Voltage	V_{OS}		0.5	mV MAX
Offset Voltage Temperature Coefficient	TCV_{OS}	–40°C ≤ T_j ≤ 85°C	6.0	µV/°C MAX
Input Bias Current	I_B	V_{CM} = 0V	225	pA MAX
Input Offset Current	I_{OS}	V_{CM} = 0V	75	pA MAX
Input Voltage Range	IVR	(Note 1)	±11	V MIN
Common-Mode Rejection	CMR	V_{CM} = ±11V	76	dB MIN
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	100	µV/V MAX
Large-Signal Voltage Gain	A_{VO}	R_L = 2kΩ	250	V/mV MIN
Output Voltage Swing	V_O	R_L = 2kΩ	±12.0	V MIN
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±20/±60	mA MIN/MAX
Supply Current	I_{SY}	No Load V_O = 0V	7.0	mA MAX
Slew Rate	SR	R_L = 2kΩ, C_L = 50pF	16.5	V/µs MIN

NOTES:
1. Guaranteed by CMR test.

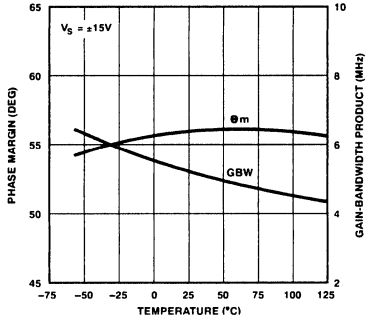
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

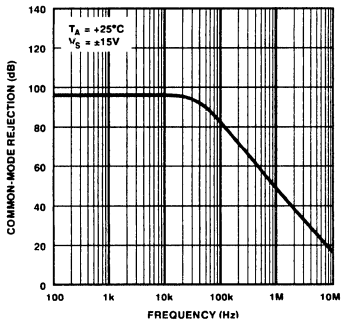
OPEN-LOOP GAIN, PHASE vs FREQUENCY



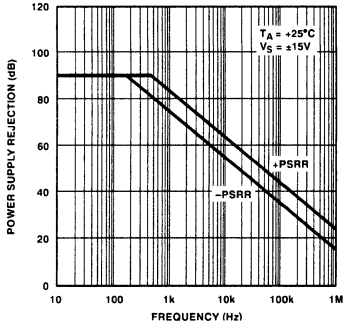
GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE



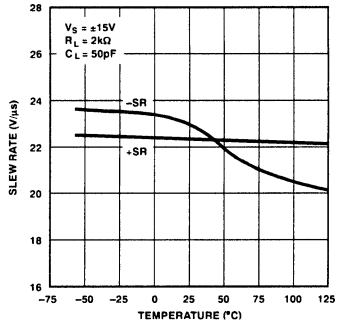
COMMON-MODE REJECTION vs FREQUENCY



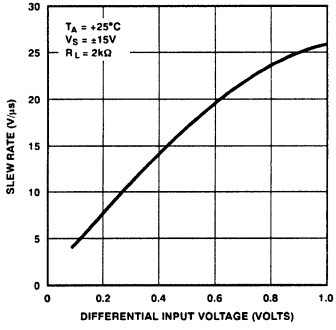
POWER SUPPLY REJECTION vs FREQUENCY



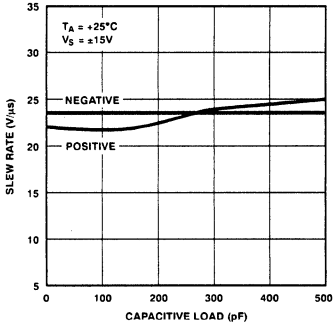
SLEW RATE vs TEMPERATURE



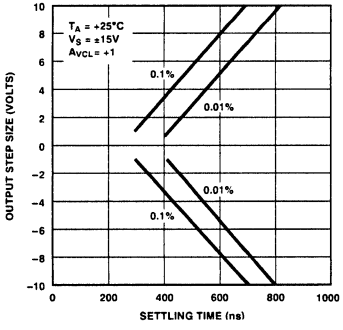
SLEW RATE vs DIFFERENTIAL INPUT VOLTAGE



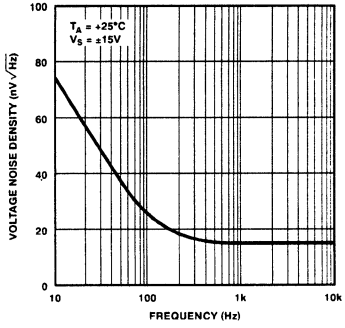
SLEW RATE vs CAPACITIVE LOAD



SETTLING TIME vs STEP SIZE

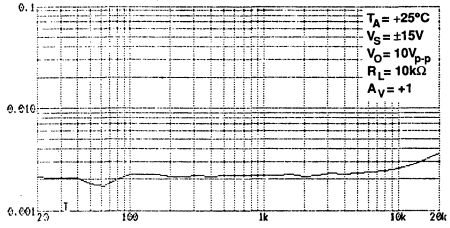


VOLTAGE NOISE DENSITY vs FREQUENCY

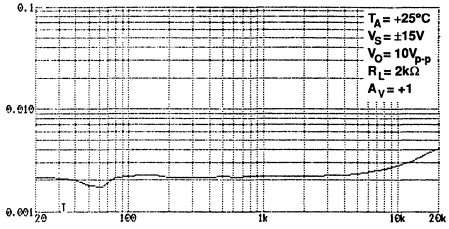


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

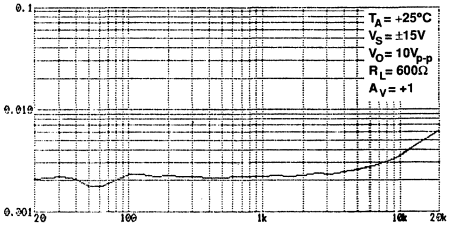
DISTORTION vs FREQUENCY



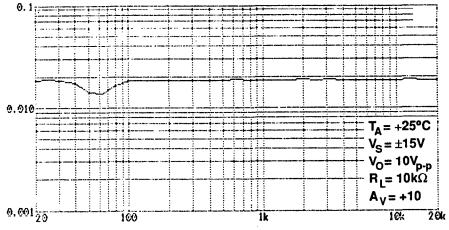
DISTORTION vs FREQUENCY



DISTORTION vs FREQUENCY



DISTORTION vs FREQUENCY



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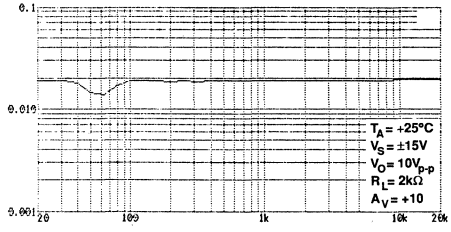

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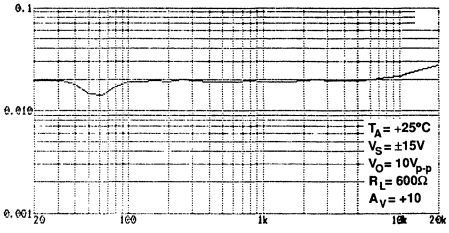
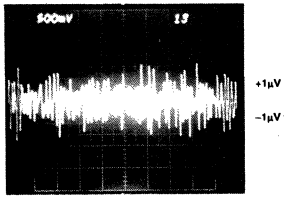


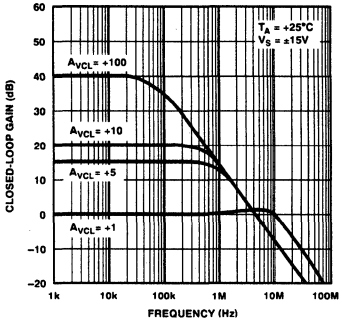
LOW FREQUENCY NOISE



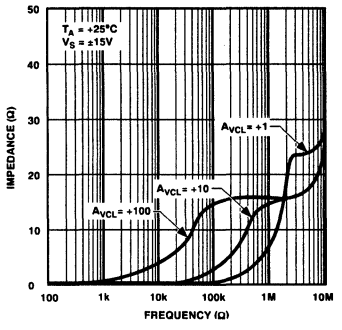
BANDWIDTH (0.1Hz TO 10Hz)

T_A = +25°C V_S = ±15V

CLOSED-LOOP GAIN vs FREQUENCY

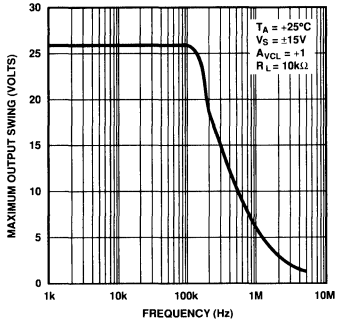


CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

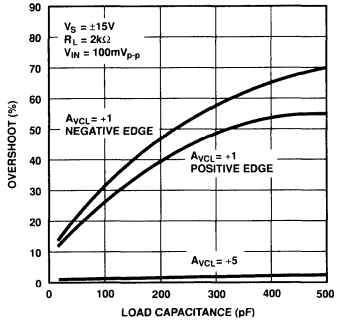


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

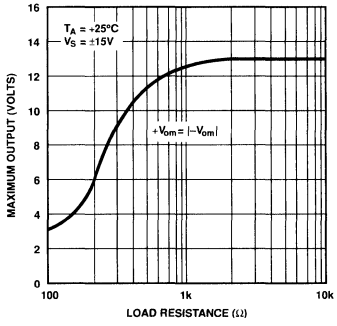
MAXIMUM OUTPUT SWING vs FREQUENCY



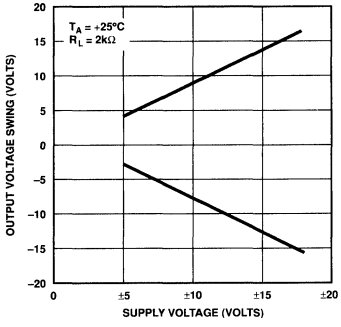
SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



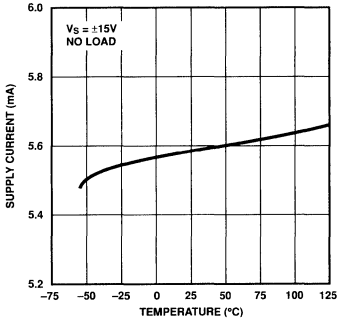
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



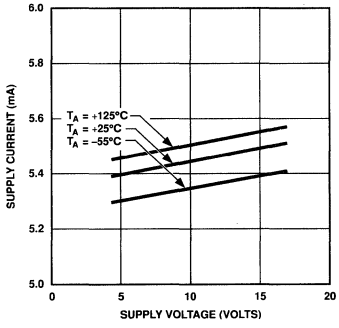
OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE



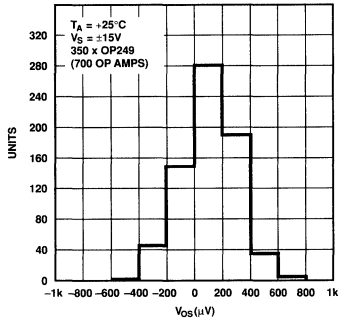
SUPPLY CURRENT vs TEMPERATURE



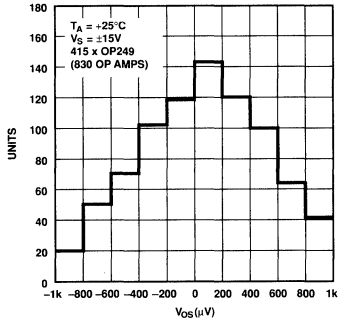
SUPPLY CURRENT vs SUPPLY VOLTAGE



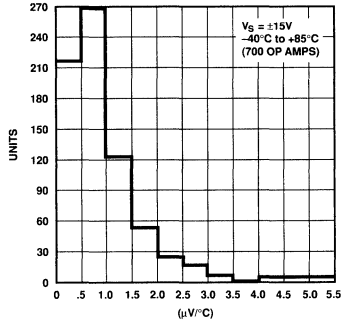
V_{OS} DISTRIBUTION (J PACKAGE)



V_{OS} DISTRIBUTION (P PACKAGE)



TCV_{OS} DISTRIBUTION (J PACKAGE)



TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

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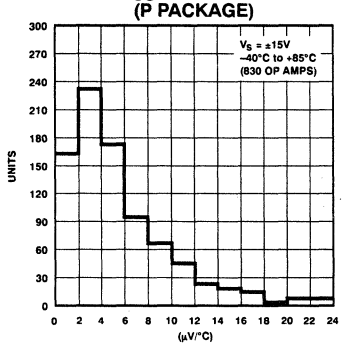
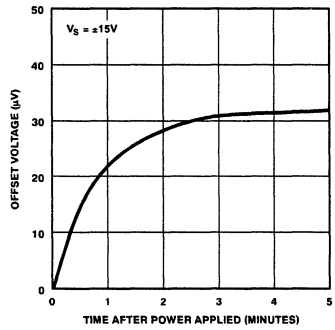
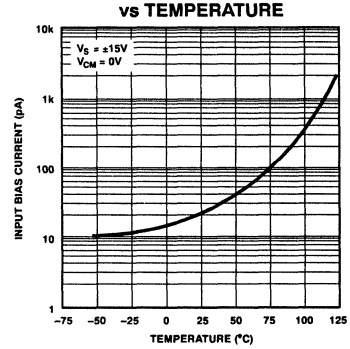


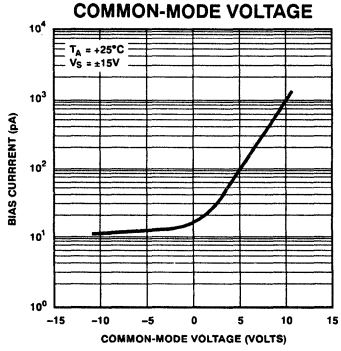
OFFSET VOLTAGE WARM-UP DRIFT



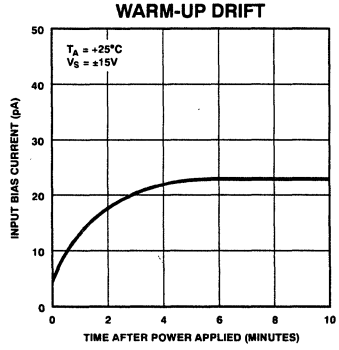
INPUT BIAS CURRENT vs TEMPERATURE



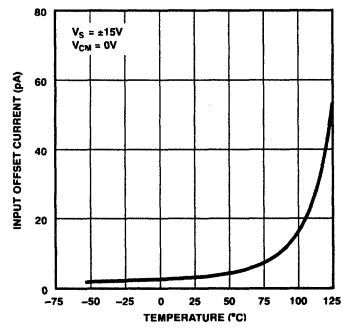
BIAS CURRENT vs COMMON-MODE VOLTAGE



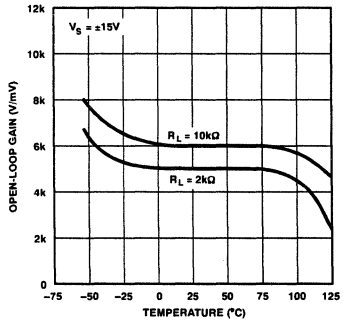
BIAS CURRENT WARM-UP DRIFT



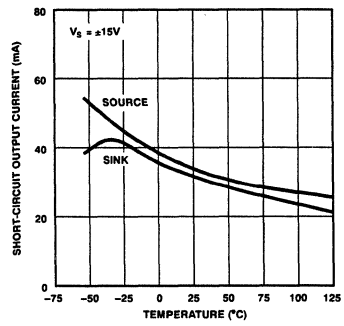
INPUT OFFSET CURRENT vs TEMPERATURE



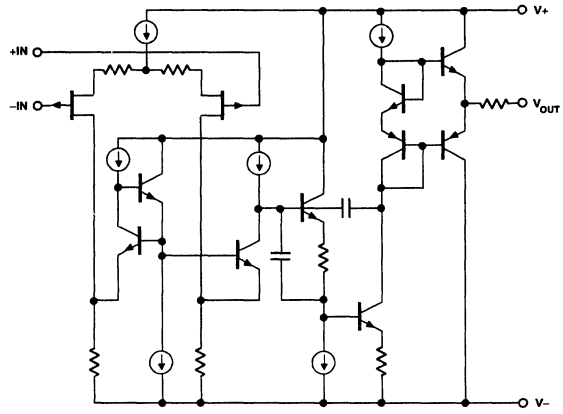
OPEN-LOOP GAIN vs TEMPERATURE



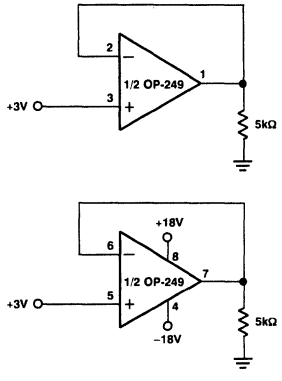
SHORT-CIRCUIT OUTPUT CURRENT vs JUNCTION TEMPERATURE



SIMPLIFIED SCHEMATIC (1/2 OP-249)



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

The OP-249 represents a reliable JFET amplifier design, featuring an excellent combination of DC precision and high speed. A rugged output stage provides the ability to drive a 600Ω load and still maintain a clean AC response. The OP-249 features a large-signal response that is more linear and symmetric than previously available JFET input amplifiers – compare the OP-249's large-signal reponse, as illustrated in Figure 1, to other industry standard dual JFET amplifiers.

Typically, JFET amplifier's slewing performance is simply specified as just a number of volts/μs. There is no discussion on the quality, i.e., linearity, symmetry, etc. of the slewing response.

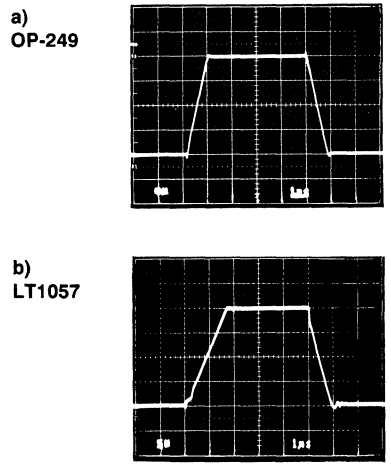


FIGURE 1: *Large-Signal Transient Response, A_V = +1, V_{IN} = 20V_{p-p}, Z_L = 2kΩ||200pF, V_S = ±15V*

The OP-249 was carefully designed to provide symmetrically matched slew characteristics in both the negative and positive directions, even when driving a large output load.

An amplifier's slewing limitation determines the maximum frequency at which a sinusoidal output can be obtained without significant distortion. It is, however, important to note that the nonsymmetric slewing typical of previously available JFET amplifiers adds a higher series of harmonic energy content to the resulting response – and an additional DC output component. Examples of potential problems of nonsymmetric slewing behaviour could be in audio amplifier applications, where a natural, low-distortion sound quality is desired, and in servo or signal processing systems where a net DC offset cannot be tolerated. The linear and symmetric slewing feature of the OP-249 makes it an ideal choice for applications that will exceed the full-power-bandwidth range of the amplifier.

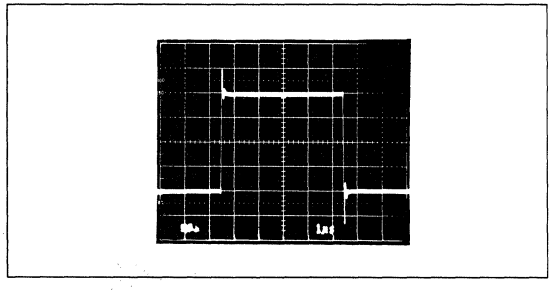


FIGURE 2: *Small-Signal Transient Response, A_V = +1, Z_L = 2kΩ\|\|100pF, No Compensation, V_S = ±15V*

As with most JFET-input amplifiers, the output of the OP-249 may undergo phase inversion if either input exceeds the specified input voltage range. Phase inversion will not damage the amplifier, nor will it cause an internal latch-up condition.

Supply decoupling should be used to overcome inductance and resistance associated with supply lines to the amplifier. A 0.1μF and a 10μF capacitor should be placed between each supply pin and ground.

OPEN-LOOP GAIN LINEARITY

The OP-249 has both an extremely high open-loop gain of 1kV/mV minimum and constant gain linearity. This feature of the OP-249 enhances its DC precision, and provides superb accuracy in high closed-loop gain applications. Figure 3 illustrates the typical open-loop gain linearity – high gain accuracy is assured, even when driving a 600Ω load.

OFFSET VOLTAGE ADJUSTMENT

The inherent low offset voltage of the OP-249 will make offset adjustments unnecessary in most applications. However, where a lower offset error is required, balancing can be performed with simple external circuitry, as illustrated in Figures 4 and 5.

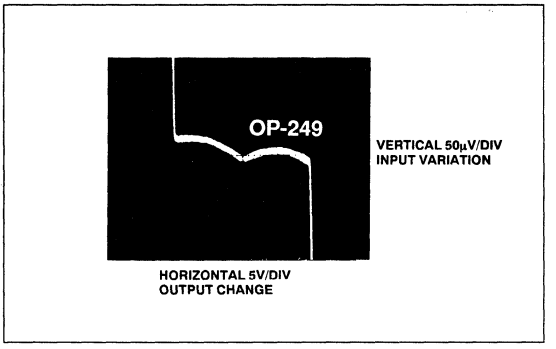


FIGURE 3: *Open-Loop Gain Linearity. Variation in Open-Loop Gain Results in Errors in High Closed-Loop Gain Circuits. R_L = 600Ω, V_S = ±15V*

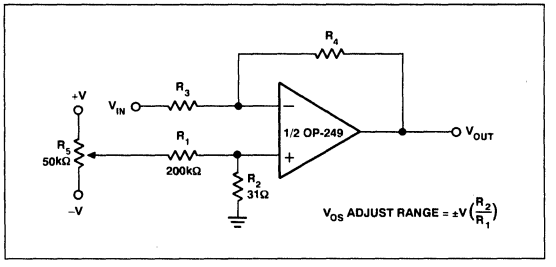


FIGURE 4: *Offset Adjust for Inverting Amplifier Configuration*

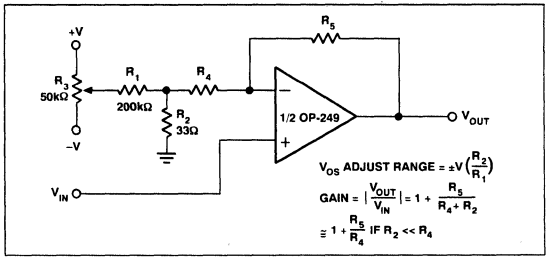


FIGURE 5: *Offset Adjust for Noninverting Amplifier Configuration*

In Figure 4, the offset adjustment is made by supplying a small voltage at the noninverting input of the amplifier. Resistors R_1 and R_2 attenuates the pot voltage, providing a ±2.5mV (with V_S = ±15V) adjustment range, referred to the input. Figure 5 illustrates offset adjust for the noninverting amplifier configuration, also providing a ±2.5mV adjustment range. As indicated in the equations in Figure 5, if R_4 is not much greater than R_2, there will be a resulting closed-loop gain error that must be accounted for.

Settling time is the time between when the input signal begins to change and when the output permanently enters a prescribed error band. The error bands on the output are 5mV and 0.5mV, respectively, for 0.1% and 0.01% accuracy.

Figure 6 illustrates the OP-249's typical settling time of 870ns. Moreover, problems in settling response, such as thermal tails and long-term ringing are nonexistent.

DAC OUTPUT AMPLIFIER

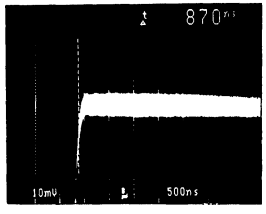


FIGURE 6: *Settling Characteristics of the OP-249 to 0.01%.*

Unity-gain stability, a low offset voltage of 300μV typical, and a fast settling time of 870ns to 0.01%, makes the OP-249 an ideal amplifier for fast digital-to-analog converters.

For CMOS DAC applications, the low offset voltage of the OP-249 results in excellent linearity performance. CMOS DACs, such as the PM-7545, will typically have a code-dependent output resistance variation between 11kΩ and 33kΩ. The change in output resistance, in conjunction with the 11kΩ feedback resistor, will result in a noise gain change. This causes variations in the offset error, increasing linearity errors. The OP-249 features low offset voltage error, minimizing this effect and maintaining 12-bit linearity performance over the full scale range of the converter.

Since the DAC's output capacitance appears at the operational amplifiers inputs, it is essential that the amplifier is adequately compensated. Compensation will increase the phase margin, and ensure an optimal overall settling response. The required lead compensation is achieved with capacitor C in Figure 7.

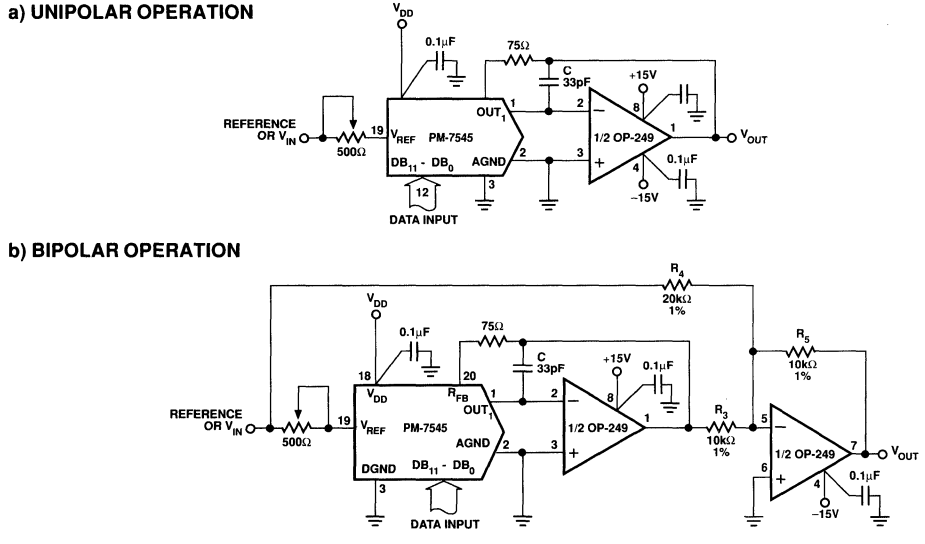


FIGURE 7: *Fast Settling and Low Offset Error of the OP-249 Enhances CMOS DAC Performance*

Figure 8 illustrates the effect of altering the compensation on the output response of the circuit in Figure 6a. Compensation is required to address the combined effect of the DAC's output capacitance, the op amp's input capacitance, and any stray capacitance. Slight adjustments to the compensation capacitor may be required to optimize settling response for any given application.

The settling time of the combination of the current output DAC and the op amp can be approximated by:

$$t_{S\ TOTAL} = \sqrt{(t_{S\ DAC})^2 + (t_{S\ AMP})^2}$$

The actual overall settling time is affected by the noise gain of the amplifier, the applied compensation, and the equivalent input capacitance at the amplifier's input.

DISCUSSION ON DRIVING A/D CONVERTERS

Settling characteristics of operational amplifiers also include an amplifier's ability to recover, i.e., settle, from a transient current output load condition. An example of this includes an op amp driving the input from a SAR type A/D converter. Although the comparison point of the converter is usually diode clamped, the input swing of plus-and-minus a diode drop still gives rise to a significant modulation of input current. If the closed-loop output impedance is low enough and bandwidth of the amplifier is sufficiently large, the output will settle before the converter makes a comparison decision which will prevent linearity errors or missing codes.

Figure 9 shows a settling measurement circuit for evaluating recovery from an output current transient. An output disturbing

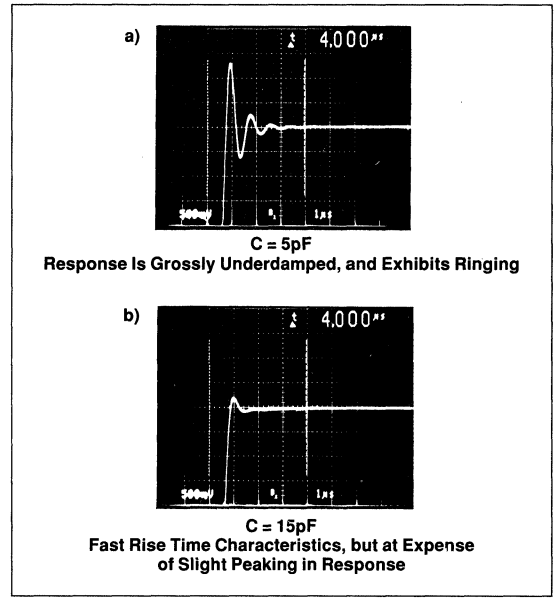


FIGURE 8: *Effect of Altering Compensation from Circuit in Figure 7a – PM-7545 CMOS DAC with 1/2 OP-249, Unipolar Operation. Critically Damped Response Will Be Obtained with C ≈ 33pF*

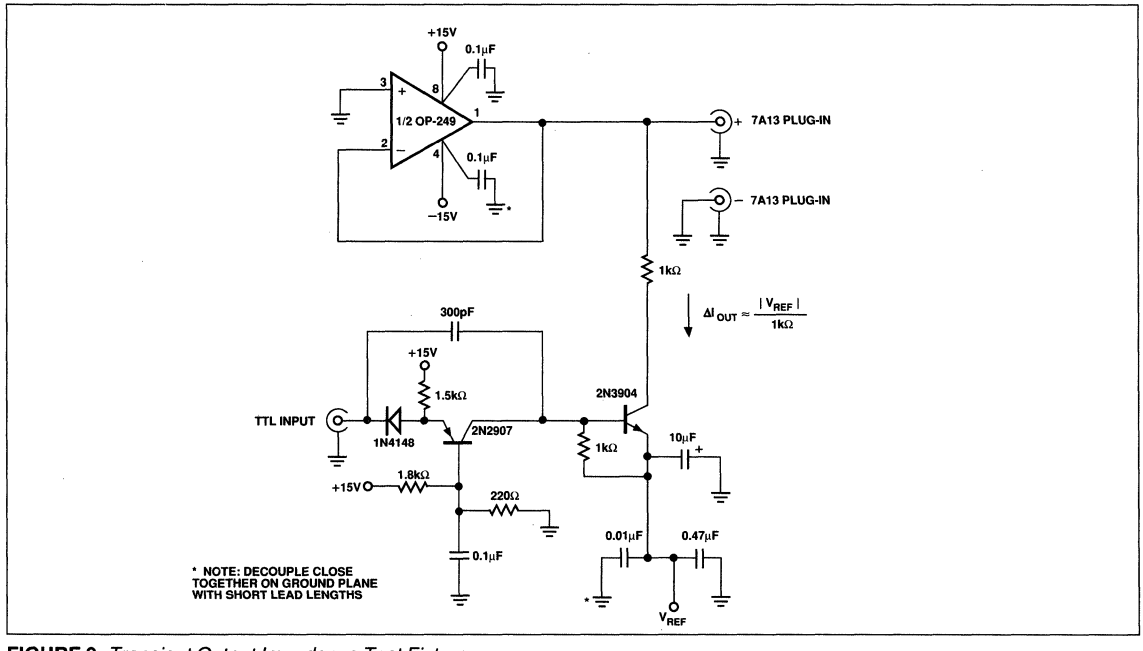


FIGURE 9: *Transient Output Impedance Test Fixture*

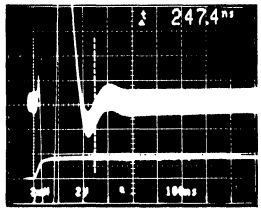


FIGURE 10: *OP-249's Transient Recovery Time from a 1mA Load Transient to 0.01%*

current generator provides the transient change in output load current of 1mA. As seen in Figure10, the OP-249 has extremely fast recovery of 274ns (to 0.01%), for a 1mA load transient. The performance makes it an ideal amplifier for data acquisition systems.

The combination of high speed and excellent DC performance of the OP-249 makes it an ideal amplifier for 12-bit data acquisition systems. Examining the circuit in Figure 11, one amplifier in the OP-249 provides a stable –5V reference voltage for the V_{REF} input of the ADC-912. The other amplifier in the OP-249 performs high-speed buffering of the A/D's input.

Examining the worst case transient voltage error (Figure 12) at the Analog In node of the A/D converter: the OP-249 recovers in less than 100ns. The fast recovery is due to both the OP-249's wide bandwidth and low DC output impedance.

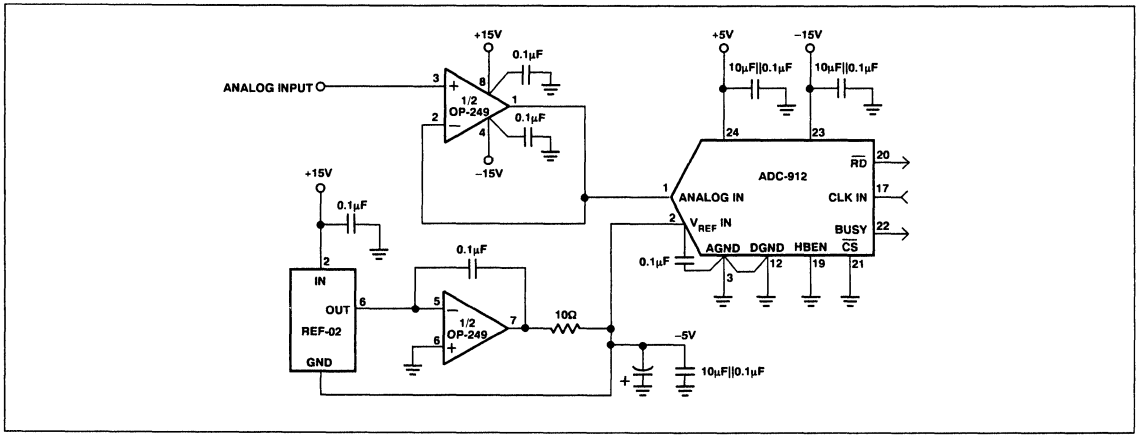


FIGURE 11: *OP-249 Dual Amplifiers Provide Both Stable –5V Reference Input, and Buffers Input to ADC-912*

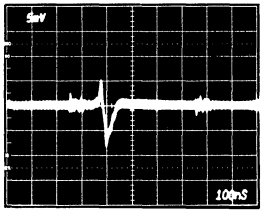


FIGURE 12: *Worst Case Transient Voltage, at Analog In, Occurs at the Half-Scale Point of the A/D. OP-249 Buffers the A/D Input from Figure 11, and Recovers in Less than 100ns*

OP-249 SPICE MACRO-MODEL

Figures 13 and 14 show the node and net list for a SPICE macro-model of the OP-249. The model is a simplified version of the actual device and simulates important DC parameters such as V_{OS}, I_{OS}, I_B, A_{VO}, CMR, V_O and I_{SY}. AC parameters such as slew rate, gain and phase reponse and CMR change with frequency are also simulated by the model.

The model uses typical parameters for the OP-249. The poles and zeros in the model were determined from the actual open and closed-loop gain and phase reponse of the OP-249. In this way the model presents an accurate AC representation of the actual device. The model assumes an ambient temperature of 25°C.

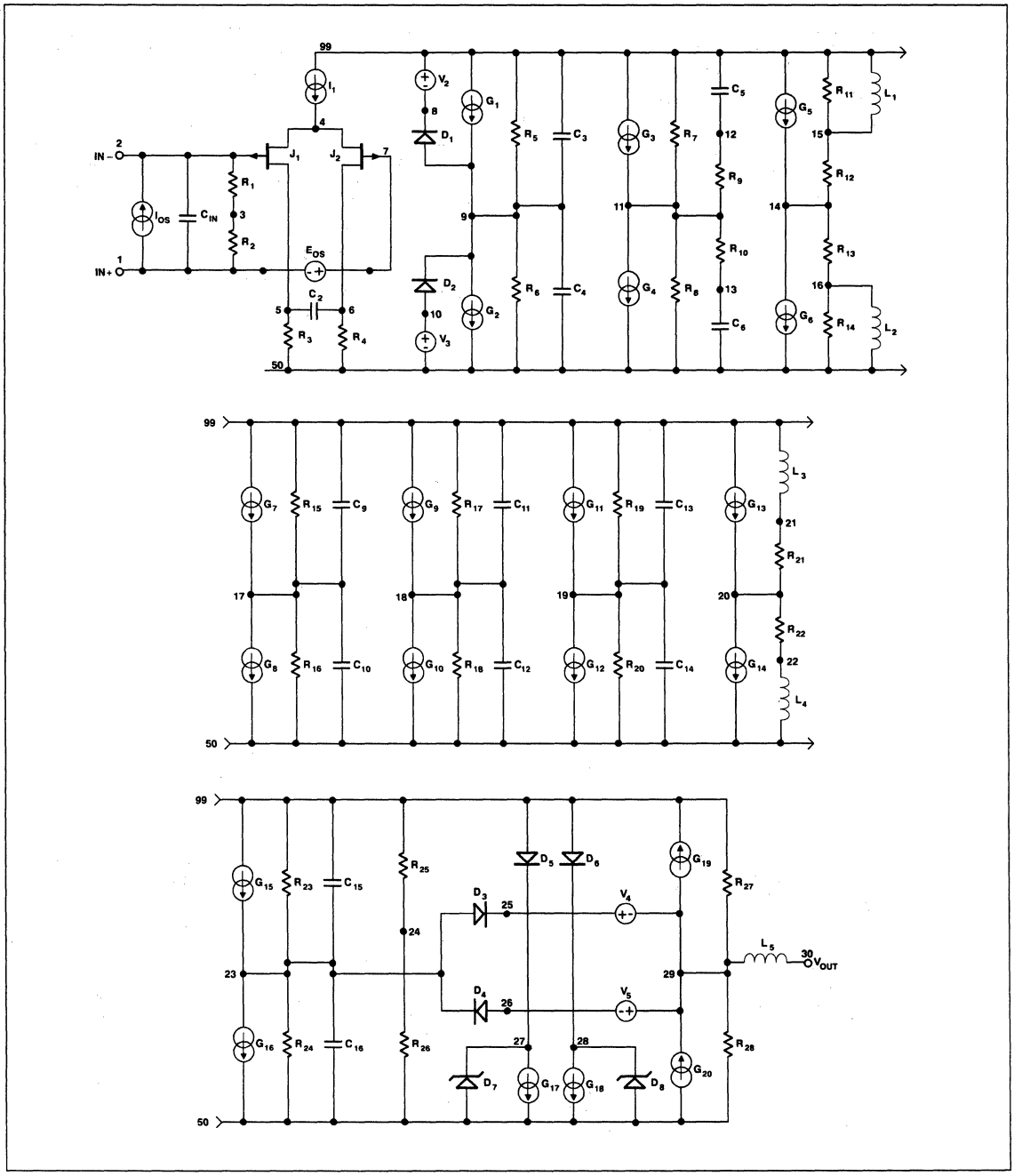


FIGURE 13: *OP-249 Macro-Model*

```
OP-249 MACRO-MODEL,  © PMI 1989
*
* subckt OP-249 1  2 30 99 50
*
INPUT STAGE & POLE AT 100MHz
*
r1   2    3          5E11
r2   1    3          5E11
r3   5    50         652.3
r4   6    50         652.3
cin  1    2          5E-12
c2   5    6          1.22E-12
i1   99   4          1E-3
ios  1    2          3.1E-12
eos  7    1          poly(1) 20 24 150E-6 1
j1   5    2    4     jx
j2   6    7    4     jx
*
* SECOND STAGE & POLE AT 12.2Hz
*
r5   9    99         326.1E6
r6   9    50         326.1E6
c3   9    99         40E-12
c4   9    50         40E-12
g1   99   9          poly(1) 5 6 4.25E-3 1.533E-3
g2   9    50         poly(1) 6 5 4.25E-3 1.533E-3
v2   99   8          2.9
v3   10   50         2.9
d1   9    8          dx
d2   10   9          dx
*
* POLE-ZERO PAIR AT 2MHz/4.0MHz
*
r7   11   99         1E6
r8   11   50         1E6
r9   11   12         1E6
r10  11   13         1E6
c5   12   99         37.79E-15
c6   13   50         37.79E-15
g3   99   11         9  24 1E-6
g4   11   50         24 9  1E-6
*
* ZERO-POLE PAIR AT 4MHz/8MHz
*
r11  99   15         1E6
r12  14   15         1E6
r13  14   16         1E6
r14  50   16         1E6
l1   99   15         19.89E-3
l2   50   16         19.89E-3
g5   99   14         11 24 1E-6
g6   14   50         24 11 1E-6
*
* POLE AT 20MHz
*
r15  17   99         1E6
r16  17   50         1E6
c9   17   99         7.96E-15
c10  17   50         7.96E-15
g7   99   17         14 24 1E-6
g8   17   50         24 14 1E-6
*
* POLE AT 50MHz
*
r17  18   99         1E6
r18  18   50         1E6
c11  18   99         3.18E-15
c12  18   50         3.18E-15
g9   99   18         17 24 1E-6
g10  18   50         24 17 1E-6
*
* POLE AT 50MHz
*
r19  19   99         1E6
r20  19   50         1E6
c13  19   99         3.18E-15
c14  19   50         3.18E-15
g11  99   19         18 24 1E-6
g12  19   50         24 18 1E-6
*
* COMMON-MODE GAIN NETWORK WITH ZERO AT 60kHz
*
r21  20   21         1E6
r22  20   22         1E6
l3   21   99         2.65
l4   22   50         2.65
g13  99   20         3  24 1.78E-11
g14  20   50         24 3  1.78E-11
*
* POLE AT 50MHz
*
r23  23   99         1E6
r24  23   50         1E6
c15  23   99         3.18E-15
c16  23   50         3.18E-15
g15  99   23         19 24 1E-6
g16  23   50         24 19 1E-6
*
* OUTPUT STAGE
*
r25  24   99         135E3
r26  24   50         135E3
r27  29   99         70
r28  29   50         70
l5   29   30         4E-7
g17  27   50         23 29 14.3E-3
g18  28   50         29 23 14.3E-3
g19  29   99         99 23 14.3E-3
g20  50   29         23 50 14.3E-3
v4   25   29         .4
v5   29   26         .4
d3   23   25         dx
d4   26   23         dx
d5   99   27         dx
d6   99   28         dx
d7   50   27         dy
d8   50   28         dy
*
* MODELS USED
*
• model jx PJF(BETA=1.175E-3 VTO=–2.000 IS=21E-12)
• model dx   D(IS=1E-15)
• model dy   D(IS=1E-15 BV=50)
• ends OP-249
```

FIGURE 14: *OP-249 SPICE Net List*

* PSpice is a registered trademark of MicroSim Corporation.
** HSPICE is a tradename of Meta-Software, Inc.

Dual, High-Speed, Current Feedback Operational Amplifier

OP-260

FEATURES

- Very High Slew Rate ..... 550V/μs Typ
- -3dB Bandwidth (A_V=+10) ..... 40MHz Typ
- Bandwidth Independent of Gain
- Unity-Gain Stable
- Low Supply Current ..... 4.5mA per amp Typ

ORDERING INFORMATION†

T_A = 25°C V_{IOS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	PLASTIC	LCC 20-CONTACT	
3.5	OP260AJ*	–	OP260ARC/883	MIL
3.5	OP260EJ	–	–	XIND
5.0	OP260FJ	–	–	XIND
7.0	–	OP260GP	–	XIND
7.0	–	OP260GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerDIP, plastic DIP, and TO-can packages.

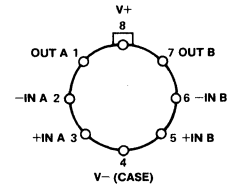
†† For availability and burn-in information on SO packages, contact your local sales office.

GENERAL DESCRIPTION

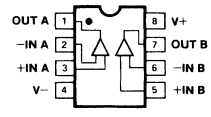
The dual OP-260 represents a new concept in monolithic operational amplifiers. Built on PMI's high-speed bipolar process, the OP-260

continued

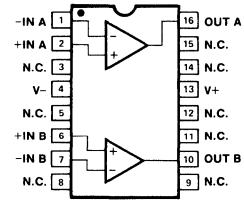
PIN CONNECTIONS



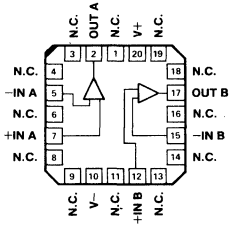
TO-99
(J-Suffix)



EPOXY MINI-DIP
(P-Suffix)
CERDIP
(Z-Suffix)

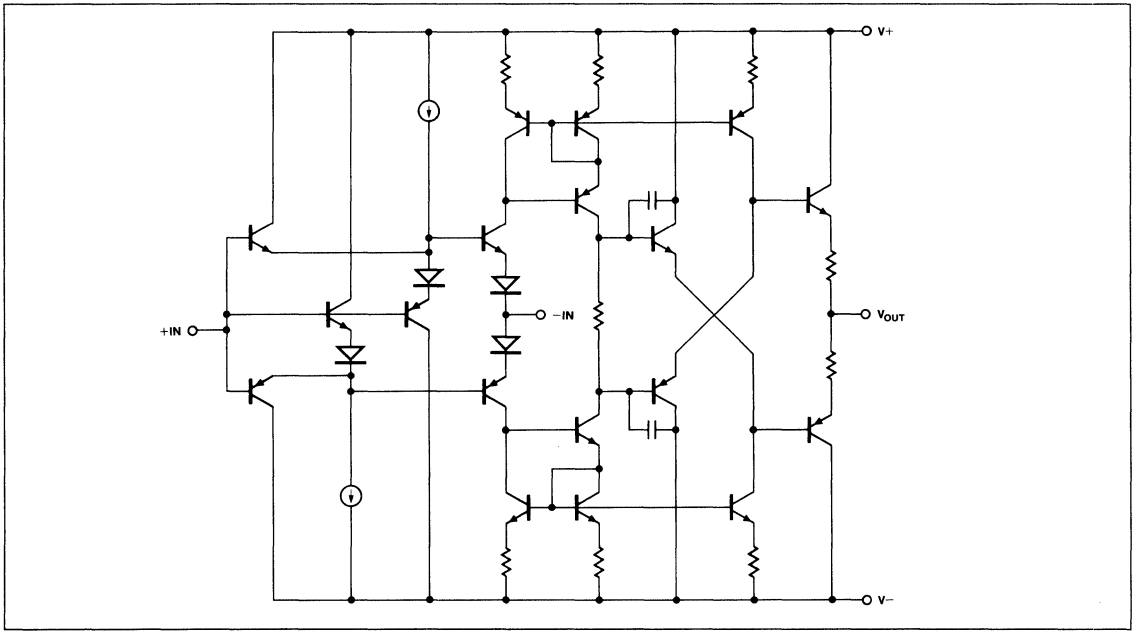


16-PIN SOL
(S-Suffix)



20-CONTACT
HERMETIC LCC
(RC-Suffix)

SIMPLIFIED SCHEMATIC (One of Two Amplifiers)



GENERAL DESCRIPTION *Continued*

employs current feedback to provide consistently wideband operation regardless of gain. The OP-260's –3dB bandwidth of 90MHz at A_V=+1 combines with a slew rate of 1000V/µs for extremely high-speed operation. For its high-speed bandwidth, the OP-260 requires only 4.5mA of supply current per amplifier, a considerable power savings over other high-speed operational amplifiers.

The OP-260 is easy to design with, since most of the circuit assumptions for voltage feedback amplifiers can also be used for current feedback amplifiers. The two independent amplifiers of the OP-260 allow two channel amplification with matched AC performance. It is also ideal for high-speed instrumentation amplifiers. Other applications for the OP-260 include ultrasound and sonar systems, video amplifiers and high-speed data acquisition systems.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Input Voltage ..... Supply Voltage
Differential Input Voltage ..... ±1V
Inverting Input Current ..... ±7mA Continuous
..... ±20mA Peak
Output Short-Circuit Duration ..... 10 sec
Operating Temperature Range
OP-260A, (J, RC, Z) ..... –55°C to +125°C
OP-260E/F (J, Z) ..... –40°C to +85°C
OP-260G (P, S) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +175°C
Junction Temperature Range (J, RC) ..... –65°C to +175°C
Junction Temperature Range (P, S) ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
TO-99 (J)	145	16	°C/W
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, V_{CM} = 0V, R_F = 2.5kΩ, T_A = +25°C, unless otherwise noted.

			OP-260A/E			OP-260F			OP-260G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{IOS}		–	1	3.5	–	2	5	–	3	7	mV
Input Bias Current	I_{B+} I_{B-}	Noninverting Input Inverting Input	– –	0.2 3	1 8	– –	0.3 4	2 10	– –	0.5 5	3 15	µA
Input Bias Current Common-Mode Rejection Ratio	$CMRRI_{B-}$	Inverting Input V_{CM} = ±11V	–	0.04	0.1	–	0.06	0.2	–	0.1	0.5	µA/V
Input Bias Current Power Supply Rejection Ratio	$PSRRI_{B-}$ $PSRRI_{B+}$	Inverting Input Noninverting Input V_S = ±9V to ±18V	– –	0.02 0.002	0.1 0.02	– –	0.04 0.004	0.2 0.04	– –	0.05 0.01	0.5 0.1	µA/V
Common-Mode Rejection	CMR	V_{CM} = ±11V	56	62	–	50	60	–	50	60	–	dB
Power Supply Rejection	PSR	V_S = ±9V to ±18V	66	72	–	60	66	–	60	66	–	dB
Open-Loop Transimpedance	R_T	R_L = 1kΩ V_O = ±10V	5	7	–	4	5	–	4	5	–	MΩ
Input Voltage Range	IVR		±11	–	–	±11	–	–	±11	–	–	V
Output Voltage Swing	V_O	R_L = 1kΩ I_{OUT} = ±20mA	±12 ±11	±12.6 ±11.5	– –	±12 ±11	±12.6 ±11.5	– –	±12 ±11	±12.6 ±11.5	– –	V
Supply Current	I_{SY}	No Load, Both Amplifiers	–	9	10.5	–	9	10.5	–	9	10.5	mA
Slew Rate	SR	A_V = +1, V_O = ±10V, R_L = 1kΩ, Test at V_O = ±5V	–	1000	–	–	1000	–	–	1000	–	V/µs
		A_V = +10, V_O = ±10V, R_L = 1kΩ, Test at V_O = ±5V	375	550	–	300	550	–	300	550	–	
		A_V = +10, V_O = ±10V, R_L = 1kΩ, Test at V_O = ±5V 8-pin Hermetic DIP (Z) Package	300	–	–	300	–	–	–	–	–	

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $V_{CM} = 0V$, $R_F = 2.5k\Omega$, $T_A = 25°C$, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-260A/E MIN	OP-260A/E TYP	OP-260A/E MAX	OP-260F MIN	OP-260F TYP	OP-260F MAX	OP-260G MIN	OP-260G TYP	OP-260G MAX	UNITS
–3dB Bandwidth	BW	–3dB point, $A_V = -1$ $R_L = 500\Omega$, $A_V = +1$ $A_V = +10$	– – –	55 90 40	– – –	– – –	55 90 40	– – –	– – –	55 90 40	– – –	MHz
Settling Time	t_S	$A_V = -1$, 10V step, 0.1%	–	250	–	–	250	–	–	250	–	ns
Input Capacitance	C_{IN}	Noninverting and Inverting Inputs	–	4.5	–	–	4.5	–	–	4.5	–	pF
Channel Separation	CS	$f_O = 100kHz$, $V_O = 10Vp\text{-}p$, $R_L = 100\Omega$	–	100	–	–	100	–	–	100	–	dB

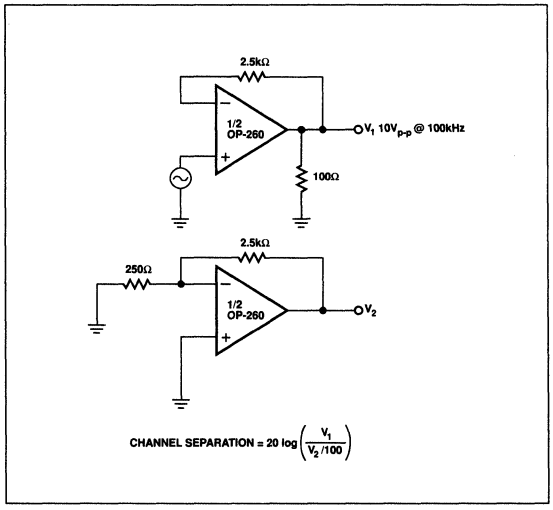
ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $V_{CM} = 0V$, $R_F = 2.5k\Omega$, $-55°C \le T_A \le +125°C$, for the OP-260A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-260A MIN	OP-260A TYP	OP-260A MAX	UNITS
Input Offset Voltage	V_{IOS}		–	1.8	6	mV
Average Input Offset Voltage Drift	TCV_{IOS}		–	8	–	µV/°C
Input Bias Current	I_{B+} I_{B-}	Noninverting Input Inverting Input	– –	0.3 4	2 12	µA
Input Bias Current Common Mode Rejection Ratio	$CMRRI_{B-}$	Inverting Input $V_{CM} = \pm11V$	–	0.05	0.2	µA/V
Input Bias Current Power Supply Rejection Ratio	$PSRRI_{B-}$ $PSRRI_{B+}$	Inverting Input Noninverting Input $V_S = \pm9V$ to $\pm18V$	– –	0.03 0.003	0.2 0.05	µA/V
Common Mode Rejection	CMR	$V_{CM} = \pm11V$	52	58	–	dB
Power Supply Rejection	PSR	$V_S = \pm9V$ to $\pm18V$	62	70	–	dB
Open-Loop Transimpedance	R_T	$R_L = 1k\Omega$, $V_O = \pm10V$	3	4.8	–	MΩ
Input Voltage Range	IVR		±11	–	–	V
Output Voltage Swing	V_O	$R_L = 1k\Omega$ $I_{OUT} = \pm20mA$	±11.5 ±10.5	±12.4 ±11.1	– –	V
Supply Current	I_{SY}	No load, Both Amplifiers	–	9	11.5	mA

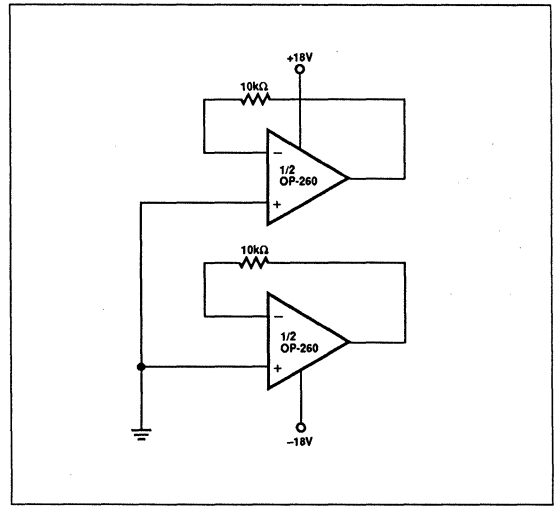
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $V_{CM} = 0V$, $R_F = 2.5k\Omega$, $-40°C \leq T_A \leq +85°C$ for the OP-260E/F/G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-260E MIN	OP-260E TYP	OP-260E MAX	OP-260F MIN	OP-260F TYP	OP-260F MAX	OP-260G MIN	OP-260G TYP	OP-260G MAX	UNITS
Input Offset Voltage	V_{IOS}		–	1.4	6	–	2.5	8	–	3.7	10	mV
Average Input Offset Voltage Drift	TCV_{IOS}		–	6	–	–	8	–	–	10	–	µV/°C
Input Bias Current	I_{B+} I_{B-}	Noninverting Input Inverting Input	– –	0.3 4	2 12	– –	0.4 5	3 15	– –	0.6 7	5 20	µA
Input Bias Current Common Mode Rejection Ratio	$CMRRI_{B-}$	Inverting Input $V_{CM} = \pm 11V$	–	0.05	0.2	–	0.7	0.4	–	0.15	1.0	µA/V
Input Bias Current Power Supply Rejection Ratio	$PSRRI_{B-}$ $PSRRI_{B+}$	Inverting Input Noninverting Input	– –	0.03 0.003	0.2 0.05	– –	0.05 0.005	0.4 0.1	– –	0.1 0.01	1.0 0.2	µA/V
Common Mode Rejection	CMR	$V_{CM} = \pm 11V$	52	60	–	50	58	–	50	58	–	dB
Power Supply Rejection	PSR	$V_S = \pm 9V$ to $\pm 15V$	62	70	–	60	64	–	60	64	–	dB
Open-Loop Transimpedance	R_T	$R_L = 1k\Omega$, $V_O = \pm 10V$	3	5	–	2	4	–	2	4	–	MΩ
Input Voltage Range	IVR		±11	–	–	±11	–	–	±11	–	–	V
Output Voltage Swing	V_O	$R_L = 1k\Omega$ $I_{OUT} = \pm 20mA$	±11.5 ±10.5	±12.5 ±11.1	– –	±11.5 ±10.5	±12.5 ±11.1	– –	±11.5 ±10.5	±12.5 ±11.1	– –	V
Supply Current	I_{SY}	No Load, Both Amplifiers	–	9	11.5	–	9	11.5	–	9	11.5	mA

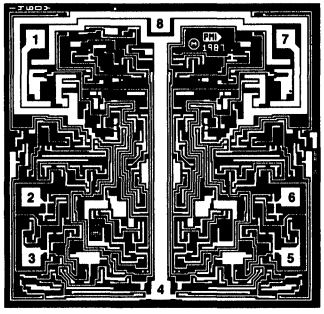
CHANNEL SEPARATION TEST CIRCUIT



BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.089 x 0.086 inch, 7,654 sq. mils
(2.26 x 2.18 mm, 4.93 sq. mm)

1. OUT A
2. - IN A
3. + IN A
4. V-
5. + IN B
6. - IN B
7. OUT B
8. V +

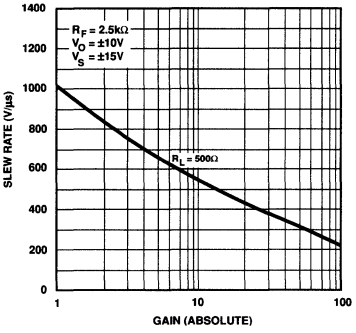
WAFER TEST LIMITS at V_S = ±15V, V_{CM} = 0V, R_F = 2.5kΩ, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-260GBC LIMITS	UNITS
Input Offset Voltage	V_{IOS}		5	mV MAX
Input Bias Current	I_{B+} I_{B-}	Noninverting Input Inverting Input	2 10	µA MAX
Input Bias Current Common Mode Rejection Ratio	$CMRRI_B$	Inverting Input V_{CM} = +11V	0.2	µA/V MAX
Input Bias Current Power Supply Rejection Ratio	$PSRRI_{B-}$ $PSRRI_{B+}$	Inverting Input Noninverting Input V_S = ±9V to ±18V	0.2 0.04	µA/V MAX
Common Mode Rejection	CMR	V_{CM} = ±11V	50	dB MIN
Power Supply Rejection	PSR	V_S = ±9V to ±18V	60	dB MIN
Open-Loop Transimpedance	R_T	R_L = 1kΩ, V_O = ±10V	4	MΩ MIN
Input Voltage Range	IVR		±11	V MIN
Output Voltage Swing	V_O	R_L = 1kΩ I_{OUT} = ±20mA	±12 ±11	V MIN
Supply Current	I_{SY}	No Load, Both Amplifiers	10.5	mA MAX

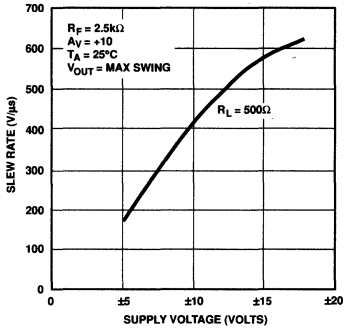
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS

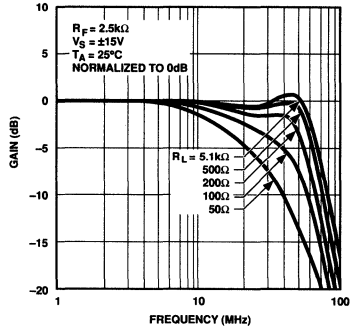
SLEW RATE vs GAIN



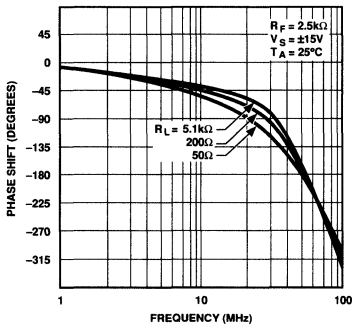
SLEW RATE vs SUPPLY VOLTAGE



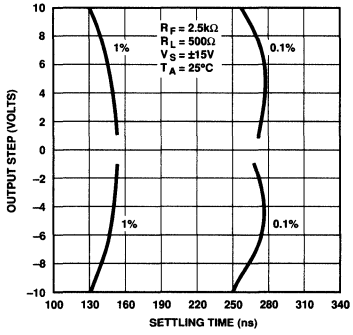
GAIN vs FREQUENCY A_V = –1



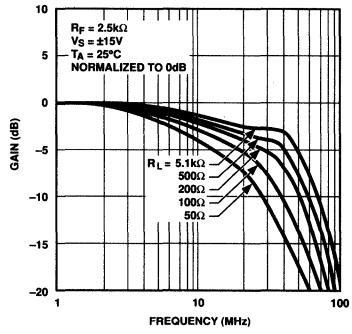
PHASE SHIFT vs FREQUENCY A_V = –1



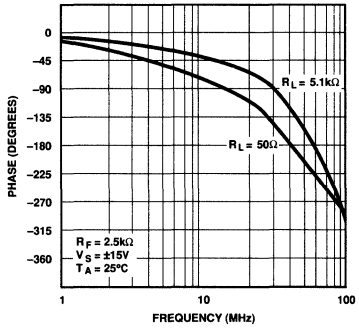
SETTLING TIME vs OUTPUT STEP A_V = –1



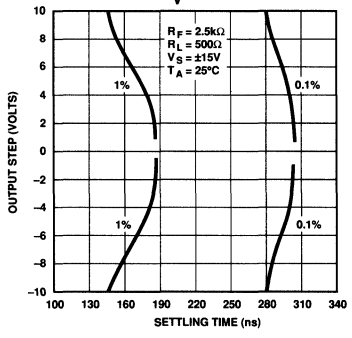
GAIN vs FREQUENCY A_V = –10



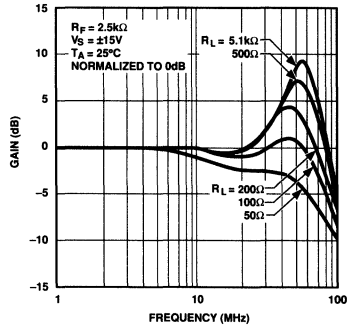
PHASE vs FREQUENCY A_V = –10



SETTLING TIME vs OUTPUT STEP A_V = –10

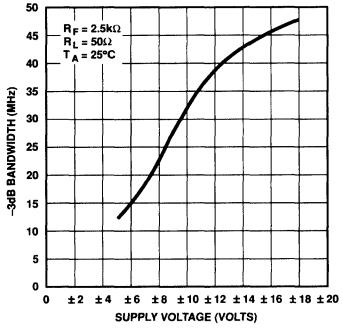


GAIN vs FREQUENCY A_V = +1

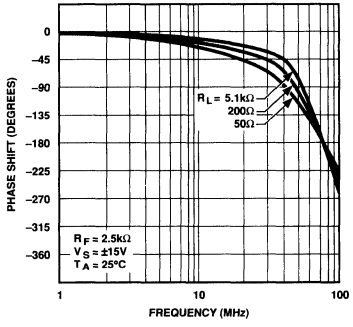


TYPICAL ELECTRICAL CHARACTERISTICS *Continued*

SMALL-SIGNAL –3dB BANDWIDTH vs SUPPLY VOLTAGE
A_V = +1



PHASE SHIFT vs FREQUENCY
A_V = +1



GAIN vs FREQUENCY
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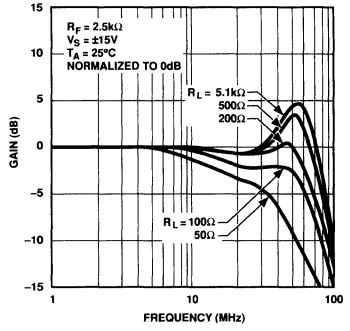
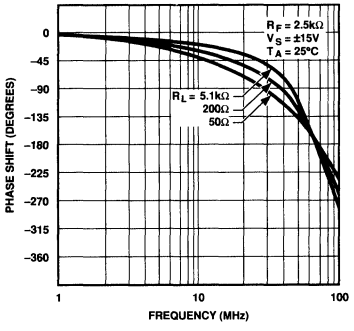
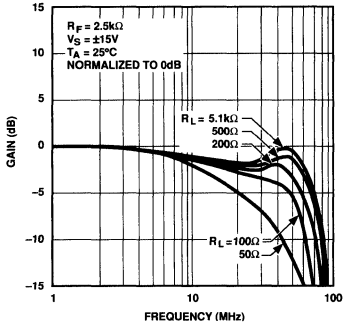


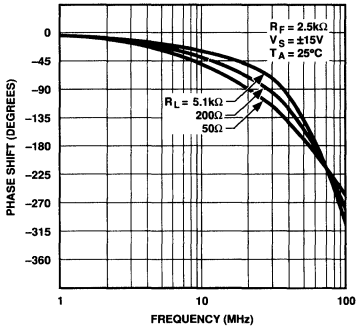
PHASE SHIFT vs FREQUENCY
A_V = +2



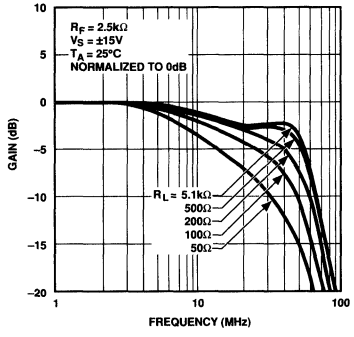
GAIN vs FREQUENCY
A_V = +5



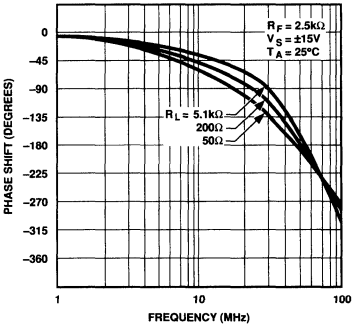
PHASE SHIFT vs FREQUENCY
A_V = +5



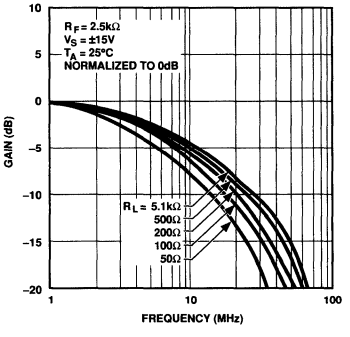
GAIN vs FREQUENCY
A_V = +10



PHASE SHIFT vs FREQUENCY
A_V = +10

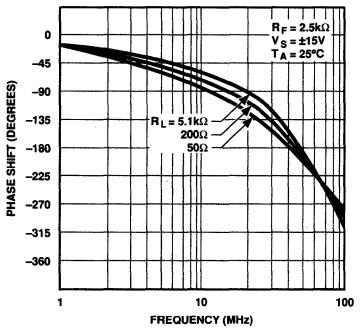


GAIN vs FREQUENCY
A_V = +50

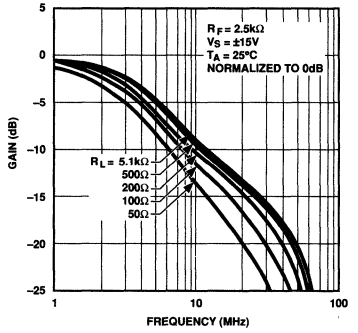


TYPICAL ELECTRICAL CHARACTERISTICS *Continued*

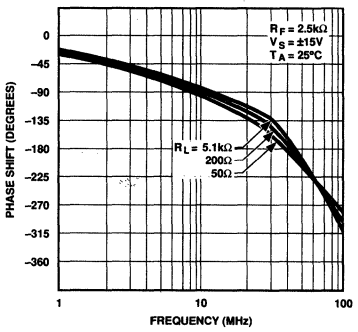
PHASE SHIFT vs FREQUENCY
A_V = +50



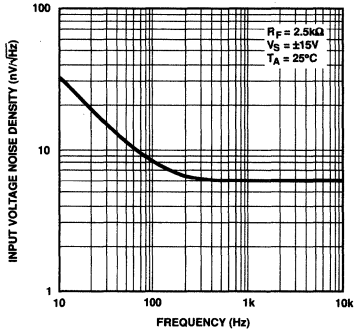
GAIN vs FREQUENCY
A_V = +100



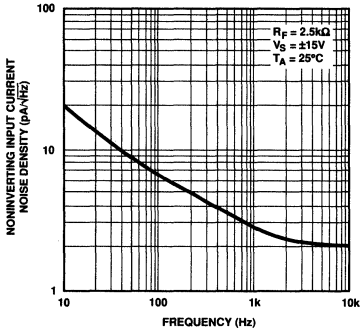
PHASE SHIFT vs FREQUENCY
A_V = +100



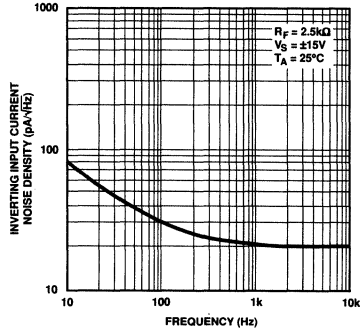
INPUT VOLTAGE NOISE DENSITY vs FREQUENCY



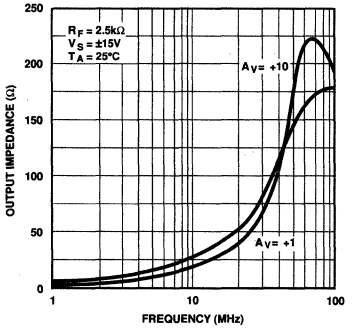
NONINVERTING INPUT CURRENT NOISE DENSITY vs FREQUENCY



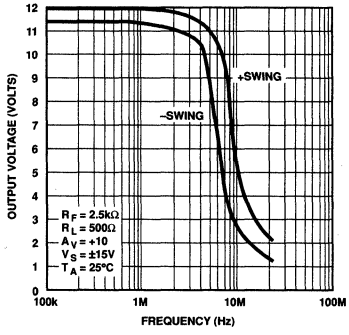
INVERTING INPUT CURRENT NOISE DENSITY vs FREQUENCY



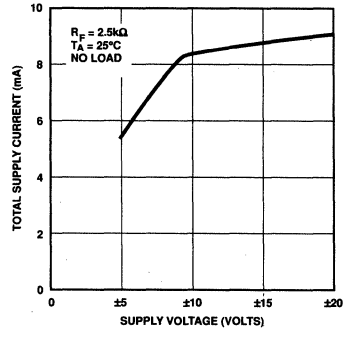
OUTPUT IMPEDANCE vs FREQUENCY



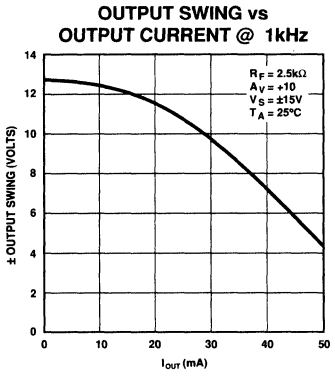
MAXIMUM OUTPUT SWING vs FREQUENCY

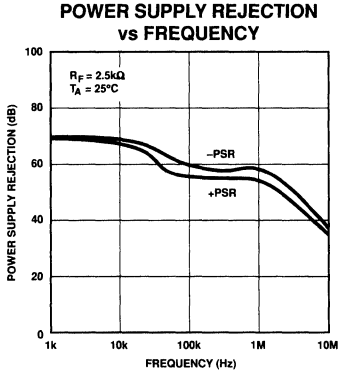


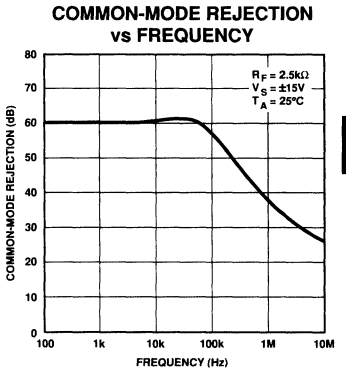
TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE



TYPICAL ELECTRICAL CHARACTERISTICS *Continued*







2

APPLICATIONS INFORMATION

CURRENT VERSUS VOLTAGE FEEDBACK AMPLIFIERS

The dual OP-260 employs a unique circuit topology that sets it apart from conventional op amps. By using a transimpedance amplifier configuration, the OP-260 provides substantial improvements in bandwidth and slew rate over voltage feedback op amps. Figure 1 compares models of these two different amplifier configurations.

A voltage feedback op amp multiplies the differential voltage at its inputs by its open-loop gain. The feedback loop forces the output to a voltage that, when divided by R_1 and R_2, equalizes the input voltages. Unlike a voltage feedback op amp, which has high impedance inputs, the current feedback amplifier has a high and a low impedance input. The current feedback amplifier's input stage consists of a unity-gain voltage buffer between the noninverting and inverting inputs. The inverting "input" is in reality a low impedance output. Current can flow into or out of the inverting input. A transimpedance stage follows the input buffer that converts the buffer output current into a linearly proportional amplifier output voltage.

The current feedback amplifier loop works in the following fashion (Figure 1b). As the noninverting input voltage rises, the inverting input follows and the buffer sources current through R_1. This current, multiplied by the transimpedance stage, causes the amplifier's output voltage to rise until the current flowing into R_2 from the amplifier's output equalizes the current through R_1, replacing the buffer's output current. At steady state, only a very small buffer output current must flow to sustain the proper output voltage. The ratio $(1 + R_2/R_1)$ determines the

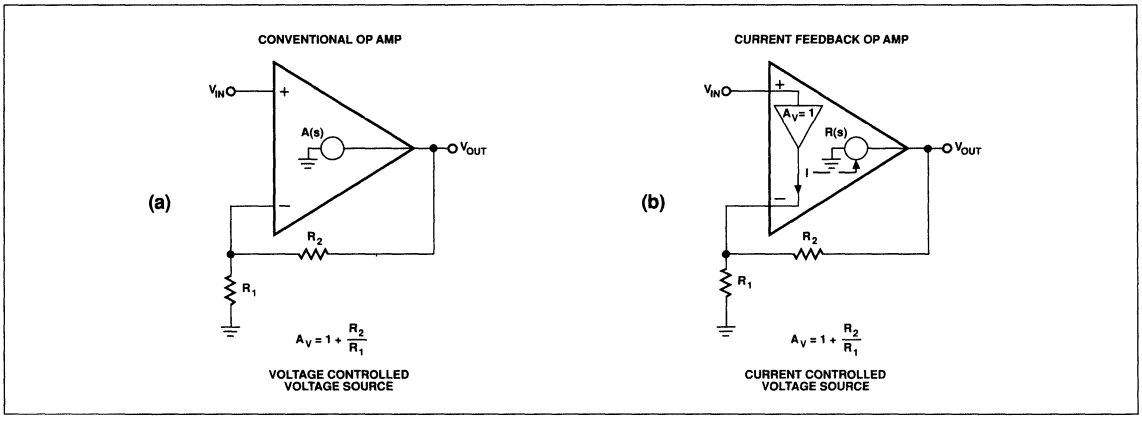


FIGURE 1: *The conventional op amp (a) can be modelled as a voltage-controlled voltage source. In contrast, the current feedback op amp (b), resembles a current-controlled voltage source.*

closed-loop gain of the circuit. The result is that when designing with current feedback amplifiers the familiar op amp assumptions can still be used for circuit analysis:

1. The voltage across the inputs equals zero.
2. The current into the inputs equals zero.

BANDWIDTH VERSUS GAIN

A unique feature of the current feedback amplifier design is that the closed-loop bandwidth remains relatively constant as a function of closed-loop gain. Voltage feedback op amps suffer from a bandwidth reduction as closed-loop gain increases, as quantified by the gain-bandwidth product (GBWP). This is illustrated in Figure 2 which shows the frequency response of the OP-260 for various closed-loop gains and the frequency response of a voltage feedback op amp with a gain-bandwidth product of 30MHz. The bandwidth of the OP-260 is much less dependent upon closed-loop gain than the voltage feedback op amp.

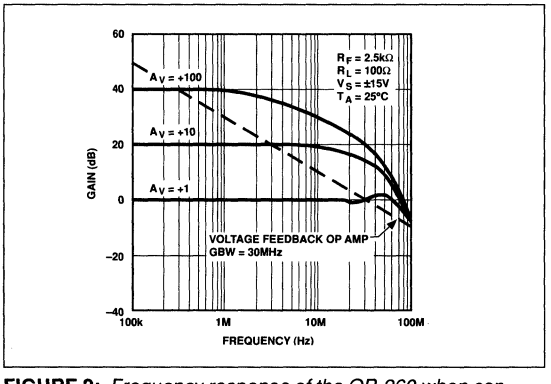


FIGURE 2: *Frequency response of the OP-260 when connected in various closed-loop gains with R_F = 2.5kΩ and R_L = 100Ω. Note that the frequency response of the OP-260 does not follow the asymptotic roll-off characteristic of a voltage feedback op-amp.*

FEEDBACK RESISTANCE AND BANDWIDTH

The closed-loop frequency response of the OP-260 shown in Figure 2 applies for a fixed feedback resistor of 2.5kΩ. The frequency response of a current feedback amplifier is primarily dependent on the value of the feedback resistor. The design of the OP-260 has been optimized for a feedback resistance of 2.5kΩ. By holding the feedback resistor value constant, the –3dB frequency point will also remain constant within a moderate range of closed-loop gain.

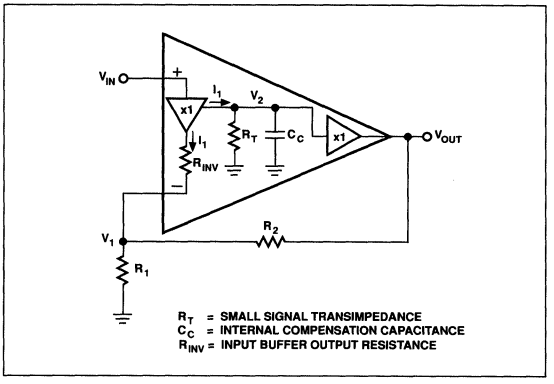


FIGURE 3: *Simple frequency response model of the current feedback amplifier.*

The model shown in Figure 3 can be used to determine the frequency response of a current feedback amplifier. With this model, the frequency response dependency on the value of the feedback resistance is easily seen.

From the model of Figure 3, nodal equations may be written for V_1 and V_2.

$$V_1 = \frac{V_{IN}\left(\frac{R_2}{R_{INV}}\right) + V_{OUT}}{1 + \frac{R_2}{R_1} + \frac{R_2}{R_{INV}}}$$

$$V_2 = \frac{R_T}{1 + sR_TC_C} I_1$$

where $I_1 = \frac{V_{IN} - V_1}{R_{INV}} = V_1\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{V_{OUT}}{R_2}$, and $V_{OUT} = V_2$.

Combining these equations yields:

$$V_{OUT} = \left[\left(\frac{V_{IN}\left(\frac{R_2}{R_{INV}}\right) + V_{OUT}}{1 + \frac{R_2}{R_1} + \frac{R_2}{R_{INV}}}\right)\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{V_{OUT}}{R_2}\right] \frac{R_T}{1 + sR_TC_C}$$

If the transimpedance of the amplifier, R_T, is » R_2 and R_{INV}, then the transfer function may be simplified to:

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{1 + \frac{R_2}{R_1}}{1 + s\left[R_2 + \left(1 + \frac{R_2}{R_1}\right)R_{INV}\right]C_C}$$

The transfer function shows that the dominant closed-loop pole is mainly dependent on the value of the feedback resistance, R_2, and the internal compensation capacitor, C_C. For example, at unity gain, where R_1 is infinite, R_2 determines the –3dB frequency.

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{1}{1 + sR_2C_C}$$

$$f_{-3dB} = \frac{1}{2\pi R_2 C_C}$$

where $R_2 \gg R_{INV}$.

For higher gains, the –3dB frequency is determined by R_2 plus the output resistance of the buffer, R_{INV} (typically 100Ω), which is multiplied by the closed-loop gain. As the closed-loop gain increases, the multiplying effect on R_{INV} becomes dominant, causing the bandwidth to decrease. However, the closed-loop bandwidth of a current feedback amplifier still far exceeds that of a voltage feedback op amp for moderate values of gain.

Figure 4 shows the effect of the feedback resistance on the bandwidth of the OP-260 for various closed-loop gains.

2

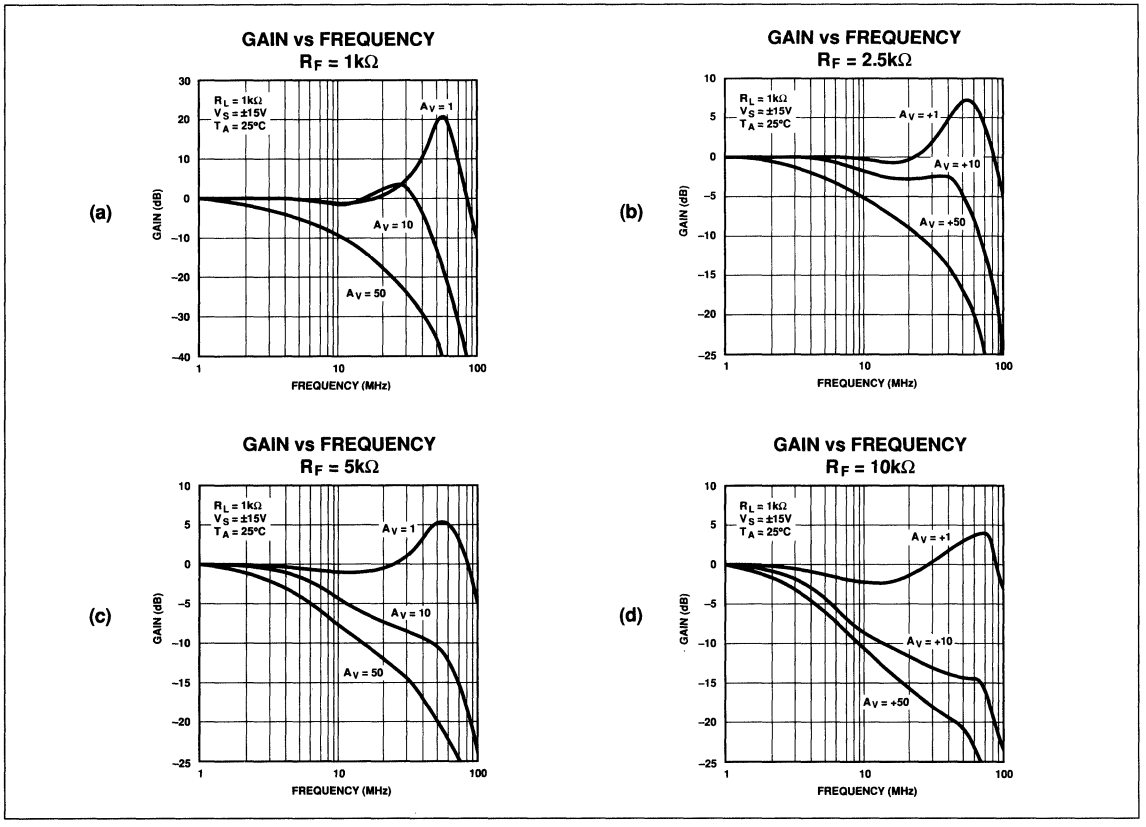


FIGURE 4: *Bandwidth will vary with feedback resistance. Peaking increases as the feedback resistance is decreased. R_F = 2.5kΩ is the recommended value. All graphs are normalized to 0dB.*

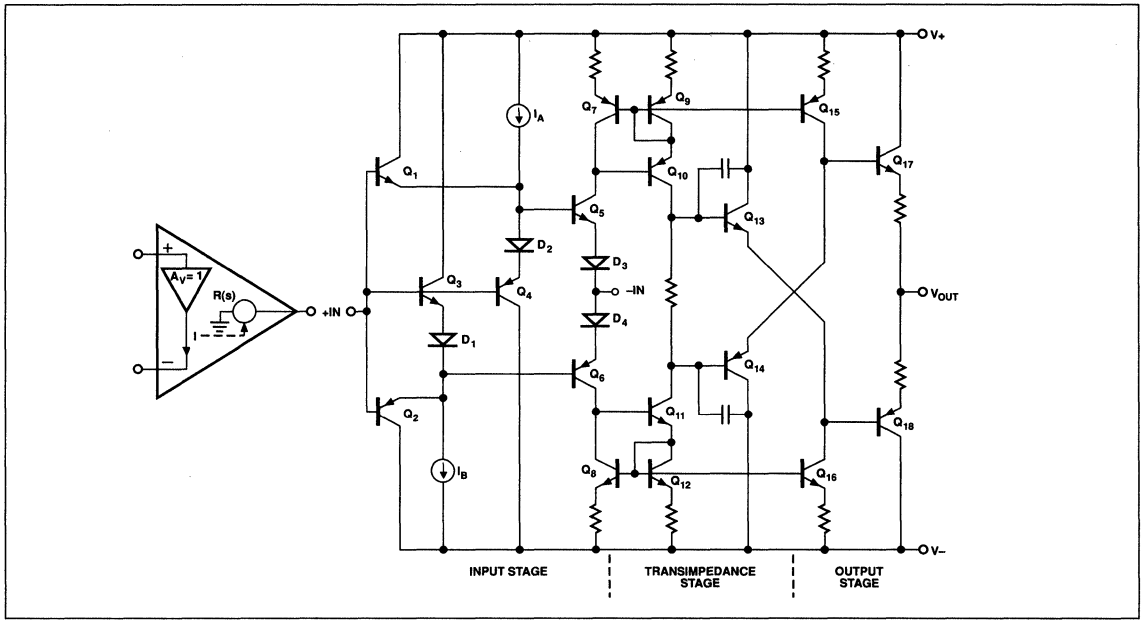


FIGURE 5: *Simplified schematic of the OP-260 showing the three stages of the amplifier.*

SLEW RATE AND GAIN

The simplified schematic in Figure 5 shows the three stages of the OP-260. The input stage consists of a unity-gain emitter-follower amplifier. Q_5 and Q_6 form a class AB output stage at the inverting input which can source or sink current. The current flowing through the inverting input is sensed by the top current mirror, formed by Q_7, Q_9, and Q_{10}, or the bottom current mirror, formed by Q_8, Q_{11}, and Q_{12}. When the buffer sources current to a load, current flows out of the inverting input, increasing Q_5's collector current and causing more current to flow through Q_9 and Q_{15}. This increases the base drive to the output transistor Q_{17}. Simultaneously, the increased current in Q_9 drives Q_{13} which reduces base drive to the complementary output transistor Q_{18}. This push-pull action produces a very fast output slew rate. For a small voltage step, the OP-260's slew rate is dependent on the available current from the two current sources (I_A and I_B) that drive Q_5 and Q_6.

To increase the slew rate, transistors Q_1 and Q_2 have been added to boost the base drive to Q_5 and Q_6. In closed-loop gains below 10, a large input step will turn on Q_1 or Q_2 increasing the slew rate dramatically as illustrated in Figure 6.

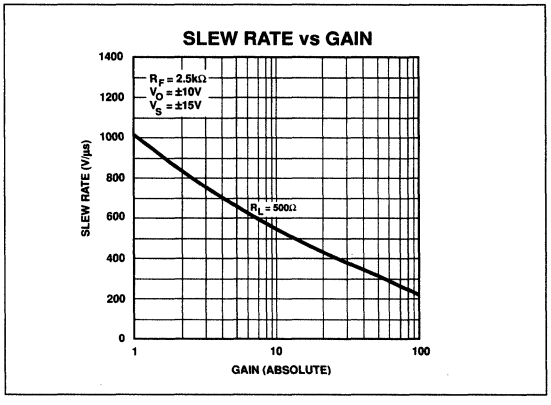


FIGURE 6: *Slew rate of the OP-260 is highest in gains below ±10.*

AMPLIFIER NOISE PERFORMANCE

Simplified noise models of the OP-260 in the noninverting and inverting amplifier configurations are shown in Figure 7. All resistors are assumed to be noiseless.

For the noninverting amplifier, the equivalent input voltage noise, referred to the input, is:

$$E_n = \sqrt{(R_5\, i_{nn})^2 + e_n^2 + \frac{(R_2\, i_{ni})^2}{(A_{VLC})^2}}$$

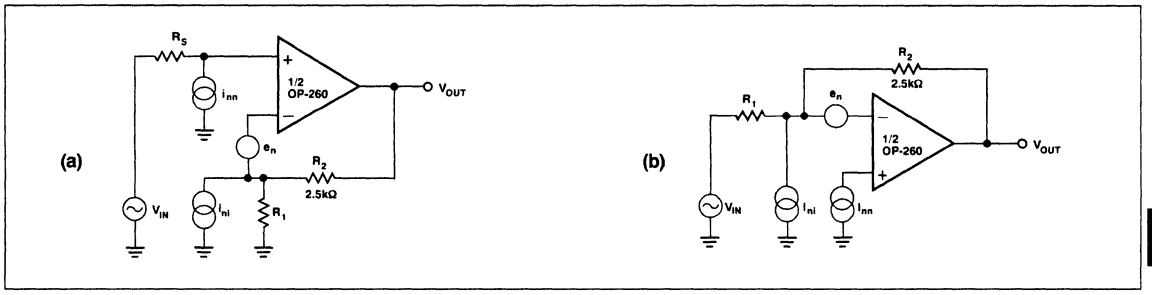


FIGURE 7: *Simplified noise models for the OP-260 in noninverting (a) and inverting (b) gain.*

where:

E_N = total input referred noise
e_n = amplifier voltage noise
i_{nn} = noninverting input current noise
i_{ni} = inverting input current noise
R_S = source resistance
A_{VCL} = closed loop gain = $1 + R_2/R_1$

For the inverting amplifier, the equivalent input voltage noise, referred to the input, is:

$$E_n = \sqrt{e_n^2 \left(\frac{1 + |A_{VLC}|}{|A_{VLC}|}\right)^2 + \frac{(R_2\, i_{ni})^2}{(|A_{VLC}|)^2}}$$

assuming $R_S \ll R_1$. A_{VCL} = closed loop gain = $-R_2/R_1$.

Typical values @ 1kHz for the noise parameters of the OP-260 are:

e_n = 5.0nV/$\sqrt{Hz}$
i_{nn} = 3.0pA/$\sqrt{Hz}$
i_{ni} = 20.0pA/$\sqrt{Hz}$

SHORT CIRCUIT PERFORMANCE

To avoid sacrificing bandwidth and slew rate performance the OP-260's output is **not** short circuit protected. Do not short the amplifier's output to ground or to the supplies. Also, the buffer output current should not exceed a value of ±20mA peak or ±7mA continuous.

POWER SUPPLY BYPASSING AND LAYOUT CONSIDERATIONS

Proper power supply bypassing is critical in all high-frequency circuit applications. For stable operation of the OP-260, the power supplies must maintain a low impedance-to-ground over an extremely wide bandwidth. This is most critical when driving a low resistance or large capacitance, since the current required to drive the load comes from the power supplies. A 10µF and 0.1µF bypass capacitor are recommended for each supply, as shown in Figure 8, and will provide adequate high-frequency bypassing in most applications. The bypass capacitors should be placed at the supply pins of the OP-260. As with all high frequency amplifiers, circuit layout is a critical factor in obtaining optimum performance from the OP-260. Proper high frequency layout reduces unwanted signal coupling in the circuit. When breadboarding a high frequency circuit, use direct point-to-point wiring, keeping all lead lengths as short as possible. Do not use wire-wrap boards or "plug-in" prototyping boards.

During PC board layout, keep all lead lengths and traces as short as possible to minimize inductance. The feedback and gain-setting resistors should be as close as possible to the inverting input to reduce stray capacitance at that point. To further reduce stray capacitance, remove the ground plane from the area around the inputs of the OP-260. Elsewhere, the use of a solid unbroken ground plane will insure a good high-frequency ground.

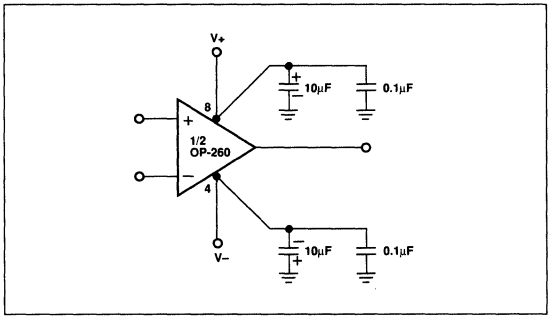


FIGURE 8: *Proper power supplying bypassing is required to obtain optimum performance with the OP-260.*

APPLICATIONS

NONINVERTING AMPLIFIER

The OP-260 can be used as a voltage-follower or noninverting amplifier as shown in Figure 9. A current feedback amplifier in this configuration yields the same transfer function as a voltage feedback op amp:

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_2}{R_1}.$$

Remember to use a 2.5kΩ feedback resistor in voltage-follower application.

In noninverting applications, stray capacitance at the inverting input of a current feedback amplifier will cause peaking which will increase as the closed-loop gain decreases. The gain setting resistor, R_1, is in parallel with this stray capacitance creating a zero in the closed-loop response. For large noninverting gains, R_1 is small, creating a very high frequency open-loop pole which has limited effect on the closed-loop response. As the noninverting gain is decreased, R_1 becomes larger and the stray zero becomes lower in frequency, having a much greater effect on the closed-loop response. To reduce peaking at low noninverting gains, place a series resistor, R_C, in series with the noninverting input as shown in Figure 9. This resistor combines with the stray capacitance at the noninverting input to form a low-pass filter that will reduce the peaking. The value of R_C should be determined experimentally in the actual PCB layout. Less peaking will occur in inverting gain configurations since the inverting input is a virtual ground which forces a constant voltage across the stray capacitance.

A common practice to stabilize voltage feedback op amps is to use a capacitor across the feedback resistance. This creates a zero in the voltage feedback amplifier response to offset the loss of phase margin due to a parasitic pole. In current feedback amplifiers, this technique will cause the amplifier to become unstable because the closed-loop bandwidth will increase beyond the stable operating frequency. For the same reason, current feedback amplifiers will not be stable in integrator applications.

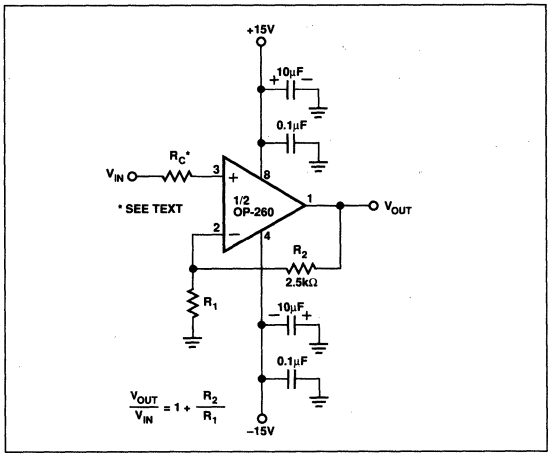


FIGURE 9: *The OP-260 as a voltage follower or noninverting amplifier.*

INVERTING AMPLIFIER

The OP-260 is also capable of operation as an inverting amplifier (see Figure 10). The transfer function of this circuit is identical to that using a voltage feedback op amp:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_2}{R_1}.$$

An optional offset voltage trim is shown in Figure 11.

AUTOMATIC GAIN CONTROL AMPLIFIER

One of the shortcomings of using voltage feedback op amps in an Automatic-Gain-Control amplifier is that its bandwidth drops off rapidly as gain increases, limiting the useful bandwidth. However, for current feedback amplifiers, bandwidth is relatively independent of gain,

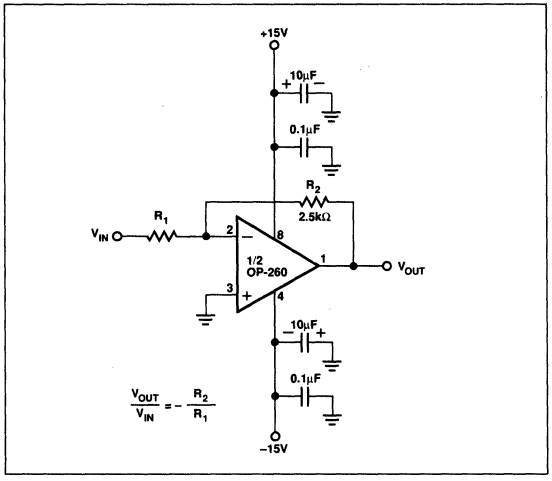


FIGURE 10: *The OP-260 as an inverting amplifier.*

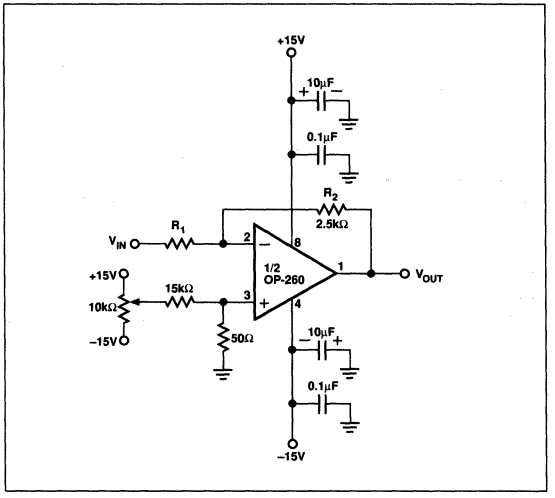


FIGURE 11: *Optional offset voltage trim circuit for the OP-260.*

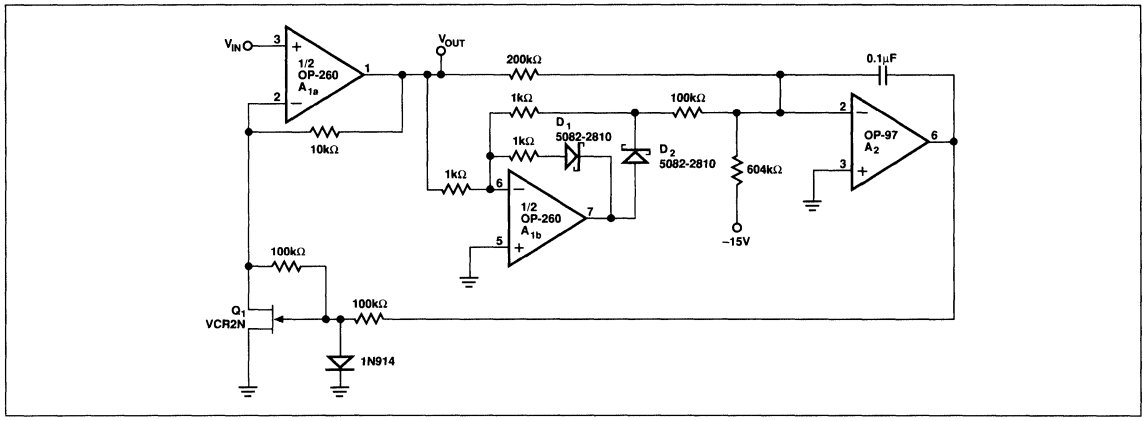


FIGURE 12: *The OP-260 eliminates the problem of variable bandwidth in AGC amplifiers using voltage feedback op amps.*

eliminating this problem. Figure 12 shows a simple AGC amplifier design using the OP-260. Amplifier A_{1a} is used as the gain stage. Its output is rectified by the second amplifier A_{1b}. If the output voltage swings more negative, diode D_2 forward biases and D_1 reverse biases, closing the loop on amplifier A_{1b}. A positive voltage appears on the anode of D_2; but, if the output voltage swings positive, D_2 reverse biases and D_1 forward biases, keeping the loop closed on A_{1b}. This prevents the amplifier from saturating to the negative rail. The result is an accurate positive rectification of the output signal.

The output of the rectifier is then compared with a reference current set up by the 604kΩ resistor which is biased to −15V. The output of the error amplifier A_2 will drive the FET (Q_1) to the proper voltage necessary to achieve a zero voltage at the inverting input of A_2. If there is insufficient signal, the error amplifier will detect an imbalance. This causes the error amp to drive more positive, turning FET Q_1 on harder, reducing the channel resistance and increasing the gain. Figure 13 shows the pulse response of the AGC amplifier. The AGC loop maintains a constant peak output amplitude for a square wave input signal range of $\pm 20mV_{p-p}$ to $\pm 6.0V_{p-p}$.

LOW PHASE ERROR AMPLIFIER

The simple amplifier depicted in Figure 14 utilizes the monolithic dual OP-260 and a few resistors to substantially reduce phase error over a wide frequency range compared to conventional amplifier

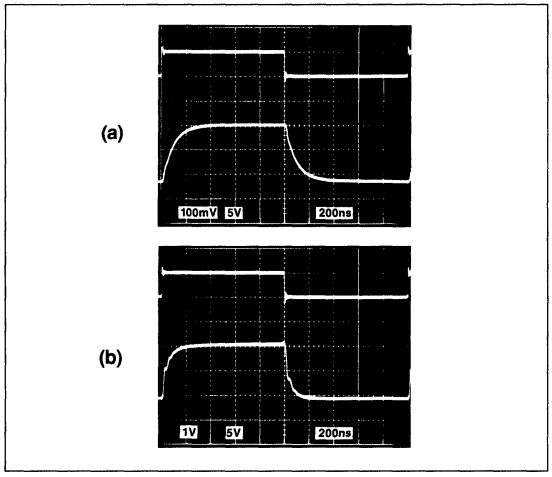


FIGURE 13: *Pulse response of the AGC amplifier at (a) low level input signal, and (b) large input signal.*

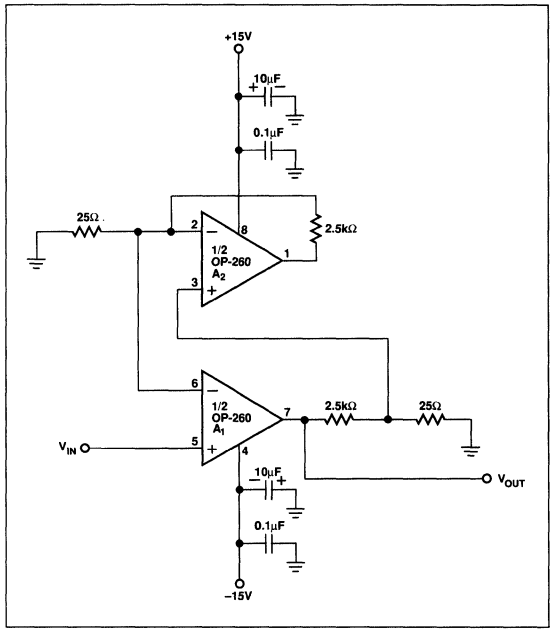


FIGURE 14: *Active feedback allows cancellation of the dominant pole, therefore reducing the phase shift significantly.*

designs. This technique relies on the matched frequency characteristics of the two current feedback amplifiers in the OP-260. Referring to the circuit, notice that each amplifier has the same feedback resistor network, corresponding to a gain of 100. Since these two amplifiers are set at equal gain and are matched due to the monolithic construction of the OP-260, they will have an identical frequency response. A pole in the feedback loop of an amplifier becomes a zero in the closed loop response. With one amplifier in the feedback loop of the other, the pole and zero are at the same frequency, thus cancelling and reducing low phase error. Figure 15 shows that the low phase error amplifier at a gain of 100 exhibits 1° of phase error up to a frequency of 1MHz. For a single voltage feedback op amp to match this performance, it would require a gain-bandwidth product exceeding 10GHz!

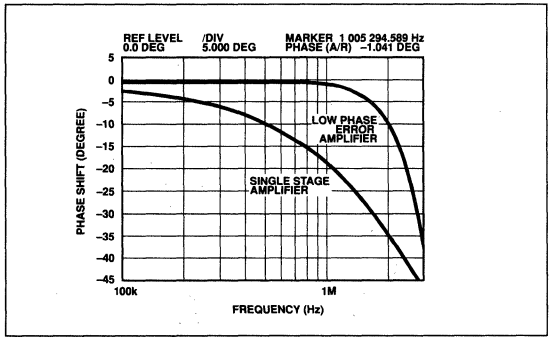


FIGURE 15: *Phase response of the ultra-low phase error amplifier compared to that of a single current feedback amplifier. Note that there is only one degree of phase error over a 1MHz bandwidth at a gain of 100.*

HIGH-SPEED INSTRUMENTATION AMPLIFIER

The circuit of Figure 16 is a high-speed instrumentation amplifier constructed with a single OP-260. Gain of the amplifier is set by resistor R_G according to the following formula:

$$\frac{V_{OUT}}{V_{IN}} = \frac{10k\Omega}{R_G} + 2.$$

The advantages of the two op amp instrumentation amplifier is that the errors in the individual amplifiers tend to cancel one another. Common-mode rejection is limited by the matching of resistors R_1 to R_4. For the best CMR performance, these resistors should be matched to 0.01% or a CMR trim can be performed on R_1. A CMRR of 90dB (measured at 60Hz) is achievable at all gains. Input offset voltage of the instrumentation amplifier is determined by the V_{IOS} matching of the OP-260, which is typically under 0.5mV.

Figure 17 shows the relationship between gain and bandwidth for the instrumentation amplifier. Reducing resistors R_1 to R_4 to 2.5kΩ increases the bandwidth but makes circuit performance more dependent on board layout.

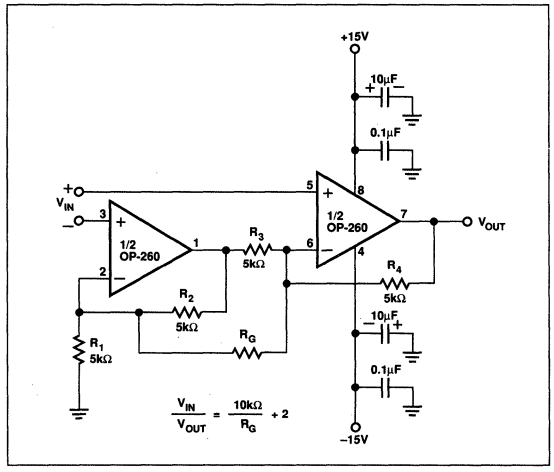


FIGURE 16: *High Speed Instrumentation Amplifier*

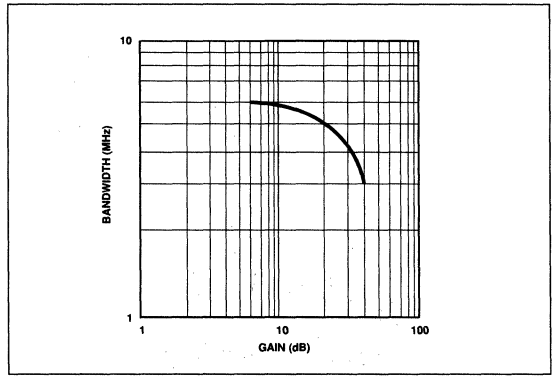


FIGURE 17: *Bandwidth versus gain for the high speed instrumentation amplifier.*

* PSpice is a registered trademark of MicroSim Corporation.
** HSpice is a tradename of Meta-Software, Inc.

OP-260 SPICE MACRO-MODEL

Figure 18 shows the SPICE macro-model for the OP-260 dual, high-speed, current feedback operational amplifier. This model was tested with, and is compatible with PSpice* and HSpice**. The schematic and net-list are included here so that the model can easily be used. This model uses a unique current feedback topology to accurately model both the AC and DC characteristics of the OP-260. In addition, this model can accommodate any number of poles and zeros to further shape the AC response.

This model consists of one of the op amps in the dual OP-260 package. To use this model as a dual, just call up the model twice and specify the same power supplies for each op amp. The OP-260 SPICE macro-model uses four BJT transistors to create the input buffer just as the actual device does. However, the rest of the model contains only ideal linear elements and ideal diodes to model the OP-260's behavior. Using only four transistors reduces simulation time and simplifies model development. It simulates important DC parameters such as V_{OS}, I_B, CMR, V_O and I_{SY}. AC parameters such as slew rate, open-loop transimpedance and phase response and CMR changes with frequency are also simulated by the model. In addition, the model includes the change in input bias current with varying common-mode and power supply voltages. Both output swing and supply current are accurately modelled.

To keep the OP-260 model as simple as possible and thus save computer and development time, not all features of the op amp were modelled as listed below:

- PSR
- Crosstalk
- Varying slew rate with closed-loop gain
- No limits on power supply voltages
- Maximum input voltage range
- Temperature effects (i.e., model parameters are assumed at 25°C)
- Input noise voltage and current sources
- Parameter variations for Monte Carlo analysis (i.e., all parameters are typical only)

These parameters are considered second-order effects and are not considered necessary for circuit simulation under normal operating conditions. However, users can easily add these functions as needed.

2

* PSpice is a registered trademark of MicroSim Corporation.
** HSpice is a tradename of Meta-Software, Inc.

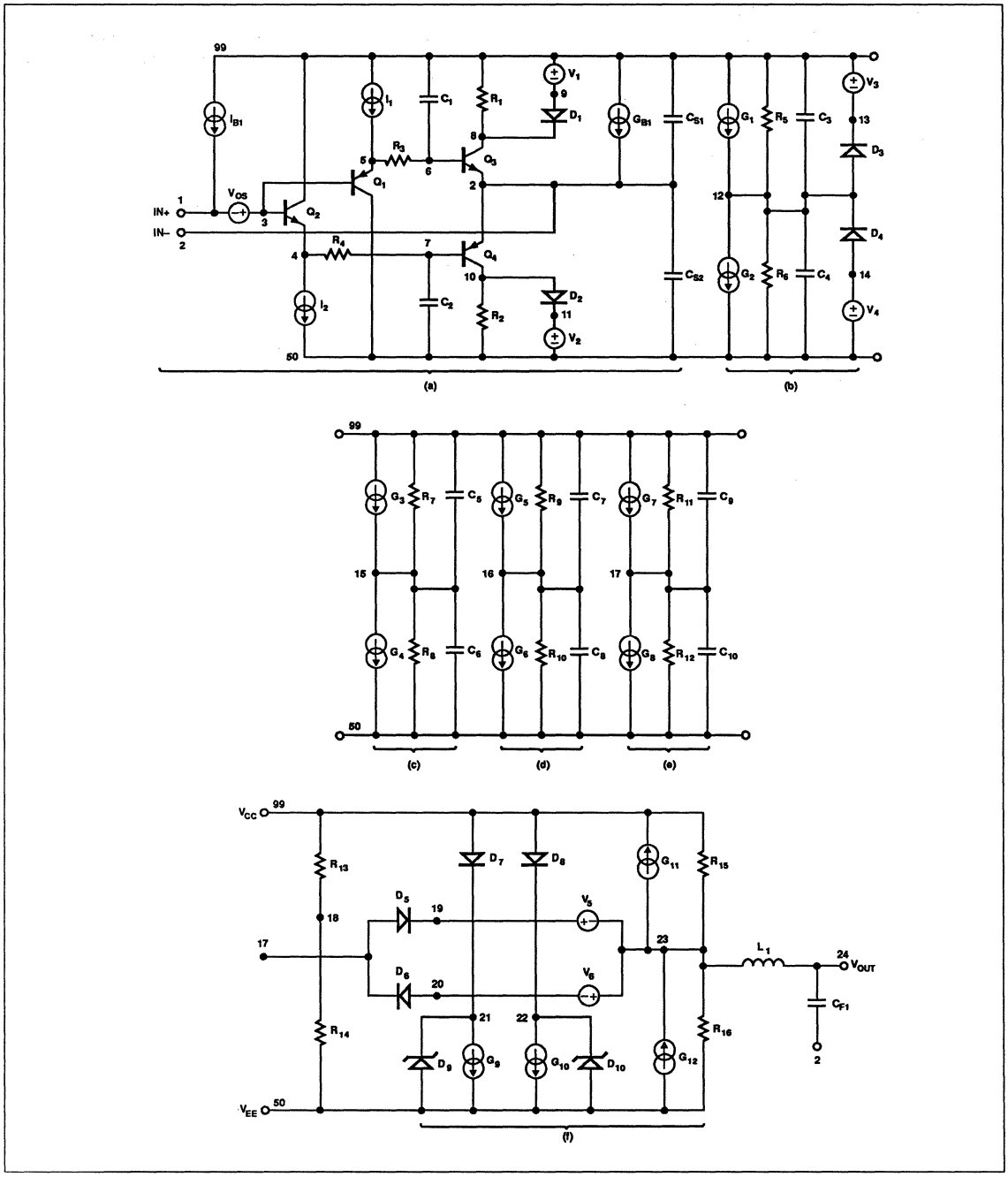


FIGURE 18: *OP-260 Macro-Model Schematic*

```
OP-260 MACRO-MODEL © PMI 1989
*
* SUBCKT OP-260 1  2 24 99 50
*
* INPUT STAGE
*
R1    99  8       4K
R2    10  50      4K
V1    99  9       1.1
D1    9   8       DX
V2    11  50      1.1
D2    10  11      DX
I1    99  5       15OU
I2    4   50      15OU
Q1    50  3   5   QP
Q2    99  3   4   QN
Q3    8   6   2   QN
Q4    10  7   2   QP
R3    5   6       14.3K
R4    4   7       14.3K
C1    99  6       0.133P
C2    50  7       0.133P
*
* INPUT ERROR SOURCES
*
GB1   99  2       POLY(1)  1  18  3E-6  4E-8
IB1   99  1       2E-7
VOS   3   1       1E-3
CS1   99  2       0.8E-12
CS2   50  2       0.8E-12
*
* GAIN STAGE & DOMINANT POLE
*
R5    12  99      10E6
R6    12  50      10E6
C3    12  99      0.6P
C4    12  50      0.6P
G1    99  12      POLY (1)  99  8   4E-3    0.25E-3
G2    12  50      POLY (1)  10  50  4E-3    0.25E-3
V3    99  13      2.2
V4    14  50      2.2
D3    12  13      DX
D4    14  12      DX
*
* POLE AT 64 MHz
*
R7    15  99      1E6
R8    15  50      1E6
C5    15  99      2.5E-15
C6    15  50      2.5E-15
G3    99  15      12  18    1E-6
G4    15  50      18  12    1E-6
*
* POLE AT 72 MHz
*
R9    16  99      1E6
R10   16  50      1E6
C7    16  99      2.2E-15
C8    16  50      2.2E-15
G5    99  16      15  18    1E-6
G6    16  50      18  15    1E-6
*
* POLE  AT 80 MHz
*
R11   17  99      1E6
R12   17  50      1E6
C9    17  99      2E-15
C10   17  50      2E-15
G7    99  17      16  18    1E-6
G8    17  50      18  16    1E-6
*
* OUTPUT STAGE
*
R13   18  99      3.333E3
R14   18  50      3.333E3
R15   23  99      150
R16   23  50      150
L1    23  24      1.5E-8
CF1   24  2       1.8P
G9    21  50      17  23    6.66667E-3
G10   22  50      23  17    6.66667E-3
G11   23  99      99  17    6.66667E-3
G12   50  23      17  50    6.66667E-3
V5    19  23      1.55
V6    23  20      1.55
D5    17  19      DX
D6    20  17      DX
D7    99  21      DX
D8    99  22      DX
D9    50  21      DY
D10   50  22      DY
*
*MODELS USED
*
.MODEL   QN  NPN (BF = 1E9   IS = 1E-15   VAF = 150)
.MODEL   QP  PNP (BF = 1E9   IS = 1E-15   VAF = 150)
.MODEL   DX  D (IS = 1E-15)
.MODEL   DY  D (IS = 1E-15    BV =50)
.ENDS OP-260
```

FIGURE 19: *OP-260 SPICE Net-List*

ANALOG DEVICES

High Speed Dual Operational Amplifier

OP-271

FEATURES

- **Excellent Speed ..... 8.5V/μs Typ**
- **Fast Settling (0.01%) ..... 2μs Typ**
- **Unity-Gain Stable**
- **High Gain-Bandwidth ..... 5MHz Typ**
- **Low Input Offset Voltage ..... 200μV Max**
- **Low Offset Voltage Drift ..... 2μV/°C Max**
- **High Gain ..... 400V/mV Min**
- **Outstanding CMR ..... 106 dB Min**
- **Industry Standard 8-Pin Dual Pinout**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC	PACKAGE LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
200	OP271AZ*	–	OP271ARC/883	MIL
200	OP271EZ	–	–	XND
300	OP271FZ	–	–	XND
400	–	OP271GP	–	XND
400	–	OP271GS††	–	XND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

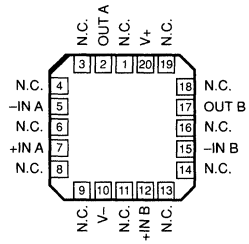
GENERAL DESCRIPTION

The OP-271 is a unity-gain stable monolithic dual op amp featuring excellent speed, 8.5V/μs typical, and fast settling time, 2μs typical to 0.01%. The OP-271 has a gain-bandwidth of 5MHz with a high phase margin of 62°.

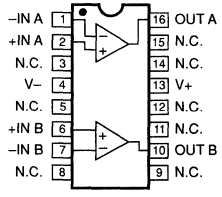
Input offset voltage of the OP-271 is under 200μV with input offset voltage drift below 2μV/°C, guaranteed over the full military temperature range. Open-loop gain exceeds 400,000 into a 10kΩ load ensuring outstanding gain accuracy and linearity. The input bias current is under 20nA limiting errors due to source resistance. The OP-271's outstanding CMR, over 106dB, and low PSRR, under 5.6μV/V, reduce errors caused by ground noise and power supply fluctuations. In addition, the OP-271 exhibits high CMR and PSRR over a wide frequency range, further improving system accuracy.

Continued

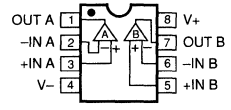
PIN CONNECTIONS



LCC
(RC-Suffix)



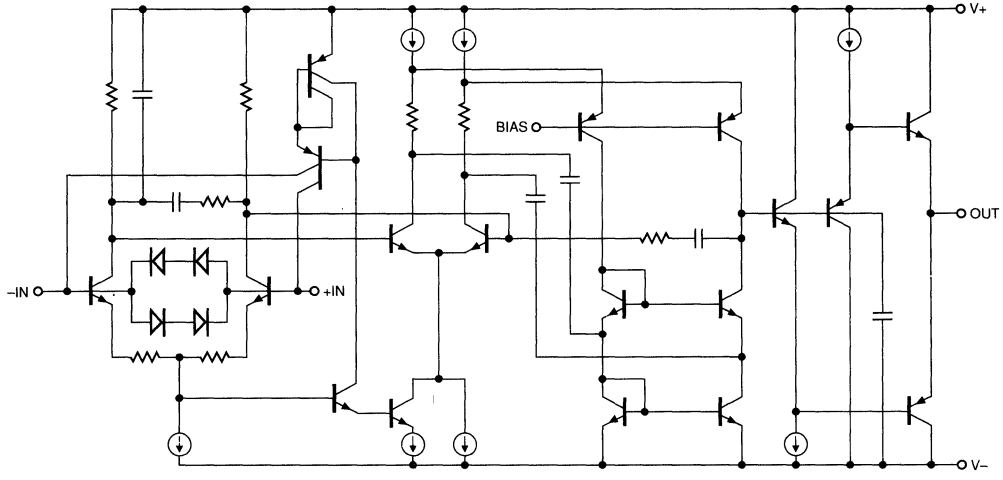
16-PIN SOL
(S-Suffix)



EPOXY MINI-DIP
(P-Suffix)

8-PIN HERMETIC DIP
(Z-Suffix)

SIMPLIFIED SCHEMATIC (One of the two amplifiers is shown.)



The OP-271 offers outstanding DC and AC matching between channels. This is especially valuable for applications such as multiple gain blocks, high-speed instrumentation and amplifiers, buffers and active filters.

The OP-271 conforms to the industry standard 8-pin dual op amp pinout. It is pin compatible with the TL072, TL082, LF412, and 1458/1558 dual op amps and can be used to significantly improve systems using these devices.

For applications requiring lower voltage noise, see the OP-270. For a quad version of the OP-271, see the OP-471.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage (Note 2) ..... ±1.0V
Differential Input Current (Note 2) ..... ±25mA
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature (T_j) ..... –65°C to +150C
Operating Temperature Range
OP-271A ..... –55°C to +125°C
OP-271E, OP-271F, OP-271G ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
8-Pin SO (S)	92	27	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. The OP-271's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±1.0V, the input current should be limited to ±25mA.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

			OP-271A/E			OP-271F			OP-271G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		–	75	200	–	150	300	–	200	400	µV
Input Offset Current	I_{OS}	V_{CM} = 0V	–	1	10	–	4	15	–	7	20	nA
Input Bias Current	I_B	V_{CM} = 0V	–	4	20	–	6	40	–	12	60	nA
Input Noise Voltage Density	e_n	f_O = 1kHz	–	7.6	–	–	7.6	–	–	7.6	–	nV/ Hz
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 10kΩ	400	650	–	300	500	–	250	400	–	V/mV
		R_L = 2kΩ	300	500	–	200	300	–	175	250	–	
Input Voltage Range	IVR	(Note 1)	±12	±12.5	–	±12	±12.5	–	±12	±12.5	–	V
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12	±13	–	±12	±13	–	±12	±13	–	V
Common-Mode Rejection	CMR	V_{CM} = ±12V	106	120	–	100	115	–	90	105	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	–	0.6	3.2	–	1.8	5.6	–	2.4	7.0	µV/V
Slew Rate	SR		5.5	8.5	–	5.5	8.5	–	5.5	8.5	–	V/µs
Phase Margin	$ø_m$	A_V = +1	–	62	–	–	62	–	–	62	–	deg
Supply Current (All Amplifiers)	I_{SY}	No Load	–	4.5	6.5	–	4.5	6.5	–	4.5	6.5	mA
Gain Bandwidth Product	GBW		–	5	–	–	5	–	–	5	–	MHz
Channel Separation	CS	V_O = 20V_{p-p} f_O = 10Hz (Note 2)	125	175	–	125	175	–	–	175	–	dB
Input Capacitance	C_{IN}		–	3	–	–	3	–	–	3	–	pF
Input Resistance Differential-Mode	R_{IN}		–	0.4	–	–	0.4	–	–	0.4	–	MΩ
Input Resistance Common-Mode	R_{INCM}		–	20	–	–	20	–	–	20	–	GΩ
Settling Time	t_s	A_V = +1, 10V Step to 0.01%	–	2	–	–	2	–	–	2	–	µs

NOTES:
1. Guaranteed by CMR test.
2. Guaranteed but not 100% tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$ for OP-271A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-271A MIN	OP-271A TYP	OP-271A MAX	UNITS
Input Offset Voltage	V_{OS}		—	115	400	μV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.4	2	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	1.5	30	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	7	60	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 300 200	 600 500	 — —	V/mV
Input Voltage Range	IVR	(Note 1)	±12	±12.5	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 12V$	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	1.0	5.6	μV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	—	5.3	7.5	mA

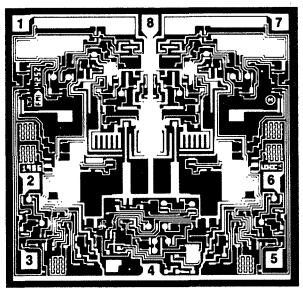
NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-40°C \leq T_A \leq +85°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-271A/E MIN	OP-271A/E TYP	OP-271A/E MAX	OP-271F MIN	OP-271F TYP	OP-271F MAX	OP-271G MIN	OP-271G TYP	OP-271G MAX	UNITS
Input Offset Voltage	V_{OS}		–	100	330	–	215	560	–	300	700	μV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.4	2	–	1	4	–	2.0	5	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	–	1	30	–	5	40	–	15	50	nA
Input Bias Current	I_B	$V_{CM} = 0V$	–	6	60	–	10	70	–	15	80	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 300 200	 600 500	 – –	 200 100	 500 400	 – –	 150 90	 400 300	 – –	V/mV
Input Voltage Range	IVR	(Note 1)	±12	±12.5	–	±12	±12.5	–	±12	±12.5	–	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	–	±12	±13	–	±12	±13	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 12V$	100	120	–	94	115	–	90	100	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	–	0.7	5.6	–	51.8	10	–	2.0	15	μV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	–	5.2	7.2	–	5.2	7.2	–	5.2	7.2	mA

NOTE:
1. Guaranteed by CMR test.

DICE CHARACTERISTICS



1. OUT A
2. −IN A
3. +IN A
4. V−
5. +IN B
6. −IN B
7. OUT B
8. V+

DIE SIZE 0.094 × 0.092 inch, 8,648 sq. mils (2.39 × 2.34 mm, 5.60 sq. mm)

For additional DICE ordering information, refer to PMI's Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

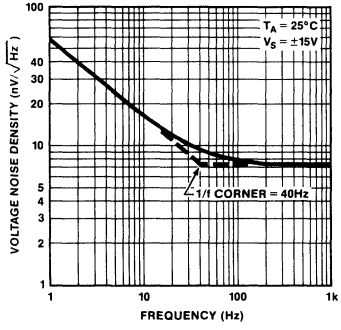
PARAMETER	SYMBOL	CONDITIONS	OP-271GBC LIMIT	UNITS
Input Offset Voltage	V_{OS}		300	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	15	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	40	nA MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 300 200	 V/mV MIN
Input Voltage Range	IVR	(Note 1)	±12	V MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 12V$	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	5.6	μV/V MAX
Supply Current (All Amplifiers)	I_{SY}	No Load	6.5	mA MAX

NOTES:
1. Guaranteed by CMR test.

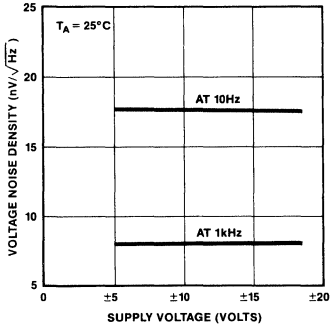
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

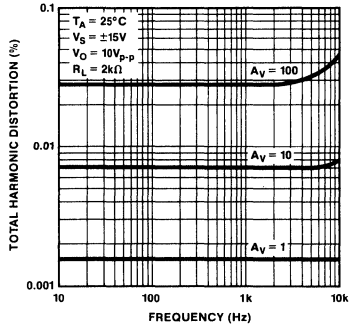
VOLTAGE NOISE DENSITY vs FREQUENCY



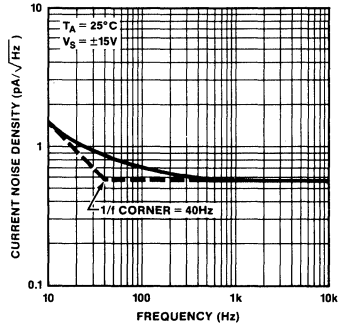
VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE



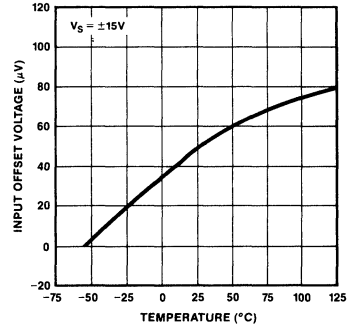
TOTAL HARMONIC DISTORTION vs FREQUENCY



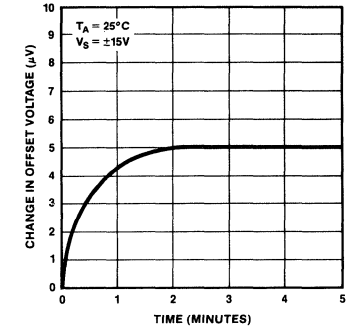
CURRENT NOISE DENSITY vs FREQUENCY



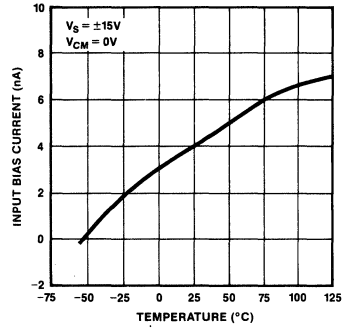
INPUT OFFSET VOLTAGE vs TEMPERATURE



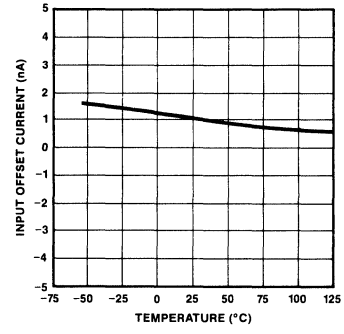
WARM-UP OFFSET VOLTAGE DRIFT



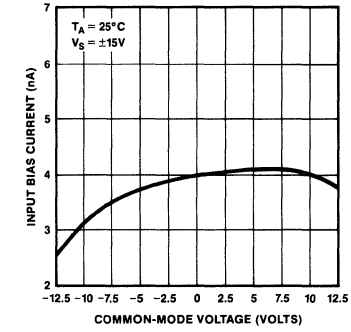
INPUT BIAS CURRENT vs TEMPERATURE



INPUT OFFSET CURRENT vs TEMPERATURE

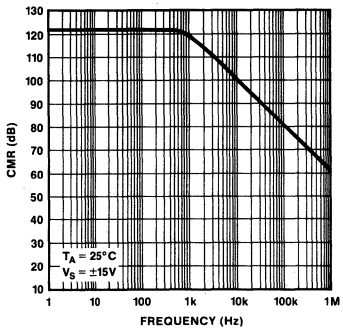


INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

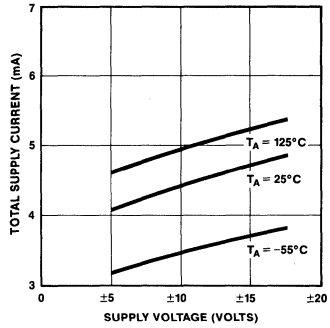


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

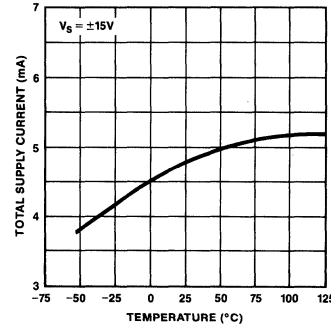
CMR vs FREQUENCY



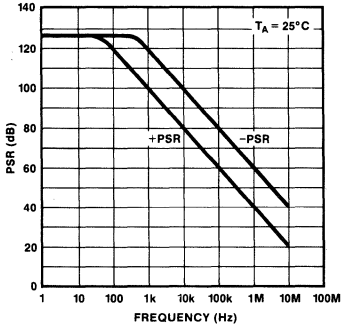
TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE



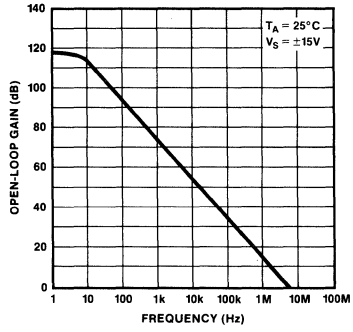
TOTAL SUPPLY CURRENT vs TEMPERATURE



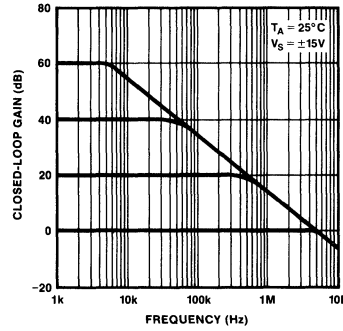
PSR vs FREQUENCY



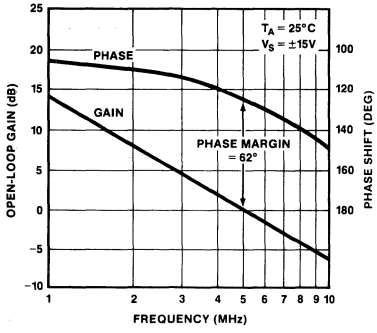
OPEN-LOOP GAIN vs FREQUENCY



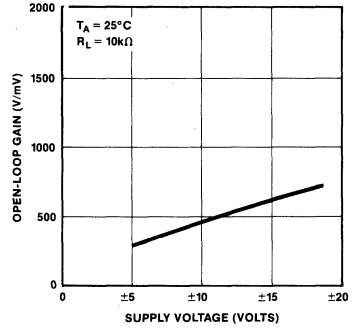
CLOSED-LOOP GAIN vs FREQUENCY



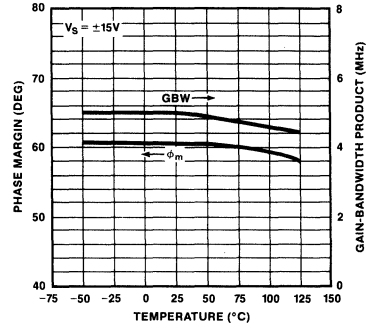
OPEN-LOOP GAIN, PHASE SHIFT vs FREQUENCY



OPEN-LOOP GAIN vs SUPPLY VOLTAGE

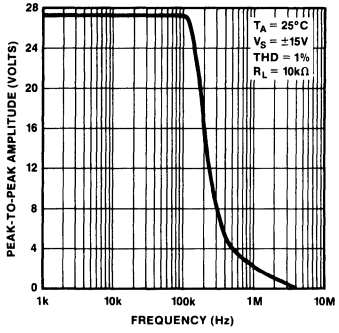


GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE

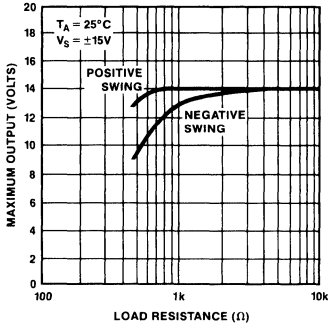


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

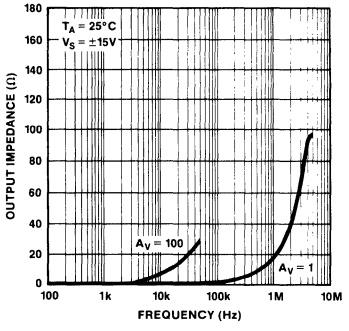
MAXIMUM OUTPUT SWING vs FREQUENCY



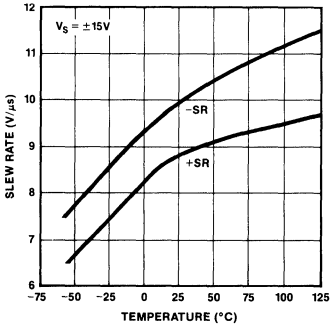
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



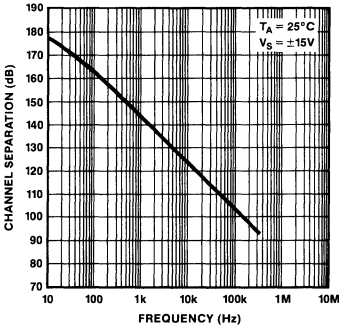
OUTPUT IMPEDANCE vs FREQUENCY



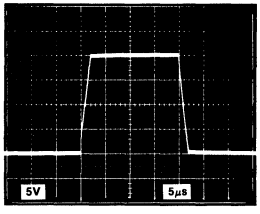
SLEW RATE vs TEMPERATURE



CHANNEL SEPERATION vs FREQUENCY

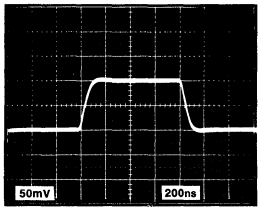


LARGE-SIGNAL TRANSIENT RESPONSE



T_A = 25°C
V_S = ±15V
A_V = +1

SMALL-SIGNAL TRANSIENT RESPONSE



T_A = 25°C
V_S = ±15V
A_V = +1

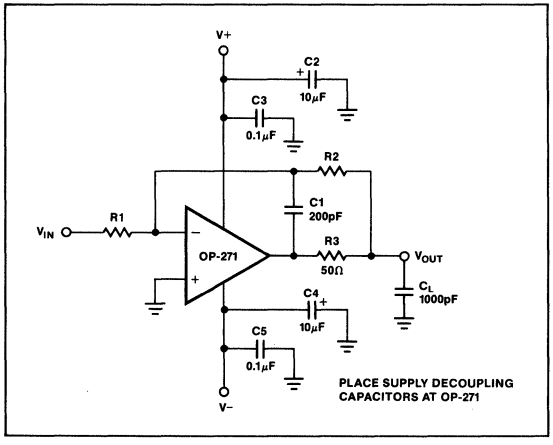
APPLICATIONS INFORMATION

CAPACITIVE LOAD DRIVING AND POWER SUPPLY CONSIDERATIONS

The OP-271 is unity-gain stable and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply bypassing is highly recommended. Proper supply bypassing reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP-271.

In the standard feedback amplifier, the op amp's output resistance combines with the load capacitance to form a low-pass filter that adds phase shift in the feedback network and reduces stability. A simple circuit to eliminate this effect is shown in Figure 1. The added components, C1 and R3, decouple the amplifier from the load capacitance and provide additional stability. The values of C1 and R3 shown in Figure 8 are for a load capacitance of up to 1000pF when used with the OP-271.

FIGURE 1: Driving Large Capacitive Loads

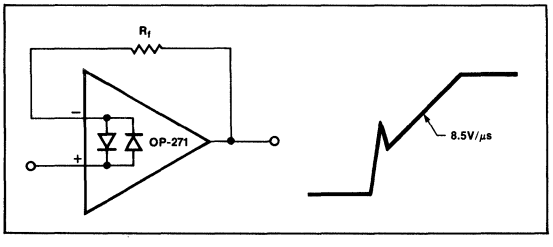


UNITY-GAIN BUFFER APPLICATIONS

When $R_f \leq 100\Omega$ and the input is driven with a fast, large-signal pulse (>1V), the output waveform will look as shown in Figure 2.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at 10V); the amplifier will stay in its active mode and a smooth transition will occur.

FIGURE 2: Pulsed Operation



When $R_f > 3k\Omega$, a pole created by R_f and the amplifier's input capacitance (3pF) creates additional phase shift and reduces phase margin. A small capacitor in parallel with R_f helps eliminate this problem.

COMPUTER SIMULATIONS

Many electronic design and analysis programs include models for op amps which calculate AC performance from the location of poles and zeros. As an aid to designers utilizing such a program, major poles and zeros of the OP-271 are listed below. Their location will vary slightly between production lots. Typically, they will be within ±15% of the frequency listed. Use of this data will enable the designer to evaluate gross circuit performance quickly, but should not supplant rigorous characterization of a breadboarded circuit.

POLES	ZEROS
15 Hz	2.5 MHz
1.2 MHz	4 × 23 MHz
2 × 32 MHz	—
8 × 40 MHz	—

APPLICATIONS

LOW PHASE ERROR AMPLIFIER

The simple amplifier depicted in Figure 3 utilizes a monolithic dual operational amplifier and a few resistors to substantially reduce phase error compared to conventional amplifier designs. At a given gain, the frequency range for a specified phase accuracy is over a decade greater than for a standard single op amp amplifier.

The low phase error amplifier performs second-order frequency compensation through the response of op amp A2 in the feedback loop of A1. Both op amps must be extremely well matched in frequency response. At low frequencies, the A1 feedback loop forces $V_2/(K1 + 1) = V_{IN}$. The A2 feedback loop forces $V_O/(K1 + 1) = V_2/(K1 + 1)$ yielding an overall transfer function of $V_O/V_{IN} = K1 + 1$. The DC gain is determined by the resistor divider at the output, V_O, and is not directly affected by the resistor divider around A2. Note that, like a conventional single op amp amplifier, the DC gain is set by resistor ratios only. Minimum gain for the low phase error amplifier is 10.

FIGURE 3: Low Phase Error Amplifier

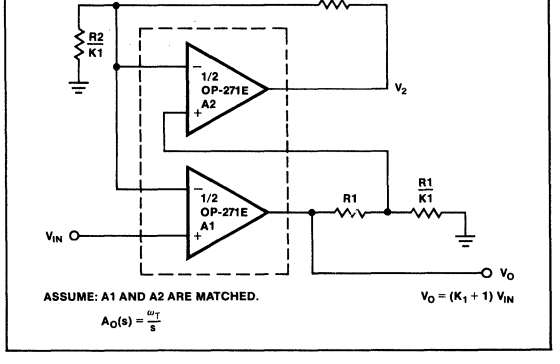


FIGURE 4: Phase Error Comparison

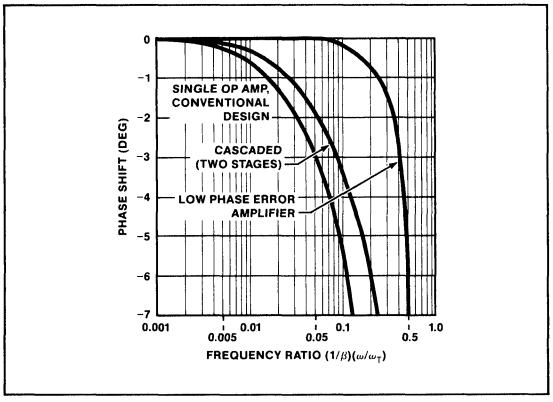


Figure 4 compares the phase error performance of the low phase error amplifier with a conventional single op amp amplifier and a cascaded two-stage amplifier. The low phase error amplifier shows a much lower phase error, particularly for frequencies where $\omega/\beta\omega_T < 0.1$. For example, phase error of $-0.1°$ occurs at $0.002\ \omega/\beta\omega_T$ for the single op amp amplifier, but at $0.11\ \omega/\beta\omega_T$ for the low phase error amplifier.

For more detailed information on the low phase error amplifier, see Application Note AN-107.

DUAL 12-BIT VOLTAGE OUTPUT DAC

The dual voltage output DAC shown in Figure 5 will settle to 12-bit accuracy from zero to full scale in $2\mu s$ typically. The CMOS DAC-8222 utilizes a 12-bit, double-buffered input structure allowing faster digital throughput and minimizing digital feedthrough.

FAST CURRENT PUMP

Maximum output current of the fast current pump shown in Figure 6 is ± 11mA. Voltage compliance exceeds ± 10V with ± 15V supplies. The current pump has an output resistance of over $3M\Omega$ and maintains 12-bit linearity over its entire output range.

FIGURE 6: Fast Current Pump

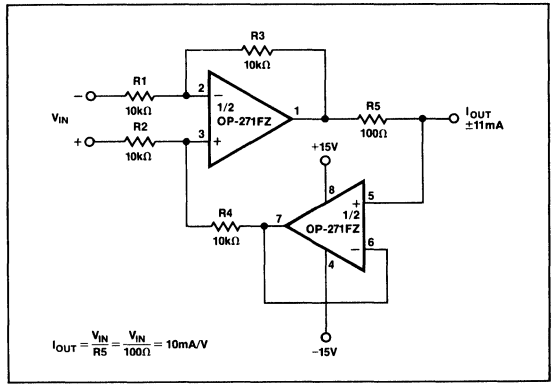
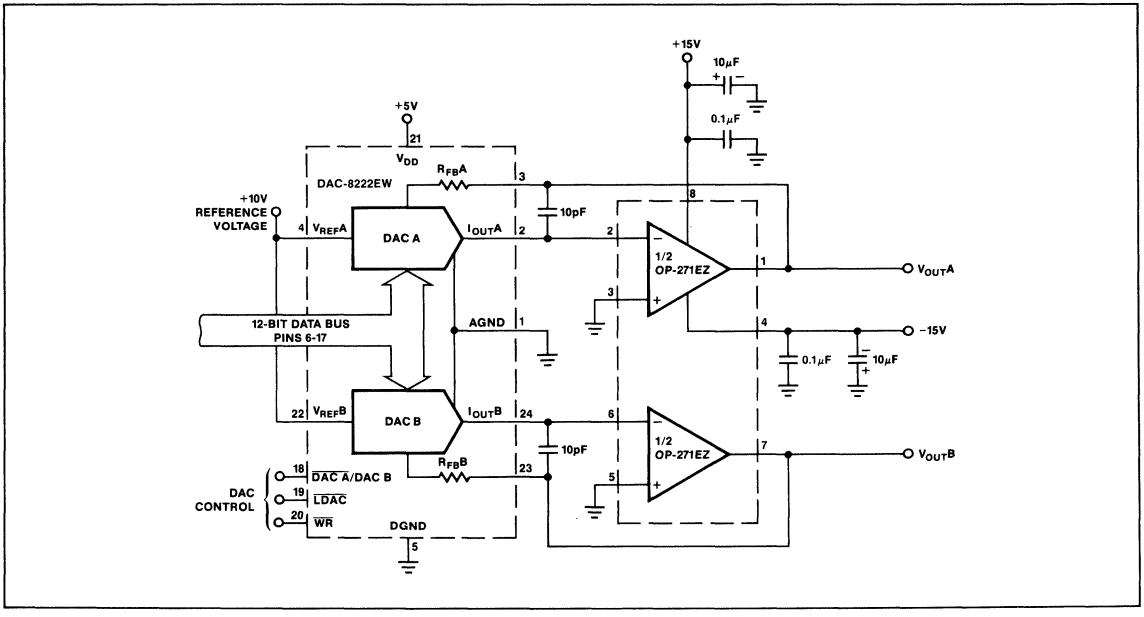


FIGURE 5: Dual 12-Bit Voltage Output DAC



Dual Bipolar/JFET, Low Distortion Operational Amplifier

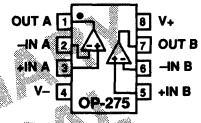
OP-275*

FEATURES
"Sounds Good"
Low Noise: 5 nV/√Hz
Low Distortion: 0.0006%
High Slew Rate: 20 V/μs
Wide Bandwidth: 8 MHz
Low Supply Current: 2 mA/Amplifier
Low Offset Voltage: 1 mV
Low Offset Current: 2 nA
Unity Gain Stable

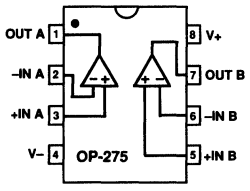
APPLICATIONS
High Performance Audio
Active Filters
Fast Amplifiers
Integrators

PIN CONNECTIONS

8-Lead Narrow Body SOIC (S Suffix)



8-Lead Epoxy DIP (P Suffix)



GENERAL DESCRIPTION

The OP-275 is the first amplifier to feature the Butler Amplifier front-end. This new front-end design combines the accuracy and low noise performance of bipolar transistors with the speed and sound quality of JFETs. This yields better THD and noise performance than previous audio amplifiers, at much lower supply currents.

Bias and offset currents are also greatly reduced over bipolar designs.

The OP-275 is specified over the extended industrial and military temperature ranges. OP-275s are available in plastic and ceramic DIP plus SOIC 8-pin surface mount packages.

ORDERING GUIDE

Model	Temperature Range	Package Option
OP275AZ/883	−55°C to +125°C	14-Pin Cerdip
OP275ARC/883	−55°C to +125°C	20-Contact LCC
OP275GP	−40°C to +85°C	8-Pin Plastic DIP
OP275GS	−40°C to +85°C	8-Pin SOIC
OP275GBC	+25°C	DICE

*Patent pending.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Input Voltage[2] . . . . . ± 18 V
Differential Input Voltage[2] . . . . . 36 V
Output Short-Circuit Duration . . . . . Limited
Storage Temperature Range
  Y, Z, RC Package . . . . . −65°C to +175°C
  P, S Package . . . . . −65°C to +150°C
Operating Temperature Range
  OP-275A . . . . . −55°C to +125°C
  OP-275G . . . . . −40°C to +85°C
Junction Temperature Range
  Y, Z, RC Package . . . . . −65°C to +150°C
  P, S Package . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Cerdip (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W
20-Contact LCC (RC)	NA	NA	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

OP-275—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1		mV
Input Bias Current	I_B	V_{CM} = 0 V		150		nA
Input Offset Current	I_{OS}	V_{CM} = 0 V		2		nA
Input Voltage Range	V_{CM}		−11		+11	V
Common-Mode Rejection	CMR	V_{CM} = ±11 V	86			dB
Large Signal Voltage Gain	A_{VO}	R_L = 600 Ω		200		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			5		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 10 kΩ	−13		13	V
		R_L = 600 Ω, V_S = ±18 V		±17		V
Open Loop Output Resistance	R_{OUT}					Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ± 9 V to ±15 V		80		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V, R_L = ∞		2		mA
Supply Voltage Range	V_S		±4.5		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		20		V/µs
Full-Power Bandwidth	BW_P					kHz
Settling Time	t_S					µs
Gain Bandwidth Product	GBP			8		MHz
Total Harmonic Distortion	THD	@ 20 kHz		0.002		%
		@ 1 kHz		0.0006		%
Phase Margin	∅o			62		degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p–p					µV p–p
Voltage Noise Density	e_n	f = 30 Hz, V_S = ±18 V, V_{IN} = 10 V rms		8		nV/√Hz
Voltage Noise Density	e_n	f = 1 kHz, V_S = ±18 V, V_{IN} = 10 V rms		5		nV/√Hz
Current Noise Density	i_n	f = 30 Hz				pA/√Hz
Current Noise Density	i_n	f = 1 kHz				pA/√Hz
Overshoot Factor		V_{IN} = 100 mV, A_{VD} = 1, R_L = 600 Ω, C_L = 100 pF		10		%

WAFER TEST LIMITS (@ V_S=±15.0 V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}			mV max
Input Bias Current	I_B	V_{CM} = 0 V		nA max
Input Offset Current	I_{OS}	V_{CM} = 0 V		nA max
Input Voltage Range[1]				V min
Common-Mode Rejection	CMRR	V_{CM} = ± 11 V		dB min
Power Supply Rejection Ratio	PSRR	V = ±9 V to ±15 V		µV/V
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ		V/mV min
Output Voltage Range	V_O	R_L = 10 kΩ		V min
Supply Current/Amplifier	I_{SY}	V_O = 0 V, R_L = ∞		mA max

NOTES

Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

[1]Guaranteed by CMR test.

Specifications subject to change without notice.

High Speed Low Noise Quad Operational Amplifier

OP-471

FEATURES

- **Excellent Speed** ..... **8V/μs Typ**
- **Low Noise** ..... **11nV/√Hz @ 1kHz Max**
- **Unity-Gain Stable**
- **High Gain-Bandwidth** ..... **6.5MHz Typ**
- **Low Input Offset Voltage** ..... **0.8mV Max**
- **Low Offset Voltage Drift** ..... **4μV/° C Max**
- **High Gain** ..... **500V/mV Min**
- **Outstanding CMR** ..... **105 dB Min**
- **Industry Standard Quad Pinouts**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE			OPERATING TEMPERATURE RANGE
	CERDIP	PLASTIC	LCC*	
800	OP471AY*	–	OP471ATC/883	MIL
800	–	–	OP471ARC/883	MIL
800	OP471EY	–	–	IND
1500	OP471FY	–	–	IND
1800	–	OP471GP	–	XIND
1800	–	OP471GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

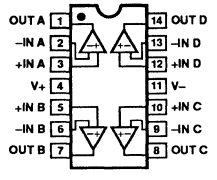
GENERAL DESCRIPTION

The OP-471 is a monolithic quad op amp featuring low noise, 11nV/√Hz Max @ 1kHz, excellent speed, 8V/μs typical, a gain-bandwidth of 6.5MHz, and unity-gain stability.

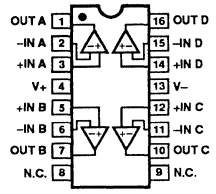
The OP-471 has an input offset voltage under 0.8mV and an input offset voltage drift below 4μV/°C, guaranteed over the full military temperature range. Open loop gain of the OP-471 is over 500,000 into a 10kΩ load insuring outstanding gain accuracy and linearity. The input bias current is under 25nA

2

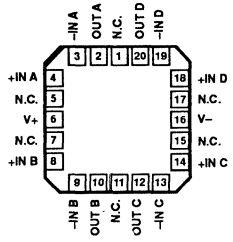
PIN CONNECTIONS



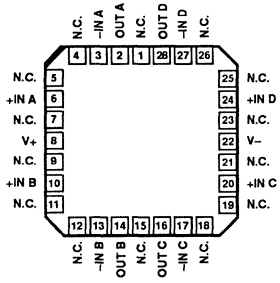
14-PIN HERMETIC DIP (Y-Suffix)
14-PIN PLASTIC DIP (P-Suffix)



16-PIN SOL (S-Suffix)

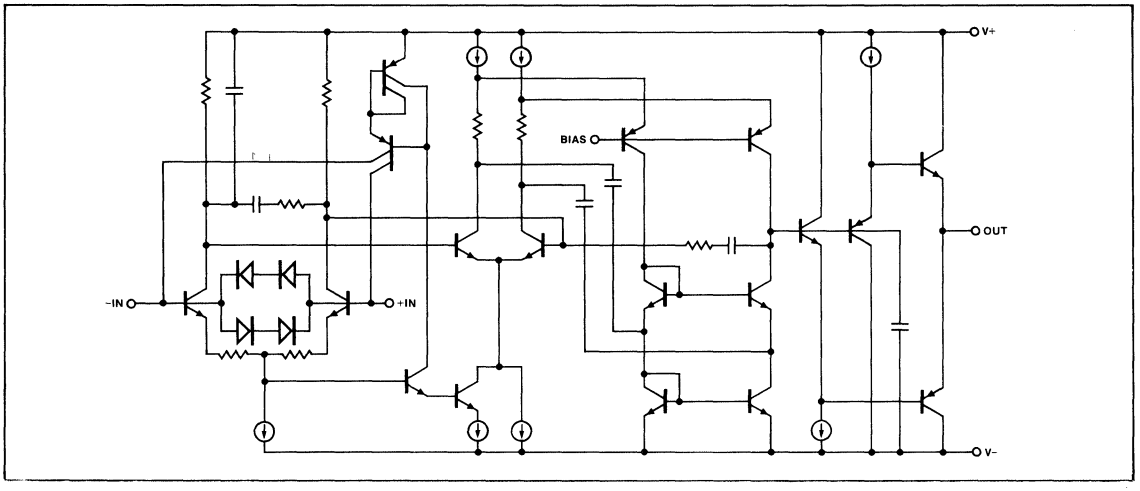


20-LEAD LCC (RC-Suffix)



28-LEAD LCC (TC-Suffix)

SIMPLIFIED SCHEMATIC (One of four amplifiers is shown.)



limiting errors due to signal source resistance. The OP-471's CMR of over 105dB and PSRR of under 5.6μV/V significantly reduce errors caused by ground noise and power supply fluctuations.

The OP-471 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low-noise instrumentation amplifiers, quad buffers and low-noise active filters.

The OP-471 conforms to the industry standard 14-pin DIP pinout. It is pin compatible with the OP-11, LM148/149, HA4741, RM4156, MC33074, TL084 and TL074 quad op amps and can be used to upgrade systems using these devices.

For applications requiring even lower voltage noise the OP-470, with a voltage density of $5nV/\sqrt{Hz}$ Max @ 1kHz, is recommended.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage (Note 3) ..... ±1.0V
Differential Input Current (Note 3) ..... ±25mW
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P, RC, TC, Y-Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_j) ..... –65°C to +150°C
Operating Temperature Range
OP-471A ..... –55°C to +125°C
OP-471E, OP-471F ..... –25°C to +85°C
OP-471G ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
20-Contact LCC (RC)	78	30	°C/W
28-Contact LCC (TC)	70	28	°C/W
16-Pin SOL (S)	88	23	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.
3. The OP-471's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±1.0V, the input current should be limited to ±25mA.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

			OP-471A/E			OP-471F			OP-471G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.25	0.8	—	0.5	1.5	—	1.0	1.8	mV
Input Offset Current	I_{OS}	V_{CM} = 0V	—	4	10	—	7	20	—	12	30	nA
Input Bias Current	I_B	V_{CM} = 0V	—	7	25	—	15	50	—	25	60	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 1)	—	250	500	—	250	500	—	250	500	nV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz	—	9	16	—	9	16	—	9	16	$nV/\sqrt{Hz}$
		f_O = 100Hz	—	7	12	—	7	12	—	7	12	
		f_O = 1kHz (Note 2)	—	6.5	11	—	6.5	11	—	6.5	11	
Input Noise Current Density	i_n	f_O = 10Hz	—	1.7	—	—	1.7	—	—	1.7	—	$pA/\sqrt{Hz}$
		f_O = 100Hz	—	0.7	—	—	0.7	—	—	0.7	—	
		f_O = 1kHz	—	0.4	—	—	0.4	—	—	0.4	—	
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V										
		R_L = 10kΩ	500	700	—	300	500	—	300	500	—	V/mV
		R_L = 2kΩ	350	550	—	175	275	—	175	275	—	
Input Voltage Range	IVR	(Note 3)	±11	±12	—	±11	±12	—	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	105	120	—	95	115	—	95	115	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	—	1	5.6	—	5.6	17.8	—	5.6	17.8	μV/V
Slew Rate	SR		6.5	8	—	6.5	8	—	6.5	8	—	V/μs

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-471A/E MIN	OP-471A/E TYP	OP-471A/E MAX	OP-471F MIN	OP-471F TYP	OP-471F MAX	OP-471G MIN	OP-471G TYP	OP-471G MAX	UNITS
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.2	11	—	9.2	11	—	9.2	11	mA
Gain-Bandwidth Product	GBW	$A_V = +10$	—	6.5	—	—	6.5	—	—	6.5	—	MHz
Channel Separation	CS	$V_O = 20V_{p-p}$ $f_O = 10Hz$ (Note 1)	125	150	—	125	150	—	125	150	—	dB
Input Capacitance	C_{IN}		—	2.6	—	—	2.6	—	—	2.6	—	pF
Input Resistance Differential-Mode	R_{IN}		—	1.1	—	—	1.1	—	—	1.1	—	MΩ
Input Resistance Common-Mode	R_{INCM}		—	11	—	—	11	—	—	11	—	GΩ
Settling Time	t_s	$A_V = +1$ to 0.1% to 0.01%	— —	4.5 7.5	— —	— —	4.5 7.5	— —	— —	4.5 7.5	— —	μs

NOTES:
1. Guaranteed but not 100% tested.
2. Sample tested.
3. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$ for OP-471A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-471A MIN	OP-471A TYP	OP-471A MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.4	1.2	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	1	4	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	6	20	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	16	50	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 375 250	 500 350	 — —	V/mV
Input Voltage Range	IVR	(Note 1)	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	115	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	5.6	10	μV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.3	11	mA

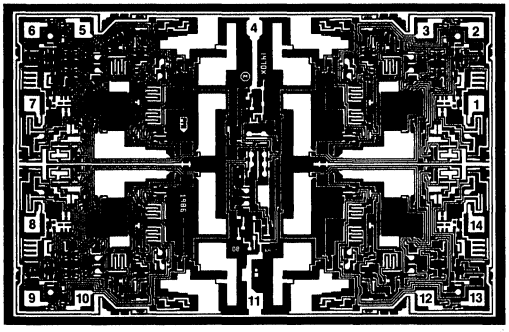
NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25°C \le T_A \le +85°C$ for OP-471E/F, $-40°C \le T_A \le +85°C$ for OP-471G, unless otherwise noted.

			OP-471E			OP-471F			OP-471G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}		—	0.3	1.1	—	0.6	2.0	—	1.2	2.5	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	1	4	—	2	7	—	4	—	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	5	20	—	8	40	—	20	50	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	13	50	—	25	70	—	40	75	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$										
		$R_L = 10k\Omega$	375	600	—	200	400	—	200	400	—	V/mV
		$R_L = 2k\Omega$	250	400	—	125	200	—	125	200	—	
Input Voltage Range	IVR	(Note 1)	±11	±12	—	±11	±12	—	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	115	—	90	110	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	3.2	10	—	18	31.6	—	18	31.6	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.3	11	—	9.3	11	—	9.3	11	mA

NOTE:
1. Guaranteed by CMR test.

DICE CHARACTERISTICS



1. OUT A
2. −IN A
3. +IN A
4. V+
5. +IN B
6. −IN B
7. OUT B
8. OUT C
9. −IN C
10. +IN C
11. V−
12. +IN D
13. −IN D
14. OUT D

DIE SIZE 0.163 × 0.106 inch, 17,278 sq. mils
(4.14 × 2.69 mm, 11.14 sq. mm)

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

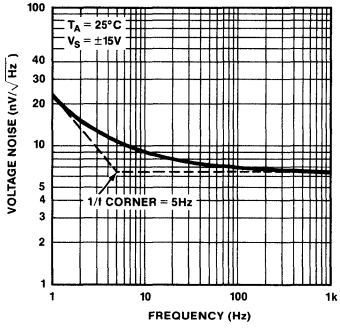
PARAMETER	SYMBOL	CONDITIONS	OP-471GBC LIMIT	UNITS
Input Offset Voltage	V_{OS}		1.5	mV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	20	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	50	nA MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 300 175	 V/mV MIN
Input Voltage Range	IVR	Note 1	±11	V MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	95	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	17.8	μV/V MAX
Slew Rate	SR		6.5	V/μs MIN
Supply Current (All Amplifiers)	I_{SY}	No Load	11	mA MAX

NOTES:
1. Guaranteed by CMR test.

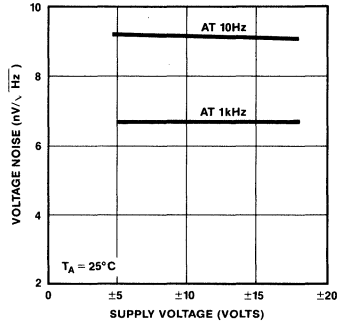
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

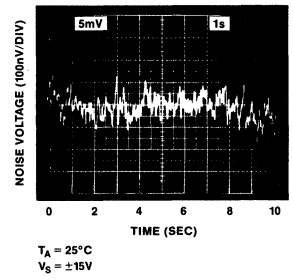
VOLTAGE NOISE DENSITY vs FREQUENCY



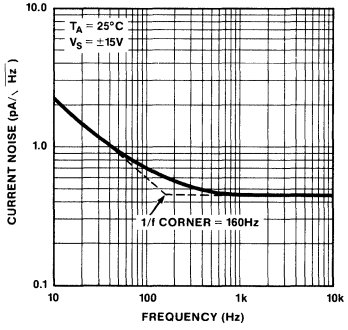
VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE



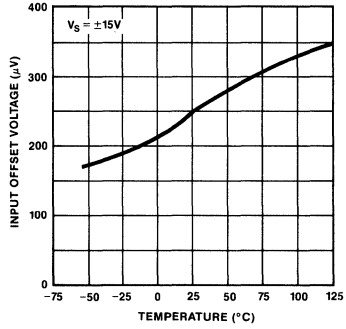
0.1Hz TO 10Hz NOISE



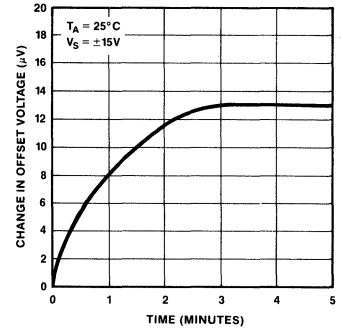
CURRENT NOISE DENSITY vs FREQUENCY



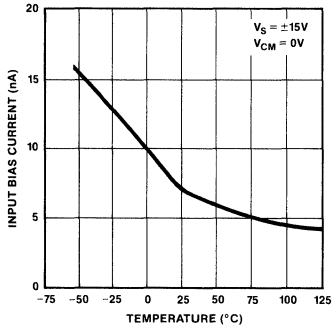
INPUT OFFSET VOLTAGE vs TEMPERATURE



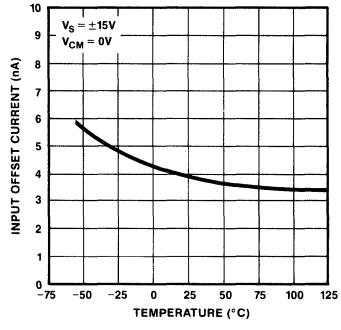
WARM-UP OFFSET VOLTAGE DRIFT



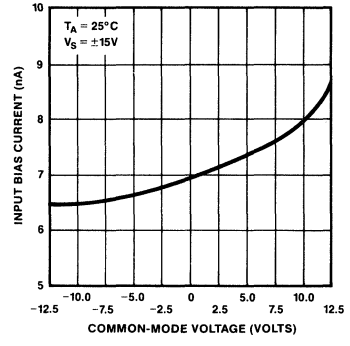
INPUT BIAS CURRENT vs TEMPERATURE



INPUT OFFSET CURRENT vs TEMPERATURE

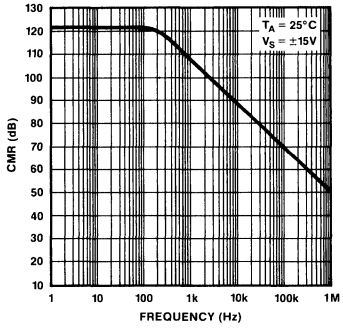


INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

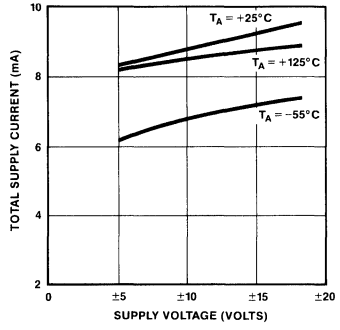


TYPICAL PERFORMANCE CHARACTERISTICS

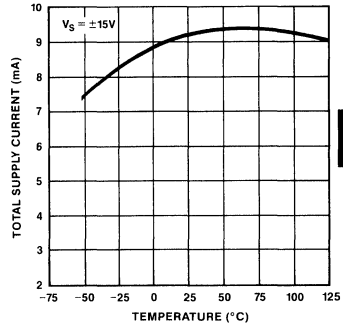
CMR vs FREQUENCY



TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE

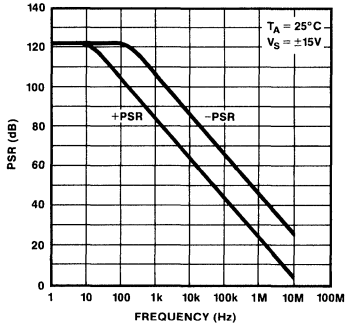


TOTAL SUPPLY CURRENT vs TEMPERATURE

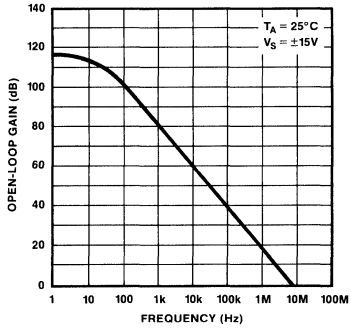


2

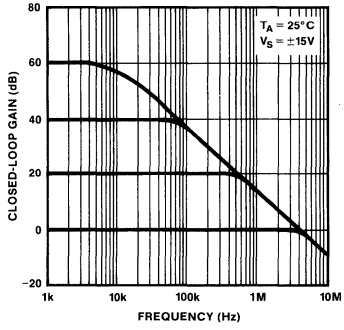
PSR vs FREQUENCY



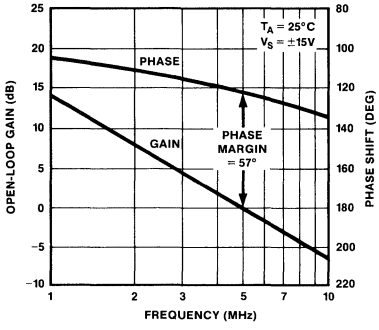
OPEN-LOOP GAIN vs FREQUENCY



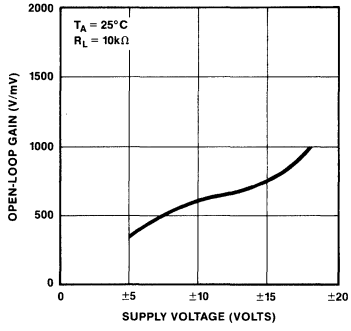
CLOSED-LOOP GAIN vs FREQUENCY



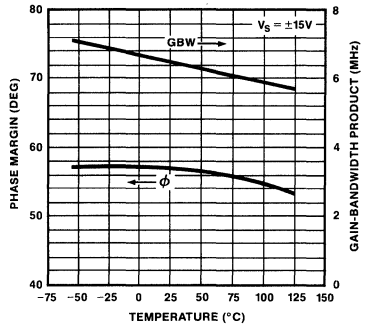
OPEN-LOOP GAIN, PHASE SHIFT vs FREQUENCY



OPEN-LOOP GAIN vs SUPPLY VOLTAGE

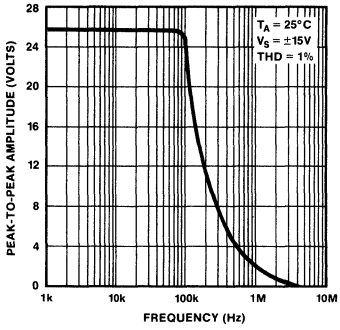


GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE

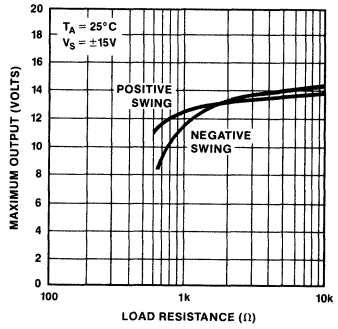


TYPICAL PERFORMANCE CHARACTERISTICS

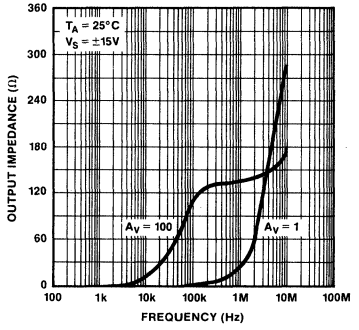
MAXIMUM OUTPUT SWING vs FREQUENCY



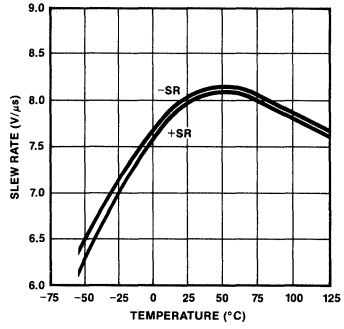
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



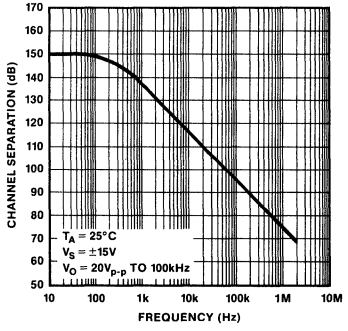
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



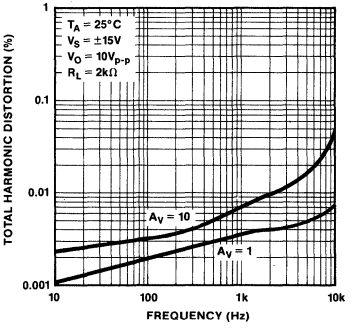
SLEW RATE vs TEMPERATURE



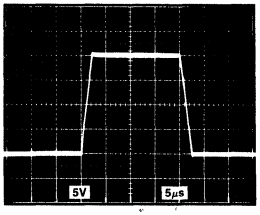
CHANNEL SEPARATION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY

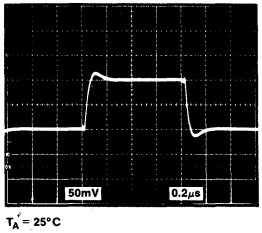


LARGE-SIGNAL TRANSIENT RESPONSE



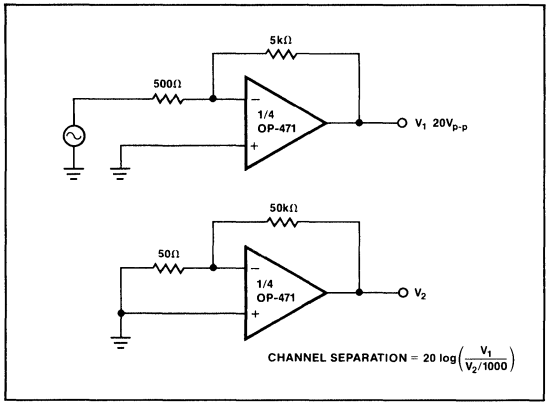
T_A = 25°C
V_S = ±15V
A_V = +1

SMALL-SIGNAL TRANSIENT RESPONSE

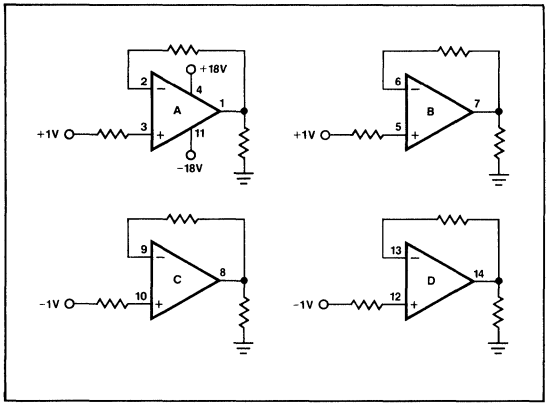


T_A = 25°C
V_S = ±15V
A_V = +1

CHANNEL SEPARATION TEST CIRCUIT



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

VOLTAGE AND CURRENT NOISE

The OP-471 is a very low-noise quad op amp, exhibiting a typical voltage noise of only 6.5nV/$\sqrt{Hz}$ @ 1kHz. The low noise characteristic of the OP-471 is in part achieved by operating the input transistors at high collector currents since the voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. As a result, the outstanding voltage noise performance of the OP-471 is gained at the expense of current noise performance which is typical for low noise amplifiers.

To obtain the best noise performance in a circuit it is vital to understand the relationship between voltage noise (e_n), current noise (i_n), and resistor noise (e_t).

TOTAL NOISE AND SOURCE RESISTANCE

The total noise of an op amp can be calulated by:

$$E_n = \sqrt{(e_n)^2 + (i_n R_S)^2 + (e_t)^2}$$

where:

E_n = total input referred noise

e_n = op amp voltage noise

i_n = op amp current noise

e_t = source resistance thermal noise

R_S = source resistance

The total noise is referred to the input and at the output would be amplified by the circuit gain.

Figure 1 shows the relationship between total noise at 1kHz and source resistance. For $R_S < 1k\Omega$ the total noise is domi-

FIGURE 1: Total Noise vs Source Resistance (Including Resistor Noise) at 1kHz

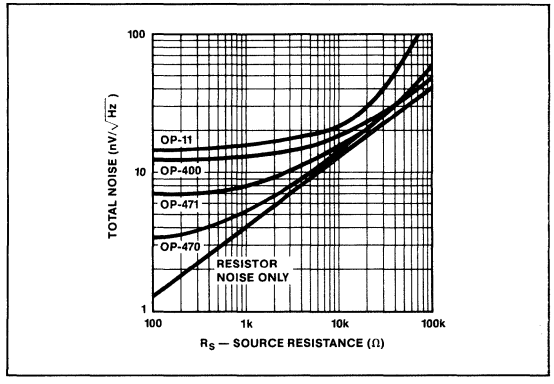
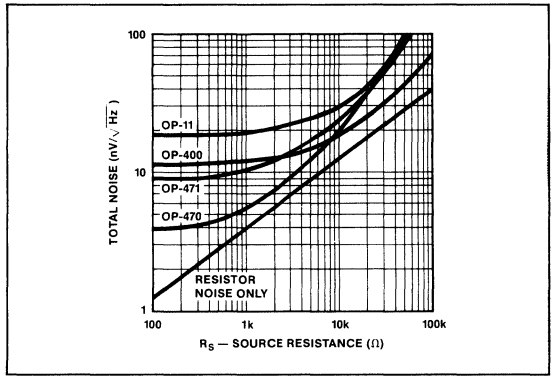


FIGURE 2: Total Noise vs Source Resistance (Including Resistor Noise) at 10Hz



nated by the voltage noise of the OP-471. As R_S rises above 1kΩ, total noise increases and is dominated by resistor noise rather than by voltage or current noise of the OP-471. When R_S exceeds 20kΩ, current noise of the OP-471 becomes the major contributor to total noise.

Figure 2 also shows the relationship between total noise and source resistance, but at 10Hz. Total noise increases more quickly than shown in Figure 1 because current noise is inversely proportional to the square root of frequency. In Figure 2, current noise of the OP-471 dominates the total noise when $R_S > 5k\Omega$.

From Figures 1 and 2 it can be seen that to reduce total noise, source resistance must be kept to a minimum. In applications with a high source resistance, the OP-400, with lower current noise than the OP-471, will provide lower total noise.

Figure 3 shows peak-to-peak noise versus source resistance over the 0.1Hz to 10Hz range. Once again, at low values of R_S, the voltage noise of the OP-471 is the major contributor to peak-to-peak noise. Current noise becomes the major contributor as R_S increases. The crossover point between the OP-471 and the OP-400 for peak-to-peak noise is at $R_S = 17k\Omega$.

The OP-470 is a lower noise version of the OP-471, with a typical noise voltage density of $3.2nV/\sqrt{Hz}$ @ 1kHz. The OP-470 offers lower offset voltage and higher gain than the OP-471, but is a slower speed device, with a slew rate of $2V/\mu s$ compared to a slew rate of $8V/\mu s$ for the OP-471.

For reference, typical source resistances of some signal sources are listed in Table I.

FIGURE 3: Peak-To-Peak Noise (0.1Hz To 10Hz) vs Source Resistance (Includes Resistor Noise)

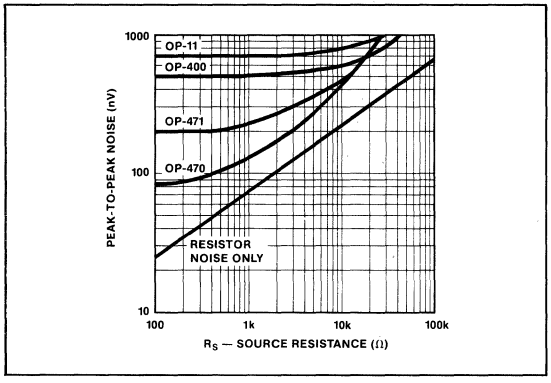


TABLE I

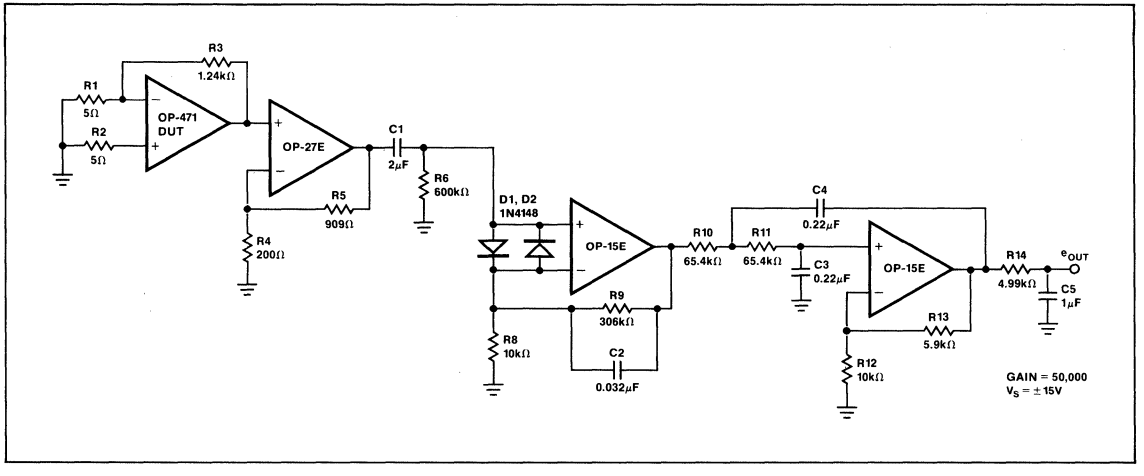
DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500Ω	Typically used in low-frequency applications.
Magnetic tapehead	<1500Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-471 I_B can be neglected.
Magnetic phonograph cartridges	<1500Ω	Similar need for low I_B in direct coupled applications. OP-471 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

For further information regarding noise calculations, see "Minimization of Noise in Op-Amp Applications", Application Note AN-15.

NOISE MEASUREMENTS — PEAK-TO-PEAK VOLTAGE NOISE

The circuit of Figure 4 is a test setup for measuring peak-to-peak voltage noise. To measure the 500nV peak-to-peak

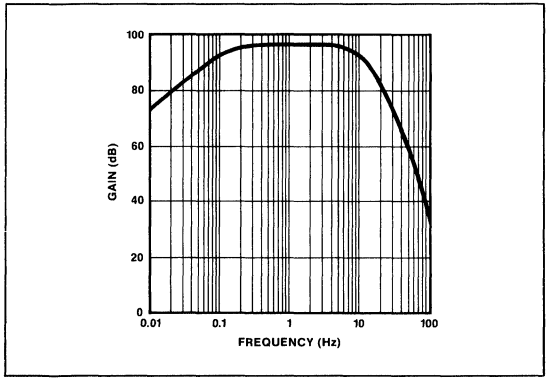
FIGURE 4: Peak-To-Peak Voltage Noise Test Circuit (0.1Hz To 10Hz)



noise specification of the OP-471 in the 0.1Hz to 10Hz range, the following precautions must be observed:

1. The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 13μV due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.
2. For similar reasons, the device has to be well-shielded from air currents. Shielding also minimizes thermocouple effects.
3. Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.
4. The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve of Figure 5, the 0.1Hz corner is defined by only one pole. The test time of 10 seconds acts as an additional pole to eliminate noise contribution from the frequency band below 0.1Hz.
5. A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.
6. Power should be supplied to the test circuit by well bypassed low-noise supplies, e.g. batteries. These will minimize output noise introduced through the amplifier supply pins.

FIGURE 5: 0.1Hz To 10Hz Peak-To-Peak Voltage Noise Test Circuit Frequency Response



NOISE MEASUREMENT — NOISE VOLTAGE DENSITY

The circuit of Figure 6 shows a quick and reliable method of measuring the noise voltage density of quad op amps. Each individual amplifier is series-connected and is in unity-gain, save the final amplifier which is in a noninverting gain of 101. Since the ac noise voltages of each amplifier are uncorrelated, they add in rms fashion to yield:

$$e_{OUT} = 101\ (\sqrt{e_{nA}^2 + e_{nB}^2 + e_{nC}^2 + e_{nD}^2})$$

The OP-471 is a monolithic device with four identical amplifiers. The noise voltage density of each individual amplifier will match, giving:

$$e_{OUT} = 101\ (\sqrt{4e_n^2}) = 101\ (2e_n)$$

FIGURE 6: Noise Voltage Density Test Circuit

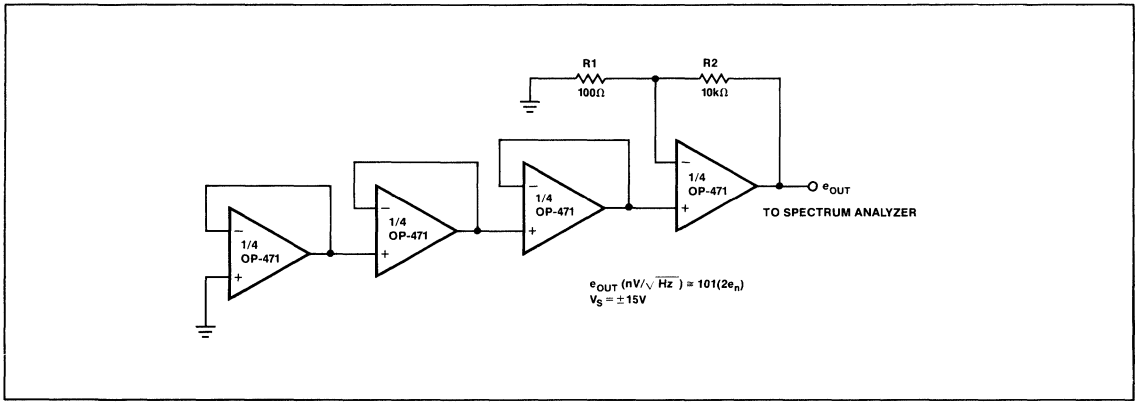
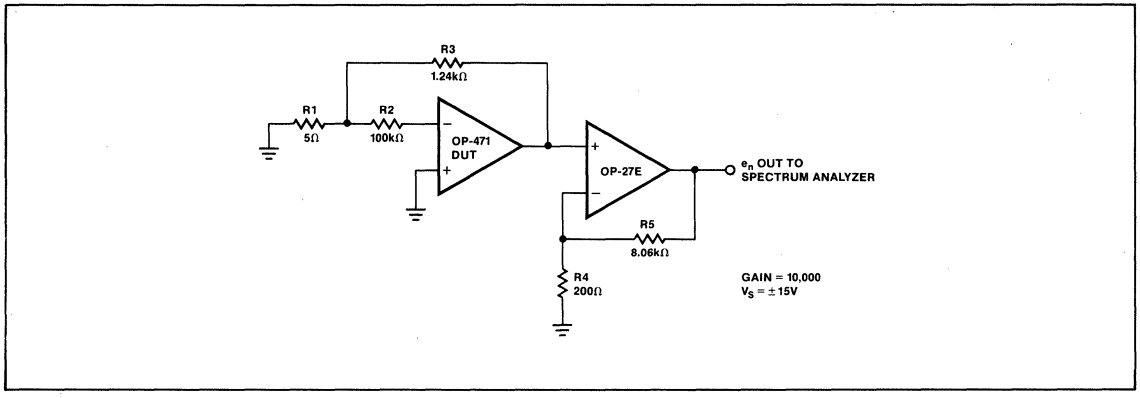


FIGURE 7: Current Noise Density Test Circuit



NOISE MEASUREMENT — CURRENT NOISE DENSITY

The test circuit shown in Figure 7 can be used to measure current noise density. The formula relating the voltage output to current noise density is:

$$i_n = \frac{\sqrt{\left(\frac{e_{nOUT}}{G}\right)^2 - \left(40nV/\sqrt{Hz}\right)^2}}{R_S}$$

where:

G = gain of 10000
R_S = 100kΩ source resistance

CAPACITIVE LOAD DRIVING AND POWER SUPPLY CONSIDERATIONS

The OP-471 is unity-gain stable and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply bypassing is highly recommended. Proper supply bypassing reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP-471.

In the standard feedback amplifier, the op amp's output resistance combines with the load capacitance to form a low-pass filter that adds phase shift in the feedback network and reduces stability. A simple circuit to eliminate this effect is shown in Figure 8. The added components, C1 and R3, decouple the amplifier from the load capacitance and provide additional stability. The values of C1 and R3 shown in Figure 8 are for load capacitances of up to 1000pF when used with the OP-471.

In applications where the OP-471's inverting or noninverting inputs are driven by a low source impedance (under 100Ω) or connected to ground, if V+ is applied before V–, or when V– is disconnected, excessive parasitic currents will flow. Most

FIGURE 8: Driving Large Capacitive Loads

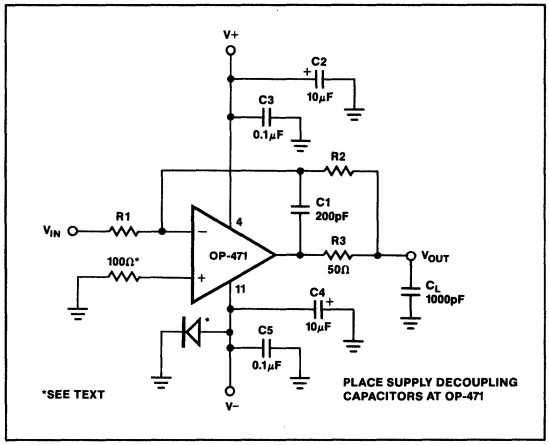
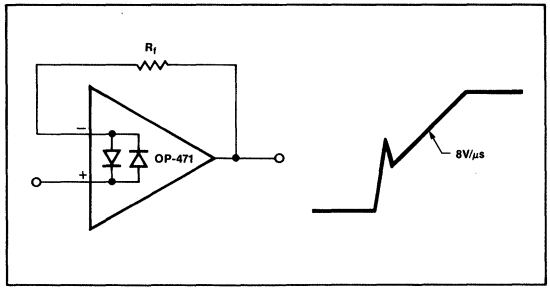


FIGURE 9: Pulsed Operation



applications use dual tracking supplies and with the device supply pins properly bypassed, power-up will not present a problem. A source resistance of at least 100Ω in series with all inputs (Figure 8) will limit the parasitic currents to a safe level if V– is disconnected. It should be noted that any source resistance, even 100Ω, adds noise to the circuit. Where noise is required to be kept at a minimum, a germanium or Schottky diode can be used to clamp the V– pin and eliminate the parasitic current flow instead of using series limiting resistors. For most applications, only one diode clamp is required per board or system.

UNITY-GAIN BUFFER APPLICATIONS

When $R_f \leq 100\Omega$ and the input is driven with a fast, large-signal pulse (>1V), the output waveform will look as shown in Figure 9.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at 10V); the amplifier will stay in its active mode and a smooth transition will occur.

When $R_f > 3k\Omega$, a pole created by R_f and the amplifier's input capacitance (2.6pF) creates additional phase shift and reduces phase margin. A small capacitor (20 to 50pF) in parallel with R_f helps eliminate this problem.

APPLICATIONS

LOW NOISE AMPLIFIER

A simple method of reducing amplifier noise by paralleling amplifiers is shown in Figure 10. Amplifier noise, depicted in Figure 11, is around $5nV/\sqrt{Hz}$ @ 1kHz (R.T.I.). Gain for each paralleled amplifier and the entire circuit is 100. The 200Ω resistors limit circulating currents and provide an effective output resistance of 50Ω. The amplifier is stable with a 10nF capacitive load and can supply up to 30mA of output drive.

HIGH-SPEED DIFFERENTIAL LINE DRIVER

The circuit of Figure 12 is a unique line driver widely used in professional audio applications. With ±18V supplies the line driver can deliver a differential signal of $30V_{p-p}$ into a 1.5kΩ load. The output of the differential line driver looks exactly like a transformer. Either output can be shorted to ground without changing the circuit gain of 5, so the amplifier can easily be set for inverting, noninverting, or differential operation. The line driver can drive unbalanced loads, like a true transformer.

HIGH OUTPUT AMPLIFIER

The amplifier shown in Figure 13 is capable of driving $20V_{p-p}$ into a floating 400Ω load. Design of the amplifier is based on a bridge configuration. A1 amplifies the input signal and drives the load with the help of A2. Amplifier A3 is a unity-gain inverter which drives the load with help from A4. Gain of the high output amplifier with the component values shown is 10, but can easily be changed by varying R1 or R2.

FIGURE 10: Low Noise Amplifier

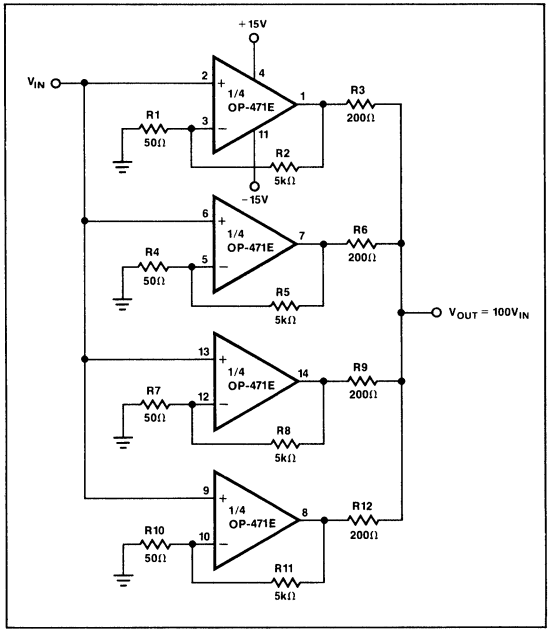


FIGURE 11: Noise Density of Low Noise Amplifier, G = 100

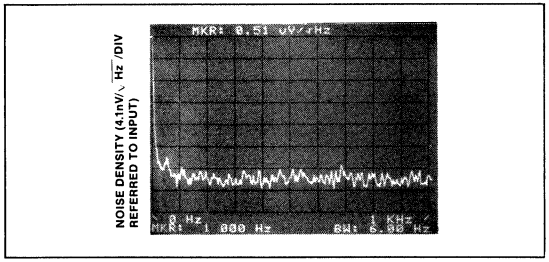


FIGURE 12: High-Speed Differential Line Driver

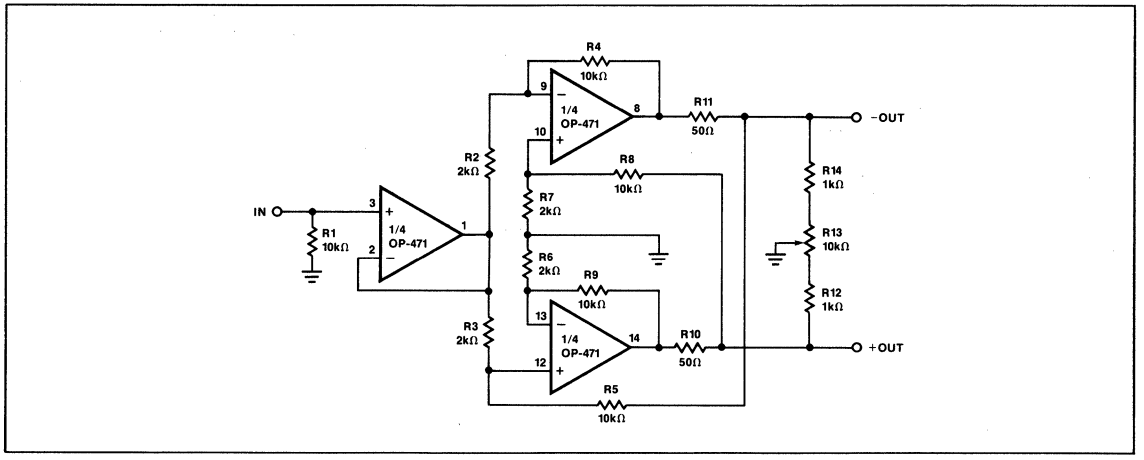
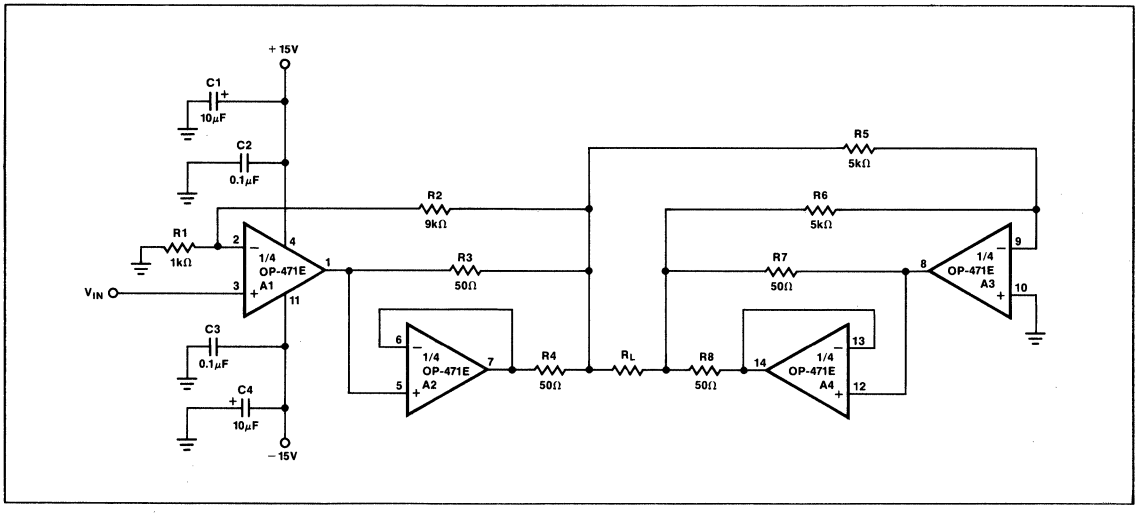


FIGURE 13: High Output Amplifier



QUAD PROGRAMMABLE GAIN AMPLIFIER

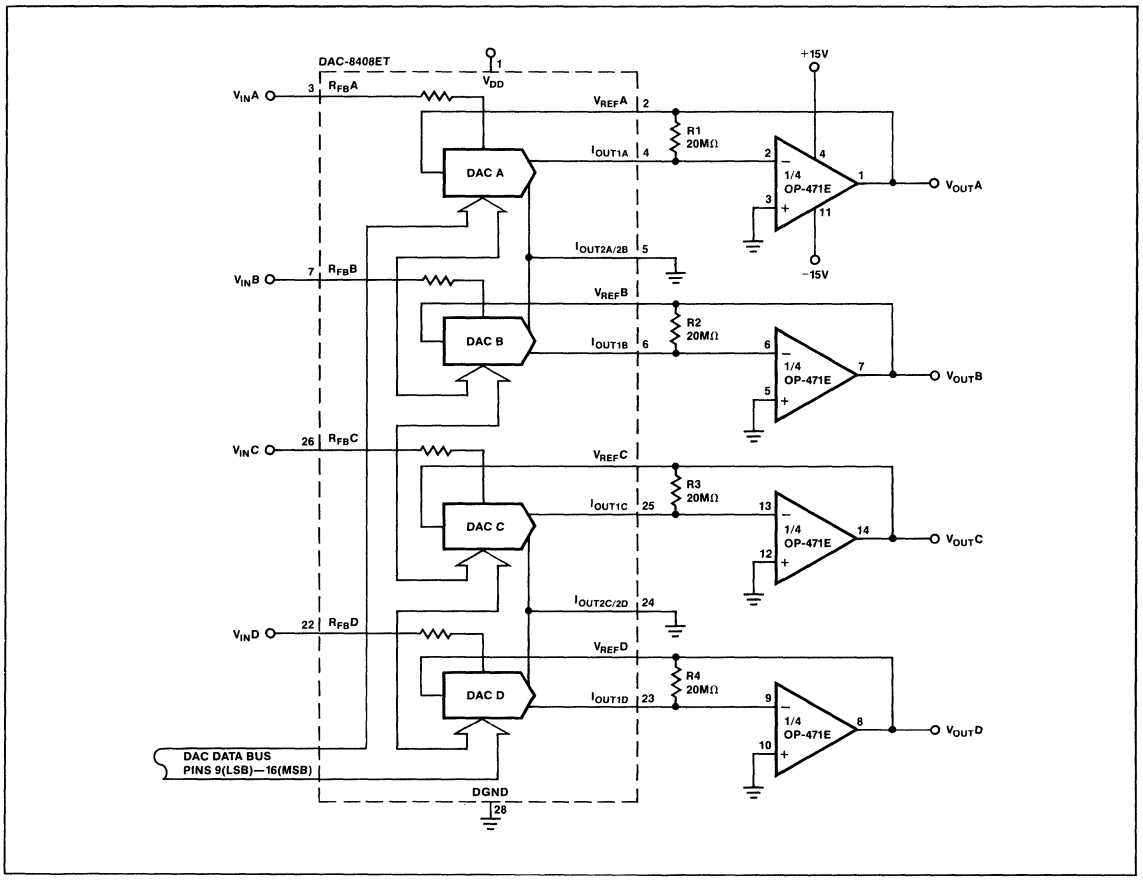
The combination of the quad OP-471 and the DAC-8408, a quad 8-bit CMOS DAC, creates a space-saving quad programmable gain amplifier. The digital code present at the DAC, which is easily set by a microprocessor, determines the ratio between the fixed DAC feedback resistor and the impedance the DAC ladder presents to the op amp feedback loop. Gain of each amplifier is:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{256}{n},$$

where n equals the decimal equivalent of the 8-bit digital code present at the DAC. If the digital code present at the DAC consists of all zeros, the feedback loop will be open causing the op amp output to saturate. The 20MΩ resistors placed in parallel with the DAC feedback loop eliminates this problem with a very small reduction in gain accuracy.

2

FIGURE 14: Quad Programmable Gain Amplifier



LOW PHASE ERROR AMPLIFIER

The simple amplifier depicted in Figure 15 utilizes monolithic matched operational amplifiers and a few resistors to substantially reduce phase error compared to conventional amplifier designs. At a given gain, the frequency range for a specified phase accuracy is over a decade greater than for a standard single op amp amplifier.

The low phase error amplifier performs second-order frequency compensation through the response of op amp A2 in the feedback loop of A1. Both op amps must be extremely well matched in frequency response. At low frequencies, the A1 feedback loop forces $V_2/(K1 + 1) = V_{IN}$. The A2 feedback loop forces $V_O/(K1 + 1) = V_2/(K1 + 1)$ yielding an overall transfer function of $V_O/V_{IN} = K1 + 1$. The DC gain is determined by the resistor divider at the output, V_O, and is not directly affected by the resistor divider around A2. Note, that like a conventional single op amp amplifier, the DC gain is set by resistor ratios only. Minimum gain for the low phase error amplifier is 10.

Figure 16 compares the phase error performance of the low phase error amplifier with a conventional single op amp amplifier and a cascaded two-stage amplifier. The low phase error amplifier shows a much lower phase error, particularly for frequencies where $\omega/\beta\omega_T < 0.1$. For example, phase error of $-0.1°$ occurs at $0.002\ \omega/\beta\omega_T$ for the single op amp amplifier, but at $0.11\ \omega/\beta\omega_T$ for the low phase error amplifier.

For more detailed information on the low phase error amplifier, see Application Note AN-107.

FIGURE 15: Low Phase Error Amplifier

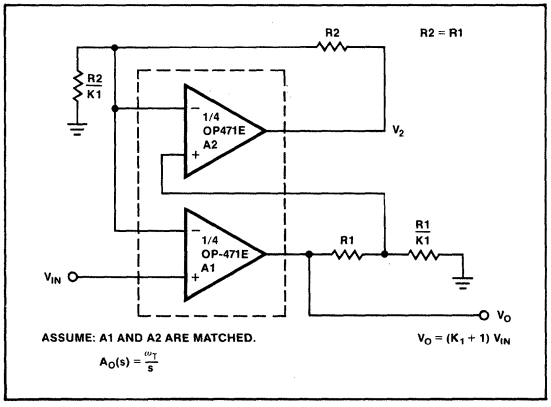
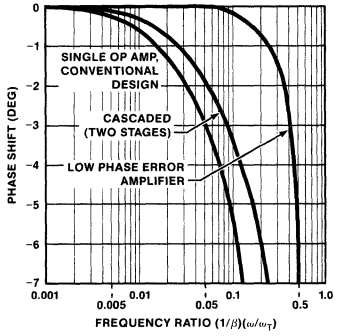


FIGURE 16: Phase Error Comparison



ANALOG DEVICES

Ultra-Low Distortion, High Speed Audio Operational Amplifier

SSM-2131

FEATURES

- **Low Distortion – DC to 40kHz, A_V = +10 ..... 0.01% Typ**
- **High Slew Rate ..... 40V/μs Min**
- **Gain-Bandwidth Product ..... 10MHz Typ**
- **High Gain ..... 200,000 Typ**
- **Common-Mode Rejection ..... 80dB Min**

APPLICATIONS

- **Power Amplifier Driver**
- **Active Filter Circuits**
- **Parametric Equalizers**
- **Graphic Equalizers**
- **Mixing Consoles**
- **Voltage Summers**
- **Active Crossover Networks**

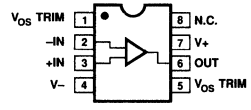
GENERAL DESCRIPTION

The SSM-2131 is a fast JFET input operational amplifier intended for use in audio applications. The SSM-2131 offers a symmetric 50V/μs slew rate for low distortion and is internally compensated for unity gain operation. Power supply current is less than 6.5mA. Unity-gain stability, a wide full-power bandwidth of 800kHz, and excellent ability to handle transient overloads make the SSM-2131 an ideal amplifier for use in high performance audio amplifier circuits.

The SSM-2131's common-mode rejection of 80dB minimum over a ±11 range is exceptional for a high-speed amplifier. High CMR, combined with a minimum 500V/mV gain into a 10kΩ load ensures excellent linearity in both noninverting and inverting gain configurations. This means that distortion will be very low over a wide range of circuit configurations. The low offset provided by the JFET input stage often eliminates the need for AC coupling or for external offset trimming.

The SSM-2131 conforms to the standard 741 pinout with nulling to V–. The SSM-2131 upgrades the performance of circuits using the TL071 by direct replacement.

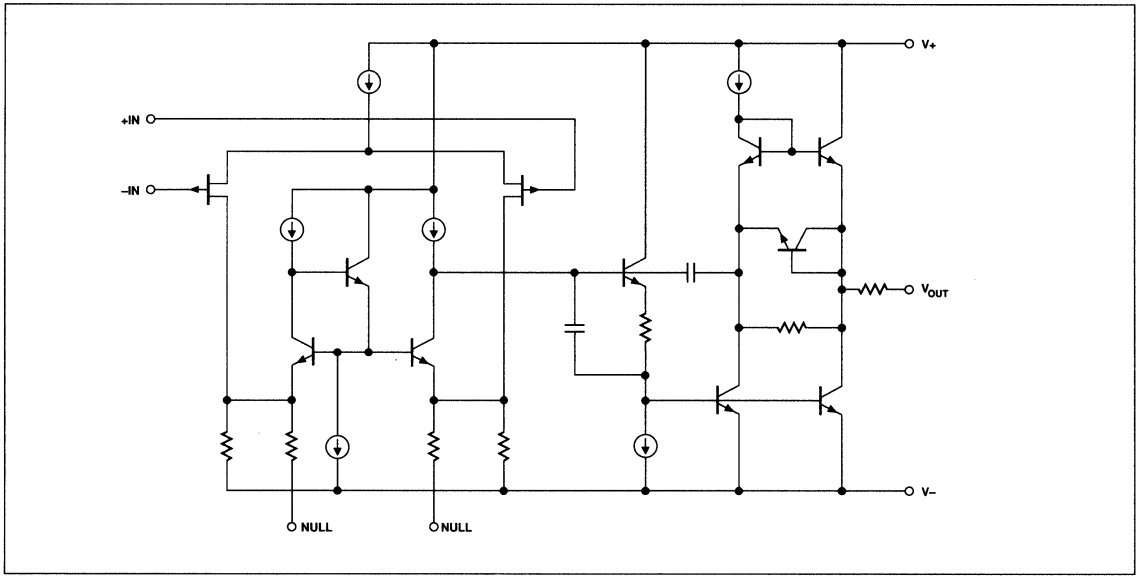
PIN CONNECTIONS



PLASTIC MINI-DIP (P-Suffix)

8-PIN SO (S-Suffix)

SIMPLIFIED SCHEMATIC



ORDERING INFORMATION

PACKAGE		OPERATING TEMPERATURE RANGE
PLASTIC 8-PIN	SO 8-PIN	
SSM2131P	SSM2131S	XIND*

*XIND = –40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Input Voltage (Note 1) ..... ±20V
Differential Input Voltage (Note 1) 40V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to +175°C
Operating Temperature Range ..... –40°C to +85°C
Junction Temperature ..... –65°C to +175°C
Lead Temperature Range (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. For supply voltages less than ±20V, the absolute maximum input voltage is equal to the supply voltage.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

			SSM-2131			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Slew Rate	SR		40	50	–	V/µs
Gain-Bandwidth Product	GBW	f_O = 10kHz	–	10	–	MHz
Full-Power Bandwidth	BW_p	(Note 2)	600	800	–	kHz
Total Harmonic Distortion	THD	DC to 40kHz, R_L = 10kΩ, A_V = +10	–	0.01	–	%
Voltage Noise Density	e_n	f_O = 10Hz f_O = 1kHz	– –	38 13	– –	nV/√Hz
Current Noise Density	i_n	f_O = 1kHz	–	0.007	–	pA/√Hz
Large-Signal Voltage Gain	A_{VO}	R_L = 10kΩ, V_O = ±10V R_L = 2kΩ T_j = 25°C R_L = 1kΩ	500 200 100	900 260 170	– – –	V/mV
Output Voltage Swing	V_O	R_L = 1kΩ	±11.5	+12.5 –11.9	–	V
Offset Voltage	V_{OS}		–	1.5	6.0	mV
Input Bias Current	I_B	V_{CM} = 0V T_j = 25°C	–	130	250	pA
Input Offset Current	I_{OS}	V_{CM} = 0V T_j = 25°C	–	6	50	pA
Input Voltage Range	IVR	(Note 1)	±11.0	+12.5 –12.0	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	80	92	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	–	12	50	µV/V
Supply Current	I_{SY}	No Load V_O = 0V	–	5.1	6.5	mA
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±20	+33 –28	±60	mA
Settling Time	t_s	10V Step 0.01% (Note 3)	–	0.9	1.2	µs
Overload Recovery Time	t_{OR}		–	700	–	ns

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	SSM-2131 MIN	TYP	MAX	UNITS
Phase Margin	ϕ_O	0dB Gain	–	47	–	degrees
Gain Margin	A_{180}	180° Open-Loop Phase Shift	–	9	–	dB
Capacitive Load Drive Capability	C_L	Unity-Gain Stable (Note 4)	100	300	–	pF
Supply Voltage Range	V_S		±8	±15	±20	V

NOTES:
1. Guaranteed by CMR test.
2. Guaranteed by slew-rate test and formula $BW_p = SR/(2\pi 10V_{PEAK})$.
3. Settling time is guaranteed but not tested.
4. Guaranteed but not tested.

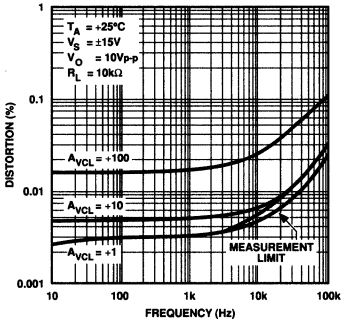
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-40°C \leq T_A \leq 85°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2131 MIN	TYP	MAX	UNITS
Slew Rate	SR	$R_L = 2k\Omega$	40	50	–	V/µs
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$ (Note 1) $R_L = 2k\Omega$ $V_O = \pm 10V$	200 100	500 160	– –	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	±11.0	+12.3 −11.8	–	V
Offset Voltage	V_{OS}		–	2.0	7.0	mV
Offset Voltage Temperature Coefficient	TCV_{OS}		–	8	–	µV/°C
Input Bias Current	I_B	(Note 1)	–	0.6	2.0	nA
Input Offset Current	I_{OS}	(Note 1)	–	0.06	0.4	nA
Input Voltage Range	IVR	(Note 2)	±11.0	+12.5 −12.0	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	80	94	–	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	–	6	50	µV/V
Supply Current	I_{SY}	No Load $V_O = 0V$	–	5.1	6.5	mA
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±8	–	±60	mA

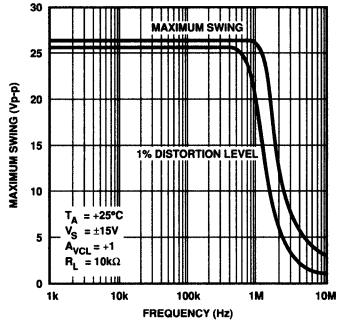
NOTES:
1. $T_j = 85°C$.
2. Guaranteed by CMR test.

TYPICAL PERFORMANCE CHARACTERISTICS

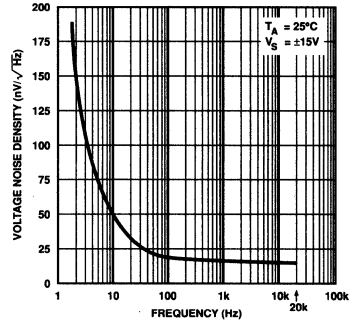
DISTORTION vs FREQUENCY



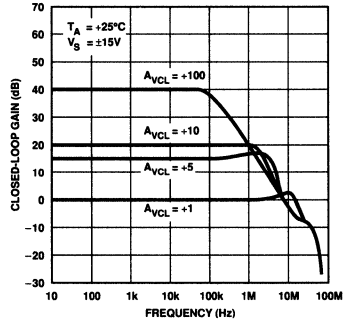
MAXIMUM OUTPUT SWING vs FREQUENCY



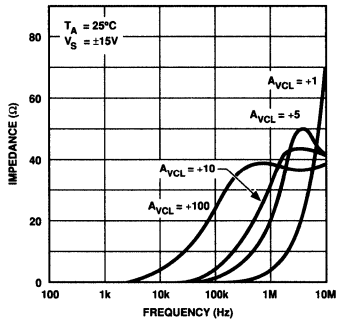
VOLTAGE NOISE DENSITY vs FREQUENCY



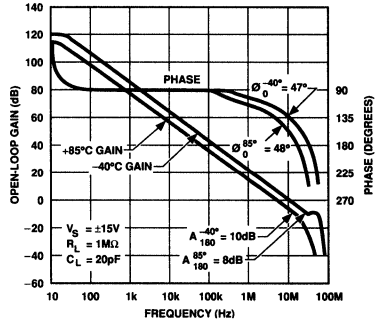
CLOSED-LOOP GAIN vs FREQUENCY



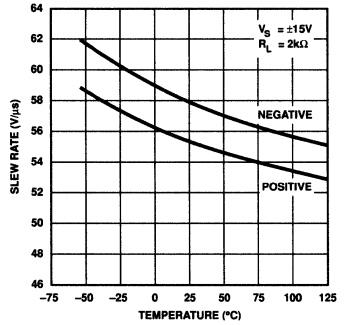
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



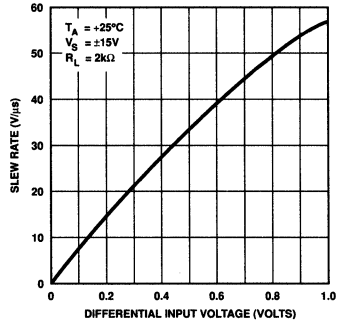
OPEN-LOOP GAIN, PHASE vs FREQUENCY



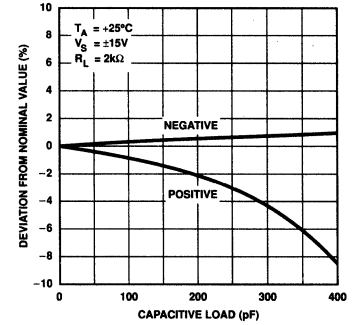
SLEW RATE vs TEMPERATURE



SLEW RATE vs DIFFERENTIAL INPUT VOLTAGE

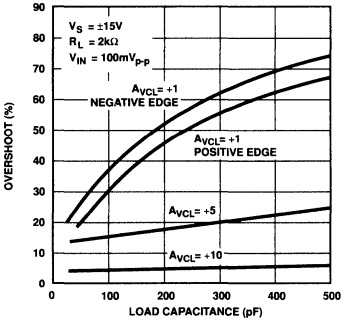


SLEW RATE vs CAPACITIVE LOAD

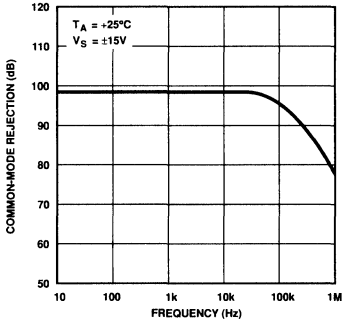


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

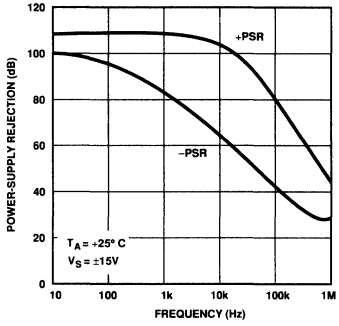
SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



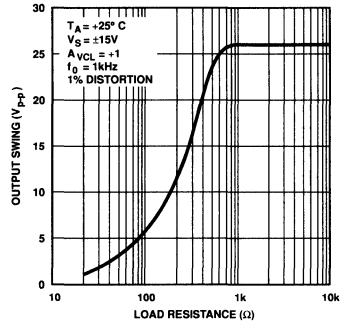
COMMON-MODE REJECTION vs FREQUENCY



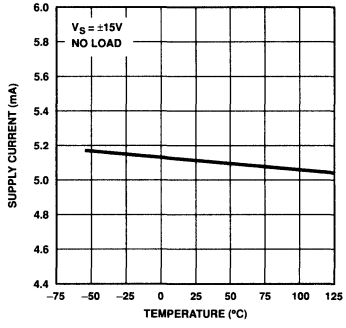
POWER-SUPPLY REJECTION vs FREQUENCY



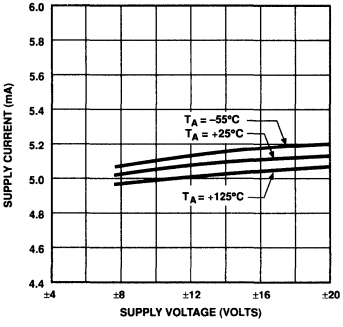
OUTPUT SWING vs LOAD RESISTANCE



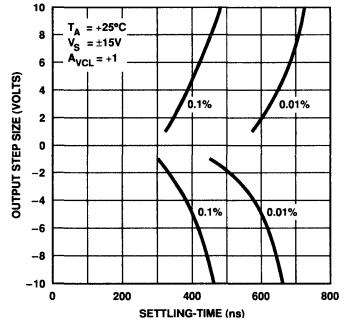
SUPPLY CURRENT vs TEMPERATURE



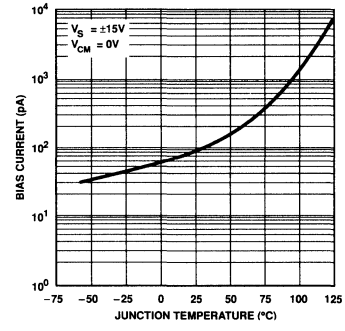
SUPPLY CURRENT vs SUPPLY VOLTAGE



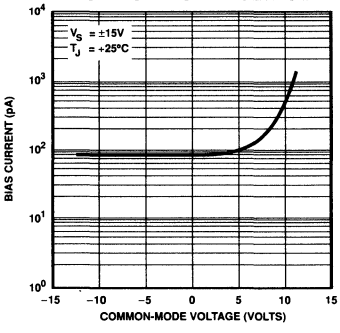
SETTLING-TIME vs STEP SIZE



BIAS CURRENT vs JUNCTION TEMPERATURE



BIAS CURRENT vs COMMON-MODE VOLTAGE



APPLICATIONS INFORMATION

The SSM-2131 combines speed with a high level of input precision usually found only with slower devices. Well-behaved AC performance in the form of clean transient response, symmetrical slew rates and a high degree of forgiveness to supply decoupling are the hallmarks of this amplifier. AC gain and phase response are quite independent of temperature or supply voltage. Figure 1 shows the SSM-2131's small-signal response. Even with 75pF loads, there is minimal ringing in the output waveform. Large-signal response is shown in Figure 2. This figure clearly shows the SSM-2131's exceptionally close matching between positive and negative slew rates. Slew rate symmetry decreases the DC offset a system encounters when processing high-frequency signals, and thus reduces the DC current necessary for load driving.

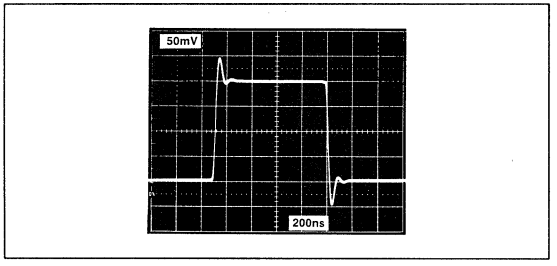


FIGURE 1: *Small-Signal Transient Response, Z_L = 2kΩ//75pF*

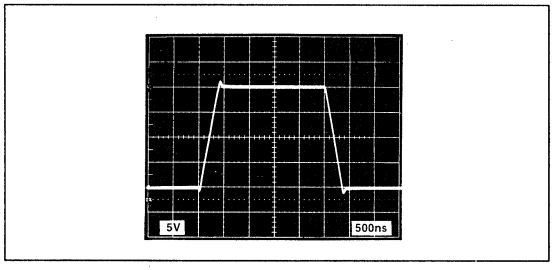


FIGURE 2: *Large-Signal Transient Response, Z_L = 2kΩ//75pF*

As with most JFET-input amplifiers, the output of the SSM-2131 may undergo phase inversion if either input exceeds the specified input voltage range. Phase inversion will not damage the amplifier, nor will it cause an internal latch-up.

Supply decoupling should be used to overcome inductance and resistance associated with supply lines to the amplifier.

For most applications, a 0.1µF to 0.01µF capacitor should be placed between each supply pin and ground.

OFFSET VOLTAGE ADJUSTMENT

Offset voltage is adjusted with a 10kΩ to 100kΩ potentiometer as shown in Figure 3. The potentiometer should be connected between pins 1 and 5 with its wiper connected to the V– supply.

Alternately, V_{OS} may be nulled by attaching the potentiometer wiper through a 1MΩ resistor to the positive supply rail.

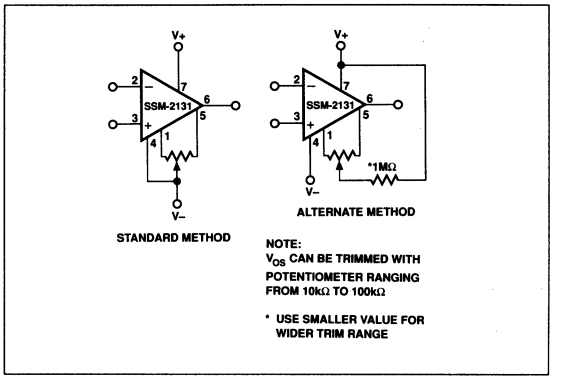


FIGURE 3: *Input Offset Voltage Nulling*

VOLTAGE SUMMING

Because of its extremely low input bias current and large unity-gain bandwidth, the SSM-2131 is ideal for use as a voltage summer or adder.

The following figures show both an inverting and noninverting voltage adder.

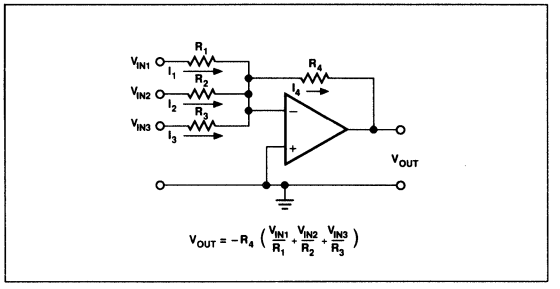


FIGURE 4: *Inverting Adder*

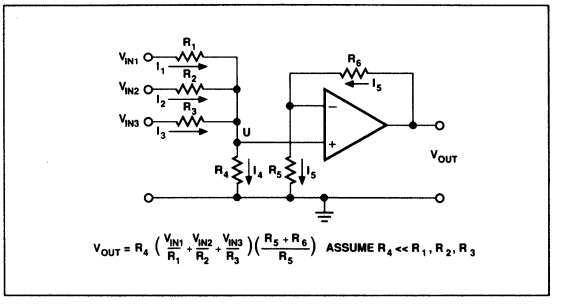


FIGURE 5: *Noninverting Adder*

CURRENT FEEDBACK

AUDIO POWER AMPLIFIER

The SSM-2131 can be used as the input buffer in a current feedback audio power amplifier as shown in Figure 6. This design is capable of very good performance as shown in Figures 7, 8 and 9. At 1kHz and 50 watts output into an 8Ω load, the amplifier generates just 0.002% THD, and is flat to 1MHz. The slew rate for the overall amplifier is more than adequate at 300V/μs and is responsible for the very low dynamic intermodulation distortion (DIM-100) that was measured at just 0.0017% at 50 watts output into 8 ohms. The total amplifier idling current for all tests was approximately 300mA; the V+/V++ and V–/V–– power supplies were both ±40V; and the gain was set to 24.0.

In a current feedback amplifier, a unity or low gain input buffer drives a low impedance network. Any differential current that flows in the collectors of the buffer (SSM-2131) output transistors is fed, via the two complementary Wilson current mirrors A and B, to a high impedance gain node where the high output voltage is generated.

This voltage is then buffered by a double emitter follower driver stage and fed to the complementary power MOSFET output stage. No RC compensation network to ground or output inductor is required at the output of this amplifier to make it stable. As the 100kHz square wave response shows, there's no evidence of any instability in the circuit. Capacitive load compensation can be provided by the components marked TBD on the amplifier schematic. These were not used in the test, however.

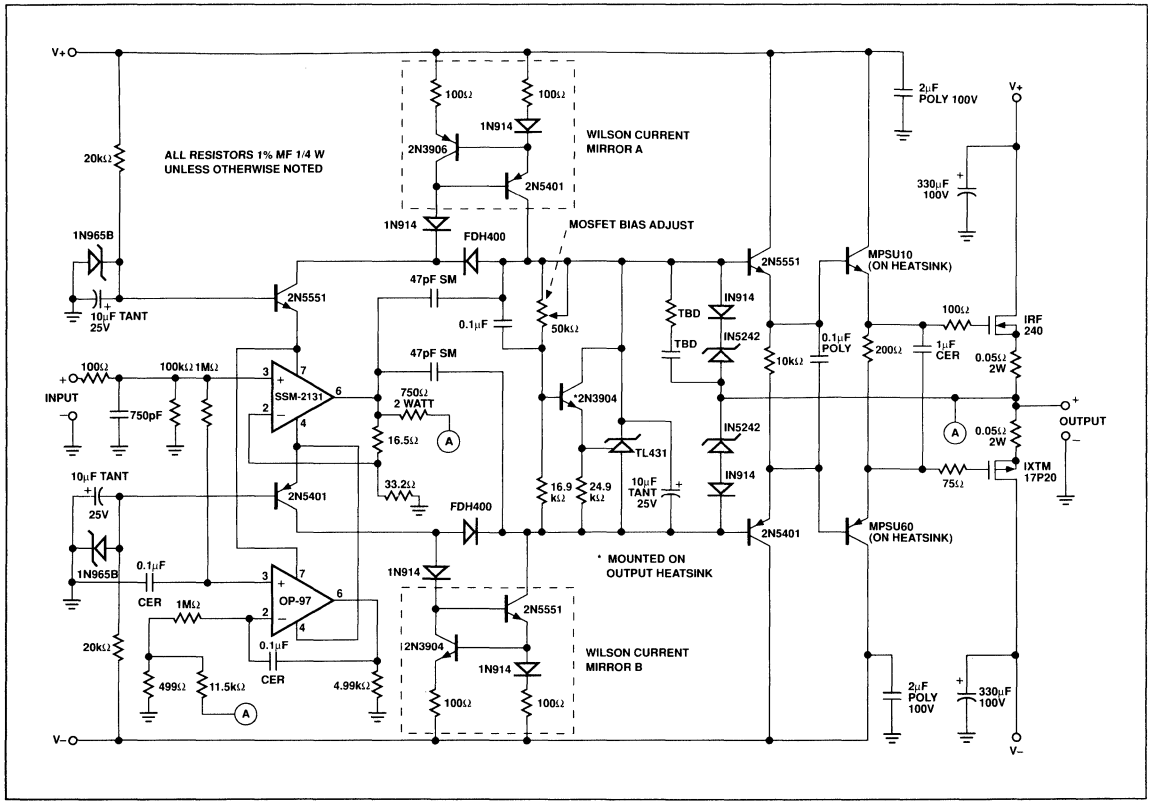


FIGURE 6: *Audio Power Amplifier Schematic*

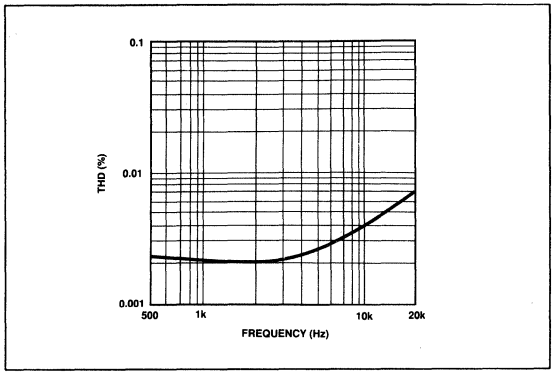


FIGURE 7: *THD vs. Frequency (at 50W into 8Ω).*

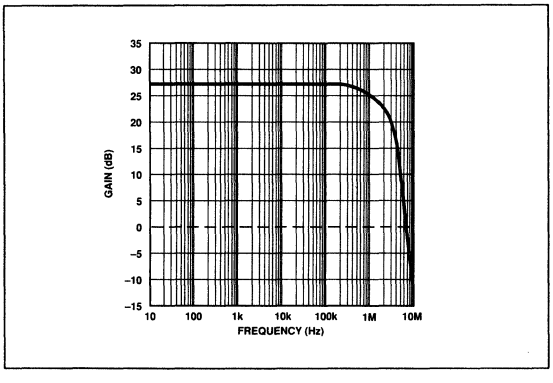


FIGURE 8: *Frequency Response*

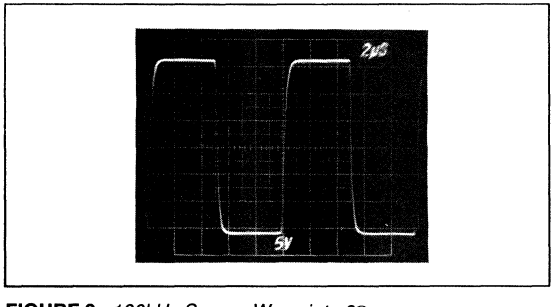


FIGURE 9: *100kHz Square Wave into 8Ω.*

One problem that is commonly encountered with current feedback amplifiers is that the mismatch between the two current mirrors A and B forces a small bias current to appear at the input buffer's output terminal. This bias current (usually in the range of 1-100μA) is multiplied by the feedback resistor of 750Ω and generates an output offset that could be tens of millivolts in magnitude. Matched transistors could be used in the current mirrors, but these do not completely eliminate the output offset problem.

An inexpensive solution is to use a low power precision DC op amp, such as the OP-97, to control the amplifier's DC characteristics, thus overriding the DC offset due to mismatch in the current feedback loop. The OP-97 acts as a current output DC-servo amplifier that injects a compensating current into the emitters of the low voltage regulator transistors (that power the SSM-2131) to correct for current mirror mismatch. Since the OP-97 is set for an overall input-to-output gain of 24.0 as well, the DC output offset is equal to the OP-97's V_{OS} x 24.0, which is roughly 1 millivolt. Thus, any offset trimming can be completely eliminated. Together, the SSM-2131 and OP-97 provide a level of performance that exceeds most of the requirements for audio power amplifers. The driver circuit can handle several pairs of power MOSFETs in the output stage if required. This topology can be used in circuits that must deliver several hundreds of watts to a load by using higher voltage transistors in the driver stage. Operation with rail voltages in excess of ±100V is possible. If more gain is desired, the SSM-2131 input buffer can have its gain increased from the nominal value of 1.5 used in this example to as much as 10 before its bandwidth drops below that of the current feedback section.

DRIVING A HIGH-SPEED ADC

The SSM-2131's open-loop output resistance is approximately 50Ω. When feedback is applied around the amplifier, output resistance decreases in proportion to closed-loop gain divided by open-loop gain (A_{VCL}/A_{VOL}). Output impedance increases as open-loop gain rolls-off with frequency. High-speed analog-to-digital converters require low source impedances at high frequency. Output impedance at 1MHz is typically 5Ω for an SSM-2131 operating at unity-gain. If lower output impedances are required, an output buffer may be placed at the output of the SSM-2131.

HIGH-CURRENT OUTPUT BUFFER

The circuit in Figure 10 shows a high-current output stage for the SSM-2131 capable of driving a 75Ω load with low distortion. Output current is limited by R_1 and R_2. For good tracking between the output transistors Q_1, Q_2, and this biasing diodes D_1 and D_2, thermal contact must be maintained between the transistor and its associated diode. If good thermal contact is not maintained, R_1 and R_2 must be increased to 5-6Ω in order to prevent thermal runaway. Using 5Ω resistors, the circuit easily drives a 75Ω load (Figure 11). Output resistance is decreased and heavier loads may be driven by decreasing R_1 and R_2.

Base current and biasing for Q_1 and Q_2 are provided by two current sources, the SSM-2131 and the JFET. The 2kΩ potentiometer in the JFET current source should be trimmed for optimum transient performance. The case of the SSM-2210 should be connected to V–, and decoupled to ground with a 0.1μF capacitor. Compensation for the SSM-2131's input capacitance is provided by C_C. The circuit may be operated at any gain, in the usual op amp configurations.

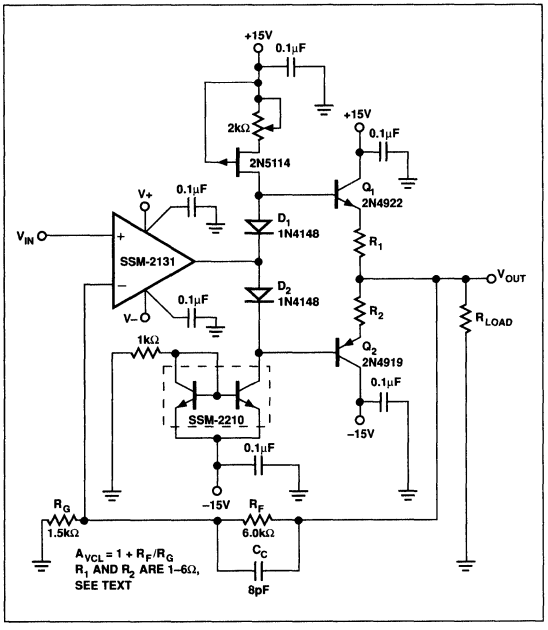


FIGURE 10: *High-Current Output Buffer*

DRIVING CAPACITIVE LOADS

Best performance will always be achieved by minimizing input and load capacitances around any high-speed amplifier. However, the SSM-2131 is guaranteed capable of driving a 100pF capacitive load over its full operating temperature range while

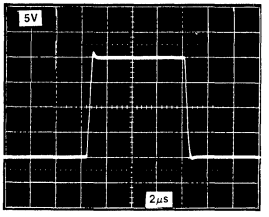


FIGURE 11: *Output Buffer Large-Signal Response*

operating at any gain including unity. Typically, an SSM-2131 will drive more than 250pF at any temperature. Supply decoupling does affect capacitive load driving ability. Extra care should be given to ensure good decoupling when driving capacitive loads; between 1μF and 10μF should be placed on each supply rail.

Large capacitive loads may be driven utilizing the circuit shown in Figure 12. R_1 and C_1 introduce a small amount of feedforward compensation around the amplifier to counteract the phase lag induced by the ouput impedance and load capacitance. At DC and low frequencies, R_1 is contained within the feedback loop. At higher frequencies, feedforward compensation becomes increasingly dominant, and R_1's effect on output impedance will become more noticeable.

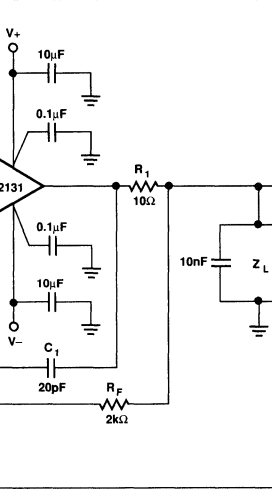


FIGURE 12: *Compensation for Large Capacitive Loads*

When driving very large capacitances, slew rate will be limited by the short-circuit current limit. Although the unloaded slew rate is insensitive to variations in temperature, the output current limit has a negative temperature coefficient, and is asymmetrical with regards to sourcing and sinking current. Therefore, slew rate into excessive capacities will decrease with increasing temperature, and will lose symmetry.

DAC OUTPUT AMPLIFIER

The SSM-2131 is an excellent choice for a DAC output amplifier, since its high speed and fast settling-time allow quick transitions between codes, even for full-scale changes in output level. The DAC output capacitance appears at the operational amplifier inputs, and must be compensated to ensure optimal settling speed. Compensation is achieved with capacitor C in Figure 13. C must be adjusted to account for the DAC's output capacitance, the op amp's input capacitance, and any stray capacitance at the inputs. With a bipolar DAC, an additional shunt resistor may be used to optimize response. This technique is described in PMI's application AN-24.

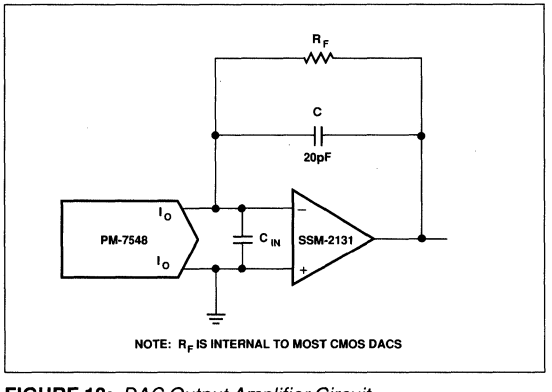


FIGURE 13: *DAC Output Amplifier Circuit*

Highest speed is achieved using bipolar DACs such as PMI's DAC-08, DAC-10 or DAC-312. The output capacitances of these converters are up to an order of magnitude lower than their CMOS counterparts, resulting in substantially faster settling-times. The high output impedance of bipolar DACs allows the output amplifier to operate in a true current-to-voltage mode, with a noise gain of unity, thereby retaining the amplifier's full bandwidth. Offset voltage has minimal effect on linearity with bipolar converters.

CMOS digital-to-analog converters have higher output capacitances and lower output resistances than bipolar DACs. This results in slower settling-times, higher sensitivity to offset voltages and a reduction in the output amplifier's bandwidth. These tradeoffs must be balanced against the CMOS DAC's advantages in terms of interfacing capability, power dissipation, accuracy levels and cost. Using the internal feedback resistor which is present on most CMOS converters, the gain applied to offset voltage varies between 4/3 and 2, depending upon output code. Contributions to linearity error will be as much as 2/3 V_{OS}. In a 10-volt 12-bit system, this may add up to an additional 1/5LSB DNL with the SSM-2131. Amplifier bandwidth is reduced by the same gain factor applied to offset voltage, however the SSM-2131's 10MHz gain-bandwidth product results in no reduction of the CMOS converter's multiplying bandwidth.

Individual DAC data sheets should be consulted for more complete descriptions of the converters and their circuit applications.

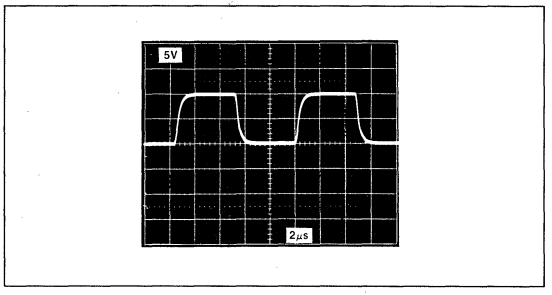


FIGURE 14: *DAC Output Amplifier Response (PM-7545 DAC)*

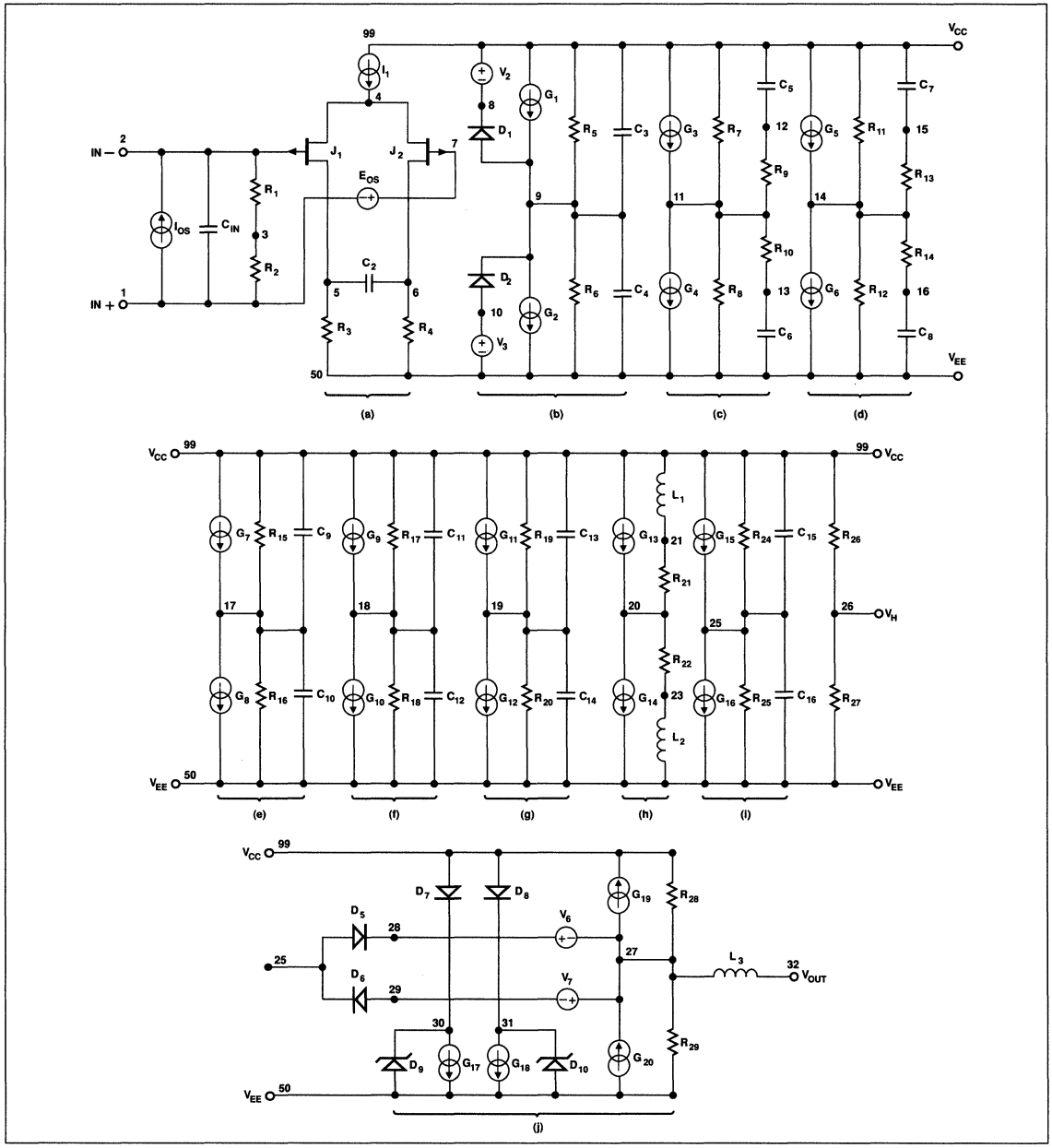
COMPUTER SIMULATIONS

The following pages show the SPICE macro-model for the SSM-2131 high-speed audio operational amplifier. This model was tested with, and is compatible with PSpice* and HSPICE**. The schematic and net-list are included here so that the model can easily be used. This model can accommodate multiple frequency poles and multiple zeroes, which is an advanced concept that results in more accurate AC and transient responses necessary for simulating the behavior of today's high-speed op amps. For example, 8 poles and 2 zeroes are required to sufficiently simulate the SSM-2131, which this advanced model can easily accommodate.

Throughout the SSM-2131 macro-model, RC networks produce the multiple poles and zeroes which simulate the SSM-2131's AC behavior. Each stage contains a pole or a pole-zero pair. The stages are separated from each other by voltage-controlled current sources so that the poles and zero locations do not interact. The only nonlinear elements in the entire model are two p-channel JFETs which comprise the input stage. Limiting the model to almost entirely linear circuit elements significantly reduces simulation time and simplifies model development.

*PSpice is a registered trademark of MicroSim Corporation.
**HSPICE is a tradmark of Meta-Software, Inc.

```
SSM-2131 MACRO-MODEL  © PMI 1989
*
* subckt SSM-2131  1  2 32  99  50
*
* INPUT STAGE & POLE AT 15.9 MHz
*
r1   1   3        5E11
r2   2   3        5E11
r3   5   50       707.36
r4   6   50       707.36
cin  1   2        5E-12
c2   5   6        7.08E-12
i1   99  4        1E-3
ios  1   2        4E-12
eos  7   1        poly(1) 20 26 1E-3 1
j1   5   2   4    jx
j2   6   7   4    jx
*
* SECOND STAGE & POLE AT 45 Hz
*
r5   9   99       176.84E6
r6   9   50       176.84E6
c3   9   99       20E-12
c4   9   50       20E-12
g1   99  9        poly(1) 5 6 3.96E-3 1.4137E-3
g2   9   50       poly(1) 6 5 3.96E-3 1.4137E-3
v2   99  8        2.5
v3   10  50       3.1
d1   9   8        dx
d2   10  9        dx
*
* POLE-ZERO PAIR AT 1.80 MHz/2.20 MHz
*
r7   11  99       1E6
r8   11  50       1E6
r9   11  12       4.5E6
r10  11  13       4.5E6
c5   12  99       16.1E-15
c6   13  50       16.1E-15
g3   99  11       9  26  1E-6
g4   11  50       26  9  1E-6
*
* POLE-ZERO PAIR AT 1.80 MHz/2.20 MHz
*
r11  14  99       1E6
r12  14  50       1E6
r13  14  15       4.5E6
r14  14  16       4.5E6
c7   15  99       16.1E-15
c8   16  50       16.1E-15
g5   99  14       11 26 1E-6
g6   14  50       26 11 1E-6
*
* POLE AT 53 MHz
*
r15  17  99       1E6
r16  17  50       1E6
c9   17  99       3E-15
c10  17  50       3E-15
g7   99  17       14 26 1E-6
g8   17  50       26 14 1E-6
*
* POLE  AT 53 MHz
*
r17  18  99       1E6
r18  18  50       1E6
c11  18  99       3E-15
c12  18  50       3E-15
g9   99  18       17 26 1E-6
g10  18  50       26 17 1E-6
*
* POLE AT 53 MHz
*
r19  19  99       1E6
r20  19  50       1E6
c13  19  99       3E-15
c14  19  50       3E-15
g11  99  19       18 26 1E-6
g12  19  50       26 18 1E-6
*
*COMMON-MODE GAIN NETWORK WITH ZERO AT 100 kHZ
*
r21  20  21       1E6
r22  20  23       1E6
l1   21  99       1.5915
l2   23  50       1.5915
g13  99  20       3  26 1E-11
g14  20  50       26  3 1E-11
*
*POLE AT 79.6 MHz
*
r24  25  99       1E6
r25  25  50       1E6
c15  25  99       2E-15
c16  25  50       2E-15
g15  99  25       19 26 1E-6
g16  25  50       26 19 1E-6
*
*OUTPUT STAGE
*
r26  26  99       111.1E3
r27  26  50       111.1E3
r28  27  99       90
r29  27  50       90
l3   27  32       2.5E-7
g17  30  50       25 27 11.1111E-3
g18  31  50       27 25 11.1111E-3
g19  27  99       99 25 11.1111E-3
g20  50  27       25 50 11.1111E-3
v6   28  27       0.7
v7   27  29       0.7
d5   25  28       dx
d6   29  25       dx
d7   99  30       dx
d8   99  31       dx
d9   50  30       dy
d10  50  31       dy
*
* MODELS USED
*
.model jx PJF(BETA=999.3E-6 VTO=-2.000 IS=4E-11)
.model dx   D(IS=1E-15)
.model dy   D(IS=1E-15 BV=50)
.ends SSM-2131
```


99
V_{CC}
I_1
4
V_2
8
D_1
G_1
R_5
C_3
G_3
R_7
C_5
12
R_9
G_5
R_{11}
C_7
15
R_{13}
2
IN –
J_1
J_2
7
E_{OS}
R_1
I_{OS}
C_{IN}
3
R_2
1
IN +
C_2
5
6
R_3
R_4
9
11
14
D_2
10
G_2
V_3
R_6
C_4
G_4
R_8
R_{10}
13
C_6
G_6
R_{12}
R_{14}
16
C_8
50
V_{EE}
(a)
(b)
(c)
(d)
V_{CC} 99
G_7 R_{15} C_9
G_9 R_{17} C_{11}
G_{11} R_{19} C_{13}
G_{13} L_1 21 R_{21}
G_{15} R_{24} C_{15} R_{26}
17
18
19
20
25
26 V_H
G_8 R_{16} C_{10}
G_{10} R_{18} C_{12}
G_{12} R_{20} C_{14}
R_{22}
G_{14} 23 L_2
G_{16} R_{25} C_{16} R_{27}
V_{EE} 50
(e)
(f)
(g)
(h)
(i)
V_{CC} 99
D_7
D_8
G_{19}
R_{28}
D_5
28
V_6
25
27
L_3
32 V_{OUT}
D_6
29
V_7
30
31
R_{29}
D_9
G_{17}
G_{18}
D_{10}
G_{20}
V_{EE} 50
(j)

Low Noise Audio Operational Amplifier

SSM-2134

FEATURES

- Very Low Input Noise Voltage ..... 3.5nV/ $\sqrt{Hz}$ Typ
- Wide Small-Signal Bandwidth ..... 10MHz Typ
- High Current Drive Capability ($10V_{RMS}$ into 600Ω @ $V_S = \pm 18V$)
- High Slew Rate ..... 13V/μs Typ
- Wide Power Bandwidth ..... 200kHz Typ
- High Open-Loop Gain ..... 200V/mV Typ
- Extended Industrial Temperature Range ..... –40°C to +85°C
- Direct Replacement for Industry Standard 5534AN

APPLICATIONS

- High Quality Audio Amplifiers
- Telephone Channel Amplifiers
- Active Filter Designs
- Microphone Preamplifiers
- Audio Line Drivers
- Low-Level Signal Detection
- Servo Control Systems

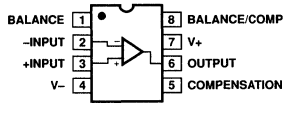
GENERAL DESCRIPTION

The SSM-2134 is a high performance low noise operational amplifier which offers exceptionally low voltage noise of 3.5nV/$\sqrt{Hz}$, outstanding output drive capability, and very high small-signal and power bandwidth. This makes the SSM-2134 an ideal choice for use in high quality and professional audio equipment, instrumentation, and control circuits.

The SSM-2134 is internally compensated for $A_V \geq 3$. However, the frequency response can be optimized with an external compensation capacitor to enable the SSM-2134 to operate at unity-gain or drive large capacitive loads.

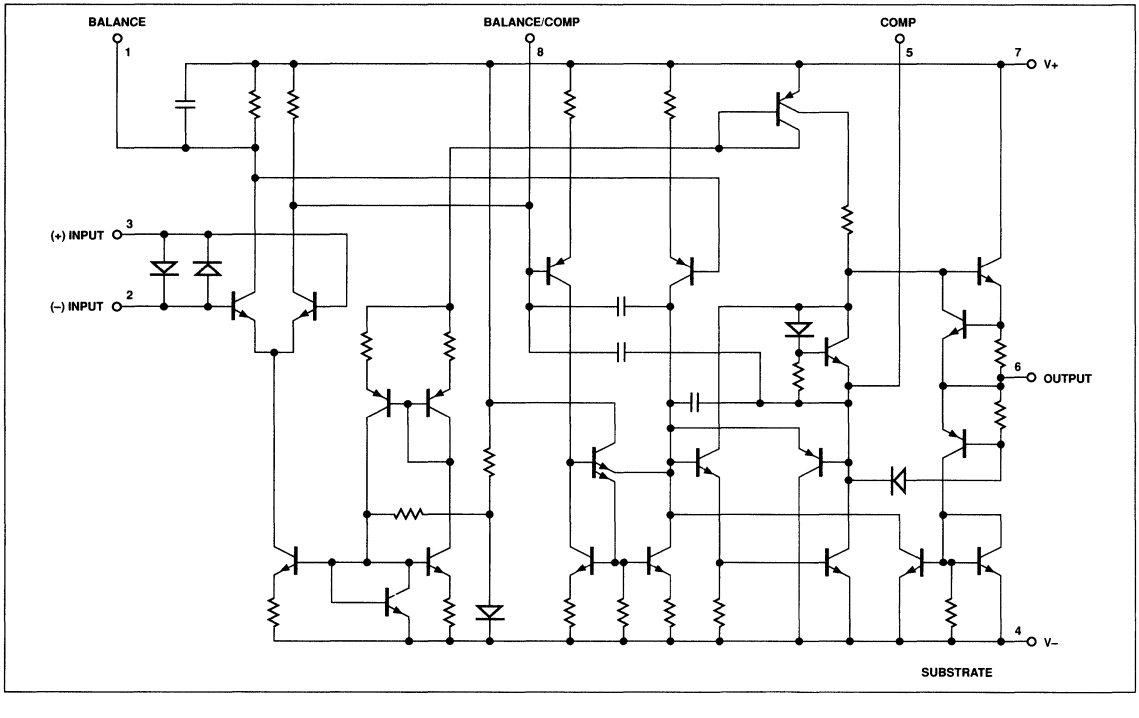
The SSM-2134 is offered in an 8-pin plastic DIP and its performance and characteristics are guaranteed over the extended industrial temperature range of –40°C to +85°C.

PIN CONNECTIONS



8-PIN EPOXY DIP (P-Suffix)

SIMPLIFIED SCHEMATIC



ORDERING INFORMATION †

PACKAGE		OPERATING TEMPERATURE RANGE
SSM2134P	8-Pin Plastic	–40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Differential Input Voltage (Note 1) ..... ±0.5V
Input Voltage (Note 2) ..... ±22V
Power Dissipation 300mW
Derate Above +24°C ..... 2.5mW/°C
Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature ..... –60°C to +150°C

NOTES:
1. The SSM-2134's inputs are protected by diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.6V, the input current should be limited to 10mA.
2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
3. Output maybe shorted to ground at V_S = ±15V, T_A = +25°C. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS at V_S = ±15V and T_A = +25°C, unless otherwise noted.

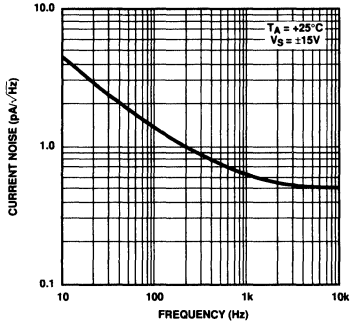
			SSM-2134P			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}		–	0.3	2	mV
		–40°C ≤ T_A ≤ +85°C	–	0.4	3	
Input Offset Current	I_{OS}		–	15	300	nA
		–40°C ≤ T_A ≤ +85°C	–	25	400	
Input Bias Current	I_B		–	350	1500	nA
		–40°C ≤ T_A ≤ +85°C	–	500	2000	
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 600Ω, V_O = ±10V	25	200	–	V/mV
		R_L ≥ 600Ω, V_O = ±10V –40°C ≤ T_A ≤ +85°C	15	150	–	
Supply Current	I_{SY}	No Load	–	4.5	6.5	mA
Output Voltage Swing	V_O	V_S = ±15V, R_L ≥ 600Ω	±12	±13	–	V
		V_S = ±18V, R_L ≥ 600Ω	±15	±16	–	
Output Short-Circuit Current	I_{SC}	(Note 1)	–	65	–	mA
Input Resistance-Differential-Mode	R_{IN}	(Note 2)	30	100	–	kΩ
Input Voltage Range	IVR		±12	±13	–	V
Common-Mode Rejection	CMR	V_{CM} = ±12V	70	114	–	dB
Power Supply Rejection Ratio	PSRR		–	6	100	µV/V
Rise Time	t_r	R_L ≥ 600Ω, C_C = 22pF	–	20	–	ns
Overshoot	OS	C_L = 100pF	–	20	–	%
AC Gain		C_C = 0, f_O = 10kHz	–	6	–	V/mV
		C_C = 22pF, f_O = 10kHz	–	2.2	–	
Unity-Gain Bandwidth	GBW	C_C = 22pF, C_L = 100 p F	–	10	–	MHz
Slew Rate	SR	C_C = 0	–	13	–	V/µs
		C_C = 22pF	–	6	–	
Full Power Bandwidth	BW_P	V_O = ±10V, C_C = 22pF	–	95	–	kHz
		C_C = 0	–	200	–	
Input Noise Voltage Density	e_n	f_O = 30Hz	–	5.5	7.0	nV/√Hz
		f_O = 1kHz	–	3.5	4.5	
Input Noise Current Density	i_n	f_O = 30Hz	–	2.5	–	pA/√Hz
		f_O = 1kHz	–	0.6	–	
Broadband Noise Figure	F_N	R_S = 5kΩ, f = 10Hz to 20kHz	–	0.7	–	dB
Total Harmonic Distortion	THD	V_{IN} = 3V_{RMS}, A_V = +1000, R_L = 2kΩ	–	0.025	–	%

NOTES:
1. Output may be shorted to ground at V_S = ±15V, T_A = +25°C. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.
2. Guaranteed by design.

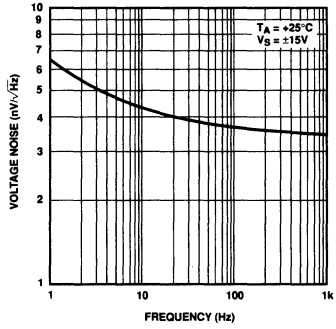
Specifications subject to change, Consult latest data sheet.

TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

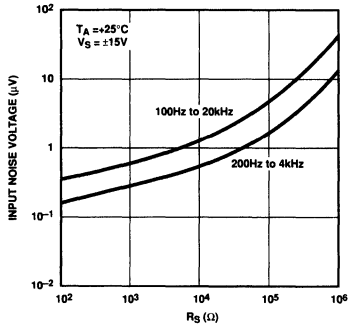
CURRENT NOISE DENSITY vs FREQUENCY



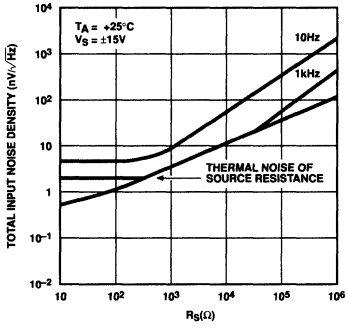
VOLTAGE NOISE DENSITY vs FREQUENCY



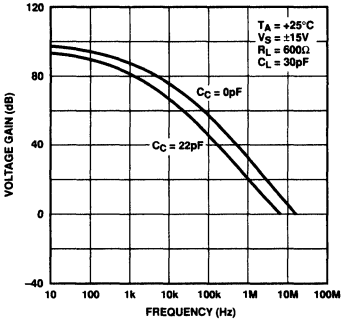
BROADBAND INPUT NOISE VOLTAGE



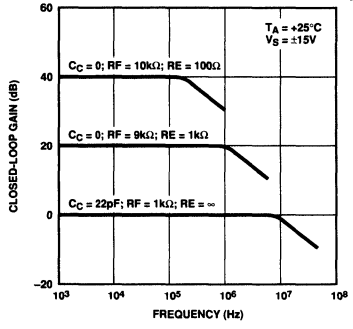
TOTAL INPUT NOISE DENSITY



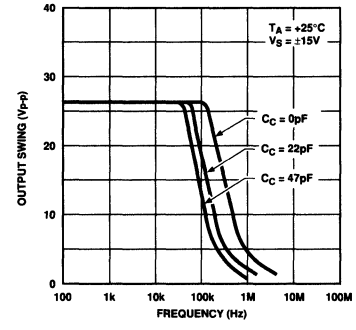
OPEN-LOOP GAIN vs FREQUENCY



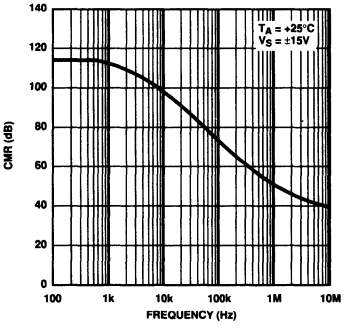
CLOSED-LOOP GAIN vs FREQUENCY



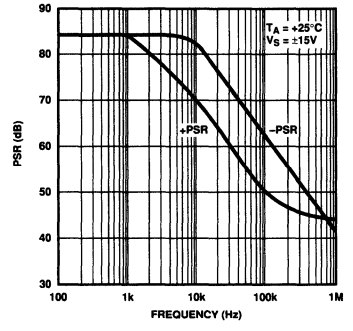
OUTPUT VOLTAGE SWING vs FREQUENCY



CMR vs FREQUENCY

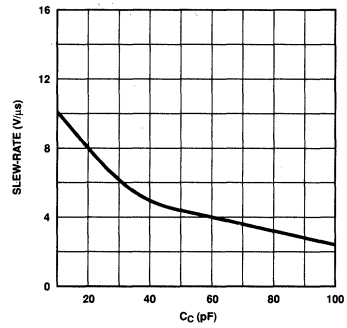


PSR vs FREQUENCY

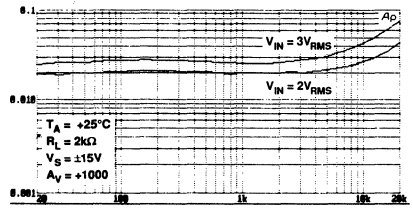


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

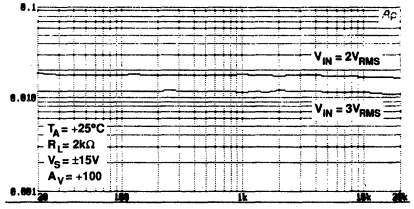
SLEW RATE vs COMPENSATION CAPACITOR



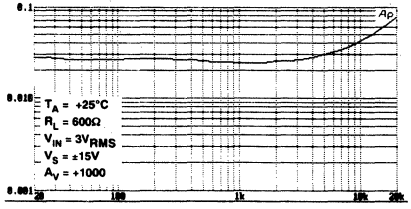
TOTAL HARMONIC DISTORTION vs FREQUENCY



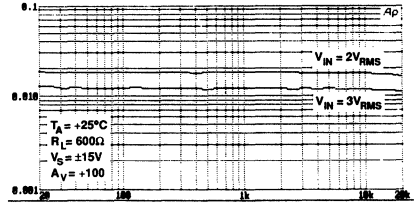
TOTAL HARMONIC DISTORTION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY

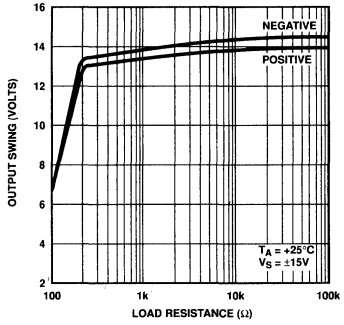


TOTAL HARMONIC DISTORTION vs FREQUENCY

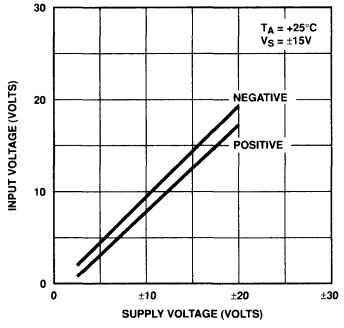


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

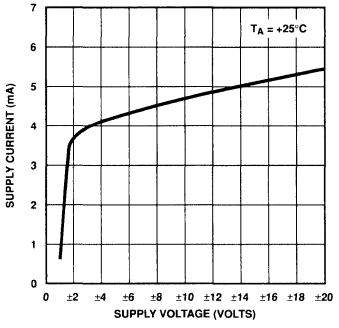
OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



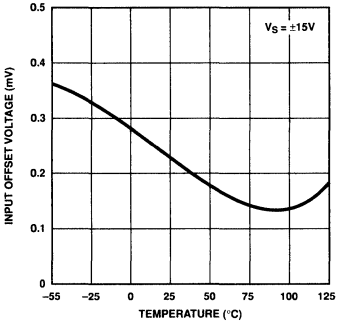
INPUT COMMON-MODE VOLTAGE vs SUPPLY VOLTAGE



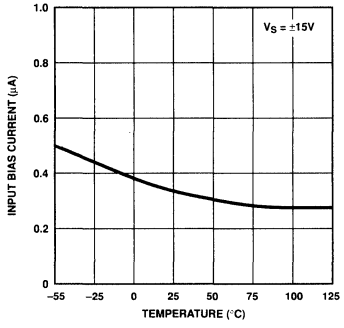
SUPPLY CURRENT vs SUPPLY VOLTAGE



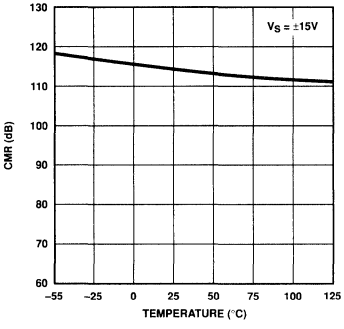
INPUT OFFSET VOLTAGE vs TEMPERATURE



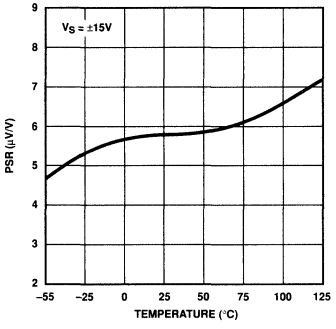
INPUT BIAS CURRENT vs TEMPERATURE



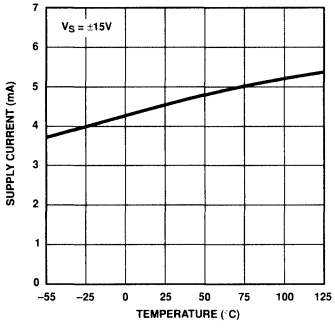
CMR vs TEMPERATURE



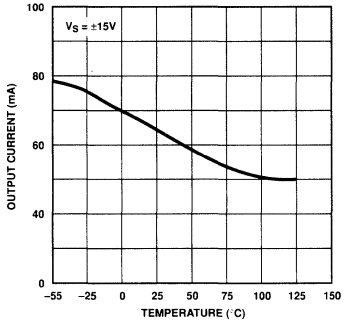
PSR vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE

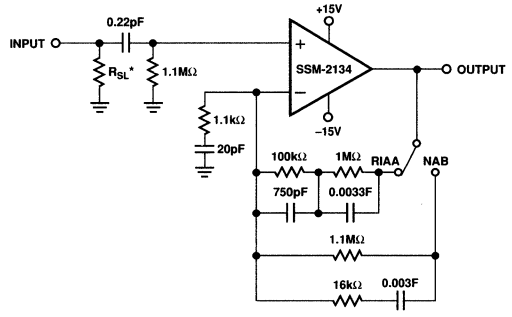


SHORT-CIRCUIT CURRENT vs TEMPERATURE

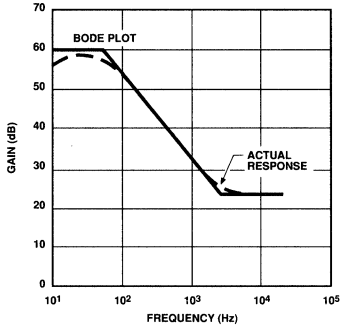


APPLICATIONS INFORMATION

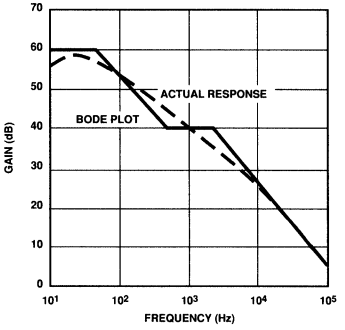
PREAMPLIFIER-RIAA/NAB COMPENSATION



*SELECT TO PROVIDE SPECIFIED TRANSDUCER LOADING
OUTPUT NOISE 0.8mV$_{RMS}$ (WITH INPUT SHORTED)



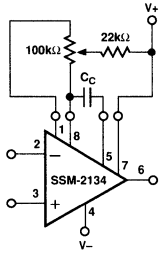
BODE PLOT OF RIAA EQUALIZATION AND THE RESPONSE REALIZED IN AN ACTUAL CIRCUIT USING THE SSM-2134



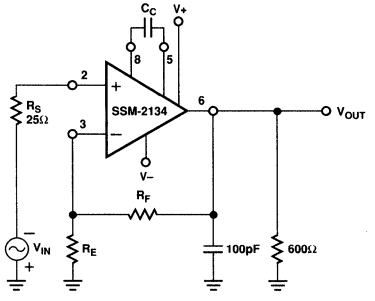
BODE PLOT OF NAB EQUALIZATION AND THE RESPONSE REALIZED IN THE ACTUAL CIRCUIT USING THE SSM-2134

TEST CIRCUIT

FREQUENCY COMPENSATION AND OFFSET VOLTAGE ADJUSTMENT CIRCUIT



CLOSED-LOOP FREQUENCY RESPONSE



Dual, Low Noise, High-Speed Audio Operational Amplifier ($A_{VCL} \geq 3$)

SSM-2139

FEATURES

- **Ultra-Low Voltage Noise ..... 3.2nV/$\sqrt{Hz}$**
- **High Slew Rate 11V/μs**
- **Excellent Gain Bandwidth Product 30MHz**
- **Low Supply Current (Both Amplifiers) 4mA**
- **Low Offset Voltage 500μV**
- **High Gain 1,700V/mV**
- **Compensated for Minimum Gain of 3**
- **Low Cost**
- **Industry Standard 8-Pin Plastic Dual Pinout**

APPLICATIONS

- **Microphone Preamplifiers**
- **Audio Line Drivers**
- **Active Filters**
- **Phono and Tape Head Preamplifiers**
- **Equalizers**

ORDERING INFORMATION

PACKAGE		OPERATING TEMPERATURE RANGE
PLASTIC 8-PIN	16-PIN SOL	
SSM2139P	SSM2139S	XIND*

* XIND = –40°C to +85°C

For availability on SOL package, contact your local sales office.

GENERAL DESCRIPTION

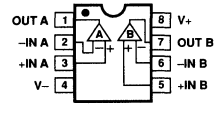
The SSM-2139 is a low noise, high-speed dual audio operational amplifier which has been internally compensated for gains equal to, or greater than three.

This monolithic bipolar op amp offers exceptional voltage noise performance of 3.2nV/$\sqrt{Hz}$ (typical) with a guaranteed specification of only 5nV/$\sqrt{Hz}$ MAX @ 1kHz.

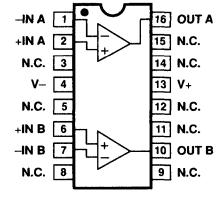
The high slew rate of 11V/μs and the gain-bandwidth product of 30MHz is achieved without compromising the power consumption of the device. The SSM-2139 draws only 4mA of supply current for both amplifiers.

Continued

PIN CONNECTIONS

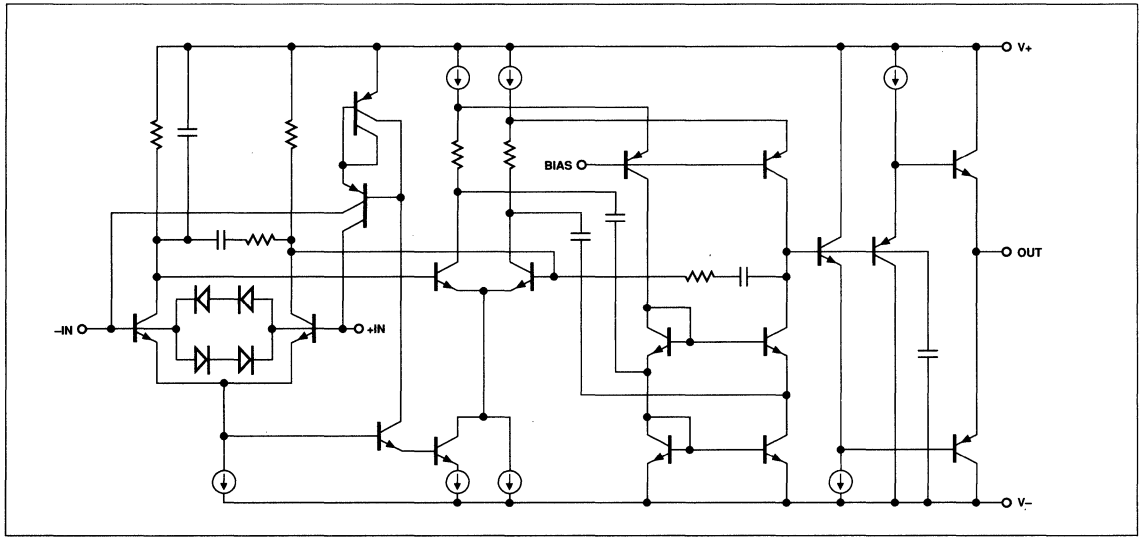


8-PIN PLASTIC MINI-DIP (P-Suffix)



16-PIN SOL (S-Suffix)

SIMPLIFIED SCHEMATIC (One of two amplifiers is shown.)



These characteristics make the SSM-2139 an ideal choice for use in high quality professional audio equipment, instrumentation, and control circuit applications.

The low offset voltage V_{OS} of 500µV MAX (20µV typical) and offset voltage drift of only 2.5µV/°C MAX assures system accuracy and eliminates the need for external V_{OS} adjustments.

The SSM-2139's outstanding open-loop gain of 1,700,000 and its exceptional gain linearity eliminate incorrectable system nonlinearities and provides superior performance in high closed-loop gain applications, such as preamplifiers.

The SSM-2139 is offered in an 8-pin plastic DIP and Small Outline (SO) package and its performance and characteristics are guaranteed over the extended industrial temperature range of –40°C to +85°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Differential Input Voltage (Note 2) ..... ±1.0V
Differential Input Current (Note 2) ..... ±25mA
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range ..... –65°C to +150C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_J) ..... –65°C to +150°C
Operating Temperature Range
SSM-2139 (P, S) ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
8-Pin Plastic DIP (P)	96	37	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.
2. The SSM-2139 inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±1.0V, the input current should be limited to ±25mA.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

			SSM-2139			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 1)	–	80	200	nV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz	–	3.6	6.5	nV/√Hz
		f_O = 100Hz	–	3.2	5.5	
		f_O = 1kHz (Note 2)	–	3.2	5.0	
Input Noise Current Density	i_n	f_O = 10Hz	–	1.1	–	pA/√Hz
		f_O = 100Hz	–	0.7	–	
		f_O = 1kHz	–	0.6	–	
Slew Rate	SR		7	11	–	V/µs
Gain Bandwidth Product	GBW	f_O = 100kHz	–	30	–	MHz
Full Power Bandwidth	BWp	$V_O = 27V_{p-p}$, R_L = 2kΩ (Note 3)	–	130	–	kHz
Supply Current (All Amplifiers)	I_{SY}	No Load	–	4	6.5	mA
Total Harmonic Distortion	THD	R_L = 2kΩ, $V_O = 3V_{RMS}$, f_O = 1kHz	–	0.002	–	%
Input Offset Voltage	V_{OS}		–	20	500	µV
Input Offset Current	I_{OS}	V_{CM} = 0V	–	1	50	nA
Input Bias Current	I_B	V_{CM} = 0V	–	5	80	nA
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V				V/mV
		R_L = 10kΩ	1000	1700	–	
		R_L = 2kΩ	500	900	–	
		R_L = 600Ω	–	900	–	
Output Voltage Swing	V_O	$R_L \geq$ 2kΩ	±12	±13.5	–	V
	V_O+	$R_L \geq$ 600Ω	–	+13	–	
	V_O–	$R_L \geq$ 600Ω	–	–10	–	
Common-Mode Rejection	CMR	V_{CM} = ±12V	94	115	–	dB

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	SSM-2139 MIN	TYP	MAX	UNITS
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	105	120	–	dB
Input Voltage Range	IVR	(Note 4)	±12.0	±12.5	–	V
Output Short-Circuit Current	I_{SC}	Sink Source	– –	20 40	– –	mA
Input Resistance Common-Mode	R_{INCM}		–	20	–	GΩ
Input Resistance Differential-Mode	R_{IN}		–	0.4	–	MΩ
Input Capacitance	C_{IN}		–	3	–	pF
Channel Separation	CS	V_O = 20V_{p-p} f_O = 10Hz (Note 1)	125	175	–	dB

NOTES:
1. Guaranteed but not 100% tested.
2. Sample tested.
3. $BW_p = SR/2\pi V_{PEAK}$.
4. Guaranteed by CMR test.

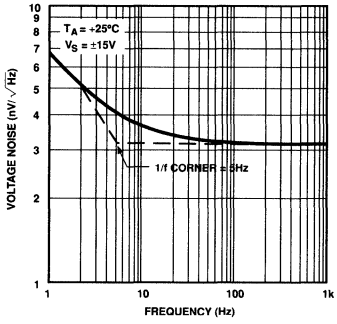
ELECTRICAL CHARACTERISTICS at V_S = ±15V, –40°C ≤ T_A ≤ 85°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2139 MIN	TYP	MAX	UNITS
Supply Current (All Amplifiers)	I_{SY}	No Load	–	4.4	7.2	mA
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	–	V
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 10kΩ R_L = 2kΩ	500 250	1400 700	– –	V/mV
Input Offset Voltage	V_{OS}		–	45	700	µV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.4	2.5	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0V	–	1.5	60	nA
Input Bias Current	I_B	V_{CM} = 0V	–	6	90	nA
Common-Mode Rejection	CMR	V_{CM} = ±12V	94	115	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 to ±18V	100	115	–	dB
Input Voltage Range	IVR	(Note 1)	±12	±12.5	–	V

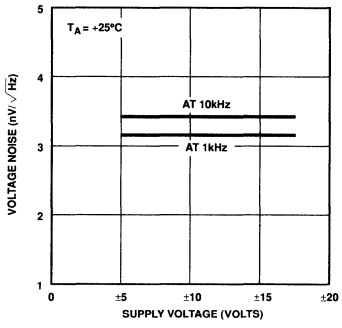
NOTES:
1. Guaranteed by CMR test.

TYPICAL PERFORMANCE CHARACTERISTICS

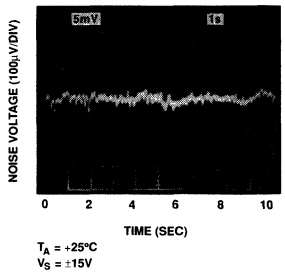
VOLTAGE NOISE DENSITY vs FREQUENCY



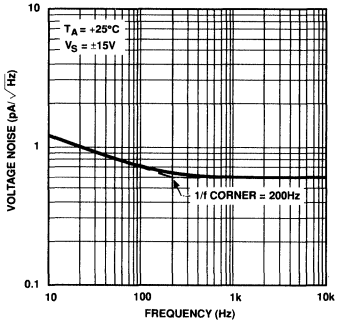
VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE



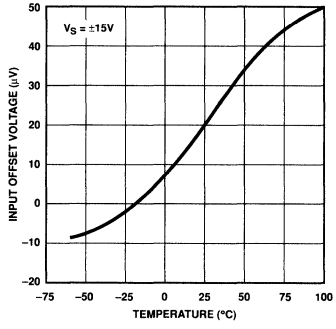
0.1Hz TO 10Hz NOISE



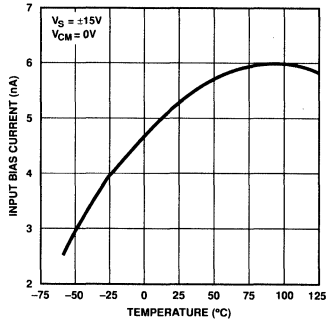
CURRENT NOISE DENSITY vs FREQUENCY



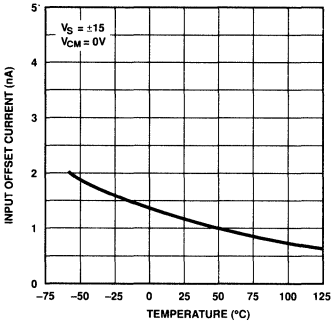
INPUT OFFSET VOLTAGE vs TEMPERATURE



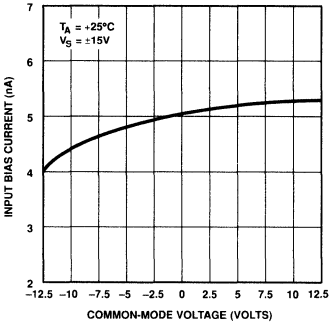
INPUT BIAS CURRENT vs TEMPERATURE



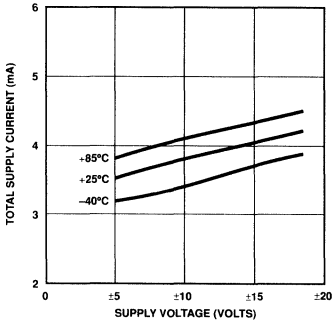
INPUT OFFSET CURRENT vs TEMPERATURE



INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

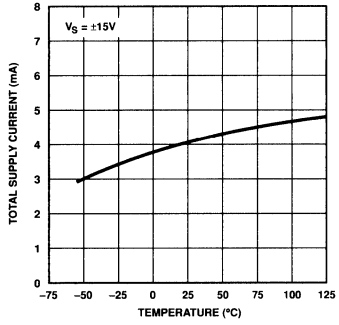


TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE

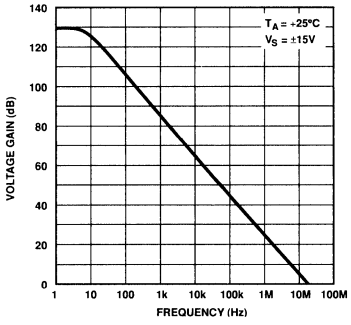


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

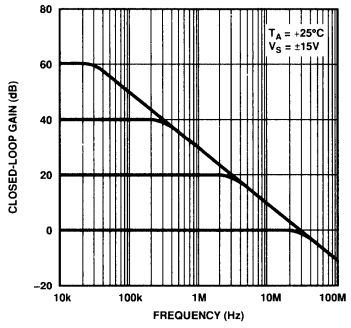
TOTAL SUPPLY CURRENT vs TEMPERATURE



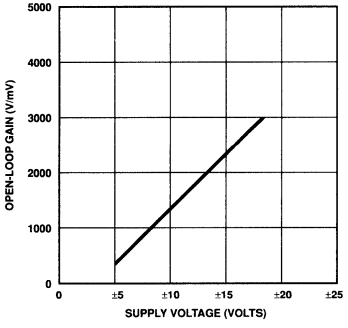
OPEN-LOOP GAIN vs FREQENCY



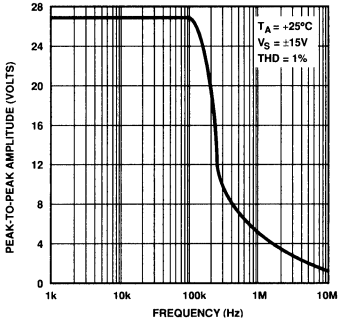
CLOSED-LOOP GAIN vs FREQUENCY



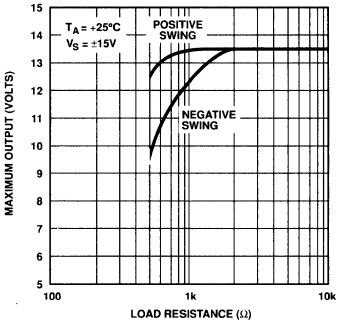
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



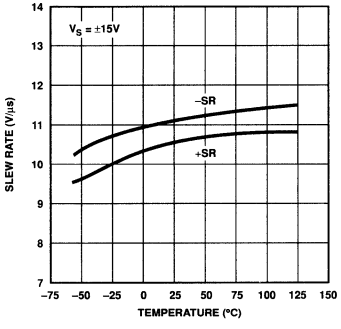
MAXIMUM OUTPUT SWING vs FREQUENCY



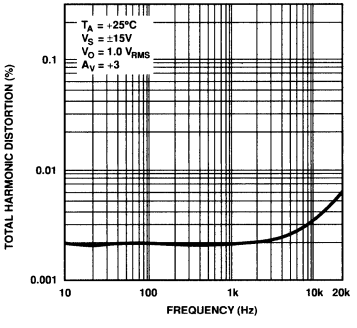
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



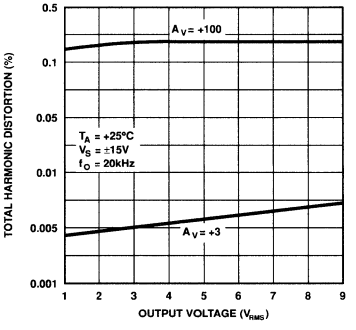
SLEW RATE vs TEMPERATURE



TOTAL HARMONIC DISTORTION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs OUTPUT VOLTAGE



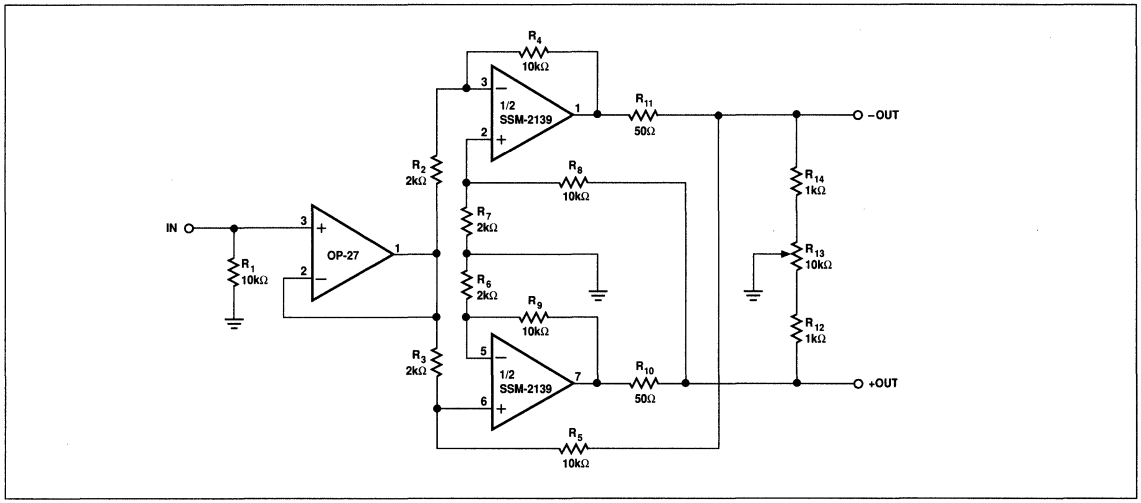


FIGURE 1: *High-Speed Differential Line Driver*

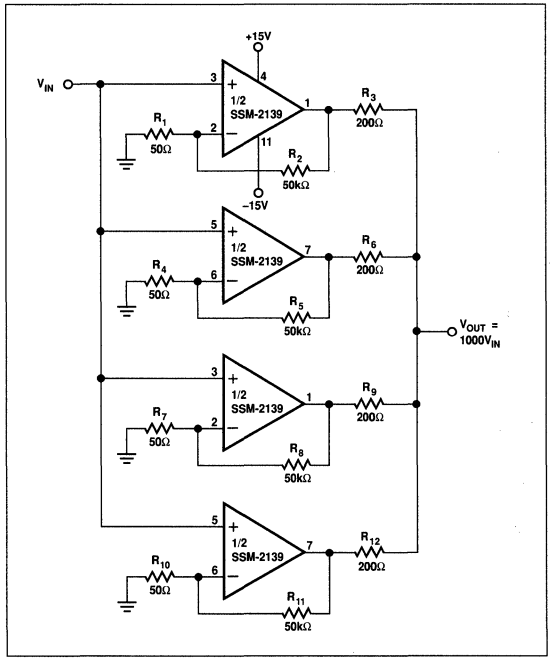


FIGURE 2: *Low Noise Amplifier*

APPLICATIONS INFORMATION

HIGH-SPEED DIFFERENTIAL LINE DRIVER

The circuit of Figure 1 is a unique approach to a line driver circuit widely used in professional audio applications. With ±18V supplies, the line driver can deliver a differential signal of 30Vp-p into a 1.5kΩ load. The output of the differential line driver looks exactly like a transformer. Either output can be shorted to ground without changing the circuit gain of 5, so the amplifier can easily be set for inverting, noninverting, or differential operation. The line driver can drive unbalanced loads, like a true transformer.

LOW NOISE AMPLIFIER

A simple method of reducing amplifier noise is by paralleling amplifiers as shown in Figure 2. Amplifier noise, depicted in Figure 3, is around $2nV/\sqrt{Hz}$ @ 1kHz (R.T.I.). Gain for each paralleled amplifier and the entire circuit is 1000. The 200Ω resistors limit circulating currents and provide an effective output resistance of 50Ω.

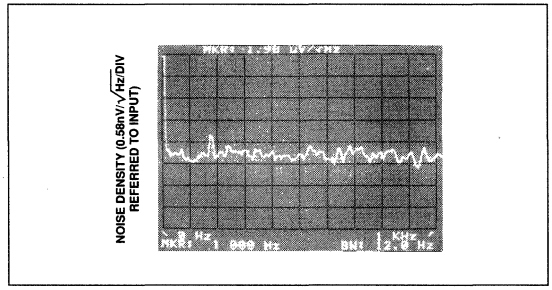


FIGURE 3: *Noise Density of Low Noise Amplifier, G = 1000*

VOLTAGE AND CURRENT NOISE

The SSM-2139 is a low noise, high-speed dual op amp, exhibiting a typical voltage noise of only 3.2nV/$\sqrt{Hz}$ @ 1kHz. The exceptionally low noise characteristics of the SSM-2139 is in part achieved by operating the input transistors at high collector currents since the voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. As a result, the outstanding voltage noise performance of the SSM-2139 is gained at the expense of current noise performance, which is normal for low noise amplifiers.

To obtain the best noise performance in a circuit, it is vital to understand the relationship between voltage noise (e_n), current noise (i_n), and resistor noise (e_t).

TOTAL NOISE AND SOURCE RESISTANCE

The total noise of an op amp can be calculated by:

$$E_n = \sqrt{(e_n)^2 + (i_n R_S)^2 = (e_t)^2}$$

where:

E_n = total input referred noise

e_n = op amp voltage noise

i_n = op amp current noise

e_t = source resistance thermal noise

R_S = source resistance

The total noise is referred to the input and at the output would be amplified by the circuit gain.

Figure 4 shows the relationship between total noise at 1kHz and source resistance. For $R_S < 1k\Omega$, the total noise is dominated by the voltage noise of the SSM-2139. As R_S rises above 1kΩ, total noise increases and is dominated by resistor noise rather than by voltage or current noise of the SSM-2139. When R_S exceeds 20kΩ, current noise of the SSM-2139 becomes the major contributor to total noise.

Figure 5 also shows the relationship between total noise and source resistance, but at 10Hz. Total noise increases more quickly than shown in Figure 4 because current noise is inversely proportional to the square root of frequency. In Figure 5, current noise of the SSM-2139 dominates the total noise when $R_S > 5k\Omega$.

From Figures 4 and 5, it can be seen that to reduce total noise, source resistance must be kept to a minimum.

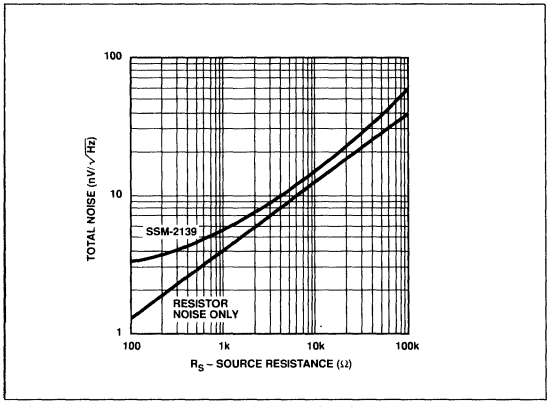


FIGURE 4: *Total Noise vs. Source Resistance (Including Resistor Noise) at 1kHz*

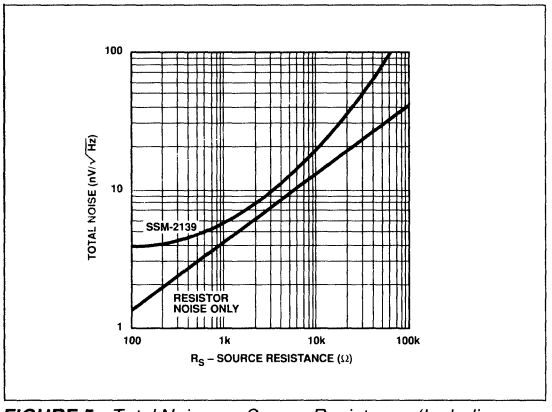


FIGURE 5: *Total Noise vs. Source Resistance (Including Resistor Noise) at 10Hz*

Figure 6 shows peak-to-peak noise versus source resistance over the 0.1Hz to 10Hz range. Once again, at low values of R_S, the voltage noise of the SSM-2139 is the major contributor to peak-to-peak noise with current noise the major contributor as R_S increases.

For reference, typical source resistances of some signal sources are listed in Table 1.

For further information regarding noise calculations, see "Minimization of Noise in Op Amp Applications," Application Note AN-15.

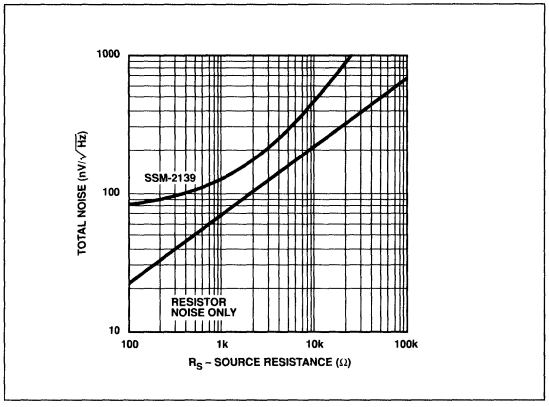


FIGURE 6: *Peak-to-Peak Noise (0.1Hz to 10Hz) vs. Source Resistance (Includes Resistor Noise)*

TABLE 1

DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain Gauge	<500Ω	Typically used in low-frequency applications.
Magnetic Tapehead, Microphone	<1500Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. SSM-2139 I_B can be neglected.
Magnetic Phonograph Cartridge	<1500Ω	Similar need for low I_B in direct coupled applications. SSM-2139 will not introduce any self-magnetization problem.
Linear Variable Differential Transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

NOISE MEASUREMENTS – PEAK-TO-PEAK VOLTAGE NOISE

The circuit of Figure 7 is a test setup for measuring peak-to-peak voltage noise. To measure the 200nV peak-to-peak noise specification of the SSM-2139 in the 0.1Hz to 10Hz range, the following precautions must be observed:

1. The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 2μV due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.
2. For similar reasons, the device has to be well-shielded from air currents. Shielding also minimizes thermocouple effects.

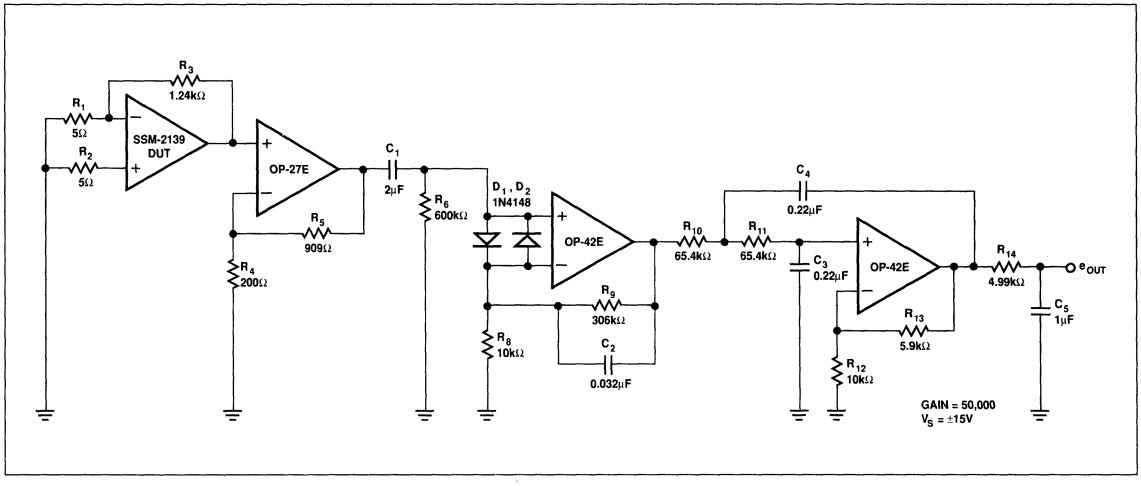


FIGURE 7: *Peak-to-Peak Voltage Noise Test Circuit (0.1Hz to 10Hz)*

3. Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.
4. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve of Figure 8, the 0.1Hz corner is defined by only one pole. The test time of 10 seconds acts as a additional pole to eliminate noise contribution from the frequency band below 0.1Hz.
5. A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.
6. Power should be supplied to the test circuit by well bypassed low-noise supplies, e.g. batteries. These will minimize output noise introduced via the amplifier supply pins.

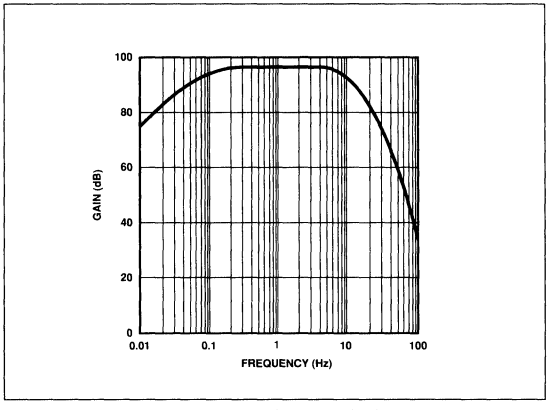
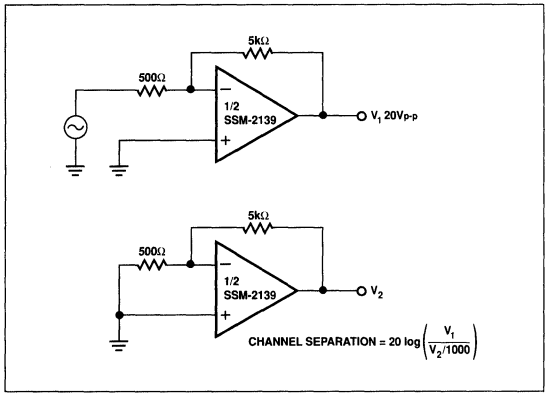


FIGURE 8: *0.1Hz to 10Hz Peak-to-Peak Voltage Noise Test Circuit Frequency Response*

2

CHANNEL SEPARATION TEST CIRCUIT



Audio A/D Converters
Contents

Selection Guide
Audio Analog-to-Digital Converters

Model	Res Bits	Converter Type	Channels	SNR 0 dB–dB typ	THD+N % typ	Input Architecture	Input Range Volts	Supplies Volts	Power mW typ	Pins	Page
AD1876	16	Sampling	Single	No Spec	90[1]	Single-ended	±3 V	±5, ±12	235	16	3-3
AD1879	18	ΣΔ	Dual	103	98	Differential	±3 V	±5	1100	28	3-17
AD1878	16	ΣΔ	Dual	98	98	Differential	±3 V	±5	1100	28	3-15
AD1885	16	ΣΔ	Dual	85	85	Differential	±3 V	±5	500	28	3-19

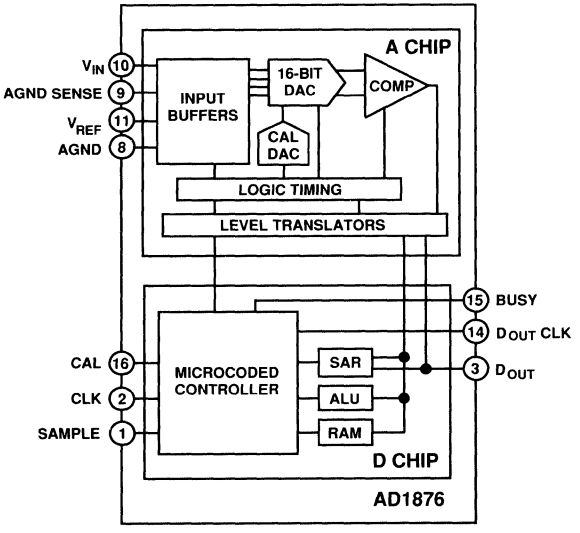
[1]–0.05 dB Input, A-Weighted Filter

16-Bit 100 kSPS Sampling ADC

AD1876

FEATURES
Autocalibrating
0.002% THD
90 dB S/(N+D)
1 MHz Full Power Bandwidth
On-Chip Sample & Hold Function
2× Oversampling for Audio Applications
16-Pin DIP Package
Serial Twos Complement Output Format
Low Input Capacitance—typ 50 pF
AGND Sense for Improved Noise Immunity

FUNCTIONAL BLOCK DIAGRAM



PRODUCTION DESCRIPTION

The AD1876 is a 16-bit serial output sampling A/D converter which uses a switched capacitor/charge redistribution architecture to achieve a 100 kSPS conversion rate (10 μs total conversion time). Overall performance is optimized by digitally correcting internal nonlinearities through on-chip autocalibration.

The circuitry of the AD1876 is partitioned onto two monolithic chips, a digital control chip fabricated with Analog Devices' DSP CMOS process and an analog ADC chip fabricated with the BiMOS II process. Both chips are contained in a single package.

The serial output interface requires an external clock and sample command signal. The output data rate may be as high as 2.08 MHz, and is controlled by the external clock. The twos complement format of the output data is MSB first and is directly compatible with the NPC SM5805 digital decimation filter used in consumer audio products. The AD1876 is also compatible with a variety of DSP processors.

The AD1876 is packaged in a space saving 16-pin plastic DIP and operates from +5 V and ±12 V supplies; typical power consumption is 235 mW. The digital supply (V_{DD}) is isolated from the linear supplies (V_{EE} and V_{CC}) for reduced digital crosstalk. Separate analog and digital grounds are also provided.

AD1876—SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)[1]

Parameter	AD1876J Min	Typ	Max	Units
TEMPERATURE RANGE	0		70	°C
TOTAL HARMONIC DISTORTION (THD)[2]				
−0.05 dB Input		−95	**−88**	dB
		0.002	**0.004**	%
−20 dB Input		−78		dB
		0.01		%
−60 dB Input		−40		dB
		1.0		%
D-RANGE, −60 dB, A-WEIGHTED		92		dB
SIGNAL-TO-NOISE AND DISTORTION (S/(N+D)) RATIO[3]				
−0.05 dB Input, A-Weighted		92		dB
−0.05 dB Input, 48 kHz Bandwidth	**83**	90		dB
−20 dB Input, A-Weighted		73		dB
−20 dB Input, 48 kHz Bandwidth		70		dB
−60 dB Input, A-Weighted		34		dB
−60 dB Input, 48 kHz Bandwidth		31		dB
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		−99	**−89**	dB
INTERMODULATION DISTORTION (IMD)[4]				
2nd Order Products		−102		dB
3rd Order Products		−98		dB
FULL POWER BANDWIDTH		1		MHz
VOLTAGE REFERENCE INPUT RANGE[5] (V_{REF})	3	5	10.0	V
ANALOG INPUT[6]				
Input Range (V_{IN})			$\pm V_{REF}$	V
Input Impedance		*		
Input Capacitance During Sample		50*		pF
Aperture Delay		6		ns
Aperture Jitter		100		ps
POWER SUPPLIES				
Operating Current				
I_{CC}		9	12	mA
I_{EE}		9	12	mA
I_{DD}		3	12	mA
Power Consumption		235	350	mW

NOTES

[1]V_{REF} = 5.00 V; conversion rate = 96 kSPS; f_{IN} = 1.06 kHz; V_{IN} = −0.05 dB unless otherwise indicated. All measurements referred to a 0 dB (10 V_{PP}) input signal. Values are post calibration.

[2]Includes first 19 harmonics.

[3]Minimum value of S/(N+D) corresponds to 5.0 V reference; typical values of S/(N+D) correspond to 10.0 V reference.

[4]f_a = 1008 Hz; f_b = 1055 Hz. See Definition of Specifications section and Figure 14.

[5]See Applications section for recommended voltage reference circuit and Figure 11 for performance with other reference voltage values.

[6]See Applications section for recommended input buffer circuit.

*For explanation of input characteristics, see "Analog Input" section.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all devices at final electrical test at worst case temperature. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

ORDERING GUIDE

Model	Temperature Range	THD dB	Package Description	Package Option*
AD1876JN	0°C to +70°C	−95	Plastic 16-Pin DIP	N-16

*N = Narrow Plastic DIP. For outline information see Package Information section.

DIGITAL SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)

Parameter		Test Conditions	Min	Typ	Max	Units
LOGIC INPUTS						
V_{IH}	High Level Input Voltage		2.4			V
V_{IL}	Low Level Input Voltage		−0.3		0.8	V
I_{IH}	High Level Input Current	$V_{IH} = V_{DD}$	−10		+10	μA
I_{IL}	Low Level Input Current	V_{IL} = 0 V	−10		+10	μA
C_{IN}	Input Capacitance				10	pF
LOGIC OUTPUTS						
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	V_{DD}−1 V			V
		I_{OH} = 0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA			0.4	V

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all devices at final electrical test at worst case temperature. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

3

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to V_{EE} . . . . . −0.3 V to +26.4 V
V_{DD} to DGND . . . . . −0.3 V to +7 V
V_{CC} to AGND . . . . . −0.3 V to +18 V
V_{EE} to AGND . . . . . −18 V to +0.3 V
AGND to DGND . . . . . ±0.3 V
Digital Inputs to DGND . . . . . 0 V to 5.5 V
Analog Inputs, V_{REF} to AGND . . . . . (V_{CC} + 0.3 V) to (V_{EE} −0.3 V)
Soldering . . . . . +300°C, 10 sec
Storage Temperature . . . . . −60°C to +100°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

The AD1876 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD1876 has been classified as a Category 1 Device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment, and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam discharged to the destination socket before devices are removed. For further information on ESD precaution, refer to Analog Devices' *ESD Prevention Manual.*

TIMING SPECIFICATIONS[1] (T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%, V_{REF} = 5.00 V)

Parameter	Symbol	Min	Typ	Max	Units
Sampling Rate[2]	$f_S = 1/t_S$	1		100	kSPS
Sampling Period[2]	$t_S = 1/f_S$	10		1000	μs
Acquisition Time (Included in t_S)	t_A	2			μs
Calibration Time	t_{CT}			5000	t_C
CLK Period	t_C	480			ns
CAL to BUSY Delay	t_{CALB}	0			ns
CLK to BUSY Delay	t_{CB}	50	120	175	ns
CLK to D_{OUT} Hold Time	t_{CD}	10			ns
CLK HIGH	t_{CH}	160			ns
CLK LOW	t_{CL}	50			ns
D_{OUT} CLK LOW	t_{DCL}	30	80	200	ns
SAMPLE LOW to 1st CLK Delay	t_{SC}	50			ns
CAL HIGH Time	t_{CALH}	4			t_C
CLK to D_{OUT} CLK	t_{CDH}	150	200	275	ns
SAMPLE LOW	t_{SL}	50			ns

NOTES
[1]See Figure 1 and Figure 2 and the Conversion Control and Autocalibration sections for detailed explanations of the above timing.
[2]Depends upon external clock frequency; includes acquisition time and conversion time. The minimum sampling rate/maximum sampling period is specified to account for droop of the internal sample/hold. Operation at slower rates than specified may degrade performance.

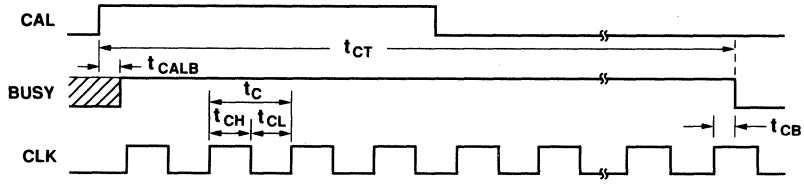


Figure 1. AD1876 Calibration Timing

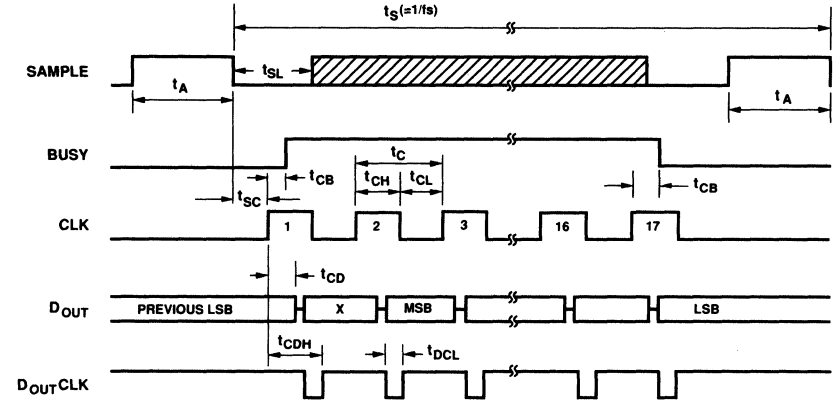


Figure 2. Recommended AD1876 Conversion Timing

Definition of Specifications

NYQUIST FREQUENCY
An implication of the Nyquist sampling theorem, the "Nyquist Frequency" of a converter is that input frequency which is one-half the sampling frequency of the converter.

TOTAL HARMONIC DISTORTION
Total harmonic distortion (THD) is measured as the ratio of the rms sum of the first nineteen harmonic components to the rms value of a 1 kHz full-scale sine wave input signal and is expressed in percent (%) or decibels (dB). For input signals or harmonics that are above the Nyquist frequency, the aliased component is used.

SIGNAL-TO-NOISE PLUS DISTORTION RATIO
Signal-to-noise plus distortion (S/N+D) is defined to be the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

D-RANGE DISTORTION
D-range distortion is the ratio of the distortion plus noise to the signal at a signal amplitude of −60 dB. In this case, an A-weight filter is used. The value specified for D-range performance is the ratio measured plus 60 dB.

BANDWIDTH
The full power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, f_a and f_b, any device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of $mf_a \pm nf_b$, where m, n = 0, 1, 2, 3 . . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are $(f_a + f_b)$ and $(f_a - f_b)$, and the third order terms are $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$ and $(f_a - 2f_b)$. The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude, and the peak value of their sum is −0.05 dB from full scale. The IMD products are normalized to a 0 dB input signal.

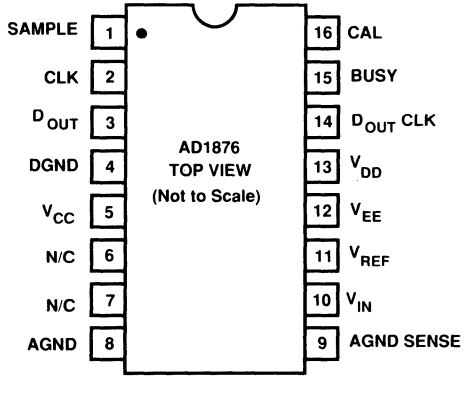
APERTURE DELAY
Aperture delay is the time required after SAMPLE is taken LOW for the internal sample-hold of the AD1876 to open, thus holding the value of V_{IN}.

APERTURE JITTER
Aperature jitter is the variation in the aperture delay from sample to sample.

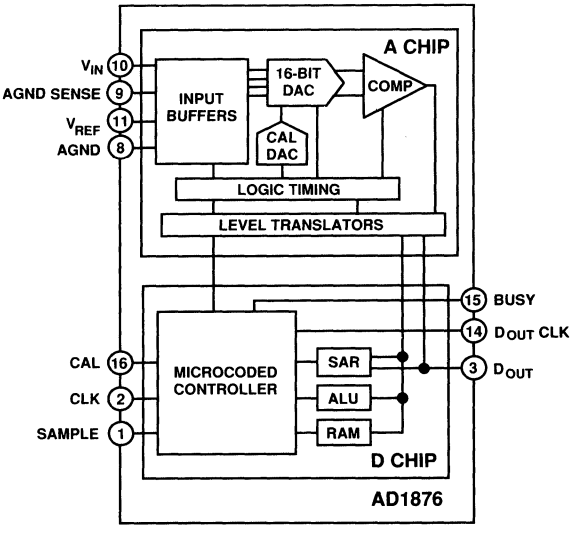
PIN DESCRIPTION

Pin No.	Name	Type	Description
1	SAMPLE	DI	V_{IN} Acquisition Control Pin. During conversion, SAMPLE controls the state of the internal Sample-Hold Amplifier and initiates conversion (see "Conversion Control" paragraph). During calibration, SAMPLE is active HIGH, forcing D_{OUT} (Pin 3) LOW. If SAMPLE is LOW during calibration, D_{OUT} will output diagnostic information (See "Autocalibration" paragraph.)
2	CLK	DI	Master Clock Input. The AD1876 requires 17 clock pulses to execute a conversion. CLK is also used to derive D_{OUT} CLK (Pin 14). During calibration, 5000 clock pulses are applied.
3	D_{OUT}	DO	Serial Output Data, Twos Complement format.
4	DGND	P	Digital Ground.
5	V_{CC}	P	+12 V Analog Supply Voltage.
6	N/C	-	No Connection.
7	N/C	-	No Connection.
8	AGND	P/AI	Analog Ground.
9	AGND SENSE	AI	Analog Ground Sense.
10	V_{IN}	AI	Analog Input Voltage, referred the AGND SENSE.
11	V_{REF}	AI	External Voltage Reference Input, referred to AGND.
12	V_{EE}	P	−12 V Analog Supply Voltage.
13	V_{DD}	P	+5 V Logic Supply Voltage.
14	D_{OUT} CLK	DO	The rising edge of D_{OUT} CLK may be used to latch D_{OUT} (Pin 3). D_{OUT} CLK is derived from CLK.
15	BUSY	DO	Status Line for Converter. Active HIGH, indicating a conversion or calibration in progress.
16	CAL	DI	Calibration Control Pin (asynchronous).

Type: AI = Analog Input.
DI = Digital Input.
DO = Digital Output.
P = Power.



Package Pinout



Functional Block Diagram

FUNCTIONAL DESCRIPTION

The AD1876 is a 16-bit analog-to-digital converter including a sample/hold input circuit, successive approximation register, ground sensing circuitry, serial output port and a microcontroller based autocalibration circuit. These functions are segmented onto two monolithic chips, an analog signal processor and a digital controller. Both chips are contained within the AD1876 package.

The AD1876 employs a successive-approximation technique to determine the value of the analog input voltage. However, instead of the traditional laser-trimmed resistor-ladder approach, the AD1876 uses a capacitor-array, charge-redistribution technique. An array of binary-weighted capacitors subdivides the input value to perform the actual analog to digital conversion. This capacitor array also serves a sample/hold function without the need for additional external circuitry.

The autocalibration circuit within the AD1876 employs a microcontroller and calibration DAC to measure and compensate capacitor mismatch errors. As each error is determined, its value is stored in on-chip memory (RAM). Subsequent conversions use these RAM values to improve conversion accuracy. The autocalibration routine may be invoked at any time. Autocalibration insures high performance while eliminating the need for any user adjustments, and is described in detail below.

The microcontroller controls all of the various functions within the AD1876. These include the actual successive approximation routine, the autocalibration routine, the sample/hold operation, and the serial data transmission.

AUTOCALIBRATION

The AD1876 achieves rated performance without the need for user trims or adjustments. This is accomplished through the use of on-chip autocalibration.

In the autocalibration sequence, sample/hold offset is nulled by internally connecting the input circuit to the ground sense circuit. The resulting offset voltage is measured and stored in RAM for later use. Next, the capacitor representing the most significant bit (MSB) is charged to the reference voltage. This charge is then inverted and shared between the MSB capacitor and one of equal size composed of all the least significant bits. The difference in the summation of the charges in each of the equally sized capacitors represents the amount of capacitor mismatch. A calibration D/A converter (DAC) adds an appropriate value of error correction voltage to cancel the mismatch. This correction factor is also stored in RAM. This process is repeated for each of the capacitors representing the remaining bits. The accumulated values in RAM are then used during subsequent conversions to adjust conversion results.

As shown in Figure 1, when CAL is taken HIGH the AD1876 internal circuitry is reset, the BUSY pin is driven HIGH and the part prepares for calibration. This is a 'hard' reset and will interrupt any conversion or calibration currently in progress. In order to guarantee that all internal undefined states are cleared, the CAL pin should be held HIGH for at least 4 CLK cycles. Actual calibration begins when the CAL pin is taken LOW and completes in less than 5000 clock cycles or about 2.5 msec with a continuous 500 nsec clock.

During calibration the SAMPLE pin adopts an alternative function. If it is held LOW, D_{OUT} provides diagnostic test information (not intended to be used by the customer). If SAMPLE is held HIGH, D_{OUT} will be forced LOW. In either case, D_{OUT} CLK will continue pulsing. Since the SAMPLE pin has no control over the actual calibration process, normal conversion timing may also be used for calibration. In this case, however, the D_{OUT} pin will output test information during those periods that SAMPLE is LOW. BUSY going LOW will always indicate the end of calibration.

A calibration sequence should be followed by one "dummy" conversion to clear the internal circuitry of the AD1876 in order to guarantee subsequent conversion accuracy.

In most applications, it is sufficient to calibrate the AD1876 only upon power-up, in which case care should be taken that the power supplies and voltage reference have stabilized first.

CONVERSION CONTROL

The AD1876 is controlled by two signals: SAMPLE and CLK, as shown in Figure 2. It is assumed that the part has been calibrated and the digital I/O pins have the levels shown at the start of the timing diagram.

A conversion consists of an input acquisition followed by 17 clock pulses which are required to run the 16-bit internal successive approximation routine. The analog input is acquired by taking the SAMPLE line HIGH for a minimum acquisition time of t_A. The actual sample taken is the voltage present on V_{IN} at the instant the SAMPLE pin is brought LOW. Care should be taken to ensure that this negative edge is well defined and jitter free to reduce the uncertainty (noise) in ac signal acquisition. On that edge the AD1876 commits itself to the initiated conversion—the input at V_{IN} is disconnected from the internal capacitor array and the SAMPLE input will be ignored until the conversion is completed (i.e., BUSY goes LOW). After a delay of at least t_{SC} (SAMPLE to CLK setup) the 17 CLK cycles are applied. BUSY is asserted after the first positive edge on CLK and reset after the 17th. Both the D_{OUT} and the D_{OUT} CLK outputs are generated in response to the rising edges of valid CLK pulses. As indicated in the timing diagram, the 2s complement output data is presented MSB first. This data may be captured with the rising edge of D_{OUT} CLK or the falling edge of CLK provided $t_{CH} \geq t_{CDH}$. The AD1876 will ignore CLK after BUSY has gone LOW and not change D_{OUT} or D_{OUT} CLK until a new sample is acquired. SAMPLE will no longer be ignored after BUSY goes LOW, and so an acquisition may be initiated even during the HIGH time of the 17th CLK pulse for maximum throughput rate while enabling full settling of the sample/hold circuitry. Note that if SAMPLE is already HIGH when BUSY goes LOW, then an acquisition is immediately initiated and t_A starts from that time.

During signal acquisition and conversion, care should be taken with the logic inputs to avoid digital feedthrough noise. It is not recommended that CLK be running during V_{IN} sampling. If a continuous CLK is used, then the user must avoid CLK edges at the instant of disconnecting V_{IN}, i.e., the falling edge of SAMPLE (see the t_{SC} specifications). The LOW level time of CLK (t_{CL}) should be at least 100 ns to avoid the negative edge transition disturbing the internal comparator's settling (whose decision is latched on the positive edge of each valid CLK). For the same reason, it is also not recommended that the SAMPLE pin change state during conversion (i.e., until after BUSY returns LOW).

Internal dc error terms such as comparator voltage offset are sampled, stored on internal capacitors and used to correct for their corresponding errors when needed. Because these voltages

are stored on capacitors, they are subject to leakage decay and so require refreshing. For this reason the part is required to be run continuously—i.e., there is a minimum t_S specification. If the part has been idle for too long (i.e., t_S has expired) then a dummy conversion cycle is required to refresh these correction voltages.

BUSY is HIGH during a conversion and goes LOW when the conversion is completed. The twos complement output data is presented MSB first, with MSB data valid on the rising edge of the second D_{OUT} CLK pulse. Subsequent data is valid on rising edges of subsequent D_{OUT} CLK pulses. Table I illustrates the AD1876 output coding.

V_{IN}	Output Code
−Full Scale	100. . . 00
−Full Scale + 1 LSB	100. . . 01
Midscale − 1 LSB	111. . . 11
Midscale	000. . . 00
Midscale + 1 LSB	000. . . .01
Full Scale − 1 LSB	011. . . 10
Full Scale	011. . . 11

Table I. Serial Output Coding Format (Twos Complement)

A simple method for generating the required signals for the AD1876 is to connect one or more AD1876s to an NPC SM5805 digital filter. This device supplies all signals required to operate the AD1876 at a 96 kHz sample rate, which is 2 × F_S for audio applications. This is more fully discussed in the applications section of this data sheet, accompanied by Figures 9 and 10.

APPLICATIONS

POWER SUPPLIES AND DECOUPLING

The AD1876 has three power supply input pins. V_{EE} and V_{CC} provide the supply voltages to operate the analog portions of the AD1876 including the ADC and SHA. V_{DD} provides the supply voltage which operates the digital portions of the AD1876 including the serial output port and the autocalibration controller.

Decoupling capacitors should be used on all power supply pins. These capacitors should be placed as close as possible to the package pins as well as the ground connections. The logic supply (V_{DD}) should be decoupled to digital common (DGND) with a 0.1 μF ceramic capacitor, and the analog supplies (V_{EE} and V_{CC}) should be decoupled to analog common (AGND) with 4.7 μF and 0.1 μF tantalum capacitors in parallel, represented by C1. An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The recommended decoupling scheme is illustrated in Figure 3.

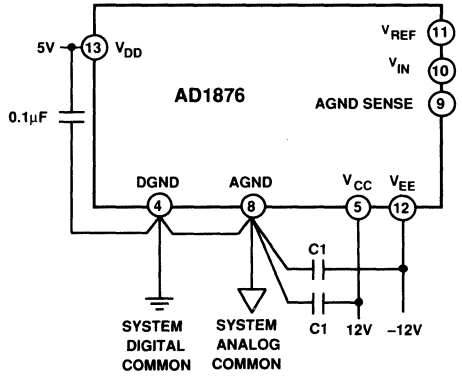


Figure 3. Grounding and Decoupling the AD1876

As with most high performance linear circuits, changes in the power supplies can produce undesired changes in the performance of the circuit. Analog Devices recommends that well regulated power supplies with less than 1% ripple be incorporated into the design of any system using these devices.

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is a significant issue. A 1.22 mA current through a 0.5 Ω trace will develop a voltage drop of 0.6 mV, which is 4 LSBs at the 16 bit level for a 10 V full-scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals. Finally, power supplies need to be decoupled in order to filter ac noise.

Analog and digital signals should not share a common return path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them, if at all, only at right angles. A solid analog ground plane around the AD1876 will isolate large switching ground currents. For these reasons, the use of wire wrap circuit construction is not recommended; careful printed circuit construction is preferred.

GROUNDING

The AD1876 has three grounding pins, designated ANALOG GROUND (AGND), DIGITAL GROUND (DGND) and ANALOG GROUND SENSE (AGND SENSE). The analog ground pin is the "high quality" ground reference point for the device. The analog ground pin should be connected to the analog common point in the system.

AGND SENSE is intended to be connected to the input signal ground reference point. This allows for slight differences in level between the analog ground point in the system and the input signal ground point. However, no more than 100 mV is recommended between the analog ground pin and the analog ground sense pin for specified performance.

The digital ground pin is the reference point for all of the digital signals that operate the AD1876. This pin should be connected to the digital common point in the system. As illustrated in Figure 3, the analog and digital grounds should be connected together at one point in the system.

VOLTAGE REFERENCE

The AD1876 requires the use of an external voltage reference. The input voltage range is determined by the value of the reference voltage; in general, a reference voltage of n volts produces an input range of ±n volts. Signal-to-noise performance is increased proportionately with input signal range. The AD1876 is specified with a 5.0 V reference and an analog input of ±5 V. In the presence of a fixed amount of system noise, increasing the LSB size (which results from increasing the reference voltage) will increase the effective S/(N+D) performance for input values below the point where input distortion occurs. Figure 11 illustrates S/(N+D) as a function of input amplitude and reference voltage.

During a conversion, the switched capacitor array of the AD1876 presents a dynamically changing current load at the voltage reference as the successive-approximation algorithm cycles through various choices of capacitor weighting. The output impedance of the reference circuitry must be low so that the output voltage will remain sufficiently constant as the current drive changes. In most applications, this requires that the output of the voltage reference be buffered by an amplifier with low impedance at relatively high frequencies. A (10 μF or larger) capacitor connected between V_{REF} and AGND will reduce the demands on the reference by decreasing the magnitude of high frequency components.

The following two sections represent typical design approaches.

VOLTAGE REFERENCE—AUDIO APPLICATIONS

Audio applications require optimal ac performance over a relatively narrow temperature range, with low cost being important. Figure 4 shows one such approach towards attaining these goals. A voltage reference, consisting of a Zener diode, capacitor, resistor and op amp with typical component values, is shown. This simple circuit has the advantage of low cost, but the reference voltage value is sensitive to changes in the +12 V supply. Additionally, changes in the Zener value due to temperature variations will also be reflected in the reference voltage. R_{OPTION} may be required for other component selections if the Zener requires more current than the op amp can supply.

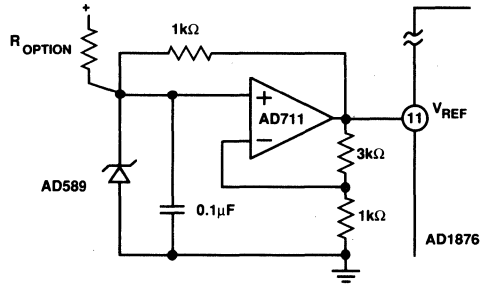


Figure 4. Low Cost Voltage Reference Circuit

VOLTAGE REFERENCE—PRECISION MEASUREMENT APPLICATIONS

In applications other than audio, parameters such as low drift over temperature and static accuracy are important. Figure 5 shows a voltage reference circuit featuring the 5 V AD586. The AD586 is a low cost reference which utilizes a buried Zener architecture to provide low noise and drift. Over the 0°C to +70°C range, the AD586L grade exhibits less than a 2.25 mV output change from its initial value at +25°C. A noise-reduction capacitor, C_N, reduces the broadband noise of the AD586 output, thereby optimizing the overall performance of the AD1876.

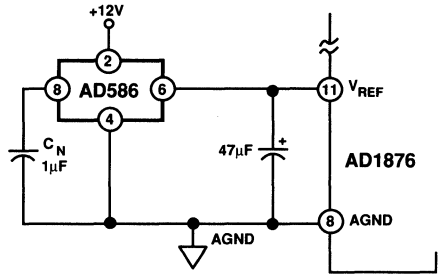


Figure 5.

For higher performance needs, the AD588 reference provides improved drift, low noise, and excellent initial accuracy. The AD588 uses a proprietary ion-implanted buried Zener diode in conjunction with laser-trimmed thin-film resistors for low offset and gain. The AD588 output is accurate to 0.65 mV from its value at +25°C over the 0°C to +70°C range. The circuit shown in Figure 6 includes a noise-reduction network on Pins 4, 6 and 7. The 1 μF capacitors form low pass filters with the internal resistance of the AD588 and external 3.9 kΩ resistor. This reduces the wide-band (to 1 MHz) noise of the AD588, providing optimum performance of the AD1876.

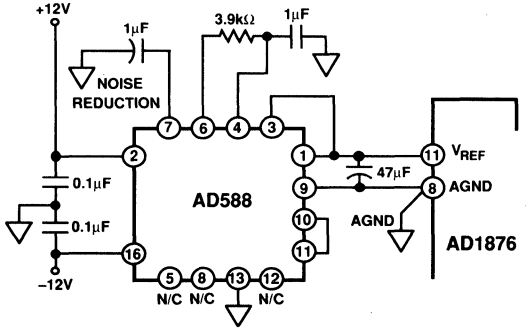


Figure 6.

ANALOG INPUT

As previously discussed, the analog input voltage range for the AD1876 is $\pm V_{REF}$. For purposes of ground drop and common-mode rejection, the V_{IN} and V_{REF} inputs each have their own ground. V_{REF} is referred to the local analog system ground (AGND), and V_{IN} is referred to the analog ground sense pin (AGND SENSE) which allows a remote ground sense for the input signal. If AGND SENSE is not used, it should be connected to the AGND pin at the package. The AGND SENSE pin is intended to be tied to potentials within 100 mV of AGND to maintain specified performance.

The AD1876 analog inputs (V_{IN}, V_{REF} and AGND SENSE) exhibit dynamic characteristics. When a conversion cycle begins, each analog input is connected to an internal, discharged 50 pF capacitor which then charges to the voltage present at the corresponding pin. The capacitor is disconnected when SAMPLE is

taken LOW and the stored charge is used in the subsequent A/D conversion. In order to limit the demands placed on the external source by this high initial charging current, an internal buffer amplifier is employed between the input and this capacitance for a few hundred nanoseconds. During this time the input pin exhibits typically 20 kΩ input resistance, 10 pF input capacitance and ±40 μA bias current. Next, the input is switched directly to the now precharged capacitor and allowed to fully settle, after which SAMPLE is taken LOW. During this time the input sees only a 50 pF capacitor. Once the sample is taken, the input is internally floated so that the external input source sees a very high input resistance and a parasitic input capacitance of typically only 2 pF. As a result, the only dominant input characteristic which must be considered is the high current steps which occur when the internal buffers are switched in and out.

In most cases, it is desirable to use external op amps to drive the AD1876. For ac applications where low cost and low distortion are desired, the AD711 may be used as shown in Figure 7. Another option is the 5532/5534 series. Care should always be taken with op amp selection—many available op amps do not meet the necessary low distortion requirements with even moderate loading conditions.

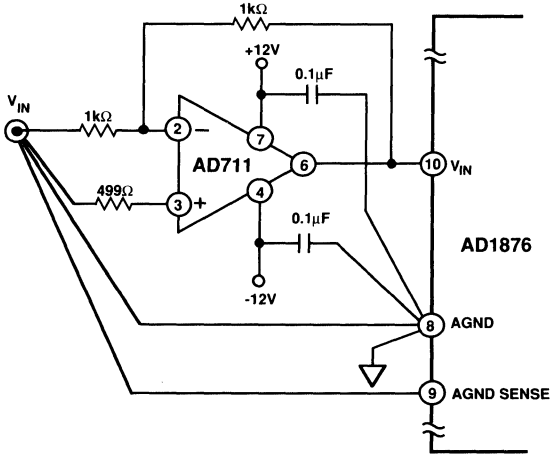


Figure 7.

TESTING THE AD1876

Analog Devices employs a high performance mixed signal VLSI tester to verify the electrical performance of every AD1876. The test system consists of two main sections, an input signal generator and a digital data and control section.

The stimulus section is responsible for providing a high purity, noise-free, band limited tone to the input of the device. This input frequency is 1.06 kHz. The test tone is passed through a bandpass filter to remove distortion products and then buffered by a high performance op amp. An external 5.000 V reference voltage is also supplied by this section.

The control section of the test equipment provides an external clock and the control signals for calibration, conversion and data transmission. This section of the tester also contains the processing unit that calculates the actual performance of the device under test.

The test procedure consists of the following steps. First, the device is calibrated by its on-board controller. Next, the device under test digitizes the input waveform. This conversion is performed at a 96 kSPS rate and transmits the resulting serial data to the tester. The tester performs an FFT on the test data and determines the actual performance of the device.

AC PERFORMANCE

Using the aforementioned test methodology, ac performance of the AD1876 is measured. AC parameters, which include S/(N+D), THD, etc., reflect the AD1876's effect on the spectral content of the analog input signal. Figures 11 through 15 provide information on the AD1876's ac performance under a variety of conditions.

As a general rule, averaging the results from several conversions reduces the effects of noise and, therefore, improves such parameters as S/(N+D) and THD. AD1876 performance is optimized by operating the device at its maximum sample rate of 100 kSPS and digitally filtering the resulting bit stream to the desired signal bandwidth. This succeeds in distributing noise over a wider frequency range, thus reducing the noise density in the frequency band of interest. This subject is discussed in the following section.

OVERSAMPLING AND NOISE FILTERING

The Nyquist rate for a converter is defined as one-half its sampling rate. This is established by the Nyquist theorem, which requires that a signal be sampled at a rate corresponding to at least twice its widest bandwidth of interest in order to preserve the information content. Oversampling is a conversion technique in which the sampling frequency is an integral (2 or more) multiple of twice the frequency bandwidth of interest. In audio applications, the AD1876 can operate at a 2× oversampling rate.

In quantized systems, the information content of the analog input is represented in the frequency spectrum from dc to the Nyquist rate of the converter. Within this same spectrum are higher frequency aliased noise components. Antialias, or low-pass, filters are used at the input to the ADC to remove the portion of these noise components attributed to high frequency analog input noise. However, wideband noise contributed by the AD1876 will not be reduced by the antialias filter. The AD1876 contributed noise is evenly distributed from dc to the Nyquist rate, and this fact can be used to minimize its overall effect.

The AD1876 contributed noise effects can be reduced by oversampling—sampling at a rate higher than defined by the Nyquist theorem. This spreads the noise energy over a distribution of frequencies wider than the frequency band of interest, and by judicious selection of a digital filter, noise frequencies outside the bandwidth of interest may be eliminated. The process of quantization inherently produces noise, known as quantization noise. The magnitude of this noise is a function of the resolution of the converter, and manifests itself as a limit to the theoretical signal-to-noise ratio achievable. This limit is described by $S/(N+D) = (6.02\ n + 1.76 + 10 \log F_S/2\ F_a)$ dB, where n is the resolution of the converter in bits, F_S is the sampling frequency, and F_a is the signal bandwidth of interest. For audio bandwidth applications, the AD1876 is capable of operating at a 2× oversample rate (96 kSPS), which typically produces an improvement in S/(N+D) of 3 dB compared with operating at the Nyquist conversion rate of 48 kSPS. Oversampling has another advantage as well; the demands on the antialias filter are

lessened. In summary, system performance is optimized by running the AD1876 at or near its maximum sampling rate of 100 kHz and digitally filtering the resulting spectrum to eliminate undesired frequencies.

DSP INTERFACE

Figure 8 illustrates the use of the Analog Devices ADSP-2101 digital signal processor with the AD1876. The ADSP-2101 FO (flag out) pin of serial port 1 (SPORT 1) is connected to the SAMPLE line and is used to control acquisition of data. The ADSP-2101 timer is used to provide precise timing of the FO pin.

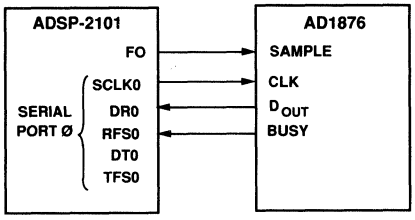


Figure 8. ADSP-2101 Interface

The SCLK pin of the ADSP-2101 SPORT0 provides the CLK input for the AD1876. The clock should be programmed to be approximately 2 MHz to comply with AD1876 specifications. To minimize digital feedthrough, the clock should be disabled (by setting Bit 14 in SPORT0 control register to 0) during data acquisition. Since the clock floats when disabled, a pulldown resistor of 12 k–15 kΩ should be connected to SCLK to ensure it will be LOW at the falling edge of SAMPLE. To maximize the conversion rate, the serial clock should be enabled immediately after SAMPLE is brought LOW (hold mode).

The AD1876 BUSY signal is connected to RF0 to notify SPORT0 when a new data word is coming. SPORT0 should be configured in normal, external, noninverting framing mode and can be programmed to generate an interrupt after the last data bit is received. To maximize the conversion rate, SAMPLE should be brought HIGH immediately after the last data bit is received.

SIGNAL PROCESSING

An audio spectrum analyzer can be produced by combining an AD1876 and an ADSP-2101 signal processing microcomputer. This system can analyze signals from dc to 50 kHz depending on the sample rate. This is ideal for applications such as audio analysis, but could also be applied to vibration analysis as well.

AUDIO DELAY LINE

A high performance, 16-bit stereo delay line can be constructed from two AD1876 audio ADCs, a signal processing microcomputer and two AD1856 audio DACs. Depending on the length of the internal buffer which produces the delay, a variable delay is possible. Other applications are also possible with only a change in software. For example, a reverb or echo effect could be generated as well.

AD1876 AND SM5805 DIGITAL FILTER @ 2 F_S

A simple method for generating the required signals for the AD1876 is to connect one or more AD1876s to an NPC SM5805 digital filter. This device supplies all signals required to operate the AD1876 at a 96 kHz sample rate, which is 2 × F_S for audio applications.

To minimize group delay distortion, the input to the AD1876 is filtered only by a low order analog filter. The AD1876 samples the output of the filter at 2 F_S (96 kHz). To prevent aliasing, the SM5805 filters the data with a sharp, linear phase filter rolling off at 0.5 F_S. The resulting data is decimated to a sample rate of 48 kSPS.

Interfacing the two chips is straight forward, as shown in Figure 9. The start signal for the AD1876 (for 96 kSPS operation) is provided by the S/H pin of the SM5805, and CLK is derived from the BCC pin. Figure 10 illustrates the corresponding timing diagram.

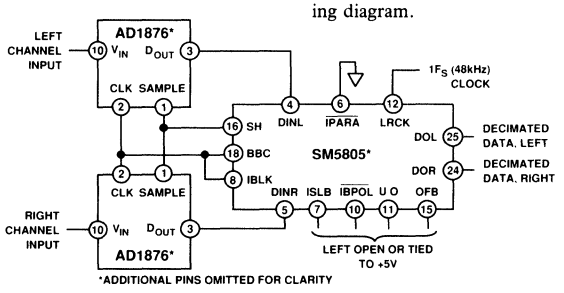


Figure 9. AD1876 and SM5805 Digital Filter

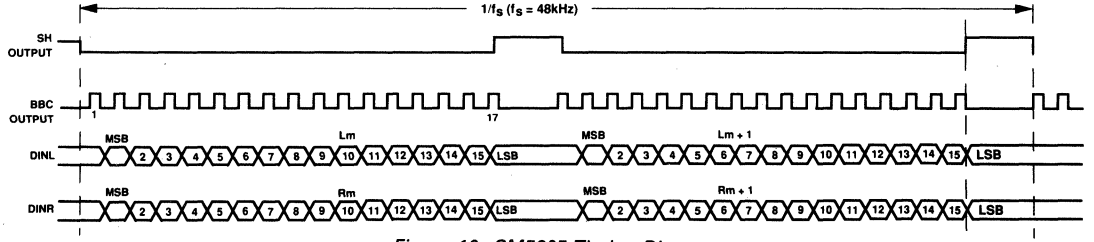


Figure 10. SM5805 Timing Diagram

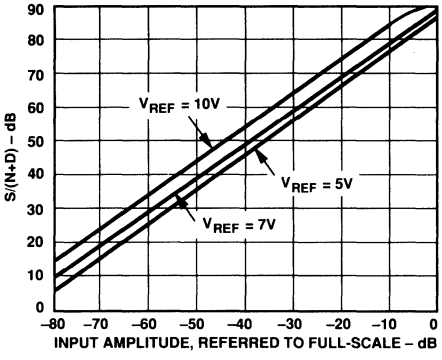


Figure 11. S/(N+D) vs. V_{REF} vs. Input Amplitude

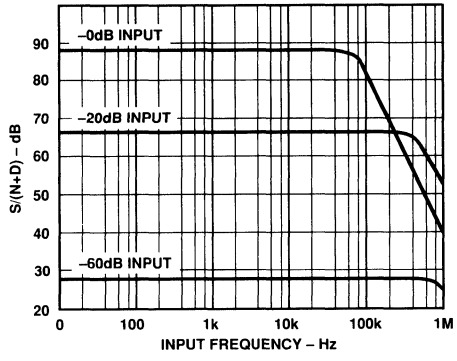


Figure 12. S/(N+D) vs. Input Frequency and Amplitude

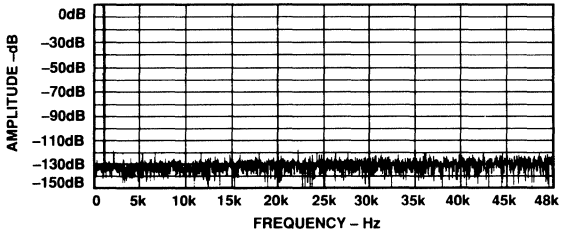


Figure 13. 4096 Point FFT at 96 kSPS, f_{IN} = 1.06 kHz

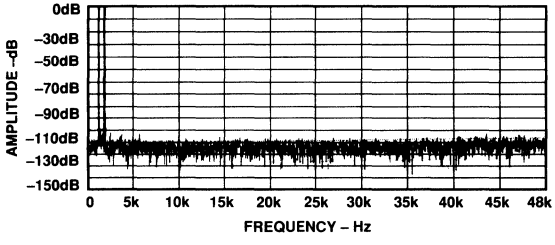


Figure 14. IMD Plot for f_{IN} = 1008 Hz (f_a), 1055 Hz (f_b) at 96 kSPS

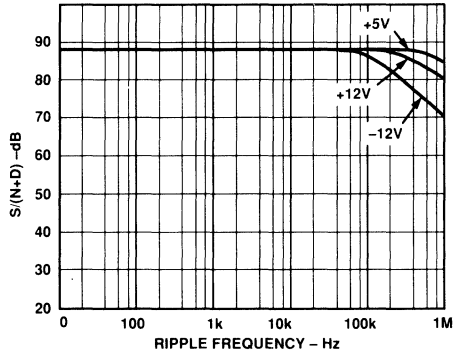


Figure 15. Power Supply Rejection (f_{IN} = 1.06 kHz, f_{SAMPLE} = 96 kSPS, V_{RIPPLE} = 0.3 V p–p)

ANALOG DEVICES

High Performance Stereo 16-Bit Oversampled ADC

AD1878

FEATURES
Dual Channel
98 dB Signal-to-Noise Ratio
98 dB THD+N
0.0004 dB Passband Ripple
115 dB Stopband Attenuation
64× Oversampling
Linear Phase

APPLICATIONS
DAT and DCC Tape Players
Direct-to-Disc Recorders
Digital Audio Editors
Digital Mixing Consoles

PRODUCT DESCRIPTION

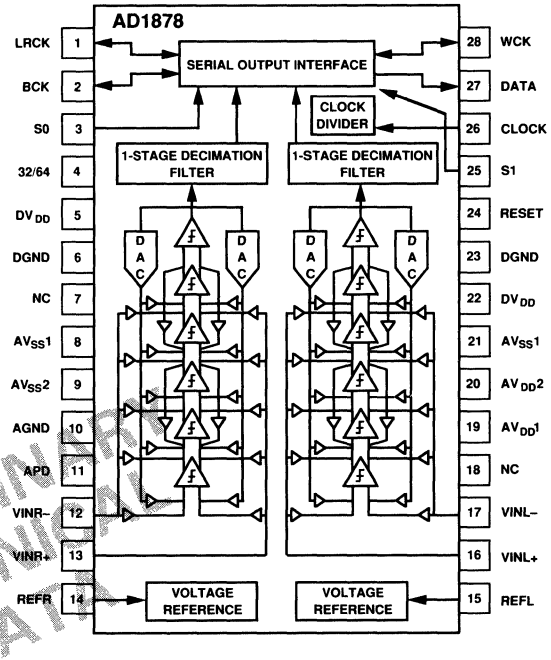
The AD1878 is a two-channel, 16-bit oversampled digital audio ADC. Each channel incorporates a high performance one-bit noise shaping modulator and a digital decimating filter. An on-board voltage reference is also included. ADC output data is transmitted from a flexible serial data port. The circuitry of the AD1878 is segmented between two monolithic chips.

The voltage reference and one-bit modulators are fabricated on a BiCMOS chip. The reference circuitry provides a reference voltage that is stable over temperature and time. Using an external master clock, the one-bit modulators operate at a 64 × F_S oversampling ratio. This oversampling ratio permits the antialias filters to be simple resistor-capacitor combinations and results in linear phase throughout the passband. The modulators are 5th order and employ differential switched capacitor filters to provide the required noise shaping characteristics and extremely low distortion.

The digital decimating filters and serial port are fabricated using a CMOS process. Using a proprietary technique, these single-stage digital filters provide a narrow transition band, deep stopband attenuation and low passband ripple.

The output port provides a single, serial bit stream which can operate in several MASTER or SLAVE modes. It is controlled by a clock and mode select pins. The format of the data is twos complement, MSB first. The output signals are TTL and 5 volt CMOS compatible. Output words may be transmitted in a right-justified, I^2S or user-defined format.

FUNCTIONAL BLOCK DIAGRAM



The AD1878 operates with ±5 volt power supplies. Separate digital and analog power supplies and ground connections are provided for reduced digital crosstalk. The AD1878 is guaranteed to operate over a temperature range of −25°C to +70°C and is packaged in a 28-pin plastic DIP.

PRODUCT HIGHLIGHTS

1. 64 × F_S sampling rate.
2. From 2.5 kHz to 50 kHz output word rates.
3. Passband ripple is less than 0.001 dB.
4. Stopband attenuation is 115 dB.
5. Excellent low level signal performance is achieved.
6. No sample-and-hold circuits are required.

AD1878—SPECIFICATIONS @ ± 5 volt Supplies, T_A = +25°C, Clock = 12.288 MHz

Parameter	Target	Units
RESOLUTION	18	Bits
OVERSAMPLING RATIO	64	× F_S
DYNAMIC RANGE, 0 kHz to 20 kHz, No A-Weight Filter		
Stereo Mode[1]	98	dB
Mono Mode[2]	101	dB
SIGNAL TO (NOISE + DISTORTION)		
0 dB, 1 kHz	98	dB
−20 dB, 1 kHz	85	dB
−60 dB, 1 kHz	45	dB
ANALOG INPUTS		
Input Range	±3	V
Input Impedance	12.8	kΩ
REFERENCE OUTPUT		
Output Voltage	3	V
Output Impedance	TBD	
DC ACCURACY		
Gain Matching	TBD	dB
Gain Error	TBD	%
Gain Drift	TBD	ppm/°C
Midscale Error	20	LSBs
Midscale Drift	TBD	ppm/°C
PHASE DEVIATION (Interchannel)	Below Measurable Limit	Degrees
CROSSTALK		
20 kHz, EIAJ Method	105	dB
DIGITAL FILTER CHARACTERISTICS		
Passband Ripple	0.001	dB
Stopband Attenuation	115	dB
12.288 MHz Master Clock[4]		
Passband Edge	21.7	kHz
Stopband Edge	26.2	kHz
11.2896 MHz Clock[5]		
Passband Edge	20	kHz
Stopband Edge	24.1	kHz
DIGITAL INPUTS AND OUTPUTS		
V_{IH}	2.0	V
V_{IL}	0.8	V
I_{IH} @ V_{IH} = 5 V	10	μA
I_{IL} @ V_{IL} = 0 V	10	μA
V_{OH} @ I_{OH} = 4 mA	4.5	V
V_{OL} @ I_{OL} = 4 mA	0.5	V
NOMINAL MASTER CLOCK FREQUENCY	12.288	MHz
POWER SUPPLIES		
Voltage, $+V_L$ and $+V_S$	5	V
Voltage, $-V_L$ and $-V_S$	−5	V
Current, $+I_L$ and $+I_S$	TBD	mA
Current, $-I_L$ and $-I_S$	TBD	mA
POWER DISSIPATION		
Operation	900	mW
Power Down APD = "1"	400	mW
POWER SUPPLY REJECTION RATIO	67	dB
TEMPERATURE RANGE		
Specification	25	°C
Operation	−25 to +70	°C
Storage	−60 to +100	°C

NOTES
[1]Stereo Mode uses output of each channel independently.
[2]Mono Mode sums output words to derive higher Dynamic Range.
[3]16-bit LSBs.
[4]Master Clock Frequency for 48 kHz sample rate.
[5]Master Clock Frequency for 44.1 kHz sample rate.
Specifications subject to change without notice.

High Performance Stereo 18-Bit Oversampled ADC

AD1879

FEATURES
Dual Channel
103 dB Signal-to-Noise Ratio
98 dB THD+N
0.0004 dB Passband Ripple
115 dB Stopband Attenuation
64× Oversampling
Linear Phase

APPLICATIONS
Pro Audio Digital Tape Recorders
Direct-to-Disc Recorders
Digital Audio Editors
Digital Mixing Consoles

PRODUCT DESCRIPTION

The AD1879 is a two-channel, 18-bit oversampled digital audio ADC. Each channel incorporates a high performance one-bit noise shaping modulator and a digital decimating filter. An on-board voltage reference is also included. ADC output data is transmitted from a flexible serial data port. The circuitry of the AD1879 is segmented between two monolithic chips.

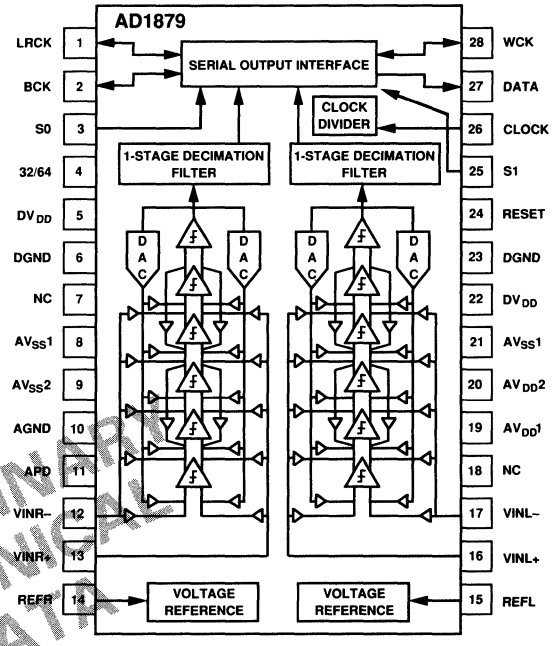
The voltage reference and one-bit modulators are fabricated on a BiCMOS chip. The reference circuitry provides a reference voltage that is stable over temperature and time. Using an external master clock, the one-bit modulators operate at a 64 × F_S oversampling ratio. This oversampling ratio permits the antialias filters to be simple resistor-capacitor combinations and results in linear phase throughout the passband. The modulators are 5th order and employ differential switched capacitor filters to provide the required noise shaping characteristics and extremely low distortion.

The digital decimating filters and serial port are fabricated using a CMOS process. Using a proprietary technique, these single-stage digital filters provide a narrow transition band, deep stopband attenuation and low passband ripple.

The output port provides a single, serial bit stream which can operate in several MASTER or SLAVE modes. It is controlled by clock and mode select pins. The format of the data is twos complement, MSB first. The output signals are TTL and 5 volt CMOS compatible. Output words may be transmitted in a right-justified, I^2S or user-defined format.

The AD1879 operates with ±5 volt power supplies. Separate digital and analog power supplies and ground connections are provided for reduced digital crosstalk. The AD1879 is guaranteed to operate over a temperature range of −25°C to +70°C and is packaged in a 28-pin plastic DIP.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. 64 × F_S sampling rate.
2. Passband ripple is less than 0.001 dB.
3. Stopband attenuation is 115 dB.
4. Excellent low level signal performance is achieved.
5. No sample-and-hold circuits are required.
6. Fully differential analog inputs.
7. Extremely flexible serial data output port.

AD1879—SPECIFICATIONS @ ±5 V Supplies, T_A = 25°C, Clock = 12.288 MHz

Parameter	Target	Units
RESOLUTION	18	Bits
OVERSAMPLING RATIO	64	× F_S
DYNAMIC RANGE, 0 kHz to 20 kHz, No A-Weight Filter		
Stereo Mode[1]	103	dB
Mono Mode[2]	106	dB
SIGNAL TO (NOISE + DISTORTION)		
0 dB, 1 kHz	98	dB
−20 dB, 1 kHz	85	dB
−60 dB, 1 kHz	45	dB
ANALOG INPUTS		
Input Range	±3	V
Input Impedance	12.8	kΩ
REFERENCE OUTPUT		
Output Voltage	3	V
Output Impedance	TBD	
DC ACCURACY		
Gain Matching	TBD	dB
Gain Error	TBD	%
Gain Drift	TBD	ppm/°C
Midscale Error	20	LSBs
Midscale Drift	TBD	ppm/°C
PHASE DEVIATION (Interchannel)	Below Measurable Limit	Degrees
CROSSTALK		
20 kHz, EIAJ Method	105	dB
DIGITAL FILTER CHARACTERISTICS		
Passband Ripple	0.001	dB
Stopband Attenuation	115	dB
12.288 MHz Master Clock[4]		
Passband Edge	21.7	kHz
Stopband Edge	26.2	kHz
11.2896 MHz Clock[5]		
Passband Edge	20	kHz
Stopband Edge	24.1	kHz
DIGITAL INPUTS AND OUTPUTS		
V_{IH}	2.0	V
V_{IL}	0.8	V
I_{IH} @ V_{IH} = 5 V	10	μA
I_{IL} @ V_{IL} = 0 V	10	μA
V_{OH} @ I_{OH} = 4 mA	4.5	V
V_{OL} @ I_{OL} = 4 mA	0.5	V
NOMINAL MASTER CLOCK FREQUENCY	12.288	MHz
POWER SUPPLIES		
Voltage, $+V_L$ and $+V_S$	5	V
Voltage, $-V_L$ and $-V_S$	−5	V
Current, $+I_L$ and $+I_S$	TBD	mA
Current, $-I_L$ and $-I_S$	TBD	mA
POWER DISSIPATION		
Operation	900	mW
Power Down APD = "1"	400	mW
POWER SUPPLY REJECTION RATIO	67	dB
TEMPERATURE RANGE		
Specification	25	°C
Operation	−25 to +70	°C
Storage	−60 to +100	°C

NOTES
[1]Stereo mode uses output of each channel independently.
[2]Mono mode sums output words to derive higher dynamic range.
[3]16-bit LSBs.
[4]Master Clock Frequency for 48 kHz sample rate.
[5]Master Clock Frequency for 44.1 kHz sample rate.
Specifications subject to change without notice.

Low-Cost Stereo 16-Bit Oversampled ADC

AD1885

FEATURES
Dual Channel
85 dB Signal-to-Noise Ratio
85 dB THD+N
±0.01 dB Passband Ripple
80 dB Stopband Attenuation
64 Times Oversampling
Linear Phase

APPLICATIONS
RDAT Machines
High Performance Sampling Keyboards
Multimedia Workstations

PRODUCT DESCRIPTION

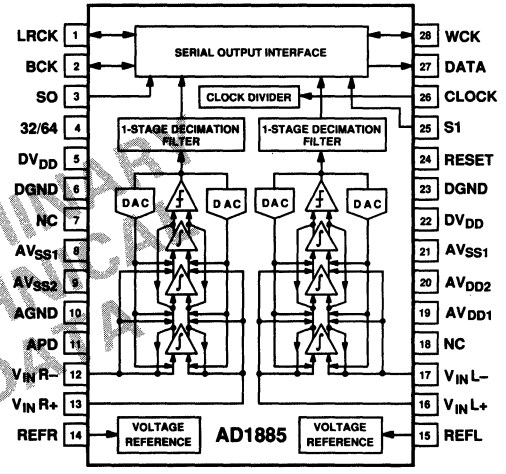
The AD1885 is a two-channel, 16-bit oversampled Digital Audio ADC. Each channel incorporates a high performance one-bit noise-shaping modulator and a digital decimating filter. An on-board voltage reference is also included. ADC output data is transmitted from a flexible serial data port. The circuitry of the AD1885 is segmented between two monolithic chips.

The reference circuitry provides a reference voltage that is stable over temperature and time. Using an external master clock, the one-bit modulator operates at 64 × F_S oversampling rate. This oversampling rate permits the antialias filters to be simple resistor-capacitor combinations and results in linear phase throughout the passband. The third-order modulators employ differential switched capacitor filters to provide the required noise-shaping characteristics and extremely low distortion.

The digital decimating filters and serial port are fabricated using a CMOS process. Using a proprietary technique, these single-stage digital filters provide a narrow transition band, deep stopband attentuation and low passband ripple.

The output port provides right and left channel data in a single, serial bit stream controlled by user-supplied BCK, LRCK and WCK signals. The twos complement, MSB first data can be transmitted in a right-justified, left-justified or user-defined format.

FUNCTIONAL BLOCK DIAGRAM



NC = NO CONNECT

The AD1885 operates with ±5 V power supplies. Separate digital and analog ground connections are provided for reduced digital crosstalk. The AD1885 is guaranteed to operate over a temperature range of −25°C to +70°C. The AD1885 is packaged in a 28-pin plastic SOIC.

PRODUCT HIGHLIGHTS

1. 64 × F_S sampling rate.
2. 44.1, 48 and 32 kHz output word rates.
3. Passband ripple is less than ±0.01 dB.
4. Stopband attenuation is 80 dB.
5. Excellent low-level performance.
6. No sample-and-hold circuits are required.
7. Analog inputs are fully differential.
8. Serial data output port.

AD1885—SPECIFICATIONS (@ ±5 V Supplies, T_A = +25°C, Clock = 18 × 432 MHz (= 384 ×48 kHz))

Parameter	Target	Unit
RESOLUTION	16	Bits
OVERSAMPLING RATIO	64	× F_S
DYNAMIC RANGE, 0 to 20 kHz, NO A-WEIGHT FILTER		
Stereo Mode[1]	85	dB
THD+N (SIGNAL TO (NOISE + DISTORTION))		
0 dB, 1 kHz	85	dB
−20 dB, 1 kHz	TBD	dB
−60 dB, 1 kHz	TBD	dB
ANALOG INPUTS		
Input Range	±3	V
Input Impedance	30	kΩ
REFERENCE OUTPUT		
Output Voltage	3	V
Output Impedance	TBD	
DC ACCURACY		
Gain Matching	TBD	dB
Gain Error	TBD	%
Gain Drift	TBD	ppm/°C
Midscale Error	TBD	LSBs[2]
Midscale Drift	TBD	ppm/°C
PHASE DEVIATION (INTERCHANNEL)	TBD	Degrees
CROSSTALK		
20 kHz, EIAJ Method	90	dB
DIGITAL FILTER CHARACTERISTICS		
Passband Ripple	±0.01	dB
Stopband Attenuation	80	dB
18.432 MHz Master Clock[3] (= 384 × 48 kHz)		
Passband Edge	21.6	kHz
Stopband Edge	26.4	kHz
16.9344 MHz Master Clock[4] (= 384 × 44.1 kHz)		
Passband Edge	19.8	kHz
Stopband Edge	24.3	kHz
DIGITAL INPUT AND OUTPUTS		
V_{IH}	2.0	V
V_{IL}	0.8	V
I_{IH} @ V_{IH} = 5 V	10	µA
I_{IL} @ V_{IL} = 0 V	10	µA
V_{OH} @ I_{OH} = 4 mA	4.5	V
V_{OL} @ I_{OL} = 4 mA	0.5	V
MASTER CLOCK FREQUENCY	18.432	MHz
POWER SUPPLIES		
Voltage, AVDD1 and AVDD2	5	V
Voltage, AVSS1 and AVSS2	−5	V
Current, $+I_L$ and I_S	TBD	mA
Current, $-I_L$ and $-I_S$	TBD	mA
POWER DISSIPATION		
Operation	500	mW
Power Down APD = "1"	375	mW
POWER SUPPLY REJECTION RATIO (IN BAND)	50	dB
TEMPERATURE RANGE		
Specification	+25	°C
Operation	−25 to +70	°C
Storage	−60 to +100	°C

NOTES
[1]Stereo mode uses output of each channel.
[2]16-bit LSBs.
[3]Master Clock Frequency for 48 kHz sample rate.
[4] Master Clock Frequency for 44.1 kHz sample rate.
Specifications subject to change without notice.

Video A/D Converters
Contents

4

Selection Guide
Video Analog-to-Digital Converters

Model	Res Bits	Sample Rate (MSPS)	Input Bandwidth MHz, −3 dB	Power Dissipation W	Page	Comments
AD9048	8	35	15	0.55	4-31	
					4-31	
					4-31	
					4-31	
AD773	10	18	100	1.3	4-3	On-Board Track and Hold, Evaluation PCB
AD9020	10	60	175	2.8	4-19	Evaluation PCB
					4-19	
AD9060	10	75	175	2.8	4-39	Evaluation PCB
					4-39	

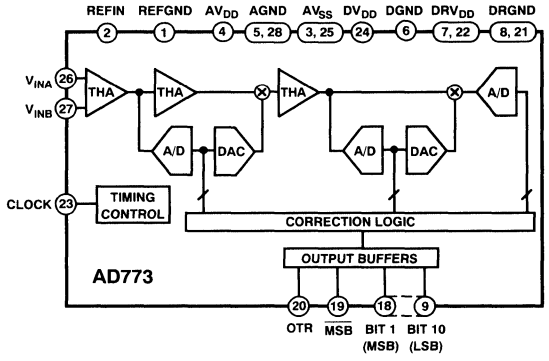
10-Bit 18 MSPS Monolithic A/D Converter

AD773

FEATURES

Monolithic 10-Bit 18 MSPS A/D Converter
Low Power Dissipation: 1.2 W
Signal-to-Noise Plus Distortion Ratio
f_{IN} = 1 MHz: 55 dB
f_{IN} = 8 MHz: 52 dB
Guaranteed No Missing Codes
On-Chip Track-and-Hold Amplifier
100 MHz Full Power Bandwidth
High Impedance Reference Input
Out of Range Output
Twos Complement and Binary Output Data
Available in Commercial and Military Temperature Ranges

FUNCTIONAL BLOCK DIAGRAM



4

PRODUCT DESCRIPTION

The AD773 is a monolithic 10-bit, 18 MSPS analog-to-digital converter incorporating an on-board, high performance track-and-hold amplifier (THA). The AD773 converts video bandwidth signals without the use of an external THA. The AD773 implements a multistage differential pipelined architecture with output error correction logic. The AD773 offers accurate performance and guarantees no missing codes over the full operating temperature range.

Output data is presented in binary and twos complement format. An out of range (OTR) signal indicates the analog input voltage is beyond the specified input range. OTR can be decoded with the MSB/$\overline{\text{MSB}}$ pins to signal an underflow or overflow condition. The high impedance reference input allows multiple AD773s to be driven in parallel from a single reference.

The combined dc precision and dynamic performance of the AD773 is useful in a variety of applications. Typical applications include: video enhancement, HDTV, ghost cancellation, ultrasound imaging, radar and high speed data acquisition.

The AD773 was designed using Analog Devices' ABCMOS-1 process which utilizes high speed bipolar and 2-micron CMOS transistors on a single chip. High speed, precision analog circuits are now combined with high density logic circuits. Laser trimmed thin film resistors are used to optimize accuracy and temperature stability.

The AD773 is packaged in a 28-pin ceramic DIP and is available in commercial (0°C to +70°C) and military (−55°C to +125°C) grades.

PRODUCT HIGHLIGHTS

1. On-board THA
   The high impedance differential input THA eliminates the need for external buffering or sample and hold amplifiers. The THA offers the choice of differential or single-ended inputs. Input current is typically 5 μA.
2. High Impedance Reference Input
   The high impedance reference input (200 kΩ) allows direct connection with standard +2.5 V references, such as the AD680, AD580 and REF43.
3. Output Data Flexibility
   Output data is available in bipolar offset and bipolar twos complement binary format.
4. Out of Range (OTR)
   The OTR output bit indicates when the input signal is beyond the AD773's input range.

AD773—SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5 V ± 5%, AV_{SS} = −5 V ± 5%, DV_{DD} = +5 V ± 5%, DRV_{DD} = +5 V ± 5%, V_{REF} = +2.500 V unless otherwise indicated)

Parameter	AD773J Min	AD773J Typ	AD773J Max	AD773K Min	AD773K Typ	AD773K Max	Units
RESOLUTION	10			10			Bits
DC ACCURACY (+25°C)							
Integral Nonlinearity							LSB
T_{MIN} to T_{MAX}		±1			±0.75	±2	LSB
Differential Linearity Error							LSB
T_{MIN} to T_{MAX}		±1			±0.75	±1	LSB
Offset		0.5			0.5	3.5	% FSR
Gain Error		0.5			0.5	2.0	% FSR
No Missing Codes					GUARANTEED		
ANALOG INPUT							
Input Range		1			1		V p–p
Input Current		5	20		5	20	μA
Input Capacitance			10			10	pF
REFERENCE INPUT							
Reference Input Resistance	50	200		50	200		kΩ
Reference Input		2.5			2.5		Volts
LOGIC INPUT							
High Level Input Voltage	+3.5			+3.5			V
Low Level Input Voltage			+1.0			+1.0	V
High Level Input Current (V_{IN} = DV_{DD})	−10		+10	−10		+10	μA
Low Level Input Current (V_{IN} = 0 V)	−10		+10	−10		+10	μA
Input Capacitance		10			10		pF
LOGIC OUTPUTS							
High Level Output Voltage (I_{OH} = 0.5 mA)	+2.4			+2.4			V
Low Level Output Voltage (I_{OL} = 1.6 mA)			+0.4			+0.4	V
POWER SUPPLIES							
Operating Voltages							
AV_{DD}	+4.75		+5.25	+4.75		+5.25	Volts
AV_{SS}	−5.25		−4.75	−5.25		−4.75	Volts
DV_{DD}, DRV_{DD}	+4.75		+5.25	+4.75		+5.25	Volts
Operating Current							
IAV_{DD}		85	100		85	100	mA
IAV_{SS}		−140	−185		−140	−185	mA
IDV_{DD}		15	20		15	20	mA
$IDRV_{DD}$[1]		10	15		10	15	mA
POWER CONSUMPTION[2]		1.2	1.5		1.2	1.5	W
POWER SUPPLY REJECTION		6	16		6	16	mV/V
TEMPERATURE RANGE							
Specified (J/K)	0		+70	0		+70	°C

NOTES
[1] C_L = 15 pF typical.
[2] 100% production tested.

Specifications subject to change without notice. See Definition of Specifications for additional information.

AC SPECIFICATIONS

(T_{MIN} to T_{MAX} with AV_{DD} = +5 V ± 5%, AV_{SS} = −5 V ± 5%, DV_{DD} = +5 V ± 5%, DRV_{DD} = +5 V ± 5%, V_{REF} = +2.500 V unless otherwise indicated, f_{SAMPLE} = 18 MSPS, f_{IN} amplitude = −0.3 dB)

Parameter	AD773J Min	AD773J Typ	AD773J Max	AD773K Min	AD773K Typ	AD773K Max	Units
DYNAMIC PERFORMANCE[1]							
Signal-to-Noise plus Distortion (S/N+D) Ratio							
f_{IN} = 1 MHz	52	56		54	56		dB
f_{IN} = 8.1 MHz	45	53		47	53		dB
f_{IN} = 9 MHz		53			53		dB
Effective Number of Bits (ENOB)							
f_{IN} = 1 MHz		9.0			9.0		Bits
f_{IN} = 8.1 MHz		8.5			8.5		Bits
f_{IN} = 9 MHz		8.5			8.5		Bits
Total Harmonic Distortion (THD)							
f_{IN} = 1 MHz		−64	−57		−64	−59	dB
f_{IN} = 8.1 MHz		−55	−46		−55	−48	dB
f_{IN} = 9 MHz		−56			−56		dB
Spurious Free Dynamic Range[2]		−67			−67		dB
Full Power Bandwidth		100			100		MHz
Intermodulation Distortion (IMD)[3]							
Second Order Products		−69			−69		dB
Third Order Products		−63			−63		dB
Differential Phase		0.2			0.2		Degree
Differential Gain		0.8			0.8		%
Transient Response		25			25		ns
Overvoltage Recovery Time		25			25		ns

NOTES
[1]For typical dynamic performance curves at f_{SAMPLE} = 16.2 MSPS and 18 MSPS, see Figures 2 through 13.
[2]f_{IN} = 1 MHz.
[3]fa = 1.0 MHz, fb = 1.05 MHz.
Specifications subject to change without notice.

TIMING SPECIFICATIONS

(for all grades T_{MIN} to T_{MAX} with AV_{DD} = +5 V ± 5%, AV_{SS} = −5 V ± 5%, DV_{DD} = +5 V ± 5%, DRV_{DD} = +5 V ± 5%, V_{REF} = +2.500 V unless otherwise indicated, f_{SAMPLE} = 18 MSPS)

	Symbol	Min	Typ	Max	Units
Conversion Rate				18	MSPS
Clock Period	t_{CLK}	55			ns
Clock High	t_{CH}	27			ns
Clock Low	t_{CL}	27			ns
Output Delay	t_{OD}		20		ns
Aperture Delay			7		ns
Aperture Jitter			9	32	ps
Pipeline Delay (Latency)				4	Clock Cycles

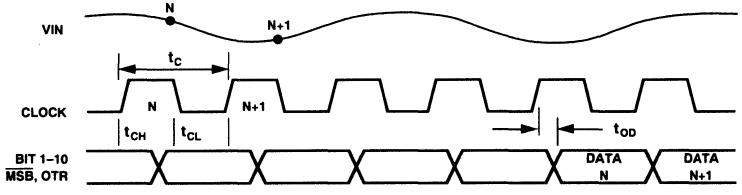


Figure 1. AD773 Timing Diagram

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AV_{DD}	AGND	−0.5	+6.5	V
AV_{SS}	AGND	−6.5	+0.5	V
DV_{DD}, DRV_{DD}	DGND, DRGND	−0.5	+6.5	V
AGND	DGND, DRGND	−1.0	+1.0	V
AV_{DD}, AV_{SS}	DV_{DD}, DRV_{DD}	−6.5	+0.5	V
CLK	DV_{DD}, DRV_{DD}	−6.5	+0.5	V
REFIN	REFGND, AGND	−0.5	+6.5	V
Junction Temperature			+150	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec)			+300	°C

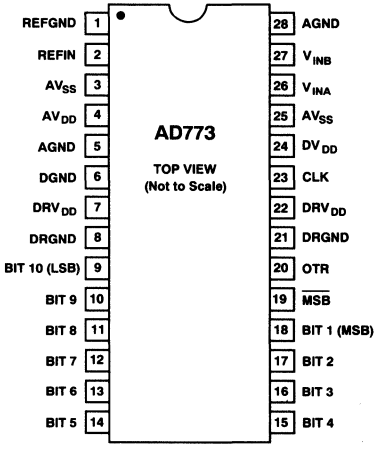
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Description	Package Option*
AD773JD	0°C to +70°C	28-Pin Ceramic DIP	D-28
AD773KD	0°C to +70°C	28-Pin Ceramic DIP	D-28

*D = Ceramic DIP. For outline information see Package Information section.

PIN CONFIGURATION



PIN DESCRIPTION

Symbol	Pin No.	Type	Name and Function
AGND	5, 28	P	Analog Ground.
AV_{DD}	4	P	+5 V Analog Supply.
AV_{SS}	3, 25	P	−5 V Analog Supply.
BIT 1 (MSB)	18	DO	Most Significant Bit.
BIT 2–BIT 9	17–10	DO	Data Bit 2 through Data Bit 9.
BIT 10 (LSB)	9	DO	Least Significant Bit.
CLK	23	DI	Clock Input. The AD773 will initiate a conversion on the falling edge of the clock input. See the Timing Diagram for details.
DV_{DD}	24	P	+5 V Digital Supply.
DRV_{DD}	7, 22	P	+5 V Digital Supply for the output drivers.
DGND	6	P	Digital Ground.
DRGND	8, 21	P	Digital Ground for the output drivers.
$\overline{MSB}$	19	DO	Inverted Most Significant Bit. Provides twos complement output data format.
OTR	20	DO	Out of Range is Active HIGH on the leading edge of Code 0 or the trailing edge of Code 1023. See Output Data Format Table II.
REF GND	1	AI	REF GND is connected to the ground of the external reference.
REF IN	2	AI	REF IN is the external 2.5 V reference input, taken with respect to REF GND.
V_{INA}	26	AI	(+) Analog input signal to the differential input THA.
V_{INB}	27	AI	(−) Analog input signal to the differential input THA.

Type: AI = Analog Input; DI = Digital Input; DO = Digital Output; P = Power.

INTEGRAL NONLINEARITY (INL)
Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale." The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line.

DIFFERENTIAL LINEARITY ERROR (DNL, NO MISSING CODES)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value.

OFFSET
The first transition should occur at a level 1/2 LSB above "zero." Offset is defined as the deviation of the actual first code transition from that point.

GAIN ERROR
The last code transition should occur for an analog value 1 1/2 LSB below the nominal full scale. The gain error is the deviation of the actual level at the last transition from the ideal level.

POWER SUPPLY REJECTION
One of the effects of power supply variation on the performance of the device will be a change in gain error. The specification shows the maximum gain error deviation as the supplies are varied from their nominal values to their specified limits.

SIGNAL-TO-NOISE PLUS DISTORTION (S/N+D) RATIO
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

EFFECTIVE NUMBER OF BITS (ENOB)
ENOB is calculated from the following expression:

S/N+D = 6.02N + 1.76, where N is equal to the effective number of bits.

TOTAL HARMONIC DISTORTION (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

SPURIOUS FREE DYNAMIC RANGE
The peak spurious or peak harmonic component is the largest spectral component excluding the input signal and dc. This value is expressed in decibels relative to the rms value of a full-scale input signal.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of mfa±nfb, where m, n = 0, 1, 2, 3 . . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa+fb) and (fa−fb) and the third order terms are (2fa+fb), (2fa−fb), (fa+2fb) and (fa−2fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals are of equal amplitude and the peak value of their sums is −0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

DIFFERENTIAL GAIN
The percentage difference between the output amplitudes of a small high frequency sine wave at two stated levels of a low frequency signal on which it is superimposed.

DIFFERENTIAL PHASE
The difference in the output phase of a small high frequency sine wave at two stated levels of a low frequency signal on which it is superimposed.

TRANSIENT RESPONSE
The time required for the AD773 to achieve its rated accuracy after a full-scale step function is applied to its input.

OVERVOLTAGE RECOVERY TIME
The time required for the ADC to recover to full accuracy after an analog input signal 150% of full scale is reduced to 50% of the full-scale value.

APERTURE DELAY
The difference between the switch delay and the analog delay of the THA. This effective delay represents the point in time, relative to the rising edge of the CLOCK input, that the analog input is sampled.

APERTURE JITTER
The variations in aperture delay for successive samples.

PIPELINE DELAY (LATENCY)
The number of clock cycles between conversion initiation and the associated output data being made available. New output data is provided every clock cycle.

FULL POWER BANDWIDTH
The input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

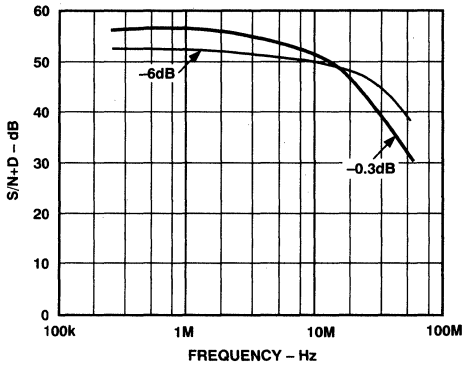


Figure 2. S/N+D vs. Input Frequency, f_{CLK} = 18 MSPS

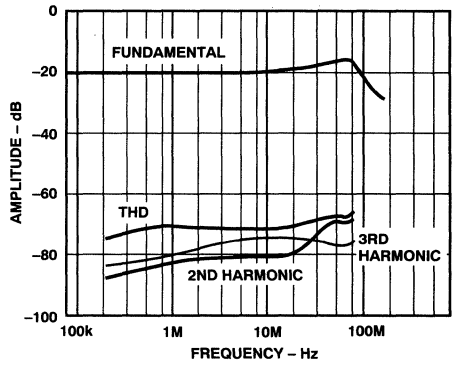


Figure 5. Harmonic Distortion vs. Input Frequency, f_{CLK} = 18 MSPS: Small Signal

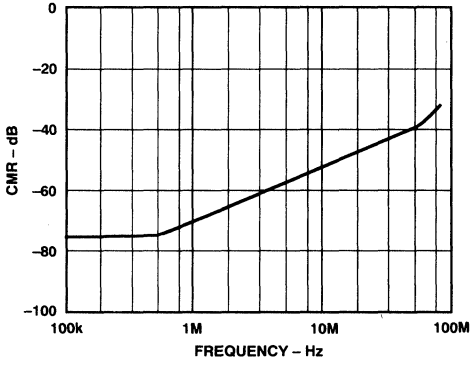


Figure 3. CMR vs. Input Frequency f_{CLK} = 18 MSPS

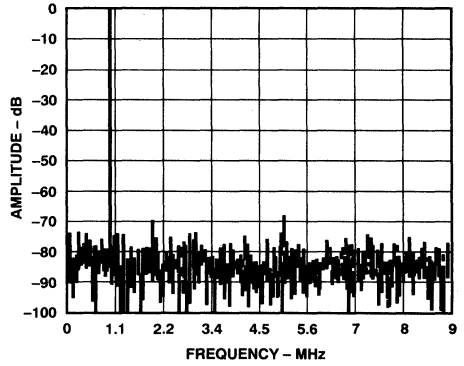


Figure 6. Typical FFT Plot of AD773, f_{CLK} = 18 MSPS, f_{IN} = 1 MHz at 1 V p–p

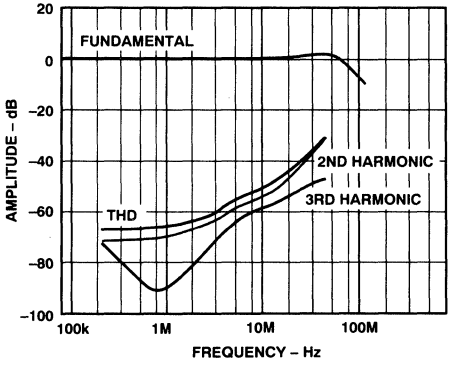


Figure 4. Harmonic Distortion vs. Input Frequency, f_{CLK} = 18 MSPS: Full Power

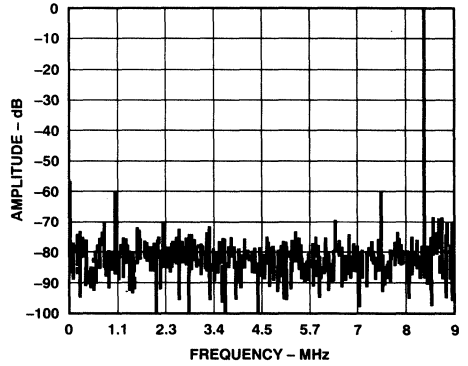


Figure 7. Typical FFT Plot of AD773, f_{CLK} = 18 MSPS, f_{IN} = 8.5 MHz at 1 V p–p

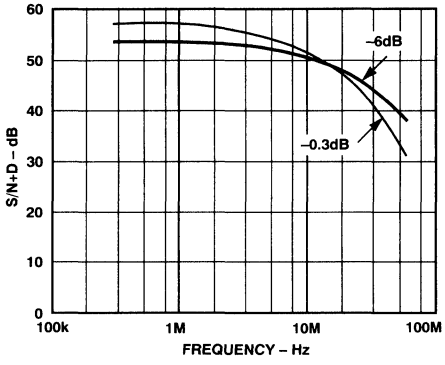


Figure 8. S/N+D vs. Input Frequency, f_{CLK} = 16.2 MSPS

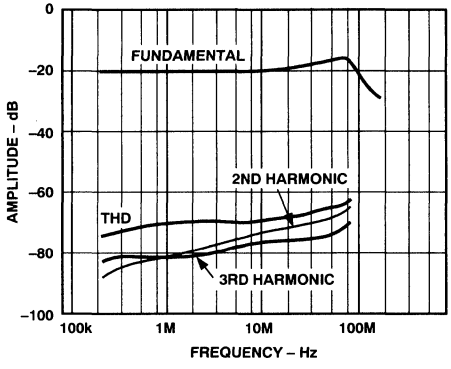


Figure 11. Harmonic Distortion vs. Input Frequency, f_{CLK} = 16.2 MSPS: Small Signal

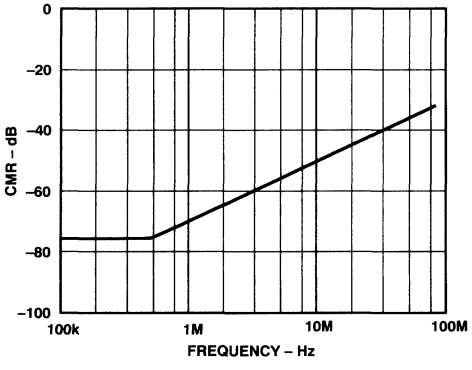


Figure 9. CMR vs. Input Frequency, f_{CLK} = 16.2 MSPS

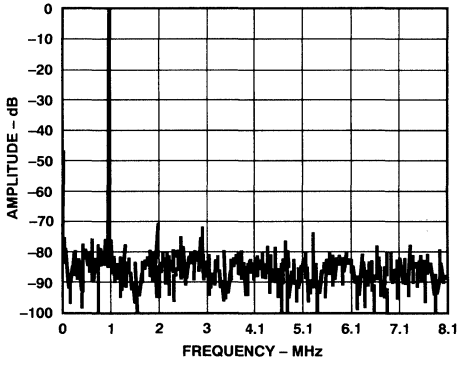


Figure 12. Typical FFT Plot of AD773, f_{CLK} = 16.2 MHz, f_{IN} = 1 MHz at 1 V p–p

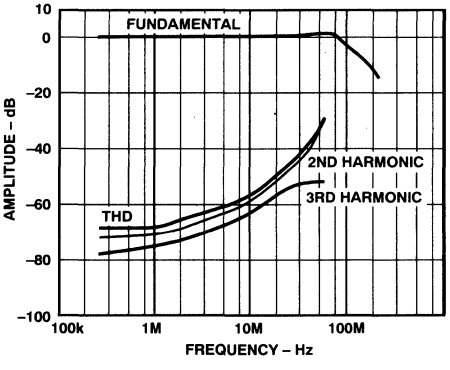


Figure 10. Harmonic Distortion vs. Input Frequency, f_{CLK} = 16.2 MSPS: Full Power

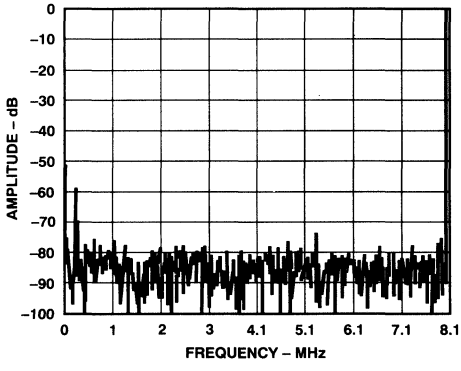


Figure 13. Typical FFT Plot of AD773, f_{CLK} = 16.2 MHz, f_{IN} = 8.05 MHz at 1 V p–p

Theory of Operation

The AD773 uses a pipelined multistage architecture with a differential input, fast settling track-and-hold amplifier (THA). Traditionally, high speed ADCs have used parallel, or flash architectures. When compared to flash converters, multistage architectures reduce the power dissipation and die size by reducing the number of comparators. For example, the AD773 uses 48 comparators compared to 1023 comparators for a 10-bit flash architecture.

The AD773's main signal path transmits differential current mode signals. Low impedance current summing techniques are employed, increasing speed by reducing sensitivity to parasitic capacitances. Pipelining allows the stages to operate concurrently and maximizes system throughput.

The input THA is followed by three 4-bit conversion stages. At any given time, the first stage operates on the most recent sample, while the second stage operates on a signal dependent on the previous sample. This process continues throughout all three stages. The twelve digital bits provided by the three 4-bit stages are combined in the correction logic to produce a 10-bit representation of the sampled analog input.

Pipeline delay, or latency, is four clock cycles. New output data is provided every clock cycle and is provided in both binary and twos complement format. The AD773 will flag an out-of-range condition when the analog input exceeds the specified analog input range.

Applying the AD773

DRIVING THE AD773 INPUT

The AD773 may be driven in a single-ended or differential fashion. V_{INA} is the positive input, and V_{INB} is the negative input. In the signle-ended configuration either V_{INA} or V_{INB} is connected to Analog Ground (AGND) while the other input is driven with a full-scale input of ±500 mV p–p. An inverted mode of operation can be achieved by simply interchanging the input connections.

Both inputs of the AD773, V_{INA} and V_{INB}, are high impedance and do not need to be driven by a low impedance source. Note, however, that as the source impedance increases, the input node becomes more susceptible to noise. The increased noise at the input will degrade performance. A 10 pF capacitor across V_{INA} and V_{INB} as shown in Figure 14 is recommended to bypass high frequency noise.

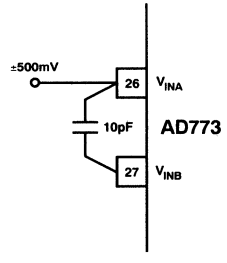


Figure 14. AD773 Single-Ended Input Connection

INPUT CONDITIONING

In some cases, it may be appropriate to buffer the input source, add dc offset, or otherwise condition the input signal of the AD773. Choosing an appropriate op amp will vary with system requirements and the desired level of performance. Some suggested op amps are the AD9617, AD842, and AD827.

Figure 15 shows a typical application where a unipolar signal is level shifted to the bipolar input range of the AD773. Note that the reference used with the AD773 can also provide a noise-free voltage source to generate the dc offset.

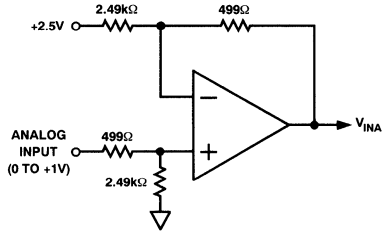


Figure 15. Unipolar to Bipolar Input Connection

DIFFERENTIAL INPUT CONNECTIONS

Operating the AD773 with fully differential inputs offers the advantage of rejecting common-mode signals present on both V_{INA} and V_{INB}. The full-scale input range of V_{INA} and V_{INB} when driven differentially is ±250 mV p–p as shown in Table I.

Table I. AD773's Maximum Differential Input Voltage

V_{INA}	V_{INB}	V_{INA}–V_{INB}
+250 mV	−250 mV	+500 mV
−250 mV	+250 mV	−500 mV

In some applications it may be desirable to convert a single-ended signal to a differential signal before being applied to the AD773. Figure 16 shows a single-ended to differential video line driver capable of driving doubly terminated cables.

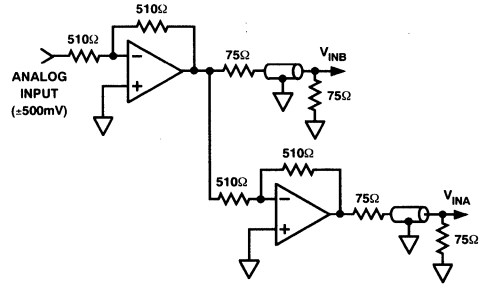


Figure 16. Single-Ended to Differential Connection

REFERENCE INPUT

The AD773's high impedance reference input allows direct connection with standard voltage references. Unlike the resistor ladder requirements of a flash converter the AD773's single pin, high impedance input can be driven from one low cost, low power reference. The high impedance input allows multiple AD773's to be driven from one reference thus minimizing drift errors.

Figure 17 shows the AD773 connected to the AD680. The AD680 is a single supply, low power, low cost 2.5 V reference with performance specifications ideally suited for the AD773. The low pass filter minimizes the AD680's wideband noise. Other recommended 2.5 V references are the AD580 and REF43.

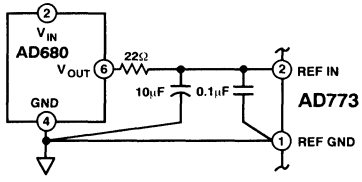


Figure 17. Recommended AD773 to AD680 Connection

CLOCK INPUT

The AD773's pipelined architecture operates on both the rising and falling edges of the clock input. A low jitter, symmetrical clock will provide the highest level of performance. The recommended logic families to drive the clock input are HC and F. The AD773's minimum clock half cycle may necessitate the use of an external divide-by-two circuit as shown in Figure 18. Power dissipation will vary with input clock frequency. Figure 19 shows the AD773's power dissipation vs. input clock frequency.

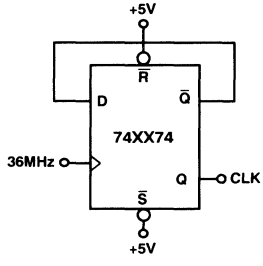


Figure 18. Divide-by-Two Clock Circuit

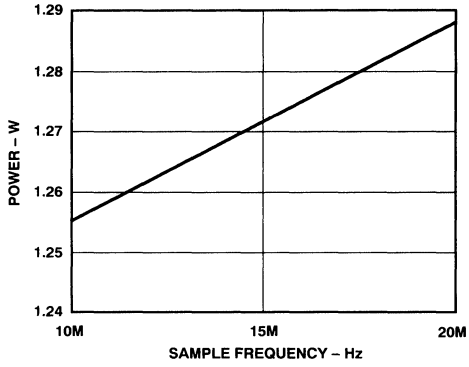


Figure 19. Power Dissipation vs. Sample Frequency

EQUIVALENT ANALOG INPUT CIRCUIT

The AD773 equivalent analog input circuit is shown in Figure 20. The typical input bias current is 5 μA, while input capacitance is typically 5 pF. In the single-ended input configuration one input is connected to AGND while the second input is driven to full scale (±500 mV). Under nominal conditions the collector of the input transistor is at +1.15 V. This allows signals to be offset by up to +0.65 V without significantly degrading performance. In the negative direction, the emitter of the input transistor should not drop below −1.25 V. Therefore, signals can be offset by −0.65 V without significant performance degradation. Figure 21 shows signal-to-noise ratio vs. common-mode input voltage.

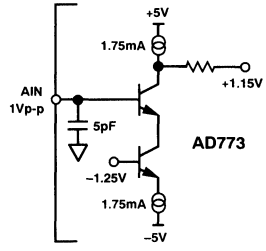


Figure 20. Equivalent Analog Input Circuit

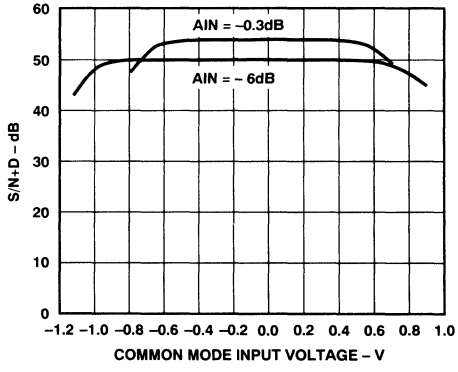


Figure 21. S/N+D vs. Common-Mode Input Voltage, f_{CLK} = 18 MSPS

EQUIVALENT REFERENCE INPUT CIRCUIT

The AD773 is designed to have a reference to analog input voltage ratio of 2.5:1. When the AD773 is configured for single-ended operation a 2.5 volt reference input establishes a full-scale analog input voltage of 1 V p–p (±500 mV with respect to V_{INB}). Although the AD773 is specified and tested with V_{REF} equal to 2.5 V and V_{IN} equal to ±500 mV the reference input voltage and analog input voltages can be changed. To optimize the AD773's performance the 2.5:1 ratio should be maintained. The simplified model of the AD773's reference input circuit is shown in Figure 22.

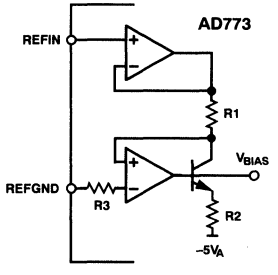


Figure 22. Typical Reference Input Circuit

The 2.5 V external reference is applied across resistor R1 producing a current which in turn generates a voltage V_{BIAS}. Multiple reference currents are generated from V_{BIAS} and are used throughout the converter. R3 is used to cancel errors induced by the input bias current of the REFGND buffer. Figure 23 shows the SNR performance as the reference voltage is varied from its nominal value of 2.5 V. The input full-scale voltage is defined by the following equation,

$$\textit{Input Full-Scale Voltage} = \frac{\textit{Reference Voltage}}{2.5}$$

The power dissipation is modulated by variations in the reference voltage. Figure 24 shows the variation in power dissipation versus reference voltage.

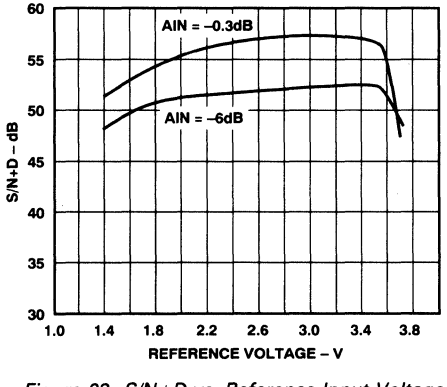


Figure 23. S/N+D vs. Reference Input Voltage, f_{CLK} = 18 MSPS, f_{IN} = 1 MHz

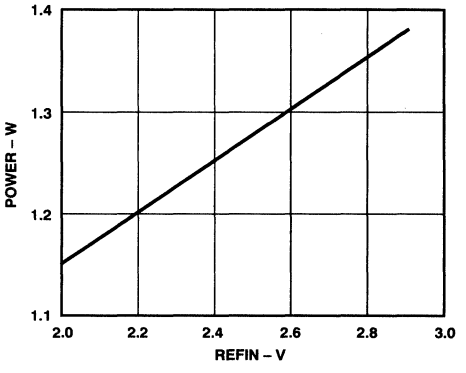


Figure 24. Power Dissipation vs. Reference Input Voltage

TRANSIENT RESPONSE

The fast settling input THA accurately converts full-scale input voltage swings in under one clock cycle. The THA's high impedance, fast slewing performance is critical in multiplexed or dc stepped (charge coupled devices, infrared detectors) systems. Figure 25 show the AD773's settling performance with an input signal stepped from −500 mV to 0V. As can be seen, the output code settles to its final value in under one clock cycle.

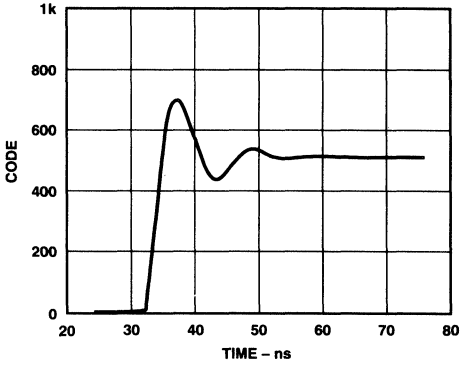


Figure 25. Typical AD773 Settling Time

OUTPUT DATA FORMAT

The AD773 provides both MSB and $\overline{MSB}$ outputs, delivering positive true offset binary and twos complement output data. Table II shows the AD773's output data format.

Table II. Output Data Format

Analog Input	Digital Output		
V_{INA}–V_{INB}	Offset Binary	Twos Complement	OTR
≥499.5 mV	11 1111 1111	01 1111 1111	1
499 mV	11 1111 1111	01 1111 1111	0
0 mV	10 0000 0000	00 0000 0000	0
−500 mV	00 0000 0000	10 0000 0000	0
≤−500.5 mV	00 0000 0000	10 0000 0000	1

OUT OF RANGE

An out-of-range condition exists when the analog input voltage is beyond the input range (±500 mV) of the converter. [Note the AD773 has a 4 clock cycle latency rating.] OTR (Pin 20) is set low when the analog input voltage is within the analog input range. OTR is set HIGH and will remain HIGH when the analog input voltage exceeds the input range by 1/2 LSB from the center of the ± full-scale output codes. OTR will remain HIGH until the analog input is within the input range. By logical ANDing OTR with the MSB and its complement, overrange high or underrange low conditions can be detected. Table III is a truth table for the over/under range circuit in Figure 26. Systems requiring programmable gain conditioning prior to the AD773 can immediately detect an out of range condition, thus eliminating gain selection iterations.

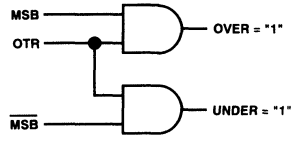


Figure 26. Overrange or Underrange Logic

Table III. Out-of-Range Truth Table

OTR	MSB	ANALOG INPUT IS
0	0	In Range
0	1	In Range
1	0	Underrange
1	1	Overrange

GROUNDING AND LAYOUT RULES

As is the case for any high performance device, proper grounding and layout techniques are essential in achieving optimal performance. The analog and digital grounds on the AD773 have been separated to optimize the management of return currents in a system. It is recommended that a 4-layer printed circuit board (PCB) which employs ground planes and power planes be used with the AD773. The use of ground and power planes offers distinct advantages:

1. The minimization of the loop area encompassed by a signal and its return path.
2. The minimization of the impedance associated with ground and power paths.
3. The inherent distributed capacitor formed by the power plane, PCB insulation, and ground plane.

These characteristics result in both a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

It is important to design a layout which prevents noise from coupling onto the input signal. The wide input bandwidth of the AD773 permits noise outside the desired Nyquist bandwidth to be digitized along with the desired signal. This can result in a higher overall level of spurious noise in the digitized spectrum. Digital signals should not be run in parallel with the input signal traces and should be routed away from the input circuitry. It is also suggested that the traces associated with V_{INA} and V_{INB} be the same length.

Separate analog and digital ground should be joined together directly under the AD773 (see Figure 30). A solid ground plane under the AD773 is also acceptable if care is taken in the management of the power and ground return currents. A general "rule-of-thumb" for mixed signal layouts dictate that the return currents from digital circuitry should not pass through critical analog circuitry.

POWER SUPPLY DECOUPLING

The analog and digitals supplies of the AD773 have been separated to prevent the typically large transients associated with digital circuitry from coupling into the analog supplies (AV_{DD}, AV_{SS}). Each power supply pin should be decoupled with a 0.1 μF capacitor located as close to the pin as possible. Additional 0.1 μF capacitors in parallel with the DRV_{DD} and DDV_{DD} bypass capacitors are required to adequately suppress high frequency noise. For optimal performance, surface-mount capacitors are recommended. The inductance associated with the leads of through-hole ceramic capacitors typically render them ineffective at higher frequencies. A *complete* system will also incorporate tantalum capacitors in the 10–100 μF range to decouple low frequency noise and ferrite beads to limit high frequency noise.

The digital supplies have additionally been separated into DRV_{DD} and DV_{DD}. The DRV_{DD} pins provide power for the digital output drivers of the AD773 and are likely to contain high energy transients. Pin 22 should be decoupled directly to Pin 21 (DRGND) and Pin 7 should be decoupled directly to Pin 8 (DRGND) to minimize the length of the return path for these transients. A single +5 V supply is all that is required for DRV_{DD} and DV_{DD}, but decoupling DV_{DD} with an RC filter network is suggested (see Figure 27).

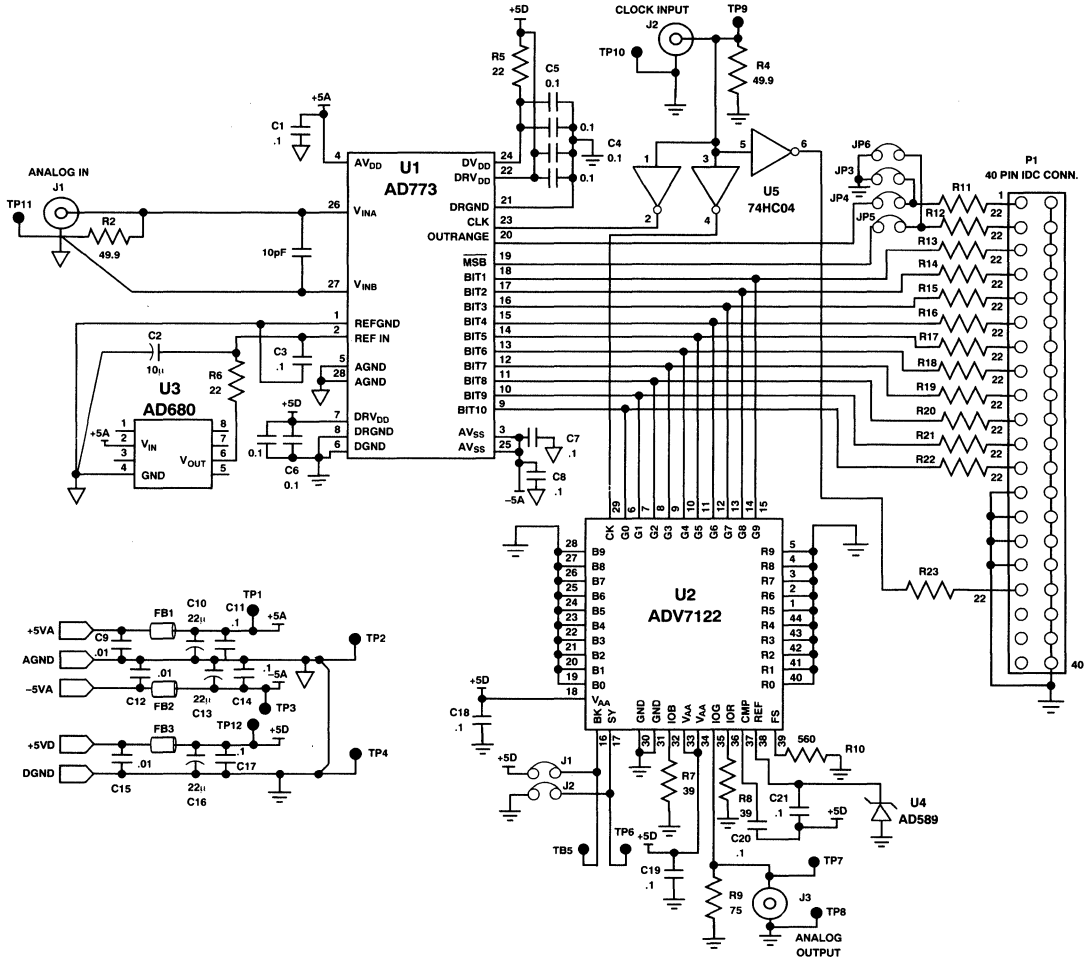


Figure 27. AD773 Evaluation Board Schematic

Table IV. Components List

Reference Designator	Description	Quantity
R2, R4	Resistor, 1%, 49.9 Ω	2
R5, R6, R11–R22	Resistor, 5%, 22 Ω	14
R7, R8	Resistor, 5%, 39 Ω	2
R9	Resistor, 5%, 75 Ω	1
R10	Resistor, 5%, 560 Ω	1
C1, C3–C8, C11, C14, C17–C21	Chip Cap, 0.1 μF	14
C2	Capacitor, Tantalum, 10 μF	1
C9, C12, C15	Chip Cap, 0.01 μF	3
C10, C13, C16	Capacitor, Tantalum, 22 μF	3
U1	AD773	1
U2	ADV7122	1
U3	AD680	1
U4	AD589	1
U5	74AS04	1
FB1–FB3	Ferrite Bead	3

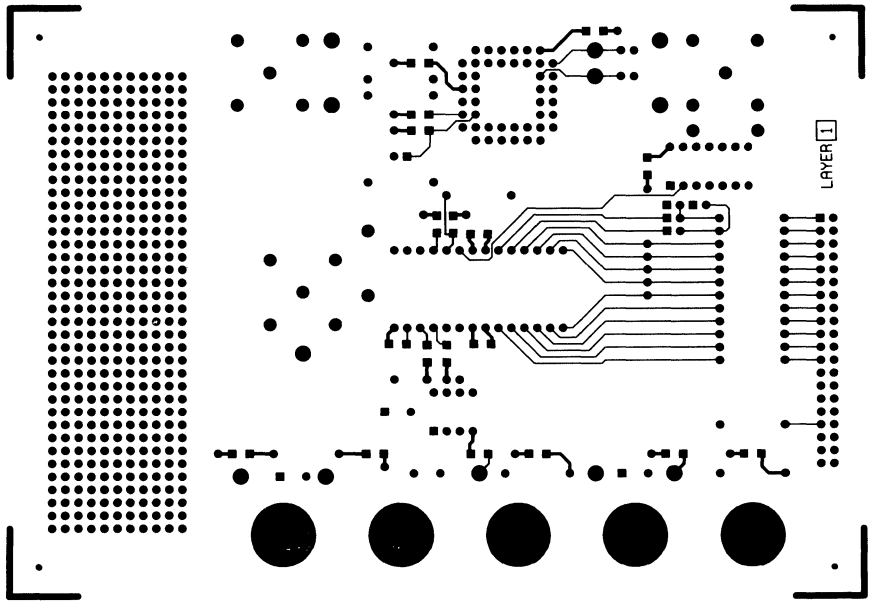


Figure 28. Component Side PCB Layout

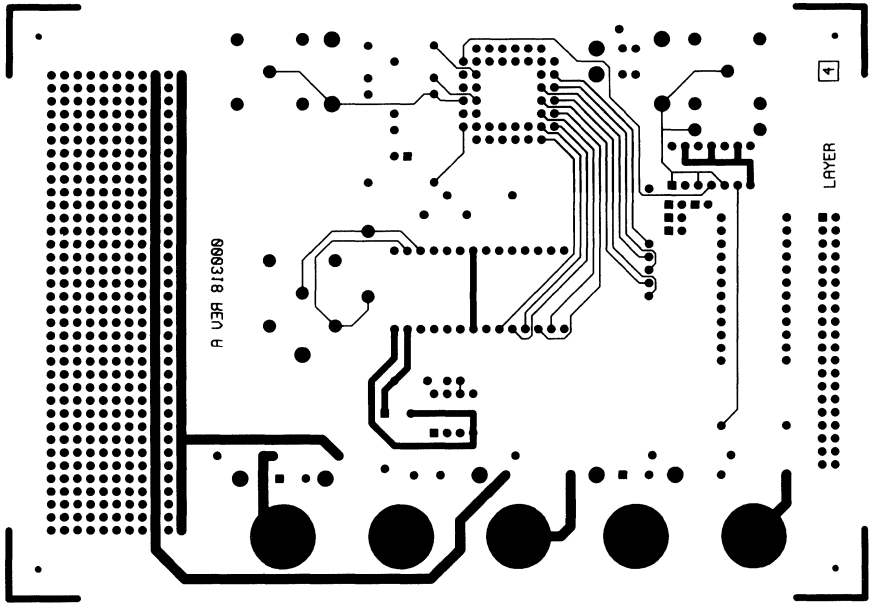


Figure 29. Solder Side PCB Layout

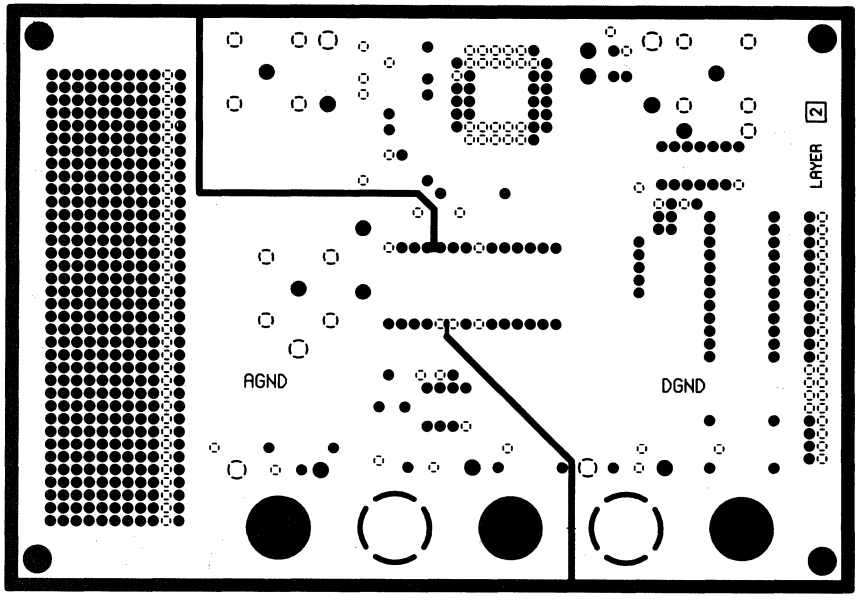


Figure 30. Ground Layer PCB Layout

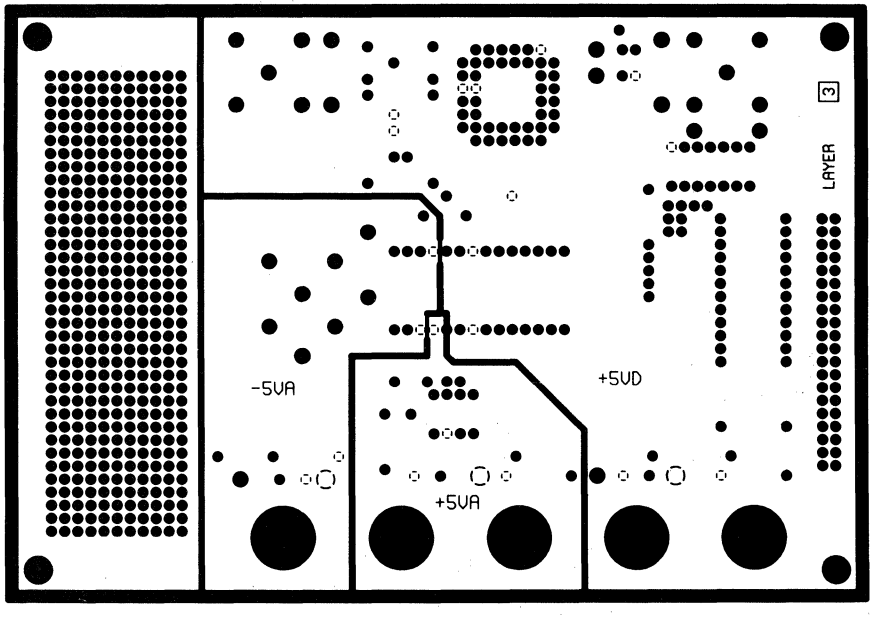


Figure 31. Power Layer PCB Layout

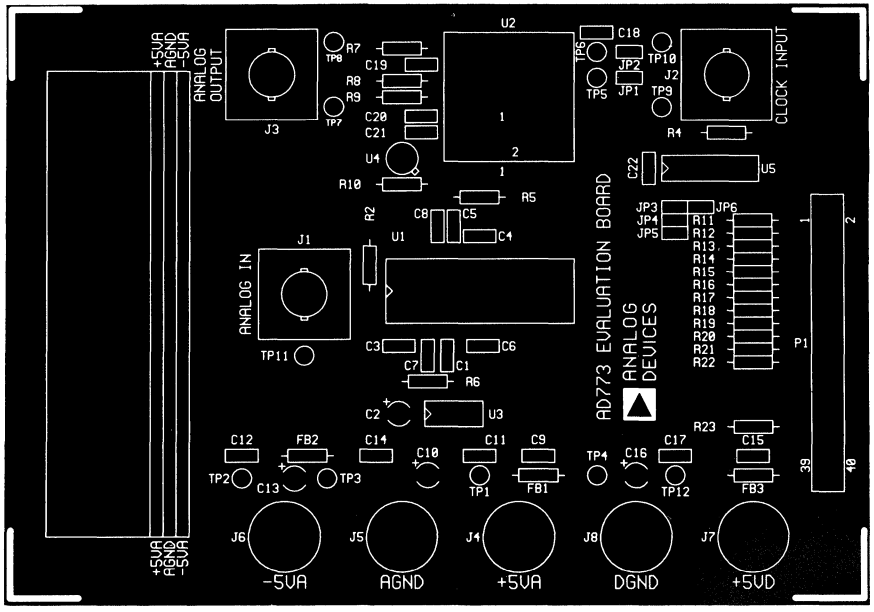


Figure 32. Silkscreen Layer PCB Layout

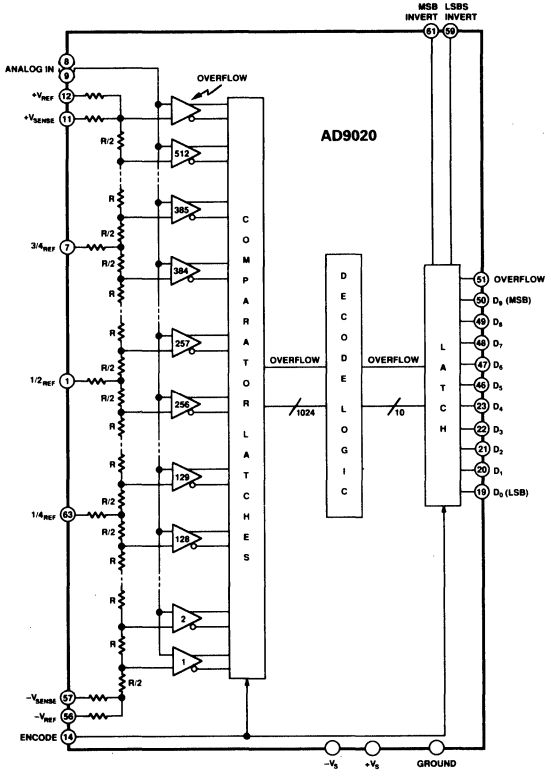
10-Bit, 60 MSPS A/D Converter

AD9020

FEATURES
Monolithic 10-Bit/60 MSPS Converter
TTL Outputs
Bipolar (±1.75 V) Analog Input
56 dB SNR @ 2.3 MHz Input
Low (45 pF) Input Capacitance
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Digital Oscilloscopes
Medical Imaging
Professional Video
Radar Warning/Guidance Systems
Infrared Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9020 A/D converter is a 10-bit monolithic converter capable of word rates of 60 MSPS and above. Innovative architecture using 512 input comparators instead of the traditional 1024 required by other flash converters reduces input capacitance and improves linearity.

Encode and outputs are TTL-compatible, making the AD9020 an ideal candidate for use in low power systems. An overflow bit is provided to indicate analog input signals greater than $+V_{SENSE}$.

Voltage sense lines are provided to insure accurate driving of the $\pm V_{REF}$ voltages applied to the units. Quarter-point taps on the resistor ladder help optimize the integral linearity of the unit.

Either 68-pin ceramic leaded (gull wing) packages or ceramic LCCs are available and are specifically designed for low thermal impedances. Two performance grades for temperatures of both 0 to +70°C and −55°C to +125°C ranges are offered to allow the user to select the linearity best suited for each application. Dynamic performance is fully characterized and production tested at +25°C. MIL-STD-883 units are available.

The AD9020 A/D Converter is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD9020/883B data sheet for detailed specifications.

AD9020—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$	+6 V
$-V_S$	−6 V
ANALOG IN	−2 V to +2 V
$+V_{REF}$, $-V_{REF}$, $3/4_{REF}$, $1/2_{REF}$, $1/4_{REF}$	−2 V to +2 V
$+V_{REF}$ to $-V_{REF}$	4.0 V
DIGITAL INPUTS	−0.5 V to $+V_S$
$3/4_{REF}$, $1/2_{REF}$, $1/4_{REF}$ Current	±10 mA
Digital Output Current	20 mA
Operating Temperature	
AD9020JE/KE/JZ/KZ	0 to +70°C
Storage Temperature	−65°C to +150°C
Maximum Junction Temperature[2]	+175°C
Lead Soldering Temp (10 sec)	+300°C

ELECTRICAL CHARACTERISTICS ($\pm V_S$ = ±5 V; $\pm V_{SENSE}$ = ±1.75 V; ENCODE = 40 MSPS unless otherwise noted)[3]

Parameter (Conditions)	Temp	Test Level	AD9020JE/JZ Min	AD9020JE/JZ Typ	AD9020JE/JZ Max	AD9020KE/KZ Min	AD9020KE/KZ Typ	AD9020KE/KZ Max	Units
RESOLUTION			10			10			Bits
DC ACCURACY[3]									
Differential Nonlinearity	+25°C	I		1.0	1.25		0.75	1.0	LSB
	Full	VI			1.5			1.25	LSB
Integral Nonlinearity	+25°C	I		1.25	2.0		1.0	1.5	LSB
	Full	VI			2.5			2.0	LSB
No Missing Codes	Full	VI					Guaranteed		
ANALOG INPUT									
Input Bias Current[4]	+25°C	I		0.4	1.0		0.4	1.0	mA
	Full	VI			2.0			2.0	mA
Input Resistance	+25°C	I	2.0	7.0		2.0	7.0		kΩ
Input Capacitance[4]	+25°C	V		45			45		pF
Analog Bandwidth	+25°C	V		175			175		MHz
REFERENCE INPUT									
Reference Ladder Resistance	+25°C	I	22	37	56	22	37	56	Ω
	Full	VI	14		66	14		66	Ω
Ladder Tempco	Full	V		0.1			0.1		Ω/°C
Reference Ladder Offset									
Top of Ladder	+25°C	I		45	90		45	90	mV
	Full	VI			90			90	mV
Bottom of Ladder	+25°C	I		45	90		45	90	mV
	Full	VI			90			90	mV
Offset Drift Coefficient	Full	V		50			50		μV/°C
SWITCHING PERFORMANCE									
Conversion Rate	+25°C	I	60			60			MSPS
Aperture Delay (t_A)	+25°C	V		1			1		ns
Aperture Uncertainty (Jitter)	+25°C	V		5			5		ps, rms
Output Delay (t_{OD})[5]	+25°C	I	6	10	13	6	10	13	ns
Output Time Skew[5]	+25°C	I		3	5		3	5	ns
DYNAMIC PERFORMANCE									
Transient Response	+25°C	V		10			10		ns
Overvoltage Recovery Time	+25°C	V		10			10		ns
Effective Number of Bits (ENOB)									
f_{IN} = 2.3 MHz	+25°C	I	8.6	9.0		8.6	9.0		Bits
f_{IN} = 10.3 MHz	+25°C	IV	8.0	8.4		8.0	8.4		Bits
f_{IN} = 15.3 MHz	+25°C	IV	7.5	8.0		7.5	8.0		Bits
Signal-to-Noise Ratio[6]									
f_{IN} = 2.3 MHz	+25°C	I	54	56		54	56		dB
f_{IN} = 10.3 MHz	+25°C	I	50	53		50	53		dB
f_{IN} = 15.3 MHz	+25°C	I	47	50		47	50		dB
Signal-to-Noise Ratio[6] (Without Harmonics)									
f_{IN} = 2.3 MHz	+25°C	I	54	56		54	56		dB
f_{IN} = 10.3 MHz	+25°C	I	51	54		51	54		dB
f_{IN} = 15.3 MHz	+25°C	I	48	52		48	52		dB

Parameter (Conditions)	Temp	Test Level	AD9020JE/JZ Min	AD9020JE/JZ Typ	AD9020JE/JZ Max	AD9020KE/KZ Min	AD9020KE/KZ Typ	AD9020KE/KZ Max	Units
DYNAMIC PERFORMANCE (CONTINUED)									
Harmonic Distortion									
f_{IN} = 2.3 MHz	+25°C	I	61	67		61	67		dBc
f_{IN} = 10.3 MHz	+25°C	I	55	59		55	59		dBc
f_{IN} = 15.3 MHz	+25°C	I	49	53		49	53		dBc
Two-Tone Intermodulation Distortion Rejection[7]	+25°C	V		70			70		dBc
Differential Phase	+25°C	V		0.5			0.5		Degree
Differential Gain	+25°C	V		1			1		%
ENCODE INPUT									
Logic "1" Voltage	Full	VI	2.0			2.0			V
Logic "0" Voltage	Full	VI			0.8			0.8	V
Logic "1" Current	Full	VI			20			20	μA
Logic "0" Current	Full	VI			800			800	μA
Input Capacitance	+25°C	V		5			5		pF
Pulse Width (High)	+25°C	I	6			6			ns
Pulse Width (Low)	+25°C	I	6			6			ns
DIGITAL OUTPUTS									
Logic "1" Voltage (I_{OH} = 2 mA)	Full	VI	2.4			2.4			V
Logic "0" Voltage (I_{OL} = 10 mA)	Full	VI			0.4				V
POWER SUPPLY									
$+V_S$ Supply Current	+25°C	I		440	530		440	530	mA
	Full	VI			542			542	mA
$-V_S$ Supply Current	+25°C	I		140	170		140	170	mA
	Full	VI			177			177	mA
Power Dissipation	+25°C	I		2.8	3.3		2.8	3.3	W
	Full	VI			3.4			3.4	W
Power Supply Rejection Ratio (PSRR)[8]	Full	VI		6	10		6	10	mV/V

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances (part soldered onto board): 68-pin leaded ceramic chip carrier: θ_{JC} = 1°C/W; θ_{JA} = 17°C/W (no air flow); θ_{JA} = 15°C/W (air flow = 500 LFM). 68-pin ceramic LCC: θ_{JC} = 2.6°C/W; θ_{JA} = 15°C/W (no air flow); θ_{JA} = 13°C/W (air flow = 500 LFM).

[3]$3/4_{REF}$, $1/2_{REF}$, and $1/4_{REF}$ reference ladder taps are driven from dc sources at +0.875 V, 0 V, and −0.875 V, respectively. Accuracy of the overflow comparator is not tested and not included in linearity specifications.

[4]Measured with ANALOG IN = $+V_{SENSE}$.

[5]Output delay measured as worst-case time from 50% point of the rising edge of ENCODE to 50% point of the slowest rising or falling edge of D_0–D_9. Output skew measured as worst-case difference in output delay among D_0–D_9.

[6]RMS signal to rms noise with analog input signal 1 dB below full scale at specified frequency.

[7]Intermodulation measured with analog input frequencies of 2.3 MHz and 3.0 MHz at 7 dB below full scale.

[8]Measured as the ratio of the worst-case change in transition voltage of a single comparator for a 5% change in $+V_S$ or $-V_S$.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS
Test Level

I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

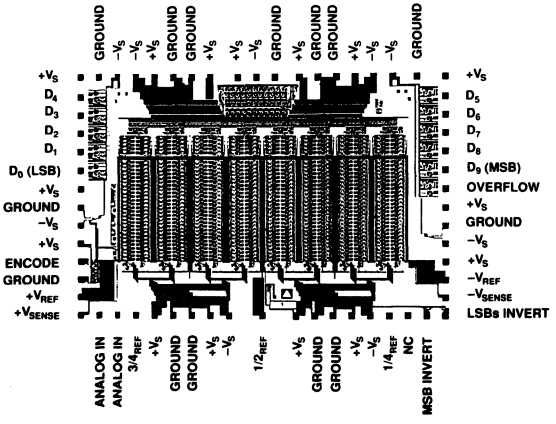
ORDERING GUIDE

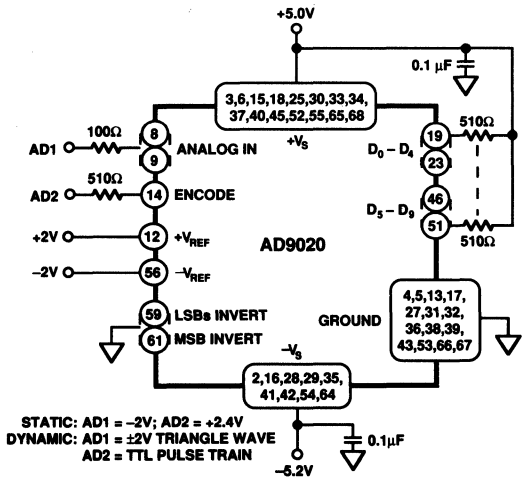
Device	Temperature Range	Description	Package Option*
AD9020JZ	0 to +70°C	68-Pin Leaded Ceramic	Z-68
AD9020JE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9020KZ	0 to +70°C	68-Pin Leaded Ceramic	Z-68
AD9020KE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9020SZ/883	−55°C to +125°C	68-Pin Leaded Ceramic	Z-68
AD9020SE/883	−55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9020TZ/883	−55°C to +125°C	68-Pin Leaded Ceramic	Z-68
AD9020TE/883	−55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9020/PCB	0 to +70°C	Evaluation Board	

*E = Ceramic Leadless Chip Carrier; Z = Ceramic Leaded Chip Carrier.
For outline information see Package Information section.

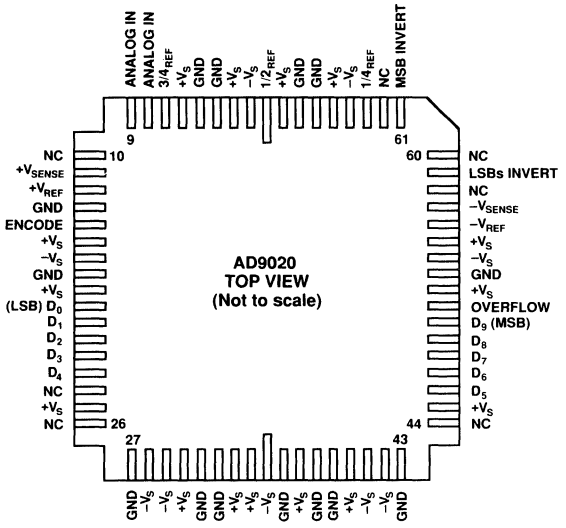
DIE LAYOUT AND MECHANICAL INFORMATION

Die Dimensions . . . . . 206 × 140 × 15 (±2) mils
Pad Dimensions . . . . . 4 × 4 mils
Metalization . . . . . Gold
Backing . . . . . None
Substrate Potential . . . . . $-V_S$
Passivation . . . . . Nitride





AD9020 Burn-In Circuit



AD9020 Pin Designations

AD9020 PIN DESCRIPTIONS

Pin No.	Name	Function
1	$1/2_{REF}$	Midpoint of internal reference ladder.
2, 16, 28, 29, 35, 41, 42, 54, 64	$-V_S$	Negative supply voltage; nominally −5.0 V ±5%.
3, 6, 15, 18, 25, 30, 33, 34, 37, 40, 45, 52, 55, 65, 68	$+V_S$	Positive supply voltage; nominally +5 V ±5%.
4, 5, 13, 17, 27, 31, 32 36, 38, 39, 43, 53, 66, 67	GROUND	All ground pins should be connected together and to low-impedance ground plane.
7	$3/4_{REF}$	Three-quarter point of internal reference ladder.
8, 9	ANALOG IN	Analog input; nominally between ±1.75 V.
11	$+V_{SENSE}$	Voltage sense line to most positive point on internal resistor ladder. Normally +1.75 V.
12	$+V_{REF}$	Voltage force connection for top of internal reference ladder. Normally driven to provide +1.75 V at $+V_{SENSE}$.
14	ENCODE	TTL-compatible convert command used to begin digitizing process.
19–23, 46–50	D_0–D_9	TTL-compatible digital output data.
51	OVERFLOW	TTL-compatible output indicating ANALOG IN > $+V_{SENSE}$.
56	$-V_{REF}$	Voltage force connection for bottom of internal reference ladder. Normally driven to provide −1.75 V at $-V_{SENSE}$.
57	$-V_{SENSE}$	Voltage sense line to most negative point on internal resistor ladder. Normally −1.75 V.
59	LSBs INVERT	Normally grounded. When connected to $+V_S$, lower order bits (D_0–D_8) are inverted.
61	MSB INVERT	Normally grounded. When connected to $+V_S$, most significant bit (MSB; D_9) is inverted.
63	$1/4_{REF}$	One-quarter point of internal reference ladder.

THEORY OF OPERATION

Refer to the AD9020 block diagram. As shown, the AD9020 uses a modified "flash", or parallel, A/D architecture. The analog input range is determined by an external voltage reference ($+V_{REF}$ and $-V_{REF}$), nominally ±1.75 V. An internal resistor ladder divides this reference into 512 steps, each representing two quantization levels. Taps along the resistor ladder ($1/4_{REF}$, $1/2_{REF}$ and $3/4_{REF}$) are provided to optimize linearity. Rated performance is achieved by driving these points at 1/4, 1/2 and 3/4, respectively, of the voltage reference range.

The A/D conversion for the nine most significant bits (MSBs) is performed by 512 comparators. The value of the least significant bit (LSB) is determined by a unique interpolation scheme between adjacent comparators. The decoding logic processes the comparator outputs and provides a 10-bit code to the output stage of the converter.

Flash architecture has an advantage over other A/D architectures because conversion occurs in one step. This means the performance of the converter is limited primarily by the speed and matching of the individual comparators. In the AD9020, an innovative interpolation scheme takes advantage of flash architecture but minimizes the input capacitance, power and device count usually associated with that method of conversion.

These advantages occur because of using only half the normal number of input comparator cells to accomplish the conversion. In addition, a proprietary decoding scheme minimizes error codes. Input control pins allow the user to select from among Binary, Inverted Binary, Twos Complement and Inverted Twos Complement coding (See AD9020 Truth Table).

APPLICATIONS

Many of the specifications used to describe analog/digital converters have evolved from system performance requirements in these applications. Different systems emphasize particular specifications, depending on how the part is used. The following applications highlight some of the specifications and features that make the AD9020 attractive in these systems.

Wideband Receivers

Radar and communication receivers (baseband and direct IF digitization), ultrasound medical imaging, signal intelligence and spectral analysis all place stringent ac performance requirements on analog-to-digital converters (ADCs). Frequency domain characterization of the AD9020 provides signal-to-noise ratio (SNR) and harmonic distortion data to simplify selection of the ADC.

Receiver sensitivity is limited by the *Signal-to-Noise Ratio (SNR)* of the system. The SNR for an ADC is measured in the frequency domain and calculated with a Fast Fourier Transform (FFT). The SNR equals the ratio of the fundamental component of the signal (rms amplitude) to the rms value of the "noise." The noise is the sum of all other spectral components, including harmonic distortion, but excluding dc.

Good receiver design minimizes the level of spurious signals in the system. Spurious signals developed in the ADC are the result of imperfections in the device transfer function (nonlinearities, delay mismatch, varying input impedance, etc.). In the ADC, these spurious signals appear as Harmonic Distortion. Harmonic Distortion is also measured with an FFT and is specified as the ratio of the fundamental component of the signal (rms amplitude) to the rms value of the worst case harmonic (usually the 2nd or 3rd).

Two-Tone Intermodulation Distortion (IMD) is a frequently cited specification in receiver design. In narrow-band receivers, third-order IMD products result in spurious signals in the pass band of the receiver. Like mixers and amplifiers, the ADC is characterized with two, equal-amplitude, pure input frequencies. The IMD equals the ratio of the power of either of the two input signals to the power of the strongest third-order IMD signal. Unlike mixers and amplifiers, the IMD does not always behave as it does in linear devices (reduced input levels do not result in predictable reductions in IMD).

Performance graphs provide typical harmonic and SNR data for the AD9020 for increasing analog input frequencies. In choosing an A/D converter, always look at the dynamic range for the analog input frequency of interest. The AD9020 specifications provide guaranteed minimum limits at three analog test frequencies.

Aperture Delay is the delay between the rising edge of the ENCODE command and the instant at which the analog input is sampled. Many systems require simultaneous sampling of more than one analog input signal with multiple ADCs. In these situations, timing is critical and the absolute value of the aperture delay is not as critical as the matching between devices.

Aperture Uncertainty, or jitter, is the sample-to-sample variation in aperture delay. This is especially important when sampling high slew rate signals in wide bandwidth systems. Aperture uncertainty is one of the factors which degrades dynamic performance as the analog input frequency is increased.

Digitizing Oscilloscopes

Oscilloscopes provide amplitude information about an observed waveform with respect to time. Digitizing oscilloscopes must accurately sample this signal, without distorting the information to be displayed.

One figure of merit for the ADC in these applications is *Effective Number of Bits (ENOBs)*. ENOB is calculated with a sine wave curve fit and equals:

$$ENOB = N - LOG_2 [Error\ (measured)/Error\ (ideal)]$$

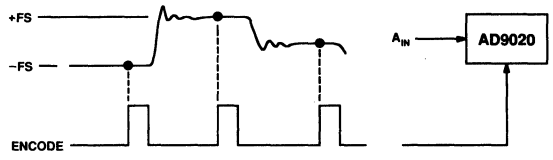
N is the resolution (number of bits) of the ADC. The measured error is the actual rms error calculated from the converter outputs with a pure sine wave input.

The *Analog Bandwidth* of the converter is the analog input frequency at which the spectral power of the fundamental signal is reduced 3 dB from its low frequency value. The analog bandwidth is a good indicator of a converter's slewing capabilities.

The *Maximum Conversion Rate* is defined as the encode rate at which the SNR for the lowest analog signal test frequency tested drops by no more than 3 dB below the guaranteed limit.

Imaging

Visible and infrared imaging systems both require similar characteristics from ADCs. The signal input (from a CCD camera, or multiplexer) is a time division multiplexed signal consisting of a series of pulses whose amplitude varies in direct proportion to the intensity of the radiation detected at the sensor. These varying levels are then digitized by applying encode commands at the correct times, as shown below.



Imaging Application Using AD9020

The actual resolution of the converter is limited by the thermal and quantization noise of the ADC. The low frequency test for SNR or ENOB is a good measure of the noise of the AD9020. At this frequency, the static errors in the ADC determine the useful dynamic range of the ADC.

Although the signal being sampled does not have a significant slew rate, this does not imply dynamic performance is not important. The *Transient Response and Overvoltage Recovery Time* specifications insure that the ADC can track full-scale changes in the analog input sufficiently fast to capture a valid sample.

Transient Response is the time required for the AD9020 to achieve full accuracy when a step function is applied. *Overvoltage Recovery Time* is the time required for the AD9020 to recover to full accuracy after an analog input signal 150% of full scale is reduced to the full-scale range of the converter.

Professional Video

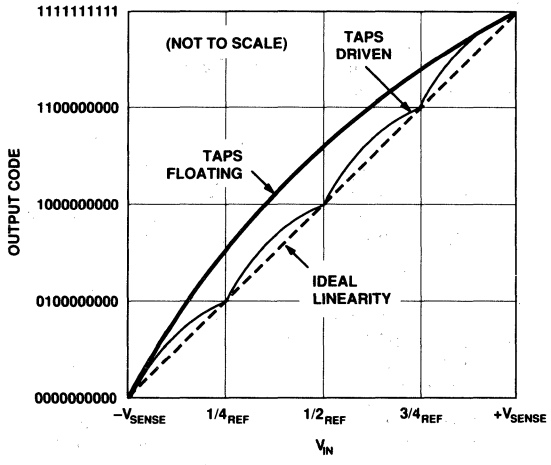
Digital Signal Processing (DSP) is now common in television production. Modern studios rely on digitized video to create state-of-the-art special effects. Video instrumentation also requires high resolution ADCs for studio quality measurement and frame storage.

The AD9020 provides sufficient resolution for these demanding applications. Conversion speed, dynamic performance and analog bandwidth are suitable for digitizing both composite and RGB video sources.

USING THE AD9020

Voltage References

The AD9020 requires that the user provide two voltage references: $+V_{REF}$ and $-V_{REF}$. These two voltages are applied across an internal resistor ladder (nominally 37 Ω) and set the analog input voltage range of the converter. The voltage references should be driven from a stable, low impedance source. In addition to these two references, three evenly spaced taps on the resistor ladder ($1/4_{REF}$, $1/2_{REF}$, $3/4_{REF}$) are available. Providing a reference to these quarter points on the resistor ladder will improve the integral linearity of the converter and improve ac performance. (AC and dc specifications are tested while driving the quarter points at the indicated levels.) The figure below is not intended to show the transfer function of the ADC, but illustrates how the linearity of the device is affected by reference voltages applied to the ladder.



Effect of Reference Taps on Linearity

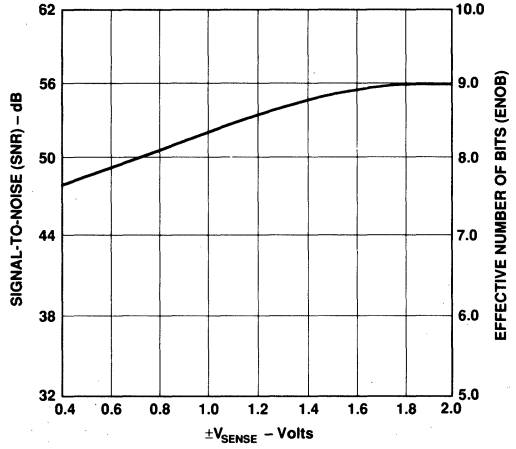
Resistance between the reference connections and the taps of the first and last comparators causes offset errors. These errors, called "top and bottom of the ladder offsets," can be nulled by using the voltage sense lines, $+V_{SENSE}$ and $-V_{SENSE}$, to adjust the reference voltages. Current through the sense lines should be limited to less than 100 μA. Excessive current drawn through the voltage sense lines will affect the accuracy of the sense line voltage.

The next page shows a reference circuit which nulls out the offset errors using two op amps and provides appropriate voltage references to the quarter-point taps. Feedback from the sense lines causes the op amps to compensate for the offset errors. The two transistors limit the amount of current drawn directly from the op amps; resistors at the base connections stabilize their operation. The 10 kΩ resistors (R1–R4) between the voltage sense lines form an external resistor ladder; the quarter point voltages are taken off this external ladder and buffered by an op amp. The actual values of resistors R1–R4 are not critical, but they should match well and be large enough (≥10 kΩ) to limit the amount of current drawn from the voltage sense lines.

The select resistors (R_S) shown in the schematic (each pair can be a potentiometer) are chosen to adjust the quarter-point voltage references, but are not necessary if R1–R4 match within 0.05%.

An alternative approach for defining the quarter-point references of the resistor ladder is to evaluate the integral linearity error of an individual device, and adjust the voltage at the quarter-points to minimize this error. This may improve the low frequency ac performance of the converter.

Performance of the AD9020 has been optimized with an analog input voltage of ±1.75 V (as measured at $\pm V_{SENSE}$). If the analog input range is reduced below these values, relatively larger differential nonlinearity errors may result because of comparator mismatches. As shown in the figure below, performance of the converter is a function of $\pm V_{SENSE}$.



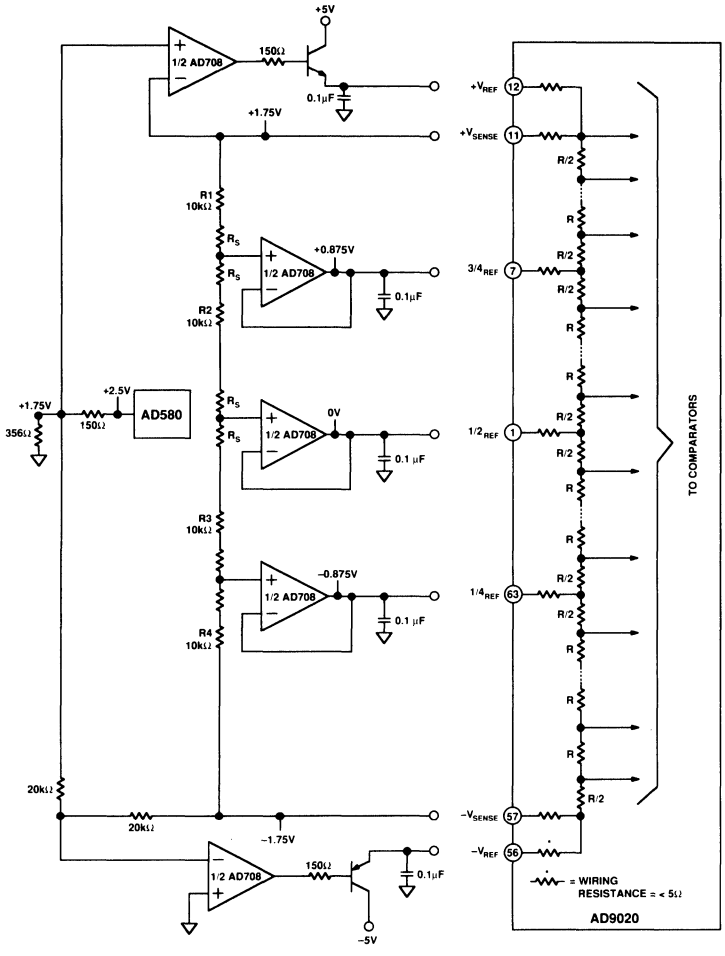
AD9020 SNR and ENOB vs. Reference Voltage

Applying a voltage greater than 4 V across the internal resistor ladder will cause current densities to exceed rated values, and may cause permanent damage to the AD9020. The design of the reference circuit should limit the voltage available to the references.

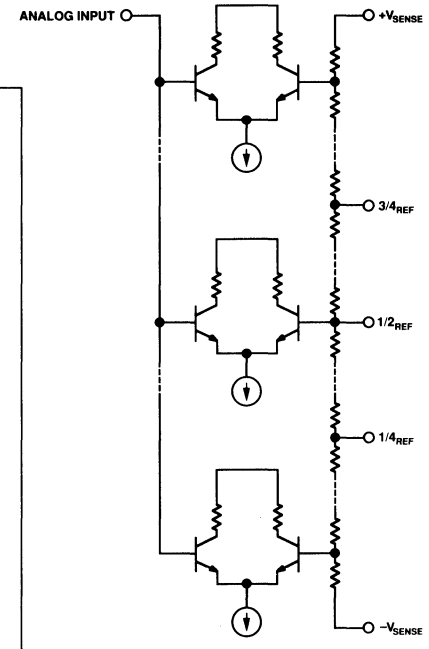
Analog Input Signal

The signal applied to ANALOG IN drives the inputs of 512 parallel comparator cells (see Equivalent Analog Input figure). This connection typically has an input resistance of 7 kΩ, and input capacitance of 45 pF. The input capacitance is nearly constant over the analog input voltage range, as shown in the graph which illustrates that characteristic.

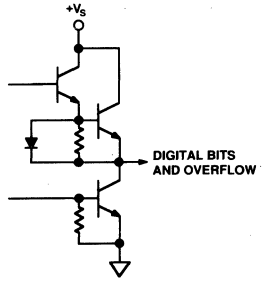
The analog input signal should be driven from a low distortion, low noise amplifier. A good choice is the AD9617, a wide bandwidth, monolithic operational amplifier with excellent ac and dc performance. The input capacitance should be isolated by a small series resistor (24 Ω for the AD9617) to improve the ac performance of the amplifier (see AD9020/PCB Evaluation Board Block Diagram).



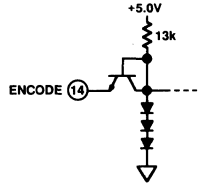
AD9020 Reference Circuit



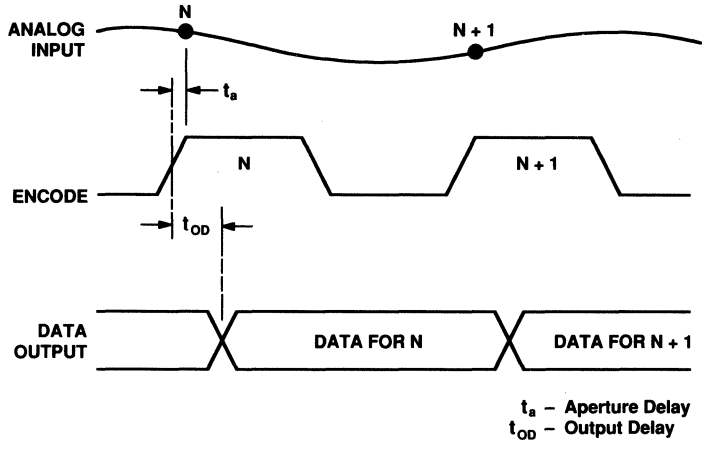
AD9020 Equivalent Analog Input



AD9020 Equivalent Digital Outputs



AD9020 Equivalent Encode Circuit



AD9020 Timing Diagram

Timing

In the AD9020, the rising edge of the ENCODE signal triggers the A/D conversion by latching the comparators. (See the AD9020 Timing Diagram.)

The ENCODE is TTL/CMOS compatible and should be driven from a low jitter (phase noise) source. Jitter on the ENCODE signal will raise the noise floor of the converter. Fast, clean edges will reduce the jitter in the signal and allow optimum ac performance. Locking the system clock to a crystal oscillator also helps reduce jitter. The AD9020 is designed to operate with a 50% duty cycle; small (10%) variations in duty cycle should not degrade performance.

Data Format

The format of the output data (D_0– D_9) is controlled by the MSB INVERT and LSBs INVERT pins. These inputs are dc control inputs, and should be connected to GROUND or $+V_S$. The AD9020 Truth Table gives information to choose from among Binary, Inverted Binary, Twos Complement and Inverted Twos Complement coding.

The OVERFLOW output is an indication that the analog input signal has exceeded the voltage at $+V_{SENSE}$. The accuracy of the overflow transition voltage and output delay are not tested or included in the data sheet limits. Performance of the overflow indicator is dependent on circuit layout and slew rate of the encode signal. The operation of this function does not affect the other data bits (D_0–D_9). It is not recommended for applications requiring a critical measure of the analog input voltage.

Layout and Power Supplies

Proper layout of high speed circuits is always critical but is particularly important when both analog and digital signals are involved.

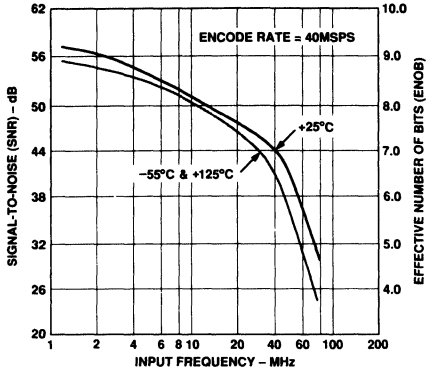
Analog signal paths should be kept as short as possible and be properly terminated to avoid reflections. The analog input voltage and the voltage references should be kept away from digital signal paths; this reduces the amount of digital switching noise that is capacitively coupled into the analog section of the circuit. Digital signal paths should also be kept short, and run lengths should be matched to avoid propagation delay mismatch.

In high speed circuits, layout of the ground circuit is a critical factor. A single, low impedance ground plane, on the component side of the board, will reduce noise on the circuit ground. Power supplies should be capacitively coupled to the ground plane to reduce noise in the circuit. Multilayer boards allow designers to lay out signal traces without interrupting the ground plane and provide low impedance power planes.

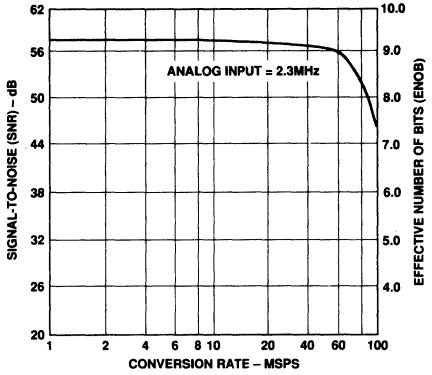
It is especially important to maintain the continuity of the ground plane under and around the AD9020. In systems with dedicated digital and analog grounds, all grounds of the AD9020 should be connected to the analog ground plane.

The power supplies ($+V_S$ and $-V_S$) of the AD9020 should be isolated from the supplies used for external devices; this further reduces the amount of noise coupled into the A/D converter. Sockets limit the dynamic performance and should be used only for prototypes or evaluation—PCK Elastomerics Part # CCS-68-55 is recommended for the LCC package. (Tel. 215-672-0787)

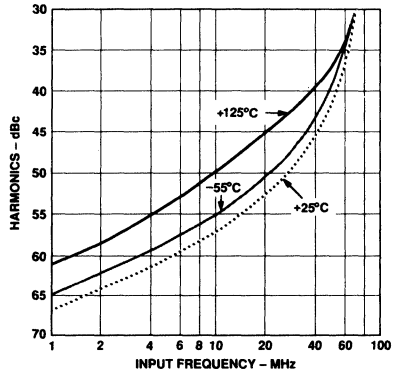
An evaluation board is available to aid designers and provide a suggested layout.



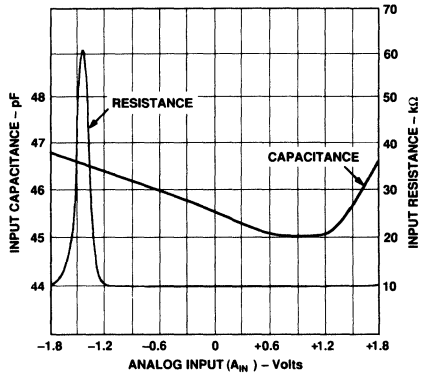
AD9020 SNR and ENOB vs. Input Frequency



AD9020 SNR and ENOB vs. Conversion Rate



AD9020 Harmonics vs. Input Frequency



Input Capacitance/Resistance vs. Input Voltage

Step	Range	Offset Binary		Twos Complement	
		True	Inverted	True	Inverted
	0 = −1.75 V FS = +1.75 V	MSB INV = "0" LSBs INV = "0"	MSB INV = "1" LSBs INV = "1"	MSB INV = "1" LSBs INV = "0"	MSB INV = "0" LSBs INV = "1"
1024	>+1.7500	(1)1111111111	(1)0000000000	(1)0111111111	(1)1000000000
1023	+1.7466	1111111111	0000000000	0111111111	1000000000
1022	+1.7432	1111111110	0000000001	0111111110	1000000001
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
512	+0.0034	1000000000	0111111111	0000000000	1111111111
511	0.000	0111111111	1000000000	1111111111	0000000000
510	−0.0034	0111111110	1000000001	1111111110	0000000001
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
02	−1.7432	0000000010	1111111101	1000000010	0111111101
01	−1.7466	0000000001	1111111110	1000000001	0111111110
00	<−1.7466	0000000000	1111111111	1000000000	0111111111

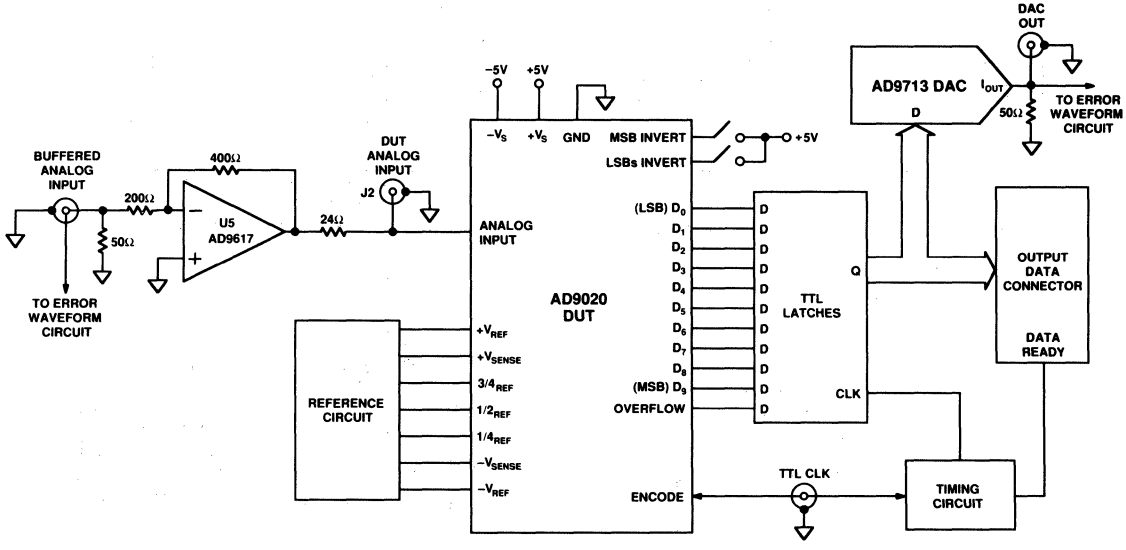
The overflow bit is always 0 except where noted in parentheses ( ). MSB INVERT and LSBs INVERT are considered dc controls.

AD9020 Truth Table

AD9020/PCB EVALUATION BOARD

The AD9020/PCB Evaluation Board is available from the factory and is shown here in block diagram form. The board includes a reference circuit that allows the user to adjust both references and the quarter-point voltages. The AD9617 is included as the drive amplifier, and the user can configure the gain from −1 to −15.

On-board reconstruction of the digital data is provided through the AD9713, a 12-bit monolithic DAC. The analog and reconstructed waveforms can be summed on the board to allow the user to observe the linearity of the AD9020 and the effects of the quarter-point voltages. The digital data and an adjustable Data Ready signal are available through a 37-pin edge connector.



AD9020/PCB Evaluation Board Block Diagram

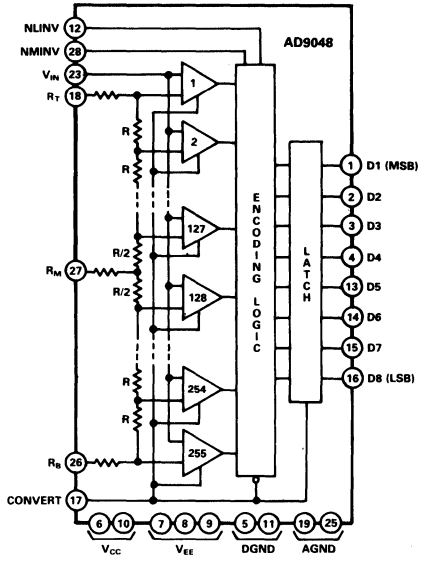
Monolithic 8-Bit Video A/D Converter

AD9048

FEATURES
35MSPS Encode Rate
16pF Input Capacitance
550mW Power Dissipation
Industry-Standard Pinouts
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Professional Video Systems
Special Effects Generators
Electro-Optics
Digital Radio
Electronic Warfare (ECM, ECCM, ESM)

FUNCTIONAL BLOCK DIAGRAM



4

GENERAL DESCRIPTION

The AD9048 is an 8-bit, 35MSPS flash converter, made on a high speed bipolar process, which is an alternate source for the TDC1048 unit but offers enhancements over its predecessor. Lower power dissipation makes the AD9048 attractive for a variety of system designs.

Because of its wide bandwidth, it is an ideal choice for real-time conversion of video signals. Input bandwidth is flat with no missing codes.

Clocked latching comparators, encoding logic and output buffer registers operating at minimum rates of 35MSPS preclude a need for a sample-and-hold (S/H) or track-and-hold (T/H) in most system designs using the AD9048. All digital control inputs and outputs are TTL compatible.

Devices operating over two ambient temperature ranges and with two grades of linearity are available. Linearities of either 0.5LSB or 0.75LSB can be ordered for a commercial range of 0 to +70°C, or extended case temperatures of −55°C to +125°C. Commercial versions are packaged in 28-pin DIPs; extended temperature versions are available in ceramic DIP and ceramic LCC packages. Both commercial units and MIL-STD-883 units are standard products.

The AD9048 A/D converter is available in versions compliant with MIL-STD-883. Refer to the Analog Devices *Military Products Databook* or current AD9048/883B data sheet for detailed specifications.

AD9048 – SPECIFICATIONS (typical with nominal supplies unless otherwise noted)

ABSOLUTE MAXIMUM RATINGS[1]

V_{CC} to DGND . . . . . −0.5V dc to +7.0V dc
AGND to DGND . . . . . −0.5V dc to +0.5V dc
V_{EE} to AGND . . . . . +0.5V dc to −7.0V dc
V_{IN}, V_{RT} or V_{RB} to AGND . . . . . +0.5V to V_{EE}
V_{RT} to V_{RB} . . . . . −2.2V dc to +2.2V dc
CONV, NMINV or NLINV to DGND . −0.5V dc to +5.5V dc
Applied Output Voltage to DGND . −0.5V dc to +5.5V dc[2]
Applied Output Current, Externally Forced
. . . . . −1.0mA to +6.0mA[3, 4]
Output Short-Circuit Duration . . . . . 1.0sec[5]
Operating Temperature Range (Ambient)
AD9048JN/KN/JJ/KJ/JQ/KQ . . . . . 0 to +70°C
AD9048SE/SQ/TE/TQ . . . . . −55°C to +125°C
Maximum Junction Temperature (Plastic) . . . . . +150°C[6]
Maximum Junction Temperature (Hermetic) . . . . . +175°C[6]
Lead Temperature (Soldering, 10sec) . . . . . +300°C
Storage Temperature Range . . . . . −65°C to +150°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0V; V_{EE} = −5.2V; Differential Reference Voltage = 2.0V, unless otherwise noted)

			AD9048JN/JJ/JQ			AD9048KN/KJ/KQ			AD9048SE/SQ			AD9048TE/TQ			
Parameter (Conditions)	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
RESOLUTION			8			8			8			8			Bits
DC ACCURACY															
Differential Nonlinearity	+25°C	I		0.4	0.75		0.3	0.5		0.4	0.75		0.3	0.5	LSB
	Full	VI			1.0			0.75			1.0			0.75	LSB
Integral Nonlinearity	+25°C	I		0.6	0.75		0.4	0.5		0.6	0.75		0.4	0.5	LSB
	Full	VI			1.0			0.75			1.0			0.75	LSB
No Missing Codes	Full	VI	GUARANTEED			GUARANTEED			GUARANTEED			GUARANTEED			
INITIAL OFFSET ERROR															
Top of Reference Ladder	+25°C	I		5	12		5	12		5	12		5	12	mV
	Full	VI			12			12			12			12	mV
Bottom of Reference Ladder	+25°C	I		4	8		4	8		4	8		4	8	mV
	Full	VI			8			8			8			8	mV
Offset Drift Coefficient	Full	V		20			20			20			20		μV/°C
ANALOG INPUT															
Input Voltage Range	Full	V		−2.1; +0.1			−2.1; +0.1			−2.1; +0.1			−2.1; +0.1		V
Input Bias Current[7, 8, 9]	+25°C	I		36	60		36	60		36	60		36	60	μA
	Full	VI			100			100			100			100	μA
Input Resistance	+25°C	I	200	300		200	300		200	300		200	300		kΩ
	Full	VI	40			40			40			40			kΩ
Input Capacitance	+25°C	III		16	20		16	20		16	20		16	20	pF
Full Power Bandwidth[10]	+25°C	III	10	15		10	15		10	15		10	15		MHz
REFERENCE INPUT															
Positive Reference Voltage[11]	Full	V		0.0			0.0			0.0			0.0		V
Negative Reference Voltage[11]	Full	V		−2.0			−2.0			−2.0			−2.0		V
Differential Reference Voltage	Full	V		2.0			2.0			2.0			2.0		V
Reference Ladder Resistance	Full	VI	50	90	125	50	90	125	50	90	125	50	90	125	Ω
Ladder Temperature Coefficient	Full	V		0.22			0.22			0.22			0.22		Ω/°C
Reference Ladder Current[12]	Full	VI		23	40		23	40		23	40		23	40	mA
Reference Input Bandwidth	+25°C	V		10			10			10			10		MHz
DYNAMIC PERFORMANCE[13]															
Conversion Rate[12, 14]	+25°C	I	35	38		35	38		35	38		35	38		MHz
Aperture Delay	+25°C	III		2.4	5		2.4	5		2.4	5		2.4	5	ns
Aperture Uncertainty (Jitter)	+25°C	III		25	50		25	50		25	50		25	50	ps
Output Delay (t_{PD})[8, 12]	+25°C	I		13	15		9	15		9	15		9	15	ns
Output Hold Time (t_{OH})[15]	+25°C	I	5	8		5	8		5	8		5	8		ns
Transient Response[16]	+25°C	I		6	20		6	20		6	20		6	20	ns
Overvoltage Recovery Time[17]	+25°C	V		8			8			8			8		ns
Rise Time	+25°C	I			9			9			9			9	ns
Fall Time	+25°C	I			14			14			14			14	ns
Output Time Skew[18]	+25°C	I		4.5	7		4.5	7		4.5	7		4.5	7	ns
NMINV and NLINV INPUTS[8, 12]															
+0.4V Input Current	Full	VI			200			200			200			200	μA
+2.4V Input Current	Full	VI			10			10			10			10	μA
+5.5V Input Current	Full	VI			10			10			10			10	μA
CONVERT INPUT															
Logic "1" Voltage	Full	VI	2.0			2.0			2.0			2.0			V
Logic "0" Voltage	Full	VI			0.8			0.8			0.8			0.8	V
Logic "1" Current (V_I = +2.4V)[8, 12]	Full	VI			15			15			15			15	μA
Logic "1" Current (V_I = +5.5V)[8, 12]	Full	VI			15			15			15			15	μA
Logic "0" Current[8, 12]	Full	VI			500			500			500			500	μA
Input Capacitance	+25°C	III		4	6		4	6		4	6		4	6	pF
Convert Pulse Width (LOW)	+25°C	I	18			18			18			18			ns
Convert Pulse Width (HIGH)	+25°C	I	10			10			10			10			ns

Parameter (Conditions)	Temp	Test Level	AD9048JN/JJ/JQ Min	AD9048JN/JJ/JQ Typ	AD9048JN/JJ/JQ Max	AD9048KN/KJ/KQ Min	AD9048KN/KJ/KQ Typ	AD9048KN/KJ/KQ Max	AD9048SE/SQ Min	AD9048SE/SQ Typ	AD9048SE/SQ Max	AD9048TE/TQ Min	AD9048TE/TQ Typ	AD9048TE/TQ Max	Units
AC LINEARITY															
In-Band Harmonics															
dc to 2.438MHz[19]	+25°C	I	47	50		49	55		47	50		49	55		dBc
dc to 9.35MHz[20]	+25°C	V		48			48			48			48		dBc
Signal-to-Noise Ratio (SNR)[19]															
1.248MHz Input Frequency[21]	+25°C	I	43.5	44		45	46		43.5	44		45	46		dB
2.438MHz Input Frequency[21]	+25°C	I	43	44		44	46		43	44		44	46		dB
1.248MHz Input Frequency[22]	+25°C	I	52.5	53		54	55		52.5	53		54	55		dB
2.438MHz Input Frequency[22]	+25°C	I	52	53		53	55		52	53		53	55		dB
Signal-to-Noise Ratio (SNR)[20]															
1.248MHz Input Frequency[21]	+25°C	I	43.5	44		45	46		43.5	44		45	46		dB
9.35MHz Input Frequency[21]	+25°C	V		40.5			40.5			40.5			40.5		dB
Noise Power Ratio (NPR)[23]	+25°C	III	36.5	39		36.5	39		36.5	39		36.5	39		dB
Differential Phase[24]	+25°C	III			1			1			1			1	Degree
Differential Gain[24]	+25°C	III			2			2			2			2	%
DIGITAL OUTPUTS															
Logic "1" Voltage[14]	Full	VI	2.4			2.4			2.4			2.4			V
Logic "0" Voltage[9, 14]	Full	VI			0.5			0.5			0.5			0.5	V
Short Circuit Current[5]	Full	VI			30			30			30			30	mA
POWER SUPPLY															
Positive Supply Current (+5.5V)	+25°C	I		34	46		34	46		34	46		34	46	mA
(V_{EE} = −5.5V)	Full	VI			48			48			48			48	mA
Negative Supply Current (−5.5V)	+25°C	I		90	110		90	110		90	110		90	110	mA
	Full	VI			120			120			120			120	mA
Nominal Power Dissipation	+25°C	V		550			550			550			550		mW
Reference Ladder Dissipation	+25°C	V		45			45			45			45		mW

NOTES:
[1]Maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the device may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.
[2]Applied voltage must be current-limited to specified range.
[3]Forcing voltage must be limited to specified range.
[4]Current is specified as negative when flowing into the device.
[5]Output High; one pin to ground; one second duration.
[6]Typical thermal impedances (no air flow) are as follows:
Ceramic DIP: θ_{JA} = 49°C/W; θ_{JC} = 15°C/W LCC: θ_{JA} = 69°C/W; θ_{JC} = 21°C/W
Plastic DIP: θ_{JA} = 58°C/W; θ_{JC} = 16°C/W PLCC: θ_{JA} = 59; θ_{JC} = 19
To calculate junction temperature (T_J), use power dissipation (PD) and thermal impedance:
$T_J = PD(\theta_{JA}) + T_{AMBIENT} = PD(\theta_{JC}) = + T_{CASE}$
[7]Measured with V_{IN} = 0V and CONVERT low (sampling mode).
[8]V_{CC} = +5.5V
[9]V_{EE} = −5.5V
[10]Determined by beat frequency testing for no missing codes.
[11]$V_{RT} \geq V_{RB}$ under all circumstances.
[12]V_{EE} = −4.9V
[13]Outputs terminated with 40pF and 810Ω pull-up resistors.
[14]V_{CC} = +4.5V
[15]Interval from 50% point of leading edge CONVERT pulse to change in output data.
[16]For full scale step input, 8-bit accuracy attained in specified time.
[17]Recovers to 8-bit accuracy in specified time after −3V input overvoltage.
[18]Output time skew includes high-to-low and low-to-high transitions as well as bit-to-bit time skew differences.
[19]Measured at 20MHz encode rate with analog input 1dB below full scale.
[20]Measured at 35MHz encode rate with analog input 1dB below full scale.
[21]RMS signal to rms noise.
[22]Peak signal to rms noise.
[23]DC to 8MHz noise bandwidth with 1.248MHz slot; four sigma loading; 20MHz encode.
[24]Clock frequency = 4 × NTSC = 14.32MHz. Measured with 40-IRE modulated ramp.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

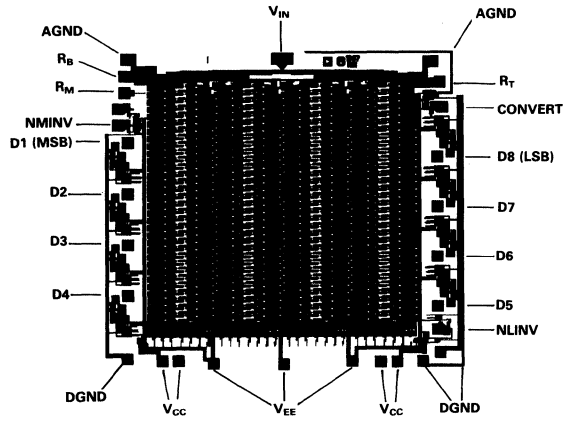
Test Level I – 100% production tested.
Test Level II – 100% production tested at +25°C and sample tested at specified temperatures.
Test Level III – Sample tested only.
Test Level IV – Parameter is guaranteed by design and characterization testing.
Test Level V – Parameter is a typical value only.
Test Level VI – All devices are 100% production tested at 25°C. 100% production tested at temperature extremes for military temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

Model	Linearity	Temperature	Package Option[1]
AD9048JN	0.75LSB	0 to +70°C	N-28
AD9048KN	0.5LSB	0 to +70°C	N-28
AD9048JJ	0.75LSB	0 to +70°C	J-28
AD9048KJ	0.5LSB	0 to +70°C	J-28
AD9048JQ	0.75LSB	0 to +70°C	Q-28
AD9048KQ	0.5LSB	0 to +70°C	Q-28
AD9048SE[2]	0.75LSB	−55°C to +125°C	E-28A
AD9048TE[2]	0.5LSB	−55°C to +125°C	E-28A
AD9048SQ[2]	0.75LSB	−55°C to +125°C	Q-28
AD9048TQ[2]	0.5LSB	−55°C to +125°C	Q-28

NOTES
[1]E = Leadless Ceramic Chip Carrier; J = J-Leaded Ceramic; N = Plastic DIP; Q = Cerdip. For outline information see Package Information section.
[2]For specifications, refer to Analog Devices *Military Products Databook*.

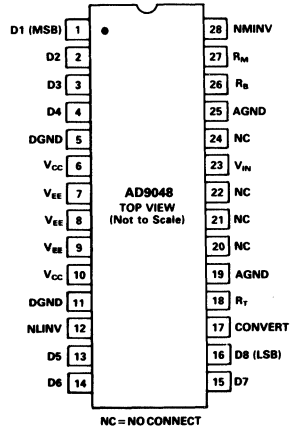
MECHANICAL INFORMATION



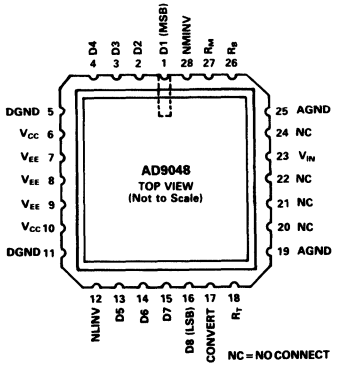
Die Dimensions	127 × 140 × 4 (±2) mils
Pad Dimensions	4 × 4 mils
Metalization	Gold
Backing	None
Substrate Potential	V_{EE}
Passivation	Nitride
Die Attach	Gold Eutectic
Bond Wire	1 mil Gold; Gold Ball Bonding

PIN CONFIGURATIONS

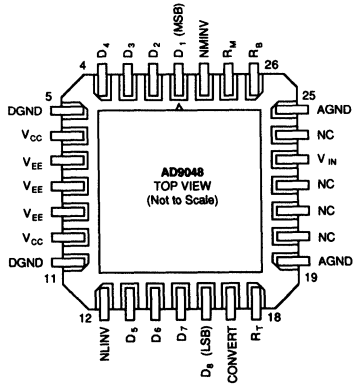
DIP



LCC

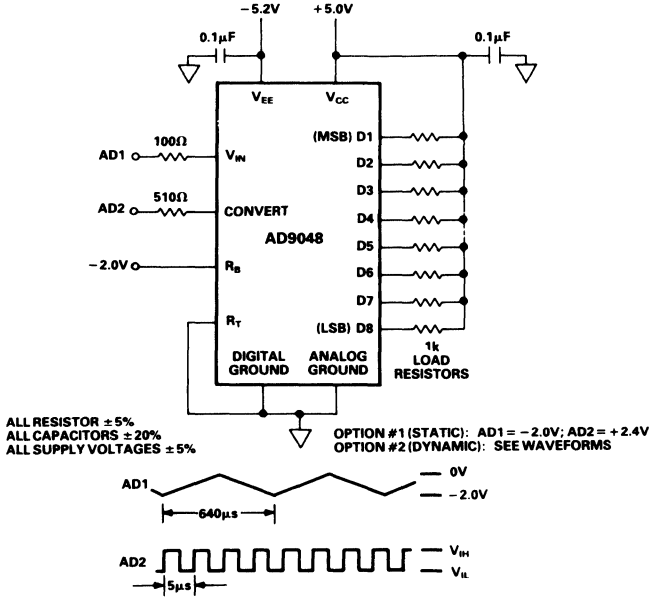


J-Leaded Ceramic



FUNCTIONAL DESCRIPTION

Pin Name	Description
D1 – D8	Eight digital outputs. D1 (MSB) is the most significant bit of the digital output word; D8 (LSB) is the least significant bit.
AGND	One of two analog ground returns. Both grounds should be connected together and to low impedance ground plane near the AD9048.
DGND	One of two digital ground returns. Both grounds should be connected together and to low impedance ground plane near the AD9048.
V_{CC}	Positive supply terminals; nominally +5.0V.
V_{EE}	Negative supply terminals; nominally −5.2V.
CONVERT	Input for conversion signal; sample of analog input signal taken on rising edge of this pulse.
R_B	Most negative reference voltage for internal reference ladder.
R_M	Midpoint tap on internal reference ladder.
R_T	Most positive reference voltage for internal reference ladder.
V_{IN}	Analog input signal pin.
NMINV	"Not Most Significant Bit Invert." In normal operation, this pin floats high; logic LOW at NMINV inverts most significant bit of digital output word [D1 (MSB)].
NLINV	"Not Least Significant Bit Invert." In normal operation, this pin floats high; logic LOW at NLINV inverts the seven least significant bits of the digital output word.



AD9048 Burn-In Diagram

THEORY OF OPERATION

Refer to the block diagram of the AD9048. The AD9048 comprises three functional sections: a comparator array, encoding logic, and output latches.

Within the array, the analog input signal to be digitized is compared with 255 reference voltages. The outputs of all comparators whose references are below the input signal level will be high; and outputs whose references are above that level will be low.

The n-of-255 code which results from this comparison is applied to the encoding logic where it is converted into binary coding. When it is inverted with dc signals applied to the NLINV and/or NMINV pins, it becomes twos complement.

After encoding, the signal is applied to the output latch circuits where it is held constant between updates controlled by the application of CONVERT pulses.

The AD9048 uses strobed latching comparators in which comparator outputs are either high or low, as dictated by the analog input level. Data appearing at the output pins have a pipeline delay of one encode cycle.

Input signal levels between the references applied to R_T (Pin 18) and R_B (Pin 26) will appear at the output as binary numbers between 0 and 255, inclusive. Signals outside that range will show up as either full-scale positive or full-scale negative outputs. No damage will occur to the AD9048 as long as the input is within the voltage range of V_{EE} to +0.5V.

The significantly reduced input capacitance of the AD9048 lowers the drive requirements of the input buffer/amplifier and also induces much smaller phase shift in the analog input signal.

Applications which depend on controlled phase shift at the converter input can benefit from using the AD9048 because of its inherently lower phase shift.

The CONVERT, analog input and digital output circuits are shown in Figure 1, AD9048 Input/Output Circuits.

System timing which provides details on delays through the AD9048, as well as the relationships of various timing events, is shown in Figure 2, AD9048 Timing Diagram.

Dynamic performance of the AD9048, i.e., typical signal-to-noise ratio, is illustrated in Figures 3 and 4.

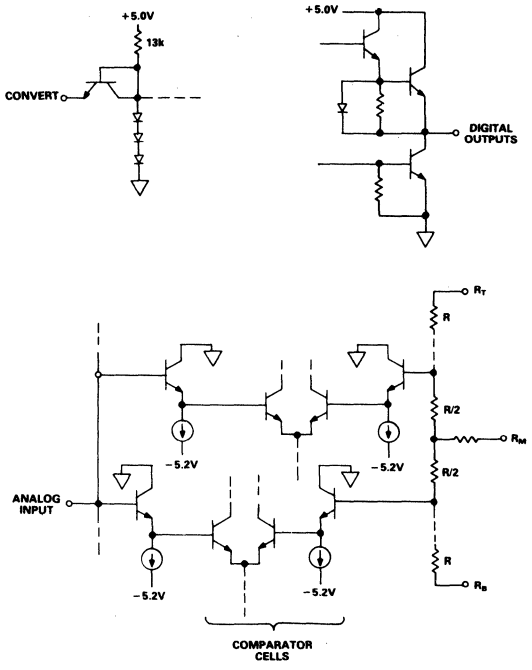


Figure 1. Input/Output Circuits

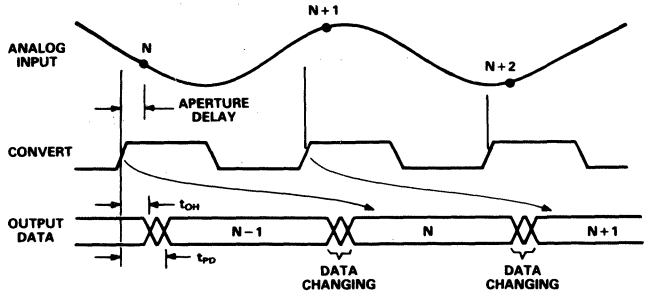


Figure 2. AD9048 Timing Diagram

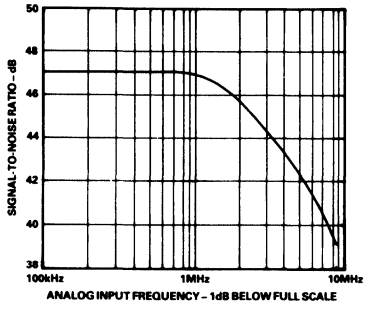


Figure 3. AD9048 Dynamic Performance (20MHz Encode Rate)

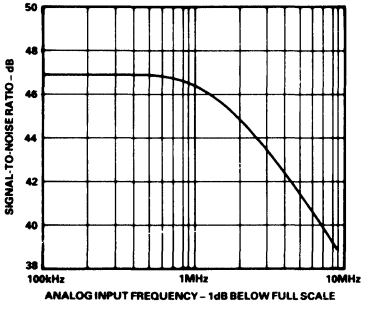


Figure 4. AD9048 Dynamic Performance (35MHz Encode Rate)

LAYOUT SUGGESTIONS

Designs which use the AD9048 or any other high-speed device must follow some basic layout rules to insure optimum performance.

The first requirement is to have a large, low impedance ground plane under and around the converter. If the system uses separate analog and digital grounds, both should be connected solidly together and to the ground plane as close to the AD9048 as practical, to avoid ground loop currents.

Ceramic 0.1μF decoupling capacitors should be placed as close as possible to the supply pins of the AD9048. For decoupling low frequency signals, use 10μF tantalum capacitors, also connected as close as practical to voltage supply pins.

Within the AD9048, reference currents may vary because of coupling between the clock and input signals. Because of this, it is important that the ends of the reference ladder, R_T (Pin 18) and R_B (Pin 28), be connected to low impedances (as measured from ground).

If the AD9048 is being used in a circuit in which the reference is not varied, a bypass capacitor to ground is strongly recommended. In applications which use varying references, they must be driven from a low impedance source.

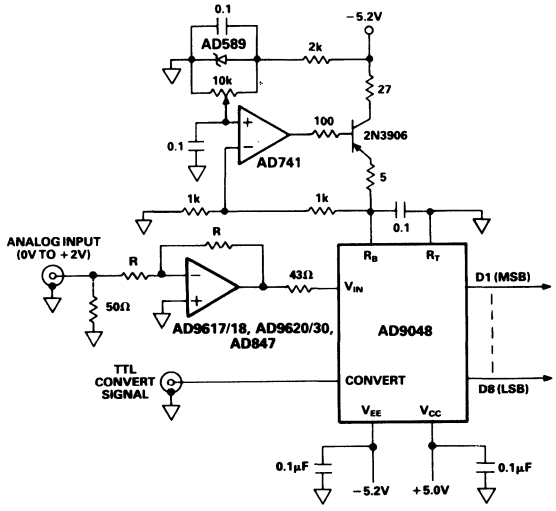


Figure 5. AD9048 Typical Connections

AD9048 Truth Table

Step	Range		Binary		Offset Twos Complement	
			True	Inverted	True	Inverted
	−2.000V FS	−2.0480V FS	NMINV = 1	0	0	1
	7.8431mV Step	8.000mV Step	NLINV = 1	0	1	0
000	0.0000V	0.0000V	00000000	11111111	10000000	01111111
001	−0.0078V	−0.0080V	00000001	11111110	10000001	01111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
127	−0.9961V	−1.0160V	01111111	10000000	11111111	00000000
128	−1.0039V	−1.0240V	10000000	01111111	00000000	11111111
129	−1.0118V	−1.0320V	10000001	01111110	00000001	11111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
254	−1.9921V	−2.0320V	11111110	00000001	01111110	10000001
255	−2.0000V	−2.0400V	11111111	00000000	01111111	10000000

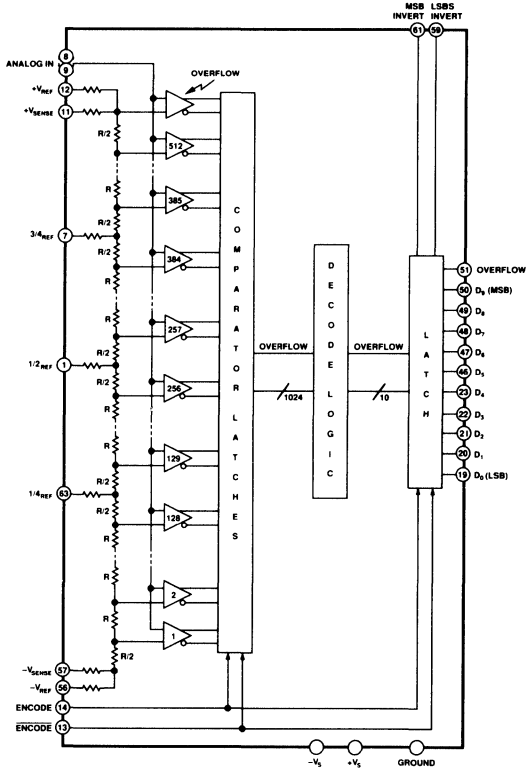
10-Bit, 75 MSPS A/D Converter

AD9060

FEATURES
Monolithic 10-Bit/75 MSPS Converter
ECL Outputs
Bipolar (±1.75 V) Analog Input
57 dB SNR @ 2.3 MHz Input
Low (45 pF) Input Capacitance
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Digital Oscilloscopes
Medical Imaging
Professional Video
Radar Warning/Guidance Systems
Infrared Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9060 A/D converter is a 10-bit monolithic converter capable of word rates of 75 MSPS and above. Innovative architecture using 512 input comparators instead of the traditional 1024 required by other flash converters reduces input capacitance and improves linearity.

Inputs and outputs are ECL-compatible, which makes the AD9060 the recommended choice for systems with conversion rates >30 MSPS, to minimize system noise. An overflow bit is provided to indicate analog input signals greater than $+V_{SENSE}$.

Voltage sense lines are provided to insure accurate driving of the $\pm V_{REF}$ voltages applied to the units. Quarter-point taps on the resistor ladder help optimize the integral linearity of the unit.

Either 68-pin ceramic leaded (gull wing) packages or ceramic LCCs are available and are specifically designed for low thermal impedances. Two performance grades for temperatures of both 0 to +70°C and −55°C to +125°C ranges are offered to allow the user to select the linearity best suited for each application. Dynamic performance is fully characterized and production tested at +25°C. MIL-STD-883 units are available.

The AD9060 A/D converter is available in versions compliant with MIL-STD-883. Refer to the Analog Devices *Military Products Databook* or current AD9060/883B data sheet for detailed specifications.

AD9060—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$	+6 V
$-V_S$	−6 V
ANALOG IN	−2 V to +2 V
$+V_{REF}$, $-V_{REF}$, $3/4_{REF}$, $1/2_{REF}$, $1/4_{REF}$	−2 V to +2 V
$+V_{REF}$ to $-V_{REF}$	4.0 V
ENCODE, $\overline{\text{ENCODE}}$	0 V to $-V_S$
$3/4_{REF}$, $1/2_{REF}$, $1/4_{REF}$ Current	±10 mA
Digital Output Current	20 mA
Operating Temperature	
AD9060JE/KE/JZ/KZ	0 to +70°C
Storage Temperature	−65°C to +150°C
Maximum Junction Temperature[2]	+175°C
Lead Soldering Temp (10 sec)	+300°C

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5 V; $-V_S$ = −5.2 V; $\pm V_{SENSE}$ = ±1.75 V; ENCODE = 60 MSPS unless otherwise noted)[3]

Parameter (Conditions)	Temp	Test Level	AD9060JE/JZ Min	AD9060JE/JZ Typ	AD9060JE/JZ Max	AD9060KE/KZ Min	AD9060KE/KZ Typ	AD9060KE/KZ Max	Units
RESOLUTION			10			10			Bits
DC ACCURACY[3]									
Differential Nonlinearity	+25°C	I		1.0	1.25		0.75	1.0	LSB
	Full	VI			1.5			1.25	LSB
Integral Nonlinearity	+25°C	I		1.25	2.0		1.0	1.5	LSB
	Full	VI			2.5			2.0	LSB
No Missing Codes	Full	VI					Guaranteed		
ANALOG INPUT									
Input Bias Current[4]	+25°C	I		0.4	1.0		0.4	1.0	mA
	Full	VI			2.0			2.0	mA
Input Resistance	+25°C	I	2.0	7.0		2.0	7.0		kΩ
Input Capacitance[4]	+25°C	V		45			45		pF
Analog Bandwidth	+25°C	V		175			175		MHz
REFERENCE INPUT									
Reference Ladder Resistance	+25°C	I	22	37	56	22	37	56	Ω
	Full	VI	14		66	14		66	Ω
Ladder Tempco	Full	V		0.1			0.1		Ω/°C
Reference Ladder Offset									
Top of Ladder	+25°C	I		45	90		45	90	mV
	Full	VI			90			90	mV
Bottom of Ladder	+25°C	I		45	90		45	90	mV
	Full	VI			90			90	mV
Offset Drift Coefficient	Full	V		50			50		μV/°C
SWITCHING PERFORMANCE									
Conversion Rate	+25°C	I	75			75			MSPS
Aperture Delay (t_A)	+25°C	V		1			1		ns
Aperture Uncertainty (Jitter)	+25°C	V		5			5		ps, rms
Output Delay (t_{OD})[5]	+25°C	I	2	4	9	2	4	9	ns
Output Rise Time	+25°C	I		1	3		1	3	ns
Output Fall Time	+25°C	I		1	3		1	3	ns
Output Time Skew[5]	+25°C	I		1.5	3		1.5	3	ns
DYNAMIC PERFORMANCE									
Transient Response	+25°C	V		10			10		ns
Overvoltage Recovery Time	+25°C	V		10			10		ns
Effective Number of Bits (ENOB)									
f_{IN} = 2.3 MHz	+25°C	I	8.7	9.1		8.7	9.1		Bits
f_{IN} = 10.3 MHz	+25°C	IV	8.0	8.6		8.0	8.6		Bits
f_{IN} = 29.3 MHz	+25°C	IV	7.0	7.4		7.0	7.4		Bits
Signal-to-Noise Ratio[6]									
f_{IN} = 2.3 MHz	+25°C	I	54	56		54	56		dB
f_{IN} = 10.3 MHz	+25°C	I	51	54		51	54		dB
f_{IN} = 29.3 MHz	+25°C	I	44	47		44	47		dB

Parameter (Conditions)	Temp	Test Level	AD9060JE/JZ Min	AD9060JE/JZ Typ	AD9060JE/JZ Max	AD9060KE/KZ Min	AD9060KE/KZ Typ	AD9060KE/KZ Max	Units
DYNAMIC PERFORMANCE (CONTINUED)									
Signal-to-Noise Ratio[6] (Without Harmonics)									
f_{IN} = 2.3 MHz	+25°C	I	54	56		54	58		dB
f_{IN} = 10.3 MHz	+25°C	I	51	55		51	55		dB
f_{IN} = 29.3 MHz	+25°C	I	46	48		46	48		dB
Harmonic Distortion									
f_{IN} = 2.3 MHz	+25°C	I	61	65		61	65		dBc
f_{IN} = 10.3 MHz	+25°C	I	55	58		55	58		dBc
f_{IN} = 29.3 MHz	+25°C	I	47	50		47	50		dBc
Two-Tone Intermodulation Distortion Rejection[7]	+25°C	V		70			70		dBc
Differential Phase	+25°C	V		0.5			0.5		Degree
Differential Gain	+25°C	V		1			1		%
ENCODE INPUT									
Logic "1" Voltage	Full	VI	−1.1			−1.1			V
Logic "0" Voltage	Full	VI			−1.5			−1.5	V
Logic "1" Current	Full	VI		150	300		150	300	μA
Logic "0" Current	Full	VI		150	300		150	300	μA
Input Capacitance	+25°C	V		5			5		pF
Pulse Width (High)	+25°C	I	6			6			ns
Pulse Width (Low)	+25°C	I	6			6			ns
DIGITAL OUTPUTS									
Logic "1" Voltage	Full	VI	−1.1			−1.1			V
Logic "0" Voltage	Full	VI			−1.5			−1.5	V
POWER SUPPLY									
$+V_S$ Supply Current	+25°C	VI		420	500		420	500	mA
	Full	VI			500			500	mA
$-V_S$ Supply Current	+25°C	VI		150	180		150	180	mA
	Full	VI			190			190	mA
Power Dissipation	+25°C	VI		2.8	3.3		2.8	3.3	W
	Full	VI			3.5			3.5	W
Power Supply Rejection Ratio (PSRR)[8]	Full	VI		6	10		6	10	mV/V

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances (part soldered onto board): 68-pin leaded ceramic chip carrier: θ_{JC} = 1°C/W; θ_{JA} = 17°C/W (no air flow); θ_{JA} = 15°C/W (air flow = 500 LFM). 68-pin ceramic LCC: θ_{JC} = 2.6°C/W; θ_{JA} = 15°C/W (no air flow); θ_{JA} = 13°C/W (air flow = 500 LFM).

[3]$3/4_{REF}$, $1/2_{REF}$, and $1/4_{REF}$ reference ladder taps are driven from dc sources at +0.875 V, 0 V, and −0.875 V, respectively. Outputs terminated through 100 Ω to −2.0 V; C_L < 4 pF. Accuracy of the overflow comparator is not tested and not included in linearity specifications.

[4]Measured with ANALOG IN = $+V_{SENSE}$.

[5]Output delay measured as worst-case time from 50% point of the rising edge of ENCODE to 50% point of the slowest rising or falling edge of D_0–D_9. Output skew measured as worst-case difference in output delay among D_0–D_9.

[6]RMS signal to rms noise with analog input signal 1 dB below full scale at specified frequency.

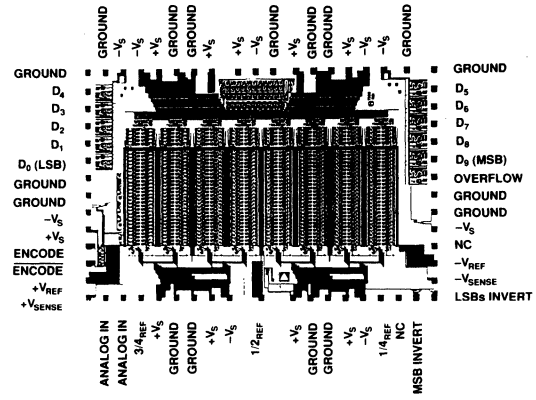
[7]Intermodulation measured with analog input frequencies of 2.3 MHz and 3.0 MHz at 7 dB below full scale.

[8]Measured as the ratio of the worst-case change in transition voltage of a single comparator for a 5% change in $+V_S$ or $-V_S$.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS
Test Level

I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.



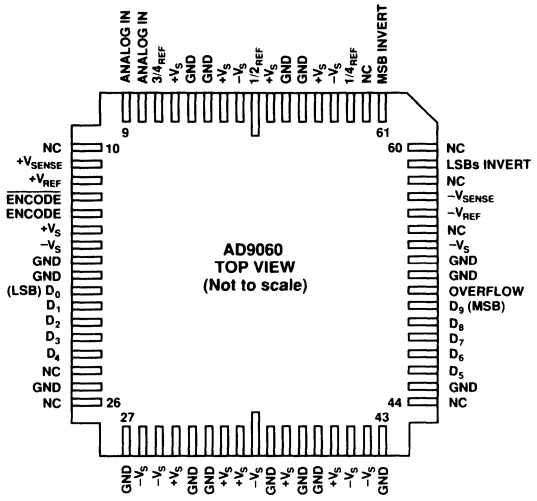
ORDERING GUIDE

Device	Temperature Range	Package Option[1]
AD9060JZ	0 to +70°C	Z-68
AD9060JE	0 to +70°C	E-68A
AD9060KZ	0 to +70°C	Z-68
AD9060KE	0 to +70°C	E-68A
AD9060SZ[2]	−55°C to +125°C	Z-68
AD9060SE[2]	−55°C to +125°C	E-68A
AD9060TZ[2]	−55°C to +125°C	Z-68
AD9060TE[2]	−55°C to +125°C	E-68A
AD9060/PCB	0 to +70°C	Evaluation Board

NOTES
[1]E = Ceramic Leadless Chip Carrier; Z = Ceramic Leaded Chip Carrier. For outline information see Package Information section.
[2]For specifications, refer to Analog Devices *Military Products Databook*.

DIE LAYOUT AND MECHANICAL INFORMATION

Die Dimensions . . . . . 206 × 140 × 15 (±2) mils
Pad Dimensions . . . . . 4 × 4 mils
Metalization . . . . . Gold
Backing . . . . . None
Substrate Potential . . . . . $-V_S$
Passivation . . . . . Nitride



AD9060 Pin Designations

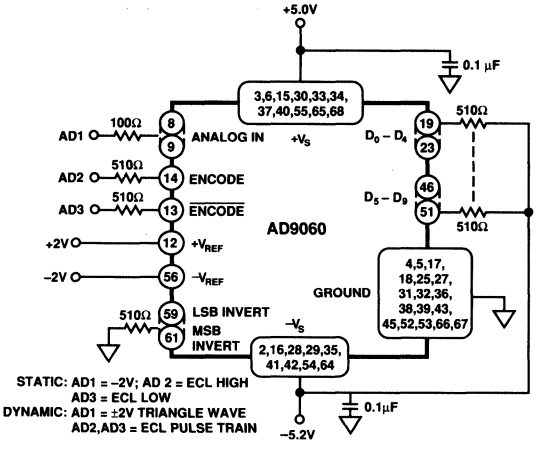
AD9060 PIN DESCRIPTIONS

Pin No.	Name	Function
1	$1/2_{REF}$	Midpoint of internal reference ladder.
2, 16, 28, 29, 35, 41, 42, 54, 64	$-V_S$	Negative supply voltage; nominally −5.2 V ±5%.
3, 6, 15, 30, 33, 34, 37, 40, 65, 68	$+V_S$	Positive supply voltage; nominally +5 V ±5%.
4, 5, 17, 18, 25, 27, 31, 32, 36, 38, 39, 43, 45, 52, 53, 66, 67	GROUND	All ground pins should be connected together and to low-impedance ground plane.
7	$3/4_{REF}$	Three-quarter point of internal reference ladder.
8, 9	ANALOG IN	Analog input; nominally between ±1.75 V.
11	$+V_{SENSE}$	Voltage sense line to most positive point on internal resistor ladder. Normally +1.75 V.
12	$+V_{REF}$	Voltage force connection for top of internal reference ladder. Normally driven to provide +1.75 V at $+V_{SENSE}$.
13	$\overline{\text{ENCODE}}$	Differential ECL convert signal which starts digitizing process.
14	ENCODE	ECL-compatible convert command used to begin digitizing process.
19–23, 46–50	D_0–D_9	ECL-compatible digital output data.
51	OVERFLOW	ECL-compatible output indicating ANALOG IN > $+V_{SENSE}$.
56	$-V_{REF}$	Voltage force connection for bottom of internal reference ladder. Normally driven to provide −1.75 V at $-V_{SENSE}$.
57	$-V_{SENSE}$	Voltage sense line to most negative point on internal resistor ladder. Normally −1.75 V.
59	LSBs INVERT	Normally grounded. When connected to $+V_S$, lower order bits (D_0–D_8) are inverted. Not ECL-compatible.
61	MSB INVERT	Normally grounded. When connected to $+V_S$, most significant bit (MSB; D_9) is inverted. Not ECL-compatible.
63	$1/4_{REF}$	One-quarter point of internal reference ladder.

MIL-STD-883 Compliance Information

The AD9060 devices are classified within Microcircuits Group 57, Technology Group D (bipolar A/D converters) and are constructed in accordance with MIL-STD-883. The AD9060 is electrostatic sensitive and falls within electrostatic sensitivity classification Class 1. Percent Defective Allowance (PDA) is computed based on Subgroup 1 of the specified Group A test list. Quality Assurance (QA) screening is in accordance with Alternate Method A of Method 5005.

The following apply: Burn-In per 1015; Life Test per 1005; Electrical Testing per 5004. (Note: Group A electrical testing assumes $T_A = T_C = T_J$.) MIL-STD-883-compliant devices are marked with "C" to indicate compliance.



AD9060 Burn-In Connections

THEORY OF OPERATION

Refer to the AD9060 block diagram. As shown, the AD9060 uses a modified "flash," or parallel, A/D architecture. The analog input range is determined by an external voltage reference ($+V_{REF}$ and $-V_{REF}$), nominally ±1.75 V. An internal resistor ladder divides this reference into 512 steps, each representing two quantization levels. Taps along the resistor ladder ($1/4_{REF}$, $1/2_{REF}$ and $3/4_{REF}$) are provided to optimize linearity. Rated performance is achieved by driving these points at 1/4, 1/2 and 3/4, respectively, of the voltage reference range.

The A/D conversion for the nine most significant bits (MSBs) is performed by 512 comparators. The value of the least significant bit (LSB) is determined by a unique interpolation scheme between adjacent comparators. The decoding logic processes the comparator outputs and provides a 10-bit code to the output stage of the converter.

Flash architecture has an advantage over other A/D architectures because conversion occurs in one step. This means the performance of the converter is limited primarily by the speed and matching of the individual comparators. In the AD9060, an innovative interpolation scheme takes advantage of flash architecture but minimizes the input capacitance, power and device count usually associated with that method of conversion.

These advantages occur because of using only half the normal number of input comparator cells to accomplish the conversion. In addition, a proprietary decoding scheme minimizes error codes. Input control pins allow the user to select from among Binary, Inverted Binary, Twos Complement and Inverted Twos Complement coding (See AD9060 Truth Table).

APPLICATIONS

Many of the specifications used to describe analog/digital converters have evolved from system performance requirements in these applications. Different systems emphasize particular specifications, depending on how the part is used. The following applications highlight some of the specifications and features that make the AD9060 attractive in these systems.

Wideband Receivers

Radar and communication receivers (baseband and direct IF digitization), ultrasound medical imaging, signal intelligence and spectral analysis all place stringent ac performance requirements on analog-to-digital converters (ADCs). Frequency domain characterization of the AD9060 provides signal-to-noise ratio (SNR) and harmonic distortion data to simplify selection of the ADC.

Receiver sensitivity is limited by the *Signal-to-Noise Ratio (SNR)* of the system. The SNR for an ADC is measured in the frequency domain and calculated with a Fast Fourier Transform (FFT). The SNR equals the ratio of the fundamental component of the signal (rms amplitude) to the rms value of the "noise." The noise is the sum of all other spectral components, including harmonic distortion, but excluding dc.

Good receiver design minimizes the level of spurious signals in the system. Spurious signals developed in the ADC are the result of imperfections in the device transfer function (nonlinearities, delay mismatch, varying input impedance, etc.). In the ADC, these spurious signals appear as *Harmonic Distortion*. Harmonic Distortion is also measured with an FFT and is specified as the ratio of the fundamental component of the signal (rms amplitude) to the rms value of the worst case harmonic (usually the 2nd or 3rd).

Two-Tone Intermodulation Distortion (IMD) is a frequently cited specification in receiver design. In narrow-band receivers, third-order IMD products result in spurious signals in the pass band of the receiver. Like mixers and amplifiers, the ADC is characterized with two, equal-amplitude, pure input frequencies. The IMD equals the ratio of the power of either of the two input signals to the power of the strongest third-order IMD signal. Unlike mixers and amplifiers, the IMD does not always behave as it does in linear devices (reduced input levels do not result in predictable reductions in IMD).

Performance graphs provide typical harmonic and SNR data for the AD9060 for increasing analog input frequencies. In choosing an A/D converter, always look at the dynamic range for the analog input frequency of interest. The AD9060 specifications provide guaranteed minimum limits at three analog test frequencies.

Aperture Delay is the delay between the rising edge of the ENCODE command and the instant at which the analog input is sampled. Many systems require simultaneous sampling of more than one analog input signal with multiple ADCs. In these situations, timing is critical and the absolute value of the aperture delay is not as critical as the matching between devices.

Aperture Uncertainty, or jitter, is the sample-to-sample variation in aperture delay. This is especially important when sampling high slew rate signals in wide bandwidth systems. Aperture uncertainty is one of the factors which degrades dynamic performance as the analog input frequency is increased.

Digitizing Oscilloscopes

Oscilloscopes provide amplitude information about an observed waveform with respect to time. Digitizing oscilloscopes must accurately sample this signal, without distorting the information to be displayed.

One figure of merit for the ADC in these applications is *Effective Number of Bits (ENOBs)*. ENOB is calculated with a sine wave curve fit and equals:

$$ENOB = N - LOG_2 [Error\ (measured)/Error\ (ideal)]$$

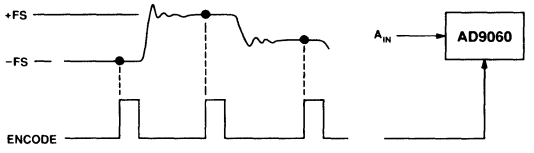
N is the resolution (number of bits) of the ADC. The measured error is the actual rms error calculated from the converter outputs with a pure sine wave input.

The *Analog Bandwidth* of the converter is the analog input frequency at which the spectral power of the fundamental signal is reduced 3 dB from its low frequency value. The analog bandwidth is a good indicator of a converter's slewing capabilities.

The *Maximum Conversion Rate* is defined as the encode rate at which the SNR for the lowest analog signal test frequency tested drops by no more than 3 dB below the guaranteed limit.

Imaging

Visible and infrared imaging systems both require similar characteristics from ADCs. The signal input (from a CCD camera, or multiplexer) is a time division multiplexed signal consisting of a series of pulses whose amplitude varies in direct proportion to the intensity of the radiation detected at the sensor. These varying levels are then digitized by applying encode commands at the correct times, as shown below.



Imaging Application Using AD9060

The actual resolution of the converter is limited by the thermal and quantization noise of the ADC. The low frequency test for SNR or ENOB is a good measure of the noise of the AD9060. At this frequency, the static errors in the ADC determine the useful dynamic range of the ADC.

Although the signal being sampled does not have a significant slew rate, this does not imply dynamic performance is not important. The *Transient Response and Overvoltage Recovery Time* specifications insure that the ADC can track full-scale changes in the analog input sufficiently fast to capture a valid sample.

Transient Response is the time required for the AD9060 to achieve full accuracy when a step function is applied. *Overvoltage Recovery Time* is the time required for the AD9060 to recover to full accuracy after an analog input signal 150% of full scale is reduced to the full-scale range of the converter.

Professional Video

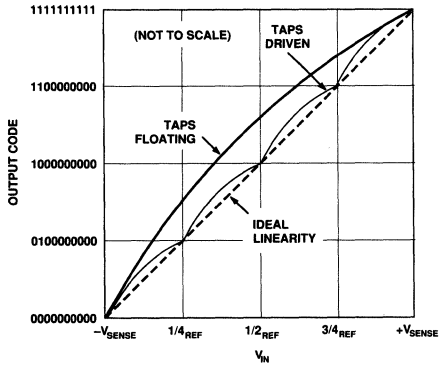
Digital Signal Processing (DSP) is now common in television production. Modern studios rely on digitized video to create state-of-the-art special effects. Video instrumentation also requires high resolution ADCs for studio quality measurement and frame storage.

The AD9060 provides sufficient resolution for these demanding applications. Conversion speed, dynamic performance and analog bandwidth are suitable for digitizing both composite and RGB video sources.

USING THE AD9060

Voltage References

The AD9060 requires that the user provide two voltage references: $+V_{REF}$ and $-V_{REF}$. These two voltages are applied across an internal resistor ladder (nominally 37 Ω) and set the analog input voltage range of the converter. The voltage references should be driven from a stable, low impedance source. In addition to these two references, three evenly spaced taps on the resistor ladder ($1/4_{REF}$, $1/2_{REF}$, $3/4_{REF}$) are available. Providing a reference to these quarter points on the resistor ladder will improve the integral linearity of the converter and improve ac performance. (AC and dc specifications are tested while driving the quarter points at the indicated levels.) The figure below is not intended to show the transfer characteristic of the ADC, but illustrates how the linearity of the device is affected by reference voltages applied to the ladder.

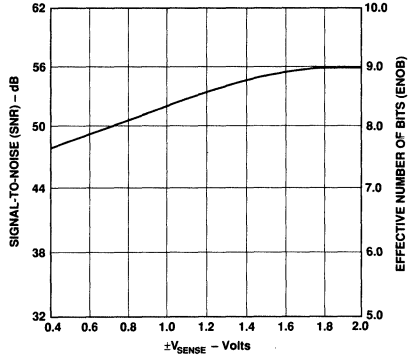


Effect of Reference Taps on Linearity

Resistance between the reference connections and the taps of the first and last comparators causes offset errors. These errors, called "top and bottom of the ladder offsets," can be nulled by using the voltage sense lines, $+V_{SENSE}$ and $-V_{SENSE}$, to adjust the reference voltages. Current through the sense lines should be limited to less than 100 μA. Excessive current drawn through the voltage sense lines will affect the accuracy of the sense line voltage.

The next page shows a reference circuit which nulls out the offset errors using two op amps and provides appropriate voltage references to the quarter-point taps. Feedback from the sense lines causes the op amps to compensate for the offset errors. The two transistors limit the amount of current drawn directly from the op amps; resistors at the base connections stabilize their operation. The 10 kΩ resistors (R1–R4) between the voltage sense lines form an external resistor ladder; the quarter point voltages are taken off this external ladder and buffered by an op amp. The actual values of resistors R1–R4 are not critical, but they should match well and be large enough (≥10 kΩ) to limit the amount of current drawn from the voltage sense lines.

The select resistors (R_S) shown in the schematic (each pair can be a potentiometer) are chosen to adjust the quarter-point voltage references, but are not necessary if R1–R4 match within 0.05%.



AD9060 SNR and ENOB vs. Reference Voltage

An alternative approach for defining the quarter-point references of the resistor ladder is to evaluate the integral linearity error of an individual device, and adjust the voltage at the quarter-points to minimize this error. This may improve the low frequency ac performance of the converter.

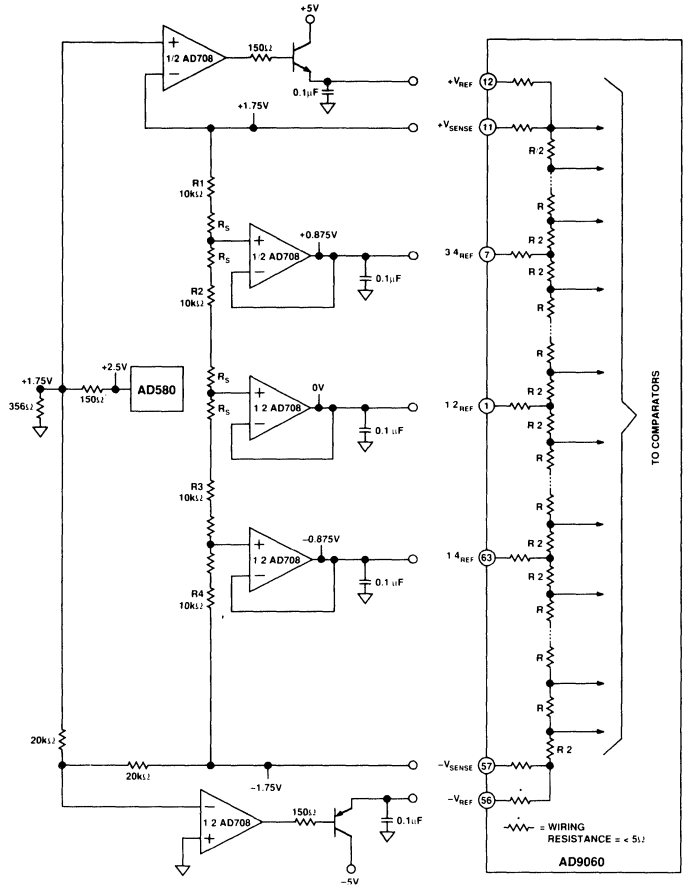
Performance of the AD9060 has been optimized with an analog input voltage of ±1.75 V (as measured at $\pm V_{SENSE}$). If the analog input range is reduced below these values, relatively larger differential nonlinearity errors may result because of comparator mismatches. As shown in the figure below, performance of the converter is a function of $\pm V_{SENSE}$.

Applying a voltage greater than 4 V across the internal resistor ladder will cause current densities to exceed rated values, and may cause permanent damage to the AD9060. The design of the reference circuit should limit the voltage available to the references.

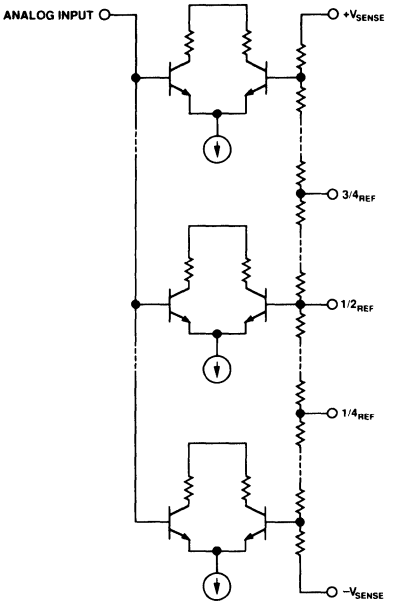
Analog Input Signal

The signal applied to ANALOG IN drives the inputs of 512 parallel comparator cells (see Equivalent Analog Input figure). This connection typically has an input resistance of 7 kΩ, and input capacitance of 45 pF. The input capacitance is nearly constant over the analog input voltage range, as shown in the graph which illustrates that characteristic.

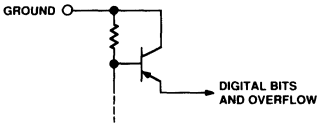
The analog input signal should be driven from a low distortion, low noise amplifier. A good choice is the AD9617, a wide bandwidth, monolithic operational amplifier with excellent ac and dc performance. The input capacitance should be isolated by a small series resistor (24 Ω for the AD9617) to improve the ac performance of the amplifier (see AD9060/PCB Evaluation Board Block Diagram).



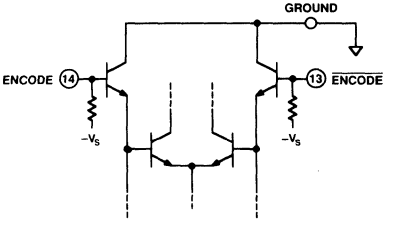
AD9060 Reference Circuit



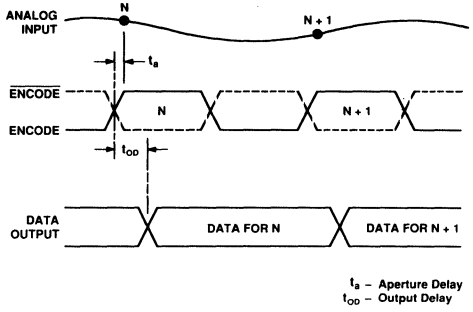
AD9060 Equivalent Analog Input



AD9060 Equivalent Digital Outputs



AD9060 Encode and $\overline{\text{Encode}}$ Equivalent Circuits



AD9060 Timing Diagram

Timing

In the AD9060, the rising edge of the ENCODE signal triggers the A/D conversion by latching the comparators. (See the AD9060 Timing Diagram.) These ENCODE and $\overline{\text{ENCODE}}$ signals are ECL compatible and should be driven differentially. Jitter on the ENCODE signal will raise the noise floor of the converter. Differential signals, with fast clean edges, will reduce the jitter in the signal, and allow optimum ac performance. In applications with a fixed, high frequency encode rate, converter performance is also improved (jitter reduced) by using a crystal oscillator as the system clock.

The AD9060 units are designed to operate with a 50% duty cycle encode signal; adjustment of the duty cycle may improve the dynamic performance of individual devices. Since the ENCODE and $\overline{\text{ENCODE}}$ signals are differential, the logic levels are not critical. Users should remember, however, that reduced logic levels will reduce the slew rate of the edges, and effectively increase the jitter of the signal. ECL terminations for the ENCODE and $\overline{\text{ENCODE}}$ signals should be as close as possible to the AD9060 package to avoid reflections.

In systems where only single-ended signals are available, the use of a high speed comparator (such as the AD96685) is recommended to convert to differential signals. An alternative is to connect +1.3 V (ECL midpoint) to $\overline{\text{ENCODE}}$ and drive the ENCODE connection single ended. In such applications, clean, fast edges are necessary to minimize jitter in the signal.

Output data of the AD9060, D_0–D_9 and OVERFLOW, are also ECL compatible, and should be terminated through 100 Ω to −2 V (or an equivalent load).

Data Format

The format of the output data (D_0–D_9) is controlled by the MSB INVERT and LSBs INVERT pins. These inputs are dc control inputs, and should be connected to GROUND or $+V_S$. The AD9060 Truth Table gives information to choose from among Binary, Inverted Binary, Twos Complement and Inverted Twos Complement coding.

The OVERFLOW output is an indication that the analog input signal has exceeded the voltage at $+V_{SENSE}$. The accuracy of the overflow transition voltage and output delay are not tested or included in the data sheet limits. Performance of the overflow indicator is dependent on circuit layout and slew rate of the encode signal. The operation of this function does not affect the other data bits (D_0–D_9). It is not recommended for applications requiring a critical measure of analog input voltage.

Layout and Power Supplies

Proper layout of high speed circuits is always critical but is particularly important when both analog and digital signals are involved.

Analog signal paths should be kept as short as possible and be properly terminated to avoid reflections. The analog input voltage and the voltage references should be kept away from digital signal paths; this reduces the amount of digital switching noise that is capacitively coupled into the analog section of the circuit.

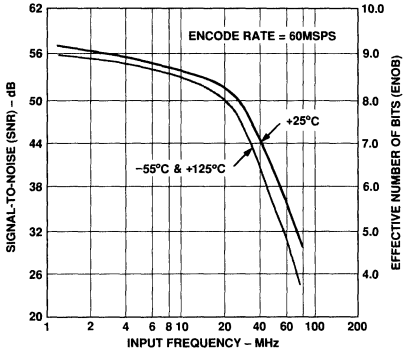
Digital signal paths should also be kept short, and run lengths should be matched to avoid propagation delay mismatch. Terminations for ECL signals should be as close as possible to the receiving gate.

In high speed circuits, layout of the ground circuit is a critical factor. A single, low impedance ground plane, on the component side of the board, will reduce noise on the circuit ground. Power supplies should be capacitively coupled to the ground plane to reduce noise in the circuit. Multilayer boards allow designers to lay out signal traces without interrupting the ground plane and provide low impedance power planes.

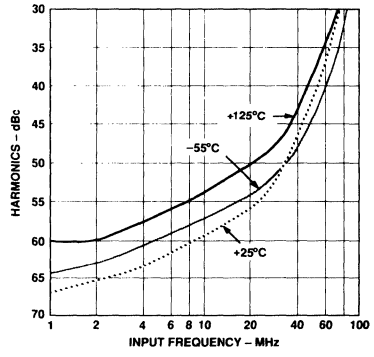
It is especially important to maintain the continuity of the ground plane under and around the AD9060. In systems with dedicated digital and analog grounds, all grounds of the AD9060 should be connected to the analog ground plane.

The power supplies ($+V_S$ and $-V_S$) of the AD9060 should be isolated from the supplies used for external devices; this further reduces the amount of noise coupled into the A/D converter. Sockets limit the dynamic performance and should be used only for prototypes or evaluation—PCK Elastomerics Part No. CCS-68-55 is recommended for the LCC package. (Tel. 215-672-0787)

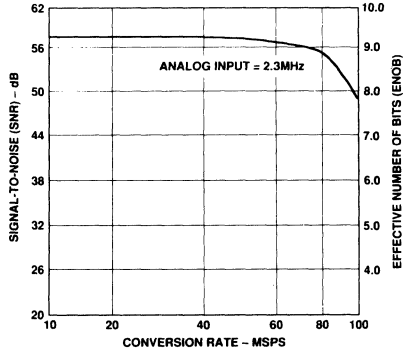
An evaluation board is available to aid designers and provide a suggested layout.



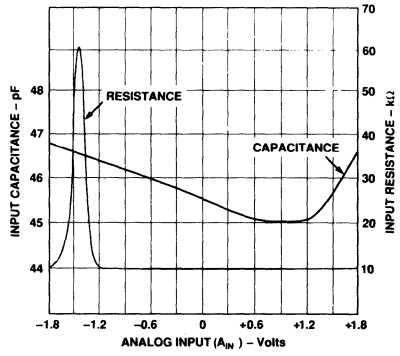
AD9060 SNR and ENOB vs. Input Frequency



AD9060 Harmonics vs. Input Frequency



AD9060 SNR and ENOB vs. Conversion Rate

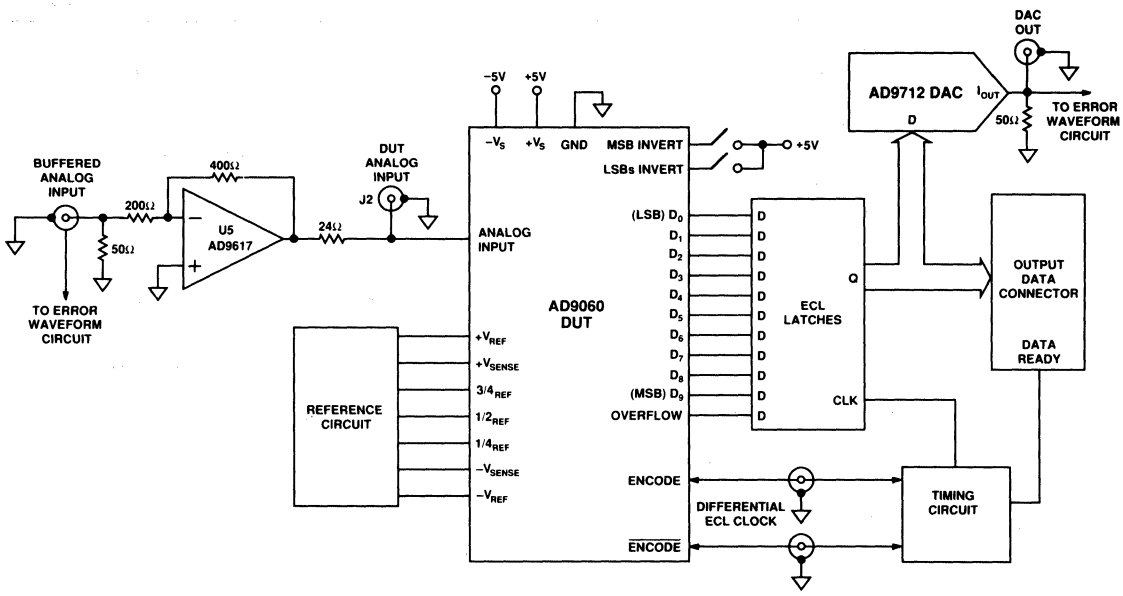


Input Capacitance/Resistance vs. Input Voltage

Step	Range	Offset Binary		Twos Complement	
		True	Inverted	True	Inverted
	0 = −1.75 V FS = +1.75 V	MSB INV = "0" LSBs INV = "0"	MSB INV = "1" LSBs INV = "1"	MSB INV = "1" LSBs INV = "0"	MSB INV = "0" LSBs INV = "1"
1024	>+1.7500	(1)1111111111	(1)0000000000	(1)0111111111	(1)1000000000
1023	+1.7466	1111111111	0000000000	0111111111	1000000000
1022	+1.7432	1111111110	0000000001	0111111110	1000000001
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
512	+0.0034	1000000000	0111111111	0000000000	1111111111
511	0.000	0111111111	1000000000	1111111111	0000000000
510	−0.0034	0111111110	1000000001	1111111110	0000000001
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
02	−1.7432	0000000010	1111111101	1000000010	0111111101
01	−1.7466	0000000001	1111111110	1000000001	0111111110
00	<−1.7466	0000000000	1111111111	1000000000	0111111111

The overflow bit is always 0 except where noted in parentheses ( ). MSB INVERT and LSBs INVERT are considered dc controls.

AD9060 Truth Table



AD9060/PCB Evaluation Board Block Diagram

AD9060/PCB EVALUATION BOARD

The AD9060/PCB Evaluation Board is available from the factory and is shown here in block diagram form. The board includes a reference circuit that allows the user to adjust both references and the quarter-point voltages. The AD9617 is included as the drive amplifier, and the user can configure the gain from −1 to −15.

On-board reconstruction of the digital data is provided through the AD9712, a 12-bit monolithic DAC. The analog and reconstructed waveforms can be summed on the board to allow the user to observe the linearity of the AD9060 and the effects of the quarter-point voltages. The digital data and an adjustable Data Ready signal are available via a 37-pin edge connector.

Audio D/A Converters
Contents

5

Selection Guide
Audio Digital-to-Analog Converters

Model	Res Bits	Channels	SNR 0 dB–dB typ	THD+N % typ	Supplies Volts	Power mW typ	Pins	Page
AD1851	16	Single	110	0.003	±5	100	16	5-3
AD1856	16	Single	No Spec	0.002	±5 to ±12	110	16	5-13
AD1860	18	Single	No Spec	0.002	±5 to ±12	110	16	5-21
AD1861	18	Single	110	0.003	±5	100	16	5-3
AD1862	20	Single	119	0.0012	±5 to ±12	288	16	5-33
AD1864	18	Dual	108	0.0017	±5 to ±12	225	24 / 28	5-43
AD1865	18	Dual	110	0.0017	±5	225	24 / 28	5-55
AD1866	16	Dual	95	0.005	5	45	16	5-65
AD1868	18	Dual	97.5	0.004	5	50	16	5-67

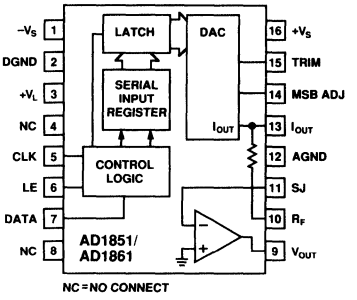
16-Bit/18-Bit, 16× F_S PCM Audio DACs

AD1851/AD1861

FEATURES
110 dB SNR
Fast Settling Permits 16× Oversampling
±3 V Output
Optional Trim Allows Super-Linear Performance
±5 V Operation
16-Pin Plastic DIP and SOIC Packages
Pin-Compatible with AD1856 & AD1860 Audio DACs
2s Complement, Serial Input

APPLICATIONS
High-End Compact Disc Players
Digital Audio Amplifiers
DAT Recorders and Players
Synthesizers and Keyboards

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1851/AD1861 is a monolithic PCM audio DAC. The AD1851 is a 16-bit device, while the AD1861 is an 18-bit device. Each device provides a voltage output amplifier, DAC, serial-to-parallel register and voltage reference. The digital portion of the AD1851/AD1861 is fabricated with CMOS logic elements that are provided by Analog Devices' 2 μm ABCMOS process. The analog portion of the AD1851/AD1861 is fabricated with bipolar and MOS devices as well as thin-film resistors.

This combination of circuit elements, as well as careful design and layout techniques, results in high performance audio playback. Laser-trimming of the linearity error affords low total harmonic distortion. An optional linearity trim pin is provided to allow residual differential linearity error at midscale to be eliminated. This feature is particularly valuable for low distortion reproductions of low amplitude signals. Output glitch is also small, contributing to the overall high level of performance. The output amplifier achieves fast settling and high slew rates, providing a full ±3 V signal at load currents up to 8 mA. When used in current output mode, the AD1851/AD1861 provides a ±1 mA output signal. The output amplifier is short circuit protected and can withstand indefinite shorts to ground.

The serial input interface consists of the clock, data and latch enable pins. The serial 2s complement data word is clocked into the DAC, MSB first, by the external clock. The latch enable signal transfers the input word from the internal serial input register to the parallel DAC input register. The AD1851 input clock can support a 12.5 MHz data rate, while the AD1861 input clock can support a 13.5 MHz data rate. This serial input port is compatible with second generation digital filter chips used in consumer audio products. These filters operate at oversampling rates of 2×, 4×, 8× and 16× sampling frequencies.

The critical specifications of THD+N and signal-to-noise ratio are 100% tested for all devices.

The AD1851/AD1861 operates with ±5 V power supplies, making it suitable for home use markets. The digital supply, V_L, can be separated from the analog supplies, V_S and $-V_S$, for reduced digital crosstalk. Separate analog and digital ground pins are also provided. Power dissipation is 100 mW typical.

The AD1851/AD1861 is available in either a 16-pin plastic DIP or a 16-pin plastic SOIC package. Both packages incorporate the industry standard pinout found on the AD1856 and AD1860 PCM audio DACs. As a result, the AD1851/AD1861 is a drop-in replacement for designs where ±5 V supplies have been used with the AD1856/AD1860. Operation is guaranteed over the temperature range of −25°C to +70°C and over the voltage supply range of ±4.75 V to ±5.25 V.

PRODUCT HIGHLIGHTS

1. AD1851 16-bit resolution provides 96 dB dynamic range. AD1861 18-bit resolution provides 108 dB dynamic range.
2. No external components are required.
3. Operates with ±5 V supplies.
4. Space saving 16-pin SOIC and plastic DIP packages.
5. 100 mW power dissipation.
6. High input clock data rates and 1.5 μs settling time permits 2×, 4×, 8× and 16× oversampling.
7. ±3 V or ±1 mA output capability.
8. THD + Noise and SNR are 100% tested.
9. Pin-compatible with AD1856 & AD1860 PCM audio DACs.

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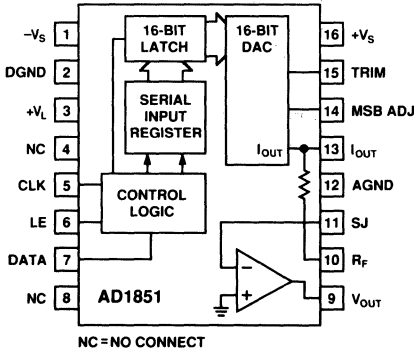
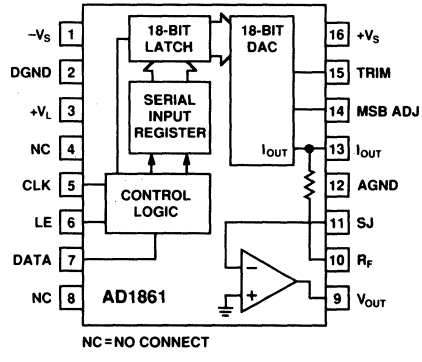
AD1851/AD1861—SPECIFICATIONS (T_A @ +25°C and ±5 V supplies, unless otherwise noted)

	Min	Typ	Max	Units
DIGITAL INPUTS				
V_{IH}	2.0		$+V_L$	V
V_{IL}			0.8	V
I_{IH}, $V_{IH} = V_L$			**1.0**	μA
I_{IL}, $V_{IL} = 0.4$			**−10**	μA
ACCURACY				
Gain Error		±1		%
Midscale Output Voltage		±10		mV
DRIFT (0°C to +70°C)				
Total Drift		±25		ppm of FSR/°C
Bipolar Zero Drift		±4		ppm of FSR/°C
SETTLING TIME (To ±0.0015% of FSR)				
Voltage Output				
6 V Step		1.5		μs
1 LSB Step		1.0		μs
Slew Rate		9		V/μs
Current Output				
1 mA Step 10 Ω to 100 Ω Load		350		ns
1 kΩ Load		350		ns
OUTPUT				
Voltage Output Configuration				
Bipolar Range	**±2.88**	±3.0	**±3.12**	V
Output Current	±8			mA
Output Impedance		0.1		Ω
Short Circuit Duration		Indefinite to Common		
Current Output Configuration				
Bipolar Range (±30%)		±1.0		mA
Output Impedance (±30%)		1.7		kΩ
POWER SUPPLY				
Voltage				
$+V_L$ and $+V_S$	4.75		5.25	V
$-V_S$	−5.25		−4.75	V
TEMPERATURE RANGE				
Specification	0	+25	+70	°C
Operation	−25		+70	°C
Storage	−60		+100	°C
WARMUP TIME	1			min

Specifications subject to change without notice.



AD1851 Functional Block Diagram



AD1861 Functional Block Diagram

AD1851

	Min	Typ	Max	Units
RESOLUTION			**16**	Bits
TOTAL HARMONIC DISTORTION + NOISE				
0 dB, 990.5 Hz				
AD1851N-J, R-J		0.003	**0.004**	%
AD1851N, R		0.004	**0.008**	%
−20 dB, 990.5 Hz				
AD1851N-J, R-J		0.009	**0.016**	%
AD1851N, R		0.009	**0.040**	%
−60 dB, 990.5 Hz				
AD1851N-J, R-J		0.9	**1.6**	%
AD1851N, R		0.9	**4.0**	%
D-RANGE* (With A-Weight Filter)				
−60 dB, 990.5 Hz AD1851N, R	**88**			dB
AD185IN-J, R-J	**96**			dB
SIGNAL-TO-NOISE RATIO	**107**	110		dB
MAXIMUM CLOCK INPUT FREQUENCY	**12.5**			MHz
ACCURACY				
Differential Linearity Error		±0.001		% of FSR
MONOTONICITY		14		Bits
POWER SUPPLY				
Current				
+I		10.0	**13.0**	mA
−I		−10.0	**−15.0**	mA
Power Dissipation		100		mW

AD1861

	Min	Typ	Max	Units
RESOLUTION			**18**	Bits
TOTAL HARMONIC DISTORTION + NOISE				
0 dB, 990.5 Hz				
AD1861N-J, R-J		0.003	**0.004**	%
AD1861N, R		0.004	**0.008**	%
−20 dB, 990.5 Hz				
AD1861N-J, R-J		0.009	**0.016**	%
AD1861N, R		0.009	**0.040**	%
−60 dB, 990.5 Hz				
AD1861N-J, R-J		0.9	**1.6**	%
AD1861N, R		0.9	**4.0**	%
D-RANGE* (With A-Weight Filter)				
−60 dB, 990.5 Hz AD1861N, R	**88**			dB
AD186IN-J, R-J	**96**			dB
SIGNAL-TO-NOISE RATIO	**107**	110		dB
MAXIMUM CLOCK INPUT FREQUENCY	**13.5**			MHz
ACCURACY				
Differential Linearity Error		±0.001		% of FSR
MONOTONICITY		15		Bits
POWER SUPPLY				
Current				
+I		10.0	**13.0**	mA
−I		−10.0	**−15.0**	mA
Power Dissipation		100		mW

*Tested in accordance with EIAJ Test Standard CP-307.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_L to DGND . . . . . 0 V to 6.50 V
V_S to AGND . . . . . 0 V to 6.50 V
$-V_S$ to AGND . . . . . −6.50 V to 0 V
Digital Inputs to DGND . . . . . −0.3 V to V_L
AGND to DGND . . . . . ±0.3 V
Short Circuit . . . . . Indefinite Short to Ground
Soldering . . . . . +300°C, 10 sec
Storage Temperature . . . . . −60°C to +100°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENTS

1	$-V_S$	ANALOG NEGATIVE POWER SUPPLY
2	DGND	LOGIC GROUND
3	V_L	LOGIC POSITIVE POWER SUPPLY
4	NC	NO CONNECTION
5	CLK	CLOCK INPUT
6	LE	LATCH ENABLE INPUT
7	DATA	SERIAL DATA INPUT
8	NC	NO INTERNAL CONNECTION*
9	V_{OUT}	VOLTAGE OUTPUT
10	R_F	FEEDBACK RESISTOR
11	SJ	SUMMING JUNCTION
12	AGND	ANALOG GROUND
13	I_{OUT}	CURRENT OUTPUT
14	MSB ADJ	MSB ADJUSTMENT TERMINAL
15	TRIM	MSB TRIMMING POTENTIOMETER TERMINAL
16	V_S	ANALOG POSITIVE POWER SUPPLY

*PIN 8 HAS NO INTERNAL CONNECTION; $-V_L$ FROM AD1856 OR AD1860 SOCKET CAN BE SAFELY APPLIED.

CAUTION

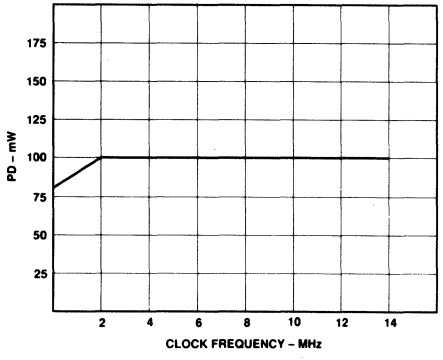
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

ORDERING GUIDE

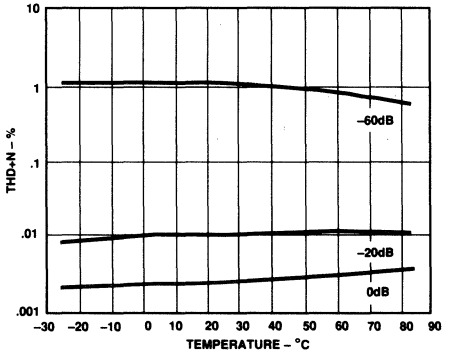
Model	Resolution	THD+N	Package Option*
AD1851N	16 Bits	0.008%	N-16
AD1851N-J	16 Bits	0.004%	N-16
AD1851R	16 Bits	0.008%	R-16A
AD1851R-J	16 Bits	0.004%	R-16A
AD1861N	18 Bits	0.008%	N-16
AD1861N-J	18 Bits	0.004%	N-16
AD1861R	18 Bits	0.008%	R-16A
AD1861R-J	18 Bits	0.004%	R-16A

*N = Plastic DIP Package; R = Small Outline (SOIC) Package.
For outline information see Package Information section.

Typical Performance



Power Dissipation vs. Clock Frequency



THD vs. Temperature

TOTAL HARMONIC DISTORTION

Total harmonic distortion plus noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the values of the first 19 harmonics and noise to the value of the fundamental input frequency. It is usually expressed in percent (%).

THD+N is a measure of the magnitude and distribution of linearity error, differential linearity error, quantization error and noise. The distribution of these errors may be different, depending on the amplitude of the output signal. Therefore, to be most useful, THD+N should be specified for both large (0 dB) and small signal amplitudes (−20 dB and −60 dB).

The THD+N figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. This specification, therefore, provides a direct method to classify and choose an audio DAC for a desired level of performance.

SETTLING TIME

Settling time is the time required for the output of the DAC to reach and remain within a specified error band about its final value, measured from the digital input transition. It is a primary measure of dynamic performance.

MIDSCALE ERROR

Midscale error, or bipolar zero error, is the deviation of the actual analog output from the ideal output (0 V) when the 2s complement input code representing half scale is loaded in the input register.

D-RANGE DISTORTION

D-range distortion is equal to the value of the total harmonic distortion + noise (THD+N) plus 60 dB when a signal level of −60 dB below full scale is reproduced. D-range is tested with a 1 kHz input sine wave. This is measured with a standard A-weight filter as specified by EIAJ Standard CP-307.

SIGNAL-TO-NOISE RATIO

The signal-to-noise ratio (SNR) is defined as the ratio of the amplitude of the output when a full-scale output is present to the amplitude of the output with no signal present. This is measured with a standard A-weight filter as specified by EIAJ Standard CP-307.

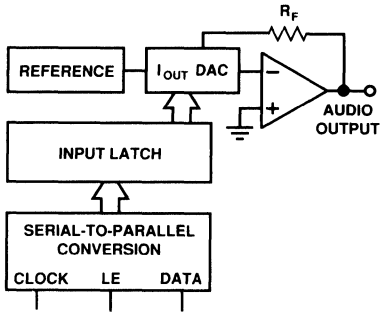


Figure 1. AD1851/AD1861 Functional Block Diagram

FUNCTIONAL DESCRIPTION

The AD1851/AD1861 is a complete monolithic PCM audio DAC. No additional external components are required for operation. As shown in Figure 1 above, each chip contains a voltage reference, an output amplifier, a DAC, an input latch and a parallel input register.

The voltage reference consists of a bandgap circuit and buffer amplifier. This combination of elements produces a reference voltage that is unaffected by changes in temperature and age. The DAC output voltage, which is derived from the reference voltage, is also unaffected by these environmental changes.

The output amplifier uses both MOS and bipolar devices to produce low offset, high slew rate and optimum settling time. When combined with the on-chip feedback resistor, the output op amp converts the output current of the AD1851/AD1861 to a voltage output.

The DAC uses a combination of segmented decoder and R-2R architecture to achieve consistent linearity and differential linearity. The resistors which form the ladder structure are fabricated with silicon chromium thin film. Laser-trimming of these resistors further reduces linearity error, resulting in low output distortion.

The input register and serial-to-parallel converter are fabricated with CMOS logic gates. These gates allow the achievement of fast switching speeds and low power consumption. This contributes to the overall low power dissipation of the AD1851/AD1861.

Analog Circuit Considerations

GROUNDING RECOMMENDATIONS

The AD1851/AD1861 has two ground pins, designated Analog and Digital ground. The analog ground pin is the "high quality" ground reference point for the device. The analog ground pin should be connected to the analog common point in the system. The output load should also be connected to that same point.

The digital ground pin returns ground current from the digital logic portions of the AD1851/AD1861 circuitry. This pin should be connected to the digital common point in the system.

As illustrated in Figure 2, the analog and digital grounds should be connected together at one point in the system.

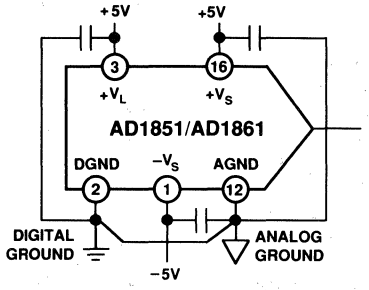


Figure 2. Recommended Circuit Schematic

POWER SUPPLIES AND DECOUPLING

The AD1851/AD1861 has three power supply input pins. The $\pm V_S$ supplies provide the supply voltages to operate the linear portions of the DAC including the voltage reference, output amplifier and control amplifier. The $\pm V_S$ supplies are designed to operate at ± 5 V.

The $+V_L$ supply operates the digital portions of the chip including the input shift register and the input latching circuitry. The $+V_L$ supply is designed to operate at $+5$ V.

Decoupling capacitors should be used on all power supply pins. Furthermore, good engineering practice suggests that these capacitors be placed as close as possible to the package pins as well as to the common points. The logic supply, $+V_L$, should be decoupled to digital common, while the analog supplies, $\pm V_S$, should be decoupled to analog common.

The use of three separate power supplies will reduce feedthrough from the digital portion of the system to the linear portion of the system, thus contributing to improved performance.

However, three separate voltage supplies are not necessary for good circuit performance. For example, Figure 3 illustrates a system where only a single positive and a single negative supply are available.

In this example, the positive logic and positive analog supplies must both be connected to $+5$ V, while the negative analog supply will be connected to -5 V. Performance would benefit from a measure of isolation between the supplies introduced by using simple low pass filters in the individual power supply leads.

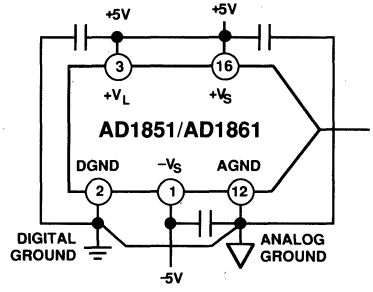


Figure 3. Alternate Recommended Schematic

As with most linear circuits, changes in the power supplies will affect the output of the DAC. Analog Devices recommends that well regulated power supplies with less than 1% ripple be incorporated into the design of any system using the AD1851/AD1861.

OPTIONAL MSB ADJUSTMENT

Use of an optional adjustment circuit allows residual differential linearity error around midscale to be eliminated. This error is especially important when low amplitude signals are being reproduced. In those cases, as the signal amplitude decreases, the ratio of the midscale differential linearity error to the signal amplitude increases, thereby increasing THD.

Therefore, for best performance at low output levels, the optional MSB adjust circuitry shown in Figure 4 may be used to improve performance. The adjustment should be made with a small signal input (-20 dB or -60 dB).

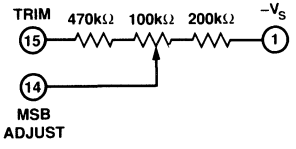


Figure 4. Optional THD Adjust Circuit

AD1851 DIGITAL CIRCUIT CONSIDERATIONS

AD1851 Input Data

Data is transmitted to the AD1851 in a bit stream composed of 16-bit words with a serial, MSB first format. Three signals must be present to achieve proper operation. They are the Data, Clock and Latch Enable (LE) signals. Input data bits are clocked into the input register on the rising edge of the Clock signal. The LSB is clocked in on the 16th clock pulse. When all data bits are loaded, a low-going Latch Enable pulse updates the DAC input. Figure 5 illustrates the general signal requirements for data transfer to the AD1851.

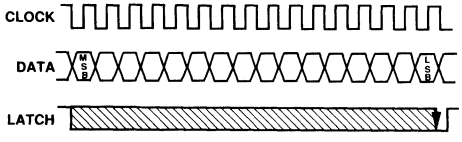


Figure 5. Signal Requirements for AD1851

Figure 6 illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished properly. The input pins of the AD1851 are both TTL and 5 V CMOS compatible. The input requirements illustrated in Figures 5 and 6 are compatible with data outputs provided by popular DSP filter chips used in digital audio playback systems. The AD1851 input clock can run at a 12.5 MHz rate. This clock rate will allow data transfer rates for 2×, 4× or 8× or 16× oversampling reconstructions.

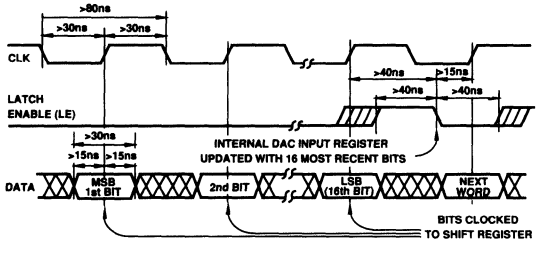


Figure 6. Timing Relationships of AD1851 Input Signals

AD1861 DIGITAL CIRCUIT CONSIDERATIONS

AD1861 Input Data

Data is transmitted to the AD1861 in a bit stream composed of 18-bit words with a serial, MSB first format. Three signals must be present to achieve proper operation. They are the Data, Clock and Latch Enable (LE) signals. Input data bits are clocked into the input register on the rising edge of the Clock signal. The LSB is clocked in on the 18th clock pulse. When all data bits are loaded, a low-going Latch Enable pulse updates the DAC input. Figure 7 illustrates the general signal requirements for data transfer to the AD1861.

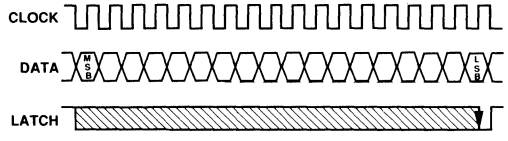


Figure 7. Signal Requirements for AD1861

Figure 8 illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished properly. The input pins of the AD1861 are both TTL and 5 V CMOS compatible. The input requirements illustrated in Figures 7 and 8 are compatible with data outputs provided by popular DSP filter chips used in digital audio playback systems. The AD1861 input clock can run at a 13.5 MHz rate. This clock rate will allow data transfer rates for 2×, 4× or 8× or 16× oversampling reconstructions.

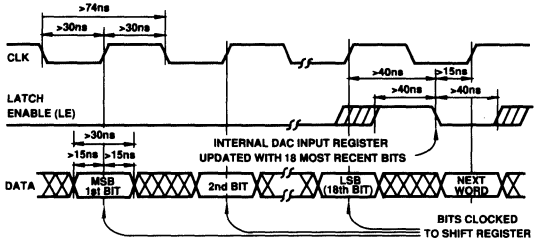


Figure 8. Timing Relationships of AD1861 Input Signals

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APPLICATIONS

Figures 9 through 12 show connection diagrams for the AD1851 and AD1861 and the Yamaha YM3434 and the NPC SM5813AP/APT digital filter chips.

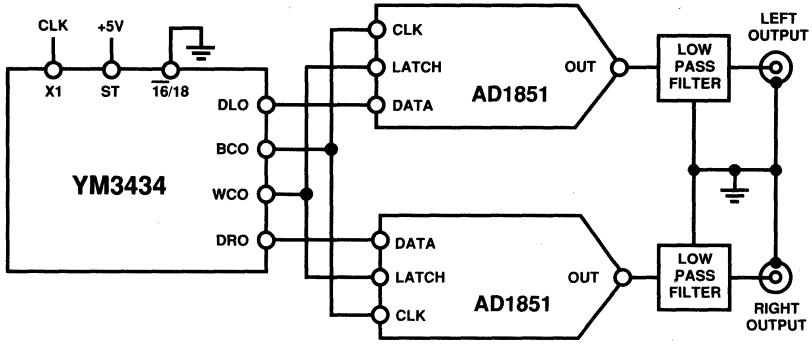

Figure 9. AD1851 with Yamaha YM3434 Digital Filter

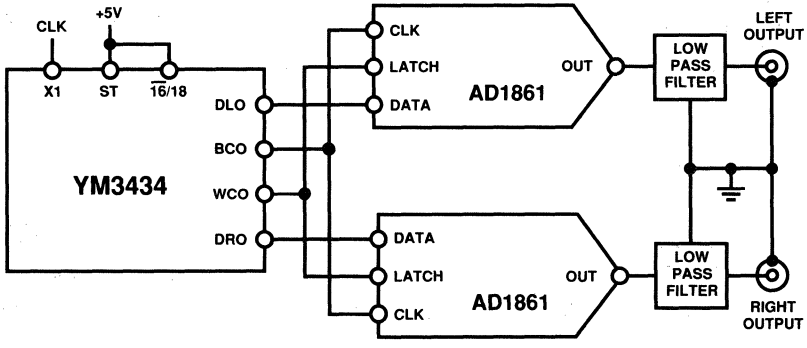

Figure 10. AD1861 with Yamaha YM3434 Digital Filter

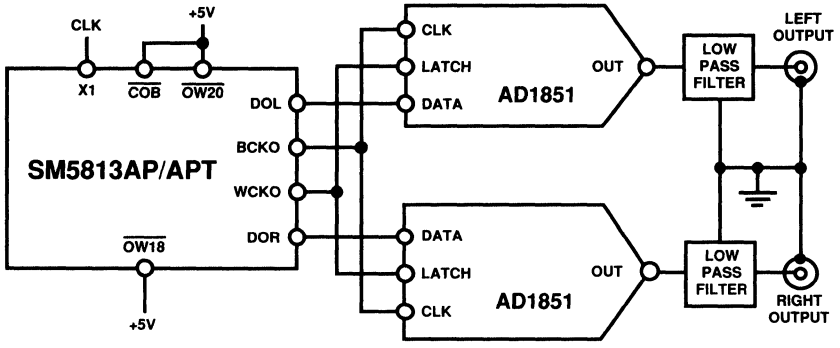

Figure 11. AD1851 with NPC SM5813AP/APT Digital Filter

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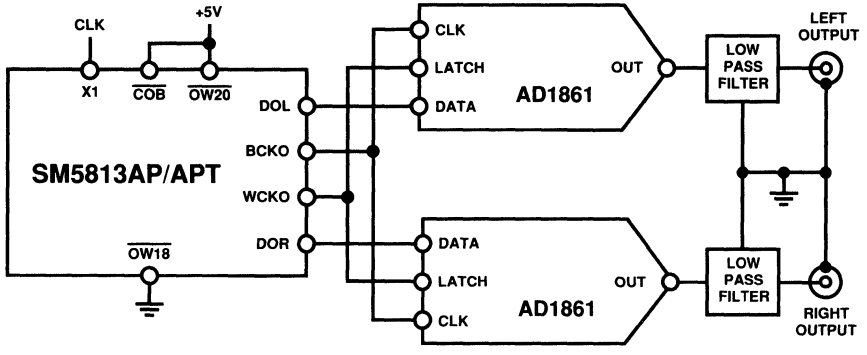


Figure 12. AD1861 with NPC SM5813AP/APT Digital Filter

ANALOG DEVICES

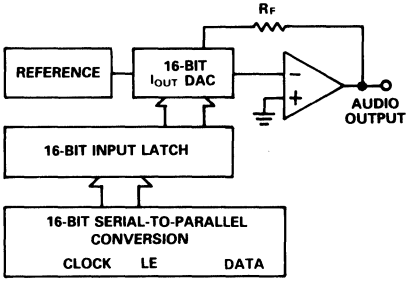
16-Bit PCM Audio DAC

AD1856

FEATURES
0.0025% THD
Fast Settling Permits 2×, 4× or 8× Oversampling
±3V Output
Optional Trim Allows Superlinear Performance
±5V to ±12V Operation
16-Pin Plastic DIP or SOIC Package
Serial Input

APPLICATIONS
Compact Disc Players
Digital Audio Amplifiers
DAT Recorders and Players
Synthesizers and Keyboards

BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1856 is a monolithic 16-bit PCM Audio DAC. Each device provides a voltage output amplifier, 16-bit DAC, 16-bit serial-to-parallel input register and voltage reference. The digital portion of the AD1856 is fabricated with CMOS logic elements that are provided by Analog Devices' BiMOS II process. The analog portion of the AD1856 is fabricated with bipolar and MOS devices as well as thin film resistors.

This combination of circuit elements, as well as careful design and layout techniques, results in high performance audio playback. Laser trimming of the linearity error affords extremely low total harmonic distortion. An optional linearity trim pin is provided to allow residual differential linearity error at midscale to be eliminated. This feature is particularly valuable for low distortion reconstructions of low amplitude signals. Output glitch is also small contributing to the overall high level of performance. The output amplifier achieves fast settling and high slew rates, providing a full ±3V signal at load currents up to 8mA. The output amplifier is short circuit protected and can withstand indefinite shorts to ground.

The serial input interface consists of the clock, data and latch enable pins. The serial 2s complement data word is clocked into the DAC, MSB first, by the external data clock. The latch enable signal transfers the input word from the internal serial input register to the parallel DAC input register. The input clock can support a 10MHz clock rate. This serial input port is compatible with popular digital filter chips used in consumer audio products. These filters operate at oversampling rates of 2×, 4× and 8× sampling frequency.

The AD1856 can operate with ±5V to ±12V power supplies making it suitable for both the portable and home-use markets. The digital supplies, V_L and $-V_L$, can be separated from the analog supplies, V_S and $-V_S$, for reduced digital crosstalk. Separate analog and digital ground pins are also provided.

Power dissipation is 110mW typical with ±5V supplies and is a typical 300mW when ±12V supplies are used.

The AD1856 is packaged in a 16-pin plastic DIP or SOIC package and incorporates the industry-standard pinout. Operation is guaranteed over the temperature range of −25°C to +70°C and over the voltage supply range of ±4.75 to ±13.2V.

PRODUCT HIGHLIGHTS

1. Total harmonic distortion is 100% tested.
2. MSB trim feature allows superlinear operation.
3. The AD1856 operates with ±5V to ±12V supplies.
4. Serial interface is compatible with digital filter chips.
5. 1.5µs settling time permits 2×, 4× and 8× oversampling.
6. No external components are required.
7. 96dB dynamic range.
8. ±3V or ±1mA output capability.
9. 16-bit resolution.
10. 2s complement serial input words.
11. Low cost.
12. 16-pin plastic DIP or SOIC package.

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AD1856—SPECIFICATIONS (typical at T_A = +25°C and ±5V supplies unless otherwise noted)

		Min	Typ	Max	Units
RESOLUTION				**16**	Bits
DIGITAL INPUTS	V_{IH}	2.4		V_L	V
	V_{IL}	0		0.8	V
	I_{IH},V_{IH} = V_L			**1.0**	μA
	I_{IL},V_{IL} = 0.4			**−10**	μA
Clock Input Frequency		**10**			MHz
ACCURACY					
Gain Error			±2.0		%
Bipolar Zero Error			±30		mV
Differential Linearity Error			±0.001		% of FSR
Noise (rms, 20Hz to 20kHz) @ Bipolar Zero			6		μV
TOTAL HARMONIC DISTORTION					
0dB, 990.5Hz	AD1856N-K, R-K		0.002	**0.0025**	%
	AD1856N-J, R-J		0.002	**0.004**	%
	AD1856N, R		0.002	**0.008**	%
−20dB, 990.5Hz	AD1856N-K, R-K		0.018	**0.020**	%
	AD1856N-J, R-J		0.018	**0.040**	%
	AD1856N, R		0.018	**0.040**	%
−60dB, 990.5Hz	AD1856N-K, R-K		1.8	**2.0**	%
	AD1856N-J, R-J		1.8	**4.0**	%
	AD1856N, R		1.8	**4.0**	%
MONOTONICITY			15		Bits
DRIFT (0 to +70°C)					
Total Drift			±25		ppm of FSR/°C
Bipolar Zero Drift			±4		ppm of FSR/°C
SETTLING TIME (to ±0.006% of FSR)					
Voltage Output	6V Step		1.5		μs
	1LSB Step		1.0		μs
	Slew Rate		9		V/μs
Current Output	1mA Step 10Ω to 100Ω Load		350		ns
	1kΩ Load		350		ns
WARM-UP TIME		1			min
OUTPUT					
Voltage Output Configuration					
Bipolar Range			±3		V
Output Current		±8			mA
Output Impedance			0.1		Ω
Short Circuit Duration			Indefinite to Common		
Current Output Configuration					
Bipolar Range (±30%)			1.0		mA
Output Impedance (±30%)			1.7		kΩ
POWER SUPPLY					
Voltage, $+V_L$ and $+V_S$		4.75	5	13.2	V
Voltage, $-V_L$ and $-V_S$		−13.2	−5	−4.75	V
Current, +I, V_L and V_S = +5V, 10MHz Clock			10	**15**	mA
Current, −I, $-V_L$ and $-V_S$ = −5V, 10MHz Clock			−12	**−15**	mA
Current, +I, V_L and V_S = +12V, 10MHz Clock			12		mA
Current, −I, $-V_L$ and $-V_S$ = −12V, 10MHz Clock			−15		mA
POWER DISSIPATION					
V_S and V_L = ±5V, 10MHz Clock			110	**150**	mW
V_S and V_L = ±12V, 10MHz Clock			135		mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operation		−25		+70	°C
Storage		−60		+100	°C

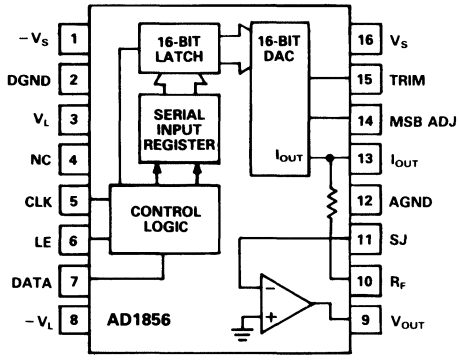
Specifications subject to change without notice.
Specifications shown in **boldface** are tested on all production units at final test.

ABSOLUTE MAXIMUM RATINGS*

V_L to DGND . . . . . 0 to 13.2V
V_S to AGND . . . . . 0 to 13.2V
$-V_L$ to DGND. . . . . -13.2 to 0V
$-V_S$ to AGND . . . . . -13.2 to 0V
Digital Inputs to DGND . . . . . -0.3 to V_L
AGND to DGND . . . . . ± 0.3V
Short Circuit Protection . . . . . Indefinite Short to Ground
Soldering . . . . . +300°C, 10sec
Storage Temperature . . . . . −60°C to +100°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM



PIN DESIGNATIONS

Pin	Function	Description
1	$-V_S$	Analog Negative Power Supply
2	DGND	Digital Ground
3	V_L	Logic Positive Power Supply
4	NC	No Connection
5	CLK	Data Clock Input
6	LE	Latch Enable Input
7	DATA	Serial Data Input
8	$-V_L$	Logic Negative Power Supply
9	V_{OUT}	Voltage Output
10	R_F	Feedback Resistor
11	SJ	Summing Junction
12	AGND	Analog Ground
13	I_{OUT}	Current Output
14	MSB ADJ	MSB Adjustment Terminal
15	TRIM	MSB Trimming Potentiometer Terminal
16	V_S	Analog Positive Power Supply

5

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

Definition of Specifications

TOTAL HARMONIC DISTORTION

Total Harmonic Distortion (THD) is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental input frequency. It is expressed in percent (%) or decibels (dB).

THD is a measure of the magnitude and distribution of linearity error and differential linearity error. The distribution of these errors may be different, depending on the amplitude of the output signal. Therefore, to be most useful, THD should be specified for both large and small signal amplitudes.

SETTLING TIME

Settling Time is the time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition. It is the primary measure of dynamic performance.

DYNAMIC RANGE

Dynamic Range is the specification that indicates the ratio of the smallest signal the converter can resolve to the largest signal it is able to produce. As a ratio, it is usually expressed in decibels (dB). The theoretical dynamic range of an n-bit converter is approximately (6×n) dB. In the case of the 16-bit AD1856, that is 96dB. The actual dynamic range of a converter is less than the theoretical value due to limitations imposed by noise and quantization and other errors.

BIPOLAR ZERO ERROR

Bipolar Zero Error is the deviation in the actual analog output from the ideal output (0V) when the 2s complement input code representing half scale (all 0s) is loaded in the input register.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in the digital input. Monotonic behavior requires that the differential linearity error not exceed 1LSB in the negative direction.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

FUNCTIONAL DESCRIPTION

The AD1856 is a complete, monolithic 16-bit PCM audio DAC. No additional external components are required for operation. As shown in the block diagram, each chip contains a voltage reference, an output amplifier, a 16-bit DAC, a 16-bit input latch and a 16-bit serial-to-parallel input register.

The voltage reference consists of a bandgap circuit and buffer amplifier. This circuitry produces an output voltage that is stable over time and temperature changes.

The 16-bit D/A converter uses a combination of segmented decoder and R-2R architectures to achieve consistent linearity and differential linearity. The resistors which form the ladder structure are fabricated with silicon-chromium thin film. Laser trimming of these resistors further reduces linearity error resulting in low output distortion.

The output amplifier uses both MOS and bipolar devices to produce low offset, high slew-rate and optimum settling time. When combined with the on-board feedback resistor, the output op amp can convert the output current of the AD1856 to a voltage output.

ANALOG CIRCUIT CONSIDERATIONS

GROUNDING RECOMMENDATIONS

The AD1856 has two ground pins, designated ANALOG and DIGITAL ground. The analog ground pin is the "high quality" ground reference point for the device. The analog ground pin should be connected to the analog common point in the system. The output load should also be connected to that same point.

The digital ground pin returns ground current from the digital logic portions of the AD1856 circuitry. This pin should be connected to the digital common point in the system.

As illustrated in Figure 1, the analog and digital grounds should be connected together at one point in the system.

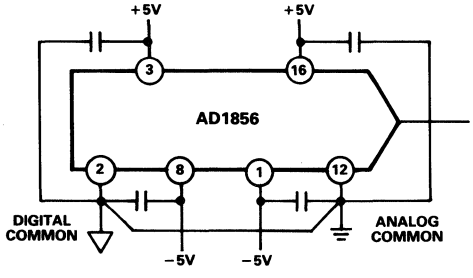


Figure 1. Recommended Circuit Schematic

POWER SUPPLIES AND DECOUPLING

The AD1856 has four power supply input pins. $\pm V_S$ provide the supply voltages to operate the linear portions of the DAC including the voltage reference, output amplifier and control amplifier. The $\pm V_S$ supplies are designed to operate from ±5V to ±12V.

The $\pm V_L$ supplies operate the digital portions of the chip including the input shift register and the input latching circuitry. The $\pm V_L$ supplies are also designed to operate from ±5V to ±12V subject only to the limitation that $-V_L$ may not be more negative than $-V_S$.

Decoupling capacitors should be used on all power supply pins. Furthermore, good engineering practice suggests that these capacitors be placed as close as possible to the package pins as well as the common points. The logic supplies, $\pm V_L$, should be decoupled to digital common; and the analog supplies, $\pm V_S$, should be decoupled to analog common.

The use of four separate power supplies will reduce feedthrough from the digital portion of the system to the linear portions of the system, thus contributing to good performance. However,

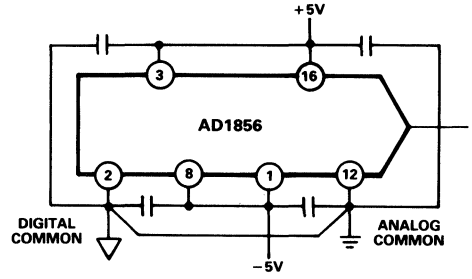


Figure 2. Alternate Recommended Schematic

four separate voltage supplies are not necessary for good circuit performance. For example, Figure 2 illustrates a system where only a single positive and a single negative supply are available. Given that these two supplies are within the range of ±5V to ±12V, they may be used to power the AD1856. In this case, the positive logic and positive analog supplies may both be connected to the single positive supply. The negative logic and negative analog supplies may both be connected to the single negative supply. Performance would benefit from a measure of isolation between the supplies introduced by using simple low-pass filters in the individual power supply leads.

As with most linear circuits, changes in the power supplies will affect the output of the DAC. Analog Devices recommends that well regulated power supplies with less than 1% ripple be incorporated into the design of any system using these devices.

TOTAL HARMONIC DISTORTION

The THD figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. The THD specification, therefore, provides a direct method to classify and choose an audio DAC for a desired level of performance.

Analog Devices tests and grades all AD1856s on the basis of THD performance. A block diagram of the test setup is shown in Figure 3. In this test setup, a digital data stream, representing a 0db, −20dB or −60dB sine wave is sent to the device under test. The frequency of this waveform is 990.5Hz. Input data is sent to the AD1856 at a $4\times F_S$ rate (176.4kHz). The AD1856 under test produces an analog output signal with the on-board op amp.

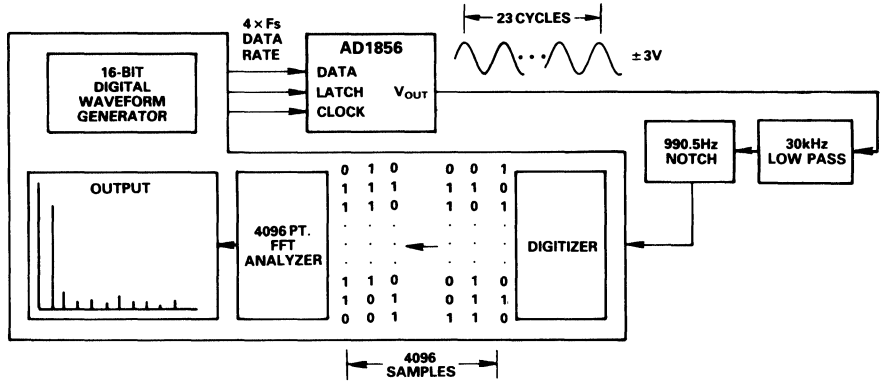


Figure 3. Block Diagram of Distortion Test Circuit

The automatic test equipment digitizes 4096 samples of the output test waveform, incorporating 23 complete cycles of the sine wave. A 4096 point FFT is performed on the results of the test. Based on the first 9 harmonics of the fundamental 990.5Hz output wave, the total harmonic distortion of the device is calculated. Neither a deglitcher nor an MSB trim is used during the THD test.

The circuit design, layout and manufacturing techniques employed in the production of the AD1856 result in excellent THD performance. Figure 4 shows the typical unadjusted THD performance of the AD1856 for various amplitudes of a 1kHz output signal. As can be seen, the AD1856 offers excellent performance, even at amplitudes as low as −60dB. Figure 5 illustrates the typical THD vs. frequency performance.

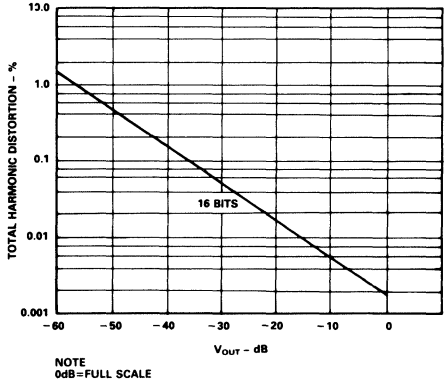


Figure 4. Typical Unadjusted THD vs. Amplitude

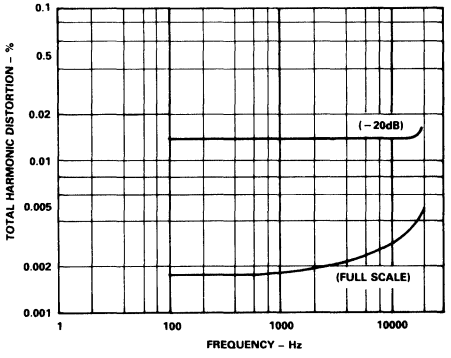


Figure 5. Typical THD vs. Frequency

OPTIONAL MSB ADJUSTMENT

Use of an optional adjustment circuit allows residual differential linearity errors around midscale to be eliminated. These errors are especially important when low amplitude signals are being reproduced. In those cases, as the signal amplitude decreases, the ratio of the midscale differential linearity error to the signal amplitude increases and THD increases.

Therefore, for best performance at low output levels, the optional MSB adjust circuitry shown in Figure 6 may be used. This circuit allows the differential linearity error at midscale to be zeroed out. However, no adjustments are required to meet data sheet specifications.

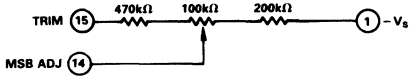


Figure 6. Optional THD Adjust Circuit

DIGITAL CIRCUIT CONSIDERATIONS

Input Data

Data is transmitted to the AD1856 in a bit stream composed of 16-bit words with a serial, MSB first format. Three signals must be present to achieve proper operation: the Data, Clock and Latch Enable signals. Input data bits are clocked into the input register on the rising edge of the Clock signal. The LSB is clocked in on the 16th clock pulse. When all data bits are loaded, a low-going Latch Enable pulse updates the DAC input. Figure 7 illustrates the general signal requirements for data transfer for the AD1856.

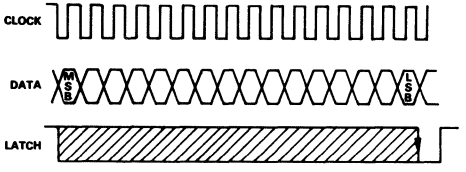


Figure 7. Signal Requirements of AD1856

Figure 8 provides the specific timing requirements that must be met in order for the data transfer to be accomplished properly.

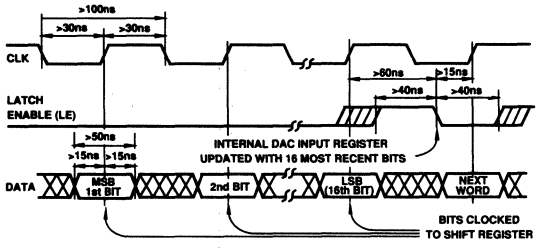


Figure 8. Timing Relationships of Input Signals

The input pins of the AD1856 are both TTL and 5V CMOS compatible, independent of power supply voltages used.

The input requirements illustrated in Figures 7 and 8 are compatible with the data outputs provided by popular DSP filter chips used in digital audio playback systems. The AD1856 input clock can run at a 10MHz rate. This clock rate will allow data transfer rates for 2×, 4× or 8× oversampling reconstruction. The application section of this data sheet contains additional guides for using the AD1856 with various DSP filter chips available from Sony, NPC and Yamaha.

APPLICATIONS OF THE AD1856 PCM AUDIO DAC

The AD1856 is a versatile digital-to-analog converter designed for applications in consumer digital audio equipment. Portable, car and home compact disc player, digital audio-amplifier and DAT systems can all use the AD1856. Various circuit architectures are popular in these systems. They include stereo playback sections featuring one DAC per system, one DAC per audio channel (left/right) or even multiple DACs per channel. Furthermore, these architectures use different output reconstruction rates to accomplish these functions including reproduction at the sample rate F_S (1×), at twice the sample rate (2×F_S), at four times the sample rate (4×F_S) and even at eight times the sample rate (8×F_S). F_S is 44.1kHz for CD and 48kHz for DAT applications.

One DAC per System

Figure 9 shows a circuit using one AD1856 per system to reproduce both stereo channels of a typical first generation digital

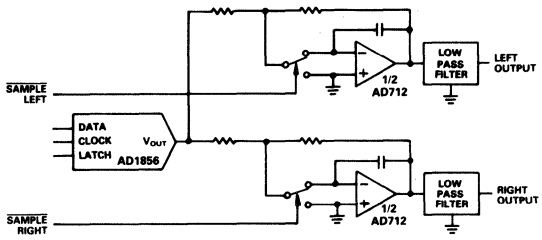


Figure 9. AD1856 in a One DAC per System Architecture

audio system. The input data is fed to the AD1856 in a format which alternates between left channel data and right channel data. The output of the AD1856 is switched between the left channel and right channel output sample/hold amplifiers (SHAs). The SHAs demultiplex and deglitch the output of the AD1856. The timing diagram for the control signals for this circuit is shown in Figure 10.

The architecture illustrated in Figure 9 is suitable for low-end home or portable systems. However, its usefulness in mid- or high-end digital audio reproduction is limited by the phase delay which is introduced in the multiplexed output. This phase delay is due to the fact that the information contained in the input bit stream represents left and right channel audio sampled simultaneously but reconstructed alternately. One obvious solution to this problem may be arrived at by incorporating a third, noninverting SHA to delay the output of one channel to "catch up to" the other channel. This eliminates the phase shift by restoring simultaneous reproduction. This solution is illustrated in Figure 11.

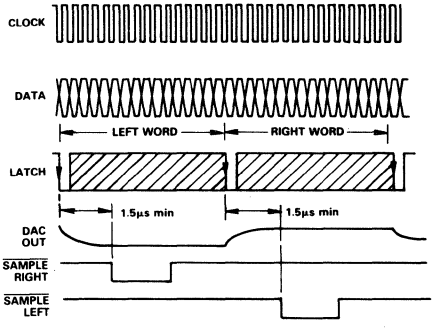


Figure 10. Control Signals for One DAC Circuit

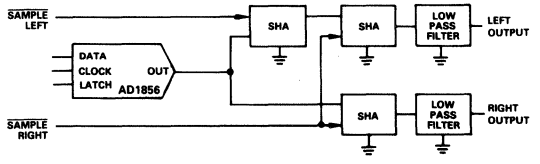


Figure 11. Third SHA Eliminates Phase Delay

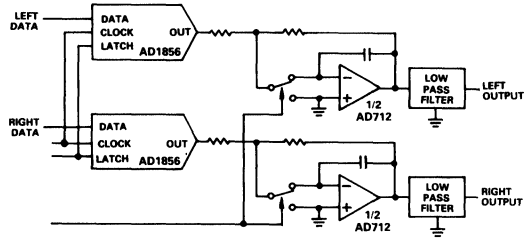


Figure 12. One DAC per Channel Architecture

One DAC per Channel

Another approach used to eliminate phase delay between left and right channels employs one DAC per channel. In this architecture, the input data bit streams for the left channel and the right channel are simultaneously sent and latched into each DAC. This "second generation" approach, shown in Figure 12, is suitable for higher performance digital-audio playback units.

Two DACs per Channel (Four DAC System)

Another architecture uses two DACs per channel. In this scheme, shown in Figure 13, each DAC reproduces one half of the output waveform. The advantage obtained is that midscale differential linearity error no longer effects the zero-crossing points of the waveforms. Its effects are shifted to the points where the output waveform crosses ±3/4 full scale. The result is that THD performance for low amplitude signals is greatly improved. Not shown in Figure 13 is a VLSI circuit required to separate the incoming data into the appropriate form required by each DAC.

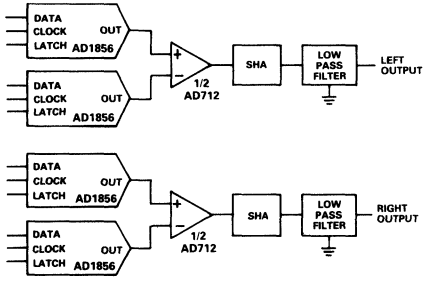


Figure 13. Two DACs per Channel Eliminate Midscale Distortion from the Zero-Crossing Points

DIGITAL FILTERING AND OVERSAMPLING

Oversampling is a term which refers to playback techniques in which the reconstruction frequency used is an integral (2 or more) multiple of the original quantized data rate. For example, in compact disc stereo digital audio playback units, the original quantized data sample rate is 44.1kHz. Popular oversampling rates are 2× or 4× F_S yielding reconstruction rates of 88.2 and 176.4kHz, respectively.

Oversampling is used to ease the performance constraints of the low-pass filters which usually follow the reconstruction DAC. In any signal reconstructed from sampled data, unwanted frequency components are introduced in the output spectrum; these components are centered at the reconstruction frequency.

When a 44.1kHz reconstruction frequency is used, the actual frequency band of interest is 20Hz to 20kHz, and the band of unwanted "image" frequency components extends from 44.1kHz to approximately 24kHz and from 44.1kHz to 64kHz. These unwanted components must be removed with a low-pass filter of very high order. First generation digital audio systems often use low-pass filters of 9, 11 and even 13 poles. Linear implementations of these filters are expensive, difficult to manufacture and can produce distortion due to varying group delay characteristics.

When a 2× reconstruction frequency (88.2kHz) is used, the lowest unwanted frequency components now extend down to approximately 68kHz. A 4× rate (176.4kHz) has unwanted components extending down to approximately 156kHz. The filter response needed to remove these frequency components can now be less steep. This means that a lower order filter may be used resulting in less distortion at lower cost. Linear filters with 3 or 5 poles are adequate to do the job and are quite common in digital audio products employing oversampling techniques.

Oversampling techniques require that the serial input data stream run at the same integral multiple of the original data rate. So, while the constraints on the output low-pass filter are eased, the constraints on the serial digital input port and the settling time of the output stage are not.

The actual oversampling operation takes place in the digital filter chip which is located "upstream" from the DAC. The digital filter accepts data from the media and adds the additional reconstruction points according to the algorithm and coefficients stored in the filter chip. Since the digital filters actually interpolate these additional reconstruction points, they have earned the name "interpolation filters."

The AD1856 is compatible with popular digital filter chips used in digital audio products such as the NPC SM5807, NPC SM5805, Yamaha YM3414, and Sony CXD1136.

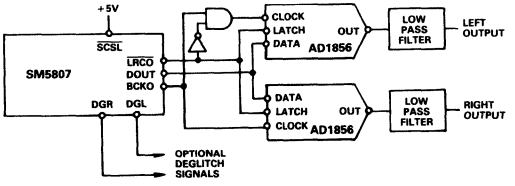


Figure 14. NPC SM5807 and AD1856 Interface

DUAL DAC, 4× F_S OVERSAMPLING ARCHITECTURE

Figure 14 illustrates the use of an NPC digital filter chip with two AD1856 audio DACs. This scheme achieves four times oversampling reconstruction with a dedicated DAC per channel. In this example of a typical compact disc player application, the digital filter chip accepts serial input words from the digital decoder/processor at a 44.1kHz sample rate. Through the use of oversampling, the SM5807 transmits data to the two DACs at a 176.4kHz rate. The serial DAC input data is sent out of the DOUT pin to the serial inputs of the DACs. Left channel and right channel data are sent alternately down the same wire. The Left/Right Channel Output signal, $\overline{\text{LRCO}}$ and two logic gates demultiplex the data clock signals from BCKO. In this example,

the BCKO rate is 192×F_S. However, a 196×F_S clock can be used if $\overline{SCSL}$ is wired to a logic zero. Finally, left and right channel deglitching signals are provided. At the user's option, these signals may be used to control external sample-hold amplifiers in order to obtain optimal performance.

ACHIEVING 8× F_S OVERSAMPLING WITH AD1856S AND YAMAHA YM3414

Figure 15 illustrates the combination of a Yamaha YM3414 digital filter chip and two AD1856 audio DACs. In this scheme, the use of a 16.9344MHz clock allows an 8 times oversampling rate for extremely high performance. In addition, a lower-order low-pass filter may be used without sacrificing performance. The DAC input data is simultaneously transmitted to the input registers of the DACs through dedicated left and right channel output pins on the YM3414. As before, optional sample/hold signals are provided.

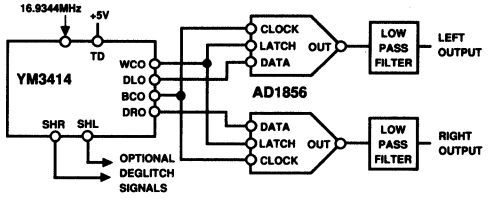


Figure 15. Yamaha YM3414 and AD1856 Interface

ORDERING GUIDE

Model	THD @ FS	Package Option*
AD1856N, R	0.008%	N-16, R-16A
AD1856N-J, R-J	0.004%	N-16, R-16A
AD1856N-K, R-K	0.0025%	N-16, R-16A

*N = Plastic DIP; R = Small Outline IC. For outline information see Package Information section.

ANALOG DEVICES

18-Bit PCM Audio DAC

AD1860

FEATURES
0.002% THD + Noise
Fast Settling Permits 8× Oversampling
±3V Output
Optional Trim Allows Superlinear Performance
±5V to ±12V Operation
16-Pin Plastic DIP and SOIC Packages
Industry Standard Pinout
2s Complement, Serial Input

APPLICATIONS
High End Compact Disc Players
Digital Audio Amplifiers
DAT Recorders and Players
Synthesizers and Keyboards

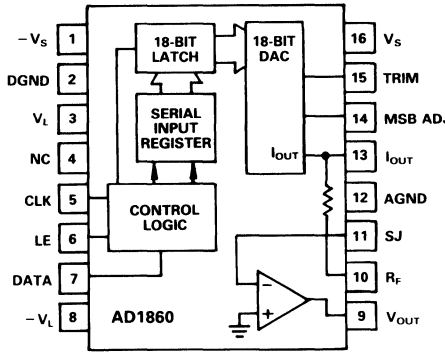
PRODUCT DESCRIPTION

The AD1860 is a monolithic 18-bit PCM Audio DAC. Each device provides a voltage output amplifier, 18-bit DAC, 18-bit serial to parallel input register and voltage reference. The digital portion of the AD1860 is fabricated with CMOS logic elements that are provided by Analog Devices' BiMOS II process. The analog portion of the AD1860 is fabricated with bipolar and MOS devices as well as thin film resistors.

This combination of circuit elements, as well as careful design and layout techniques, results in high performance audio playback. Laser trimming of the linearity error affords extremely low total harmonic distortion. An optional linearity trim pin is provided to allow residual differential linearity error at midscale to be eliminated. This feature is particularly valuable for low distortion reproductions of low amplitude signals. Output glitch is also small contributing to the overall high level of performance. The output amplifier achieves fast settling and high slew rates, providing a full ±3V signal at load currents up to 8mA. When used in current output mode, the AD1860 provides a ±1mA output signal. The output amplifier is short circuit protected and can withstand indefinite shorts to ground.

The serial input interface consists of the clock, data and latch enable pins. The serial 2s complement data word is clocked into the DAC, MSB first, by the external data clock. The latch enable signal transfers the input word from the internal serial input register to the parallel DAC input register. The input clock can support a 12.5MHz data rate. This serial input port is compatible with second generation digital filter chips used in consumer audio products. These filters operate at oversampling rates of 2×, 4× and 8× sampling frequencies.

FUNCTIONAL BLOCK DIAGRAM



The AD1860 can operate with ±5V to ±12V power supplies making it suitable for both the portable and home use markets. The digital supplies, V_L and $-V_L$, can be separated from the analog supplies, V_S and $-V_S$, for reduced digital crosstalk. Separate analog and digital ground pins are also provided.

Power dissipation is 110mW typical with ±5V supplies and is 225mW typical when +5V/−12V supplies are used.

The AD1860 is available in either a 16-pin plastic DIP or a 16-pin plastic SOIC surface mount package. Operation is guaranteed over the temperature range of −25°C to +70°C and over the voltage supply range of ±4.75 to ±13.2V.

PRODUCT HIGHLIGHTS

1. 18-bit resolution provides 108dB dynamic range.
2. No external components are required.
3. Operates with ±5V to ±12V supplies.
4. 16-pin DIP or space saving SOIC package.
5. 110mW power dissipation.
6. 1.5μs settling time permits 2×, 4× and 8× oversampling.
7. ±3V or ±1mA output capability.
8. THD + Noise is 100% tested.

5

AD1860—SPECIFICATIONS (T_A at +25°C and ±5V supplies unless otherwise noted)

	Min	Typ	Max	Units
RESOLUTION			**18**	Bits
DIGITAL INPUTS V_{IH}	2.0		$+V_L$	V
V_{IL}			0.8	V
I_{IH}, $V_{IH}=V_L$			**1.0**	μA
I_{IL}, $V_{IL}=0.4$			**−10**	μA
Clock Input Frequency	**12.5**			MHz
ACCURACY				
Gain Error		±2.0		%
Midscale Output Voltage		±30		mV
Differential Linearity Error		±0.001		% of FSR
TOTAL HARMONIC DISTORTION + NOISE				
0dB, 990.5Hz AD1860N-K, R-K		0.002	**0.0025**	%
AD1860N-J, R-J		0.002	**0.004**	%
AD1860N, R		0.004	**0.008**	%
−20dB, 990.5Hz AD1860N-K, R-K		0.006	**0.020**	%
AD1860N-J, R-J		0.010	**0.020**	%
AD1860N, R		0.010	**0.040**	%
−60dB, 990.5Hz AD1860N-K, R-K		0.9	**2.0**	%
AD1860N-J, R-J		0.9	**2.0**	%
AD1860N, R		0.9	**4.0**	%
SIGNAL TO NOISE RATIO (A-Weight Filter)	**102**	108		dB
DRIFT (0 to +70°C)				
Total Drift		±25		ppm of FSR/°C
Bipolar Zero Drift		±4		ppm of FSR/°C
SETTLING TIME (to ±0.0015% of FSR)				
Voltage Output, 6V Step		1.5		μs
1LSB Step		1.0		μs
Slew Rate		9		V/μs
Current Output 1mA Step 10Ω to 100Ω Load		350		ns
1kΩ Load		350		ns
MONOTONICITY		15		Bits
OUTPUT				
Voltage Output Configuration				
Bipolar Range	**±2.88**	±3.0	**±3.12**	V
Output Current	±8			mA
Output Impedance		0.1		Ω
Short Circuit Duration		Indefinite to Common		
Current Output Configuration				
Bipolar Range (±30%)		±1.0		mA
Output Impedance (±30%)		1.7		kΩ
POWER SUPPLY				
Voltage V_L and V_S	4.75		13.2	V
Voltage $-V_L$ and $-V_S$	−13.2		−4.75	V
Current +I, V_L and $V_S=5V$, 10MHz Clock		10.0	**13.0**	mA
−I, $-V_L$ and $-V_S=-5V$, 10MHz Clock		12.0	**−15.0**	mA
Current +I, V_L and $V_S=12V$, 10MHz Clock		10.5		mA
−I, $-V_L$ and $-V_S=-12V$, 10MHz Clock		13.5		mA
Current +I, V_L and $+V_S=+5V$, 10MHz Clock		10		mA
−I, $-V_L$ and $-V_S=-12V$, 10MHz Clock		14		mA
POWER DISSIPATION				
V_S and $V_L=\pm5V$, 10MHz Clock		110		mW
V_S and $V_L=\pm12V$, 10MHz Clock		288		mW
V_S and $V_L=+5V$, $-V_S$ and $-V_L=-12V$, 10MHz Clock		318		mW

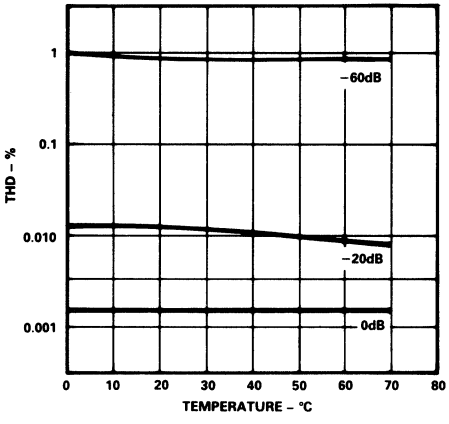
	Min	Typ	Max	Units
TEMPERATURE RANGE				
Specification	0	+25	+70	°C
Operation	−25		+70	°C
Storage	−60		+100	°C
WARMUP TIME	1			min

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

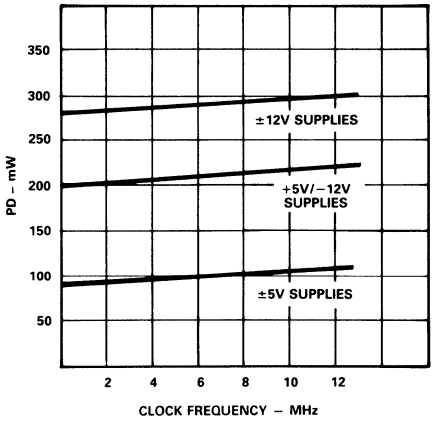
V_L to DGND . . . . . 0 to 13.2V
V_S to AGND . . . . . 0 to 13.2V
$-V_L$ to DGND . . . . . −13.2 to 0V
$-V_S$ to AGND . . . . . −13.2 to 0V
Digital Inputs to DGND . . . . . −0.3 to V_L
AGND to DGND . . . . . ± 0.3V
Short Circuit . . . . . Indefinite Short to Ground
Soldering . . . . . +300°C, 10sec
Storage Temperature . . . . . −60°C to +100°C

Note
*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

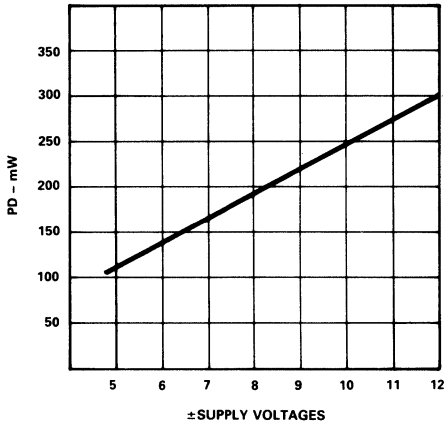


THD vs. Temperature

TYPICAL PERFORMANCE



Power Dissipation vs. Clock Frequency

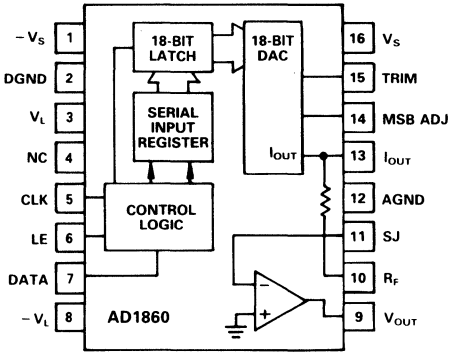


Power Dissipation vs. Supply Voltages

5

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



Functional Block Diagram

PIN ASSIGNMENTS

1	$-V_S$	Analog Negative Power Supply
2	DGND	Logic Ground
3	V_L	Logic Positive Power Supply
4	NC	No Connection
5	CLK	Data Clock Input
6	LE	Latch Enable Input
7	DATA	Serial Data Input
8	$-V_L$	Logic Negative Power Supply
9	V_{OUT}	Voltage Output
10	R_F	Feedback Resistor
11	SJ	Summing Junction
12	AGND	Analog Ground
13	I_{OUT}	Current Output
14	MSB ADJ	MSB Adjustment Terminal
15	TRIM	MSB Trimming Potentiometer Terminal
16	V_S	Analog Positive Power Supply

ORDERING GUIDE

Model	THD @ FS	Package Option*
AD1860N	0.008%	N-16
AD1860R	0.008%	R-16A
AD1860N-J	0.004%	N-16
AD1860R-J	0.004%	R-16A
AD1860N-K	0.0025%	N-16
AD1860R-K	0.0025%	R-16A

*N = Plastic DIP; R = Small Outline IC (Surface Mount Package). For outline information see Package Information section.

TOTAL HARMONIC DISTORTION + NOISE

Total Harmonic Distortion plus Noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the value of the fundamental input frequency. It is usually expressed in percent (%).

THD+N is a measure of the magnitude and distribution of linearity error, differential linearity error, quantization error and noise. The distribution of these errors may be different, depending on the amplitude of the output signal. Therefore, to be most useful, THD+N should be specified for both large and small signal amplitudes.

SETTLING TIME

Settling Time is the time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition. It is a primary measure of dynamic performance.

DYNAMIC RANGE

Dynamic Range is the specification that indicates the ratio of the smallest signal the converter can resolve to the largest signal it is able to produce. As a ratio, it is usually expressed in decibels (dBs). The theoretical dynamic range of an n-bit converter is (6×n) dB. In the case of the 18-bit AD1860, that is 108dB. The actual dynamic range of a converter is less than the theoretical value due to limitations imposed by noise and other errors.

MIDSCALE ERROR

Midscale Error, or bipolar zero error, is the deviation of the actual analog output from the ideal output (0V) when the 2s complement input code representing half scale is loaded in the input register.

DIFFERENTIAL LINEARITY ERROR

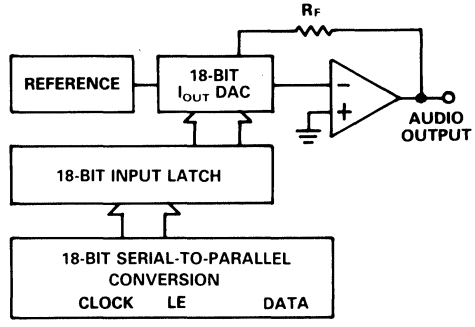
Differential Linearity Error is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in the digital input. Monotonic behavior requires that the differential linearity error not exceed 1LSB in the negative direction.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

SIGNAL-TO-NOISE RATIO

The Signal-to-Noise Ratio is defined as the ratio of the amplitude of the output with a full-scale output present to the amplitude of the output when no signal is present. This is measured with a standard A-Weight filter.



AD1860 Block Diagram

FUNCTIONAL DESCRIPTION

The AD1860 is a complete monolithic 18-bit PCM Audio DAC. No additional external components are required for operation. As shown in the block diagram, each chip contains a voltage reference, an output amplifier, an 18-bit DAC, an 18-bit input latch and an 18-bit serial to parallel input register.

The voltage reference consists of a bandgap circuit and buffer amplifier. This combination of elements produces a reference voltage that is unaffected by changes in temperature and age. The DAC output voltage, which is derived from the reference voltage, is also unaffected by these environmental changes.

The output amplifier uses both MOS and bipolar devices to produce low offset, high slew rate and optimum settling time. When combined with the on chip feedback resistor, the output op amp converts the output current of the AD1860 to a voltage output.

The 18-bit D/A converter uses a combination of segmented decoder and R-2R architecture to achieve consistent linearity and differential linearity. The resistors which form the ladder structure are fabricated with silicon chromium thin film. Laser trimming of these resistors further reduces linearity error resulting in low output distortion.

The input register and serial to parallel converter are fabricated with CMOS logic gates. These gates allow the achievement of fast switching speeds and low power consumption. This contributes to the overall low power dissipation of the AD1860.

AD1860—Analog Circuit Considerations

GROUNDING RECOMMENDATIONS

The AD1860 has two ground pins, designated Analog and Digital ground. The analog ground pin is the "high quality" ground reference point for the device. The analog ground pin should be connected to the analog common point in the system. The output load should also be connected to that same point.

The digital ground pin returns ground current from the digital logic portions of the AD1860 circuitry. This pin should be connected to the digital common point in the system.

As illustrated in Figure 1, the analog and digital grounds should be connected together at one point in the system.

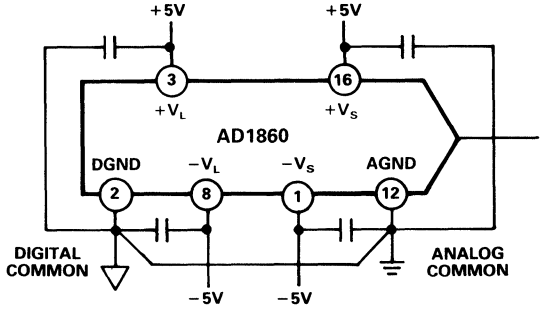


Figure 1. Recommended Circuit Schematic

POWER SUPPLIES AND DECOUPLING

The AD1860 has four power supply input pins. $\pm V_S$ provide the supply voltages to operate the linear portions of the DAC including the voltage reference, output amplifier and control amplifier. The $\pm V_S$ supplies are designed to operate from ±5V to ±12V.

The $\pm V_L$ supplies operate the digital portions of the chip including the input shift register and the input latching circuitry. The $\pm V_L$ supplies are also designed to be operated from ±5V to ±12 V subject only to the limitation that $-V_L$ may not be more negative than $-V_S$.

Decoupling capacitors should be used on all power supply pins. Furthermore, good engineering practice suggests that these capacitors be placed as close as possible to the package pins as well as the common points. The logic supplies, $\pm V_L$, should be decoupled to digital common; and the analog supplies, $\pm V_S$, should be decoupled to analog common.

The use of four separate power supplies will reduce feedthrough from the digital portion of the system to the linear portion of the system, thus contributing to good performance. However, four separate voltage supplies are not necessary for good circuit performance. For example, Figure 2 illustrates a system where only a single positive and a single negative supply are available.

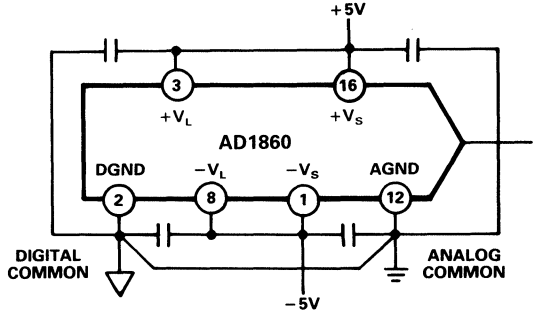


Figure 2. Typical Power Supply Sensitivity

Given that these two supplies are within the range of ±5V to ±12V, they may be used to power the AD1860. In this case, the positive logic and positive analog supplies may both be connected to the single positive supply. The negative logic and negative analog supplies may both be connected to the single negative supply. Performance would benefit from a measure of isolation between the supplies introduced by using simple low pass filters in the individual power supply leads.

As with most linear circuits, changes in the power supplies will affect the output of the DAC. Analog Devices recommends that well regulated power supplies with less than 1% ripple be incorporated into the design of any system using these devices.

TOTAL HARMONIC DISTORTION + NOISE

The THD figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. The THD specification, therefore, provides a direct method to classify and choose an audio DAC for a desired level of performance.

By combining noise measurement with THD measurement, a THD+N specification is produced. This specification measures all undesirable signal produced by the DAC, including harmonic products of the test tone as well as noise.

Analog Devices tests and grades all AD1860s on the basis of THD+N performance. A block diagram of the test setup is shown in Figure 3. In this test setup, a digital data stream representing a 0dB, −20dB or −60dB sinewave is sent to the device under test. The frequency of this waveform in 990.5 Hz.

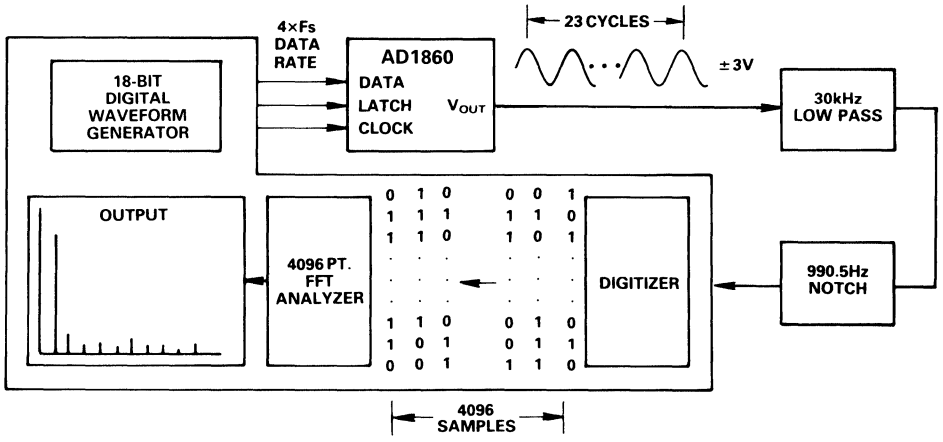


Figure 3. Block Diagram of DistortionTest Circuit

5

Input data is sent to the AD1860 at a $4\times F_S$ rate (176.4kHz). The AD1860 under test produces an output signal with its onboard op amp. The automatic test equipment digitizes 4096 samples of the output test waveform, incorporating 23 complete cycles of the sinewave. A 4096 point FFT is performed on the results of the test. Based on the harmonics of the fundamental 990.5Hz test tone and the noise components, the total harmonic distortion + noise of the device is calculated. Neither a deglitcher nor an MSB trim is used during this test.

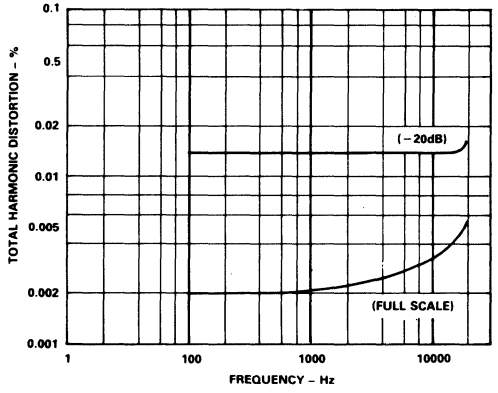


Figure 4. Typical THD vs Frequency

The circuit design, layout and manufacturing techniques employed in the production of the AD1860 result in excellent THD performance. Figure 4 shows the typical unadjusted THD performance of the AD1860 for various amplitudes and frequencies of output signals. As can be seen, the AD1860 offers excellent performance, even at low amplitudes.

OPTIONAL MSB ADJUSTMENT

Use of an optional adjust circuitry allows residual differential linearity error around midscale to be eliminated. This error is especially important when low amplitude signals are being reproduced. In those cases, as the signal amplitude decreases, the ratio of the midscale differential linearity error to the signal amplitude increases, thereby increasing THD.

Therefore, for best performance at low output levels, the optional MSB adjust circuitry shown in Figure 5 may be used to improve performance.

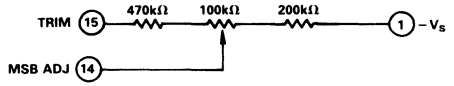


Figure 5. Optional THD Adjust Circuit

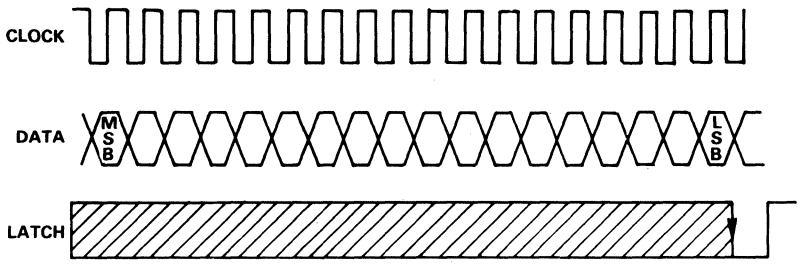


Figure 6. Signal Requirements for AD1860

DIGITAL CIRCUIT CONSIDERATIONS

Input Data

Data is transmitted to the AD1860 in a bit stream composed of 18-bit words with a serial, MSB first format. Three signals must be present to achieve proper operation. They are the Data, Clock and Latch Enable signals. Input data bits are clocked into the input register on the rising edge of the Clock signal. The LSB is clocked in on the 18th clock pulse. When all data bits are loaded, a low-going Latch Enable pulse updates the DAC input. Figure 6 illustrates the general signal requirements for data transfer for the AD1860.

Timing

Figure 7 illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished properly. The input pins of the AD1860 are both TTL and 5V CMOS compatible, independent of the power supplies used. The input requirements illustrated in Figures 6 and 7 are compatible with the data outputs provided by popular DSP filter chips used in digital audio playback systems. The AD1860 input clock can run at a 12.5MHz rate. This clock rate will allow data transfer rates for 2×, 4× or 8× oversampling reconstruction. The application section of this datasheet contains additional guides for using the AD1860 with various DSP filter chips available from Sony, NPC and Yamaha.

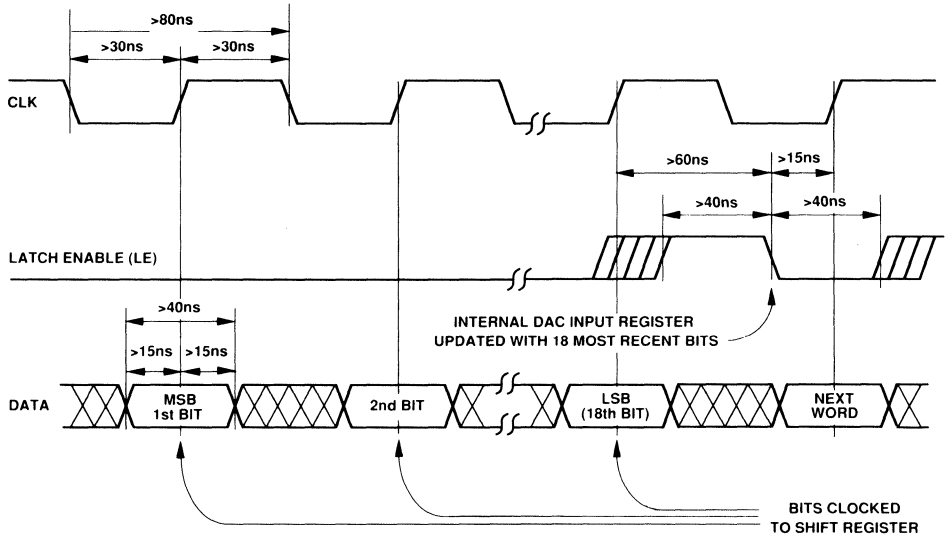


Figure 7. Timing Relationships of Input Signals

APPLICATIONS OF THE AD1860 PCM AUDIO DAC

The AD1860 is a versatile digital-to-analog converter designed for applications in consumer digital audio equipment. Portable, car and home compact disc player, digital audio amplifier and DAT schemes can all use the AD1860. Various circuit architectures are popular in these systems. They include stereo playback sections featuring one DAC per system, one DAC per audio channel (left/right) or multiple DACs per channel. Furthermore, these architectures use different output reconstruction rates to accomplish these functions including reproduction at the sample rate F_S (1×), at twice the sample rate (2×F_S), at four times the sample rate (4×F_S) and even at eight times the sample rate (8×F_S). F_S is 44.1kHz for CD and 48kHz for DAT applications.

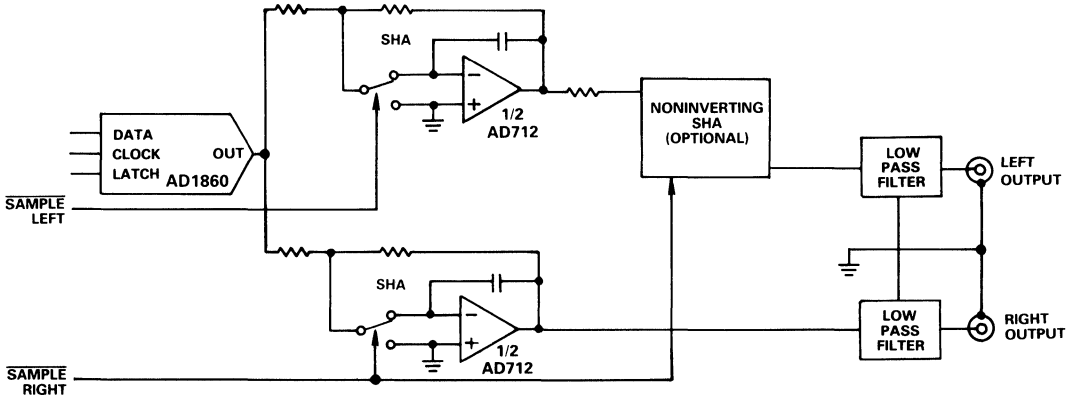


Figure 8. AD1860 in a One DAC per System Architecture

One DAC per System

Figure 8 shows a circuit using one AD1860 per system to reproduce both channels of a typical first generation stereo digital audio system. The input data is fed to the AD1860 in a format which alternates between left channel data and right channel data. The output of the AD1860 is switched between the left channel and right channel output sample/hold amplifiers (SHAs). The SHAs demultiplex and deglitch the output of the AD1860. The timing diagram for the control signals for this circuit are shown in Figure 9.

However, when only two SHAs are used, the actual system performance is limited by the phase delay introduced by the demultiplexed format. This undesirable phase delay is caused by the fact that the data words presented to the inputs of the DAC represent samples taken at precisely the same point in time. But when reconstructed and demultiplexed by a single DAC, these same outputs occur at slightly different times.

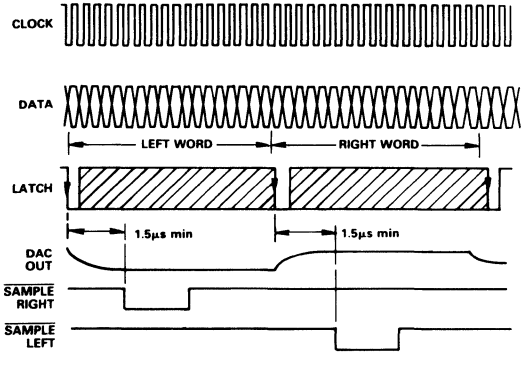


Figure 9. Control Signals for One DAC Circuit

By incorporating a noninverting SHA into the circuit, the phase delay can be eliminated. In Figure 8, the optional SHA ensures that the left channel output appears at the same time as the right channel output. This minor change to the circuit eliminates the artificially induced phase delay by restoring simultaneous outputs.

Following the outputs of the SHAs are low pass filters. These filters are required in any sampled data system to remove unwanted aliased components introduced by the sample and reconstruction operations.

One DAC per Channel

A second approach used to eliminate phase delay between left and right channels employs one DAC per channel. In this architecture, the input data bitstream for each channel is transmitted and then latched into the input register of each DAC. This "second generation" approach is illustrated in Figure 10. A standard implementation of a low pass filter is shown at the output of each DAC. An optional sample/hold amplifier could be connected between the DACs and the LPFs to deglitch the outputs. This is not required, however, to achieve the specified performance.

Two DACs per Channel

Another architecture uses two DACs per channel. In this scheme each DAC reproduces one half of the output waveform. The advantage obtained with this structure is that midscale differential linearity error no longer affects the zero crossing points of the waveforms. Its effects are shifted to the points where the output waveform crosses 1/2 ± 1/4 full scale. The result is that THD performance for low amplitude signals is greatly improved.

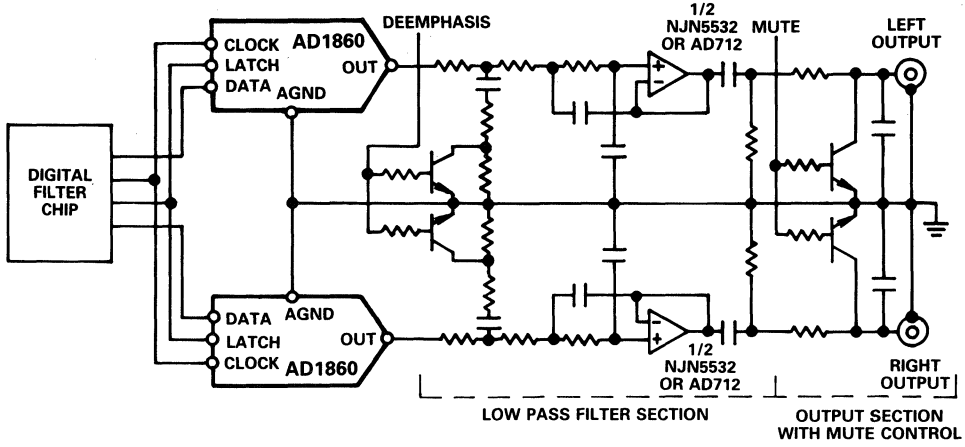


Figure 10. One DAC per Channel Architecture with LPF

DIGITAL FILTERING AND OVERSAMPLING

Oversampling is a term which refers to playback techniques in which the reconstruction frequency used is an integral (2 or more) multiple of the original quantized data rate. For example, in compact disc stereo digital audio playback units, the original quantized data sample rate is 44.1kHz. Popular oversampling rates are 2× or 4×F_S, yielding reconstruction rates of 88.2 and 176.4kHz, respectively.

Oversampling is used to ease the performance constraints of the low pass filters which follow the reconstruction DAC. In any signal reconstructed from sampled data, unwanted frequency components are introduced in the output spectrum; these components are centered at the reconstruction frequency. When a 44.1kHz reconstruction frequency is used, the actual frequency band of interest is 20Hz to 20kHz, and the band of unwanted "image" frequency components extends from 44.1kHz to approximately 24kHz. These unwanted components must be removed with a low-pass filter of very high order. First generation digital audio systems often used low-pass filters of 9, 11 and even 13 poles. Linear implementations of these filters are expensive, difficult to manufacture and can produce distortion due to varying group delay characteristics.

When a 2×reconstruction frequency (88.2kHz) is used, the lowest frequency components now extend down to approximately 68kHz. A 4×rate (176.4kHz) has unwanted components extending down to approximately 156kHz. The filter response needed to remove these frequency components can now be less steep. This means that a lower order filter may be used resulting in less distortion at lower cost. Linear filters with 3 or 5 poles, as shown in Figure 10, are adequate to do the job and are quite common in digital audio products employing oversampling techniques.

Oversampling techniques require the serial input data stream to run at the same integral multiple of the original data rate. So, while the constraints on the output low-pass filter are eased, the constraints on the serial digital input port and the settling time of the output stage are not.

The actual oversampling operation takes place in the digital filter chip (DSP) which is located "upstream" from the DAC. The digital filter accepts data from the media and adds the additional reconstruction points according to the algorithm and coefficients stored in the filter chip. Since the digital filters actually interpolate these additional reconstruction points, they have earned the name "interpolation filters".

The AD1860 is compatible with popular digital filter chips used in digital audio products such as the Sony CXD1088, the Yamaha YM3434 and the NPC SM5813.

Figure 11 illustrates the combination of a second generation digital filter chip, the Sony CXD1088, and the AD1860 audio DAC. The digital filter chip provides 18-bit data words to the DACs at $4\times F_S$. Very high performance can be achieved.

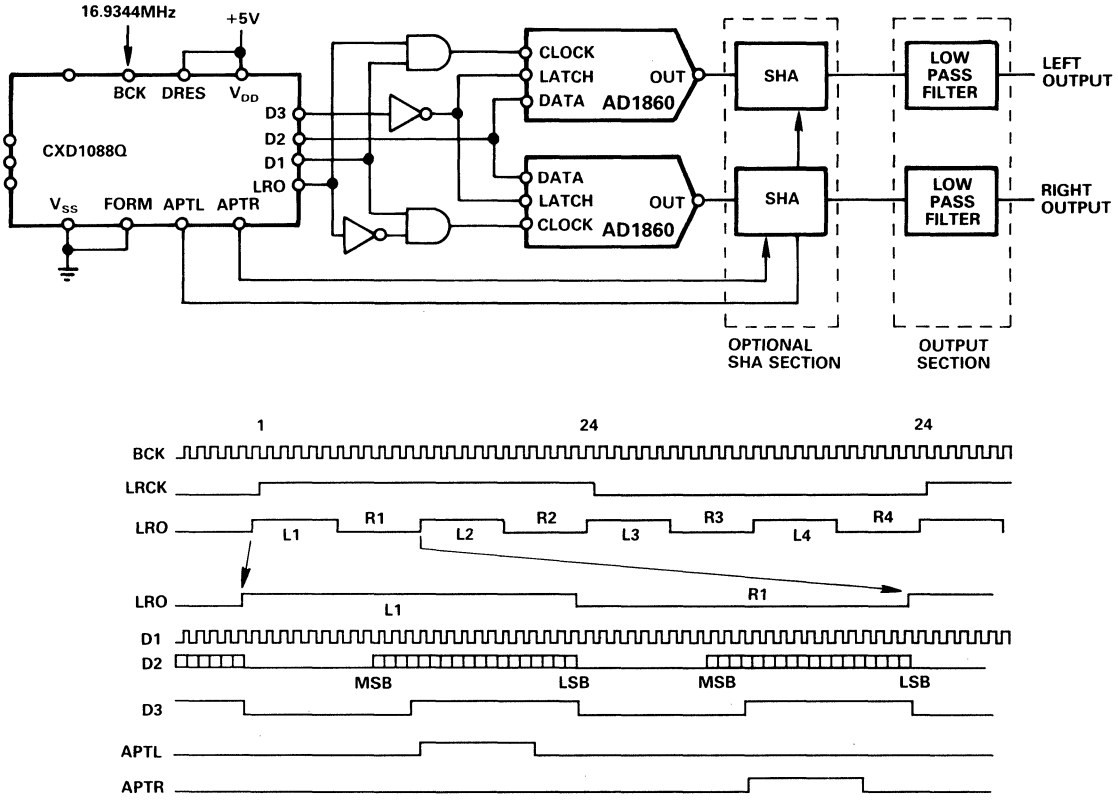


Figure 11. $4\times F_S$ with the CXD1088Q

Figure 12 illustrates the combination of a Yamaha YM3434 digital filter chip and two AD1860 audio DACs. This combination of components results in $8\times F_S$ oversampling reconstruction rates. This rate allows the use of lower order output low pass filters than would be required with lower oversampling rates, without sacrificing performance. In this high performance CD player application, the DAC input data is simultaneously transmitted to the input registers of the DACs through dedicated left and right channel output pins on the YM3434. This implementation does not require any external components to achieve the full 108dB dynamic range afforded by the 18-bit AD1860 audio DAC. As before, optional sample/hold signals are provided.

Figure 13 shows the schematic for $8\times F_S$ when two AD1860s are used with an NPC SM5813AP/APT digital filter chip. As can be seen, this application is very similar to the one shown in Figure 12. See Figure 10 for an example of a typical LPF.

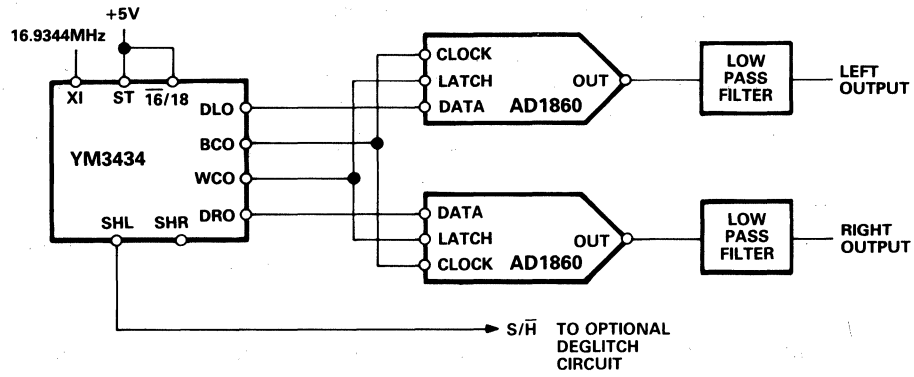


Figure 12. YM3434 and AD1860 Achieve $8\times F_S$

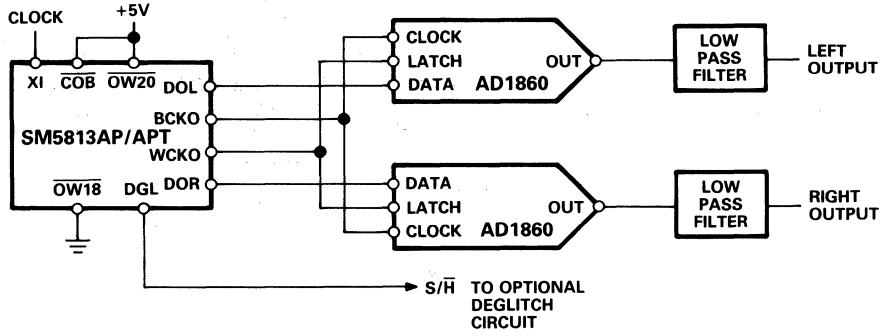


Figure 13. SM5813AP/APT and AD1860 Achieve $8\times F_S$

ANALOG DEVICES

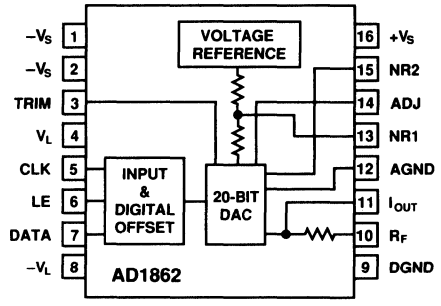
Ultralow Noise 20-Bit Audio DAC

AD1862*

FEATURES
119 dB Signal-to-Noise Ratio
102 dB D-Range Performance
±1 dB Gain Linearity
±1 mA Output Current
16-Pin DIP Package
0.0012% THD + N

APPLICATIONS
High-Performance Compact Disc Players
Digital Audio Amplifiers
Synthesizer Keyboards
Digital Mixing Consoles
High-Resolution Signal Processing

FUNCTIONAL BLOCK DIAGRAM



5

PRODUCT DESCRIPTION

The AD1862 is a monolithic 20-bit digital audio DAC. Each device provides a 20-bit DAC, 20-bit serial-to-parallel input register and voltage reference. The digital portion of the AD1862 is fabricated with CMOS logic elements that are provided by Analog Devices' BiMOS II process. The analog portion of the AD1862 is fabricated with bipolar and MOS devices as well as thin-film resistors.

New design, layout and packaging techniques all combine to produce extremely high-performance audio playback. The design of the AD1862 incorporates a digital offset circuit which improves low-level distortion performance. Low-stress packaging techniques are used to minimize stress-induced parametric shifts. Stress-sensitive circuit elements are located in die areas which are least affected by packaging stress. Laser-trimming of initial linearity error affords extremely low total harmonic distortion. Output glitch is also small, contributing to the overall high level of performance.

The noise performance of the AD1862 is excellent. When used with the recommended two external noise-reduction capacitors, it achieves 119 dB signal-to-noise ratio.

The serial input port consists of the clock, data and latch enable pins. A serial 20-bit, 2s complement data word is clocked into the DAC, MSB first, by the external data clock. A latch-enable signal transfers the input word from the internal serial input register to the DAC input register. The data clock can function at 17 MHz, allowing 16 × F_S operation. The serial input port is compatible with second-generation digital filter chips for consumer audio products such as the NPC SM5813 and SM5818.

The AD1862 operates with ±5 V to ±12 V supplies for the digital power supplies and ±12 V supplies for the analog supplies. The digital and analog supplies can be separated for reduced digital crosstalk. Separate analog and digital common pins are also provided. The AD1862 typically dissipates less than 300 mW.

The AD1862 is packaged in a 16-pin plastic DIP. The operating range is guaranteed to be −25°C to +70°C.

PRODUCT HIGHLIGHTS

1. 119 dB signal-to-noise ratio (typical)
2. 102 dB D-Range performance (minimum)
3. ±1 dB gain linearity @ −90 dB amplitude
4. 20-bit resolution provides 120 dB of dynamic range
5. 16×F_S operation
6. 0.0012% THD+N @ 0 dB signal amplitude (typical)
7. Space saving 16-pin DIP package
8. ±1 mA output current

*Protected by U.S. Patents Numbers: 4,349,811; 4,857,862; 4,855,618; 3,961,326; 4,141,004; 4,902,959.

AD1862—SPECIFICATIONS (T_A at +25°C and ±12 V supplies, see Figure 10 for test circuit schematic)

	Min	Typ	Max	Units
RESOLUTION	20			Bits
DIGITAL INPUTS V_{IH}	2.0	**4.0**		V
V_{IL}		**0.4**	0.8	V
I_{IH} @ V_{IH} = 4.0 V			**1.0**	μA
I_{IL} @ V_{IL} = 0.4 V			**−10**	μA
Maximum Clock Input Frequency	**17**			MHz
ACCURACY				
Gain Error			**±2**	%
Midscale Output Error		±2	**±5**	μA
TOTAL HARMONIC DISTORTION + NOISE (EIAJ)[1]				
0 dB, 990.5 Hz AD1862N-J		−98 (0.0012)	**−96 (0.0016)**	dB (%)
AD1862N		−94 (0.0019)	**−92 (0.0025)**	dB (%)
−20 dB, 990.5 Hz AD1862N, N-J		−84 (0.0063)	**−80 (0.01)**	dB (%)
−60 dB, 990.5 Hz AD1862N, N-J		−45 (0.56)	**−42 (0.8)**	dB (%)
D-Range, −60 dB, A-Weight Filter	**102**			dB
SIGNAL-TO-NOISE RATIO[2] (EIAJ)[1]				
A-Weight Filter AD1862N-J	**113**	119		dB
AD1862N	**110**	119		dB
GAIN LINEARITY				
@ −90 dB AD1862N-J		±1		dB
AD1862N		±1		dB
OUTPUT CURRENT				
Bipolar Range		±1		mA
Tolerance		±1	**±2**	%
Output Impedance (±30%)		2.1		kΩ
Settling Time		350		ns
FEEDBACK RESISTOR				
Value		3		kΩ
Tolerance		±1	**±2**	%
POWER SUPPLY				
Voltage V_L and $-V_L$	4.75	**12.0**	13.2	±V
Voltage V_S and $-V_S$	10.8	**12.0**	13.2	±V
Current +I, V_L and V_S = 12 V, 17 MHz Clock		11	**15**	mA
−I, $-V_L$ and $-V_S$ = −12 V, 17 MHz Clock		13	**16**	mA
POWER DISSIPATION				
V_L and V_S = 12 V, $-V_L$ and $-V_S$ = −12 V, 17 MHz Clock		288	372	mW
TEMPERATURE RANGE				
Specification		**+25**		°C
Operation	−25		+70	°C
Storage	−60		+100	°C

NOTE

[1]Test Method complies with EIAJ Standard CP-307.

[2]The signal-to-noise measurement includes noise contributed by the SE5534A op amp used in the test fixture but does not include the noise contributed by the low pass filter used in the test fixture.

Specifications in **boldface** are tested on all production units at final electrical test.

Specifications subject to change without notice.

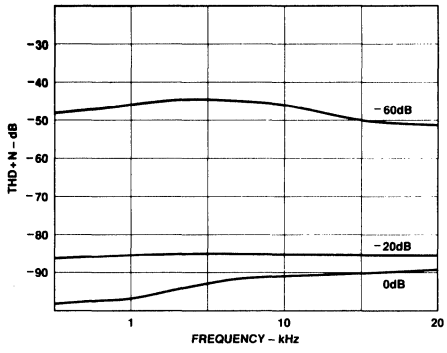


Figure 1. THD+N vs. Frequency

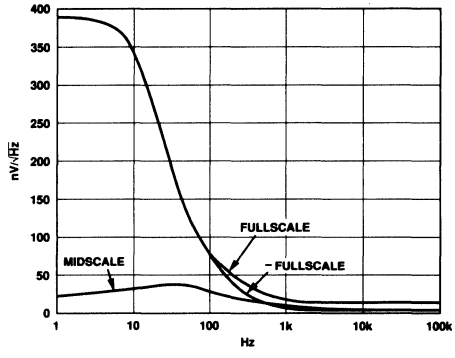


Figure 2. Noise Density

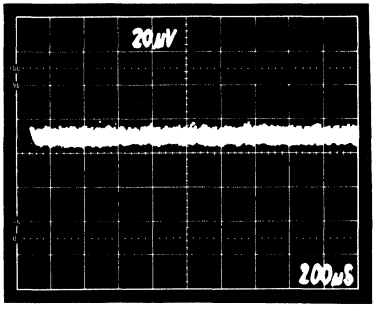


Figure 3. Broadband Noise (20 kHz Bandwidth, Midscale)

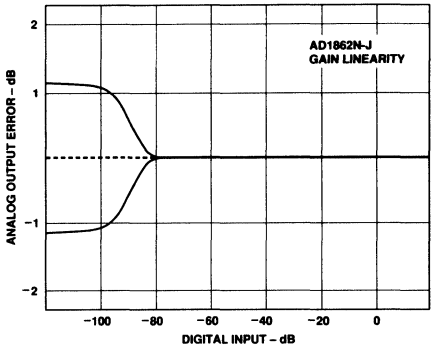


Figure 4. Gain Linearity

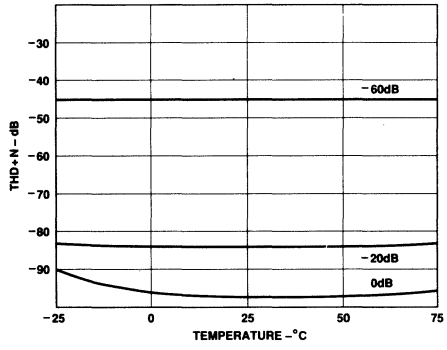


Figure 5. THD+N vs. Temperature (1 kHz)

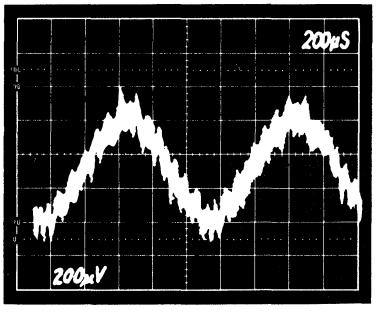


Figure 6. Midscale Differential Linearity

ABSOLUTE MAXIMUM RATINGS*

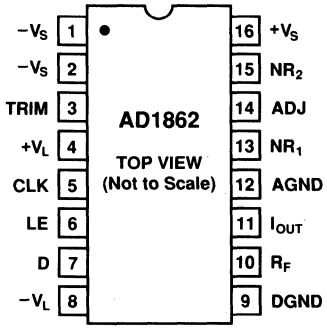
V_L to DGND . . . . . 0 to +13.2 V
$-V_L$ to DGND . . . . . $-V_S$ to 0 V
V_S to AGND . . . . . 0 to +13.2 V
$-V_S$ to AGND . . . . . −13.2 to 0 V
AGND to DGND . . . . . −0.3 to +0.3 V
Digital Inputs to DGND . . . . . −0.3 to V_L
Soldering . . . . . +300°C, 10 sec
Storage Temperature . . . . . −60°C to +100°C

NOTE
*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

PIN CONFIGURATION



PIN DESIGNATIONS

Pin	Function	Description
1	$-V_S$	Bias Capacitor
2	$-V_S$	Analog Negative Supply
3	TRIM	Trim Pot Connection
4	$+V_L$	Positive Logic Supply
5	CLK	External Clock Input
6	LE	Latch Enable Input
7	D	Data Input
8	$-V_L$	Negative Logic Supply
9	DGND	Digital Ground
10	R_F	Feedback Resistor
11	I_{OUT}	Output Current
12	AGND	Analog Ground
13	NR_1	Reference Capacitor
14	ADJ	Midscale Adjust
15	NR_2	Bias Capacitor
16	$+V_S$	Positive Analog Supply

ORDERING GUIDE

Model	Operating Temperature Range	THD+N @ FS	SNR	Package Option*
AD1862N	−25°C to +70°C	−92 dB, 0.0025%	110 dB	N-16
AD1862N-J	−25°C to +70°C	−96 dB, 0.0016%	113 dB	N-16

*N = Plastic DIP. For outline information see Package Information section.

TOTAL HARMONIC DISTORTION + NOISE

Total Harmonic Distortion plus Noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the value of the fundamental input frequency. It is usually expressed in percent (%) or decibels (dB).

D-RANGE DISTORTION

D-Range Distortion is the ratio of the signal amplitude to the distortion plus noise at −60 dB. In this case, an A-Weight filter is used. The value specified for D-Range performance is the ratio measured plus 60 dB.

SETTLING TIME

Settling Time is the time required for the output to reach and remain within ±1/2 LSB about its final value, measured from the digital input transition. It is a primary measure of dynamic performance and is usually expressed in nanoseconds (ns).

SIGNAL-TO-NOISE RATIO

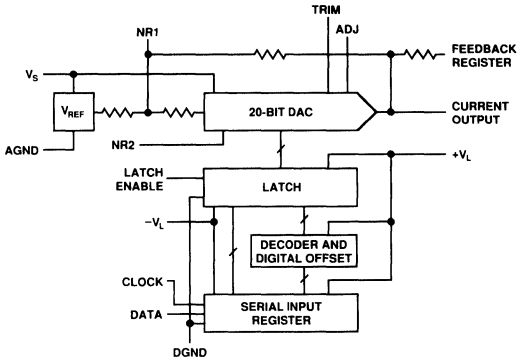
The Signal-to-Noise Ratio is defined as the ratio of the amplitude of the output with full-scale present to the amplitude of the output when no signal is present. It is expressed in decibels (dB) and measured using an A-Weight filter.

GAIN LINEARITY

Gain Linearity is a measure of the deviation of the actual output amplitude from the ideal output amplitude. It is determined by measuring the amplitude of the output signal as the amplitude of that output signal is digitally reduced to a low level. A perfect D/A converter exhibits no difference between the ideal and actual amplitudes. Gain linearity is expressed in decibels (dB).

MIDSCALE ERROR

Midscale Error, or bipolar zero error, is the deviation of the actual analog output from the ideal output when the 2s complement input code representing midscale is loaded in the input register. The AD1862 is a current output D/A converter. Therefore, this error is expressed in μA.



AD1862 Block Diagram

FUNCTIONAL DESCRIPTION

The AD1862 is a high performance, monolithic 20-bit audio DAC. Each device includes a voltage reference, a 20-bit DAC, 20-bit input latch and a 20-bit serial-to-parallel input register. A special digital offset circuit, combined with segmentation circuitry, produces excellent THD+N and D-range performance.

Extensive noise-reduction features are utilized to make the noise performance of the AD1862 as high as possible. For example, the voltage reference circuit is a low-noise, 9 volt bandgap cell. This cell supplies the reference voltage to the bipolar offset circuit and the DAC. An external noise-reduction capacitor is connected to NR1 to form a low-pass filter network.

Additional noise-reduction techniques are used in the control amplifier of the DAC. By connecting an external noise-reduction capacitor to NR2 output noise contributions from the control portion of the DAC are similarly reduced. The noise-reduction efforts result in a signal-to-noise ratio of 119 dB.

The design of the AD1862 uses a combination of segmented decoder, R-2R topology and digital offset to produce low distortion at all signal amplitudes. The digital offset technique shifts the midscale output voltage (0 V) away from the MSB transition of the device. Therefore, small amplitude signals are not affected by an MSB change. An extra DAC cell is included to avoid clipping the output at full scale.

The DAC supplies a ±1 mA output current to an external I-to-V converter. An on-board 3 kΩ feedback resistor is also supplied. Both the output current and feedback resistor are laser-trimmed to ±2% tolerance, simplifying the selection of external filter and/or deemphasis network components. The input register and serial-to-parallel converter are fabricated with CMOS logic gates. These gates allow the achievement of fast switching speeds and low power consumption. Internal TTL-to-CMOS converters are used to insure TTL and 5 V CMOS compatibility.

Analog Circuit Considerations

GROUNDING RECOMMENDATIONS

The AD1862 has two ground pins, designated analog ground (AGND) and digital ground (DGND). The analog ground pin is the "high-quality" ground reference for the device. The analog ground pin should be connected to the analog common point in the system. The reference bypass capacitor, the noninverting terminal of the current-to-voltage conversion op amp, and any output loads should be connected to this point. The digital ground pin returns ground current from the digital logic portions of the AD1862 circuitry. This pin should be connected to the digital common point in the system.

As illustrated in Figure 7, AGND and DGND should be connected together at one point in the system.

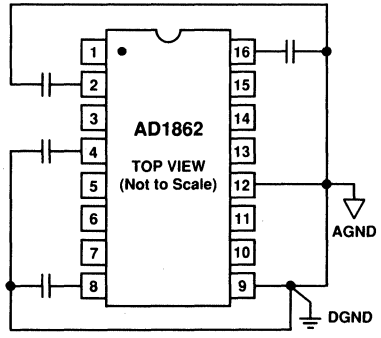


Figure 7. Grounding and Bypassing Recommendations

POWER SUPPLIES AND DECOUPLING

The AD1862 has four power supply input pins. $\pm V_S$ provide the supply voltages which operate the linear portions of the DAC including the voltage reference and control amplifier. The $\pm V_S$ supplies are designed to operate with ±12 volts.

The $\pm V_L$ supplies operate the digital portions of the chip including the input shift register, the input latching circuitry and the TTL-to-CMOS level shifters. The $\pm V_L$ supplies are designed to be operated from ±5 V to ±12 V supplies subject only to the limitation that $-V_L$ may not be more negative than $-V_S$.

Decoupling capacitors should be used on all power supply input pins. Good engineering practice suggests that these capacitors be placed as close as possible to the package pins and the common points. The logic supplies, $\pm V_L$, should be decoupled to DGND and the analog supplies, $\pm V_S$, should be decoupled to AGND.

EXTERNAL NOISE REDUCTION COMPONENTS

Two external capacitors are required to achieve low-noise operation. Their correct connection is illustrated in Figure 8. Capacitor C1 is connected between the pin labeled NR1 and analog common. C1 forms a low-pass filter element which reduces noise contributed by the voltage reference circuitry. The proper choice for this capacitor is a tantalum type with value of 10 µF or more. This capacitor should be connected to the package pins as closely as possible. This will minimize the effects of parasitic inductance of the leads and connections circuit connections.

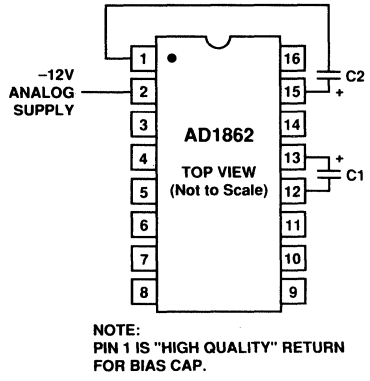


Figure 8. Noise Reduction Capacitors

Capacitor C2 is connected between the pin labeled NR2 and the negative analog supply, $-V_S$. This capacitor reduces the portion of output noise contributed by the control amplifier circuitry. C2 should be chosen to be a tantalum capacitor with a value of about 1 µF. Again, the connections between the AD1862 and C2 should be made as short as possible.

The recommended values for C1 and C2 are 10 µF and 1 µF, respectively. The ratio between C1 and C2 should be approximately 10. Additional noise reduction can be gained by choosing slightly higher values for C1 and C2 such as 22 µF and 2.2 µF. Figure 2 illustrates the noise performance of the AD1862 with 10 µF and 1 µF.

EXTERNAL AMPLIFIER CONNECTIONS

The AD1862 is a current-output D/A converter. Therefore, an external amplifier, in combination with the on-board feedback resistor, is required to derive an output voltage. Figure 9 illustrates the proper connections for an external operational amplifier. The output of the AD1862 is intended to drive the summing junction of an external current-to-voltage conversion op amp. Therefore, the voltage on the output current pin of the AD1862 should be approximately the same as that on the AGND pin of the device.

The on-board 3 kΩ feedback resistor and the ±1 mA output current typically have ±1% tolerance or less. This makes the choice of external components very simple and eliminates additional trimming. For example, if a user wishes to derive an output voltage higher than the ±3 V swing offered by the output current and feedback resistor combination, all that is required is to combine a standard value resistor with the feedback resistor to achieve the appropriate output voltage swing. This technique can be extended to include the choice of elements in the deemphasis network, etc.

TOTAL HARMONIC DISTORTION + NOISE

The THD figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. The THD specification, therefore, provides a direct method to classify and choose an audio DAC for a desired level of performance.

By combining noise measurement with the THD measurement, a THD+N specification is realized. This specification indicates all of the undesirable signal produced by the DAC, including harmonic products of the test tone as well as noise.

Analog Devices tests all AD1862s on the basis of THD+N performance. In this test procedure, a digital data stream representing a 0 dB, −20 dB or −60 dB sine wave is sent to the device under test. The frequency of the waveform is 990.5 Hz. Input data is sent to the AD1862 at an 8 × F_S rate (352.8 kHz). The AD1862 under test produces an output current which is converted to an output voltage by an external amplifier. Figure 10 illustrates the recommended test circuit. Deglitchers and trims are not used during this test procedure. The automatic test equipment digitizes 4096 samples of the output test waveform, incorporating 23 complete cycles of the sine wave. A 4096 point FFT is performed on the test data.

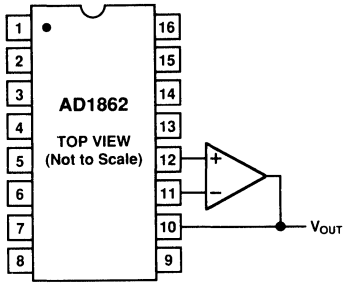


Figure 9. External Amplifier Connections

Based upon the harmonics of the fundamental 990.5 Hz test tone, and the noise components in the audio band, the total harmonic distortion + noise of the device is calculated. The AD1862 is available in two performance grades. The AD1862N produces a maximum of 0.0025% THD+N at 0 dB signal levels. The higher performance AD1862N-J produces a maximum of 0.0016% THD+N at 0 dB signal levels.

SIGNAL-TO-NOISE RATIO

The Signal-to-Noise Ratio (SNR) of the AD1862 is tested in the following manner. The amplitude of a 0 dB signal is measured. The device under test is then set to midscale output voltage (0 volts). The amplitude of all noise present to 30 kHz is measured. The SNR is the ratio of these two measurements. The SNR figure for the AD1862 includes the output noise contributed by the NE5534 op amp used in the test fixture but does not include the noise contributed by the low-pass filter used in the test fixture.

The AD1862N has a minimum SNR of 110 dB. The higher performance AD1862N-J has a minimum SNR of 113 dB.

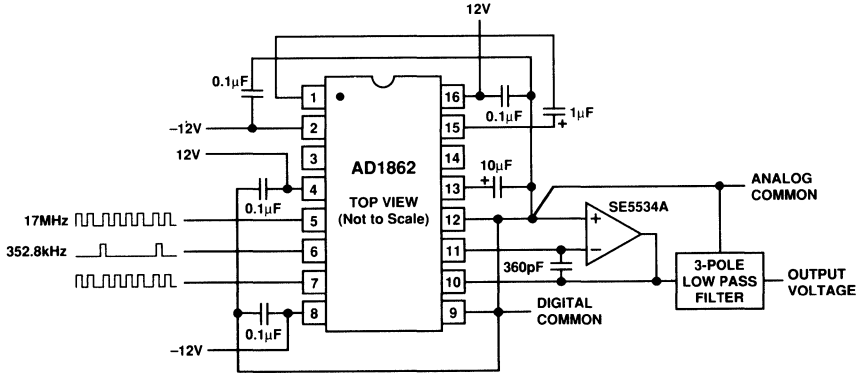


Figure 10. Recommended Test Circuit

Testing the AD1862

OPTIONAL TRIM ADJUSTMENT

The AD1862 includes an external midscale adjust feature. Should an application require improved distortion performance under small and very small signal amplitudes (−60 dB and lower), an adjustment is possible. Two resistors and one potentiometer form the adjustment network. Figure 11 illustrates the correct configuration of the external components. Analog Devices recommends that this adjustment be performed with −60 dB signal amplitudes or lower. Minor performance improvement is achieved with larger signal amplitudes such as −20 dB. Almost no improvement is possible when this adjustment is performed with 0 dB signal amplitudes.

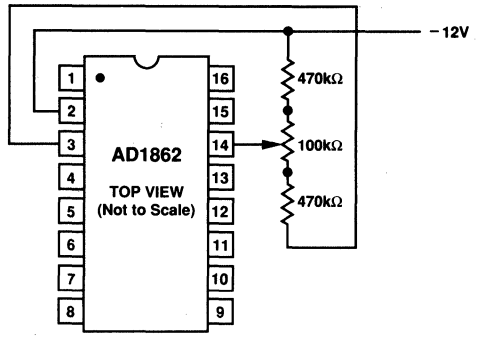


Figure 11. External Midscale Adjust

DIGITAL CIRCUIT CONSIDERATIONS

INPUT DATA

Data is transmitted to the AD1862 in a bit stream composed of 20-bit words with a serial, 2s complement, MSB first format. Three signals must be present to achieve proper operation. They are the data, clock and latch enable signals. Input data bits are clocked into the input register on the rising edge of the clock signal (CLK). The LSB is clocked in on the 20th clock pulse. When all data bits are loaded, a low going latch enable (LE) pulse updates the DAC input. Figure 12a illustrates the general signal requirements for data transfer for the AD1862.

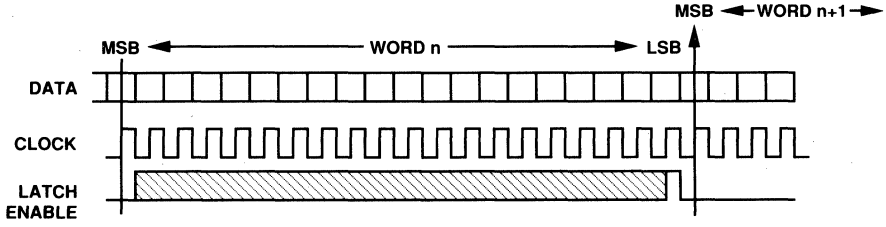


Figure 12a. Input Data

TIMING

Figure 12b illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished successfully. The input pins of the AD1862 are both TTL and 5 V CMOS compatible, independent of the power supplies used in the application. The input requirements illustrated in Figure 12b are compatible with the data outputs provided by popular digital interpolation filter chips used in digital audio playback systems. The AD1862 input clock will run at 17 MHz allowing data to be transferred at a rate of 16 × F_S. Of course, it will also function at slower rates such as 2 ×, 4 × or 8 × F_S.

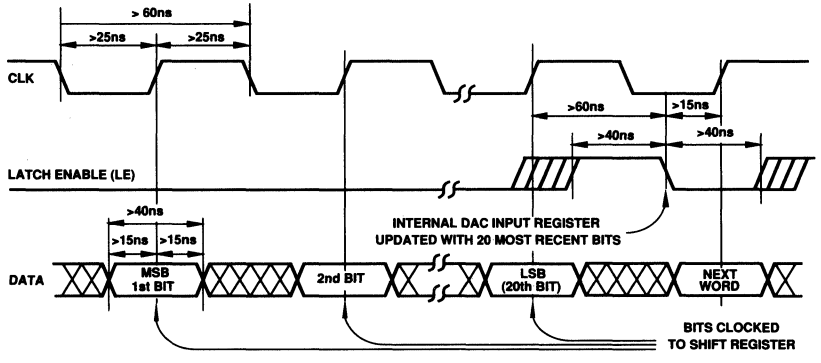


Figure 12b. Timing Requirements

The AD1862 is an extremely high performance DAC designed for high-end consumer and professional digital audio applications. Compact disc players, digital preamplifiers, digital musical instruments and sound processors benefit from the extended dynamic range, low THD+Noise and high signal-to-noise ratio. For the first time, the D/A converter is no longer the basic limitation in the performance of a CD player.

The performance of professional audio gear, such as mixing consoles, digital tape recorders and multivoice synthesizers can utilize the wide dynamic range and signal-to-noise ratio to achieve greater performance. And, the AD1862's space saving 16-pin package contributes to compact system design. This permits a system designer to incorporate more voices in multivoice synthesizers, more tracks in multitrack tape recorders and more channels in multichannel mixing consoles.

Furthermore, high-resolution signal processing and waveform generation applications are equally well served by the AD1862.

HIGH PERFORMANCE CD PLAYER

Figure 13 illustrates the application of AD1862s in a high performance CD player. Two AD1862s are used, one for the left channel and one for the right channel. The CXD11XX chip decodes the digital data coming from the read electronics and sends it to the SM5813. Input data is sent to each AD1862 by the SM5813 digital interpolating filter. This device operates at 8 times oversampling. The NE5534 op amps are chosen for current-to-voltage converters due to their low distortion and low noise. The output filters are 5-pole designs. For the purpose of clarity, all bypass capacitors have been omitted from the schematic.

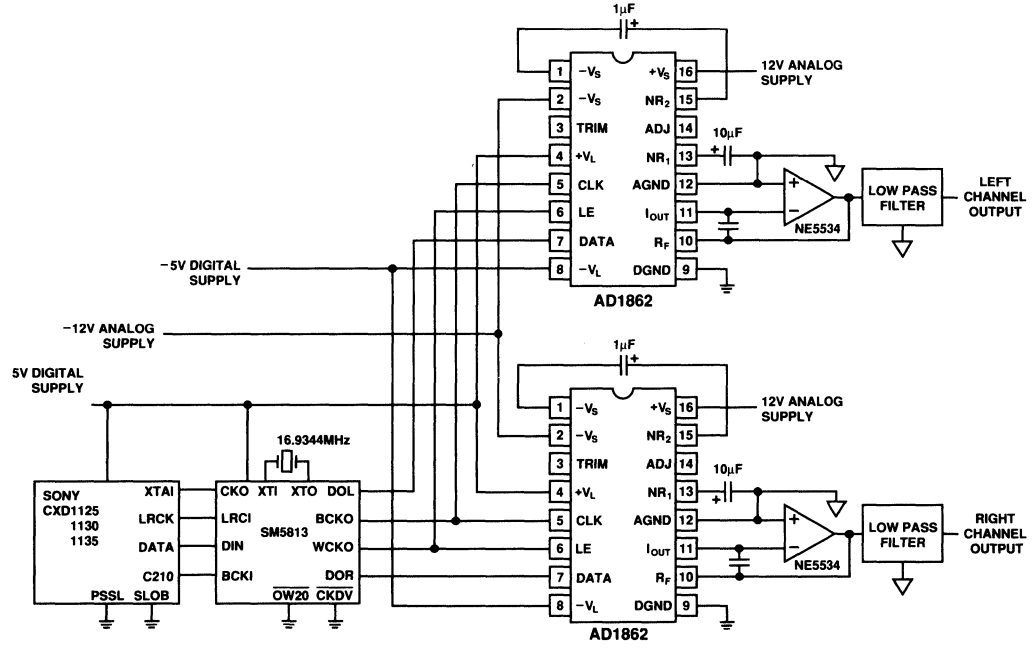


Figure 13. High Performance 20-Bit 8 × Oversampling CD Player Application

HIGH-RESOLUTION SIGNAL PROCESSING

Figure 14 illustrates the AD1862 combined with the DSP56000. In high-resolution applications, the combination of the 24-bit architecture of the DSP56000 and the low noise and high resolution of the AD1862 can produce a high-resolution, low-noise system.

As shown in Figure 14, the clock signal supplied by the DSP processor must be inverted to be compatible with the input of the AD1862. The exact architecture of the output low-pass filter depends on the sample rate of the output data. In general, the higher the oversampling rate, the fewer number of filter poles are required to prevent aliasing.

The 20-bit resolution is particularly suitable for professional audio, mixing or equalization equipment. Its resolution allows 24 dB of equalization to be performed on 16-bit input words without signal truncation. Furthermore, up to sixteen 16-bit input words can be mixed and output directly to the AD1862. In this case, no loss of signal information would be encountered.

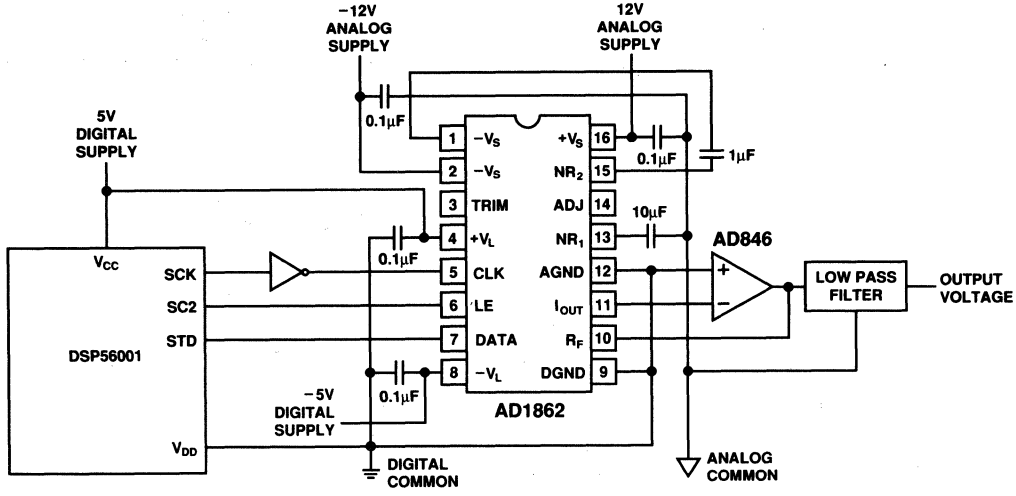


Figure 14. DSP56001 and AD1862 Produces High Resolution Signal Processing System

ANALOG DEVICES

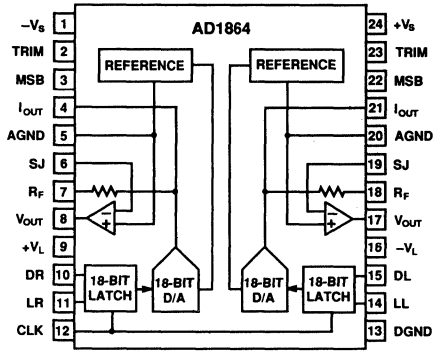
Complete Dual 18-Bit Audio DAC

AD1864*

FEATURES
Dual Serial Input, Voltage Output DACs
No External Components Required
Operates at 8 × Oversampling per Channel
±5 Volt to ±12 Volt Operation
Cophased Outputs
115 dB Channel Separation
±0.3% Interchannel Gain Matching
0.0017% THD+N

APPLICATIONS
Multichannel Audio Applications:
Compact Disc Players
Multi-Voice Keyboard Instruments
DAT Players and Recorders
Digital Mixing Consoles
Multimedia Workstations

AD1864 DIP BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1864 is a complete dual 18-bit DAC offering excellent THD+N, while requiring no external components. Two complete signal channels are included. This results in cophased voltage or current output signals and eliminates the need for output demultiplexing circuitry. The monolithic AD1864 chip includes CMOS logic elements, bipolar and MOS linear elements and laser-trimmed thin-film resistor elements, all fabricated on Analog Devices BiMOS II process.

The DACs on the AD1864 chip employ a partially-segmented architecture. The first four MSBs of each DAC are segmented into 15 elements. The 14 LSBs are produced using standard R-2R techniques. Segment and R-2R resistors are laser-trimmed to provide extremely low total harmonic distortion. This architecture minimizes errors at major code transitions resulting in low output glitch and eliminating the need for an external deglitcher. When used in the current output mode, the AD1864 provides two cophased ±1 mA output signals.

Each channel is equipped with a high performance output amplifier. These amplifiers achieve fast settling and high slew rate, producing ±3 V signals at load currents up to 8 mA. Each output amplifier is short-circuit protected and can withstand indefinite short circuits to ground.

The AD1864 was designed to balance two sets of opposing requirements, channel separation and DAC matching. High channel separation is the result of careful layout techniques. At the same time, both channels of the AD1864 have been designed to ensure matched gain and linearity as well as tracking over time and temperature. This assures optimum performance when used in stereo and multi-DAC per channel applications.

A versatile digital interface allows the AD1864 to be directly connected to standard digital filter chips. This interface employs five signals: Data Left (DL), Data Right (DR), Latch Left (LL), Latch Right (LR) and Clock (CLK). DL and DR are the serial input pins for the left and right DAC input registers. Input data bits are clocked into the input register on the rising edge of CLK. A low-going latch edge updates the respective DAC output. For systems using only a single latch signal, LL and LR may be connected together. For systems using only one DATA signal, DR and DL may be connected together.

The AD1864 operates from ±5 V to ±12 V power supplies. The digital supplies, V_L and $-V_L$, can be separated from the analog supplies, V_S and $-V_S$, for reduced digital feedthrough. Separate analog and digital ground pins are also provided. The AD1864 typically dissipates only 225 mW, with a maximum power dissipation of 265 mW.

The AD1864 is packaged in both a 24-pin plastic DIP and a 28-pin PLCC. Operation is guaranteed over the temperature range of −25°C to +70°C and over the voltage supply range of ±4.75 V to ±13.2 V.

PRODUCT HIGHLIGHTS

1. The AD1864 is a complete dual 18-bit audio DAC.
2. 108 dB signal-to-noise ratio for low noise operation.
3. THD+N is typically 0.0017%.
4. Interchannel gain and midscale matching.
5. Output voltages and currents are cophased.
6. Low glitch for improved sound quality.
7. Both channels are 100% tested at 8 × F_S.
8. Low Power — only 225 mW typ, 265 mW max.
9. 5-wire interface for individual DAC control.

AD1864—SPECIFICATIONS (T_A = +25°C, $\pm V_L = \pm V_S = \pm 5$ V, F_S = 352.8 kHz, without MSB adjustment)

	Min	Typ	Max	Units
RESOLUTION		18		Bits
DIGITAL INPUTS				
V_{IH}	2.0		$+V_L$	V
V_{IL}			0.8	V
I_{IH}, $V_{IH} = +V_L$			**1.0**	μA
I_{IL}, V_{IL} = 0.4 V			**−10**	μA
Clock Input Frequency	**12.7**			MHz
ACCURACY				
Gain Error		0.4	**1.0**	% of FSR
Interchannel Gain Matching		0.3	**0.8**	% of FSR
Midscale Error		4		mV
Interchannel Midscale Matching		5		mV
Gain Linearity Error (0 dB to −90 dB)		<2		dB
DRIFT (0°C to +70°C)				
Gain Drift		±25		ppm of FSR/°C
Midscale Drift		±4		ppm of FSR/°C
TOTAL HARMONIC DISTORTION + NOISE*				
0 dB, 990.5 Hz AD1864N, P		0.004	**0.006**	%
AD1864N-J, P-J		0.003	**0.004**	%
AD1864N-K		0.0017	**0.0025**	%
−20 dB, 990.5 Hz AD1864N, P		0.010	**0.040**	%
AD1864N-J, P-J		0.010	**0.020**	%
AD1864N-K		0.010	**0.020**	%
−60 dB, 990.5 Hz AD1864N, P		1.0	**4.0**	%
AD1864N-J, P-J		1.0	**2.0**	%
AD1864N-K		1.0	**2.0**	%
CHANNEL SEPARATION*				
0 dB, 990.5 Hz	**110**	115		dB
SIGNAL-TO-NOISE RATIO*				
(20 Hz to 30 kHz) N, N-J, N-K	**102**	108		dB
P, P-J	**95**	108		
D-RANGE* (WITH A-WEIGHT FILTER)				
−60 dB, 990.5 Hz AD1864N, P	**88**	100		dB
AD1864N-J, P-J	**94**	100		dB
AD1864N-K	**94**	100		dB
OUTPUT				
Voltage Output Configuration				
Output Range (±3%)	**±2.88**	±3.0	**±3.12**	V
Output Impedance		0.1		Ω
Load Current	±8			mA
Short-Circuit Duration		Indefinite to Common		
Current Output Configuration				
Bipolar Output Range (±30%)		±1		mA
Output Impedance (±30%)		1.7		kΩ
POWER SUPPLY				
$+V_L$ and $+V_S$	4.75	**5.0**	13.2	V
$-V_L$ and $-V_S$	−13.2	**−5.0**	−4.75	V
+I, ($+V_L$ and $+V_S$ = +5 V)		22	**25**	mA
−I, ($-V_L$ and $-V_S$ = −5 V)		−23	**−28**	mA
POWER DISSIPATION, $\pm V_L = \pm V_S = \pm 5$ V		225	**265**	mW
TEMPERATURE RANGE				
Specification	0	**+25**	+70	°C
Operation	−25		+70	°C
Storage	−60		+100	°C
WARMUP TIME	1			min

NOTE
Specifications shown in **boldface** are tested on production units at final test without optional MSB adjustment.
*Tested in accordance with EIAJ Test Standard CP-307 with 18-bit data.
Specifications subject to change without notice.

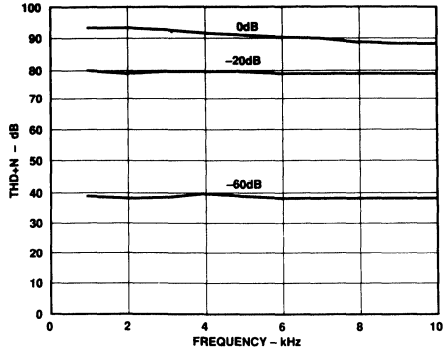


Figure 1. THD+N vs. Frequency

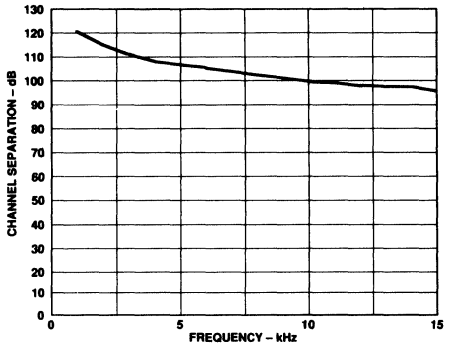


Figure 2. Channel Separation vs. Frequency

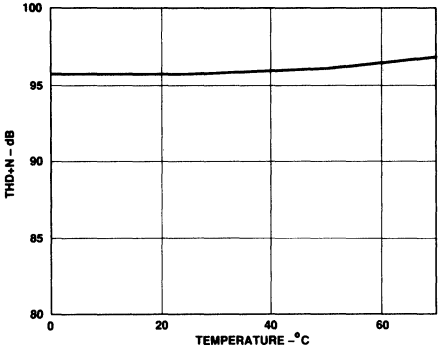


Figure 3. THD+N vs. Temperature

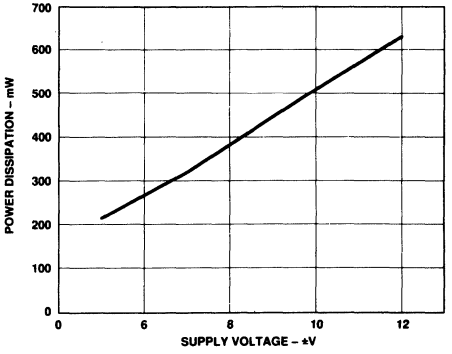


Figure 4. Power Dissipation vs. Supply Voltage

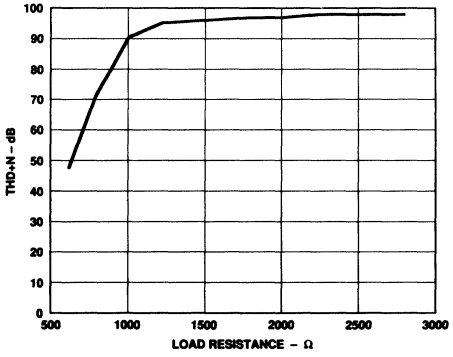


Figure 5. THD+N vs. Load Resistance

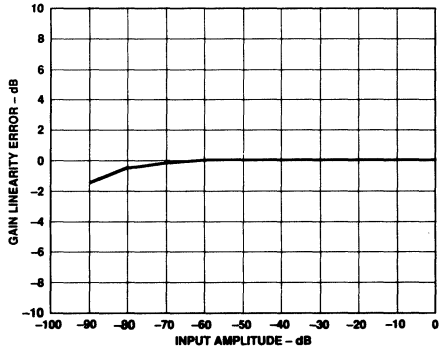


Figure 6. Gain Linearity Error vs. Input Amplitude

ABSOLUTE MAXIMUM RATINGS*

V_L to DGND	0 V to 13.2 V
V_S to AGND	0 V to 13.2 V
$-V_L$ to DGND	−13.2 V to 0 V
$-V_S$ to AGND	−13.2 V to 0 V
AGND to DGND	±0.3 V
Digital Inputs to DGND	−0.3 V to V_L
Short-Circuit Protection	Indefinite Short to Ground
Soldering (10 sec)	+300°C

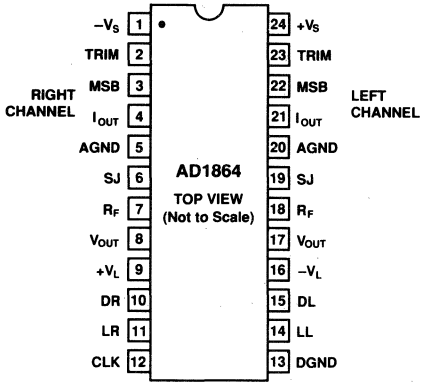
*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

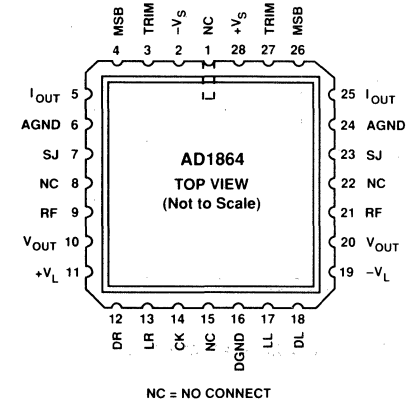
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATIONS

DIP Package



PLCC Package



NC = NO CONNECT

PIN DESIGNATIONS

SIGNAL	DESCRIPTION
$-V_S$	Negative Analog Supply
TRIM	Right Channel Trim Network Connection
MSB	Right Channel Trim Potentiometer Connection
I_{OUT}	Right Channel Output Current
AGND	Right Channel Analog Common Pin
SJ	Right Channel Amplifier Summing Junction
R_F	Right Channel Feedback Resistor
V_{OUT}	Right Channel Output Voltage
$+V_L$	Positive Digital Supply
DR	Right Channel Data Input Pin
LR	Right Channel Latch Pin
CLK	Clock Input Pin
DGND	Digital Common Pin
LL	Left Channel Latch Pin
DL	Left Channel Data Input Pin
$-V_L$	Negative Digital Supply
V_{OUT}	Left Channel Output Voltage
RF	Left Channel Feedback Resistor
SJ	Left Channel Amplifier Summing Junction
AGND	Left Channel Analog Common Pin
I_{OUT}	Left Channel Output Current
MSB	Left Channel Trim Potentiometer Wiper Connection
TRIM	Left Channel Trim Network Connection
$+V_S$	Positive Analog Supply

ORDERING GUIDE

Model	THD+N @ FS	Package Option*
AD1864N	0.006%	N-24
AD1864N-J	0.004%	N-24
AD1864N-K	0.0025%	N-24
AD1864P	0.006%	P-28A
AD1864P-J	0.004%	P-28A

*N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

TOTAL HARMONIC DISTORTION + NOISE

Total Harmonic Distortion plus Noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the amplitudes of the harmonics and noise to the value of the fundamental input frequency. It is usually expressed in percent.

THD+N is a measure of the magnitude and distribution of linearity error, differential linearity error, quantization error and noise. The distribution of these errors may be different, depending on the amplitude of the output signal. Therefore, to be most useful, THD+N should be specified for both large (0 dB) and small (−20 dB, −60 dB) signal amplitudes. THD+N measurements for the AD1864 are made using the first 19 harmonics and noise out to 30 kHz.

SIGNAL-TO-NOISE RATIO

The Signal-to-Noise Ratio is defined as the ratio of the amplitude of the output when cide midscale is entered to the amplitude of the output when a cide full scale is entered. It is measured using a standard A-Weight filter. SNR for the AD1864 is measured for noise components up to 30 kHz.

CHANNEL SEPARATION

Channel separation is defined as the ratio of the amplitude of a full-scale signal appearing on one channel to the amplitude of that same signal which couples onto the adjacent channel. It is usually expressed in dB. For the AD1864 channel separation is measured in accordance with EIAJ Standard CP-307, Section 5.5.

D-RANGE DISTORTION

D-Range distortion is equal to the value of the total harmonic distortion + noise (THD+N) plus 60 dB when a signal level of 60 dB below full-scale is reproduced. D-Range is tested with a 1 kHz input sine wave. This is measured with a standard A-Weight filter as specified by EIAJ Standard CP-307.

GAIN ERROR

The gain error specification indicates how closely the output of a given channel matches the ideal output for given input data. It is expressed in % of FSR and is measured with a full-scale output signal.

INTERCHANNEL GAIN MATCHING

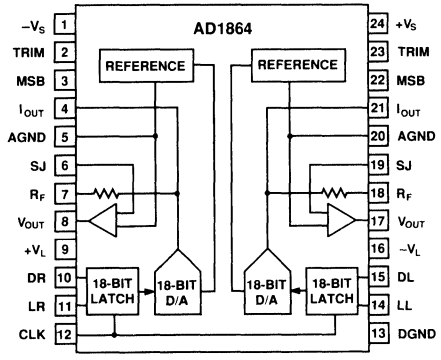
The gain matching specification indicates how closely the amplitudes of the output signals match when producing identical input data. It is expressed in % of FSR (Full-Scale Range = 6 V for the AD1864) and is measured with full-scale output signals.

MIDSCALE ERROR

Midscale error is the deviation of the actual analog output of a given channel from the ideal output (0 V) when the 2s complement input code representing half scale is loaded into the input register of the DAC. It is expressed in mV.

INTERCHANNEL MIDSCALE MATCHING

The midscale matching specification indicates how closely the amplitudes of the output signals of the two channels match when the 2s complement input code representing half scale is loaded into the input register of both channels. It is expressed in mV and is measured with half-scale output signals.



AD1864 DIP Block Diagram

FUNCTIONAL DESCRIPTION

The AD1864 is a complete, monolithic, dual 18-bit audio DAC. No external components are required for operation. As shown in the block diagram, each chip contains two voltage references, two output amplifiers, two 18-bit serial input registers and two 18-bit DACs.

The voltage reference section provides a reference voltage for each DAC circuit. These voltages are produced by low-noise bandgap circuits. Buffer amplifiers are also included. This combination of elements produces reference voltages that are unaffected by changes in temperature and time.

The output amplifiers use both MOS and bipolar devices and incorporate an all NPN output stage. This design technique produces higher slew rate and lower distortion than previous techniques. Frequency response is also improved. When combined with the appropriate on-chip feedback resistor, the output op amps convert the output current to output voltages.

The 18-bit D/A converters use a combination of segmented decoder and R-2R architecture to achieve consistent linearity and differential linearity. The resistors which form the ladder structure are fabricated with silicon chromium thin film. Laser trimming of these resistors further reduces linearity errors resulting in low output distortion.

The input registers are fabricated with CMOS logic gates. These gates allow the achievement of fast switching speeds and low power consumption, contributing to the low glitch and low power dissipation of the AD1864.

GROUNDING RECOMMENDATIONS

The AD1864 has three ground pins, two labeled AGND and one labeled DGND. AGND, the analog ground pins, are the "high quality" ground references for the device. To minimize distortion and reduce crosstalk between channels, the analog ground pins should be connected together only at the analog common point in the system. As shown in Figure 7, the AGND pins should *not* be connected at the chip.

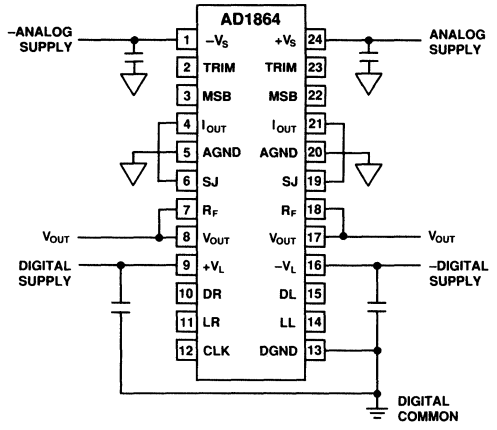


Figure 7. Recommended DIP Circuit Schematic

The digital ground pin returns ground current from the digital logic portions of the AD1864 circuitry. This pin should be connected to the digital common pin in the system. Other digital logic chips should also be referred to that point. The analog and digital grounds should be connected together at one point in the system, preferably at the power supply.

POWER SUPPLIES AND DECOUPLING

The AD1864 has four power supply pins. $\pm V_S$ provide the supply voltages which operate the analog portions of the DAC including the voltage references, output amplifiers and control amplifiers. The $\pm V_S$ supplies are designed to operate from ± 5 V to ± 12 V. These supplies should be decoupled to analog common using 0.1 μF capacitors. Good engineering practice suggests that the bypass capacitors be placed as close as possible to the package pins. This minimizes the parasitic inductive effects of printed circuit board traces.

The $\pm V_L$ supplies operate the digital portions of the chip including the input shift registers and the input latching circuitry. These supplies should be bypassed to digital common using 0.1 μF capacitors. $\pm V_L$ operates with ± 5 V to ± 12 V supplies. In order to assure proper operation of the AD1864, $-V_S$ must be the most negative power supply voltage at all times.

Though separate positive and negative power supply pins are provided for the analog and digital portions of the AD1864, it is also possible to use the AD1864 in systems featuring a single positive and a single negative power supply. In this case, the $+V_S$ and $+V_L$ input pins should be connected to the positive power supply. $-V_S$ and $-V_L$ should be connected to the single negative supply. This feature allows reduction of the cost and complexity of the system power supply.

As with most linear circuits, changes in the power supplies will affect the output of the DAC. Analog Devices recommends that well-regulated power supplies with less than 1% ripple be incorporated into the design of an audio system.

DISTORTION PERFORMANCE AND TESTING

The THD+N figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. The THD+N specification, therefore, provides a direct method to classify and choose an audio DAC for a desired level of performance. Figure 1 illustrates the typical THD+N performance of the AD1864 versus frequency. A load impedance of at least 1.5 kΩ is recommended for best THD+N performance.

Analog Devices tests and grades all AD1864s on the basis of THD+N performance. During the distortion test, a high-speed digital pattern generator transmits digital data to each channel of the device under test. Eighteen-bit data is latched into the DAC at 352.8 kHz (8 × Fs). The test waveform is a 990.5 kHz sine wave with 0 dB, −20 dB and −60 dB amplitudes. A 4096 point FFT calculates total harmonic distortion + noise, signal-to-noise ratio, D-Range and channel separation. No deglitchers or MSB trims are used.

OPTIONAL MSB ADJUSTMENT

Use of optional adjust circuitry allows residual distortion error to be eliminated. This distortion is especially important when low-amplitude signals are being reproduced. The MSB-adjust circuitry is shown in Figure 8. The trim pot should be adjusted to produce the lowest distortion using an input signal with a −60 dB amplitude.

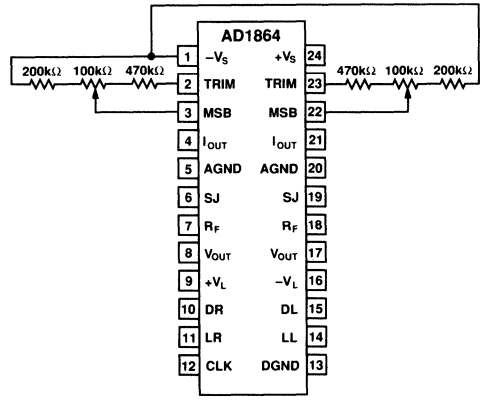


Figure 8. Optional DIP THD+N Adjust Circuitry

CURRENT OUTPUT MODE

One or both channels of the AD1864 can be operated in current output mode. I_{OUT} can be used to directly drive an external current-to-voltage (I-V) converter. The internal feedback resistor, R_F, can still be used in the feedback path of the external I-V converter, thus assuring that R_F tracks the DAC over time and temperature.

Of course, the AD1864 can also be used in voltage output mode utilizing the onboard I-V converter.

VOLTAGE OUTPUT MODES

As shown in the AD1864 block diagram, each channel of the AD1864 is complete with an I-V converter and a feedback resistor. These can be connected externally to provide direct voltage output from one or both AD1864 channels. Figure 7 shows these connections. I_{OUT} is connected to the summing junction, SJ. V_{OUT} is connected to the feedback resistor, R_F. This implementation results in the lowest possible component count and achieves the performance shown on the specifications page while operating at 8 × F_S.

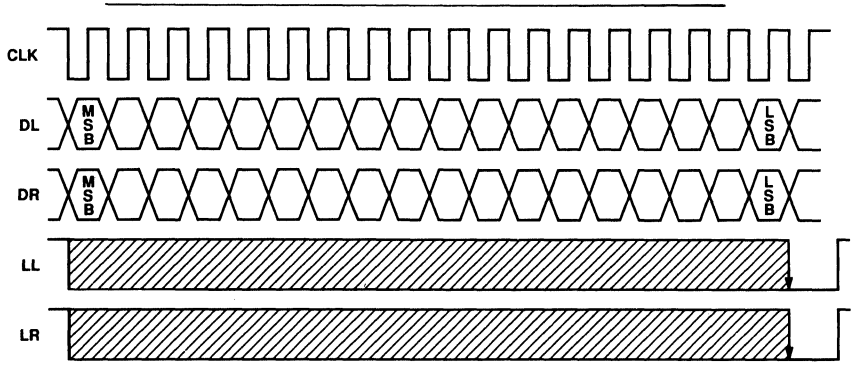


Figure 9. AD1864 Control Signals

INPUT DATA

Data is transmitted to the AD1864 in a bit stream composed of 18-bit words with a serial, 2s complement, MSB first format. Data Left (DL) and Data Right (DR) are the serial inputs for the left and right DACs, respectively. Similarly, Latch Left (LL) and Latch Right (LR) update the left and right DACs. The falling edges of LL and LR cause the last 18 bits which were clocked into the Serial Registers to be shifted into the DACs, thereby updating the DAC outputs. Left and Right channels share the Clock (CLK) signal. Data is clocked into the input registers on the rising edge of CLK.

Figure 9 illustrates the general signal requirements for data transfer for the AD1864.

TIMING

Figure 10 illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished properly. The input pins of the AD1864 are both TTL and 5 V CMOS compatible.

The minimum clock rate of the AD1864 is at least 12.7 MHz. This clock rate allows data transfer rates of 2×, 4×, 8× and 16×F_S (where F_S equals 44.1 kHz). The applications section of this datasheet contains additional guidelines for using the AD1864.

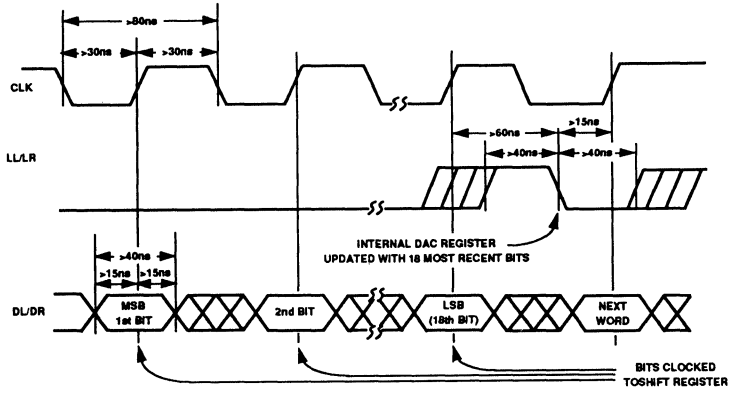


Figure 10. AD1864 Timing Diagram

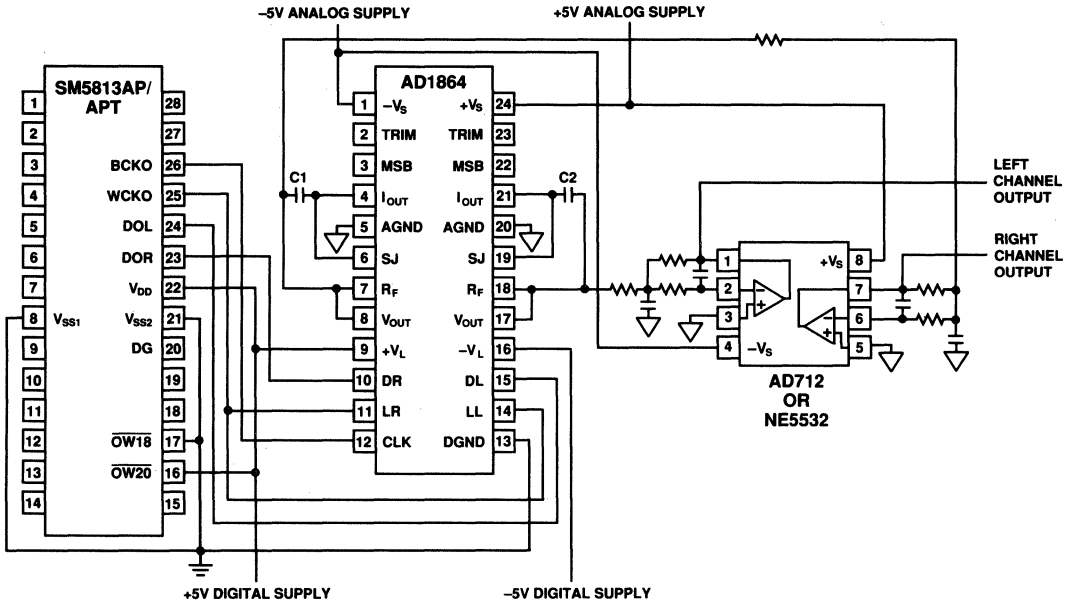


Figure 11. Complete 8 × F_S 18-Bit CD Player

18-BIT CD PLAYER DESIGN

Figure 11 illustrates an 18-bit CD player design incorporating an AD1864 D/A converter, an AD712 or NE5532 dual op amp and the SM5813 digital filter chip manufactured by NPC. In this design, the SM5813 filter transmits left and right digital data to both channels of the AD1864. The left and right latch signals, LL and LR, are both provided by the word clock signal (WCKO) of the digital filter. The digital filter supplies data at an 8 × F_S oversample rate to each channel.

The digital data is converted to analog output voltages by the output amplifiers on the AD1864. Note that no external components are required by the AD1864. Also, no deglitching circuitry is required.

An AD712 or NE5532 dual op amp is used to provide the output antialias filters required for adequate image rejection. One 2-pole filter section is provided for each channel. An additional pole is created from the combination of the internal feedback resistors (R_F) and the external capacitors C1 and C2. For example, the nominal 3 kΩ R_F with a 360 pF capacitor for C1 and C2 will place a pole at approximately 147 kHz, effectively eliminating all high frequency noise components.

Close matching of the ac characteristics of the amplifiers on the AD712 as well as their low distortion make it an ideal choice for the task.

Low distortion, superior channel separation, low power consumption and a low component count are all realized by this simple design.

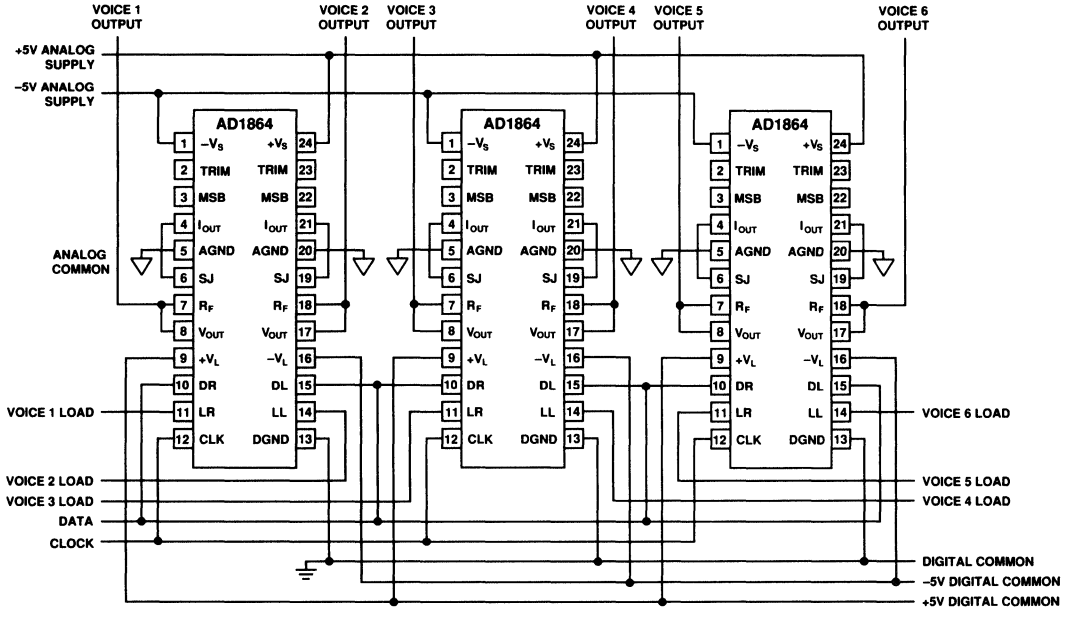


Figure 12. Cascaded AD1864s in a Multichannel Keyboard Instrument

MULTICHANNEL DIGITAL KEYBOARD DESIGN

Figure 12 illustrates how to cascade AD1864s to add multiple voices to an electronic musical instrument. In this example, the data and clock signals are shared between all six DACs. As the data representing an output for a specific voice is loaded, the appropriate DAC is updated. For example, after the 18 bits representing the next output value for Voice #4 is clocked out on the data line, then "Voice 4 Load" is pulled low. This produces a new output for Voice 4. Furthermore, all voices can be returned to the same output by pulling all six load signals low.

In this application, the advantages of choosing the AD1864 are clear. Its flexible digital interface allows the clock and data to be shared among all DACs. This reduces printed circuit board area requirements and also simplifies the actual layout of the board. The low power requirement of the AD1864 (typically 215 mW) is an advantage in a multiple DAC system where its power advantage is multiplied by the number of DACs used. The AD1864 requires no external components, simplifying the design, reducing the total number of components required and enhancing reliability.

ADDITIONAL APPLICATIONS

Figures 13 through 16 show connection diagrams for the AD1864 and a number of standard digital filter chips from Yamaha, NPC and Sony. Figure 13 shows the SM5814AP operating with pipelined data. Cophase operation is not available with the SM5814AP in 18-bit mode. Figures 14 through 16 are all examples of cophase operation. Each application operates at $8 \times F_S$ for each channel. The 2-pole Rauch low pass filters shown in Figure 11 can be used with all of the applications shown in this data sheet. The AD711 single op amp can also be used in these applications in order to ensure maximum channel separation.

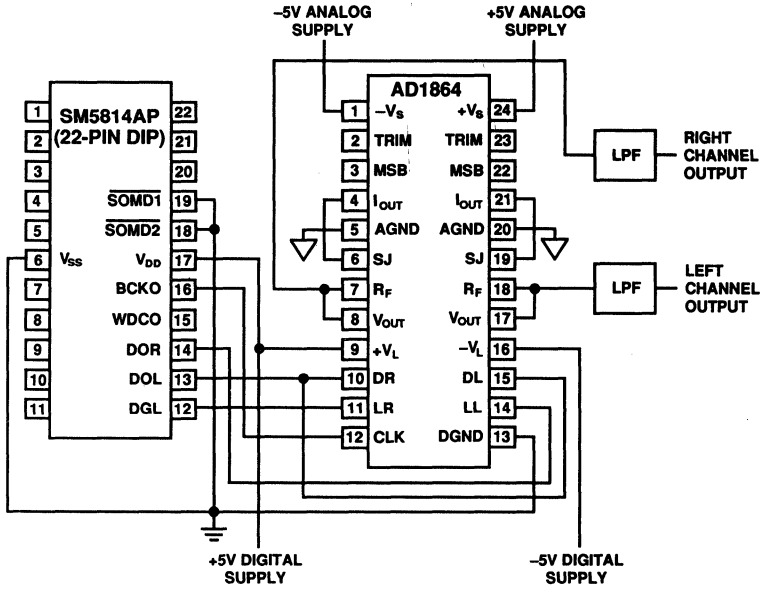


Figure 13. AD1864 with NPC SM5814AP Digital Filter

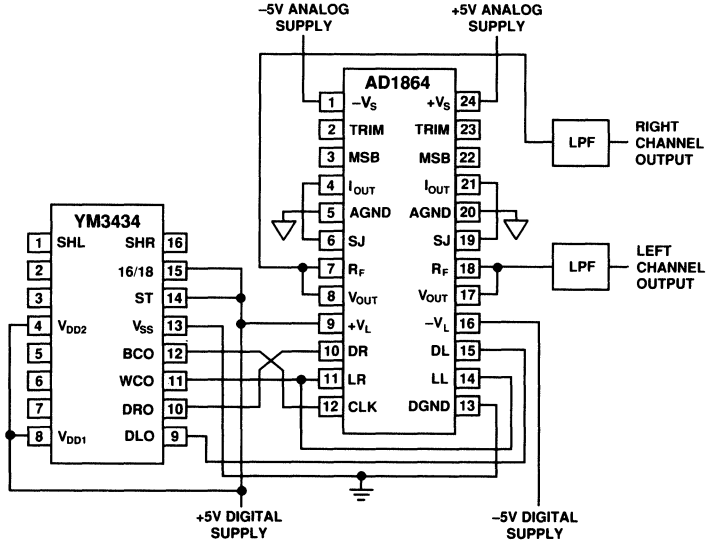


Figure 14. AD1864 with Yamaha YM3434 Digital Filter

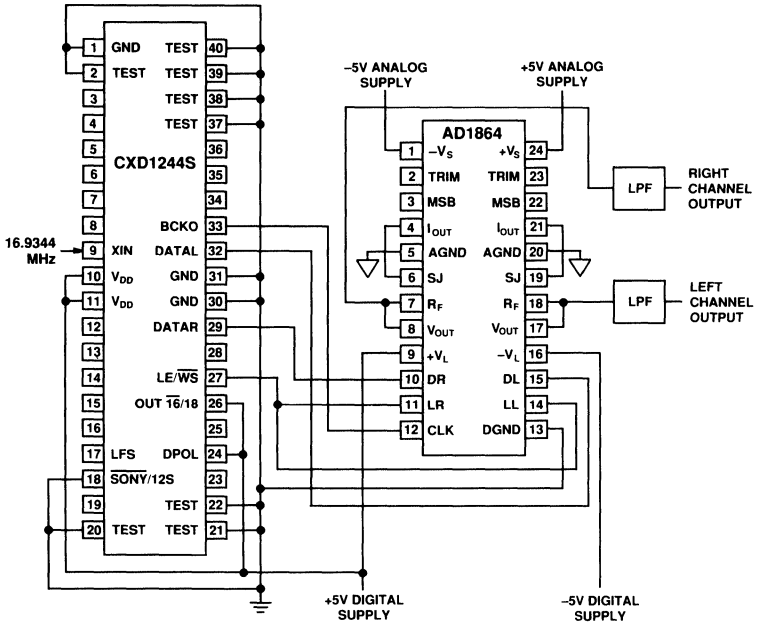


Figure 15. AD1864 with Sony CXD1244S Digital Filter

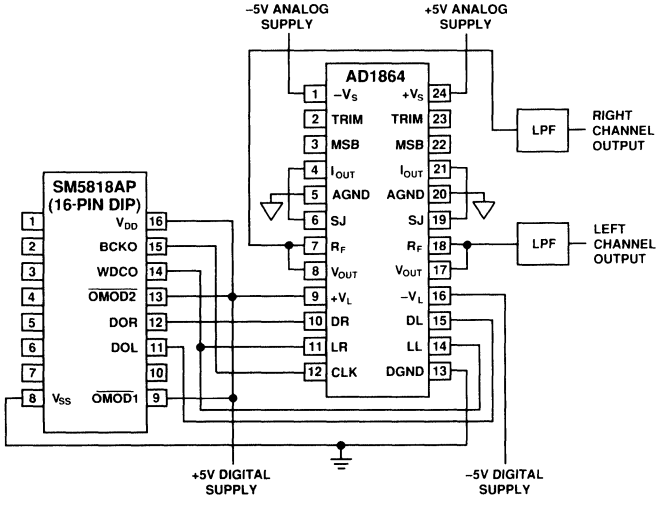


Figure 16. AD1864 with NPC SM5818AP Digital Filter

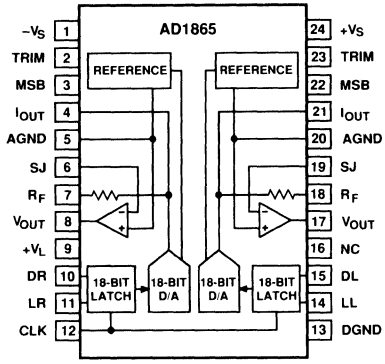
Complete Dual 18-Bit 16 × F_S Audio DAC

AD1865*

FEATURES
Dual Serial Input, Voltage Output DACs
No External Components Required
110 dB SNR
0.003% THD+N
Operates at 16 × Oversampling per Channel
±5 Volt Operation
Cophased Outputs
116 dB Channel Separation
Pin Compatible with AD1864
DIP or SOIC Packaging

APPLICATIONS
Multichannel Audio Applications:
Compact Disc Players
Multivoice Keyboard Instruments
DAT Players and Recorders
Digital Mixing Consoles
Multimedia Workstations

FUNCTIONAL BLOCK DIAGRAM
(DIP Package)



NC = NO CONNECT

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PRODUCT DESCRIPTION

The AD1865 is a complete, dual 18-bit DAC offering excellent THD+N and SNR while requiring no external components. Two complete signal channels are included. This results in cophased voltage or current output signals and eliminates the need for output demultiplexing circuitry. The monolithic AD1865 chip includes CMOS logic elements, bipolar and MOS linear elements and laser-trimmed thin-film resistor elements, all fabricated on Analog Devices' ABCMOS process.

The DACs on the AD1865 chip employ a partially segmented architecture. The first four MSBs of each DAC are segmented into 15 elements. The 14 LSBs are produced using standard R-2R techniques. Segment and R-2R resistors are laser trimmed to provide extremely low total harmonic distortion. This architecture minimizes errors at major code transitions resulting in low output glitch and eliminating the need for an external deglitcher. When used in the current output mode, the AD1865 provides two ±1 mA output signals.

Each channel is equipped with a high performance output amplifier. These amplifiers achieve fast settling and high slew rate, producing ±3 V signals at load currents up to 8 mA. Each output amplifier is short-circuit protected and can withstand indefinite short circuits to ground.

The AD1865 was designed to balance two sets of opposing requirements, channel separation and DAC matching. High channel separation is the result of careful layout. At the same time, both channels of the AD1865 have been designed to ensure matched gain and linearity as well as tracking over time and temperature. This assures optimum performance when used in stereo and multi-DAC per channel applications.

A versatile digital interface allows the AD1865 to be directly connected to standard digital filter chips. This interface employs five signals: Data Left (DL), Data Right (DR), Latch Left (LL), Latch Right (LR) and Clock (CLK). DL and DR are the serial input pins for the left and right DAC input registers. Input data bits are clocked into the input register on the rising edge of CLK. A low-going latch edge updates the respective DAC output. For systems using only a single latch signal, LL and LR may be connected together. For systems using only one DATA signal, DR and DL may be connected together.

The AD1865 operates with ±5 V power supplies. The digital supply, V_L, can be separated from the analog supplies, V_S and $-V_S$, for reduced digital feedthrough. Separate analog and digital ground pins are also provided. The AD1865 typically dissipates only 225 mW, with a maximum power dissipation of 260 mW.

The AD1865 is packaged in both a 24-pin plastic DIP and a 28-pin SOIC package. Operation is guaranteed over the temperature range of −25°C to +70°C and over the voltage supply range of ±4.75 V to ±5.25 V.

PRODUCT HIGHLIGHTS

1. The AD1865 is a Complete Dual 18-Bit Audio DAC.
2. 110 dB Signal-To-Noise Ratio for low noise operation.
3. THD+N is typically 0.003%.
4. Interchannel gain and midscale matching.
5. Output voltages and currents are cophased.
6. Low glitch for improved sound quality.
7. Both channels are 100% tested at 16 × F_S.
8. Low Power—only 225 mW typ, 260 mW max.
9. Five-wire interface for individual DAC control.
10. 24-pin DIP or 28-pin SOIC packages available.

AD1865—SPECIFICATIONS (T_A = +25°C, $+V_L$ = $+V_S$ = +5 V and $-V_S$ = −5 V, F_S = 705.6 kHz, no MSB adjustment or deglitcher)

Parameter		Min	Typ	Max	Unit
RESOLUTION			18		Bits
DIGITAL INPUTS	V_{IH}	2.0		$+V_L$	V
	V_{IL}			0.8	V
	I_{IH}, V_{IH} = $+V_L$			**1.0**	μA
	I_{IL}, V_{IL} = 0.4 V			**−10**	μA
Clock Input Frequency		**13.5**			MHz
ACCURACY					
Gain Error			0.2	**1.0**	% of FSR
Interchannel Gain Matching			0.3	**0.8**	% of FSR
Midscale Error			4		mV
Interchannel Midscale Matching			5		mV
Gain Linearity (0 dB to −90 dB)			<2		dB
DRIFT (0°C to +70°C)					
Gain Drift			±25		ppm of FSR/°C
Midscale Drift			±4		ppm of FSR/°C
TOTAL HARMONIC DISTORTION + NOISE*					
0 dB, 990.5 Hz	AD1865N, R		0.004	**0.006**	%
	AD1865N-J, R-J		0.003	**0.004**	%
−20 dB, 990.5 Hz	AD1865N, R		0.010	**0.040**	%
	AD1865N-J, R-J		0.010	**0.020**	%
−60 dB, 990.5 Hz	AD1865N, R		1.0	**4.0**	%
	AD1865N-J, R-J		1.0	**2.0**	%
CHANNEL SEPARATION*					
0 dB, 990.5 Hz		**110**	116		dB
SIGNAL-TO-NOISE RATIO* (20 Hz to 30 kHz)		**107**	110		dB
D-RANGE* (with A-Weight Filter)					
−60 dB, 990.5 Hz	AD1865N, R	**88**	100		dB
	AD1865N-J, R-J	**94**	100		dB
OUTPUT					
Voltage Output Configuration					
Output Range (±1%)		**±2.94**	±3.0	**±3.06**	V
Output Impedance			0.1		Ω
Load Current		±8			mA
Short Circuit Duration			Indefinite to Common		
Current Output Configuration					
Bipolar Output Range (±30%)			±1		mA
Output Impedance (±30%)			1.7		kΩ
POWER SUPPLY					
$+V_L$ and $+V_S$		4.75	**5.0**	5.25	V
$-V_S$		−5.25	**−5.0**	−4.75	V
+I, $+V_L$ and $+V_S$ = +5 V			22	**26**	mA
−I, $-V_S$ = −5 V			−23	**−26**	mA
POWER DISSIPATION, $+V_L$ = $+V_S$ = +5 V, $-V_S$ = −5 V			225	**260**	mW
TEMPERATURE RANGE					
Specification		0	**+25**	+70	°C
Operation		−25		+70	°C
Storage		−60		+100	°C
WARMUP TIME		1			min

Specifications shown in **boldface** are tested on production units at final test without optional MSB adjustment.
*Tested in accordance with EIAJ Test Standard CP-307 with 18-bit data.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_L to DGND . . . . . 0 to 6.0 V
V_S to AGND . . . . . 0 to 6.0 V
$-V_S$ to AGND . . . . . −6.0 to 0 V
AGND to DGND . . . . . ±0.3 V
Digital Inputs to DGND . . . . . −0.3 to V_L
Short Circuit Protection . . . . . Indefinite Short to Ground
Soldering . . . . . 300°C, 10 sec

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING GUIDE

Model	Temperature Range	THD+N @ FS	Package Option*
AD1865N	−25°C to +70°C	0.006%	N-24
AD1865N-J	−25°C to +70°C	0.004%	N-24
AD1865R	−25°C to +70°C	0.006%	R-28
AD1865R-J	−25°C to +70°C	0.004%	R-28

*N = Plastic DIP, R = Small Outline IC Package. For outline information see Package Information section.

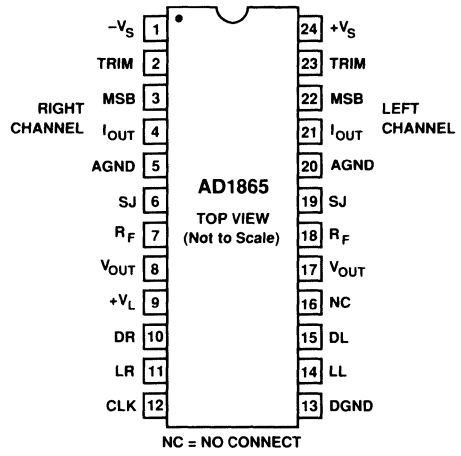
PIN DESIGNATIONS

DIP	SOIC		
1	22	$-V_S$	Negative Analog Supply
2	23	TRIM	Right Channel Trim Network Connection
3	24	MSB	Right Channel Trim Potentiometer Wiper Connection
4	26	I_{OUT}	Right Channel Output Current
5	28	AGND	Analog Common Pin
6	1	SJ	Right Channel Amplifier Summing Junction
7	2	R_F	Right Channel Feedback Resistor
8	3	V_{OUT}	Right Channel Output Voltage
9	4	$+V_L$	Positive Digital Supply
10	5	DR	Right Channel Data Input Pin
11	6	LR	Right Channel Latch Pin
12	7	CLK	Clock Input Pin
13	8	DGND	Digital Common Pin
14	9	LL	Left Channel Latch Pin
15	10	DL	Left Channel Data Input Pin
16	11, 16, 18 25, 27	NC	No Internal Connection*
17	12	V_{OUT}	Left Channel Output Voltage
18	13	R_F	Left Channel Feedback Resistor
19	14	SJ	Left Channel Amplifier Summing Junction
20	15	AGND	Analog Common Pin
21	17	I_{OUT}	Left Channel Output Current
22	19	MSB	Left Channel Trim Potentiometer Wiper Connection
23	20	TRIM	Left Channel Trim Network Connection
24	21	$+V_S$	Positive Analog Supply

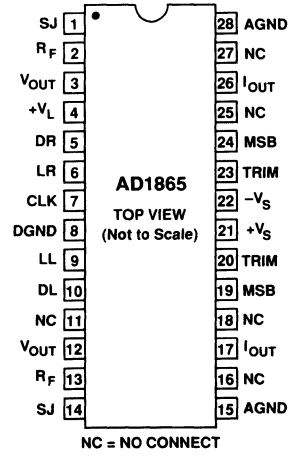
*Pin 16 has no internal connection; $-V_L$ from AD1864 DIP socket can be safely applied.

PINOUT

(24-Pin DIP Package)



(28-Pin SOIC Package)



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AD1865—Definition of Specifications

TOTAL HARMONIC DISTORTION + NOISE

Total harmonic distortion plus noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the amplitudes of the harmonics and noise to the value of the fundamental input frequency. It is usually expressed in percent.

THD+N is a measure of the magnitude and distribution of linearity error, differential linearity error, quantization error and noise. The distribution of these errors may be different, depending on the amplitude of the output signal. Therefore, to be most useful, THD+N should be specified for both large (0 dB) and small (−20 dB, −60 dB) signal amplitudes. THD+N measurements for the AD1865 are made using the first 19 harmonics and noise out to 30 kHz.

SIGNAL-TO-NOISE RATIO

The signal-to-noise ratio is defined as the ratio of the amplitude of the output when a full-scale code is entered to the amplitude of the output when a midscale code is entered. It is measured using a standard A-Weight filter. SNR for the AD1865 is measured for noise components out to 30 kHz.

CHANNEL SEPARATION

Channel separation is defined as the ratio of the amplitude of a full-scale signal appearing on one channel to the amplitude of that same signal which couples onto the adjacent channel. It is usually expressed in dB. For the AD1865 channel separation is measured in accordance with EIAJ Standard CP-307, Section 5.5.

D-RANGE DISTORTION

D-Range distortion is equal to the value of the total harmonic distortion + noise (THD+N) plus 60 dB when a signal level of −60 dB below full scale is reproduced. D-Range is tested with a 1 kHz input sine wave. This is measured with a standard A-Weight filter as specified by EIAJ Standard CP-307.

GAIN ERROR

The gain error specification indicates how closely the output of a given channel matches the ideal output for given input data. It is expressed in % of FSR and is measured with a full-scale output signal.

INTERCHANNEL GAIN MATCHING

The gain matching specification indicates how closely the amplitudes of the output signals match when producing identical input data. It is expressed in % of FSR (Full-Scale Range = 6 V for the AD1865) and is measured with full-scale output signals.

MIDSCALE ERROR

Midscale error is the deviation of the actual analog output of a given channel from the ideal output (0 V) when the twos complement input code representing half scale is loaded into the input register of the DAC. It is expressed in mV and is measured with half-scale output signals.

INTERCHANNEL MIDSCALE MATCHING

The midscale matching specification indicates how closely the amplitudes of the output signals of the two channels match when the twos complement input code representing half scale is loaded into the input register of both channels. It is expressed in mV and is measured with half-scale output signals.

FUNCTIONAL DESCRIPTION

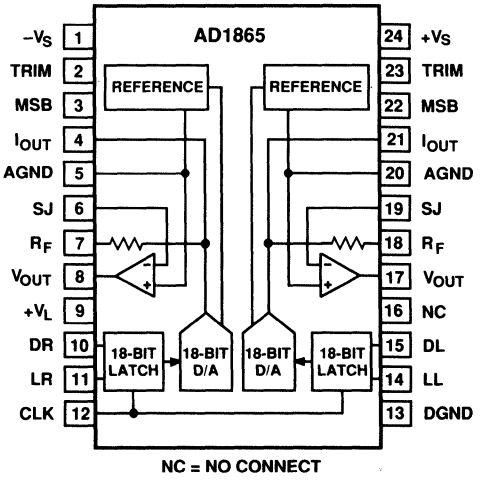
The AD1865 is a complete, monolithic, dual 18-bit audio DAC. No external components are required for operation. As shown in the block diagram, each chip contains two voltage references, two output amplifiers, two 18-bit serial input registers and two 18-bit DACs.

The voltage reference section provides a reference voltage for each DAC circuit. These voltages are produced by low-noise bandgap circuits. Buffer amplifiers are also included. This combination of elements produces reference voltages that are unaffected by changes in temperature and age.

The output amplifiers use both MOS and bipolar devices and incorporate an all NPN output stage. This design technique produces higher slew rate and lower distortion than previous techniques. Frequency response is also improved. When combined with the appropriate on-chip feedback resistor, the output op amps convert the output current to output voltages.

The 18-bit D/A converters use a combination of segmented decoder and R–2R architecture to achieve consistent linearity and differential linearity. The resistors which form the ladder structure are fabricated with silicon chromium thin film. Laser trimming of these resistors further reduces linearity errors resulting in low output distortion.

The input registers are fabricated with CMOS logic gates. These gates allow the achievement of fast switching speeds and low power consumption, contributing to the low glitch and low power dissipation of the AD1865.



AD1865 Block Diagram (DIP Package)

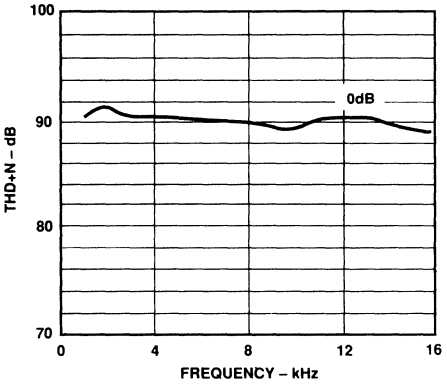


Figure 1. THD+N (dB) vs. Frequency (kHz)

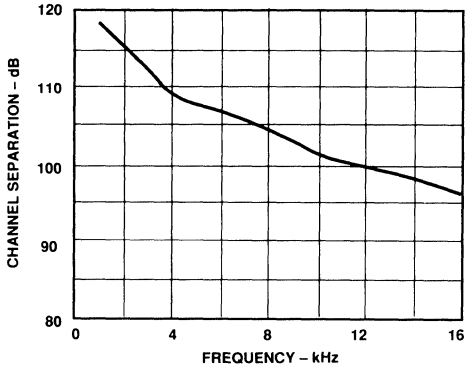


Figure 2. Channel Separation (dB) vs. Frequency (kHz)

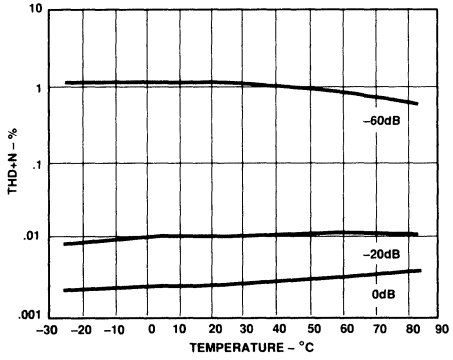


Figure 3. THD+N (%) vs. Temperature (°C)

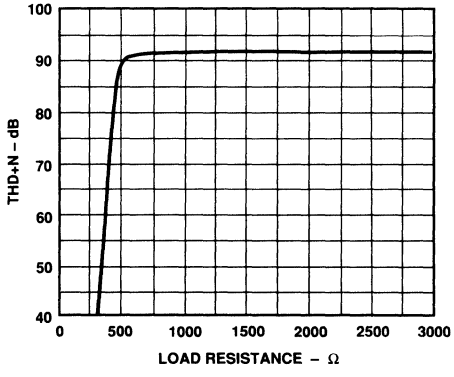


Figure 4. THD+N (dB) vs. Load Resistance (Ω)

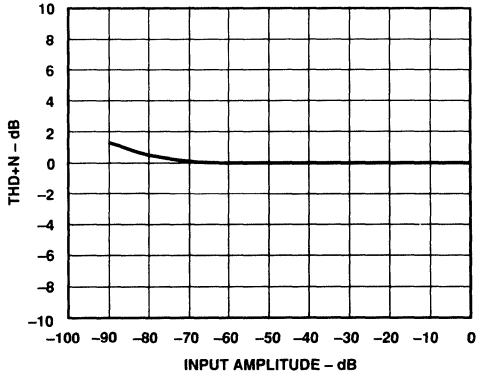


Figure 5. Gain Linearity (dB) vs. Input Amplitude (dB)

AD1865—Analog Circuit Consideration

GROUNDING RECOMMENDATIONS

The AD1865 has three ground pins, two labeled AGND and one labeled DGND. AGND, the analog ground pins, are the "high quality" ground references for the device. To minimize distortion and reduce crosstalk between channels, the analog ground pins should be connected together only at the analog common point in the system. As shown in Figure 6, the AGND pins should *not* be connected at the chip.

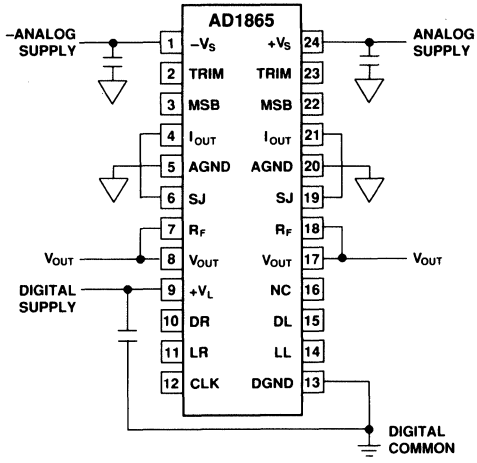


Figure 6. Recommended Circuit Schematic

The digital ground pin returns ground current from the digital logic portions of the AD1865 circuitry. This pin should be connected to the digital common pin in the system. Other digital logic chips should also be referred to that point. The analog and digital grounds should be connected together at one point in the system, preferably at the power supply.

POWER SUPPLIES AND DECOUPLING

The AD1865 has three power supply input pins. $\pm V_S$ provides the supply voltages which operate the analog portions of the DAC including the voltage references, output amplifiers and control amplifiers. The $\pm V_S$ supplies are designed to operate from ±5 V supplies. Each supply should be decoupled to analog common using a 0.1 μF capacitor in parallel with a 10 μF capacitor. Good engineering practice suggests that the bypass capacitors be placed as close as possible to the package pins. This minimizes the parasitic inductive effects of printed circuit board traces.

The $+V_L$ supply operates the digital portions of the chip including the input shift registers and the input latching circuitry. This supply should be bypassed to digital common using a 0.1 μF capacitor in parallel with a 10 μF capacitor. $+V_L$ operates with a +5 V supply. In order to assure proper operation of the AD1865, $-V_S$ must be the most negative power supply voltage at all times.

Though separate positive power supply pins are provided for the analog and digital portions of the AD1865, it is also possible to use the AD1865 in systems featuring a single +5 V power supply. In this case, both the $+V_S$ and $+V_L$ input pins should be connected to the single +5 V power supply. This feature allows reduction of the cost and complexity of the system power supply.

As with most linear circuits, changes in the power supplies will affect the output of the DAC. Analog Devices recommends that well regulated power supplies with less than 1% ripple be incorporated into the design of an audio system.

DISTORTION PERFORMANCE AND TESTING

The THD+N figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. The THD+N specification, therefore, provides a direct method to classify and choose an audio DAC for a desired level of performance. Figure 1 illustrates the typical THD+N performance of the AD1865 versus frequency. A load impedance of at least 1.5 kΩ is recommended for best THD+N performance.

Analog Devices tests and grades all AD1865s on the basis of THD+N performance. During the distortion test, a high-speed digital pattern generator transmits digital data to each channel of the device under test. Eighteen-bit data is transmitted at 705.6 kHz ($16 \times F_S$). The test waveform is a 990.5 Hz sine wave with 0 dB, −20 dB and −60 dB amplitudes. A 4096 point FFT calculates total harmonic distortion + noise, signal-to-noise ratio, D-Range and channel separation. No deglitchers or MSB trims are used in the testing of the AD1865.

OPTIONAL MSB ADJUSTMENT

Use of optional adjust circuitry allows residual distortion error to be eliminated. This distortion is especially important when low amplitude signals are being reproduced. The MSB adjust circuitry is shown in Figure 7. The trim potentiometer should be adjusted to produce the lowest distortion using an input signal with a −60 dB amplitude.

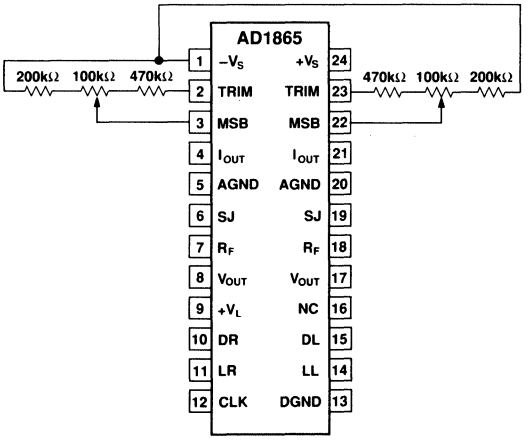


Figure 7. Optional THD+N Adjust Circuitry

CURRENT OUTPUT MODE

One or both channels of the AD1865 can be operated in current output mode. I_{OUT} can be used to directly drive an external current-to-voltage (I-V) converter. The internal feedback resistor, R_F, can still be used in the feedback path of the external I-V converter, thus assuring that R_F tracks the DAC over time and temperature.

Of course, the AD1865 can also be used in voltage output mode in order to utilize the onboard I-V converter.

VOLTAGE OUTPUT MODES

As shown on the block diagram, each channel of the AD1865 is complete with an I-V converter and a feedback resistor. These can be connected externally to provide direct voltage output from one or both AD1865 channels. Figure 6 shows these connections. I_{OUT} is connected to the Summing Junction, SJ. V_{OUT} is connected to the feedback resistor, R_F. This implementation results in the lowest possible component count and achieves the specifications shown on the Specifications page while operating at 16 × F_S.

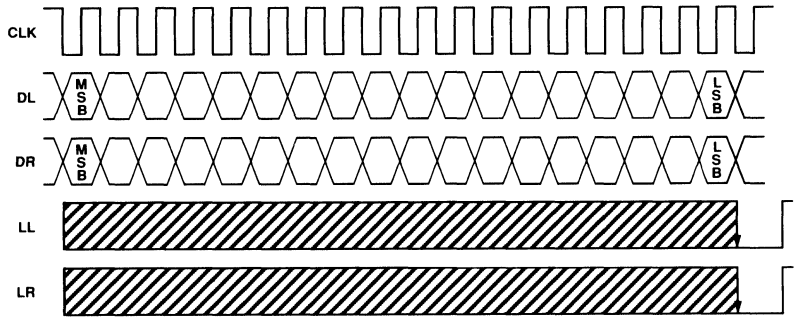


Figure 8. AD1865 Control Signals

INPUT DATA

Data is transmitted to the AD1865 in a bit stream composed of 18-bit words with a serial, twos complement, MSB first format. Data Left (DL) and Data Right (DR) are the serial inputs for the left and right DACs, respectively. Similarly, Latch Left (LL) and Latch Right (LR) update the left and right DACs. The falling edge of LL and LR cause the last 18 bits which were clocked into the Serial Registers to be shifted into the DACs, thereby updating the DAC outputs. Left and Right channels share the Clock (CLK) signal. Data is clocked into the input registers on the rising edge of CLK.

Figure 8 illustrates the general signal requirements for data transfer for the AD1865.

TIMING

Figure 9 illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished properly. The input pins of the AD1865 are both TTL and 5 V CMOS compatible.

The minimum clock rate of the AD1865 is at least 13.5 MHz. This clock rate allows data transfer rates of 2×, 4×, 8× and 16 × F_S (where F_S equals 44.1 kHz).

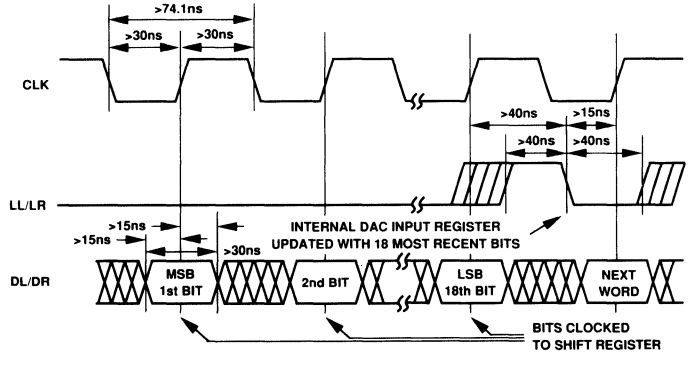


Figure 9. AD1865 Timing Diagram

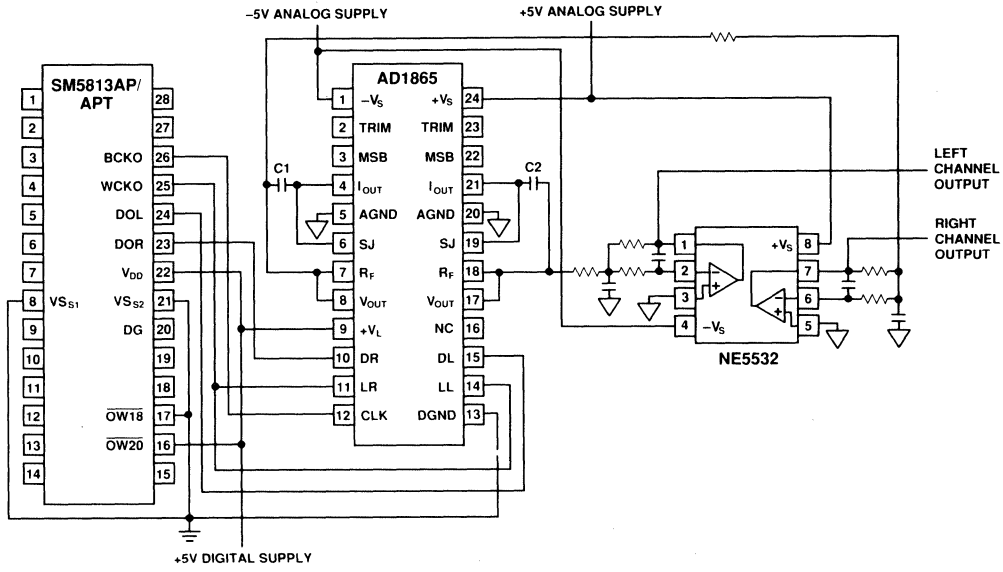


Figure 10. Complete 8 × F_S 18-Bit CD Player

18-BIT CD PLAYER DESIGN

Figure 10 illustrates an 18-bit CD player design incorporating an AD1865 D/A converter, an NE5532 dual op amp and the SM5813 digital filter chip manufactured by NPC. In this design, the SM5813 filter transmits left and right digital data to both channels of the AD1865. The left and right latch signals, LL and LR, are both provided by the word clock signal (WCKO) of the digital filter. The digital filter supplies data at an 8 × F_S oversample rate to each channel.

The digital data is converted to analog output voltages by the output amplifiers on the AD1865. Note that no external components are required by the AD1865. Also, no deglitching circuitry is required.

An NE5532 dual op amp is used to provide the output antialias filters required for adequate image rejection. One 2-pole filter section is provided for each channel. An additional pole is created from the combination of the internal feedback resistors (R_F) and the external capacitors C1 and C2. For example, the nominal 3 kΩ R_F with a 360 pF capacitor for C1 and C2 will place a pole at approximately 147 kHz, effectively eliminating all high frequency noise components.

Low distortion, superior channel separation, low power consumption and a low parts count are all realized by this simple design.

MULTICHANNEL DIGITAL KEYBOARD DESIGN

Figure 11 illustrates how to cascade AD1865's to add multiple voices to an electronic musical instrument. In this example, the data and clock signals are shared between all six DACs. As the data representing an output for a specific voice is loaded, the appropriate DAC is updated. For example, after the 18-bits representing the next output value for Voice 4 is clocked out on the data line, then "Voice 4 Load" is pulled low. This produces a new output for Voice 4. Furthermore, all voices can be returned to the same output by pulling all six load signals low.

In this application, the advantages of choosing the AD1865 are clear. Its flexible digital interface allows the clock and data to be shared among all DACs. This reduces PC board area requirements and also simplifies the actual layout of the board. The low power requirements of the AD1865 (approximately 225 mW) is an advantage in a multiple DAC system where any power advantage is multiplied by the number of DACs used. The AD1865 requires no external components, simplifying the design, reducing the total number of components required and enhancing reliability.

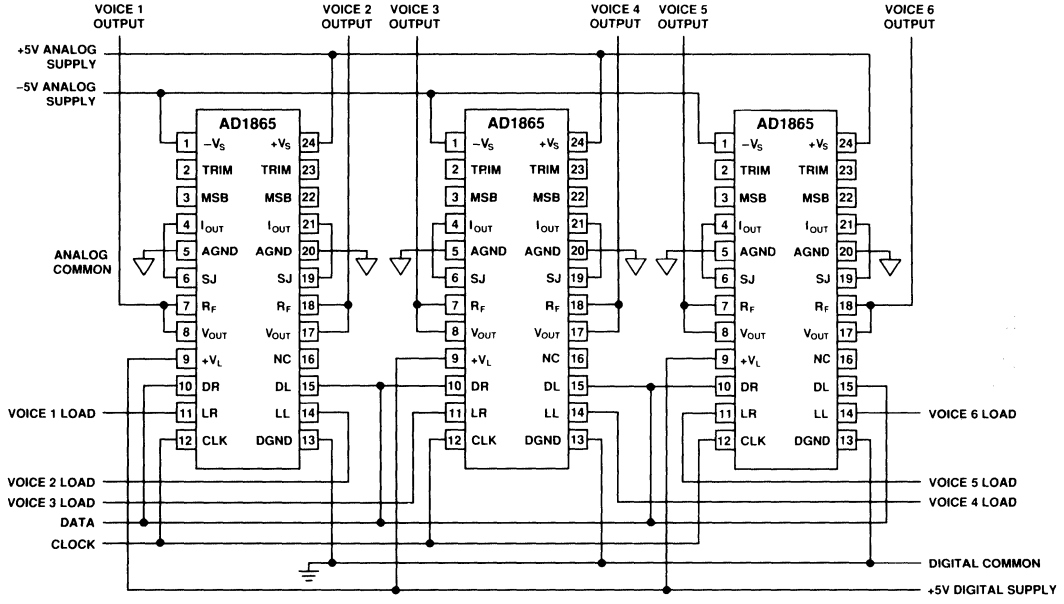


Figure 11. Cascaded AD1865s in a Multichannel Keyboard Instrument

ADDITIONAL APPLICATIONS

Figures 12 through 14 show connection diagrams for the AD1865 and standard digital filter chips from Yamaha, NPC and Sony. Each figure is an example of cophase operation operating at 8 × F_S for each channel. The 2-pole Rauch low pass filters shown in Figure 10 can be used with all of the applications shown in this data sheet.

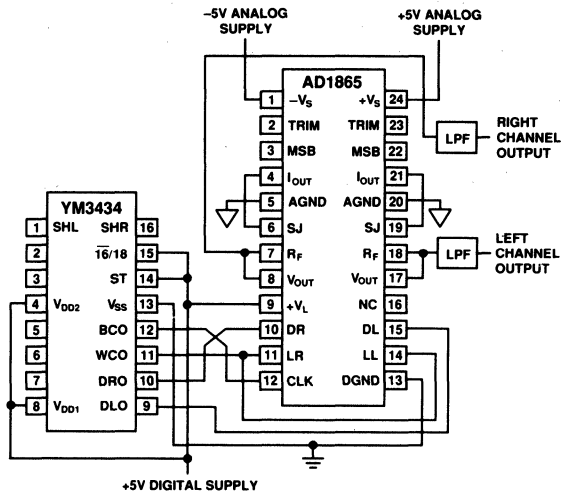


Figure 12. AD1865 with Yamaha YM3434 Digital Filter

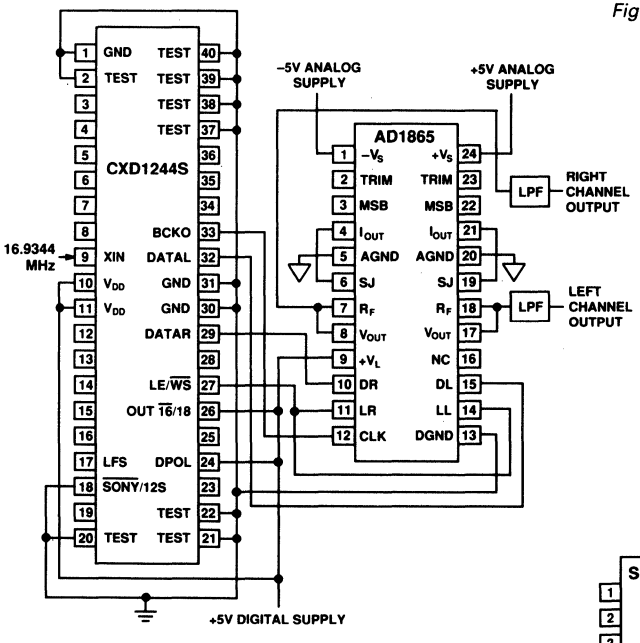


Figure 13. AD1865 with Sony CXD1244s Digital Filter

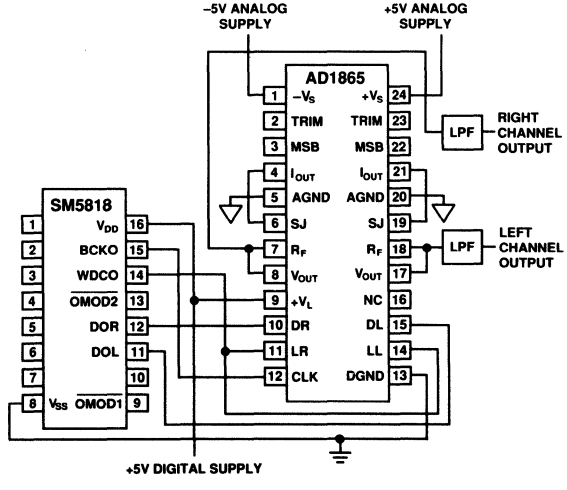


Figure 14. AD1865 with NPC SM5818AP Digital Filter

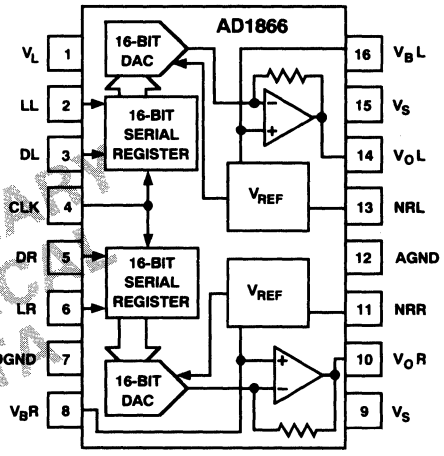
Single Supply Dual 16-Bit Audio DAC

AD1866*

FEATURES
Dual Serial Input, Voltage Output DACs
Single +5 Volt Supply
0.005% THD+N
Low Power–45 mW
115 dB Channel Separation
Operates at 8× Oversampling
16-Pin Plastic DIP or SOIC Package

APPLICATIONS
Multimedia Workstations
PC Audio Add-In Boards
Portable CD and DAT Players
Automotive CD and DAT Players
Noise Cancellation

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1866 is a complete dual 16-bit DAC offering excellent performance while requiring a single +5 V power supply. It is fabricated on Analog Devices' ABCMOS wafer fabrication process. The monolithic chip includes CMOS logic elements, bipolar and MOS linear elements and laser trimmed, thin film resistor elements. Careful design and layout techniques have resulted in low distortion, low noise, high channel separation and low power dissipation.

The DACs on the AD1866 chip employ a partially segmented architecture. The first three MSBs of each DAC are segmented into 7 elements. The 13 LSBs are produced using standard R-2R techniques. The segments and R-2R resistors are laser trimmed to provide extremely low total harmonic distortion. The AD1866 requires no deglitcher or trimming circuitry.

Each DAC is equipped with a high performance output amplifier. These amplifiers achieve fast settling and high slew rate, producing ±1 V signals at load currents up to ±1 mA. The buffered output signal range is 1.5 V to 3.5 V. The 2.5 V reference voltages eliminate the need for "false ground" networks.

A versatile digital interface allows the AD1866 to be directly connected to all digital filter chips. Fast CMOS logic elements allow for an input clock rate of up to 16 MHz. This allows for operation at 2×, 4×, 8×, or 16× the sampling frequency (where F_S = 44.1 kHz) for each channel. The digital input pins of the AD1866 are TTL and +5 V CMOS compatible.

The AD1866 operates on +5 V power supplies. The digital supply, V_L, can be separated from the analog supply, V_S, for reduced digital feedthrough. Separate analog and digital ground pins are also provided. In systems employing a single +5 volt power supply, V_L and V_S should be connected together. In battery operated systems, operation will continue even with reduced supply voltage. Typically, the AD1866 dissipates 45 mW.

The AD1866 is packaged in either a 16-pin plastic DIP or a 16-pin plastic SOIC package. Operation is guaranteed over the temperature range of −35°C to +85°C and over the voltage supply range of 4.75 V to 5.25 V.

PRODUCT HIGHLIGHTS

1. Single supply operation @ +5 V.
2. 45 mW power dissipation.
3. THD+N is 0.005% (typical).
4. Signal-to-Noise Ratio is 95 dB (typical).
5. 115 dB channel separation (typical).
6. Compatible with all digital filter chips.
7. 16-pin DIP and 16-pin SOIC packages.
8. No deglitcher required.
9. No external adjustments required.

AD1866—SPECIFICATIONS (T_A = 25°C and +5 V supplies unless otherwise noted)

	Min	Typ	Max	Unit
RESOLUTION		16		Bits
DIGITAL INPUTS V_{IH}	2.4			V
V_{IL}			0.8	V
I_{IH}, V_{IH} = V_L		1.0		μA
I_{IL}, V_{IL} = DGND		−10.0		μA
Maximum Clock Input Frequency	13.5			MHz
ACCURACY				
Gain Error		±3		% of FSR
Gain Matching		±3		% of FSR
Miscale Error		±30		mV
Midscale Error Matching		±10		mV
Gain Linearity Error		±3		dB
DRIFT (0°C to 70°C)				
Gain Drift		±100		ppm/°C
Midscale Drift		−130		μV/°C
TOTAL HARMONIC DISTORTION + NOISE				
0 dB, 990.5 Hz AD1866N		0.005	0.01	%
AD1866R		0.005	0.01	%
−20 dB, 990.5/Hz AD1866N		0.02		%
AD1866R		0.02		%
−60 dB, 990.5 Hz AD1866N		2.0		%
AD1866R		2.0		%
CHANNEL SEPARATION 1 kHz, 0 dB	108	115		dB
SIGNAL-TO-NOISE RATIO (with A-Weight Filter)		95		dB
D-RANGE (with A-Weight Filter)		90		dB
OUTPUT				
Voltage Output Pins (V_{OL}, V_{OR})				
Output Range (±3%)		±1		V
Output Impedance		0.1		Ω
Load Current		±1		mA
Bias Voltage Pins (V_{BL}, V_{BR})				
Output Range		+2.5		V
Output Impedance		350		Ω
POWER SUPPLY				
Specification, V_L and V_S	4.75	5	5.25	V
Operation, V_L and V_S	3.5		5.25	V
+I, V_L and V_S = 5 V		9	13	mA
POWER DISSIPATION		45	65	mW
TEMPERATURE RANGE				
Operation	−35		85	°C
Storage	−60		100	°C

Specifications subject to change without notice.

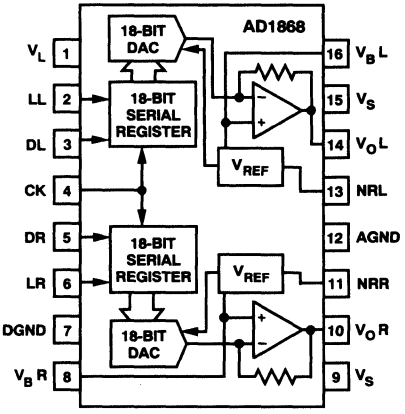
Single Supply Dual 18-Bit Audio DAC

AD1868*

FEATURES
Dual Serial Input, Voltage Output DACs
Single +5 V Supply
0.004% THD+N (typical)
Low Power: 50 mW (typical)
>115 dB Channel Separation (typical)
Operates at 8× Oversampling
16-Pin Plastic DIP or SOIC Package

APPLICATIONS
Portable Compact Disc Players
Portable DAT Players and Recorders
Automotive Compact Disc Players
Automotive DAT Players
Multimedia Workstations

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1868 is a complete dual 18-bit DAC offering excellent performance while requiring a single +5 V power supply. It is fabricated on Analog Devices' ABCMOS wafer fabrication process. The monolithic chip includes CMOS logic elements, bipolar and MOS linear elements, and laser-trimmed thin-film resistor elements. Careful design and layout techniques have resulted in low distortion, low noise, high channel separation, and low power dissipation.

The DACs on the AD1868 chip employ a partially segmented architecture. The first three MSBs of each DAC are segmented into seven elements. The 15 LSBs are produced using standard R-2R techniques. The segments and R-2R resistors are laser-trimmed to provide extremely low total harmonic distortion. The AD1868 requires no deglitcher or trimming circuitry.

Each DAC is equipped with a high performance output amplifier. These amplifiers achieve fast settling and high slew rate, producing ±1 V signals at load currents up to ±1 mA. The buffered output signal range is 1.5 V to 3.5 V. Reference voltages of 2.5 V are provided, eliminating the need for "False Ground" networks.

A versatile digital interface allows the AD1868 to be directly connected to all digital filter chips. Fast CMOS logic elements allow for an input clock rate of up to 13.5 MHz. This allows for operation at 2×, 4×, 8×, or 16× the sampling frequency (where F_S equals 44.1 kHz) for each channel. The digital input pins of the AD1868 are TTL and +5 V CMOS compatible.

The AD1868 operates on +5 V power supplies. The digital supply, V_L, can be separated from the analog supply, V_S, for reduced digital feedthrough. Separate analog and digital ground pins are also provided. In systems employing a single +5 volt power supply, V_L and V_S should be connected together. In battery-operated systems, operation will continue even with reduced supply voltage. Typically, the AD1868 dissipates 50 mW.

The AD1868 is packaged in either a 16-pin plastic DIP or a 16-pin plastic SOIC package. Operation is guaranteed over the temperature range of −35°C to +85°C and over the voltage supply range of 4.75 V to 5.25 V.

PRODUCT HIGHLIGHTS

1. Single-supply operation @ +5 V
2. 50 mW power dissipation (typical)
3. THD+N is 0.004% (typical)
4. Signal-to-Noise Ratio is 97.5 dB (typical)
5. >115 dB channel separation (typical)
6. Compatible with all digital filter chips
7. 16-pin DIP and 16-pin SOIC packages
8. No deglitcher required
9. No external adjustments required

5

*Protected by U.S. Patents Numbers: 3,961,326; 4,141,004; 4,349,811; 4,857,862; and patents pending.

AD1868—SPECIFICATIONS (T_A = +25°C and +5 V supplies unless otherwise noted)

		Min	Typ	Max	Units
RESOLUTION			18		Bits
DIGITAL INPUTS	V_{IH}	2.4			V
	V_{IL}			0.8	V
	I_{IH}, V_{IH} = V_L		1.0		μA
	I_{IL}, V_{IL} = DGND		1.0		μA
Maximum Clock Input Frequency		13.5			MHz
ACCURACY					
Gain Error			±1		% of FSR
Gain Matching			±1		% of FSR
Midscale Error			±15		mV
Midscale Error Matching			±10		mV
Gain Linearity Error			±3		dB
DRIFT (0°C to +70°C)					
Gain Drift			±100		ppm/°C
Midscale Drift			±100		μV/°C
TOTAL HARMONIC DISTORTION + NOISE					
0 dB, 990.5 Hz	AD1868N, R		0.004	0.008	%
	AD1868N-J, R-J		0.004	0.006	%
−20 dB, 990.5 Hz	AD1868N, R		0.020	0.08	%
	AD1868N-J, R-J		0.020	0.08	%
−60 dB, 990.5 Hz	AD1868N, R		2.0	5.0	%
	AD1868N-J, R-J		2.0	5.0	%
CHANNEL SEPARATION 1 kHz, 0 dB		108	>115		dB
SIGNAL-TO-NOISE RATIO (with A-Weight Filter)		95	97.5		dB
D-RANGE (with A-Weight Filter)		86	92		dB
OUTPUT					
Voltage Output Pins (V_OL, V_OR)					
Output Range (±3%)			±1		V
Output Impedance			0.1		Ω
Load Current			±1		mA
Bias Voltage Pins (V_BL, V_BR)					
Output Voltage			+2.5		V
Output Impedance			350		Ω
POWER SUPPLY					
Specification, V_L and V_S		4.75	5	5.25	V
Operation, V_L and V_S		3.5		5.25	V
+I, V_L and V_S = 5 V			10	14	mA
POWER DISSIPATION			50	70	mW
TEMPERATURE RANGE					
Operation		−35		85	°C
Storage		−60		100	°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_L to DGND . . . . . 0 to 6 V
V_S to AGND . . . . . 0 to 6 V
AGND to DGND . . . . . ±0.3 V
Digital Inputs to DGND . . . . . −0.3 to V_L
Soldering . . . . . 300°C, 10 sec

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

Typical Performance of the AD1868

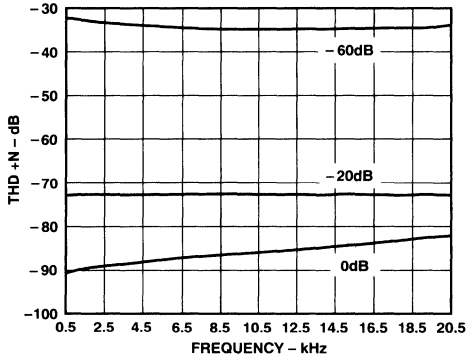


Figure 1. THD+N vs. Frequency

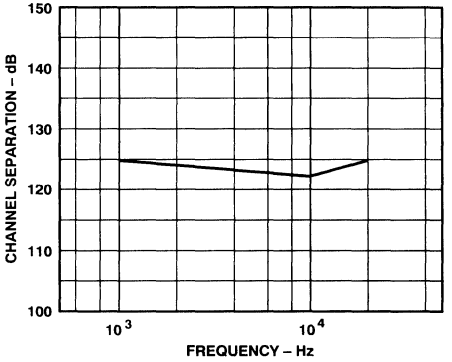


Figure 2. Channel Separation vs. Frequency

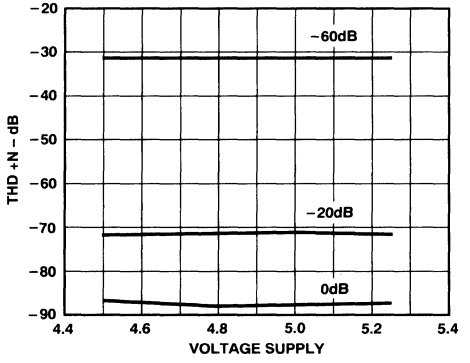


Figure 3. THD+N vs. Supply Voltage

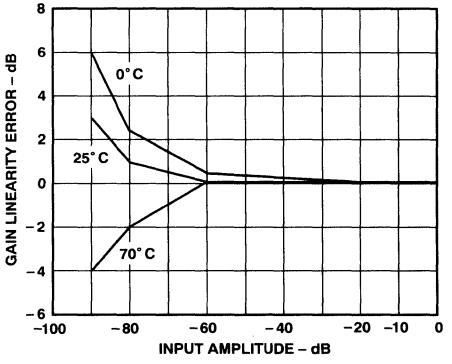


Figure 4. Gain Linearity Error vs. Input Amplitude

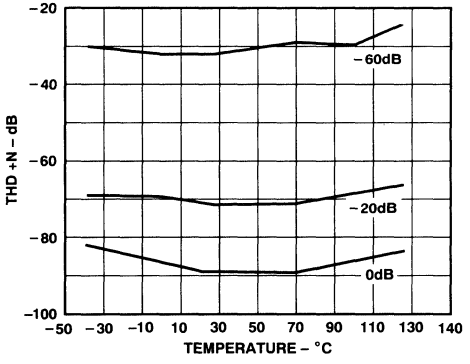


Figure 5. THD+N vs. Temperature

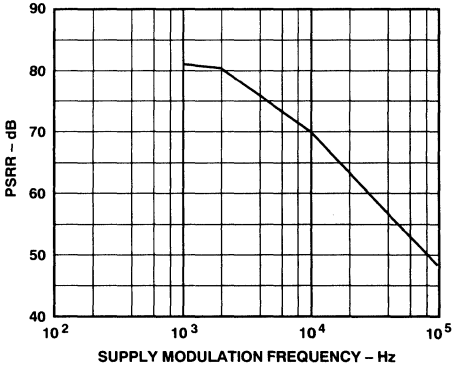
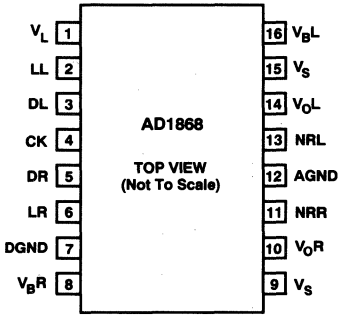


Figure 6. Power Supply Rejection Ratio vs. Frequency

PIN CONFIGURATIONS



PIN DESIGNATIONS

1	V_L	Digital Supply (+5 Volts)
2	LL	Left Channel Latch Enable
3	DL	Left Channel Data Input
4	CK	Clock Input
5	DR	RIGHT Channel Data Input
6	LR	RIGHT Channel Latch Enable
7	DGND	Digital Common
8	V_BR	Right Channel Bias
9	V_S	Analog Supply (+5 Volts)
10	V_OR	Right Channel Output
11	NRR	Right Channel Noise Reduction
12	AGND	Analog Common
13	NRL	Left Channel Noise Reduction
14	V_OL	Left Channel Output
15	V_S	Analog Supply (+5 Volts)
16	V_BL	Left Channel Bias

DEFINITION OF SPECIFICATIONS

Total Harmonic Distortion + Noise

Total harmonic distortion plus noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the amplitudes of the harmonics and noise to the amplitude of the fundamental input frequency. It is usually expressed in percent (%) or decibels (dB).

D-Range Distortion

D-range distortion is the ratio of the amplitude of the signal at an amplitude of −60 dB to the amplitude of the distortion plus noise. In this case, an A-weight filter is used. The value specified for D-range performance is the ratio measured plus 60 dB.

Signal-to-Noise Ratio

The signal-to-noise ratio is defined as the ratio of the amplitude of the output when a full-scale output is present to the amplitude of the output with no signal present. It is expressed in decibels (dB) and measured using an A-weight filter.

Gain Linearity

Gain linearity is a measure of the deviation of the actual output amplitude from the ideal output amplitude. It is determined by measuring the amplitude of the output signal as the amplitude of that output signal is digitally reduced to a lower level. A perfect D/A converter exhibits no difference between the ideal and actual amplitudes. Gain linearity is expressed in decibels (dB).

Midscale Error

Midscale error is the difference between the analog output and the bias when the twos complement input code representing midscale is loaded in the input register. Midscale error is expressed in mV.

FUNCTIONAL DESCRIPTION

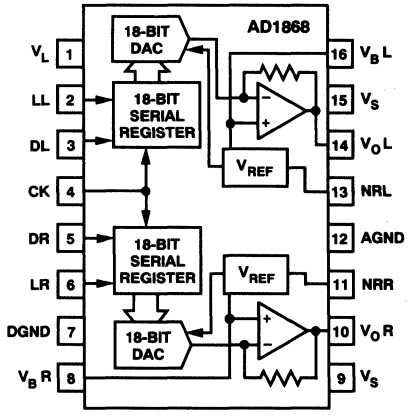
The AD1868 is a complete, voltage output dual 18-bit digital audio DAC which operates with a single +5 volt supply. As shown in the block diagram, each channel contains a voltage reference 18-bit, serial-to-parallel input register, 18-bit input-latch, 18-bit DAC, and an output amplifier.

The voltage reference section provides a reference voltage and a false ground voltage for each channel. The low noise bandgap circuits produce reference voltages that are unaffected by changes in temperature, time, and power supply.

The output amplifier uses both MOS and bipolar devices and incorporates an NPN class-A output stage. It is designed to produce high slew rate, low noise, low distortion, and optimal frequency response.

Each 18-bit DAC uses a combination of segmented decoder and R-2R architecture to achieve good integral and differential linearity. The resistors which form the ladder structure are fabricated with silicon-chromium thin film. Laser-trimming of these resistors further reduces linearity error, resulting in low output distortion.

The input registers are fabricated with CMOS logic gates. These gates allow fast switching speeds and low power consumption, contributing to the fast digital timing, low glitch, and low power dissipation of the AD1868.



AD1868 Functional Block Diagram

ANALOG CIRCUIT CONSIDERATIONS

GROUNDING RECOMMENDATIONS

The AD1868 has two ground pins, designated as AGND (Pin 12) and DGND (Pin 7). The analog ground, AGND, serves as the "high quality" reference ground for analog signals and as a return path for the supply current from the analog portion of the device. The system analog common should be located as close as possible to Pin 12 to minimize any voltage drop which may develop between these two points, although the internal circuit is designed to minimize signal dependence of the analog return current.

The digital ground, DGND, returns ground current from the digital logic portion of the device. This pin should be connected to the digital common node in the system. As shown in Figure 7, the analog and digital grounds should be joined at one point in the system. When these two grounds are remotely connected such as at the power supply ground, care should be taken to minimize the voltage difference between the DGND and AGND pins in order to ensure the specified performance.

POWER SUPPLIES AND DECOUPLING

The AD1868 has three power supply input pins. V_S (Pins 9 and 15) provide the supply voltages which operate the analog portion of the device including the 18-bit DACs, the voltage references, and the output amplifiers. The V_S supplies are designed to operate with a +5 V supply. These pins should be decoupled to analog common using a 0.1 μF capacitor. Good engineeringpractice suggests that the bypass capacitors be placed as close as possible to the package pins. This minimizes the inherent inductive effects of printed circuit board traces.

V_L (Pin 1) operates the digital portions of the chip including the input shift registers and the input latching circuitry. V_L is also designed to operate with a +5 V supply. This pin should be bypassed to digital common using a 0.1 μF capacitor, again placed as close as possible to the package pin. Figure 7 illustrates the correct connection of the digital and analog supply bypass capacitors.

An important feature of the AD1868 audio DAC is its ability to operate at reduced power supply voltages. This feature is very important in portable battery-operated systems. As the batteries discharge, the supply voltage drops. Unlike any other audio DAC, the AD1868 can continue to function at supply voltages as low as 3.5 V. Because of its unique design, the power requirements of the AD1868 diminish as the battery voltage drops, further extending the operating time of the system.

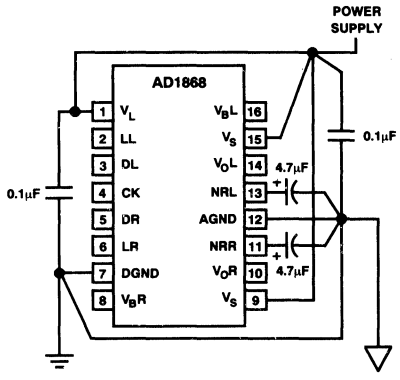


Figure 7. Recommended Circuit Schematic

NOISE REDUCTION CAPACITORS

The AD1868 has two noise-reduction pins designated as NRL (Pin 13) and NRR (Pin 11). It is recommended that external noise-reduction capacitors be connected from these pins to AGND to reduce the output noise contributed by the voltage reference circuitry. As shown in Figure 7, each of these pins should be bypassed to AGND with a 4.7 μF or larger capacitor. The connections between the capacitors, package pins and AGND should be as short as possible to achieve the lowest noise.

USING V_BL AND V_BR

The AD1868 has two bias voltage reference pins, designated as V_BR (Pin 8) and V_BL (Pin 16). These pins supply a dc reference voltage equal to the center of the output voltage swing. These bias voltages replace "False Ground" networks previously required in single-supply audio systems. At the same time, they allow dc-coupled systems, improving audio performance.

Figure 8a illustrates the traditional approach used to generate False Ground voltages in single-supply audio systems. This circuit requires additional power and circuit board space.

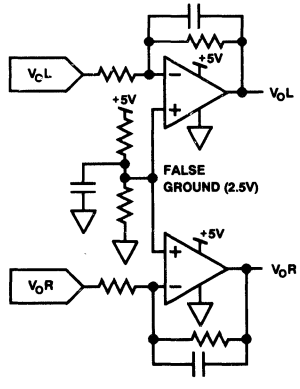


Figure 8a. Schematic Using False Ground

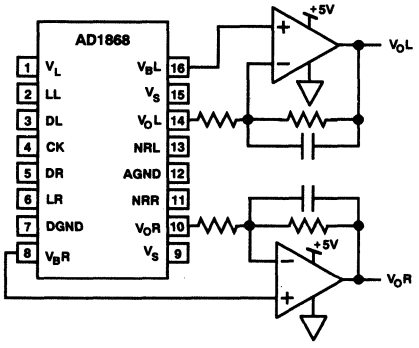


Figure 8b. Circuitry Using Voltage Biases

The AD1868 eliminates the need for "False Ground" circuitry. V_BR and V_BL generate the required bias voltages previously generated by the "False Ground." As shown in Figure 8b, V_BR and V_BL may be used as the reference point in each output channel. This permits a dc-coupled output signal path. This eliminates ac-coupling capacitors and improves low frequency performance. It should be noted that these bias outputs have relatively high output impedance and will not drive output currents larger than 100 μA without degrading the specified performance.

DISTORTION PERFORMANCE AND TESTING

The THD+N figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. Therefore, the THD+N specification provides a direct method to classify and choose an audio DAC for a desired level of performance.

Figure 1 illustrates the typical THD+N versus frequency performance of the AD1868. It is evident that the THD+N performance of the AD1868 remains stable at all three levels through a wide range of frequencies. A load impedance of at least 2 kΩ is recommended for best THD+N performance.

Analog Devices tests and grades all AD1868s on the basis of THD+N performance. During the distortion test, a high speed digital pattern generator transmits digital data to each channel of the device under test. Eighteen-bit data is latched into the DAC at 352.8 kHz ($8\times F_S$). The test waveform is a 990.5 Hz sine wave with 0 dB, −20 dB, and −60 dB amplitudes. A 4096-point FFT calculates total harmonic distortion + noise, signal-to-noise ratio, and D-range. No deglitchers or external adjustments are used.

DIGITAL CIRCUIT CONSIDERATIONS

INPUT DATA

The AD1868 digital input port employs five signals: Data Left (DL), Data Right (DR), Latch Left (LL), Latch Right (LR) and Clock (CLK). DL and DR are the serial inputs for the left and right DACs, respectively. Input data bits are clocked into the input register on the rising edge of CLK. The falling edges of LL and LR cause the last 18 bits which were clocked into the serial registers to be shifted into the DACs, thereby updating the respective DAC outputs. For systems using only a single latch signal, LL and LR may be connected together. For systems using only one DATA signal, DR and DL may be connected together. Data is transmitted to the AD1868 in a bit stream composed of 18-bit words with a serial, twos complement, MSB first format. Left and right channels share the Clock (CLK) signal.

Figure 9 illustrates the general signal requirements for data transfer for the AD1868.

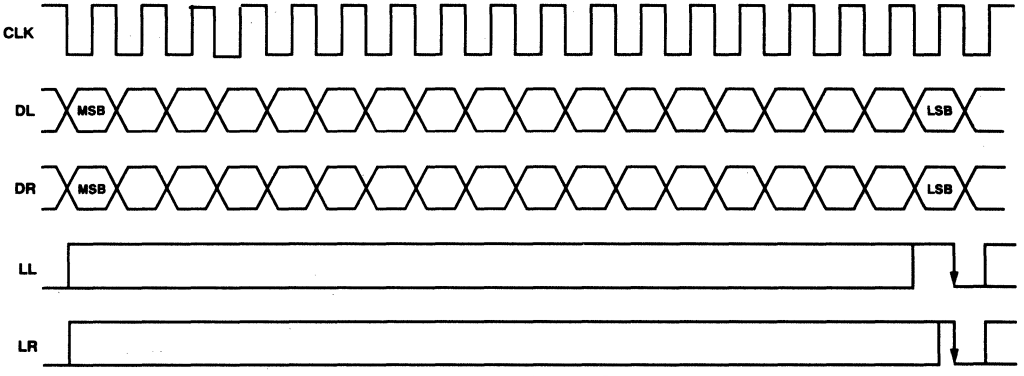


Figure 9. AD1868 Control Signals

TIMING

Figure 10 illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished properly. The input pins of the AD1868 are TTL and 5 V CMOS compatible.

The maximum clock rate of the AD1868 is specified to be at least 13.5 MHz. This clock rate allows data transfer rates of 2×, 4×, 8×, and 16× F_S (where F_S equals 44.1 kHz). The applications section of this data sheet contains additional guidelines for using the AD1868.

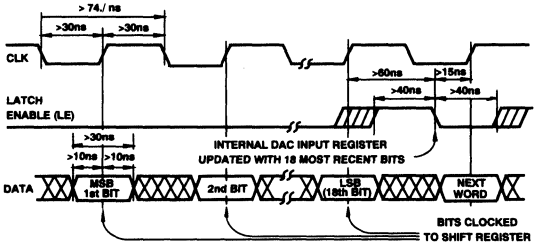


Figure 10. AD1868 Input Signal Timing

APPLICATIONS OF THE AD1868

The AD1868 is a high performance audio DAC specifically designed for portable and automotive digital audio applications. These market segments have technical requirements fundamentally different than those found in the high end or home-use market segments. Portable equipment must rely on components which require low amounts of power to offer reasonable playing times. Also, battery voltages drop as the end of the discharge cycle is approached. The AD1868's ability to operate from a single +5 V supply makes it a good choice for battery-operated gear. As the battery voltage drops, the power dissipation of the AD1868 drops. This extends the usable battery life. Finally, as the battery supply voltage drops, the bias voltages and signal swings also drop, preventing signal clipping and abrupt degradation of distortion. Figure 3 illustrates that THD+N performance of the AD1868 remains constant through a wide range of supply voltages.

Automotive equipment rely on components which are able to consistently perform in a wide range of temperatures. In addition, due to the limited space available in automotive applications, small size is essential. The AD1868 is able to satisfy both of these requirements. The device has guaranteed operation between −35°C and +85°C, and the 16-pin DIP or 16-pin SOIC package is particularly attractive where overall size is important.

Since the AD1868 provides dc bias voltages, the entire signal chain can be dc-coupled. This eliminate ac-coupling capacitors from the signal path, improving low frequency performance and lowering system cost and size.

In summary, the AD1868 is an excellent choice for battery-operated portable or automotive digital audio systems. In the following sections, some examples of high performance audio applications featuring the AD1868 are described.

AD1868 with Sony CXD2550P Digital Filter

Figure 11 illustrates an 18-bit CD player design incorporating an AD1868 DAC, a Sony CXD2550P digital filter and 2-pole antialias filters. This high performance, single-supply design operates at 8× F_S and is suitable for portable and automotive applications. In this design, the CXD2550P filter transmits left and right channel digital data to the AD1868. The left and right latch signals, LL and LR, are both provided by the word clock signal (LRCKO) of the digital filter. The digital data is converted to low distortion output voltages by the output amplifiers on the AD1868. Also, no deglitching circuitry or external adjustments are required. Bypass capacitors, noise-reduction capacitors and the antialias filter details are omitted for clarity.

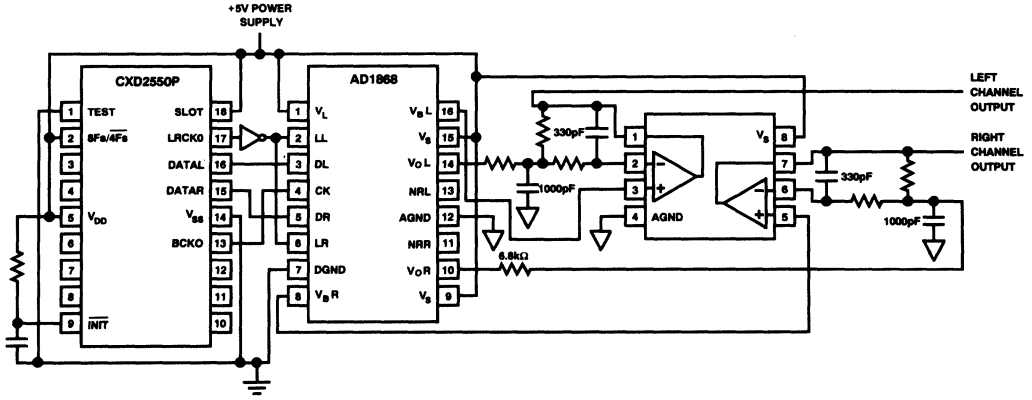


Figure 11. AD1868 with Sony CXD2550P Digital Filter

ADDITIONAL APPLICATIONS

In addition to CD player designs, the AD1868 is suitable for similar applications such as DAT, portable musical instruments, Laptop and Notebook personal computers, and PC audio I/O boards. The circuit techniques illustrated are directly applicable in those applications.

Figures 12, 13, and 14 show connection diagrams for the AD1868 with popular digital filter chips from NPC and Yamaha. Each application operates at 8× F_S operation. Please refer to the appropriate sections of this data sheet for additional information.

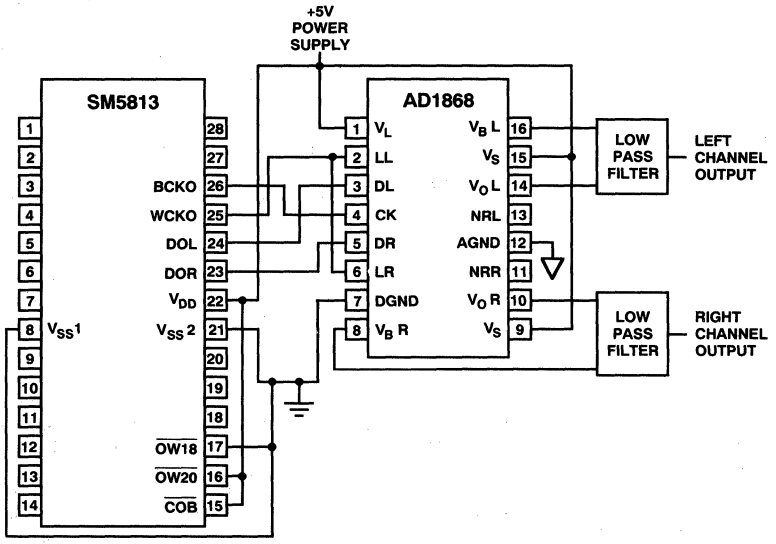


Figure 12. AD1868 with NPC SM5813 Digital Filter

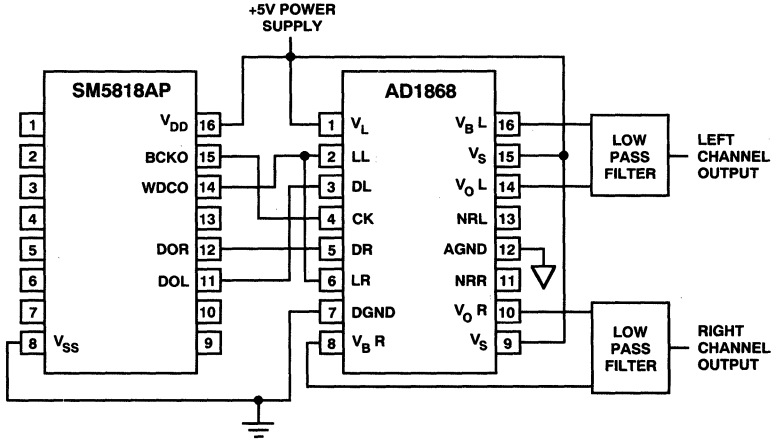


Figure 13. AD1868 with NPC SM5818AP Digital Filter

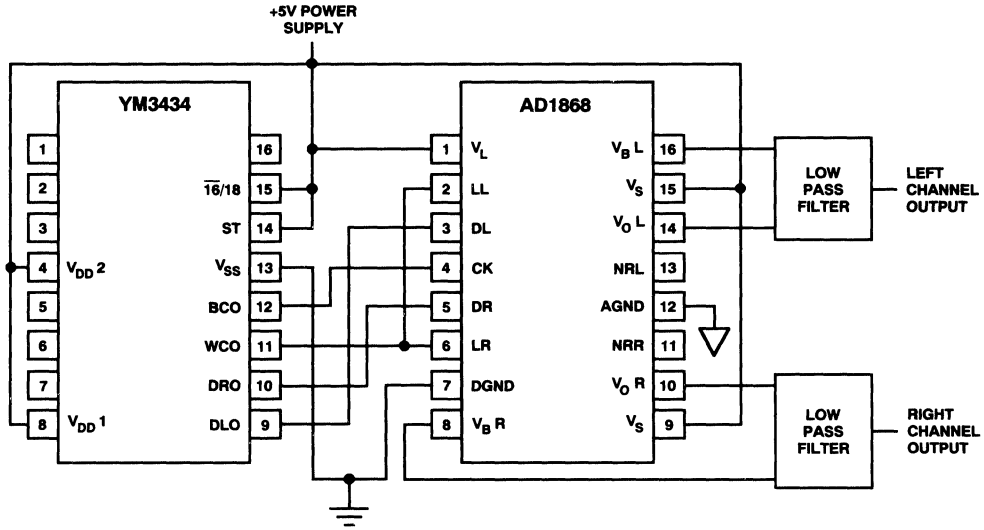


Figure 14. AD1868 with Yamaha YM3434 Digital Filter

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ORDERING GUIDE

Model	THD+N @ F_S	SNR	Package Option*
AD1868N	0.008%	95 dB	N-16
AD1868R	0.008%	95 dB	R-16
AD1868N-J	0.006%	95 dB	N-16
AD1868R-J	0.006%	95 dB	R-16

*N = Plastic DIP; R = SOIC. For outline information see Package Information section.

Video D/A Converters
Contents

Selection Guide
Video Digital-to-Analog Converters

Model	Clock Rate MHZ	D/A Converter Organization	RAM (Color Palette) Size	Overlays	Page	Comments
ADV471	35, 50, 66, 80	Triple 6-Bit	256 × 18	15 × 18	6-19	ADV478 Pin-Compatible
ADV476	35, 40, 50, 66, 80, 100	Triple 6-Bit	256 × 18		6-9	Triple 6-Bit RAM-DAC
ADV7141	35, 50, 66	Triple 6-Bit	256 × 18		6-49	CEG – Effective 24-Bit True Color
ADV7146	35, 50, 66	Triple 6-Bit	256 × 18		6-49	CEG – Effective 24-Bit True Color
ADV453	40	Triple 8-Bit	256 × 24	3 × 24	6-3	Triple 8-Bit RAM-DAC
ADV478	35, 50, 66, 80, 100	Triple 8-Bit	245 × 24	15 × 24	6-19	Triple 8-Bit RAM-DAC
ADV7148	35, 50, 66	Triple 8-Bit	256 × 24		6-49	CEG – Effective 24-Bit True Color
ADV7120	35, 50, 80	Triple 8-Bit			6-31	True Color DAC
ADV7121	35, 50, 80	Triple 10-Bit			6-37	True Color DAC
ADV7122	35, 50, 80	Triple 10-Bit			6-37	True Color DAC

CMOS 66 MHz Monolithic 256×24 Color Palette RAM-DAC

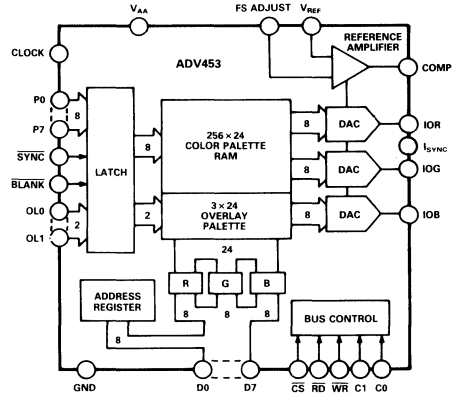
ADV453

FEATURES
66MHz Pipelined Operation
Triple 8-Bit D/A Converters
256×24 Color Palette RAM
3×24 Overlay Registers
RS-343A/RS-170 Compatible Outputs
+5V CMOS Monolithic Construction
40-Pin DIP or Small 44-Pin PLCC Package
Power Dissipation: 1000mW

APPLICATIONS
High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Desktop Publishing

AVAILABLE CLOCK RATES
66MHz
40MHz

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADV453 (ADV®) is a complete analog video output RAM-DAC on a single monolithic chip. It is specifically designed for high resolution color graphics systems. The part contains a 256×24 color lookup table, a 3×24 overlay palette as well as triple 8-bit video D/A converters. The ADV453 is capable of simultaneously displaying up to 259 colors, 256 from the lookup table and three from the overlay registers, out of a total color palette of 16.8 million addressable colors.

The three overlay registers allow for the implementation of overlaying cursors, pull down menus and grids. There is an independent, asynchronous MPU bus which allows access to the color lookup table without affecting the input of video data via the pixel port. The ADV453 is capable of generating RGB video output signals which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

The ADV453 is fabricated in a +5V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation. The part is packaged in both a 0.6", 40-pin DIP and a 44-pin plastic leaded (J-lead) chip carrier, PLCC.

PRODUCT HIGHLIGHTS

1. Fast video refresh rate, 66MHz.
2. Compatible with a wide variety of high resolution color graphics systems including VGA* and Macintosh II**.
3. Three overlay registers allow for implementation of overlaying cursors, pull down menus and grids.
4. Guaranteed monotonic. Integral and differential nonlinearities guaranteed to be a maximum of ±1LSB.
5. Low glitch energy, 50pV secs.

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ADV is a registered trademark of Analog Devices, Inc.
*VGA is a trademark of International Business Machines Corp.
**Macintosh II is a registered trademark of Apple Computer Inc.

ADV453—SPECIFICATIONS (V_{AA} = +5V ±5%, V_{REF} = +1.235V, R_{SET} = 280Ω. I_{SYNC} connected to IOG. All specifications T_{min} to T_{max}[1] unless otherwise noted.)

Parameter	All Versions	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution (Each DAC)	8	Bits	
Accuracy (Each DAC)			
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Gray Scale Error	±5%	Gray Scale max	
Coding		Binary	
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	± 1	μA max	V_{IN} = 0.4V or 2.4V
Input Capacitance, C_{IN}	10	pF typ	
DIGITAL OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 400μA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 3.2mA
Floating State Leakage Current	20	μA max	
Floating State Output Capacitance	20	pF typ	
ANALOG OUTPUTS			
Gray Scale Current Range	15	mA min	
	22	mA max	
Output Current			
White Level Relative to Blank	17.69	mA min	Typically 19.05mA
	20.40	mA max	
White Level Relative to Black	16.74	mA min	Typically 17.62mA
	18.50	mA max	
Black Level Relative to Blank	0.95	mA min	Typically 1.44mA
	1.90	mA max	
Blank Level on IOR, IOB	0	μA min	Typically 5μA
	50	μA max	
Blank Level on IOG	6.29	mA min	Typically 7.62mA
	8.96	mA max	
Sync Level on IOG	0	μA min	Typically 5μA
	50	μA max	
LSB Size	69.1	μA typ	
DAC to DAC Matching	5	% max	Typically 2%
Output Compliance, V_{OC}	−1	V min	
	+1.4	V max	
Output Impedance, R_{OUT}	10	kΩ typ	
Output Capacitance, C_{OUT}	30	pF typ	I_{OUT} = 0mA
VOLTAGE REFERENCE			
Voltage Reference Range, V_{REF}	1.14/1.26	V min/V max	
Input Current, I_{VREF}	−5	mA typ	
POWER SUPPLY			
Supply Voltage, V_{AA}	4.75/5.25	V min/V max	
Supply Current, I_{AA}	275	mA max	Typically 220mA, 66MHz Parts
	250	mA max	Typically 190mA, 40MHz Parts
Power Supply Rejection Ratio	0.5	%/% max	Typically 0.12%/%, f = 1kHz, COMP = 0.1μF
Power Dissipation	1375	mW max	Typically 1000mW, 66MHz Parts
	1250	mW max	Typically 900mW, 40MHz Parts
DYNAMIC PERFORMANCE			
Clock and Data Feedthrough[2,3]	−30	dB typ	
Glitch Impulse[2,3]	50	pV secs typ	
DAC to DAC Crosstalk	−23	dB typ	

NOTE

[1]Temperature Range (T_{min} to T_{max}); 0 to +70°C

[2]TTL input values are 0 to 3 volts, with input rise/fall times ≤3ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10pF, 37.5Ω. D0–D7 output load ≤50pF. See timing notes in Figure 2.

[3]Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1kΩ resistor to ground and are driven by 74HC logic. Glitch impulse includes clock and data feedthrough, −3dB test bandwidth = 2 × clock rate.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{AA} = +5V ±5%, V_{REF} = +1.235V, R_{SET} = 280Ω. I_{SYNC} connected to IOG. All Specifications T_{min} to T_{max}[2]).

Parameter	66MHz Version	40MHz Version	Units	Conditions/Comments
f_{max}	66	40	MHz max	Clock Rate
t_1	35	35	ns min	$\overline{CS}$, C0, C1 Setup Time
t_2	35	35	ns min	$\overline{CS}$, C0, C1 Hold Time
t_3	25	25	ns min	$\overline{RD}$, $\overline{WR}$ High Time
t_4	10	10	ns min	$\overline{RD}$ Asserted to Data Bus Driven
t_5	100	100	ns max	$\overline{RD}$ Asserted to Data Valid
t_6	15	15	ns max	$\overline{RD}$ Negated to Data Bus Three Stated
t_7	50	50	ns min	$\overline{WR}$ Low Time
t_8	35	35	ns min	Write Data Setup Time
t_9	0	0	ns min	Write Data Hold Time
t_{10}	5	7	ns min	Pixel & Control Setup Time
t_{11}	2	3	ns min	Pixel & Control Hold Time
t_{12}	15	25	ns min	Clock Cycle Time
t_{13}	5	7	ns min	Clock Pulse Width High Time
t_{14}	5	7	ns min	Clock Pulse Width Low Time
t_{15}	20	20	ns typ	Analog Output Delay
	30	30	ns max	
t_{16}	3	3	ns typ	Analog Output Rise/Fall Time
t_{17}[3]	25	25	ns typ	Analog Output Settling Time
t_{PD}	$2\times t_{12}$	$2\times t_{12}$	ns max	Pipeline Delay
t_{SK}	1	1	ns typ	Analog Output Skew
	2	2	ns max	

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10pF, 37.5Ω. D0–D7 output load ≤50pF. See timing notes in Figure 2.
[2]Temperature Range (T_{min} to T_{max}); 0 to +70°C.
[3]Settling time does not include clock and data feedthrough. For this test, the digital inputs have a 1kΩ resistor to ground and are driven by HC logic.
Specifications subject to change without notice.

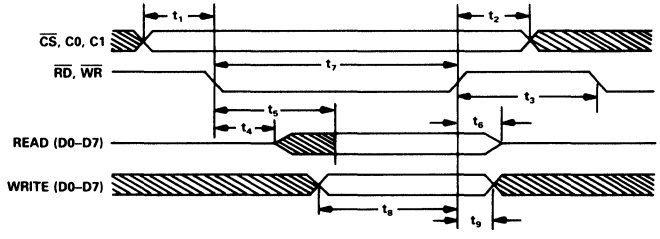
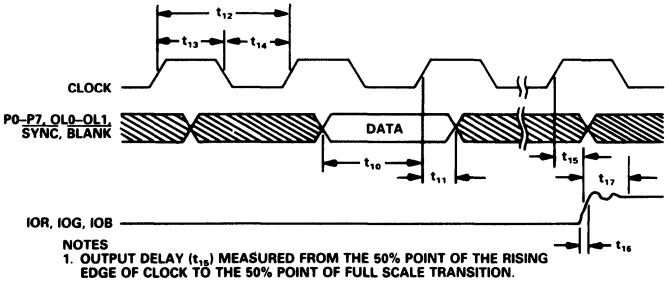


Figure 1. MPU Read/Write Timing



NOTES
1. OUTPUT DELAY (t_{15}) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL SCALE TRANSITION.
2. SETTLING TIME(t_{17}) MEASURED FROM THE 50% POINT OF FULL SCALE TRANSITION TO THE OUTPUT REMAINING WITHIN ±1LSB.
3. OUTPUT RISE/FALL TIME (t_{16}) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL SCALE TRANSITION.

Figure 2. Video Input/Output Timing

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}	4.75	5.00	5.25	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

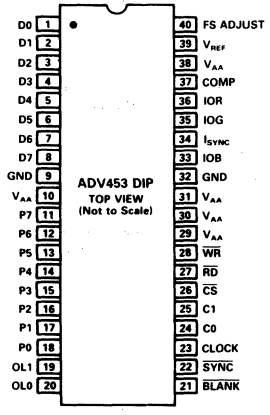
ABSOLUTE MAXIMUM RATINGS*

V_{AA} to GND . . . . . +7V
Voltage on Any Digital Pin . . . . . GND −0.5V to V_{AA} +0.5V
Ambient Operating Temperature (T_A) . . . . . 0 to +70°C
Storage Temperature (T_S) . . . . . −65°C to +150°C
Junction Temperature (T_J) . . . . . +175°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Vapor Phase Soldering (1 minute) . . . . . +220°C
IOR, IOB, IOG to GND[1] . . . . . 0V to V_{AA}

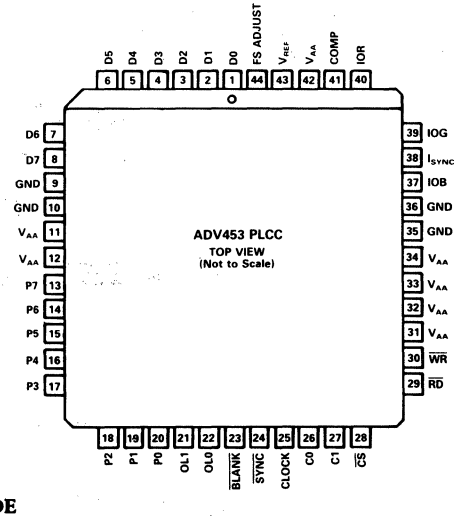
NOTES
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[1]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

PIN CONFIGURATIONS

DIP



PLCC



ORDERING GUIDE

Model	Temperature Range	Speed	Package Option*
ADV453KN66	0°C to +70°C	66MHz	N-40A
ADV453KN40	0°C to +70°C	40MHz	N-40A
ADV453KP66	0°C to +70°C	66MHz	P-44A
ADV453KP40	0°C to +70°C	40MHz	P-44A

NOTES
*N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{\text{BLANK}}$	Composite blank control input (TTL compatible). A logic zero on this control input drives the analog outputs to the blanking level, as shown in Table V. The $\overline{\text{BLANK}}$ signal is latched on the rising edge of CLOCK. While $\overline{\text{BLANK}}$ is at logical zero, the pixel and overlay inputs are ignored.
$\overline{\text{SYNC}}$	Composite sync control input (TTL compatible). A logical zero on the $\overline{\text{SYNC}}$ input switches off a 40 IRE current source on the I_{SYNC} output (see Figure 5). $\overline{\text{SYNC}}$ does not override any other control or data input, as shown in Table V; therefore, it should only be asserted during the blanking interval. $\overline{\text{SYNC}}$ is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7 and OL0–OL1 data inputs as well as the $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ control inputs. It is typically the pixel clock rate of the video system. CLOCK should be driven by a dedicated TTL buffer.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. P0–P7 pixel select inputs are latched on the rising edge of CLOCK. P0 is the LSB. Unused pixel select inputs should be connected to GND.
OL0–OL1	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information (see Table IV), i.e., the 256×24 color palette or the 3×24 overlay palette. When accessing the overlay palette, the P0–P7 inputs are ignored. OL0–OL1 are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75Ω coaxial cable, as shown in Figure 4a. All three current outputs should have similar output loads whether or not they are all being used.
I_{SYNC}	Sync current output. This high impedance current source can be directly connected to the IOG output (see Figure 3). This allows sync information to be encoded onto the green channel. I_{SYNC} does not output any current while $\overline{\text{SYNC}}$ is at logical zero. The amount of current output at I_{SYNC} while $\overline{\text{SYNC}}$ is at logical one is given by: I_{SYNC} (mA) = 1,728 * V_{REF}(V)/ R_{SET} (Ω). If sync information is not required on the green channel, I_{SYNC} should be connected to GND.
FS ADJUST	Full scale adjust control. A resistor (R_{SET}) connected between this pin and GND (see Figure 6) controls the magnitude of the full scale video signal. Note that the IRE relationships in Figure 5 are maintained, regardless of the full scale output current. The relationship between R_{SET} and the full scale output current on IOG (assuming I_{SYNC} is connected to IOG) is given by: IOG (mA) = (K + 326 + 1,728) * V_{REF}(V)/R_{SET} (Ω) The relationship between R_{SET} and the full scale output current on IOR and IOB is given by: IOR, IOB (mA) = (K + 326)* V_{REF}(V)/R_{SET}(Ω) where K = 3,993
COMP	Compensation pin. This is a compensation pin for the internal reference amplifier. A 0.1μF ceramic capacitor must be connected between COMP and V_{AA} (Figure 6).
V_{REF}	Voltage reference input. An external 1.235V voltage reference must be connected to this pin. The use of an external resistor divider network is not recommended. A 0.1μF decoupling ceramic capacitor should be connected between V_{REF} and V_{AA} (Figure 6.)
V_{AA}	Analog power supply (5V±5%). All V_{AA} pins on the ADV453 must be connected.
GND	Analog ground. All GND pins must be connected.
$\overline{\text{CS}}$	Chip select control input (TTL compatible). $\overline{\text{CS}}$ must be at logical zero to enable the reading and writing of data to and from the device. The IOR, IOG and IOB outputs are forced to the black level while $\overline{\text{CS}}$ is at logical zero. Note that the ADV453 will not operate properly if $\overline{\text{CS}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are simultaneously at logical zero.
$\overline{\text{WR}}$	Write control input (TTL compatible). $\overline{\text{CS}}$ and $\overline{\text{WR}}$ must both be at logical zero when writing data to the device. D0–D7 data is latched on the rising edge of $\overline{\text{WR}}$ or $\overline{\text{CS}}$. See Figure 1.
$\overline{\text{RD}}$	Read control input (TTL compatible). $\overline{\text{CS}}$ and $\overline{\text{RD}}$ must both be at logical zero when reading data from the device. See Figure 1.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being carried out, i.e., address register, color palette RAM or overlay registers read or write operations. See Tables I, II, III.
D0–D7	Data bus (TTL compatible). Data is transferred to and from the address register, the color palette RAM and the overlay registers over this 8-bit bidirectional data bus. D0 is the least significant bit.

CMOS Monolithic 256×18 Color Palette RAM-DAC

ADV476

FEATURES
Personal System/2* and VGA* Compatible
Plug-in Replacement for INMOS 171/176
66MHz Pipelined Operation
Three 6-Bit D/A Converters
256×18 Color Palette RAM
RS-343A/RS-170 Compatible Outputs
Blank on All Three Channels
Standard MPU Interface
Asynchronous Access to All Internal Registers
+5V CMOS Monolithic Construction
Low Power Dissipation
Standard 28-Pin, 0.6" DIP and 44-Pin PLCC

APPLICATIONS
High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Desktop Publishing

AVAILABLE CLOCK RATES
66MHz
50MHz
35MHz

GENERAL DESCRIPTION

The ADV476 (ADV®) is a pin compatible and software compatible RAM-DAC designed specifically for VGA and Personal System/2 color graphics.

The ADV476 is a complete analog output RAM-DAC on a single monolithic chip. The part contains a 256×18 color lookup table, a pixel mask register as well as a triple 6-bit video D/A converter. The ADV476 is capable of simultaneously displaying up to 256 colors, from a total color palette of 262,144 addressable colors.

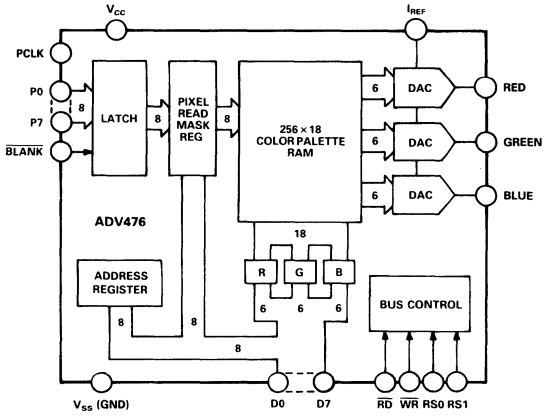
The on-chip asynchronous MPU bus allows access to the color lookup table without affecting the input video data via the pixel port. The pixel read mask register provides a convenient way of altering the displayed colors without updating the color lookup table. The ADV476 is capable of generating RGB video output signals which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

The ADV476 is fabricated in a +5V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation and small board area. The part is packaged in a 0.6", 28-pin DIP and a 44-pin PLCC.

***Personal System/2 and VGA are trademarks of International Business Machines Corp.**

ADV is a registered trademark of Analog Devices, Inc.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. Standard video refresh rates, 35MHz, 50MHz and 66MHz.
2. Fully compatible with VGA and Personal System/2 color graphics.
3. Guaranteed monotonic. Integral and differential linearity guaranteed to be a maximum of ±1LSB.
4. Low glitch energy, 75pV secs.

6

ADV476—SPECIFICATIONS (V_{CC} = +5V ±10%, I_{REF} = 8.88mA. All Specifications T_{min} to T_{max}[1] unless otherwise noted.)

Parameter	All Versions	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution (Each DAC)	6	Bits	
Accuracy (Each DAC)			
Integral Nonlinearity	±0.5	LSB max	Guaranteed Monotonic
Full Scale Error	±5	% max	Full Scale = $2.15 \times I_{REF} \times R_L$, I_{REF} = 8.39mA
Blank Level	±0.5	LSB max	$\overline{BLANK}$ = Logic Low
Offset Error	±0.5	LSB max	$\overline{BLANK}$ = Logic High
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±10	µA max	V_{CC} = 5.5V, V_{IN} = 0.4V to V_{CC}
Input Current ($\overline{RD}$ Input Only)	±100	µA max	V_{CC} = 5.5V, V_{IN} = 0.4V to V_{CC}
Input Capacitance, C_{IN}	7	pF typ	
DIGITAL OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 500µA, V_{CC} = 4.5V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 5.0mA, V_{CC} = 4.5V
Floating-State Leakage Current	±50	µA max	V_{CC} = 5.5V, 0.4V < V_{IN} < V_{CC}
Floating-State Output Capacitance	7	pF typ	
ANALOG OUTPUTS			
Max Output Voltage	1.5	V min	IO ≤ 10mA, IO = $2.15 \times I_{REF}$
Max Output Current	21	mA min	VO ≤ 1V
DAC to DAC Matching[2]	±2.5	% max	
Analog Output Capacitance	10	pF typ	$\overline{BLANK}$ = Logic Low
CURRENT REFERENCE			
Input Current (I_{REF}) Range	−3/−10	mA min/mA max	
Voltage at I_{REF}	V_{CC} −3/V_{CC}	V min/V max	I_{REF} = 8.88mA
POWER SUPPLY			
Supply Voltage, V_{CC}	4.5/5.5	V min/V max	
Supply Current, I_{CC}	220	mA max	f_{MAX} = 66MHz, IO = $2.15 \times I_{REF}$, D0 to D7 Unloaded
Power Supply Rejection Ratio	6	%/V	4.5 < V_{CC} < 5.5V, IO = $2.15 \times I_{REF}$, R_L = 37.5Ω, C_L = 30pF, I_{REF} = 8.88mA
DYNAMIC PERFORMANCE			
Clock and Data Feedthrough[3, 4]	−35	dB typ	
Glitch Impulse[3, 4]	75	pV secs typ	

NOTES

[1]Temperature range (T_{min} to T_{max}); 0 to +70°C.

[2]Relative to the midpoint of the distribution of the three DACs measured at full scale.

[3]TTL input values are 0 to 3 volts, with input rise/fall times ≤3ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10pF, 37.5Ω. D0–D7 output load ≤50pF. See timing notes in Figure 2.

[4]Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1kΩ resistor to ground and are driven by 74HC logic. Glitch impulse includes clock and data feedthrough, −3dB test bandwidth = 2×clock rate.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{CC} = +5V±10%. All Specifications T_{min} to T_{max}[2])

Parameter	66MHz Version	50MHz Version	35MHz Version	Units	Conditions/Comments
f_{max}	66	50	35	MHz	Clock Rate
t_1	10	10	15	ns min	RS0, RS1 Setup Time
t_2	10	10	15	ns min	RS0, RS1 Hold Time
t_3	5	5	5	ns min	$\overline{RD}$ Asserted to Data Bus Driven
t_4	40	40	40	ns max	$\overline{RD}$ Asserted to Data Valid
t_5	20	20	20	ns max	$\overline{RD}$ Negated to Data Bus 3-Stated
t_6	10	10	15	ns min	Write Data Setup Time
t_7	10	10	15	ns min	Write Data Hold Time
t_8	50	50	50	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width Low
t_9	$4\times t_{12}$	$4\times t_{12}$	$4\times t_{12}$	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width High
t_{10}	3	3	4	ns min	Pixel & Control Setup Time
t_{11}	3	3	4	ns min	Pixel & Control Hold Time
t_{12}	15.3	20	28	ns min	Clock Cycle Time
t_{13}	5	6	7	ns min	Clock Pulse Width High Time
t_{14}	5	6	9	ns min	Clock Pulse Width Low Time
t_{15}	30	30	30	ns max	Analog Output Delay
	5	5	5	ns min	
t_{16}	6	8	8	ns max	Analog Output Rise/Fall Time
t_{17}[3]	15.3	20	25	ns typ	Analog Output Settling Time
t_{18}	2	2	2	ns min	Analog Output Skew
t_{PD}	4	4	4	clocks	Pipeline Delay

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load≤10 pF, 37.5Ω. D0–D7 output load≤50 pF. See timing notes in Figure 2.
[2]Temperature Range (T_{min} to T_{max}); 0 to +70°C
[3]Settling time does not include clock and data feedthrough. For this test, the digital inputs have a 1kΩ resistor to ground and are driven by 74HC logic.
Specifications subject to change without notice.

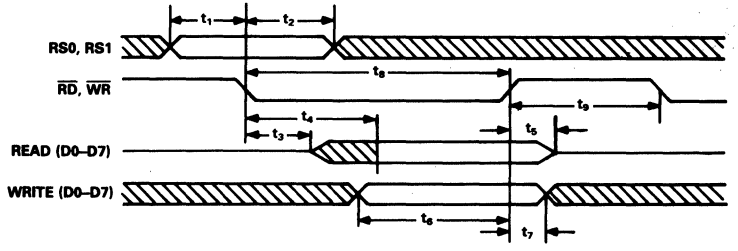
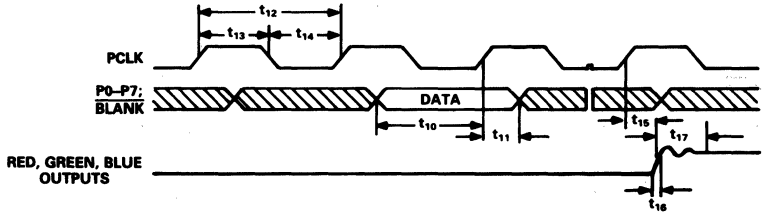


Figure 1. MPU Read/Write Timing



NOTES
1. OUTPUT DELAY (t_{15}) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF THE PCLK TO THE 50% POINT OF FULL SCALE TRANSITION.
2. SETTLING TIME (t_{17}) MEASURED FROM THE 50% POINT OF FULL SCALE TRANSITION TO THE OUTPUT REMAINING WITHIN ±1/4 LSB.
3. OUTPUT RISE/FALL TIME (t_{16}) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL SCALE TRANSITION.

Figure 2. Video Input/Output Timing

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to GND . . . . . +7V
Voltage on any Digital Pin . . . . . GND−0.5V to V_{CC}+0.5V
Ambient Operating Temperature (T_A) . . . . . −55°C to +125°C
Storage Temperature (T_S) . . . . . −65°C to +150°C
Junction Temperature (T_J) . . . . . +175°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Vapor Phase Soldering (1 minute) . . . . . +220°C
Red, Green, Blue to GND[1] . . . . . 0V to V_{CC}

NOTES
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[1]Analog output short circuit to any power supply or common can be of an indefinite duration.

ORDERING GUIDE[1, 2]

Model	Speed	Package Type	Package Option[3]
ADV476KN35	35MHz	28-Pin DIP	N-28
ADV476KN50	50MHz	28-Pin DIP	N-28
ADV476KN66	66MHz	28-Pin DIP	N-28
ADV476KP35	35MHz	44-Pin PLCC	P-44A
ADV476KP50	50MHz	44-Pin PLCC	P-44A
ADV476KP66	66MHz	44-Pin PLCC	P-44A

NOTES
[1]All devices are specified for 0 to +70°C operation.
[2]Devices are packaged in 0.6" 28-pin plastic DIPs (N-28), and 44-pin J-leaded PLCC (P-44A).
[3]N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

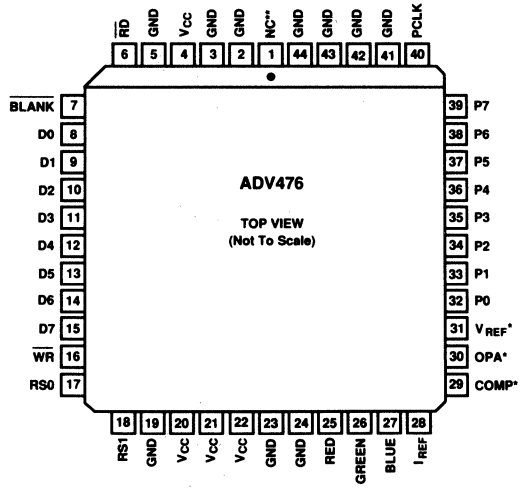
RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{CC}	4.5	5.00	5.5	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Reference Current	I_{REF}	−3		−10	mA

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

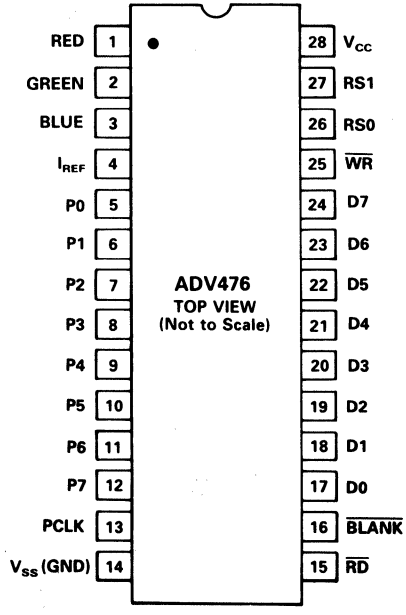
PLCC PIN CONFIGURATION



*V_{REF} MUST BE TERMINATED THROUGH A 0.1μF CERAMIC CAPACITOR TO V_{CC}. OPA IS LEFT UNCONNECTED; COMP IS CONNECTED TO I_{REF} (SEE FIGURE 8).
**NC = NO CONNECT

The above pins allow the ADV476KP (44-Pin PLCC) to be alternatively driven by a voltage reference. If it is desired to use a voltage reference configuration instead of the current reference configuration described in this data sheet, the above listed pins must be connected as described in Figure 6 of the ADV478/ADV471 data sheet of this reference manual.

DIP PIN CONFIGURATION



PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{\text{BLANK}}$	Composite blank control input (TTL compatible). A logic zero on this control input drives the analog outputs to the blanking level, as shown in Table V. The $\overline{\text{BLANK}}$ signal is latched on the rising edge of PCLK. While $\overline{\text{BLANK}}$ is a logical zero, the pixel inputs are ignored.
PCLK	Clock input (TTL compatible). The rising edge of PCLK latches the P0–P7 data inputs and the $\overline{\text{BLANK}}$ control input. It is typically the pixel clock rate of the video system. PCLK should be driven by a dedicated TTL buffer.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. P0–P7 pixel select inputs are latched on the rising edge of PCLK. P0 is the LSB. Unused pixel select inputs should be connected to GND.
RED, GREEN, BLUE	Red, green and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75Ω coaxial cable, as shown in Figure 4a. All three current outputs should have similar output loads whether or not they are all being used.
V_{CC}	Analog power supply (5V ±10%).
GND	Analog ground.
I_{REF}	Current reference input. The relationship between the current input and the full scale output voltage of the DACs is given by the following expression: I_{REF} = VO (Full Scale)/2.15 × R_L R_L = Load Resistance
$\overline{\text{WR}}$	Write control input (TTL compatible). $\overline{\text{WR}}$ must be at logical zero when writing data to the device. D0–D7 data is latched on the rising edge of $\overline{\text{WR}}$. See Figure 1.
$\overline{\text{RD}}$	Read control input (TTL compatible). $\overline{\text{RD}}$ must both be at logical zero when reading data from the device. See Figure 1.
RS0, RS1	Command control inputs (TTL compatible). RS0 and RS1 specify the type of read or write operation being carried out, i.e., address register or color palette RAM read or write operations. See Tables I, II, III.
D0–D7	Data bus (TTL compatible). Data is transferred to and from the address register and the color palette RAM over this 8-bit bidirectional data bus. D0 is the least significant bit.

TERMINOLOGY

Blanking Level
The level separating the SYNC portion from the Video portion of the waveform. Usually referred to as the Front Porch or Back Porch. At 0 IRE Units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

Color Video (RGB)
This usually refers to the technique of combining the three primary colors of Red, Green and Blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs are required, one for each color.

Gray Scale
The discrete levels of video signal between Reference Black and Reference White levels. An 8-bit DAC contains 256 different levels while a 6-bit DAC contains 64.

Raster Scan
The most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level
The maximum negative polarity amplitude of the video signal.

Reference White Level
The maximum positive polarity amplitude of the video signal.

Video Signal
That portion of the composite video signal which varies in gray scale levels between Reference White and Reference Black. Also referred to as the picture signal, this is the portion which may be visually observed.

MPU Interface

As illustrated in the functional block diagram, the ADV476 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM .

The RS0 and RS1 control inputs specify whether the MPU is accessing the address register or the color palette RAM, as shown in Table I. The 8-bit address register is used to address the color palette RAM, eliminating the requirement for external address multiplexers.

RS1	RS0	Addressed by MPU
0	0	Pixel Address Register (RAM Write Mode)
1	1	Pixel Address Register (RAM Read Mode)
0	1	Color Palette RAM
1	0	Pixel Read Mask Register

Table I. Control Input Truth Table

To write color data, the MPU writes to the address register with the 8-bit address of the color palette RAM location which is to be modified. The MPU performs three successive write cycles (six bits of red data, six bits of green data and six bits of blue data). During the blue write cycle, the three bytes of color information are concatenated into an 18-bit word and written to the location specified by the address register. The address register then automatically increments to the next location which the MPU may modify by simply writing another sequence of red, green and blue data.

To read back color data, the MPU loads the address register with the address of the color palette RAM location to be read. The MPU performs three successive read cycles (6 bits each of red, green and blue data). Following the blue read cycle, the address register increments to the next location which the MPU may read by simply reading another sequence of red, green and blue data.

This 6-bit color data is right justified, i.e., the lower six bits of the data bus with D0 being the LSB and D5 the MSB. D6 and D7 are ignored during a color write cycle and are set to zero during a color read cycle.

During color palette RAM access, the address register resets to 00H following a blue read or write operation to RAM location FFH.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. Color (RGB) data is normally loaded to the color palette RAM during video screen retrace, i.e., during the video waveform blanking period, see Figure 5.

To keep track of the red, green and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table II. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register, incremented following a blue read or write cycle, (ADDR0–7) are accessible to the MPU, and are used to address color palette RAM locations, as shown in Table III. ADDR0 is the LSB when the MPU is accessing the RAM. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Figure 1 illustrates the MPU read/write timing and Table III shows the associated functional instructions.

	Value	RS1	RS0	Addressed by MPU
ADDRa,b (Counts Modulo 3)	00 01 10			Red Value Green Value Blue Value
ADDR0–7 (Counts Binary)	00H–FFH	0	1	Color Palette RAM

Table II. Address Register (ADDR) Operation

$\overline{RD}$	$\overline{WR}$	RS0	RS1	ADDRa	ADDRb	Operation Performed	
1	0	0	0	X	X	Write Address Register;	D0–D7 → ADDR0–7 0 → ADDRa,b
1	0	1	0	0	0	Write Red Value;	Increment ADDRa–b
1	0	1	0	0	1	Write Green Value;	Increment ADDRa–b
1	0	1	0	1	0	Write Blue Value;	Modify RAM Location Increment ADDR0–7 Increment ADDRa–b
0	1	1	1	X	X	Read Address Register;	ADDR0–7 → D0–D7
0	1	1	0	0	0	Read Red Value;	Increment ADDRa–b
0	1	1	0	0	1	Read Green Value;	Increment ADDRa–b
0	1	1	0	1	0	Read Blue Value;	Increment ADDR0–7 Increment ADDRa–b
0	0	X	X	X	X	Invalid Operation	

Table III. Truth Table for Read/Write Operations

Frame Buffer Interface

The P0–P7 inputs are used to address the color palette RAM, as shown in Table IV. These inputs are latched on the rising edge of PCLK and address any of the 256 locations in the color palette RAM. The addressed location contains 18 bits of color (6 bits of red, 6 bits of green and 6 bits of blue) information. This data is transferred to the three DACs and is then converted to an analog output (RED, GREEN, BLUE), these outputs then control the red, green and blue electron guns in the monitor.

The $\overline{\text{BLANK}}$ input is also latched on the rising edge of PCLK. This is to maintain synchronization with the color data.

P0–P7	Addressed by Frame Buffer
00H	Color Palette RAM Location 00H
01H	Color Palette RAM Location 01H
•	• •
•	• •
FFH	Color Palette RAM Location FFH

Table IV. Pixel Select/Color Palette Control Truth Table

Pixel Read Mask Register

The Pixel Read Mask Register in the ADV476 can be used to implement register level pixel processing, thereby cutting down on software overhead. This is achieved by gating the input pixel stream (P0–P7) with the contents of the pixel read mask register. The operation is a bitwise logical ANDing of the pixel data. The contents of this register can be accessed and altered at any time by the MPU (D0–D7). Table I shows the relevant control signals.

This pixel masking operation can be used to alter the displayed colors without changing the contents of either the video frame buffer or the color palette RAM. The effect of this operation is to partition the color palette into a user determined number of color planes. This process can be used for special effects including animation, overlays and flashing objects.

(See also application note entitled "Animation Using the Pixel Read Mask Register of the ADV47x Series of Video RAM-DACs," available from Analog Devices (Pub No. E1316–15–10/89).

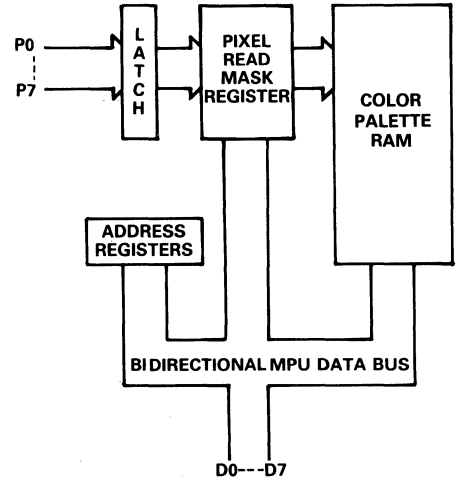


Figure 3. Block Diagram Showing Pixel Read Mask Register

Analog Interface

The ADV476 has three analog outputs, corresponding to the Red, Green and Blue video signals.

The Red, Green and Blue analog outputs of the ADV476 are high impedance current sources. Each one of these three RGB current outputs is capable of directly driving a 37.5Ω load, such as a doubly-terminated 75Ω coaxial cable. Figure 4a shows the required configuration for each of the three RGB outputs connected into a doubly-terminated 75Ω load. This arrangement will develop RS-343A video output voltage levels across a 75Ω monitor. A simple method of driving RS-170 video levels into a 75Ω monitor is shown in Figure 4b. The output current levels of the DACs remain unchanged but the source termination resistance, Z_S, on each of the three DACs is increased from 75Ω to 150Ω.

More detailed information regarding load terminations for various output configurations, including RS-343A and RS-170, is available in an application note entitled "Video Formats & Required Load Terminations" available from Analog Devices.

Figure 5 shows the video waveforms associated with the three RGB outputs, driving the doubly terminated 75Ω load of Figure 4a. The $\overline{\text{BLANK}}$ control input drives the analog outputs to the Black Level. $\overline{\text{BLANK}}$ is asserted prior to horizontal and vertical screen retrace. Table V details how the $\overline{\text{BLANK}}$ input modifies the output levels.

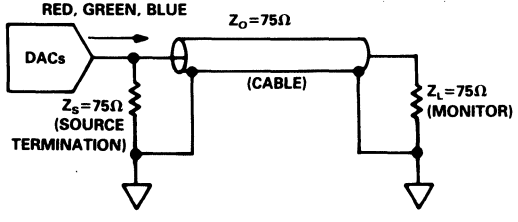


Figure 4a. Recommended Analog Output Termination for RS-343A

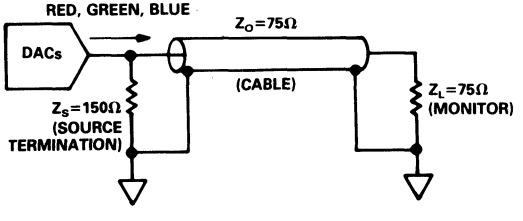
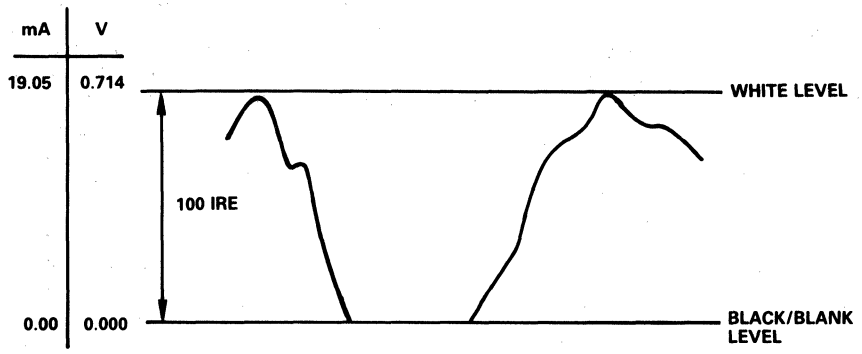


Figure 4b. Recommended Analog Output Termination for RS-170



NOTES
1. **OUTPUTS CONNECTED TO A DOUBLY TERMINATED 75Ω LOAD.**
2. **I_{REF}=8.88mA.**
3. **RS-343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.**

Figure 5. RGB Video Output Waveform

Description	RED, GREEN, BLUE, (mA)[1]	$\overline{\text{BLANK}}$	DAC Input Data
WHITE LEVEL	19.05	1	FFH
VIDEO	Video	1	DATA
BLACK LEVEL	0	1	00H
BLANK LEVEL	0	0	xxH

NOTE
[1]Typical with full scale RED, GREEN, BLUE = 19.05mA. I_{REF} = 8.88mA.

Table V. Video Output Truth Table

Reference Input

The ADV476 requires an active current reference to enable the DACs provide stable and accurate video output levels. The relationship between the output voltage and the required input reference current is given by:

$$I_{REF}=\frac{VO\ (FULL\ SCALE)}{2.15\times R_L}$$

where R_L = 37.5Ω (for doubly terminated 75Ω load)
= 75Ω (for singly terminated 75Ω load)

and VO = 0.714V (RS-343A video levels)
= 1.0V (RS-170 video levels).

In a standard application which requires RS-343A video levels to be driven into a doubly terminated 75Ω load (R_L = 37.5Ω), the necessary reference input current is:

I_{REF} = 8.88mA.

To drive the same levels into a singly terminated 75Ω load (R_L = 75Ω), the reference current is:

I_{REF} = 4.44mA.

A suggested current reference design for the doubly terminated case, with RS-343A video levels and based on the LM334, a three-terminal adjustable current source, is shown in Figure 6.

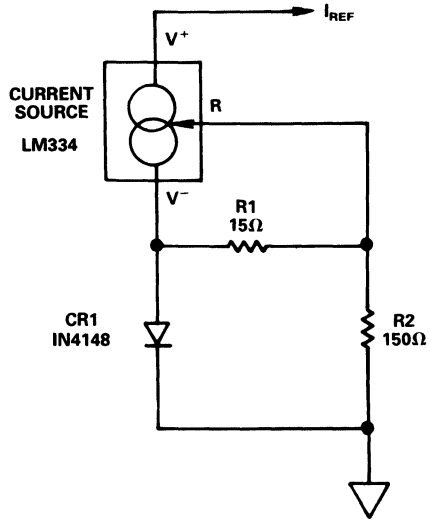


Figure 6. Current Reference Design Using an LM334 Current Source

PC BOARD LAYOUT CONSIDERATIONS

The ADV476 is optimally designed for lowest noise performance, both radiated and conducted noise. For optimum system noise performance, it is imperative that great care be given to the PC board layout. The layout should be optimized for lowest noise on the ADV476 power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{CC} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all ADV476 ground pins, voltage reference circuitry, power supply bypass circuitry, the analog output traces and all the digital signal traces leading up to the ADV476.

Power Planes

The PC board layout should have two distinct power planes, one for analog circuitry and one for digital circuitry. The analog power plane (V_{CC}) should encompass the ADV476 and all associated analog circuitry. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 7. This bead should be located within three inches of the ADV476.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV476 power pins, current reference circuitry and any output amplifiers.

The PCB power and ground planes should not overlay portions of the analog power plane. Keeping the PCB power and ground planes from overlaying the analog power plane will contribute to a reduction in plane-to-plane noise coupling.

Supply Decoupling

Noise on the analog power plane can be further reduced by the use of multiple decoupling capacitors, see Figure 7.

Optimum performance is achieved by the use of 0.1μF ceramic capacitors. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

It is important to note that while the ADV476 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise. A dc power supply filter (Murata BNX002) will provide EMI suppression between the switching power supply and the main PCB. Alternatively, consideration could be given to using a three terminal voltage regulator.

Digital Signal Interconnect

The digital signal lines to the ADV476 should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.

Due to the high clock rates used, long clock lines to the ADV476 should be avoided so as to minimize noise pickup.

Any active pull-up termination resistors for the digital inputs should be connected to the regular PCB power plane and not the analog power plane.

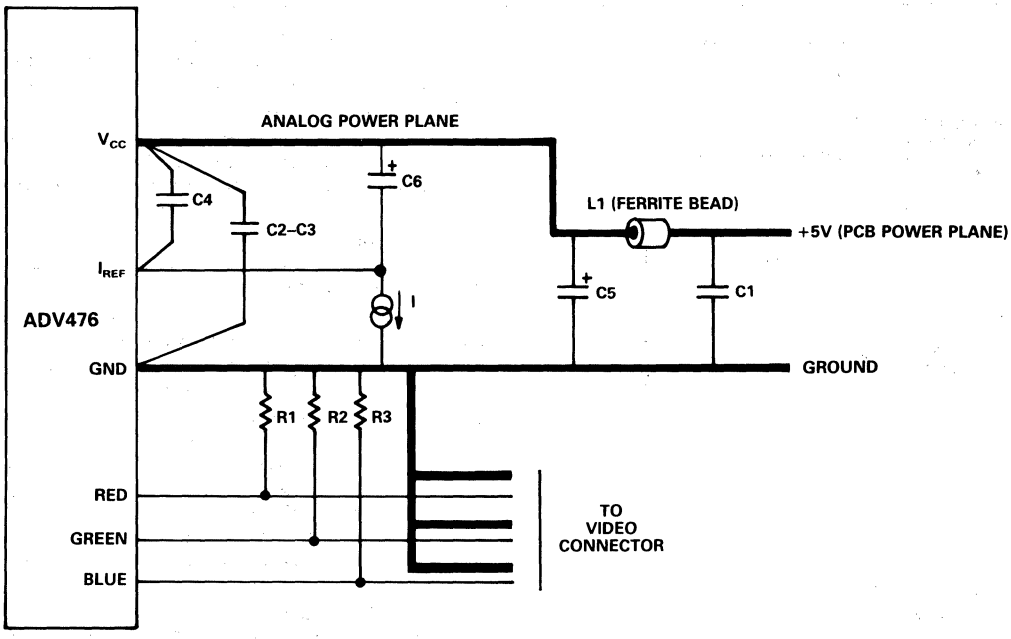
Analog Signal Interconnect

The ADV476 should be located as close as possible to the output connectors thus minimizing noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, thereby maximizing the high frequency power supply rejection.

For optimum performance, the analog outputs should each have a source termination resistance to ground of 75Ω. This termination resistance should be as close as possible to the ADV476 to minimize reflections.

Note: For additional information on PC Board Layout see application note "Design and Layout of a Video Graphics System for Reduced EMI," available from Analog Devices (Pub. No. E1309–15–10/89).



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1–C4	0.1μF CERAMIC CAPACITOR	ERIE RPE112Z5U104M50V
C5	10μF TANTALUM CAPACITOR	MALLORY CSR13G106KM
C6	47μF TANTALUM CAPACITOR	MALLORY CSR13F476KM
L1	FERRITE BEAD	FAIR-RITE 2743001111
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF-55C

Figure 7. ADV476 Typical Connection Diagram and Component List

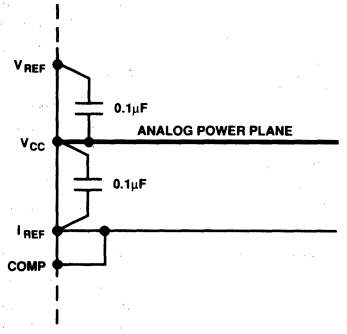


Figure 8. Connection of V_{REF} and COMP with the ADV476KP (44-Pin PLCC)

CMOS 80MHz Monolithic 256 × 24(18) Color Palette RAM-DACs

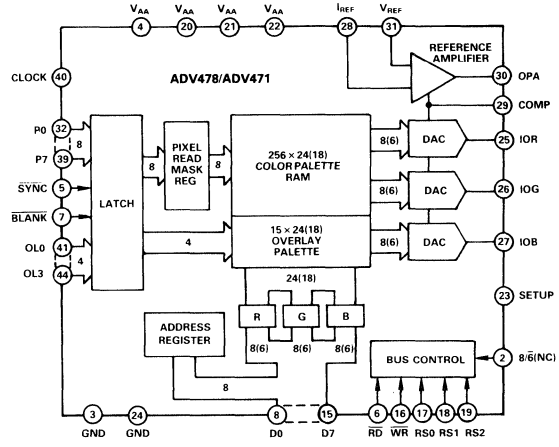
ADV478/ADV471

FEATURES
Personal System/2* Compatible
80MHz Pipelined Operation
Triple 8-Bit (6-Bit) D/A Converters
256 × 24(18) Color Palette RAM
15 × 24(18) Overlay Registers
RS-343A/RS-170 Compatible Outputs
Sync on All Three Channels
Programmable Pedestal (0 or 7.5 IRE)
External Voltage or Current Reference
Standard MPU Interface
+5V CMOS Monolithic Construction
44-Pin PLCC Package
Power Dissipation: 800mW

APPLICATIONS
High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Desktop Publishing

AVAILABLE CLOCK RATES
80MHz
66MHz
50MHz
35MHz

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. NUMBERS IN PARENTHESIS INDICATE PIN NAMES FOR THE ADV471.
2. NC = NO CONNECT

GENERAL DESCRIPTION

The ADV478 (ADV®) and ADV471 are pin compatible and software compatible RAM-DACs designed specifically for Personal System/2 compatible color graphics.

The ADV478 has a 256 × 24 color lookup table with triple 8-bit video D/A converters. It may be configured for either 6 bits or 8 bits per color operation. The ADV471 has a 256 × 18 color lookup table with triple 6-bit video D/A converters.

Options on both parts include a programmable pedestal (0 or 7.5 IRE) and use of an external voltage or current reference. Fifteen overlay registers provide for overlaying cursors, grids, menus, EGA emulation, etc. Also supported is a pixel read mask register and sync generation on all three channels.

The ADV478 and ADV471 generate RS-343A compatible video signals into a doubly terminated 75Ω load, and RS-170 compatible video signals into a singly terminated 75Ω load, without requiring external buffering. Differential and integral linearity errors are guaranteed to be a maximum of ±1LSB for the ADV478 and ±1/4LSB for the ADV471 over the full temperature range.

ADV478/ADV471—SPECIFICATIONS

(V_{AA}[1] = +5V, SETUP = 8/$\overline{6}$ = V_{AA}, V_{REF} = +1.235V. R_{SET} = 147Ω. All Specifications T_{min} to T_{max}[2] unless otherwise noted.)

Parameter	All Versions	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution (Each DAC)[3]	8 (6)	Bits	
Accuracy (Each DAC)[3]			
Integral Nonlinearity	±1 (1/4)	LSB max	
Differential Nonlinearity	±1 (1/4)	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	% Gray Scale max	
Coding	Binary		
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±1	μA max	V_{IN} = 0.4V or 2.4V
Input Capacitance, C_{IN}	7	pF max	
DIGITAL OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 400μA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 3.2mA
Floating-State Leakage Current	50	μA max	
Floating-State Output Capacitance	7	pF max	
ANALOG OUTPUTS			
Gray Scale Current Range	20	mA max	
Output Current			
White Level Relative to Blank	17.69	mA min	Typically 19.05mA
	20.40	mA max	
White Level Relative to Black	16.74	mA min	Typically 17.62mA
	18.50	mA max	
Black Level Relative to Blank	0.95	mA min	Typically 1.44mA
(SETUP = V_{AA})	1.90	mA max	
Black Level Relative to Blank	0	μA min	Typically 5μA
(SETUP = GND)	50	μA max	
Blank Level	6.29	mA min	Typically 7.62mA
	8.96	mA max	
Sync Level	0	μA min	Typically 5μA
	50	μA max	
LSB Size[3]	69.1 (279.68)	μA typ	8/$\overline{6}$ = Logical 1 for ADV478
DAC to DAC Matching	5	% max	Typically 2%
Output Compliance, V_{OC}	−1	V min	
	+1.5	V max	
Output Impedance, R_{OUT}	10	kΩ typ	
Output Capacitance, C_{OUT}	30	pF max	I_{OUT} = 0mA
VOLTAGE REFERENCE			
Voltage Reference Range, V_{REF}	1.14/1.26	V min/V max	
Input Current, I_{VREF}	10	μA typ	Tested in Voltage Reference Configuration with V_{REF} = 1.235V
POWER SUPPLY			
Supply Voltage, V_{AA}	4.75/5.25	V min/V max	80MHz and 66MHz Parts
	4.50/5.50	V min/V max	50MHz and 35MHz Parts
Supply Current, I_{AA}	220	mA max	Typically 180mA
Power Supply Rejection Ratio	0.5	%/% max	f = 1kHz, COMP = 0.1μF
Power Dissipation	1100	mW max	Typically 900mW, V_{AA} = 5V
DYNAMIC PERFORMANCE			
Clock and Data Feedthrough[4,5]	−30	dB typ	
Glitch Impulse[4,5]	75	pV secs typ	
DAC to DAC Crosstalk[6]	−23	dB typ	

NOTES

[1] ±5% for 80MHz and 66MHz parts; ±10% for 50MHz and 35MHz parts.

[2] Temperature Range (T_{min} to T_{max}); 0 to +70°C.

[3] Numbers in parentheses indicate ADV471 parameter value.

[4] Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1kΩ resistor to ground and are driven by 74HC logic. Glitch impulse includes clock and data feedthrough, −3dB test bandwidth = 2 × clock rate.

[5] TTL input values are 0 to 3 volts, with input rise/fall times ≤3ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10pF, D0 − D7 output load ≤50pF. See timing notes in Figure 2.

[6] DAC to DAC crosstalk is measured by holding one DAC high while the other two are making low to high and high to low transitions.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{AA}[2] = +5V, SETUP = 8/$\overline{6}$ = V_{AA}, V_{REF} = 1.235V. R_{SET} = 147Ω. All Specifications T_{min} to T_{max}[3].)

Parameter	KP80 Version	KP66 Version	KP50 Version	KP35 Version	Units	Conditions/Comments
f_{max}	80	66	50	35	MHz	Clock Rate
t_1	10	10	10	10	ns min	RS0 – RS2 Setup Time
t_2	10	10	10	10	ns min	RS0 – RS2 Hold Time
t_3	5	5	5	5	ns min	$\overline{RD}$ Asserted to Data Bus Driven
t_4	40	40	40	40	ns max	$\overline{RD}$ Asserted to Data Valid
t_5	20	20	20	20	ns max	$\overline{RD}$ Negated to Data Bus 3-Stated
t_6	10	10	10	10	ns min	Write Data Setup Time
t_7	10	10	10	10	ns min	Write Data Hold Time
t_8	50	50	50	50	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width Low
t_9	$6 \times t_{12}$	$6 \times t_{12}$	$6 \times t_{12}$	$6 \times t_{12}$	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width High
t_{10}	3	3	3	3	ns min	Pixel and Control Setup Time
t_{11}	3	3	3	3	ns min	Pixel and Control Hold Time
t_{12}	12.5	15.3	20	28	ns min	Clock Cycle Time
t_{13}	4	5	6	7	ns min	Clock Pulse Width High Time
t_{14}	4	5	6	9	ns min	Clock Pulse Width Low Time
t_{15}	30	30	30	30	ns max	Analog Output Delay
t_{16}	3	3	3	3	ns typ	Analog Output Rise/Fall Time
t_{17}[4]	13	15.3	20	28	ns typ	Analog Output Settling Time
t_{18}	2	2	2	2	ns max	Analog Output Skew
t_{PD}	$4 \times t_{12}$	$4 \times t_{12}$	$4 \times t_{12}$	$4 \times t_{12}$	ns min	Pipeline Delay

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10pF, 37.5Ω. D0 – D7 output load ≤50pF. See timing notes in Figure 2.
[2]±5% for 80MHz and 66MHz parts; ±5% for 50MHz and 35MHz parts.
[3]Temperature Range (T_{min} to T_{max}); 0 to +70°C.
[4]Settling time does not include clock and data feedthrough. For this test, the digital inputs have a 1kΩ resistor to ground and are driven by 74HC logic.
Specifications subject to change without notice

6

TIMING DIAGRAMS

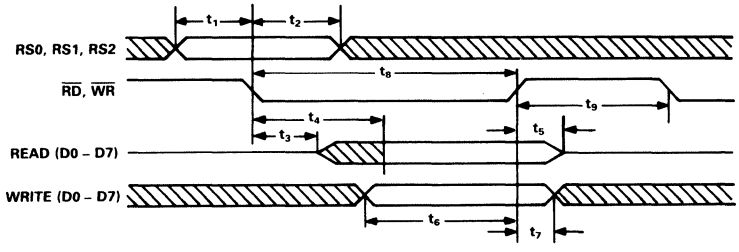
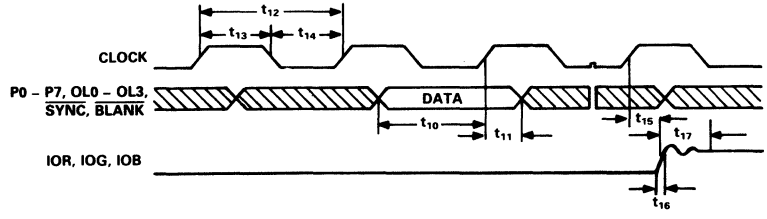


Figure 1. MPU Read/Write Timing



NOTES
1. OUTPUT DELAY (t_{15}) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL SCALE TRANSITION.
2. SETTLING TIME (t_{17}) MEASURED FROM THE 50% POINT OF FULL SCALE TRANSITION TO THE OUTPUT REMAINING WITHIN ±1LSB (ADV478) OR ±1/4LSB (ADV471).
3. OUTPUT RISE/FALL TIME (t_{16}) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL SCALE TRANSITION.

Figure 2. Video Input/Output Timing

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}				
80MHz, 66MHz Parts		4.75	5.00	5.25	Volts
50, 35MHz Parts		4.5	5.00	5.5	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Voltage Reference Configuration					
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts
Current Reference Configuration					
Reference Current	I_{REF}	−3		−10	mA

CAUTION

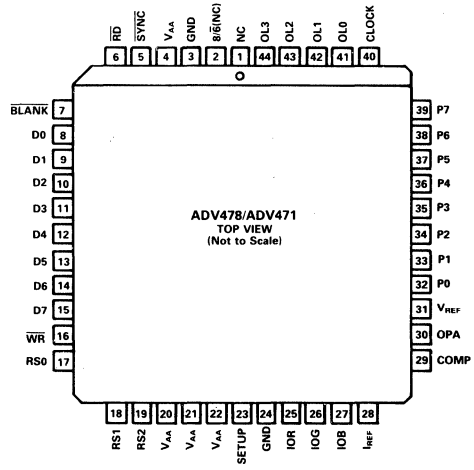
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ABSOLUTE MAXIMUM RATINGS*

V_{AA} to GND . . . . . +7V
Voltage on Any Digital Pin . . . GND −0.5V to V_{AA} +0.5V
Ambient Operating Temperature (T_A) . . . −55°C to +125°C
Storage Temperature (T_S) . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Junction Temperature (T_J) . . . . . +175°C
Vapor Phase Soldering (1 minute) . . . . . 220°C
IOR, IOB, IOG to GND[1] . . . . . 0V to V_{AA}

NOTES
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[1]Analog output short circuit to any power supply or common can be of an indefinite duration.

PLCC PIN CONFIGURATION



NOTES
1. NUMBERS IN PARENTHESIS INDICATE PIN NAMES FOR THE ADV471.
2. NC = NO CONNECT

ORDERING GUIDE

Model	Temperature Range	Color Palette RAM	Speed	Package Option*
ADV471KP80	0°C to +70°C	256 × 18	80MHz	P-44A
ADV471KP66	0°C to +70°C	256 × 18	66MHz	P-44A
ADV471KP50	0°C to +70°C	256 × 18	50MHz	P-44A
ADV471KP35	0°C to +70°C	256 × 18	35MHz	P-44A
ADV478KP80	0°C to +70°C	256 × 24	80MHz	P-44A
ADV478KP66	0°C to +70°C	256 × 24	66MHz	P-44A
ADV478KP50	0°C to +70°C	256 × 24	50MHz	P-44A
ADV478KP35	0°C to +70°C	256 × 24	35MHz	P-44A

*P = Plastic Leaded Chip Carrier (PLCC). For outline information see Package Information section.

PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{\text{BLANK}}$	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level as illustrated in Tables IV and V. It is latched on the rising edge of CLOCK. When $\overline{\text{BLANK}}$ is a logical zero, the pixel and overlay inputs are ignored
SETUP	Setup control input. Used to specify either a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = V_{AA}) blanking pedestal.
$\overline{\text{SYNC}}$	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 3 and 4). $\overline{\text{SYNC}}$ does not override any other control or data input, as shown in Tables IV and V; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0 – P7, OL0 – OL3, $\overline{\text{SYNC}}$, and $\overline{\text{BLANK}}$ inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer.
P0 – P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0 – OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table III. When accessing the overlay palette, the P0 – P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75Ω coaxial cable (Figures 5 and 6).
I_{REF}	Full-scale adjust control. Note that the IRE relationships in Figures 3 and 4 are maintained, regardless of the full-scale output current. When using an external voltage reference (Figure 5), a resistor (R_{SET}) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between R_{SET} and the full-scale output current on each output is: R_{SET} (Ω) = K * 1,000 * V_{REF} (V)/I_{OUT} (mA) K is defined in the table below, along with corresponding R_{SET} values for doubly terminated 75Ω loads. When using an external current reference (Figure 6), the relationship between I_{REF} and the full-scale output current on each output is: I_{REF} (mA) = I_{OUT} (mA)/K

Mode	Pedestal	K	R_{SET} (Ω)
6-Bit	7.5 IRE	3.170	147
8-Bit	7.5 IRE	3.195	147
6-Bit	0 IRE	3.000	147
8-Bit	0 IRE	3.025	147

COMP	Compensation pin. If an external voltage reference is used (Figure 5), this pin should be connected to OPA. If an external current reference is used, this pin should be connected to I_{REF}. A 0.1μF ceramic capacitor must always be used to bypass this pin to V_{AA}.
V_{REF}	Voltage reference input. If an external voltage reference is used (Figure 5), it must supply this input with a 1.2V (typical) reference. If an external current reference is used (Figure 6), this pin should be left floating, except for the bypass capacitor. A 0.1μF ceramic capacitor must always be used to decouple this input to V_{AA} as shown in Figures 5 and 6.
OPA	Reference amplifier output. If an external voltage reference is used (Figure 5), this pin must be connected to COMP. When using an external current reference (Figure 6), this pin should be left floating.
V_{AA}	Analog power. All V_{AA} pins must be connected to the Analog Power Plane.
GND	Analog ground. All GND pins must be connected to the Ground Plane.
$\overline{\text{WR}}$	Write control input (TTL compatible). D0 – D7 data is latched on the rising edge of $\overline{\text{WR}}$, and RS0 – RS2 are latched on the falling edge of $\overline{\text{WR}}$ during MPU write operations. See Figure 1.

PIN FUNCTION DESCRIPTION (Continued)

Pin Mnemonic	Function
$\overline{RD}$	Read control input (TTL compatible). To read data from the device, $\overline{RD}$ must be a logical zero. RS0 – RS2 are latched on the falling edge of $\overline{RD}$ during MPU read operations.
RS0, RS1, RS2	Register select inputs (TTL compatible). RS0 – RS2 specify the type of read or write operation being performed as illustrated in Tables I and II.
D0 – D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
8/$\overline{6}$	8-bit/6-bit select input (TTL compatible). This control input specifies whether the MPU is reading and writing 8-bits (logical one) or 6-bits (logical zero) of color information each cycle. For 8-bit operation, D7 is the most significant data bit during color read/write cycles. For 6-bit operation, D5 is the most significant data bit during color read/write cycles (D6 and D7 are ignored during color write cycles and are logical zero during color read cycles). This control input is implemented only on the ADV478.

TERMINOLOGY

Blanking Level
The level seperating the SYNC portion from the video portion of the waveform. Usually referred to as the front porch or back porch. At 0 IRE units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

Color Video (RGB)
This usually refers to the technique of combining the three primary colors of red, green and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs would be required, one for each color.

Composite SYNC Signal (SYNC)
The position of the composite video signal which synchronizes the scanning process.

Composite Video Signal
The video signal with or without setup, plus the composite SYNC signal.

Gray Scale
The discrete levels of video signal between reference black and reference white levels. An 8-bit DAC contains 256 different levels while a 6-bit DAC contains 64.

Raster Scan
The most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level
The maximum negative polarity amplitude of the video signal.

Reference White Level
The maximum positive polarity amplitude of the video signal.

Setup
The difference between the reference black level and the blanking level.

SYNC Level
The peak level of the composite SYNC signal.

Video Signal
That portion of the composite video signal which varies in gray scale levels between reference white and reference black. Also referred to as the picture signal, this is the portion which may be visually observed.

CIRCUIT DESCRIPTION

MPU Interface

As illustrated in the functional block diagram, the ADV478 and ADV471 support a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0 – RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers or read mask register, as shown in Table I. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers.

To write color data, the MPU writes to the address register (selecting RAM or overlay write mode) with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (8 or 6 bits each of red, green and blue), using RS0 – RS2 to select either the color palette RAM or overlay registers. During the blue write cycle, the three bytes of color information are concatenated into a 24-bit word (18-bit word for the ADV471) and written to the location specified by the address register. The address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green and blue data.

RS2	RS1	RS0	Addressed by MPU
0	0	0	Address Register (RAM Write Mode)
0	1	1	Address Register (RAM Read Mode)
0	0	1	Color Palette RAM
0	1	0	Pixel Read Mask Register
1	0	0	Address Register (Overlay Write Mode)
1	1	1	Address Register (Overlay Read Mode)
1	0	1	Overlay Registers
1	1	0	Reserved

Table I. Control Input Truth Table

To read color data, the MPU loads the address register (selecting RAM or overlay read mode) with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles (8 or 6 bits each of red, green and blue), using RS0 – RS2 to select either the color palette RAM or overlay registers. Following the blue read cycle, the address register increments to the next location which the MPU may read by simply reading another sequence of red, green and blue data.

When accessing the color palette RAM, the address register resets to 00H following a blue read or write cycle to RAM location FFH. When accessing the overlay color registers, the address register increments following a blue read or write cycle. However, while accessing the overlay color registers, the four most significant bits of the address register (ADDR4 – 7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM/overlay registers and the color registers (R, G and B in the block diagram) are synchronized by internal logic and occur in the period between MPU accesses. As only one pixel clock cycle is required to complete the transfer, the color palette RAM and overlay registers may be accessed at any time with no noticeable disturbance on the display screen.

To keep track of the red, green and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table II. They are reset to zero when the MPU writes to the address register and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register, incremented following a blue read or write cycle (ADDR0 – 7), are accessible to the MPU and are used to address color palette RAM locations and overlay registers, as shown in Table II. ADDR0 is the LSB when the MPU is accessing the RAM or overlay registers. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Figure 1 illustrates the MPU read/write timing.

	Value	RS2	RS1	RS0	Addressed By MPU
ADDRa,b (Counts Modulo 3)	00				Red Value
	01				Green Value
	10				Blue Value
ADDR0 – 7 (Counts Binary)	00H – FFH	0	0	1	Color Palette RAM
	XXXX 0000	1	0	1	Reserved
	XXXX 0001	1	0	1	Overlay Color 1
	XXXX 0010	1	0	1	Overlay Color 2
	•	•	•	•	•
	•	•	•	•	•
	XXXX 1111	1	0	1	Overlay Color 15

Table II. Address Register (ADDR) Operation

ADV478 Data Bus Interface
On the ADV478, the 8/$\overline{6}$ control input is used to specify whether the MPU is reading and writing 8 bits (8/$\overline{6}$ = logical one) or 6 bits (8/$\overline{6}$ = logical zero) of color information each cycle.

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

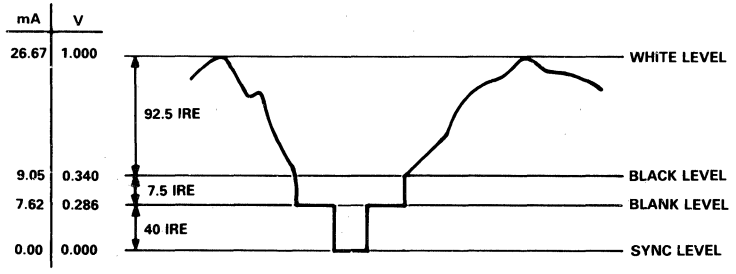
For 6-bit operation (and also when using the ADV471), color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

ADV471 Data Bus Interface
Color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

Frame Buffer Interface
The P0 – P7 and OL0 – OL3 inputs are used to address the color palette RAM and overlay registers, as shown in Table III.

OL0 – OL3	P0 – P7	Addressed by Frame Buffer
0H	00H	Color Palette RAM Location 00H
0H	01H	Color Palette RAM Location 01H
•	•	•
•	•	•
0H	FFH	Color Palette RAM Location FFH
1H	XXH	Overlay Color 1
2H	XXH	Overlay Color 2
•	•	•
•	•	•
FH	XXH	Overlay Color 15

Table III. Pixel and Overlay Control Truth Table (Pixel Read Mask Register = FFH)



NOTES
1. CONNECTED WITH A 75Ω DOUBLY TERMINATED LOAD, SETUP = V_{AA}.
2. EXTERNAL VOLTAGE OR CURRENT REFERENCE ADJUSTED FOR 26.67mA FULL-SCALE OUTPUT.
3. RS-343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 3. Composite Video Output Waveform (SETUP = V_{AA})

Description	I_{OUT} (mA)[1]	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE LEVEL	26.67	1	1	FFH
DATA	data + 9.05	1	1	data
DATA-SYNC	data + 1.44	0	1	data
BLACK LEVEL	9.05	1	1	00H
BLACK-SYNC	1.44	0	1	00H
BLANK LEVEL	7.62	1	0	xxH
SYNC LEVEL	0	0	0	xxH

NOTES
[1]Typical with full-scale IOG = 26.67mA, SETUP = V_{AA}.
External voltage or current reference adjusted for 26.67mA full-scale output.

Table IV. Video Output Truth Table (SETUP = V_{AA})

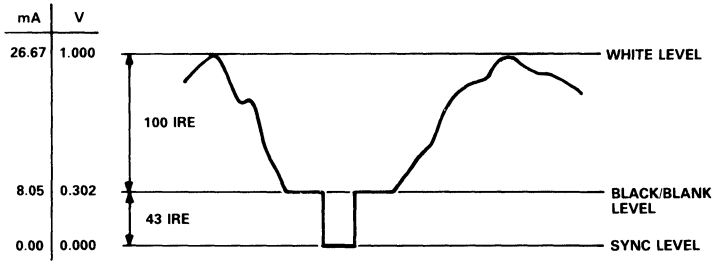
The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P0 – P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides 24 bits (18 bits for the ADV471) of color information to the three D/A converters.

For additional information on Pixel Mask Register, see application note "Animation Using the Pixel Read Mask Register of the ADV47X Series of Video RAM-DACs"(Publication Number E1316–15–10/89).

The $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 3 and 4. Tables IV and V detail how the $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs modify the output levels.

The SETUP input is used to specify whether a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = V_{AA}) blanking pedestal is to be used.

The analog outputs of the ADV478 and ADV471 are capable of directly driving a 37.5Ω load, such as a doubly terminated 75Ω coaxial cable.



NOTES
1. CONNECTED WITH A 75Ω DOUBLY TERMINATED LOAD, SETUP = GND.
2. EXTERNAL VOLTAGE OR CURRENT REFERENCE ADJUSTED FOR 26.67mA FULL-SCALE OUTPUT.
3. RS-343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 4. Composite Video Output Waveform (SETUP = GND)

Description	I_{OUT} (mA)[1]	$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	DAC Input Data
WHITE LEVEL	26.67	1	1	FFH
DATA	data + 8.05	1	1	data
DATA-SYNC	data	0	1	data
BLACK LEVEL	8.05	1	1	00H
BLACK-SYNC	0	0	1	00H
BLANK LEVEL	8.05	1	0	xxH
SYNC LEVEL	0	0	0	xxH

NOTES
[1]Typical with full-scale IOG = 26.67mA, SETUP = GND
External voltage or current reference adjusted for 26.67mA full-scale output.

Table V. Video Output Truth Table (SETUP = GND)

PC BOARD LAYOUT CONSIDERATIONS

PC Board Considerations

The layout should be optimized for lowest noise on the ADV478/ADV471 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all ADV478/ADV471 ground pins, current/voltage reference circuitry, power supply bypass circuitry for the ADV478/ADV471, the analog output traces and all the digital signal traces leading up to the ADV478/ADV471.

Power Planes

The ADV478/ADV471 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead, as illustrated in Figures 5 and 6. This bead should be located within three inches of the ADV478/ADV471.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV478/ADV471 power pins and current/voltage reference circuitry.

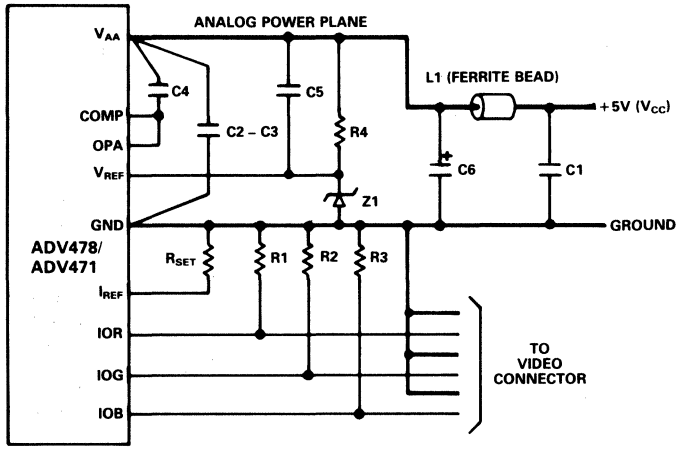
Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

Best performance is obtained with a 0.1μF ceramic capacitor decoupling each of the two groups of V_{AA} pins to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the ADV478 and ADV471 contain circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1 – C5	0.1μF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	10μF Tantalum Capacitor	Mallory CSR13G106KM
L1	Ferrite Bead	Fair-Rite 2743001111
R1, R2, R3	75Ω 1% Metal Film Resistor	Dale CMF-55C
R4	1kΩ 5% Resistor	
R_{SET}	1% Metal Film Resistor	Dale CMF-55C
Z1	1.2V Voltage Reference	Analog Devices AD589KH

Figure 5. Typical Connection Diagram and Component List (External Voltage Reference)

Digital Signal Interconnect

The digital inputs to the ADV478/ADV471 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the ADV478/ADV471 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

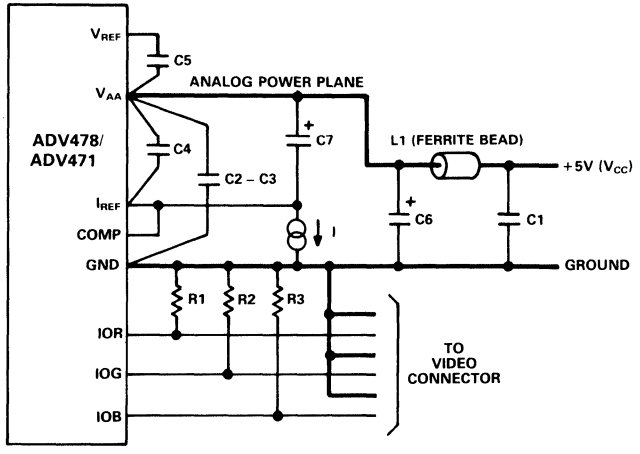
Analog Signal Interconnect

The ADV478/ADV471 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75Ω load resistor connected to GND. The connection between the current output and GND should be as close as possible to the ADV478/ADV471 to minimize reflections.

NOTE: Additional information on PC Board layout can be obtained in an application note entitled "Design and Layout of a Video Graphics System for Reduced EMI" from Analog Devices (Publication Note E1309–15–10/89).



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1 – C5	0.1μF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	10μF Tantalum Capacitor	Mallory CSR13G106KM
C7	47μF Tantalum Capacitor	Mallory CSR13F476KM
L1	Ferrite Bead	Fair-Rite 2743001111
R1, R2, R3	75Ω 1% Metal Film Resistor	Dale CMF-55C

Figure 6. Typical Connection Diagram and Component List (External Current Reference)

APPLICATION INFORMATION

External Voltage vs. Current Reference

The ADV478/ADV471 is designed to have excellent performance using either an external voltage or current reference. The voltage reference design (Figure 5) has the advantages of temperature compensation, simplicity, lower cost and provides excellent power supply rejection. The current reference design (Figure 6) requires more components to provide adequate power supply rejection and temperature compensation (two transistors, three resistors and additional capacitors).

RS-170 Video Generation

For generation of RS-170 compatible video, it is recommended that the DAC outputs be connected to a singly terminated 75Ωload. If the ADV478/ADV471 is not driving a large capacitive load, there will be negligible difference in video quality between doubly terminated 75Ω and singly terminated 75Ω loads.

If driving a large capacitive load (load RC> $1/(2\pi f_C)$), it is recommended that an output buffer (such as an AD848 or AD9617 with an unloaded gain>2) be used to drive a doubly terminated 75Ω load.

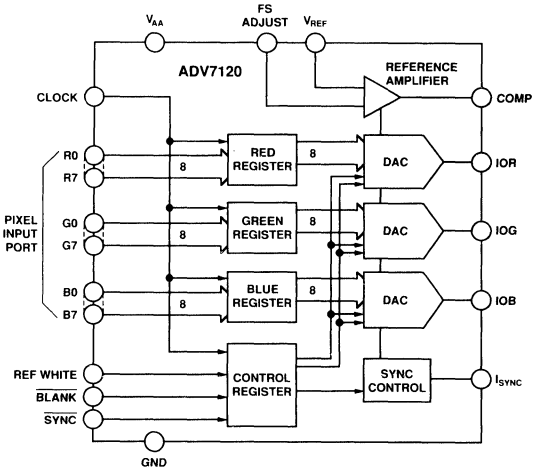
CMOS
80 MHz, Triple 8-Bit Video DAC
ADV7120

FEATURES
80 MHz Pipelined Operation
Triple 8-Bit D/A Converters
RS-343A/RS-170 Compatible Outputs
TTL Compatible Inputs
+5 V CMOS Monolithic Construction
40-Pin DIP or 44-Pin PLCC Package
Power Dissipation: 400 mW

APPLICATIONS
High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Video Signal Reconstruction
Desktop Publishing
Direct Digital Synthesis (DDS)

SPEED GRADES
80 MHz
50 MHz
30 MHz

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADV7120 (ADV®) is a digital to analog video converter on a single monolithic chip. The part is specifically designed for high resolution color graphics and video systems. It consists of three, high speed, 8-bit, video D/A converters (RGB); a standard TTL input interface and high impedance, analog output, current sources.

The ADV7120 has three separate, 8-bit, pixel input ports, one each for red, green and blue video data. Additional video input controls on the part include composite sync, blank and reference white. A single +5 V supply, an external 1.23 V reference and pixel clock input are all that are required to make the part operational.

The ADV7120 is capable of generating RGB video output signals, which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

The ADV7120 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation. The part is packaged in both a 0.6", 40-pin plastic DIP and a 44-pin plastic leaded (J-lead) chip carrier, PLCC.

PRODUCT HIGHLIGHTS

1. Fast video refresh rate, 80 MHz.
2. Compatible with a wide variety of high resolution color graphics video systems.
3. Guaranteed monotonic with a maximum differential nonlinearity of ±0.5 LSB. Integral nonlinearity is guaranteed to be a maximum of ±1 LSB.

ADV7120—SPECIFICATIONS

(V_{AA} = +5 V ±5%; V_{REF} = +1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 560 Ω. I_{SYNC} connected to IOG. All Specifications T_{MIN} to T_{MAX}[1] unless otherwise noted).

Parameter	All Versions	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution (Each DAC)	8	Bits	
Accuracy (Each DAC)			
Integral Nonlinearity, INL	±1	LSB max	
Differential Nonlinearity, DNL	±0.5	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	% Gray Scale max	Max Gray Scale Current: IOG = (V_{REF}* 12,082/R_{SET}) mA
			IOR, IOB = (V_{REF}* 8,627/R_{SET}) mA
Coding	Binary		
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±1	μA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}[2]	10	pF max	
ANALOG OUTPUTS			
Gray Scale Current Range	15	mA min	
	22	mA max	
Output Current			
White Level Relative to Blank	17.69	mA min	Typically 19.05 mA
	20.40	mA max	
White Level Relative to Black	16.74	mA min	Typically 17.62 mA
	18.50	mA max	
Black Level Relative to Blank	0.95	mA min	Typically 1.44 mA
	1.90	mA max	
Blank Level on IOR, IOB	0	μA min	Typically 5 μA
	50	μA max	
Blank Level on IOG	6.29	mA min	Typically 7.62 mA
	9.5	mA max	
Sync Level on IOG	0	μA min	Typically 5 μA
	50	μA max	
LSB Size	69.1	μA typ	
DAC to DAC Matching	5	% max	Typically 2%
Output Compliance, V_{OC}	−1	V min	
	+1.4	V max	
Output Impedance, R_{OUT}[2]	100	kΩ typ	
Output Capacitance, C_{OUT}[2]	30	pF max	I_{OUT} = 0 mA
VOLTAGE REFERENCE			
Voltage Reference Range, V_{REF}	1.14/1.26	V min/V max	V_{REF} = 1.235 V for Specified Performance
Input Current, I_{VREF}	−5	mA typ	
POWER REQUIREMENTS			
V_{AA}	5	V nom	
I_{AA}	125	mA max	Typically 80 mA: 80 MHz Parts
	100	mA max	Typically 70 mA: 50 MHz & 35 MHz Parts
Power Supply Rejection Ratio	0.5	%/% max	Typically 0.12%/%: f = 1 kHz, COMP = 0.1 μF
Power Dissipation	625	mW max	Typically 400 mW: 80 MHz Parts
	500	mW max	Typically 350 mW: 50 MHz & 30 MHz Parts
DYNAMIC PERFORMANCE			
Glitch Impulse[2, 3]	50	pV secs typ	
DAC Noise[2, 3, 4]	200	pV secs typ	
Analog Output Skew	2	ns max	Typically 1 ns

NOTES

[1]Temperature Range (T_{min} to T_{max}); 0 to +70°C.

[2]Sample tested at +25°C to ensure compliance.

[3]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. See timing notes in Figure 1.

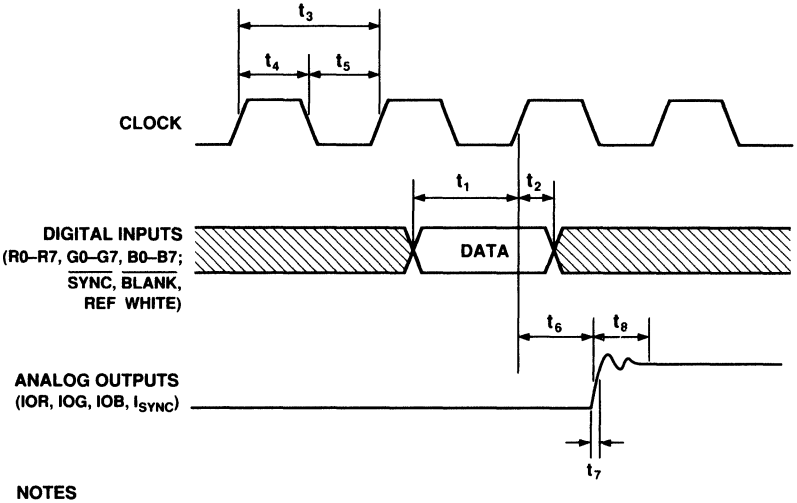
[4]This includes effects due to clock and data feedthrough as well as RGB analog crosstalk.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{AA} = +5 V ±5%; V_{REF} = +1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 560 Ω. I_{SYNC} connected to IOG. All Specifications T_{min} to T_{max}[2] unless otherwise noted.)

Parameter	80 MHz Version	50 MHz Version	30 MHz Version	Units	Conditions/Comments
f_{max}	80	50	30	MHz max	Clock Rate
t_1	3	6	8	ns min	Data & Control Setup Time
t_2	2	2	2	ns min	Data & Control Hold Time
t_3	12.5	20	33.3	ns min	Clock Cycle Time
t_4	4	7	9	ns min	Clock Pulse Width High Time
t_5	4	7	9	ns min	Clock Pulse Width Low Time
t_6	30	30	30	ns max	Analog Output Delay
	20	20	20	ns typ	
t_7	3	3	3	ns max	Analog Output Rise/Fall Time
t_8[3]	12	15	15	ns typ	Analog Output Transition Time

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. See timing notes in Figure 1.
[2]Temperature range (T_{min} to T_{max}): 0 to +70°C
[3]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.



NOTES
1. OUTPUT DELAY (t_6) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL-SCALE TRANSITION.
2. TRANSITION TIME (t_8) MEASURED FROM THE 50% POINT OF FULL-SCALE TRANSITION TO WITHIN 2% OF THE FINAL OUTPUT VALUE.
3. OUTPUT RISE/FALL TIME (t_7) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL TRANSITION.

Figure 1. Video Input/Output Timing

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}	4.75	5.00	5.25	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts

ABSOLUTE MAXIMUM RATINGS*

V_{AA} to GND . . . . . +7 V
Voltage on Any Digital Pin . . . . GND −0.5 V to V_{AA} +0.5 V
Ambient Operating Temperature (T_A) . . . . . 0 to +70°C
Storage Temperature (T_S) . . . . . −65°C to +150°C
Junction Temperature (T_J) . . . . . +175°C
Soldering Temperature (10 secs) . . . . . 300°C
Vapor Phase Soldering (1 minute) . . . . . 220°C
IOR, IOB, IOG, I_{SYNC} to GND[1] . . . . . 0 V to V_{AA}

NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

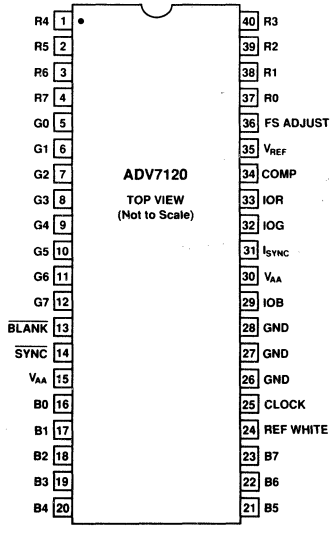
ORDERING GUIDE

Model	Speed	Temperature Range	Package Option*
ADV7120KN80	80 MHz	0°C to +70°C	N-40A
ADV7120KN50	50 MHz	0°C to +70°C	N-40A
ADV7120KN30	30 MHz	0°C to +70°C	N-40A
ADV7120KP80	80 MHz	0°C to +70°C	P-44A
ADV7120KP50	50 MHz	0°C to +70°C	P-44A
ADV7120KP30	30 MHz	0°C to +70°C	P-44A

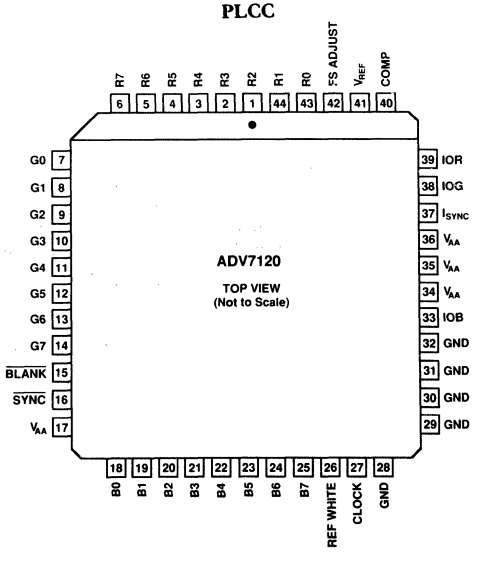
*N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

PIN CONFIGURATIONS

DIP



PLCC



PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{\text{BLANK}}$	Composite blank control input (TTL compatible). A logic zero on this control input drives the analog outputs, IOR, IOB and IOG, to the blanking level. The $\overline{\text{BLANK}}$ signal is latched on the rising edge of CLOCK. While $\overline{\text{BLANK}}$ is a logical zero, the R0–R7, G0–G7, R0–R7 and REF WHITE pixel and control inputs are ignored.
$\overline{\text{SYNC}}$	Composite sync control input (TTL compatible). A logical zero on the $\overline{\text{SYNC}}$ input switches off a 40 IRE current source on the I_{SYNC} output. $\overline{\text{SYNC}}$ does not override any other control or data input; therefore, it should only be asserted during the blanking interval. $\overline{\text{SYNC}}$ is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0–R7, G0–G7, B0–B7, $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ and REF WHITE pixel and control inputs. It is typically the pixel clock rate of the video system. CLOCK should be driven by a dedicated TTL buffer.
REF WHITE	Reference white control input (TTL compatible). A logical one on this input forces the IOR, IOG and IOB outputs to the white level, regardless of the pixel input data (R0–R7, G0–G7 and B0–B7). REF WHITE is latched on the rising edge of clock.
R0–R7, G0–G7, B0–B7	Red, green and blue pixel data inputs (TTL compatible). Pixel data is latched on the rising edge of CLOCK. R0, G0 and B0 are the least significant data bits. Unused pixel data inputs should be connected to either the regular PCB power or ground plane.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable. All three current outputs should have similar output loads whether or not they are all being used.
I_{SYNC}	Sync current output. This high impedance current source can be directly connected to the IOG output. This allows sync information to be encoded onto the green channel. I_{SYNC} does not output any current while $\overline{\text{SYNC}}$ is at logical zero. The amount of current output at I_{SYNC} while $\overline{\text{SYNC}}$ is at logical one is given by: $I_{SYNC}\,(mA) = 3{,}455 \times V_{REF}\,(V)/\,R_{SET}\,(\Omega)$ If sync information is not required on the green channel, I_{SYNC} should be connected to AGND.
FS ADJUST	Full-scale adjust control. A resistor (R_{SET}) connected between this pin and GND, controls the magnitude of the full-scale video signal. Note that the IRE relationships are maintained, regardless of the full-scale output current. The relationship between R_{SET} and the full-scale output current on IOG (assuming I_{SYNC} is connected to IOG) is given by: $R_{SET}\,(\Omega) = 12{,}082 \times V_{REF}\,(V)/IOG\,(mA)$ The relationship between R_{SET} and the full-scale output current on IOR and IOB is given by: $IOR,\ IOB\,(mA) = 8{,}628 \times V_{REF}\,(V)/\,R_{SET}\,(\Omega)$
COMP	Compensation pin. This is a compensation pin for the internal reference amplifier. A 0.1 μF ceramic capacitor must be connected between COMP and V_{AA}.
V_{REF}	Voltage reference input. An external 1.2 V voltage reference must be connected to this pin. The use of an external resistor divider network is not recommended. A 0.1 μF decoupling ceramic capacitor should be connected between V_{REF} and V_{AA}.
V_{AA}	Analog power supply (5 V ± 5%). All V_{AA} pins on the ADV7120 must be connected.
GND	Ground. All GND pins must be connected.

6

TERMINOLOGY

Blanking Level
The level separating the $\overline{\text{SYNC}}$ portion from the video portion of the waveform. Usually referred to as the front porch or back porch. At 0 IRE units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

Color Video (RGB)
This usually refers to the technique of combining the three primary colors of red, green and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs are required, one for each color.

Sync Signal ($\overline{\text{SYNC}}$)
The position of the composite video signal which synchronizes the scanning process.

Gray Scale
The discrete levels of video signal between reference black and reference white levels. An 8-bit DAC contains 256 different levels while a 6-bit DAC contains 64.

Raster Scan
The most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level
The maximum negative polarity amplitude of the video signal.

Reference White Level
The maximum positive polarity amplitude of the video signal.

Sync Level
The peak level of the $\overline{\text{SYNC}}$ signal.

Video Signal
That portion of the composite video signal which varies in gray scale levels between reference white and reference black. Also referred to as the picture signal, this is the portion which may be visually observed.

ANALOG DEVICES

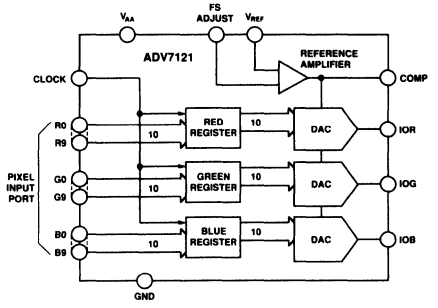
CMOS 80 MHz, Triple 10-Bit Video DACs

ADV7121/ADV7122

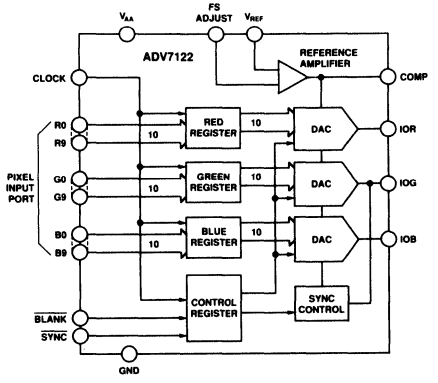
FEATURES
80 MHz Pipelined Operation
Triple 10-Bit D/A Converters
RS-343A/RS-170 Compatible Outputs
TTL Compatible Inputs
+5 V CMOS Monolithic Construction
40-Pin DIP Package (ADV7121)
44-Pin PLCC Package (ADV7122)
Power Dissipation: 400 mW

APPLICATIONS
High Definition Television (HDTV)
High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Video Signal Reconstruction
Direct Digital Synthesis (DDS)

SPEED GRADES
80 MHz
50 MHz
30 MHz



ADV7121 Functional Block Diagram



ADV7122 Functional Block Diagram

GENERAL DESCRIPTION

The ADV7121/ADV7122 (ADV®) is a video speed, digital-to-analog converter on a single monolithic chip. The part is specifically designed for high resolution color graphics and video systems including high definition television (HDTV). It consists of three, high speed, 10-bit, video D/A converters (RGB), a standard TTL input interface and high impedance, analog output, current sources.

The ADV7121/ADV7122 has three separate, 10-bit, pixel input ports, one each for red, green and blue video data. A single +5 V power supply, an external 1.23 V reference and pixel clock input is all that is required to make the part operational. The ADV7122 has additional video control signals, composite $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$.

The ADV7121/ADV7122 is capable of generating RGB video output signals which are compatible with RS-343A, RS-170 and most proposed production system HDTV video standards, including SMPTE 240M.

The ADV7121/ADV7122 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation. The ADV7121 is packaged in a 0.6", 40-pin plastic DIP package. The ADV7122 is packaged in a 44-pin plastic leaded (J-lead) chip carrier, PLCC.

PRODUCT HIGHLIGHTS

1. Fast video refresh rate, 80 MHz.
2. Guaranteed monotonic to 10 bits. Ten bits of resolution allows for implementation of linearization functions such as gamma correction and contrast enhancement.
3. Compatible with a wide variety of high resolution color graphics systems including RS-343A/RS-170 and the proposed SMPTE 240M standard for HDTV.

6

ADV7121—SPECIFICATIONS (V_{AA} = +5 V ± 5%; V_{REF} = +1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 560 Ω. All Specifications T_{min} to T_{max}[1] unless otherwise noted.)

Parameter	J Version	K Version	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution (Each DAC)	10	10	Bits	
Accuracy (Each DAC)				
Integral Nonlinearity, INL	±3	±2	LSB max	
Differential Nonlinearity, DNL	+1.5/−1.0	±1	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	±5	% Gray Scale max	Max Gray Scale Current = (V_{REF}* 7,969/ R_{SET}) mA
Coding			Binary	
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2	2	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current, I_{IN}	±1	±1	μA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}[2]	10	10	pF max	
ANALOG OUTPUTS				
Gray Scale Current Range	15	15	mA min	
	22	22	mA max	
Output Current				
White Level	16.74	16.74	mA min	Typically 17.62 mA
	18.50	18.50	mA max	
Black Level	0	0	μA min	Typically 5 μA
	50	50	μA max	
LSB Size	17.28	17.28	μA typ	
DAC to DAC Matching	5	5	% max	Typically 2%
Output Compliance, V_{OC}	−1	−1	V min	
	+1.4	+1.4	V max	
Output Impedance, R_{OUT}[2]	100	100	kΩ typ	
Output Capacitance, C_{OUT}[2]	30	30	pF max	I_{OUT} = 0 mA
VOLTAGE REFERENCE				
Voltage Reference Range, V_{REF}	1.14/1.26	1.14/1.26	V min/V max	V_{REF} = 1.235 V for Specified Performance
Input Current, I_{VREF}	−5	−5	mA typ	
POWER REQUIREMENTS				
V_{AA}	5	5	V nom	
I_{AA}	125	125	mA max	Typically 80 mA: 80 MHz Parts
	100	100	mA max	Typically 70 mA: 50 MHz & 35 MHz Parts
Power Supply Rejection Ratio[2]	0.5	0.5	% / % max	Typically 0.12 %/%: f = 1 kHz, COMP = 0.1 μF
Power Dissipation	625	625	mW max	Typically 400 mW: 80 MHz Parts
	500	500	mW max	Typically 350 mW: 50 MHz & 35 MHz Parts
DYNAMIC PERFORMANCE				
Glitch Impulse[2, 3]	50	50	pV secs typ	
DAC Noise[2, 3, 4]	200	200	pV secs typ	
Analog Output Skew	2	2	ns max	Typically 1 ns

NOTES

[1]Temperature Range (T_{min} to T_{max}): 0 to +70°C.

[2]Sample tested at 25°C to ensure compliance.

[3]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. See timing notes in Figure 1.

[4]This includes effects due to clock and data feedthrough as well as RGB analog crosstalk.

Specifications subject to change without notice.

ADV7122—SPECIFICATIONS

(V_{AA} = +5 V ± 5%; V_{REF} = +1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 560 Ω. All Specifications T_{min} to T_{max}[1] unless otherwise noted.)

Parameter	J Version	K Version	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution (Each DAC)	10	10	Bits	
Accuracy (Each DAC)				
Integral Nonlinearity, INL	±3	±2	LSB max	
Differential Nonlinearity, DNL	+1.5/−1.0	±1	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	±5	% Gray Scale max	Max Gray Scale Current: IOG = (V_{REF}*12.082/R_{SET}) mA
				IOR, IOB = (V_{REF}*8,627/R_{SET}) mA
Coding			Binary	
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2	2	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current, I_{IN}	±1	±1	μA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}[2]	10	10	pF max	
ANALOG OUTPUTS				
Gray Scale Current Range	15	15	mA min	
	22	22	mA max	
Output Current				
White Level Relative to Blank	17.69	17.69	mA min	Typically 19.05 mA
	20.40	20.40	mA max	
White Level Relative to Black	16.74	16.74	mA min	Typically 17.62 mA
	18.50	18.50	mA max	
Black Level Relative to Blank	0.95	0.95	mA min	Typically 1.44 mA
	1.90	1.90	mA max	
Black Level on IOR, IOB	0	0	μA min	Typically 5 μA
	50	50	μA max	
Black Level on IOG	6.29	6.29	mA min	Typically 7.62 mA
	9.5	9.5	mA max	
Sync Level on IOG	0	0	μA min	Typically 5 μA
	50	50	μA max	
LSB Size	17.28	17.28	μA typ	
DAC to DAC Matching	5	5	% max	Typically 2%
Output Compliance, V_{OC}	−1	−1	V min	
	+1.4	+1.4	V max	
Output Impedance, R_{OUT}[2]	100	100	kΩ typ	
Output Capacitance, C_{OUT}[2]	30	30	pF max	I_{OUT} = 0 mA
VOLTAGE REFERENCE				
Voltage Reference Range, V_{REF}	1.14/1.26	1.14/1.26	V min/V max	V_{REF} = 1.235 V for Specified Performance
Input Current, I_{VREF}	−5	−5	mA typ	
POWER REQUIREMENTS				
V_{AA}	5	5	V nom	
I_{AA}	125	125	mA max	Typically 80 mA: 80 MHz Parts
	100	100	mA max	Typically 70 mA: 50 MHz & 35 MHz Parts
Power Supply Rejection Ratio[2]	0.5	0.5	%/% max	Typically 0.12%/%: f = 1 kHz, COMP = 0.01 μF
Power Dissipation	625	625	mW max	Typically 400 mW: 80 MHz Parts
	500	500	mW max	Typically 350 mW: 50 MHz & 35 MHz Parts
DYNAMIC PERFORMANCE				
Glitch Impulse[2, 3]	50	50	pV secs typ	
DAC Noise[2, 3, 4]	200	200	pV secs typ	
Analog Output Skew	2	2	ns max	Typically 1 ns

NOTES

[1]Temperature Range (T_{min} to T_{max}): 0 to +70°C.

[2]Sample tested at 25°C to ensure compliance.

[3]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. See timing notes in Figure 1.

[4]This includes effects due to clock and data feedthrough as well as RGB analog crosstalk.

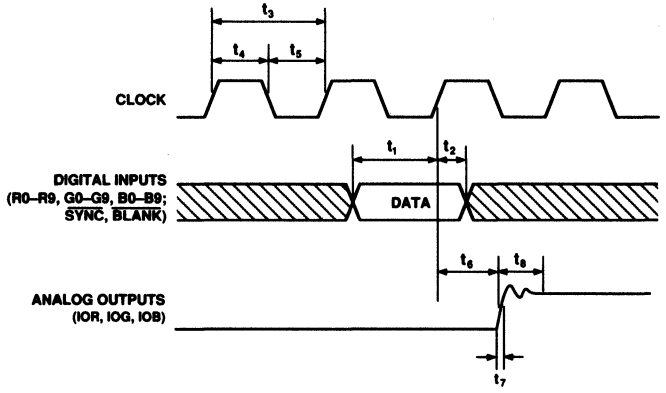
Specifications subject to change without notice.

6

TIMING CHARACTERISTICS[1] (V_{AA} = +5 V ± 5%; V_{REF} = +1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 560 Ω. All Specifications T_{min} to T_{max}[2] unless otherwise noted.)

Parameter	80 MHz Versions	50 MHz Versions	30 MHz Versions	Units	Conditions/Comments
fmax	80	50	30	MHz max	Clock Rate
t_1	3	6	8	ns min	Data & Control Setup Time
t_2	2	2	2	ns min	Data & Control Hold Time
t_3	12.5	20	33.3	ns min	Clock Cycle Time
t_4	4	7	9	ns min	Clock Pulse Width High Time
t_5	4	7	9	ns min	Clock Pulse Width Low Time
t_6	30	30	30	ns max	Analog Output Delay
	20	20	20	ns typ	
t_7	3	3	3	ns max	Analog Output Rise/Fall Time
t_8[3]	12	15	15	ns typ	Analog Output Transition Time

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. See timing notes in Figure 1.
[2]Temperature range (T_{min} to T_{max}): 0 to +70°C.
[3]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.



NOTES
1. OUTPUT DELAY (t_6) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF THE CLOCK TO THE 50% POINT OF FULL-SCALE TRANSITION.
2. TRANSITION TIME (t_8) MEASURED FROM THE 50% POINT OF FULL-SCALE TRANSITION TO WITHIN 2% OF THE FINAL OUTPUT VALUE.
3. OUTPUT RISE/FALL TIME (t_7) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL-SCALE TRANSITION.
4. SYNC AND BLANK DIGITAL INPUTS ARE NOT PROVIDED ON THE ADV7121.

Figure 1. Video Input/Output Timing

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}	4.75	5.00	5.25	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts

ORDERING GUIDE

Model	Speed	Accuracy DNL	Accuracy INL	Temperature	Package Option[1]
ADV7121JN80	80 MHz	+1.5	±3	0°C to +70°C	N-40A
ADV7121JN50	50 MHz	+1.5	±3	0°C to +70°C	N-40A
ADV7121JN30	30 MHz	+1.5	±3	0°C to +70°C	N-40A
ADV7121KN80	80MHz	±1	±2	0°C to +70°C	N-40A
ADV7121KN50	50MHz	±1	±2	0°C to +70°C	N-40A
ADV7121KN30	30 MHz	±1	±2	0°C to +70°C	N-40A
ADV7122JP80	80 MHz	+1.5	±3	0°C to +70°C	P-44A[2]
ADV7122JP50	80 MHz	+1.5	±3	0°C to +70°C	P-44A[2]
ADV7122JP30	80 MHz	+1.5	±3	0°C to +70°C	P-44A[2]
ADV7122KP80	80 MHz	±1	±2	0°C to +70°C	P-44A[2]
ADV7122KP50	50 MHz	±1	±2	0°C to +70°C	P-44A[2]
ADV7122KP30	30 MHz	±1	±2	0°C to +70°C	P-44A[2]

NOTES
[1]N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.
[2]PLCC: Plastic Leaded Chip Carrier (J-lead).

ABSOLUTE MAXIMUM RATINGS*

V_{AA} to GND . . . . . +7 V
Voltage on Any Digital Pin . . . . . GND −0.5 V to V_{AA}+0.5 V
Ambient Operating Temperature (T_A) . . . . . 0 to +70°C
Storage Temperature (T_S) . . . . . −65°C to +150°C
Junction Temperature (T_J) . . . . . +175°C
Soldering Temperature (5 secs) . . . . . 220°C
Vapor Phase Soldering (1 minute) . . . . . 220°C
IOR, IOB, IOG to GND[1] . . . . . 0 V to V_{AA}

NOTES
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[1]Analog output short circuit to any power supply or common can be of an indefinite duration.

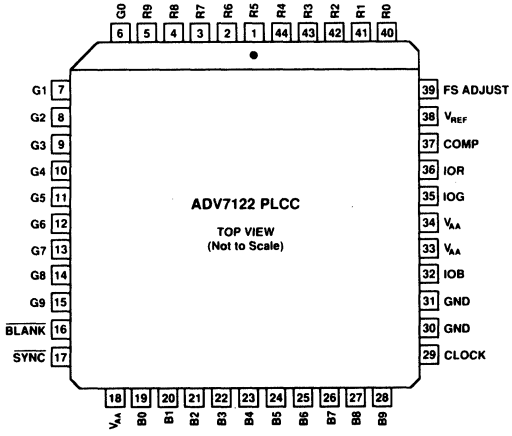
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

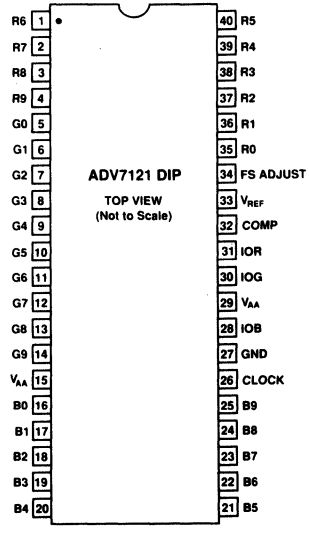
6

PIN CONFIGURATIONS

PLCC (P-44A) Package



DIP (N-40A) Package



PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{\text{BLANK}}$*	Composite blank control input (TTL compatible). A logic zero on this control input drives the analog outputs, IOR, IOB and IOG, to the blanking level. The $\overline{\text{BLANK}}$ signal is latched on the rising edge of CLOCK. While $\overline{\text{BLANK}}$ is a logical zero, the R0–R9, G0–G9 and R0–R9 pixel inputs are ignored.
$\overline{\text{SYNC}}$*	Composite sync control input (TTL compatible). A logical zero on the $\overline{\text{SYNC}}$ input switches off a 40 IRE current source. This is internally connected to the IOG analog output. $\overline{\text{SYNC}}$ does not override any other control or data input, therefore, it should only be asserted during the blanking interval. $\overline{\text{SYNC}}$ is latched on the rising edge of CLOCK. If sync information is not required on the green channel, the $\overline{\text{SYNC}}$ input should be tied to logical zero.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0–R9, G0–G9, B0–B9, $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ pixel and control inputs. It is typically the pixel clock rate of the video system. CLOCK should be driven by a dedicated TTL buffer.
R0–R9, G0–G9, B0–B9	Red, green and blue pixel data inputs (TTL compatible). Pixel data is latched on the rising edge of CLOCK. R0, G0 and B0 are the least significant data bits. Unused pixel data inputs should be connected to either the regular PCB power or ground plane.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable. All three current outputs should have similar output loads whether or not they are all being used.
FS ADJUST	Full-scale adjust control. A resistor (R_{SET}) connected between this pin and GND, controls the magnitude of the full-scale video signal. Note that the IRE relationships are maintained, regardless of the full-scale output current. The relationship between R_{SET} and the full-scale output current on IOG (assuming I_{SYNC} is connected to IOG) is given by: R_{SET} (Ω) = 12,082 × V_{REF} (V)/IOG (mA) The relationship between R_{SET} and the full-scale output current on IOR, IOG and IOB is given by: IOG* (mA) = 12,082 × V_{REF} (V)/R_{SET} (Ω) ($\overline{\text{SYNC}}$ being asserted) IOR, IOB (mA) = 8,628 × V_{REF} (V)/R_{SET} (Ω) The equation for IOG will be the same as that for IOR and IOB when $\overline{\text{SYNC}}$ is not being used, i.e., $\overline{\text{SYNC}}$ tied permanently low. For the ADV7121, all three analog output currents are as described by: IOR, IOG, IOB (mA) = 7,969 × V_{REF} (V)/R_{SET} (Ω)
COMP	Compensation pin. This is a compensation pin for the internal reference amplifier. A 0.1 μF ceramic capacitor must be connected between COMP and V_{AA}.
V_{REF}	Voltage reference input. An external 1.23V voltage reference must be connected to this pin. The use of an external resistor divider network is not recommended. A 0.1 μF decoupling ceramic capacitor should be connected between V_{REF} and V_{AA}.
V_{AA}	Analog power supply (5 V ± 5%). All V_{AA} pins on the ADV7121/ADV7122 must be connected.
GND	Ground. All GND pins must be connected.

*$\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ functions are not provided on the ADV7121.

TERMINOLOGY

Blanking Level
The level separating the $\overline{\text{SYNC}}$ portion from the video portion of the waveform. Usually referred to as the front porch or back porch. At 0 IRE units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

Color Video (RGB)
This usually refers to the technique of combining the three primary colors of red, green and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs are required, one for each color.

Sync Signal ($\overline{\text{SYNC}}$)
The position of the composite video signal which synchronizes the scanning process.

Gray Scale
The discrete levels of video signal between reference black and reference white levels. A 10-bit DAC contains 1024 different levels, while an 8-bit DAC contains 256.

Raster Scan
The most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level
The maximum negative polarity amplitude of the video signal.

Reference White Level
The maximum positive polarity amplitude of the video signal.

Sync Level
The peak level of the $\overline{\text{SYNC}}$ signal.

Video Signal
That portion of the composite video signal which varies in gray scale levels between reference white and reference black. Also referred to as the picture signal, this is the portion which may be visually observed.

CIRCUIT DESCRIPTION & OPERATION

The ADV7121/ADV7122 contains three 10-bit D/A converters, with three input channels, each containing a 10-bit register. Also integrated on board the part is a reference amplifier. CRT control functions $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ are integrated on board the ADV7122.

Digital Inputs
Thirty bits of pixel data (color information) R0–R9, G0–G9 and B0–B9 are latched into the device on the rising edge of each clock cycle. This data is presented to to the three 10-bit DACs and is then converted to three analog (RGB) output waveforms. See Figure 2.

The ADV7122 has two additional control signals, which are latched to the analog video outputs in a similar fashion. $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ are each latched on the rising edge of CLOCK to maintain synchronization with the pixel data stream.

The $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ functions allow for the encoding of these video synchronization signals onto the RGB video output. This is done by adding appropriately weighted current sources to the analog outputs, as determined by the logic levels on the $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ digital inputs. Figure 3 shows the analog output, RGB video waveform of the ADV7121/ADV7122 . The influence of $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ on the analog video waveform is illustrated.

Table I details the resultant effect on the analog outputs of $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$.

All these digital inputs are specified to accept TTL logic levels.

Clock Input
The CLOCK input of the ADV7121/ADV7122 is typically the pixel clock rate of the system. It is also known as the dot rate. The dot rate, and hence the required CLOCK frequency, will be determined by the on-screen resolution, according to the following equation:

$$\textit{Dot Rate} = \frac{(\textit{Horiz Res}) \times (\textit{Vert Res}) \times (\textit{Refresh Rate})}{(\textit{Retrace Factor})}$$

Horiz Res	=	Number of Pixels/Line.
Vert Res	=	Number of Lines/Frame.
Refresh Rate	=	Horizontal Scan Rate. This is the rate at which the screen must be refreshed, typically 60 Hz for a noninterlaced system or 30 Hz for an interlaced system.
Retrace Factor	=	Total Blank Time Factor. This takes into account that the display is blanked for a certain fraction of the total duration of each frame (e.g., 0.8).

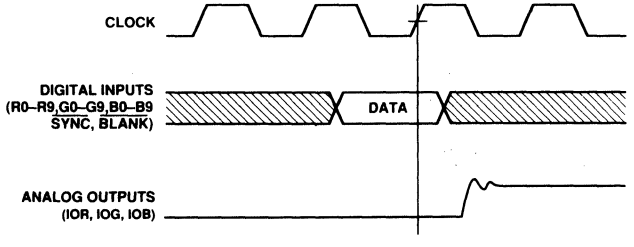


Figure 2. Video Data Input/Output

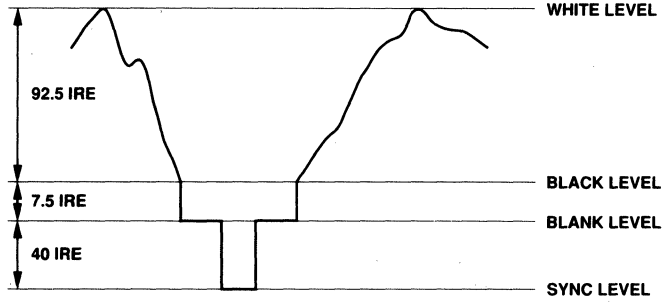
If we therefore have a graphics system with a 1024 × 1024 resolution, a noninterlaced 60 Hz refresh rate and a retrace factor of 0.8, then:

Dot Rate = 1024 × 1024 × 60/0.8
= 78.6 MHz

The required CLOCK frequency is thus 78.6 MHz.

All video data and control inputs are latched into the ADV7121/ADV7122 on the rising edge of CLOCK, as previously described in the "Digital Inputs" section. It is recommended that the CLOCK input to the ADV7121/ADV7122 be driven by a TTL buffer (e.g., 74F244).

RED, BLUE		GREEN	
mA	V	mA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0	0	7.62	0.286
		0	0



NOTES
1. OUTPUTS CONNECTED TO A DOUBLY TERMINATED 75Ω LOAD.
2. V_{REF} = 1.235V, R_{SET} = 560Ω .
3. RS-343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 3. RGB Video Output Waveform

Description	IOG (mA)[1]	IOR, IOB (mA)	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE LEVEL	26.67	19.05	1	1	3FFH
VIDEO	video + 9.05	video + 1.44	1	1	data
VIDEO to BLANK	video + 1.44	video + 1.44	0	1	data
BLACK LEVEL	9.05	1.44	1	1	00H
BLACK to BLANK	1.44	1.44	0	1	00H
BLANK LEVEL	7.62	0	1	0	xxH
SYNC LEVEL	0	0	0	0	xxH

NOTE
[1]Typical with full-scale IOG = 26.67 mA. V_{REF} = 1.235 V, R_{SET} = 560 Ω, I_{SYNC} connected to IOG.

Table Ia. Video Output Truth Table for the ADV7122

Description	IOR, IOG, IOB (mA)[1]	DAC Input Data
WHITE LEVEL	17.62	3FF
VIDEO	video	data
VIDEO to BLACK	video	data
BLACK LEVEL	0	00H

NOTE
[1]Typical with full-scale = 17.62 mA. V_{REF} = 1.235 V, R_{SET} = 560 Ω.

Table Ib. Video Output Truth Table for the ADV7121

Video Synchronization & Control

The ADV7122 has a single composite sync ($\overline{SYNC}$) input control. Many graphics processors and CRT controllers have the ability of generating horizontal sync (HSYNC), vertical sync (VSYNC) and composite $\overline{SYNC}$.

In a graphics system which does not automatically generate a composite $\overline{SYNC}$ signal, the inclusion of some additional logic circuitry will enable the generation of a composite $\overline{SYNC}$ signal.

The sync current is internally connected directly to the IOG output, thus encoding video synchronization information onto the green video channel. If it is not required to encode sync information onto the ADV7122, the $\overline{SYNC}$ input should be tied to logic low.

Reference Input

An external 1.23 V voltage reference is required to drive the ADV7121/ADV7122. The AD589 from Analog Devices is an ideal choice of reference. It is a two-terminal, low cost, temperature compensated bandgap voltage reference which provides a fixed 1.23 V output voltage for input currents between 50 μA and 5 mA. Figure 4 shows a typical reference circuit connection diagram. The voltage reference gets its current drive from the ADV7121/ADV7122's V_{AA} through an on-board 1 kΩ resistor to the V_{REF} pin. A 0.1 μF ceramic capacitor is required between the COMP pin and V_{AA}. This is necessary so as to provide compensation for the internal reference amplifier.

A resistance R_{SET} connected between FS ADJUST and GND determines the amplitude of the output video level according to Equations 1 and 2 for the ADV7122 and Equation 3 for the ADV7121:

$$IOG^{*}\ (mA) = 12{,}082 \times V_{REF}\ (V)/R_{SET}\ (\Omega) \quad \ldots\ldots\ldots\ (1)$$

$$IOR,\ IOB\ (mA) = 8{,}628 \times V_{REF}\ (V)/R_{SET}\ (\Omega) \quad \ldots\ldots\ (2)$$

$$IOR,\ IOG,\ IOB\ (mA) = 7{,}969 \times V_{REF}\ (V)/R_{SET}\ (\Omega) \quad \ldots\ (3)$$

**Only applies to the ADV7122 when $\overline{SYNC}$ is being used. If $\overline{SYNC}$ is not being encoded onto the green channel, then Equation 1 will be similar to Equation 2.*

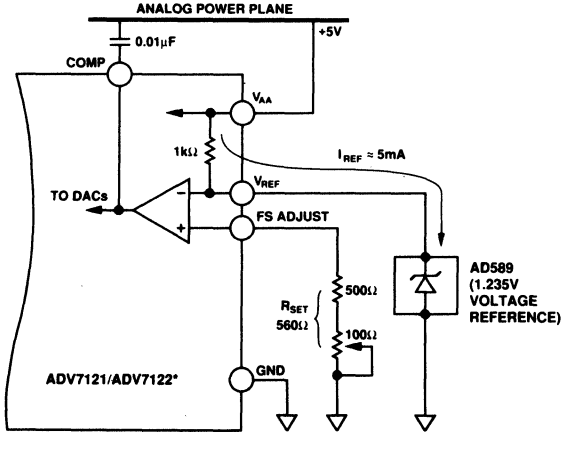


Figure 4. Reference Circuit

Using a variable value of R_{SET}, as shown in Figure 4, allows for accurate adjustment of the analog output video levels. Use of a fixed 560 Ω R_{SET} resistor yields the analog output levels as quoted in the specification page. These values typically correspond to the RS-343A video waveform values as shown in Figure 3.

D/A Converters

The ADV7121/ADV7122 contains three matched 10-bit D/A converters. The DACs are designed using an advanced, high speed, segmented architecture. The bit currents corresponding to each digital input are routed to either the analog output (bit = "1") or GND (bit = "0") by a sophisticated decoding scheme. As all this circuitry is on one monolithic device, matching between the three DACs is optimized. As well as matching, the use of identical current sources in a monolithic design guarantees monotonicity and low glitch. The on-board operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

Analog Outputs

The ADV7121/ADV7122 has three analog outputs, corresponding to the red, green and blue video signals.

The red, green and blue analog outputs of the ADV7121/ADV7122 are high impedance current sources. Each one of these three RGB current outputs is capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable. Figure 5a shows the required configuration for each of the three RGB outputs connected into a doubly terminated 75 Ω load. This arrangement will develop RS-343A video output voltage levels across a 75 Ω monitor.

A suggested method of driving RS-170 video levels into a 75 Ω monitor is shown in Figure 5b. The output current levels of the DACs remain unchanged, but the source termination resistance, Z_S, on each of the three DACs is increased from 75 Ω to 150 Ω.

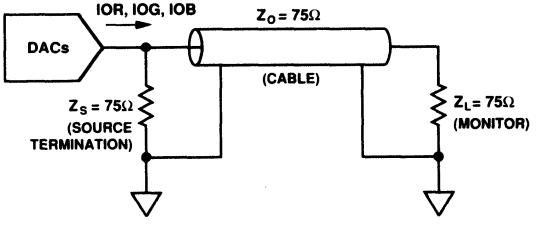


Figure 5a. Analog Output Termination for RS-343A

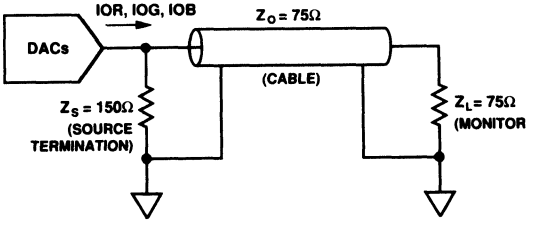


Figure 5b. Analog Output Termination for RS-170

More detailed information regarding load terminations for various output configurations, including RS-343A and RS-170, is available in an Application Note entitled "Video Formats & Required Load Terminations" available from Analog Devices, publication no. E1228–15–1/89.

Figure 3 shows the video waveforms associated with the three RGB outputs driving the doubly terminated 75 Ω load of Figure 5a. As well as the gray scale levels, Black Level to White Level, the diagram also shows the contributions of $\overline{SYNC}$ and $\overline{BLANK}$ for the ADV7122. These control inputs add appropriately weighted currents to the analog outputs, producing the specific output level requirements for video applications. Table Ia details how the $\overline{SYNC}$ and $\overline{BLANK}$ inputs modify the output levels.

Gray Scale Operation

The ADV7121/ADV7122 can be used for stand-alone, gray scale (monochrome) or composite video applications (i.e., only one channel used for video information). Any one of the three channels, RED, GREEN or BLUE can be used to input the digital video data. The two unused video data channels should be tied to logical zero. The unused analog outputs should be terminated with the same load as that for the used channel. In other words, if the red channel is used and IOR is terminated with a doubly-terminated 75 Ω load (37.5 Ω), IOB and IOG should be terminated with 37.5 Ω resistors. See Figure 6.

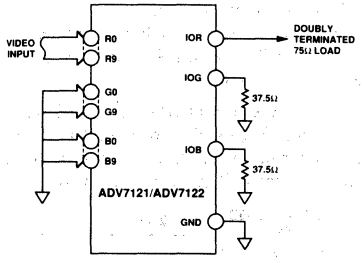


Figure 6. Input and Output Connections for Stand-Alone Gray Scale or Composite Video

Video Output Buffers

The ADV7121/ADV7122 is specified to drive transmission line loads, which is what most monitors are rated as. The analog output configurations to drive such loads are described in the Analog Interface section and illustrated in Figure 5. However, in some applications it may be required to drive long "transmission line" cable lengths. Cable lengths greater than 10 meters can attenuate and distort high frequency analog output pulses. The inclusion of output buffers will compensate for some cable distortion. Buffers with large full power bandwidths and gains between 2 and 4 will be required. These buffers will also need to be able to supply sufficient current over the complete output voltage swing. Analog Devices produces a range of suitable op amps for such applications. These include the AD84x series of monolithic op amps. In very high frequency applications (80 MHz), the AD9617 is recommended. More information on line driver buffering circuits is given in the relevant op amp data sheets.

Use of buffer amplifiers also allows implementation of other video standards besides RS-343A and RS-170. Altering the gain components of the buffer circuit will result in any desired video level.

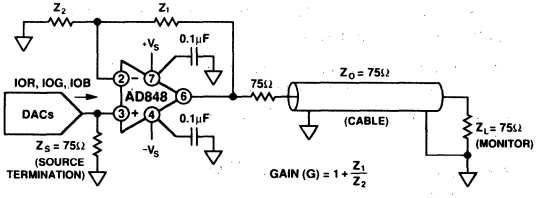


Figure 7. AD848 As an Output Buffer

PC Board Layout Considerations

The ADV7121/ADV7122 is optimally designed for lowest noise performance, both radiated and conducted noise. To complement the excellent noise performance of the ADV7121/ADV7122 it is imperative that great care be given to the PC board layout. Figure 8 shows a recommended connection diagram for the ADV7121/ADV7122.

The layout should be optimized for lowest noise on the ADV7121/ADV7122 power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The ADV7121/ADV7122 and associated analog circuitry, should have a separate ground plane referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 8. This bead should be located as close as possible (within 3 inches) to the ADV7121/ADV7122.

The analog ground plane should encompass all ADV7121/ADV7122 ground pins, voltage reference circuitry, power supply bypass circuitry, the analog output traces and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces, excluding the ground pins, leading up to the ADV7121/ADV7122.

Power Planes

The PC board layout should have two distinct power planes, one for analog circuitry and one for digital circuitry. The analog power plane should encompass the ADV7121/ADV7122 (V_{AA}) and all associated analog circuitry. This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead, as illustrated in Figure 8. This bead should be located within three inches of the ADV7121/ADV7122.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV7121/ADV7122 power pins, voltage reference circuitry and any output amplifiers.

The PCB power and ground planes should not overlay portions of the analog power plane. Keeping the PCB power and ground planes from overlaying the analog power plane will contribute to a reduction in plane-to-plane noise coupling.

Supply Decoupling

Noise on the analog power plane can be further reduced by the use of multiple decoupling capacitors (see Figure 8).

Optimum performance is achieved by the use of 0.1μF ceramic capacitors. Each of the two groups of V_{AA} should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

It is important to note that while the ADV7121/ADV7122 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise. A dc power supply filter (Murata BNX002) will provide EMI suppression between the switching power supply and the main PCB. Alternatively, consideration could be given to using a three terminal voltage regulator.

Digital Signal Interconnect

The digital signal lines to the ADV7121/ADV7122 should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.

Due to the high clock rates used, long clock lines to the ADV7121/ADV7122 should be avoided so as to minimize noise pickup.

Any active pull-up termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

Analog Signal Interconnect

The ADV7121/ADV7122 should be located as close as possible to the output connectors thus minimizing noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, thereby maximizing the high frequency power supply rejection.

For optimum performance, the analog outputs should each have a source termination resistance to ground of 75 Ω (doubly terminated 75 Ω configuration). This termination resistance should be as close as possible to the ADV7121/ADV7122 so as to minimize reflections.

Additional information on PCB design is available in an application note entitled "Design and Layout of a Video Graphics System for Reduced EMI." This application note is available from Analog Devices, publication no. E1309–15–10/89.

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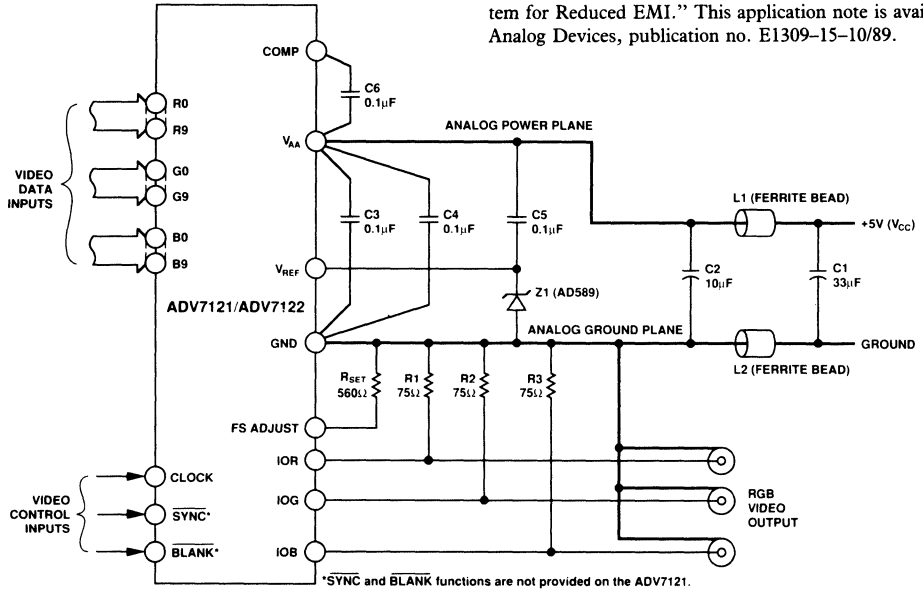


COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1	33μF TANTALUM CAPACITOR	
C2	10μF TANTALUM	
C3, C4, C5,C6	0.1μF CERAMIC CAPACITOR	
L1, L2	FERRITE BEAD	FAIR-RITE 2743001111 OR MURATA BL01/02/03
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF-55C
R_{SET}	560Ω 1% METAL FILM RESISTER	DALE CMF-55C
Z1	1.235V VOLTAGE REFERENCE	ANALOG DEVICES AD589JH

Figure 8. ADV7121/ADV7122 Typical Connection Diagram and Component List

CMOS Continuous Edge Graphics RAM-DACs (CEG/DACs)

ADV7141/ADV7146/ADV7148*

FEATURES

Proprietary Antialiasing Function
Dejagging of Lines, Arcs, Circles, Fonts, etc.
Effective 24-Bit True Color Performance
Dynamic Palette Load (DPL) Function
Plug-in Upgrade for Standard VGA RAM-DACs
ADV478/ADV471, ADV476 (ADV®) & Inmos 171/176†
Fully PS/2†, VGA† and 8514/A† Compatible
66 MHz Pipelined Operation
Triple 8-Bit/6-Bit D/A Converters
256 × 24 (18) Color Palette RAM
On-Board Gamma-Correction
On-Board Antisparkle Circuit
RS-343A/RS-170 Compatible Outputs
External Voltage or Current Reference
Standard MPU Interface
+5 V CMOS Monolithic Construction

APPLICATIONS

High Resolution Color Graphics
True Color Graphics
Digital Typography (Smooth Fonts)
Scientific Visualization
3-D Solids Modeling
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Desktop Publishing

AVAILABLE CLOCK RATES

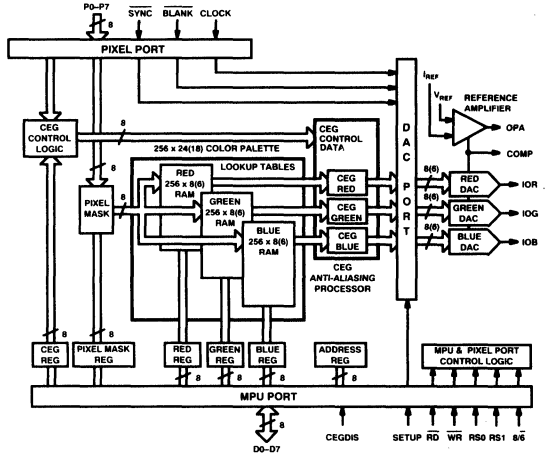
66 MHz
50 MHz
35 MHz

GENERAL DESCRIPTION

The Analog Devices' Continuous Edge Graphics† RAM-DAC (CEG†/DAC) dramatically improves image quality of standard analog color systems, by eliminating the jagged edges of computer generated images (antialiasing) and by providing an extended color palette for 3D modeling. This increased performance is achieved while at the same time maintaining full pin and functional compatibility with existing video RAM-DACs and color palettes used in VGA graphics systems.

The CEG/DAC implements a proprietary antialiasing or "dejagging" function. This is used to smooth the jagged edges associated with lines, circles and other nonrectangular objects displayed on a regular CRT screen. The part also allows for the effective display of 24-bit true color images on a standard 8-bit system, without the requirement of increased memory. More than 740,000 colors can be simultaneously displayed on an 8-bit/pixel system as against the 256 colors normally associated with 8-bit/pixel systems. This is achieved by a combination of the antialiasing function and a unique dynamic palette load

FUNCTIONAL BLOCK DIAGRAM



(DPL) feature. DPL allows for color palette writes (color alterations) during a single frame image.

The CEG/DAC combines a color lookup table (CLUT), three matched video speed computational units and associated control logic as well as three digital-to-analog converters (DACs). These all combine to significantly enhance the video image display quality of standard 8-bit/pixel graphics systems.

The ADV7148 and ADV7141 are pin and functional compatible with the ADV478 and ADV471, with the exception that the ADV7148 and the ADV7141 do not contain the overlay palette. The ADV7146 is pin and functional compatible with the ADV476 and the Inmos IMSG171/176.

CEG requires two closely connected components—the CEG/DAC chip and the software driver. Conventional antialiasing schemes are implemented entirely in software and operate on the pixel data in the graphics pipeline, resulting in a significant speed performance penalty. In contrast, the CEG software driver takes application software information and encodes the frame buffer with a sequence of data and commands for the CEG/DAC. The CEG/DAC hardware performs all of the antialiasing calculations. In this way, the visual benefits of antialiased graphics are provided with a minimal increase in software overhead.

*Protected by U.S. Patent Nos. 4,482,893 and 4,704,605.
†Inmos is a trademark of Inmos Ltd.
Personal System/2, VGA and 8514/A are trademarks of International Business Machines Corp.
Edsun Continuous Edge Graphics and CEG are registered trademarks of Edsun Laboratories, Inc.
ADV is a registered trademark of Analog Devices, Inc.

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ADV7141/ADV7146/ADV7148—SPECIFICATIONS

(V_{AA}[1] = 5 V; SETUP = 8/$\overline{6}$ = V_{AA}; V_{REF} = 1.235 V (ADV7148/ADV7141); I_{REF} = −8.39 mA (ADV7146); R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 147 Ω. All Specifications T_{min} to T_{max}[2] unless otherwise noted.)

Parameter	All Versions	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution (Each DAC)	8	Bits	
Accuracy (Each DAC)			
Integral Nonlinearity[3]	±1 (±1/2)	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	% Gray Scale	
Coding		Binary	
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±1	μA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}	7	pF max	f = 1 MHz, V_{IN} = 2.4 V
DIGITAL OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 400 μA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 3.2 mA
Floating-State Leakage Current	50	μA max	
Floating-State Leakage Capacitance	7	pF max	
ANALOG OUTPUTS			
Gray Scale Current Range	20	mA max	
Output Current			
White Level Relative to Blank/Black	17.4/20.40	mA min/mA max	Typically 19.05 mA
White Level Relative to Black[4]	16.5/18.50	mA min/mA max	Typically 17.62 mA, SETUP = V_{AA}
Black Level Relative to Blank[4]	0.95	mA min	Typically 1.44 mA, SETUP = V_{AA}
(Pedestal = 7.5 IRE)	1.90	mA max	
Black Level Relative to Blank	0	μA min	Typically 5 μA, SETUP = GND
(Pedestal = 0 IRE)	50	μA max	
Blank Level[4]	6.29	mA min	Typically 7.62 mA
(Sync Enabled)	8.96	mA max	
Blank Level	0	μA min	Typically 5 μA
(Sync Disabled)	50	μA max	
Sync Level[4]	0	μA min	Typically 5 μA
	50	μA max	
LSB size	69.1	μA typ	
DAC to DAC Matching	5	% max	Typically 2%
Output Compliance, V_{OC}	0/+1.5	V min/V max	
Output Impedance, R_{OUT}	10	kΩ typ	
Output Capacitance, C_{OUT}	30	pF max	
VOLTAGE REFERENCE			ADV7148 & ADV7141 Only
Voltage Reference Range	1.14/1.26	V min/V max	
Input Current, I_{VREF}	10	μA typ	
CURRENT REFERENCE			ADV7146 Only
Input Current (I_{REF}) Range	−3/−10	mA min/mA max	
Voltage at I_{REF}	V_{CC} − 3/V_{CC}	V min/max	
POWER SUPPLY			
Supply Voltage, V_{AA}	4.75/5.25	V min/V max	66 MHz Parts
	4.50/5.50	V min/V max	50 & 35 MHz Parts
Supply Current, I_{AA}	350	mA max	Typically 200 mA
Power Supply Rejection Ratio	0.5	%/% max	f = 1 kHz, COMP = 0.1 μF
DYNAMIC PERFORMANCE			
Clock and Data Feedthrough[5, 6]	−30	dB typ	
Glitch Impulse[5, 6]	75	pV secs typ	
DAC to DAC Crosstalk[7]	−23	dB typ	

NOTES

[1]±5% for 66 MHz parts; ±10% for 50 MHz & 35 MHz parts.

[2]Temperature range (T_{min} to T_{max}): 0 to +70°C.

[3]Tested to 8-bit linearity (tested to 6-bit linearity, ADV7146 only).

[4]ADV7141 and ADV7148 only.

[5]Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. Glitch impulse includes clock and data feedthrough.

[6]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured at the 10% and 90% points. Timing reference points at 50% for inputs and outputs.

[7]DAC to DAC crosstalk is measured by holding one DAC high while the other two are making low to high and high to low transitions.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{AA}[2] = 5 V; SETUP = 8/$\overline{6}$ = V_{AA}; V_{REF} = 1.235 V (ADV7148/ADV7141); I_{REF} = −8.39 mA (ADV7146); R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 147 Ω. All Specifications T_{min} to T_{max}[3] unless otherwise noted.)

Parameter	66 MHz Version	50 MHz Version	35 MHz Version	Units	Conditions/Comments
f_{max}	66	50	35	MHz	Clock Rate
t_1	10	10	15	ns min	RS0–RS1 Setup Time
t_2	10	10	15	ns min	RS0–RS1 Hold Time
t_3[4]	2	2	2	ns min	$\overline{RD}$ Asserted to Data Bus Driven
t_4[4]	40	40	40	ns max	$\overline{RD}$ Asserted to Data Valid
t_5[5]	20	20	20	ns max	$\overline{RD}$ Negated to Data Bus 3-Stated
t_6[5]	5	5	5	ns min	Read Data Hold Time
t_7	10	10	15	ns min	Write Data Setup Time
t_8	15	15	15	ns min	Write Data Hold Time
t_9	50	50	50	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width Low
t_{10}	6 × t_{13}	6 × t_{13}	6 × t_{13}	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width High
t_{11}	3	3	4	ns min	Pixel & Control Setup Time
t_{12}	3	3	4	ns min	Pixel & Control Hold Time
t_{13}	15	20	28	ns min	Clock Cycle Time
t_{14}	5	6	7	ns min	Clock Pulse Width High Time
t_{15}	5	6	9	ns min	Clock Pulse Width Low Time
t_{16}	30	30	30	ns max	Analog Output Delay
t_{17}	3	3	3	ns typ	Analog Output Rise/Fall Time
t_{18}[6]	13	20	28	ns max	Analog Output Settling Time
t_{SK}	2	2	2	ns max	Analog Output Skew
t_{PD}					Pipeline Delay
Compatibility Mode	3 × t_{13}	3 × t_{13}	3 × t_{13}	ns min	
CEG Mode	6 × t_{13}	6 × t_{13}	6 × t_{13}	ns min	

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10 pF, D0–D7 output load ≤50 pF. See timing notes in Figure 2.
[2]±5% for 66 MHz parts; ±10% for 50 MHz & 35 MHz parts; t_{15} measured at V_{AA} = 5 V for 66 MHz parts.
[3]Temperature Range (T_{min} to T_{max}): 0 to +70°C.
[4]t_3 and t_4 are measured with the load circuit of Figure 3 and defined as the time required for an output to cross 0.4 V or 2.4 V.
[5]t_5 and t_6 are derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 3. The measured number is then extrapolated back to remove the effects of charging the 50 pF capacitor. This means that the times, t_5 and t_6, quoted in the timing characteristics are the true values for the device and as such are independent of external bus loading capacitances.
[6]Settling time does not include clock and data feedthrough.
Specifications subject to change without notice.

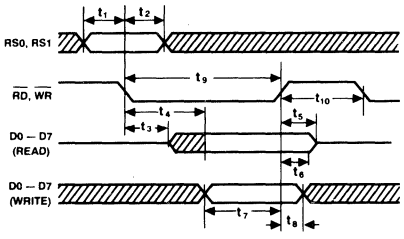


Figure 1. MPU Read/Write Timing

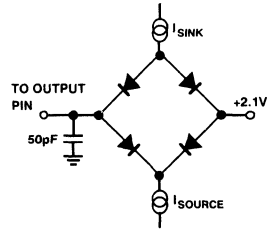


Figure 3. Load Circuit for Bus Access and Relinquish Time

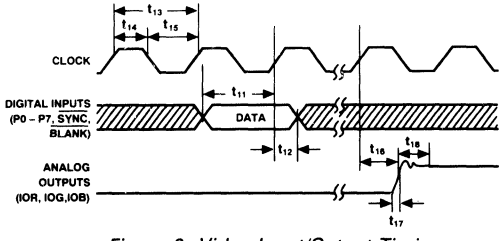


Figure 2. Video Input/Output Timing

NOTES
1. OUTPUT DELAY MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL SCALE TRANITION.
2. SETTLING TIME MEASURED FROM THE 50% POINT OF FULL SCALE TRANSITION TO THE OUTPUT REMAINING WITHIN ±1 LSB.
3. OUTPUT RISE/FALL TIME MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL SCALE TRANSITION.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
POWER SUPPLY	V_{AA}				
66 MHz Parts		4.75	5.00	5.25	Volts
50, 35 MHz Parts		4.5	5.00	5.5	Volts
AMBIENT OPERATING TEMPERATURE	T_A	0		+70	°C
OUTPUT LOAD	R_L		37.5		Ω
VOLTAGE REFERENCE CONFIGURATION					
Voltage Reference	V_{REF}	1.14	1.235	1.26	Volts
CURRENT REFERENCE CONFIGURATION					
I_{REF} CURRENT	I_{REF}				
STANDARD RS-343A		−3	−8.39	−10	mA
PS/2 Compatible		−3	−8.88	−10	mA

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

ABSOLUTE MAXIMUM RATINGS

V_{AA} to GND . . . . . −0.5 V to +7 V
Voltage on Any Digital Pin . . . . GND −0.5 V to V_{AA} + 0.5 V
Ambient Operating Temperature (T_A) . . . . . −55°C to +125°C
Storage Temperature (T_S) . . . . . −45°C to +125°C
Junction Temperature (T_J) . . . . . +175°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Vapor Phase Soldering (2 minutes) . . . . . +220°C
IOR, IOG, IOB to GND[1] . . . . . 0 V to V_{AA}

NOTES
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[1]Analog output short circuit to any power supply or common can be of an indefinite duration.

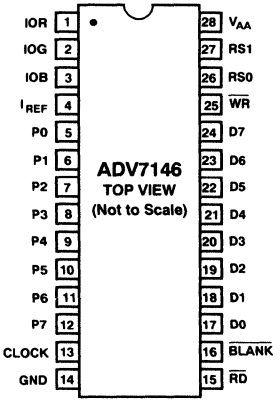
ORDERING GUIDE

Model[1]	Speed	Resolution[2]	Package Option[3, 4]
ADV7146KN66	66 MHz	6-Bit	N-28
ADV7146KN50	50 MHz	6-Bit	N-28
ADV7146KN35	35 MHz	6-Bit	N-28
ADV7141KP66	66 MHz	6-Bit	P-44A
ADV7141KP50	50 MHz	6-Bit	P-44A
ADV7141KP35	35 MHz	6-Bit	P-44A
ADV7148KP66	66 MHz	8-Bit/6-Bit	P-44A
ADV7148KP50	50 MHz	8-Bit/6-Bit	P-44A
ADV7148KP35	35 MHz	8-Bit/6-Bit	P-44A

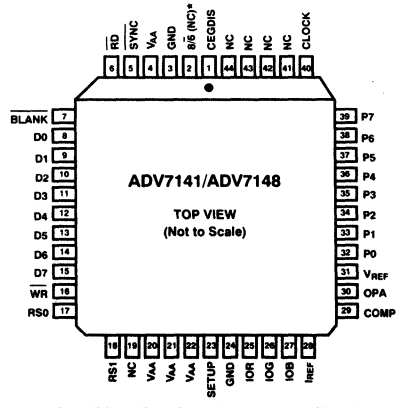
NOTES
[1]All devices are specified for 0°C to +70°C operation.
[2]Refers to "Compatibility Mode." In "CEG Mode," resolution for all options is 8 bits.
[3]28-pin DIP devices are packaged in 28-pin 0.6" plastic dual-in-line packages. 44-pin PLCC devices are packaged in 44-pin plastic leaded (J-lead) chip carriers.
[4]N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC). For outline information see Package Information section.

PIN CONFIGURATIONS

28-Pin DIP



44-Pin PLCC



NC = NO CONNECT; THESE PINS MAY BE LEFT UNCONNECTED
* (NC) INDICATES THE ADV7141 ONLY

PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{\text{BLANK}}$	Composite blank control input (TTL compatible). A Logic 0 drives the analog outputs to the blanking level. It is latched on the rising edge of CLOCK. When $\overline{\text{BLANK}}$ is a logical zero, the pixel and overlay inputs are ignored.
SETUP	Setup control input. Used to specify either a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = V_{AA}) blanking pedestal (ADV7141/ADV7148 only).
$\overline{\text{SYNC}}$	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs. $\overline{\text{SYNC}}$ does not override any other control or data input, therefore it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK (ADV7141/ADV7148 only).
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7, $\overline{\text{SYNC}}$, and $\overline{\text{BLANK}}$ inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable.
I_{REF}	Current Reference input (Current Reference configuration)/Full-scale adjust control (Voltage Reference configuration). When using an external voltage reference, a resistor (R_{SET}) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between R_{SET} and the full-scale output current on each output is: $$R_{SET}\,(\Omega) = K \times 1{,}000 \times V_{REF}\,(v)/I_{OUT}\,(mA)$$ K is defined in the table below, along with corresponding R_{SET} values for doubly terminated 75 Ω loads. When using an external current reference, the relationship between I_{REF} and the full-scale output current on each output is: $$I_{REF}\,(mA) = I_{OUT}\,(mA)/K$$
COMP	Compensation pin. If an external voltage reference is used, this pin should be connected to OPA. If an external current reference is used, this pin should be connected to I_{REF}. A 0.1 μF ceramic capacitor must always be used to bypass this pin to V_{AA} (ADV7141/ADV7148 *only*).
V_{REF}	Voltage reference input. If an external voltage reference is used, it must supply this input with a 1.2 V (typical) reference. If an external current reference is used, this pin should be left floating, except for the bypass capacitor. A 0.1 μF ceramic capacitor must always be used to decouple this input to V_{AA} (ADV7141/ADV7148 *only*).
OPA	Reference amplifier output. If an external voltage reference is used, this pin must be connected to COMP. When using an external current reference, this pin should be left floating (ADV7141/ADV7148 *only*).
V_{AA}	Analog power. All V_{AA} pins must be connected.
GND	Analog ground. All GND pins must be connected.
$\overline{\text{WR}}$	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of $\overline{\text{WR}}$, and RS0–RS1 are latched on the falling edge of $\overline{\text{WR}}$ during MPU write operations.
$\overline{\text{RD}}$	Read control input (TTL compatible). To read data from the device, $\overline{\text{RD}}$ must be a logical zero. RS0–RS1 are latched on the falling edge of $\overline{\text{RD}}$ during MPU read operations.
RS0, RS1	Register select inputs (TTL compatible). RS0–RS1 specify the type of read or write operation being performed.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
8/$\overline{6}$	8-bit/6-bit select input (TTL compatible). This input specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle. For 8-bit operation, D7 is the most significant bit (MSB) while for 6-bit operation, D5 is the MSB. D6 and D7 are ignored during 6-bit operation. All parts operate in 8-bit format while in CEG mode. 6-Bit operation is the default VGA mode on the ADV7146 and ADV7141. The 8/$\overline{6}$ bit must be set to Logical 0 on the ADV7148 to make it VGA compatible. If left unconnected, this pin remains in a low state.
CEGDIS	CEG disable (TTL compatible). Driving this pin active high disables all CEG functions. Software will detect a non-CEG device if this pin is high (ADV7141/ADV7148 only). If left unconnected, this pin remains in a low state.

Mode	Pedestal	K	R_{SET} (Ω)*
6-Bit	7.5 IRE	3.170	147
8-Bit	7.5 IRE	3.195	147
6-Bit	0 IRE	3.000	147
8-Bit	0 IRE	3.025	147

*For PS/2 applications (i.e., 0.7 V into 50 Ω with no SYNC), a 182 Ω R_{SET} resistor is recommended.

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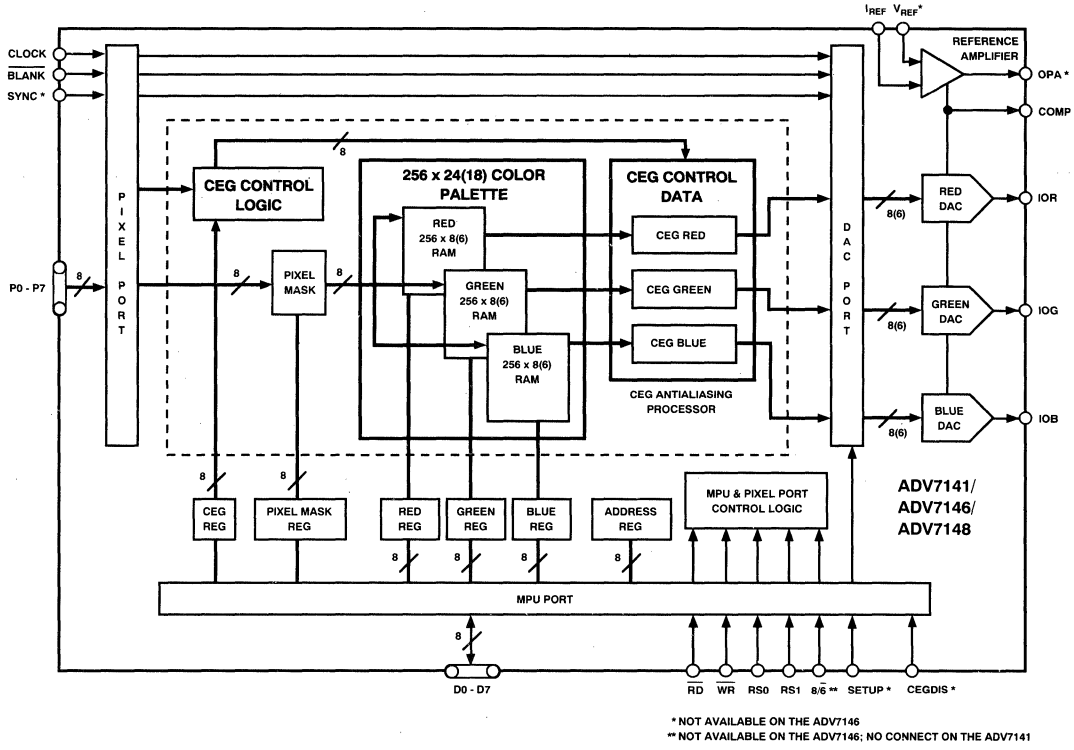

Functional Block Diagram of CEG/DAC

TERMINOLOGY

Blanking Level
The level separating the SYNC portion from the video portion of the waveform. Usually referred to as the front porch or back porch. At 0 IRE units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

Color Video (RGB)
This usually refers to the technique of combining the three primary colors of red, green and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs would be required, one for each color.

Composite Sync Signal (SYNC)
The position of the composite video signal which synchronizes the scanning process.

Composite Video Signal
The video signal with or without setup, plus the composite SYNC signal.

Gray Scale
The discrete levels of video signal between Reference Black and Reference White levels. An 8-bit DAC contains 256 different levels while a 6-bit DAC contains 64.

Raster Scan
The most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level
The maximum negative polarity amplitude of the video signal.

Reference White Level
The maximum positive polarity amplitude of the video signal.

Setup
The difference between the reference black level and the blanking level.

Sync Level
The peak level of the composite SYNC signal.

Video Signal
That portion of the composite video signal which varies in gray scale levels between Reference White and Reference Black. Also referred to as the picture signal, this is the portion which may be visually observed.

ANTIALIASING

Antialiasing is a technique used to smooth the jagged edges associated with lines, circles, and other nonrectangular objects represented on a CRT screen. Without antialiasing, each pixel (picture element) on a CRT is either "on" or "off." If the edge of a smooth shape passes through a pixel, the software is forced to approximate the edge as best it can (i.e., the pixel is "on" if more than half of the pixel is covered by the object). Even when a large number of pixels are used to represent an object, the eye quickly detects the series of "on" and "off" dots along the picture edge.

CEG achieves antialiasing by allowing the software to choose not only the discrete palette colors, but also a linear mix of those colors. For example, if only 1/3 of the pixel is covered by an object, the pixel would be displayed in the ratio of 33:67 between the object color and the background color. The eye perceives the new boundary as a completely smooth edge. The software driver defines the value of every pixel on a shape boundary, thereby dramatically increasing the perceived resolution of any computer display. By mixing colors in real time, the CEG/DAC can generate up to 800,000 simultaneously displayable colors without altering the contents of the standard 256 color look-up-table.

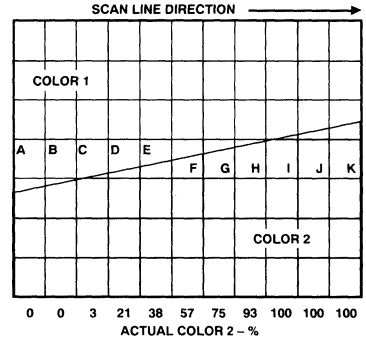

Figure 4. An Edge Crossing Scan Line

Figure 4 shows an enlargement of an object edge, with each square representing a screen pixel. An object is drawn in Color 2 on a background of Color 1—the actual colors are determined by the contents of the CLUT.

Without CEG, pixels labelled "A" through "E" will be displayed as Color 1 (Figure 5). Pixels are defined as Color 2 when more than 50% of the pixel is defined by that color, as shown in pixels "F" through "J." CEG blends colors to more closely approximate the intended color boundary as shown in Figure 6.

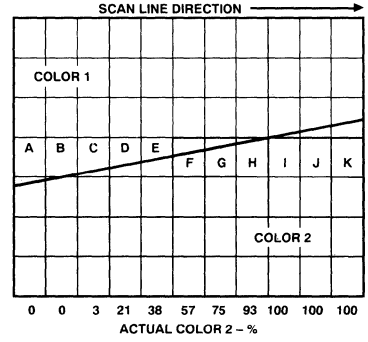

Figure 5. Traditional Pixel Coverage (Aliasing)

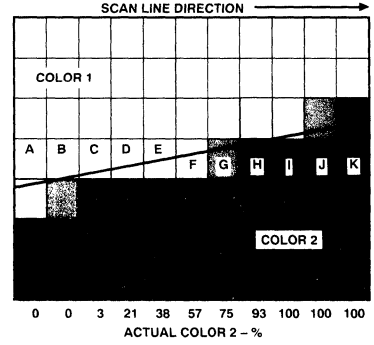

Figure 6. Dejagging or Antialiasing Using CEG

CEG FUNCTIONAL DESCRIPTION

CEG uses two data ports, a pixel port and an MPU data port. Three analog signals are produced which can directly drive the red, green, and blue inputs of a standard analog display monitor. The CEG/DAC consists of four major blocks: CEG logic, three 8-bit DACs, 256 × 24 lookup table RAM, and MPU control.

The CEG/DAC is a real-time signal processor which interprets data in the frame buffer as either colors, mix commands, or both. CEG uses a special sequence of lookup table accesses to enable and disable the CEG logic. The nonCEG mode allows full backward compatibility with current video palette products. The circuit is powered-up in nonCEG mode. CEG-aware software activates CEG modes and provides the advantages of alias-free images.

In nonCEG systems and software applications, the CEG/DAC behaves identical to normal palette DACs, providing complete physical and functional compatibility with all VGA compatible PCs. The CEG/DAC is available in packages compatible with the most popular palette DACs, including ADV471, ADV476, and ADV478 devices.

MPU Data Port

The MPU data port allows the system processor to access the color palette address register, color palette RAM and pixel mask register. Register selection is identical to the associated non-CEG, VGA compatible parts.

If the CEG device is operating in 8-bit mode, all 8 bits of the lookup table color data register are significant. In 6-bit modes, lookup table color data should be written and read back right-justified to/from D5–D0. During readback, in 6-bit modes, D6 and D7 are forced to Logic 0.

Pixel Port

Pixel information is latched into the CEG/DAC via the pixel port. For each clock cycle, the state of the P7–P0, BLANK and SYNC define the state of the DAC outputs.

Pixel port inputs are logically "AND"ed with the contents of the pixel mask register, for simple animation applications. The pixel mask register is accessed via the MPU interface. In general, the pixel mask register should be set to FFH for any of the CEG modes. See Appendix A for sample code to access the pixel mask register.

Two selectable features in CEG mode are "partial shading" and "pixel replication." Certain video controllers repeat each pixel twice in low resolution modes. In these modes, the pixel data is sampled every other CLOCK.

Systems which use only 4 bits per pixel should be connected to P3–P0, tying P7–P4 to ground. This type of system must use the "partial shading" Advanced-4 Method, which allows 8 colors (0–7) and 8 mix commands (8–15) in increments of 12%.

CEG PROGRAMMING BASICS

CEG Computation

When CEG is active, the CEG/DAC computes a real time weighted average on each of the primary colors which are read out of the palette RAM. This calculation, as represented by the generalized diagram of Figure 7, is expressed by the following equation:

$$P_{MC} = [(Color\ B \times Mix) + (Color\ A \times (31\text{–}Mix) + 16)]\ 131$$

where: P_{MC} = mixed color.

Or alternatively, it can be described by:

Mixed color = (ratio of previous color × previous color) + (ratio of new color × new color)

The mixed colors, one mixed color each for red, green and blue are then input to a gamma correction circuit. The output of this circuit drive each of the three RGB-DACs.

CEG MODES

Although there is one algorithm in the CEG/DAC, there are three ways of encoding the pixels in the frame buffer, namely, the Basic-8, Advanced-4 and Advanced-8 methods. These are described as follows:

Basic-8 16 drawing colors with 8 mixes plus explicit loading of new or old color (suitable for CAD type applications where few colors are needed).

Advanced-4 8 drawing colors with 8-mix shading (suitable for antialiasing in 4-bits/pixel systems).

Advanced-8 223 drawing colors with full 32-mix shading (suitable for 3-D solid modeling and true-color image rendition).

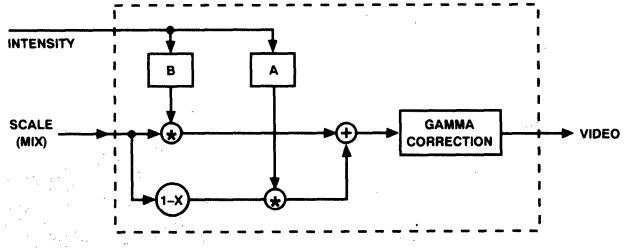

Figure 7. Block Diagram Representation of the CEG Algorithm

CIRCUIT DESCRIPTION

MPU Interface

As illustrated in the functional block diagram, the ADV7141/ADV7146/ADV7148 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM, pixel mask register and address register.

The RS0–RS1 select inputs specify whether the MPU is accessing the address register, color palette RAM, or pixel mask register, as illustrated in Table I. The 8-bit address register is used to address the color palette RAM.

Table I. Control Input Truth Table

RS1	RS0	Addressed by MPU
0	0	Address Register (RAM Write Mode)
1	1	Address Register (RAM Read Mode)
0	1	Color Palette RAM
1	0	Pixel Read Mask Register

To write color data, the MPU writes the address register with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (8 or 6 bits each of red, green and blue). During the blue write cycle, the three bytes of color information are concatenated into a 24-bit word (18-bit word for VGA backward compatible data). This color value is then written to the location in the palette RAM pointed to by the address register. The address register then increments and points to the next palette RAM location which the MPU may modify by simply writing another sequence of red, green and blue data. See Appendix A for sample code to write to the palette.

To read color data, the MPU loads the address register with the address of the color palette RAM location to be read. The MPU performs three successive read cycles (8 or 6 bits each of red, green, and blue), using RS0–RS1 to select the color palette RAM. Following the blue read cycle, the address register increments to the next location which the MPU may read by simply reading another sequence of red, green, and blue data. See Appendix A for sample code to read from the palette.

When accessing the color palette RAM, the address register resets to 00H following a blue read or write cycle to RAM location FFH.

For 8-bit operation, D0 is the LSB, and D7 is the MSB of color data.

For 6-bit operation, color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

See Compatibility section for details of 6/8-bit operation.

Table II. Address Register (ADDR) Operation

	Value	RS1	RS0	Addressed by MPU
ADDRa, b				
Counts Modulo 3	00			Red Value
	01			Green Value
	10			Blue Value
ADDR0–7				
Counts Binary	00H–FFH	0	1	Color Palette RAM

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. As only one pixel clock cycle is required to complete the transfer, the color palette RAM may be accessed at any time with no noticeable disturbance on the display screen.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table II. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register (ADDR0–7), incremented following a blue read or write cycle, are accessible to the MPU, and are used to address color palette RAM locations, as shown in Table II. ADDR0 is the LSB when the MPU is accessing the RAM. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Figure 1 illustrates the MPU read/write timing.

Frame Buffer Interface

The P0–P7 inputs are used to address the color palette RAM, as shown in Table III.

Table III. Pixel Input Truth Table (Pixel Read Mask Register = FFH)

P0–P7	Addressed by Frame Buffer
00H	Color Palette RAM Location 00H
01H	Color Palette RAM Location 01H
.	.
FFH	Color Palette RAM Location FFH

The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P0–P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides 24 bits (18 bits in compatibility mode) of color information to the three D/A converters.

(See Application Note entitled "Animation Using the Pixel Read Mask Register of the ADV47X Series of Video RAM-DACs" available from Analog Devices, Publication No. E1316-15-10/89.)

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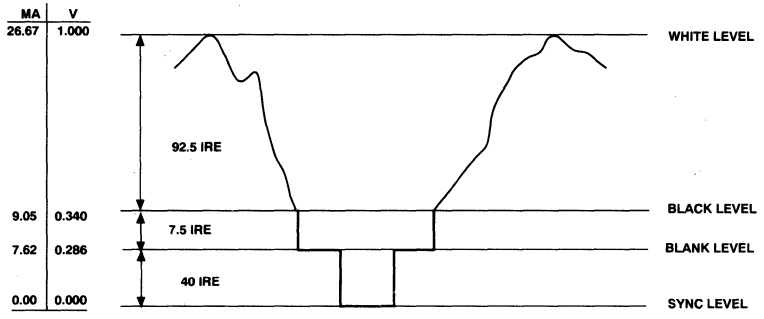


NOTES
1. CONNECTED WITH A 75 Ω DOUBLY TERMINATED LOAD.
2. EXTERNAL VOLTAGE OR CURRENT REFERENCE ADJUSTED FOR 26.67 mA FULL SCALE OUTPUT.
3. RS - 343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 8. ADV7141/ADV7148 RGB Video Output Waveform (SETUP = V_{AA})

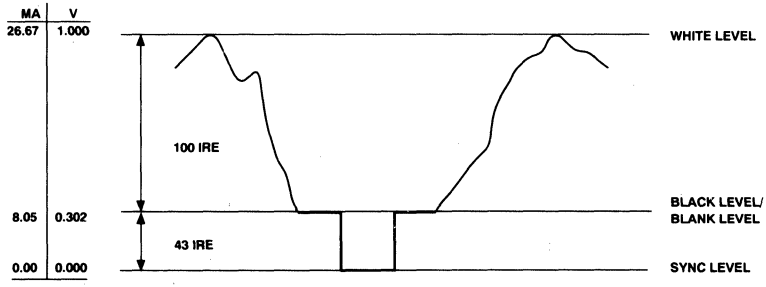
Table IV. ADV7141/ADV7148 RGB Video Output Truth Table (SETUP = V_{AA})

Description	I_{OUT} (mA)[1]	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE	26.67	1	1	FFH
DATA	Data + 9.05	1	1	Data
DATA-SYNC	Data + 1.44	0	1	Data
BLACK	9.05	1	1	00H
BLACK-SYNC	1.44	0	1	00H
BLANK	7.62	1	0	xxH
SYNC	0	0	0	xxH

NOTES
[1]Typical with full-scale IOG = 26.67 mA.
External voltage or current reference adjusted for 26.67 mA full-scale output.

The $\overline{SYNC}$ and $\overline{BLANK}$ inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 8, 9 and 10. Tables IV, V and VI detail how the $\overline{SYNC}$ and $\overline{BLANK}$ inputs modify the output levels.

The SETUP input, on the ADV7141 and ADV7148, is used to specify whether a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = V_{AA}) blanking pedestal is to be used.



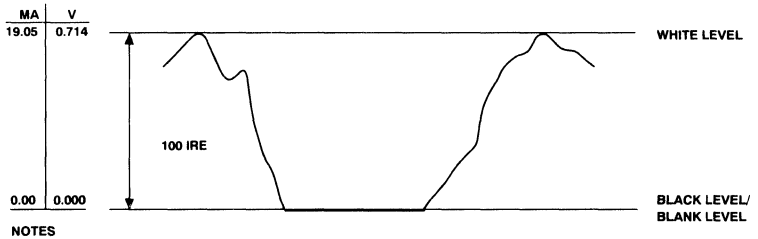
NOTES
1. CONNECTED WITH A 75 Ω DOUBLY TERMINATED LOAD.
2. EXTERNAL VOLTAGE OR CURRENT REFERENCE ADJUSTED FOR 26.67 mA FULL SCALE OUTPUT.
3. RS - 343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 9. ADV7141/ADV7148 RGB Video Output Waveform (SETUP = GND)

Table V. ADV7141/ADV7148 RGB Video Output Truth Table (SETUP = GND)

Description	I_{OUT} (mA)[1]	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE	26.67	1	1	FFH
DATA	Data + 8.05	1	1	Data
DATA-SYNC	Data	0	1	Data
BLACK	8.05	1	1	00H
BLACK-SYNC	0	0	1	00H
BLANK	8.05	1	0	xxH
SYNC	0	0	0	xxH

NOTE
[1]Typical with full-scale IOG = 26.67 mA.
External voltage or current reference adjusted for 26.67 mA full-scale output.



NOTES
1. CONNECTED WITH A 75 Ω DOUBLY TERMINATED LOAD.
2. EXTERNAL CURRENT REFERENCE ADJUSTED FOR 19.05 mA FULL SCALE OUTPUT.
3. RS - 343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 10. ADV7146 RGB Video Output Waveform

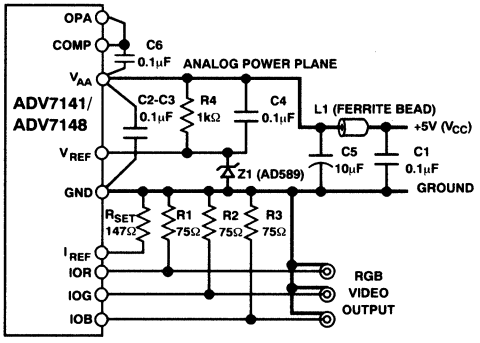
Table VI. ADV7146 RGB Video Output Truth Table

Description	I_{OUT} (mA)[1]	$\overline{BLANK}$	DAC Input Data
WHITE Level	19.05	1	FFH
VIDEO	Video	1	Data
BLACK Level	0	1	00H
BLANK Level	0	0	xxH

NOTE
[1]Typical with full-scale IOR, IOG, IOB = 19.05 mA, I_{REF} = 8.88 mA.

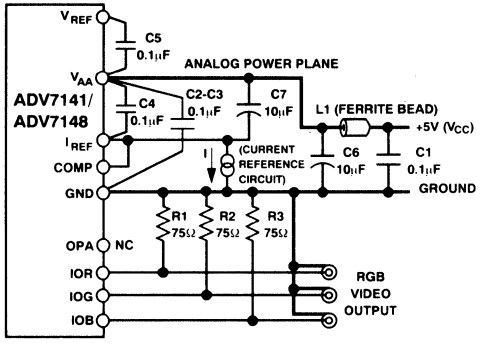
PC BOARD LAYOUT CONSIDERATIONS

The ADV7141, ADV7146 and ADV7148 CEG/DACs are optimally designed for lowest noise performance, both radiated and conducted noise. To complement the excellent noise performance of these parts, it is imperative that great care be given to the PC board layout. Figures 11, 12 and 13 show recommended connection diagrams for the ADV7141/ADV7148 in voltage reference and current reference modes and the ADV7146.



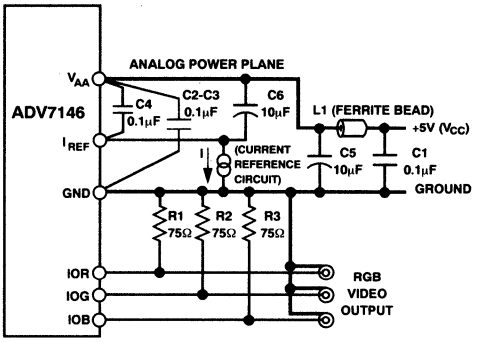
COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1–C5	0.1µF CERAMIC CAPACITOR	
C6	10µF TANTALUM CAPACITOR	
L1	FERRITE BEAD	FAIR-RITE 274300111 OR/ MURATA BL01/02/03
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF-55C
R_{SET}	147Ω 1% METAL FILM RESISTOR	DALE CMF-55C
Z1	1.235V VOLTAGE REFERENCE	ANALOG DEVICES AD589JH

Figure 11. ADV7148/ADV7141 Typical Connection Diagram and Component List (Voltage Reference Configuration)



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1–C5	0.1µF CERAMIC CAPACITOR	
C6–C7	10µF TANTALUM CAPACITOR	
L1	FERRITE BEAD	FAIR-RITE 274300111 OR/ MURATA BL01/02/03
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF-55C

Figure 12. ADV7148/ADV7141 Typical Connection Diagram and Component List (Current Reference Configuration)



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1–C4	0.1µF CERAMIC CAPACITOR	
C5–C6	10µF TANTALUM CAPACITOR	
L1	FERRITE BEAD	FAIR-RITE 274300111 OR/ MURATA BL01/02/03
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF-55C

Figure 13. ADV7146 Typical Connection Diagram and Component List (Current Reference Configuration)

The layout should be optimized for lowest noise on the CEG/DAC power and ground lines. This is achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all the CEG/DAC ground pins, current/voltage reference circuitry, power supply bypass circuitry, the analog output traces, any output amplifiers and all the digital signal traces leading up to the CEG/DAC.

Power Planes

The PC board layout should have two distinct power planes, one for analog circuitry and one digital circuitry. The analog power plane should encompass all the CEG/DAC power pins and all associated analog circuitry. This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead, as illustrated in Figures 11, 12 and 13. This bead should be located within three inches of the part.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all the CEG/DACs power pins, voltage reference circuitry and any output amplifiers.

The PCB power and ground planes should not overlay portions of the analog power plane. Keeping the PCB power and ground planes from overlaying the analog power plane will contribute to a reduction in plane-to-plane noise coupling.

Supply Decoupling

Noise on the analog power plane can be further reduced by the use of multiple decoupling capacitors.

Optimum performance is achieved by the use of 0.1 μF ceramic capacitors. Each of the two groups of V_{AA} (ADV7141/AD7148) should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

It is important to note that while the CEG/DAC contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise. A dc power supply filter (Murata BNX002) will provide EMI suppression between the switching power supply and the main PCB. Alternatively, consideration could be given to using a three terminal voltage regulator.

Digital Signal Interconnect

The digital signal lines to the CEG/DAC should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.

Due to the high clock rates used, long clock lines to the CEG/DAC should be avoided so as to minimize noise pickup.

Any active pull-up termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

Analog Signal Interconnect

The CEG/DAC should be located as close as possible to the output connectors thus minimizing noise pick-up and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, thereby maximizing the high frequency power supply rejection.

For optimum performance, the analog outputs should each have a source termination resistance to ground of 75 Ω (doubly terminated 75 Ω configuration). This termination resistance should be as close as possible to the CEG/DAC so as to minimize reflections.

Additional information on PCB design is available in an Application Note entitled "Design and Layout of a Video Graphics System for Reduced EMI." This application note is available from Analog Devices, Publication No. E1309–15–10/89.

REGISTER LEVEL PROGRAMMING OF THE CEG/DAC

Compatibility

CEG/DACs are available in several plug-in compatible replacements for most popular palette DACs including the Analog Devices ADV471, ADV476 and ADV478, the Inmos IMSG171 and IMSG176 and the Brooktree BT471 and BT478. All are compatible with standard VGA controllers.

The CEG/DAC powers-up in compatibility mode with the CEG circuitry bypassed. CEG mode is enabled with a software key sequence of reserved palette accesses. See Appendix A for a software example of setting the CEG mode.

In compatibility mode the ADV7141 and ADV7146 always use six bits for each red, green and blue palette component. The ADV7148 uses either 6 or 8 bits, depending on the setting of the 8/$\overline{6}$ pin (see Table VII below).

Table VII. CEG/DAC Bits per Color Component

	Compatibility Mode		CEG Mode
CEG/DAC	6-Bit Colors	8-Bit Colors	8-Bit Colors
ADV7141	*		*
ADV7146	*		*
ADV7148	*	*	*

In 6-bit compatibility mode the CEG/DAC shifts color data as it writes to and reads from the palette. The microprocessor writes right justified data in bits D5 to D0 into the palette. In the palette the data is stored left justified with bits D1 and D0 set to 0. During palette read operations the data is returned to the microprocessor in bits D5 to D0 with bits D7 and D6 set to 0.

The CEG mode byte, which is written to the blue palette location 223, is also shifted when it is written, but not when read.

All eight bits of the palette data register are significant when CEG is enabled. Set the CEG mode before writing CEG 8-bit palette information to avoid the shifting operations that occur when the chip is in compatibility mode.

The Encoding Methods

The Continuous Edge Graphics Level 3 specification describes in detail the two advanced encoding methods. Table VIII lists the characteristics of each CEG encoding method.

Basic-8 encoding provides 16 colors with 8 mixes, plus explicit loading of the A or B color registers. The Basic-8 method is appropriate for applications where 8-bits per pixel are available and a moderate number of colors are required, such as CAD applications.

Table VIII. CEG Encoding Methods

Encoding Method	Bits per Pixel	Palette Colors	Mixes	CEG Colors	DPL	Notes
Basic-8	8	16 + 16	8	16 × 16 × 8 = 2048		Mixes and Colors in the Same Pixel
Advanced-4	4	8	8	8 × 8 × 7/2 = 224	Yes	Mixes and Colors in Different Pixels
Advanced-8	8	223	32	223 × 222 × 32/2 = 792,096	Yes	Mixes and Colors in Different Pixels

The two Advanced methods store colors and op codes in different pixels. The Advanced-4 encoding supports 4-bits-per-pixel graphics, making it the CEG method to use in 4-bit systems such as the standard IBM VGA. Advanced-4 provides eight palette colors and eight mixes. Advanced-8 provides 223 drawing colors with full 32-mix shading. Use the Advanced-8 encoding method when there is a requirement for many colors, such as solid model rendering and computer imaging.

In the Advanced methods, an entry in the palette can also be reserved for the DPL op code. The dynamic palette further expands the number of colors available.

Basic-8 Encoding

The Basic-8 method encodes the 16 drawing colors and eight mixes into the eight bit pixel as shown in Figure 14. Table IX below shows the mix ratios that correspond to each pixel value in the mix field.

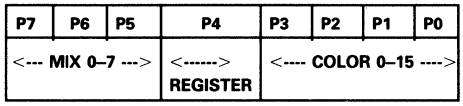


Figure 14. Pixel Encoding for Basic-8

Table IX. Basic-8 Mix Values

Mix Value	Ratio	
	Color A	Color B
0	31/31	0/31
1	27/31	4/31
2	22/31	9/31
3	18/31	13/31
4	13/31	18/31
5	9/31	22/31
6	4/31	27/31
7	0/31	31/31

The register bit selects whether the color is placed in the A register or the B register. When the register bit is set to 0, the A register is used. When the register bit is set to 1, the B register is used. The register bit also selects which portion of the palette is accessed by the color field, because the A and B registers use different palette ranges.

The color field of the pixel data refers to the first 16 colors in the palette (Colors 0–15) when the register bit equals 0 (for the A register). When the register bit equals 1 (for the B register), the color field refers to the second 16 colors in the palette (colors 16 to 31). To find the palette location for the B register, add 16 to the color bits in P0–P3 (e.g., when the register bit = 1, color 0 refers to palette location 16). Generally, these two palette banks are loaded with the same sets of colors, but different colors can be used to increase the possible number of colors.

Advanced Encoding

In the two Advanced encoding methods, the pixel contains either a color or an op code. Mix op codes operate on the colors in the A and B registers. The companion publication, Continuous Edge Graphics Level 3, describes how the two colors are stored in the registers and how they are displayed. The Advanced-4 encoding method combines eight palette colors with eight mixes in the 4-bit pixel, providing 224 CEG colors. The 4 LSBs of the pixel value refer to either palette locations 0–7 or a mix op code as shown in Table X below.

As shown in the Figure 15, when using the Advanced-4 encoding, inputs P3–P0 contain data and inputs P7–P4 are ignored.

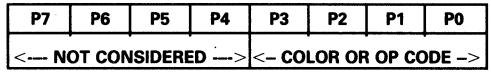


Figure 15. Pixel Encoding for Advanced-4

Table X. Advanced-4 Mix Values

Mix Value	Ratio		
	Color A	Color B	Description
0			Palette Color 0
1	-	-	Palette Color 1
2	-	-	Palette Color 2
3	-	-	Palette Color 3
4	-	-	Palette Color 4
5	-	-	Palette Color 5
6	-	-	Palette Color 6
7	-	-	Palette Color 7 or DPL Op Code
8	31/31	0/31	Mix Op Code
9	27/31	4/31	Mix Op Code
10	22/31	9/31	Mix Op Code
11	18/31	13/31	Mix Op Code
12	13/31	18/31	Mix Op Code
13	9/31	22/31	Mix Op Code
14	4/31	27/31	Mix Op Code
15	0/31	31/31	Mix Op Code

Advanced-8 encoding uses 8-bit pixels and offers 223 palette colors with 32 mixes, resulting in 792,096 CEG colors. The eight bits of the pixel value refer to either a color in the palette or to an op code as shown in Table XI.

Table XI. Advanced-8 Mix Values

Mix Value	Ratio		
	Color A	Color B	Description
0–190	-	-	Palette Colors
191	-	-	Palette Color or DPL Op Code
192	31/31	0/31	Mix Op Code
193	30/31	1/31	Mix Op Code
194	29/31	2/31	Mix Op Code
195	28/31	3/31	Mix Op Code
.	.	.	. .
.	.	.	. .
221	2/31	29/31	Mix Op Code
222	1/31	30/31	Mix Op Code
223	0/31	31/31	Mix Op Code
224–255	-	-	Palette Colors

DYNAMIC PALETTE LOADING (DPL)

The two Advanced CEG encoding methods can use dynamic palette loading, allowing the CEG/DAC to load palette colors from the bit map. With DPL enabled, an entry from the color palette is reserved as the DPL op code (7 in Advanced-4, 191 in Advanced-8). The data following this op code describes the new color to load and specifies the palette address. Note that CEG/DAC addresses are ANDed with the pixel mask register. To avoid misaddressing a DPL entry, load the mask with 255. See Mask Register for more information.

The DPL op code and data are not displayed on the screen. Instead, the color value preceding the DPL op code is repeated in place of the palette load sequence pixels. The two pixels preceding the DPL op code must be of the same kind (two colors or two mixes). For example, Color 1 Color 2 DPL is a valid sequence but Color Mix DPL is not.

DPL Examples

In the Advanced-8 encoding method, a DPL sequence requires five pixels, one for the op code, three for the new color and one for the palette address. Table XII below shows the sequence.

Table XII. DPL Op Code Sequence for Advanced-8

Pixel No.	1	2	3	4	5
Contents	DPL Op Code	New Red	New Green	New Blue	Palette Address

In 4-bits-per-pixel graphics two pixels are needed to specify one 8-bit color value. Therefore, in the Advanced-4 encoding, a DPL requires eight pixels; one for the op code, six for the new color (two each red, green and blue), and one for the palette address. Table XII shows the DPL op code sequence.

Figure 16 shows an example of a DPL op code sequence in the Advanced-4 encoding method and how the op code alters the palette and affects the display. In this example the color at palette address 2 is reassigned with the DPL. As the new color is loaded into the palette the CEG chip displays the pixel color to the left of the op code, Color 3, on the screen. After CEG loads the new color (shown as R2G2B2) at palette address 2, it is displayed whenever Color 2 is used.

Pixel Replication Compensation

Some VGA controllers repeat each pixel twice in low resolution displays (such as 320 × 200). The CEG chip, however, expects pixels in sequences and therefore it provides pixel replication compensation to undo this duplication. When pixel replication compensation is enabled, the CEG/DAC chip samples P7–P0 on every second CLOCK to ignore the repeated data (see Figure 17). Because the CEG/DAC is reversing a duplication made by the controller hardware, the compensation does not affect the graphics programmer. The bit map is written as before.

If the scan line period (video time plus $\overline{\text{BLANK}}$ time) has an even number of clock cycles, then even numbered pixels are displayed. That is, after the end of $\overline{\text{BLANK}}$, the first pixel is ignored, the second displayed, the third ignored, the fourth displayed etc. If the scan line period has an odd number of clock periods, then the first pixel after the end of $\overline{\text{BLANK}}$ is displayed, and the second is also displayed, and thereafter only even numbered pixels are displayed (the fourth, the sixth, etc.).

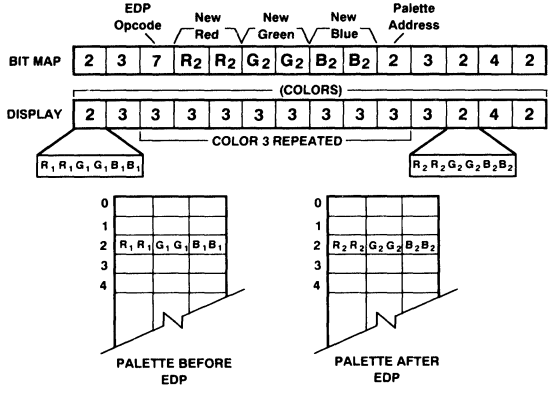


Figure 16. DPL Op Code in the Bit Map

Table XIII. DPL Op Code Sequence for Advanced-4

Pixel No.	1	2	3	4	5	6	7	8
Contents	DPL Op code	New Red	New Red	New Green	New Green	New Blue	New Blue	Palette Address
Color bits		R7–R4	R3–R0	G7–G4	G3–G0	B7–B4	B3–B0	

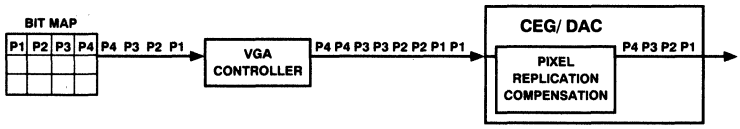


Figure 17. Pixel Replication Compensation

CEG/DAC MODES

The CEG/DAC supports a number of modes. A mode is a combination of attributes. The possible attributes are:

- CEG Encoding (Basic-8 or Advanced-4 or Advanced-8)
- Dynamic Palette Loading (DPL)
- Pixel Replication Compensation

The mode is selected under software control by a key sequence followed by a mode byte.

Enabling CEG

The CEG/DAC employs an unused sequence of palette accesses to enable the CEG logic. This long sequence was specially designed to prevent accidental mode changes. To enable the CEG/DAC the software must perform the following steps:

1. Write a palette read address (222).
2. Write three specific bytes of palette RAM data.
3. Repeat Steps 1 and 2 twice more.

There are eight bytes of special palette RAM data followed by the CEG mode byte. The mode byte determines the CEG functionality. Table XIV shows the special palette RAM data and the mode byte. The CEG/DAC Modes table shows the mode byte values. Appendix A contains sample software routines to set the VGA CEG/DAC mode.

Table XIV. CEG Key Sequence (Decimal Values)

Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
67	69	71	69	68	83	85	78	Mode

The key sequence must be written exactly as shown and cannot be interrupted by any other palette accesses. The entire key sequence must be reentered to change CEG modes. If the key sequence is wrong or the CEGDIS pin is high, the chip remains in compatibility mode. After the mode is set it can be read from palette location 223 blue. Note that, as with other palette data, the mode byte is shifted as it is written to the palette (see Compatibility section).

Table XV shows the CEG/DAC modes. Unpredictable results can occur if a mode not listed in the table is used.

Table XV. CEG/DAC Modes

Mode	CEG Encoding Method	DPL	Pixel Replication
5	Basic-8		
6	Basic-8		*
9	Advanced-4		
10	Advanced-4		*
11	Advanced-4	*	
13	Advanced-8		
14	Advanced-8		*
15	Advanced-8	*	

Writing palette data to location 223 immediately disables CEG operations and returns the device to full power-up compatibility mode (there are no side effects to this and no need to clear any registers). Appendix A contains sample software that clears the CEG/DAC mode and returns the hardware to its initial power-up compatibility mode (in a VGA system).

Gamma Correction

The CEG/DAC automatically applies full gamma correction in all CEG modes. Gamma correction is required to compensate for the nonlinear relationship between the CEG/DAC outputs and the CRT display. To avoid any incompatibility, gamma correction is disabled in compatibility mode. The CEG/DAC uses a gamma value of 2.3 to perform this correction.

Identifying a CEG/DAC

Software determines whether a CEG/DAC is present by reading the mask register. Whenever a CEG mode set is selected, the four most significant bits of the mask register become write only. When read, these four MSBs do not relay the contents of the mask, but rather, give information about the CEG hardware installed.

Mask register Bit D7 is reserved and Bits D6–D4 read back the revision code of the CEG/DAC chip. The revision number always contains at least one "0" to allow software to distinguish CEG/DAC chips from other DACs. An ordinary palette DAC returns the full eight bits of the mask register.

In other words, by enabling CEG, loading the mask register with 255 and then reading the mask register, the software can determine whether or not the hardware uses a CEG/DAC. Devices that return the value loaded (those which read back 255) do not have CEG. Those that return a different value use a CEG/DAC. Appendix A contains sample software which determines the version by inspecting the mask register.

APPENDIX A. CEG SAMPLE CODE

The following code samples are available on diskette

Setting the CEG/DAC Mode

```
SET_CEG_MODE:   ; Set the CEG/DAC mode by entering a key sequence.
                ; 8086/286/386/486 assembler for a CEG/DAC in a VGA
                ; Desired MODE is passed in AL
        PUSH    DX              ; Save DX
        PUSH AX                 ; Save MODE for later
RVRT    equ     00001000b       ; Vertical retrace bit
        MOV     DX,     03DAH   ; Set to Video status port
SYNC0:  IN      AL,     DX      ; Get from Status Port
        TEST    AL,     RVRT    ; Are we in vertical retrace ?
        JNZ     SYNC0           ; Yes, wait until we aren't
SYNC1:  IN      AL,     DX      ; Get from status port
        TEST    AL,     RVRT    ; Are we in vertical retrace ?
        JZ      SYNC1           ; No, loop until we are
ENTER_KEY:
        MOV     DX,     03C7H   ; Set up DAC for read from 222
        MOV     AL,     222
        OUT     DX,     AL
        MOV     DX,     03C9H   ; Put write data address in DX
        MOV     AL,     67      ; Write key byte 1
        OUT     DX,     AL
        MOV     AL,     69      ; Write key byte 2
        OUT     DX,     AL
        MOV     AL,     71      ; Write key byte 3
        OUT     DX,     AL
        MOV     DX,     03C7H   ; Set up DAC for read from 222
        MOV     AL,     222
        OUT     DX,     AL
        MOV     DX,     03C9H   ; Put write data address in DX
        MOV     AL,     69      ; Write key byte 4
        OUT     DX,     AL
        MOV     AL,     68      ; Write key byte 5
        OUT     DX,     AL
        MOV     AL,     83      ; Write key byte 6
        OUT     DX,     AL
        MOV     DX,     03C7H   ; Set up DAC for read from 222
        MOV     AL,     222
        OUT     DX,     AL
        MOV     DX,     03C9H   ; Put write address in DX
        MOV     AL,     85      ; Write key byte 7
        OUT     DX,     AL
        MOV     AL,     78      ; Write key byte 8
        OUT     DX,     AL
        POP     AX              ; Retrieve desired MODE
        OUT     DX,     AL      ; Write the MODE
        POP     DX              ; Restore DX
        RET                     ; return from subroutine
```

Clearing the CEG/DAC Mode

```
CLEAR_CEG_MODE:                                  ; Clear CEG mode and return to
                                                 ; power-up compatibility mode
; 8086/286/386/486 assembler code to clear the CEG/DAC mode and
; return the hardware to its initial power-up Compatibility mode
; (in a VGA system)
;           To clear CEG mode:
;           1) Wait for the Beginning of a vertical retrace
;           2) Write to palette location 223d
            PUSH    DX                           ; Save DX
            PUSH    AX                           ; Save MODE for later
RVRT        equ     00001000b                    ; Vertical retrace bit
; Trigger during vertical retrace so DPLs won't interrupt reset
            MOV     DX,     03DAH                ; Set to Video status port
SYNC0:      IN      AL,     DX                   ; Get from Status Port
            TEST    AL,     RVRT                 ; Are we in vertical retrace ?
            JNZ     SYNC0                        ; Yes, wait until we aren't
SYNC1:      IN      AL,     DX                   ; Get from status port
            TEST    AL,     RVRT                 ; Are we in vertical retrace ?
            JZ      SYNC1                        ; No, loop until we are
                                                 ; Safe to write
            MOV     DX,     03C8H
            MOV     AL,     223                  ; Set write address
            OUT     DX,     AL
            MOV     DX,     03C9H
            MOV     AL,     0                    ; Clear CEG mode
            OUT     DX,     AL                   ; Write the byte
            POP     AX                           ; Restore AX
            POP     DX                           ; Restore DX
            RET
```

Determining the CEG/DAC Version (Reading the Mask Register)

```
GET_VERSION:                                     ; Identify CEG version number
; 8086\286\386\486 assembler code for the VGA sequence to
; determine the version by inspecting the mask register
            MOV     AL,     013DH                ; Any legal mode will do
            CALL    SET_CEG_MODE                 ; Set the mode
            MOV     DX,     03C6H                ; Set DX to mask reg. address
            MOV     AL,     255                  ; Write mask bits to all ones
            OUT     DX,     AL
            IN      AL,     DX                   ; Read contents of mask reg
            SHR     AL,     1                    ; Shift result to lowest bits
            SHR     AL,     1
            SHR     AL,     1
            SHR     AL,     1
            AND     AX,     7                    ; Mask to keep only three bits
; The revision code is now in the low nibble of AL
; Valid revision codes are 0-6
; Revision code 7 indicates Non CEG compatible device
; This specification refers to chip revision 00
```

Writing the Palette

```
; 8086/286/386/486 assembler code for the VGA sequence to
; write to the palette
WRITE_PAL:                                  ; Write to Palette locations
                MOV   DX,   03C8h           ; Set up CEG/DAC for Write
                MOV   AL,   0               ; Will write location zero
                OUT   DX,   AL              ;
                MOV   DX,   03C9h           ; Put data address into DX
                OUT   DX,   AL              ; Write Red Byte          Location 0
                OUT   DX,   AL              ; Write Green Byte        Location 0
                OUT   DX,   AL              ; Write Blue Byte         Location 0
; Palette Address will Auto-increment - keep writing
                OUT   DX,   AL              ; Write Red Byte          Location 1
                OUT   DX,   AL              ; Write Green Byte        Location 1
                OUT   DX,   AL              ; Write Blue Byte         Location 1
```

Reading the Palette

```
; 8086/286/386/486 assembler code for the VGA sequence to
; read from the palette
READ_PAL:                                   ; Read From Palette locations
                MOV   DX,   03C7h           ; Set up CEG/DAC for read
                MOV   AL,   50              ; Will read from location 50
                OUT   DX,   AL              ;
                MOV   DX,   03C9h           ; Put Data address into DX
                IN    AL,   DX              ; Read Red Byte into AL
                IN    AH,   DX              ; Read Green Byte into AH
                IN    BL,   DX              ; Read Blue Byte into BL
; Palette Address will Auto-increment - keep reading
                IN    AL,   DX              ; Read Red Byte           Location 51
                IN    AH,   DX              ; Read Green Byte         Location 51
                IN    BL,   DX              ; Read Blue Byte          Location 51
```

Accessing the Pixel Mask Register

```
; 8086/286/386/486 assembler code for the VGA sequence to access the
; Pixel Mask Register
ACCESS_REG
                MOV   DX,   3C6h            ; Pixel Mask Register Port Address
                MOV   AL,   255             ; Write all ones to register
                OUT   DX,   AL              ;
                IN    DX,   AL              ; Read back contents of register
```

Special Function Audio Products
Contents

Selection Guide
Special Function Audio Products

Audio Preamplifiers (All Values Typical)

Model	Input Voltage Noise nV/√Hz, G = 1000	THD+N %, G = 1000, f = 1 kHz	Slew Rate V/μs	Gain Bandwidth MHz, G = 1000	CMRR dB, G = 1000 f = 60 Hz	Page	Comments
SSM-2015	1.3	0.007	8	0.7	100	7-59	Programmable Input Stage for Noise vs. Source Impedance Optimization
SSM-2016	0.8	0.009	10	0.55	100	7-65	±9 V to ±36 V Operation
SSM-2017	0.95	0.012	17	1	112	7-73 7-73	Only One External Component Required

Volume Control

Voltage Controlled Amplifiers (All Values Typical)

Model	# Channels	Audio Dynamic Range dB	THD+N %, @ 1 kHz G = 1	Gain/Atten Range dB	Gain Bandwidth MHz	Gain Core Class	Page	Comments
SSM-2013	1	106	0.004	115	0.8	A	7-51	Includes Mute Function
SSM-2014		Discontinued – Specify Pin-Compatible Upgrade SSM-2018						
SSM-2018	1	117[1]	0.006[2]	140	10	A/AB	7-81 7-81	Programmable Gain Core Class
SSM-2024	4	82	0.05			A	7-93	Lowest Cost Per VCA
SSM-2120/2	2	100	0.005	140	0.25	A	7-111 7-111	SSM-2120 Contains Two Level Detection Side Chains On-Chip
AD600	2	98		40	3980	A	7-5 7-5	32 dB/V Scale Factor
AD602	2	108		40	1258	A	7-5 7-5	32 dB/V Scale Factor

LogDACs

Model	# Channels	Step Resolution dB	Attenuation Range dB	Page	Comments
AD7111	1	0.375	89.6	7-9	8-Bit Control Input
AD7118	1	1.5	88.5	7-15	6-Bit Control Input

Dolby* Pro-Logic Decoders** (All Values Typical Unless Otherwise Noted)

Model	Audio Dynamic Range dB	THD+N %, @ 1 kHz, 0 dBd = 500 mV rms	Min Channel Separation dB C_{IN} to L, R_{OUT}	Min Channel Separation dB All Other Channels	Page	Comments
SSM-2125	103	0.02	35	25	7-123	Autobalance, Noise Sequencer On-Chip
SSM-2126	103	0.02	25	25	7-123	Autobalance, Noise Sequencer On-Chip

Audio Line Driver and Receivers (All Values Typical)

Balanced Line Driver

Model	Audio Dynamic Range dB	THD+N %, @ 1 kHz V_{IN} = 10 V rms	Output CMRR dB, f = 1 kHz	Slew Rate V/μs	Page	Comments
SSM-2142	116	0.006	−45	15	7-139	No External Components Required, Drives Difficult Loads

Differential Line Receivers

Model	Audio Dynamic Range dB	THD+N %, @ 1 kHz, 10 V rms	Input CMRR dB, f = 60 Hz	Slew Rate V/μs	Gain	Page	Comments
SSM-2141	126	0.001	100	9.5	1	7-133	No External Components Required
SSM-2143	128	0.0008	90	10	1/2 or 2	7-145	No External Components Required

[1]Class AB.
[2]Trimmed, Class AB.
*Dolby is a registered trademark of Dolby Laboratories Licensing Corporation, San Francisco, CA.
**Available only to licensees of Dolby Laboratories

Selection Guide
Special Function Audio Products

Audio Switches (All Values Typical)

Model	# Switches	Noise Voltage nV/√Hz	THD+N % @ 1 kHz	OFF Isolation dB 20 Hz to 20 kHz	Charge Injection pC	Page	Comments
SSM-2402	2	1	0.003	120	50	7-167	Handles +24 dBu Signals (20 V supplies)
SSM-2404	4	0.8	0.0009	100	35	7-181	Lowest Cost-Per-Switch
SSM-2412	2	1	0.003	120	150	7-167	Faster Version of SSM-2402 (t_{ON} = 4 ms)

Matched Transistors

Model	Type	Voltage Noise Max nV/√Hz, f = 1 kHz	Hfe Min	Δhfe Max %, Ic = 1 mA	Unity Gain Bandwidth MHz, I_C = 10 mA (typ)	Voltage Offset Max µV	Page	Comments
SSM-2210	Dual NPN	1	300	5	200	200	7-147	Low Cost
SSM-2220	Dual PNP	1	80	6	180	200	7-159	Low Cost
MAT-04	Quad NPN	2.5	400	2	300	200	7-21	Low Cost

Other Special Function Audio Products

Model	Page	Comments
PKD-01	7-33	Monolithic Peak Detector
SSM-2110	7-99	RMS-to-DC Converter

ANALOG DEVICES

Dual, Low Noise, Wideband Variable Gain Amplifiers

AD600/AD602*

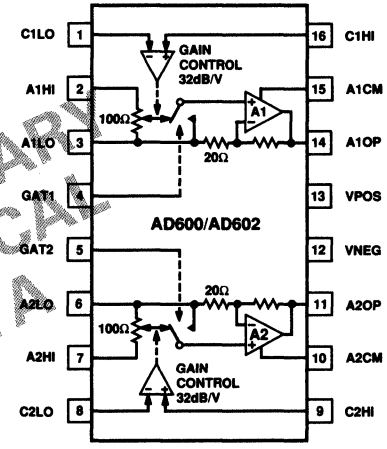
FEATURES

Two Channels with Independent Gain Control
"Linear in dB" Gain
Two Gain Ranges:
AD600: 0 dB to +40 dB
AD602: −10 dB to +30 dB
Accurate Absolute Gain: ±0.5 dB
Low Input Noise: 1.4 nV/√Hz
Low Distortion: −60 dBc THD at ±1 V Output
High Bandwidth: DC to 35 MHz (−3 dB)
Stable Group Delay: ±2 ns
Low Power: 125 mW (Max) per Amplifier
Signal Gating Function for Each Amplifier
Drives A/D Converter Directly

APPLICATIONS

Ultrasound and Sonar Time-Gain Control
High Performance Audio and RF AGC Systems
Signal Measurement
Range Extension for A/D Converters

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD600 and AD602 are dual channel, low noise variable gain amplifiers, based on Analog Devices' proprietary X-AMP™ technique. They are optimized for use in ultrasound imaging systems, but are applicable to any application requiring very precise gain, low noise and distortion, and wide bandwidth. Each channel provides a gain of 0 to +40 dB in the AD600 and −10 dB to +30 dB in the AD602. The lower gain of the AD602 results in an improved signal-to-noise ratio at the output. However, both products have the same 1.4 nV/√Hz input noise spectral density. The decibel gain is directly proportional to a control voltage, and is accurately calibrated and temperature stable.

To achieve the difficult performance objectives, a new circuit form—the X-AMP—has been developed. Each channel of the X-AMP comprises a variable attenuator of 0 dB to −42.14 dB followed by a high-speed fixed-gain amplifier. In this way, the amplifier never has to cope with large inputs, and can benefit from the use of negative feedback to precisely define the gain and dynamics. The attenuator is realized as a seven-stage R-2R ladder network having an input resistance of 100 Ω, laser-trimmed to ±2%. The attenuation between tap points is 6.02 dB; the gain-control circuit provides continuous interpolation between these taps. The resulting gain is very exact, although there is a small ripple (about ±0.2 dB) in the gain error.

The gain-control interfaces are fully differential, providing an input resistance of ~15 MΩ and a scale factor of 32 dB/V (that is, 31.25 mV/dB) defined by an internal voltage reference. The response time of this interface is less than 1 μs. Each channel also has an independent gating facility which optionally blocks signal transmission and sets the dc output level to within a few millivolts of the output ground. The gating control input is TTL and CMOS compatible.

The gain of the AD600 is 41.07 dB and that of the AD602 is 31.07 dB; the −3 dB bandwidth of both the AD600 and AD602 is nominally 35 MHz, essentially independent of the gain. The instantaneous signal-to-noise ratio (ISNR) for a 1 V rms output and a 1 MHz noise bandwidth is typically 76 dB for the AD600 and 86 dB for the AD602. The amplitude response is within ±0.5 dB from 100 kHz to 10 MHz; over this frequency range the group delay varies by less than ±2 ns at all gain settings.

Each amplifier section can drive a variety of load impedances with low distortion. The peak specified output is ±2.5 V minimum into a 500 Ω load, or ±1 V into a 100 Ω load. For a 200 Ω load in shunt with 5 pF, the total harmonic distortion for a ±1 V sinusoidal output at 10 MHz is typically −60 dBc.

With appropriate precautions, amplifier sections may be cascaded to provide a gain-control range of 80 dB. A variety of control options can then be employed. For example, the gain-control inputs can be driven in simple parallel to provide a scaling of 64 dB/V, when the ISNR decreases essentially linearly as the gain is increased. A gain offset of just 3 dB between the two sections results in the lowest ripple in the gain error. Alternatively, the gain-control inputs may be offset by 40 dB to achieve the highest possible ISNR at any gain within the full gain range.

The AD600 and AD602 are available in either a 16-pin plastic DIP or 16-pin SOIC, and are guaranteed for operation over the commercial temperature range of 0°C to +70°C.

***Patent pending.**
X-AMP is a trademark of Analog Devices, Inc.

AD600/AD602—SPECIFICATIONS (Each VGA, at T_A = +25°C, V_S = ±5 V, −625 mV ≤ V_G ≤ +625 mV, R_L = 500 Ω, and C_L = 5 pF, unless otherwise noted. Specifications for AD600 and AD602 are identical unless otherwise noted.)

Parameter	Conditions	AD600J/AD602J Min	Typ	Max	Units
AMPLIFIER INPUT CHARACTERISTICS					
Input Resistance	Pin 2 to 3; Pin 6 to 7	98	100	102	Ω
Input Capacitance			2		pF
Input Noise Spectral Density[1]	−625 mV ≤ V_G ≤ +625 mV		1.4		nV/√Hz
Peak Input Voltage				±2	V
Common-Mode Rejection Ratio	f = 1 MHz		TBD		dB
AMPLIFIER OUTPUT CHARACTERISTICS					
−3 dB Bandwidth	V_{OUT} = 100 mV rms		35		MHz
Slew Rate			275		V/μs
Peak Output[2]	R_L ≥ 500Ω	±2.5	±3		V
Output Impedance	f ≤ 10 MHz		2		Ω
Output Short-Circuit Current			TBD	TBD	mA
Group Delay Change vs. Gain	f = 3 MHz; Full Gain Range		±2		ns
Group Delay Change vs. Frequency	V_G = 0 V; f = 1 to 10 MHz		±2		ns
Distortion	THD; R_L = 200 Ω, V_O = 1 V		−60		dBc
AMPLIFIER GAIN ACCURACY					
AD600					
Gain Accuracy	V_G = −625 mV	−0.5	0	+0.5	dB
	V_G = 0 V	19.8	20	20.2	dB
	V_G = +625 mV	39.5	40	40.5	dB
Output Offset Voltage[3]	V_G = 0		15	30	mV
Output Offset Variation	−625 mV ≤ V_G ≤ +625 mV			TBD	mV
AD602					
Gain Accuracy	V_G = − 625 mV	−10.5	−10	−9.5	dB
	V_G = 0 V	9.8	10	10.2	dB
	V_G = + 625 mV	29.5	30	30.5	dB
Output Offset Voltage[3]	V_G = 0		5	10	mV
Output Offset Variation	−625 mV ≤ V_G ≤ +625 mV			TBD	mV
GAIN CONTROL INTERFACE					
Gain Scaling Factor		31.7	32	32.3	dB/V
Input Voltage Range		−0.75		2.5	V
Input Bias Current			0.15	1	μA
Input Offset Current			10	TBD	nA
Differential Input Resistance	Pins 1 to 16; Pins 8 to 9		15		MΩ
Response Time	Full 40 dB Gain Change		40		dB/μs
SIGNAL GATING INTERFACE					
Logic Input "LO" (Output ON)				0.8	V
Logic Input "HI" (Output OFF)		2.4			V
Response Time	ON to OFF, OFF to ON		1		μs
Input Resistance	Pin 4 to 3; Pin 5 to 6		30		kΩ
Output Gated OFF					
Output Offset Voltage			±10		mV
Output Noise Spectral Density			11		nV/√Hz
Signal Feedthrough			TBD		dB
POWER SUPPLY					
Specified Operating Range		±4.75		±5.25	V
Quiescent Current			22	25	mA
Power Supply Rejection Ratio	±4.75 V ≤ V_S ≤ 5.25 V		TBD		dB

NOTES

[1]Open or short-circuited input; noise is lower when system is set to maximum gain and input is short-circuited.

[2]Using resistive loads of 500Ω or greater, or with the addition of a 1 kΩ pull-down resistor when driving lower loads.

[3]Note that because the amplifier's gain is X113 (41 dB) in the AD600, an input offset of only 100 μV becomes an 11.3 mV offset at the output; in the AD602, the amplifier's gain is 35.7 (31 dB), and an input offset of 100 μV becomes a 3.57 mV offset at the output.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage $\pm V_S$ . . . . . ± 7.5 V
Input Voltages
Pins 1, 8, 9, 16 . . . . . $\pm$XX V
Pins 2, 3, 6, 7 . . . . . $\pm$XX V
Pins 4, 5 . . . . . $\pm V_S$
Internal Power Dissipation . . . . . 600 mW
Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature, Soldering 60 sec . . . . . +300°C

NOTE
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

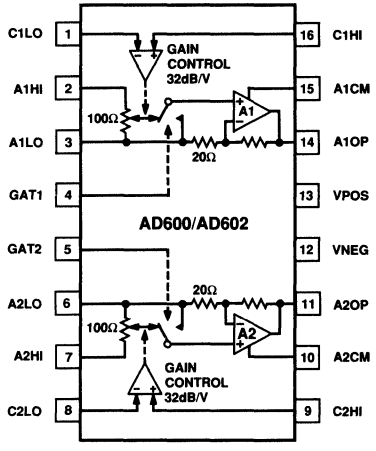
Thermal Characteristics:
16-Pin Plastic Package: θ_{JA} = 85°C/Watt
16-Pin SOIC Package: θ_{JA} = 100°C/Watt

CAUTION

ESD (electrostatic discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

CONNECTION DIAGRAM

16-Pin Plastic DIP (N) Package
16-Pin Plastic SOIC (R) Package



ORDERING GUIDE

Model	Gain Range	Temperature Range	Package Option*
AD600JN	0 dB to +40 dB	0°C to +70°C	N-16
AD600JR	0 dB to +40 dB	0°C to +70°C	R-16
AD602JN	−10 dB to +30 dB	0°C to +70°C	N-16
AD602JR	−10 dB to +30 dB	0°C to +70°C	R-16

*N = Plastic DIP; R = Small Outline IC (SOIC). For outline information see Package Information section.

PIN DESCRIPTIONS

Pin	Function	Description
Pin 1	C1LO	CH1 Gain-Control Input "LO" (Positive Voltage Reduces CH1 Gain).
Pin 2	A1HI	CH1 Signal Input "HI" (Positive Voltage Increases CH1 Output).
Pin 3	A1LO	CH1 Signal Input "LO" (Usually Taken to CH1 Input Ground).
Pin 4	GAT1	CH1 Gating Input (A Logic "HI" Shuts Off CH1 Signal Path).
Pin 5	GAT2	CH2 Gating Input (A Logic "HI" Shuts Off CH2 Signal Path).
Pin 6	A2LO	CH2 Signal Input "LO" (Usually Taken to CH2 Input Ground).
Pin 7	A2HI	CH2 Signal Input "HI" (Positive Voltage Increases CH2 Output).
Pin 8	C2LO	CH2 Gain-Control Input "LO" (Positive Voltage Reduces CH2 Gain).
Pin 9	C2HI	CH2 Gain-Control Input "HI" (Positive Voltage Increases CH2 Gain).
Pin 10	A2CM	CH2 Common (Usually Taken to CH2 Output Ground).
Pin 11	A2OP	CH2 Output.
Pin 12	VNEG	Negative Supply for Both Amplifiers.
Pin 13	VPOS	Positive Supply for Both Amplifiers.
Pin 14	A1OP	CH1 Output.
Pin 15	A1CM	CH1 Common (Usually Taken to CH1 Output Ground).
Pin 16	C1HI	CH1 Gain-Control Input "HI" (Positive Voltage Increases CH1 Gain).

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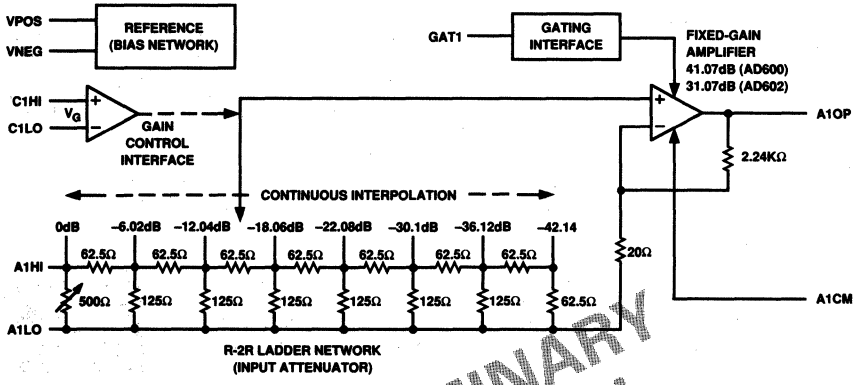


AD600 and AD602 Simplified Architecture

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

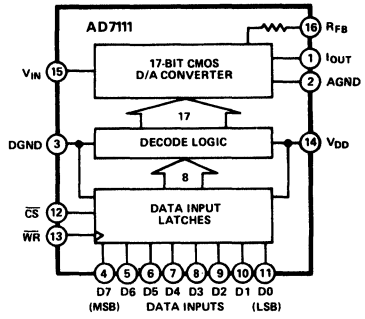
LOGDAC
CMOS Logarithmic D/A Converter

AD7111*

FEATURES
Dynamic Range: 88.5dB
Resolution: 0.375dB
On-Chip Data Latches
Full ±25V Input Range Multiplying DAC
Low Distortion
Single +5V Supply
Latch-Up Free (No Protection Schottky Required)

APPLICATIONS
Digitally Controlled AGC Systems
Audio Attenuators
Wide Dynamic Range A/D Converters
Sonar Systems
Function Generators

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The LOGDAC™ AD7111 is a CMOS multiplying D/A converter which can attenuate an analog input signal over the range 0 to −88.5dB in 0.375dB steps.

The degree of attenuation is determined by an 8-bit data word which is latched into on-chip data latches using microprocessor compatible control signals $\overline{CS}$ and $\overline{WR}$. Operating frequency range of the device is from dc to several hundred kHz.

The device is available in a standard 16-pin DIP and in a 20-terminal surface mount package.

ORDERING GUIDE

Model	Temperature Range	Specified Accuracy Range	Package Option*
AD7111KN	0°C to +70°C	0dB to 60dB	N-16
AD7111BQ	−25°C to +85°C	0dB to 60dB	Q-16
AD7111TQ	−55°C to +125°C	0dB to 60dB	Q-16
AD7111LN	0°C to +70°C	0dB to 72dB	N-16
AD7111CQ	−25°C to +85°C	0dB to 72dB	Q-16
AD7111UQ	−55°C to +125°C	0dB to 72dB	Q-16
AD7111TE/883B	−55°C to +125°C	0dB to 60dB	E-20A

*E = Leadless Ceramic Chip Carrier; N = Plastic DIP; Q = Cerdip.
For outline information see Package Information section.

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*U.S. Patent No. 4521764
LOGDAC is a trademark of Analog Devices Inc.

AD7111—SPECIFICATIONS (V_{DD} = +5V, V_{IN} = −10V dc, I_{OUT} = AGND = DGND = 0V, output amplifier AD544 except where stated)

Parameter	AD7111L/C/U GRADES T_A = +25°C	AD7111L/C/U GRADES T_A = T_{min}, T_{max}	AD7111K/B/T GRADES T_A = +25°C	AD7111K/B/T GRADES T_A = T_{min}, T_{max}	Units	Conditions/Comments
NOMINAL RESOLUTION	0.375	0.375	0.375	0.375	dB	
ACCURACY RELATIVE TO 0dB ATTENUATION						
0.375dB Steps:						
Accuracy ≤ ±0.17dB	0 to 36	0 to 36	0 to 30	0 to 30	dB min	Guaranteed attenuation ranges
Monotonic	0 to 54	0 to 54	0 to 48	0 to 48	dB min	for specified step sizes
0.75dB Steps:						
Accuracy ≤ ±0.35dB	0 to 48	0 to 42	0 to 42	0 to 36	dB min	
Monotonic	0 to 72	0 to 66	0 to 72	0 to 60	dB min	
1.5dB Steps:						
Accuracy ≤ ±0.7dB	0 to 54	0 to 48	0 to 48	0 to 42	dB min	
Monotonic	Full Range	0 to 78	0 to 85.5	0 to 72	dB min	Full Range is from 0 to 88.5dB
3.0dB Steps:						
Accuracy ≤ ±1.4dB	0 to 66	0 to 54	0 to 60	0 to 48	dB min	
Monotonic	Full Range	Full Range	Full Range	Full Range		
6.0dB Steps:						
Accuracy ≤ ±2.7dB	0 to 72	0 to 60	0 to 60	0 to 48	dB min	
Monotonic	Full Range	Full Range	Full Range	Full Range		
GAIN ERROR	±0.1	±0.15	±0.15	±0.20	dB max	
V_{IN} INPUT RESISTANCE (PIN 15)	9/11/15	9/11/15	7/11/18	7/11/18	kΩ min/typ/max	
R_{FB} INPUT RESISTANCE (PIN 16)	9.3/11.5/15.7	9.3/11.5/15.7	7.3/11.5/18.8	7.3/11.5/18.8	kΩ min/typ/max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±10	±1	±10	µA max	Digital Inputs = V_{DD}
SWITCHING CHARACTERISTICS[1]						
t_{CS}	0	0	0	0	ns min	Chip Select to Write Setup Time
t_{CH}	0	0	0	0	ns min	Chip Select to Write Hold Time
t_{WR}	350	500	350	500	ns min	Write Pulse Width
t_{DS}	175	250	175	250	ns min	Data Valid to Write Setup Time
t_{DH}	10	10	10	10	ns min	Data Valid to Write Hold Time
t_{RFSH}	3	4.5	3	4.5	µs min	Refresh Time
POWER SUPPLY						
V_{DD}	+5	+5	+5	+5	V	
I_{DD}	1	4	1	4	mA max	Digital Inputs = V_{IH} or V_{IL}
	500	1000	500	1000	µA max	Digital Inputs = 0V or V_{DD}. See Figure 7.

NOTE
[1] Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not subject to test.
V_{DD} = +5V, V_{IN} = −10V dc except where stated, I_{OUT} = AGND = DGND = 0V, output amplifier AD544 except where stated.

Parameter	AD7111L/C/U GRADES T_A = 25°C	AD7111L/C/U GRADES T_A = T_{min}, T_{max}	AD7111K/B/T GRADES T_A = +25°C	AD7111K/B/T GRADES T_A = T_{min}, T_{max}	Units	Conditions/Comments
DC Supply Rejection, ΔGain/ΔV_{DD}	0.001	0.005	0.001	0.005	dB per % max	ΔV_{DD} = ±10%, Input Code = 00000000
Propagation Delay	3.0	4.5	3.0	4.5	µs max	Full Scale Change Measured from $\overline{WR}$ going high, $\overline{CS}$ = 0V.
Digital-to-Analog Glitch Impulse	100	–	100	–	nV secs typ	Measured with ADLH0032CG as Output Amplifier for Input Code Transition 10000000 to 00000000. C1 of Figure 1 is 0pF
Output Capacitance, Pin 1	185	185	185	185	pF max	
Input Capacitance, Pin 15 and Pin 16	7	7	7	7	pF max	
Feedthrough at 1kHz	–94	–72	–92	–68	dB max	Feedthrough is also determined by circuit
Total Harmonic Distortion	–91	–91	–91	–91	dB typ	layout (see Figure 4).
Output Noise Voltage Density	70	70	70	70	nV/√Hz max	V_{IN} = 6V rms at 1kHz
Digital Input Capacitance	7	7	7	7	pF max	Includes AD544 Amplifier Noise

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} (to DGND)	+7V
V_{IN} (to AGND)	+35V
Digital Input Voltage to DGND	−0.3V to V_{DD} +0.3V
I_{OUT} to AGND	−0.3V to V_{DD}
V_{IN} to AGND	±35V
AGND to DGND	0 to V_{DD}
DGND to AGND	0 to V_{DD}
Power Dissipation (Any Package)	
To +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial (K, L Versions)	0 to +70°C
Industrial (B, C Versions)	−25°C to +85°C
Extended (T, U Versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RESOLUTION: Nominal change in attenuation when moving between two adjacent codes.

MONOTONICITY: The device is monotonic if the analog output decreases (or remains constant) as the digital code increases.

FEEDTHROUGH ERROR: That portion of the input signal which reaches the output when all digital inputs are high. See section on Applications.

OUTPUT LEAKAGE CURRENT: Current which appears on the I_{OUT} terminal with all digital inputs high.

TOTAL HARMONIC DISTORTION: A measure of the harmonics introduced by the circuit when a pure sinusoid is applied to the input. It is expressed as the harmonic energy divided by the fundamental energy at the output.

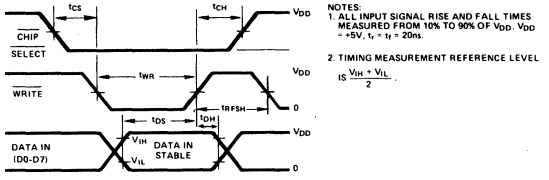
ACCURACY: The difference (measured in dB) between the ideal transfer function as listed in Table I and the actual transfer function as measured with the device.

OUTPUT CAPACITANCE: Capacitance from I_{OUT} to ground.

DIGITAL-TO-ANALOG GLITCH IMPULSE: The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-Secs or nV-Secs depending upon whether the glitch is measured as a current or voltage signal. Glitch impulse is measured with V_{IN} = AGND.

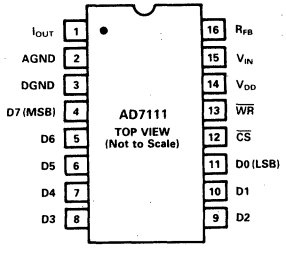
PROPAGATION DELAY: This is a measure of the internal delays of the circuit and is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

WRITE CYCLE TIMING DIAGRAM

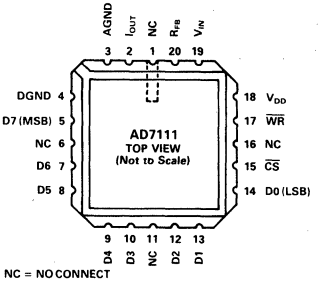


PIN CONFIGURATIONS

DIP



LCCC



NC = NO CONNECT

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7111 consists of a 17-bit R-2R CMOS multiplying D/A converter with extensive digital logic. The logic translates the 8-bit binary input into a 17-bit word which is used to drive the D/A converter. Input data on the D7–D0 bus is loaded into the input data latches using $\overline{CS}$ and $\overline{WR}$ control signals. The rising edge of $\overline{WR}$ latches the input data and initiates the internal data transfer to the decoder. A minimum time t_{RFSH}, the refresh time, is required for the data to propagate through the decoder before a new data write is attempted.

The transfer function for the circuit of Figure 1 is given by:

$$V_O = -V_{IN}\ 10\ \exp -\frac{0.375\ N}{20}$$

or

$$\left|\frac{V_O}{V_{IN}}\right| \text{ dB} = -0.375\ N$$

Where 0.375 is the step size (resolution) in dB and N is the input code in decimal for values 0 to 239. For $240 \leqslant N \leqslant 255$ the output is zero. Table I gives the output attenuation relative to 0dB for all possible input codes.

The graphs on the last page give a pictorial representation of the specified accuracy and monotonic ranges for all grades of the AD7111. High attenuation levels are specified with less accuracy than low attenuation levels. The range of monotonic behavior depends upon the attenuation step size used. For example, the AD7111L is guaranteed monotonic in 0.375dB steps from 0 to -54dB inclusive and in 0.75dB steps from 0 to -72dB inclusive. To achieve monotonic operation over the entire 88.5dB range it is necessary to select input codes so that the attenuation step size at any point is consistent with the step size guaranteed for monotonic operation at that point.

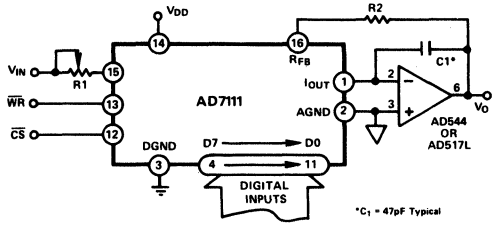


Figure 1. Typical Circuit Configuration

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows a simplified circuit of the D/A converter section of the AD7111 and Figure 3 gives an approximate equivalent circuit.

The current source $I_{LEAKAGE}$ is composed of surface and junction leakages and as with most semiconductor devices, approximately doubles every 10°C—see Figure 11. The resistor R_O as shown in Figure 3 is the equivalent output resistance of the device which varies with input code (excluding all 0's code) from 0.8R to 2R. R is typically 11kΩ. C_{OUT} is the capacitance due to the N channel switches and varies from about 60pF to 185pF depending upon the digital input. For further information on CMOS multiplying D/A converters refer to "Application Guide to CMOS Multiplying D/A converters" which is available from Analog Devices, Publication Number G479–15–8/78.

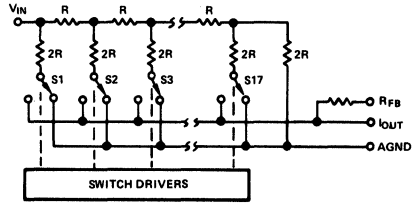


Figure 2. Simplified D/A Circuit of AD7111

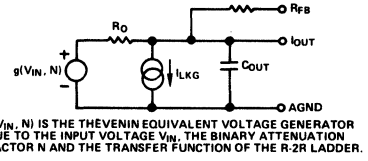


Figure 3. Equivalent Analog Output Circuit of AD7111

D3-D0 / D7-D4	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	0.0	0.375	0.75	1.125	1.5	1.875	2.25	2.625	3.0	3.375	3.75	4.125	4.5	4.875	5.25	5.625
0001	6.0	6.375	6.75	7.125	7.5	7.875	8.25	8.625	9.0	9.375	9.75	10.125	10.5	10.875	11.25	11.625
0010	12.0	12.375	12.75	13.125	13.5	13.875	14.25	14.625	15.0	15.375	15.75	16.125	16.5	16.875	17.25	17.625
0011	18.0	18.375	18.75	19.125	19.5	19.875	20.25	20.625	21.0	21.375	21.75	22.125	22.5	22.875	23.25	23.625
0100	24.0	24.375	24.75	25.125	25.5	25.875	26.25	26.625	27.0	27.375	27.75	28.125	28.5	28.875	29.75	29.625
0101	30.0	30.375	30.75	31.125	31.5	31.875	32.25	32.625	33.0	33.375	33.75	34.125	34.5	34.875	35.25	35.625
0110	36.0	36.375	36.75	37.125	37.5	37.875	38.25	38.625	39.0	39.375	39.75	40.125	40.5	40.875	41.25	41.625
0111	42.0	42.375	42.75	43.125	43.5	43.875	44.25	44.625	45.0	45.375	45.75	46.125	46.5	46.875	47.25	47.625
1000	48.0	48.375	48.75	49.125	49.5	49.875	50.25	50.625	51.0	51.375	51.75	52.125	52.5	52.875	53.25	53.625
1001	54.0	54.375	54.75	55.125	55.5	55.875	56.25	56.625	57.0	57.375	57.75	58.125	58.5	58.875	59.25	59.625
1010	60.0	60.375	60.75	61.125	61.5	61.875	62.25	62.625	63.0	63.375	63.75	64.125	64.5	64.875	65.25	65.625
1011	66.0	66.375	66.75	67.125	67.5	67.875	68.25	68.625	69.0	69.375	69.75	70.125	70.5	70.875	71.25	71.625
1100	72.0	72.375	72.75	73.125	73.5	73.875	74.25	74.625	75.0	75.375	75.75	76.125	76.5	76.875	77.25	77.625
1101	78.0	78.375	78.75	79.125	79.5	79.875	80.25	80.625	81.0	81.375	81.75	82.125	82.5	82.875	83.25	83.625
1110	84.0	84.375	84.75	85.125	85.5	85.875	86.25	86.625	87.0	87.375	87.75	88.125	88.5	88.875	89.25	89.625
1111	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE

Table I. Ideal Attenuation in dB vs. Input Code

DYNAMIC PERFORMANCE

The dynamic performance of the AD7111 will depend upon the gain and phase characteristics of the output amplifier, together with the optimum choice of PC board layout and decoupling components. Figure 4 shows a printed circuit layout which minimizes feedthrough from V_{IN} to the output in multiplying applications. Circuit layout is most important if the optimum performance of the AD7111 is to be achieved. Most application problems stem from either poor layout, grounding errors, or inappropriate choice of amplifier.

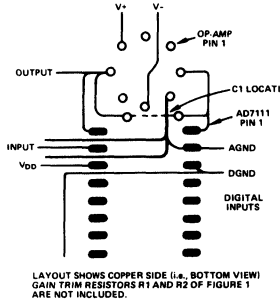


Figure 4. Suggested Layout for AD7111 and Op-Amp

It is recommended that when using the AD7111 with a high speed amplifier, a capacitor (C1) be connected in the feedback path as shown in Figure 1. This capacitor, which should be between 30pF and 50pF, compensates for the phase lag introduced by the output capacitance of the D/A converter. Figures 5 and 6 show the performance of the AD7111 using the AD517, a fully compensated high gain superbeta amplifier, and the AD544, a fast FET input amplifier. The performance without C1 is shown in the middle trace and the response with C1 in circuit is shown in the bottom trace.

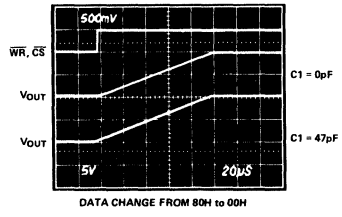


Figure 5. Response of AD7111 with AD517

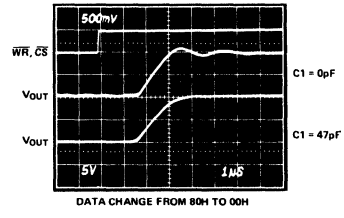


Figure 6. Response of AD7111 with AD544

In conventional CMOS D/A converter design parasitic capacitance in the N-channel D/A converter switches can give rise to glitches on the D/A converter output. These glitches result from digital feedthrough. The AD7111 has been designed to minimize these glitches as much as possible.

For operation beyond 250kHz, capacitor C1 may be reduced in value. This gives an increase in bandwidth at the expense of a poorer transient response as shown in Figures 6 and 12. In circuits where C1 is not included the high frequency roll-off point is primarily determined by the characteristics of the output amplifier and not the AD7111.

Feedthrough and absolute accuracy are sensitive to output leakage current effects. For this reason it is recommended that the operating temperature of the AD7111 be kept as close to 25°C as is practically possible, particularly where the device's performance at high attenuation levels is important. A typical plot of leakage current vs. temperature is shown in Figure 11.

Some solder fluxes and cleaning materials can form slightly conductive films which cause leakage effects between analog input and output. The user is cautioned to ensure that the manufacturing process for circuits using the AD7111 does not allow such films to form. Otherwise the feedthrough, accuracy and maximum usable range will be affected.

STATIC ACCURACY PERFORMANCE

The D/A converter section of the AD7111 consists of a 17-bit R-2R type converter. To obtain optimum static performance at this level of resolution it is necessary to pay great attention to amplifier selection, circuit grounding, etc.

Amplifier input bias current results in a dc offset at the output of the amplifier due to the current flowing through the feedback resistor R_{FB}. It is recommended that an amplifier with an input bias current of less than 10nA be used (e.g., AD517 or AD544) to minimize this offset.

Another error arises from the output amplifier's input offset voltage. The amplifier is operated with a fixed feedback resistance, but the equivalent source impedance (the AD7111 output impedance) varies as a function of attenuation level. This has the effect of varying the "noise" gain of the amplifier, thus creating a varying error due to amplifier offset voltage. It is recommended that an amplifier with less than 50µV of input offset be used (such as the AD517 or AD OP-07) in dc applications. Amplifiers with higher offset voltage may cause audible "thumps" in ac applications due to dc output changes.

The AD7111 accuracy is specified and tested using only the internal feedback resistor. Any Gain Error (i.e., mismatch of R_{FB} to the R-2R ladder) that may exist in the AD7111 D/A converter circuit results in a constant attenuation error over the whole range. The AD7111 accuracy is specified relative to 0dB attenuation, hence "Gain" trim resistors—R1 and R2 in Figure 1—can be used to adjust $V_{OUT} = V_{IN}$ precisely (i.e., 0dB attenuation) with input code 00000000. The accuracy and monotonic range specifications of the AD7111 are not affected in any way by this gain trim procedure. For the AD7111L/C/U grades, suitable values for R1 and R2 of Figure 1 are R1 = 500Ω, R2 = 180Ω; for the K/B/T grades suitable values are R1 = 1000Ω, R2 = 270Ω. For additional information on gain error the reader is referred to Application Note "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs" by Phil Burton available from Analog Devices Inc., Publication Number E630–10–6/81.

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AD7111—Typical Performance Characteristics

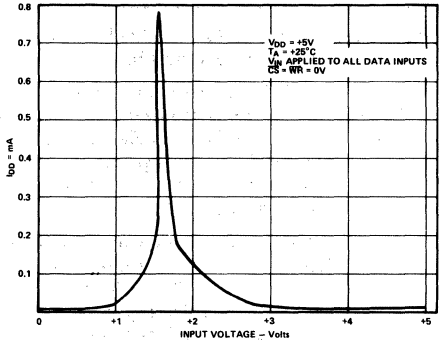


Figure 7. Typical Supply Current vs. Logic Input Level

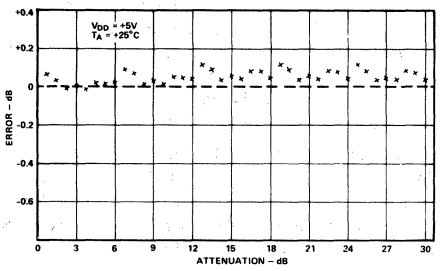


Figure 8. Typical Attenuation Error for 0.75dB Steps

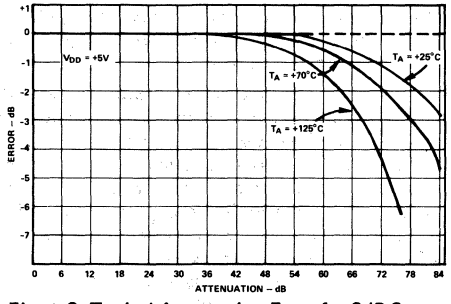


Figure 9. Typical Attenuation Error for 3dB Steps vs. Temperature

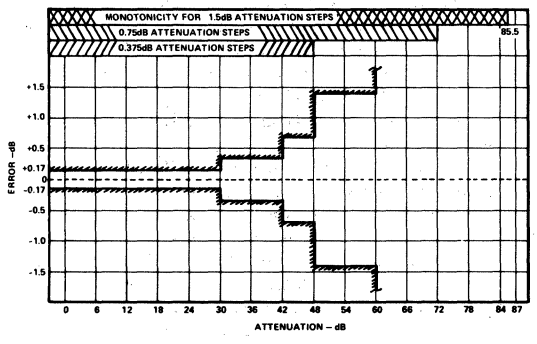


Figure 10. Accuracy Specification for K/B/T Grade Devices at T_A = +25°C

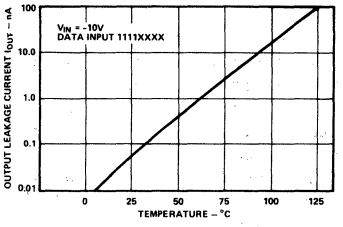


Figure 11. Output Leakage Current vs. Temperature

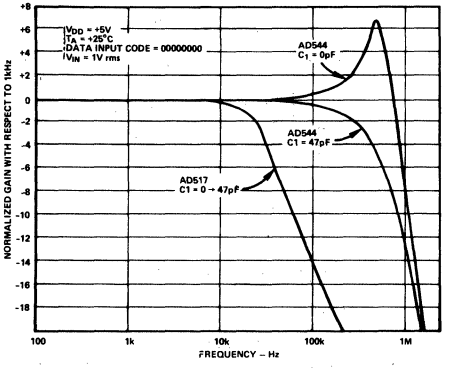


Figure 12. Frequency Response with AD544 and AD517 Amplifiers

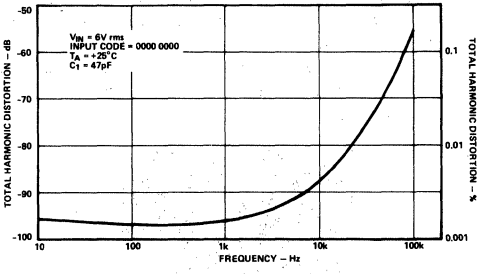


Figure 13. Distortion vs. Frequency Using AD544 Amplifier

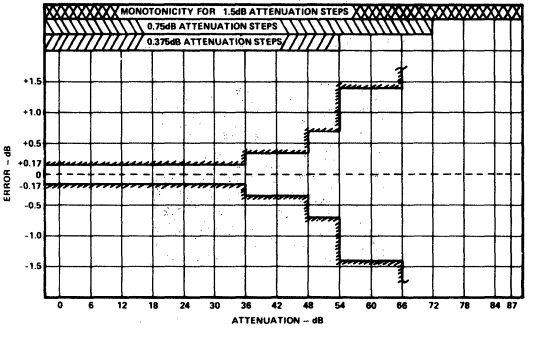


Figure 14. Accuracy Specification for L/C/U Grade Devices at T_A = +25°C

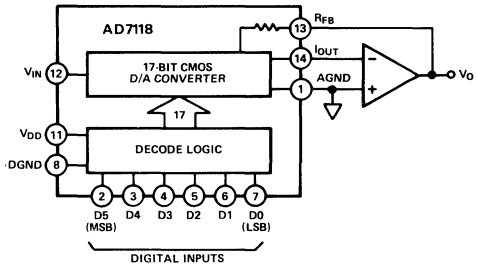
ANALOG DEVICES

LOGDAC
CMOS Logarithmic D/A Converter
AD7118*

FEATURES
Dynamic Range 85.5dB
Resolution 1.5dB
Full ±25V Input Range Multiplying DAC
Full Military Temperature Range -55°C to +125°C
Low Distortion
Low Power Consumption
Latch Proof Operation (Schottky Diodes Not Required)
Single 5V to 15V Supply

APPLICATIONS
Digitally Controlled AGC Systems
Audio Attenuators
Wide Dynamic Range A/D Converters
Sonar Systems
Function Generators

FUNCTIONAL DIAGRAM

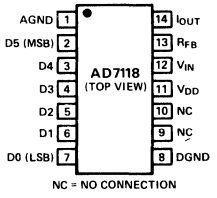


GENERAL DESCRIPTION

The LOGDAC™ AD7118 is a CMOS multiplying D/A converter which attenuates an analog input signal over the range 0 to −85.5dB in 1.5dB steps. The analog output is determined by a six-bit attenuation code applied to the digital inputs. Operating frequency range of the device is from dc to several hundred kHz.

The device is manufactured using an advanced monolithic silicon gate thin-film on CMOS process and is packaged in a 14-pin dual-in-line package.

PIN CONFIGURATION (Not to Scale)



NC = NO CONNECTION

ORDERING GUIDE

Model	Temperature Range	Specified Accuracy Range	Package Option[1]
AD7118KN	0 to +70°C	0 to 42dB	N-16
AD7118LN	0 to +70°C	0 to 48dB	N-16
AD7118BQ	−25°C to +85°C	0 to 42dB	Q-16
AD7118CQ	−25°C to +85°C	0 to 48dB	Q-16
AD7118TQ[2]	−55°C to +125°C	0 to 42dB	Q-16
AD7118UQ[2]	−55°C to +125°C	0 to 48dB	Q-16

NOTES
[1]N = Plastic DIP; Q = Cerdip. For outline information see Package Information section.
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number.

*Protected by U.S. Patent No. 4521,764.
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AD7118—SPECIFICATIONS (V_{DD} = +5V or +15V, V_{IN} = −10V dc, I_{OUT} = AGND = DGND = 0V, output amplifier AD544 except where stated)

PARAMETER		T_A = +25°C		T_A = T_{min}, T_{max}		UNITS	TEST CONDITIONS/ COMMENTS
		V_{DD} = +5V	V_{DD} = +15V	V_{DD} = +5V	V_{DD} = +15V		
NOMINAL RESOLUTION		1.5	1.5	1.5	1.5	dB	
ACCURACY RELATIVE TO V_{IN}							
AD7118L/C/U							
0 to −30dB		±0.35	±0.35	±0.4	±0.4	dB max	Accuracy is measured using
−31.5 to −42dB		±0.7	±0.5	±0.8	±0.7	dB max	circuit of Figure 1 and includes
−43.5 to −48dB		±1.0	±0.7	±1.3	±1.0	dB max	any effects due to mismatch
AD7118K/B/T							between R_{FB} and the R-2R
0 to −30dB		±0.5	±0.5	±0.5	±0.5	dB max	ladder circuit.
−31.5 to −42dB		±0.75	±0.75	±1.0	±0.8	dB max	
MONOTONIC RANGE							
Nominal 1.5dB Steps	L/C/U Grade	Monotonic Over Full		0 to −72	0 to −72	dB	Digital Inputs 000000 to 110000
	K/B/T Grade	Code Range		0 to −66	0 to −66	dB	Digital Inputs 000000 to 101100
Nominal 3dB Steps	All Grades	Monotonic Over Full Code Range					
V_{IN} INPUT RESISTANCE	All Grades	9	9	9	9	kΩ min	
(PIN 12)	L/C/U Grade	17	17	17	17	kΩ max	
	K/B/T Grade	21	21	21	21	kΩ max	
R_{FB} INPUT RESISTANCE	All Grades	9.45	9.45	9.45	9.45	kΩ min	
(PIN 13)	L/C/U Grade	18	18	18	18	kΩ max	
	K/B/T Grade	22	22	22	22	kΩ max	
DIGITAL INPUTS							
Input High Voltage Requirements V_{IH}		3.0	13.5	3.0	13.5	V min	
Input Low Voltage Requirements V_{IL}		0.8	1.5	0.8	1.5	V max	
Input Leakage Current		±1	±1	±10	±10	μA max	Digital Inputs = V_{DD}
POWER SUPPLY							
V_{DD} for Specified Accuracy		5	–	5	–	V min	
		–	15	–	15	V max	
I_{DD}		0.5	1	1	2	mA max	Digital Inputs = 0V or V_{DD} (See Figure 7)

Specifications subject to change without notice.

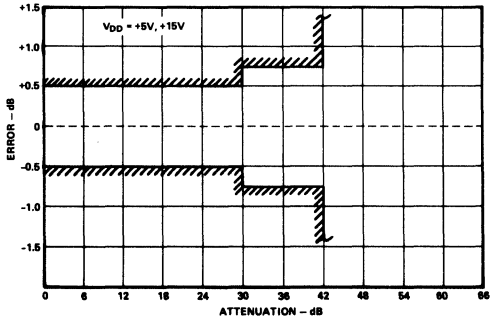
AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not subject to test.

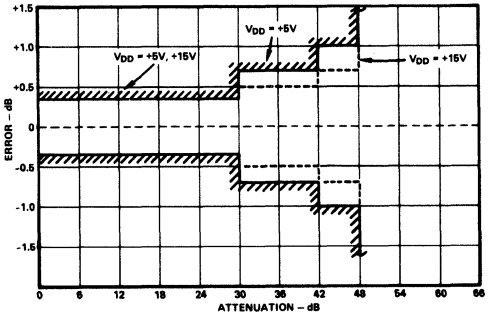
V_{DD} = +5V or +15V, V_{IN} = −10V except where stated, I_{OUT} = AGND = DGND = 0V, output amplifier AD544 except where stated.

PARAMETER		T_A = +25°C		T_A = T_{min}, T_{max}		UNITS	
		V_{DD} = +5V	V_{DD} = +15V	V_{DD} = +5V	V_{DD} = +15V		
DC Supply Rejection, ΔGain/ΔV_{DD}		0.01	0.005	0.01	0.005	dB per % max	ΔV_{DD} = ±10%, Input code = 100000
Propagation Delay		1.8	0.4	2.2	0.5	μs max	Full Scale Change
Digital to Analog Glitch Impulse		225	1200	–	–	nV secs typ	Measured with ADLH0032CG as output amplifier for input code transition 100000 to 000000. C1 of Figure 1 is 0pF.
Output Capacitance (Pin 14)		100	100	100	100	pF max	
Input Capacitance Pin 12 and Pin 13		7	7	7	7	pF max	
Feedthrough at 1kHz	L/C/U Grade	−86	−86	−68	−68	dB max	Feedthrough is also deter-
	K/B/T Grade	−80	−80	−63	−63	dB max	mined by circuit layout
Total Harmonic Distortion		−85	−85	−85	−85	dB typ	V_{IN} = 6V rms
Intermodulation Distortion		−79	−79	−79	−79	dB typ	per DIN 45403 Blatt 4
Output Noise Voltage Density		70	70	70	70	nV/√Hz max	Includes AD544 amplifier noise
Digital Input Capacitance		7	7	7	7	pF max	

Specifications subject to change without notice.



Accuracy Specification for K/B/T Grade Devices at T_A = +25°C



Accuracy Specification for L/C/U Grade Devices at T_A = +25°C

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

V_{DD} (to DGND) . . . . . +17V
V_{IN} (to AGND) . . . . . ±35V
Digital Input Voltage to DGND . . . . . −0.3V to V_{DD} +0.3V
I_{OUT} to AGND . . . . . −0.3V to V_{DD}
AGND to DGND . . . . . 0 to V_{DD}
DGND to AGND . . . . . 0 to V_{DD}
Power Dissipation (Any Package)
To +75°C . . . . . 450 mW
Derates Above +75°C by . . . . . 6mW/°C

Operating Temperature Range
Commercial (K, L Versions) . . . . . 0 to +70°C
Industrial (B, C Versions) . . . . . −25°C to +85°C
Extended (T, U Versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periodsmay affect device reliability.

CAUTION
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RESOLUTION: Nominal change in attenuation when moving between two adjacent binary codes.

MONOTONICITY: The device is monotonic if the analog output decreases (or remains constant) as the digital code increases.

FEEDTHROUGH ERROR: That portion of the input signal which reaches the output when all digital inputs are high. See section on Applications.

OUTPUT LEAKAGE CURRENT: Current which appears on the I_{OUT} terminal with all digital inputs high.

TOTAL HARMONIC DISTORTION: Is a measure of the harmonics introduced by the circuit when a pure sinusoid is applied to the input. It is expressed as the harmonic energy divided by the fundamental energy at the output.

ACCURACY: Is the difference (measured in dB) between the ideal transfer function as listed in Table 1 and the actual transfer function as measured with the device.

OUTPUT CAPACITANCE: Capacitance from I_{OUT} to ground.

DIGITAL-TO-ANALOG GLITCH IMPULSE: The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-Secs or nV-Secs depending upon whether the glitch is measured as a current or voltage signal. Digital charge injection is measured with V_{IN} = AGND.

PROPAGATION DELAY: This is a measure of the internal delays of the circuit and is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

INTERMODULATION DISTORTION: Is a measure of the interaction w hich takes place within the circuit between two sinusoids applied simultaneously to the input.

The reader is referred to Hewlett Packard Application Note 192 for further information.

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CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7118 consists of a 17-bit R-2R CMOS multiplying D/A converter with extensive digital input logic. The logic translates the 6-bit binary input into a 17-bit word which is used to drive the D/A converter. Table I gives the nominal output voltages (and levels relative to 0dB = 10V) for all possible input codes. The transfer function for the circuit of Figure 1 is given by:

$$V_O = -V_{IN}\ 10\ \exp - \left\{\frac{1.5N}{20}\right\}$$

$$\text{or } \left|\frac{V_O}{V_{IN}}\right|_{dB} = -1.5N$$

where N is the binary input for values 0 to 57. For $60 \leqslant N \leqslant 63$ the output is zero. See note 3 at bottom of Table 1.

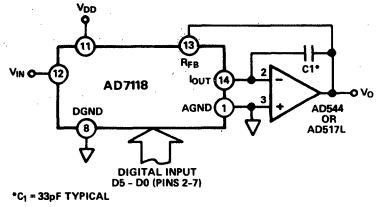


Figure 1. Typical Circuit Configuration

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows a simplified circuit of the D/A converter section of the AD7118 and Figure 3 gives an approximate equivalent circuit.

The current source $I_{LEAKAGE}$ is composed of surface and junction leakages and as with most semiconductor devices, roughly doubles every 10°C—see Figure 10. The resistor R_O as shown in Figure 3 is the equivalent output resistance of the device which varies with input code (excluding all 0's code) from 0.8R to 2R. R is typically 12kΩ. C_{OUT} is the capacitance due to the N channel switches and varies from about 50pF to 80pF depending upon the digital input. For further information on CMOS multiplying D/A converters refer to "Application Guide to CMOS Multiplying D/A Converters" which is available from Analog Devices, Publication Number G479–15–8/78.

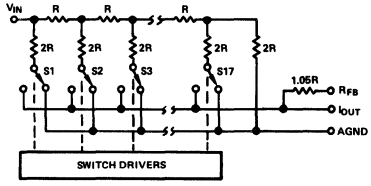


Figure 2. Simplified D/A Circuit of AD7118

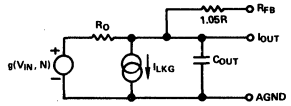


Figure 3. Equivalent Analog Output Circuit of AD7118

N	Digital Input D5 D0	Attenuation dB	V_{OUT}[1]	N	Digital Input	Attenuation	V_{OUT}[1]
0	00 00 00	0.0	10.00	31	01 11 11	46.5	0.0473
1	00 00 01	1.5	8.414	32	10 00 00	48.0	0.0398
2	00 00 10	3.0	7.079	33	10 00 01	49.5	0.0335
3	00 00 11	4.5	5.957	34	10 00 10	51.0	0.0282
4	00 01 00	6.0	5.012	35	10 00 11	52.5	0.0237
5	00 01 01	7.5	4.217	36	10 01 00	54.0	0.0200
6	00 01 10	9.0	3.548	37	10 01 01	55.5	0.0168
7	00 01 11	10.5	2.985	38	10 01 10	57.0	0.0141
8	00 10 00	12.0	2.512	39	10 01 11	58.5	0.0119
9	00 10 01	13.5	2.113	40	10 10 00	60.0	0.0100
10	00 10 10	15.0	1.778	41	10 10 01	61.5	0.00841
11	00 10 11	16.5	1.496	42	10 10 10	63.0	0.00708
12	00 11 00	18.0	1.259	43	10 10 11	64.5	0.00596
13	00 11 01	19.5	1.059	44	10 11 00	66.0	0.00501
14	00 11 10	21.0	0.891	45	10 11 01	67.5	0.00422
15	00 11 11	22.5	0.750	46	10 11 10	69.0	0.00355
16	01 00 00	24.0	0.631	47	10 11 11	70.5	0.00299
17	01 00 01	25.5	0.531	48	11 00 00	72.0	0.00251
18	01 00 10	27.0	0.447	49	11 00 01	73.5	0.00211
19	01 00 11	28.5	0.376	50	11 00 10	75.0	0.00178
20	01 01 00	30.0	0.316	51	11 00 11	76.5	0.00150
21	01 01 01	31.5	0.266	52	11 01 00	78.0	0.00126
22	01 01 10	33.0	0.224	53	11 01 01	79.5	0.00106
23	01 01 11	34.5	0.188	54	11 01 10	81.0	0.000891
24	01 10 00	36.0	0.158	55	11 01 11	82.5	0.000750
25	01 10 01	37.5	0.133	56	11 10 00	84.0	0.000631
26	01 10 10	39.0	0.112	57	11 10 01	85.5	0.000531
27	01 10 11	40.5	0.0944	58	11 10 10	87.0	0.000447
28	01 11 00	42.0	0.0794	59	11 10 11	88.5	0.000376
29	01 11 01	43.5	0.0668	60	11 11 XX[2]	∞	
30	01 11 10	45.0	0.0562				

NOTES
[1] V_{IN} = −10V dc
[2] X = 1 or 0. Output is fully muted for N⩾60
[3] Monotonic operation is not guaranteed for N = 58, 59

Table I. Ideal Attenuation vs. Input Code

DYNAMIC PERFORMANCE

The dynamic performance of the AD7118 will depend upon the gain and phase characteristics of the output amplifier, together with the optimum choice of PC board layout and decoupling components. Figure 4 shows a printed circuit layout which minimizes feedthrough from V_{IN} to the output in multiplying applications. Circuit layout is most important if the optimum performance of the AD7118 is to be achieved. Most application problems stem from either poor layout, grounding errors, or inappropriate choice of amplifier.

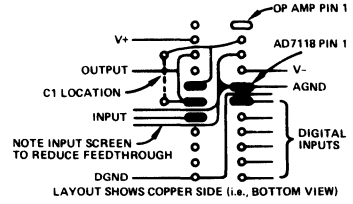


Figure 4. Suggested Layout for AD7118 and Op Amp

It is recommended that when using the AD7118 with a high speed amplifier, a capacitor C1 be connected in the feedback path as shown in Figure 1. This capacitor, which should be between 30pF and 50pF, compensates for the phase lag introduced by the output capacitance of the D/A converter. Figures 5 and 6 show the performance of the AD7118 using the AD517, a fully compensated high gain superbeta amplifier, and the AD544, a fast FET input amplifier. The performance without C1 is shown in the middle trace and the response with C1 in circuit is shown in the bottom trace.

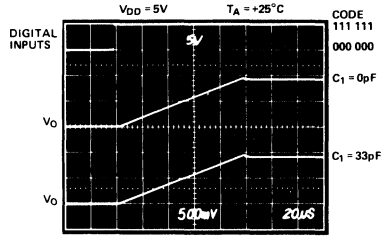


Figure 5. Response of AD7118 with AD517L

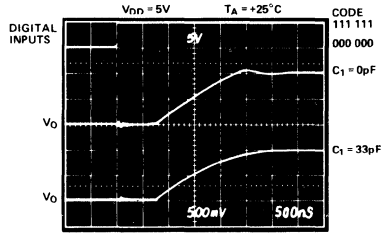


Figure 6. Response of AD7118 with AD544S

In conventional CMOS D/A converter design parasitic capacitance in the N-channel D/A converter switches can give rise to glitches on the D/A converter output. These glitches result from digital feedthrough. The AD7118 has been designed to minimize these glitches as much as possible. It is recommended that for minimum glitch energy the AD7118 be operated with V_{DD} = 5V. This will reduce the available energy for coupling across the parasitic capacitance. It should be noted that the accuracy of the AD7118 improves as V_{DD} is increased (see Figure 8) but the device maintains monotonic behavior to at least -66dB in the range $5 \leqslant V_{DD} \leqslant 15$ volts.

For operation beyond 250kHz, capacitor C1 may be reduced in value. This gives an increase in bandwidth at the expense of a poorer transient response as shown in Figures 6 and 11. In circuits where C1 is not included the high frequency roll-off point is primarily determined by the characteristics of the output amplifier and not the AD7118.

Feedthrough and absolute accuracy for attenuation levels beyond 42dB are sensitive to output leakage current effects. For this reason it is recommended that the operating temperature of the AD7118 be kept as close to 25°C as is practically possible, particularly where the device's performance at high attenuation levels is important. A typical plot of leakage current vs. temperature is shown in Figure 10.

Some solder fluxes and cleaning materials can form slightly conductive films which cause leakage effects between analog input and output. The user is cautioned to ensure that the manufacturing process for circuits using the AD7118 does not allow such films to form. Otherwise the feedthrough, accuracy and maximum usable range will be affected.

STATIC ACCURACY PERFORMANCE

The D/A converter section of the AD7118 consists of a 17-bit R-2R type converter. To obtain optimum static performance at this level of resolution it is necessary to pay great attention to amplifier selection, circuit grounding, etc.

Amplifier input bias current results in a dc offset at the output of the amplifier due to the current flowing through the feedback resistor R_{FB}. It is recommended that an amplifier with an input bias current of less than 10nA be used (e.g., AD517 or AD544) to minimize this offset.

Another error arises from the output amplifier's input offset voltage. The amplifier is operated with a fixed feedback resistance, but the equivalent source impedance (the AD7118 output impedance) varies as a function of attenuation level. This has the effect of varying the "noise" gain of the amplifier, thus creating a varying error due to amplifier offset voltage. To achieve an output offset error less than one half the smallest step size, it is recommended that an amplifier with less than 50µV of input offset be used (such as the AD517 or AD OP-07).

If dc accuracy is not critical in the application, it should be noted that amplifiers with offset voltage up to approximately 2 millivolts can be used. Amplifiers with higher offset voltage may cause audible "thumps" due to dc output changes.

The AD7118 accuracy is specified and tested using only the internal feedback resistor. It is not recommended that "gain" trim resistors be used with the AD7118 because the internal logic of the circuit executes a proprietary algorithm which approximates a logarithmic curve with a binary D/A converter: as a result no single point on the attenuator transfer function can be guaranteed to lie exactly on the theoretical curve. Any "gain-error" (i.e., mismatch of R_{FB} to the R-2R ladder) that may exist in the AD7118 D/A converter circuit results in a constant attenuation error over the whole range. Since the gain-error of CMOS multiplying D/A converters is normally less than 1%, the accuracy error contribution due to "gain-error" effects is normally less than 0.09dB.

AD7118—Typical Performance Characteristics

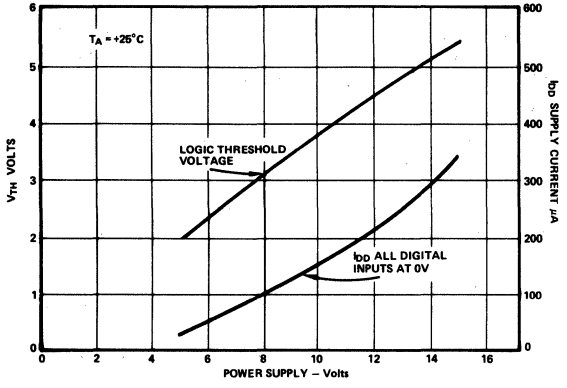


Figure 7. Digital Threshold & Power Supply Current vs Power Supply

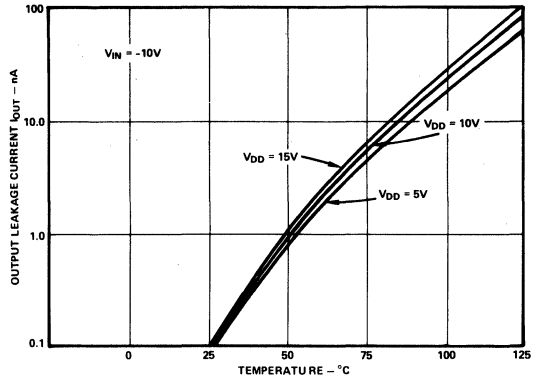


Figure 10. Output Leakage Current vs Temperature at V_{DD} = 5, 10 and 15 Volts

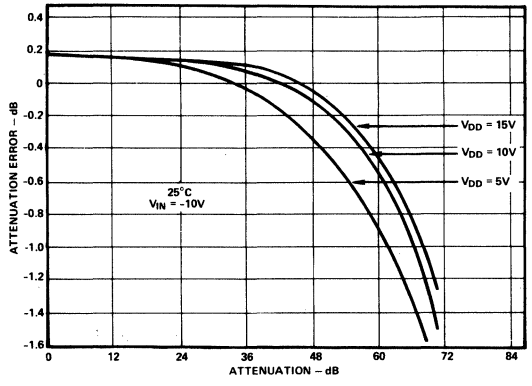


Figure 8. DC Attenuation Error vs. Attenuation & V_{DD}

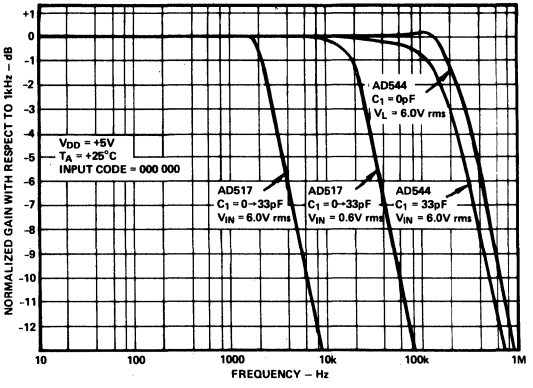


Figure 11. Frequency Response with AD544 and AD517 Amplifiers

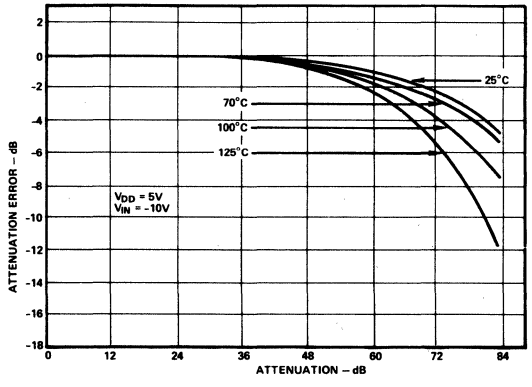


Figure 9. DC Attenuation Error vs. Attenuation & Temperature

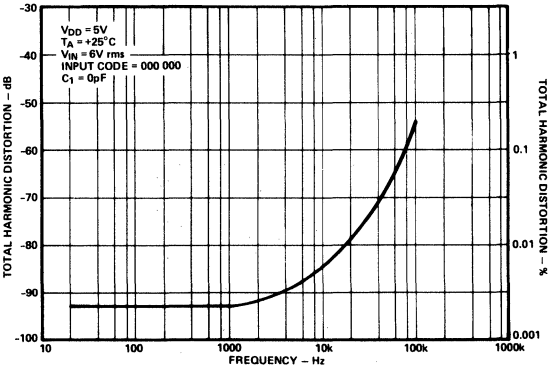


Figure 12. Distortion vs. Frequency Using AD544 Amplifier

ANALOG DEVICES

Matched Monolithic Quad Transistor

MAT-04

FEATURES

- **Low Offset Voltage ..... 200μV Max**
- **High Current Gain ..... 400 Min**
- **Excellent Current Gain Match ..... 2% Max**
- **Low Noise Voltage at 100Hz, 1mA ..... 2.5nV/ Hz Max**
- **Excellent Log Conformance ..... rBE = 0.6Ω Max**
- **Matching Guaranteed for All Transistors**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE CERDIP 14-PIN	PACKAGE PLASTIC 14-PIN	OPERATING TEMPERATURE RANGE
200	MAT04AY*	—	MIL
200	MAT04EY	—	IND
400	MAT04BY*	—	MIL
400	MAT04FY	MAT04FP	XIND
400	—	MAT04FS††	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

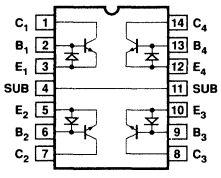
GENERAL DESCRIPTION

The MAT-04 is a quad monolithic NPN transistor that offers excellent parametric matching for precision amplifier and non-linear circuit applications. Performance characteristics of the MAT-04 include high gain (400 minimum) over a wide range of collector current, low noise (2.5nV/$\sqrt{\text{Hz}}$ maximum at 100Hz, I_C = 1 mA) and excellent logarithmic conformance. The MAT-04 also features a low offset voltage of 200μV and tight current gain matching, to within 2%. Each transistor of the MAT-04 is individually tested to data sheet specifications. For matching parameters (offset voltage, input offset current, and gain match), each of the dual transistor combinations are verified to meet stated limits. Device performance is guaranteed at 25°C and over the industrial and military temperature ranges.

The long-term stability of matching parameters is guaranteed by the protection diodes across the base-emitter junction of each transistor. These diodes prevent degradation of beta and matching characteristics due to reverse bias base-emitter current.

The superior logarithmic conformance and accurate matching characteristics of the MAT-04 makes it an excellent choice for use in log and antilog circuits. The MAT-04 is an ideal choice in applications where low noise and high gain are required.

PIN CONNECTIONS



14-PIN CERDIP (Y-Suffix)

14-PIN PLASTIC DIP (P-Suffix)

14-PIN SO (S-Suffix)

ABSOLUTE MAXIMUM RATINGS (Note 1)

Collector-Base Voltage (BV_{CBO}) 40V
Collector-Emitter Voltage (BV_{CEO}) 40V
Collector-Collector Voltage (BV_{CC}) 40V
Emitter-Emitter Voltage (BV_{EE}) 40V
Collector Current 30mA
Emitter Current 30mA
Substrate (Pin-4 to Pin-11) Current 30mA
Operating Temperature Range
MAT-04AY, BY ..... –55°C TO +125°C
MAT-04EY ..... –25°C TO +85°C
MAT-04FY,FP,FS ..... –40°C to +85°C
Storage Temperature
Y Package ..... –65°C to +150°C
P Package ..... –65°C to +125°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
14-Pin CERDIP (Y)	108	16	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
14-Pin SO (S)	120	36	°C/W

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

7

ELECTRICAL CHARACTERISTICS at T_A = 25°C unless otherwise noted. Each transistor is individually tested. For matching parameters (V_{OS}, I_{OS}, Δh_{FE}) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-04A/E MIN	MAT-04A/E TYP	MAT-04A/E MAX	MAT-04B/F MIN	MAT-04B/F TYP	MAT-04B/F MAX	UNITS
Current Gain	h_{FE}	10μA ≤ I_C ≤ 1mA 0V ≤ V_{CB} ≤ 30V (Note 1)	400	800	—	300	600	—	
Current Gain Match	Δh_{FE}	I_C = 100μA 0V ≤ V_{CB} ≤ 30V (Note 2)	—	0.5	2	—	1	4	%
Offset Voltage	V_{OS}	10μA ≤ I_C ≤ 1mA 0V ≤ V_{CB} ≤ 30V (Note 4)	—	50	200	—	100	400	μV
Offset Voltage Change vs Collector Current	$\Delta V_{OS}/\Delta I_C$	10μA ≤ I_C ≤ 1mA V_{CB} = 0V (Note 4)	—	5	25	—	10	50	μV
Offset Voltage Change vs V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	10μA ≤ I_C ≤ 1mA 0V ≤ V_{CB} ≤ 30V (Note 4)	—	50	100	—	100	200	μV
Bulk Emitter Resistance	r_{BE}	10μA ≤ I_C ≤ 1mA V_{CB} = 0V (Note 5)	—	0.4	0.6	—	0.4	0.6	Ω
Input Bias Current	I_B	I_C = 100μA 0V ≤ V_{CB} ≤ 30V	—	125	250	—	165	330	nA
Input Offset Current	I_{OS}	I_C = 100μA V_{CB} = 0V	—	0.6	5	—	2	13	nA
Breakdown Voltage	BV_{CEO}	I_C = 10μA	40	—	—	40	—	—	V
Collector Saturation Voltage	$V_{CE(SAT)}$	I_B = 100μA I_C = 1mA	—	0.03	0.06	—	0.03	0.06	V
Collector-Base Leakage Current	I_{CBO}	V_{CB} = 40V	—	5	—	—	5	—	pA
Noise Voltage Density	e_n	V_{CB} = 0V f_O = 10Hz I_C = 1mA f_O = 100Hz (Note 3) f_O = 1kHz	— — —	2 1.8 1.8	3 2.5 2.5	— — —	2 1.8 1.8	4 3 3	nV/√Hz
Gain Bandwidth Product	f_T	I_C = 1mA V_{CE} = 10V	—	300	—	—	300	—	MHz
Output Capacitance	C_{OBO}	V_{CB} = 15V I_E = 0 f = 1MHz	—	10	—	—	10	—	pF
Input Capacitance	C_{EBO}	V_{BE} = 0V I_C = 0 f = 1MHz	—	40	—	—	40	—	pF

NOTES:

1. Current gain measured at I_C = 10μA, 100μA and 1mA.
2. Current gain match is defined as: $\Delta h_{FE} = \frac{100\,(\Delta I_B)\,(h_{FE}\,\text{min})}{I_C}$
3. Sample tested.
4. Measured at I_C = 10μA and guaranteed by design over the specified range of I_C.
5. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $-25°C \le T_A \le +85°C$ for MAT-04E, $-40°C \le T_A \le +85°C$ for MAT-04F, unless otherwise noted. Each transistor is individually tested. For matching parameters (V_{OS}, I_{OS}) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

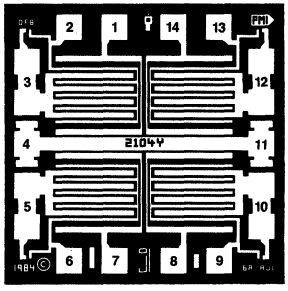
			MAT-04E			MAT-04F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Current Gain	h_{FE}	$10\mu A \le I_C \le 1mA$ $0V \le V_{CB} \le 30V$ (Note 1)	225	625	—	200	500	—	
Offset Voltage	V_{OS}	$10\mu A \le I_C \le 1mA$ $0V \le V_{CB} \le 30V$ (Note 3)	—	60	260	—	120	520	μV
Average Offset Voltage Drift	TCV_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$ (Note 2)	—	0.2	1	—	0.4	2	μV/°C
Input Bias Current	I_B	$I_C = 100\mu A$ $0V \le V_{CB} \le 30V$	—	160	445	—	200	500	nA
Input Offset Current	I_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$	—	4	20	—	8	40	nA
Average Offset Current Drift	TCI_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$	—	50	—	—	100	—	pA/°C
Breakdown Voltage	BV_{CEO}	$I_C = 10\mu A$	40	—	—	40	—	—	V
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = 40V$	—	0.5	—	—	0.5	—	nA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = 40V$	—	5	—	—	5	—	nA
Collector-Substrate Leakage Current	I_{CS}	$V_{CS} = 40V$	—	0.7	—	—	0.7	—	nA

ELECTRICAL CHARACTERISTICS at $-55°C \le T_A \le 125°C$ unless otherwise noted. Each transistor is individually tested. For matching parameters (V_{OS}, I_{OS}) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

			MAT-04A			MAT-04B			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Current Gain	h_{FE}	$10\mu A \le I_C \le 1mA$ $0V \le V_{CB} \le 30V$ (Note 1)	175	475	—	125	425	—	
Offset Voltage	V_{OS}	$10\mu A \le I_C \le 1mA$ $0V \le V_{CB} \le 30V$ (Note 3)	—	70	300	—	140	600	μV
Average Offset Voltage Drift	TCV_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$ (Note 2)	—	0.2	1	—	0.4	2	μV/°C
Input Bias Current	I_B	$I_C = 100\mu A$ $0V \le V_{CB} \le 30V$	—	210	570	—	235	800	nA
Input Offset Current	I_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$	—	6	30	—	12	60	nA
Average Offset Current Drift	TCI_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$	—	50	—	—	100	—	pA/°C
Breakdown Voltage	BV_{CEO}	$I_C = 10\mu A$	40	—	—	40	—	—	V
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = 40V$	—	5	—	—	5	—	nA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = 40V$	—	100	—	—	100	—	nA
Collector-Substrate Leakage Current	I_{CS}	$V_{CS} = 40V$	—	7	—	—	7	—	nA

NOTES:
1. Current gain measured at $I_C = 10\mu A$, $100\mu A$ and 1mA.
2. Guaranteed by V_{OS} test ($TCV_{OS} \le V_{OS}/T$ for $V_{OS} << V_{BE}$) $T = 298°K$ for $T_A = 25°C$.
3. Measured at $I_C = 10\mu A$ and guaranteed by design over the specified range of I_C.

DICE CHARACTERISTICS



1. Q_1 COLLECTOR
2. Q_1 BASE
3. Q_1 EMITTER
4. SUBSTRATE
5. Q_2 EMITTER
6. Q_2 BASE
7. Q_2 COLLECTOR
8. Q_3 COLLECTOR
9. Q_3 BASE
10. Q_3 EMITTER
11. SUBSTRATE
12. Q_4 EMITTER
13. Q_4 BASE
14. Q_4 COLLECTOR

DIE SIZE 0.060 x 0.060 inch, 3600 sq. mils
(1.52 x 1.52 mm, 2.31 sq. mm)

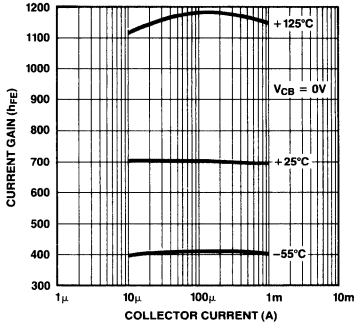
WAFER TEST LIMITS at T_A = +25°C unless otherwise noted. Each transistor is individually tested. For matching parameters (V_{OS}, I_{OS}, Δh_{FE}) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-04N LIMITS	UNITS
Current Gain	h_{FE}	I_C = 100µA 0V ≤ V_{CB} ≤ 30V	300	MIN
Current Gain Match	Δh_{FE}	I_C = 100µA, V_{CB} = 0V	4	% MAX
Offset Voltage	V_{OS}	10µA ≤ I_C ≤ 1mA 0V ≤ V_{CB} ≤ 30V (Note 1)	400	µV MAX
Offset Voltage Change vs Collector Current	$\Delta V_{OS}/\Delta I_C$	10µA ≤ I_C ≤ 1mA V_{CB} = 0V (Note 1)	50	µV MAX
Offset Voltage Change us VCB	$\Delta V_{OS}/\Delta V_{CB}$	10µA ≤ I_C ≤ 1mA 0V ≤ V_{CB} ≤ 30V (Note 1)	200	µV MAX
Bulk Emitter Resistance	r_{BE}	10µA ≤ I_C ≤ 1mA V_{CB} = 0V (Note 2)	0.6	Ω MAX
Collector Saturation Voltage	$V_{CE(SAT)}$	I_B = 100µA I_C = 1mA	0.06	V MAX
Input Bias Current	I_B	I_C = 100µA 0V ≤ V_{CB} ≤ 30V	330	nA MAX
Input Offset Current	I_{OS}	I_C = 100µA V_{CB} = 0V	13	nA MAX
Breakdown Voltage	BV_{CEO}	I_C = 10µA	40	V MIN

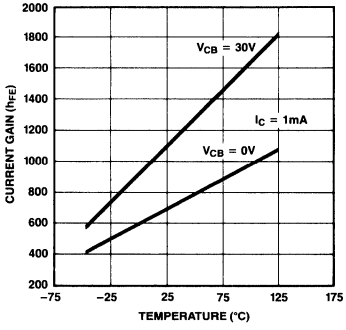
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

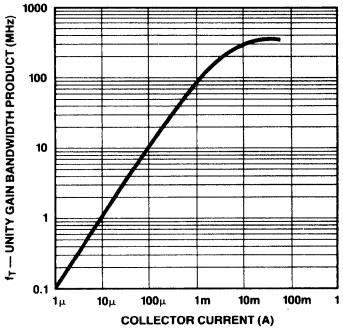
CURRENT GAIN vs COLLECTOR CURRENT



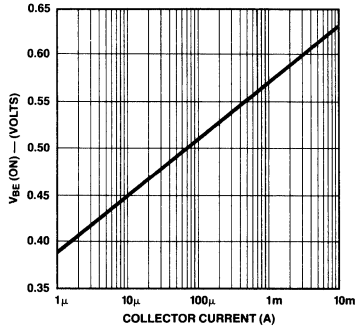
CURRENT GAIN vs TEMPERATURE



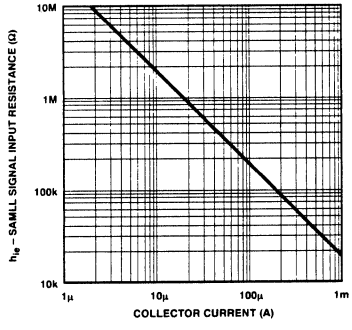
GAIN BANDWIDTH vs COLLECTOR CURRENT



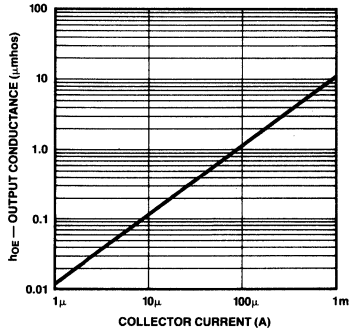
BASE-EMITTER-ON-VOLTAGE vs COLLECTOR CURRENT



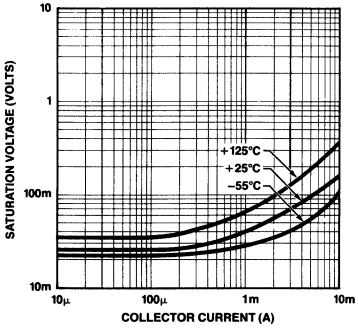
SMALL SIGNAL INPUT RESISTANCE (h_{ie}) vs COLLECTOR CURRENT



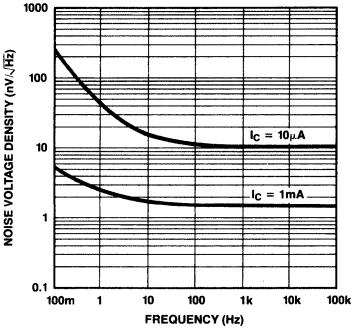
SMALL SIGNAL OUTPUT CONDUCTANCE vs COLLECTOR CURRENT



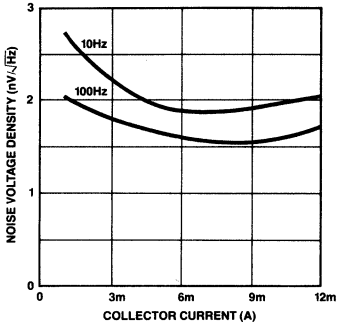
SATURATION VOLTAGE vs COLLECTOR CURRENT



NOISE VOLTAGE DENSITY vs FREQUENCY



NOISE VOLTAGE DENSITY vs COLLECTOR CURRENT



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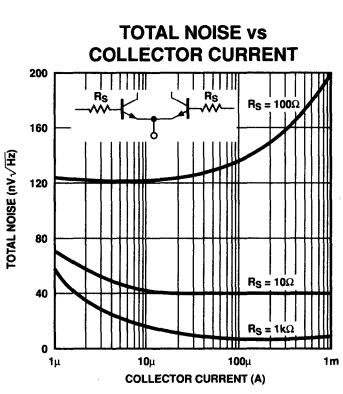
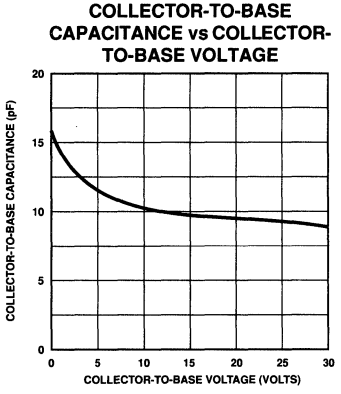
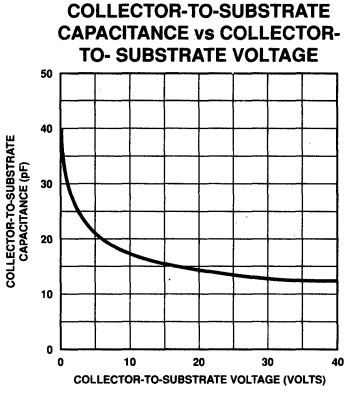
TYPICAL PERFORMANCE CHARACTERISTICS *Continued*







APPLICATION NOTES

It is recommended that one of the substrate pins (Pins 4 and 11) be tied to the most negative circuit potential to minimize coupling between devices. Pins 4 and 11 are internally connected.

APPLICATIONS

CURRENT SOURCES

The MAT-04 can be used to implement a variety of high impedance current mirrors as shown in Figures 1, 2, and 3. These current mirrors can be used as biasing elements and load devices for amplifier stages.

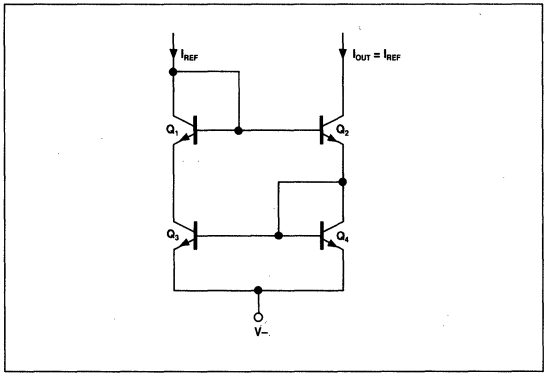


FIGURE 1: *Unity Gain Current Mirror, $I_{OUT} = I_{REF}$*

The unity-gain current mirror of Figure 1, using a MAT-04AY, has an accuracy of better than 1% and an output impedance of over 100MΩ at 100µA. Figures 2 and 3 show modified current mirrors designed for a current gain of two, and one-half respectively. The accuracy of these mirrors is reduced from that of the unity-gain source due to base current errors but is still better than 2%.

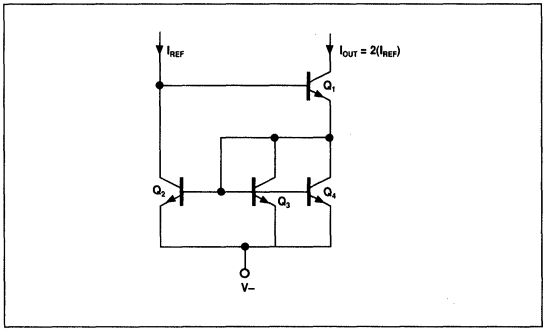


FIGURE 2: *Current Mirror, $I_{OUT} = 2(I_{REF})$*

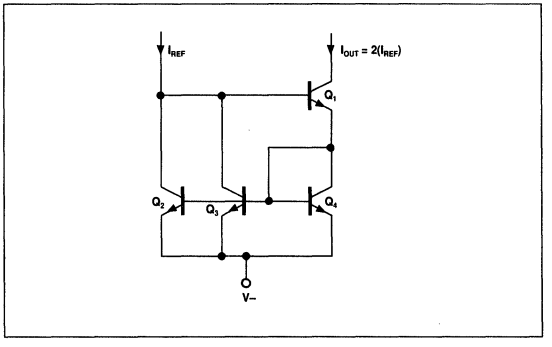
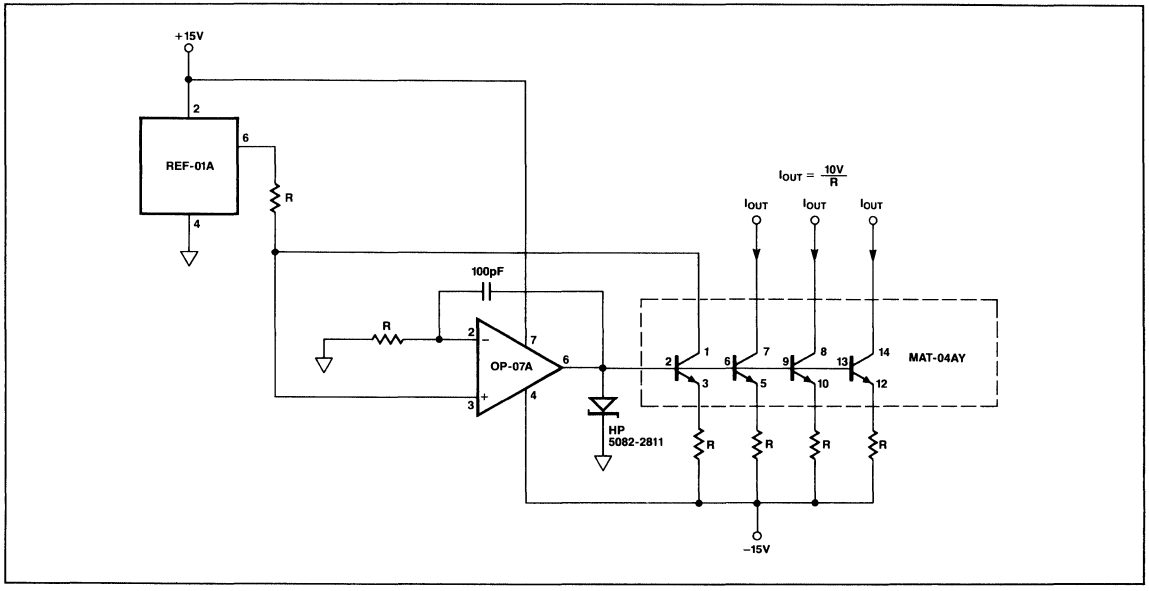


FIGURE 2: *Current Mirror, $I_{OUT} = 2(I_{REF})$*

Figure 4 is a temperature independent current sink that has an accuracy of better than 1% over the military temperature range at an output current of 100µA to 1 mA. The Schottky diode acts as a clamp to insure correct circuit start-up at power on. The resistors used in this circuit should be 1% metal-film type.

FIGURE 4: Temperature Independent Current Sink, I_{OUT} = 10V/RΩ



NONLINEAR FUNCTIONS

An application where precision matched-transistors are a powerful tool is in the generation of nonlinear functions. These circuits are based on the transistor's logarithmic property which takes the following idealized form:

$$V_{BE} = \frac{kT}{q} \ln \frac{I_C}{I_S}$$

The MAT-04, with its excellent logarithmic conformance, maintains this idealized function over many decades of collector current. This, in addition to the stringent parametric matching of the MAT-04, enables the implementation of extremely accurate log/antilog circuits.

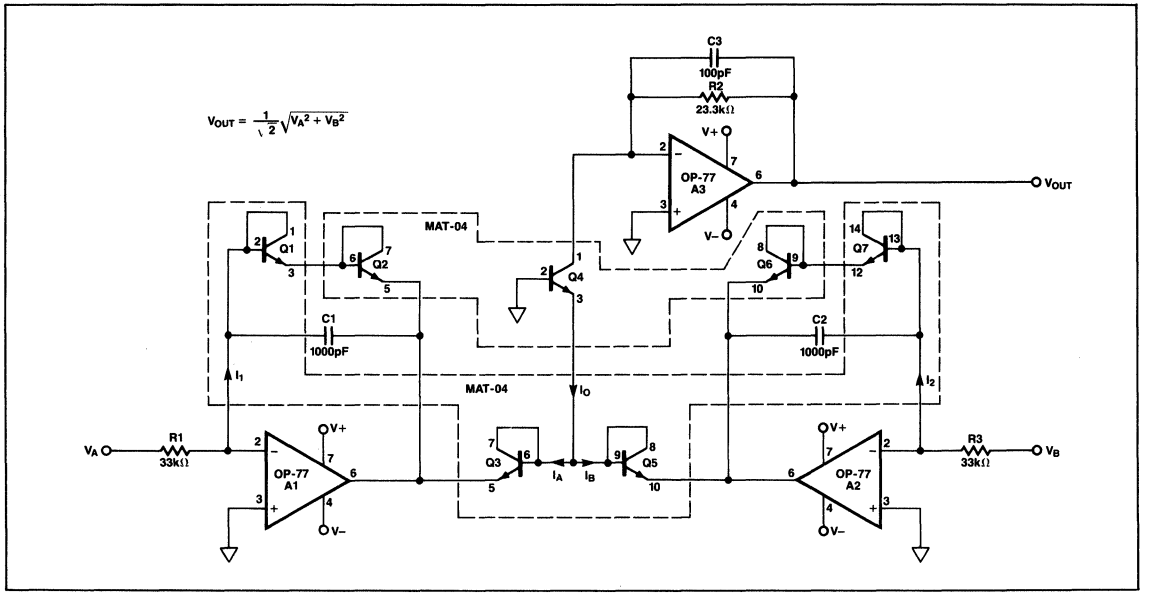
The circuit of Figure 5 is a vector summer that adds and subtracts logged inputs to generate the following transfer function:

$$V_{OUT} = \frac{1}{\sqrt{2}} \sqrt{V_A^2 + V_B^2}$$

This circuit uses two MAT-04AYs and maintains an accuracy of better than 0.5% over an input range of 10mV to 10V. The layout of the MAT-04s reduces errors due to matching and temperature differences between the two precision quad matched-transistors.

Op amps A1 and A2 translate the input voltages into logarithmic valued currents (I_A and I_B in Figure 5) that flow through transistor Q_3 and Q_5. These currents are summed by transistor Q_4 ($I_O = I_A + I_B = \sqrt{I_1^2 + I_2^2}$) which feeds the current-to-voltage converter consisting of op amp A3. To maintain accuracy, 1% metal-film resistors should be used.

FIGURE 5: Vector Summer



LOW NOISE, HIGH SPEED INSTRUMENTATION AMPLIFIER

The circuit of Figure 6 is a very low noise, high speed amplifier, ideal for use in precision transducer and professional audio applications. The performance of the amplifier is summarized in Table I. Figure 7 shows the input referred spot noise over the 0-25kHz bandwidth to be flat at 1.2nV/ $\sqrt{Hz}$. Figure 8 highlights the low 1/f noise corner at 2Hz.

The circuit uses a high speed op amp, the OP-17, preceded by an input amplifier. This consists of a precision dual matched-transistor, the MAT-02, and a feedback V-to-I converter, the MAT-04. The arrangement of the MAT-04 is known as a "linearized cross quad" which performs the voltage-to-current conversion. The OP-17 acts as an overall nulling amplifier to complete the feedback loop. Resistors R1, R2, and R3, R4 form voltage dividers that attenuate the output voltage swing since the "cross quad" arrangement has a limited input range. Biasing for the input stage is set by zener diode Z1. At low currents the effective zener voltage is about 3.3V due to the soft knee characteristic of the zener diode. This results in a bias current of 530μA per side for the input stage. The gain of this amplifier with the values shown in Figure 6 is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{33000}{R_G}$$

TABLE I: Instrumentation Amplifier Characteristics

Input Noise Voltage Density	G = 1000	1.2nV/ $\sqrt{Hz}$
	G = 100	3.6nV/ $\sqrt{Hz}$
	G = 10	30nV/ $\sqrt{Hz}$
Bandwidth	G = 500	400kHz
	G = 100	1MHz
	G = 10	1.2MHz
Slew Rate		40V/μs
Common-Mode Rejection	G = 1000	130dB
Distortion	G = 100 f = 20Hz to 20kHz	0.03%
Settling Time	G = 1000	10μs
Power Consumption		350mW

FIGURE 6: Low Noise, High Speed Instrumentation Amplifier

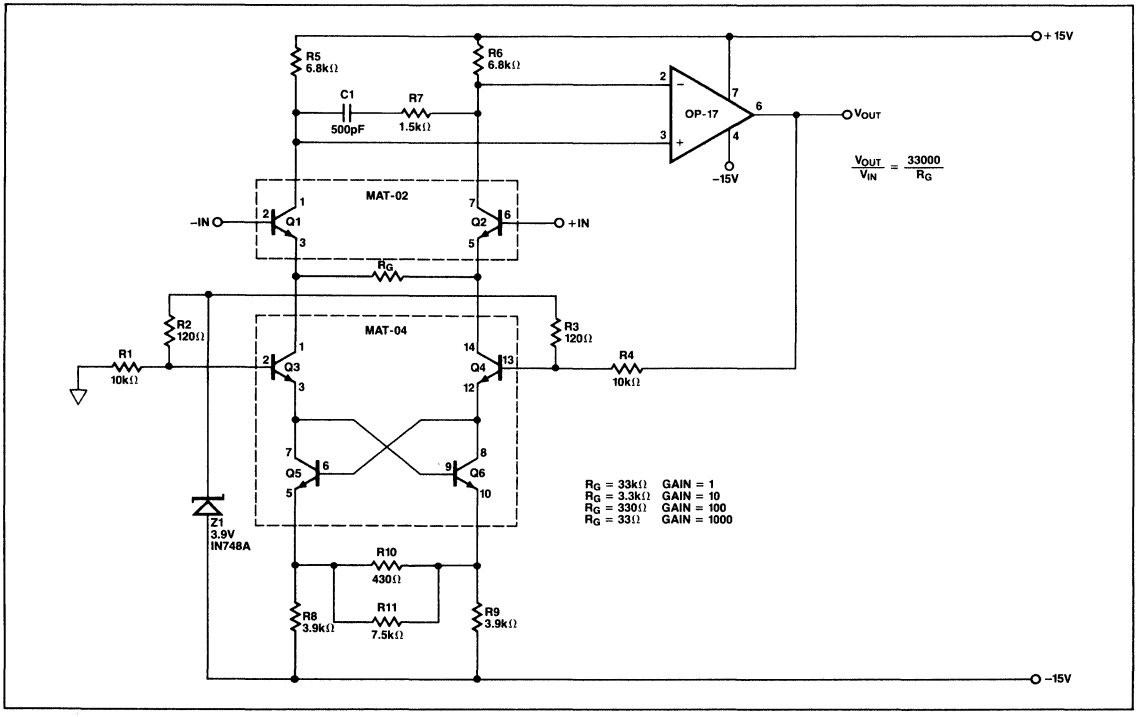
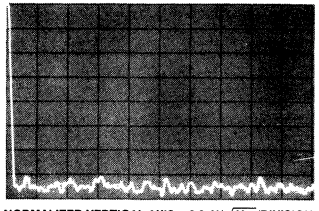
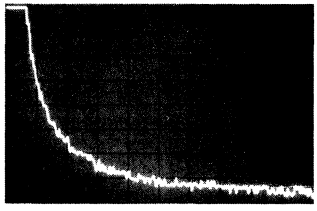


FIGURE 7: Spot Noise of the Instrumentation Amplifier from 0-25kHz at a Gain of 1000



NORMALIZED VERTICAL AXIS = 2.6nV/$\sqrt{Hz}$ /DIVISION
REFERENCED TO INPUT.
HORIZONTAL AXIS = 0 TO 25kHz.

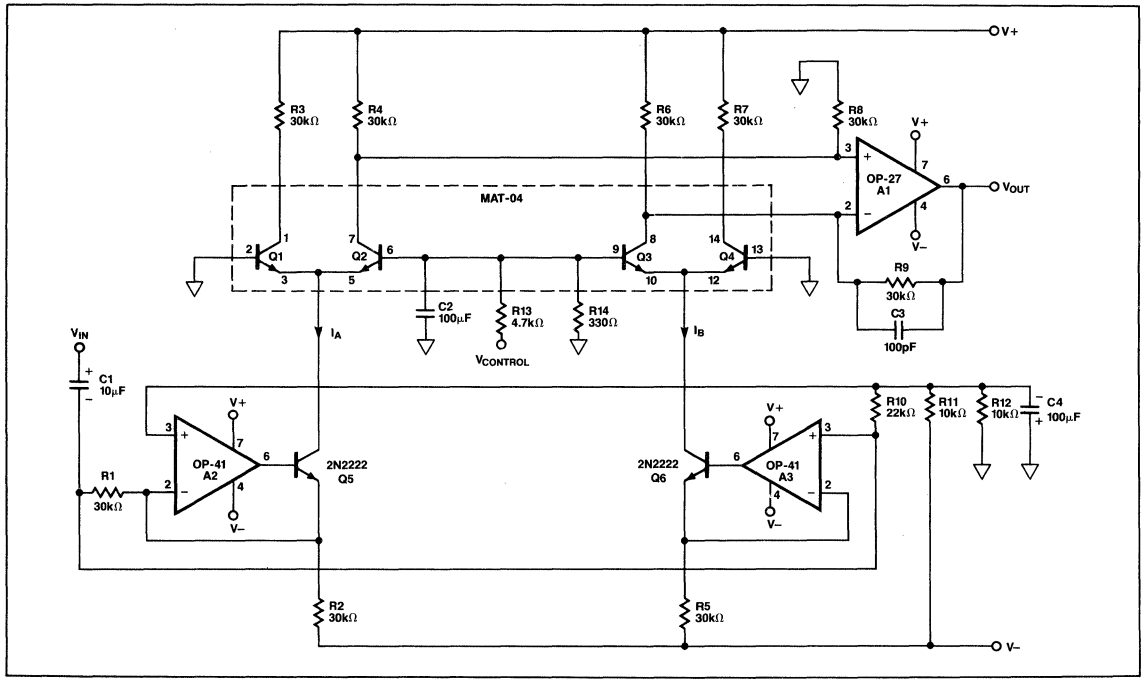
FIGURE 8: Low Frequency Noise Spectrum Showing Low 2Hz Noise Corner. Gain = 1000.



HORIZONTAL AXIS = 0 TO 5Hz

7

FIGURE 9: Voltage-Controlled Attenuator



VOLTAGE-CONTROLLED ATTENUATOR

The voltage-controlled attenuator (VCA) of Figure 9, widely used in professional audio circles, can easily be implemented using a MAT-04. The excellent matching characteristics of the MAT-04 enables the VCA to have a distortion level of under 0.03% over a wide range of control voltages. The VCA accepts a 3V RMS input and easily handles the full 20Hz-20kHz audio bandwidth as shown in Figure 10. Noise level for the VCA is more than 110dB below maximum output.

In the voltage-controlled attenuator, the input signal modulates the stage current of each differential pair. Op amps A2 and A3 in conjunction with transistors Q5 and Q6 form voltage-to-current converters that transform a single input voltage into differential currents which form the stage currents of each differential pair. The control voltage shifts the current between each side of the two differential pairs, regulating the signal level reaching the output stage which consists of op amp A1. Figure 11 shows the increase in signal attenuation as the control voltage becomes more negative.

The ideal transfer function for the voltage-controlled attenuator is:

$$V_{OUT}/V_{IN} = \frac{2}{1 + \exp\left((-V_{CONTROL})\left(\frac{R14}{R13 + R14}\right)\Big/\left(\frac{kT}{q}\right)\right)}$$

Where k = Boltzmann constant 1.38×10^{-23} J/°K
T = temperature in °K
q = electronic charge = 1.602×10^{-19}C

From the transfer function it can be seen that the maximum gain of the circuit is 2 (6dB).

To insure best performance, resistors R2 through R7 should be 1% metal film resistors. Since capacitor C2 can see small amounts of reverse bias when the control voltage is positive, it may be prudent to use a nonpolarized tantalum capacitor.

FIGURE 10: Voltage-Controlled Attenuator, Attenuation vs Frequency

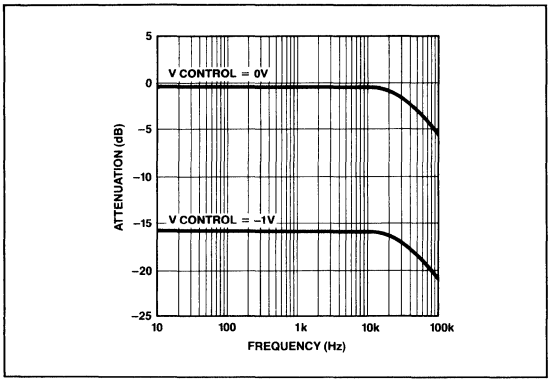
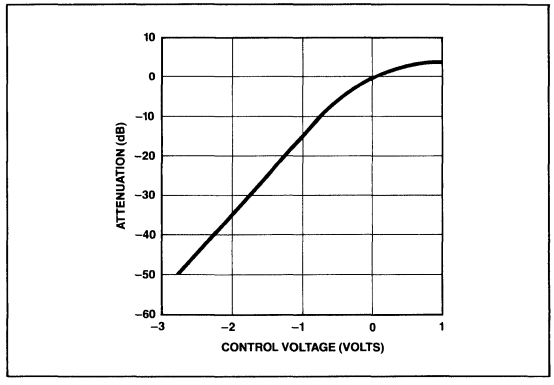


FIGURE 11: Voltage-Controlled Attenuator, Attenuation vs Control Voltage



7

Monolithic Peak Detector with Reset-and-Hold Mode

PKD-01

FEATURES

- **Monolithic Design for Reliability and Low Cost**
- **High Slew Rate** **0.5V/μs**
- **Low Droop Rate**
  - **T_A = 25°C** **0.1mV/ms**
  - **T_A = 125°C** **10mV/ms**
- **Low Zero-Scale Error** **4mV**
- **Digitally Selected Hold and Reset Modes**
- **Reset to Positive or Negative Voltage Levels**
- **Logic Signals TTL and CMOS Compatible**
- **Uncommitted Comparator on Chip**
- **Available in Die Form**

ORDERING INFORMATION†

25°C V_{ZS} (mV)	PACKAGE 14-PIN DUAL-IN-LINE PACKAGE HERMETIC*	PLASTIC	OPERATING TEMPERATURE RANGE
4	PKD01AY*	—	MIL
4	PKD01EY	—	IND
7	PKD01FY	—	IND
4	—	PKD01EP	COM
7	—	PKD01FP	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The PKD-01 tracks an analog input signal until a maximum amplitude is reached. The maximum value is then retained as a peak voltage on a hold capacitor. Being a monolithic circuit, the PKD-01 offers significant performance and package density advantages over hybrid modules and discrete designs without sacrificing system versatility. The matching characteristics attained in a monolithic circuit provide inherent advantages when charge injection and droop rate error reduction are primary goals.

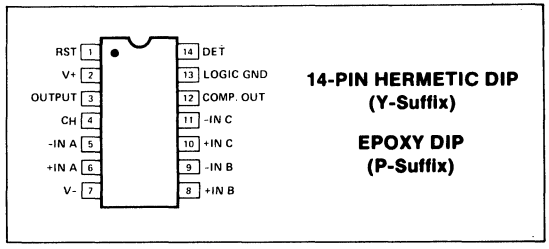
Innovative design techniques maximize the advantages of monolithic technology. Transconductance (g_m) amplifiers were chosen over conventional voltage amplifier circuit building blocks. The "g_m" amplifiers simplify internal frequency compensation, minimize acquisition time and maximize circuit accuracy. Their outputs are easily switched by low glitch current steering circuits. The steered outputs are clamped to reduce charge injection errors upon entering the hold mode or exiting the reset mode. The inherently low zero-scale error is reduced further by active "Zener-Zap" trimming to optimize overall accuracy.

The output buffer amplifier features an FET input stage to reduce droop rate error during lengthy peak hold periods. A bias current cancellation circuit minimizes droop error at high ambient temperatures.

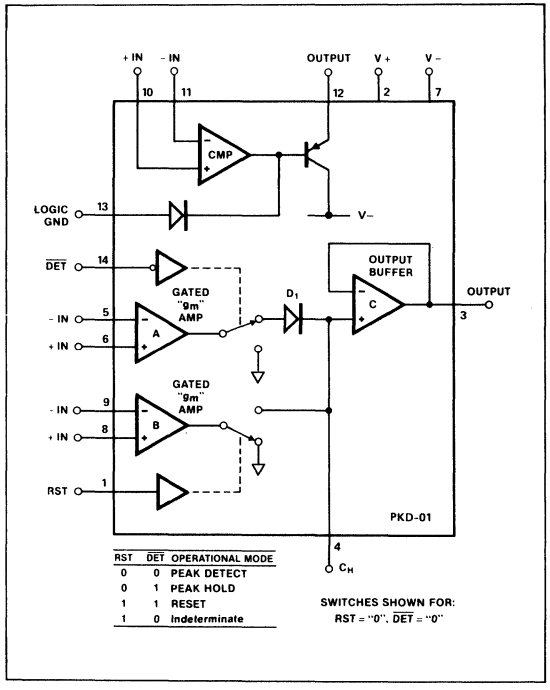
Through the $\overline{DET}$ control pin, new peaks may either be detected or ignored. Detected peaks are presented as positive output levels. Positive or negative peaks may be detected without additional active circuits since amplifier A can operate as an inverting or noninverting gain stage.

An uncommitted comparator provides many application options. Status indication and logic shaping/shifting are typical examples.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



7

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Input Voltage ..... Equal to Supply Voltage
Logic and Logic Ground Voltage ..... Equal to Supply Voltage
Output Short-Circuit Duration ..... Indefinite
Amplifier A or B Differential Input Voltage ..... ±24V
Comparator Differential Input Voltage ..... ±24V
Comparator Output Voltage ..... Equal to Positive Supply Voltage
Hold Capacitor Short-Circuit Duration ..... Indefinite
Lead Temperature (Soldering, 60 sec) ..... 300°C
Storage Temperature Range
PKD-01AY, PKD-01EY, PKD-01FY ..... –65°C to +150°C
PKD-01EP, PKD-01FP ..... –65°C to +125°C
Operating Temperature Range
PKD-01AY ..... –55°C to +125°C
PKD-01EY, PKD-01FY ..... –25°C to +85°C
PKD-01EP, PKD-01FP ..... 0°C to +70°C
Junction Temperature ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	99	12	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	PKD-01A/E MIN	PKD-01A/E TYP	PKD-01A/E MAX	PKD-01F MIN	PKD-01F TYP	PKD-01F MAX	UNITS
"g_m" AMPLIFIERS A, B									
Zero-Scale Error	V_{ZS}		—	2	4	—	3	7	mV
Input Offset Voltage	V_{OS}		—	2	3	—	3	6	mV
Input Bias Current	I_B		—	80	150	—	80	250	nA
Input Offset Current	I_{OS}		—	20	40	—	20	75	nA
Voltage Gain	A_V	$R_L = 10k\Omega$, $V_O = \pm 10V$	18	25	—	10	25	—	V/mV
Open-Loop Bandwidth	BW	$A_V = 1$	—	0.4	—	—	0.4	—	MHz
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	80	90	—	74	90	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	86	96	—	76	96	—	dB
Input Voltage Range	V_{CM}	(Note 1)	±10	±11	—	±10	±11	—	V
Slew Rate	SR		—	0.5	—	—	0.5	—	V/μs
Feedthrough Error		$\Delta V_{IN} = 20V$, DET = 1, RST = 0, (Note 1)	66	80	—	66	80	—	dB
Acquisition Time to 0.1% Accuracy	t_{aq}	20V Step, $A_{VCL} = +1$, (Note 1)	—	41	70	—	41	70	μs
Acquisition Time to 0.01% Accuracy	t_{aq}	20V Step, $A_{VCL} = +1$, (Note 1)	—	45	—	—	45	—	μs
COMPARATOR									
Input Offset Voltage	V_{OS}		—	0.5	1.5	—	1	3	mV
Input Bias Current	I_B		—	700	1000	—	700	1000	nA
Input Offset Current	I_{OS}		—	75	300	—	75	300	nA
Voltage Gain	A_V	2kΩ Pull-up Resistor to 5V	5	7.5	—	3.5	7.5	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	82	106	—	82	106	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	76	90	—	76	90	—	dB
Input Voltage Range	V_{CM}	(Note 1)	±11.5	±12.5	—	±11.5	±12.5	—	V

NOTES:
1. Guaranteed by design.
2. Due to limited production test times, the droop current corresponds to junction temperature (T_J). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_J) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.
3. $\overline{DET} = 1$, RST = 0.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25°C$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PKD-01A/E MIN	PKD-01A/E TYP	PKD-01A/E MAX	PKD-01F MIN	PKD-01F TYP	PKD-01F MAX	UNITS
Low Output Voltage	V_{OL}	$I_{SINK} \leq 5mA$, Logic GND = 0V	-0.2	0.15	0.4	-0.2	0.15	0.4	V
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	—	25	80	—	25	80	µA
Output Short-Circuit Current	I_{SC}	$V_{OUT} = 5V$	7	12	45	7	12	45	mA
Response Time	t_S	5mV Overdrive, (Note 3) 2kΩ Pull-up Resistor to 5V	—	150	—	—	150	—	ns
DIGITAL INPUTS-RST, $\overline{DET}$ (See Note 3)									
Logic "1" Input Voltage	V_H		2	—	—	2	—	—	V
Logic "0" Input Voltage	V_L		—	—	0.8	—	—	0.8	V
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	—	0.02	1	—	0.02	1	µA
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	—	1.6	10	—	1.6	10	µA
MISCELLANEOUS									
Droop Rate	V_{DR}	$T_j = 25°C$, $T_A = 25°C$ (See Note 2)	— —	0.01 0.02	0.07 0.15	— —	0.01 0.03	0.1 0.20	mV/ms
Output Voltage Swing: Amplifier C	V_{OP}	$\overline{DET} = 1$ $R_L = 2.5k$	±11.5	±12.5	—	±11	±12	—	V
Short-Circuit Current: Amplifier C	I_{SC}		7	15	40	7	15	40	mA
Switch Aperture Time	t_{ap}		—	75	—	—	75	—	ns
Switch Switching Time	ts		—	50	—	—	50	—	ns
Slew Rate: Amplifier C	SR	$R_L = 2.5k$	—	2.5	—	—	2.5	—	V/µs
Power Supply Current	I_{SY}	No Load	—	5	7	—	6	9	mA

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $-55°C \leq T_A \leq +125°C$ for PKD-01AY, $-25°C \leq T_A \leq +85°C$ for PKD-01EY, PKD-01FY and $0°C \leq T_A \leq +70°C$ for PKD-01EP, PKD-01FP.

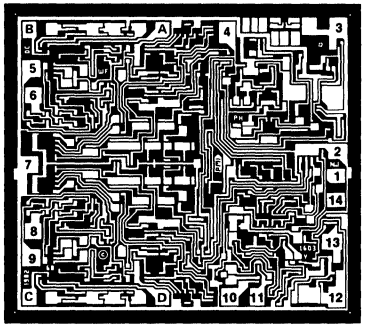
PARAMETER	SYMBOL	CONDITIONS	PKD-01A/E MIN	PKD-01A/E TYP	PKD-01A/E MAX	PKD-01F MIN	PKD-01F TYP	PKD-01F MAX	UNITS
"g_m" AMPLIFIERS A, B									
Zero-Scale Error	V_{ZS}		—	4	7	—	6	12	mV
Input Offset Voltage	V_{OS}		—	3	6	—	5	10	mV
Average Input Offset Drift	TCV_{OS}	(Note 1)	—	-9	-24	—	-9	-24	µV/°C
Input Bias Current	I_B		—	160	250	—	160	500	nA
Input Offset Current	I_{OS}		—	30	100	—	30	150	nA
Voltage Gain	A_V	$R_L = 10k\Omega$, $V_O = \pm 10V$	7.5	9	—	5	9	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \leq V_{CM} \leq +10V$	74	82	—	72	80	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \leq V_S \leq \pm 18V$	80	90	—	70	90	—	dB
Input Voltage Range	V_{CM}	(Note 1)	±10	±11	—	±10	±11	—	V
Slew Rate	SR		—	0.4	—	—	0.4	—	V/µs
Acquisition Time to 0.1% Accuracy	t_{aq}	20V Step, $A_{VCL} = +1$, (Note 1)	—	60	—	—	60	—	µs
COMPARATOR									
Input Offset Voltage	V_{OS}		—	2	2.5	—	2	5	mV
Average Input Offset Drift	TCV_{OS}	(Note 1)	—	-4	-6	—	-4	-6	µV/°C
Input Bias Current	I_B		—	1000	2000	—	1100	2000	nA

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$; $C_H = 1000pF$, $-55°C \le T_A \le +125°C$ for PKD-01AY, $-25°C \le T_A \le +85°C$ for PKD-01EY, PKD-01FY and $0°C \le T_A \le +70°C$ for PKD-01EP, PKD-01FP. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PKD-01A/E MIN	PKD-01A/E TYP	PKD-01A/E MAX	PKD-01F MIN	PKD-01F TYP	PKD-01F MAX	UNITS
Input Offset Current	I_{OS}		—	100	600	—	100	600	nA
Voltage Gain	A_V	2kΩ Pull-up Resistor to 5V	4	6.5	—	2.5	6.5	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	80	100	—	80	92	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	72	82	—	72	86	—	dB
Input Voltage Range	V_{CM}	(Note 1)	±11	—	—	±11	—	—	V
Low Output Voltage	V_{OL}	$I_{SINK} \le 5mA$, Logic GND = 0V	−0.2	0.15	0.4	−0.2	0.15	0.4	V
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	—	25	100	—	100	180	µA
Output Short-Circuit Current	I_{SC}	$V_{OUT} = 5V$	6	10	45	6	10	45	mA
Response Time	t_S	5mV Overdrive, 2kΩ Pull-up Resistor to 5V	—	200	—	—	200	—	ns
DIGITAL INPUTS-RST, DET (See Note 3)									
Logic "1" Input Voltage	V_H		2	—	—	2	—	—	V
Logic "0" Input Voltage	V_L		—	—	0.8	—	—	0.8	V
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	—	0.02	1	—	0.02	1	µA
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	—	2.5	15	—	2.5	15	µA
MISCELLANEOUS									
Droop Rate	V_{DR}	T_j = Max. Operating Temp T_A = Max. Operating Temp. DET = 1, (Note 2)	— —	1.2 2.4	10 20	— —	3 6	15 20	mV/ms
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	±11	±12	—	±10.5	±12	—	V
Short-Circuit Current: Amplifier C	I_{SC}		6	12	40	6	12	40	mA
Switch Aperture Time	t_{ap}		—	75	—	—	75	—	ns
Slew Rate: Amplifier C	SR	$R_L = 2.5k$	—	2	—	—	2	—	V/µs
Power Supply Current	I_{SY}	No Load	—	5.5	8	—	6.5	10	mA

NOTES:
1. Guaranteed by design.
2. Due to limited production test times, the droop current corresponds to junction temperature (T_j). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_j) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.
3. $\overline{DET} = 1$, RST = 0.

DICE CHARACTERISTICS



1. RST (RESET CONTROL)
2. V+
3. OUTPUT
4. C_H (HOLD CAPACITOR)
5. INVERTING INPUT (A)
6. NONINVERTING INPUT (A)
7. V−
8. NONINVERTING INPUT (B)
9. INVERTING INPUT (B)
10. COMPARATOR NONINVERTING INPUT
11. COMPARATOR INVERTING INPUT
12. COMPARATOR OUTPUT
13. LOGIC GROUND
14. $\overline{DET}$ (PEAK DETECT CONTROL)
    A,B (A) NULL
    C,D (B) NULL

DIE SIZE 0.101 × 0.091 inch, 9191 sq. mils
(2.565 × 2.311mm, 5.93 sq mm)

WAFER TEST LIMITS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	PKD-01N LIMIT	UNITS
"g_m" AMPLIFIERS A, B				
Zero-Scale Error	V_{ZS}		7	mV MAX
Input Offset Voltage	V_{OS}		6	mV MAX
Input Bias Current	I_B		250	nA MAX
Input Offset Current	I_{OS}		75	nA MAX
Voltage Gain	A_V	$R_L = 10k\Omega$, $V_O = \pm 10V$	10	V/mV MIN
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	74	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	76	dB MIN
Input Voltage Range	V_{CM}	(Note 1)	±11.5	V MIN
Feedthrough Error		$\Delta V_{IN} = 20V$, $\overline{DET} = 1$, RST = 0, (Note 1)	66	dB MIN
COMPARATOR				
Input Offset Voltage	V_{OS}		3	mV MAX
Input Bias Current	I_B		1000	nA MAX
Input Offset Current	I_{OS}		300	nA MAX
Voltage Gain	A_V	2kΩ Pull-up Resistor to 5V, (Note 1)	3.5	V/mV MIN
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	82	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	76	dB MIN
Input Voltage Range	V_{CM}	(Note 1)	±11.5	V MIN
Low Output Voltage	V_{OL}	$I_{SINK} \le 5mA$, Logic GND = 5V	0.4 −0.2	V MAX V MIN
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	80	µA MAX
Output Short-Circuit Current	I_{SC}	$V_{OUT} = 5V$	45 7	mA MAX mA MIN

NOTES:
1. Guaranteed by design.
2. Due to limited production test times, the droop current corresponds to junction temperature (T_j). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_j) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.
3. $\overline{DET} = 1$, RST = 0.

WAFER TEST LIMITS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25°C$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PKD-01N LIMIT	UNITS
DIGITAL INPUTS-RST, DET (See Note 3)				
Logic "1" Input Voltage	V_H		2	V MIN
Logic "0" Input Voltage	V_L		0.8	V MAX
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	1	µA MAX
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	10	µA MAX
MISCELLANEOUS				
Droop Rate	V_{DR}	$T_j = 25°C$, $T_A = 25°C$ (See Note 2)	0.1 0.20	mV/ms MAX mV/ms MAX
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	±11	V MIN
Short-Circuit Current: Amplifier C	I_{SC}		40 7	mA MAX mA MIN
Power Supply Current	I_{SY}	No Load	9	mA MAX

NOTES:
1. Guaranteed by design.
2. Due to limited production test times, the droop current corresponds to junction temperature (T_j). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_j) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperatures. Ambient (T_A) temperature specifications are not subject to production testing.
3. $\overline{DET} = 1$, RST = 0.

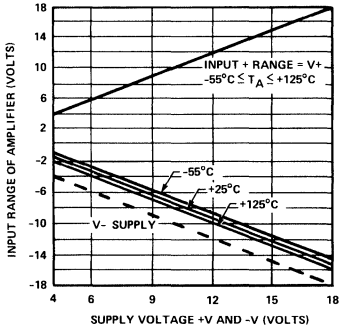
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, and $T_A = 25°C$, unless otherwise noted.

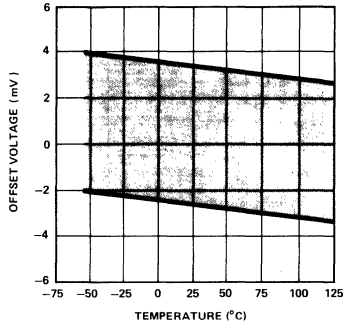
PARAMETER	SYMBOL	CONDITIONS	PKD-01N TYPICAL	UNITS
"g_m" AMPLIFIERS A, B				
Slew Rate	SR		0.5	V/µs
Acquisition Time	t_a	0.1% Accuracy, 20V step, $A_{VCL} = 1$, (Note 1)	41	µs
Acquisition Time	t_a	0.01% Accuracy, 20V step, $A_{VCL} = 1$, (Note 1)	45	µs
COMPARATOR				
Response Time		5mV Overdrive, 2kΩ Pull-up Resistor to +5V	150	ns
MISCELLANEOUS				
Switch Aperature Time	t_{ap}		75	ns
Switching Time	t_S		50	ns
Buffer Slew Rate	SR	$R_L = 2.5k\Omega$	2.5	V/µs

TYPICAL PERFORMANCE CHARACTERISTICS

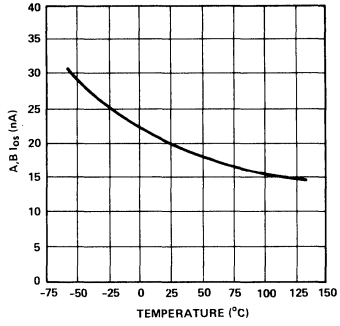
A AND B INPUT RANGE vs SUPPLY VOLTAGE



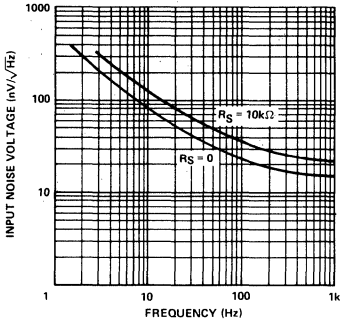
A AND B AMPLIFIERS OFFSET VOLTAGE vs TEMPERATURE



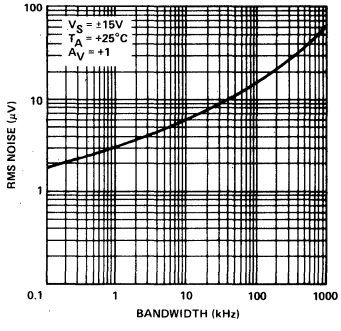
A, B I_{OS} vs TEMPERATURE



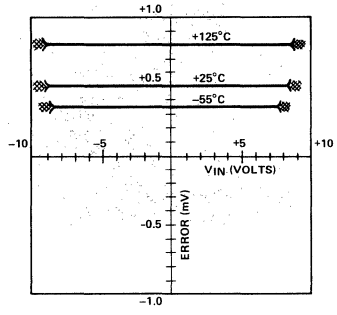
INPUT SPOT NOISE vs FREQUENCY



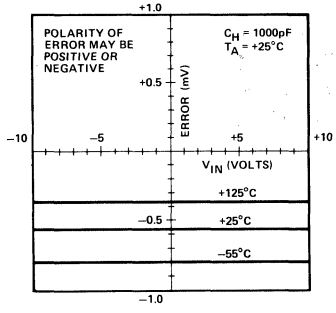
WIDEBAND NOISE vs BANDWIDTH



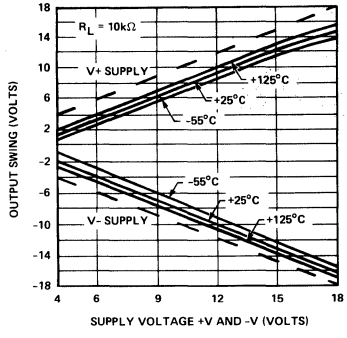
AMPLIFIER B CHARGE INJECTION ERROR vs INPUT VOLTAGE AND TEMPERATURE



AMPLIFIER A CHARGE INJECTION ERROR vs INPUT VOLTAGE AND TEMPERATURE

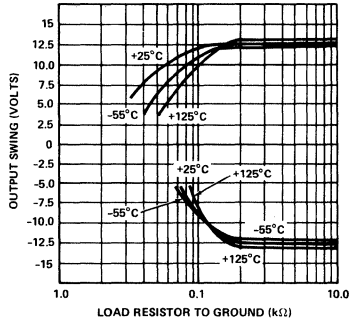


OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE (DUAL SUPPLY OPERATION)

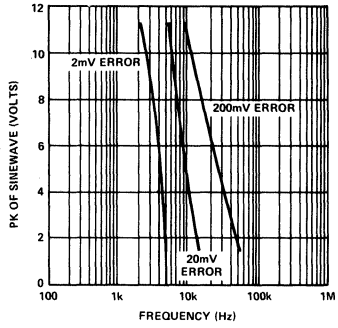


TYPICAL PERFORMANCE CHARACTERISTICS

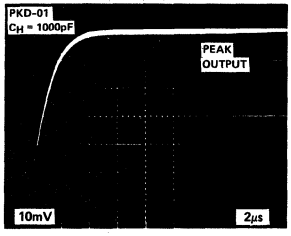
OUTPUT VOLTAGE vs LOAD RESISTANCE



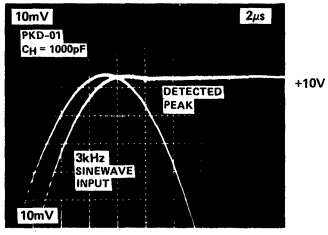
OUTPUT ERROR vs FREQUENCY AND INPUT VOLTAGE



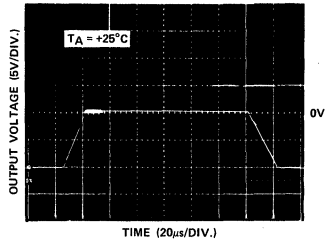
PKD-01 SETTLING RESPONSE



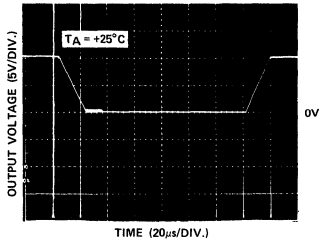
PKD-01 SETTLING RESPONSE



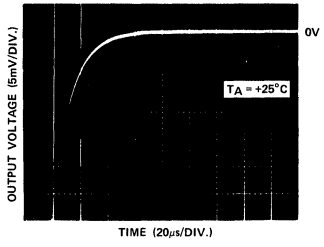
LARGE-SIGNAL INVERTING RESPONSE



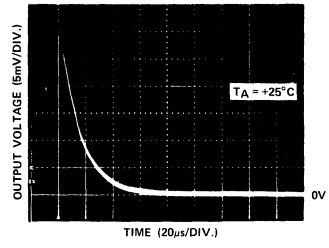
LARGE-SIGNAL NONINVERTING RESPONSE



SETTLING TIME FOR −10V TO 0V STEP INPUT

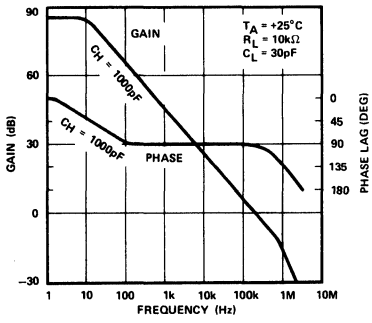


SETTLING TIME FOR +10V TO 0V STEP INPUT

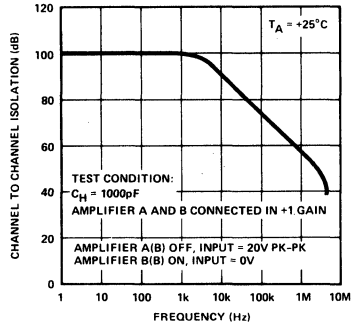


TYPICAL PERFORMANCE CHARACTERISTICS

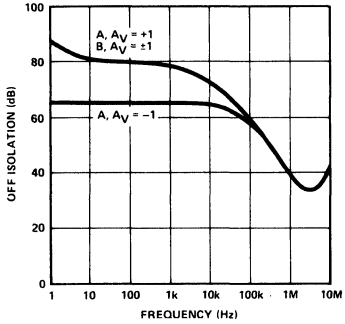
SMALL-SIGNAL OPEN LOOP GAIN/PHASE vs FREQUENCY



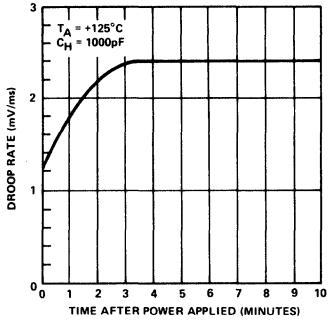
CHANNEL TO CHANNEL ISOLATION vs FREQUENCY



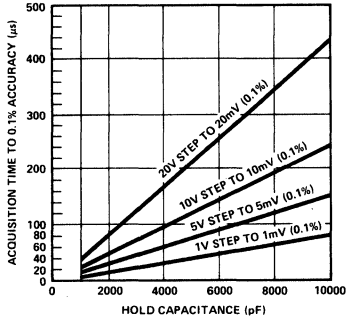
OFF ISOLATION vs FREQUENCY



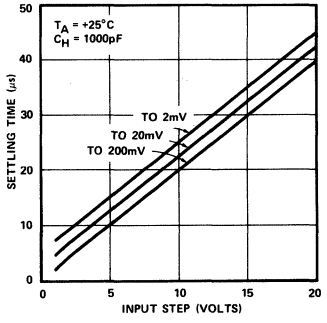
DROOP RATE vs TIME AFTER POWER ON



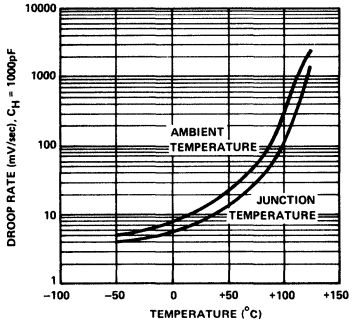
ACQUISITION TIME vs EXTERNAL HOLD CAPACITOR AND ACQUISITION STEP



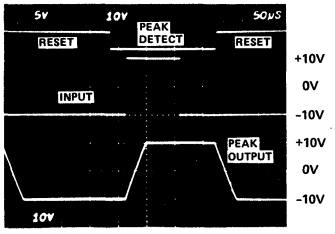
ACQUISITION TIME vs INPUT VOLTAGE STEP SIZE



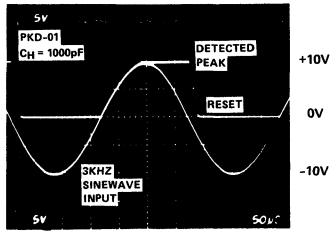
DROOP RATE vs TEMPERATURE



ACQUISITION OF STEP INPUT



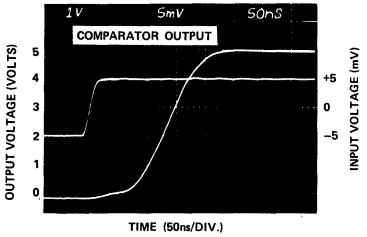
ACQUISITION OF SINEWAVE PEAK



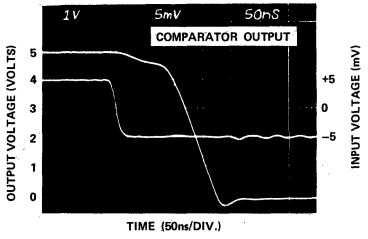
7

TYPICAL PERFORMANCE CHARACTERISTICS

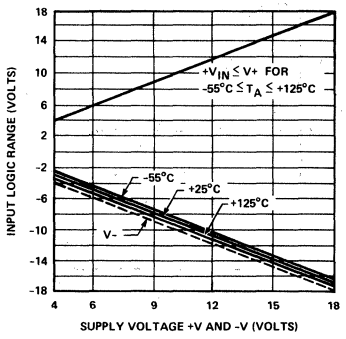
COMPARATOR OUTPUT RESPONSE TIME (2kΩ PULL-UP RESISTOR, T_A = +25°C)



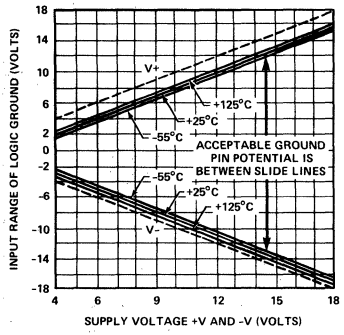
COMPARATOR OUTPUT RESPONSE TIME (2kΩ PULL-UP RESISTOR, T_A = +25°C)



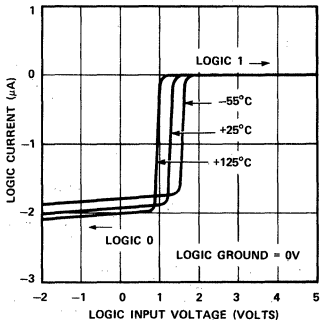
INPUT LOGIC RANGE vs SUPPLY VOLTAGE



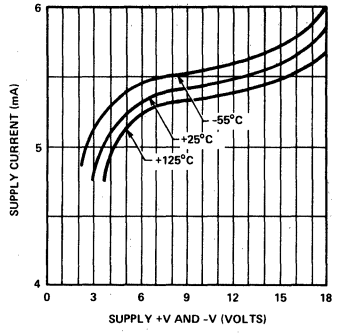
INPUT RANGE OF LOGIC GROUND vs SUPPLY VOLTAGE



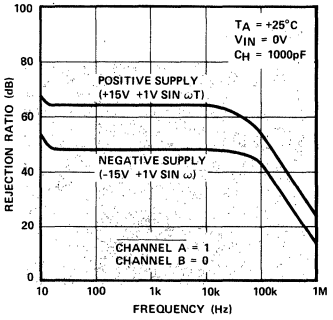
LOGIC INPUT CURRENT vs LOGIC INPUT VOLTAGE



SUPPLY CURRENT vs SUPPLY VOLTAGE

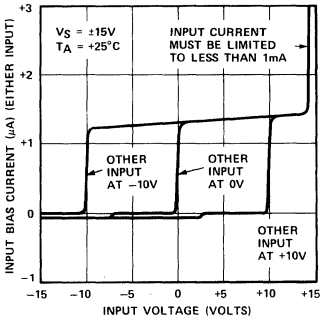


HOLD MODE POWER SUPPLY REJECTION vs FREQUENCY

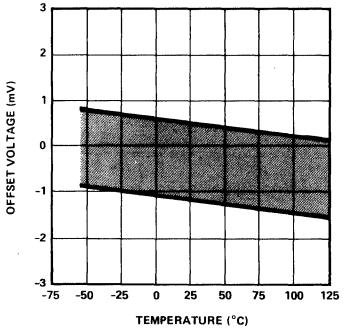


TYPICAL PERFORMANCE CHARACTERISTICS

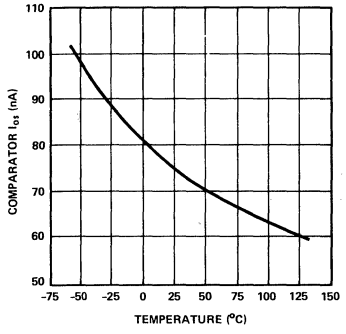
COMPARATOR INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



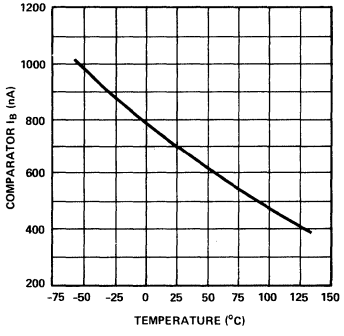
COMPARATOR OFFSET VOLTAGE vs TEMPERATURE



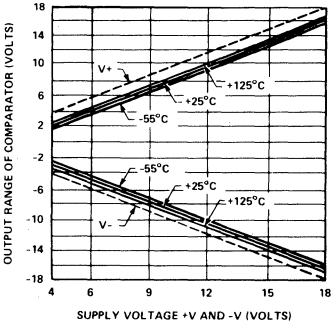
COMPARATOR I_{OS} vs TEMPERATURE



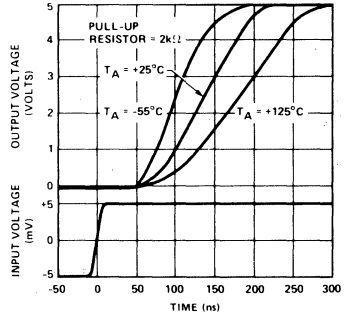
COMPARATOR I_B vs TEMPERATURE



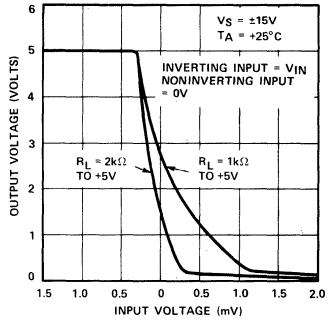
OUTPUT SWING OF COMPARATOR vs SUPPLY VOLTAGE



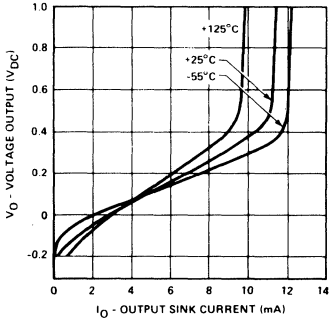
COMPARATOR RESPONSE TIME vs TEMPERATURE



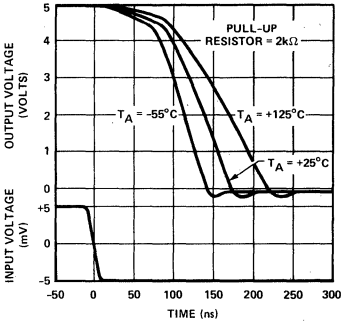
COMPARATOR TRANSFER CHARACTERISTIC



COMPARATOR OUTPUT VOLTAGE vs OUTPUT CURRENT AND TEMPERATURE



COMPARATOR RESPONSE TIME vs TEMPERATURE



7

THEORY OF OPERATION

The typical peak detector uses voltage amplifiers and a diode or an emitter follower to charge the hold capacitor, C_H, unidirectionally (Figure 1). The output impedance of A plus D_1's dynamic impedance, r_d, make up the resistance which determines the feedback loop pole. The dynamic impedance is $r_d = \frac{kT}{qI_d}$. I_d is the capacitor charging current.

The pole moves toward the origin of the S plane as I_d goes to zero. The pole movement in itself will not significantly lengthen the acquisition time since the pole is enclosed in the system feedback loop.

When the moving pole is considered with the typical frequency compensation of voltage amplifiers there is however, a loop stability problem. The necessary compensation can increase the required acquisition time. PMI's approach replaces the input voltage amplifier with a transconductance amplifier; Figure 2.

The PKD-01 transfer function can be reduced to:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 + \frac{sC_H}{g_m} + \frac{1}{g_m R_{OUT}}} \approx \frac{1}{1 + \frac{sC_H}{g_m}}$$

Where: $g_m \approx 1\mu A/mV$, $R_{OUT} \approx 20M\Omega$.

The diode in series with A's output (Figure 2) has no effect because it is a resistance in series with a current source. In addition to simplifying the system compensation, the input transconductance amplifier output current is switched by current steering. The steered output is clamped to reduce and match any charge injection.

Fig. 3 shows a simplified schematic of the reset "g_m" amplifier, B. In the track mode, Q_1 & Q_4 are ON and Q_2 & Q_3 are OFF. A current of 2I passes through D_1, I is summed at "B" and passes through Q_1, and is summed with $g_m V_{IN}$. The current sink can absorb only 3I, thus, the current passing through D_2 can only be: $2K - g_m V_{IN}$. The net current into the hold capacitor node then, is $g_m V_{IN} (C_H = 2I - (2I - g_m V_{IN})$. The hold mode, Q_2 & Q_3 are ON while Q_1 & Q_4 are OFF. The net current into the top of D_1 is $-I$ until D_3 turns ON. With Q_1 OFF, the bottom of D_2 is pulled up with a current I until D_4 turns ON, thus D_1 & D_2 are reverse biased by $\approx 0.6V$ and charge injection is independent of input level.

The monolithic layout results in points A and B having equal nodal capacitance. In addition, matched diodes D_1 and D_2 have equal diffusion capacitance. When the transconductance amplifier outputs are switched open, points A and B are ramped equally but in opposite phase. Diode clamps D_3 and D_4 cause the swings to have equal amplitudes. The net charge injection (voltage change) at node C is therefore zero.

The peak transconductance amplifier, A, is shown in Figure 4. Unidirectional hold capacitor charging requires diode D_1 to be connected in series with the output. Upon entering the peak hold mode D_1 is reverse biased. The voltage clamp limits charge injection to approximately 1pC and the hold step to 0.6mV.

Minimizing acquisition time dictated a small C_H capacitance. A 1000pF value was selected. Droop rate was also minimized by providing the output buffer with an FET input stage. A current cancellation circuit further reduces droop current and minimizes the gate current's tendency to double for every 10°C temperature change.

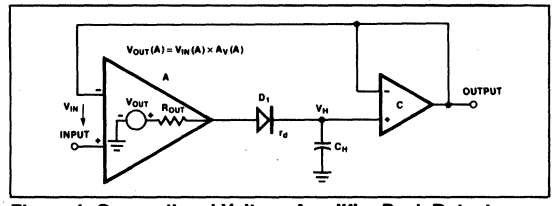


Figure 1. Conventional Voltage Amplifier Peak Detector

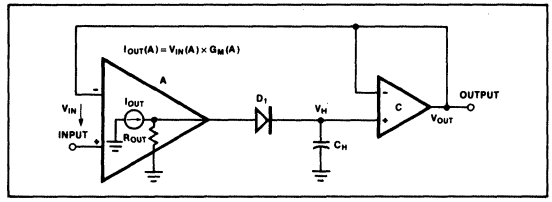


Figure 2. Transconductance Amplifier Peak Detector

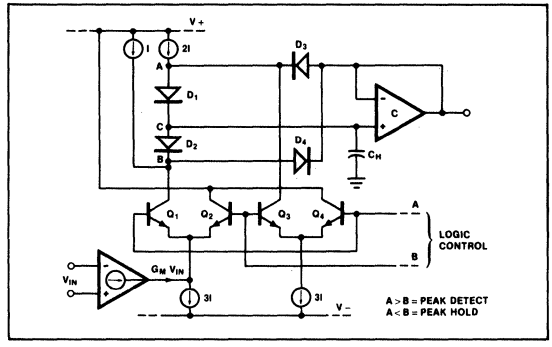


Figure 3. Transconductance Amplifier with Low Glitch Current Switch

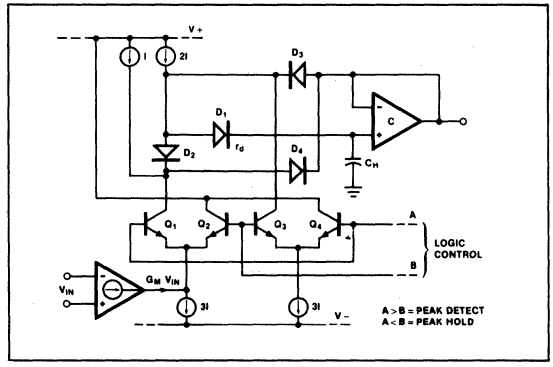


Figure 4. Peak Detecting Transconductance Amplifier with Switched Output

APPLICATIONS INFORMATION

OPTIONAL OFFSET VOLTAGE ADJUSTMENT

Offset voltage is the primary zero scale error component since a variable voltage clamp limits voltage excursions at D_1's anode and reduces charge injection. The PKD-01 circuit gain and operational mode (positive or negative peak detection) determine the applicable null circuit. Figures A through D are suggested circuits. Each circuit corrects amplifier C offset voltage error also.

A. NULLING GATED OUTPUT g_m AMPLIFIER A. Diode D_1 must be conducting to close the feedback circuit during amplifier A V_{OS} adjustment. Resistor network $R_A - R_C$ cause D_1 to conduct slightly. With DET = 0 and V_{IN} = 0V monitor the PKD-01 output. Adjust the null potentiometer until V_{OUT} = 0V. After adjustment, disconnect R_C from C_H.

B. NULLING GATED g_m AMPLIFIER B. Set amplifier B signal input to V_{IN} = 0V and monitor the PKD-01 output. Set DET = 1, RST = 1 and adjust the null potentiometer for V_{OUT} = 0V. The circuit gain — inverting or noninverting — will determine which null circuit illustrated in Figures A through D is applicable.

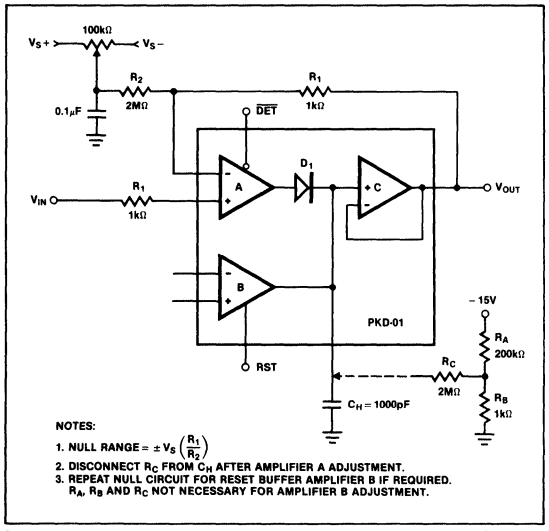


Figure A. V_{OS} Null Circuit for Unity Gain Positive Peak Detector

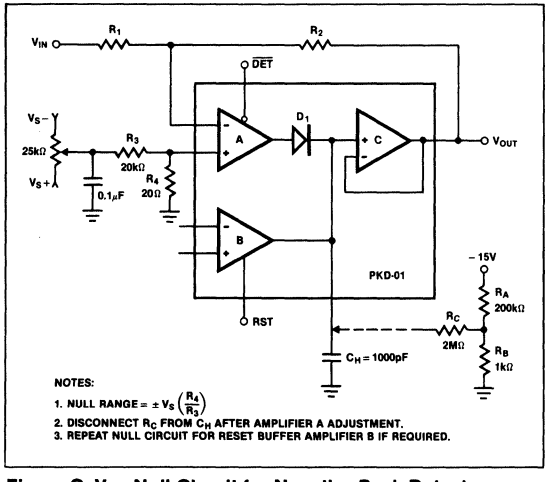


Figure C. V_{OS} Null Circuit for Negative Peak Detector

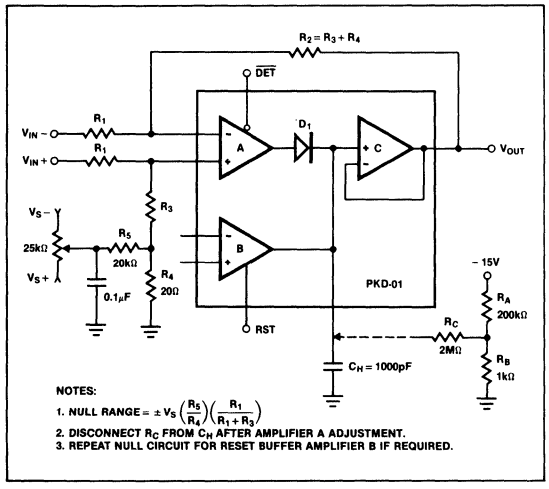


Figure B. V_{OS} Null Circuit for Differential Peak Detector

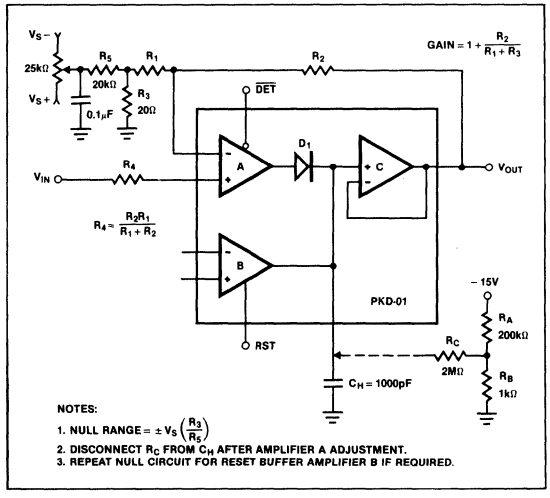


Figure D. V_{OS} Null Circuit for Positive Peak Detector With Gain

PEAK HOLD CAPACITOR RECOMMENDATIONS

The hold capacitor (C_H) serves as the peak memory element and compensating capacitor. Stable operation requires a minimum value of 1000pF. Larger capacitors may be used to lower droop rate errors, but acquisition time will increase.

Zero scale error is internally trimmed for C_H = 1000pF. Other C_H values will cause a zero scale shift which can be approximated with the following equation.

$$\Delta V_{ZS}(mV) = \frac{1 \times 10^3(pC)}{C_H(nF)} - 0.6mV$$

The peak hold capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85°C, a polystyrene capacitor is recommended, while a Teflon capacitor is recommended for high temperature environments.

CAPACITOR GUARDING AND GROUND LAYOUT

Ground planes are recommended to minimize ground path resistance. Separate analog and digital grounds should be used. The two ground systems are tied together only at the common system ground. This avoids digital currents returning to the system ground through the analog ground path.

The C_H terminal (Pin 4) is a high-impedance point. To minimize gain errors and maintain the PKD-01's inherently low droop rate, guarding Pin 4 as shown in Figure 2 is recommended.

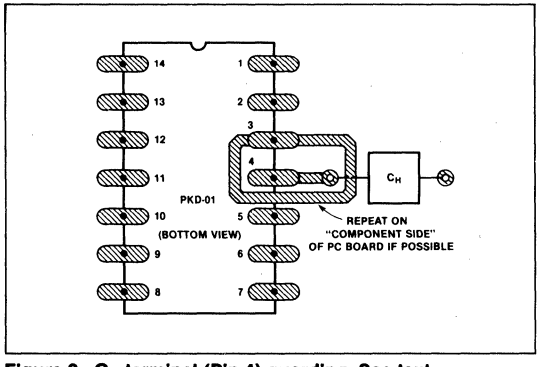


Figure 2. C_H terminal (Pin 4) guarding. See text.

COMPARATOR

The comparator output high level (V_{OH}) is set by external resistors. It's possible to optimize noise immunity while interfacing to all standard logic families — TTL, DTL, and CMOS. Figure 1 shows the comparator output with external level setting resistors. Table I gives typical R_1 and R_2 values for common circuit conditions.

The maximum comparator high output voltage (V_{OH}) should be limited to:

$V_{OH}(maximum) < V^+ - 2.0V$

With the comparator in the low state (V_{OL}), the output stage will be required to sink a current approximately equal to V_C/R_1.

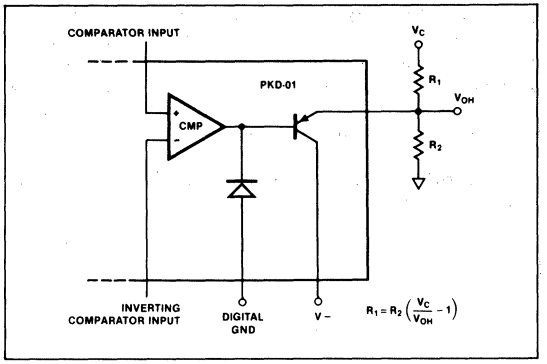


Figure 1

Table I.

V_C	V_{OH}	R_1	R_2
5	3.5	2.7K	6.2K
5	5.0	2.7K	∞
15	3.5	4.7K	1.5K
15	5.0	4.7K	2.4K
15	7.5	7.5K	7.5K
15	10.0	7.5K	15K

$$R_1 \approx \frac{V_C}{I_{SINK}}$$

$$R_2 \approx \left(\frac{1}{\frac{V_C}{V_{OH}} - 1}\right)$$

PEAK DETECTOR LOGIC CONTROL (RST, $\overline{DET}$)

The transconductance amplifier outputs are controlled by the digital logic signals RST and $\overline{DET}$. The PKD-01 operational mode is selected by steering the current (I_1) through Q_1 and Q_2, thus providing high-speed switching and a predictable logic threshold. The logic threshold voltage is 1.4 volts when digital ground is at zero volts.

Other threshold voltages (V_{TH}) may be selected by applying the formula:

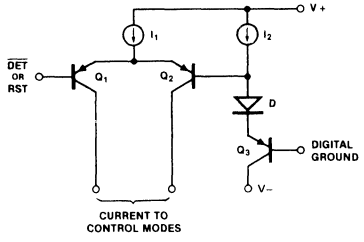
$V_{TH} \approx 1.4V$ + Digital Ground Potential.

For proper operation, digital ground must always be at least 3.5V below the positive supply and 2.5V above the negative supply. The RST or $\overline{DET}$ signal must always be at least 2.8V above the negative supply.

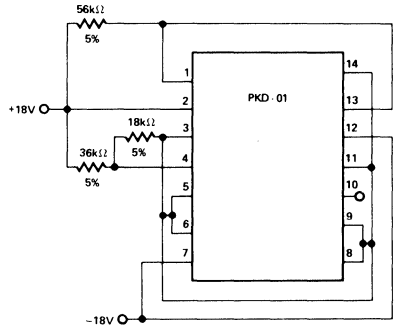
Operating the digital ground at other than zero volts does influence the comparator output low voltage. The V_{OL} level is referenced to digital ground and will follow any changes in digital ground potential:

$V_{OL} \approx 0.2V$ + Digital Ground Potential.

PKD-01 LOGIC CONTROL

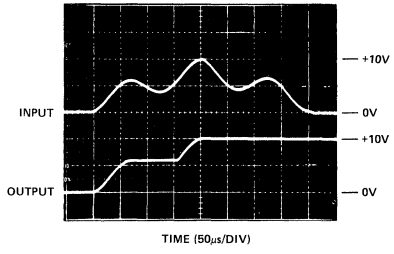


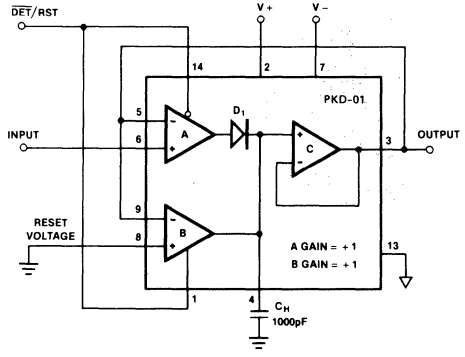
BURN-IN CIRCUIT



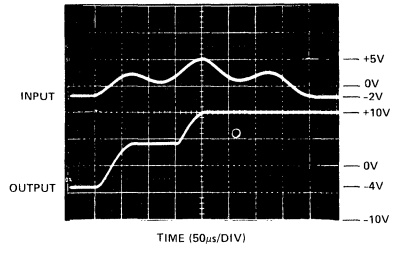
TYPICAL CIRCUIT CONFIGURATIONS

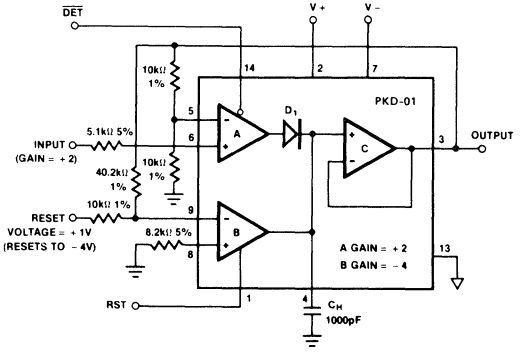
UNITY GAIN POSITIVE PEAK DETECTOR





POSITIVE PEAK DETECTOR WITH GAIN





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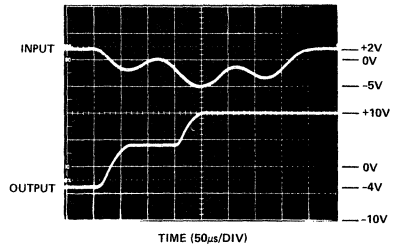
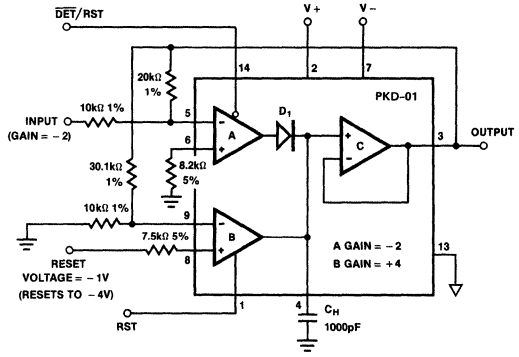
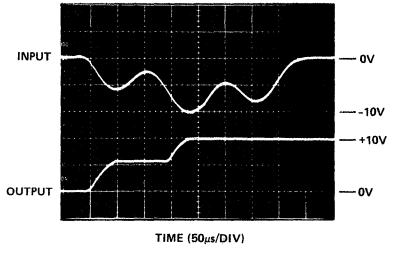
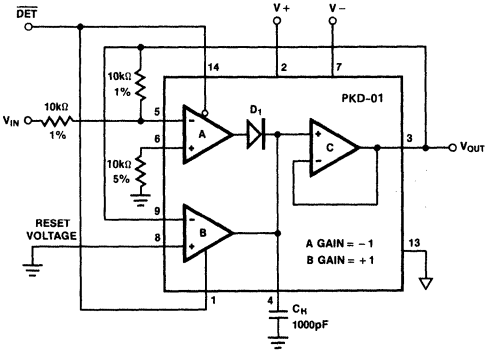
NEGATIVE PEAK DETECTOR WITH GAIN



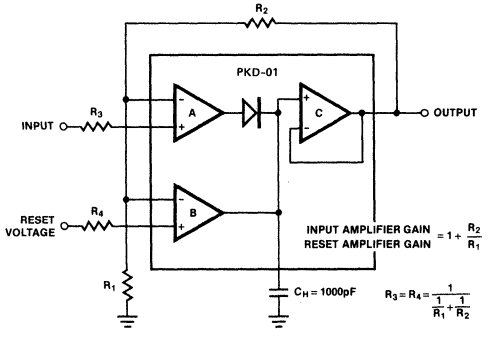


UNITY GAIN NEGATIVE PEAK DETECTOR





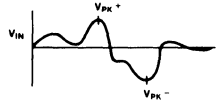
ALTERNATE GAIN CONFIGURATION

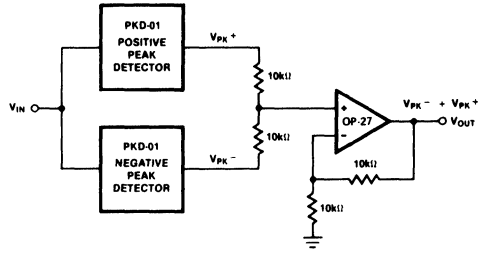


IF BOTH INPUT SIGNAL (AMPLIFIER A INPUT) AND THE RESET VOLTAGE (AMPLIFIER B INPUT HAVE THE SAME POSITIVE VOLTAGE GAIN THE GAIN CAN BE SET BY A SINGLE VOLTAGE DIVIDER FOR BOTH INPUT AMPLIFIERS.

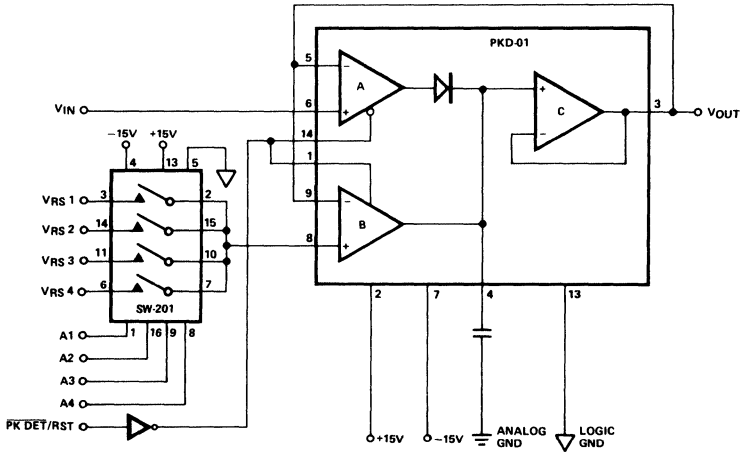
NOTE:
R1, R2, R3 AND R4 > 5kΩ

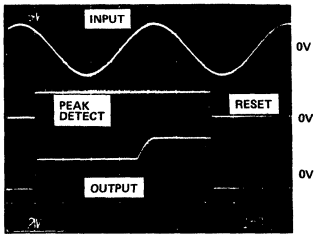
PEAK-TO-PEAK DETECTOR





POSITIVE PEAK DETECTOR WITH SELECTABLE RESET VOLTAGE





NOTES:
RESET VOLTAGE = -1.0V
TRACE 1 = 2V/DIV.
TRACE 2 = 5V/DIV.
TRACE 3 = 2V/DIV.

7

ANALOG DEVICES

Voltage-Controlled Amplifier

SSM-2013

FEATURES

- 0.01% THD Typ
- 0.03% IMD Typ
- 800kHz Unity-Gain Bandwidth
- 12dB Headroom (at Rating)
- 40dB Gain Capability
- 106dB Dynamic Range (17.5 Bits)
- Full Class A Performance
- Mute and Exponential Controls

APPLICATIONS

- Compressor/Limiters
- Noise Gates
- Automatic Gain Control
- Noise Reduction Systems
- Telephone Line Interfaces

ORDERING INFORMATION

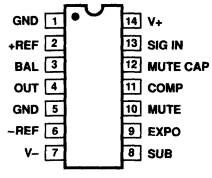
PACKAGE	OPERATING TEMPERATURE RANGE
PLASTIC 14-PIN	
SSM2013P	–10°C to +55°C

GENERAL DESCRIPTION

The SSM-2013 is a high-performance monolithic Class A Voltage Controlled Amplifier. Operating with current mode inputs and outputs, the SSM-2013 is ideal when logarithmic control of gain is needed. The output current gain or attenuation is controlled by applying a control voltage to the EXPO pin 9. The amplifier offers wide bandwidth, easy signal summing and minimum external component count.

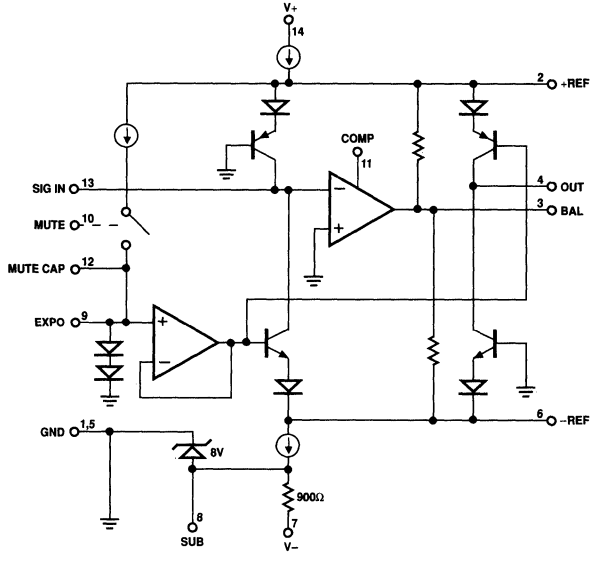
The SSM-2013 can operate with more than 12dB of headroom at the rated specifications or be configured for gains as high as 40dB. Inherently low control feedthrough and 2nd harmonic distortion make trimming unnecessary for most applications. An extremely wide control range of 110dB regulated by a flexible antilogarithmic control port make this VCA a versatile analog building block. With 800kHz bandwidth and 94dB S/N ratio at 0.01% THD, the SSM-2013 provides a useful solution for a variety of signal conditioning needs in applications ranging from professional audio to analog instrumentation, process controls and more.

PIN CONNECTIONS



14-PIN PLASTIC DIP (P-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... 36V or ±18V
Junction Temperature ..... +150°C
Operating Temperature Range ..... –10°C to +55°C
Storage Temperature Range ..... –65°C to +150°C
Maximum Current into any Pin 10mA
Lead Temperature Range (Soldering 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (NOTE 1)	Θ_{JC}	UNITS
14-Pin Plastic DIP (P)	90	47	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V and T_A = 25°C, unless otherwise noted.

		SSM-2013			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Supply Voltage Negative Supply Voltage (Note 1)		+12 –7.9	+15 –8.5	+18 –90	V
Positive Supply Current Negative Supply Current		5.4 6.0	8.7 8.7	10.4 11.0	mA
Negative Supply Bias Resistor (Pin 7 to Pin 8)		675	900	1170	Ω
Expo Input Bias	V_e = GND (Note 2)	–	1.0	3.2	µA
Expo Control Sensitivity	at Pin 9	–	–10	–	mV/dB
Mute Off (Logic Low)		0.0	–	1.0	V
Mute On (Logic High)		3.0	5	15	V
Mute Attenuation	(@ 1kHz, $V_{PIN\ 10}$ = +5V)	–	–90	–	dB
Current Gain	V_e = GND	0.90	1.0	1.1	
Current Output Offset	V_e = GND	–7.5	0	+7.5	µA
Output Leakage	V_e = +600mV	–50	0	+50	nA
Max Available Output Current	V_e = GND, 15k (pin 3 to –V)	±1.2	–	–	mA
Current Bandwidth (3dB)	V_e = GND	–	800	–	kHz
Signal Feedthrough	V_e = +1.2V	–	–90	–	dB
Signal to Noise (20Hz - 20kHz) (Notes 3, 4)	V_e = GND, No Signal	92.5	–94	–	dB
THD (Untrimmed) (Note 4)	V_e = GND, I_{IN} = 600µA_{p-p}	–	0.01	0.06	%
THD (Trimmed)	V_e = GND, I_{IN} = 600µA_{p-p}	–	0.004	–	%
IMD (Untrimmed) SMPTE (Note 4)	V_e = GND, I_{IN} = 600µA_{p-p}	–	0.03	0.12	%
IMD (Trimmed) SMPTE	V_e = GND, I_{IN} = 600µA_{p-p}	–	0.012	–	%

NOTES:
1. Measured at pin 8, pin 7 = –15V.
2. V_e is voltage on pin 9 (V_{EXPO}).
3. Referred to a 400µA_{p-p} input level.
4. Parameter is sample tested to max limit (0.4% AQL).

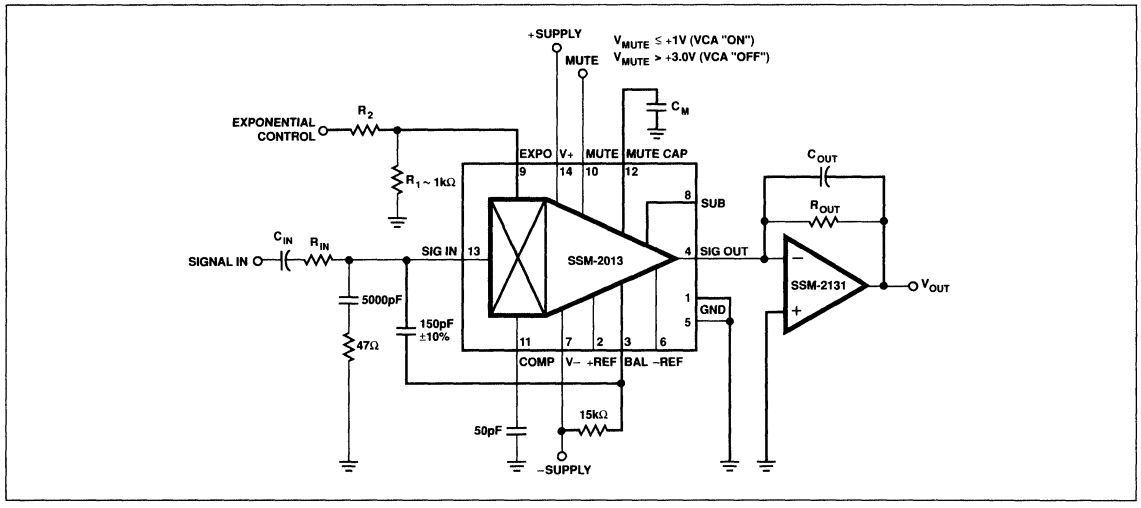


FIGURE 1: *Typical Connection*

THEORY OF OPERATION

The SSM-2013 is a current input/current output device. It is essentially a current mode amplifier where the output current/input current transfer function is controlled by a control voltage applied at the EXPO pin (9). Current mode operation allows easy adaptation to various voltage ranges at the input, output and control port. As configured, it offers large attenuation plus moderate gain capability.

CHOOSING R_{IN}

Most applications use the typical connection of Figure 1. In this configuration, The SSM-2013 will accomodate input currents up to 1.2mA without significant distortion or clipping. To set the maximum operating current to 1.2mA, select R_{IN} to equal Vpeak/1.2mA.

As an example: For a $7V_{p-p}$ nominal signal level (±3.5V), select $R_{IN} = 12k\Omega$. Here, I_{IN} operating is: $3.5V/12k = 300\mu A$, which yields 12dB headroom from 1.2mA. In some applications such as broadcast equipment, 16 - 24dB headroom may be required.

Selecting ±300µA nominal operating current yields 12dB headroom. Figure 2 shows the IMD/THD (Intermodulation and Total Harmonic Distortion) characteristics of the SSM-2013 at this 300µA or 600µA peak-to-peak operating level.

Operation at higher input currents will increase distortion effects whereas operation at lower currents will improve distortion but decrease the S/N ratio. For example, operation with 20dB headroom versus 12dB will improve the relative effects of IMD/THD shown in Figure 2 by 2.5 times. For 20dB headroom, use ±120µA nominal operating input current. At this level, the signal-to-noise ratio will be 86dB.

The SSM-2013 is capable of 40dB gain and as much as –95dB attenuation. Gain or attenuation levels are set by the EXPO control pin as described in the next section. Figure 2 shows how IMD/THD performance degrades with current gain and attenuation. Note also that distortion in the SSM-2013 is nearly all 2nd harmonic. From a sonic standpoint, this is much less objectionable than other types of distortion.

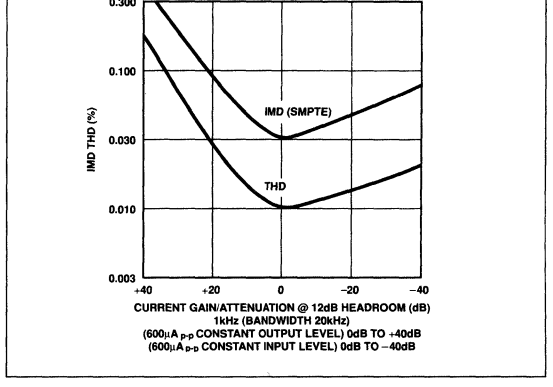


FIGURE 2:

For best performance, choose C_{IN} and R_{IN} for a cutoff frequency below the audio band. C_{IN} will block DC offsets from previous stages.

OUTPUT SECTION

When establishing circuit gain or attenuation, it is important to consider the tradeoffs between gain/attenuation for the SSM-2013 versus the gain of the output amplifier/current to voltage

converter. Operating the SSM-2013 with current gain above 20 or 30dB increases distortion as shown in Figure 2. Gain in the output amplifier amplifies the VCA noise. This will directly increase the equivalent VCA noise floor by the amplifier gain. A compromise within these constraints will determine the best tradeoff between SSM-2013 current gain and the amplifier gain. Figure 3 shows how output noise increases as current gain increases.

CONTROL PIN EXPO

The control port EXPO (pin 9) is a high impedance input with an exponential control sensitivity of –1dB/10mV or –10mV/dB. The overall control range is +40dB to –95dB. This pin is easily adaptable to any control voltage range by selecting the R_1 and R_2 divider appropriately. Note the negative control relationship where positive voltages at pin 9 result in signal attenuation whereas negative voltages yield gain. The control pin is accurate to within ±1.5dB over a ±36dB range.

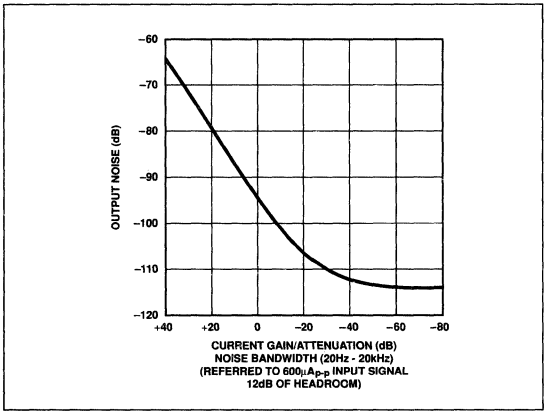


FIGURE 3

The transfer characteristics for the control pin is shown in Figure 4. Note the dotted line showing an optional improvement in gain accuracy. To achieve this improved transfer characteristic, refer to the circuit of Figure 5. As the recommended circuit for control summing applications, this technique offers a significant improvement in linearity over a wider control voltage range.

The control port sensitivity has a –3300ppm/°C temperature coefficient. To compensate for this drift, use a +3300ppm/°C tempsistor* in place of R_1 shown in Figure 1.

MUTING FUNCTION

The mute circuit turns the device on or off independent of the control pin EXPO. Muting is activated when the MUTE (pin 10) is raised above 3.0V and is compatible up to 15V. Muting is off when MUTE is below 1.0V.

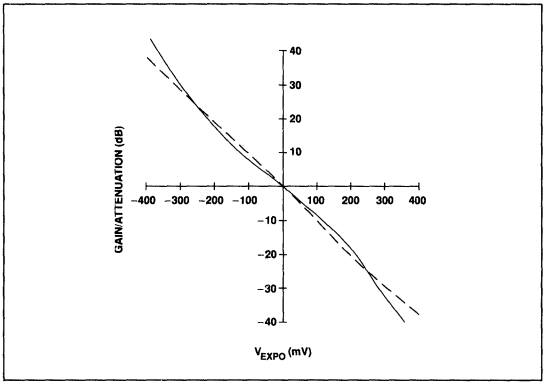


FIGURE 4: *Circuit Gain/Attenuation vs. V_{EXPO}*

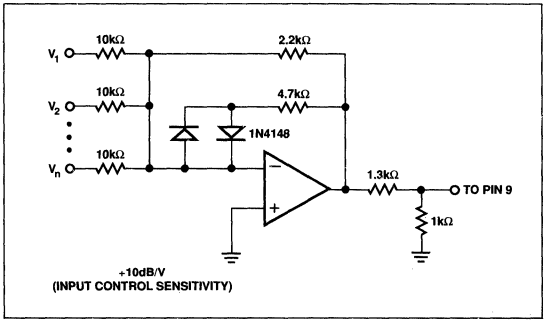


FIGURE 5: *Control Summer with Improved Linearity over Wider Control Range*

A selectable MUTE CAP connected between pin 12 and ground determines the controlled turn on/turn off rate. The recommended 1µF mute cap and internal 10kΩ impedance gives a 10ms time constant. This transition timing is considered quick without being too abrupt or "poppy."

To disable the muting function, simply ground pin 10.

APPLICATIONS INFORMATION

OUTPUT AMPLIFIER

Note the importance of including C_{OUT} in parallel with R_{OUT} to ensure stability under all signal and output loading conditions. A corner frequency of 300kHz for the R_{OUT}, C_{OUT} combination is sufficient, but a lower frequency may also be chosen to limit noise output the audio band. This, however will result in a slower transient response.

* RCD Components, Inc. Part Number LP1/4, 3301 Bedford Street, Manchester, NH U.S.A., (603) 669-0054, Telex 943512

CONTROL FEEDTHROUGH TRIMMING

Control feedthrough is defined as the portion of the control signal fed to the output in the absence of an input signal. A single shunt resistor across pins 2 and 6 will reduce both control feedthrough and noise (see Figure 6). Values from 3.3kΩ to 5.4kΩ offer an improvement in control feedthrough from 20dB to 10dB, respectively.

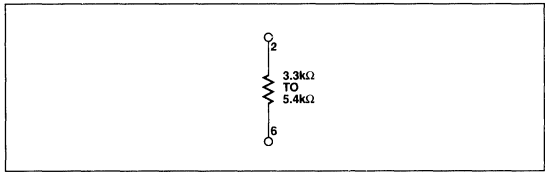


FIGURE 6

This trim will tradeoff an increase in THD by roughly 3 to 5 times. THD increases slightly more using a lower resistor value. With 3.3kΩ, the worst case is about 0.4% over gain and attenuation. By comparison, THD ranges from 0.05% to 0.1% with no shunt resistor.

TRIMMING DISTORTION

The SSM-2013 has very good distortion, offset and control feedthrough at unity current gain. For applications requiring over 10dB to 20dB gain, trimming allows the best overall distortion versus gain.

Distortion Trim Procedure for High Gain Applications:

1. Apply voltage at pin 9 corresponding to maximum current gain.
2. Set input level so output is just below clipping.
3. Adjust trimming per Figure 7 until distortion is at a minimum.

COMPENSATION

To compensate, connect a 50pF capacitor from pin 11 (COMP) to GND as shown in the typical connection.

ON-BOARD REFERENCE

An on-chip zener diode helps establish the –8V available at the SUB output (pin 8). This is a general purpose reference that can be used to introduce DC offsets.

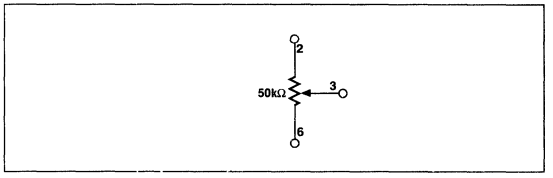


FIGURE 7

BREADBOARDING THE SSM-2013

A typical connection identical to Figure 1 and redrawn for breadboarding purposes is shown in Figure 8.

MEASURING NOISE

When measuring audio noise in the SSM-2013, bandwidth should be limited to 20kHz to 30kHz. This is due to the presence of broadband noise which is caused by a zero at 600kHz. The zero results from the 5000pF-47Ω network at the input. Beyond 30kHz, the noise floor increases at approximately 6dB per octave from 45kHz to 600kHz where it rolls off.

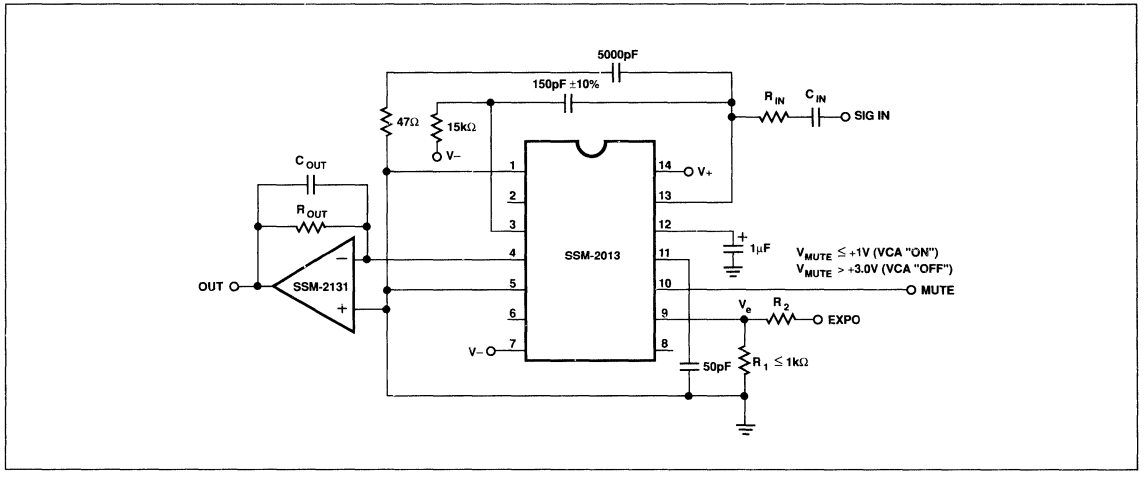


FIGURE 8: *Typical Connection for Breadboarding*

ANALOG DEVICES

Voltage-Controlled Amplifier/OVCE

SSM-2014*

FEATURES

- **Wide Dynamic Range ..... 116dB (Class AB)**
  ..... 104dB (Class A)
- **12MHz Effective Gain-Bandwidth Product**
- **100dB Open-Loop Gain**
- **0.01% THD Class A (Any Gain/Signal) @ = 10dBV$_{IN/OUT}$**
- **Minimum External Component Count**
- **No Trimming in Many Applications**
- **Low Cost**

Not recommended for new designs; replace with SSM-2018.

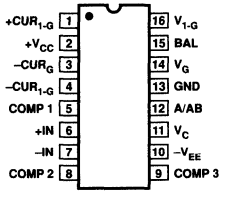
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... 36V or ±18V
Junction Temperature ..... +150°C
Operating Temperature Range ..... –10°C to +55°C
Storage Temperature Range .....–65°C to +150°C
Maximum Current Into Any Pin 10mA
Lead Temperature Range (Soldering, 60 sec) ..... +300°C

ORDERING INFORMATION

PACKAGE PLASTIC 16-PIN	OPERATING TEMPERATURE RANGE
SSM2014P	–10°C to +55°C

PIN CONNECTIONS



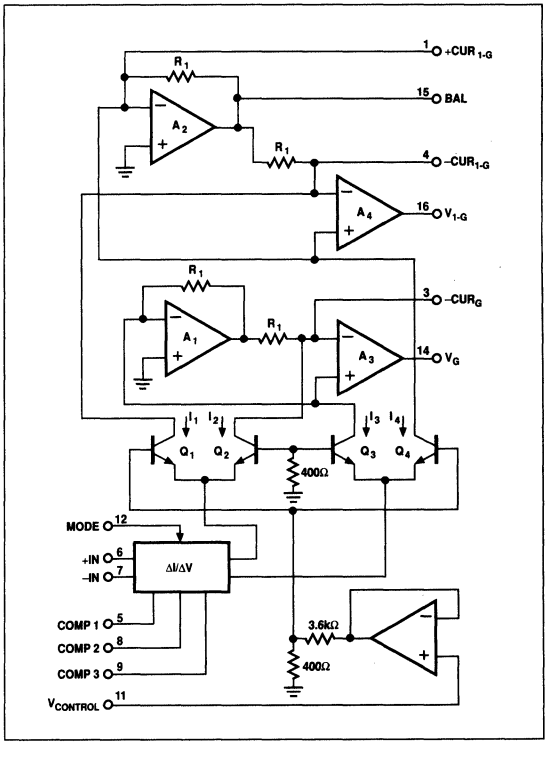
16-PIN PLASTIC DIP (P-Suffix)

DESCRIPTION

The SSM-2014 is an extremely flexible VCA building block that rivals the best monolithic VCAs while approaching the performance of modular devices. This versatile device acts as a VCA or OVCE (Operational Voltage-Controlled Element) and has inputs and outputs that can operate either in the current or voltage domain. To optimize performance at different signal levels, the SSM-2014 features programmable Class A or Class AB operation. This feature, along with the many configurations possible for operation make the SSM-2014 a unique and powerful signal processing tool. The device can be configured as a VCA or VCP (Voltage-Controlled Panner) and can replace a standard VCA and two or more operational amplifiers. Operation as a standard VCA provides up to 50dB gain and excellent specifications at any signal level.

The SSM-2014 is not recommended for new designs or purchases – the SSM-2018 is a pin-compatible upgrade at a lower cost.

BLOCK DIAGRAM



7

* Protected by U.S. Patents: 4,471,320 and 4, 560, 947. Other Patents pending. Mask work protected under the Semiconductor Chip Protection Act of 1983.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and $T_A = \pm 25°C$, unless otherwise specified.

PARAMETER	CONDITIONS	SSM-2014 MIN	TYP	MAX	UNITS
INPUT AMPLIFIER					
Bias Current		–	100	300	nA
Input Offset Current		–	15	30	nA
Input Offset Voltage		–	0.5	2	mV
Input Impedance		0.5	1	–	MΩ
Equivalent Input Noise	@ 1kHz	–	18	–	nV/√Hz
Common-Mode Range		–	+13, –13	–	V
Open-Loop Gain		75	100	–	V/mV
Effective Gain BW Product	VCA Configuration VCP Configuration	– –	12 .5	– –	MHz
Slew Rate	VCA Configuration	–	6	–	V/µs
Supply Current - Positive		–	7.5	9	mA
Supply Current - Negative		–	10	12	mA
OUTPUT AMPLIFIERS					
Offset Voltage		–	10	20	mV
Minimum Load Resistor	For Full Output Swing	10	9	–	kΩ
Output Voltage Swing		–	±13.5	–	V
Noise Residual	20kHz Bandwidth	–	8	–	µV
CONTROL PORT					
Bias Current		–	150	300	nA
Input Impedance		–	1	–	MΩ
Gain Constant	Ratio of Outputs	–	–30	–	mV/dB
Gain Constant Temperature Coefficient		–	–3300	–	ppm/°C
Gain Linearity		–	0.5	–	%
Control Feedthrough (Trimmed) Class A Class AB Intermediate	100Hz Sine Wave Applied to Control Port Causing –30dB to +20dB of Gain	 – – –	 2 0.5 1	 – – –	mV
Control Feedthrough (Untrimmed) Class A Class AB (Note 1) Intermediate (Note 1)	100Hz Sine Wave Applied to Control Port Causing –30dB to +20dB of Gain	 – – –	 25 5 15	 75 15 45	mV
Off Isolation	@ 1kHz	100	105	–	dB
Channel Specifications					
Noise - Class A (Note 2)	$R_{PIN\ 12}$ = 33kΩ, 20kHz BW	–	–85	–81	dBV
Noise - Class AB (Note 2)	$R_{PIN\ 12}$ = 330kΩ, 20kHz BW	–	–95	–92	dBV
Noise - Intermediate (Note 2)	$R_{PIN\ 12}$ = 43kΩ, 20kHz BW	–	–88	–85	dBV
THD - A @ A_V = 0dB (Note 3)	$R_{PIN\ 12}$ = 33kΩ	–	0.005	0.02	%
THD - A @ A_V = ±20dB (Note 3)	$R_{PIN\ 12}$ = 33kΩ	–	0.02	0.04	%
THD - AB @ A_V = 0dB (Note 3)	$R_{PIN\ 12}$ = 330kΩ	–	0.02	0.05	%
THD - AB @ A_V = ±20dB (Note 3)	$R_{PIN\ 12}$ = 330kΩ	–	0.06	0.12	%
THD - Intermediate @ A_V = 0dB (Note 3)	$R_{PIN\ 12}$ = 43kΩ	–	0.01	0.03	%
THD - Intermediate @ A_V = ±20dB (Note 3)	$R_{PIN\ 12}$ = 43kΩ	–	0.03	0.06	%

NOTES:
1. Symmetry trim only.
2. Parameter sample lot tested to maximum limits
3. V_{IN} and/or V_{OUT} = +10dBV. Specifications may be subject to change without notice.

ANALOG DEVICES

Low Noise Microphone Preamplifier

SSM-2015

FEATURES

- **Ultra Low Voltage Noise ..... 1.3nV/√Hz**
- **Wide Bandwidth ..... 700kHz @ G = 100**
- **High Slew Rate 8V/μs**
- **Very Low Harmonic Distortion ..... 0.007% @ G = 100**
- **Excellent CMR 100dB**
- **True Differential "Instrumentation" Type Inputs**
- **Programmable Input Stage Optimizes e_n vs R_{IN}**
- **Low Cost**

ORDERING INFORMATION

	OPERATING TEMPERATURE RANGE
SSM-2015P	–10°C to +55°C
Storage Temperature	–55°C to +125°C

GENERAL DESCRIPTION

The SSM-2015 is an ultra-low noise audio preamplifier particularly suited to microphone preamplification. Gains from 10 to over 2000 can be selected with wide bandwidth and low distortion over the full gain range.

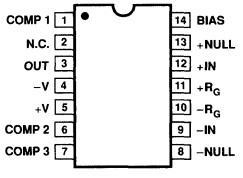
The very low voltage noise performance (1.3nV/√Hz) of the SSM-2015 is enhanced by a programmable input stage which allows overall noise to be optimized for source impedances of up to 4kΩ.

The SSM-2015's true differential inputs with high common-mode rejection provide easy interfacing to flotation transducers such as balanced microphone outputs, as well as single ended devices.

The SSM-2015 also offers high slew rate of about 8V/μs and full DC coupling without any crossover distortion.

This device is packaged in a 14-pin epoxy DIP and is guaranteed over the operating temperature range of –10°C to +55°C.

PIN CONNECTION



14-PIN EPOXY DIP (P-Suffix)

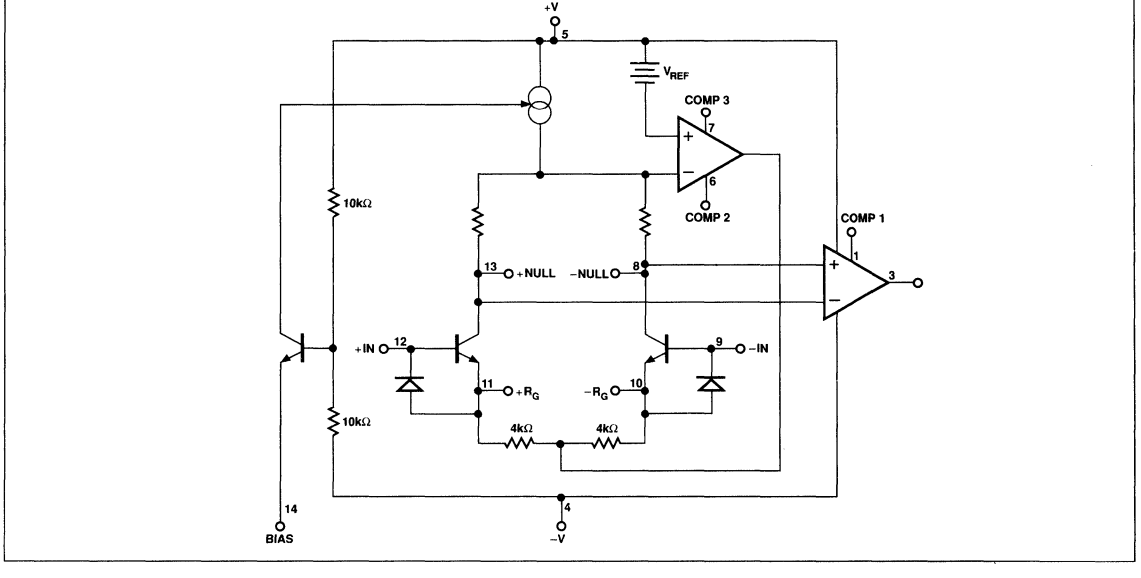
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Operating Temperature Range ..... –10°C to +55°C
Junction Temperature ..... +150C
Storage Temperature ..... –55°C to +125°C
Lead Temperature Range (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
14-Pin Plastic DIP (P)	76	33	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, $R_{BIAS} = 33k\Omega$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2015 MIN	SSM-2015 TYP	SSM-2015 MAX	UNITS
Total Harmonic Distortion (Note 1)	THD	V_{OUT} = 7V RMS, $R_L = 10k\Omega$				
		G = 1000				
		f = 1kHz	–	0.007	0.01	
		f = 10kΩ	–	0.015	0.02	
		G = 100				%
		f = = 1kHz	–	0.007	0.01	
		f = 10kHz	–	0.007	0.01	
		G = 10				
		f = 1kHz	–	0.01	0.015	
		f = 10kHz	–	0.01	0.015	
Input Referred Voltage Noise (Note 1)	E_n	Inputs Shorted to GND				
		20kHz Bandwidth				
		R_{BIAS} = 33KΩ				
		G = 1000	–	0.2	0.3	
		G = 100	–	0.3	0.5	
		G = 10	–	1.1	1.7	μV RMS
		R_{BIAS} = 150kΩ				
		G = 1000	–	0.28	0.45	
		G = 100	–	0.41	0.65	
		G = 10	–	1.1	1.7	
Input Current Noise (Note 1)	I_n	20kHz Bandwidth				
		R_{BIAS} = 33kΩ	–	250	380	
		R_{BIAS} = 68kΩ	–	200	300	pA RMS
		R_{BIAS} = 150kΩ	–	130	200	
Error From Gain Equation	ΔG	$R_1 = R_2 = 10k\Omega$				
		G = 1000	–	0.1	0.3	
		G = 100	–	0.1	0.3	dB
		G = 10	–	0.2	0.8	
Input Offset Voltage	V_{OS}	$R_1 = R_2 = 10k\Omega$				
		G = 1000	–	0.25	2	
		G = 100	–	0.3	7	mV
		G = 10	–	3	70	
Input Bias Current	I_B	V_{CM} = 0V				
		R_{BIAS} = 33kΩ	–	4.5	15	μA
		R_{BIAS} = 150kΩ	–	1	4	
Input Offset Current	I_{OS}	V_{CM} = 0V				
		R_{BIAS} = 33kΩ	–	0.5	2.5	μA
		R_{BIAS} = 150kΩ	–	0.15	0.7	
Common-Mode Rejection Ratio	CMRR	$R_1 = R_2 = 10k\Omega$				
		G = 1000	90	100	–	
		G = 100	70	95	–	dB
		G = 10	60	75	–	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 12$ to $\pm 17V$	–	100	–	dB
Common-Mode Voltage Range	CMVR		±4	±5.5	–	V
Common-Mode Input Impedance	R_{INCM}		–	50	–	MΩ
Differential-Mode Input Impedance	R_{IN}	G = 1000	–	0.5	–	
		G = 100	–	5	–	MΩ
		G = 10	–	20	–	
Output Voltage Swing	V_O	$R_L = 2k\Omega$	±10.5	±12.5	–	V
Output Current (Note 2)	I_{OUT}	Source	15	25	–	mA
		Sink	8	14	–	
–3dB Bandwidth	GBW	G = 1000	–	150	–	
		G = 100	–	700	–	kHz
		G = 10	–	1000	–	
Slew Rate	SR		–	8	–	V/μs
Supply Current	I_{SY}		8	12	16	mA

NOTES:

1. Parameter is sample tested to maximum limits.
2. Output is protected from short circuits to ground or either supply.

Specifications subject to change; consult latest data sheet.

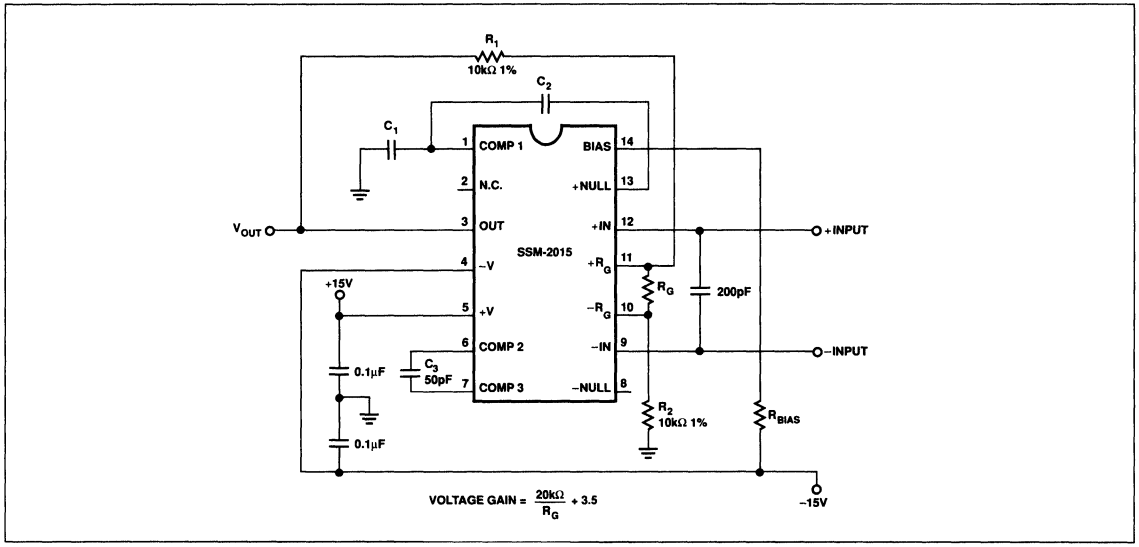


FIGURE 1: *Typical Application*

APPLICATIONS INFORMATION

PRINCIPLE OF OPERATION

Figure 1 shows a typical application for the SSM-2015. This device operates as a true differential amplifier with feedback returned directly to the emitters of the input stage transistors by R_1. This system produces both optimum noise and common-mode rejection while retaining a very high input impedance at both input terminals. An internal feedback loop maintains the input stage current at a value controlled by an external resistor (R_{BIAS}) from pin 14 to V–. This provides a programmability function which allows noise to be optimized for source impedances of up to 4kΩ.

GAIN SETTING

The nominal gain of the SSM-2015 is given by:

$$G \cong \frac{R_1 + R_2}{R_G} + \frac{R_1 + R_2}{8k\Omega} + 1$$

or

$$G = \frac{20k\Omega}{R_G} + 3.5 \quad \text{For } R_1,\ R_2 = 10k\Omega$$

R_1 and R_2 should be equal to 10kΩ for best results (see Figure 1). It is vital that good quality resistors be used in the gain setting network, since low quality types (notably carbon composition) can generate significant amounts of distortion and, under some conditions, low frequency noise. The SSM-2015 will function at gains above 10. Table 1 gives R_G values for most commonly used gains.

TABLE 1: R_G Values for Commonly Used Gains

$$R_G = \frac{R_1 + R_2}{G - 3.5}$$

GAIN	R_G	ERROR
10	3kΩ	+0.14dB
50	430Ω	+0.002dB
100	200Ω	+0.3dB
500	39Ω	+0.28dB
1000	20Ω	+0.03dB

FREQUENCY COMPENSATION

Referring to Figure 1, C_3 (50pF) provides compensation for the input stage current regulator, while C_1 and C_2 compensate the overall amplifier. The latter two depend on the value of R_{BIAS} chosen. Table 2 shows the recommended values for C_1 and C_2 at various R_{BIAS} levels. These values are valid for all gain settings.

TABLE 2: Recommended Compensation Values

R_{BIAS}	C_1	C_2
27kΩ - 47kΩ	15pF	15pF
47kΩ - 68kΩ	15pF	10pF
68kΩ - 150kΩ	30pF	5pF

The SSM-2015 has a bandwidth of at least 70kHz under worst case conditions (G = 1000, R_{BIAS} = 150kΩ) and considerably greater at higher set currents and lower gains. This excellent performance is supplemented by a highly symmetric slew rate for optimum large signal audio performance. The SSM-2015 provides stable operation with load capacitances of up to 150pF; larger capacitances should be decoupled with a 100Ω resistor in series with the output (R_1 in Figure 1 should remain connected to pin 3).

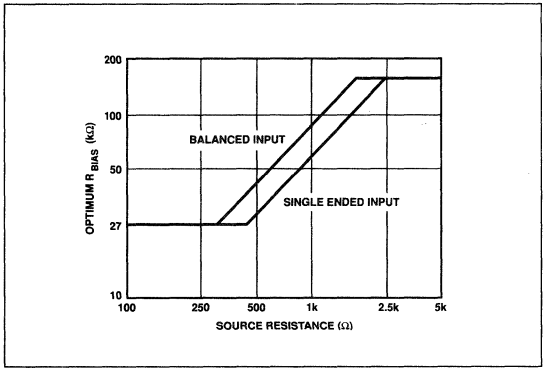


FIGURE 2: *Optimum R_{BIAS} vs. Source Resistance*

NOISE

The programmability of the SSM-2015 provides close to optimum performance for source impedances of up to 4kΩ, and is within 1dB of the theoretical minimum value between 500Ω and 2.5kΩ.

Figure 2 shows the recommended bias resistor (R_{BIAS}) versus source impedance, for balanced or single-ended inputs.

INPUTS

Although the SSM-2015 inputs are fully floating, care must be exercised to ensure that both inputs have a DC bias connection capable of maintaining them within the input common-mode range. The usual method of achieving this is to ground one side of the transducer as in Figure 3(a), but an alternative way is to float the transducer and use two resistors to set the bias point as in Figure 3(b). The value of these resistors can be up to 10kΩ, but they should be kept as small as possible to limit common-mode noise. Noise generated in the resistors themselves is negligible since it is attenuated by the transducer impedance. Balanced transducers give the best noise immunity, and interface directly as in Figure 3(c).

TRIMMING

The gain of the SSM-2015 can be easily trimmed by adjustment of R_G. However, two further trims may be desirable: Offset Voltage and Common-mode Rejection, although the SSM-2015 provides excellent untrimmed performance in both respects.

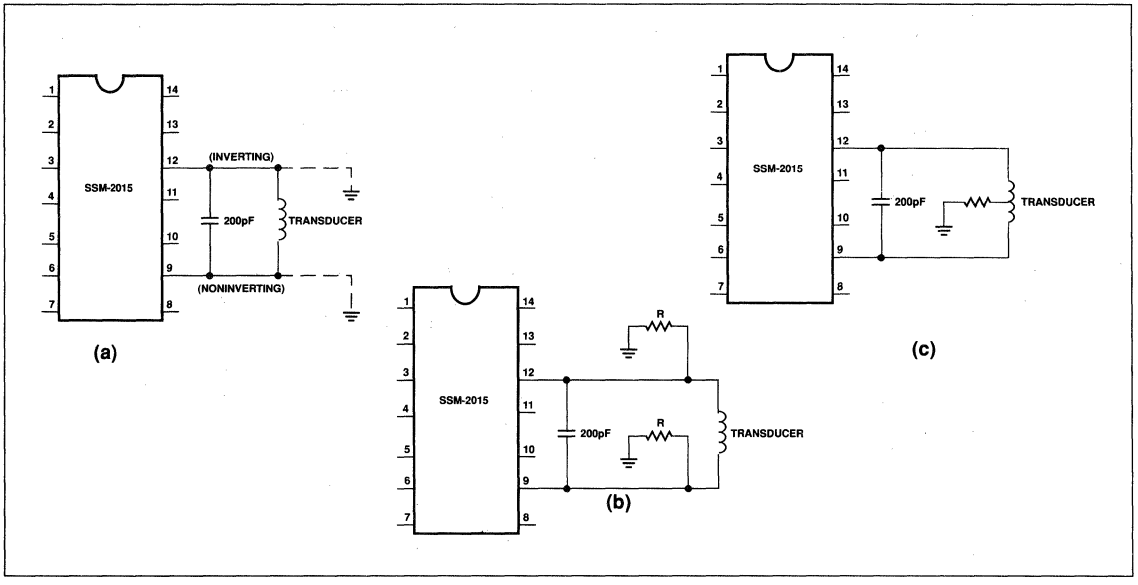


FIGURE 3: *Three Ways of Interfacing Transducers for High Noise Immunity*
(a) Single Ended (b) Pseudo Differential (c) True Differential

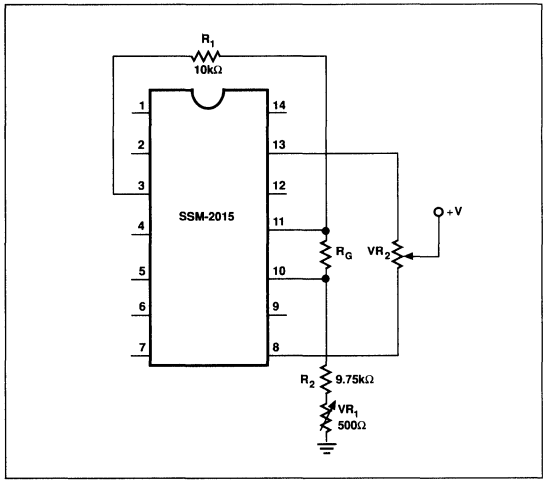


FIGURE 4: *Trimming the SSM-2015*

Figure 4 shows the trimming method for both parameters.

V_{R1} is the CMR trim and should be adjusted for minimum output with an $8V_{p\text{-}p}$ amplitude 60Hz Sine Wave common to both inputs.

V_{R2} is the offset voltage trim, and should be selected from Table 3. The offset trim should follow the CMR trim, since there is a small (non-reciprocal) interaction.

The offset trim can also be used to null out the gain control feedthrough. The output offset at low gains is determined by matching of the feedback resistors while at high gains it is determined by the matching of the input resistors. If the gain setting is changed rapidly, the output shift can cause an (audible) click or thump. To reduce or eliminate this, the offset at high gains is adjusted to be equal to the offset at low gains.

TABLE 3: Recommended Values for the Offset Voltage Trim

	R_{BIAS}		
	27kΩ - 47kΩ	**47kΩ - 68kΩ**	**68kΩ - 150kΩ**
V_{R2}, G = 10	500kΩ	250kΩ	250kΩ
V_{R2}, G = 100	500kΩ	100kΩ	100kΩ
V_{R2}, G = 1000	250kΩ	100kΩ	50kΩ

PHANTOM POWER

A recommended circuit for phantom microphone powering is shown in Figure 5. Z_1 through Z_4 provide transient overvoltage protection for the SSM-2015 whenever microphones are plugged in and out.

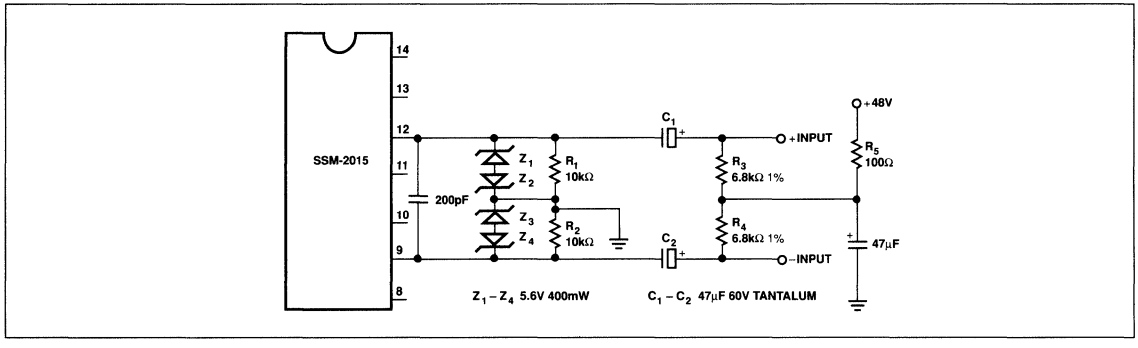


FIGURE 5: *SSM-2015 with Phantom Power*

Ultra Low Noise Differential Audio Preamplifier

SSM-2016

FEATURES

- **Ultra Low Voltage Noise ..... 800pV/√Hz Typ**
- **High Slew Rate ..... 10V/μs Typ**
- **Very Low Harmonic Distortion ..... @ G = 1000 0.009% Typ**
- **Wide Bandwidth ..... @ G = 1000 650kHz Typ**
- **Very Wide Supply Voltage Range ..... ±9V to ±36V**
- **High Output Drive Capability ..... ±40mA Min**
- **High Common-Mode Rejection ..... 100dB Typ**
- **Low Cost**

APPLICATIONS

- **Low Noise High-Gain Microphone Preamplifier**
- **Bus Summing Amplifier**
- **Differential Line Receiver**
- **Low Noise Instrumentation Amplifier**

ORDERING INFORMATION

PACKAGE PLASTIC 16-PIN	OPERATING TEMPERATURE RANGE
SSM2016P	–25°C to +55°C

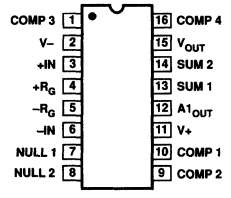
GENERAL DESCRIPTION

The SSM-2016 is an ultra low noise, low distortion differential audio preamplifier. The input referred noise of the SSM-2016 is about 800pV/√Hz which will result in a noise figure of 1dB when operated with a 150Ω source impedance. This ensures that a large number of inputs can be paralleled without seriously degrading the signal-to-noise ratio. In addition, this device provides exceptionally low harmonic distortion of only 0.009%(G = 1000, f = 1kHz) Typ.

Fabricated on a high voltage process, the SSM-2016 is capable of operating from a wide supply voltage range of ±9V to ±36V. A copper lead- frame DIP package is used to permit 1.5W of dissipation when driving heavy loads or operating from elevated supplies.

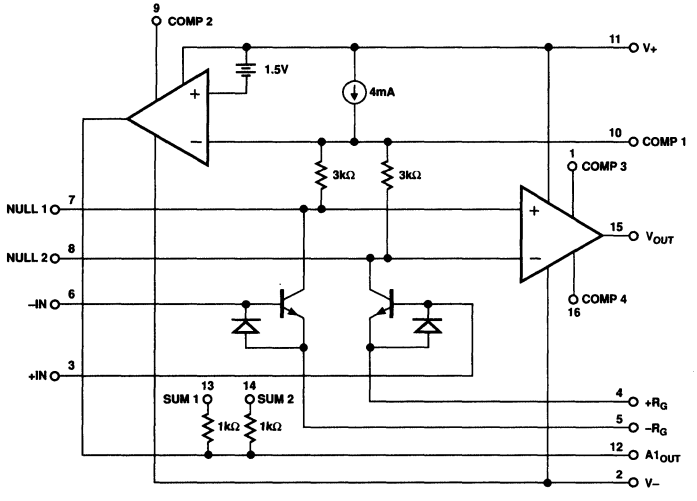
Continued

PIN CONNECTIONS



16-PIN PLASTIC DIP (P-Suffix)

BLOCK DIAGRAM



The SSM-2016 has been granted mask work protection under the Semiconductor Chip Protection Act of 1983.

GENERAL DESCRIPTION *Continued*

The SSM-2016 can source or sink a minimum of 40mA allowing a jack-field to be driven directly.

At low gains, the SSM-2016 offers a bandwidth of about 1MHz and 650kHz at 60dB of gain. Slew rate is typically 10V/µs at all gains.

The SSM-2016 is packaged in a 16-pin epoxy DIP and performance and characteristics are guaranteed over the operating temperature range of –25°C to +55°C.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±38V
Recommended Supply
Voltage Range ..... ±9V to ±36V
Current Into Any Pin
(Except Pins 2, 11, and 15) 40mA
Lead Temperature (Soldering, 60 sec) ..... 300°C
Storage Temperature ..... –65°C to +150°C
Package Dissipation 2W
Short-Circuit Duration (Note 1) ..... Indefinite
Operating Temperature Range ..... –25°C to 55°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
16-Pin Plastic DIP (P)	76	33	°C/W

NOTES:
1. Short-circuit duration is indefinite, provided dissipation limit is not exceeded.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package.

ELECTRICAL CHARACTERISTICS at V_S = ±18V, $R_1 = R_2$ = 5kΩ, $R_3 = R_4$ = 2kΩ, T_A = +25°C, unless otherwise noted.

			SSM-2016			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Total Harmonic Distortion	THD	$V_O = 10V_{RMS}$, R_L = 2kΩ				%
		G = 1000				
		f = 1kHz	–	0.009	0.015	
		f = 10kHz	–	0.015	0.02	
		G = 100				
		f = 1kHz	–	0.003	0.005	
		f = 10kHz	–	0.005	0.007	
		G = 10				
		f = 1kHz	–	0.002	0.003	
		f = 10kHz	–	0.003	0.005	
		$V_O = 10V_{RMS}$, R_L = 600Ω, V_S = ±20V				
		G = 1000				
		f = 1kHz	–	0.025	0.04	
		f = 10kHz	–	0.06	0.09	
		G = 100				
		f =1kHz	–	0.008	0.015	
		f = 10kHz	–	0.02	0.04	
		G = 10				
		f = 1kHz	–	0.005	0.008	
		f =10kHz	–	0.008	0.015	
Input Referred Voltage Noise (Note 1)	e_n	20kHz Bandwidth				μV_{RMS}
		G = 1000	–	0.11	0.16	
		G = 100	–	0.20	0.30	
		G = 10	–	0.80	1.2	
Input Current Noise (Note 1)	I_n	20 kHz Bandwidth	–	350	550	$pA/_{RMS}$
Slew Rate	SR		–	10	–	V/µs
–3dB Bandwidth (Note 2)	GBW	G = 1000	–	0.55	–	MHz
		G ≤ 100	–	1	–	
Input Offset Voltage	V_{OS}	G = 1000	–	0.5	2.5	mV
		G = 100	–	1.5	10	
		G = 10	–	5	8	
Input Bias Current	I_B	V_{CM} = 0V	–	9	25	µA
Input Offset Current	I_{OS}	V_{CM} = 0V	–	1.5	5.0	µA
Common-Mode Rejection Ratio	CMRR	G = 1000	96	100	–	dB
		G = 100	80.5	95	–	
		G = 10	64	75	–	
Power Supply Rejection Ratio	PSRR	V_S = ±9V to ±36V	90	100	–	dB
Common-Mode Voltage Range	CMVR		±7	±10	–	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 18V$, $R_1 = R_2 = 5k\Omega$, $R_3 = R_4 = 2k\Omega$, $T_A = +25°C$, unless otherwise noted.
Continued

PARAMETER	SYMBOL	CONDITIONS	SSM-2016 MIN	SSM-2016 TYP	SSM-2016 MAX	UNITS
Common-Mode Input Impedance	R_{INEM}		–	20	–	MΩ
Differential-Mode Input Impedance	R_{IN}	G = 1000 G = 100 G = 10	– – –	0.3 3 10	– – –	MΩ
Output Voltage Swing (Note 1)	V_O	$R_L = 2k\Omega$ $R_L = 600\Omega$, $V_S = \pm 20V$	±15 ±15	±17 ±17	– –	V
Output Current (Note 3)	I_{OUT}	Source Sink	40 40	70 70	– –	mA
Supply Current	I_{SY}	$V_{CM} = 0V$	10	12	16	mA
Error From Gain Equation			–	0.1	0.3	dB

NOTES:
1. Sample tested.
2. Bandwidth will be slew-rate limited at high output levels.
3. Output is protected from short circuits to ground or either supply.

Specifications subject to change; consult latest data sheet.

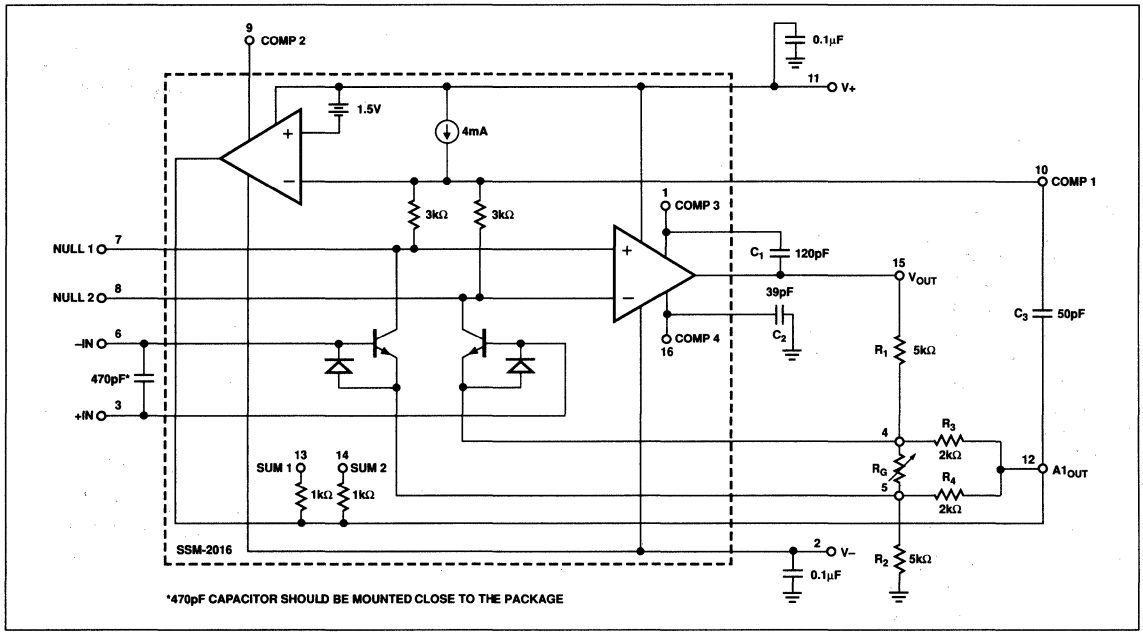


FIGURE 1: *Typical Preamplifier Amplification*

APPLICATIONS INFORMATION

PRINCIPLE OF OPERATION

The SSM-2016 operates as a true differential amplifier with feedback returned directly to the emitters of the input stage transistors by R_1 (See Figure 1). The differential pair is fed by a current source at the collectors and the required emitter current is supplied by a nulling (servo) amplifier through the external resistors R_3 and R_4 (Figure 1). This system produces both optimum noise and common-mode rejection while retaining a very high input impedance. The internal "servo" amplifier is used to control the input stage current independently of common-mode voltage and its output is accessible via pin 12.

GAIN SETTING

The nominal gain of the SSM-2016 is given by:

$$G = \frac{R_1 + R_2}{R_g} + \frac{R_1 + R_2}{R_3 + R_4} + 1$$

or

$$G = \frac{10k\Omega}{R_g} + 3.5 \quad \text{For } R_1 = R_2 = 5k\Omega,\ R_3 = R_4 = 2k\Omega$$

R_1 and R_2 should be equal to 5kΩ for best results. It is vital that good quality resistors be used in the gain setting network, since low quality types (notably carbon composition) can generate significant amounts of distortion and, under some conditions, low frequency noise.

The SSM-2016 is capable of operating at gains down to 3.5 at full performance. Gain range can be extended further by increasing R_3 and R_4 in Figure 1, but at the penalty of reduced common-mode input range. Gains below 2.5 are not practical unless the negative supply voltage is increased.

Note that tolerance of R_1 - R_4 directly affects the gain error and that good matching between R_1 - R_4 is essential to prevent degradation of the common-mode rejection performance.

The SSM-2016 provides internal 1kΩ resistors to replace R_3 and R_4 in applications where distortion is not too critical.

FREQUENCY COMPENSATION

The SSM-2016's internal "servo" amplifier is compensated by C_3, while C_1 and C_2 (see Figure 1) compensate the overall amplifier. The values shown maintain a very wide bandwidth with a good symmetrical slew rate. If desired, the bandwidth can be reduced by increasing the value of C_1.

NOISE PERFORMANCE

The SSM-2016's input referred noise is $0.11\mu V_{RMS}$ (20kHz bandwidth) at 60dB of gain, $0.2\mu V_{RMS}$ at 40dB, and $0.8\mu V_{RMS}$ at 20dB. The apparent increase at low gains is due to noise incurred in the feedback resistors and second stage becoming dominant. This noise is actually present at all times but becomes masked by input stage noise as the gain is increased.

The SSM-2016 is optimized for source impedances of 1kΩ or less and under these conditions, the noise performance is equal to the best discrete component designs. Considering that a "standard" microphone with impedance of 150Ω generates $1.6nV/\sqrt{Hz}$ of thermal noise, the SSM-2016's $800pV/\sqrt{Hz}$ of voltage noise or the corresponding noise figure of typically 1dB make the device virtually transparent to the user.

In applications where higher source impedances than 1kΩ are desired, the SSM-2015 preamplifier is recommended.

Another source of noise degradation is the chip's total power dissipation, since any increase in temperature will increase the noise. This effect is more pronounced at higher gains. As a result, the SSM-2016 uses a copper lead-frame package which greatly helps the power dissipation and the noise performance. The best noise performance of the SSM-2016 can be achieved at low supply voltages while driving light loads.

TOTAL HARMONIC DISTORTION

Figures 2 - 5 show the distortion behavior of SSM-2016. All measurements were taken at a $10V_{RMS}$ output to ensure a true "worst case" condition. No crossover distortion is observed at lower ouput levels. At 20dB of gain (Figure 2) total harmonic distortion (plus noise) is well below 0.01% at all audio frequencies. At 40dB of gain (Figure 3) some loading effects are evident, especially at higher frequencies, but the overall THD is still very low. The measurements at 60dB of gain (Figure 4) are a little misleading because the noise floor is at an equivalent level of 0.0085% at this gain. In fact, the real distortion components are not greatly increased from the 40dB case.

Figure 5 shows the intermodulation distortion performance of the SSM-2016. A basic SMPTE type test was performed with the main generator swept from 2.5kHz to 20kHz. The 60dB reading is once more mostly noise.

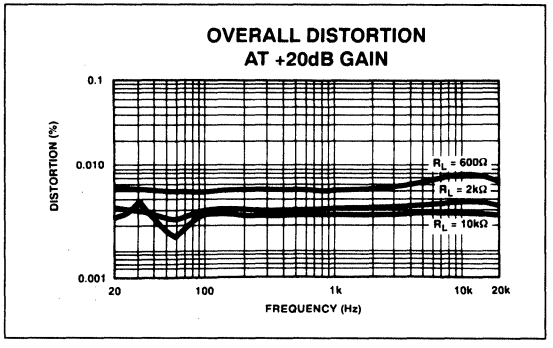


FIGURE 2

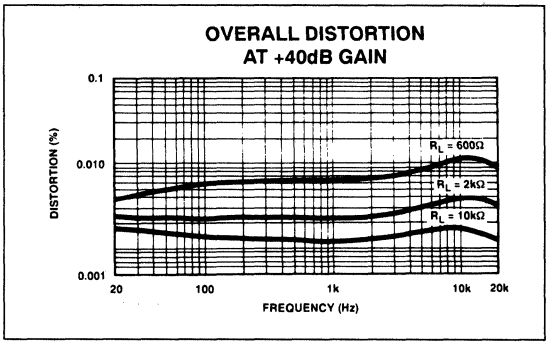


FIGURE 3

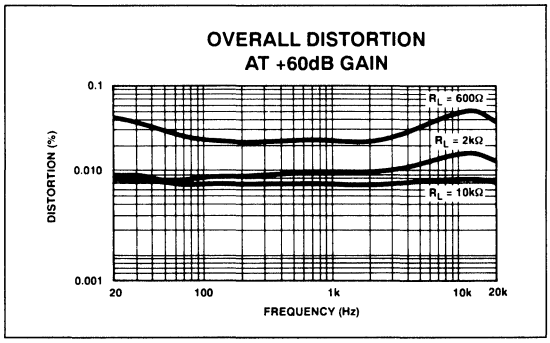


FIGURE 4

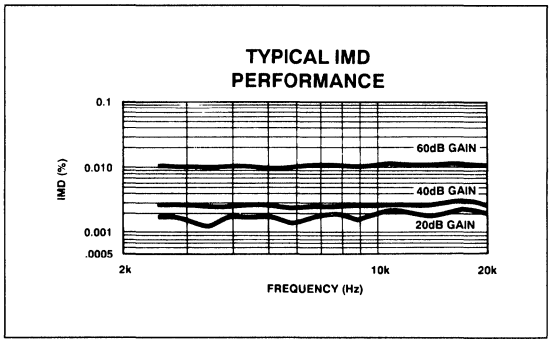


FIGURE 5

DRIVE CAPABILITY

Fabricated on a high voltage process, the SSM-2016 is capable of operating from ±9V to ±36V supplies. In addition, the powerful output stage is designed to drive a jack-field directly. The SSM-2016 is capable of driving a $10V_{RMS}$ sine wave into 600Ω load using ±18V supplies. However, ±20V or greater supplies are recommended to give a more comfortable headroom. A copper lead-frame DIP package is used to permit 1.5W of dissipation when driving heavy loads or operating from elevated supplies.

INPUTS

The SSM-2016 offers protection diodes across the base-emitter junctions of the input transistors. These prevent accidental avalanche breakdown which could seriously degrade noise performance. Additional clamp diodes are also provided to prevent the inputs from being forced too far beyond the supplies.

Although the SSM-2016's inputs are fully floating, care must be exercised to ensure that both inputs have a DC bias connection capable of maintaining them within the input common-mode range. The usual method of achieving this is to ground one side of the transducer as in Figure 6a, but an alternative way is to float the transducer and use two resistors to set the bias point as in figure 6b. The value of these resistors can be up to 10kΩ, but they should be kept as small as possible to limit common-mode pickup. Noise contribution by resistors themselves is negligible since it is attenuated by the transducer's impedance. Balanced transducers give the best noise immunity, and interface directly as in Figure 6c.

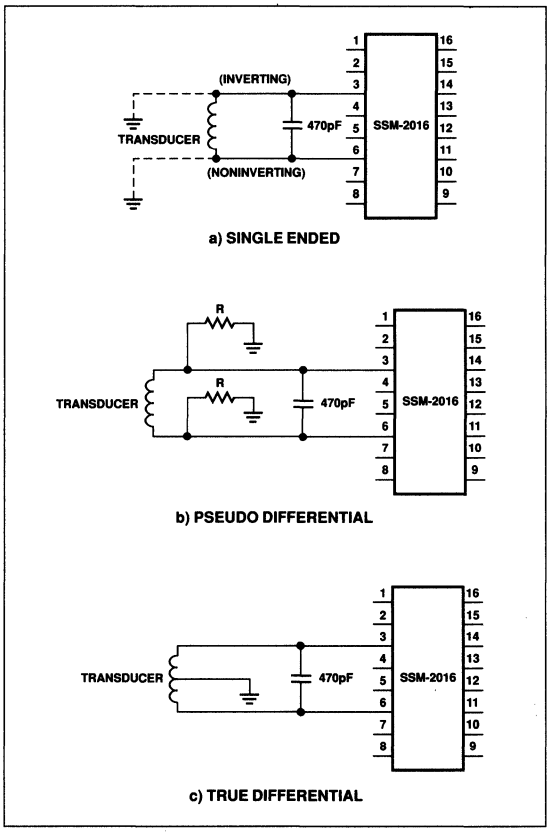


FIGURE 6: *Three Ways of Interfacing Transducers for High-Noise Immunity*

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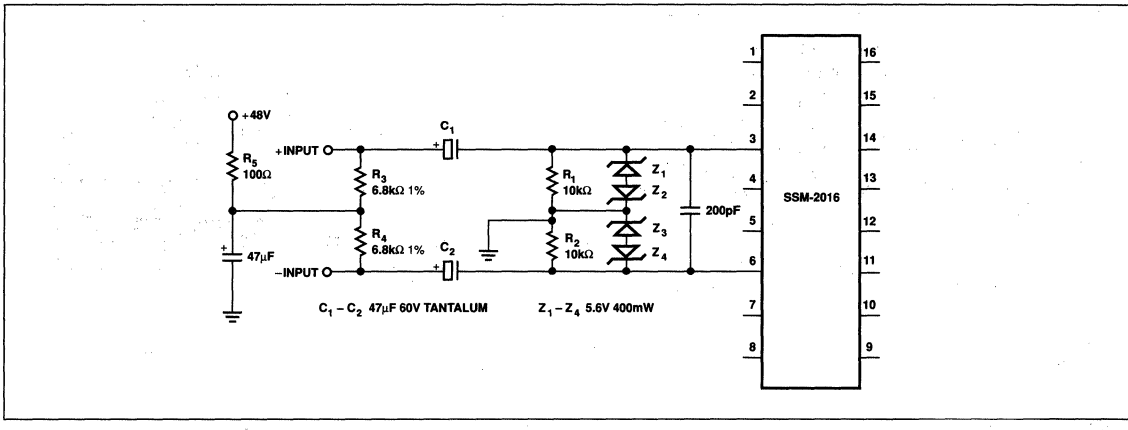


FIGURE 7: *SSM-2016 with Phantom Power*

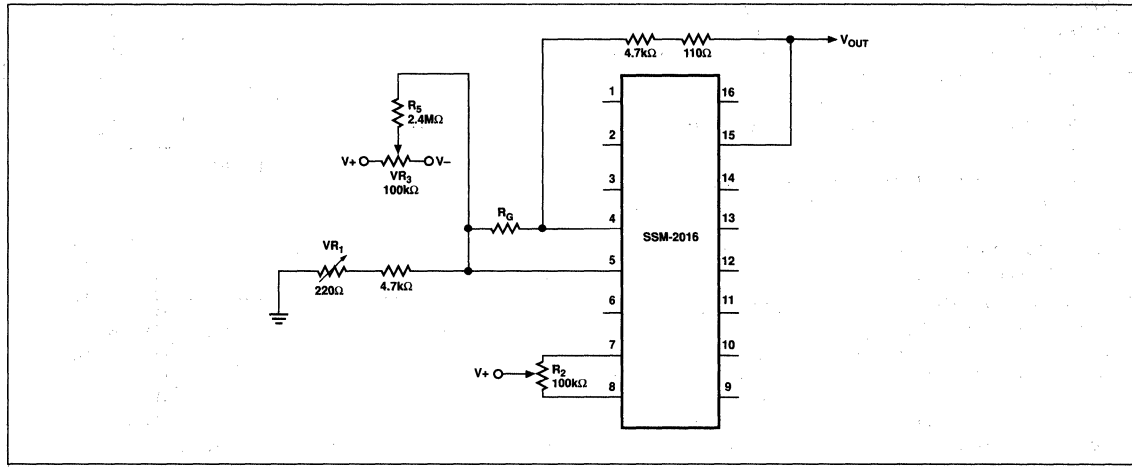


FIGURE 8: *Trimming Circuit*

PHANTOM POWERING

A typical phantom microphone powering circuit is shown in Figure 7. Z_1 through Z_4 provide transient overvoltage protection for the SSM-2016 whenever microphones are plugged in and out.

TRIMMING

The SSM-2016 accommodates four types of trimming: gain, high-gain offset, low-gain offset, and common-mode rejection. All four can be accomplished with the circuits shown in Figure 8.

Gain trim on the SSM-2016 is readily accomplished by adjusting R_G. VR_1 adjusts the common-mode rejection, VR_2 the high-gain offset, and VR_3 the low-gain offset. Common-mode rejection is best adjusted by applying an $8V_{p-p}$ 60Hz (50Hz in Europe) sine wave to both inputs and adjusting VR_1 for minimum output. Interaction is minimized by trimming the high-gain offset first, followed by the CMR and finally the low-gain offset. A two-pass trim is recommended for best results. Note that the overall gain has been reduced slightly to allow convenient values of resistors.

If the low-gain offset trim is not used, then gain control feedthrough can still be reduced by adjusting the high-gain offset to equal the low-gain offset by means of VR_2.

BUS SUMMING AMPLIFIER

In addition to its use as a microphone preamplifier, the SSM-2016 can be used as a very low noise summing amplifier. Such a circuit is particularly useful when many medium impedance outputs are summed together to produce a high effective noise gain.

The principle of the summing amplifier is to ground the SSM-2016 inputs . Under these conditions, pins 4 and 5 are AC virtual grounds sitting about 0.65V below ground. Any current injected into these points must flow through the feedback resistor (R_1) and hence are amplified to appear in the the output. Moreover, both positive (pin 5) and negative (pin 6) transfer characteristics are available simultaneously in contrast to the usual "inverting only" configuration.

To remove the 0.65V offset, the circuit of Figure 9 is recommended.

A_2 forms a "servo" amplifier feeding the SSM-2016's inputs. This places pins 4 and 5 at a true DC virtual ground. R_6 in conjunction with C_6 remove the voltage noise of A_2 and in fact just about any operational amplifier will work well here since it is removed from the signal path. If the DC offset at pins 4 and 5 is not too critical, then the servo loop can be replaced by the diode biasing scheme of Figure 9a. If AC coupling is used throughout, then pins 3 and 6 may be directly grounded.

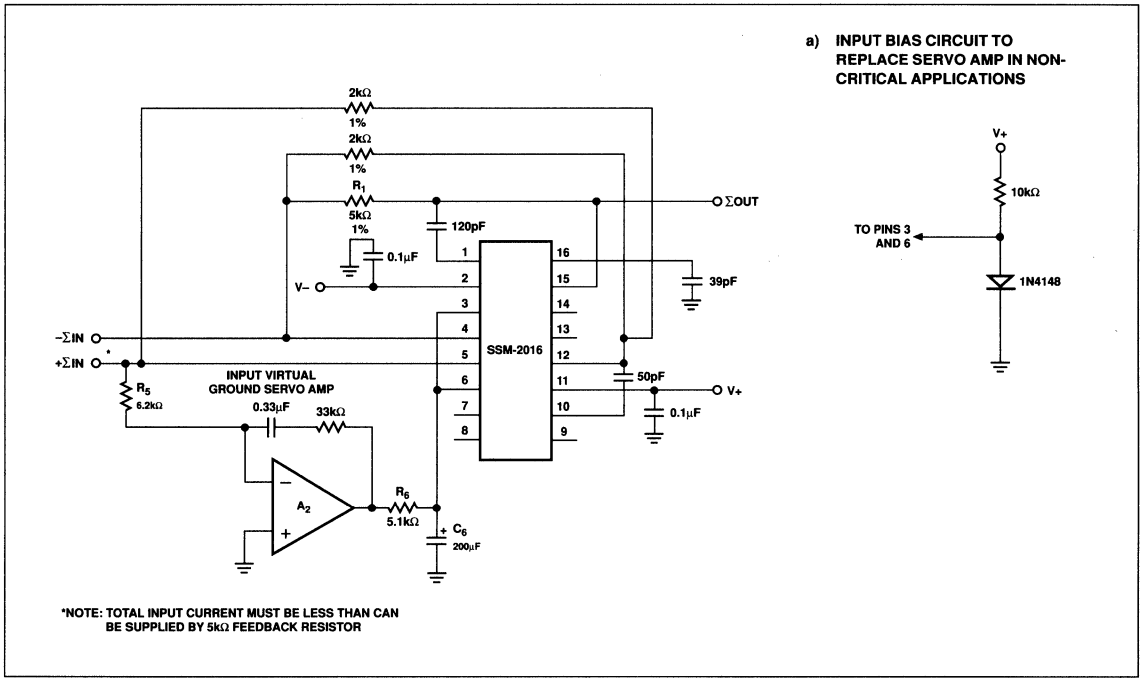


FIGURE 9: *Bus Summing Amplifier*

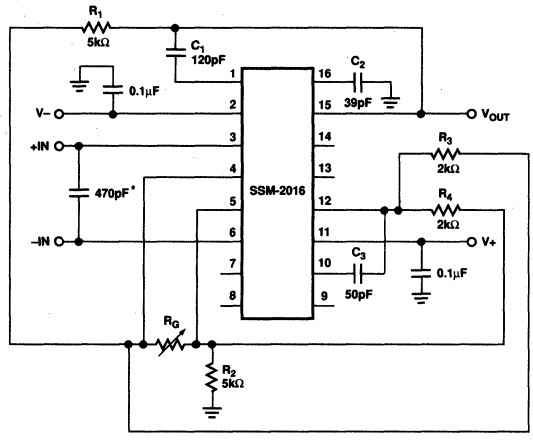


FIGURE 10: *Typical Connection for Breadboarding Purposes*

Self-Contained Audio Preamplifier

SSM-2017

FEATURES

Excellent Noise Performance: 950 pV/$\sqrt{Hz}$ or 1.5 dB Noise Figure
Ultralow THD: <0.01% @ G = 100 Over the Full Audio Band
Wide Bandwidth: 1 MHz @ G = 100
High Slew Rate: 17 V/μs typ
Unity Gain Stable
True Differential Inputs
Subaudio 1/f Noise Corner
8-Pin Mini-DIP with Only One External Component Required
Very Low Cost
Extended Temperature Range: −40°C to +85°C

APPLICATIONS

Audio Mix Consoles
Intercom/Paging Systems
Two-Way Radio
Sonar
Digital Audio Systems

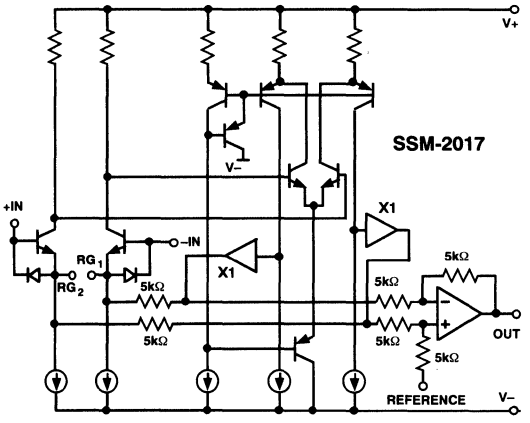
GENERAL DESCRIPTION

The SSM-2017 is a latest generation audio preamplifier combining SSM preamplifier design expertise with advanced processing. The result is excellent audio performance from a self-contained 8-pin mini-DIP device, requiring only one external gain set resistor or potentiometer. The SSM-2017 is further enhanced by its unity gain stability.

Key specifications include ultralow noise (1.5 dB noise figure) and THD (<0.01% at G = 100), complemented by wide bandwidth and high slew rate.

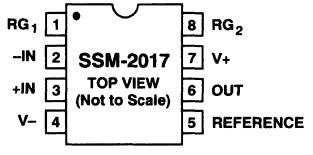
Applications for this low cost device include microphone preamplifiers and bus summing amplifiers in professional and consumer audio equipment, sonar, and other applications requiring a low noise instrumentation amplifier with high gain capability.

FUNCTIONAL BLOCK DIAGRAM

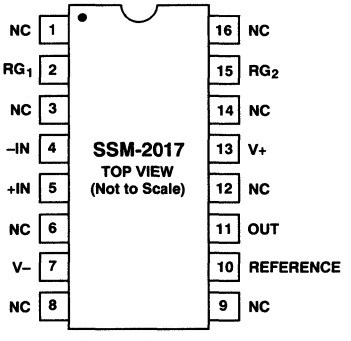


PIN CONNECTIONS

Epoxy Mini-DIP (P Suffix)
and
Hermetic DIP (Z Suffix)



16-Pin SOIC (S Suffix)



NC = NO CONNECT

7

SSM-2017—SPECIFICATIONS (V_S = ±15 V and −40°C ≤ T_A ≤ +85°C, unless otherwise specified. Typical specifications apply at T_A = +25°C.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
DISTORTION PERFORMANCE		T_A = +25°C V_O = 7 V_{RMS} R_L = 5 kΩ				
Total Harmonic Distortion Plus Noise	THD+N	G = 1000, f = 1 kHz		0.012		%
		G = 100, f = 1 kHz		0.005		%
		G = 10, f = 1 kHz		0.004		%
		G = 1, f = 1 kHz		0.008		%
NOISE PERFORMANCE						
Input Referred Voltage Noise Density	e_n	f = 1 kHz, G = 1000		0.95		$nV/\sqrt{Hz}$
		f = 1 kHz; G = 100		1.95		$nV/\sqrt{Hz}$
		f = 1 kHz; G = 10		11.83		$nV/\sqrt{Hz}$
		f = 1 kHz; G = 1		107.14		$nV/\sqrt{Hz}$
Input Current Noise Density	i_n	f = 1 kHz, G = 1000		2		$pA/\sqrt{Hz}$
DYNAMIC RESPONSE						
Slew Rate	SR	G = 10 R_L = 4.7 kΩ C_L = 50 pF T_A = +25°C	10	17		V/μs
Small Signal Bandwidth	$BW_{-3\ dB}$	G = 1000		200		kHz
		G = 100		1000		kHz
		G = 10		2000		kHz
		G = 1		4000		kHz
INPUT						
Input Offset Voltage	V_{IOS}			0.1	1.2	mV
Input Bias Current	I_B	V_{CM} = 0 V		6	25	μA
Input Offset Current	I_{OS}	V_{CM} = 0 V		±0.002	±2.5	μA
Common-Mode Rejection	CMR	V_{CM} = ±8 V				
		G = 1000	80	112		dB
		G = 100	60	92		dB
		G = 10	40	74		dB
		G = 1, T_A = +25°C	26	54		dB
		G = 1, T_A = −40°C to +85°C	20	54		dB
Power Supply Rejection	PSR	V_S = ±6 V to ±18 V				
		G = 1000	80	124		dB
		G = 100	60	118		dB
		G = 10	40	101		dB
		G = 1	26	82		dB
Input Voltage Range	IVR		±8			V
Input Resistance	R_{IN}	Differential, G = 1000		1		MΩ
		G = 1		30		MΩ
		Common Mode, G = 1000		5.3		MΩ
		G = 1		7.1		MΩ
OUTPUT						
Output Voltage Swing	V_O	R_L = 2 kΩ; T_A = +25°C	±11.0	±12.3		V
Output Offset Voltage	V_{OOS}			−40	500	mV
Minimum Resistive Load Drive		T_A = +25°C		2		kΩ
		T_A = −40°C to +85°C		4.7		kΩ
Maximum Capacitive Load Drive				50		pF
Short Circuit Current Limit	I_{SC}	Output-to-Ground Short		±50		mA
Output Short Circuit Duration					10	sec
GAIN						
Gain Accuracy	$R_G = \frac{10\ k\Omega}{G-1}$	T_A = +25°C				
		R_G = 10 Ω, G = 1000		0.25	1	dB
		R_G = 101 Ω, G = 100		0.20	1	dB
		R_G = 1.1 kΩ, G = 10		0.20	1	dB
		R_G = ∞, G = 1		0.05	0.5	dB
Maximum Gain	G			70		dB

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
REFERENCE INPUT						
Input Resistance				10		kΩ
Voltage Range				±8		V
Gain to Output				1		V/V
POWER SUPPLY						
Supply Voltage Range	V_S		±6		±22	V
Supply Current	I_{SY}	V_{CM} = 0 V, R_L = ∞		±10.6	±14.0	mA

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±22 V
Input Voltage . . . . . Supply Voltage
Output Short Circuit Duration . . . . . 10 sec
Storage Temperature Range (P, Z Packages) . −65°C to +150°C
Junction Temperature (T_J) . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C
Operating Temperature Range . . . . . −40°C to +85°C
Thermal Resistance[1]
8-Pin Hermetic DIP (Z): θ_{JA} = 134; θ_{JC} = 12 . . . . . °C/W
8-Pin Plastic DIP (P): θ_{JA} = 96; θ_{JC} = 37 . . . . . °C/W
16-Pin SOIC (S): θ_{JA} = 92; θ_{JC} = 27 . . . . . °C/W

NOTE
[1]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and plastic DIP; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

ORDERING GUIDE

Model	Operating Temperature Range*	Package
SSM-2017P	−40°C to +85°C	8-Pin Plastic DIP
SSM-2017Z	−40°C to +85°C	8-Pin Hermetic DIP
SSM-2017S	−40°C to +85°C	16-Lead SOIC

*XIND = −40°C to +85°C.

Typical Performance Characteristics

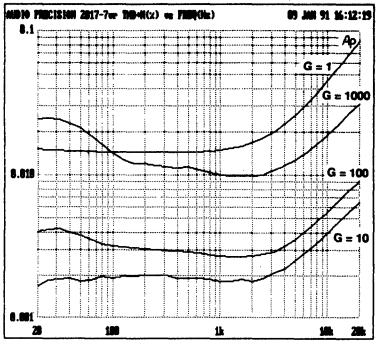


Figure 1. Typical THD+Noise at G = 1, 10, 100, 1000; V_O = 7 V_{RMS}, V_S = ±15 V, R_L = 5 kΩ; T_A = +25°C*

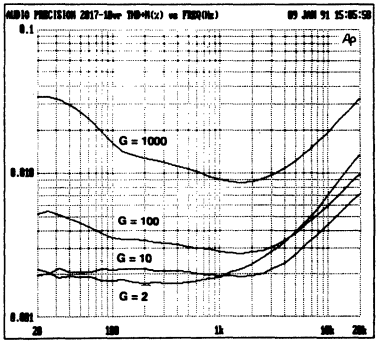


Figure 2. Typical THD+Noise at G = 2, 10, 100, 1000; V_O = 10 V_{RMS}, V_S = ±18 V, R_L = 5 kΩ; T_A = +25°C*

*80 kHz low-pass filter used for Figures 1–2.

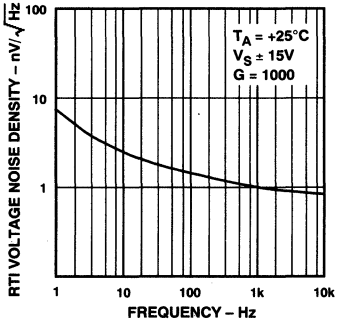


Figure 3. Voltage Noise Density vs. Frequency

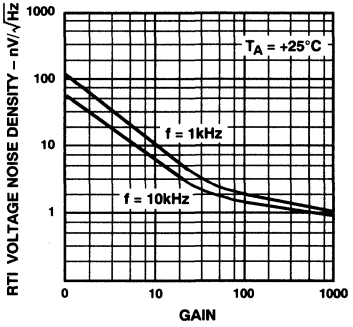


Figure 4. RTI Voltage Noise Density vs. Gain

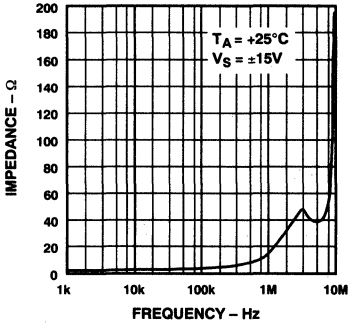


Figure 5. Output Impedance vs. Frequency

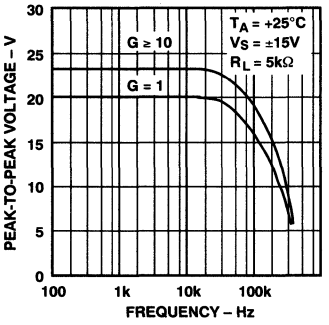


Figure 6. Maximum Output Swing vs. Frequency

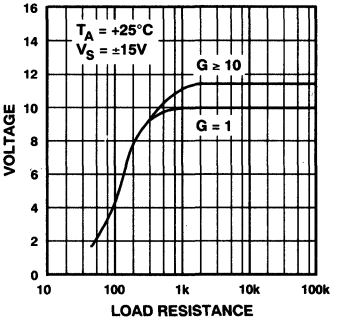


Figure 7. Maximum Output Voltage vs. Load Resistance

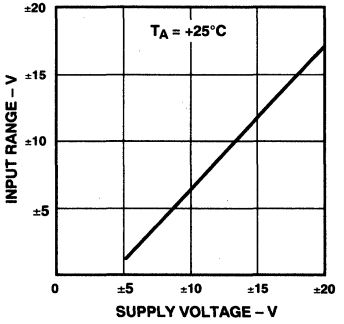


Figure 8. Input Voltage Range vs. Supply Voltage

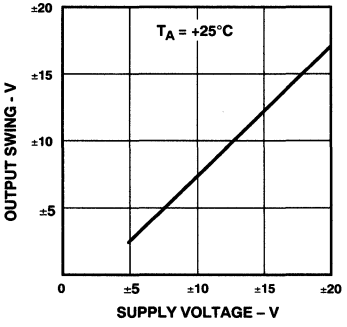


Figure 9. Output Voltage Range vs. Supply Voltage

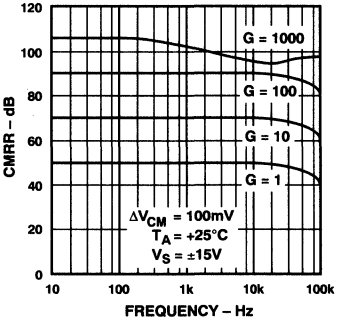


Figure 10. CMRR vs. Frequency

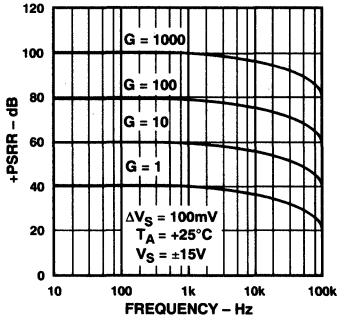


Figure 11. +PSRR vs. Frequency

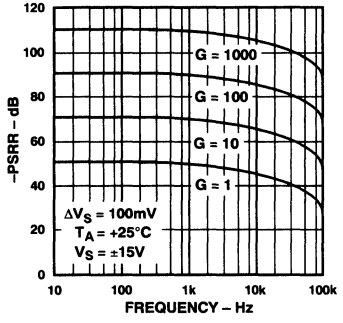


Figure 12. –PSRR vs. Frequency

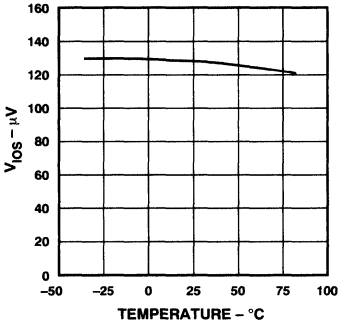


Figure 13. V_{IOS} vs. Temperature

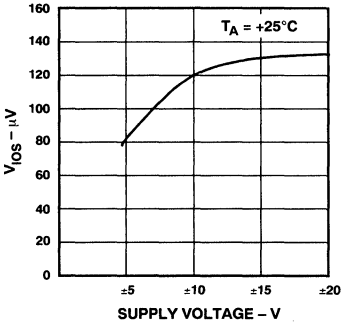


Figure 14. V_{IOS} vs. Supply Voltage

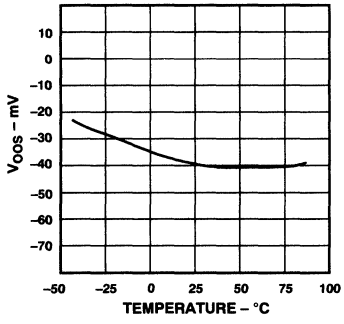


Figure 15. V_{OOS} vs. Temperature

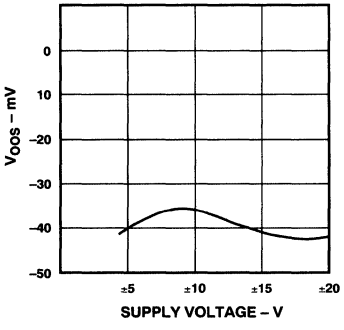


Figure 16. V_{OOS} vs. Supply Voltage

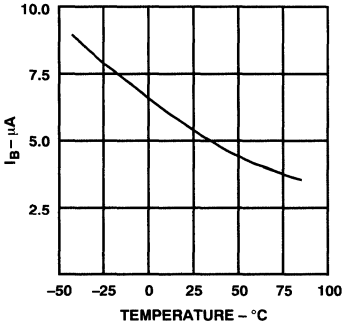


Figure 17. I_B vs. Temperature

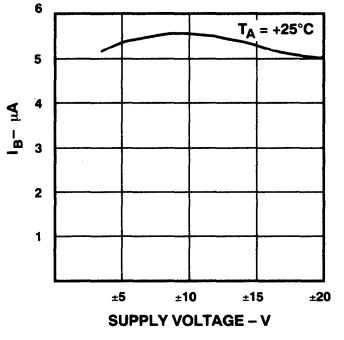


Figure 18. I_B vs. Supply Voltage

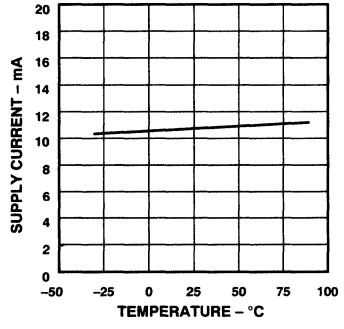


Figure 19. I_{SY} vs. Temperature

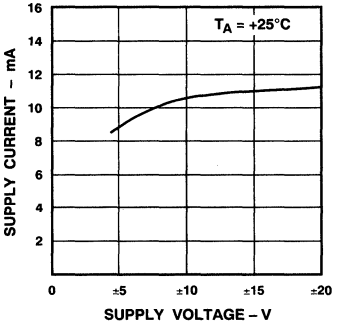
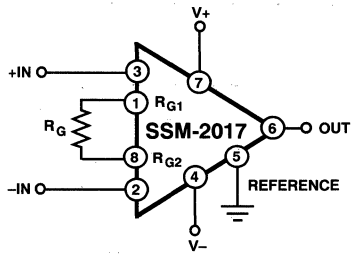


Figure 20. I_{SY} vs.Supply Voltage

7



$$G = \frac{V_{OUT}}{(+IN) - (-IN)} = \left(\frac{10k\Omega}{R_G}\right) + 1$$

Basic Circuit Connections

GAIN

The SSM-2017 only requires a single external resistor to set the voltage gain. The voltage gain, G, is:

$$G = \frac{10\ k\Omega}{R_G} + 1$$

and

$$R_G = \frac{10\ k\Omega}{G - 1}$$

For convenience, Table I lists various values of R_G for common gain levels.

Table I. Values of R_G for Various Gain Levels

A_V	dB	R_G
1	0	NC
3.2	10	4.7k
10	20	1.1k
31.3	30	330
100	40	100
314	50	32
1000	60	10

The voltage gain can range from 1 to 3500. A gain set resistor is not required for unity gain applications. Metal-film or wire-wound resistors are recommended for best results.

The total gain accuracy of the SSM-2017 is determined by the tolerance of the external gain set resistor, R_G, combined with the gain equation accuracy of the SSM-2017. Total gain drift combines the mismatch of the external gain set resistor drift with that of the internal resistors (20 ppm/°C typ).

Bandwidth of the SSM-2017 is relatively independent of gain as shown in Figure 21. For a voltage gain of 1000, the SSM-2017 has a small-signal bandwidth of 200 kHz. At unity gain, the bandwidth of the SSM-2017 exceeds 4 MHz.

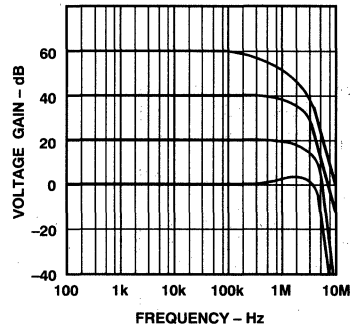


Figure 21. Bandwidth of the SSM-2017 for Various Values of Gain

NOISE PERFORMANCE

The SSM-2017 is a very low noise audio preamplifier exhibiting a typical voltage noise density of only 1 nV/$\sqrt{Hz}$ at 1 kHz. The exceptionally low noise characteristics of the SSM-2017 are in part achieved by operating the input transistors at high collector currents since the voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. As a result, the outstanding voltage noise performance of the SSM-2017 is obtained at the expense of current noise performance. At low preamplifier gains, the effect of the SSM-2017's voltage and current noise is insignificant.

The total noise of an audio preamplifier channel can be calculated by:

$$E_n = \sqrt{e_n^2 + (i_n R_s)^2 + e_t^2}$$

where:

E_n = total input referred noise

e_n = amplifier voltage noise

i_n = amplifier current noise

R_s = source resistance

e_t = source resistance thermal noise.

For a microphone preamplifier, using a typical microphone impedance of 150 Ω the total input referred noise is:

e_n = 1 *nV*/$\sqrt{Hz}$ @ 1 *kHz*, *SSM*-2017 e_n

i_n = 2 *pA*/$\sqrt{Hz}$ @ 1 *kHz*, *SSM*-2017 i_n

R_S = 150 Ω, *microphone source impedance*

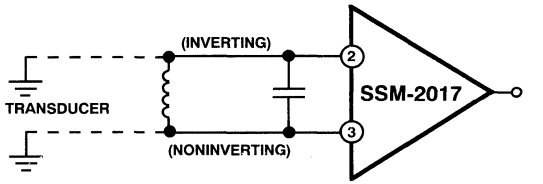
e_t = 1.6 *nV*/$\sqrt{Hz}$ @ 1 *kHz*, *microphone thermal noise*

$E_n = \sqrt{(1\ nV/\sqrt{Hz})^2 + 2\,(2\ pA/\sqrt{Hz} \times 150\ \Omega)^2 + (1.6\ nV/\sqrt{Hz})^2} =$ 1.93 *nV*/$\sqrt{Hz}$ @ 1 *kHz*.

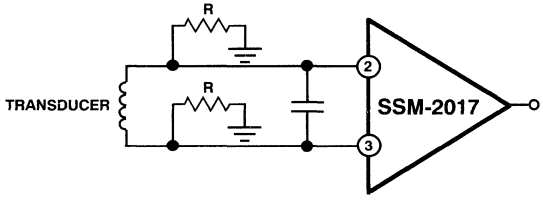
This total noise is extremely low and makes the SSM-2017 virtually transparent to the user.

INPUTS

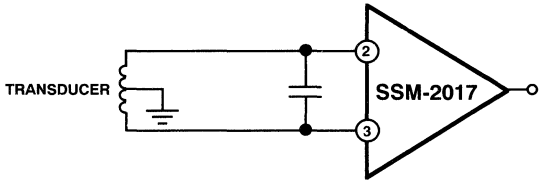
The SSM-2017 has protection diodes across the base emitter junctions of the input transistors. These prevent accidental avalanche breakdown which could seriously degrade noise performance. Additional clamp diodes are also provided to prevent the inputs from being forced too far beyond the supplies.



a. Single Ended



b. Pseudo Differential



c. True Differential

Figure 22. Three Ways of Interfacing Transducers for High Noise Immunity

Although the SSM-2017's inputs are fully floating, care must be exercised to ensure that both inputs have a dc bias connection capable of maintaining them within the input common-mode range. The usual method of achieving this is to ground one side of the transducer as in Figure 22a, but an alternative way is to float the transducer and use two resistors to set the bias point as in Figure 22b. The value of these resistors can be up to 10 kΩ, but they should be kept as small as possible to limit common-mode pickup. Noise contribution by resistors themselves is negligible since it is attenuated by the transducer's impedance. Balanced transducers give the best noise immunity and interface directly as in Figure 22c.

REFERENCE TERMINAL

The output signal is specified with respect to the reference terminal, which is normally connected to analog ground. The reference may also be used for offset correction or level shifting. A reference source resistance will reduce the common-mode rejection by the ratio of 5 kΩ/R_{REF}. If the reference source resistance is 1 Ω, then the CMR will be reduced to 74 dB (5 kΩ/1 Ω = 74 dB).

COMMON-MODE REJECTION

Ideally, a microphone preamplifier responds only to the difference between the two input signals and rejects common-mode voltages and noise. In practice, there is a small change in output voltage when both inputs experience the same common-mode voltage change; the ratio of these voltages is called the common-mode gain. Common-mode rejection (CMR) is the logarithm of the ratio of differential-mode gain to common-mode gain, expressed in dB.

PHANTOM POWERING

A typical phantom microphone powering circuit is shown in Figure 23. Z_1 through Z_4 provide transient overvoltage protection for the SSM-2017 whenever microphones are plugged in or unplugged.

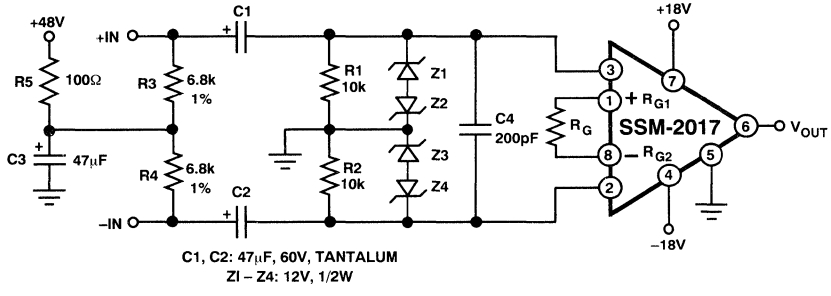


Figure 23. SSM-2017 in Phantom Powered Microphone Circuit

BUS SUMMING AMPLIFIER

In addition to is use as a microphone preamplifier, the SSM-2017 can be used as a very low noise summing amplifier. Such a circuit is particularly useful when many medium impedance outputs are summed together to produce a high effective noise gain.

The principle of the summing amplifier is to ground the SSM-2017 inputs. Under these conditions, Pins 1 and 8 are ac virtual grounds sitting about 0.55 V below ground.

To remove the 0.55 V offset, the circuit of Figure 24 is recommended.

A_2 forms a "servo" amplifier feeding the SSM-2017's inputs. This places Pins 1 and 8 at a true dc virtual ground. R4 in conjunction with C2 remove the voltage noise of A_2, and in fact just about any operational amplifier will work well here since it is removed from the signal path. If the dc offset at Pins 1 and 8 is not too critical, then the servo loop can be replaced by the diode biasing scheme of Figure 24. If ac coupling is used throughout, then Pins 2 and 3 may be directly grounded.

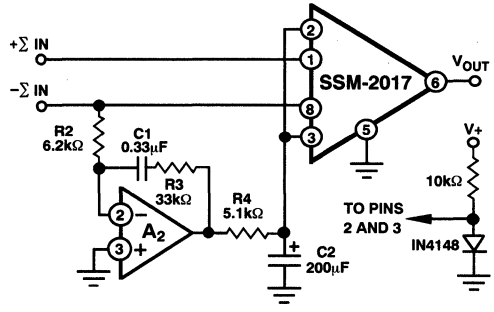


Figure 24. Bus Summing Amplifier

ANALOG DEVICES

Voltage-Controlled Amplifier/OVCE

SSM-2018

FEATURES

Wide Dynamic Range
118 dB typ (Class AB)
108 dB typ (Class A)
Wide Gain Range
140 dB typ
Excellent THD and IMD Performance Over Gain, Attenuation and Frequency
Low Control Feedthrough
1 mV typ (Class AB)
Buffered Control Port and Current and Voltage Outputs
Accepts Low or High Impedance Inputs
Low External Parts Count
Low Cost

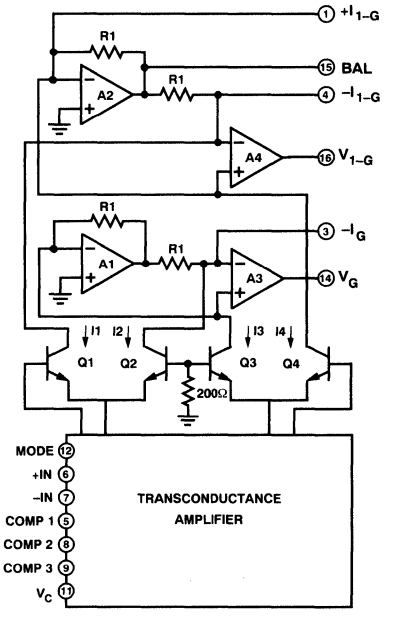
APPLICATIONS

Voltage-Controlled Amplifiers
Mixing Console Fader Automation Systems
Compressors/Limiters
Noise Gates
Noise Reduction Systems
Telephone Line Interfaces
Automatic or Remote Volume Controllers
Voltage-Controlled Equalizers
Voltage-Controlled Panners

GENERAL DESCRIPTION

The SSM-2018 voltage-controlled amplifier is an advanced integrated audio gain block featuring exceptional performance in voltage-controlled amplifier, panner, equalizer, and preamplifier functions. An extremely flexible architecture features inputs and outputs which can be configured for differential and single-ended signals, in both current and voltage modes. Also, the control port input and voltage outputs of the SSM-2018 are buffered, assuring optimal performance while significantly reducing the external parts count compared to other VCA products. The internal gain core can be programmed by the user for Class A, Class AB, or Intermediate operation by the selection of an external resistor. The SSM-2018 features excellent noise performance and exhibits negligible increase in distortion in Class AB operation over Class A, resulting in unusually low noise and distortion simultaneously.

FUNCTIONAL DIAGRAM



The SSM-2018's unique operational voltage-controlled element (OVCE) architecture is easily configured into many voltage-controlled functions by utilizing the simple feedback connections. Existing SSM-2014 sockets can be directly upgraded to the SSM-2018, with the additional benefit of a significant reduction in the number of external components needed to achieve full performance.

Combined with a voltage output DAC and multiplexed sample-and-hold circuit such as the DAC-7224 and SMP-08, or a multiple DAC such as the DAC-8800, high quality digital control of many audio functions can be realized with very low parts count, and at low cost.

7

SSM-2018—SPECIFICATIONS

(V_S = ±15 V and −40°C ≤ T_A ≤ +85°C with 18 kΩ feedback resistors, unless otherwise specified. Typical specifications apply to operation at T_A = +25°C.)

Parameters	Symbol	Conditions	Min	Typ	Max	Units
INPUT AMPLIFIER						
Bias Current	I_B	V_{CM} = 0 V		0.25	1	μA
Input Offset Voltage	V_{IOS}	V_{CM} = 0 V		1	20	mV
Input Offset Current	I_{IOS}	V_{CM} = 0 V		10	100	nA
Input Impedance	Z_{IN}			4		MΩ
Equivalent Input Noise	e_n	f = 1 kHz		14		nV/√Hz
Common-Mode Range	CMR			+13, −13		V
Gain Bandwidth	GBW	VCA Configuration (See Figure 18)		12		MHz
		VCP Configuration (See Figure 22)		0.7		MHz
Slew Rate	SR	VCA Configuration (See Figure 18)		10		V/μs
Supply Current	I_{SY}	No Load		11	15	mA
OUTPUT AMPLIFIERS						
Offset Voltage	V_{OOS}	V_{IN} = 0 V		−1.0	20	mV
Minimum Load Resistor	R_L	For Full Output Swing		9		kΩ
Output Voltage Swing		I_{OUT} = 1.5 mA	+10	+13.0		V
			−10	−14.0		V
CONTROL PORT						
Bias Current	I_B			0.36	1	μA
Input Impedance	Z_{IN}			1		MΩ
Gain Constant	G/(1−G)	Ratio of Outputs		−28		mV/dB
Gain Constant Temperature Coefficient	$G/(1-G)_{TC}$			−2700		ppm/°C
Control Feedthrough (Untrimmed)						
Class A		60 Hz Sine Wave Applied to Control Port, Causing −30 dB to +20 dB of Gain		−10		mV
Class AB[1]				−1		mV
Maximum Attenuation		f = 1 kHz, V_C = +4 V		100		dB

AUDIO SPECIFICATIONS[2]

Parameter	Conditions	Min	Typ	Max	Units
Noise					
Class A	R_B = 30 kΩ, BW = 20 Hz − 20 kHz, 0 dBV = 1 V rms, A_V = 0 dB		−88	−85	dBV
Class AB	R_B = 150 kΩ, BW = 20 Hz − 20 kHz, 0 dBV = 1 V rms, A_V = 0 dB		−97	−95	dBV
THD-A @ A_V = 0 dB	R_B= 30 kΩ, V_{IN} = +10 dBV @ 1 kHz		0.006	0.015	%
THD-A @ A_V = ±20 dB	R_B = 30 kΩ, V_{IN} = +10 dBV @ 1 kHz		0.009	0.025	%
THD-AB @ A_V = 0 dB	R_B = 150 kΩ, V_{IN} = +10 dBV @ 1 kHz, w/Sym Trim		0.006	0.02	%
THD-AB @ A_V = ±20 dB	R_B = 150 kΩ, V_{IN} = +10 dBV @ 1 kHz, w/Sym Trim		0.013	0.04	%

NOTES
[1]Symmetry trim only.
[2]Guaranteed specifications, based on characterization data.
Specifications subject to change without notice.

ORDERING GUIDE

Model	Operating Temperature Range	Package Option[1]
SSM-2018P	XIND[2]	16-Pin Plastic
SSM-2018S	XIND	16-Pin SOIC

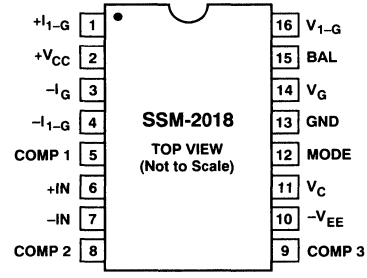
NOTES
[1]For outline information see Package Information section.
[2]XIND = −40°C to +85°C.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . ±18 V
Input Voltage . . . . . Supply Voltage
Junction Temperature . . . . . +150°C
Operating Temperature Range . . . . . −40°C to +85°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SSM-2018 PIN CONFIGURATION
16-Pin Plastic Dip—P Suffix
16-Pin SOIC—S Suffix



Typical Performance Characteristics

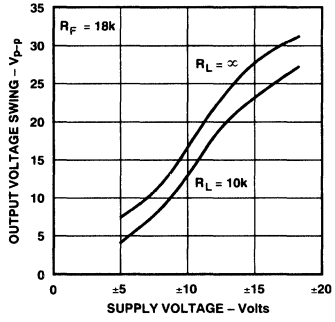


Figure 1. Maximum Output Swing vs. Supply Voltage

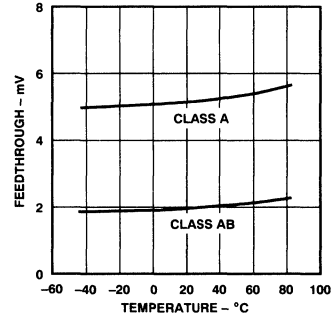


Figure 3. Trimmed Feedthrough vs. Temperature

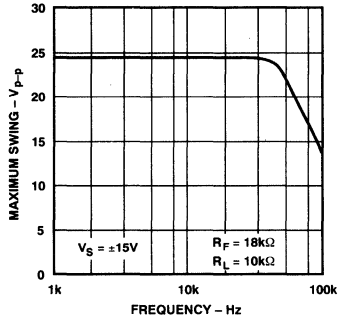


Figure 2. Maximum Output Swing vs. Frequency

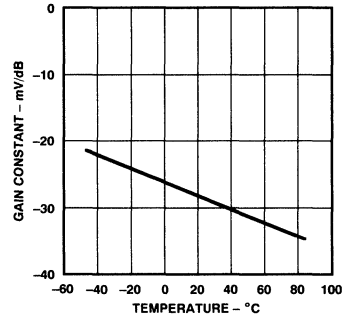


Figure 4. Gain Constant vs. Temperature

7

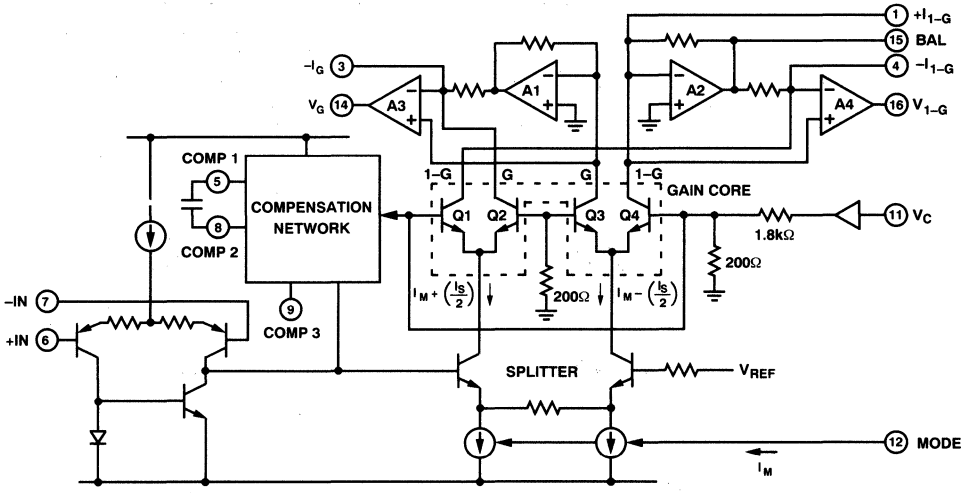


Figure 5. SSM-2018 Functional Diagram

OPERATIONAL VOLTAGE-CONTROLLED ELEMENT THEORY OF OPERATION

The operational voltage-controlled element, or OVCE, is a new analog functional building block. It combines the function of an op amp and a voltage-controlled amplifier into a single integrated device. However, because of the special circuit topology used, this design offers higher performance than would be possible with two separate circuits. The OVCE can replace any VCA in any application simply by reconfiguring the external feedback connection. Additionally, it can perform numerous circuit functions not readily achievable with conventional VCAs.

As shown in Figure 5, the OVCE consists of three basic sections, which are:

1. The input differential pair, with compensation network;
2. A programmable current splitter which generates the biasing current for the gain core;
3. The four-transistor gain core (essentially a dual two-quadrant multiplier) and the output buffers.

The differential input pair structure is the same as that used in operational amplifiers, and generates a single-ended output current corresponding to the differential input voltage. Variable-gain amplifiers face a unique problem in maintaining optimal compensation over a wide range of selected gains. In the OVCE, an adaptive network following the input section effectively divides the external compensation capacitor by a value corresponding to the current value of VCA gain. In voltage-controlled potentiometer configurations, the adaptive network is not used because the global feedback is constant with changes in gain, requiring fixed compensation only.

The current generated by the input differential pair is split to drive the gain core transistors with currents containing equal and opposite signal components. The common-mode component of these currents (I_M) determines the class of operation of the OVCE. This current corresponds to the current injected into Pin 12, which is determined by a user-selected external bias resistor. Under small-signal conditions, there is a tradeoff between I_M and the noise produced in the gain core transistors.

The gain core consists of two very carefully matched differential pairs, utilizing large-geometry, high gain transistors designed to produce minimum noise and distortion. Examining Figure 6, it can be seen that a differential pair (which is forward-biased by the current source) divides the tail current I into two currents I_{C1} and I_{C2} according to the applied voltage V_B. With the high beta of these devices, we can assume that the emitter current is equal to the collector current, expressed as $I_C = I_S \times \exp(aV_{BE})$, where I_S is the reverse saturation current. Then, since $I_{C1} + I_{C2} = I$ and $V_B = V_{BE1} - V_{BE2}$, the ratio of currents can be expressed as:

$$G = \frac{I_{C2}}{I} = \frac{exp(aV_B)}{1 + exp(aV_B)} \quad and \quad 1 - G = \frac{I_{C1}}{I} = \frac{1}{1 + exp(aV_B)}$$

These relationships are precisely reproduced in both pairs of the gain core, resulting in differential collector currents which accurately correspond to a function of the applied control voltage. The SSM-2018 is unique in providing both gain-multiplied and remainder-multiplied outputs, resulting in an infinitely flexible gain block.

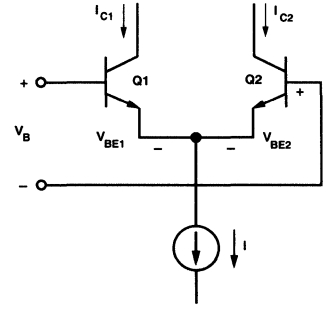


Figure 6. The OVCE Gain Core Differential Pair

The differential outputs of the gain core transistor pairs are applied to differential current-to-single ended voltage converters, composed of buffers A1 through A4 in Figure 5. Amplifiers A1 and A2 act as precision current mirrors, while A3 and A4 are current-to-voltage converters. Additionally, connections to A2 allow the user to balance the current mirror gain to achieve perfect symmetry in the positive and negative half-cycles of the output waveforms. Note that the noninverting inputs of A3 and A4 are connected to the inverting inputs of A1 and A2 respectively, thus cancelling the error contributions of the current mirror circuitry. For this reason it is recommended that in applications requiring additional output drive, external amplifiers be connected outside the feedback loops as voltage followers for best OVCE response and dynamic range.

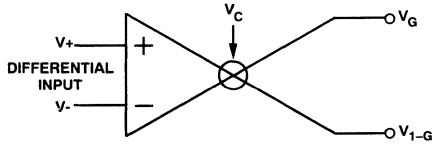


Figure 7. The OVCE Symbol

USING THE OVCE

The symbol for the OVCE is shown in Figure 7. The OVCE has two outputs, V_G and V_{1-G}. Both respond to the input, but in addition are in a ratio determined by the control port voltage, V_C, applied to Pin 11. Specifically,

$$V_G = (V(+) - V(-)) \times G \times A$$

and

$$V_{1-G} = (V(+) - V(-)) \times (1-G) \times A$$

where A is the open-loop gain of the circuit and

$$G = \frac{exp(a \times V_C)}{1 + exp(a \times V_C)}$$

As a result, the ratio of the outputs is

$$\frac{V_G}{V_{1-G}} = exp(a \times V_C)$$

The control constant a is approximately -4 at room temperature.

Application circuits are easily understood if it is assumed that the voltages at the inputs of the OVCE are equal, as is commonly done with op amps when simplifying a negative-feedback circuit with high open-loop gain. Consider the basic follower/VCA connection for the OVCE shown in Figure 8. In this example, the input signal V_{IN} drives the noninverting input, and the V_{1-G} output is tied back to the inverting input. In closed-loop operation we can simplify by saying that the inputs are approximately equal, and so the V_{1-G} output follows the input for all control inputs. However, since from above

$$V_G = V_{1-G} \times exp(a \times V_C)$$

then

$$V_G = V_{IN} \times exp(a \times V_C)$$

Therefore, this OVCE configuration provides the function of a voltage follower at the V_{1-G} output, and the function of an exponential VCA at the V_G output. The direct feedback connection between the V_{1-G} output and the inverting input could be easily replaced with any general feedback network, as is commonly done in op amp circuits.

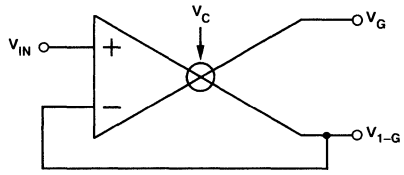
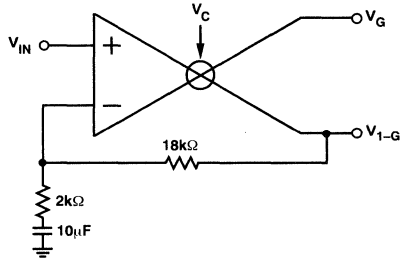
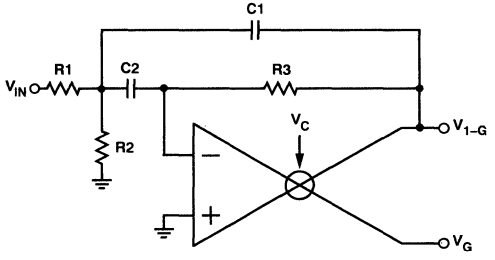


Figure 8. OVCE Follower/VCA Connection

A wide variety of transfer functions from the input to the V_{1-G} output are possible, independent of the control voltage input. At the same time, as discussed above the signal seen at the V_G output will then be equal to the transfer function times the control voltage exponential. As demonstrated in the two examples in Figure 9, this configuration provides the functions of both an operational amplifier and exponential VCA in a single device, allowing considerable flexibility in applications.



a. Voltage-Controlled Preamplifier



b. Voltage-Controlled Inverting Bandpass Filter

Figure 9. OVCE Configurations

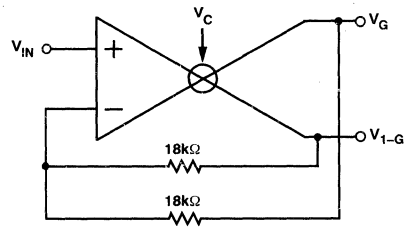


Figure 10. Basic VCP Connection

Figure 10 shows the OVCE configured with feedback applied from both outputs. Here the signal returned to the inverting input is one half of the sum of the two outputs, which must be equal to V_{IN} if we remember the approximation that the difference between the inputs is zero. The two outputs are then given by:

$$V_G = 2G \times V_{IN} \text{ and } V_{1-G} = 2(1 - G) \times V_{IN}$$

It can be seen that this provides a panning function as G ranges between 0 and 1 when V_C sweeps through its range. For instance, when $V_C = 0$, $V_G = V_{1-G} = V_{IN}$. This configuration is called a voltage-controlled potentiometer (VCP). Note that the VCP shares the quasi-exponential gain characteristics of VCAs which operate as attenuators only. An endless variety of VCA and VCP configurations are possible using the SSM-2018, in both inverting and noninverting operation. The applications discussion below demonstrates the performance of a number of circuits.

INPUT SECTION

The differential inputs are similar to those seen in an operational amplifier. The user may wish to utilize clamp diodes to avoid overdriving the input stage by high speed transients.

SETTING THE GAIN CORE CLASS OF OPERATION

The mode of operation is determined by the user by programming the gain core bias current with resistor R_B. The positive supply can be used to provide a current into Pin 12, which must be between 90 μA and 500 μA for proper operation. The suggested value for the set resistor R_B is 30 kΩ for Class A operation and 150 kΩ for Class AB. Without this current input, the output signal will appear half-wave rectified. In earlier designs, Class AB operation has always been preferred for lower noise operation, while Class A was the choice where distortion performance was the greater concern. However, as the distortion graphs below demonstrate, the SSM-2018 offers Class AB performance rivaling that of Class A. Most applications, except those demanding the lowest possible distortion performance, will bias the gain core as Class AB. Note that control feedthrough in the SSM-2018 will be significantly lower in Class AB operation. Alternatively, Intermediate Class operation offers an excellent compromise between the low noise of Class AB and the superior distortion of Class A.

CONTROL SECTION

The sensitivity of the control port is −28 mV/dB at the input (Pin 11). A resistive divider is commonly used to scale the control voltage source range. Since this input can draw as much as 250 nA of bias current, it is recommended that the impedance of the divider to ground be kept under 10 kΩ to minimize gain error. The user should take care to avoid coupling stray signals and ground errors into the control pin, which will directly affect the performance of the device. As shown in the application examples, a 1 μF capacitor is recommended, located near the pin. Noisy environments may require that this value be increased to 10 μF.

Due to temperature effects on the gain core transistors, the control port has a −2700 ppm/°C temperature coefficient which can be compensated with a single +2700 ppm/°C tempsistor (RCD Components, Inc., Manchester, NH, (605) 669-0054) in the control voltage divider chain.

COMPENSATION

In the VCA configuration, the SSM-2018 utilizes a unique adaptive compensation network to maximize the internal closed-loop gain of the device independent of overall system gain. As shown in the application circuits, a compensation capacitor is connected between Pins 5 and 8, and Pin 9 is unconnected. In VCP circuits, the feedback of the system is constant with gain and the adaptive circuit is defeated by connecting Pin 9 to ground. In circuits requiring moderate gain, the value of the compensation capacitor can be reduced in order to obtain wider signal bandwidth.

OUTPUT SECTION

The SSM-2018 has two voltage outputs, and three current outputs which can deliver a minimum of 750 μA when operating from ±15 V supplies. Feedback resistors for the internal or external op amps which convert the currents to a desired voltage should be greater than 17 kΩ with ±15 V supplies. As shown in the functional diagram, the current outputs are virtual grounds in normal operation. Amplifiers A1 and A2 act as current mirrors which maintain the $+I_{1-G}$ potential to ground. A3 and A4 are current-to-voltage converters which keep the outputs $-I_G$ and $-I_{1-G}$ at ground potential, with current outputs capable of sinking greater than 10 mA and sourcing a minimum of 1.65 mA.

TRIMMING THE SSM-2018

The network recommended for correcting waveform symmetry and trimming offset is shown in Figure 11. Both trims affect offset and control feedthrough. The symmetry trim also controls distortion performance and is mandatory for Class AB operation, but may not be necessary in less critical applications operating in Class A. The offset trim is appropriate in those situations requiring improved control feedthrough.

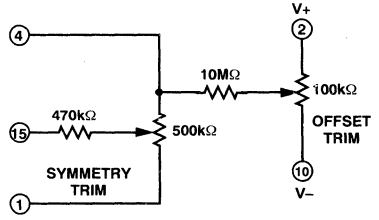


Figure 11. Symmetry and Offset Trim Network

TRIM PROCEDURE

Symmetry Trim

If the symmetry trim is to be performed, it should precede the offset adjustment.

1. Apply a 1 kHz sine wave of +10 dBV to the input, with the control voltage set at unity gain.
2. Adjust the symmetry trim potentiometer to minimize distortion of the output signal.

Offset Trim (Optional)

The offset trim corrects for control feedthrough error.

1. Ground the input signal and apply a 60 Hz sine wave to the control port. The sine wave should have its high and low peaks correspond to the highest gain to be used in the application and 30 dB attenuation, respectively. For example, a range of +20 dB maximum gain and 30 dB attenuation requires that a sine wave swinging between −560 mV and +840 mV be applied to Pin 11.
2. Adjust the offset trim potentiometer to null the control feedthrough seen at the output.

The incorporation of dc blocking capacitors at the inputs will prevent offsets from previous stages from affecting the performance of the SSM-2018. Many applications, such as panning and equalizer circuits, will not require the offset trim. The control settings for these circuits are usually established at setup and changed infrequently. Audible control feedthrough can be suppressed by inserting a time constant of 10–20 ms in the control signal path.

APPLICATIONS INFORMATION

Circuits which illustrate four basic applications of the SSM-2018 are included below, accompanied by graphs demonstrating the observed performance. Armed with a basic understanding of the OVCE structure, the user can easily modify these circuits for his particular needs and realize additional functions such as voltage-controlled preamplifiers, compressors/limiters, and many other functions. Data taken on the Audio Precision System One utilizes the internal 30 kHz noise filter, with an input signal of +10 dBV.

THE BASIC OVCE

The basic configuration for the OVCE with differential inputs discussed in Figure 7 is demonstrated in Figure 12, which includes the recommended offset and symmetry trim circuitry. Note that the feedback for the output amplifiers includes a minimum 5 pF capacitor for high frequency cutoff and noise limiting, and that the 1:4 control voltage divider is accompanied by 1 μF, to avoid control errors due to noise. The observed performance of this circuit is illustrated in Figures 13 through 17.

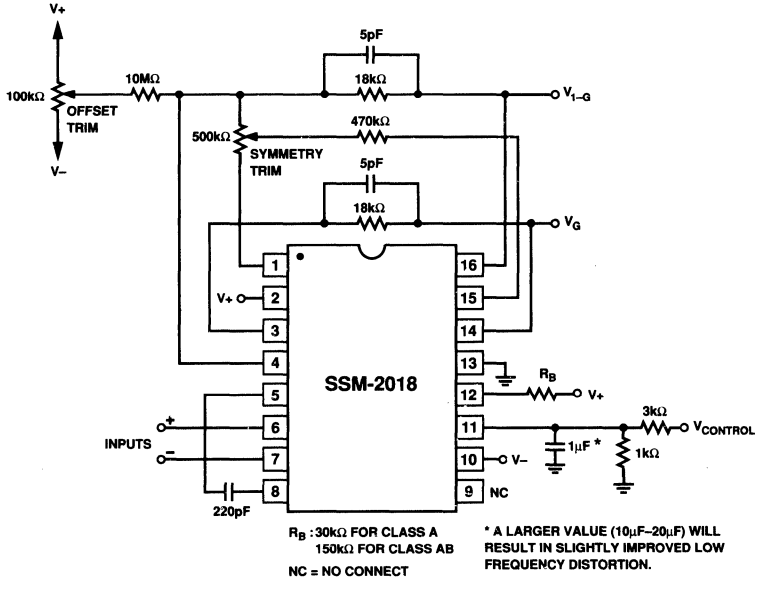


Figure 12. OVCE Application Circuit

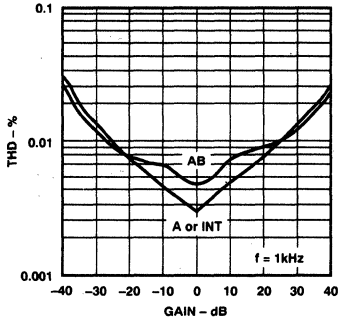


Figure 13. OVCE THD vs. Gain

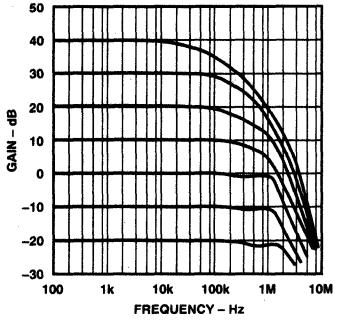


Figure 14. OVCE Bandwidth vs. Gain

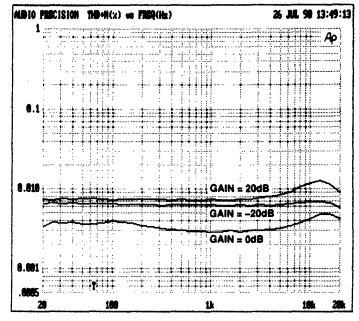


Figure 15. OVCE THD+N vs. Frequency, Class A Operation

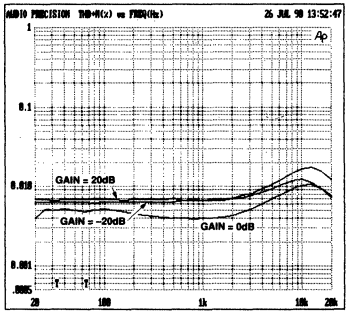


Figure 16. OVCE THD+N vs. Frequency, Class AB Operation

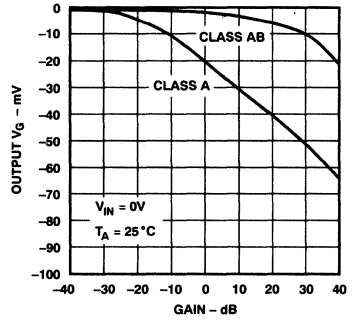


Figure 17. OVCE Output vs. Gain

USING THE OVCE TO BUILD A SIMPLE VCA

This circuit demonstrates the flexibility of the SSM-2018 by using differential current feedback to realize a complete, minimum parts count voltage-controlled amplifier with differential or single-ended inputs. Amplifier A4 is defeated to allow current feedback to the OVCE input and enhance the frequency response and slew rate. See Figure 18. Feedback from the $+I_{1-G}$ output to the inverting input and from $-I_{1-G}$ to the noninverting input creates differential virtual ground inputs. Single-ended operation allows inverting or noninverting gain, with the unused input unconnected. The output from amplifier A3 is available at Pin 14. A capacitor of any value can be connected across buffer A3 (Pin 3 to Pin 14) to band-limit the output signal as desired. Refer to Figures 19 through 21 for the typical performance obtained with this implementation.

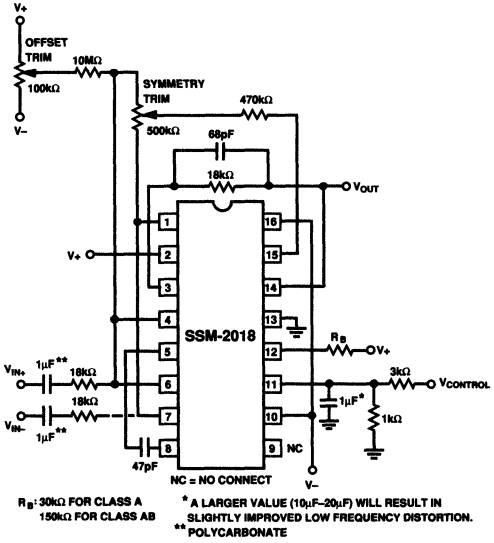


Figure 18. Simple VCA Application Circuit

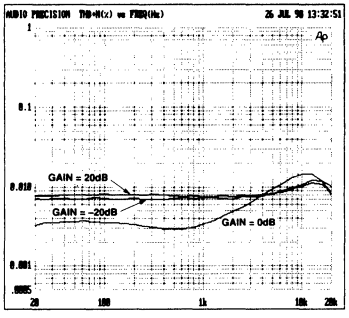


Figure 19. VCA THD+N vs. Frequency, Class A Operation

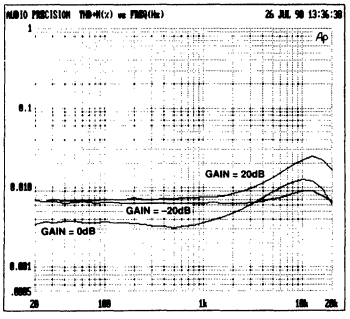


Figure 20. VCA THD+N vs. Frequency, Class AB Operation

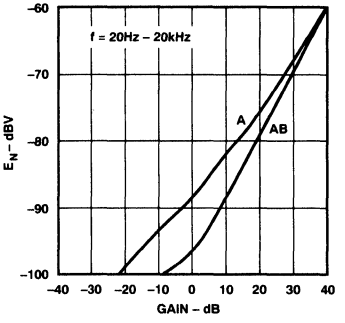


Figure 21. VCA/OVCE Noise vs. Gain

A VOLTAGE-CONTROLLED PANNER

The ratiometric outputs of the SSM-2018 allow the user to realize an excellent potentiometer with minimal external components, as shown in Figure 22. As first shown in Figure 10, the outputs are summed and fed back to the noninverting input to perform the basic panning function. Figures 23 through 29 demonstrate the performance observed with this configuration.

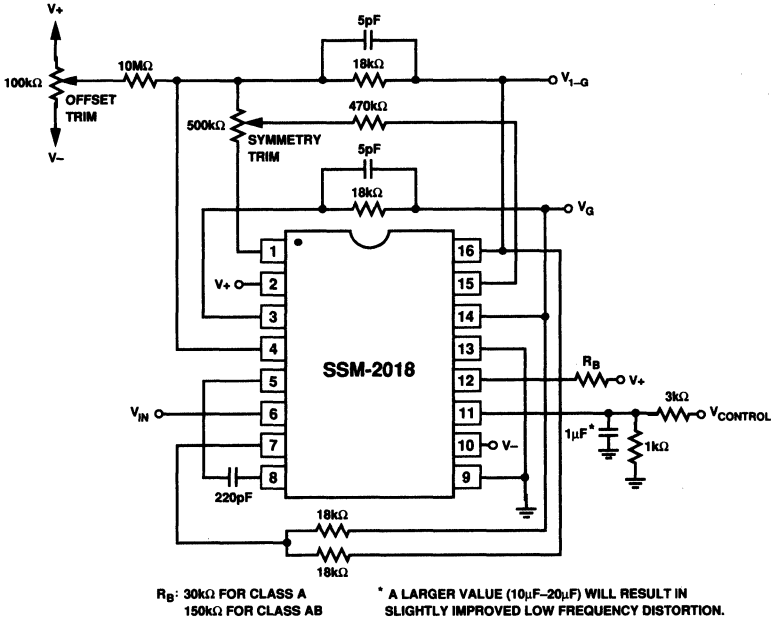


Figure 22. VCP Application Circuit

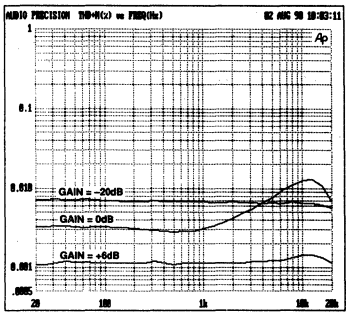


Figure 23. VCP THD+N vs. Frequency, Class A Operation

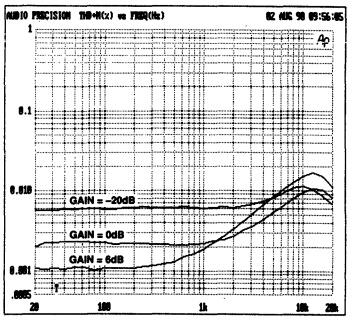


Figure 24. VCP THD+N vs. Frequency, Class AB Operation

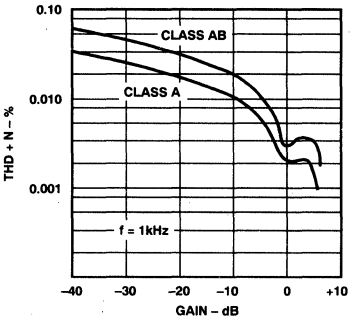


Figure 25. VCP THD+N vs. Gain

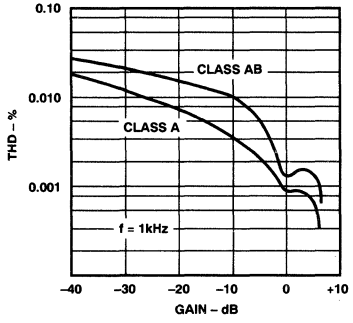


Figure 26. VCP THD vs. Gain

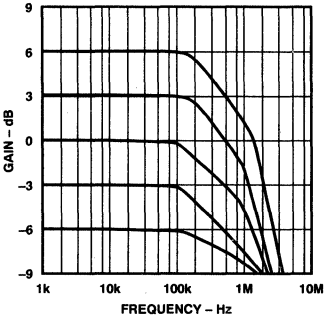


Figure 27. VCP Bandwidth vs. Gain, Class A Operation

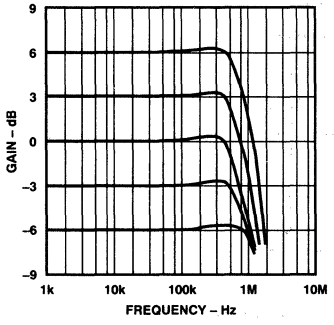


Figure 28. VCP Bandwidth vs. Gain, Class AB Operation

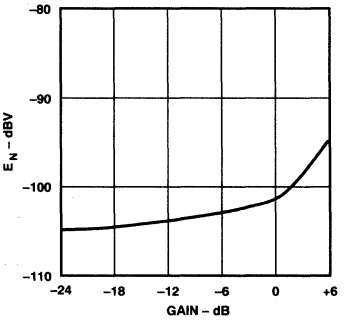


Figure 29. VCP Noise vs. Gain, Class AB Operation

A HIGH QUALITY VOLTAGE-CONTROLLED EQUALIZER USING THE SSM-2018

Figure 30 shows the SSM-2018 in the VCEQ configuration, utilizing a simple RC high pass filter network to generate a basic reciprocal high frequency equalizer with excellent noise and distortion characteristics. The noise and gain performance obtained with this circuit is shown in Figures 31 through 34. The user is free to replace the filter network in order to obtain the desired gain characteristics. Any other noninverting filter, including low-pass or bandpass functions, will yield a voltage-controlled equalizer with the form of the filter transfer function. The addition of voltage control to the equalization function creates an extremely attractive alternative.

UPGRADING SSM-2014 SOCKETS WITH THE SSM-2018

The SSM-2018 is a drop-in replacement for the SSM-2014, offering noticeable performance improvements with minor changes in the original circuitry. The SSM-2014 requires external compensation to assure optimal performance, including RC networks on Pins 1, 3, and 4, and a capacitor on Pin 9. These components are not necessary when using the SSM-2018, and should be removed in order to realize the full performance of the device. For best results, the SSM-2018 should not be evaluated in an SSM-2014 evaluation board. An SSM-2018 evaluation board is available through your local sales office.

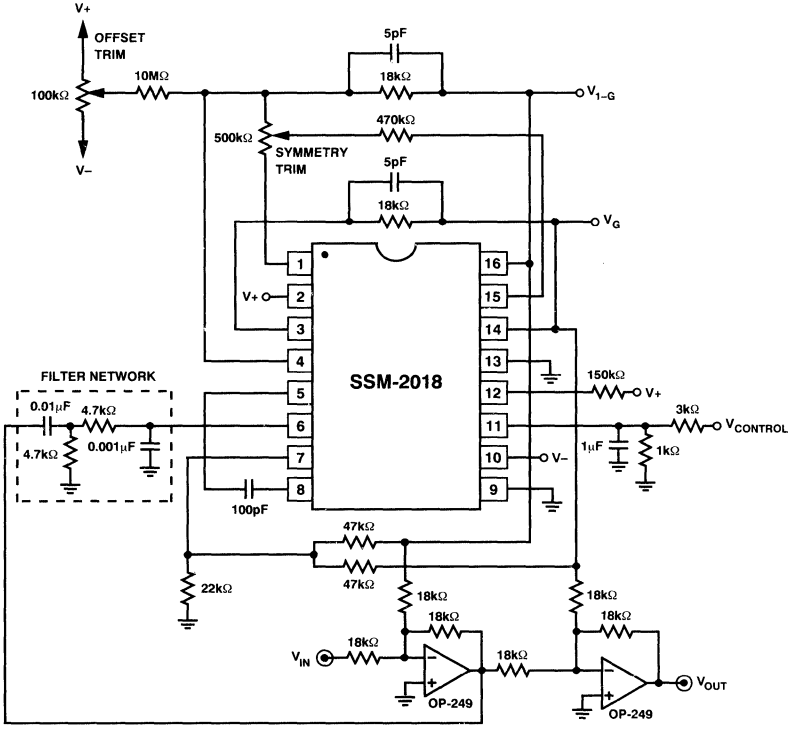


Figure 30. Voltage Controlled Equalizer Application Circuit

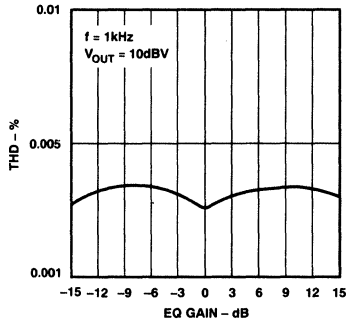


Figure 31. Equalizer THD+N vs. Gain

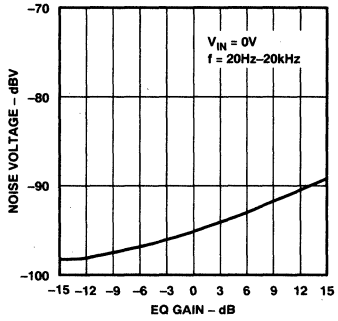


Figure 32. Equalizer Noise vs. Gain

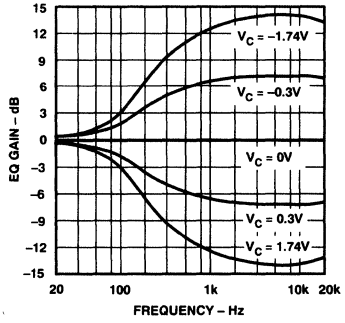


Figure 33. Equalizer Frequency Response vs. Gain

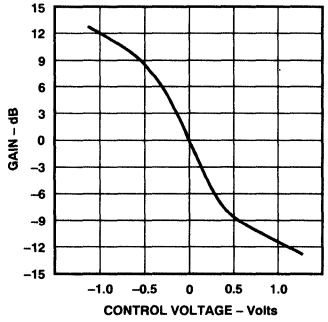


Figure 34. Equalizer Gain vs. Control Voltage

ANALOG DEVICES

Quad Current-Controlled Amplifier

SSM-2024

FEATURES

- **Four VCAs in One Package**
- **Ground Referenced Current Control Inputs**
- **82dB S/N at 0.3 % THD**
- **Full Class A Operation**
- **–40dB Control Feedthrough (Untrimmed)**
- **Easy Signal Summing**
- **6% Gain Matching**

APPLICATIONS

- **Electronic Musical Instruments**
- **Noise Gating**
- **Compressor/Limiters**
- **Signal Mixing**
- **Automatic Gain Control**
- **Voltage-Controlled Oscillators**

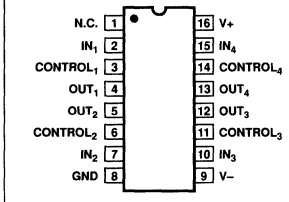
ORDERING INFORMATION

PACKAGE	OPERATING TEMPERATURE RANGE
PLASTIC 16-PIN	
SSM2024P	–10°C to +50°C

GENERAL DESCRIPTION

The SSM-2024 is a quad Class A noninverting current-controlled transconductance amplifier. Each of the four VCAs is completely independent and includes a ground referenced linear current gain control. These voltage-in/current-out amplifiers offer over 82dB S/N at 0.3% THD. Other features include low control voltage feedthrough and minimal external components for most applications. With four matched VCAs in a single IC, the SSM-2024 provides a convenient solution for applications requiring multiple amplifiers. The pinout groups the four outputs for easy signal summing for circuits such as four-channel mixers.

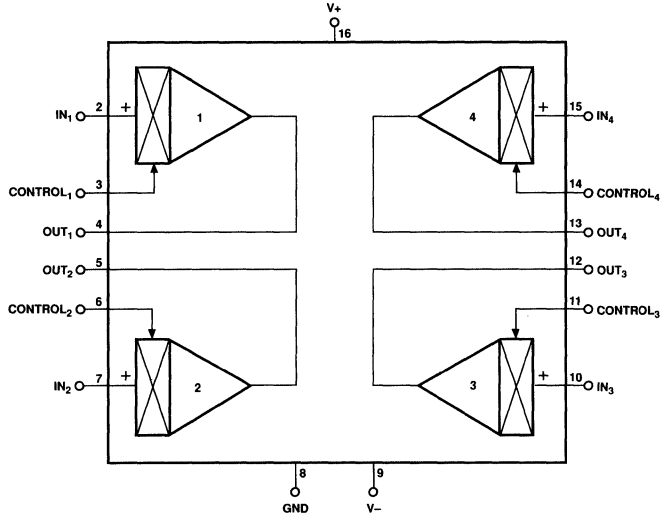
PIN CONNECTIONS



16-PIN PLASTIC DIP (P-Suffix)

7

BLOCK DIAGRAM



The SSM-2024 is mask work protected under the Semiconductor Chip Protection Act of 1983.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... 36V or ±18V
Junction Temperature ..... +150°C
Operating Temperature Range ..... –10 to +50°C
Storage Temperature Range ..... –65 to +150°C
Maximum Current into Any Pin 10mA
Lead Temperature Range (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
14-Pin Plastic DIP (P)	90	47	°C/W

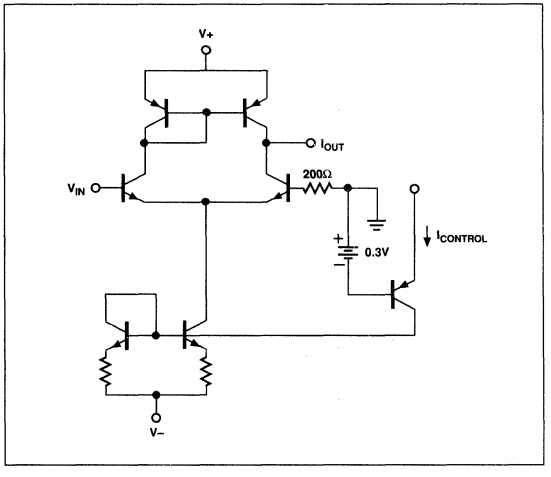
NOTES:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

			SSM-2024			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Positive Supply Current	$+I_{SY}$	I_{CON} (1-4) = 0 V_S = ±15V I_{CON} (1-4) = 0 V_S = ±16.5V	0.95 1.05	1.40 1.55	1.85 2.05	mA
Negative Supply Current	$-I_{SY}$	I_{CON} (1-4) = 0 V_S = ±15V I_{CON} (1-4) = 0 V_S = ±16.5V	1.05 1.20	1.55 1.65	2.05 2.25	mA
Gain	G	I_{CON} (1-4) = ±500µA	3842	4085	4330	µmhos
Gain Matching	ΔG	I_{CON} (1-4) = ±500µA	–	–	±6	%
Input Offset Voltage	V_{OS}	V_{IN} = 0V I_{CON} (1-4) = ±500µA I_{CON} (1-4) = +250µA	–	±.4	±1.3	mV
Change in Offset Voltage	ΔV_{OS}	+2.5µA ≤ I_{CON} (1-4) ≤ +250µA +250nA ≤ I_{CON} (1-4) ≤ +250µA	– –	±100 ±250	±840 ±840	µV
Output Leakage	I_{OL}	I_{CON} (1-4) = 0	–	0.1	±5	nA
Control Rejection (Untrimmed)	CVR	I_{CON} (1-4) = 500µA V_{IN} (1-4) = 40mV_{p-p}	30	41.5	–	dB
Signal-to-Noise	S/N	V_{IN} (1-4) = 40mV_{p-p}	–	82	–	dB
Distortion	THD	V_{IN} (1-4) = 40mV_{p-p}	–	0.3	–	%
Threshold Input Control Voltage	V_{TCI}	I_{OUT} (1-4) = 0	+160	–	+220	mV

NOTE: Specifications subject to change; consult latest data sheet.

SIMPLIFIED SCHEMATIC (1 OF 4 AMPLIFIERS)



THEORY OF OPERATION

The SSM-2024 is a quad transconductance amplifier. Its voltage-in/current-out transfer functions are controlled by ground referenced linear current inputs. As shown in the simplified schematic, the control current is mirrored in the input stage current source. This sets the operating level for the input differential pair. The operating level established by $I_{CONTROL}$ will determine the slope of the I_{OUT}/V_{IN} transfer characteristic. Each independent device is configured as a noninverting transconductance amplifier and rated for ±15V operation.

SIGNAL INPUTS

The signal inputs offer the best offset and control rejection when shunted with 200Ω to ground. This resistor along with R_{IN} form the voltage divider to scale the input signal. Select R_{IN} to set the maximum operating level for the largest input signal.

This selection will determine the VCAs operating levels which have tradeoffs as shown in Figures 1 and 2. As the input signal level is increased, the effective signal-to-noise and control rejection will increase (improve). However, a larger input signal also means more THD.

The signal at the input of the device will be:

$$V_{IN}' = V_{IN}\left(\frac{200}{R_{IN} + 200}\right)$$

(where V_{IN} is the **applied** input). The circuit transconductance I_{OUT}/V_{IN}' is:

$$g_m = 8.17\ I_{CONTROL} = \frac{I_{OUT}}{V_{IN}'}$$

Therefore, the output current expressed as a function of the control current and the applied input signal is:

$$I_{OUT} = 8.17\ I_{CONTROL}\left(\frac{200}{R_{IN} + 200}\right)V_{IN}$$

A graph of some typical operating levels is shown in Figure 3. Note this plot is for a general application where

$R_{IN} = R_{CONTROL} = 10k\Omega$

For output voltage vs. V_{IN} see the right axes of the graph using

$R_{OUT} = 10k\Omega$.

CONTROL INPUTS

Each control input is a low impedance, ground referenced linear current control input. When operated in its active region, input impedance is approximately 250Ω. When operating with an applied control voltage, connect a series resistor. Select R_{CON} so $V_{CONTROL}$ max/R_{CON} is no more than 500μA.

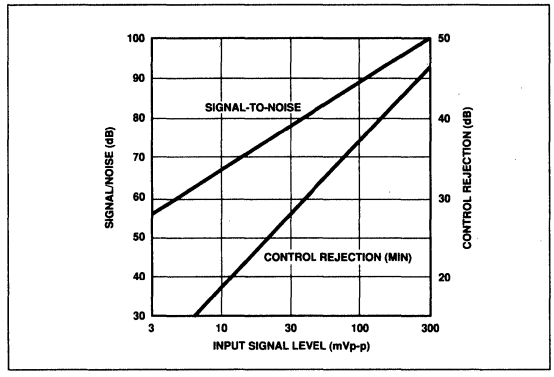


FIGURE 1: Text for figures is italic, normal

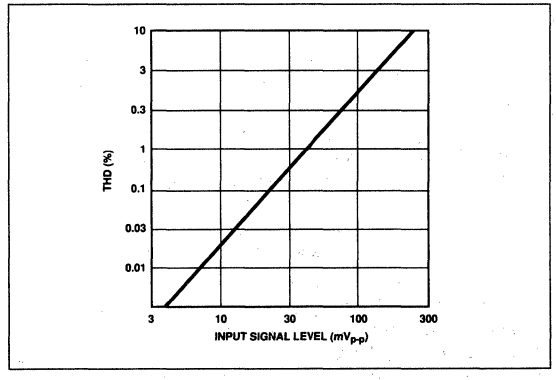


FIGURE 2

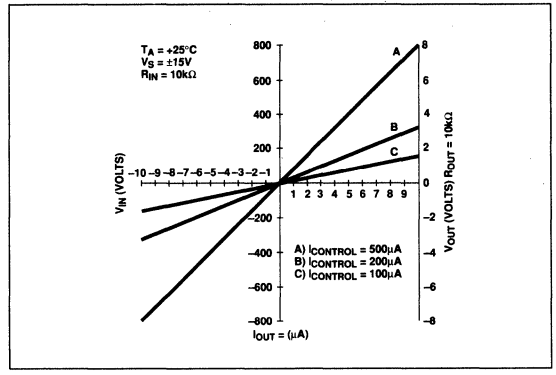


FIGURE 3: *SSM-2024 $g_m = I_{OUT}/V_{IN}$*

7

The VCA will turn completely off as the control voltage drops below approximately 200mV. The control pin can go as low as V– with no adverse effects. Control voltages usually do not exceed 10V. It is possible to operate at higher voltages with current limiting. If the control pin is shorted directly to V+, however, the power dissipation rating of the package will be exceeded within 10 to 20 seconds.

OUTPUTS

The SSM-2024 is a current output device. Operating in the current mode as virtual grounds, the outputs have a voltage compliance of only about 500mV. For large output voltages an op amp is used as a current-to-voltage converter as shown in Figure 4. Selecting R_{OUT} will determine the output voltage range as

$$V_{OUT} = I_{OUT} (R_{OUT}).$$

The outputs can be used directly in many applications where voltage ranges are small, such as the exponential input of a voltage-controlled filter or other logarithmic-control voltage devices.

Outputs are conveniently located together at the center of the package for easy connections in signal summing applications.

DISTORTION

As shown in Figure 2, operation at higher signal levels will increase THD (Total Harmonic Distortion). For many applications such as control paths where a single input signal is being processed, distortion effects are minimal. This is because distortion only slightly alters the harmonic structure of a saw, pulse or triangle shaped waveform already rich in harmonics.

In the final VCA, however, where two or more signals are present, the effects of IMD (Intermodulation Distortion) become more significant. Intermodulation distortion is unwanted sideband signals produced by the circuit at frequencies that are the sums and differences of the harmonics present at the inputs.

In a Class A VCA, IMD will increase with increasing input signal level at the same rate as THD. For such applications, we recommend use of the SSM-2024 at signal levels corresponding to THD of no more than 0.3% (see Figure 2).

APPLICATIONS

The following examples were developed for musical instrument applications but also illustrate general methods of use. Applications for the SSM-2024 are numerous in programmable music systems. A waveform mixer following tone sources is shown in Figure 4. This type of mixer can be configured in several ways to allow the various waveforms and tone sources to be mixed under program control. Choice of mixer configurations depends on system philosophy and the number of tone and noise sources to be considered.

The SSM-2024 can also be used as the final VCA/volume and filter controls. This would make keyboard tracking and envelope sweep programmable.

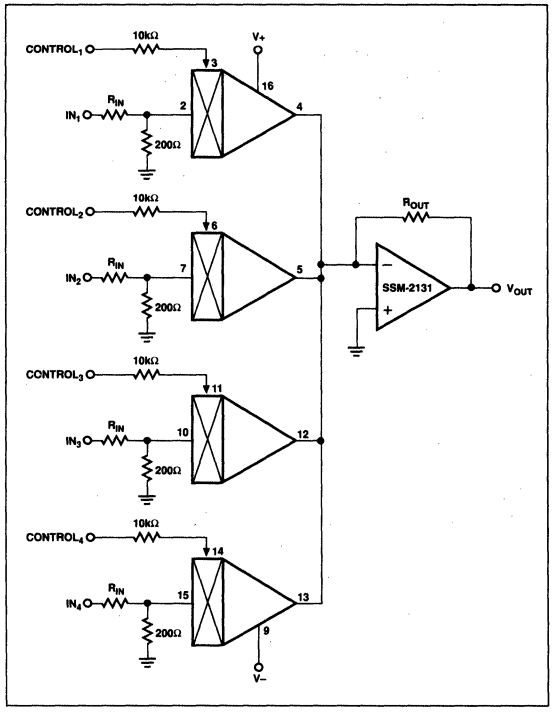


FIGURE 4: *Four-Channel Mixer (4–1)*

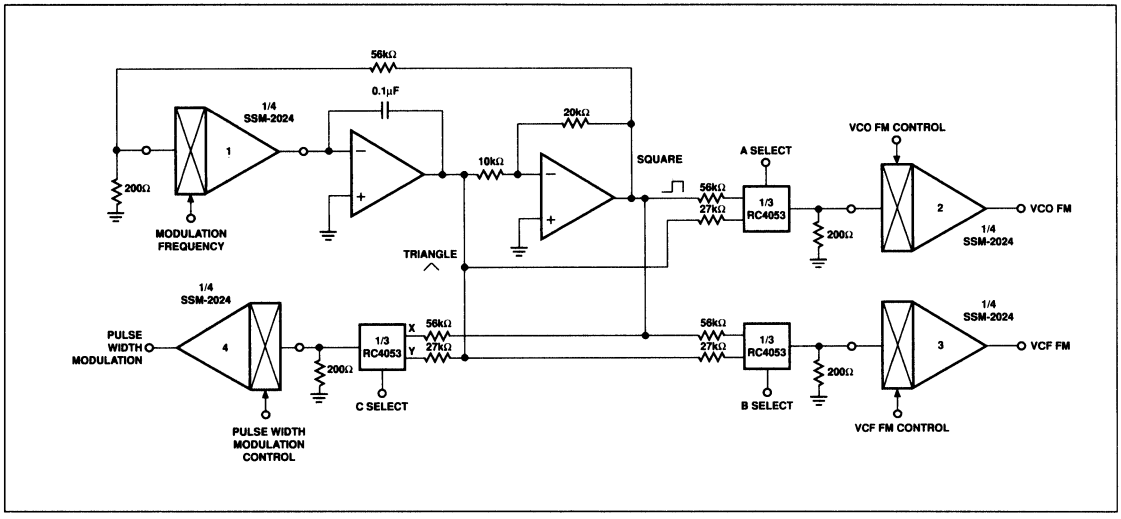


FIGURE 5: *Modulation Oscillator*

A practical modulation oscillator is shown in Figure 5. Here, the device is used in the circuit to control the oscillator frequency and the amount of modulation signal onto the modulation buses.

A VCA with programmable amplitude modulation control is shown in Figure 6. This circuit also exhibits direct interface to the SSM-2044 VCF without adding an op amp or offset adjustments.

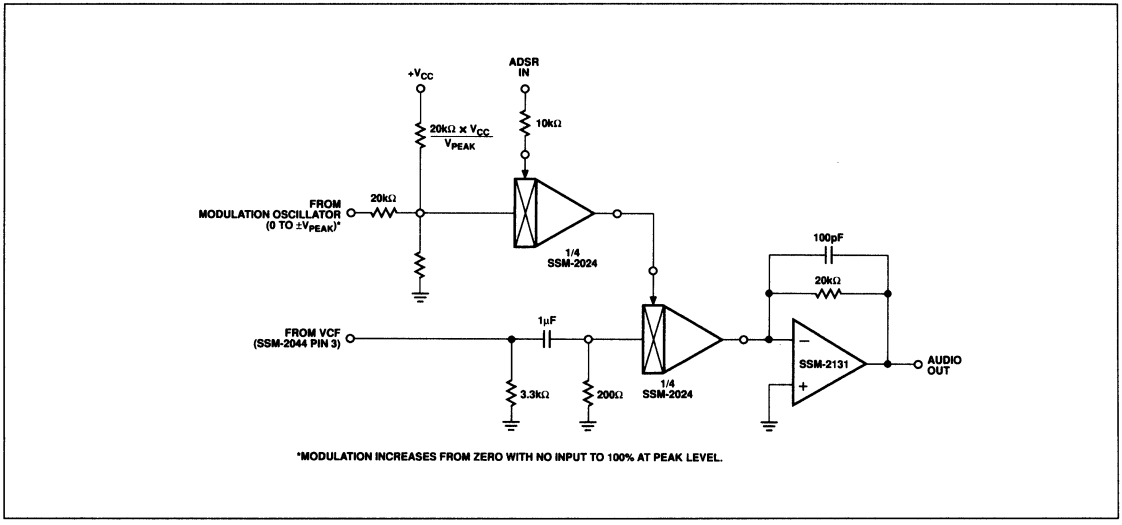


FIGURE 6: *VCA with Amplitude Modulation*

Two of the SSM-2024 channels can be used with the SSM-2220 dual PNP transistor in an exponential cross-fade circuit. Figure 7 shows how the PNP splits a common linear control current according to the bias of the PNP pair. Here, the voltage called "exponential cross-fade control" will determine the relative amount of the two signals at the inputs of the VCAs in the mix.

The transfer characteristic of this circuit is shown in Figure 8. This plot is normalized to the balance point where each VCA has equal current (250µA). This is plotted as the 0dB or unity-gain point. As the control voltage is swept positive or negative, the control current in each VCA is varied logarithmically. As the control voltage is increased, VCA B receives increased current as VCA A's current attenuates at a more rapid logarithmic rate. This applies inversely for decreasing control voltages. At the maximum positive or negative control voltages, VCA B or VCA A receives virtually all 500µA and is 6dB above the balance point.

To operate a single VCA with exponential control sensitivity, simply ground the collector of the unused PNP.

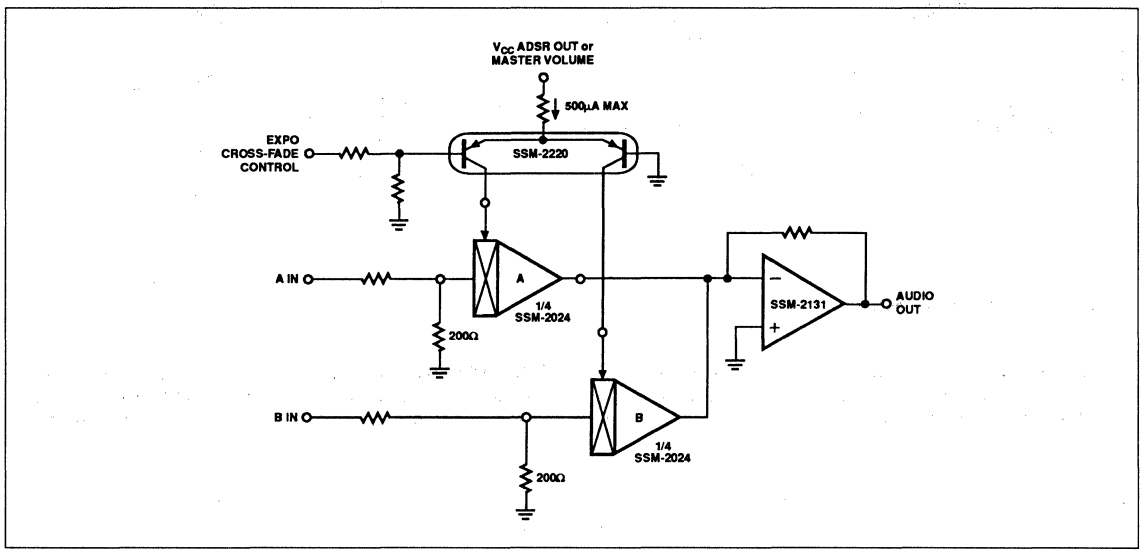


FIGURE 7: *Exponential Cross-Fade Controller*

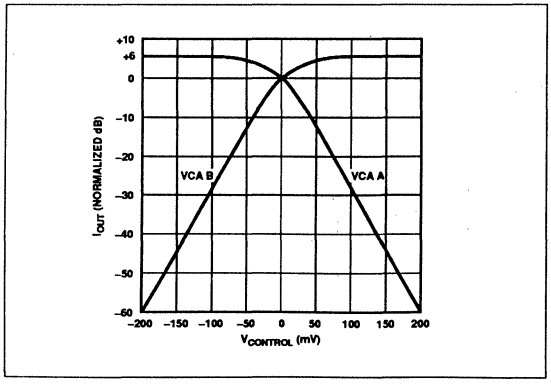


FIGURE 8: *Normalized Transfer Characteristic of a Exponential Cross-Fade Controller*

True RMS-to-DC Converter

SSM-2110

FEATURES

- **Multiple Output Options (Absolute Value, RMS, Log RMS, Log Absolute Value, Average Absolute Value)**
- **Wide Dynamic Range 100dB**
- **Prebias Option for Fast Response at Low Signal Levels**
- **On-Chip Log Output Amplifier**
- **Optional Internal Log Output Temperature Compensation**
- **Low Drift Internal Voltage Reference**
- **Low Cost**

APPLICATIONS

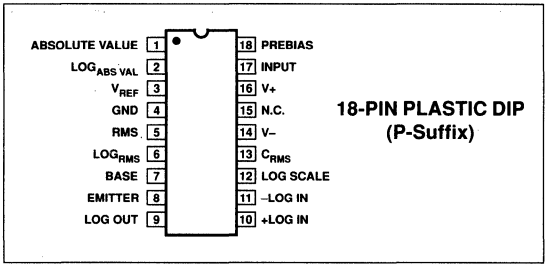
- **Audio Dynamic Range Processors**
- **Audio Metering Systems**
- **Digital Multimeters**
- **Noise Testers**
- **Panel Meters**
- **Power Meters**
- **Process Control Systems**

GENERAL DESCRIPTION

The SSM-2110 is a true RMS-to-DC converter designed to provide multiple linear and logarithmic output options. The linear outputs, true RMS and absolute value, can be obtained simultaneously with the absolute value output configurable to give a peak function. The logarithmic outputs can provide log RMS, log absolute value or log average absolute value. Full on-chip temperature compensation is available for each output option.

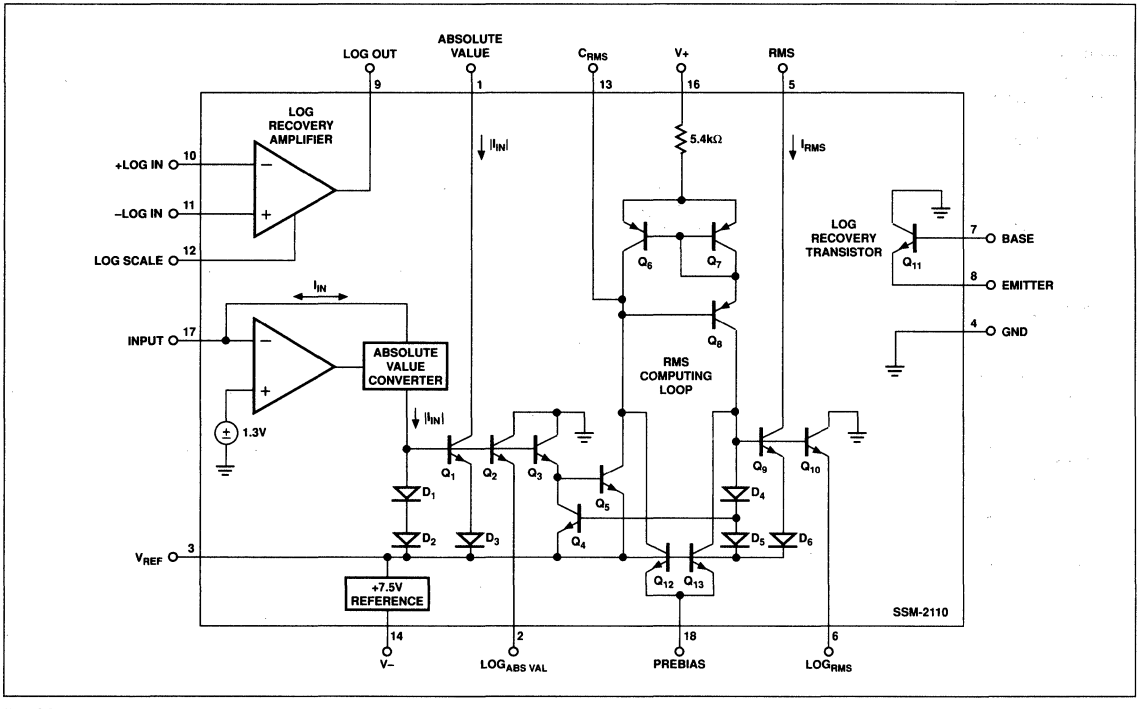
Continued

PIN CONNECTIONS



18-PIN PLASTIC DIP (P-Suffix)

FUNCTIONAL DIAGRAM



The SSM-2110 has been granted mask work protection under the Semiconductor Chip Protection Act of 1983.

GENERAL DESCRIPTION *Continued*

The SSM-2110 has a dynamic range of 100dB. A unique on-chip prebias circuit enables the users to trade dynamic range at low signal levels for a faster response time. As a precision level detector, the SSM-2110 has applications in digital multimeters, panel meters, process control and audio systems.

ORDERING INFORMATION

PACKAGE	OPERATING TEMPERATURE RANGE
PLASTIC 18-PIN	
SSM2110P	–25°C to +75°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature Range
(Soldering, 60 sec) ..... +300°C
Junction Temperature ..... +150°C
Operating Temperature Range ..... –25°C to +75°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
18-Pin Plastic DIP (P)	75	33	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$ and $R_{SCALE} = 4.7k\Omega$, unless otherwise noted.

			SSM-2110			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Dynamic Range	DR	$30nA_{p-p} \le I_{INp-p} \le 3mA_{p-p}$	100	110	–	dB
Unadjusted Gain		$I_{IN} = \pm 1mA$	0.95	1.0	1.05	
Error (Mean or RMS)			–	–	±0.5	dB
Output Offset Current	I_{OOS}	$I_{IN} = \pm 1mA$	–	5	15	nA
I_{OS} Shift	ΔI_{OOS}	$R_{PREBIAS} = 3M\Omega$	–	50	120	nA
Crest Factor @ $1mA_{RMS}$	CF	For 0.1dB Additional Error	–	2.5	–	
		For 0.5dB Additional Error	–	5	–	
		For 1.0dB Additional Error	–	8	–	
RMS Filter Time Constant	t_{CON}	$I_{RMS} > 10\mu A_{RMS}$		$11k\Omega \times C_{INT}$		
Frequency Response (Sine Wave)						
For 0.1dB Additional Error		$I_{IN} > 1mA_{RMS}$	–	400	–	
		$I_{IN} > 10\mu A_{RMS}$	–	10	–	
		$I_{IN} > 1\mu A_{RMS}$	–	2	–	
For 0.5dB Additional Error	BW	$I_{IN} > 1mA_{RMS}$	–	1000	–	kHz
		$I_{IN} > 10\mu A_{RMS}$	–	50	–	
		$I_{IN} > 1\mu A_{RMS}$	–	7.5	–	
–3dB Bandwidth		$I_{IN} > 1mA_{RMS}$	–	1500	–	
		$I_{IN} > 10\mu A_{RMS}$	–	300	–	
		$I_{IN} > 1\mu A_{RMS}$	–	50	–	
Log Amp Output Offset Current (Pin 9)	$I_{OOS-LOG}$		–	±3.3	±13	µA
Max Log Amp Output (Pin 9)	$I_{OUT-LOG}$		±250	±265	±288	µA
Log Scale Factor (Pin 2 or Pin 6)			–	+6	–	mV/dB
Log Mode Zero Crossing (Mean or RMS, Pin 9)		RMS In To Get Zero Out (See Figure 7)	–	10	–	µA
Log Amp Linearity (Pin 9)		$-240mV < V_{PIN\ 10} - V_{PIN\ 11} < +240mV$	–	0.1	0.25	dB
Log Output Tempco	T_C	$0°C < T_A < +70°C$	–	±75	–	ppm/°C
V_{REF} (Pin 3 to V–)			6.7	7.5	7.8	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$ and $R_{SCALE} = 4.7k\Omega$, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	SSM-2110 MIN	SSM-2110 TYP	SSM-2110 MAX	UNITS
Positive Supply Current	I_S+	$I_{IN} = 0$	480	–	920	µA
Negative Supply Current	I_S-		2.1	–	3.3	mA
Supply Voltage Range	V_S		±12	–	±18	V

Specifications subject to change; consult latest data sheet.

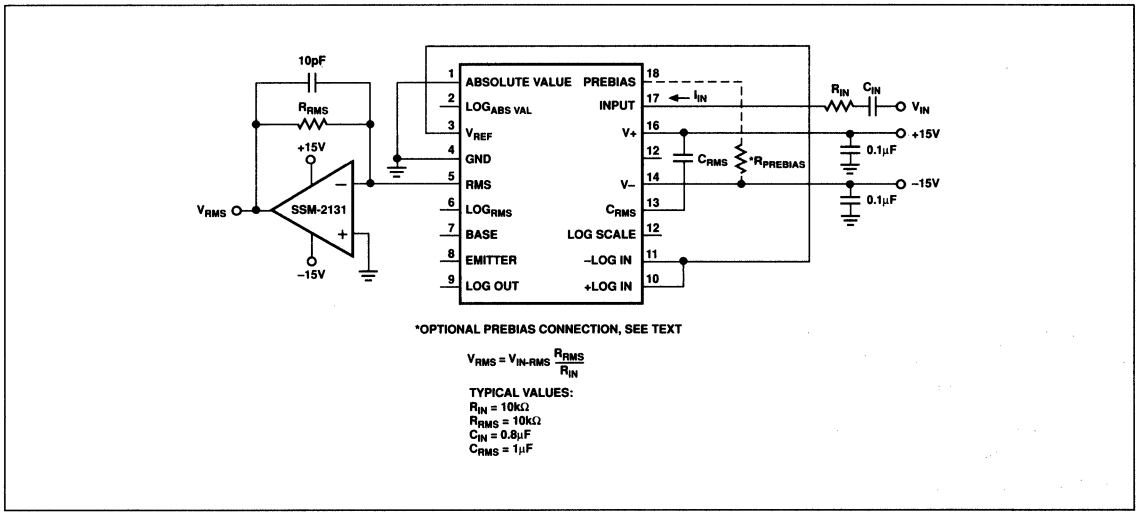


FIGURE 1: *RMS Output Circuit*

THE RMS COMPUTING LOOP

The RMS section of the SSM-2110 consists of an implicit RMS computing loop whose output follows the equation:

$$I_O = \frac{I_{IN}^2}{\overline{I_O}}$$

where $\overline{I_O}$ is the average of I_O

The time constant for averaging is determined by the value of the averaging cap C_{RMS} (on pin 13) and an internal resistor whose effective value is 10.8kΩ. A very low leakage capacitor must be used for C_{RMS} to prevent limiting the dynamic range.

Increasing the value of C_{RMS} will result in lower levels of ripple on the RMS Output at the expense of an increase in settling time for a step change in the input signal amplitude. This is a proportional relationship where increasing the value of C_{RMS} tenfold results in a tenfold increase in the settling time.

For the circuit in Figure 1, the peak-to-peak ripple approximately follows the equation:

$$V_{RIPPLE(p-p)} = \frac{2\sqrt{2} \times V_{RMS}}{4\pi f R_{INT} C_{RMS}} \times \frac{R_{RMS}}{R_{IN}}$$

where $R_{INT} \approx 10.8k\Omega$

The settling time of the SSM-2110 also depends on the frequency of the signal being processed. It takes approximately 100ms for a 300µA p-p, 50Hz signal to settle within 0.1% when $C_{RMS} = 1\mu F$, and it takes 10ms for a 500Hz signal to settle within the same value. The general rule is a tenfold increase in frequency causes a tenfold reduction in settling time. The settling time also varies with the amplitude of the signal. The larger the signal level the faster the settling time.

INPUT

The INPUT (pin 17) is an AC virtual ground with approximately +1.3V DC offset voltage. The useful dynamic range of input current the device can process is 100dB (3mA$_{p-p}$ to 30nA$_{p-p}$). The input RC network is usually chosen to allow close to 20dB of headroom in order to process high crest factor signals and provide a DC block below a given frequency band. Since in every case the ratio of R_{OUT} (R_{AV} and R_{RMS}) to R_{IN} determines the overall gain of the circuit, R_{OUT} must also be considered when selecting the low frequency breakpoint. The maximum recommended values for R_{OUT} vary from 4kΩ to 10kΩ for the circuits in Figures 1, 3, 4, and 5.

Referring to the circuit in Figure 3, and assuming a gain of 1 is desired, R_{IN} should be set to 4kΩ (R_{RMS} and R_{AV} = 4kΩ). Based on this value of R_{IN}, C_{IN} should be 2μF to place the subsonic filter pole at 20Hz. If you wish to limit the lower frequency to something other than 20 Hz then C_{IN} should be changed accordingly. The low frequency pole is governed by the simple equation

$$f_{MIN} = 1/2\pi R_{IN} C_{IN}.$$

C_{IN} should be a very low leakage capacitor to avoid impairing the dynamic range at low signal levels (many electrolytic types will not work).

The choice of R_{IN} = 10kΩ in Figure 1 is good for processing 0dBV reference signals. Given a nominal signal level of 0dBV (2.828V$_{p-p}$ = 1 V_{RMS}), this voltage across the 10kΩ input resistor gives a nominal input current of 283μA$_{p-p}$, which allows 20dB of headroom. The three other common choices for R_{IN} are 4kΩ, 5kΩ and 8kΩ, which provide 12dB, 14dB, and 18dB respectively.

The values of C_{IN}, R_{IN} and R_{OUT} can be changed accordingly to vary output levels to system requirements.

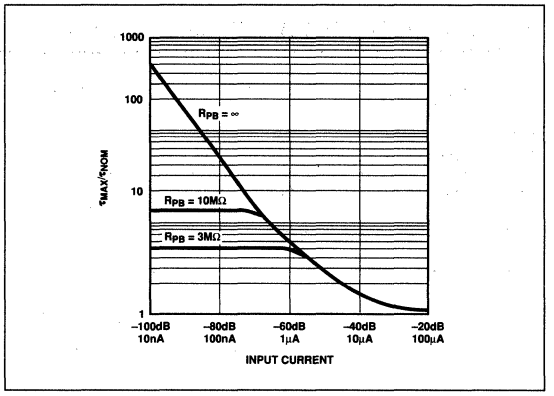


FIGURE 2: *Normalized Time Constant Relative to 1mA$_{RMS}$*

The PREBIAS pin (pin 18), can be used to increase the speed of the RMS computing loop at low signal levels at some expense to the dynamic range. Below a 10μA$_{RMS}$ input level, the time constant of the RMS loop will increase from its nominal value by a factor of 10 for every 20dB drop in level.

By use of the PREBIAS pin, one can ensure that the loop time constant will not increase above a chosen maximum as the signal level continues to decrease. The equation relating the maximum time constant increase to the value of $R_{PREBIAS}$ connected between pin 18 and V– is given by:

$$\frac{\tau_{MAX}}{\tau_{NOM}} = \frac{10\mu A \times R_{PREBIAS}}{6.8V} \quad \text{(See Figure 2)}$$

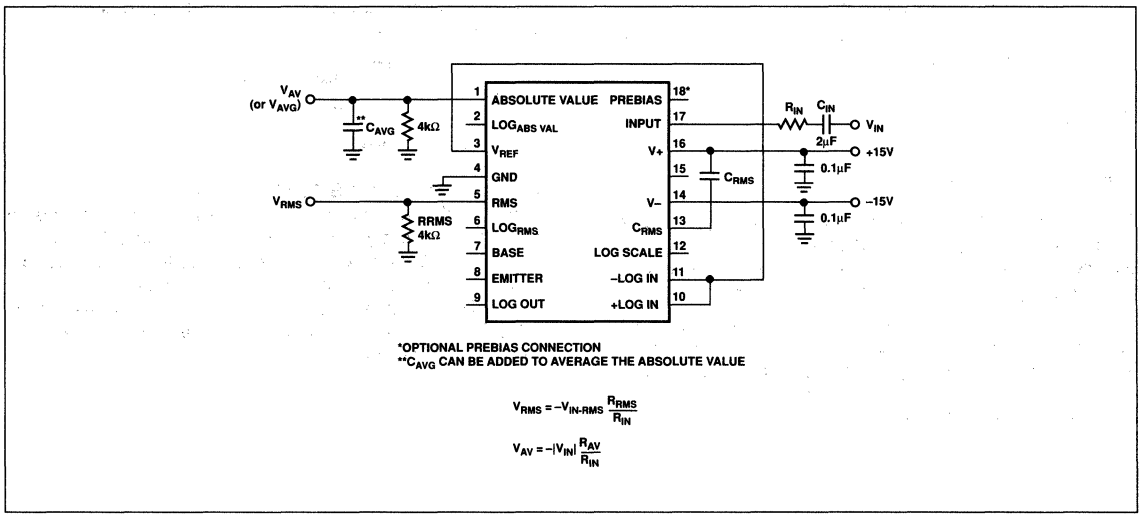


FIGURE 3: *Simple RMS/Absolute Value/Average Absolute Value Configuration*

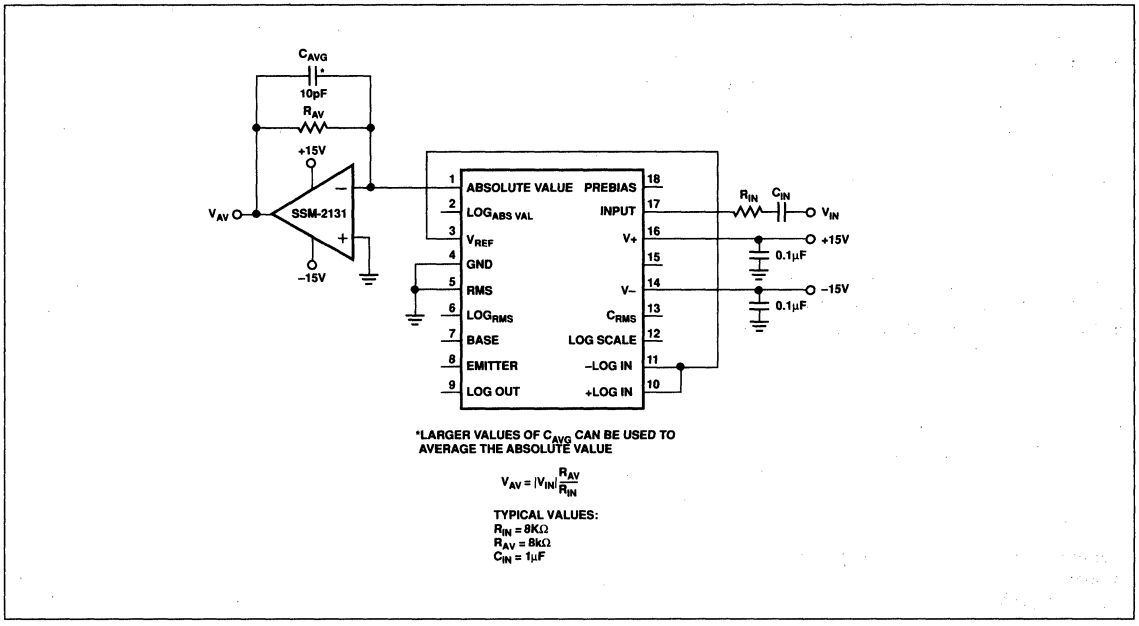


FIGURE 4: *Absolute Value and Average Absolute Value Output*

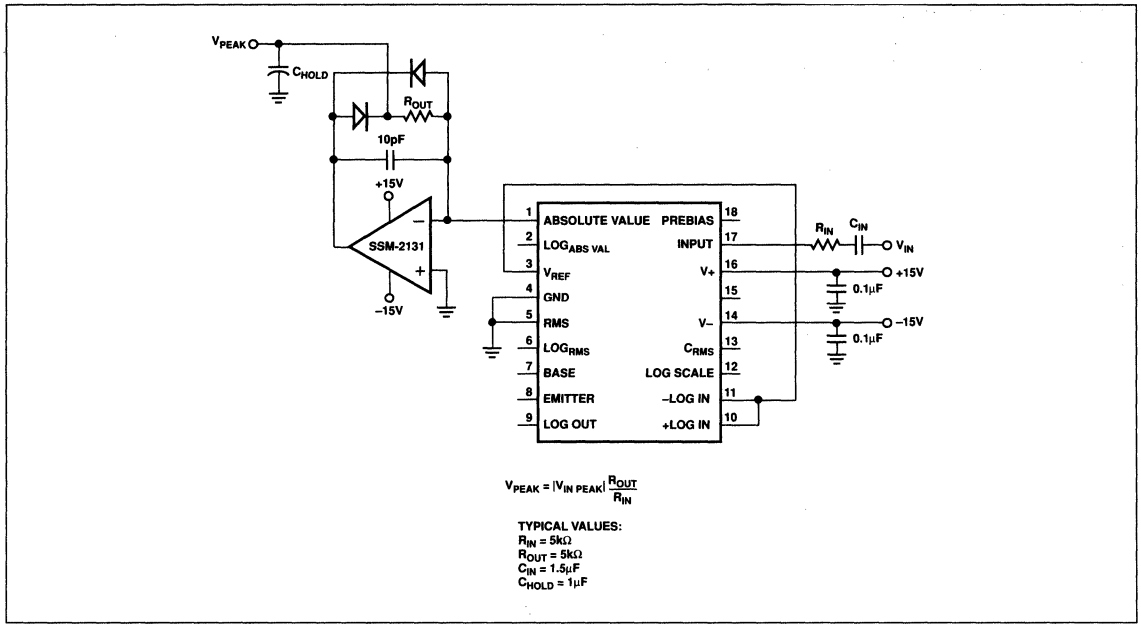


FIGURE 5: *Peak Voltage Output*

LINEAR OUTPUTS (ABSOLUTE VALUE AND RMS)

The instantaneous absolute value of the input signal appears as a current absolute value pin (pin 1). The true RMS value of the input signal similarly appears as a current into the RMS pin (pin 5). With ±15 volt supplies, the voltage compliance on these outputs is from +15 to −6 volts. For simple applications it is possible to convert these currents to negative output voltages by connecting a resistor in series with the pin(s) to ground (see Figure 3). For a maximum $3mA_{p-p}$ input signal, the resistor(s) value should be 4.0kΩ or less. To obtain an average of the absolute value output, capacitor C_{AVG} can be added in parallel with R_{AV}.

More commonly, a positive going voltage at low impedance is desired as an output. This can be accomplished by connecting a linear output pin to the virtual ground of an op amp configured as a current-to-voltage converter (see Figures 1 and 4). The scale factor for the conversion is determined by the value of R_{IN} and the feedback resistor (R_{RMS} or R_{AV}).

For the absolute value circuit in Figure 4, a maximum feedback resistor (R_{AV}) of 8kΩ allows maximum swing of the SSM-2131 output amplifier. Given a maximum output signal of $1.5mA_{PEAK}$ the SSM-2131 will be able to swing to +12V. If values larger than 8kΩ are used, then signal clipping may result.

For the RMS output circuit in Figure 1, the maximum feedback resistor (R_{RMS}) can be 10kΩ since the RMS level should never exceed 1.2mA.

A peak output can be implemented by using the circuit in Figure 5. The output scale factor is determined by R_{OUT}/R_{IN}. The decay time constant is equal to the product $R_{OUT}C_{HOLD}$. For this circuit, the feedback resistor (R_{OUT}) should be kept below 5kΩ.

A small capacitor (10pF) is usually added in parallel with the feedback resistor for stability particularly if a high slew rate JFET input op amp is used. In Figure 4, this capacitor (C_{AVG}) can be made large to obtain an average of the absolute value output. If the averaging circuit is implemented then R_{IN} can be increased to a maximum of 10kΩ since the 1.5mA peaks will no longer be present.

If the signal levels being processed are less than $3mA_{p-p}$ then the above mentioned feedback resistors can be increased accordingly.

The circuits in Figures 1 and 4 can be connected at the same time providing the user with multiple functions from a single SSM-2110. R_{IN}, R_{RMS} and R_{AV} should be set so that clipping does not occur.

The linear output pins must be kept within their voltage compliance range for proper device operations. An unused linear output must always be terminated, preferably to ground.

LOG OUTPUTS (LOG_{RMS} AND $LOG_{ABS\ VAL}$)

The log of the instantaneous absolute value and the log of true RMS of the input signal appears as voltages on pins 2 and 6 respectively. However, these outputs must be buffered, level shifted and, in many applications, temperature compensated in order to be made useful.

The log recovery transistor is an internal level shifting component which may be switched between the two log outputs. This will reference the log output(s) to the internal voltage regulator which is about 7.5V above the negative supply (see Figure 6).

Figures 6, 7, and 8 show the recommended connection between the log output transistor Q_2 or Q_{10}, and the log recovery transistor Q_{11}. Note that although the log recovery transistor can be switched between the two log outputs, only one log output can be recovered at a time. With the resistor values R_{REF1} and R_{REF2} shown, the output swing at the emitter of Q_{11} over the dynamic

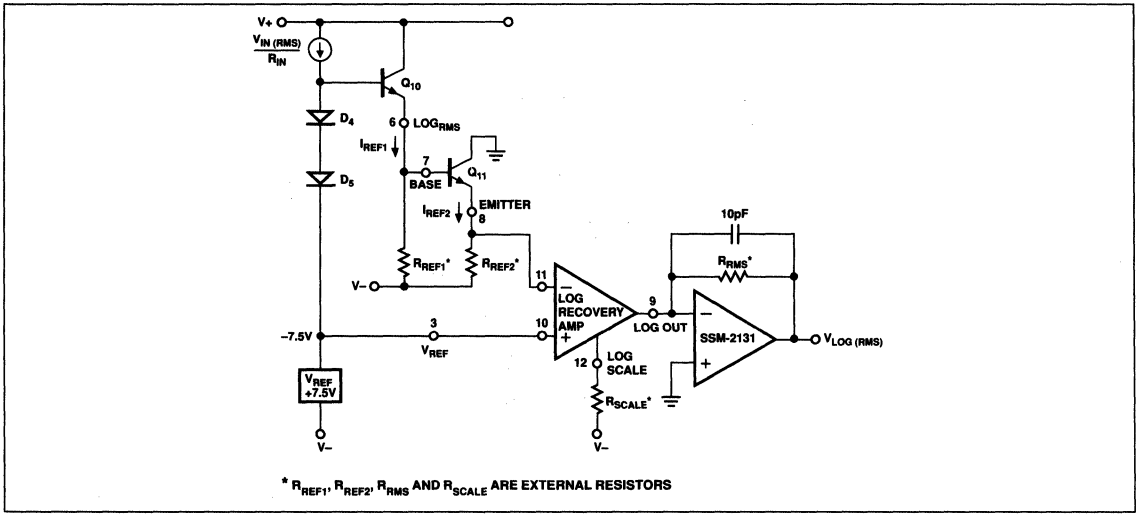


FIGURE 6: *Log Recovery Circuit*

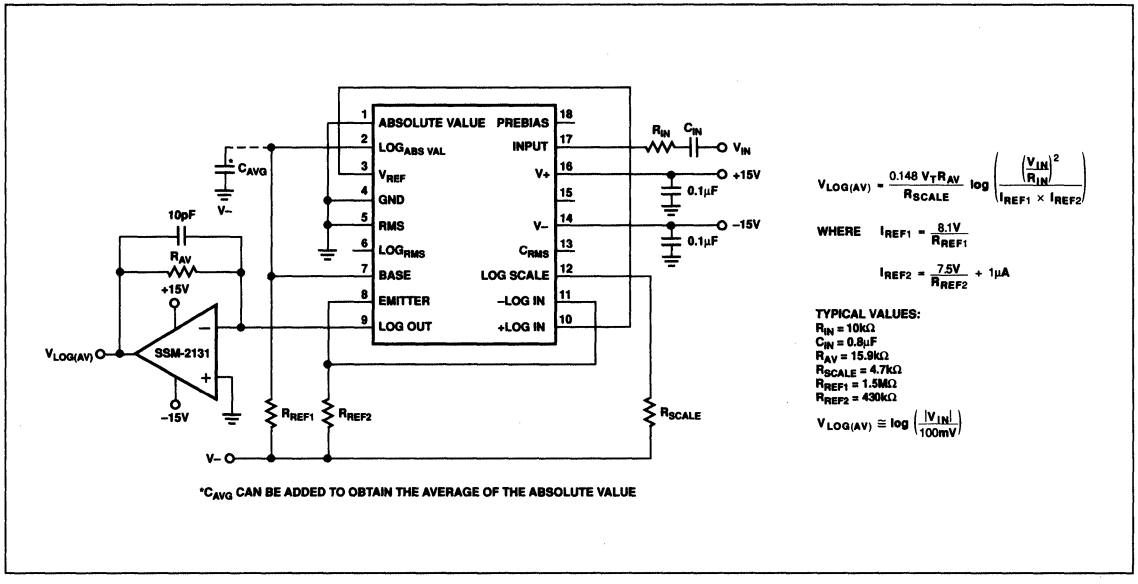


FIGURE 7: *Log of Absolute Value/Average Absolute Value*

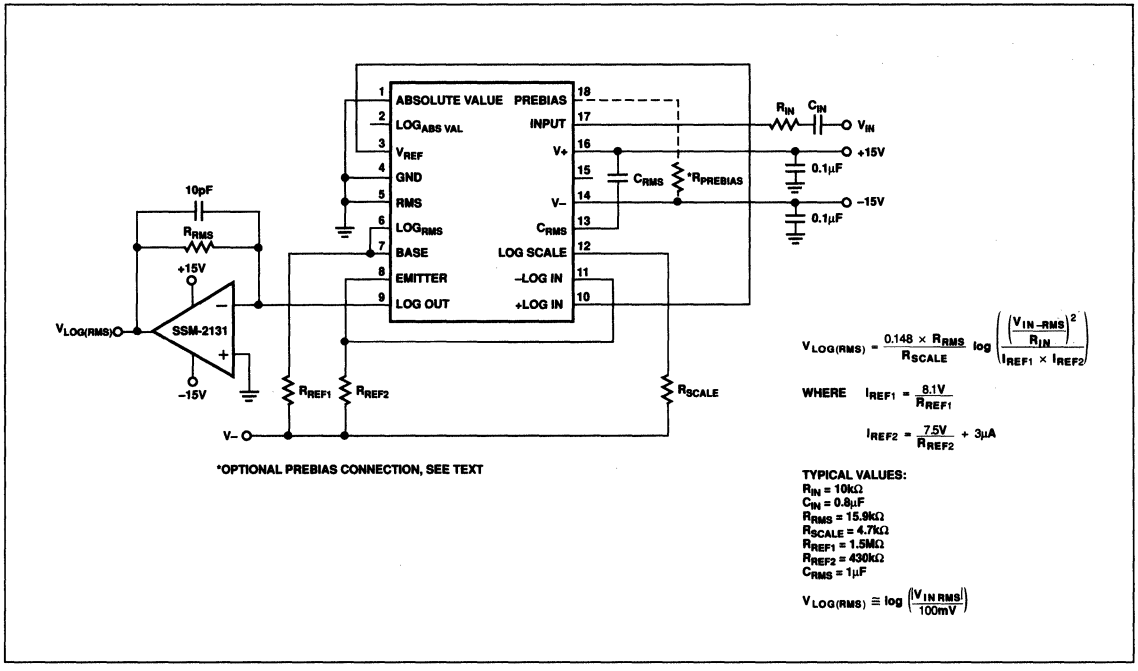


FIGURE 8: *Log of RMS*

range of the device will be roughly symmetrical about the internal negative voltage reference. Also, the output impedance will be low enough to drive the log amplifier's input(s) without introducing significant errors. The bias current into the pins of the log amplifier is typically less than 1μA but can be as high as 2μA. For this reason the current through the log recovery transistor Q_{11} should always be set higher than 5μA. The current I_{REF1} should not be set too high (above 50μA) because the base current of Q_{10} induces errors in the RMS computing loop. If higher reference currents are required then they should be taken care of by changing the current through Q_{11}. This can be done by changing R_{REF2}. The Log Recovery Amplifier Section explains this in more detail.

The output sensitivity at EMITTER (pin 8) is about +60mV for every 10dB of signal level increase at 25°C. This sensitivity has a temperature coefficient of +3300ppm/°C.

The log of absolute value output can be converted to a log of mean value by connecting a capacitor between $LOG_{ABS\ VAL}$ (pin 2) and V– (see Figure 7). Since this is an emitter follower output, the response to a large-signal level increase will be fast while the time constant of the output following a large-signal level decrease will be determined by the product of capacitor C_{AVG} and resistor R_{REF1}.

One might think that connecting a capacitor to the log output would produce the average of the log of the absolute value. However, since the capacitor enforces an AC ground at the emitter of the output transistor, the capacitor charging currents are proportional to the antilog of the signal at the base. Since the base voltage is the log of the absolute value, the log and the antilog terms cancel, and the capacitor is charged as a linear integrator with a current directly proportional to the absolute value of the input current. This effectively inverts the order of the averaging and logging operations. The signal at the output, therefore, is the log of the average of the absolute value of the input signal.

LOG RECOVERY AMPLIFIER (PINS 9,10, 11 AND 12)

The log recovery amplifier is a linearized voltage-to-current transconductor whose gain can be made proportional to absolute temperature. It is used to reference the log output(s) to ground and also to temperature compensate the V_T (KT/q) terms in the log output recovery transistors (Q_2/Q_{10} and Q_{11}).

One input of the log recovery amplifier is usually connected to EMITTER (the emitter of the log recovery transistor–pin 8) while the other is connected to V_{REF} (pin 3).

Figure 6 shows the internal and external connections used to obtain an output voltage equal to $V_{LOG(RMS)}$. The transfer characteristic of the log recovery transistors is given by the following equation:

$$\Delta V_{IN} = V_T \times \ln\left(\frac{(V_{IN(RMS)}/R_{IN})^2}{I_{REF1} \times I_{REF2}}\right)$$

where, $I_{REF1} \approx \left(\frac{8.1V}{R_{REF1}}\right)$

$$I_{REF2} \approx \left(\frac{7.5V}{R_{REF2}}\right) + 1\mu A$$

The transfer characteristic of the log recovery amplifier is given by the following equation:

$$I_{OUT} = \frac{64mV\ \Delta V_{IN}}{R_{SCALE}\ V_T}$$

Combining the two equations yields the overall transfer characteristic for the ouput voltage $V_{LOG(RMS)}$:

$$V_{LOG\ (RMS)} = \frac{0.148 \times R_{RMS}}{R_{SCALE}} \times \log\left(\frac{(V_{IN}/R_{IN})^2}{I_{REF1} \times I_{REF2}}\right)$$

where, $I_{REF1} \approx \left(\frac{8.1V}{R_{REF1}}\right)$

$$I_{REF2} \approx \left(\frac{7.5V}{R_{REF2}}\right) + 1\mu A$$

Ideally this voltage is completely independent of temperature. However, due to the temperature coefficient of several transistors internal to the SSM-2110, this is not entirely true. The temperature coefficient is approximately ±75ppm/°C.

With the values shown in Figures 7 and 8, this transfer function corresponds to an output change of 50mV/dB. The reference current is set to 10μA to provide the widest possible dynamic range. The following results can be expected for the circuit in Figure 8:

$V_{IN\ (RMS)}$	100μV	1mV	10mA	100mV	1V	10V
$I_{IN\ (RMS)}$	10nA	100nA	1μA	10μA	100μA	1mA
$V_{LOG\ OUT}$	–3V	–2V	–1V	0V	1V	2V

An R_{SCALE} value of approximately 4.7kΩ gives the best overall linearity and temperature compensation performance. This is an improvement of about a factor of 40 over the uncompensated drift. A 2kΩ resistor in series with a silicon diode can be connected from LOG SCALE (pin 12) to the negative supply to defeat the temperature compensation for certain applications such as compressor/limiters where the log drift will cancel the thermal gain drift of a VCA's dB/volt control port.

The maximum output current for both the compensated and uncompensated examples above is ±250μA. This output current is converted to a voltage with the circuits in Figures 7 and 8. For these circuits this corresponds to a maximum output voltage of ±3.975V. If R_{SCALE} is changed from the nominal value of 4.7kΩ the maximum output current will also change by the following equation:

$$I_{LOG\ OUT\ (MAX)} = \frac{1.18V}{R_{SCALE}}$$

If the log recovery amplifier is not used, +LOG IN (pin 10) and –LOG IN (pin 11) must be connected to V_{REF} (pin 3) for proper operation of the rest of the circuit.

It is possible to use one of the log configurations in Figure 7 or 8 in conjunction with the linear output circuits (Figures 1, 3, 4 and 5) but care must be taken in choosing the appropriate resistor values. This provides the user with substantial flexibility from a single device.

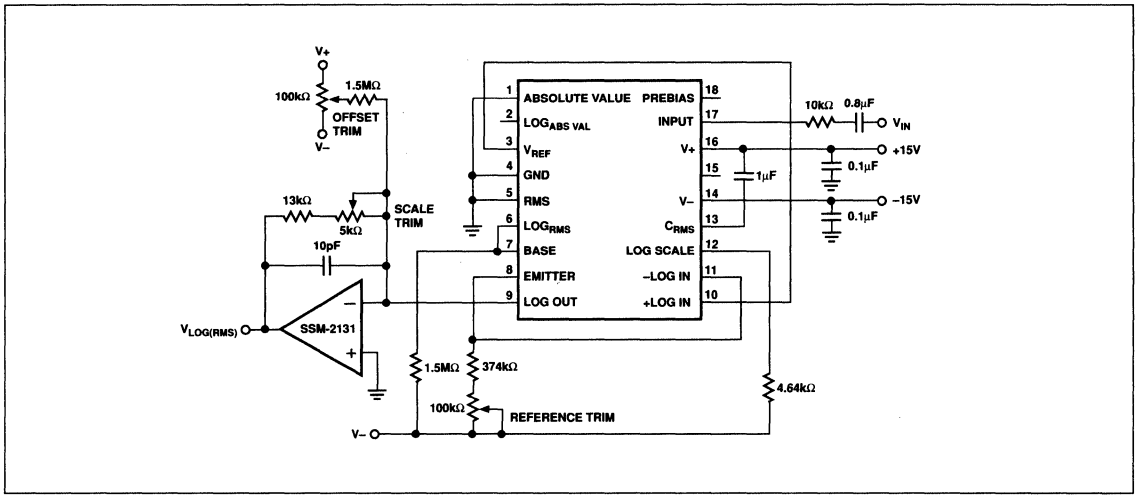


FIGURE 9: *Error Trimming*

ERROR TRIMMING

The offset, reference and scale factor trims (Figure 9) can be used to improve the overall accuracy of the device. The correct procedure for trimming out the various errors is as follows. First, +LOG IN (pin 10) and –LOG IN (pin 11) should be connected to V_{REF} (pin 3). The offset trim should be adjusted to achieve 0V at the $V_{LOG(RMS)}$ output. This nulls out any DC errors due to offsets in the log recovery amplifier. Second, reconnect the ±LOG IN pins as shown in Figure 9. Apply an input signal of $100mV_{RMS}$ ($10\mu A_{RMS}$). Adjust the reference trim to obtain 0V at the $V_{LOG(RMS)}$ output. This compensates for the input bias current of the log recovery amplifier and other errors. It sets the reference current to 10μA. Third, change the input signal to $1V_{RMS}$ ($100\mu A_{RMS}$). Adjust the scale trim to obtain 1.000V at the $V_{LOG(RMS)}$ output. This adjusts the scale factor to obtain 1V/20dB (50mV/dB). If other reference currents or scale factors are used then steps 2 and 3 will have to be changed accordingly.

This same procedure can be used for the log absolute value and log average absolute value configurations. If the log recovery amplifier is not used then the circuit in Figure 10 should be used to trim the offsets.

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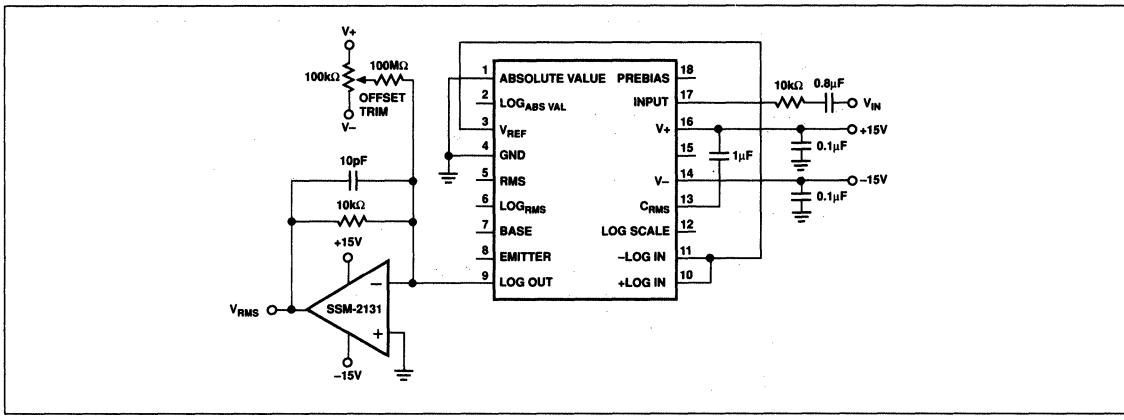
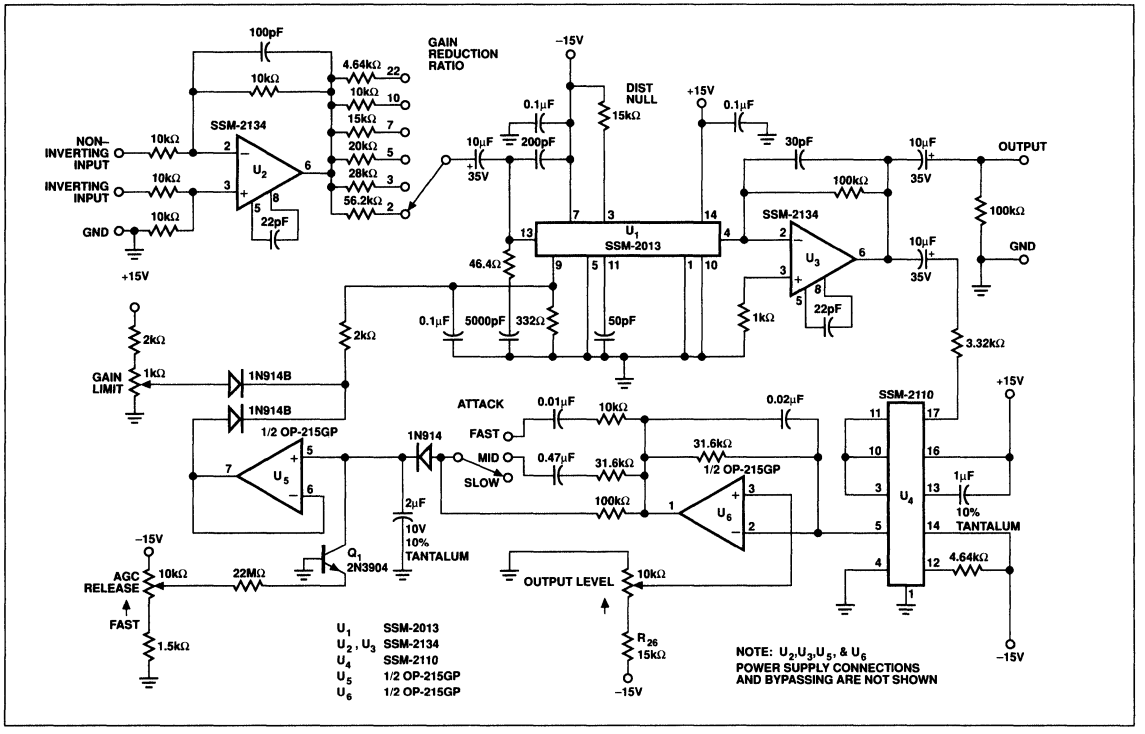


FIGURE 10: *Offset Trimming*

WAVEFORM	RMS	AVERAGE OF ABSOLUTE VALUE (A_{AV})	CREST FACTOR = $\frac{V_P}{RMS}$
V_P SINE WAVE	$\frac{V_P}{\sqrt{2}}$	$\frac{2 \cdot V_P}{\pi}$	$\sqrt{2} = 1.414$
V_P SQUARE WAVE	V_P	V_P	1
V_P TRIANGLE WAVE	$\frac{V_P}{\sqrt{3}}$	$\frac{V_P}{\sqrt{2}}$	$\sqrt{3} = 1.732$
$2V_P$ GAUSSIAN NOISE	RMS	$\sqrt{\frac{2}{\Pi}}$ x RMS	Typically varies from 1 to 6 depending on the characteristic of the noise. Theoretically, the crest factor is unlimited.

FIGURE11: *RMS, Average of Absolute Value and Crest Factors for Different Waveforms*



TYPICAL APPLICATIONS

AUTOMATIC GAIN CONTROL (AGC) AMPLIFIER

The automatic gain control amplifier shown below features selectable gain reduction compression ratios and time domain adjustable AGC attack and release. The design employs the SSM-2013 VCA, SSM-2110 true RMS-to-DC converter, two SSM-2134 low noise op amps and an OP-215 FET input op amp.

For additional information about this circuit, please see application note AN-116.

Dynamic Range Processors/Dual VCA

SSM-2120/SSM-2122

FEATURES

- 0.01% THD at +10dBV In/Out
- 100dB VCA Dynamic Range
- Low VCA Control Feedthrough
- 100dB Level Detection Range
- Log/Antilog Control Paths
- Low External Component Count

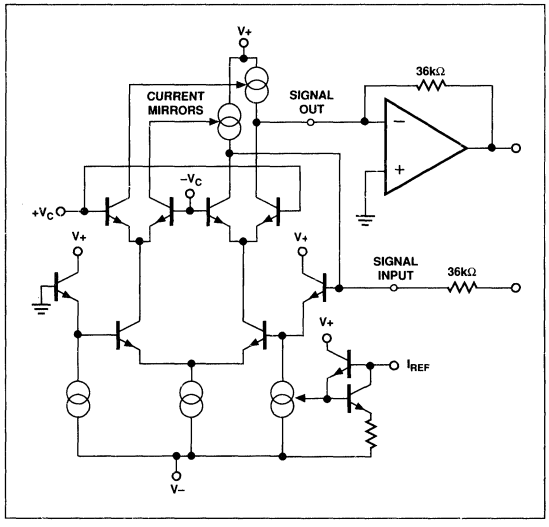
APPLICATIONS

- Compressors
- Expanders
- Limiters
- AGC Circuits
- Voltage-Controlled Filters
- Noise Reduction Systems
- Stereo Noise Gates

ORDERING INFORMATION

PACKAGE		OPERATING TEMPERATURE RANGE
PLASTIC 16-PIN	PLASTIC 22-PIN	
SSM2122P	SSM2120P	–10°C to +50°C

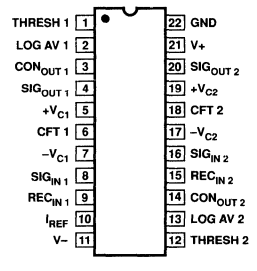
SIMPLIFIED SCHEMATIC (VCA Section Only)



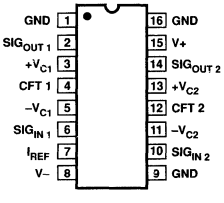
GENERAL DESCRIPTION

The SSM-2120 is a monolithic integrated circuit designed for the purpose of processing dynamic signals in various analog systems including audio. This "dynamic range processor" consists of two VCAs and two level detectors (the SSM-2122 consists of two VCAs only). These circuit blocks allow the user to logarithmically control the gain or attenuation of the signals presented to the level detectors depending on their magnitudes. This allows the compression, expansion or limiting of AC signals, some of the primary applications for the SSM-2120.

PIN CONNECTIONS



SSM-2120
22-PIN PLASTIC DIP
(P-Suffix)



SSM-2122
16-PIN PLASTIC DIP
(P-Suffix)

7

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Operating Temperature Range ..... –10° to +55°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65° to +150°C
Maximum Current into Any Pin 10mA
Lead Temperature Range (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
16-Pin Plastic DIP (P)	86	10	°C/W
22-Pin Plastic DIP (P)	70	7	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, I_{REF} = 200µA, A_V = 1, unless otherwise noted.

		SSM-2120/SSM-2122			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
POWER SUPPLY					
Supply Voltage Range		±5	–	±18	V
Positive Supply Current		–	8	10	mA
Negative Supply Current		–	6	8	mA
VCAs					
Max I_{SIGNAL} (In/Out)		±387	±400	±413	µA
Output Offset		–	±1	±2	µA
Control Feedthrough (Trimmed)	$R_{IN} = R_{OUT} = 36k\Omega$, $A_V \leq 0dB \leq -30dB$	–	750	–	µV
Gain Control Range	Unity-Gain	–100	–	+40	dB
Control Sensitivity		–	6	–	mV/dB
Gain Scale Factor Drift		–	–3300	–	ppm/°C
Frequency Response	Unity-Gain or Less	–	250	–	kHz
Off Isolation	At 1kHz	–	100	–	dB
Current Gain	$+V_C = -V_C = 0V$	–0.25	0	+0.25	dB
THD (Unity-Gain)	+10dBV IN/OUT	–	0.005	0.02	%
Noise (20kHz Bandwidth)	RE: 0dBV	–	–80	–	dB
LEVEL DETECTORS (SSM-2120 ONLY)					
Dynamic Range		100	110	–	dB
Input Current Range		0.03	–	3000	μA_{p-p}
Rectifier Input Bias Current		–	4	16	nA
Output Sensitivity (At LOG AV Pin)		–	3	–	mV/dB
Output Offset Voltage		–	±0.5	±2	mV
Frequency Response					
$I_{IN} = 1mA_{p-p}$		–	1000	–	
$I_{IN} = 10\mu A_{p-p}$		–	50	–	kHz
$I_{IN} = 1\mu A_{p-p}$		–	7.5	–	
CONTROL AMPLIFIERS (SSM-2120 ONLY)					
Input Bias Current		–	85	175	nA
Output Drive (Max Sink Current)		5.0	7.5	–	mA
Input Offset Voltage		–	±0.5	±2	mV

NOTE:
1. Specifications are subject to change; consult latest data sheet.

VOLTAGE-CONTROLLED AMPLIFIERS

The two voltage-controlled amplifiers are full Class A current in/current out devices with complementary dB/V gain control ports. The control sensitivities are +6mV/dB and –6mV/dB. A resistor divider (attenuator) is used to adapt the sensitivity of an external control voltage to the range of the control port. It is best to use 200Ω or less for the attenuator resistor to ground.

VCA INPUTS

The signal inputs behave as virtual grounds. The input current compliance range is determined by the current into the reference current pin.

REFERENCE PIN

The reference current determines the input and output current compliance range of the VCAs. The current into the reference pin is set by connecting a resistor to V+. The voltage at the reference pin is about two volts above V– and the current will be

$$I_{REF} = \frac{[(V+) - ((V-) + 2V)]}{R_{REF}}$$

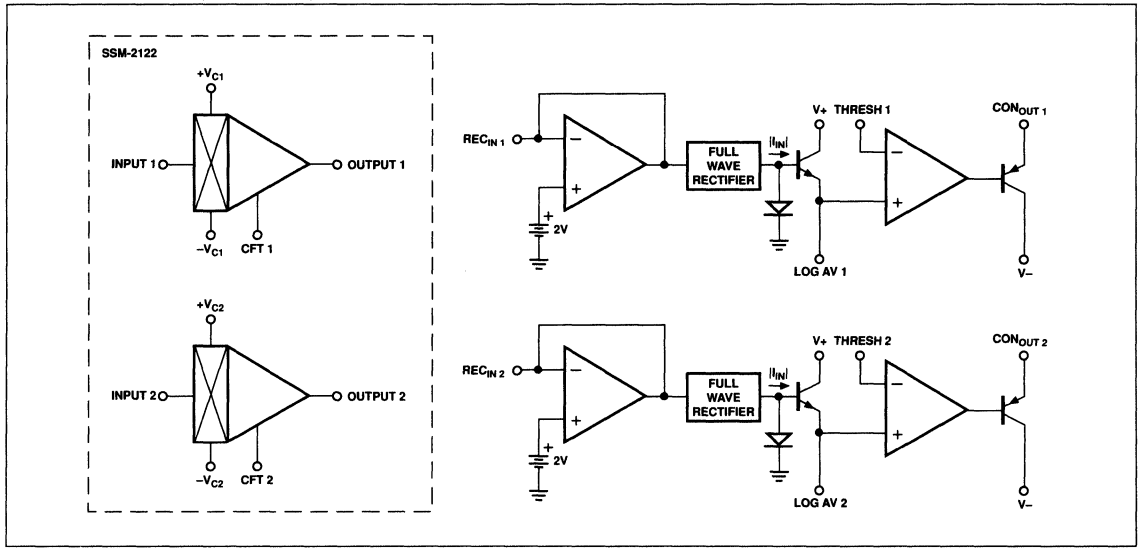
The current consumption of the VCAs will be directly proportional to I_{REF} which is nominally 200μA. The device will operate at lower current levels which will reduce the effective dynamic range of the VCAs. With a 200μA reference current, the input and output clip points will be ±400μA. In general:

$$I_{CLIP} = \pm 2 I_{REF}$$

VCA OUTPUTS

The VCA outputs are designed to interface directly with the virtual ground inputs of external cperational amplifiers configured as current-to-voltage converters. The outputs must operate at virtual ground because of the output stage's finite output impedance. The power supplies and selected compliance range determines the values of input and output resistors needed. As an example, with ±15V supplies and ±400μA maximum input and output current, choose $R_{IN} = R_{OUT} = 36k\Omega$ for an output compliance range of ±14.4 V. Note that the signal path through the VCA including the output current-to-voltage converter is noninverting.

BLOCK DIAGRAM (SSM-2120)



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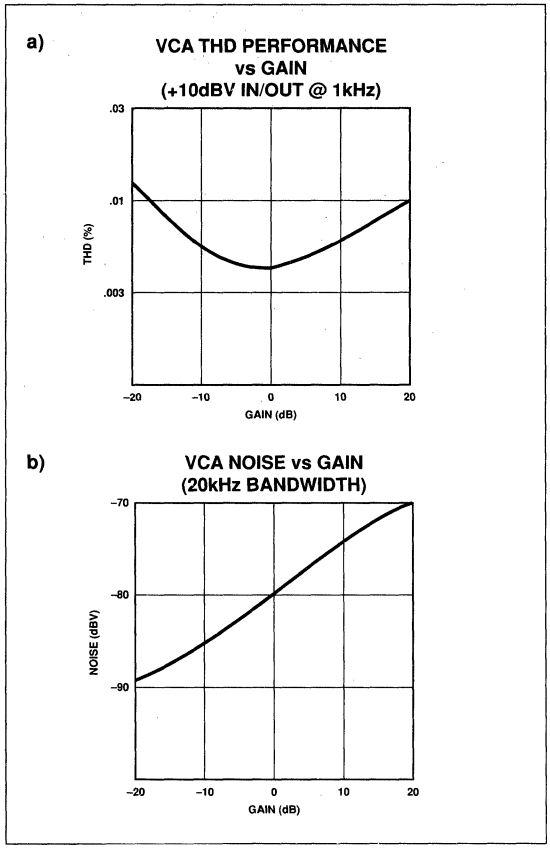

FIGURE 1: *Typical THD and Noise Performance*

VCA PERFORMANCE

Figures 1a and 1b show the typical THD and noise performance of the VCAs over ±20dB gain/attenuation. Full Class A operation provides very low THD.

TRIMMING THE VCAs

The control feedthrough (CFT) pins are optional control feedthrough null points. CFT nulling is usually required in applications such as noise gating and downward expansion. If trimming is not used, leave the CFT pins open.

Trim Procedure

1) Apply a 100Hz sine wave to the control point attenuator. The signal peaks should correspond to the control voltages which induce the VCAs maximum intended gain and at least 30dB of attenuation.

2) Adjust the 50kΩ potentiometer for the minimum feedthrough.

(Trimmed control feedthrough is typically well under $1mV_{RMS}$ when the maximum gain is unity using 36kΩ input and output resistors.)

Applications such as compressor/limiters typically do not require control feedthrough trimming because the VCA operates at unity-gain unless the signal is large enough to initiate gain reduction. In this case the signal masks control feedthrough.

This trim is ineffective for voltage-controlled filter applications.

LEVEL DETECTION CIRCUITS

The SSM-2120 contains two independent level detection circuits. Each circuit contains a wide dynamic range full-wave rectifier, logging circuit and a unipolar drive amplifier. These circuits will accurately detect the input signal level over a 100dB range from 30nA to 3mA peak-to-peak.

LEVEL DETECTOR THEORY OF OPERATION

Referring to the level detector block diagram of Figure 2, the REC_{IN} input is an AC virtual ground. The next block implements the full-wave rectification of the input current. This current is then fed into a logging transistor (Q_1) whose pair transistor (Q_2) has a fixed collector current of I_{REF}. The LOG AV output is then:

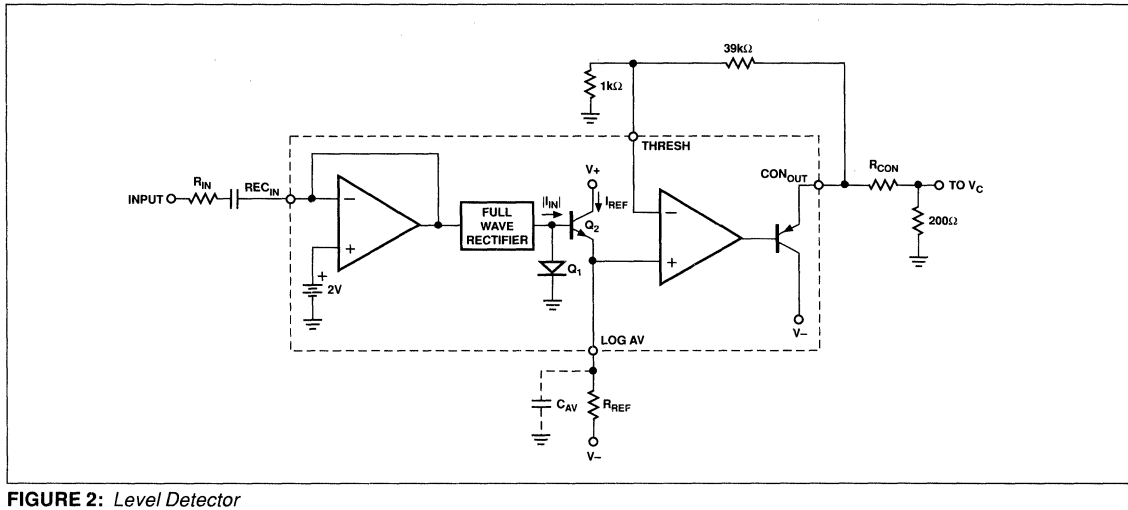

FIGURE 2: *Level Detector*

$$V_{LOG\ AV} = \frac{kT}{q} \ln\left(\frac{|I_{IN}|}{I_{REF}}\right)$$

With the use of the LOG AV capacitor the output is then the log of the average of the absolute value of I_{IN}.

(The unfiltered LOG AV output has broad flat plateaus with sharp negative spikes at the zero crossing. This reduces the "work" that the averaging capacitor must do, particularly at low frequencies.)

Note: It is natural to assume that with the addition of the averaging capacitor, the LOG AV output would become the **average of the log of the absolute value of I_{IN}**. However, since the capacitor forces an AC ground at the emitter of the output transistor, the capacitor charging currents are proportional to the **antilog** of the voltage at the base of the output transistor. Since the base voltage of the output transistor is the log of the absolute value of I_{IN}, the log and antilog terms cancel, so the capacitor becomes a linear integrator with a charging current directly proportional to the absolute value of the input current. This effectively inverts the order of the averaging and logging functions. The signal at the output therefore is the **log of the average of the absolute value of I_{IN}**.

USING DETECTOR PINS REC_{IN}, LOG_{AV}, THRESH AND CON_{OUT}

When applying signals to REC_{IN} (rectifier input) an input series resistor should be followed by a low leakage blocking capacitor since REC_{IN} has a DC voltage of approximately 2.1V above ground. Choose R_{IN} for a ±1.5mA peak signal. For ±15V operation this corresponds to a value of 10kΩ.

A 1.5MΩ value of R_{REF} from log average to –15V will establish a 10µA reference current in the logging transistor (Q_1). This will bias the transistor in the middle of the detector's dynamic current range in dB to optimize dynamic range and accuracy. The LOG AV outputs are buffered and amplified by unipolar drive op amps. The 39kΩ, 1kΩ resistor network at the THRESH pin provides a gain of 40.

An attenuator from the CON_{OUT} (control output) to the appropriate VCA control port establishes the control sensitivity. Use 200Ω for the attenuator resistor to ground and choose R_{CON} for the desired sensitivity. Care should be taken to minimize capacitive loads on the control outputs CON_{OUT}. If long lines or capacitive loads are present, it is best to connect the series resistor R_{CON} as closely to the CON_{OUT} pin as possible.

DYNAMIC LEVEL DETECTOR CHARACTERISTICS

Figures 3 and 4 show the dynamic performance of the level detector to a change in signal level. The input to the detector (not shown) is a series of 500ms tone bursts at 1kHz in successive 10dBV steps. The tone bursts start at a level of –60dBV (with R_{IN} =10k) and return to –60dBV after each successive 10dB step. Tone bursts range from –60dBV to +10dBV. Figure 3 shows the logarithmic level detector output. The output of the detector is 3mV/dB at LOG AV and the amplifier gain is 40 which yields 120mV/dB. Thus, the output at CON_{OUT} is seen to increase by 1.2V for each 10dBV increase in input level.

DYNAMIC ATTACK AND DECAY RATES

Figure 4 shows the output levels overlayed using a storage scope. The attack rate is determined by the step size and the value of C_{AV}. The attack time to final value is a function of the step size increase. The chart of Figure 5 shows the values of total settling times to within 5, 3, 2 and 1dB of final value with C_{AV} = 10µF. When step sizes exceed 40dB, the increase in settling time for larger steps is negligible. To calculate the attack time to final value for any value of C_{AV}, simply multiply the value in the chart by C_{AV}/10µF.

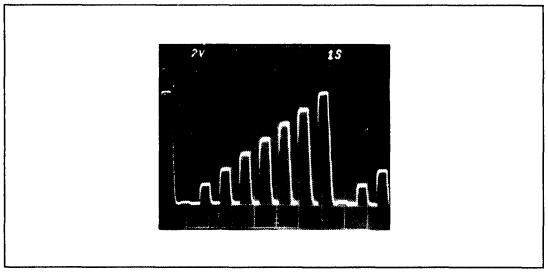

FIGURE 3: *Detector Output*

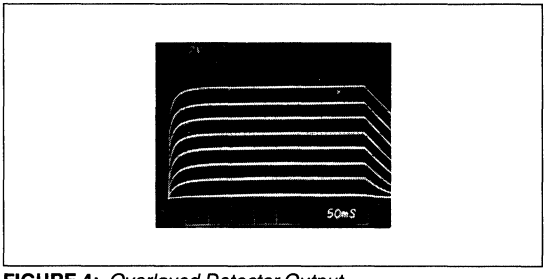

FIGURE 4: *Overlayed Detector Output*

The decay rates are linear ramps that are dependent on the current out of the LOG AV pin (set by R_{REF}) and the value of C_{AV}. The integration or decay time of the circuit is derived from the formula:

$$\text{Decrementation Rate (in dB/s)} = \frac{I_{REF} \times 333}{C_{AV}}$$

	5dB	3dB	2dB	1dB
10dB Step	11.28ms	21.46	30.19	46.09
20dB Step	16.65	26.83	35.56	51.46
30dB Step	18.15	28.33	37.06	52.96
40dB Step	18.61	27.79	37.52	53.42
50dB Step			(+144µs)	
60dB Step			(+46µs)	

FIGURE 5: *Settling Time (t_S) for C_{AV} = 10µF, $t_S' = t_S$ (C_{AV}/10µF)*

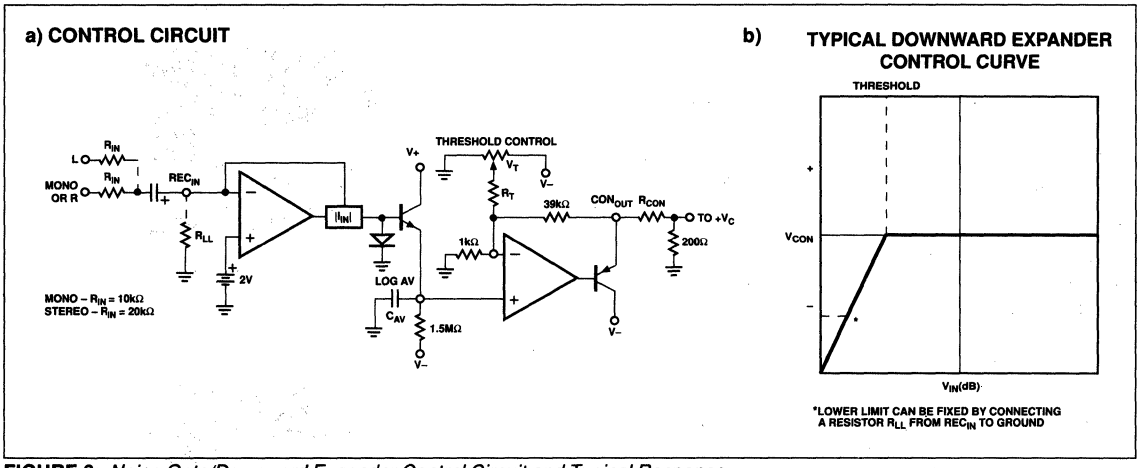

FIGURE 6: *Noise Gate/Downward Expander Control Circuit and Typical Response*

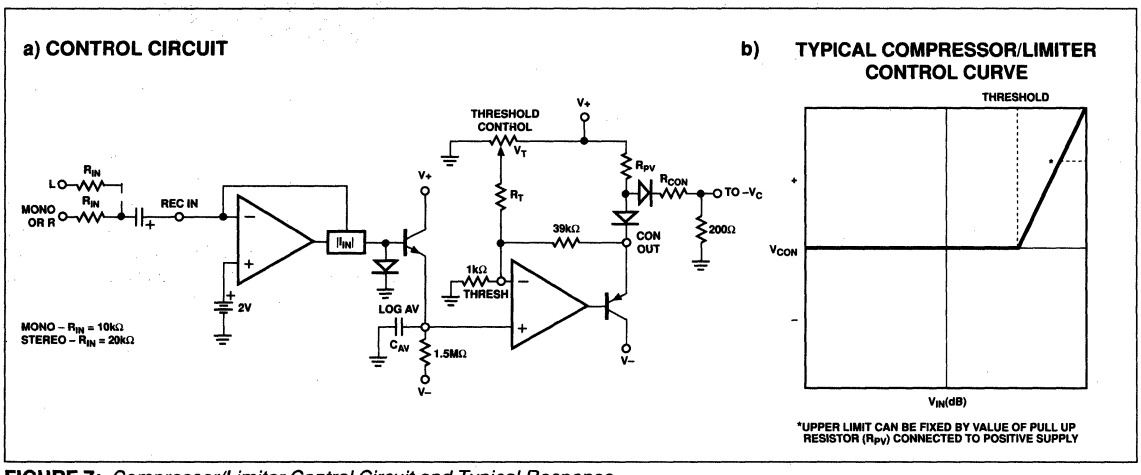

FIGURE 7: *Compressor/Limiter Control Circuit and Typical Response*

APPLICATIONS

The following applications for the SSM-2120 use both the VCAs and level detectors in conjunction to assimilate a variety of functions.

The first section describes the arrangement of the threshold control in each control circuit configuration. These control circuits form the foundation for the applications to follow which include the downward expander, compressor/limiter and compandor.

THRESHOLD CONTROL

Figure 6a shows the control circuit for a typical downward expander while Figure 6b shows a typical control curve. Here, the threshold potentiometer adjusts V_T to provide a negative unipolar control output. This is typically used in noise gate, downward expander, and dynamic filter applications. This potentiometer is used in all applications to control the signal level versus control voltage characteristics.

In the noise gate, downward expander and compressor/limiter applications, this potentiometer will establish the onset of the control action. The sensitivity of the control action depends on the value of R_T.

For a positive unipolar control output add two diodes as shown in Figure 7a. This is useful in compressor/limiter applications. Figure 7b shows a typical response.

Bipolar control outputs can be realized by adding a resistor from the op amp output to V+. This is useful in compandor circuits as

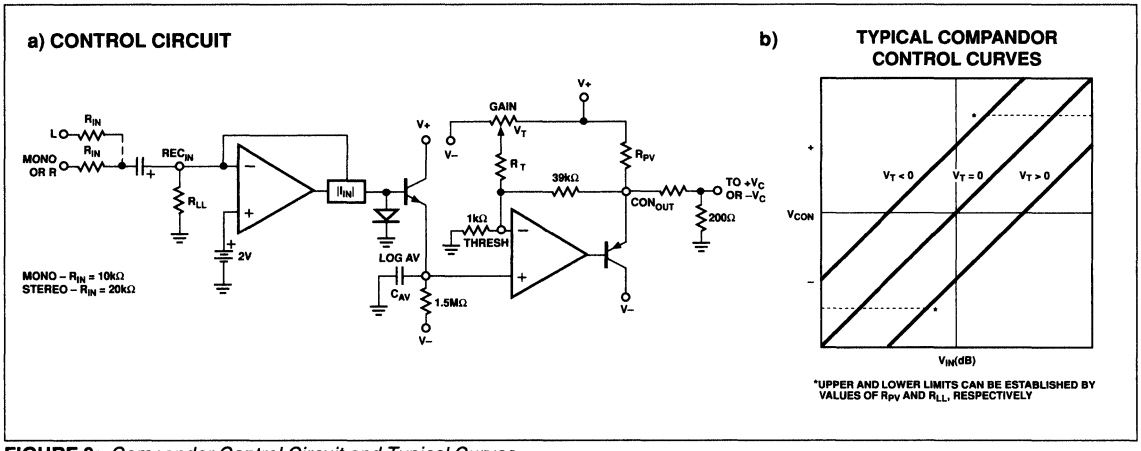

FIGURE 8: *Compandor Control Circuit and Typical Curves*

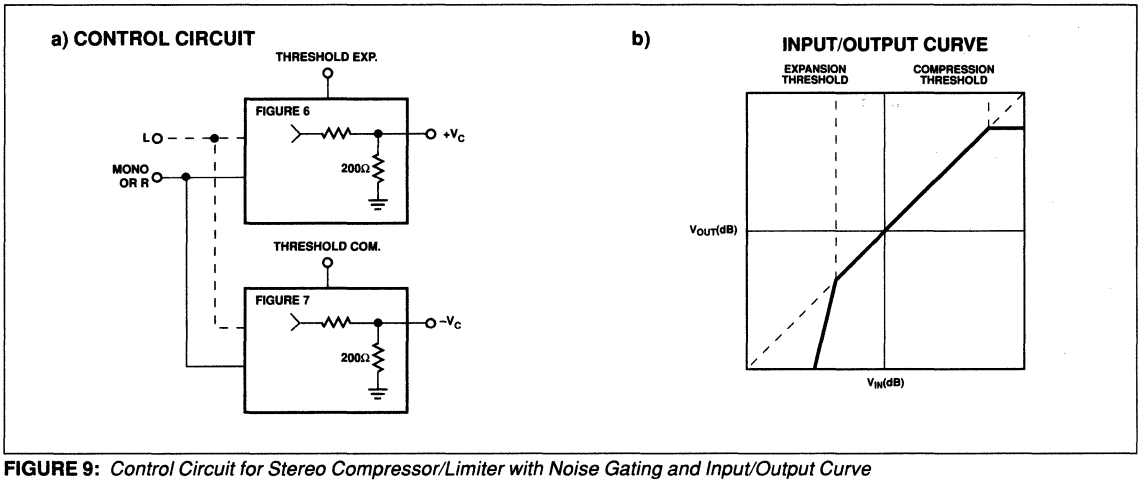

FIGURE 9: *Control Circuit for Stereo Compressor/Limiter with Noise Gating and Input/Output Curve*

shown in Figure 8a, with its response in Figure 8b. The value of the resistor R_{PV} will determine the maximum output from the control amplifier.

STEREO COMPRESSOR/LIMITER

The two control circuits of Figures 6 and 7 can be used in conjunction to produce composite control voltages. Figures 9a and 9b show this type of circuit and transfer function for a stereo compressor/limiter which also acts as a downward expander for noise gating. The output noise in the absence of a signal will be dependent on the noise of the current-to-voltage converter amplifier if the expansion ratio is high enough.

As discussed in the Threshold Control section, the use of the control circuit of Figure 5, including the R_{PV} to V+ and two diodes, yields positive unipolar control outputs.

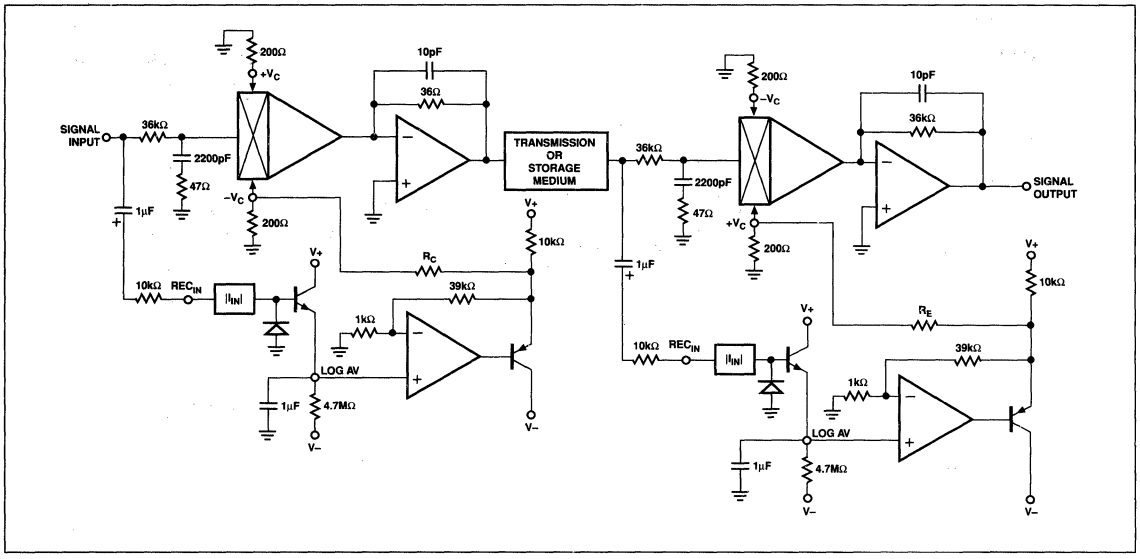

FIGURE 10: *Companding Noise Reduction System*

COMPANDING NOISE REDUCTION SYSTEM

A complete companding noise reduction system is shown in Figure 10. Normally, to obtain an overall gain of unity, the value of R_C is equal to R_E. The values of $R_{C/E}$ will determine the compression/expansion ratio.

Table 1 shows compression/expansion ratios ranging from 1.5:1 to full limiting with the corresponding values of $R_{C/E}$.

An example of a 2:1 compression/expansion ratio is plotted in Figure 11. Note that signal compression increases gain for low level signals and reduces gain for high levels while expansion does the reverse. The net result for the system is the same as the original input signal except that it has been compressed before being sent to a given medium and expanded after recovery. The compression/expansion ratio needed depends on the medium being used. As an extreme example, a household tape player would require a higher compression/expansion ratio than a professional stereo system.

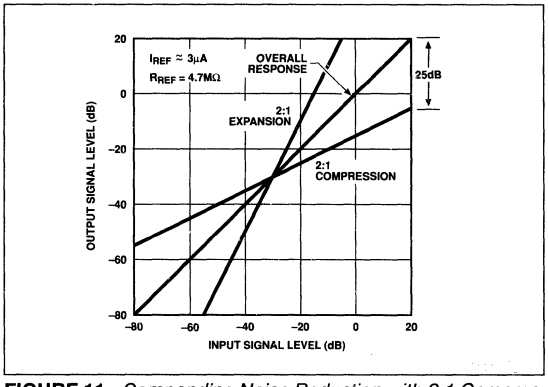

FIGURE 11: *Companding Noise Reduction with 2:1 Compression/Expansion Ratio*

TABLE 1

INPUT SIGNAL INCREASE (dB)	GAIN (REDUCTION OR INCREASE) (dB)	COMPRESSOR ONLY OUTPUT SIGNAL INCREASE (dB)	EXPANDER ONLY OUTPUT SIGNAL INCREASE (dB)	COMPRESSION/ EXPANSION RATIO	$R_{C/E}$ Ω	$\Delta V_{CONTROL}$ (mV/dB)
20	6.67	13.33	22.67	1.5:1	11,800	2.0
20	10.00	10.00	30.00	2:1	7,800	3.0
20	13.33	6.67	33.33	3:1	5,800	4.0
20	15.00	5.00	35.00	4:1	5,133	4.5
20	16.00	4.00	36.00	5:1	4,800	4.8
20	17.33	2.67	37.33	7.5:1	4,415	5.2
20	18.00	2.00	38.00	10:1	4,244	5.4
20	20.00	0	40.00	AGC*/Limiter	3,800	6.0

*AGC for Compression Only

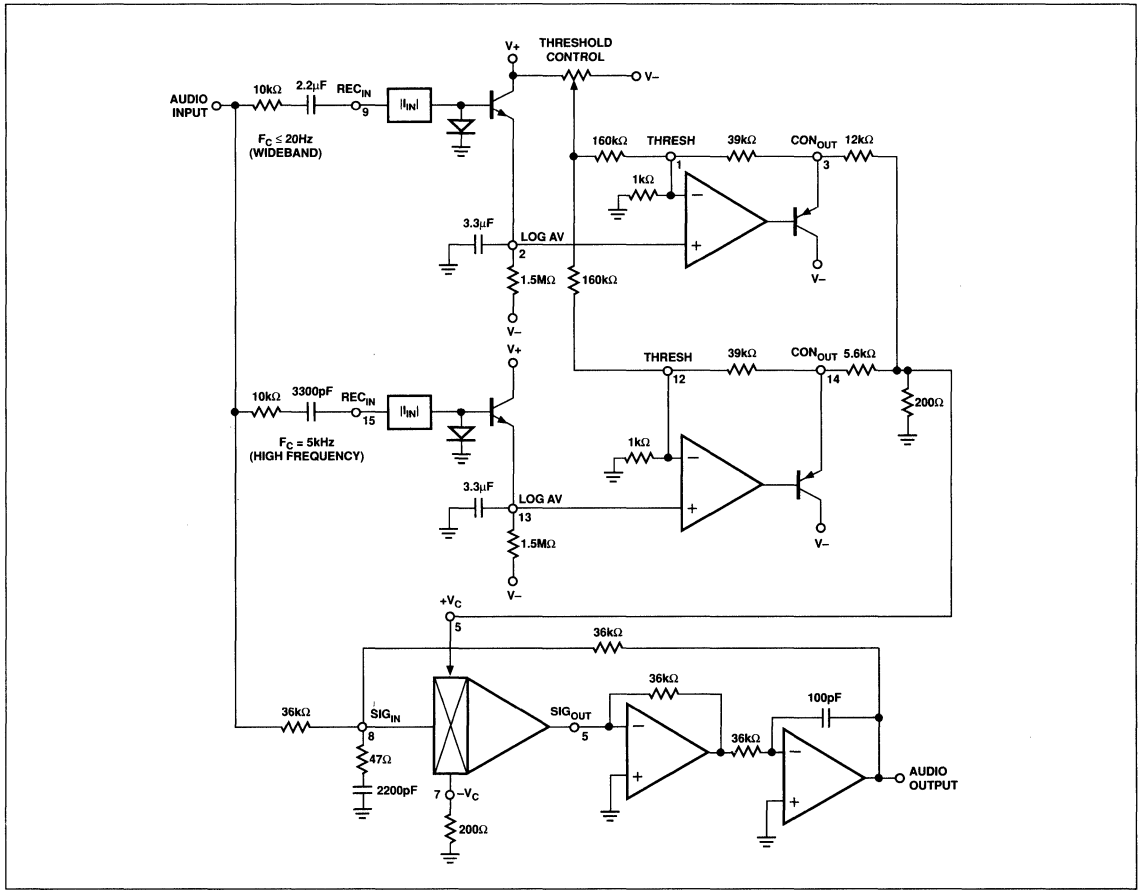

FIGURE 12: *Dynamic Noise Filter Circuit*

DYNAMIC FILTER

Figure 12 shows a control circuit for a dynamic filter capable of single ended (non-encode/decode) noise reduction. Such circuits usually suffer from a loss of high-frequency content at low signal levels because their control circuits detect the absolute amount of highs present in the signal. This circuit, however, measures wideband level as well as high-frequency band level to produce a composite control signal combined in a 1:2 ratio respectively. The upper detector senses wideband signals with a cutoff of 20Hz while the lower detector has a 5kHz cutoff to sense only high-frequency band signals. This approach allows very good noise masking with a minimum loss of "highs" when the signal level goes below the threshold.

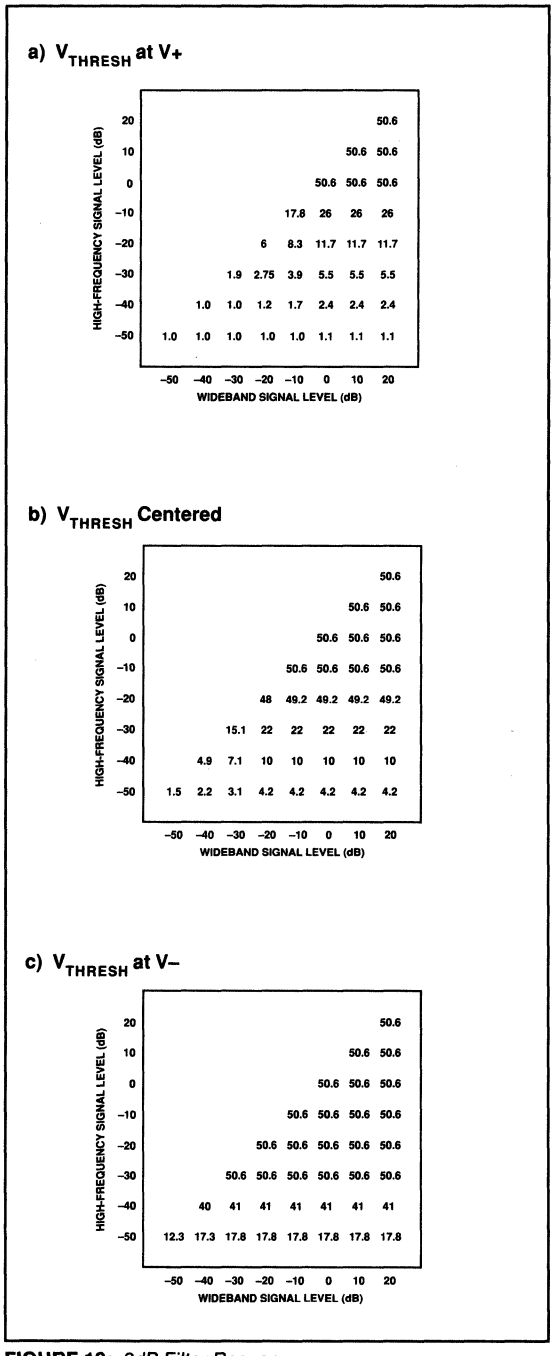

FIGURE 13: *3dB Filter Response*

Figures 13a-c show the filter's 3dB frequency response with the threshold potentiometer at V+, centered, and V−. Data was taken by applying a 300Hz signal to the wideband detector and a 20kHz signal to the high-frequency band detector simultaneously. These figures correspond to filter characteristics for 50dB, 70dB and 90dB dynamic range program source material, respectively. The system could thus treat signals from anything ranging from 1/4" magnetic tape to high-performance compact disc players.

Note that in Figure 13a the control circuit is designed so that the minimum cutoff frequency is about 1kHz. This occurs as the control circuit detects the noise floor of the source material.

Dynamic filtering limits the signal bandwidth to less than 1kHz unless enough highs are detected in the signal to cover the noise floor in the mid- and high-frequency range. In this case the filter opens to pass more of the audio band as more highs are detected. The filter's bandwidth can extend to 50kHz with a nominal signal level at the input. At other signal levels with varying high-frequency content, the filter will close to the required bandwidth. Here, noise outside the band is removed while the perceived noise is masked by other signals within the band. Even in this system, however, a certain amount of mid- and high-frequency components will be lost, especially during transients at very low signal levels. This circuit does not address low frequency noise such as "hum" and "rumble."

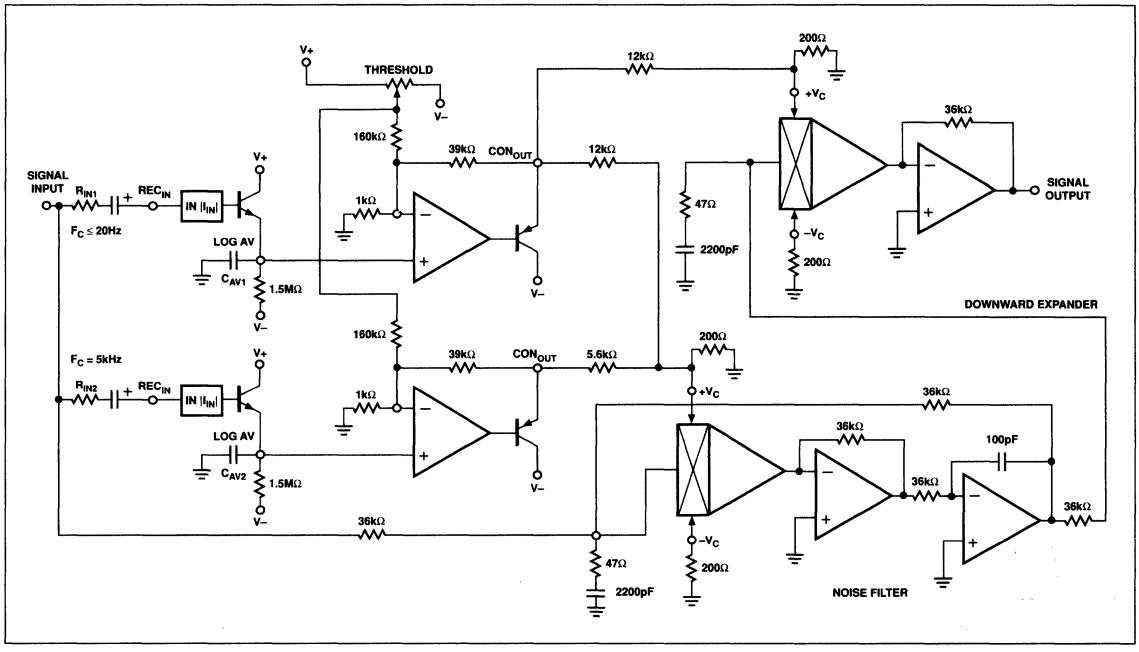

FIGURE 14: *Dynamic Filter with Downward Expander*

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DYNAMIC FILTER WITH DOWNWARD EXPANDER

A composite single-ended noise reduction system can be realized by a combination of dynamic filtering and a downward expander. As shown in Figure 14, the output from the wideband detector can also be connected to the $+V_C$ control port of the second VCA which is connected in series with the sliding filter. This will act as a downward expander with a threshold that tracks that of the filter. Although both of these techniques are used for noise reduction, each alone will pass appreciable amounts of noise under some conditions. When used together, both contribute distinct advantages while compensating for each other's deficiencies.

Downward expansion uses a VCA controlled by the level detector. This section maintains dynamic range integrity for all levels above the user adjustable threshold level. As the input level decreases below the threshold, gain reduction occurs at an increasing rate (see Figure 15). This technique reduces audible noise in fade outs or low level signal passages by keeping the standing noise floor well below the program material.

This technique by itself is less effective for signals with predominantly low frequency content such as a bass solo where wideband frequency noise would be heard at full level. Also, since the level detector has a time constant for signal averaging, percussive material can modulate the noise floor causing a "pumping" or "breathing" effect.

The dynamic filter and downward expander techniques used together can be employed more subtly to achieve a given level of noise reduction than would be required if used individually. Up to 30dB of noise reduction can be realized while preserving the crisp highs with a minimum of transient side effects.

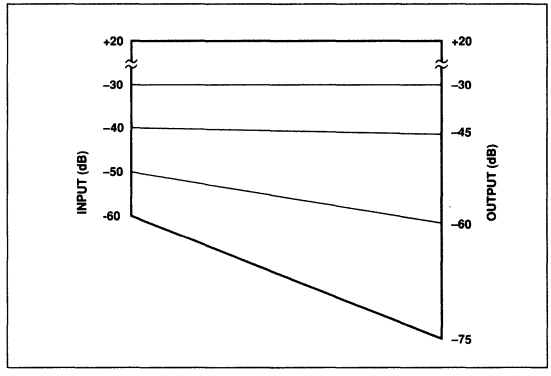

FIGURE 15: *Typical Downward Expander I/O Characteristics at –30dB Threshold Level (1:1.5 Ratio)*

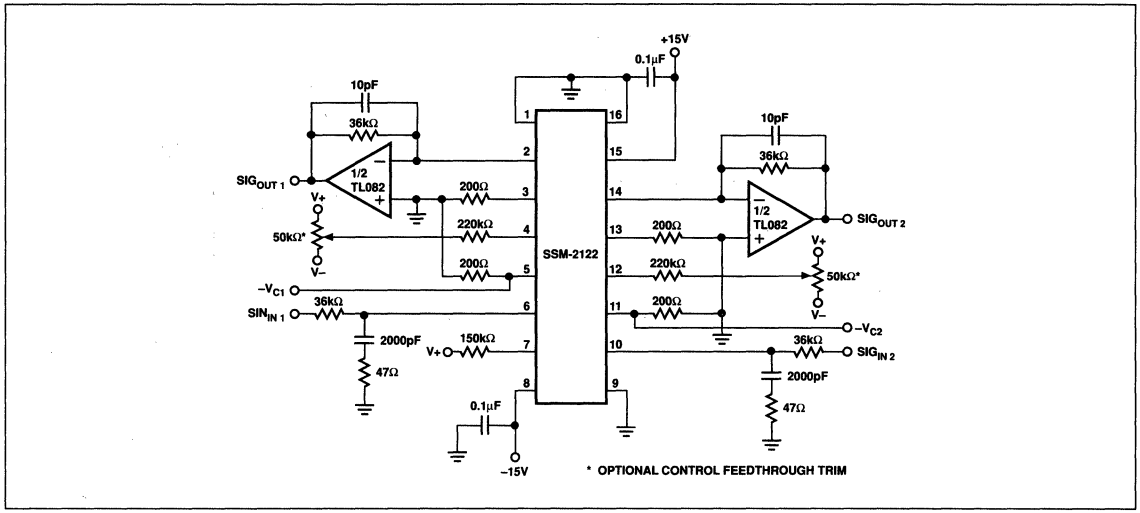

FIGURE 16: *SSM-2122 Basic Connection (Control Ports at 0V)*

FADER AUTOMATION

The SSM-2120 can be used in fader automation systems to serve two channels. The inverting control port is connected through an attenuator to the VCA control voltage source. The noninverting control port is connected to a control circuit (such as Figure 6) which senses the input signal level to the VCA. Above the threshold voltage, which can be set quite low (for example –60dBV), the VCA operates at its programmed gain. Below this threshold the VCA will downward expand at a rate determined by the $+V_C$ control port attenuator. By keeping the release time constant in the 10 to 25ms range, the modulation of the VCA standing noise floor (–80dB at unity-gain), can be kept inaudibly low.

The SSM-2300 8-channel multiplexed sample-and-hold IC makes an excellent controller for VCAs in automation systems.

Figure 16 shows the basic connection for the SSM-2122 operating as a unity-gain VCA with its noninverting control ports grounded and access to the inverting control ports. This is typical for fader automation applications. Since this device is a pinout option of the SSM-2120, the VCAs will behave exactly as described earlier in the VCA section.

The SSM-2122 can also be used with two or more op amps to implement complex voltage-controlled filter functions. Biquad and state-variable two-pole filters offering lowpass, bandpass and highpass outputs can be realized. Higher order filters can also be formed by connecting two or more such stages in series.

Dolby Pro-Logic Surround Matrix Decoder

SSM-2125/SSM-2126

FEATURES

- **Noise Generator and Autobalance Circuits are Contained On-Chip**
- **Autobalance On/Off Control**
- **4-Channel Pro-Logic and Dolby 3 (Surround Channel Defeat) Modes Available**
- **Selectable Center Channel Modes—Normal, Wideband, Phantom, Off**
- **Direct Path Bypass (Normal 2-Channel Stereo Mode)**
- **Wide Channel Separation**
  - **Center to Left, Right Channels—35 dB min (SSM-2125)**
  - **Any Channel to Another—25 dB min (SSM-2126)**
- **Wide Dynamic Range—103 dB typ**
- **Low Total Harmonic Distortion—0.02% typ**
- **Available in a 48-Pin Plastic DIP**
- **CMOS and TTL Compatible Control Logic**

APPLICATIONS

- **Direct View and Projection TV**
- **Integrated A/V Amplifiers**
- **Laserdisc and CD-V Players**
- **Video Cassette Recorders**
- **Stand-Alone Surround Decoders**
- **Home Satellite Receiver/Descramblers**

GENERAL DESCRIPTION

The SSM-2125 and SSM-2126 are Dolby* Pro-Logic Surround Decoders developed to provide multichannel outputs from Dolby Surround encoded stereo sources.

Over 2000 major films and an increasing number of broadcasts are available in Dolby Surround. Surround encoding is preserved in the stereo audio tracks of normal video discs, video cassettes, and television broadcasts, permitting the decoding to multichannel audio in the home.

Major design considerations of the SSM-2125/SSM-2126 are excellent audio performance and a high level of integration. In addition to the Adaptive Matrix and Center Mode Control, also included on-chip are the Automatic Balance Control and Noise Generator functions. A complete Pro-Logic system can be realized using the SSM-2125/SSM-2126 and few external components. Using SSM's extensive experience in the design of professional audio integrated circuits, the SSM-2125/SSM-2126 offers typical 103 dB dynamic range and 0.025% THD. A direct path bypass mode allows normal stereo operation with high fidelity without the need for external switching or parallel signal paths.

The SSM-2125 is a premium grade that is selected to a minimum channel separation specification of 35 dB for the center to left and right channels, and 25 dB for the remaining channels. The standard grade, the SSM-2126, provides minimum channel separation of 25 dB from any channel to another.

The SSM-2125/SSM-2126 is available only to licensees of Dolby Licensing Corporation, San Francisco, California, from whom licensing and application information must be obtained.

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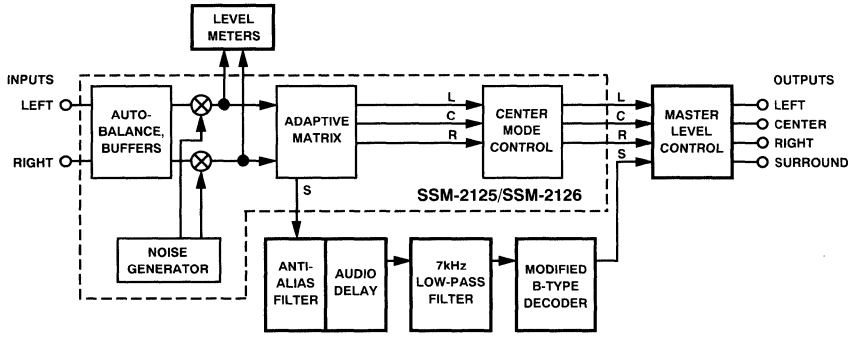
FUNCTIONAL BLOCK DIAGRAM



*Dolby is a registered trademark of Dolby Laboratories Licensing Corporation, San Francisco, California.

SSM-2125/SSM-2126—SPECIFICATIONS (V_S = ±6 V, T_A = +25°C, V_{IN} = 0 dBd at 1 kHz,[1] Center Mode Control: Wide, unless otherwise noted.)

Parameter	Symbol	Conditions	SSM-2125 Min	SSM-2125 Typ	SSM-2125 Max	SSM-2126 Min	SSM-2126 Typ	SSM-2126 Max	Units
CHANNEL SEPARATION									
Center		C Input; R, L Outputs	35	48		25	35		dB
		C Input; S Output	25	35		25	35		dB
Right		R Input; L, C, S Outputs	25	35		25	35		dB
Left		L Input; C, R, S Outputs	25	35		25	35		dB
Surround		S Input; L, R, C Outputs	25	35		25	35		dB
CHANNEL OUTPUT LEVEL		V_{IN} = 0 dB; L, R, C, S Output			±0.5			±0.5	dBd
TOTAL HARMONIC DISTORTION	THD	All Channels		0.02	0.1		0.02	0.1	%
SIGNAL-TO-NOISE RATIO	SNR	V_{IN} = 0 V, CCIR2K/ARM All Channels	−83	−87		−80	−87		dBd
HEADROOM	HR	Clipping = 3% THD All Channels	15	16		15	16		dBd
BYPASS MODE DYNAMIC RANGE		Clipping to Noise Floor		104			104		dB
NOISE SOURCE OUTPUT LEVEL		All Channels		−13.5			−13.5		dBd
NOISE SOURCE OUTPUT LEVEL MATCHING		Any Channel to Another		1			1		dB
AUTOBALANCE CAPTURE RANGE			±3	±3.8	±6		±3.8		dB
LOGIC THRESHOLD HI		Relative to L_{REF}	+2.4			+2.4			V
LO					+0.8			+0.8	V
OPERATING SUPPLY VOLTAGE	V_S	Single Supply		+12			+12		V
		Dual Supply		±6			±6		V
SUPPLY CURRENT	I_{SY}	No Input Signal		40	50		40	50	mA
INPUT IMPEDANCE	Z_{IN}	L, R Inputs		5			5		kΩ
OUTPUT IMPEDANCE	Z_{OUT}	L, R, C, S Outputs		600			600		Ω

NOTE
[1]0 dBd = 500 mV rms Dolby level output at any channel; Left and Right inputs: 500 mV rms (0 dBd); Center input: L = R = 354 mV rms (−3 dBd); Surround input: L = −R = 354 mV rms (−3 dBd).

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . +16 V or ±8 V
Logic Inputs . . . . . V+ to V−
Storage Temperature Range . . . . . −55°C to +125°C
Operating Temperature Range . . . . . −20°C to +70°C
Junction Temperature . . . . . +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C
Thermal Resistance[1]
θ_{JA} . . . . . 38°C/W
θ_{JC} . . . . . 14°C/W

NOTE
[1]θ_{JA} is specified for worst case mounting conditions, i.e., device in socket.

ORDERING GUIDE

Model	Temperature Range	Package Option
SSM2125XXXP*	−20°C to +70°C	48-Pin P-DIP
SSM2126XXXP*	−20°C to +70°C	48-Pin P-DIP

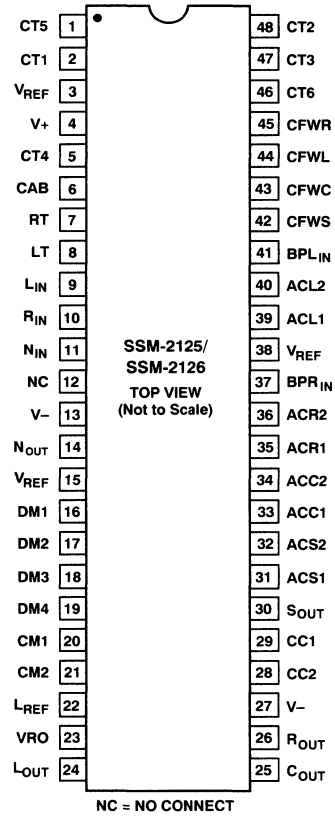
NOTES
[1]For outline information see Package Information section.
[2]The SSM-2125/SSM-2126 is available only to licensees of Dolby Laboratories. Each customer will be assigned a special part number for ordering purposes. Contact local ADI sales office for further details.

Table I. External Component List

Component	Value	Tolerance*	Comment (Noncritical Unless Otherwise Noted)
C1	0.1 μF		
C2	0.1 μF		
C3	680 pF		
C4	0.1 μF		
C5	0.1 μF		
C6	680 pF		
C7	4.7 μF	20%	Standard Electrolytic
C8	0.22 μF		
C9	0.22 μF		
C10	0.33 μF		Film
C11	0.33 μF		Film
C12	0.33 μF		Film
C13	0.33 μF		Film
C14	22 nF		Film
C15	22 nF		Film
C16	22 nF		Film
C17	22 nF		Film
C18	0.1 μF		
C19	4.7 μF	20%	Standard Electrolytic
C20	0.22 μF		
C21	0.22 μF		
C22	10 μF	20%	Standard Electrolytic
C23	—	—	Not Needed
C24	10 nF		
C25	10 nF		
C26	10 nF		
C27	100 μF	≥100 μF	Standard Electrolytic
C28	0.1 μF		
C29**	100 μF	≥100 μF	Standard Electrolytic
C30**	0.1 μF		
C31	100 μF	≥100 μF	Standard Electrolytic
C32	0.1 μF		
R1	15 kΩ	5%	
R2	47 kΩ	5%	
R3	15 kΩ	5%	
R4	47 kΩ	5%	
R5	7.5 kΩ	5%	
R6	7.5 kΩ	5%	
R7	—	—	Not Needed
R8	—	—	Not Needed
R9	22 kΩ	5%	
R10	22 kΩ	5%	
R11	10 MΩ	5%	
R12	22 kΩ	5%	

NOTES
*10% unless otherwise indicated.
**Used only in Dual Supply Application Circuit.

PIN CONNECTIONS



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PIN DESCRIPTION

Pin #	Name	Function
1	CT5	Long Time Constant, C/S
2	CT1	Short Time Constant, L/R Comparators
3	V_{REF}	Reference Voltage: Ground or Pseudoground
4	V+	Positive Supply
5	CT4	Short Time Constant, C/S Comparators
6	CAB	Autobalance Time Constant
7	RT	Buffered, Autobalanced Right Channel Signal
8	LT	Buffered, Autobalanced Left Channel Signal
9	L_{IN}	Left Channel Input
10	R_{IN}	Right Channel Input
11	N_{IN}	Filtered Noise Input
12	NC	Do Not Connect
13	V−	Negative Supply (Ground in Single Supply)
14	N_{OUT}	Noise Output
15	V_{REF}	Reference Voltage: Ground or Pseudoground
16	DM1	Digital Operating-Mode Control Input
17	DM2	Digital Operating-Mode Control Input
18	DM3	Digital Operating-Mode Control Input
19	DM4	Digital Operating-Mode Control Input
20	CM1	Digital Center-Mode Control Input
21	CM2	Digital Center-Mode Control Input
22	L_{REF}	Logic Reference Voltage (Threshold = L_{REF} + 1.4 V)
23	VRO	V_{REF} Out—Pseudoground Output
24	L_{OUT}	Left Channel Output
25	C_{OUT}	Center Channel Output
26	R_{OUT}	Right Channel Output
27	V−	Negative Supply (Ground in Single Supply)
28	CC2	Center Normal-Mode Filter Input (Z = 15 kΩ)
29	CC1	Center Normal-Mode Filter Output
30	S_{OUT}	Surround Channel Output
31	ACS1	Surround Channel Steering Signal AC Coupling and High-Pass Filter
32	ACS2	Surround Channel Steering Signal AC Coupling and High-Pass Filter
33	ACC1	Center Channel Steering Signal AC Coupling and High-Pass Filter
34	ACC2	Center Channel Steering Signal AC Coupling and High-Pass Filter
35	ACR1	Right Channel Steering Signal AC Coupling and High-Pass Filter
36	ACR2	Right Channel Steering Signal AC Coupling and High-Pass Filter
37	BPR_{IN}	Filtered Right Channel Input to Steering Signal Generator
38	V_{REF}	Reference Voltage: Ground or Pseudoground
39	ACL1	Left Channel Steering Signal AC Coupling and High-Pass Filter
40	ACL2	Left Channel Steering Signal AC Coupling and High-Pass Filter
41	BPL_{IN}	Filtered Left Channel Input to Steering Signal Generator
42	CFWS	Surround Channel Full-Wave Rectifier Low-Pass Filter
43	CFWC	Center Channel Full-Wave Rectifier Low-Pass Filter
44	CFWL	Left Channel Full-Wave Rectifier Low-Pass Filter
45	CFWR	Right Channel Full-Wave Rectifier Low-Pass Filter
46	CT6	Short Time Constant, C/S
47	CT3	Short Time Constant, L/R
48	CT2	Long Time Constant, L/R

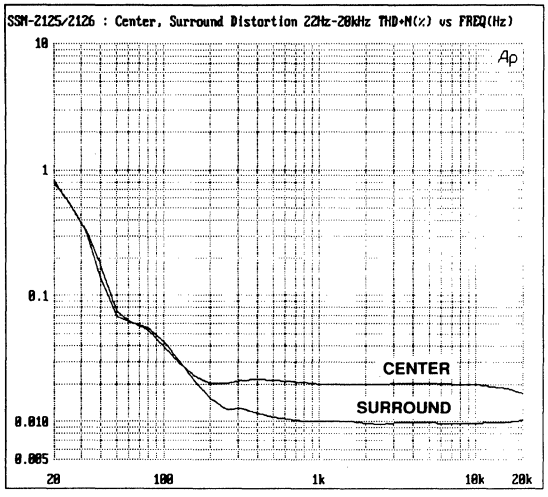

Figure 1. THD+N vs. Frequency, Center and Surround Channels (V_{IN} = 0 dBd, R_L = 100 kΩ)*

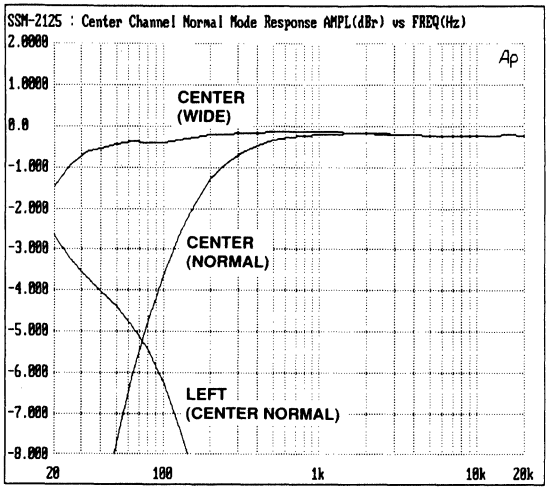

Figure 3. Bass-Splitting Filter Response (Center Channel Normal and Wide Modes)

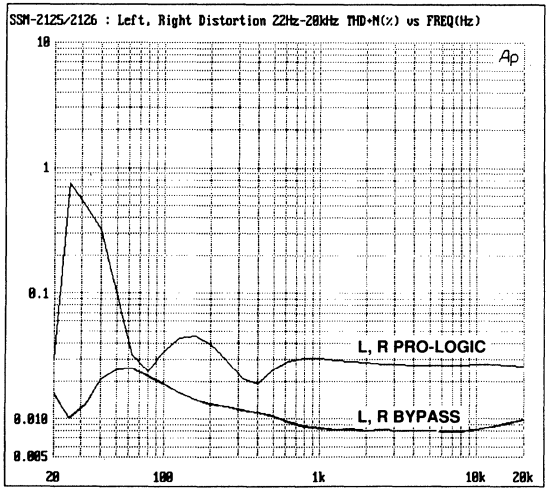

Figure 2. THD+N vs. Frequency, Left and Right Channels (V_{IN} = 0 dBd, R_L = 100 kΩ)*

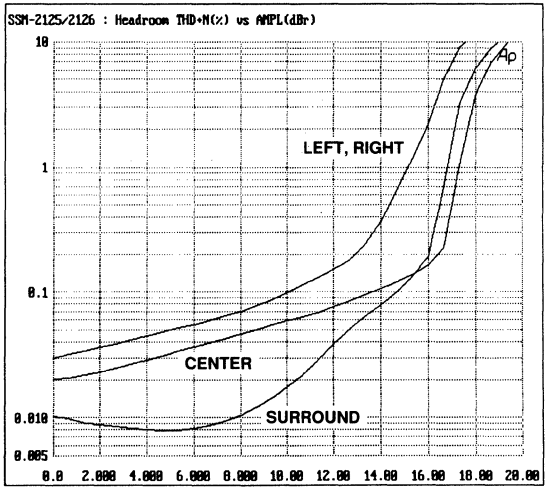

Figure 4. Headroom THD+N vs. Amplitude (0 dBr = 0 dBd = 500 mV rms)

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*80 kHz low-pass filter used for Figures 1 and 2.

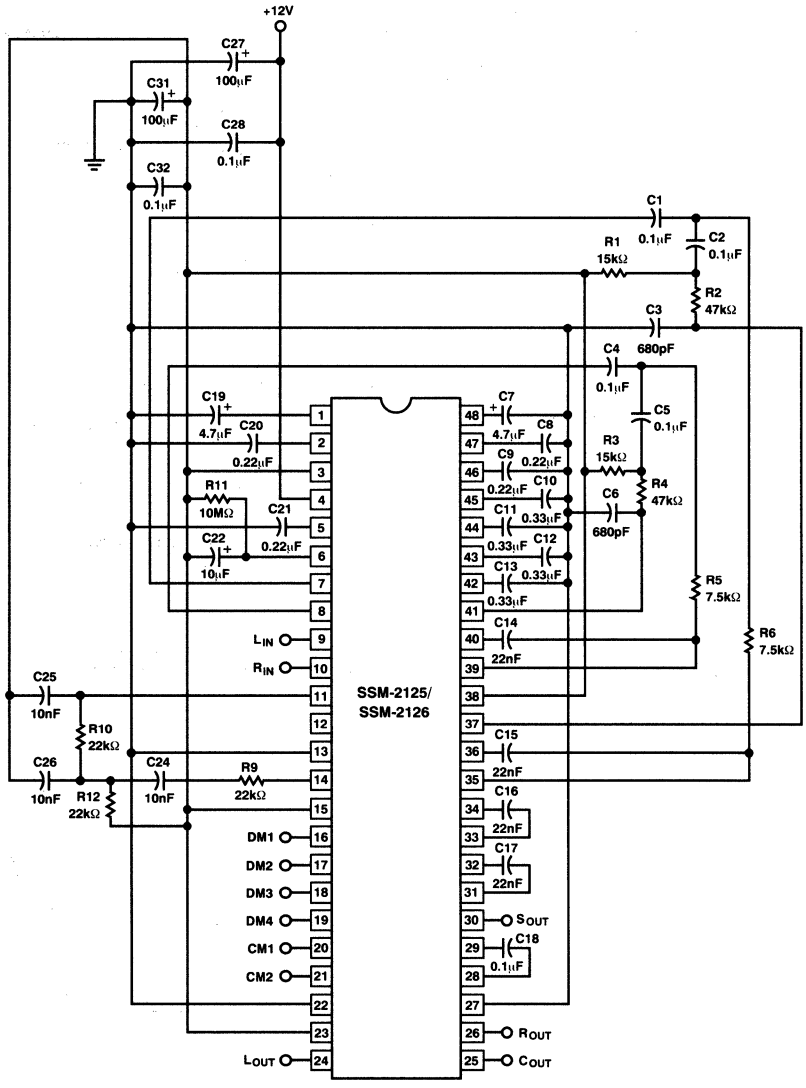

Figure 5. Single Supply Application Circuit

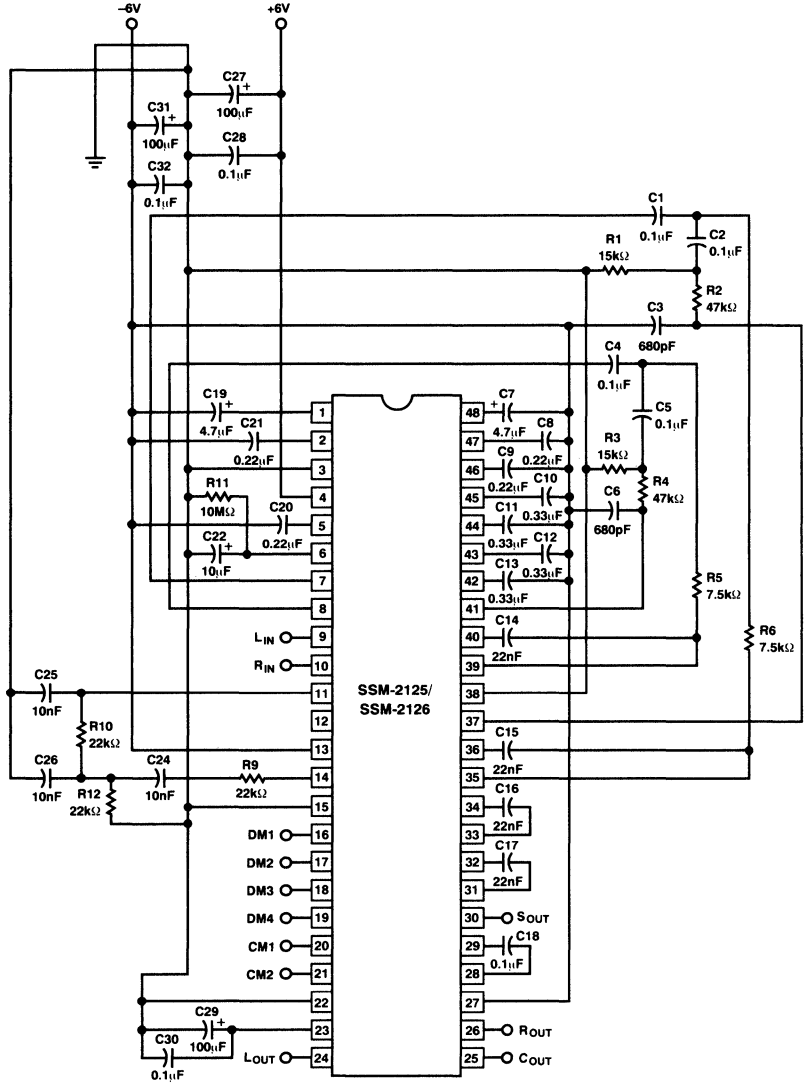

Figure 6. Dual Supply Application Circuit

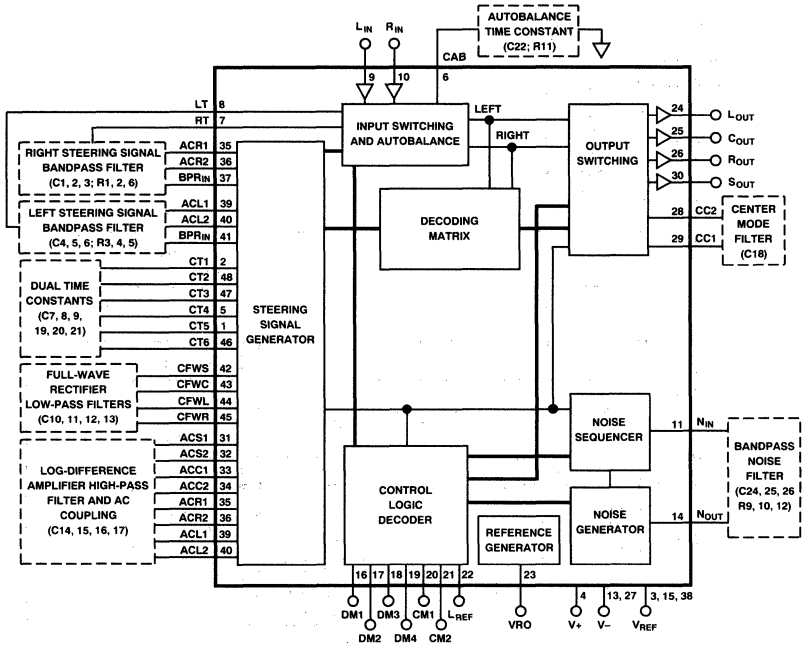

Figure 7. SSM-2125/SSM-2126 Block Diagram Showing External Component Functions

APPLICATIONS INFORMATION

POWER SUPPLIES

The SSM-2125/SSM-2126 is designed to use either a dual ±6 V or single +12 V supply, with a tolerance of ±10%. Internal reference points on the IC and a 6 V reference, generated on-chip, are brought to external pins. When operated in dual supply mode, the reference inputs (labeled V_{REF}) are connected to the external ground. In single supply mode, the internal 6 V reference (labeled VRO) is wired to the V_{REF} pins, providing a pseudoground reference. In either mode, the internal reference VRO should be decoupled with a 100 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor.

Dual supply mode offers the highest fidelity operation and eliminates the necessity for input and output decoupling capacitors. All signals are ground referenced in dual supply mode, allowing dc coupling of the inputs and outputs. Additionally, the power on settling time is reduced when operating with dual supplies.

In single supply mode, decoupling capacitors are required, as the signals are referenced to the +6 V pseudoground reference. Any noise introduced onto the V_{REF} line will appear at the output, so careful decoupling of the reference is required to maintain excellent noise and distortion performance. The 100 µF V_{REF} decoupling capacitors should be placed close to the VRO pin (Pin 23), and 0.1 µF capacitors close to each V_{REF} pin.

DOLBY LEVEL

The discrete implementation of Dolby Pro-Logic Surround used a Dolby level of 500 mV. To maintain high audio quality and excellent signal-to-noise ratio, the SSM-2125/SSM-2126 was designed to operate with a 500 mV Dolby level. With this level, the SSM-2125/SSM-2126 provides 87 dBd SNR (CCIR2K/ARM) and 16 dB of headroom. In addition, the SSM-2125/SSM-2126 is capable of operation to the Pro-Logic specification at a Dolby level of 300 mV, with the result of reduced SNR and increased headroom. At the 300 mV level, SNR is typically 83 dBd with 20 dB of headroom. Either way, total dynamic range of the device is 103 dB (0 dBd = 500 mV).

AUTOBALANCE

Left and right signals with an imbalance less than ±3.8 dB will activate the autobalance circuitry when DM3 = 1. Once activated, the circuit will correct up to 4 dB of balance error. Autobalance is available in both the Pro-Logic and stereo bypass modes. When autobalance is OFF, the autobalance VCAs are bypassed.

NOISE GENERATOR AND SEQUENCING

The SSM-2125/SSM-2126 noise source is best described as white noise passed through a 0.2 Hz comb filter and a 10 kHz low-pass filter. Thus, the noise is comprised of separate equal-amplitude peaks spaced at 0.2 Hz apart, as shown in Figure 8. Figure 9 shows overall frequency response of the filtered noise source.

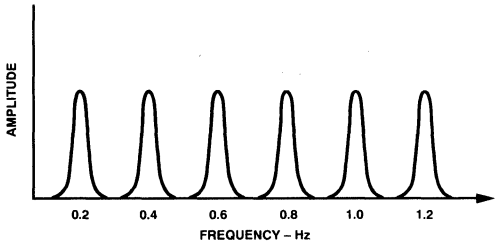

Figure 8. Comb-Filtered Noise Source Characteristics

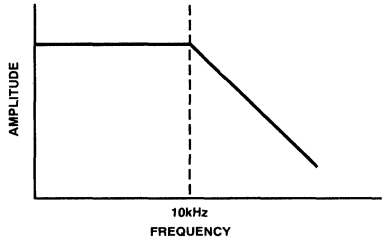

Figure 9. Overall Frequency Response of Filtered Noise Source

For systems that are not microprocessor controlled, Figure 10 suggests one option to implement automatic noise sequencing using standard logic. The CD4060 (or equivalent), although only partially used, was selected since it contains a clock and 2-bit binary counter on-chip. The timing interval is set by:

$$f = \frac{1}{2.2\,R_1\,C_3}$$

where $2R_1 < R_2 < 10R_1$.

The values shown in Figure 10 will provide a frequency of 2.9 Hz. One half of a CD4556 can be used to drive LED panel indicators if desired, as shown.

FUNCTIONAL MODES

The SSM-2125/SSM-2126 uses a positive logic system, whereby a voltage greater than 2.4 V above L_{REF} is considered a "1," and voltage levels between L_{REF} and 0.8 V are considered a "0." Tables II and III provide truth tables for logic inputs DM1 through DM4, and CM1 and CM2. "Dolby 3" mode, which disables surround steering, is available as shown. Normal operating mode for the decoder is with a "1" on all logic inputs. This provides 4-channel logic, autobalance ON, and center normal mode. Internal pullups will automatically set the chip into this state if the inputs are left unconnected.

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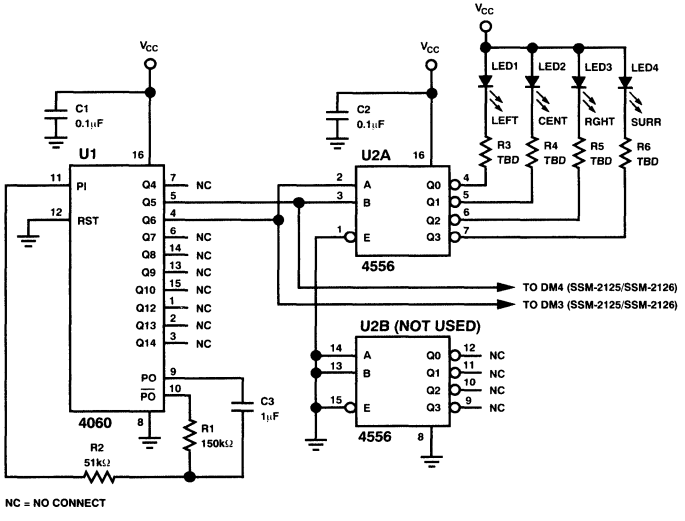


Figure 10. Automatic Noise Sequencing Circuit

Table II. Control States for DM1–DM4

DM1	DM2	DM3	DM4	Operating State
1	1	1	1	Dolby 4-Channel ("Pro-Logic"), Autobalance On
1	1	0	1	Dolby 4-Channel ("Pro-Logic"), Autobalance Off
1	0	1	1	Dolby 3-Channel ("Dolby 3"), Autobalance On
1	0	0	1	Dolby 3-Channel ("Dolby 3"), Autobalance Off
0	1	1	1	Surround Channel Noise
0	1	1	0	Right Channel Noise
0	1	0	1	Center Channel Noise
0	1	0	0	Left Channel Noise
0	0	X	1	Mute
0	0	1	0	Stereo Bypass, Autobalance On
0	0	0	0	Stereo Bypass, Autobalance Off

Table III. Center Channel Functional Modes

CM1	CM2	Mode
0	0	Center Channel Off
0	1	Center Channel Wideband
1	0	Phantom Center Channel
1	1	Normal Center Mode

High Common-Mode Rejection Differential Line Receiver

SSM-2141

FEATURES

- **High Common-Mode Rejection**
  - **DC ..... 100dB Typ**
  - **60Hz ..... 100dB Typ**
  - **20kHz ..... 70dB Typ**
  - **40kHz ..... 62dB Typ**
- **Low Distortion ..... 0.001% Typ**
- **Fast Slew Rate ..... 9.5V/μs Typ**
- **Wide Bandwidth ..... 3MHz Typ**
- **Low Cost**
- **Complements SSM-2142 Differential Line Driver**

APPLICATIONS

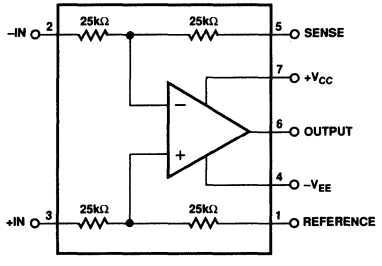
- **Line Receivers**
- **Summing Amplifiers**
- **Buffer Amplifiers – Drives 600Ω Load**

ORDERING INFORMATION

PACKAGE	OPERATING TEMPERATURE RANGE
PLASTIC 8-PIN	
SSM2141P	XIND*

*XIND = $-40°C \leq T_A \leq +85°C$

FUNCTIONAL DIAGRAM



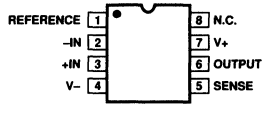
GENERAL DESCRIPTION

The SSM-2141 is an integrated differential amplifier intended to receive balanced line inputs in audio applications requiring a high level of noise immunity and optimum common-mode rejection. The SSM-2141 typically achieves 100dB of common-mode rejection (CMR), whereas implementing an op amp with four off-the-shelf precision resistors will typically achieve only 40dB of CMR – inadequate for high-performance audio.

The SSM-2141 achieves low distortion performance by maintaining a large slew rate of 9.5V/μs and high open-loop gain. Distortion is less than 0.002% over the full audio bandwidth. The SSM-2141 complements the SSM-2142 balanced line driver. Together, these devices comprise a fully integrated solution for equivalent transformer balancing of audio signals without the problems of distortion, EMI fields, and high cost.

Additional applications for the SSM-2141 include summing signals, differential preamplifiers, and 600Ω low distortion buffer amplifiers.

PIN CONNECTIONS



8-PIN PLASTIC MINI-DIP (P-Suffix)

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Input Voltage (Note 1) ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P Package ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature ..... +150°C
Operating Temperature Range ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
8-Pin Plastic DIP (P)	103	43	°C/W

NOTES:
1. For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package.

ELECTRICAL CHARACTERISTICS at V_S = ±18V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2141 MIN	SSM-2141 TYP	SSM-2141 MAX	UNITS
Offset Voltage	V_{OS}	V_{CM} = 0V	–1000	25	1000	µV
Gain Error		No Load, V_{IN} = ±10V, R_S = 0Ω	–	0.001	0.01	%
Input Voltage Range	IVR	(Note 1)	±10	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±10V	80	100	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±6V to ±18V	–	0.7	15	µV/V
Output Swing	V_O	R_L = 2kΩ	±13	±14.7	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted To Ground	+45/–15	–	–	mA
Small-Signal Bandwidth (–3dB)	BW	R_L = 2kΩ	–	3	–	MHz
Slew Rate	SR	R_L = 2kΩ	6	9.5	–	V/µs
Total Harmonic Distortion	THD	R_L = 100kΩ R_L = 600Ω	– –	0.001 0.01	– –	%
Capacitive Load Drive Capability	C_L	No Oscillation	–	300	–	pF
Supply Current	I_{SY}	No Load	–	2.5	3.5	mA

NOTE:
1. Input voltage range guaranteed by CMR test.

Specifications subject to change; consult latest data sheet.

ELECTRICAL CHARACTERISTICS at V_S = ±18V, –40°C ≤ T_A ≤ +85°C.

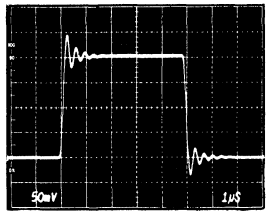
PARAMETER	SYMBOL	CONDITIONS	SSM-2141 MIN	SSM-2141 TYP	SSM-2141 MAX	UNITS
Offset Voltage	V_{OS}	V_{CM} = 0V	–2500	200	2500	µV
Gain Error		No Load, V_{IN} = ±10V, R_S = 0Ω	–	0.002	0.02	%
Input Voltage Range	IVR	(Note 1)	±10	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±10V	75	90	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±6V to ±18V	–	1.0	20	µV/V
Output Swing	V_O	R_L = 2kΩ	±13	±14.7	–	V
Slew Rate	SR	R_L = 2kΩ	–	9.5	–	V/µs
Supply Current	I_{SY}	No Load	–	2.6	4.0	mA

NOTE:
1. Input voltage range guaranteed by CMR test.

Specifications subject to change; consult latest data sheet.

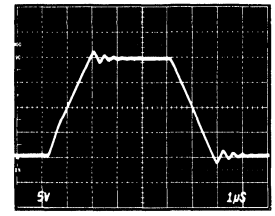
TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

SMALL-SIGNAL TRANSIENT RESPONSE



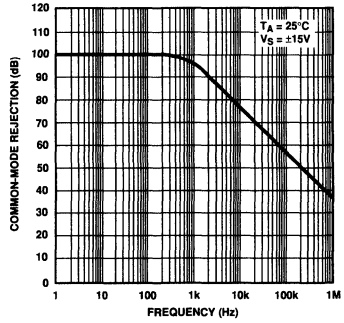
T_A = +25°C
V_S = ±15V

LARGE-SIGNAL TRANSIENT RESPONSE

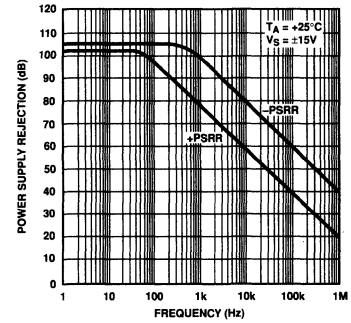


T_A = +25°C
V_S = ±15V

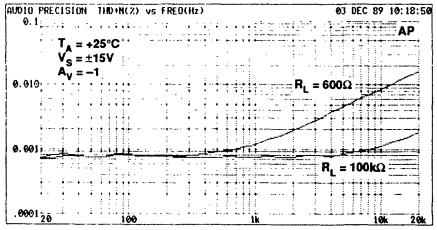
COMMON-MODE REJECTION vs FREQUENCY



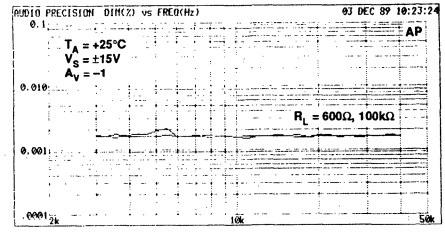
POWER SUPPLY REJECTION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY



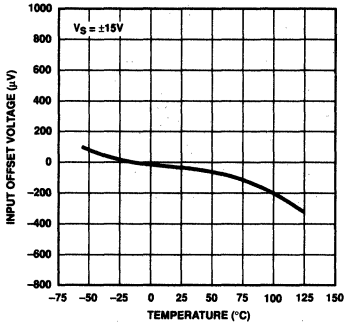
DYNAMIC INTERMODULATION DISTORTION vs FREQUENCY



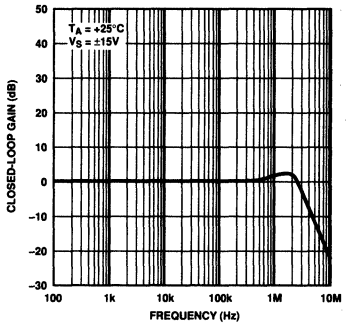
7

TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

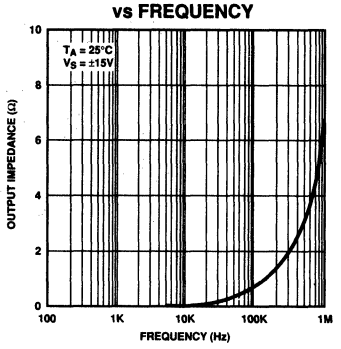
INPUT OFFSET VOLTAGE vs TEMPERATURE



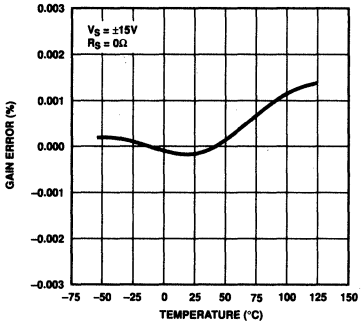
CLOSED-LOOP GAIN vs FREQUENCY



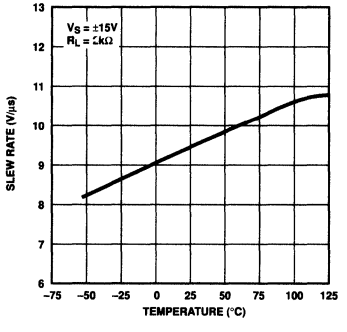
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



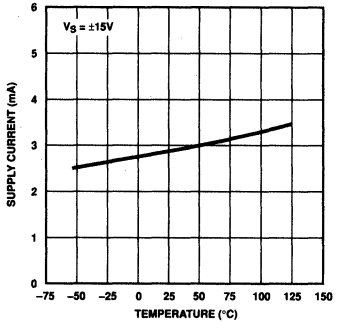
GAIN ERROR vs TEMPERATURE



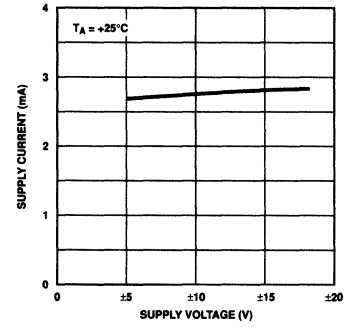
SLEW RATE vs TEMPERATURE



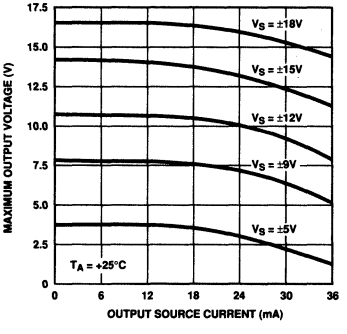
SUPPLY CURRENT vs TEMPERATURE



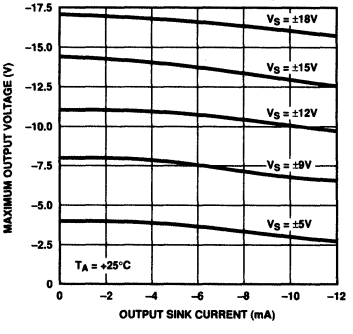
SUPPLY CURRENT vs SUPPY VOLTAGE



MAXIMUM OUTPUT VOLTAGE vs OUTPUT CURRENT (SOURCE)

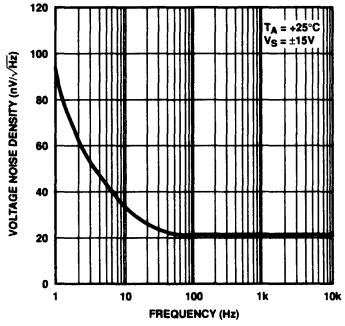


MAXIMUM OUTPUT VOLTAGE vs OUTPUT CURRENT (SINK)

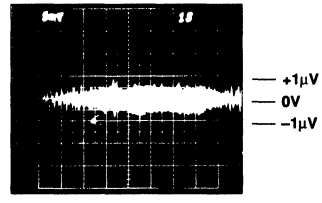


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

VOLTAGE NOISE DENSITY vs FREQUENCY

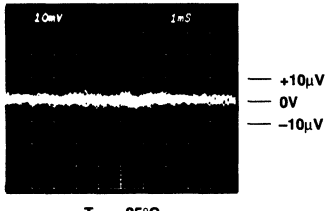


LOW FREQUENCY VOLTAGE NOISE



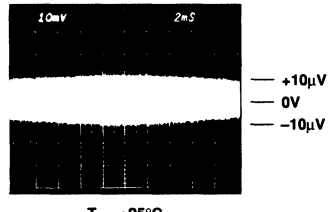
0.1 TO 10Hz PEAK-TO-PEAK NOISE

VOLTAGE NOISE FROM 0 TO 1kHz



T_A = +25°C
V_S = ±15V
NOTE: EXTERNAL AMPLIFIER GAIN = 1000;
THEREFORE, VERTICAL SCALE = 10μV/DIV.

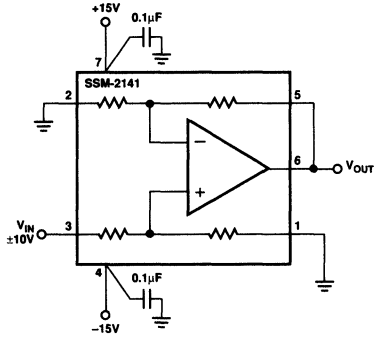
VOLTAGE NOISE FROM 0 TO 10kHz



T_A = +25°C
V_S = ±15V
NOTE: EXTERNAL AMPLIFIER GAIN = 1000;
THEREFORE, VERTICAL SCALE = 10μV/DIV.

7

SLEW RATE TEST CIRCUIT



APPLICATIONS INFORMATION

The SSM-2141 represents a versatile analog building block. In order to capitalize on fast settling time, high slew rate, and high CMR, proper decoupling and grounding techniques must be employed. For decoupling, place 0.1μF capacitor located within close proximity from each supply pin to ground.

MAINTAINING COMMON-MODE REJECTION

In order to achieve the full common-mode rejection capability of the SSM-2141, the source impedance must be carefully controlled. Slight imbalances of the source resistance will result in a degradation of DC CMR – even a 5Ω imbalance will degrade CMR by 20dB. Also, the matching of the reactive source impedance must be matched in order to preserve theCMRR over frequency.

APPLICATION CIRCUITS

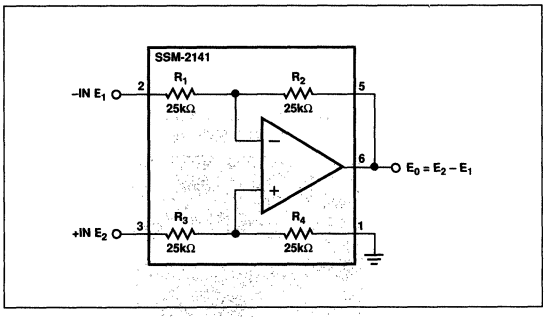


FIGURE 1: *Precision Difference Amplifier. Rejects Common-Mode Signal =* $\frac{[E_1 + E_2]}{2}$ *by 100dB*

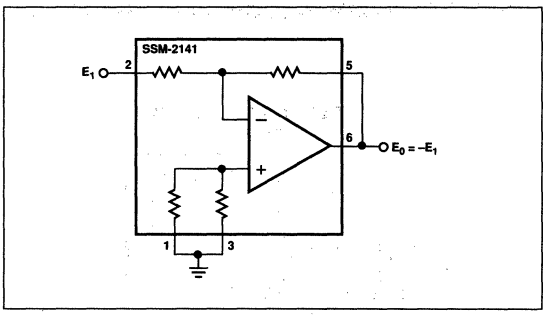


FIGURE 2: *Precision Unity-Gain Inverting Amplifier*

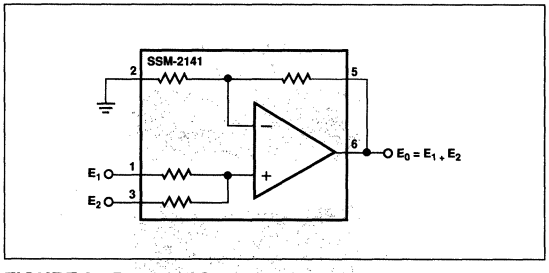


FIGURE 3: *Precision Summing Amplifier*

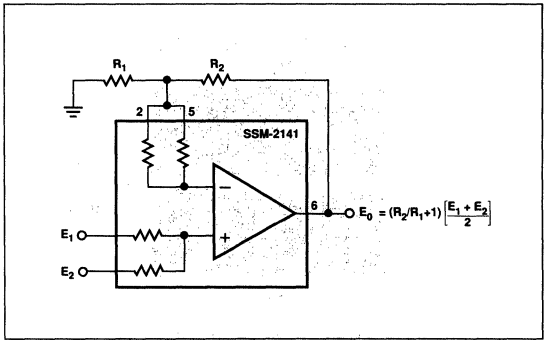


FIGURE 4: *Precision Summing Amplifier with Gain*

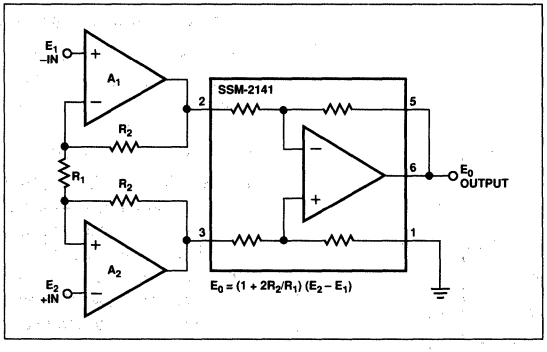


FIGURE 5: *Suitable instrumentation amplifier requirements can be addressed by using an input stage consisting of* A_1, A_2, R_1 *and* R_2.

ANALOG DEVICES

Balanced Line Driver

SSM-2142

FEATURES

Transformer-Like Balanced Output
Drives 10 V RMS Into a 600 Ω Load
Stable When Driving Large Capacitive Loads and Long Cables
Low Distortion
0.006% typ 20 Hz-20 kHz, 10 V RMS into 600 Ω
High Slew Rate
15 V/μs typ
Low Gain Error
(Differential or Single-Ended); 0.7% typ
Outputs Short-Circuit Protected
Available In Space-Saving 8-Pin Mini-DIP Package
Low Cost

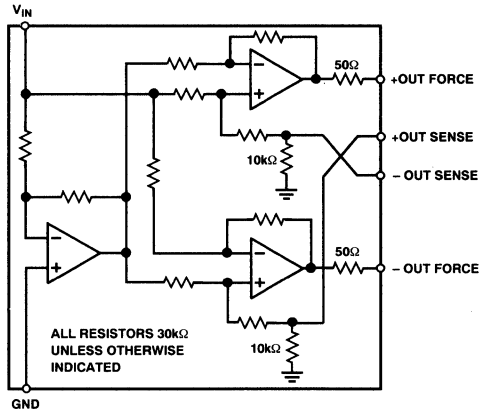
APPLICATIONS

Audio Mix Consoles
Distribution Amplifiers
Graphic and Parametric Equalizers
Dynamic Range Processors
Digital Effects Processors
Telecommunications Systems
Industrial Instrumentation
Hi-Fi Equipment

GENERAL DESCRIPTION

The SSM-2142 is an integrated differential-output buffer amplifier that converts a single-ended input signal to a balanced output signal pair with high output drive. By utilizing low noise thermally matched thin film resistors and high slew rate amplifiers, the SSM-2142 helps maintain the sonic quality of audio systems by eliminating power line hum, RF interference, voltage drops, and other externally generated noise commonly encountered with long audio cable runs. Excellent rejection of common-mode noise and offset errors is achieved by laser trimming of the onboard resistors, assuring high gain accuracy. The carefully designed output stage of the SSM-2142 is capable of driving difficult loads, yielding low-distortion performance despite extremely long cables or loads as low as 600 Ω, and is stable over a wide range of operating conditions.

FUNCTIONAL BLOCK DIAGRAM



Based on a cross-coupled, electronically balanced topology, the SSM-2142 mimics the performance of fully balanced transformer-based solutions for line driving. However, the SSM-2142 maintains lower distortion and occupies much less board space than transformers while achieving comparable common-mode rejection performance with reduced parts count.

The SSM-2142 in tandem with the SSM-2141 differential receiver establishes a complete, reliable solution for driving and receiving audio signals over long cables. The SSM-2141 features an Input Common-Mode Rejection Ratio of 100 dB at 60 Hz. Specifications demonstrating the performance of this typical system are included in the data sheet.

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SSM-2142—SPECIFICATIONS

(V_S = ±18 V, −40°C ≤ T_A ≤ +85°C, operating in differential mode unless indicated otherwise. Typical characteristics apply to operation at T_A = +25°C.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT IMPEDANCE	Z_{IN}			10		kΩ
INPUT CURRENT	I_{IN}	V_{IN} = ±7.071 V		±750	±900	μA
GAIN, DIFFERENTIAL			5.8	5.98		dB
GAIN, SINGLE-ENDED		Single-Ended Mode	5.7	5.94		dB
GAIN ERROR, DIFFERENTIAL		R_L = 600 Ω		0.7	2	%
POWER SUPPLY REJECTION RATIO STATIC	PSRR	V_S = ±13 V to ±18 V	60	80		dB
OUTPUT COMMON-MODE REJECTION	OCMR	See Test Circuit; f = 1 kHz	−38	−45		dB
OUTPUT SIGNAL BALANCE RATIO	SBR	See Test Circuit; f = 1 kHz	−35	−40		dB
TOTAL HARMONIC DISTORTION Plus Noise	THD+N	20 Hz to 20 kHz, V_O = 10 V rms, R_L = 600 Ω		0.006		%
SIGNAL-TO-NOISE RATIO	SNR	V_{IN} = 0 V, 0 dBu = 0.775 V rms		−93.4		dBu
HEADROOM	HR	CLIP Level = 10.5 V rms		+22.6		dBu
SLEW RATE	SR			15		V/μs
OUTPUT COMMON-MODE VOLTAGE OFFSET[1]	V_{OOS}	R_L = 600 Ω	−250	25	250	mV
DIFFERENTIAL OUTPUT VOLTAGE OFFSET	V_{OOD}	R_L = 600 Ω	−50	15	50	mV
DIFFERENTIAL OUTPUT VOLTAGE SWING		V_{IN} = ±7.071 V	±13.8	±14.14		V
OUTPUT IMPEDANCE	Z_O		45	50	55	Ω
SUPPLY CURRENT	I_{SY}	Unloaded, V_{IN} = 0 V		5.5	7.0	mA
OUTPUT CURRENT, SHORT CIRCUIT	I_{SC}		60	70		mA

NOTE
[1]Output common-mode offset voltage can be removed by inserting dc blocking capacitors in the sense lines. See the Applications Information.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18 V
Storage Temperature . . . . . −60°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . . +300°C
Junction Temperature . . . . . +150°C
Operating Temperature Range . . . . . −40°C to +85°C
Output Short Circuit Duration (Both Outputs) . . . . . Indefinite

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

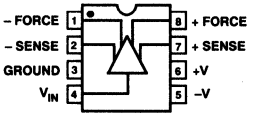
ORDERING GUIDE

Model	Operating Temperature Range	Package Option[1]
SSM2142P	−40°C to +85°C	Plastic DIP
SSM2142Z	−40°C to +85°C	Cerdip
SSM2142S[2]	−40°C to +85°C	SOIC

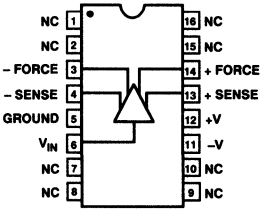
NOTES
[1]For outline information see Package Information section.
[2]For availability of SOIC package, contact your local sales office.

PIN CONNECTIONS

8-Pin Plastic DIP (P Suffix)
8-Pin Cerdip (Z Suffix)



16-Pin SOIC (S Suffix)



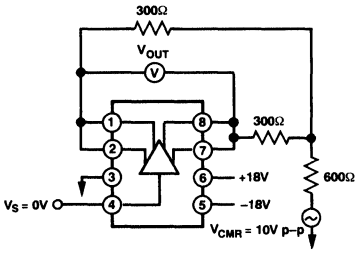


Figure 1. Output CMR Test Circuit

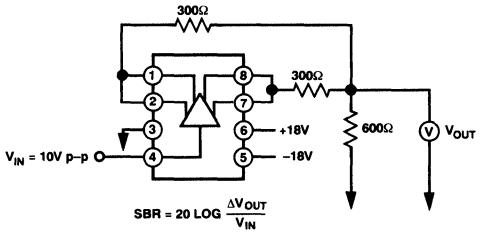


Figure 2. Signal Balance Ratio (BBC Method) Test Circuit

Typical Performance Characteristics

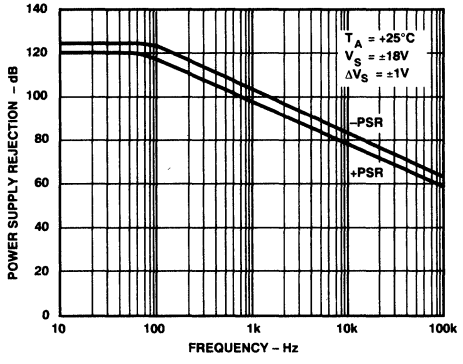


Figure 3. Power Supply Rejection vs. Frequency

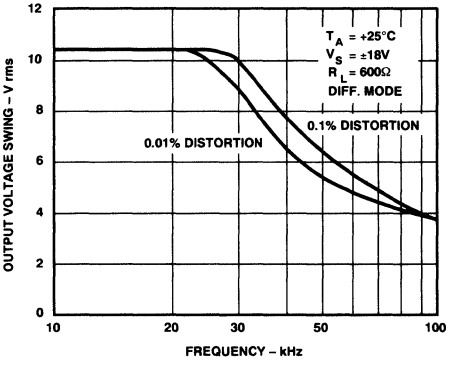


Figure 4. Maximum Output Voltage Swing vs. Frequency

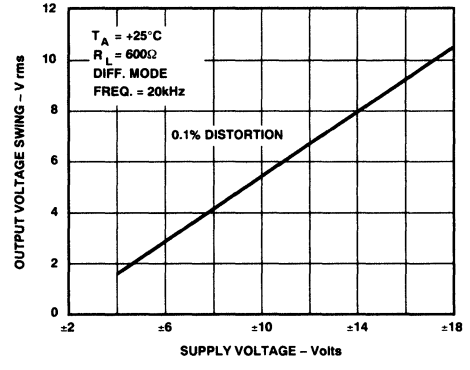


Figure 5. Output Voltage Swing vs. Supply Voltage

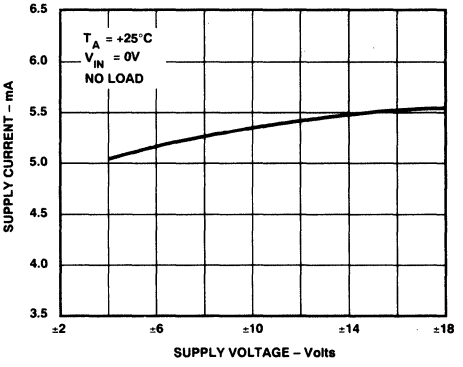
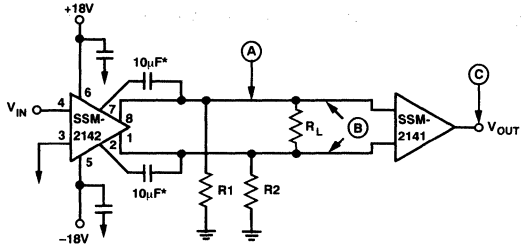


Figure 6. Supply Current vs. Supply Voltage

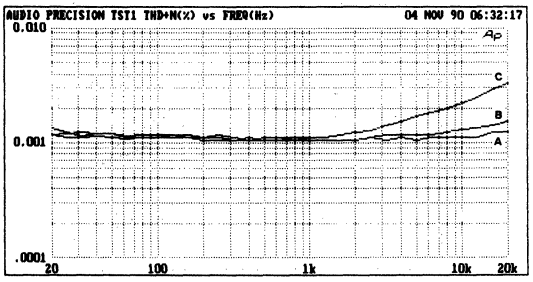
THD PERFORMANCE

The following data, taken from the THD test circuit on an Audio Precision System One using the internal 80 kHz noise filter, demonstrates the typical performance of a balanced-pair system based on the SSM-2142/SSM-2141 chip set. Both differential and single-ended modes of operation are shown, under a number of output load conditions which simulate various application situations. Note also that there is no adverse effect on system performance when using the optional series feedback capacitors, which reject dc cable offsets in order to maintain optimal ac noise rejection. The large signal transient response of the system to a 100 kHz square wave input is also shown, demonstrating the stability of the SSM-2142 under load.



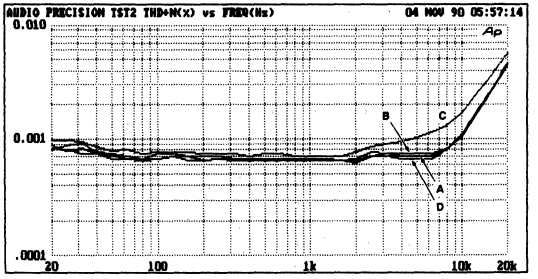
*USED ONLY IN THD PLOTS AS NOTED.
ALL CABLE MEASUREMENTS USE BELDEN 8451 CABLE.

Figure 7. THD Test Circuit



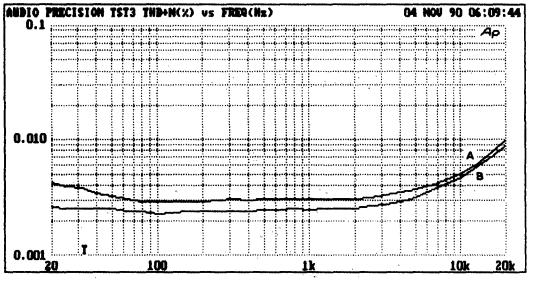
V_O = 10 V rms, NO CABLE
A: R1 = R2 = R_L = ∞
B: R1 = R2 = 600 Ω, R_L = ∞
C: R1 = R2 = ∞, R_L = 600 Ω

Figure 8. THD+N vs. Frequency at Point B (Differential Mode)



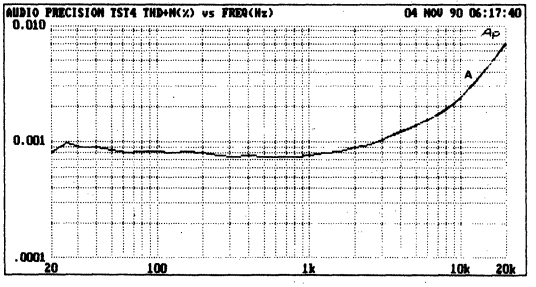
V_O = 10 V rms, WITH 500 FEET CABLE
A: R1 = R2 = R_L = ∞
B: R1 = R2 = 600 Ω, R_L = ∞
C: R1 = R2 = ∞, R_L = 600 Ω
D: R1 = R2 = R_L = ∞, WITH SERIES FEEDBACK CAPACITORS

Figure 9. THD+N vs. Frequency at Point B (Differential Mode)



V_O = 10 V rms, R2 = 0 Ω, R_L = ∞
A: R1 = 600 Ω, WITH 250 FEET CABLE
B: R1 = ∞, NO CABLE

Figure 10. THD+N vs. Frequency at Point A (Single Ended)



V_O = 10 V rms, NO CABLE
A: R1 = R2 = ∞, R_L = 600 Ω

Figure 11. THD+N vs. Frequency at Point C (SSM-2141 Output)

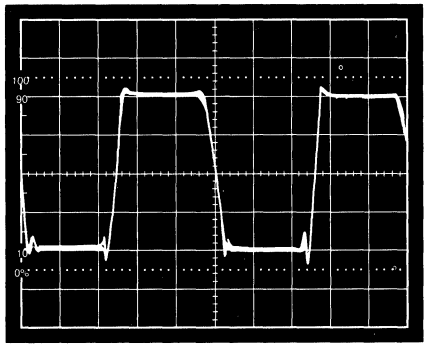


Figure 12. 100 kHz Square Wave Observed at Point B (Differential Mode). V_O = 10 V rms, R1 = R2 = ∞, R_L = 600 Ω

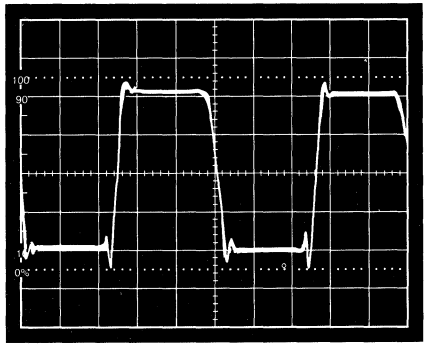


Figure 13. 100 kHz Square Wave at Point B (Differential Mode). V_O = 10 V rms, R1 = R2 = ∞, R_L = 600 Ω, with Series Feedback Capacitors

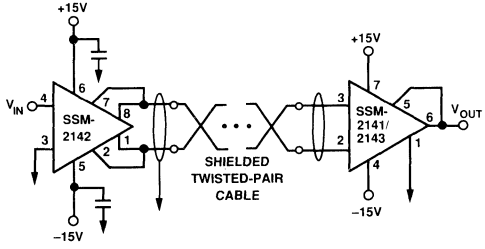


Figure 14. Typical Application of the SSM-2142 and SSM-2141/SSM-2143

APPLICATIONS INFORMATION

The SSM-2142 is designed to provide excellent common-mode rejection, high output drive, and low signal distortion and noise in a balanced line-driving system. The differential output stage consists of twin cross-coupled unity-gain buffer amplifiers with on-chip 50 Ω series damping resistors. The impedances in the output buffer pair are precisely balanced by laser trimming during production. This results in the high gain accuracy needed to obtain good common-mode noise rejection, and excellent separation between the offset error voltages common to the cable pair and the desired differential input signal. As shown in the test circuit, it is suggested that a suitable balanced, high input-impedance differential amplifier such as the SSM-2141 or SSM-2143 be used at the receiving end for best system performance. The SSM-2143 receiver output is configured for a gain of one half following the 6 dB gain of the SSM-2142, in order to maintain an overall system gain of unity.

In applications encountering a large dc offset on the cable or those wishing to ensure optimal rejection performance by avoiding differential offset error sources, dc blocking capacitors may be employed at the sense outputs of the SSM-2142. As shown in the test circuit, these components should present as little impedance as possible to minimize low-frequency errors, such as 10 μF NP (or tantalum if the polarity of the offset is known).

SYSTEM GROUNDING CONSIDERATIONS

Due to ground currents, supply variations, and other factors, the ground potentials of the circuits at each end of a signal cable may not be exactly equal. The primary purpose of a balanced-pair line is to reject this voltage difference, commonly called "longitudinal error." A measure of the ability of the system to reject longitudinal error voltage is output common-mode rejection. In order to obtain the optimal OCMR and noise rejection performance available with the SSM-2142, the user should observe the following precautions:

1. The quality of the differential output is directly dependent upon the accuracy of the input voltage presented to the device. Input voltage errors developed across the impedance of the source must be avoided in order to maintain system performance. The input of the SSM-2142 should be driven directly by an operational amplifier or buffer offering low source impedance and low noise.
2. The ground input should be in close proximity to the single-ended input's source common. Ground offset errors encountered in the source circuitry also impair system performance.
3. Make sure that the SSM-2142 is adequately decoupled with 0.1 μF bypass capacitors located close to each supply pin.
4. Avoid the use of passive circuitry in series with the SSM-2142 outputs. Any reactive difference in the line pair will cause significant imbalances and affect the gain error of the device. Snubber networks or series load resistors are not required to maintain stability in SSM-2142-based systems, even when driving signals over extremely long cables.
5. Efforts should be made to maintain a physical balance in the arrangement of the signal pair wiring. Capacitive differences due to variations in routing or wire length may cause unequal noise pickup between the pair, which will degrade the system OCMR. Shielded twisted-pair cable is the preferred choice in all applications. The shield should not be utilized as a signal conductor. Grounding the shield at one end, near the output common, avoids ground loop currents flowing in the shield which increase noise coupling and longitudinal errors.

THE CABLE PAIR

The SSM-2142 is capable of driving a 10 V rms signal into 600 Ω and will remain stable despite cable capacitances of up to 0.16 μF in either balanced or single-ended configurations. Low-impedance shielded audio cable such as the standard Belden 8451 or similar is recommended, especially in applications traversing considerable distances. The user is cautioned that the so-called "audiophile" cables may incur four times the capacitance per unit length of the standard industrial-grade product. In situations of extreme load and/or distance, adding a second parallel cable allows the user to trade off half of the total line resistance against a doubling in capacitive load.

SINGLE-ENDED OPERATION

The SSM-2142 is designed to be compatible with existing balanced-pair interface systems. Just as in transformer-based circuits, identical but opposite currents are generated by the output pair which can be ground-referenced if desired and transmitted on a single wire. Single-ended operation requires that the unused side of the output pair be grounded to a solid return path in order to avoid voltage offset errors at the nearby input common. The signal quality obtained in these systems is directly dependent on the quality of the ground at each end of the wire. Also note that in single-ended operation the gain through the device is still 6 dB, and that the SSM-2142 incurs no significant degradation in signal distortion or output drive capability, although the noise rejection inherent in balanced-pair systems is lost.

POWER SUPPLY SEQUENCING

A problem occasionally encountered in the interface system environment involves irregular application of the supplies. The user is cautioned that applying power erratically can inadvertently bias parts of the circuit into a latchup condition. The small geometries of an integrated circuit are easily breached and damaged by short-risetime spikes on a supply line, which usually demonstrate considerable overshoot. The questionable practice of exchanging components or boards while under power can create such an undesirable sequence as well. Possible options which offer improved board-level device protection include: additional bypass capacitors, high-current reverse-biased steering diodes between both supplies and ground, various transient surge suppression devices, and safety grounding connectors.

Likewise, power should be applied to the device before the output is connected to "live" systems which may carry voltages of sufficient magnitude to turn on the output devices of the SSM-2142 and damage the device. In any case, of course, the user must always observe the absolute maximum ratings shown in the specifications.

ANALOG DEVICES

−6 dB Differential Line Receiver

SSM-2143

FEATURES

High Common-Mode Rejection
- **DC: 90 dB typ**
- **60 Hz: 90 dB typ**
- **20 kHz: 85 dB typ**

Ultralow THD: 0.0006% typ @ 1 kHz
Fast Slew Rate: 10 V/μs typ
Wide Bandwidth: 7 MHz typ (G = 1/2)
Two Gain Levels Available: G = 1/2 or 2
Low Cost

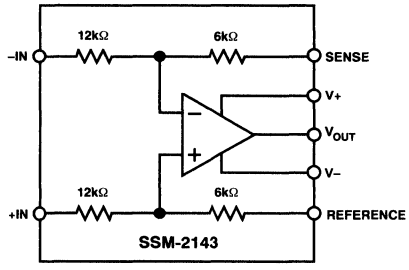
GENERAL DESCRIPTION

The SSM-2143 is an integrated differential amplifier intended to receive balanced line inputs in audio applications requiring a high level of immunity from common-mode noise. The device provides a typical 90 dB of common-mode rejection (CMR), which is achieved by laser trimming of resistances to better than 0.005%.

Additional features of the device include a slew rate of 10 V/μs and wide bandwidth. Total harmonic distortion (THD) is less than 0.004% over the full audio band, even while driving low impedance loads. The SSM-2143 input stage is designed to handle input signals as large as +28 dBu at G = 1/2. Although primarily intended for G = 1/2 applications, a gain of 2 can be realized by reversing the +IN/−IN and SENSE/REFERENCE connections.

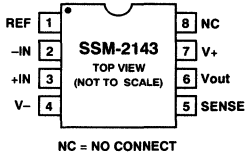
When configured for a gain of 1/2, the SSM-2143 and SSM-2142 Balanced Line Driver provide a fully integrated, unity gain solution to driving audio signals over long cable runs.

FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS

Epoxy Mini-DIP (P Suffix)
and
SOIC (S Suffix)



NC = NO CONNECT

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This is an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

SSM-2143—SPECIFICATIONS

(V_S = ±15 V, −40°C ≤ T_A ≤ +85°C, G = 1/2, unless otherwise specified. Typical specifications apply at T_A = +25°C.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
AUDIO PERFORMANCE						
Total Harmonic Distortion Plus Noise	THD+N	V_{IN} = 10 V rms, R_L = 10 kΩ, f = 1 kHz		0.0006		%
Signal-to-Noise Ratio	SNR	0 dBu = 0.775 V rms, 20 kHz BW, RTI		−107.3		dBu
Headroom	HR	Clip Point = 1% THD+N		+28.0		dBu
DYNAMIC RESPONSE						
Slew Rate	SR	R_L = 2 kΩ, C_L = 200 pF	6	10		V/μs
Small Signal Bandwidth	$BW_{-3\ dB}$	R_L = 2 kΩ, C_L = 200 pF				
		G = 1/2		7		MHz
		G = 2		3.5		MHz
INPUT						
Input Offset Voltage	V_{IOS}	V_{CM} = 0 V, RTI, G = 2	−1.2	0.05	+1.2	mV
Common-Mode Rejection	CMR	V_{CM} = ±10 V, RTO				
		f = dc	70	90		dB
		f = 60 Hz		90		dB
		f = 20 kHz		85		dB
		f = 400 kHz		60		dB
Power Supply Rejection	PSR	V_S = ±6 V to ±18 V	90	110		dB
Input Voltage Range	IVR	Common Mode		±15		V
		Differential		±28		V
OUTPUT						
Output Voltage Swing	V_O	R_L = 2 kΩ	±13	±14		V
Minimum Resistive Load Drive				2		kΩ
Maximum Capacitive Load Drive				300		pF
Short Circuit Current Limit	I_{SC}			+45, −20		mA
GAIN						
Gain Accuracy			−0.1	0.03	0.1	%
REFERENCE INPUT						
Input Resistance				18		kΩ
Voltage Range				±10		V
POWER SUPPLY						
Supply Voltage Range	V_S		±6		±18	V
Supply Current	I_{SY}	V_{CM} = 0 V, R_L = ∞		±2.7	±4.0	mA

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18 V
Common-Mode Input Voltage . . . . . ±22 V
Differential Input Voltage . . . . . ±44 V
Output Short Circuit Duration . . . . . Continuous
Operating Temperature Range . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature (T_J) . . . . . +150°C
Lead Temperature (Soldering, 60 sec) . . . . . +300°C
Thermal Resistance
8-Pin Plastic DIP (P): θ_{JA} = 103, θ_{JC} = 43 . . . . . °C/W
8-Pin SOIC (S): θ_{JA} = 150, θ_{JC} = 43 . . . . . °C/W

ORDERING GUIDE

Model	Operating Temperature Range	Package[1]
SSM-2143P	−40°C to +85°C	8-Pin Plastic DIP
SSM-2143S[2]	−40°C to +85°C	8-Pin SOIC

[1]For outline information see Package Information section.
[2]Contact sales office for availability.

ANALOG DEVICES

Audio Dual Matched NPN Transistor

SSM-2210

FEATURES

- **Very Low Voltage Noise ..... @ 100Hz, 1nV/√Hz MAX**
- **Excellent Current Gain Match ..... 0.5% TYP**
- **Tight V_{BE} Match (V_{OS}) ..... 200µV MAX**
- **Outstanding Offset Voltage Drift ..... 0.03µV/°C TYP**
- **High Gain-Bandwidth Product ..... 200MHz TYP**
- **Low Cost**
- **Direct Replacement For LM394BN/CN**

ORDERING INFORMATION †

PACKAGE		OPERATING TEMPERATURE RANGE
PLASTIC 8-PIN	SO 8-PIN	
SSM2210P	SSM2210S†	XIND*

* XIND = –40°C to +85°C

† For availability on SO package, contact your local sales office.

GENERAL DESCRIPTION

The SSM-2210 is a dual NPN matched transistor pair specifically designed to meet the requirements of ultra-low noise audio systems.

With its extremely low input base spreading resistance (rbb' is typically 28Ω), and high current gain (h_{FE} typically exceeds 600 @ I_C = 1mA), systems implementing the SSM-2210 can achieve outstanding signal-to-noise ratios. This will result in superior performance compared to systems incorporating commercially available monolithic amplifiers.

The equivalent input voltage noise of the SSM-2210 is typically only 0.8nV/√Hz over the entire audio bandwidth of 20Hz to 20KHz.

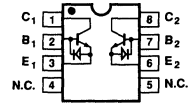
Excellent matching of the current gain (Δh_{FE}) to about 0.5% and low V_{OS} of less than 50µV (typical) make it ideal for symmetrically balanced designs which reduce high order amplifier harmonic distortion.

Stability of the matching parameters is guaranteed by protection diodes across the base-emitter junction. These diodes prevent degradation of Beta and matching characteristics due to reverse biasing of the base-emitter junction.

The SSM-2210 is also an ideal choice for accurate and reliable current biasing and mirroring circuits. Furthermore, since a current mirror's accuracy degrades exponentially with mismatches of V_{BE}'s between transistor pairs, the low V_{OS} of the SSM-2210 will preclude offset trimming in most circuit applications.

The SSM-2210 is offered in an 8-pin epoxy DIP and 8-pin SO, its performance and characteristics are guaranteed over the extended industrial temperature range of –40°C to +85°C.

PIN CONNECTIONS



8-PIN PLASTIC DIP (P-Suffix)

8-PIN SO (S-Suffix)

ABSOLUTE MAXIMUM RATINGS

Collector Current (I_C) 20mA
Emitter Current (I_E) 20mA
Collector-Collector Voltage (BV_{CC}) 40V
Collector-Base Voltage (BV_{CBO}) 40V
Collector-Emitter Voltage (BV_{CEO}) 40V
Emitter-Emitter Voltage (BV_{EE}) 40V
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature ..... –65°C to +125°C
Junction Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (NOTE 1)	Θ_{JC}	UNITS
8-Pin Plastic DIP (P)	110	50	°C/W
8-Pin SO (S)	160	44	°C/W

NOTE:

1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO packages.

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ELECTRICAL CHARACTERISTICS at V_{CB} = 15V, I_C = 10µA, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2210 MIN	TYP	MAX	UNITS
Current Gain	h_{FE}	I_C = 1mA (Note 1)	300	605	–	
		I_C = 10µA	200	550	–	
Current Gain Match	Δh_{FE}	10µA ≤ I_C ≤ 1mA (Note 2)	–	0.5	5	%
Noise Voltage Density	e_n	I_C = 1mA, V_{CB} = 0 (Note 3)				
		f_o = 10Hz	–	1.6	2	nV/√Hz
		f_o = 100Hz	–	0.9	1	
		f_o = 1kHz	–	0.85	1	
		f_o = 10kHz	–	0.85	1	
Offset Voltage	V_{OS}	V_{CB} = 0 I_C = 1mA	–	10	200	µV
Offset Voltage Change vs V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ V_{MAX} (Note 4) 1µA ≤ I_C ≤ 1mA (Note 5)	–	10	50	µV
Offset Voltage Change vs Collector Current	$\Delta V_{OS}/\Delta I_C$	V_{CB} = 0V 1µA ≤ I_C ≤ 1mA (Note 5)	–	5	70	µV
Breakdown Voltage	BV_{CEO}		40	–	–	V
Gain-Bandwidth Product	f_T	I_C = 10mA, V_{CE} = 10V	–	200	–	MHz
Collector-Base Leakage Current	I_{CBO}	V_{CB} = V_{MAX}	–	25	500	pA
Collector-Collector Leakage Current	I_{CC}	V_{CC} = V_{MAX} (Notes 6, 7)	–	35	500	pA
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = V_{MAX} (Notes 6, 7) V_{BE} = 0	–	35	500	pA
Input Bias Current	I_B	I_C = 10µA	–	–	50	nA
Input Offset Current	I_{OS}	I_C = 10µA	–	–	6.2	nA
Collector Saturation Voltage	$V_{CE(SAT)}$	I_C = 1mA I_B = 100µA	–	0.05	0.2	V
Output Capacitance	C_{OB}	V_{CB} = 15V, I_E = 0	–	23	–	pF
Bulk Resistance	r_{BE}	10µA ≤ I_C ≤ 10mA (Note 6)	–	0.3	1.6	Ω
Collector-Collector Capacitance	C_{CC}	V_{CC} = 0	–	35	–	pF

NOTES:

1. Current gain is guaranteed with Collector-Base Voltage (V_{CB}) swept from 0 to V_{MAX} at the indicated collector currents.
2. Current Gain Match (Δh_{FE}) is defined as:

$$\Delta h_{FE} = \frac{100(\Delta I_B)\ (h_{FE}\text{min})}{I_C}$$

3. Noise Voltage Density is guaranteed, but not 100% tested.
4. This is the maximum change in V_{OS} as V_{CB} is swept from 0V to 40V.
5. Measured at I_C = 10µA and guaranteed by design over the specified range of I_C.
6. Guaranteed by design.
7. I_{CC} and I_{CES} are verified by measurement of I_{CBO}.

ELECTRICAL CHARACTERISTICS at V_{CB} = 15V, –40°C ≤ T_A ≤ +85°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2210 MIN	SSM-2210 TYP	SSM-2210 MAX	UNITS
Current Gain	h_{FE}	I_C = 1mA (Note 1) I_C = 10µA	300 200	– –	– –	
Offset Voltage	V_{OS}	V_{CB} = 0 I_C = 1mA	–	–	220	µV
Average Offset Voltage Drift	TCV_{OS}	10µA ≤ I_C ≤ 1mA, 0 ≤ V_{CB} ≤ V_{MAX} (Note 2) V_{OS} Trimmed to Zero (Note 3)	– –	0.08 0.03	1 0.3	µV/°C
Input Bias Current	I_B	I_C = 10µA	–	–	50	nA
Input Offset Current	I_{OS}	I_C = 10µA	–	–	13	nA
Input Offset Current Drift	TCI_{OS}	I_C = 10µA (Note 4)	–	40	150	pA/°C
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = V_{MAX}$	–	3	–	nA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = V_{MAX}$, V_{BE} = 0	–	4	–	nA
Collector-Collector Leakage Current	I_{CC}	$V_{CC} = V_{MAX}$	–	4	–	nA

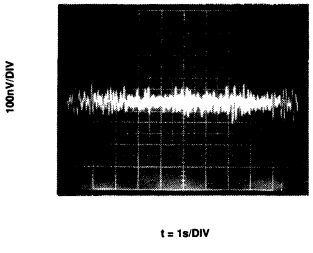
NOTES:

1. Current gain is guaranteed with Collector-Base Voltage (V_{CB}) swept from 0 to V_{MAX} at the indicated collector current.
2. Guaranteed by V_{OS} test ($TCV_{OS} \approx \frac{V_{OS}}{T} \propto V_{BE}$), T = 298K for T_A = 25°C.
3. The initial zero offset voltage is established by adjusting the ratio of I_{C1} to I_{C2} at T_A = 25°C. This ratio must be held to 0.003% over the entire temperature range. Measurements are taken at the temperature extremes and 25°C.
4. Guaranteed by design.

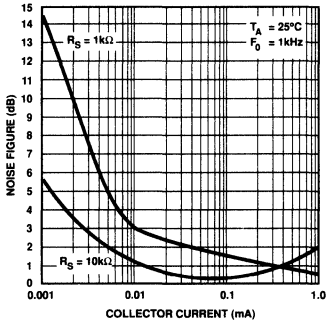
7

TYPICAL PERFORMANCE CHARACTERISTICS

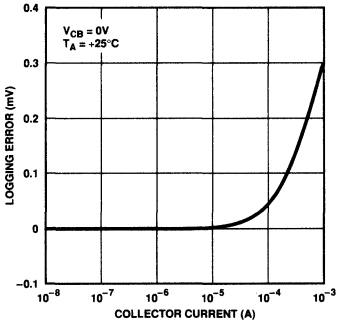
LOW FREQUENCY NOISE (0.1 Hz TO 10 Hz)



NOISE FIGURE vs COLLECTOR CURRENT

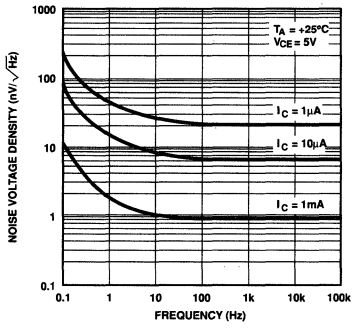


EMITTER-BASE LOG CONFORMITY

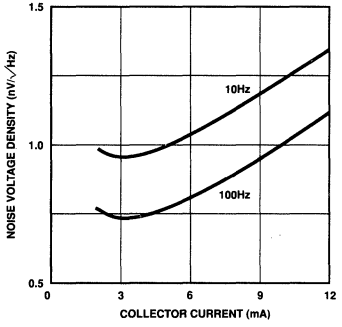


TYPICAL PERFORMANCE CHARACTERISTICS

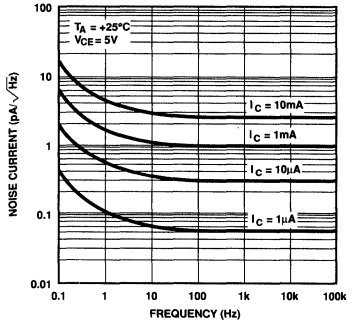
NOISE VOLTAGE DENSITY vs FREQUENCY



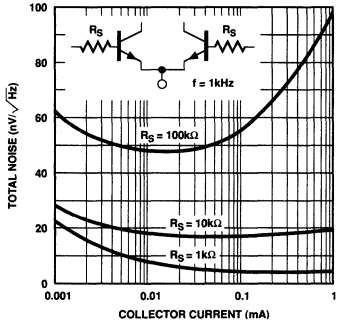
NOISE VOLTAGE DENSITY vs COLLECTOR CURRENT



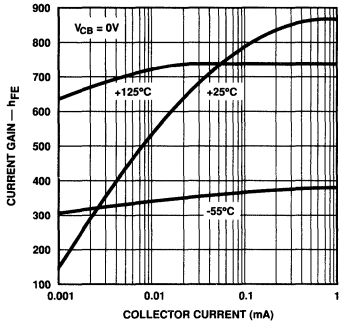
NOISE CURRENT DENSITY vs FREQUENCY



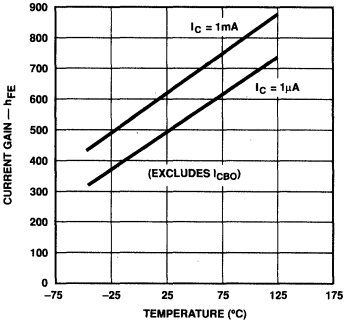
TOTAL NOISE vs COLLECTOR CURRENT



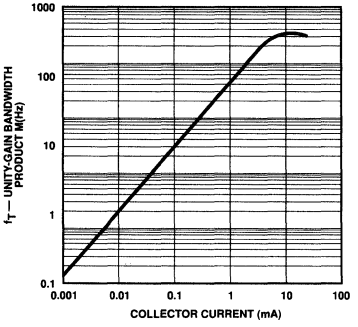
CURRENT GAIN vs COLLECTOR CURRENT



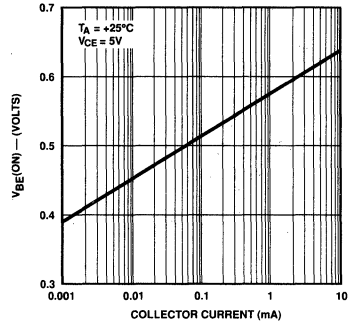
CURRENT GAIN vs TEMPERATURE



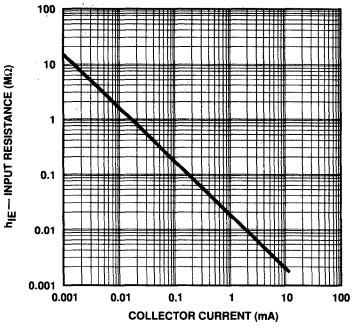
GAIN BANDWIDTH vs COLLECTOR CURRENT



BASE-EMITTER-ON-VOLTAGE vs COLLECTOR CURRENT

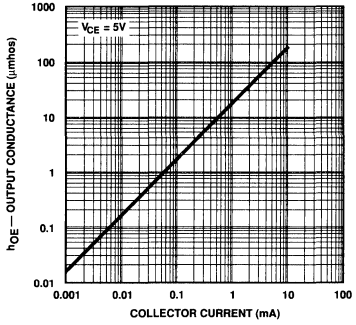


SMALL-SIGNAL INPUT RESISTANCE vs COLLECTOR CURRENT

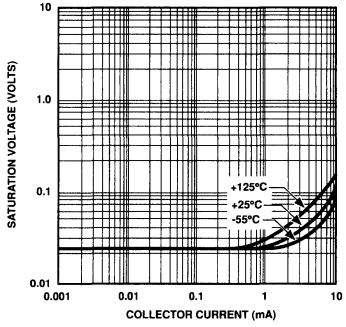


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

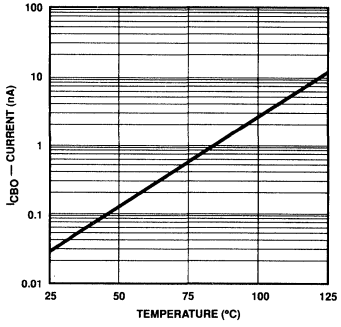
SMALL-SIGNAL OUTPUT CONDUCTANCE vs COLLECTOR CURRENT



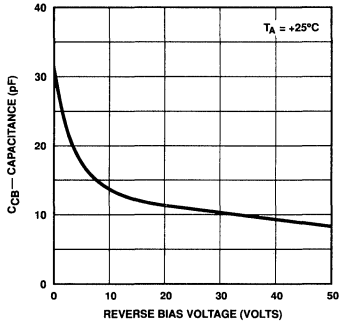
SATURATION VOLTAGE vs COLLECTOR CURRENT



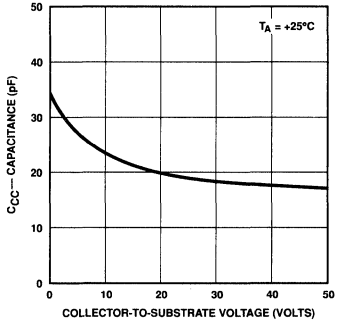
COLLECTOR-TO-BASE LEAKAGE vs TEMPERATURE



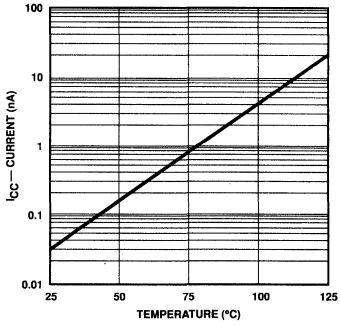
COLLECTOR-BASE CAPACITANCE vs REVERSE BIAS VOLTAGE



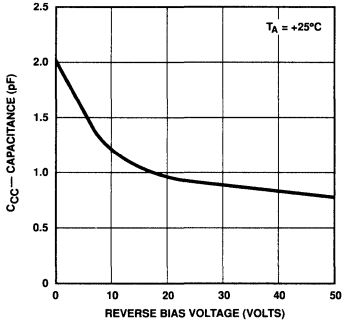
COLLECTOR-TO-COLLECTOR CAPACITANCE vs COLLECTOR-TO-SUBSTRATE VOLTAGE



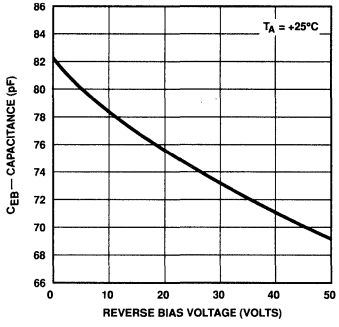
COLLECTOR-TO-COLLECTOR LEAKAGE vs TEMPERATURE



COLLECTOR-TO-COLLECTOR CAPACITANCE vs REVERSE BIAS VOLTAGE



EMITTER-BASE CAPACITANCE vs REVERSE BIAS VOLTAGE



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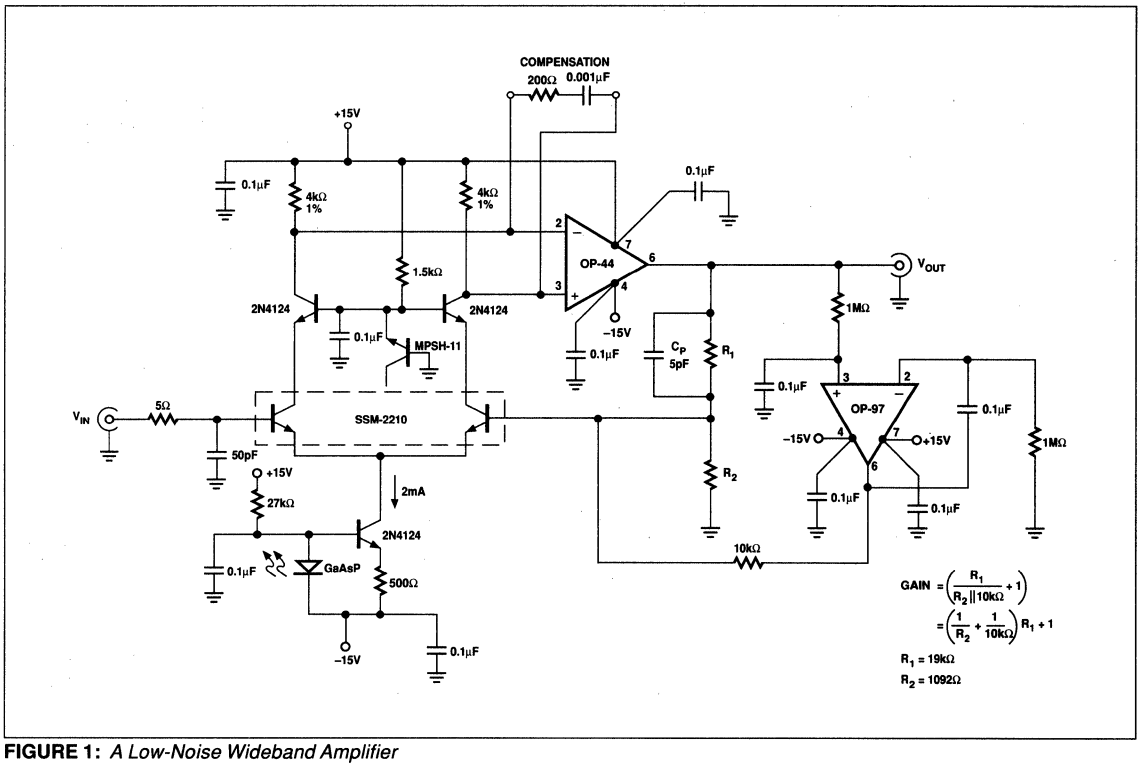

FIGURE 1: *A Low-Noise Wideband Amplifier*

A VERY LOW-NOISE, WIDEBAND AMPLIFIER

Figure 1 illustrates a low-noise, wide-band amplifier consisting of a high slew rate JFET amplifier, the OP-44, and a cascoded differential preamplifier using the SSM-2210 transistor pair. The SSM-2210 achieves extremely low input voltage noise performance ($e_n \approx 0.7nV/\sqrt{Hz}$) via a large geometry transistor design which minimizes the base-spreading resistance. This, however, results in relatively higher collector-to-base capacitance (C_{OB}) than ordinary small-signal transistors. For high gain stages, the Miller effect of C_{OB} will limit the voltage gain bandwidth; resorting to a cascode configuration reduces the Miller feedback capacitance, improving stability, bandwidth, and reducing distortion due to base-width modulation. Additionally, cascoding does not increase the noise figure of the overall amplifier system and reduces the high order harmonic distortion.

The circuit in Figure 1 balances the impedance symmetrically in the differential preamp. This serves to reject common-mode noise injected from the power supplies.

Although the SSM-2210's transistors are closely matched, an offset voltage error can still be created by imbalanced source impedances. Accordingly, a precision low-power amplifier (OP-97), configured as a noninverting integrator is implemented which servos-out the offset voltage to less than 100µV referred to the input of the amplifier.

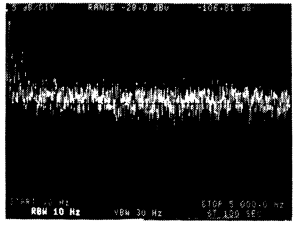

FIGURE 2: *Spectrum Analyzer Display of Wideband Amplifier Noise Spectral Density.* $e_n \approx 1.7nV/\sqrt{Hz}$

Figure 2 illustrates the composite amplifier's low voltage noise density of only $1.7nV/\sqrt{Hz}$ @ 1kHz. Figure 3 and Figure 4 show the excellent pulse response and an extremely low distortion of only 0.0015% over the audio bandwidth, respectively.

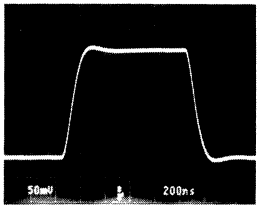

FIGURE 3: *Small-Signal Pulse Response*

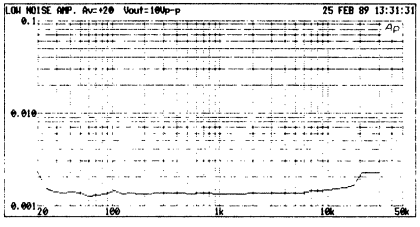

FIGURE 4: *Total Harmonic Distortion vs Frequency*

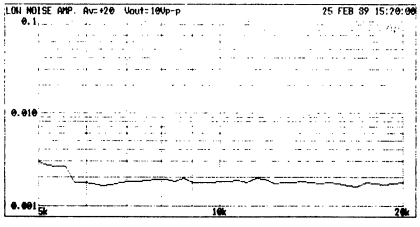

FIGURE 5: *D.I.M. vs Frequency*

A special test was performed to check for dynamic or transient intermodulation distortion. A square wave of 3.15kHz is mixed with a sine wave probe tone, and the resulting intermodulation distortion was found to be less than 0.002% (Figure 5). This is an impressively low value considering the amplifier's gain of 26dB. Interestingly, the GBW product of the composite amplifier was 63MHz which is much larger than that of the OP-44 by itself. This is made possible by the SSM-2210's cascoded preamplifier having a wide bandwidth and large signal gain.

The measured performance of this amplifier is summarized in Table 1.

TABLE 1: Measured Performance of the Low-Noise Wideband Amplifier

Slew-Rate	40V/μs
Gain-Bandwidth	63.6 MHz
Input Noise Voltage Density @ 1kHz	$1.7nV/\sqrt{Hz}$
Output Voltage Swing	±13V
Input Offset Voltage	10μV

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500pV/√Hz AMPLIFIER

In situations where low output, low-impedance transducers are used, amplifiers must have very low voltage noise to maintain a good signal-to-noise ratio. The design presented in this application is an operational amplifier with only 500pV/√Hz of broadband noise. The front end uses SSM-2210 low-noise dual transistors to achieve this exceptional performance. The op amp has superb DC specifications compatible with high-precision transducer requirements, and AC specifications suitable for professional audio work.

PRINCIPLE OF OPERATION

The design configuration in Figure 6 uses an OP-27 op amp (already a low-noise design) preceded by an amplifier consisting of three parallel-connected SSM-2210 dual transistors. Base spreading resistance (rbb) generates thermal noise which is reduced by a factor of $\sqrt{3}$ when the input transistors are parallel connected. Schottky noise, the other major noise-generating mechanism, is minimized by using a relatively high collector current (1mA per device). High current ensures a low dynamic emitter resistance, but does increase the base current and its associated current noise. Higher current noise is relatively unimportant when low-impedance transducers are used.

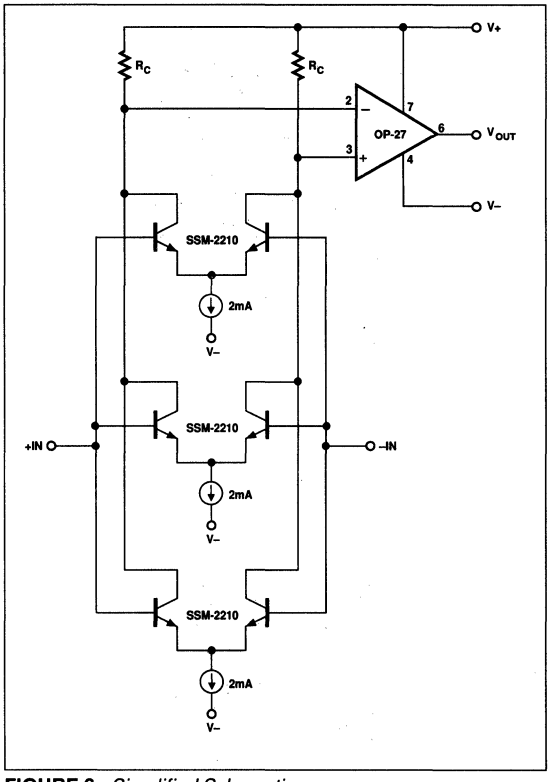

FIGURE 6: *Simplified Schematic*

CIRCUIT DESCRIPTION

The detailed circuit is shown in Figure 7. A total input-stage emitter current of 6mA is provided by Q_4. The transistor acts as a true current source to provide the highest possible common-mode rejection. R_1, R_2, and R_3 ensure that this current splits equally among the three input pairs. The constant current in Q_4 is set by using the forward voltage of a GaAsP light-emitting diode as a reference. The difference between this voltage and the base-emitter voltage of a silicon transistor is predictable and constant (to within a few percent) over the military temperature range. The voltage difference, approximately 1V, is impressed across the emitter resistor R_{12} which produces a temperature-stable emitter current.

R_6 and C_1 provide phase compensation for the amplifier and are sufficient to ensure stability at gains of ten and above.

R_7 is an input offset trim that provides approximately ±300μV trim range. The very low drift characteristics of the SSM-2210 make it possible to obtain drifts of less than 0.1μV/°C when the offset is nulled close to zero. If this trim is not required, the R_4, R_7, and R_8 network should be omitted and R_5/R_9 connected directly to V+.

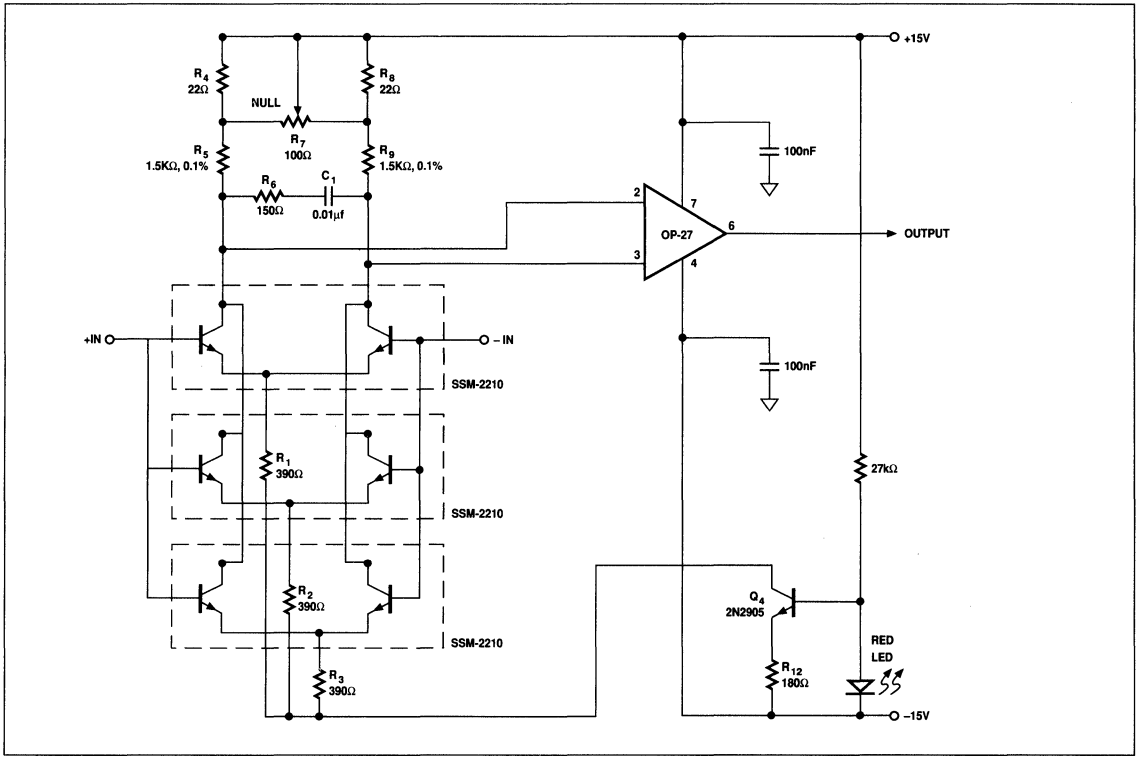

FIGURE 7: *Complete Amplifier Schematic*

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AMPLIFIER PERFORMANCE

The measured performance of the op amp is summarized in Table 2. Figure 8 shows the broadband noise spectrum which is flat at about 500pV/√Hz. Figure 9 shows the low-frequency spectrum which illustrates the low 1/f noise corner at 1.5Hz. The low-frequency characteristic in the time domain from 0.1Hz to 10Hz is shown in Figure 10; peak-to-peak amplitude is less than 40nV.

TABLE 2: Measured Performance of the Op Amp

Input Noise Voltage Density at 1kHz		500pV/√Hz
Input Noise Voltage from 0.1Hz to 10Hz		$40nV_{p-p}$
Input Noise Current at 1kHz		1.5pA/√Hz
Gain-Bandwidth	G = 10	3MHz
	G = 100	600kHz
	G = 1000	150kHz
Slew Rate		2V/μs
Open-Loop Gain		3×10^7
Common-Mode Rejection		130dB
Input Bias Current		3μA
Supply Current		10mA
Nulled TCV_{OS}		0.1μV/°C Max
T.H.D. at 1kHz	G = 1000	0.002%

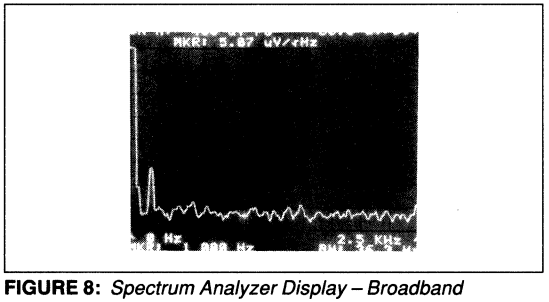

FIGURE 8: *Spectrum Analyzer Display – Broadband*

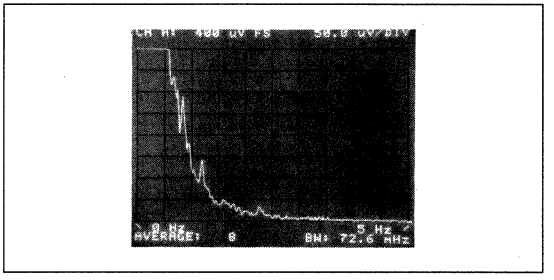

FIGURE 9: *Spectrum Analyzer Display – Low Frequency*

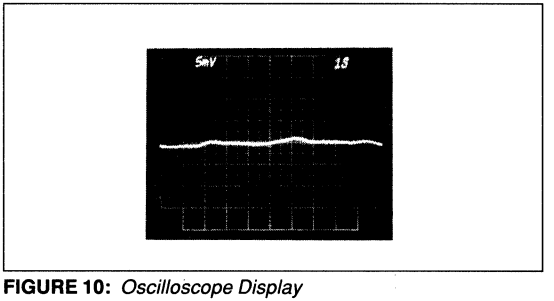

FIGURE 10: *Oscilloscope Display*

CONCLUSION

Using SSM-2210 matched transistor pairs operating at a high current level, it is possible to construct a high-performance, low-noise operational amplifier. The circuit uses a minimum of components and achieves performance levels exceeding monolithic amplifiers.

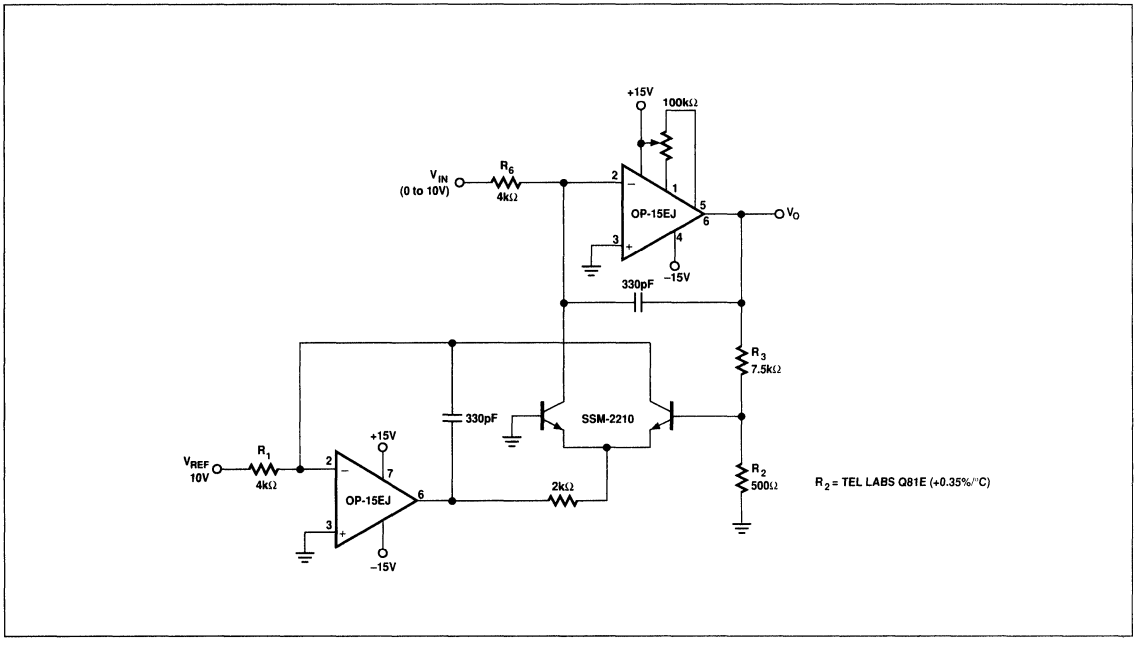

FIGURE 11: *Fast Logarithmic Amplifier*

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FAST LOGARITHMIC AMPLIFIER

The circuit of Figure 11 is a modification of a standard logarithmic amplifier configuration. Running the SSM-2210 at 2.5mA per side (full-scale) allows a fast response with wide dynamic range. The circuit has a 7 decade current range, a 5 decade voltage range, and is capable of 2.5µs settling time to 1% with a 1 to 10V step.

The output follows the equation:

$$V_O = \frac{R_3 + R_2}{R_2} \frac{kT}{q} \ln \frac{V_{REF}}{V_{IN}}$$

To compensate for the temperature dependence of the kT/q term, a resistor with a positive 0.35%/°C temperature coefficient is chosen for R_2.

The output is inverted with respect to the input, and is nominally – 1V/decade using the component values indicated.

ANALOG DEVICES

Audio Dual Matched PNP Transistor

SSM-2220

FEATURES

- **Very Low Voltage Noise ..... @ 100Hz, 1nV/√Hz Max**
- **High Gain Bandwidth ..... 190MHz Typ**
- **Excellent Gain ..... @ I_C = 1mA, 165 Typ**
- **Tight Gain Matching ..... 3% Max**
- **Outstanding Logarithmic Conformance... r_{BE} = 0.3Ω Typ**
- **Low Offset Voltage ..... 200μV Max**
- **Low Cost**

APPLICATIONS

- **Microphone Preamplifiers**
- **Tape-Head Preamplifiers**
- **Current Sources and Mirrors**
- **Low Noise Precision Instrumentation**
- **Voltage Controlled Amplifiers/Multipliers**

ORDERING INFORMATION

8-PIN EPOXY DIP	8-PIN SO*	OPERATING TEMPERATURE RANGE
SSM2220P	SSM2220S	–40°C to +85°C

* For availability of SO package, contact your local sales office.

GENERAL DESCRIPTION

The SSM-2220 is a dual low noise matched PNP transistor which has been optimized for use in audio applications.

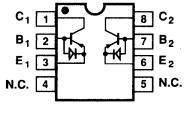
The ultra-low input voltage noise of the SSM-2220 is typically only 0.7nV/√Hz over the entire audio bandwidth of 20Hz to 20kHz. The low noise, high bandwidth (190MHz), and Offset Voltage of (200μV Max) make the SSM-2220 an ideal choice for demanding low noise preamplifier applications.

The SSM-2220 also offers excellent matching of the current gain (Δh_{FE}) to about 0.5% which will help to reduce the high order amplifier harmonic distortion. In addition, to insure the long-term stability of the matching parameters, internal protection diodes across the base-emitter junction were used to clamp any reverse base-emitter junction potential. This prevents a base-emitter breakdown condition which can result in degradation of gain and matching performance due to excessive breakdown current.

Another feature of the SSM-2220 is its very low bulk resistance of 0.3Ω typically which assures accurate logarithmic conformance.

The SSM-2220 is offered in 8-pin plastic, dual-in-line, and SO and its performance and characteristics are guaranteed over the extended industrial temperature range of –40°C to +85°C.

PIN CONNECTIONS



8-PIN EPOXY DIP (P-Suffix)

8-PIN SO (S-Suffix)

7

ABSOLUTE MAXIMUM RATINGS

Collector-Base Voltage (BV_{CBO}) 36V
Collector-Emitter Voltage (BV_{CEO}) 36V
Collector-Collector Voltage (BV_{CC}) 36V
Emitter-Emitter Voltage (BV_{EE}) 36V
Collector Current (I_C) 20mA
Emitter Current (I_E) 20mA
Operating Temperature Range
SSM-2220P ..... –40°C to +85°C
SSM-2220S ..... –40°C to +85°C
Operating Junction Temperature ..... –55°C to +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package; Θ_{JA} is specified for device soldered to printed circuit board for SO packages.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2220 MIN	SSM-2220 TYP	SSM-2220 MAX	UNITS
Current Gain (Note 1)	h_{FE}	V_{CB} = 0V, –36V I_C = 1mA I_C = 100µA I_C = 10µA	80 70 60	165 150 120	– – –	
Current Gain Matching (Note 2)	Δh_{FE}	I_C = 100µA, V_{CB} = 0V	–	0.5	6	%
Noise Voltage Density (Note 3)	e_N	I_C = 1mA, V_{CB} = 0V f_O = 10Hz f_O = 100Hz f_O = 1kHz f_O = 10kHz	– – – –	0.8 0.7 0.7 0.7	2 1 1 1	nV/√Hz
Offset Voltage (Note 4)	V_{OS}	V_{CB} = 0V, I_C = 100µA	–	40	200	µV
Offset Voltage Change vs. Collector Voltage	$\Delta V_{OS}/\Delta V_{CB}$	I_C = 100µA V_{CB1} = 0V V_{CB2} = –36V	–	11	200	µV
Offset Voltage Change vs. Collector Current	$\Delta V_{OS}/\Delta I_C$	V_{CB} = 0V I_{C1} = 10µA, I_{C2} = 1mA	–	12	75	µV
Offset Current	I_{OS}	I_C = 100µA, V_{CB} = 0V	–	6	45	nA
Collector-Base Leakage Current	I_{CB0}	V_{CB} = –36V = V_{MAX}	–	50	400	pA
Bulk Resistance	r_{BE}	V_{CB} = 0V, 10µA ≤ I_C ≤ 1mA	–	0.3	0.75	Ω
Collector Saturation Voltage	$V_{CE(SAT)}$	I_C = 1mA, I_B = 100µA	–	0.026	0.1	V

NOTES:
1. Current gain is measured at collector-base voltages (V_{CB}) swept from 0 to V_{MAX} at indicated collector current. Typicals are measured at V_{CB} = 0V.
2. Current gain matching (Δh_{FE}) is defined as:

$$\Delta h_{FE} = \frac{100(\Delta I_B)\, h_{FE}\,(MIN)}{I_C}$$

3. Sample tested. Noise tested and specified as equivalent input voltage for each transistor.
4. Offset voltage is defined as:
$V_{OS} = V_{BE1} - V_{BE2}$,
where V_{OS} is the differential voltage for

$$I_{C2} = I_{C2} : V_{OS} = V_{BE1} - V_{BE2} = \frac{KT}{q} \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

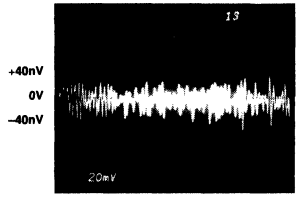
ELECTRICAL CHARACTERISTICS at $-40°C \le T_A \le +85°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2220 MIN	SSM-2220 TYP	SSM-2220 MAX	UNITS
Current Gain	h_{FE}	$V_{CB} = 0V, -36V$ $I_C = 1mA$ $I_C = 100\mu A$ $I_C = 10\mu A$	 60 50 40	 120 105 90	 – – –	
Offset Voltage	V_{OS}	$I_C = 100\mu A, V_{CB} = 0V$	–	30	265	µV
Offset Voltage Drift (Note 1)	TCV_{OS}	$I_C = 100\mu A, V_{CB} = 0V$	–	0.3	1.0	µV/°C
Offset Current	I_{OS}	$I_C = 100\mu A, V_{CB} = 0V$	–	10	200	nA
Breakdown Voltage	BV_{CEO}		36	–	–	V

NOTE:
1. Guaranteed by V_{OS} test ($TCV_{OS} = V_{OS}/T$ for $V_{OS} << V_{BE}$) where T = 298°K for T_A = 25°C.

TYPICAL PERFORMANCE CHARACTERISTICS

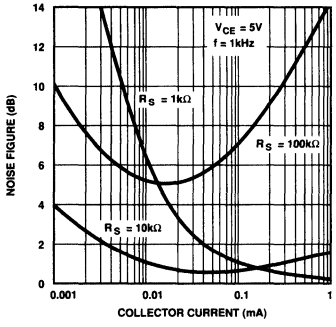
LOW FREQUENCY NOISE



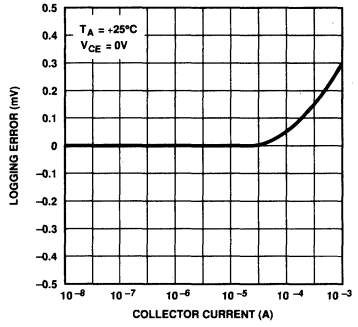
VERTICAL = 40nV/DIV
HORIZONTAL = 1s/DIV

V_{CE} = 5V
I_C = 1mA
T_A = +25°C

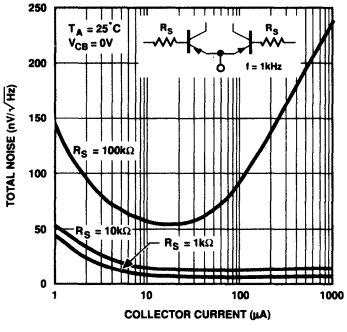
NOISE FIGURE vs COLLECTOR CURRENT



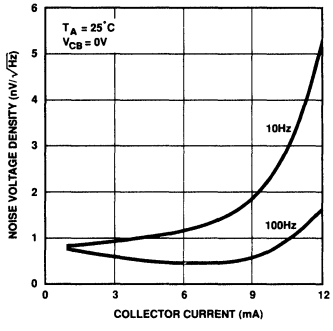
EMITTER-BASE LOG CONFORMITY



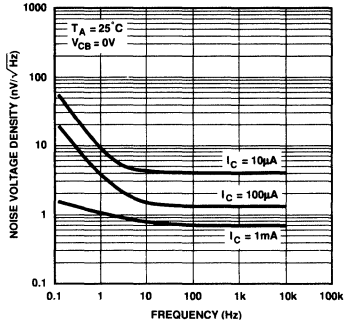
TOTAL NOISE vs COLLECTOR CURRENT



NOISE VOLTAGE DENSITY vs COLLECTOR CURRENT



NOISE VOLTAGE DENSITY vs FREQUENCY



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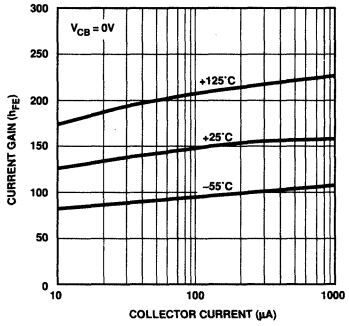
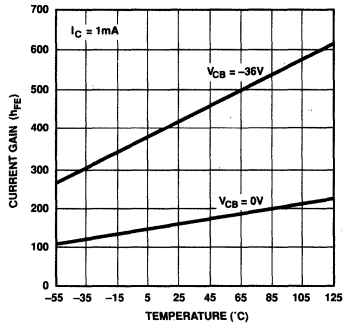
TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

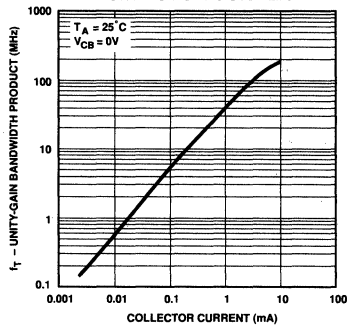
CURRENT GAIN vs COLLECTOR CURRENT



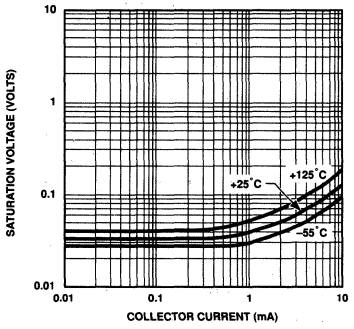
CURRENT GAIN vs TEMPERATURE



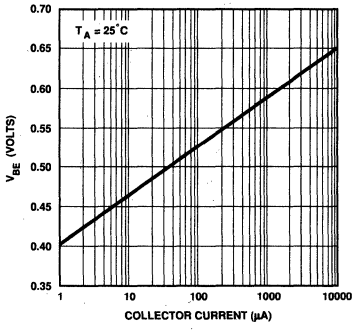
GAIN BANDWIDTH vs COLLECTOR CURRENT



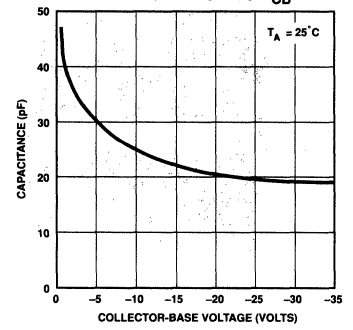
SATURATION VOLTAGE vs COLLECTOR CURRENT



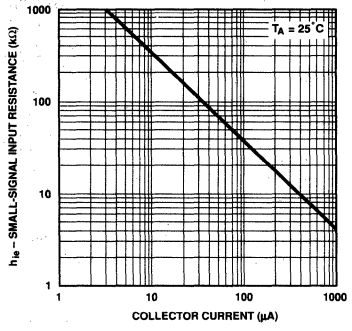
BASE-EMITTER VOLTAGE vs COLLECTOR CURRENT



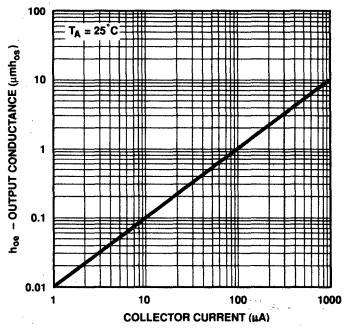
COLLECTOR-BASE CAPACITANCE vs V_{CB}



SMALL-SIGNAL INPUT RESISTANCE (h_{ie}) vs COLLECTOR CURRENT



SMALL-SIGNAL OUTPUT CONDUCTANCE (h_{oe}) vs COLLECTOR CURRENT



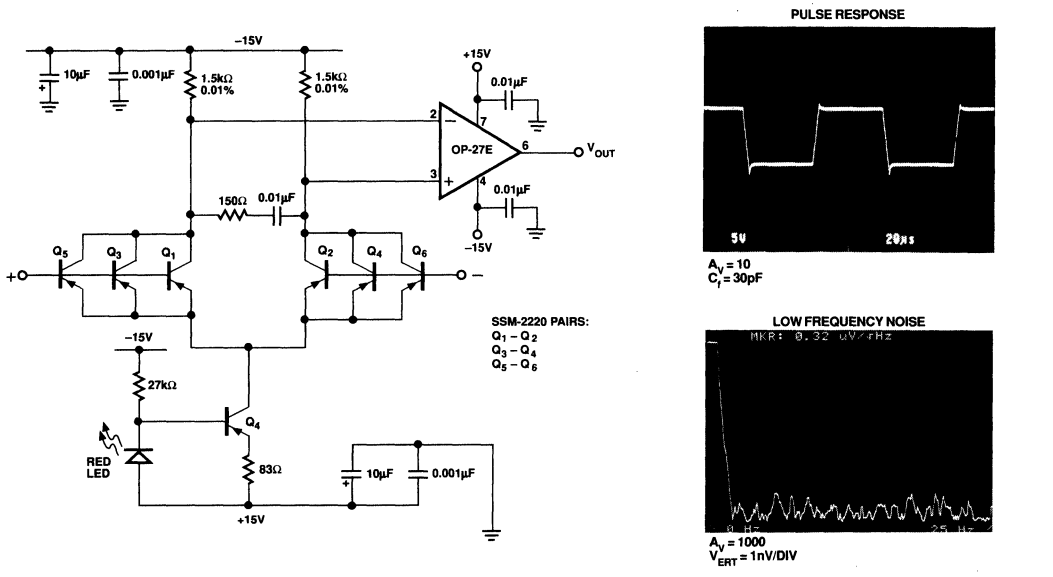


FIGURE 1a: *Super Low Noise Amplifier*

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APPLICATIONS INFORMATION

SUPER LOW NOISE AMPLIFIER

The circuit in Figure 1a is a super low noise amplifier with equivalent input voltage noise of 0.32nV/$\sqrt{Hz}$. By paralleling SSM-2220 matched pairs, a further reduction of amplifier noise is attained by a reduction of the base spreading resistance by a factor of 3, and consequently the noise by $\sqrt{3}$. Additionally, the shot noise contribution is reduced by maintaining a high collector current (2mA/device) which reduces the dynamic emitter resistance and decreases voltage noise. The voltage noise is inversely proportional to the square root of the stage current, and current noise increases proportionally to the square root of the stage current. Accordingly, this amplifier capitalizes on voltage noise reduction techniques at the expense of increasing the current noise. However, high current noise is not usually important when dealing with low impedance sources.

This amplifier exhibits excellent full power AC performance, 0.08% THD into a 600Ω load, making it suitable for exacting audio applications (see Figure 1b).

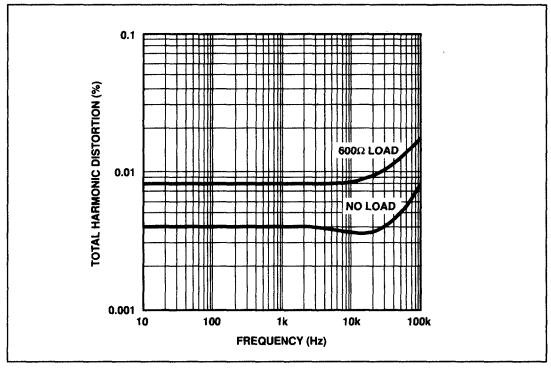

FIGURE 1b: *Super Low Noise Amplifier – Total Harmonic Distortion*

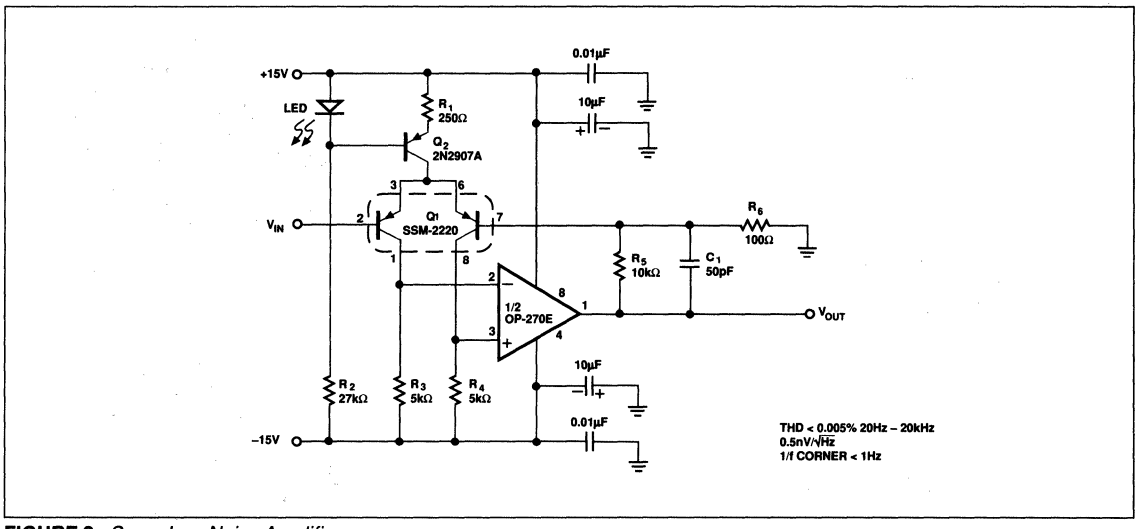

FIGURE 2: *Super Low Noise Amplifier*

LOW NOISE MICROPHONE PREAMPLIFIER

Figure 2 shows a microphone preamplifier that consists of a SSM-2220 and a low noise op amp. The input stage operates at a relatively high quiescent current of 2mA per side, which reduces the SSM-2220 transistor's voltage noise. The $1/f$ corner is less than 1Hz. Total harmonic distortion is under 0.005% for a $10V_{p\text{-}p}$ signal from 20Hz to 20kHz. The preamp gain is 100, but can be modified by varying R_5 or R_6 ($V_{OUT}/V_{IN} = R_5/R_6 + 1$).

A total input stage emitter current of 4mA is provided by Q_2. The constant current in Q_2 is set by using the forward voltage of a GaAsP LED as a reference. The difference between this voltage and the V_{BE} of a silicon transistor is predictable and constant (to a few percent) over a wide temperature range. The voltage difference, approximately 1V, is dropped across the 250Ω resistor which produces a temperature stabilized emitter current.

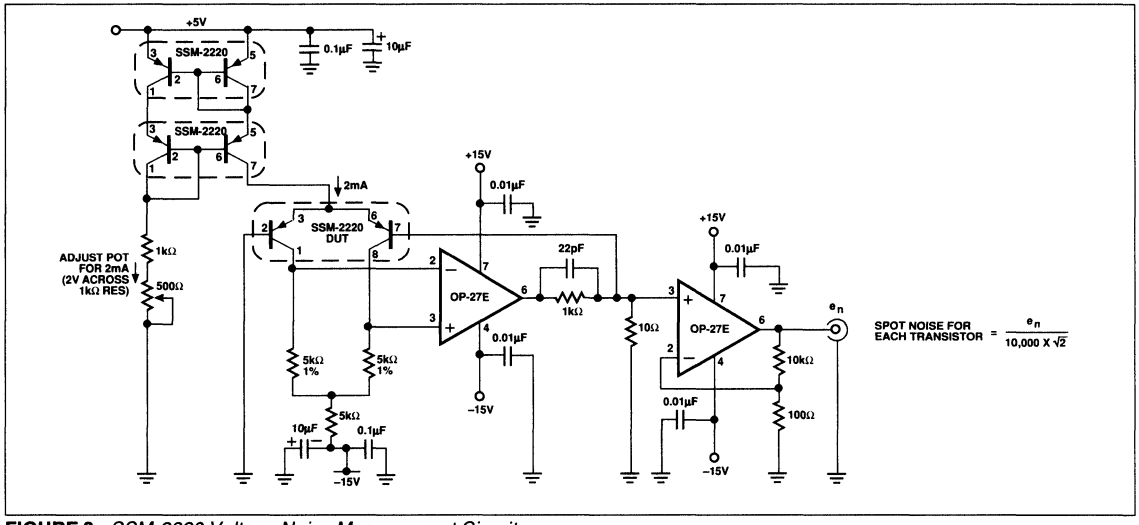

FIGURE 3: *SSM-2220 Voltage Noise Measurement Circuit*

SSM-2220 NOISE MEASUREMENT

All resistive components (Johnson noise, $e_n^2 = 4kTBR$, or $e_n = 0.13\sqrt{R}$ nV/$\sqrt{Hz}$, where R is in kΩ) and semiconductor junctions (Shot noise, caused by current flowing through a junction, produces voltage noise in series impedances such as transistor-collector load resistors, $I_n = 0.556\sqrt{I}$ pA/$\sqrt{Hz}$ where I is in µA) contribute to the system input noise.

Figure 3 illustrates a technique for measuring the equivalent input noise voltage of the SSM-2220. 1mA of stage current is used to bias each side of the differential pair. The 5kΩ collector resistors noise contribution is insignificant compared to the voltage noise of the SSM-2220. Since noise in the signal path is referred back to the input, this voltage noise is attenuated by the gain of the circuit. Consequently, the noise contribution of the collector load resistors is only 0.048nV/$\sqrt{Hz}$. This is considerably less than the typical 0.8nV/$\sqrt{Hz}$ input noise voltage of the SSM-2220 transistor.

The noise contribution of the OP-27 gain stages is also negligible due to the gain in the signal path. The op amp stages amplify the input referred noise of the transistors to increase the signal strength to allow the noise spectral density (e_{in} x 10000) to be measured with a spectrum analyzer. And, since we assume equal noise contributions from each transistor in the SSM-2220, the output is divided by $\sqrt{2}$ to determine a single transistor's input noise.

Air currents cause small temperature changes that can appear as low frequency noise. To eliminate this noise source, the measurement circuit must be thermally isolated. Effects of extraneous noise sources must also be eliminated by totally shielding the circuit.

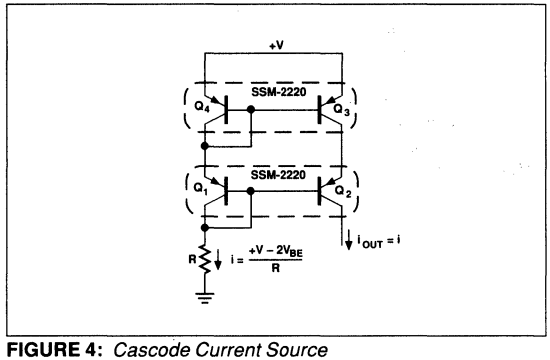

FIGURE 4: *Cascode Current Source*

CURRENT SOURCES

A fundamental requirement for accurate current mirrors and active load stages is matched transistor components. Due to the excellent V_{BE} matching (the voltage difference between V_{BE}'s required to equalize collector current) and gain matching, the SSM-2220 can be used to implement a variety of standard current mirrors that can source current into a load such as an amplifier stage. The advantages of current loads in amplifiers versus resistors is an increase of voltage gain due to higher impedances, larger signal range, and in many applications, a wider signal bandwidth.

Figure 4 illustrates a cascode current mirror consisting of two SSM-2220 transistor pairs.

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The cascode current source has a common base transistor in series with the output which causes an increase in output impedance of the current source since V_{CE} stays relatively constant. High frequency characteristics are improved due to a reduction of Miller capacitance. The small-signal output impedance can be determined by consulting "h_{oe} vs. Collector Current" typical graph. Typical output impedance levels approach the performance of a perfect current source.

Considering a typical collector current of 100µA, we have:

$$ro_{Q3} = \frac{1}{1.0\mu MHOS} = 1M\Omega.$$

Q_2 and Q_3 are in series and operate at the same current level, so the total output impedance is:

$R_O = h_{FE}\, ro_{Q3} \approx (160)(1M\Omega) = 160M\Omega.$

CURRENT MATCHING

The objective of current source or mirror design is generation of currents that are either matched or must maintain a constant ratio. However, mismatch of base-emitter voltages cause output current errors. Consider the example of Figure 5. If the resistors and transistors are equal and the collector voltages are the same, the collector currents will match precisely. Investigating the current-matching errors resulting from a non-zero V_{OS}, we define ΔI_C as the current error between the two transistors.

Graph 5 describes the relationship of current matching errors versus offset voltage for a specified average current I_C. Note that since the relative error between the currents is exponentially proportional to the offset voltage, tight matching is required to design high accuracy current sources. For example, if the offset voltage is 5mV at 100µA collector current, the current matching error would be 20%. Additionally, temperature effects such as offset drift (3µV/°C per mV of V_{OS}) will degrade performance if Q_1 and Q_2 are not well matched.

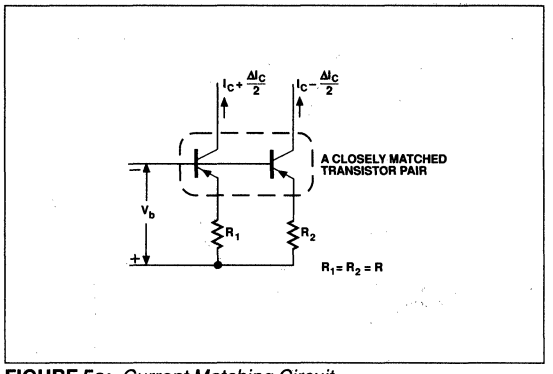


FIGURE 5a: *Current Matching Circuit*

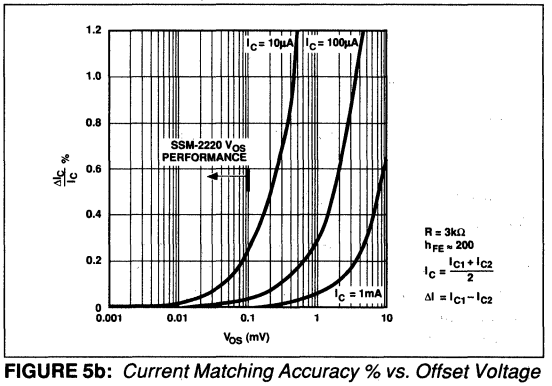


FIGURE 5b: *Current Matching Accuracy % vs. Offset Voltage*

ANALOG DEVICES

Dual Audio Analog Switches

SSM-2402/SSM-2412

FEATURES

- **"Clickless" Bilateral Audio Switching**
- **Guaranteed "Break-Before-Make" Switching**
- **Low Distortion ..... 0.003% Typ**
- **Low Noise ..... 1nV/√Hz**
- **Superb OFF-Isolation ..... 120dB Typ**
- **Low ON-Resistance ..... 60Ω Typ**
- **Wide Signal Range:**
  V_S = ±18V ..... 10V RMS
- **Wide Power Supply Range ..... ±9V to ±20V**
- **Available in Dice Form**

ORDERING INFORMATION

PACKAGE		OPERATING TEMPERATURE RANGE
PLASTIC 14-PIN	SOL 16-PIN	
SSM2402P	SSM2402S	XIND*
SSM2412P	SSM2412S	XIND*

*XIND = –40°C to +85°C

GENERAL DESCRIPTION

The SSM-2402/2412 are dual analog switches designed specifically for high-performance audio applications. Distortion and noise are negligible over the full audio operating range of 20Hz to 20kHz at signal levels of up to $10V_{RMS}$. The SSM-2402/2412 offer a monolithic integrated alternative to expensive and noisy relays or complex discrete JFET circuits. Unlike conventional general-purpose CMOS switches, the SSM-2402/2412 provide superb fidelity without audio "clicks" during switching.

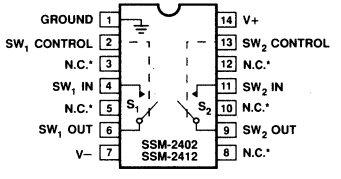
Conventional TTL or CMOS logic can be used to control the switch state. No external pull-up resistors are needed. A "T" configuration provides superb OFF-isolation and true bilateral operation. The analog inputs and outputs are protected against overload and overvoltage.

An important feature is the guaranteed "break-before-make" for **all** units, even IC-to-IC. In large systems with multiple switching channels, all separate switching units must open before any switch goes into the ON-state. With the SSM-2402/2412, you can be certain that multiple circuits will all break-before-make.

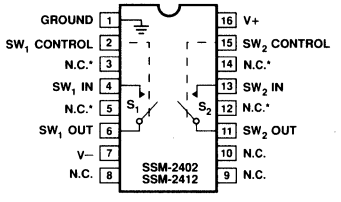
The SSM-2402/2412 represent a significant step forward in audio switching technology. Distortion and switching noise are significantly reduced in the new SSM-2402/2412 bipolar-JFET switches relative to CMOS switching technology. Based on a new circuit topology that optimizes audio performance, the SSM-2402/2412 make use of a proprietary bipolar-JFET process with thin-film resistor network capability. Nitride capacitors, which are very area efficient, are used for the proprietary ramp generator that controls the switch resistance transition. Very wide bandwidth amplifiers control the gate-to-source voltage over the full audio operating range for each switch. The ON-resistance remains constant with changes in signal amplitude and frequency, thus distortion is very low, less than 0.01% Max.

The SSM-2402 is the first analog switch truly optimized for high-performance audio applications. For broadcasting and other switching applications which require a faster switching time, we recommend the SSM-2412 – a dual analog switch with one-third of the switching time of the SSM-2402.

PIN CONNECTIONS



14-PIN PLASTIC DIP (P-Suffix)



16-PIN SOL (S-Suffix)

* GUARD PINS FOR INPUT/OUTPUT ISOLATION (GROUND FOR BEST PERFORMANCE)

CONTROL LOGIC

Logic In	Switch State
0	OFF
1	ON

Logic "0" ≤ 0.8V
Logic "1" ≥ 2.0V

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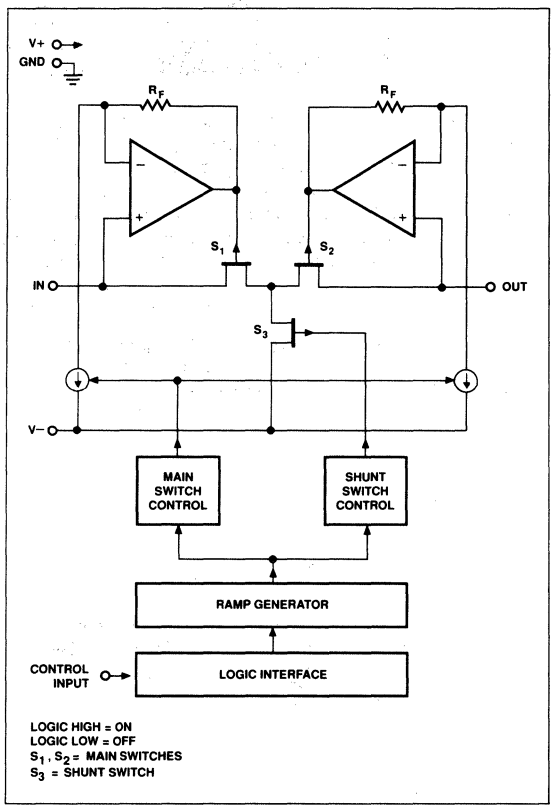
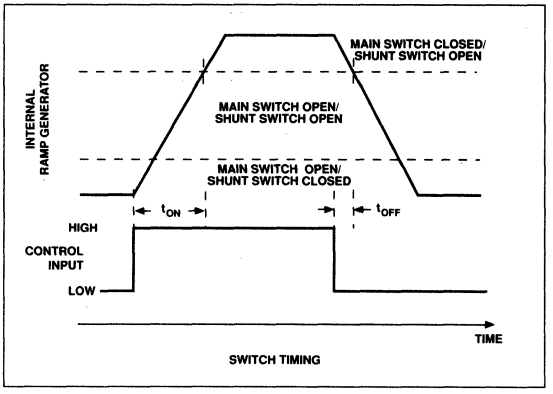
FUNCTIONAL DIAGRAM



TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range ..... –40°C to +85°C
Operating Supply Voltage Range ..... ±20V
Analog Input Voltage Range
Continuous ..... V– +3.5V ≤ V_A ≤ V+ –3.5V
Maximum Current Through Switch 20mA
Logic Input Voltage Range ..... V+ Supply to –2V
V_A to V– Supply ..... +36V

PACKAGE TYPE	Θ_{jA} (Note 1)	Θ_{jC}	UNITS
14-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTE:
1. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for P-DIP package; Θ_{jA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_S = ±18V, R_L = OPEN, and –40°C ≤ T_A ≤ +85°C, unless otherwise noted.

All specifications, tables, graphs, and application data apply to both the SSM-2402 and SSM-2412, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2402/2412 MIN	TYP	MAX	UNITS
Positive Supply Current	$+I_{SY}$	V_{IL} = 0.8V, 2.0V (Note 1)	–	6.0	7.5	mA
Negative Supply Current	$-I_{SY}$	V_{IL} = 0.8V, 2.0V (Note 1)	–	4.8	6.0	mA
Ground Current	I_{GND}	V_{IL} = 0.8V, 2.0V (Note 1)	–	0.6	1.5	mA
Digital Input High	V_{INH}	T_A = Full Temperature Range (Note 2)	2.0	–	–	V
Digital Input Low	V_{INL}	T_A = Full Temperature Range	–	–	0.8	V
Logic Input Current	I_{LOGIC}	V_{IN} = 0 to 15V (Note 3)	–	1.0	5.0	µA
Analog Voltage Range (Note 3)	V_{ANALOG}		–14.2	–	+14.2	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 18V$, R_L = OPEN, and $-40°C \le T_A \le +85°C$, unless otherwise noted. *Continued*

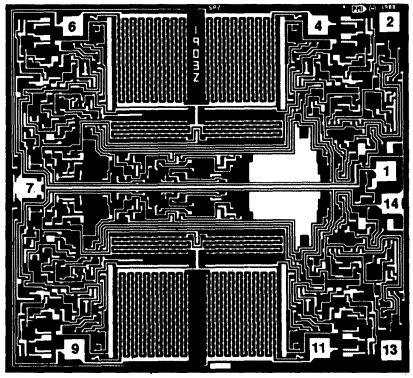
PARAMETER	SYMBOL	CONDITIONS		SSM-2402/2412 MIN	TYP	MAX	UNITS
Analog Current Range (Note 3)	I_{ANALOG}			−10	–	+10	mA
Overvoltage Input Current		$V_{IN} = \pm V_{SUPPLY}$		–	±40	–	mA
Switch ON Resistance	R_{ON}	$-14.2 \le V_A \le +14.2V$ $I_A = \pm 10mA$, $V_{IL} = 2.0V$ $T_A = +25°C$ T_A = Full Temperature Range Tempco ($\Delta R_{ON}/\Delta T$)		– – –	60 – 0.2	85 115 –	Ω Ω Ω/°C
R_{ON} Match	$R_{ON}MATCH$	$-14.2 \le V_A \le +14.2V$ $I_A = \pm 10mA$, $V_{IL} = 2.0V$		–	1	5	%
Switch ON Leakage Current (Notes 1, 3)	$I_{S(ON)}$	$V_{IL} = 2.0V$ $-14.2V \le V_A \le +14.2V$ $V_A = 0V$		– –	0.05 0.05	1.0 10.0	µA nA
Switch OFF Leakage Current (Notes 1, 3)	$I_{S(OFF)}$	$V_{IL} = 0.8V$ $-14.2V \le V_A \le +14.2V$ $V_A = 0V$		– –	0.05 0.05	1.0 10.0	µA nA
Turn-On Time (Note 5)	t_{ON}	$V_A = +10V$, $R_L = 2k\Omega$ $T_A = +25°C$, See Test Circuit	SSM-2402 SSM-2412	– –	10.0 3.5	– –	ms
Turn-Off Time (Note 6)	t_{OFF}	$V_A = +10V$, $R_L = 2k\Omega$ $T_A = +25°C$, See Test Circuit	SSM-2402 SSM-2412	– –	4.0 1.5	– –	ms
Break-Before-Make Time Delay (Note 7)	$t_{OFF} - t_{ON}$	$T_A = +25°C$	SSM-2402 SSM-2412	– –	6.0 2.0	– –	ms
Charge Injection	Q	$T_A = +25°C$	SSM-2402 SSM-2412	– –	50 150	– –	pC
ON-State Input Capacitance	$CS_{(ON)}$	$V_A = 1V_{RMS}$ f = 5kHz, $T_A = +25°C$		–	12	–	pF
OFF-State Input Capacitance	$CS_{(OFF)}$	$V_A = 1V_{RMS}$ f = 5kHz, $T_A = +25°C$		–	4	–	pF
OFF Isolation	$I_{SO(OFF)}$	$V_A = 10V_{RMS}$, 20Hz to 20kHz $T_A = +25°C$, See Test Circuit		–	120	–	dB
Channel-to-Channel Crosstalk	C_T	$V_A = 10V_{RMS}$, 20Hz to 20kHz $T_A = +25°C$		–	96	–	dB
Total Harmonic Distortion (Note 8)	THD	0 to $10V_{RMS}$, 20Hz to 20kHz $T_A = +25°C$, $R_L = 5k\Omega$		–	0.003	0.01	%
Spectral Noise Density	e_n	20Hz to 20kHz $T_A = +25°C$		–	1	–	$nV/\sqrt{Hz}$
Wideband Noise Density	$e_{n\,p\text{-}p}$	20Hz to 20kHz $T_A = +25°C$		–	0.2	–	$\mu V_{p\text{-}p}$

NOTES:

1. "V_{IL}" is the Logic Control Input.
2. Although not recommended, using unbalanced supplies with the positive rail in excess of 20V will result in an increased digital input high threshold. The threshold is set to 9.3% of the positive supply voltage.
3. Current tested at $V_{IN} = 0V$. This is the worst case condition.
4. Guaranteed by R_{ON} test condition.
5. Turn-ON Time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the final value.
6. Turn-OFF time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the initial value.
7. Switch is guaranteed by design to provide break-before-make operation.
8. THD guaranteed by design and dynamic R_{ON} testing.

DICE CHARACTERISTICS

SSM-2402/SSM-2412



DIE SIZE 0.105 x 0.097 inch, 10,185 sq. mils (2.667 x 2.464 mm, 6.57 sq. mm)

1. GROUND
2. SWITCH$_1$ CONTROL
4. SWITCH$_1$ IN
6. SWITCH$_1$ OUT
7. V– SUPPLY
9. SWITCH$_2$ IN
11. SWITCH$_2$ OUT
13. SWITCH$_2$ CONTROL
14. V+ SUPPLY

For additional DICE information, refer to PMI's Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 18V$, R_L = OPEN, and $T_A = +25°C$.

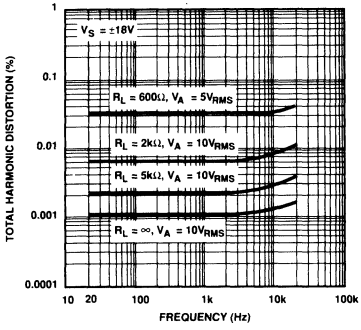
PARAMETER	SYMBOL	CONDITIONS (Note 1)	SSM-2402/2412NBC LIMIT	UNITS
Positive Supply Current	$+I_{SY}$	$V_{IL} = 0.8V$	7.5	mA MAX
Negative Supply Current	$-I_{SY}$	$V_{IL} = 0.8V$	6.0	mA MAX
Ground Current	I_{GND}	$V_{IL} = 0.8V$	1.5	mA MAX
Logic Input Current	I_{LOGIC}	$V_{IN} = 0V$ (Note 2)	5.0	µA MAX
Switch ON Resistance	R_{ON}	$-14.2 \le V_A \le +14.2V$ $I_A = \pm 10mA$, $V_{IL} = 2.0V$	85	Ω MAX
R_{ON} Match Between Switches	R_{ON}MATCH	$-14.2V \le V_A \le +14.2V$ $I_A = \pm 10mA$, $V_{IL} = 2.0V$	5	% MAX
Switch ON Leakage Current	$I_{S(ON)}$	$-14.2V \le V_A \le +14.2V$ $V_{IL} = 2.0V$	1.0	µA MAX
Switch OFF Leakage Current	$I_{S(OFF)}$	$-14.2V \le V_A \le +14.2V$ $V_{IL} = 0.8V$	1.0	µA MAX

NOTES:
1. V_{IL} = Logic Control Input
   V_A = Applied Analog Input Voltage
   I_A = Applied Analog Input Current
2. Worst Case Condition

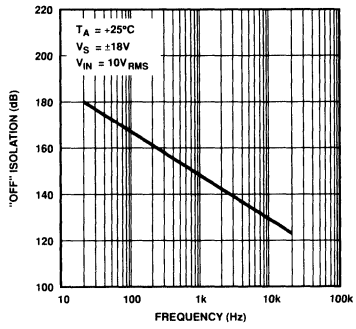
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

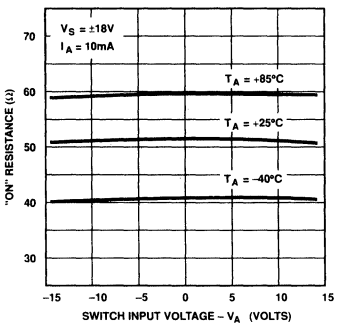
TOTAL HARMONIC DISTORTION vs FREQUENCY



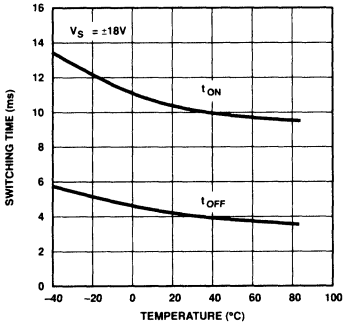
"OFF" ISOLATION vs FREQUENCY



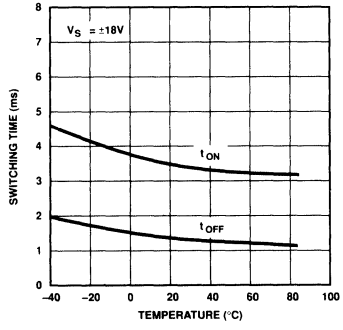
"ON" RESISTANCE vs ANALOG VOLTAGE



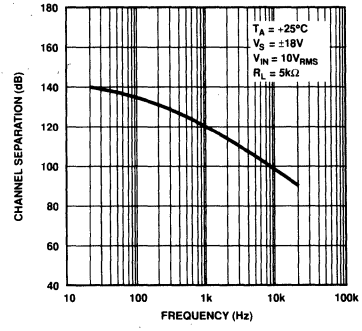
SSM-2402 SWITCHING TIME vs TEMPERATURE



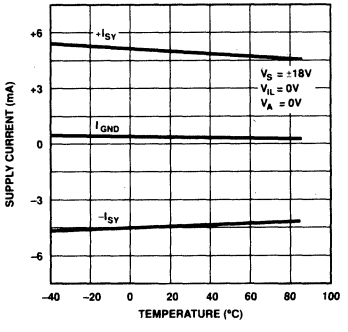
SSM-2412 SWITCHING TIME vs TEMPERATURE



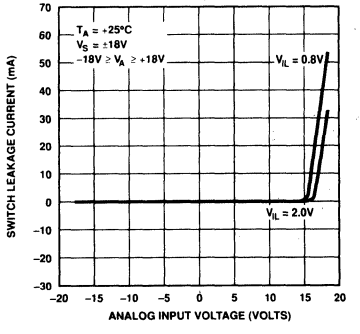
CHANNEL SEPARATION vs FREQUENCY



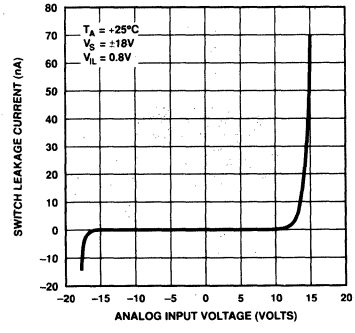
SUPPLY CURRENT vs TEMPERATURE



OVERVOLTAGE CHARACTERISTICS



LEAKAGE CURRENT vs ANALOG VOLTAGE



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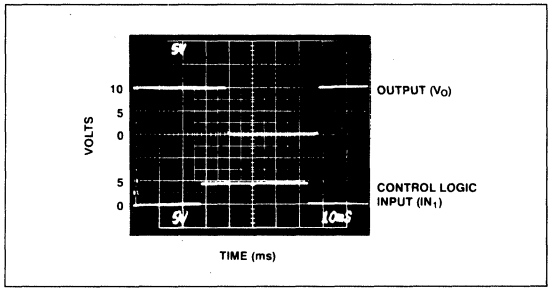
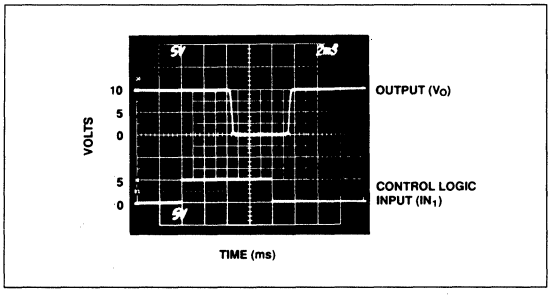
TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

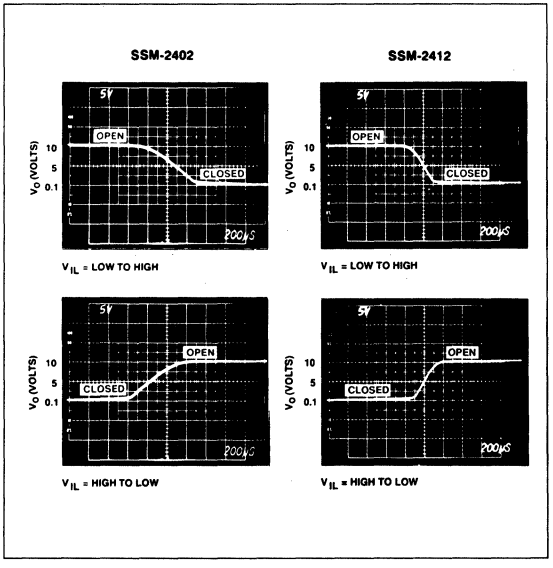
SSM-2402 T_{ON}/T_{OFF} SWITCHING RESPONSE



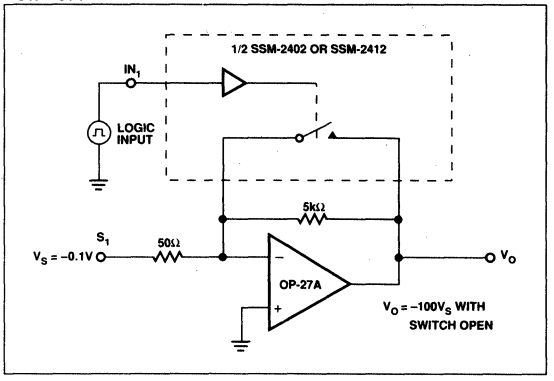
SSM-2412 T_{ON}/T_{OFF} SWITCHING RESPONSE



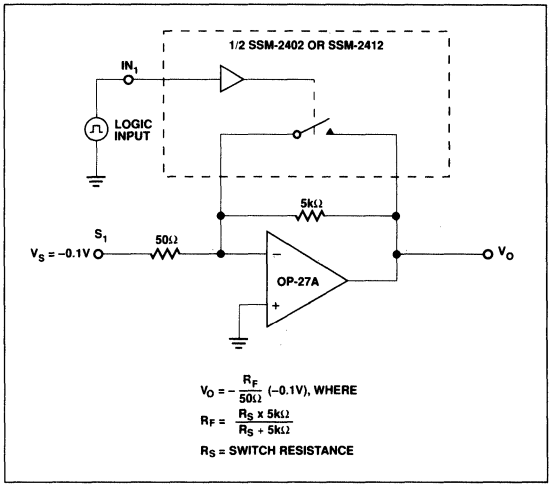
SWITCHING ON/OFF TRANSITION



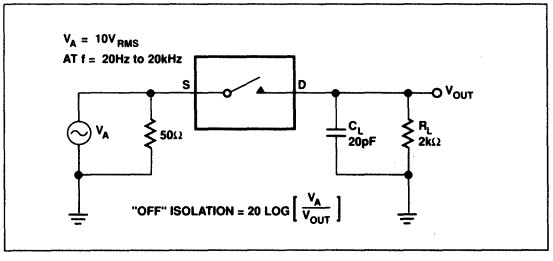
T_{ON}/T_{OFF} SWITCHING RESPONSE TEST CIRCUIT



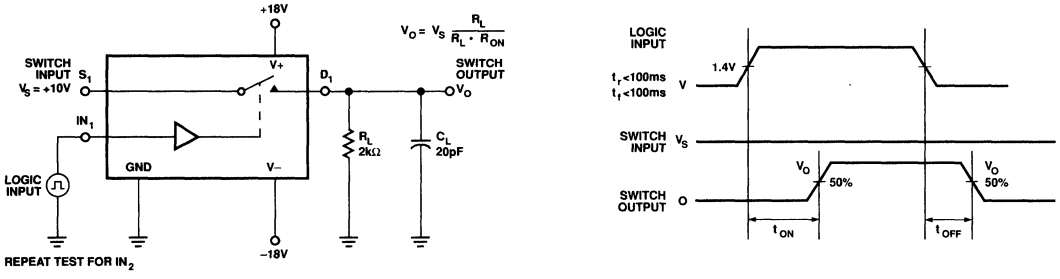
SWITCH ON/OFF TRANSITION TEST CIRCUIT



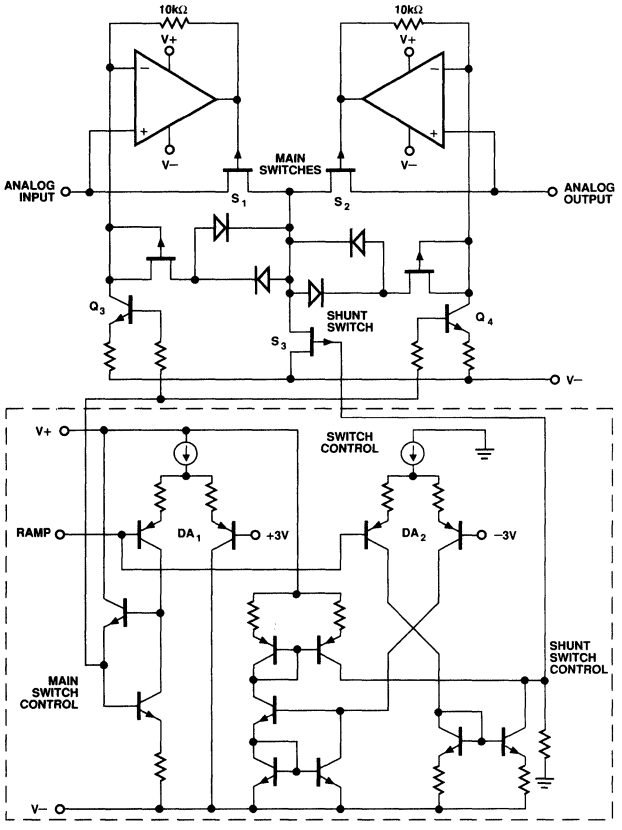
"OFF" ISOLATION TEST CIRCUIT



SWITCHING TIME TEST CIRCUIT



SIMPLIFIED SCHEMATIC



7

APPLICATIONS INFORMATION

FUNCTIONAL SECTIONS

Each half of the SSM-2402/2412 are made up of three major functional blocks:

1. **"T" Switch**
   Consists of JFET switches S_1 and S_2 in series as the main switches and switch S_3 as a shunt.

2. **Ramp Generator**
   Generates a ramp voltage on command of the Control Input (see Figure 1). A LOW-to-HIGH TTL input at Control Input initiates a ramp that goes from approximately –7V to +7V in 12ms for the SSM-2402, and 4ms for the SSM-2412. Conversely, a HIGH-to-LOW TTL transition at Control Input will cause a downward ramp from approximately +7V to –7V in 12ms for the SSM-2402, and 4ms for the SSM-2412. The Ramp Generator also supplies the +3V and –3V reference levels for Switch Control.

3. **Switch Control**
   The ramp from the Ramp Generator section is applied to two differential amplifiers (DA_1 and DA_2) in the Switch Control block. (See Simplified Schematic). One amplifier is referenced to –3V and the other is referenced to +3V. Switch Control Outputs are:

   - **Main Switch Control** – Drives two 0.25mA current sources that control the inverting inputs of each op amp. When ON, the current sources cause a gate-to-source voltage of approximately 2.5V which is sufficient to turn off S_1 and S_2. When the current sources from Main Switch Control are OFF, each op amp acts as a unity-gain follower (V_{GS} = 0) and both switches (S_1 and S_2) will be ON.
   - **Shunt Switch Control** – Controls the Shunt Switch of the "T" configuration.

SWITCH OPERATION

To see how the SSM-2402/2412 switches work, first consider an OFF-to-ON transition. The Control Input is initially LOW and the Ramp Output is at approximately –7V. The Main Switch Control is HIGH which drives current sources Q_3 and Q_4 to 0.25mA each. These currents generate 2.5V gate-to-source back bias for each JFET switch (S_1 and S_2) which holds them OFF.

The Shunt Switch Control is negative which holds the shunt JFET S_3 ON. Undesired feedthrough signals in the series JFET switches S_1 and S_2 are shunted to the negative supply rail through S_3.

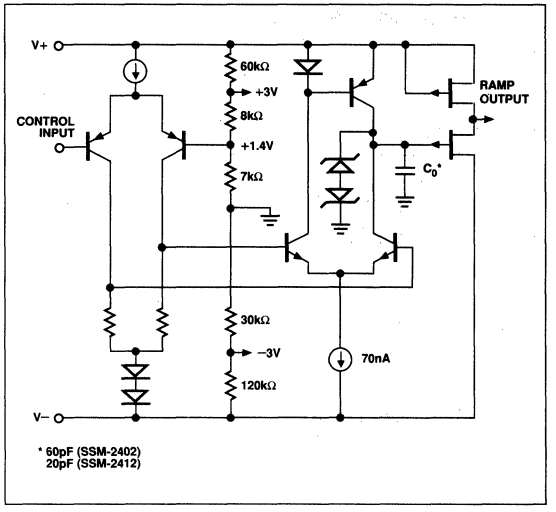


FIGURE 1: *RAMP Generator*

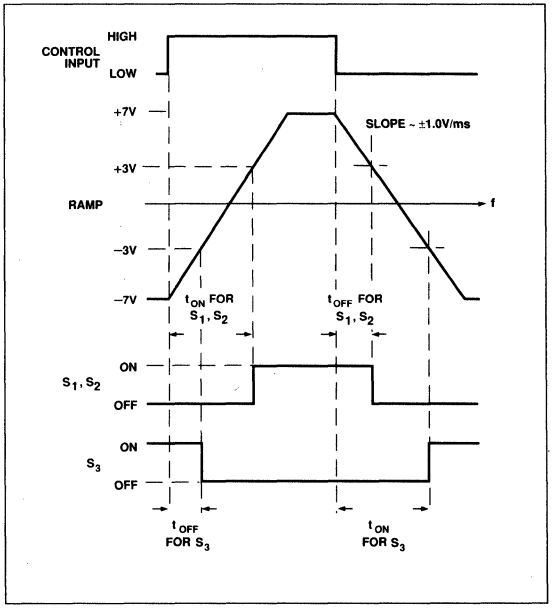


FIGURE 2: *Switch Control*

When the Control Input goes from LOW to HIGH, the Ramp Generator slews in the positive direction as shown in Figure 2. When the ramp goes more positive than –3V, the Shunt Switch Control is pulled positive by differential amplifier DA_2 which thereby puts shunt switch S_3 into the OFF state. Note that S_1 and S_2 are still OFF, so at this time all three switches in the "T" are OFF.

When the Ramp Output reaches +3V, and the drive for the Main Switch Control output is gated OFF by differential amplifier DA_1, current sources Q_3 and Q_4 go to the OFF state and the V_{GS} of each main switch goes to zero. The high-speed op amp followers provide essentially zero gate-to-source voltage over the full audio signal range; this in turn assures a constant low impedance in the ON state over the full audio signal range. Total time to turn on the SSM-2402 switch is approximately 10.0ms and 3.5ms for the SSM-2412.

In systems using a large number of separate switches, there are advantages to having faster switching into OFF state than into the ON state. Break-before-make can be maintained at the system level. To see how the SSM-2402/2412 guarantee break-before-make, consider the ON-to-OFF transition.

A Control Input LOW initiates the ON-to-OFF transition. The Ramp Generator integrates down from approximately +7V towards –7V. As the ramp goes through +3V, the comparator controlling the Main Switches (S_1 and S_2) goes HIGH and turns on current sources Q_3 and Q_4 which thereby puts S_1 and S_2 into the OFF state. At this time, all switches in the "T" are OFF. When the ramp integrates down to –3V, the Shunt Switch Control changes state and pulls shunt switch S_3 into the ON state. This completes the ON-to-OFF transistion; S_1 and S_2 are OFF, and S_3 is ON to shunt away any undesired feedthrough. Note though that the ON-to-OFF time for main switches S_1 and S_2 is only the time interval required for the ramp to go from +7V to +3V, about 4ms for the SSM-2402, and 1.5ms for the SSM-2412. The time to turn on is about 2.5 times as long as the time to turn off.

The SSM-2402/2412 are much more than a simple single solid-state switches. The "T" configuration provides superb OFF-isolation through shunting of feedthrough via shunt switch S_3. Break-before-make is inherent in the design. The ramp provides a controlled gating action that softens the ON/OFF transitions. Distortion is minimized by holding zero gate-to-source voltage for the two main FET switches, S_1 and S_2, using the two op amp followers. Figure 3 shows a distortion comparison between the SSM-2402 and a typical CMOS switch. In summary, the SSM-2402/2412 are designed specifically for high-performance audio system usage.

OVERVOLTAGE PROTECTION

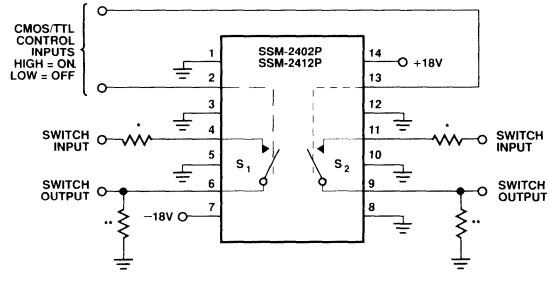
The SSM-2402/2412 are designed to guarantee correct operation with inputs of up to ±14.2V with ±18V supplies. The switch input should never be forced to go beyond the supply rails. In the OFF condition, if the inputs exceeds +14.2V, there is a risk of turning the respective input pass FET "ON." When the input voltage rises to within 3.8V of the positive supply, the op amp follower saturates and will not be able to maintain the full 2.5V of back bias on the gate-to-source junction. Under this condition, current will flow from the input through the shunt FET to the negative supply. This current is substantial, but is limited by the FET I_{DSS}. Although this current will not damage the device, there is a danger of also turning on the output pass FET, especially if the output is close to the negative rail.

This risk of signal "breakthrough" for inputs above +14.2V can be eliminated by using a source resistor of 100-500Ω in series with the analog input to provide additional current limiting.

Near the negative supply, transistors Q_3 and Q_4 saturate and can no longer keep the switch OFF. Signal breakthrough cannot happen, but the danger here is latch-up via a path to V– through the shunt FET. Additional circuitry (not shown) has been incorporated to turn OFF the shunt FET under these conditions, and the potential for latch-up is thereby eliminated.

7

TYPICAL CONFIGURATION



* OPTIONAL INPUT RESISTORS
SEE SECTION ON OVERVOLTAGE PROTECTION

** OPTIONAL LOAD RESISTORS
LOWER VALUES WILL MINIMIZE "CLICKS" BUT WITH A $10V_{RMS}$ INPUT
IT IS RECOMMENDED THAT THEY BE GREATER THAN 2kΩ

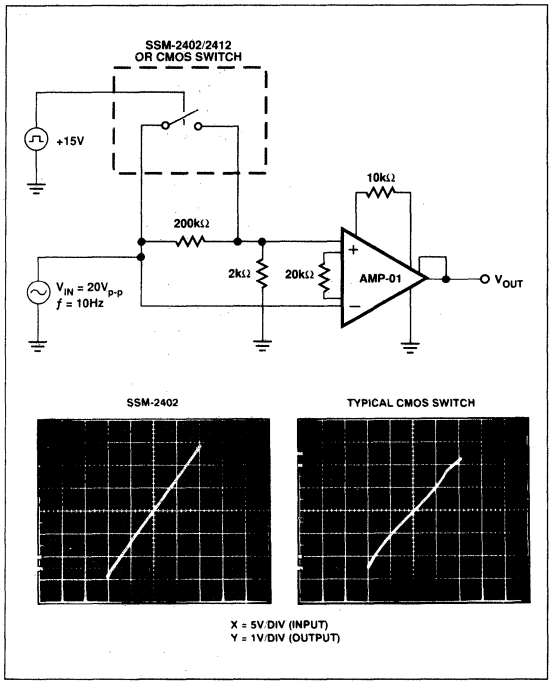


FIGURE 3: *Comparison of the SSM-2402 and Typical CMOS Switch for Distortion*

DIGITALLY-CONTROLLED ATTENUATOR

Figure 4 shows the usual approach to digitally-controlled attenuation. With S_1 closed, the signal passes unattenuated to the output. With S_1 open and S_2 closed, the signal is attenuated by R_1 and R_2. The advantage of this configuration is that the attenuator current does not have to flow through the switches. The disadvantage is that the output is undefined during the switching period, which can be several milliseconds.

The low distortion characteristics of the SSM-2402/2412 enable the alternate arrangement of Figure 5 to be used. Now only one switch is required to change between two gains, and there is always a signal path to the output. Values for R_2 will typically be in the low kilohm range.

For more gain steps and higher attenuation, the ladder arrangement of Figure 6 can be used. This enables a wide dynamic range to be achieved without the need for large value resistors, which would result in degradation of the noise performance.

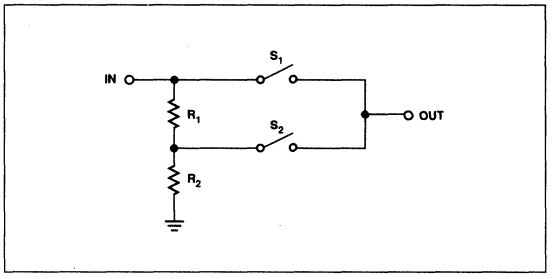


FIGURE 4

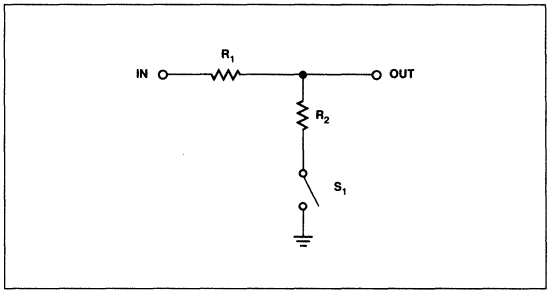


FIGURE 5

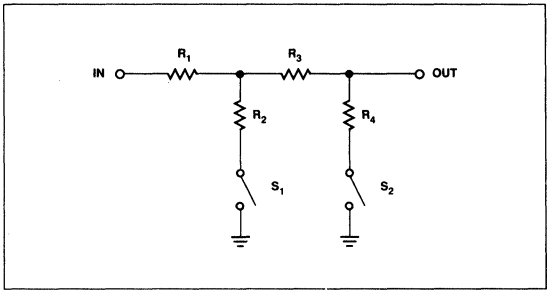


FIGURE 6

ANALOG DEVICES

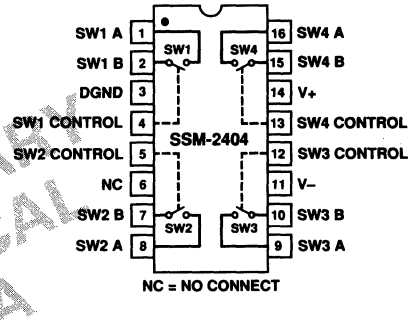
Quad Audio Switch

SSM-2404

FEATURES

- **"Clickless" Bilateral Audio Switching**
- **Four SPST Switches in a 16-Pin Package**
- **Ultralow THD+N: 0.0009% @ 1 kHz (V_{IN} = 2 V rms, R_L = 100 kΩ)**
- **Low Charge Injection: 35 pC**
- **High OFF Isolation: 100 dB**
- **Low ON Resistance: 28 Ω**
- **Low Supply Current: 900 μA**
- **Single or Dual Supply Operation: +11 V to +24 V or ±5.5 V to ±12 V**
- **Guaranteed Break-Before-Make**
- **TTL and CMOS Compatible Logic Inputs**
- **Low Cost-Per-Switch**

PIN CONNECTIONS



NC = NO CONNECT

GENERAL DESCRIPTION

The SSM-2404 integrates four SPST analog switches in a single 16-pin package. Developed specifically for high performance audio applications, distortion and noise are negligible over the full operating range of 20 Hz to 20 kHz. With very low charge injection of 35 pC, "clickless" audio switching is possible, even under the most demanding conditions.

Switch control is realized by conventional TTL or CMOS logic. Guaranteed "break-before-make" operation assures that all switches in a large system will open before any switch reaches the ON state.

Single or dual supply operation is possible. Additional features include 100 dB OFF isolation, 28 Ω ON resistance, and a wide signal handling range. Although optimized for virtual ground switching, the SSM-2404 maintains good audio performance even under low load impedance conditions.

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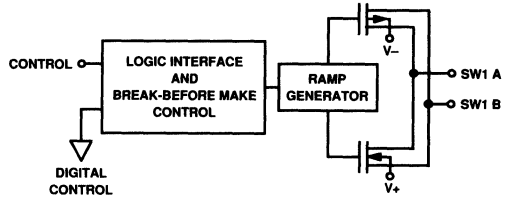
BLOCK DIAGRAM OF ONE SWITCH CHANNEL



SSM-2404—SPECIFICATIONS (V_S = ±12 V, T_A = +25°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Type	Max	Units
AUDIO PERFORMANCE						
Total Harmonic Distortion Plus Noise	THD+N	@ 1 kHz, with 80 kHz Filter, R_L = 100 kΩ, V_{IN} = 2 V rms		0.0009		%
Spectral Noise Density	e_n	20 Hz to 20 kHz		0.8		nV/√Hz
Wideband Noise Density	e_n p–p	20 Hz to 20 kHz		0.6		μV p–p
ANALOG SIGNAL SECTION						
Analog Voltage Range	V_A	V_{INH} = 2 V, I_A = ±2 mA		±12		V
Analog Current Range	I_A	V_{INH} = 2 V, V_A = 0 V		±10		mA
ON Resistance	R_{ON}	I_A = ±10 mA, V_A = 7.1 V		28		Ω
R_{ON} Matching	R_{ON} Match	I_A = ±10 mA, V_A = 0 V		1		%
ON Leakage Current	$I_{S(ON)}$	V_A = 7.1 V		0.1		nA
OFF Leakage Current	$I_{S(OFF)}$	V_A = 7.1 V		0.1		nA
Charge Injection	Q			35		pC
ON-State Input Capacitance	C_{ON}	V_A = 5 V rms, f = 5 kHz		31		pF
OFF-State Input Capacitance	C_{OFF}	V_A = 5 V rms, f = 5 kHz		17		pF
OFF Isolation	$I_{SO(OFF)}$	V_A = 7.1 V, 20 Hz–20 kHz		100		dB
Channel-to-Channel Crosstalk	C_T	V_A = 7.1 V, 20 Hz–20 kHz		100		dB
CONTROL SECTION						
Digital Input High	V_{INH}	T_A = –40°C to +85°C		2.0		V
Digital Input Low	V_{INL}	T_A = –40°C to +85°C		0.8		V
Turn-On Time[1]	t_{ON}	See Test Circuit		8		ms
Turn-Off Time[2]	t_{OFF}	See Test Circuit		5		ms
Break-Before-Make Time Delay	t_{OFF}–t_{ON}			3		ms
Logic Input Current						
Logic HI		V_{INH} = 2 V		1.3		nA
Logic LO		V_{INL} = 0.8 V		1.0		nA
POWER SUPPLY						
Supply Voltage Range	V_S	Single Supply	+11		+24	V
		Dual Supply	±5.5		±12	V
Positive Supply Current	I_{SY+}	All Channels On		0.9		mA
Negative Supply Current	I_{SY-}	All Channels On		–0.6		mA
Ground Current		All Channels On		–0.3		mA

NOTES
[1]Turn-on time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the final value.
[2]Turn-off time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the initial value.
Specifications subject to change without notice.

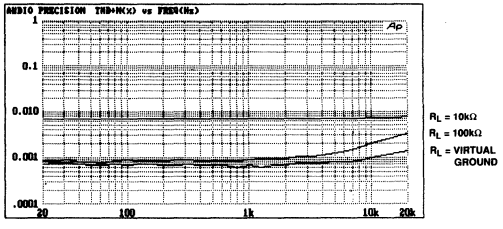
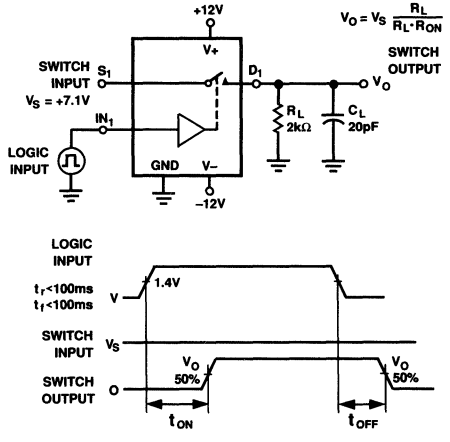


Figure 1. THD+N vs. Frequency (V_S = ±12 V, V_{IN} = 2 V rms, with 80 kHz Filter)



SSM-2404 Switch Timing Circuit

Special Function Video Products
Contents

Selection Guide
Special Function Video Products

CRT Geometry Correction Selection Guide

Model	Bandwidth MHz	Slew Rate	Peak Signal Amplitude V_P, I_P	Power Supplies Volts	Page	Comments
AD539	60		±1 mA Out, ±2 V In	±5 to ±15	8-3	2 CH, Current Output
AD633	1	20 V/μs	±10 V	±8.5 to ±15	8-11	V_{OUT}
AD734	10	450 V/μs	±10 V	±8.5 to ±15	8-21	V_{OUT}
AD834	>500		±4 mA Out, ±1 V In	±5	8-33	Current Output
DAC8408	1	1 mA/μs	±1 mA Out, ±10 V In	+5	8-49	4 CH, I_{OUT}, Parallel Data In
DAC8800	DC		V_{SS} to V_{DD}−4 V	$(V_{DD}-V_{SS})<18$	8-63	8 CH, 10 kΩ, R_{OUT}, Serial Data In
DAC8840	1	1.3 V/μs	±3 V	V_{DD} = +5, V_{SS} = −5	8-77	8 CH, V_{OUT}, Serial Data In
DAC8841	1	1.3 V/μs	0 V to +3 V	V_{DD} = +5, V_{SS} = −5	8-87	8 CH, V_{OUT}, Serial Data In

Other Special Function Video Products

Model	Page	Comments
AD720	8-19	RGB to NTSC and PAL Converter
AD9300	8-41	4 × 1 Video Multiplexer

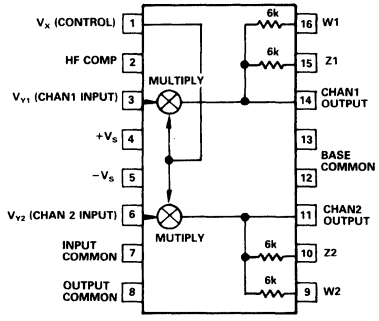
Wideband Dual-Channel Linear Multiplier/Divider

AD539

FEATURES
Two Quadrant Multiplication/Division
Two Independent Signal Channels
Signal Bandwidth of 60MHz (I_{OUT})
Linear Control Channel Bandwidth of 5MHz
Low Distortion (to 0.01%)
Fully-Calibrated, Monolithic Circuit

APPLICATIONS
Precise High Bandwidth AGC and VCA Systems
Voltage-Controlled Filters
Video-Signal Processing
High-Speed Analog Division
Automatic Signal-Leveling
Square-Law Gain/Loss Control

PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD539 is a low-distortion analog multiplier having two identical signal channels (Y1 and Y2), with a common X-input providing linear control of gain. Excellent ac characteristics up to video frequencies and a 3dB bandwidth of over 60MHz are provided. Although intended primarily for applications where speed is important the circuit exhibits good static accuracy in "computational" applications. Scaling is accurately determined by a band-gap voltage reference and all critical parameters are laser-trimmed during manufacture.

The full bandwidth can be realized over most of the gain range using the AD539 with simple resistive loads of up to 100Ω. Output voltage is restricted to a few hundred millivolts under these conditions. Using external op amps such as the AD5539 in conjunction with the on-chip scaling resistors, accurate multiplication can be achieved, with bandwidths typically as high as 50MHz.

The two channels provide flexibility. In single-channel applications they may be used in parallel, to double the output current, or in series, to achieve a square-law gain function with a control range of over 100dB, or differentially, to reduce distortion. Alternatively, they may be used independently, as in audio stereo applications, with low crosstalk between channels. Voltage-controlled filters and oscillators using the "state-variable" approach are easily designed, taking advantage of the dual channels and common control. The AD539 can also be configured as a divider with signal bandwidths up to 15MHz.

Power consumption is only 135mW using the recommended ±5V supplies. The AD539 is available in three versions: the "J" and "K" grades are specified for 0 to +70°C operation and "S" grade is guaranteed over the extended range of −55°C to +125°C. The J and K grades are available in either a hermetic ceramic DIP (D) or a low cost plastic DIP (N), while the S grade is available only in ceramic. AD539 J-grade chips are also available.

DUAL SIGNAL CHANNELS

The signal voltage inputs, V_{Y1} and V_{Y2}, have nominal full-scale (FS) values of ±2V with a peak range to ±4.2V (using a negative supply of 7.5V or greater). For video applications where differential phase is critical a reduced input range of ±1 volt is recommended, resulting in a phase variation of typically ±0.2° at 3.579MHz for full gain. The input impedance is typically 400kΩ shunted by 3pF. Signal channel distortion is typically well under 0.1% at 10kHz and can be reduced to 0.01% by using the channels differentially.

COMMON CONTROL CHANNEL

The control channel accepts positive inputs, V_X, from 0 to +3V FS, ±3.3V peak. The input resistance is 500Ω. An external, grounded capacitor determines the small-signal bandwidth and recovery time of the control amplifier; the minimum value of 3nF allows a bandwidth at mid-gain of about 5MHz. Larger compensation capacitors slow the control channel but improve the high-frequency performance of the signal channels.

FLEXIBLE SCALING

Using either one or two external op amps in conjunction with the on-chip 6kΩ scaling resistors, the output currents (nominally ±1mA FS, ±2.25mA peak) can be converted to voltages with accurate transfer functions of $V_W = -V_X V_Y/2$, $V_W = -V_X V_Y$ or $V_W = -2V_X V_Y$ (where inputs V_X and V_Y and output V_W are expressed in volts), with corresponding full-scale outputs of ±3V, ±6V and ±12V. Alternatively, low-impedance grounded loads can be used to achieve the full signal bandwidth of 60MHz, in which mode the scaling is less accurate.

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AD539—SPECIFICATIONS ($@ T_A = 25°C, V_S = \pm 5V$, unless otherwise specified)

Parameter	Conditions	AD539J Min	AD539J Typ	AD539J Max	AD539K Min	AD539K Typ	AD539K Max	AD539S Min	AD539S Typ	AD539S Max	Units
SIGNAL-CHANNEL DYNAMICS											
Minimal Configuration	Reference Figure 6a										
Bandwidth, −3dB	$R_L = 50\Omega, C_C = 0.01\mu F$	30	60		30	60		30	60		MHz
Maximum Output	$+0.1V < V_X < +3V, V_{Yac} = 1V$ rms		−10			−10			−10		dBm
Feedthrough, f<1MHz	$V_X = 0, V_{Yac} = 1.5V$ rms		−75			−75			−75		dBm
f = 20MHz			−55			−55			−55		dBm
Differential Phase Linearity											
$-1V < V_{Ydc} < +1V$	f = 3.58MHz, $V_X = +3V$,		±0.2			±0.2			±0.2		Degrees
$-2V < V_{Ydc} < +2V$	$V_{Yac} = 100mV$		±0.5			±0.5			±0.5		Degrees
Group Delay	$V_X = +3V, V_{Yac} = 1V$ rms, f = 1MHz		4			4			4		ns
Standard Dual-Channel Multiplier	Reference Figure 2										
Maximum Output	$V_X = +3V, V_{Yac} = 1.5V$ rms		4.5			4.5			4.5		V
Feedthrough, f<100kHz	$V_X = 0, V_{Yac} = 1.5V$ rms		1			1			1		mV rms
Crosstalk (CH1 to CH2)	$V_{Y1} = 1V$ rms, $V_{Y2} = 0$										
	$V_X = +3V$, f<100kHz		−40			−40			−40		dB
RTO Noise, 10Hz to 1MHz	$V_X = +1.5V, V_Y = 0$, Figure 2		200			200			200		$nV/\sqrt{Hz}$
THD + Noise, $V_X = +1V$,	f = 10kHz, $V_{Yac} = 1V$ rms		0.02			0.02			0.02		%
$V_Y = +3V$	f = 10kHz, $V_{Yac} = 1V$ rms		0.04			0.04			0.04		%
Wide Band Two-Channel Multiplier	Figure 2										
Bandwidth, −3dB (LH0032)	$+0.1V < V_X < +3V, V_{Yac} = 1V$ rms		25			25			25		MHz
Maximum Output $V_X = +3V$	$V_{Yac} = 1.5V$ rms, f = 3MHz		4.5			4.5			4.5		V rms
Feedthrough $V_X = 0V$	$V_{Yac} = 1.0V$ rms, f = 3MHz		14			14			14		mV rms
Wide Band Single Channel VCA											
(AD5539)	Reference Figure 8										
Bandwidth, −3dB	$+0.1V < V_X < +3V, V_{Yac} = 1V$ rms		50			50			50		MHz
Maximum Output	75Ω Load		±1			±1			±1		V
Feedthrough	$V_X = -0.01V$, f = 5MHz		−54			−54			−54		dB
CONTROL CHANNEL DYNAMICS											
Bandwidth, −3dB	$C_C = 3000pF, V_X dc = +1.5V$, $V_X ac = 100mV$ rms		5			5			5		MHz
SIGNAL INPUTS, V_{Y1} & V_{Y2}											
Nominal Full-Scale Input			±2			±2			±2		V
Operational Range, Degraded Performance	$-V_S \leq 7V$	**±4.2**			**±4.2**			**±4.2**			V
Input Resistance			400			400			400		kΩ
Bias Current			10	**30**		10	**20**		10	**30**	μA
Offset Voltage	$V_X = +3V, V_Y = 0$		5	**20**		5	**10**		5	**20**	mV
(T_{min} to T_{max})			10			5			15	**35**	mV
Power Supply Sensitivity	$V_X = +3V, V_Y = 0$		2			2			2		mV/V
CONTROL INPUT, V_X											
Nominal Full-Scale Input			+3.0			+3.0			+3.0		V
Operational Range, Degraded Performance		**+3.2**			**+3.2**			**+3.2**			V
Input Resistance[1]			500			500			500		Ω
Offset Voltage			1	**4**		1	**2**		1	**4**	mV
(T_{min} to T_{max})			3			2			2	**5**	mV
Power Supply Sensitivity			30			30			30		μV/V
Gain	(Figure 2)										
Absolute Gain Error	$V_X = +0.1V$ to $+3.0V$ and		0.2	**0.4**		0.1	**0.2**		0.2	**0.4**	dB
(T_{min} to T_{max})	$V_Y = \pm 2V$		0.3			0.15			0.25	**0.5**	dB
CURRENT OUTPUT[1]											
Full-Scale Output Current	$V_X = +3V, V_Y = \pm 2V$		±1			±1			±1		mA
Peak Output Current	$V_X = +3.3V, V_Y = \pm 5V, V_S = \pm 7.5V$	±2	±2.8		±2	±2.8		±2	±2.8		mA
Output Offset Current	$V_X = 0, V_Y = 0$		0.2	**1.5**		0.2	**1.5**		0.2	**1.5**	μA
Output Offset Voltage[2]	Figure 2, $V_X = 0, V_Y = 0$		3	**10**		3	**10**		3	**10**	mV
Output Resistance[1]			1.2			1.2			1.2		kΩ
Scaling Resistors											
CH1	Z1, W1 to CH1		6			6			6		kΩ
CH2	Z2, W2 to CH2		6			6			6		kΩ
VOLTAGE OUTPUTS, V_{W1} & V_{W2}[2]	(Figure 2)										
Multiplier Transfer Function,											
Either Channel			$V_W = -V_X \cdot V_Y / V_U$			$V_W = -V_X \cdot V_Y / V_U$			$V_W = -V_X \cdot V_Y / V_U$		
Multiplier Scaling Voltage, V_U		**0.98**	1.0	**1.02**	**0.99**	1.0	**1.01**	**0.98**	1.0	**1.02**	V
Accuracy			0.5	**2**		0.5	**1**		0.5	**2**	%
(T_{min} to T_{max})			1			0.5			1.0	**3**	%
Power Supply Sensitivity			0.04			0.04			0.04		%/V
Total Multiplication Error[3]	$V_X <= +3V, -2V < V_Y < 2V$		1	**2.5**		0.6	**1.5**		1	**2.5**	% FSR
T_{min} to T_{max}			2			1			2	**4**	%
Control Feedthrough	$V_X = 0$ to $+3V, V_Y = 0$		25	**60**		15	**30**		15	**60**	mV
T_{min} to T_{max}			30			15			60	**120**	mV
TEMPERATURE RANGE											
Rated Performance		0		+70	0		+70	−55		+125	°C
POWER SUPPLIES											
Operational Range		±4.5		±15	±4.5		±15	±4.5		±15	V
Current Consumption											
$+V_S$			8.5	**10.2**		8.5	**10.2**		8.5	**10.2**	mA
$-V_S$			18.5	**22.2**		18.5	**22.2**		18.5	**22.2**	mA
PACKAGE OPTIONS[4]											
Plastic (N-16)			AD539JN			AD539KN			AD539SD		
TO-116 (D-16)			AD539JD			AD539KD			AD539SD/883B		
Chips			AD539J Chips								

NOTES

[1]Resistance value and absolute current outputs subject to 20% tolerance.

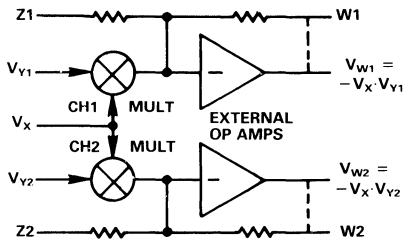
[2]Spec assumes the external op amp is trimmed for negligible input offset.

[3]Includes all errors.

[4]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.



AD539 Functional Block Diagram

CIRCUIT DESCRIPTION

Figure 1 is a simplified schematic of the AD539. Q1-Q6 are large-geometry transistors designed for low distortion and low noise. Emitter-area scaling further reduces distortion: Q1 is 3 times larger than Q2; Q4, Q5 are each 3 times larger than Q3, Q6, and these transistors are twice as large as Q1, Q2. A stable reference current I_{REF} = 1.375mA is produced by a band-gap reference circuit and applied to the common emitter node of a *controlled-cascode* formed by Q1 and Q2. When V_X = 0, all of I_{REF} flows in Q1, due to the action of the high-gain control amplifier which lowers the voltage on the base of Q2. As V_X is raised the fraction of I_{REF} flowing in Q2 is forced to balance the control current, V_X/2.5k. At the full-scale value of V_X (+3V) this fraction is 0.873. Since the bases of Q1, Q4 and Q5 are at ground potential and the bases of Q2, Q3 and Q6 are commoned, all three controlled-cascodes divide the current applied to their emitter nodes in the same proportion. The control loop is stabilized by the external capacitor, C_C.

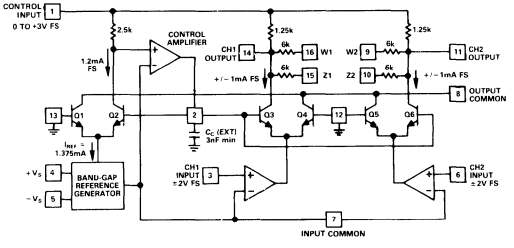


Figure 1. Simplified Schematic of AD539 Multiplier

The signal voltages V_{Y1} and V_{Y2} (generically referred to as V_Y) are first converted to currents by voltage-to-current converters with a g_m of 575μmhos; thus, the full-scale input of ±2V becomes a current of ±1.15mA, which is superimposed on a bias of 2.75mA, and applied to the common emitter node of controlled cascode Q3-Q4 or Q5-Q6. As just explained, the proportion of this current steered to the output node is linearly dependent on V_X. Thus for full-scale V_X and V_Y inputs, a signal of ±1mA (0.873 × ±1.15mA) and a bias component of 2.4mA (0.873 × 2.75mA) appear at the output. The bias component absorbed by the 1.25k resistors also connected to V_X, and the resulting signal current can be applied to an external load resistor (in which case scaling is not accurate) or can be forced into either or both of the 6kΩ feedback resistors (to the Z and W nodes) by an external op amp. In the latter case, scaling accuracy is guaranteed.

GENERAL RECOMMENDATIONS

The AD539 is a high speed circuit and requires considerable care to achieve its full performance potential. A high-quality ground plane should be used with the device either soldered directly into the board or mounted in a low-profile socket. In the figures used here an open triangle denotes a *direct, short* connection to this ground plane; pins 12 and 13 are especially prone to unwanted signal pick-up. Power supply decoupling capacitors of 0.1μF to 1μF should be connected from pins 4 and 5 to the ground plane. In applications using external high-speed op amps, separate supply decoupling should be used. It is good practice to insert small (10Ω) resistors between the primary supply and the decoupling capacitor.

The control amplifier compensation capacitor, C_C, should likewise have short leads to ground and a minimum value of 3nF. Unless maximum control bandwidth is esssential it is advisable to use a larger value of 0.01μF to 0.1μF to improve the signal channel phase response, high-frequency crosstalk and high-frequency distortion. The control bandwidth is inversely proportional to this capacitance, typically 2MHz for C_C = 0.01μF, V_X = 1.7V. The bandwidth and pulse response of the control channel can be improved by using a feedforward capacitor of 5% to 20% the value of C_C between pins 1 and 2. Optimum transient response will result when the rise/fall time of V_X are commensurate with the control-channel response time.

V_X should not exceed the specified range of 0 to +3V. The ac gain is zero for V_x<0 but there remains a feedforward path (see Figure 1) causing control feedthrough. Recovery time from negative values of V_X can be improved by adding a small-signal Schottky diode with its cathode connected to pin 2 and its anode grounded. This constrains the voltage swing on C_C. Above V_X = +3.2V, the ac gain limits at its maximum value, but any overdrive appears as control feedthrough at the output.

The power supplies to the AD539 can be as low as ±4.5V and as high as ±16.5V. The maximum allowable range of the signal inputs, V_Y, is approximately 0.5V above $+V_S$; the minimum value is 2.5V above $-V_S$. To accommodate the peak specified inputs of ±4.2V the supplies should be nominally +5V and −7.5V. While there is no performance advantage in raising supplies above these values, it may often be convenient to use the same supplies as for the op amps. The AD539 can tolerate the excess voltage with only a slight effect on dc accuracy but dissipation at ±16.5V can be as high as 535mW and some form of heat-sink is essential in the interests of reliability.

TRANSFER FUNCTION

In using any analog multiplier or divider careful attention must be paid to the matter of *scaling*, particularly in computational applications. To be *dimensionally consistent* a scaling voltage must appear in the transfer function, which, for each channel of the AD539 in the standard multiplier configuration (Figure 2) is

$$V_W = -V_X V_Y / V_U$$

where the inputs V_X and V_Y, the output V_W and the scaling voltage V_U are expressed in a consistent unit, usually volts. In this case, V_U is fixed by the design to be 1V and it is often acceptable in the interest of simplification to use the less rigorous expression

$$V_W = -V_X V_Y$$

where it is understood that *all signals must be expressed in volts*, that is, they are rendered dimensionless by division by (1V).

8

The accuracy specifications for V_U allow the use of either of the two feedback resistors supplied with each channel, since these are very closely matched, or they may be used in parallel to halve the gain (double the effective scaling voltage), when

$$V_W = -V_X V_Y/2.$$

When an external load resistor, R_L, is used the scaling is no longer exact since the internal thin-film resistors, while trimmed to high *ratiometric* accuracy, have an absolute tolerance of 20%. However, the nominal transfer function is

$$V_W = -V_X V_Y/V_U'$$

where the effective scaling voltage, V_U' can be calculated for each channel using the formula $V_U' = V_U (5R_L + 6.25)/R_L$, where R_L is expressed in kilohms. For example, when R_L = 100Ω, V_U' = 67.5V. Table II provides more detailed data for the case where both channels are used in parallel. The AD539 can also be used with no external load (output pin 11 or 14 open-circuit), when V_U' is quite accurately 5V.

BASIC MULTIPLIER CONNECTIONS

Figure 2 shows the connections for the standard two-channel multiplier, using op amps to provide useful output power and the AD539 feedback resistors to achieve accurate scaling. The transfer function for each channel is

$$V_W = -V_X V_Y$$

where inputs and outputs are expressed in volts (see TRANSFER FUNCTION). At the nominal full-scale inputs of V_X = +3V, V_Y = ±2V the full-scale outputs are ±6V. Depending on the choice of op amp, their supply voltages usually need to be about 2V more than the peak output. Thus, supplies of at least ±8V are required; the AD539 can share these supplies. Higher outputs are possible if V_X and V_Y are driven to their peak values of +3.2V and ±4.2V respectively, when the peak output is ±13.4V. This requires operating the op amps at supplies of ±15V. Under these conditions it is advisable to reduce the supplies to the AD539 to ±7.5V to limit its power dissipation; however, with some form of heat sinking it is permissible to operate the AD539 directly from ±15V supplies.

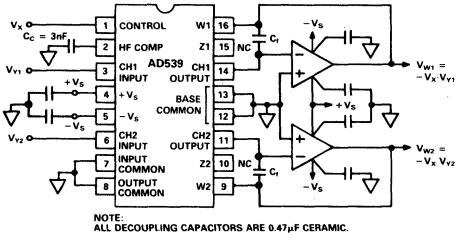


Figure 2. Standard Dual-Channel Multiplier

Viewed as a voltage-controlled amplifier, the decibel gain is simply

$$G = 20 \log V_X$$

where V_X is expressed in volts. This results in a gain of 10dB at V_X = +3.162V, 0dB at V_X = +1V, −20dB at V_X = +0.1V, and so on. In many ac applications the output offset voltage (for V_X = 0 or V_Y = 0) will not be of major concern; however, it can be eliminated using the offset nulling method recommended for the particular op amp, with $V_X = V_Y = 0$.

At small values of V_X the offset voltage of the control channel will degrade the gain/loss accuracy. For example, a ±1mV offset uncertainty will cause the nominal 40dB attenuation at V_X = +0.01V to range from 39.2dB to 40.9dB. Figure 3a shows the maximum gain error boundaries based on the guaranteed control-channel offset voltages of ±2mV for the AD539K and ±4mV for the AD539J. These curves include all scaling errors and apply to all configurations using the internal feedback resistors (W1 and W2; alternatively, Z1 and Z2).

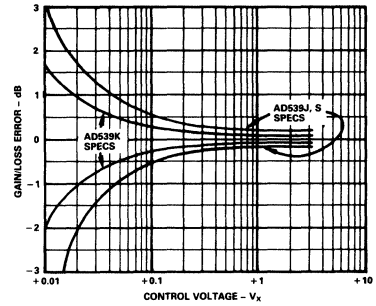


Figure 3a. Maximum ac Gain Error Boundaries

Distortion is a function of the signal input level (V_Y) and the control input (V_X). It is also a function of frequency, although in practice the op amp will generate most of the distortion at frequencies above 100kHz. Figure 3b shows typical results at f = 10kHz as a function of V_X with V_Y = 0.5 and 1.5V rms.

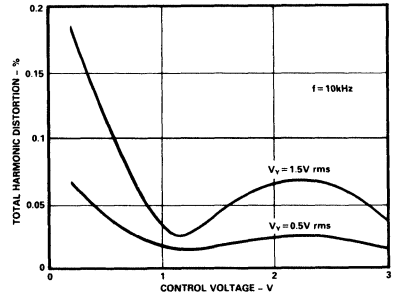


Figure 3b. Total Harmonic Distortion vs. Control Voltage

In some cases it may be desirable to alter the scaling. This can be achieved in several ways. One option is to use both the Z and W feedback resistors (see Figure 1) in parallel, in which case $V_W = -V_X V_Y/2$. This may be preferable where the output swing must be held at ±3V FS (±6.75V pk), for example, to allow the use of reduced supply voltages for the op amps. Alternatively, the gain can be doubled by connecting both channels in parallel and using only a single feedback resistor, in which case $V_W = -2V_X Y_Y$ and the full-scale output is ±12V. Another option is to insert a resistor in series with the control-channel input, permitting the use of a large (for example, 0 to +10V) control voltage. A disadvantage of this scheme is the need to

adjust this resistor to accommodate the tolerance of the nominal 500Ω input resistance at pin 1. The signal channel inputs can also be resistively attenuated to permit operation at higher values of V_Y, in which case it may often be possible to partially compensate for the response roll-off of the op amp by adding a capacitor across the upper arm of this attenuator.

Signal-Channel ac and Transient Response

The HF response is dependent almost entirely on the op amp. Note that the "noise gain" for the op amp in Figure 2 is determined by the value of the feedback resistor (6kΩ) and the 1.25kΩ control-bias resistors (Figure 1). Op amps with provision for external frequency compensation (such as the AD301 and AD518) should be compensated for a closed-loop gain of 6.

The layout of the circuit components is very important if low feedthrough and flat response at low values of V_X is to be maintained (see GENERAL RECOMMENDATIONS).

For wide-bandwidth applications requiring an output voltage swing greater than ±1V, the LH0032 hybrid op-amp is recommended. Figure 4a shows the HF response of the circuit of Figure 2 using this amplifier with V_Y = 1V rms and other conditions as shown in Table I. C_F was adjusted for 1dB peaking at V_X = +1V; the −3dB bandwidth exceeds 25MHz. The effect of signal feedthrough on the response becomes apparent at V_X = +0.01V. The minimum feedthrough results when V_X is taken slightly negative to ensure that the residual control-channel offset is exceeded and the dc gain is reliably zero. Measurements show that the feedthrough can be held to −90dB relative to full output at low frequencies and to −60dB up to 20MHz with careful board layout. The corresponding pulse response is shown in Figure 4b for a signal input of V_Y of ±1V and two values of V_X (+3V and +0.1V).

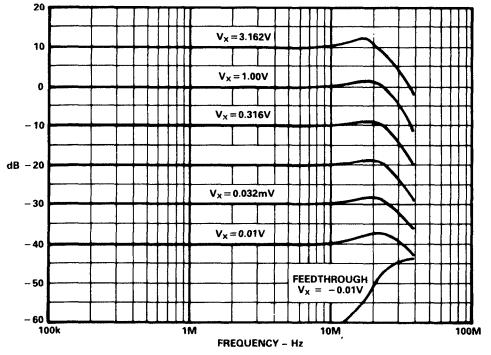
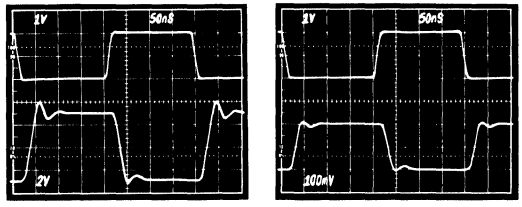


Figure 4a. Multiplier HF Response Using LH0032 Op Amps



V_X = +3V V_X = +0.1V

Figure 4b. Multiplier Pulse Response Using LH0032 Op Amps

Table I. Summary of Operating Conditions and Performance for the AD539 When Used with Various External Op-Amp Output Amplifiers

	AD711[1]	AD5539[2]	LH0032[1]
Op Amp Supply Voltages	±15V	±9V	±10V
Op Amp Compensation Capacitor	None	None	1-5pF
Feedback Capacitor, C_F	None	0.25-1.5pF	1-4pF
−3dB Bandwidth, V_X = +1V	900kHz	50MHz	25MHz
Load Capacitance	<1nF	<10pF	<100pF
HF Feedthrough, V_X = −0.01V, f = 5MHz	N/A	−54dB	−70dB
rms Output Noise, V_X = +1V, BW 10Hz-10kHz	50μV	40μV	30μV
V_X = +1V, BW 10Hz-5MHz	120μV	620μV	500μV

In all cases, 0.47μF ceramic supply-decoupling capacitors were used at each IC pin, the AD539 supplies were ±5V and the control-compensation capacitor C_C was 3nF.

NOTES
[1]For the circuit of Figure 2.
[2]For the circuit of Figure 8.

Minimal Wide-Band Configurations

The maximum bandwidth can be achieved using the AD539 with simple resistive loads to convert the output currents to voltages. These currents (nominally ±1mA FS, ±2.25mA pk, into short-circuit loads) are shunted by their source resistance of 1.25kΩ (each channel). Calculations of load power and effective scaling-voltage must allow for this shunting effect when using resistive loads. The output power is quite low in this mode, and the device behaves more like a voltage-controlled attenuator than a classical multiplier. The matching of gain and phase between the two channels is excellent. From dc to 10MHz the gains are typically within ±0.025dB (measured using precision 50Ω load resistors) and the phase difference within ±0.1°.

Table II. Summary of Performance for Minimal Configuration

Load Resistance	50Ω	75Ω	100Ω	150Ω	600Ω	O/C
FS Output Voltage	±92.6mV	±134mV	±172mV	±242mV	±612mV	±1V
	65.5mV rms	94.7mV rms	122mV rms	171mV rms	433mV rms	*
FS Output-Power in Load	0.086mW	0.12mW	0.15mW	0.195mW	0.312mW	–
	−10.5dBm	−9.2dBm	−8.3dBm	−7.1dBm	−5.05dBm	–
Pk Output Voltage	±210mV	±300mV	±388mV	±544mV	±1V	±1V
	148mV rms	212mV rms	274mV rms	385mV rms	*	*
Pk Output-Power in Load	0.44mW	0.6mW	0.75mW	1mW	±1V	±1V
	−7dBm	−4.4dBm	−2.5dBm	0dBm	*	*
Effective Scaling Voltage, V_U'	67.5V	46.7V	36.3V	25.8V	10.2V	5V

*Peak negative voltage swing limited by output compliance.

For a given load resistance the output power can be quadrupled by using both channels in parallel, as shown in Figure 5a. The small-signal silicon diode D connected between ground and pins 12 and 13 provides extra voltage compliance at the output nodes in the negative direction (to −1V at 25°C); it is not required if the output swing does not exceed −300mV. Table II compares performance for various load resistances, using this configuration.

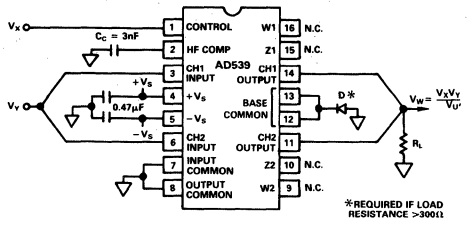


Figure 5a. Minimal Single-Channel Multiplier

Figure 5b shows the HF response for Figure 5a with the AD539 in a carefully-shielded 50Ω test-environment; the test system response was first characterized and this background removed by digital signal processing to show the inherent circuit response.

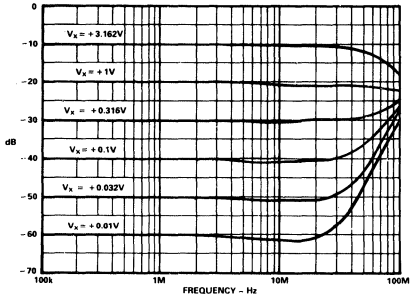


Figure 5b. HF Response in Minimal Configuration

In many applications *phase linearity* over frequency is important. Figure 5c shows the deviation from an ideal linear-phase response for a typical AD539 over the frequency range dc to 10MHz, for

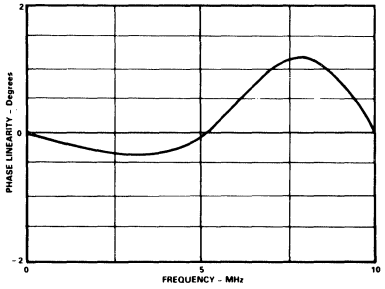


Figure 5c. Phase Linearity Error in Minimal Configuration

V_X = +3V; the peak deviation is slightly more than 1°. *Differential phase linearity* (the stability of phase over the signal window at a fixed frequency) is shown in Figure 5d for f = 3.579MHz and various values of V_X. The most rapid variation occurs for V_Y above +1V; in applications where this characteristic is critical, it is recommended that a ground-referenced, negative-going signal be used.

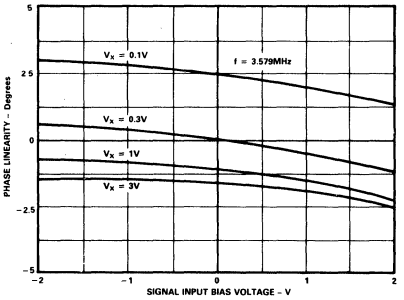


Figure 5d. Differential Phase Linearity in Minimal Configuration for a Typical Device

Differential Configurations

When only one signal channel must be handled it is often advantageous to use the channels differentially. By subtracting the CH1 and CH2 outputs any residual transient control feedthrough is virtually eliminated. Figure 6a shows a minimal configuration where it is assumed that the host system uses differential signals and a 50Ω environment throughout. This figure also shows a recommended control-feedforward network to improve large-signal

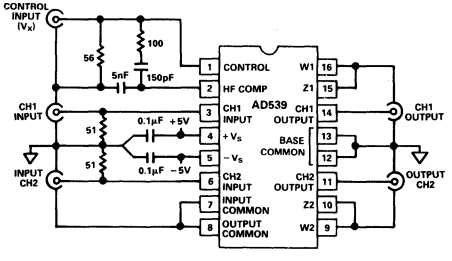


Figure 6a. High-Speed Differential Configuration

response time. The control feedthrough glitch is shown in Figure 6b, where the input was applied to CH1 and only the output of CH1 was displayed on the oscilloscope. The improvement obtained when CH1 and CH2 outputs are viewed differentially is clear in Figure 6c. The envelope rise-time is of the order of 40ns.

Lower distortion results when CH1 and CH2 are driven by *complementary* inputs and the outputs are utilized differentially, using a circuit such as Figure 7a. Resistors R1 and R2 should have a value in the range 100 to 1000Ω.

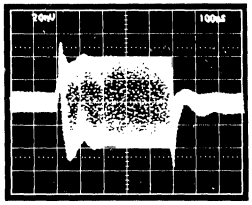


Figure 6b. Control Feedthrough One Channel of Figure 6a

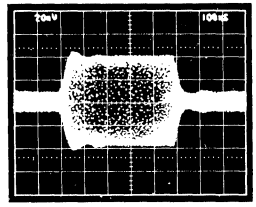


Figure 6c. Control Feedthrough Differential Mode, Figure 6a

They minimize a secondary distortion mechanism caused by a collector-modulation effect in the controlled cascodes (see CIRCUIT DESCRIPTION) by keeping the voltage-swing at the outputs to an acceptable level. Figure 7b shows the improvement in distortion over the standard configuration (compare Figure 3b). Note that the Z nodes (pins 10 and 15) are returned to the control input; this prevents the early onset of output-transistor saturation.

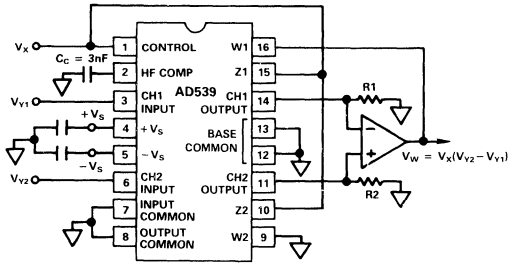


Figure 7a. Low-Distortion Differential Configuration

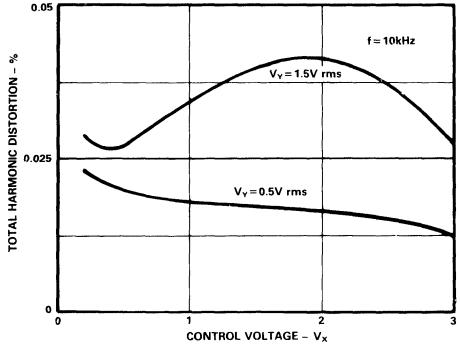


Figure 7b. Distortion in Differential Mode Using LH0032 Op Amp

Even lower distortion (0.01%, or −80dB) has been measured using two output op amps in a configuration similar to Figure 2 connected as virtual-ground current-summers (to prevent the modulation effect). Note that to generate the difference output it is merely necessary to connect the output of the CH1 op amp to the Z node of CH2. In this way, the net input to the CH2 op amp is the difference signal, and the low-distortion resultant appears as its output.

A 50MHz VOLTAGE-CONTROLLED AMPLIFIER

Figure 8 is a circuit for a 50MHz voltage-controlled amplifier (VCA) suitable for use in high-quality-video-speed applications. The outputs from the two-signal channels of the AD539 are applied to the op-amp in a subtracting configuration. This connection has two main advantages: first, it results in better rejection of the control voltage, particularly when over-driven (V_X<0 or V_X>3.3V). Secondly, it provides a choice of either non-inverting or inverting responses, using either inputs V_{Y1} or V_{Y2} respectively. In this circuit, the output of the op-amp will equal:

$$V_{OUT} = \frac{V_X\,(V_{Y1} - V_{Y2})}{2V} \text{ for } V_X > 0$$

Hence, the gain is unity at $V_X = +2V$. Since V_X can over-range to +3.3V, the maximum gain in this configuration is about 4.3dB. (Note: If pin 9 of the AD539 is grounded, rather than connected to the output of the 5539N, the maximum gain becomes 10dB.)

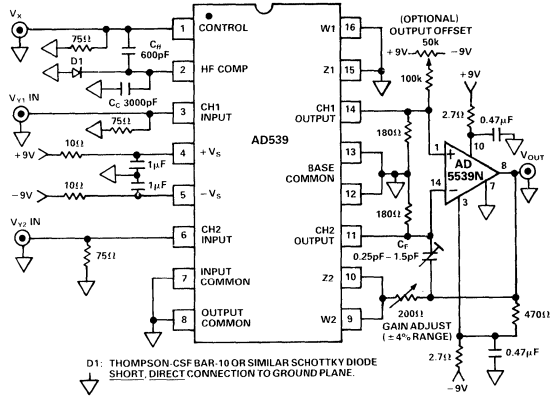


Figure 8. A Wide Bandwidth Voltage-Controlled Amplifier

The −3dB bandwidth of this circuit is over 50MHz at full gain, and is not substantially affected at lower gains. Of course, when V_X is zero (or slightly negative, to override the residual input offset) there is still a small amount of capacitive feedthrough at high frequencies; therefore, *extreme* care is needed in laying out the PC board to minimize this effect. Also, for small values of V_X, the combination of this feedthrough with the multiplier output can cause a dip in the response where they are out of phase. Figure 9a shows the ac response from the noninverting

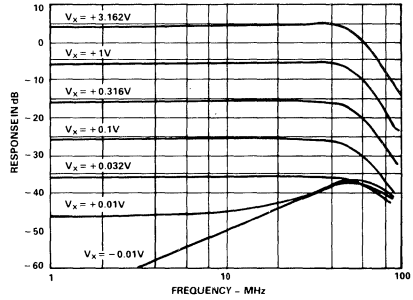


Figure 9a. AC Response of the VCA at Different Gains V_Y = 0.5V RMS

input, with the response from the inverting input, V_{Y2}, essentially identical. Test conditions: $V_{Y1} = 0.5V$ rms for values of V_X from $+10mV$ to $+3.16V$; this is with a 75Ω load on the output. The feedthrough at $V_X = -10mV$ is also shown.

The transient response of the signal channel at $V_X = +2V$, $V_Y = V_{OUT} = \pm 1V$ is shown in Figure 9b; with the VCA driving a 75Ω load. The rise and fall-times are approximately 7ns.

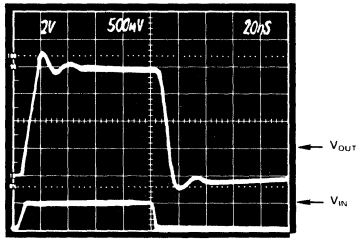


Figure 9b. Transient Response of the Voltage-Controlled Amplifier $V_X = +2$ Volts $V_Y = \pm 1$ Volt

A more detailed description of this circuit, including differential gain and phase characteristics, is given in the application note "Low Cost, Two Chip Voltage-Controlled Amplifier and Video Switch" available from Analog Devices.

BASIC DIVIDER CONNECTIONS

Standard Scaling

The AD539 provides excellent operation as a two-quadrant analog divider in wide-band wide gain-range applications, with the advantage of dual-channel operation. Figure 10a shows the simplest connections for division with a transfer function of

$$V_Y = -V_U V_W / V_X$$

Recalling that the nominal value of V_U is 1V, this can be simplified to

$$V_Y = -V_W / V_X$$

where all signals are expressed in volts. The circuit thus exhibits unity gain for $V_X = +1V$ and a gain of 40dB when $V_X = +0.01V$.

The output swing is limited to $\pm 2V$ nominal full-scale and $\pm 4.2V$ peak (using a $-V_S$ supply of at least 7.5V for the AD539). Since the maximum *loss* is 10dB (at $V_X = 3.162V$), it follows that the maximum input to V_W should be $\pm 6.3V$ (4.4V rms) for low distortion applications, and no more than $\pm 13.4V$ (9.5V rms) to avoid clipping. Note that offset adjustment will be needed

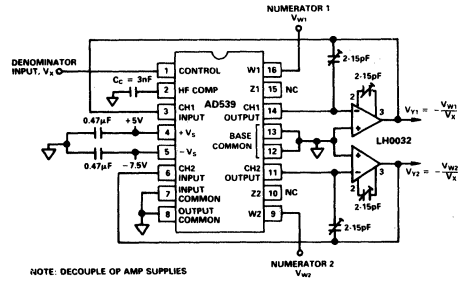


Figure 10a. Two-Channel Divider with 1V Scaling

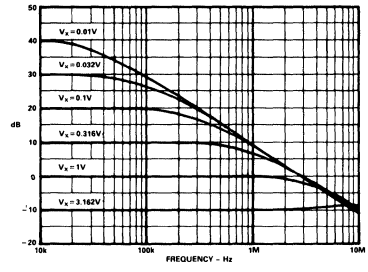


Figure 10b. HF Response of Figure 10a Divider

for the op amps to maintain accurate dc levels at the output in high gain applications: the "noise gain" is $6V/V_X$, or 600 at $V_X = +0.01V$.

The gain-magnitude response for this configuration using the LH0032 op amps with nominally 12pF compensation (pins 2 to 3) and $C_F = 7pF$ is shown in Figure 10b; of course, other amplifiers may also be used. Since there is some manufacturing variation in the HF response of the op amps, and load conditions will also affect the response, these capacitors should be adjustable: 5-15pF is recommended for both positions. The bandwidth in this configuration is nominally 17MHz at $V_X = +3.162V$, 4.5MHz at $V_X = +1V$, 350kHz at $V_X = +0.1V$ and 35kHz at $V_X = +0.01V$. The general recommendations regarding the use of a good ground plane and power-supply decoupling should be carefully observed.

ANALOG DEVICES

Low Cost Analog Multiplier

AD633

FEATURES
Four-Quadrant Multiplication
Low Cost 8-Pin Package
Complete—No External Components Required
Laser-Trimmed Accuracy and Stability
Total Error Within 2% of FS
Differential High Impedance X and Y Inputs
High Impedance Unity-Gain Summing Input
Laser-Trimmed 10 V Scaling Reference

APPLICATIONS
Multiplication, Division, Squaring
Modulation/Demodulation, Phase Detection
Voltage-Controlled Amplifiers/Attenuators/Filters

PRODUCT DESCRIPTION

The AD633 is a functionally complete, four-quadrant, analog multiplier. It includes high impedance, differential X and Y inputs and a high impedance summing input (Z). The low impedance output voltage is a nominal 10 V full scale provided by a buried Zener. The AD633 is the first product to offer these features in modestly priced 8-pin plastic DIP and SOIC packages.

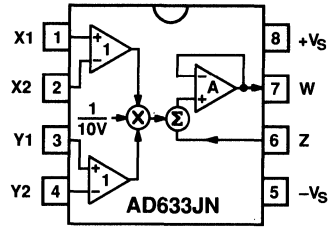
The AD633 is laser calibrated to a guaranteed total accuracy of 2% of full scale. Nonlinearity for the Y-input is typically less than 0.1% and noise referred to the output is typically less than 100 μV rms in a 10 Hz to 10 kHz bandwidth. A 1 MHz bandwidth, 20 V/μs slew rate, and the ability to drive capacitive loads make the AD633 useful in a wide variety of applications where simplicity and cost are key concerns.

The AD633's versatility is not compromised by its simplicity. The Z-input provides access to the output buffer amplifier, enabling the user to sum the outputs of two or more multipliers, increase the multiplier gain, convert the output voltage to a current, and configure a variety of applications.

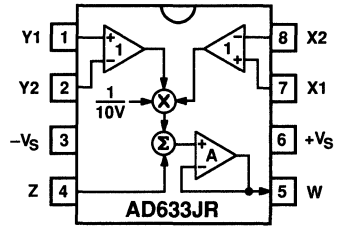
The AD633 is available in an 8-pin plastic mini-DIP package (N) and 8-pin SOIC (R) and is specified to operate over the 0°C to +70°C commercial temperature range.

AD633 CONNECTION DIAGRAMS

8-Pin Plastic DIP (N) Package



8-Pin Plastic SOIC (R) Package



$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z$$

PRODUCT HIGHLIGHTS

1. The AD633 is a complete four-quadrant multiplier offered in low cost 8-pin plastic packages. The result is a product that is cost effective and easy to apply.
2. No external components or expensive user calibration are required to apply the AD633.
3. Monolithic construction and laser calibration make the device stable and reliable.
4. High (10 MΩ) input resistances make signal source loading negligible.
5. Power supply voltages can range from ±8 V to ±18 V. The internal scaling voltage is generated by a stable Zener diode; multiplier accuracy is essentially supply insensitive.

8

AD633—SPECIFICATIONS (T_A = +25°C, V_S = ±15 V, $R_L \geq 2$ kΩ)

Model		AD633J			
TRANSFER FUNCTION		$W = \frac{(X_1-X_2)(Y_1-Y_2)}{10\ V} + Z$			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
MULTIPLIER PERFORMANCE					
Total Error	−10 V ≤ X, Y ≤ +10 V		±1	**±2**	% Full Scale
T_{min} to T_{max}			±3		% Full Scale
Scale Voltage Error	SF = 10.00 V Nominal		±0.25%		% Full Scale
Supply Rejection	V_S = ±14 V to ±16 V		±0.01		% Full Scale
Nonlinearity, X	X = ±10 V, Y = +10 V		±0.4	**±1**	% Full Scale
Nonlinearity, Y	Y = ±10 V, X = +10 V		±0.1	**±0.4**	% Full Scale
X Feedthrough	Y Nulled, X = ±10 V		±0.3	**±1**	% Full Scale
Y Feedthrough	X Nulled, Y = ±10 V		±0.1	**±0.4**	% Full Scale
Output Offset Voltage			±5	**±50**	mV
DYNAMICS					
Small Signal BW	V_O = 0.1 V rms,		1		MHz
Slew Rate	V_O = 20 V p-p		20		V/μs
Settling Time to 1%	Δ V_O = 20 V		2		μs
OUTPUT NOISE					
Spectral Density			0.8		$\mu V/\sqrt{Hz}$
Wideband Noise	f = 10 Hz to 5 MHz		1		mV rms
	f = 10 Hz to 10 kHz		90		μV rms
OUTPUT					
Output Voltage Swing		**±11**			V
Short Circuit Current	R_L = 0 Ω		30	**40**	mA
INPUT AMPLIFIERS					
Signal Voltage Range	Differential	**±10**			V
	Common Mode	**±10**			V
Offset Voltage X, Y			±5	**±30**	mV
CMRR X, Y	V_{CM} = ±10 V, f = 50 Hz	**60**	80		dB
Bias Current X, Y, Z			0.8	**2.0**	μA
Differential Resistance			10		MΩ
POWER SUPPLY					
Supply Voltage					
Rated Performance			±15		V
Operating Range		**±8**		**±18**	V
Supply Current	Quiescent		4	**6**	mA

NOTES
Specifications shown in **boldface** are tested on all production units at electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . 500 mW
Input Voltages[3] . . . . . ±18 V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range . . . . . 0°C to +70°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.
[2]8-Pin Plastic Package: θ_{JA} = 165°C/W; 8-Pin Small Outline Package: θ_{JA} = 155°C/W.
[3]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

AD633 ORDERING GUIDE

Model	Description	Package Option*
AD633JN	8-Pin Plastic DIP	N-8
AD633JR	8-Pin Plastic SOIC	R-8

*N = Plastic DIP; R = Small Outline IC (SOIC). For outline information see Package Information section.

FUNCTIONAL DESCRIPTION

The AD633 is a low cost multiplier comprising a translinear core, a buried Zener reference, and a unity gain connected output amplifier with an accessible summing node. Figure 1 shows the functional block diagram. The differential X and Y inputs are converted to differential currents by voltage-to-current converters. The product of these currents is generated by the multiplying core. A buried Zener reference provides an overall scale factor of 10 V. The sum of $(X \cdot Y)/10 + Z$ is then applied to the output amplifier. The amplifier summing node Z allows the user to add two or more multiplier outputs, convert the output voltage to a current, and configure various analog computational functions.

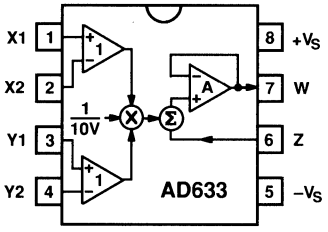


Figure 1. AD633 Functional Block Diagram (AD633JN Pinout Shown)

Inspection of the block diagram shows the overall transfer function to be:

$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10\ V} + Z \qquad \text{(Eq. 1)}$$

ERROR SOURCES

Multiplier errors consist primarily of input and output offsets, scale factor error, and nonlinearity in the multiplying core. The input and output offsets can be eliminated by using the optional trim of Figure 2. This scheme reduces the net error to scale factor errors (gain error) and an irreducible nonlinearity component in the multiplying core. The X and Y nonlinearities are typically 0.4% and 0.1% of full scale, respectively. Scale factor error is typically 0.25% of full scale. The high impedance Z input should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise, the differential X and Y inputs should be referenced to their respective grounds to realize the full accuracy of the AD633.

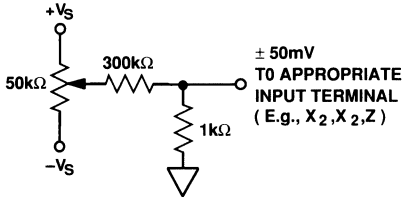


Figure 2. Optional Offset Trim Configuration

APPLICATIONS

The AD633 is well suited for such applications as modulation and demodulation, automatic gain control, power measurement, voltage controlled amplifiers, and frequency doublers. Note that these applications show the pin connections for the AD633JN pinout (8-pin DIP), which differs from the AD633JR pinout (8-pin SOIC).

Multiplier Connections

Figure 3 shows the basic connections for multiplication. The X and Y inputs will normally have their negative nodes grounded, but they are fully differential, and in many applications the grounded inputs may be reversed (to facilitate interfacing with signals of a particular polarity, while achieving some desired output polarity) or both may be driven.

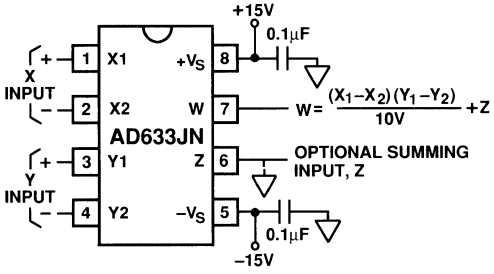


Figure 3. Basic Multiplier Connections

Squaring and Frequency Doubling

As Figure 4 shows, squaring of an input signal, E, is achieved simply by connecting the X and Y inputs in parallel to produce an output of $E^2/10$ V. The input may have either polarity, but the output will be positive. However, the output polarity may be reversed by interchanging the X or Y inputs. The Z input may be used to add a further signal to the output.

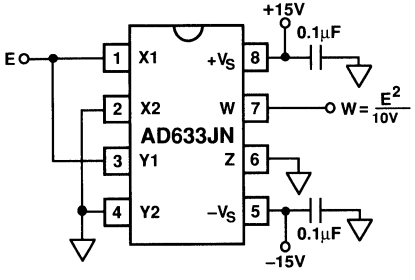


Figure 4. Connections for Squaring

When the input is a sine wave E sin ωt, this squarer behaves as a frequency doubler, since

$$\frac{(E\ sin\ \omega t)^2}{10\ V} = \frac{E^2}{20\ V}(1 - cos\ 2\ \omega t) \qquad \text{(Eq. 2)}$$

Equation 2 shows a dc term at the output which will vary strongly with the amplitude of the input, E. This can be

avoided using the connections shown in Figure 5, where an RC network is used to generate two signals whose product has no dc term. It uses the identity:

$$cos\ \theta\ sin\ \theta = \frac{1}{2}(sin\ 2\ \theta) \qquad \text{(Eq. 3)}$$

At ω_o = 1/CR, the X input leads the input signal by 45° (and is attenuated by $\sqrt{2}$), and the Y input lags the X input by 45° (and is also attenuated by $\sqrt{2}$). Since the X and Y inputs are 90° out of phase, the response of the circuit will be (satisfying Equation 3.):

$$W = \frac{1}{(10\ V)}\frac{E}{\sqrt{2}}(sin\ \omega_o t + 45°)\frac{E}{\sqrt{2}}(sin\ \omega_o t - 45°)$$

$$= \frac{E^2}{(40\ V)}(sin\ 2\ \omega_o t) \qquad \text{(Eq. 4)}$$

which has no dc component. Resistors R1 and R2 are included to restore the output amplitude to 10 V for an input amplitude of 10 V.

The amplitude of the output is only a weak function of frequency: the output amplitude will be 0.5% too low at $\omega = 0.9\ \omega_o$ and $\omega = 1.1\ \omega_o$.

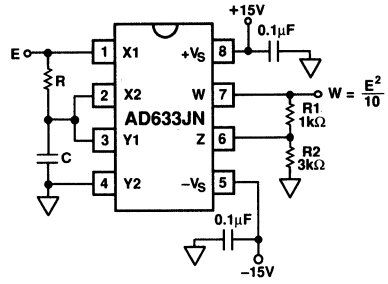


Figure 5. "Bounceless" Frequency Doubler

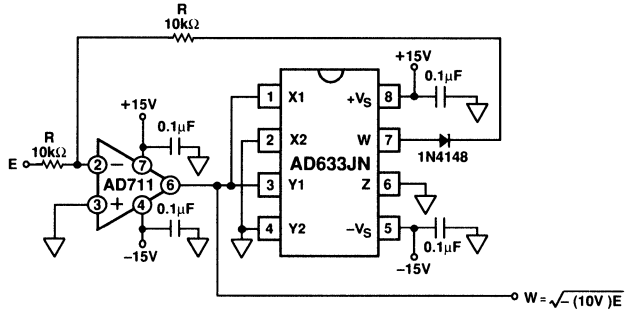


Figure 6. Connections for Squaring Rooting

Generating Inverse Functions

Inverse functions of multiplication, such as division and square rooting, can be implemented by placing a multiplier in the feedback loop of an op amp. Figure 6 shows how to implement a square rooter with the transfer function

$$W = \sqrt{-(10\ V)\ E} \qquad \text{(Eq. 5)}$$

for the condition E<0.

Likewise, Figure 7 shows how to implement a divider using a multiplier in a feedback loop. The transfer function for the divider is

$$W = -(10\ V)\frac{E}{E_X} \qquad \text{(Eq. 6)}$$

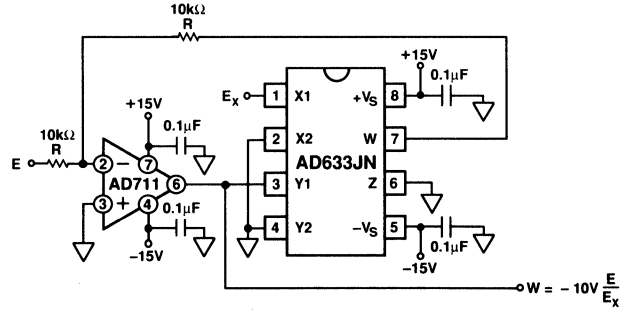


Figure 7. Connections for Division

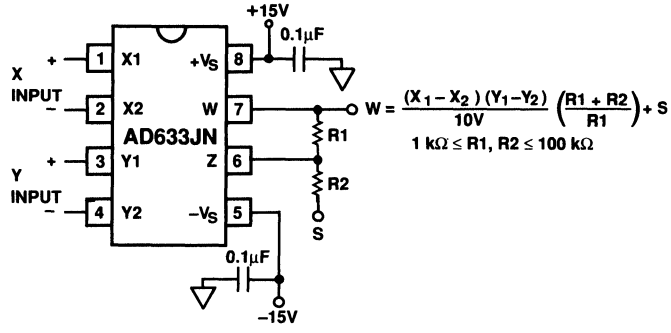


Figure 8. Connections for Variable Scale Factor

Variable Scale Factor

In some instances, it may be desirable to use a scaling voltage other than 10V. The connections shown in Figure 8 increase the gain of the system by the ratio (R1 + R2)/R1. This ratio is limited to 100 in practical applications. The summing input, S, may be used to add an additional signal to the output or it may be grounded.

Current Output

The AD633's voltage output can be converted to a current output by the addition of a resistor R between the AD633's W and Z pins as shown in Figure 9 below. This arrangement forms the basis of voltage controlled integrators and oscillators as will be shown later in this Applications section. The transfer function of this circuit has the form

$$I_O = \frac{1}{R}\frac{(X_1-X_2)(Y_1-Y_2)}{10\ V} \qquad \text{(Eq. 7)}$$

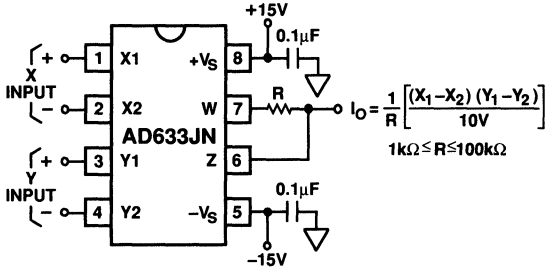


Figure 9. Current Output Connections

Linear Amplitude Modulator

The AD633 can be used as a linear amplitude modulator with no external components. Figure 10 shows the circuit. The carrier and modulation inputs to the AD633 are multiplied to produce a double-sideband signal. The carrier signal is fed forward to the AD633's Z input where it is summed with the double-sideband signal to produce a double-sideband with carrier output.

Voltage Controlled Low Pass and High Pass Filters

Figure 11 shows a single multiplier used to build a voltage controlled low pass filter. The voltage at output A is a result of filtering, E_S. The break frequency is modulated by E_C, the control input. The break frequency, f_2, equals

$$f_2 = \frac{E_C}{(20\ V)\,\pi\,RC} \qquad \text{(Eq. 8)}$$

and the rolloff is 6 dB per octave. This output, which is at a high impedance point, may need to be buffered.

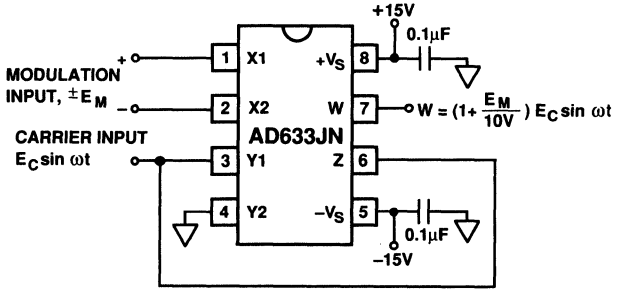


Figure 10. Linear Amplitude Modulator

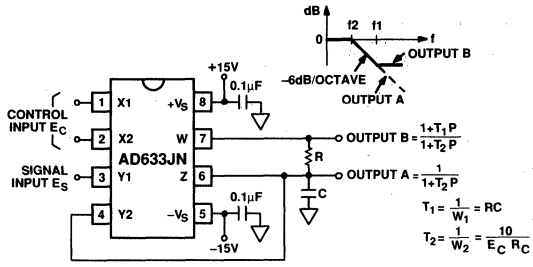


Figure 11. Voltage Controlled Low Pass Filter

The voltage at output B, the direct output of the AD633, has the same response up to frequency f_1, the natural breakpoint of the RC filter,

$$f_1 = \frac{1}{2\pi RC} \qquad \text{(Eq. 9)}$$

then levels off to a constant attenuation of $f_1/f_2 = E_C/10$.

For example, if R = 8 kΩ and C = 0.002 μF, then output A has a pole at frequencies from 100 Hz to 10 kHz for E_C ranging from 100 mV to 10 V. Output B has an additional zero at 10 kHz (and can be loaded because it is the multiplier's low impedance output). The circuit can be changed to a high pass filter by interchanging the resistor and capacitor as shown in Figure 12, below.

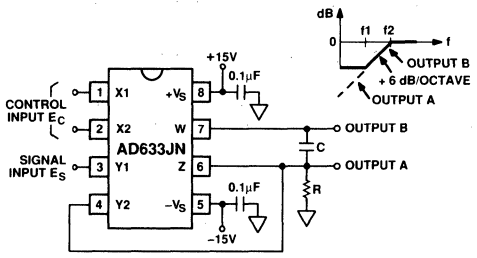


Figure 12. Voltage Controlled High Pass Filter

Voltage Controlled Quadrature Oscillator

Figure 13 shows two multipliers being used to form integrators with controllable time constants in a 2nd order differential equation feedback loop. R2 and R5 provide controlled current output operation. The currents are integrated in capacitors C1 and C2, and the resulting voltages at high impedance are applied to the X inputs of the "next" AD633. The frequency control input, E_C, connected to the Y inputs, varies the integrator gains with a calibration of 100 Hz/V. The accuracy is limited by the Y-input offsets. The practical tuning range of this circuit is 100:1. C2 (proportional to C1 and C3), R3, and R4 provide regenerative feedback to start and maintain oscillation. The diode bridge, D1 through D4 (1N914s), and Zener diode D5 provide economical temperature stabilization and amplitude stabilization at ±8.5 V by degenerative damping. The output from the second integrator (10 V sin ωt) has the lowest distortion.

AGC AMPLIFIERS

Figure 14 shows an AGC circuit that uses an rms-dc converter to measure the amplitude of the output waveform. The AD633 and A1, 1/2 of an AD712 dual op amp, form a voltage controlled amplifier. The rms dc converter, an AD736, measures the rms value of the output signal. Its output drives A2, an integrator/comparator, whose output controls the gain of the voltage controlled amplifier. The 1N4148 diode prevents the output of A2 from going negative. R8, a 50 kΩ variable resistor, sets the circuit's output level. Feedback around the loop forces the voltages at the inverting and noninverting inputs of A2 to be equal, thus the AGC.

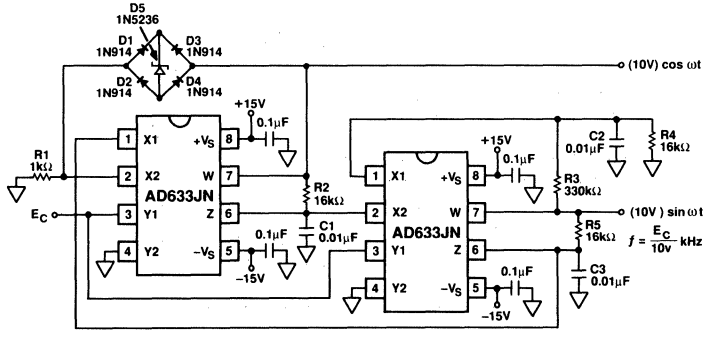


Figure 13. Voltage Controlled Quadrature Oscillator

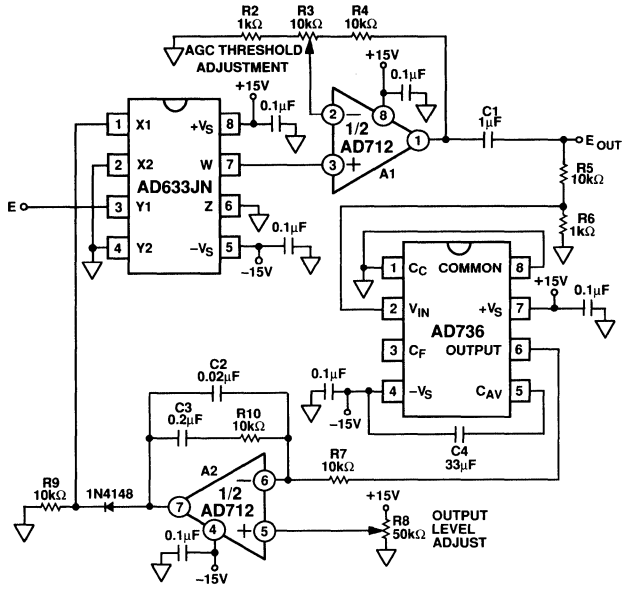


Figure 14. Connections for Use in Automatic Gain Control Circuit

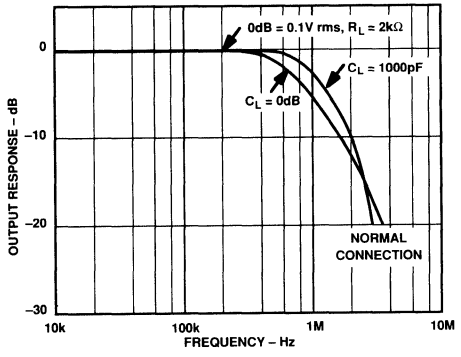


Figure 15. Frequency Response

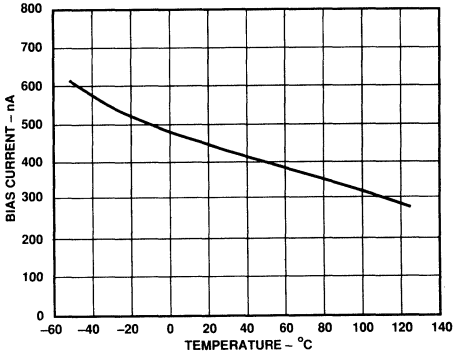


Figure 16. Input Bias Current vs. Temperature (X, Y, or Z Inputs)

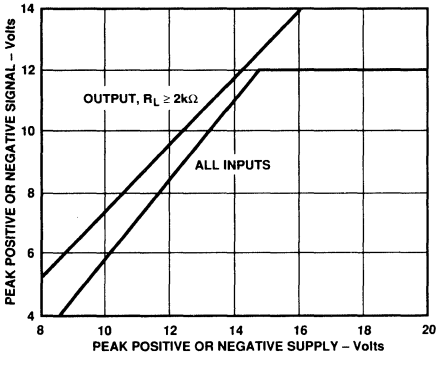


Figure 17. Input and Output Signal Ranges vs. Supply Voltages

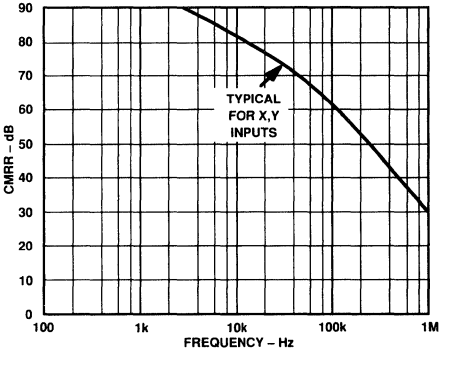


Figure 18. CMRR vs. Frequency

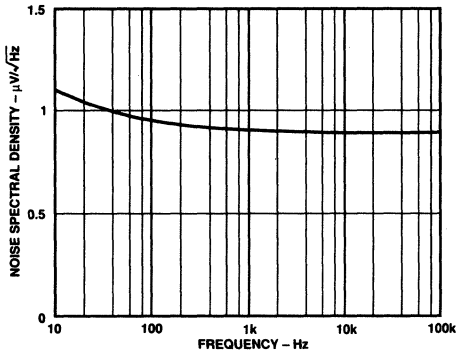


Figure 19. Noise Spectral Density vs. Frequency

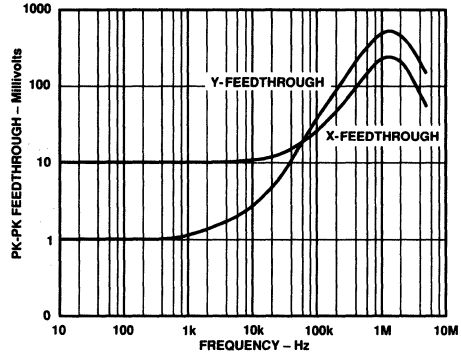


Figure 20. AC Feedthrough vs. Frequency

ANALOG DEVICES

RGB to NTSC/PAL Encoder

AD720

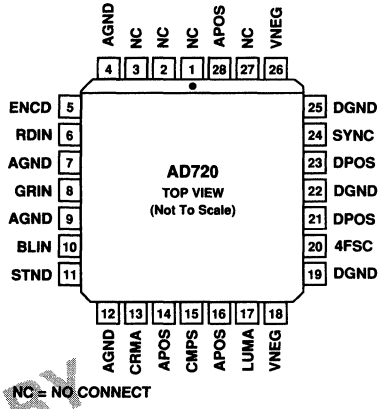
FEATURES

Separate Chrominance, Luminance, and Composite Video Outputs
Drives 75 Ω Reverse-Terminated Loads
No External Filters or Delay Lines Required
Comes in Compact 28-Pin PLCC
Logic Selectable NTSC or PAL Encoding Modes
Logic Selectable Power-Down Mode

APPLICATIONS

RGB to NTSC or PAL Encoding

PIN CONFIGURATION



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD720 RGB to NTSC/PAL Encoder is a BiCMOS LSI circuit that converts red, green and blue color component signals into their corresponding luminance (baseband amplitude) and chrominance (subcarrier amplitude/phase) signals in accordance with either NTSC or PAL standards. These two outputs are also combined to provide a composite video output. All three outputs are available separately at voltages at twice the standard signal levels as required for driving 75 Ω reverse-terminated cables.

The AD720 provides a complete, fully calibrated function, requiring only termination resistors, decoupling networks, a clock input at four times the subcarrier frequency, and a composite sync pulse. The AD720 also has two control inputs: one input selects the TV standard (NTSC/PAL) and the other (ENCD) powers down most sections of the chip when the encoding function is not in use. All logical inputs are CMOS compatible. The chip operates from ±5 V supplies.

All required low-pass filters are on chip. After the input signals pass through a precision RGB to YUV encoding matrix, two on-chip low-pass filters limit the bandwidth of the U and V color-difference signals to 1.2 MHz prior to binary modulation; a third low-pass filter at 5.5 MHz follows the modulators to limit the harmonic content of the output. The U and V signal delays in the chroma filters are matched by an on-chip sampled-data delay line in the Y signal path; to prevent aliasing, a prefilter at 5 MHz is included ahead of the delay line and a second 5 MHz filter is added after the delay line to suppress harmonics in the output. The low-pass filters are optimized for minimum pulse overshoot.

The AD720 is available in a 28-pin plastic leaded chip carrier for the 0°C to 70°C commercial temperature range.

PIN DESCRIPTIONS

ENCD	A logical low level powers down chip when not in use.
STND	A logical high level input selects NTSC encoding; A logical low level selects PAL encoding.
4FSC	Clock input at four times subcarrier frequency.
SYNC	Input pin for composite television synchronization pulses.
RDIN	Red Component Input.
GRIN	Green Component Input.
BLIN	Blue Component Input. These three analog inputs are 0 to +700 mV for PAL or 0 to 714 mV for NTSC.
CRMA	Chrominance Output (Subcarrier Only). 900 mV p-p plus burst (286 mV p-p for NTSC, 300 mV p-p for PAL).*
CMPS	Composite video output, −300 mV to +700 mV peak (PAL) or −286 mV to 950 mV (NTSC).*
LUMA	Luminance plus SYNC output, −300 mV to +714 mV peak (PAL) or −286 mV to 714 mV (NTSC).*
AGND	Analog Ground Connections (4).
DGND	Digital Ground Connections (3).
APOS	Analog Positive Supply (+5 V ±5%) (3).
DPOS	Digital Positive Supply (+5 V ±5%) (2).
VNEG	System Negative Supply (−5 V ±5%) (2).

*Measured at 75 Ω reverse-terminated load; double these values at IC pins.

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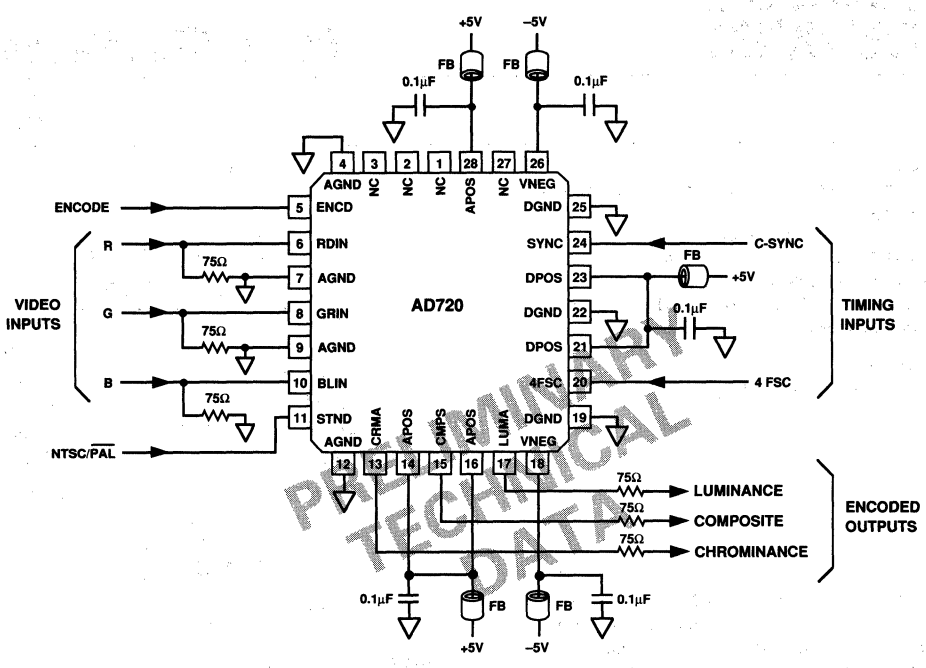


Typical Application

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

10 MHz, 4-Quadrant Multiplier/Divider

AD734

FEATURES

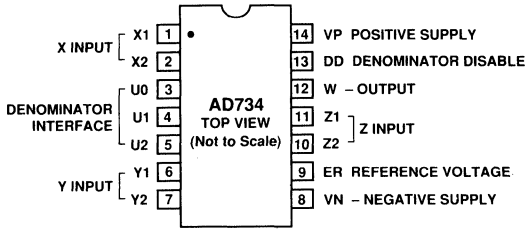
High Accuracy
0.1% Typical Error
High Speed
10 MHz Full-Power Bandwidth
450 V/μs Slew Rate
200 ns Settling to 0.1% at Full Power
Low Distortion
−80 dBc from Any Input
Third-Order IMD Typically −75 dBc at 10 MHz
Low Noise
94 dB SNR, 10 Hz to 20 kHz
70 dB SNR, 10 Hz to 10 MHz
Direct Division Mode
2 MHz BW at Gain of 100

APPLICATIONS

High Performance Replacement for AD534
Multiply, Divide, Square, Square Root
Modulator, Demodulator
Wideband Gain Control, RMS-DC Conversion
Voltage-Controlled Amplifiers, Oscillators, and Filters
Demodulator with 40 MHz Input Bandwidth

CONNECTION DIAGRAM

14-Pin DIP
(Q Package)



PRODUCT DESCRIPTION

The AD734 is an accurate high speed, four-quadrant analog multiplier that is pin-compatible with the industry-standard AD534 and provides the transfer function W = XY/U. The AD734 provides a low-impedance voltage output with a full-power (20 V pk-pk) bandwidth of 10 MHz. Total static error (scaling, offsets, and nonlinearities combined) is 0.1% of Full Scale. Distortion is typically less than −80 dBc and guaranteed. The low-capacitance X, Y and Z inputs are fully differential. In most applications, no external components are required to define the function.

The internal scaling (denominator) voltage U is 10 V, derived from a buried-Zener voltage reference. A new feature provides the option of substituting an external denominator voltage, allowing the use of the AD734 as a two-quadrant divider with a 1000:1 denominator range and a signal bandwidth that remains 10 MHz to a gain of 20 dB, 2 MHz at a gain of 40 dB and 200 kHz at a gain of 60 dB, for a gain-bandwidth product of 200 MHz.

The advanced performance of the AD734 is achieved by a combination of new circuit techniques, the use of a high speed complementary bipolar process and a novel approach to laser-trimming based on ac signals rather than the customary dc methods. The wide bandwidth (>40 MHz) of the AD734's input stages and the 200 MHz gain-bandwidth product of the multiplier core allow the AD734 to be used as a low distortion demodulator with input frequencies as high as 40 MHz as long as the desired output frequency is less than 10 MHz.

The AD734AQ and AD734BQ are specified for the industrial temperature range of −40°C to +85°C and come in a 14-pin ceramic DIP. The AD734SQ/883B, available processed to MIL-STD-883B for the military range of −55°C to +125°C, is available in a 14-pin ceramic DIP.

PRODUCT HIGHLIGHTS

The AD734 embodies more than two decades of experience in the design and manufacture of analog multipliers, to provide:

1. A new output amplifier design with more than twenty times the slew-rate of the AD534 (450 V/μs versus 20 V/μs) for a full power (20 V pk-pk) bandwidth of 10 MHz.
2. Very low distortion, even at full power, through the use of circuit and trimming techniques that virtually eliminate all of the spurious nonlinearities found in earlier designs.
3. Direct control of the denominator, resulting in higher multiplier accuracy and a gain-bandwidth product at small denominator values that is typically 200 times greater than that of the AD534 in divider modes.
4. Very clean transient response, achieved through the use of a novel input stage design and wide-band output amplifier, which also ensure that distortion remains low even at high frequencies.
5. Superior noise performance by careful choice of device geometries and operating conditions, which provide a guaranteed 88 dB of dynamic range in a 20 kHz bandwidth.

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AD734—SPECIFICATIONS (T_A = +25°C, $+V_S$ = VP = +15 V, $-V_S$ = VN = −15 V, $R_L \geq 2$ kΩ)

TRANSFER FUNCTION

$$W = A_O\left\{\frac{(X_1-X_2)(Y_1-Y_2)}{(U_1-U_2)} - (Z_1 - Z_2)\right\}$$

Parameter	Conditions	A Min	A Typ	A Max	B Min	B Typ	B Max	S Min	S Typ	S Max	Units
MULTIPLIER PERFORMANCE											
Transfer Function			W = XY/10			W = XY/10			W = XY/10		
Total Static Error[1]	−10 V ≤ X,Y ≤ 10 V		0.1	**0.4**		0.1	**0.25**		0.1	**0.4**	%
Over T_{min} to T_{max}				**1**			**0.6**			**1.25**	%
vs. Temperature	T_{min} to T_{max}		0.004			0.003			0.004		%/°C
vs. Either Supply	$\pm V_S$ = 14 V to 16 V		0.01	**0.05**		0.01	**0.05**		0.01	**0.05**	%/V
Peak Nonlinearity	−10 V ≤ X ≤ +10 V, Y = +10 V		0.05			0.05			0.05		%
	−10 V ≤ Y ≤ +10 V, X = +10 V		0.025			0.025			0.025		%
THD[2]	X = 7 V rms, Y = +10 V, f ≤ 5 kHz			**−58**			**−66**			**−58**	dBc
	T_{min} to T_{max}			**−55**			**−63**			**−55**	dBc
	Y = 7 V rms, X = +10 V, f ≤ 5 kHz			**−60**			**−80**			**−60**	dBc
	T_{min} to T_{max}			**−57**			**−74**			**−57**	dBc
Feedthrough	X = 7 V rms, Y = nulled, f ≤ 5 kHz		−85	**−60**		−85	**−70**		−85	**−60**	dBc
	Y = 7 V rms, X = nulled, f ≤ 5 kHz		−85	**−66**		−85	**−76**		−85	**−66**	dBc
Noise (RTO)	X = Y = 0										
Spectral Density	100 Hz to 1 MHz		1.0			1.0			1.0		$\mu V/\sqrt{Hz}$
Total Output Noise	10 Hz to 20 kHz		−94	**−88**		−94	**−88**		−94	**−88**	dBc
	T_{min} to T_{max}			**−85**			**−85**			**−85**	dBc
DIVIDER PERFORMANCE (Y = 10 V)											
Transfer Function			W = XY/U			W = XY/U			W = XY/U		
Gain Error	Y = 10 V, U = 100 mV to 10 V		1			1			1		%
X Input Clipping Level	Y ≤ 10 V		1.25 × U			1.25 × U			1.25 × U		V
U Input Scaling Error[3]				**0.3**			**0.15**			**0.3**	%
	T_{min} to T_{max}			**0.8**			**0.65**			**1**	%
(Output to 1%)	U = 1 V to 10 V Step , X = 1 V		100			100			100		ns
INPUT INTERFACES (X, Y, & Z)											
3 dB Bandwidth			40			40			40		MHz
Operating Range	Differential or Common Mode		±12.5			±12.5			±12.5		V
X Input Offset Voltage				**15**			**5**			**15**	mV
	T_{min} to T_{max}			**25**			**15**			**25**	mV
Y Input Offset Voltage				**10**			**5**			**10**	mV
	T_{min} to T_{max}			**12**			**6**			**12**	mV
Z Input Offset Voltage				**20**			**10**			**20**	mV
	T_{min} to T_{max}			**50**			**50**			**90**	mV
Z Input PSRR (Either Supply)	f ≤ 1 kHz	**54**	70		**66**	70		**54**	70		dB
	T_{min} to T_{max}	**50**			**56**			**50**			dB
CMRR	f = 5 kHz	**70**	85		**70**	85		**70**	85		dB
Input Bias Current (X, Y, Z Inputs)			50	**300**		50	**150**		50	**300**	nA
	T_{min} to T_{max}			**400**			**300**			**500**	nA
Input Resistance	Differential		50			50			50		kΩ
Input Capacitance	Differential		2			2			2		pF
DENOMINATOR INTERFACES (U0, U1, & U2)											
Operating Range			VN to VP-3			VN to VP-3			VN to VP-3		V
Denominator Range			1000:1			1000:1			1000:1		
Interface Resistor	U1 to U2		28			28			28		kΩ
OUTPUT AMPLIFIER (W)											
Output Voltage Swing	T_{min} to T_{max}	±12			±12			±12			V
Open-Loop Voltage Gain	X = Y = 0, Input to Z		72			72			72		dB
Dynamic Response	From X or Y Input, CL ≤ 20 pF										
3 dB Bandwidth	W ≤ 7 V rms	8	10		8	10		8	10		MHz
Slew Rate			450			450			450		V/μs
Settling Time	+20 V or −20 V Output Step										
To 1%			125			125			125		ns
To 0.1%			200			200			200		ns
Short-Circuit Current	T_{min} to T_{min}	**20**	50	80	**20**	50	80	**20**	50	80	mA
POWER SUPPLIES, $\pm V_S$											
Operating Supply Range		±8		±16.5	±8		±16.5	±8		±16.5	V
Quiescent Current	T_{min} to T_{max}	6	9	12	6	9	12	6	9	12	mA

NOTES

[1]Figures given are percent of full scale (e.g., 0.01% = 1 mV).

[2]dBc refers to deciBels relative to the full scale input (carrier) level of 7 V rms.

[3]See Figure 10 for test circuit.

All min and max specifications are guaranteed. Specifications in **Boldface** are tested on all production units at final electrical test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
for T_J max = 175°C . . . . . 500 mW
X, Y and Z Input Voltages . . . . . VN to VP
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range
Q . . . . . −65°C to +150°C
Operating Temperature Range
AD734A, B . . . . . −40°C to +85°C
AD734S . . . . . −55°C to +125°C
Lead Temperature Range (soldering 60 sec) . . . . . +300°C
Transistor Count 81

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.
[2]14-Pin Ceramic DIP: θ_{JA} = 110°C/W

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD734AQ	−40°C to +85°C	Q-14
AD734BQ	−40°C to +85°C	Q-14
AD734SQ/883B	−55°C to +125°C	Q-14

*Q = Cerdip. For outline information see Package Information section.

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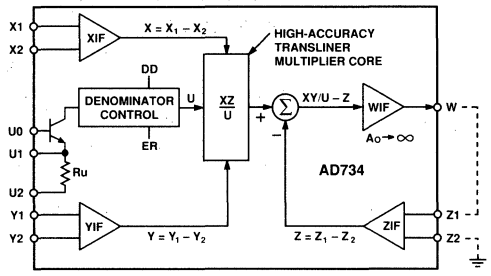

Figure 1. AD734 Block Diagram

FUNCTIONAL DESCRIPTION

Figure 1 is a simplified block diagram of the AD734. Operation is similar to that of the industry-standard AD534 and in many applications these parts are pin-compatible. The main functional difference is the provision for direct control of the denominator voltage, U, explained fully on the following page. Internal signals are actually in the form of currents, but the function of the AD734 can be understood using voltages throughout, as shown in this figure. Pins are named using upper-case characters (such as X1, Z2) while the *voltages* on these pins are denoted by subscripted variables (for example, X_1, Z_2).

The AD734's differential X, Y and Z inputs are handled by wideband interfaces that have low offset, low bias current and low distortion. The AD734 responds to the difference signals $X = X_1 - X_2$, $Y = Y_1 - Y_2$ and $Z = Z_1 - Z_2$, and rejects common-mode voltages on these inputs. The X, Y and Z interfaces provide a nominal full-scale (FS) voltage of ±10 V, but, due to the special design of the input stages, the linear range of the differential input can be as large as ±17 V. Also unlike previous designs, the response on these inputs is not clipped abruptly above ±15 V, but drops to a slope of one half.

The bipolar input signals X and Y are multiplied in a translinear core of novel design to generate the product XY/U. The denominator voltage, U, is internally set to an accurate, temperature-stable value of 10 V, derived from a buried-Zener reference. An uncalibrated fraction of the denominator voltage U appears between the voltage reference pin (ER) and the negative supply pin (VN), for use in certain applications where a temperature-compensated voltage reference is desirable. The internal denominator, U, can be disabled, by connecting the denominator disable Pin 13 (DD) to the positive supply pin (VP); the denominator can then be replaced by a fixed or variable external voltage ranging from 10 mV to more than 10 V.

The high-gain output op-amp nulls the difference between XY/U and an additional signal Z, to generate the final output W. The actual transfer function can take on several forms, depending on the connections used. The AD734 can perform all of the functions supported by the AD534, and new functions using the direct-division mode provided by the U-interface.

Each input pair (X1 and X2, Y1 and Y2, Z1 and Z2) has a differential input resistance of 50 kΩ; this is formed by "real" resistors (not a small-signal approximation) and is subject to a tolerance of ±20%. The common-mode input resistance is several megohms and the parasitic capacitance is about 2 pF.

The bias currents associated with these inputs are nulled by laser-trimming, such that when one input of a pair is optionally ac-coupled and the other is grounded, the residual offset voltage is typically less than 5 mV, which corresponds to a bias current of only 100 nA. This low bias current ensures that mismatches in the sources resistances at a pair of inputs does not cause an offset error. These currents remain low over the full temperature range and supply voltages.

The common-mode range of the X, Y and Z inputs does not fully extend to the supply rails. Nevertheless, it is often possible to operate the AD734 with one terminal of an input pair connected to either the positive or negative supply, unlike previous multipliers. The common-mode resistance is several megohms.

The full-scale output of ±10 V can be delivered to a load resistance of 1 kΩ (although the specifications apply to the standard multiplier load condition of 2 kΩ). The output amplifier is stable driving capacitive loads of at least 100 pF, when a slight increase in bandwidth results from the peaking caused by this capacitance. The 450 V/μs slew rate of the AD734's output amplifier ensures that the bandwidth of 10 MHz can be maintained up to the full output of 20 V pk-pk. Operation at reduced supply voltages is possible, down to ±8 V, with reduced signal levels.

Available Transfer Functions

The uncommitted (open-loop) transfer function of the AD734 is

$$W = A_O \left\{ \frac{(X_1 - X_2)(Y_1 - Y_2)}{U} - (Z_1 - Z_2) \right\}, \quad (1)$$

where A_O is the open-loop gain of the output op-amp, typically 72 dB. When a negative feedback path is provided, the circuit will force the quantity inside the brackets essentially to zero, resulting in the equation

$$(X_1 - X_2)(Y_1 - Y_2) = U\,(Z_1 - Z_2). \quad (2)$$

This is the most useful generalized transfer function for the AD734; it expresses a balance between the product XY and the product UZ. The absence of the output, W, in this equation only reflects the fact that we have not yet specified which of the inputs is to be connected to the op-amp output.

Most of the functions of the AD734 (including division, unlike the AD534 in this respect) are realized with Z_1 connected to W. So, substituting W in place of Z_1 in the above equation results in an output.

$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{U} + Z_2. \quad (3)$$

The free input Z2 can be used to sum another signal to the output; in the absence of a product signal, W simply follows the voltage at Z2 with the full 10 MHz bandwidth. When not needed for summation, Z2 should be connected to the ground associated with the load circuit. We can show the allowable polarities in the following shorthand form:

$$(\pm W) = \frac{(\pm X)(\pm Y)}{(+U)} + \pm Z. \quad (4)$$

In the recommended direct divider mode, the Y input is set to a fixed voltage (typically 10 V) and U is varied directly; it may have any value from 10 mV to 10 V. The magnitude of the ratio X/U cannot exceed 1.25; for example, the peak X-input for U = 1 V is ±1.25 V. Above this level, clipping occurs at the positive and negative extremities of the X-input. Alternatively, the AD734 can be operated using the standard (AD534) divider connections (Figure 8), when the negative feedback path is established via the Y_2 input. Substituting W for Y_2 in Equation (2),

we get

$$W = U\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1. \quad (5)$$

In this case, note that the variable X is now the denominator, and the above restriction (X/U ≤ 1.25) on the magnitude of the X input does not apply. However, X must be positive in order for the feedback polarity to be correct. Y_1 can be used for summing purposes or connected to the load ground if not needed. The shorthand form in this case is

$$(\pm W) = (+U)\frac{(\pm Z)}{(+X)} + (\pm Y). \quad (6)$$

In some cases, feedback may be connected to two of the available inputs. This is true for the square-rooting connections (Figure 9), where W is connected to both X_1 and Y_2. Setting X_1 = W and Y_2 = W in Equation (2), and anticipating the possibility of again providing a summing input, so setting X_2 = S and Y_1 = S, we find, in shorthand form

$$(\pm W) = \sqrt{(+U)(+Z)} + (\pm S). \quad (7)$$

This is seen more generally to be the geometric-mean function, since both U and Z can be variable; operation is restricted to one quadrant. Feedback may also be taken to the U-interface. Full details of the operation in these modes is provided in the appropriate section of this data sheet.

Direct Denominator Control

A valuable new feature of the AD734 is the provision to replace the internal denominator voltage, U, with any value from +10 mV to +10 V. This can be used (1) to simply alter the multiplier scaling, thus improve accuracy and achieve reduced noise levels when operating with small input signals; (2) to implement an accurate two-quadrant divider, with a 1000:1 gain range and an asymptotic gain-bandwidth product of 200 MHz; (3) to achieve certain other special functions, such as AGC or rms.

Figure 2 shows the internal circuitry associated with denominator control. Note first that the denominator is actually proportional to a current, Iu, having a nominal value of 356 μA for U = 10 V, whereas the primary reference is a voltage, generated by a buried-Zener circuit and laser-trimmed to have a very low temperature coefficient. This voltage is nominally 8 V with a tolerance of ±10%.

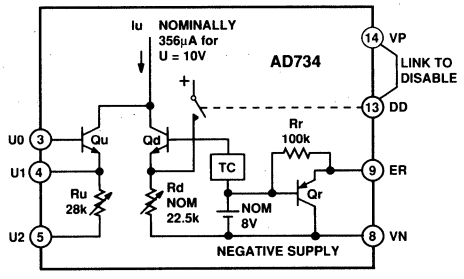

Figure 2. Denominator Control Circuitry

After temperature-correction (block TC), the reference voltage is applied to transistor Qd and trimmed resistor Rd, which generate the required reference current. Transistor Qu and resistor Ru are not involved in setting up the internal denominator, and their associated control pins U0, U1 and U2 will normally be grounded. The reference voltage is also made available, via the 100 kΩ resistor Rr, at Pin 9 (ER); the purpose of Qr is explained below.

When the control pin DD (denominator disable) is connected to VP, the internal source of Iu is shut off, and the collector current of Qu must provide the denominator current. The resistor Ru is laser-trimmed such that the multiplier denominator is exactly equal to the voltage across it (that is, across pins U1 and U2). Note that this trimming only sets up the correct internal ratio; the absolute value of Ru (nominally 28 kΩ) has a tolerance of ±20%. Also, the alpha of Qu, (typically 0.995) which might be seen as a source of scaling error, is canceled by the alpha of other transistors in the complete circuit.

In the simplest scheme (Figure 3), an externally-provided control voltage, V_G, is applied directly to U0 and U2 and the resulting voltage across Ru is therefore reduced by one V_{BE}. For example, when V_G = 2 V, the actual value of U will be about 1.3 V. This error will not be important in some closed-loop applications, such as automatic gain control (AGC), but clearly is not acceptable where the denominator value must be well-defined. When it is required to set up an accurate, fixed value of U, the on-chip reference may be used. The transistor Qr is provided to cancel the V_{BE} of Qu, and is biased by an external resistor, R2, as shown in Figure 4. R1 is chosen to set the desired value of U and consists of a fixed and adjustable resistor.

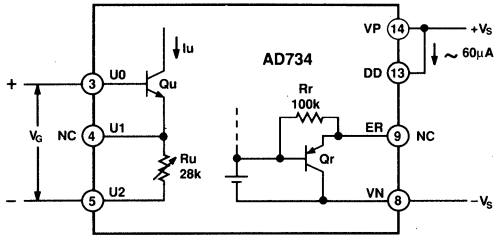

Figure 3. Low-Accuracy Denominator Control

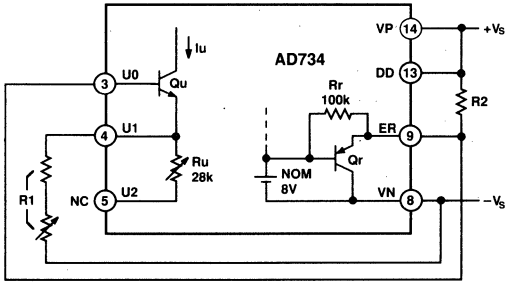

Figure 4. Connections for a Fixed Denominator

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Table I shows useful values of the external components for setting up nonstandard denominator values.

Denominator	R1 (Fixed)	R1 (Variable)	R2
5 V	34.8 kΩ	20 kΩ	120 kΩ
3 V	64.9 kΩ	20 kΩ	220 kΩ
2 V	86.6 kΩ	50 kΩ	300 kΩ
1 V	174 kΩ	100 kΩ	620 kΩ

Table I. Component Values for Setting Up Nonstandard Denominator Values

The denominator can also be current controlled, by grounding Pin 3 (U0) and withdrawing a current of Iu from Pin 4 (U1). The nominal scaling relationship is U = 28 × Iu, where u is expressed in volts and Iu is expressed in milliamps. Note, however, that while the linearity of this relationship is very good, it is subject to a scale tolerance of ±20%. Note that the common mode range on Pins 3 through 5 actually extends from 4 V to 36 V below VP, so it is not necessary to restrict the connection of U0 to ground if it should be desirable to use some other voltage.

The output ER may also be buffered, re-scaled and used as a general-purpose reference voltage. It is generated with respect to the negative supply line Pin 8 (VN), but this is acceptable when driving one of the signal interfaces. An example is shown in Figure 12, where a fixed numerator of 10 V is generated for a divider application. There, Y_2 is tied to VN but Y_1 is 10 V above this; therefore the common-mode voltage at this interface is still 5 V above VN, which satisfies the internal biasing requirements (see Specifications Table).

OPERATION AS A MULTIPLIER

All of the connection schemes used in this section are essentially identical to those used for the AD534, with which the AD734 is pin-compatible. The only precaution to be noted in this regard is that in the AD534, Pins 3, 5, 9, and 13 are not internally connected and Pin 4 has a slightly different purpose. In many cases, an AD734 can be directly substituted for an AD534 with immediate benefits in static accuracy, distortion, feedthrough, and speed. Where Pin 4 was used in an AD534 application to achieve a reduced denominator voltage, this function can now be much more precisely implemented with the AD734 using alternative connections (see Direct Denominator Control, page 5).

Operation from supplies down to ±8 V is possible. The supply current is essentially independent of voltage. As is true of all high speed circuits, careful power-supply decoupling is important in maintaining stability under all conditions of use. The decoupling capacitors should always be connected to the load ground, since the load current circulates in these capacitors at high frequencies. Note the use of the special symbol (a triangle with the letter 'L' inside it) to denote the load ground.

Standard Multiplier Connections

Figure 5 shows the basic connections for multiplication. The X and Y inputs are shown as optionally having their negative nodes grounded, but they are fully differential, and in many applications the grounded inputs may be reversed (to facilitate interfacing with signals of a particular polarity, while achieving some desired output polarity) or both may be driven.

The AD734 has an input resistance of 50 kΩ ± 20% at the X, Y, and Z interfaces, which allows ac-coupling to be achieved

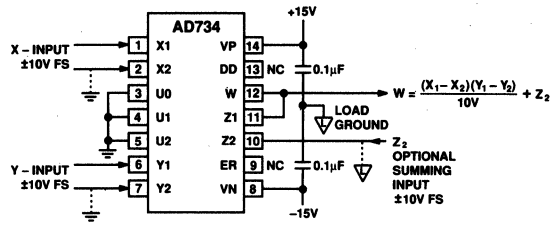


Figure 5. Basic Multiplier Circuit

with moderately good control of the high-pass (HP) corner frequency; a capacitor of 0.1 μF provides a HP corner frequency of 32 Hz. When a tighter control of this frequency is needed, or when the HP corner is above about 100 kHz, an external resistor should be added across the pair of input nodes.

At least one of the two inputs of any pair must be provided with a dc path (usually to ground). The careful selection of ground returns is important in realizing the full accuracy of the AD734. The Z2 pin will normally be connected to the load ground, which may be remote, in some cases. It may also be used as an optional summing input (see Equations (3) and (4), above) having a nominal FS input of ±10 V and the full 10 MHz bandwidth.

In applications where high absolute accuracy is essential, the scaling error caused by the finite resistance of the signal source(s) may be troublesome; for example, a 50 Ω source resistance at just one input will introduce a gain error of −0.1%; if both the X- and Y-inputs are driven from 50 Ω sources, the scaling error in the product will be −0.2%. Provided the source resistance(s) are known, this gain error can be completely compensated by including the appropriate resistance (50 Ω or 100 Ω, respectively, in the above cases) between the output W (Pin 12) and the Z1 feedback input (Pin 11). If Rx is the total source resistance associated with the X1 and X2 inputs, and Ry is the total source resistance associated with the Y1 and Y2 inputs, and neither Rx nor Ry exceeds 1 kΩ, a resistance of Rx+Ry in series with pin Z1 will provide the required gain restoration.

Pins 9 (ER) and 13 (DD) should be left unconnected in this application. The U-inputs (Pins 3, 4 and 5) are shown connected to ground; they may alternatively be connected to VN, if desired. In applications where Pin 2 (X2) happens to be driven with a high-amplitude, high-frequency signal, the capacitive coupling to the denominator control circuitry via an ungrounded Pin 3 can cause high-frequency distortion. However, the AD734 can be operated without modification in an AD534 socket, and these three pins left unconnected, with the above caution noted.

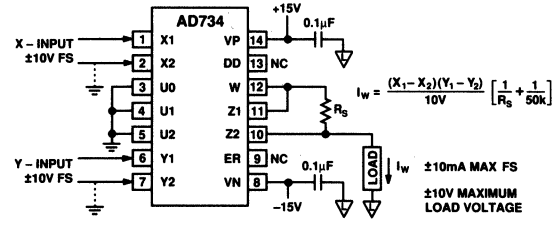


Figure 6. Conversion of Output to a Current

Current Output

It may occasionally be desirable to convert the output voltage to a current. In correlation applications, for example, multiplication is followed by integration; if the output is in the form of a current, a simple grounded capacitor can perform this function. Figure 6 shows how this can be achieved. The op-amp forces the voltage across Z1 and Z2, and thus across the resistor R_S, to be the product XY/U. Note that the input resistance of the Z interface is in shunt with R_S, which must be calculated accordingly.

The smallest FS current is simply ±10 V/50 kΩ, or ±200 μA, with a tolerance of about 20%. To guarantee a 1% conversion tolerance without adjustment, R_S must be less than 2.5 kΩ. The maximum full scale output current should be limited to about ±10 mA (thus, R_S = 1 kΩ). This concept can be applied to all connection modes, with the appropriate choice of terminals.

Squaring and Frequency-Doubling

Squaring of an input signal, E, is achieved simply by connecting the X and Y inputs in parallel; the phasing can be chosen to produce an output of E^2/U or $-E^2/U$ as desired. The input may have either polarity, but the basic output will either always be positive or negative; as for multiplication, the Z2 input may be used to add a further signal to the output.

When the input is a sinewave, a squarer behaves as a frequency doubler, since

$$(Esin\omega t)^2 = E^2\,(1 - cos2\omega t)/2 \qquad (8)$$

Equation (8) shows a dc term at the output which will vary strongly with the amplitude of the input, E. This dc term can be avoided using the connection shown in Figure 7, where an RC-network is used to generate two signals whose product has no dc term. The output is

$$W = 4\left\{\frac{E}{\sqrt{2}}\,sin\left(\omega t + \frac{\pi}{4}\right)\right\}\left\{\frac{E}{\sqrt{2}}\,sin\left(\omega t - \frac{\pi}{4}\right)\right\}\left(\frac{1}{10\ V}\right) \qquad (9)$$

for ω = 1/CR1, which is just

$$W = E^2(cos2\omega t)/(10\ V) \qquad (10)$$

which has no dc component. To restore the output to ±10 V when E = 10 V, a feedback attenuator with an approximate ratio of 4 is used between W and Z1; this technique can be used wherever it is desired to achieve a higher overall gain in the transfer function.

In fact, the values of R3 and R4 include additional compensation for the effects of the 50 kΩ input resistance of all three interfaces; R2 is included for a similar reason. These resistor values should not be altered without careful calculation of the consequences; with the values shown, the center frequency f_0 is 100 kHz for C = 1 nF. The amplitude of the output is only a weak function of frequency: the output amplitude will be 0.5% too low at f = $0.9f_0$ and f = $1.1f_0$. The cross-connection is simply to produce the cosine output with the sign shown in Equation (10); however, the sign in this case will rarely be important.

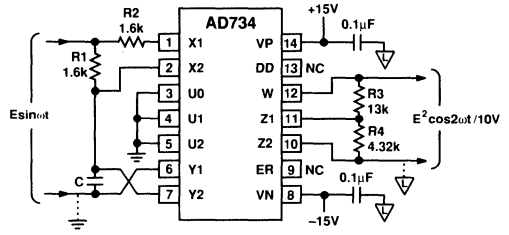


Figure 7. Frequency Doubler

OPERATION AS A DIVIDER

The AD734 supports two methods for performing analog division. The first is based on the use of a multiplier in a feedback loop. This is the standard mode recommended for multipliers having a fixed scaling voltage, such as the AD534, and will be described in this Section. The second uses the AD734's unique capability for externally varying the scaling (denominator) voltage directly, and will be described in the next section.

Feedback Divider Connections

Figure 8 shows the connections for the standard (AD534) divider mode. Feedback from the output, W, is now taken to the Y2 (inverting) input, which, provided that the X-input is positive, establishes a negative feedback path. Y1 should normally be connected to the ground associated with the load circuit, but may optionally be used to sum a further signal to the output. If desired, the polarity of the Y-input connections can be reversed, with W connected to Y1 and Y2 used as the optional summation input. In this case, either the polarity of the X-input connections must be reversed, or the X-input voltage must be negative.

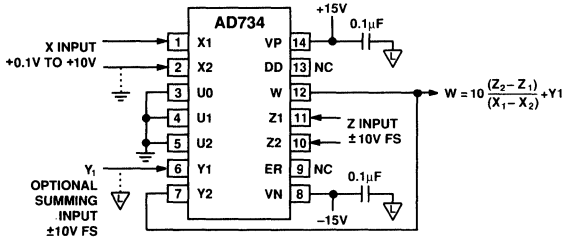


Figure 8. Standard (AD534) Divider Connection

The numerator input, which is differential and can have either polarity, is applied to pins Z1 and Z2. As with all dividers based on feedback, the bandwidth is directly proportional to the denominator, being 10 MHz for X = 10 V and reducing to 100 kHz for X = 100 mV. This reduction in bandwidth, and the increase in output noise (which is inversely proportional to the denominator voltage) preclude operation much below a denominator of 100 mV. Division using direct control of the denominator (Figure 10) does not have these shortcomings.

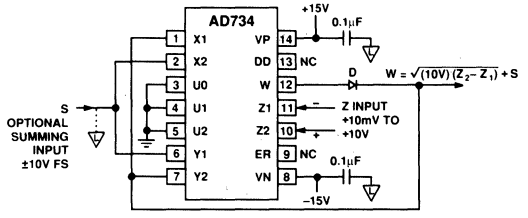


Figure 9. Connection for Square Rooting

Connections for Square-Rooting

The AD734 may be used to generate an output proportional to the square-root of an input using the connections shown in Figure 9. Feedback is now via both the X and Y inputs, and is always negative because of the reversed-polarity between these two inputs. The Z input must have the polarity shown, but because it is applied to a differential port, either polarity of input can be accepted with reversal of Z1 and Z2, if necessary. The diode D, which can be any small-signal type (1N4148 being suitable) is included to prevent a latching condition which could occur if the input momentarily was of the incorrect polarity of the input, the output will be always negative.

Note that the loading on the output side of the diode will be provided by the 25 kΩ of input resistance at X1 and Y2, and by the user's load. In high speed applications it may be beneficial to include further loading at the output (to 1 kΩ minimum) to speed up response time. As in previous applications, a further signal, shown here as S, may be summed to the output; if this option is not used, this node should be connected to the load ground.

DIVISION BY DIRECT DENOMINATOR CONTROL

The AD734 may be used as an analog divider by directly varying the denominator voltage. In addition to providing much higher accuracy and bandwidth, this mode also provides greater flexibility, because all inputs remain available. Figure 10 shows the connections for the general case of a three-input multiplier divider, providing the function

$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{(U_1 - U_2)} + Z_2, \qquad (11)$$

where the X, Y, and Z signals may all be positive or negative, but the difference $U = U_1 - U_2$ must be positive and in the range +10 mV to +10 V. If a negative denominator voltage must be used, simply ground the noninverting input of the op amp. As previously noted, the X input must have a magnitude of less than 1.25U.

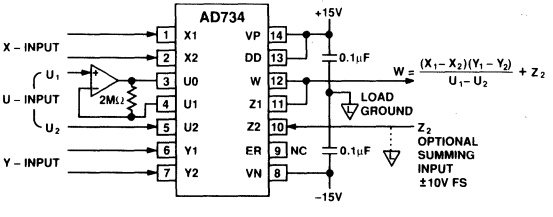


Figure 10. Three-Variable Multiplier/Divider Using Direct Denominator Control

This connection scheme may also be viewed as a variable-gain element, whose output, in response to a signal at the X input, is controllable by both the Y input (for attenuation, using Y less than U) and the U input (for amplification, using U less than Y). The ac performance is shown in Figure 11; for these results, Y was maintained at a constant 10 V. At U = 10 V, the gain is unity and the circuit bandwidth is a full 10 MHz. At U = 1 V, the gain is 20 dB and the bandwidth is essentially unaltered. At U = 100 mV, the gain is 40 dB and the bandwidth is 2 MHz. Finally, at U = 10 mV, the gain is 60 dB and the bandwidth is 250 kHz, corresponding to a 250 MHz gain-bandwidth product.

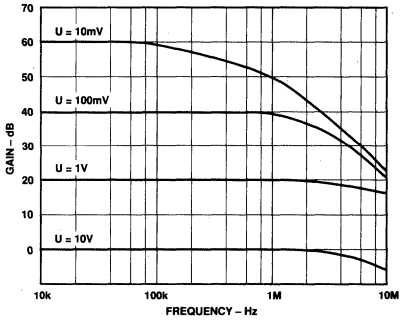


Figure 11. Three-Variable Multiplier/Divider Performance

The 2 MΩ resistor is included to improve the accuracy of the gain for small denominator voltages. At high gains, the X input offset voltage can cause a significant output offset voltage. To eliminate this problem, a low-pass feedback path can be used from W to X2; see Figure 13 for details.

Where a numerator of 10 V is needed, to implement a two-quadrant divider with fixed scaling, the connections shown in Figure 12 may be used. The reference voltage output appearing between Pin 9 (ER) and Pin 8 (VN) is amplified and buffered by the second op amp, to impose 10 V across the Y1/Y2 input. Note that Y2 is connected to the negative supply in this application. This is permissable because the common-mode voltage is still high enough to meet the internal requirements. The transfer function is

$$W = 10V\left(\frac{X_1 - X_2}{U_1 - U_2}\right) + Z_2. \qquad (12)$$

The ac performance of this circuit remains as shown in Figure 11.

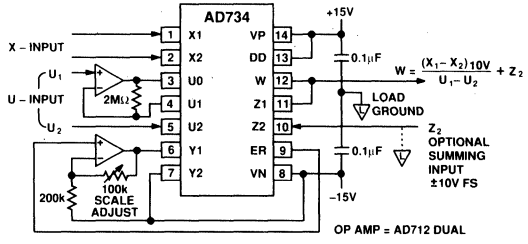


Figure 12. Two-Quadrant Divider with Fixed 10 V Scaling

A PRECISION AGC LOOP

The variable denominator of the AD734 and its high gain-bandwidth product make it an excellent choice for precise automatic gain control (AGC) applications. Figure 13 shows a suggested method. The input signal, E_{IN}, which may have a peak amplitude of from 10 mV to 10 V at any frequency from 100 Hz to 10 MHz, is applied to the X input, and a fixed positive voltage E_C to the Y input. Op amp A2 and capacitor C2 form an integrator having a current summing node at its inverting input. (The AD712 dual op amp is a suitable is a suitable choice for this application.) In the absence of an input, the current in D2 and R2 causes the integrator output to ramp negative, clamped by diode D3, which is included to reduce the time required for the loop to establish a stable, calibrated, output level once the circuit has received an input signal. With no input to the denominator (U0 and U2), the gain of the AD734 is very high (about 70 dB), and thus even a small input causes a substantial output.

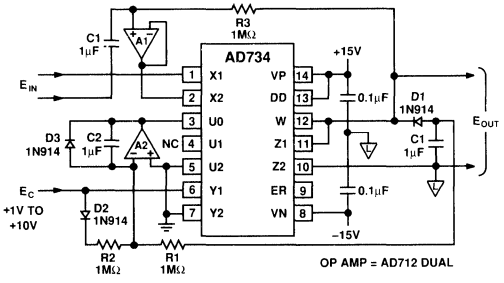


Figure 13. Precision AGC Loop

Diode D1 and C1 form a peak detector, which rectifies the output and causes the integrator to ramp positive. When the current in R1 balances the current in R2, the integrator output holds the denominator output at a constant value. This occurs when there is sufficient gain to raise the amplitude of E_{IN} to that required to establish an output amplitude of E_C over the range of +1 V to +10 V. The X input of the AD734, which has finite offset voltage, could be troublesome at the output at high gains. The output offset is reduced to that of the X input (one or two millivolts) by the offset loop comprising R3, C3, and buffer A1. The low pass corner frequency of 0.16 Hz is transformed to a high-pass corner that is multiplied by the gain (for example, 160 Hz at a gain of 1000).

In applications not requiring operation down to low frequencies, amplifier A1 can be eliminated, but the AD734's input resistance of 50 kΩ between X1 and X2 will reduce the time constant and increase the input offset. Using a non-polar 20 μF tantalum capacitor for C1 will result in the same unity-gain high-pass corner; in this case, the offset gain increases to 20, still very acceptable.

Figure 14 shows the error in the output for sinusoidal inputs at 100 Hz, 100 kHz, and 1 MHz, with E_C set to +10 V. The output error for any frequency between 300 Hz and 300 kHz is similar to that for 100 kHz. At low signal frequencies and low input amplitudes, the dynamics of the control loop determine the gain error and distortion; at high frequencies, the 200 MHz gain-bandwidth product of the AD734 limit the available gain.

The output amplitude tracks E_C over the range +1 V to slightly more than +10 V.

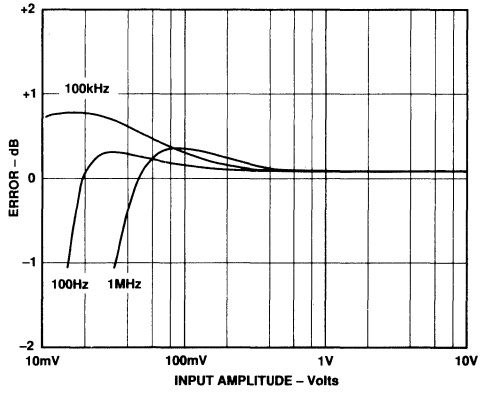


Figure 14. AGC Amplifier Output Error vs. Input Voltage

WIDEBAND RMS-DC CONVERTER USING U INTERFACE

The AD734 is well suited to such applications as implicit RMS-DC conversion, where the AD734 implements the function

$$V_{RMS} = \frac{avg\,[V_{IN}^2]}{V_{RMS}} \qquad (13)$$

using its direct divide mode. Figure 15 shows the circuit.

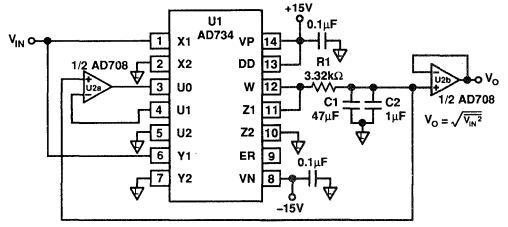


Figure 15. A 2-Chip, Wideband RMS-DC Converter

In this application, the AD734 and an AD708 dual op amp serve as a 2-chip RMS-DC converter with a 10 MHz bandwidth. Figure 16 shows the circuit's performance for square-, sine-, and triangle-wave inputs. The circuit accepts signals as high as 10 V p–p with a crest factor of 1 or 1 V p–p with a crest factor of 10. The circuit's response is flat to 10 MHz with an input of 10 V, flat to almost 5 MHz for an input of 1 V, and to almost 1 MHz for inputs of 100 mV. For accurate measurements of input levels below 100 mV, the AD734's output offset (Z interface) voltage, which contributes a dc error, must be trimmed out.

In Figure 15's circuit, the AD734 squares the input signal, and its output (V_{IN}^2) is averaged by a low-pass filter that consists of R1 and C1 and has a corner frequency of 1 Hz. Because of the implicit feedback loop, this value is both the output value, V_{RMS}, and the denominator in Equation (13). U2a and U2b, an AD708 dual dc precision op amp, serve as unity-gain buffers, supplying both the output voltage and driving the U interface.

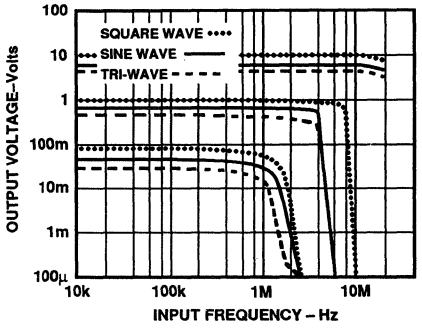


Figure 16. RMS-DC Converter Performance

LOW DISTORTION MIXER

The AD734's low noise and distortion make it especially suitable for use as a mixer, modulator, or demodulator. Although the AD734's −3 dB bandwidth is typically 10 MHz and is established by the output amplifier, the bandwidth of its X and Y interfaces and the multiplier core are typically in excess of 40 MHz. Thus, provided that the desired output signal is less than 10 MHz, as would typically be the case in demodulation, the AD734 can be used with both its X and Y input signals as high as 40 MHz. One test of mixer performance is to linearly combine two closely spaced, equal-amplitude sinusoidal signals and then mix them with a third signal to determine the mixer's 2-tone Third-Order Intermodulation Products.

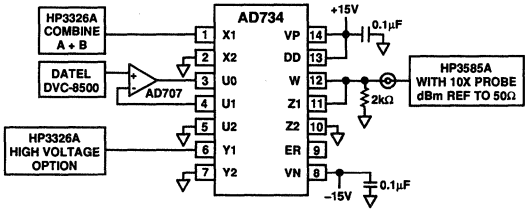


Figure 17. AD734 Mixer Test Circuit

Figure 17 shows a test circuit for measuring the AD734's performance in this regard. In this test, two signals, at 10.05 MHz and 9.95 MHz are summed and applied to the AD734's X interface. A second 9 MHz signal is applied to the AD734's Y interface. The voltage at the U interface is set to 2 V to use the full dynamic range of the AD734. That is, by connecting the W and Z1 pins together, grounding the Y2 and X2 pins, and setting U = 2 V, the overall transfer function is

$$W = \frac{X_1 Y_1}{2\,V} \qquad (14)$$

and W can be as high as 20 V p–p when X1 = 2 V p–p and Y1 = 10 V p–p. The 2 V p–p signal level corresponds to +10 dBm into a 50 Ω input termination resistor connected from X1 or Y1 to ground.

If the two X1 inputs are at frequencies f_1 and f_2 and the frequency at the Y1 input is f_0, then the two-tone third-order intermodulation products should appear at frequencies $2f_1 - f_2 \pm f_0$ and $2f_2 - f_1 \pm f_0$. Figures 18 and 19 show the output spectra of the AD734 with f_1 = 9.95 MHz, f_2 = 10.05 MHz, and f_0 = 9.00 MHz for a signal level of f_1 & f_2 of 6 dBm and f_0 of +24 dBm in Figure 18 and f_1 & f_2 of 0 dBm and f_0 of +24 dBm in Figure 19. This performance is *without* external trimming of the AD734's X and Y input-offset voltages.

The possible Two Tone Intermodulation Products are at 2 × 9.95 MHz − 10.05 MHz ± 9.00 MHz and 2 × 10.05 − 9.95 MHz ±9.00 MHz; of these only the third-order products at 0.850 MHz and 1.150 MHz are within the 10 MHz bandwidth of the AD734; the desired output signals are at 0.950 MHz and 1.050 MHz. Note that the difference (Figure 18) between the desired outputs and third-order products is approximately 78 dB, which corresponds to a computed third-order intercept point of +46 dBm.

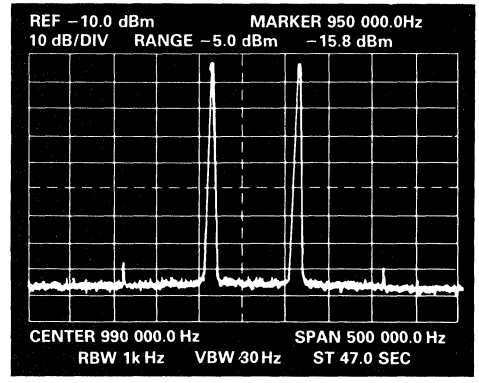


Figure 18. AD734 Third-Order Intermodulation Performance for f_1 = 9.95 MHz, f_2 = 10.05 MHz, and f_0 = 9.00 MHz and for Signal Levels of f_1 & f_2 of 6 dBm and f_0 of +24 dBm. All Displayed Signal Levels Are Attenuated 20 dB by the 10X Probe Used to Measure the Mixer's Output

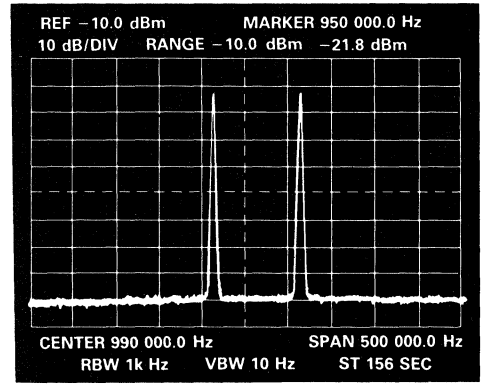


Figure 19. AD734 Third-Order Intermodulation Performance for f_1 = 9.95 MHz, f_2 = 10.05 MHz, and f_0 = 9.00 MHz and for Signal Levels of f_1 & f_2 of 0 dBm and f_0 of +24 dBm. All Displayed Signal Levels Are Attenuated 20 dB by the 10X Probe Used to Measure the Mixer's Output

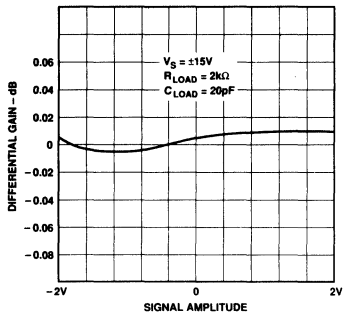


Figure 20. Differential Gain at 3.58 MHz and R_L = 2 kΩ

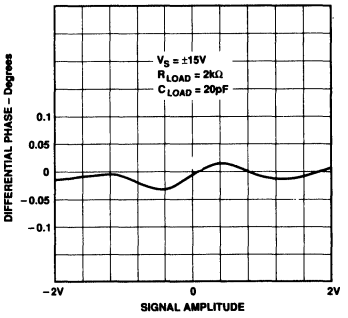


Figure 21. Differential Phase at 3.58 MHz and R_L = 2 kΩ

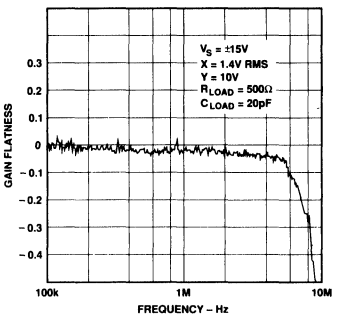


Figure 22. Gain Flatness, 300 kHz to 10 MHz, R_L = 500 Ω

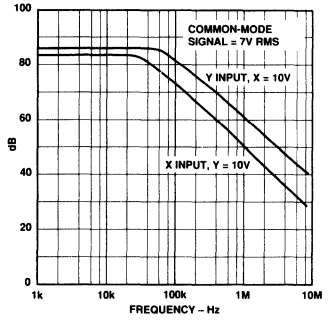


Figure 23. CMRR vs. Frequency

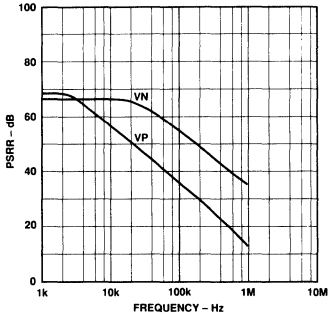


Figure 24. PSRR vs. Frequency

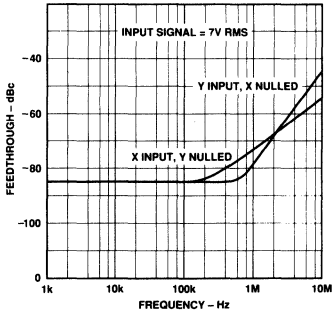


Figure 25. Feedthrough vs. Frequency

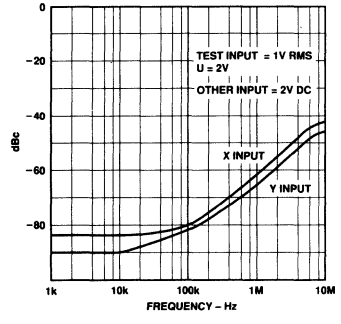


Figure 26. THD vs. Frequency, U = 2 V

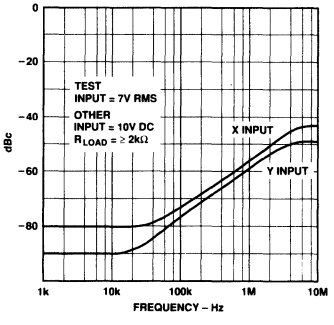


Figure 27. THD vs. Frequency, U = 10 V

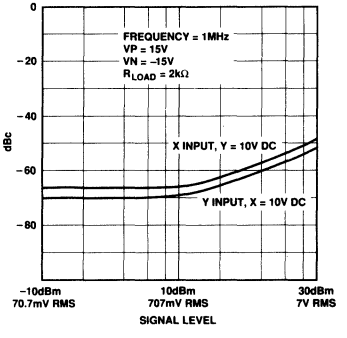


Figure 28. THD vs. Signal Level, f = 1 MHz

AD734—Typical Characteristics

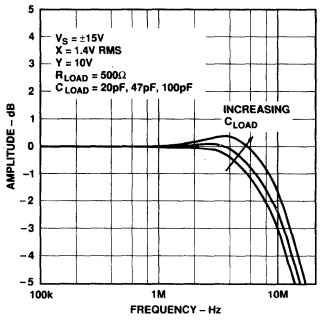


Figure 29. Gain vs. Frequency vs. C_{LOAD}

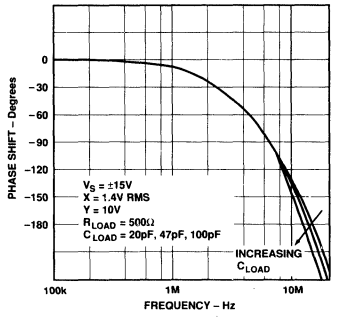


Figure 30. Phase vs. Frequency vs. C_{LOAD}

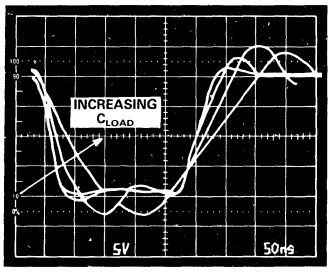


Figure 31. Pulse Response vs. C_{LOAD}, C_{LOAD} = 0 pF, 47 pF, 100 pF, 200 pF

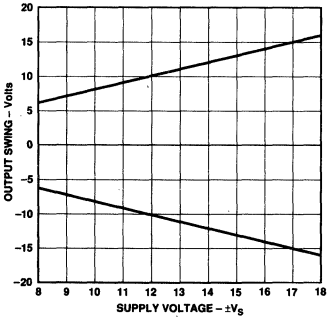


Figure 32. Output Swing vs. Supply Voltage

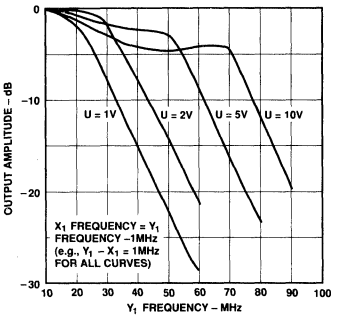


Figure 33. Output Amplitude vs. Input Frequency, When Used as Demodulator

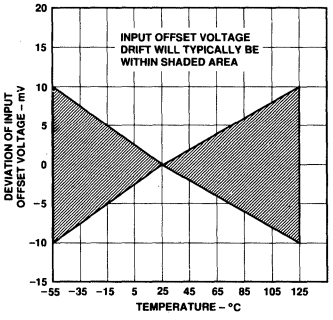


Figure 34. V_{OS} Drift, X Input

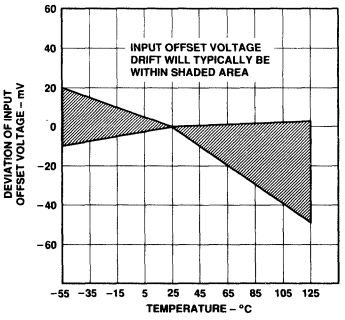


Figure 35. V_{OS} Drift, Z Input

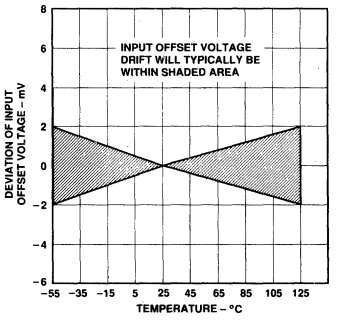


Figure 36. V_{OS} Drift, Y Input

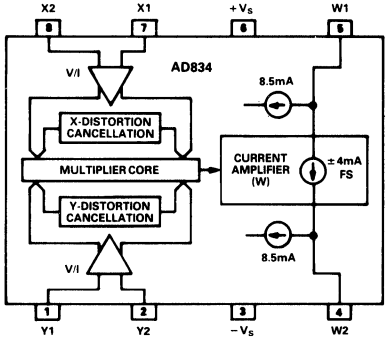
500MHz Four-Quadrant Multiplier

AD834

FEATURES
DC to >500MHz Operation
Differential ±1V Full Scale Inputs
Differential ±4mA Full Scale Output Current
Low Distortion (≤0.05% for 0dBm Input)
Supply Voltages from ±4V to ±9V
Low Power (280mW typical at V_S=±5V)

APPLICATIONS
High Speed Real Time Computation
Wideband Modulation and Gain Control
Signal Correlation and RF Power Measurement
Voltage Controlled Filters and Oscillators
Linear Keyers for High Resolution Television
Wideband True RMS

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD834 is a monolithic laser-trimmed four-quadrant analog multiplier intended for use in high frequency applications, having a transconductance bandwidth (R_L=50Ω) in excess of 500MHz from either of the differential voltage inputs. In multiplier modes, the typical total full scale error is 0.5%, dependent on the application mode and the external circuitry. Performance is relatively insensitive to temperature and supply variations, due to the use of stable biasing based on a bandgap reference generator and other design features.

To preserve the full bandwidth potential of the high speed bipolar process used to fabricate the AD834, the outputs appear as a differential pair of currents at open collectors. To provide a single ended ground referenced voltage output, some form of external current to voltage conversion is needed. This may take the form of a wideband transformer, balun, or active circuitry such as an op amp. In some applications (such as power measurement) the subsequent signal processing may not need to have high bandwidth.

The transfer function is accurately trimmed such that when X=Y=±1V, the differential output is ±4mA. This absolute calibration allows the outputs of two or more AD834s to be summed with precisely equal weighting, independent of the accuracy of the load circuit.

The AD834J is specified for use over the commercial temperature range of 0 to +70°C and is available in an 8-pin plastic DIP package and an 8-pin plastic SOIC package. AD834A is available in cerdip for operation over the industrial temperature range of −40°C to +85°C. The AD834S/883B is specified for operation over the military temperature range of −55°C to +125°C and is available in the 8-pin cerdip package. S-Grade chips are also available.

PRODUCT HIGHLIGHTS

1. The AD834 combines high static accuracy (low input and output offsets and accurate scale factor) with very high bandwidth. As a four-quadrant multiplier or squarer, the response extends from dc to an upper frequency limited mainly by packaging and external board layout considerations. A large signal bandwidth of over 500MHz is attainable under optimum conditions.
2. The AD834 can be used in many high speed nonlinear operations, such as square rooting, analog division, vector addition and rms-to-dc conversion. In these modes, the bandwidth is limited by the external active components.
3. Special design techniques result in low distortion levels (better than −60dB on either input) at high frequencies and low signal feedthrough (typically −65dB up to 20MHz).
4. The AD834 exhibits low differential phase error over the input range—typically 0.08° at 5MHz and 0.8° at 50MHz. The large signal transient response is free from overshoot, and has an intrinsic rise time of 500ps, typically settling to within 1% in under 5ns.
5. The nonloading, high impedance, differential inputs simplify the application of the AD834.

AD834—SPECIFICATIONS (T_A=+25°C and $\pm V_S$=±5V, unless otherwise noted; dBm assumes 50Ω load.)

Model	Conditions	AD834J Min	AD834J Typ	AD834J Max	AD834A, S Min	AD834A, S Typ	AD834A, S Max	Units
MULTIPLIER PERFORMANCE								
Transfer Function			$W = \frac{XY}{(1V)^2} \times 4mA$			$W = \frac{XY}{(1V)^2} \times 4mA$		
Total Error[1] (Figure 6)	−1V≤X,Y<+1V		±0.5	**±2**		±0.5	**±2**	% FS
vs. Temperature	T_{min} to T_{max}					±1.5	**±3**	% FS
vs. Supplies[2]	±4V to ±6V		0.1	**0.3**		0.1	**0.3**	% FS/V
Linearity[3]			±0.5	**±1**		±0.5	**±1**	% FS
Bandwidth[4]	See Figure 5	500			500			MHz
Feedthrough, X	X=±1V, Y=Nulled		0.2	**0.3**		0.2	**0.3**	% FS
Feedthrough, Y	X=Nulled, Y=±1V		0.1	**0.2**		0.1	**0.2**	% FS
AC Feedthrough, X[5]	X=0dBm, Y=Nulled							
	f=10MHz		−65			−65		dB
	f=100MHz		−50			−50		dB
AC Feedthrough, Y[5]	X=Nulled, Y=0dBm							
	f=10MHz		−70			−70		dB
	f=100MHz		−50			−50		dB
INPUTS (X1, X2, Y1, Y2)								
Full Scale Range	Differential		±1			±1		V
Clipping Level	Differential	**±1.1**	±1.3		**±1.1**	±1.3		V
Input Resistance	Differential		25			25		kΩ
Offset Voltage			0.5	**3**		0.5	**3**	mV
vs. Temperature	T_{min} to T_{max}		10			10		µV/°C
				4			**4**	mV
vs. Supplies[2]	±4V to ±6V		100	**300**		100	**300**	µV/V
Bias Current			45			45		µA
Common Mode Rejection	f≤100kHz; 1V p-p		70			70		dB
Nonlinearity, X	Y=1V; X=±1V		0.2	**0.5**		0.2	**0.5**	% FS
Nonlinearity, Y	X=1V; Y=±1V		0.1	**0.3**		0.1	**0.3**	% FS
Distortion, X	X=0dBm, Y=1V							
	f=10MHz		−60			−60		dB
	f==100MHz		−44			−44		dB
Distortion, Y	X=1V, Y=0dBM							
	f=10MHz		−65			−65		dB
	f=100MHz		−50			−50		dB
OUTPUTS (W1, W2)								
Zero Signal Current	Each Output		8.5			8.5		mA
Differential Offset	X=0, Y=0		±20	**±60**		±20	**±60**	µA
vs. Temperature	T_{min} to T_{max}		40			40		nA/°C
							±60	µA
Scaling Current	Differential	3.96	4	4.04	3.96	4	4.04	mA
Output Compliance		4.75		9	4.75		9	V
Noise Spectral Density	f=10Hz to 1MHz Outputs into 50Ω Load		16			16		nV/$\sqrt{Hz}$
POWER SUPPLIES								
Operating Range		±4		±9	±4		±9	V
Quiescent Current[6]	T_{min} to T_{max}							
$+V_S$			11	**14**		11	**14**	mA
$-V_S$			28	**35**		28	**35**	mA
TEMPERATURE RANGE								
Operating, Rated Performance								
Commercial (0 to +70°C)			AD834J					
Military (−55°C to +125°C)						AD834S		
Industrial (−40°C to +85°C)						AD834A		
PACKAGE OPTIONS[7]								
8-Pin SOIC (R)			AD834JR					
8-Pin Cerdip (Q)						AD834AQ		
8-Pin Plastic DIP (N)			AD834JN			AD834SQ/883B		

NOTES

[1]Error is defined as the maximum deviation from the ideal output, and expressed as a percentage of the full scale output.

[2]Both supplies taken simultaneously; sinusoidal input at f≤10kHz.

[3]Linearity is defined as residual error after compensating for input offset voltage, output offset current and scaling current errors.

[4]Bandwidth is guaranteed when configured in squarer mode. See Figure 5.

[5]Sine input; relative to full scale output; zero input port nulled; represents feedthrough of the fundamental.

[6]Negative supply current is equal to the sum of positive supply current, the signal currents into each output, W1 and W2, and the input bias currents.

[7]For outline information see Package Information section.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($+V_S$ to $-V_S$) 18V
Internal Power Dissipation 500mW
Input Voltages (X1, X2, Y1, Y2) . . . . . $+V_S$
Operating Temperature Range
AD834J . . . . . 0 to +70°C
AD834A . . . . . −40°C to +85°C
AD834S/883B . . . . . −55°C to +125°C
Storage Temperature Range Q . . . . . −65°C to +150°C
Storage Temperature Range R, N . . . . . −65°C to +125°C
Lead Temperature, Soldering 60sec . . . . . +300°C

NOTE
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

	θ_{JC}	θ_{JA}
8-Pin Cerdip Package (Q)	30°C/W	110°C/W
8-Pin Plastic SOIC (R)	45°C/W	165°C/W
8-Pin Plastic Mini-DIP (N)	50°C/W	99°C/W

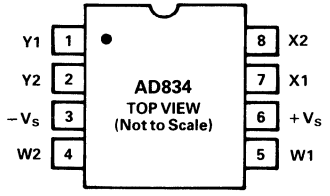
ORDERING GUIDE

Model	Temperature Range	Package Option*
AD834JN	0 to +70°C	N-8
AD834JQ	0 to +70°C	Q-8
AD834JR	0 to +70°C	R-8
AD834AQ	−40°C to +85°C	Q-8
AD834SQ/883B	−55°C to +125°C	Q-8
AD834S Chips		Chips

*N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC) Package.

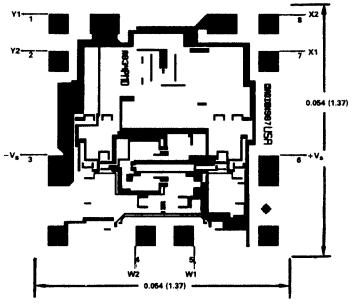
CONNECTION DIAGRAM

Small Outline (R) Package
Plastic DIP (N) Package
Cerdip (Q) Package



METALIZATION PHOTO

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



8

AD834—Typical Characteristics

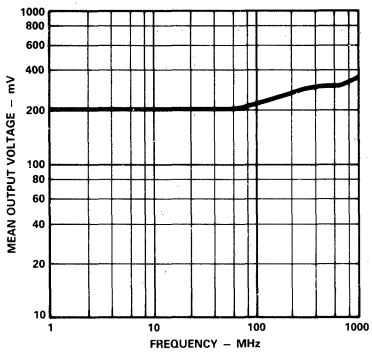


Figure 1. Mean-Square Output vs. Frequency

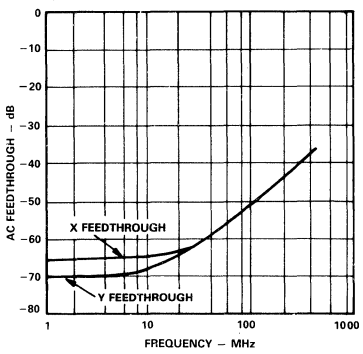


Figure 2. AC Feedthrough vs. Frequency

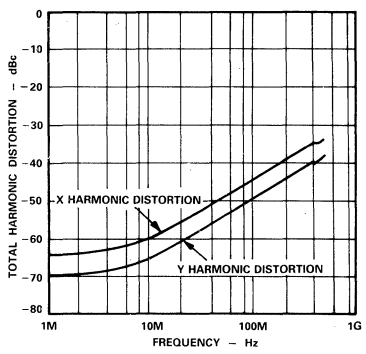


Figure 3. Total Harmonic Distortion vs. Frequency

Figure 1. Figure 1 is a plot of the mean-square output versus frequency for the test circuit of Figure 5. Note that the rising response is due to package resonances.

Figure 2. For frequencies below 1MHz, ac feedthrough is dominated by static nonlinearities in the transfer function and the finite offset voltages. The offset voltages cause a small fraction of the fundamental to appear at the output, and can be nulled out.

Figure 3. THD data represented in Figure 3 is dominated by the second harmonic, and is generated with 0dBm input on the ac input and +1V on the dc input. For a given amplitude on the ac input, THD is relatively insensitive to changes in the dc input amplitude. Varying the ac input amplitude while maintaining a constant dc input amplitude will affect THD performance.

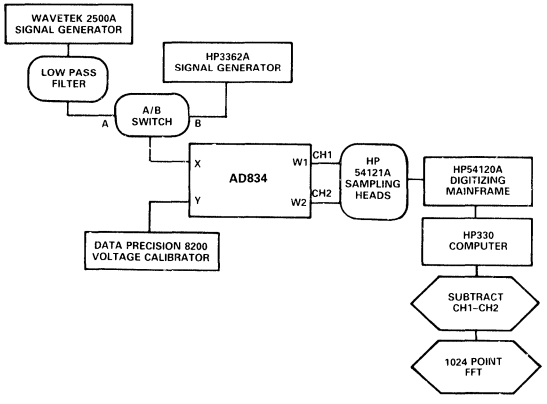


Figure 4. Test Configuration for Measuring ac Feedthrough and Total Harmonic Distortion

Figure 5. The squarer configuration shown in Figure 5 is used to determine wideband performance because it eliminates the need for (and the response uncertainties of) a wideband measurement device at the output. The wideband output of a squarer configuration is a fluctuating current at twice the input frequency with a mean value proportional to the square of the input amplitude.

By placing capacitors C3/C5 and C4/C6 across load resistors R1 and R2, a simple low-pass filter is formed, and the mean-square value is extracted. The mean-square response can be measured using a DVM connected across R1 and R2.

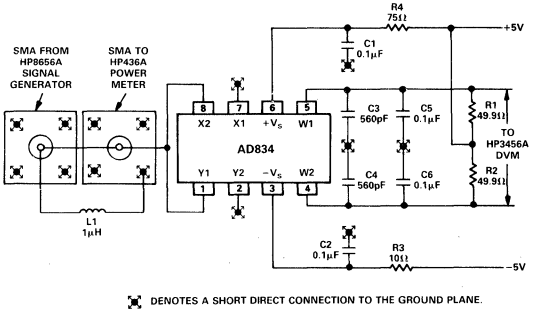


Figure 5. Bandwidth Test Circuit

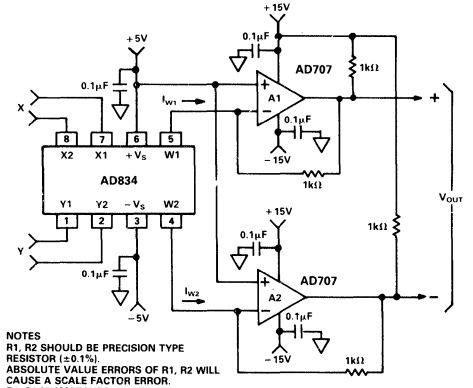


Figure 6. Low Frequency Test Circuit

BASIC OPERATION

Figure 7 is a functional equivalent of the AD834. There are three differential signal interfaces: the voltage inputs X= X1−X2 and Y=Y1−Y2, and the current output, W (see Fig. 7) which flows in the direction shown when X and Y are positive. The outputs W1 and W2 each have a standing current of typically 8.5mA.

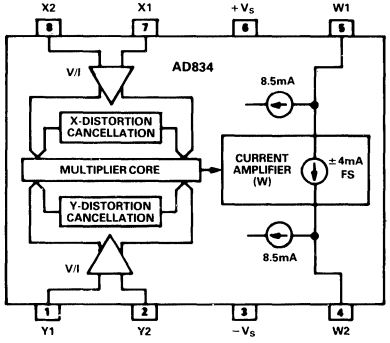


Figure 7. AD834 Functional Block Diagram

The input voltages are first converted to differential currents which drive the translinear core. The equivalent resistance of the voltage-to-current (V-I) converters is about 285Ω. This low value results in low input related noise and drift. However, the low full scale input voltage results in relatively high nonlinearity in the V-I converters. This is significantly reduced by the use of distortion cancellation circuits which operate by Kelvin sensing the voltages generated in the core — an important feature of the AD834.

The current mode output of the core is amplified by a special cascode stage which provides a current gain of nominally ×1.6, trimmed during manufacture to set up the full scale output current of ±4mA. **This output appears at a pair of open collectors which must be supplied with a voltage slightly above the voltage on Pin 6.** As shown in Figure 8, this can be arranged by inserting a resistor in series with the supply to this pin and taking the load resistors to the full supply. With R3=60Ω, the voltage drop across it is about 600mV. Using two 50Ω load resistors, the full scale differential output voltage is ±400mV.

The full bandwidth potential of the AD834 can only be realized when very careful attention is paid to grounding and decoupling. The device must be mounted close to a high quality ground plane and all lead lengths must be extremely short, in keeping with UHF circuit layout practice. In fact, the AD834 shows useful response to well beyond 1GHz, and the actual upper frequency in a typical application will usually be determined by the care with which the layout is effected. Note that R4 (in series with the $-V_S$ supply) carries about 30mA, and thus introduces a voltage drop of about 150mV. It is made large enough to reduce the Q of the resonant circuit formed by the supply lead and the decoupling capacitor. Slightly larger values can be used, particularly when using higher supply voltages. Alternatively, lossy RF chokes or ferrite beads on the supply leads may be used.

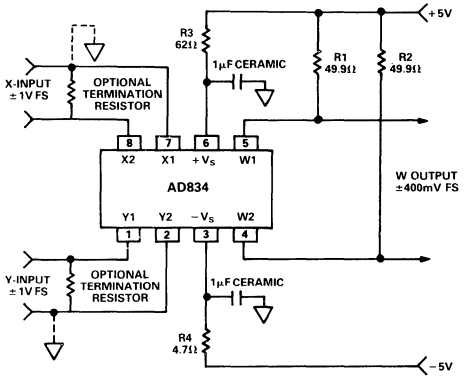


Figure 8. Basic Connections for Wideband Operation

Figure 8 shows the use of optional termination resistors at the inputs. Note that although the resistive component of the input impedance is quite high (about 25kΩ), the input bias current of typically 45μA can generate significant offset voltages if not compensated. For example, with a source and termination resistance of 50Ω (net source of 25Ω) the offset would be 25Ω×45μA=1.125mV. This can be almost fully cancelled by including (in this example) another 25Ω resistor in series with the "unused" input (in Figure 8, either X1 or Y2). In order to minimize crosstalk the input pins closest to the output (X1 and Y2) should be grounded; the effect is merely to reverse the phase of the X input and thus alter the polarity of the output.

TRANSFER FUNCTION

The output current W is the linear product of input voltages X and Y divided by $(1V)^2$ and multiplied by the "scaling current" of 4mA:

$$W = \frac{XY}{(1V)^2} \ 4mA$$

Provided that it is understood that the inputs are specified in *volts*, a simplified expression can be used:

$$W = (XY)\ 4mA$$

Alternatively, the full transfer function can be written:

$$W = \frac{XY}{1V} \cdot \frac{1}{250\Omega}$$

When both inputs are driven to their clipping level of about 1.3V, the peak output current is roughly doubled, to ±8mA, but distortion levels will then be very high.

TRANSFORMER COUPLING

In many high frequency applications where baseband operation is not required at either inputs or output, transformer coupling can be used. Figure 9 shows the use of a center-tapped output transformer, which provides the necessary dc load condition at the outputs W1 and W2, and is designed to match into the desired load impedance by appropriate choice of turns ratio. The specific choice of the transformer design will depend entirely on the application. Transformers may also be used at the inputs. Center-tapped transformers can reduce high frequency distortion and lower HF feedthrough by driving the inputs with balanced signals.

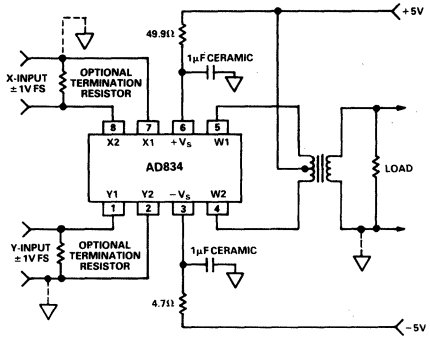


Figure 9. Transformer–Coupled Output

A particularly effective type of transformer is the balun[1] which is a short length of transmission line wound on to a toroidal ferrite core. Figure 10 shows this arrangement used to convert the bal(anced) output to an un(balanced) one (hence the use of the term). Although the symbol used is identical to that for a transformer, the mode of operation is quite different. In the first place, the load should now be equal to the characteristic impedance of the line (although this will usually not be critical for short line lengths). The collector load resistors R_C may also be chosen to reverse terminate the line, but again this will only be necessary when an electrically long line is used. In most cases, R_C will be made as large as the dc conditions allow, to minimize power loss to the load. The line may be a miniature coaxial cable or a twisted pair.

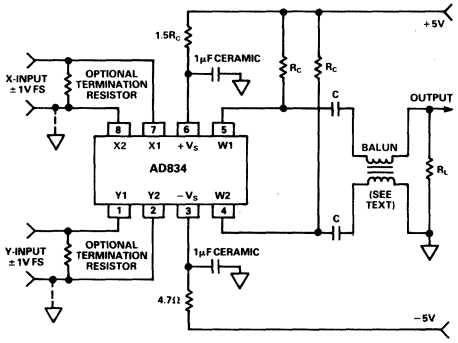


Figure 10. Using a Balun at the Output

It is important to note that the upper bandwidth limit of the balun is determined only by the quality of the transmission line; hence, it will usually exceed that of the multiplier. This is unlike a conventional transformer where the signal is conveyed as a flux in a magnetic core and is limited by core losses and leakage inductance. The lower limit on bandwidth is determined by the *series* inductance of the line, taken as a whole, and the load resistance (if the blocking capacitors C are sufficiently large). In practice, a balun can provide excellent differential-to-single-sided conversion over much wider bandwidths than a transformer.

[1]For a good treatment of baluns, see "Transmission Line Transformers" by Jerry Sevick; American Radio Relay League publication.

WIDEBAND MULTIPLIER CONNECTIONS

Where operation down to dc and a ground based output are necessary, the configuration shown in Figure 11 can be used. The element values were chosen in this example to result in a full-scale output of ±1V at the load, so the overall multiplier transfer function is

$$W = (X1-X2)(Y1-Y2)$$

where it is understood that the *inputs and output are in volts*. The polarity of the output can be reversed simply by reversing either the X or Y input.

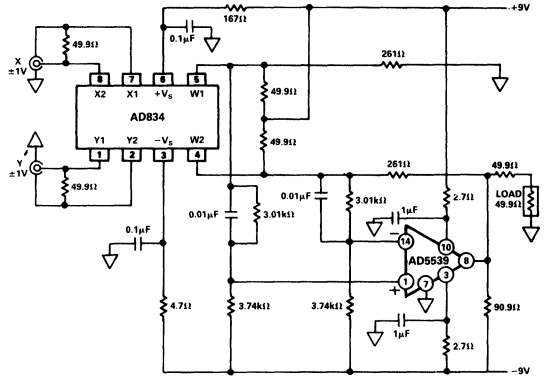


Figure 11. Wideband dc-Coupled Multiplier

The op amp should be chosen to support the desired output bandwidth. The AD5539 is shown here, providing an overall system bandwidth of 100MHz. Many other choices are possible where lower post multiplication bandwidths are acceptable. The level shifting network places the input nodes of the op amp to within a few hundred millivolts of ground using the recommended balanced supplies. The output offset may be nulled by including a 100Ω trim pot between each of the lower pair of resistors (3.74kΩ) and the negative supply.

The pulse response for this circuit shown in Figure 12; the X input was a pulse of 0 to +1V and the Y input was +1V dc. The transition times at the output are about 4ns.

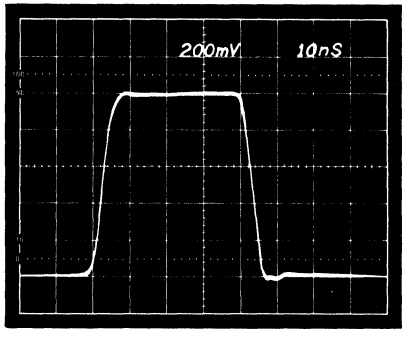


Figure 12. Pulse Response for the Circuit of Figure 11

POWER MEASUREMENT (MEAN SQUARE AND RMS)

The AD834 is well suited to measurement of average power in high frequency applications, connected either as a multiplier for the determination of the V×I product, or as a squarer for use with a single input. In these applications, the multiplier is followed by a low pass filter to extract the long term average value. Where the bandwidth extends to several hundred megahertz, the first pole of this filter should be formed by grounded capacitors placed directly at the output pins W1 and W2. This pole can be at a few kilohertz. The effective multiplication or squaring bandwidth is then limited solely by the AD834, since the following active circuitry is required to process only low frequency signals.

(Refer to Figure 5 test configuration.) Using the device as a squarer the wideband output in response to a sinusoidal stimulus is a raised cosine:

$$\sin^2\omega t = (1 + \cos 2\omega t)/2$$

Recall here that the full scale output current (when full scale input voltages of 1V are applied to both X and Y) is 4mA. In a 50Ω system, a sinusoid power of +10dBm has a peak value of 1V. Thus, at this drive level the peak output voltage across the differential 50Ω load in the absence of the filter capacitors would be 400mV (that is, 4mA ×50Ω×2), whereas the average value of the raised cosine is only 200mV. The averaging configuration is useful in evaluating the bandwidth of the AD834, since a dc voltage is easier to measure than a wideband, differential output. In fact, the squaring mode is an even more critical test than the direct measurement of the bandwidth of either channel taken independently (with a dc input on the nonsignal channel), because the phase relationship between the two channels also affects the average output. For example, a time delay difference of only 250ps between the X and Y channels would result in zero output when the input frequency is 1GHz, at which frequency the phase angle is 90 degrees and the intrinsic product is now between a sine and cosine function, which has zero average value.

The physical construction of the circuitry around the IC is critical to realizing the bandwidth potential of the device. The input is supplied from an HP8656A signal generator (100kHz to 990MHz) via an SMA connector and terminated by an HP436A power meter using an HP8482A sensor head connected via a second SMA connector. Since neither the generator nor the sensor provide a dc path to ground, a lossy 1μH inductor L1, formed by a 22-gauge wire passing through a ferrite bead (Fair-Rite type 2743001112) is included. This provides adequate impedance down to about 30MHz. The IC socket is mounted on a ground plane,with a clear area in the rectangle formed by the pins. This is important, since significant transformer action can arise if the pins pass through individual holes in the board; this has been seen to cause an oscillation at 1.3GHz in improperly constructed test jigs. The filter capacitors must be connected directly to the same point on the ground plane via the shortest possible leads. Parallel combinations of large and small capacitors are used to minimize the impedance over the full frequency range. (Refer to Figure 1 for mean-square response for the AD834 in cerdip package, using the configuration of Figure 5.)

To provide a square-root response and thus generate the rms value at the output, a second AD834, also connected as a squarer, can be used, as shown in Figure 13. Note that an attenuator is inserted both in the signal input and in the feedback path to the second AD834. This increases the maximum input capability to +15dBm and improves the response flatness by damping some of the resonances. The overall gain is unity; that is, the output voltage is exactly equal to the rms value of the input signal. The offset potentiometer at the AD834 outputs extends the dynamic range, and is adjusted for a dc output of 125.7mV when a 1MHz sinusoidal input at −5dBm is applied.

Additional filtering is provided; the time constants were chosen to allow operation down to frequencies as low as 1kHz and to provide a critically damped envelope response, which settles typically within 10ms for a full scale input (and proportionally slower for smaller inputs). The 5μF and 0.1μF capacitors may be scaled down to reduce response time if accurate rms operation at low frequencies is not required. The output op amp must be specified to accept a common-mode input near its supply. Note that the output polarity may be inverted by replacing the NPN transistor with a PNP type.

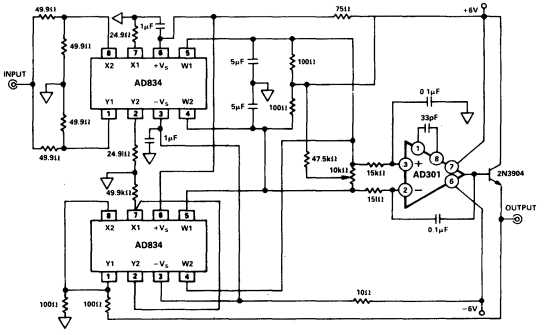


Figure 13. Connections for Wideband rms Measurement

FREQUENCY DOUBLER

Figure 14 shows another squaring application. In this case, the output filter has been removed and the wideband differential output is converted to a single sided signal using a "balun," which consists of a length of 50Ω coax cable fed through a ferrite core (Fair-Rite type 2677006301). No attempt is made to reverse terminate the output. Higher load power could be achieved by replacing the 50Ω load resistors by ferrite bead inductors. The same precautions should be observed with regard to PC board layout as recommended above. The output spectrum shown in Figure 15 is for an input power of +10dBm at a frequency of 200MHz. The second harmonic component at 400MHz has an output power of −15dBm. Some feedthrough of the fundamental occurs: it is 15dBs below the main output. It is believed that improvements in the design of the balun would reduce this feedthrough. A spurious output at 600MHz is also present, but it is 30dBs below the main output. At an input frequency of 100MHz, the measured power level at 200MHz is −16dBm, while the fundamental feedthrough is reduced to 25dBs below the main output; at an output of 600MHz the power is −11dBm and the third harmonic at 900MHz is 32dBs below the main output.

8

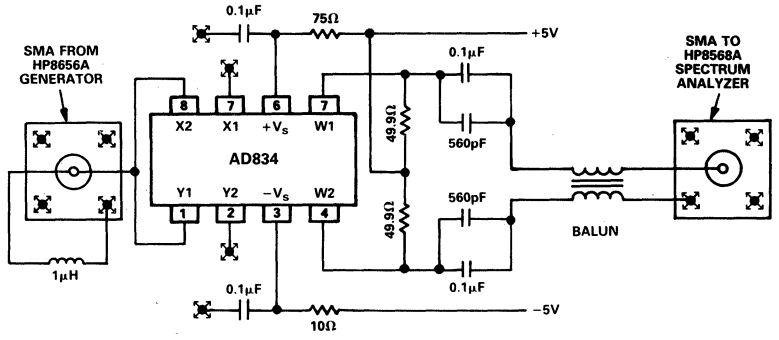


Figure 14. Frequency Doubler Connections

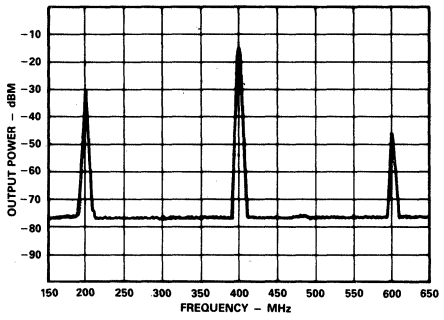


Figure 15. Output Spectrum for Configuration of Figure 14

WIDEBAND THREE SIGNAL MULTIPLIER/DIVIDER

Two AD834s and a wideband op amp can be connected to make a versatile multiplier/divider having the transfer function

$$W = \frac{(X1-X2)(Y1-Y2)}{(U1-U2)} + Z$$

with a denominator range of about 100:1. The denominator input U = U1−U2 must be positive and in the range 100mV to 10V; X, Y and Z inputs may have either polarity. Figure 16 shows a general configuration which may be simplified to suit a particular application. This circuit accepts full scale input voltages of 10V, and delivers a full scale output voltage of 10V. The optional offset trim at the output of the AD834 improves the accuracy for small denominator values. It is adjusted by nulling the output voltage when the X and Y inputs are zero and U = +100mV.

The AD840 is internally compensated to be stable without the use of any additional HF compensation. As the input U is reduced, the bandwidth falls because the feedback around the op amp is proportional to the input U.

This circuit may be modified in several ways. For example, if the differential input feature is not needed, the unused input

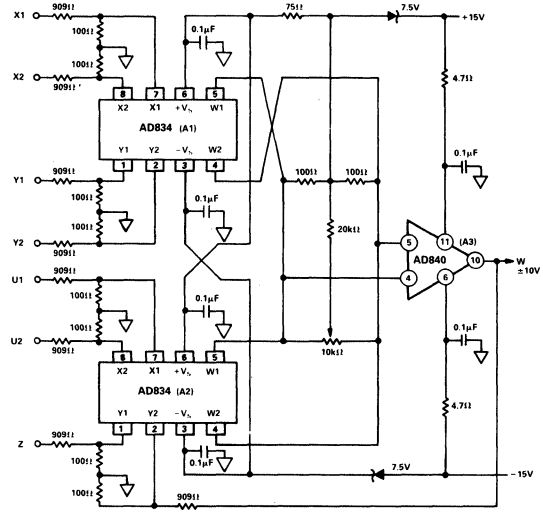


Figure 16. Wideband Three Signal Multiplier/Divider

can be connected to ground through a single resistor, equal to the parallel sum of the resistors in the attenuator section. The full scale input levels on X, Y and U can be adapted to any full scale voltage down to ±1V by altering the attenuator ratios. Note, however, that precautions must be taken if the attenuator ratio from the output of A3 back to the second AD834 (A2) is lowered. First, the HF compensation limit of the AD840 may be exceeded if the negative feedback factor is too high. Second, if the attenuated output at the AD834 exceeds its clipping level of ±1.3V, feedback control will be lost and the output will suddenly jump to the supply rails. However, with these limitations understood, it will be possible to adapt the circuit to smaller full scale inputs and/or outputs, and for use with lower supply voltages.

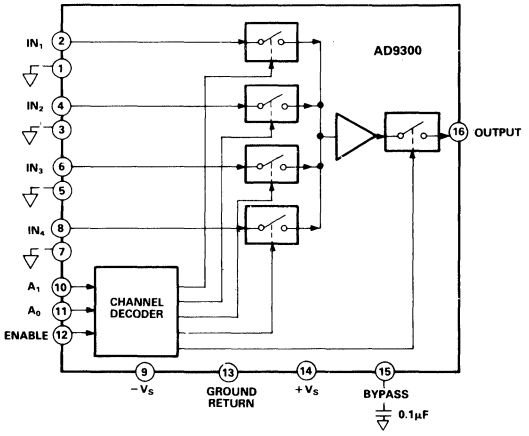
4 × 1 Wideband Video Multiplexer

AD9300

FEATURES
34MHz Full Power Bandwidth
±0.1dB Gain Flatness to 8MHz
72dB Crosstalk Rejection @ 10MHz
0.03°/0.01% Differential Phase/Gain
Cascadable for Switch Matrices
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Video Routing
Medical Imaging
Electro-Optics
ECM Systems
Radar Systems
Data Acquisition

FUNCTIONAL BLOCK DIAGRAM
(Based on Cerdip)



GENERAL DESCRIPTION

The AD9300 is a monolithic high-speed video signal multiplexer useable in a wide variety of applications.

Its four channels of video input signals can be randomly switched at megahertz rates to the single output. In addition, multiple devices can be configured in either parallel or cascade arrangements to form switch matrices. This flexibility in using the AD9300 is possible because the output of the device is in a high-impedance state when the chip is not enabled; when the chip is enabled, the unit acts as a buffer with a high input impedance and low output impedance.

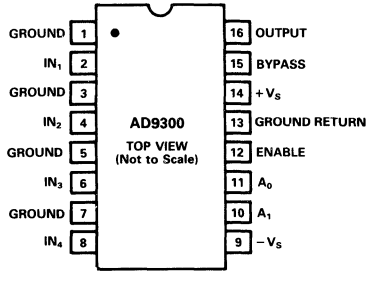
An advanced bipolar process provides fast, wideband switching capabilities while maintaining crosstalk rejection of 72dB at 10MHz. Full power bandwidth is a minimum 27MHz. The device can be operated from ±10V to ±15V power supplies.

The AD9300K is available in a 16-pin ceramic DIP and a 20-pin PLCC and is designed to operate over the commercial temperature range of 0 to +70°C. The AD9300TQ is a hermetic 16-pin ceramic DIP for military temperature range (−55°C to +125°C) applications. This part is also available processed to MIL-STD-883. The AD9300 is available in a 20-pin LCC as the model AD9300TE, which operates over a temperature range of −55°C to +125°C.

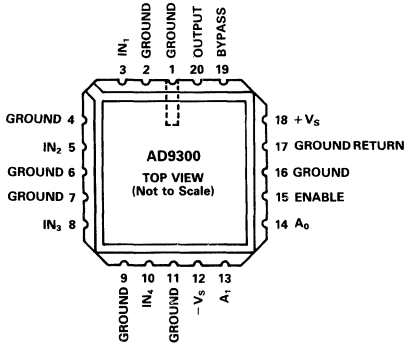
The AD9300 Video Multiplexer is available in versions compliant with MIL-STD-883. Refer to the Analog Devices *Military Products Databook* or current AD9300/883B data sheet for detailed specifications.

PIN DESIGNATIONS

DIP



LCC and PLCC



(PLCC PINOUTS SAME AS LCC)

AD9300—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($\pm V_S = \pm 12V \pm 5\%$; $C_L = 10pF$; $R_L = 2k\Omega$, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	COMMERCIAL 0°C to +70°C AD9300KQ/KP Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Input Offset Voltage	+25°C	I		3	10	mV
Input Offset Voltage	Full	VI			14	mV
Input Offset Voltage Drift[2]	Full	V		75		μV/°C
Input Bias Current	+25°C	I		15	37	μA
Input Bias Current	Full	VI			55	μA
Input Resistance	+25°C	V		3.0		MΩ
Input Capacitance	+25°C	V		2		pF
Input Noise Voltage (dc to 8MHz)	+25°C	V		16		μV rms
TRANSFER CHARACTERISTICS						
Voltage Gain[3]	+25°C	I	0.990	0.994		V/V
Voltage Gain[3]	Full	VI	0.985			V/V
DC Linearity[4]	+25°C	V		0.01		%
Gain Tolerance ($V_{IN} = \pm 1V$)						
dc to 5MHz	+25°C	I		0.05	0.1	dB
5MHz to 8MHz	+25°C	I		0.1	0.3	dB
Small-Signal Bandwidth (V_{IN} = 100mV p-p)	+25°C	V		350		MHz
Full Power Bandwidth[5] (V_{IN} = 2V p-p)	+25°C	I	27	34		MHz
Output Swing	Full	VI	±2			V
Output Current (Sinking @ = 25°C)	+25°C	V		5		mA
Output Resistance	+25°C	IV, V		9	15	Ω
DYNAMIC CHARACTERISTICS						
Slew Rate[6]	+25°C	I	170	215		V/μs
Settling Time (to 0.1% on ±2V Output)	+25°C	IV		70	100	ns
Overshoot						
To T-Step[7]	+25°C	V		<0.1		%
To Pulse[8]	+25°C	V		<10		%
Differential Phase[9]	+25°C	IV		0.03	0.1	°
Differential Gain[9]	+25°C	IV		0.01	0.1	%
Crosstalk Rejection						
Three Channels[10]	+25°C	IV	68	72		dB
One Channel[11]	+25°C	IV	70	76		dB
SWITCHING CHARACTERISTICS[12]						
A_X Input to Channel HIGH Time[13] (t_{HIGH})	+25°C	I		40	50	ns
A_X Input to Channel LOW Time[14] (t_{LOW})	+25°C	I		35	45	ns
Enable to Channel ON Time[15] (t_{ON})	+25°C	I		35	45	ns
Enable to Channel OFF Time[16] (t_{OFF})	+25°C	I		35	45	ns
Switching Transient[17]	+25°C	V		60		mV

EXPLANATION OF TEST LEVELS

Test Level I – 100% production tested.
Test Level II – 100% production tested at + 25°C, and sample tested at specified temperatures.
Test Level III – Sample tested only.
Test Level IV – Parameter is guaranteed by design and characterization testing.
Test Level V – Parameter is a typical value only.
Test Level VI – All devices are 100% production tested at + 25°C. 100% production tested at temperature extremes for military temperature devices; sample tested at temperature extremes for commercial/industrial devices.

Parameter (Conditions)	Temp	Test Level	COMMERCIAL 0°C to +70°C AD9300KQ/KP Min	Typ	Max	Units
DIGITAL INPUTS						
Logic "1" Voltage	Full	VI	2			V
Logic "0" Voltage	Full	VI			0.8	V
Logic "1" Current	Full	VI			5	μA
Logic "0" Current	Full	VI			1	μA
POWER SUPPLY						
Positive Supply Current (+12V)	+25°C	I		13	16	mA
Positive Supply Current (+12V)	Full	VI		13	16	mA
Negative Supply Current (−12V)	+25°C	I		12.5	15	mA
Negative Supply Current (−12V)	Full	VI		12.5	16	mA
Power Supply Rejection Ratio ($\pm V_S = \pm 12V \pm 5\%$)	Full	VI	67	75		dB
Power Dissipation (±12V)[18]	+25°C	V		306		mW

NOTES
[1]Permanent damage may occur if any one absolute maximum rating is exceeded. Functional operation is not implied, and device reliability may be impaired by exposure to higher-than-recommended voltages for extended periods of time.
[2]Measured at extremes of temperature range.
[3]Measured as slope of V_{OUT} versus V_{IN} with $V_{IN} = \pm 1V$.
[4]Measured as worst deviation from end-point fit with $V_{IN} = \pm 1V$.
[5]Full Power Bandwith (FPBW) based on Slew Rate (SR). FPBW = $SR/2\pi V_{PEAK}$
[6]Measured between 20% and 80% transition points of ±1V output.
[7]T-Step = Sin^2X Step, when Step between 0V and +700mV points has 10%-to-90% risetime = 125ns.
[8]Measured with a pulse input having slew rate >250V/μs.
[9]Measured at output between 0.28Vdc and 1.0Vdc with V_{IN} = 284mV p–p at 3.58MHz and 4.43MHz.
[10]This specification is critically dependent on circuit layout. Value shown is measured with selected channel grounded and 10MHz 2V p–p signal applied to remaining three channels. If selected channel is grounded through 75Ω, value is approximately 6dB higher.
[11]This specification is critically dependent on circuit layout. Value shown is measured with selected channel grounded and 10MHz 2V p–p signal applied to one other channel. If selected channel is grounded through 75Ω, value is approximately 6dB higher. Minimum specification in ( ) applies to DIPs.
[12]Consult system timing diagram.
[13]Measured from address change to 90% point of −2V to +2V output LOW-to-HIGH transition.
[14]Measured from address change to 90% point of +2V to −2V output HIGH-to-LOW transition.
[15]Measured from 50% transition point of ENABLE input to 90% transition of 0V to −2V and 0V to +2V output.
[16]Measured from 50% transition point of ENABLE input to 10% transition of +2V to 0V and −2V to 0V output.
[17]Measured while switching between two grounded channels.
[18]Maximum power dissipation is a package-dependent parameter related to the following typical thermal impedances:
16-Pin Ceramic θ_{JA} = 87°C/W; θ_{JC} = 25°C/W
20-Pin LCC θ_{JA} = 74°C/W; θ_{JC} = 10°C/W
20-Pin PLCC θ_{JA} = 71°C/W; θ_{JC} = 26°C/W

Specifications subject to change without notice.

8

ABSOLUTE MAXIMUM RATINGS[1]

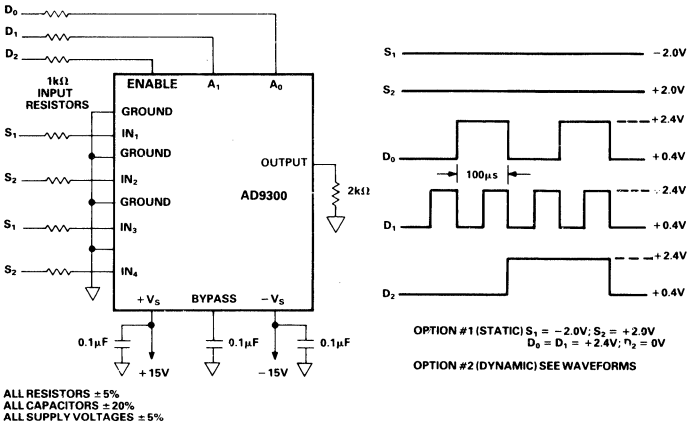
Supply Voltages ($\pm V_S$) . . . . . ±16V
Analog Input Voltage Each Input (IN_1 thru IN_4) . . . . . ±3.5V
Differential Voltage Between Any Two Inputs (IN_1 thru IN_4) 5V
Digital Input Voltages (A_0, A_1, ENABLE) . −0.5V to +5.5V
Output Current
Sinking 6.0mA
Sourcing 6.0mA
Operating Temperature Range
AD9300KQ/KP . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering (10sec) . . . . . +300°C

ORDERING GUIDE

Device	Temperature Range	Description	Package Option[1]
AD9300KQ	0 to +70°C	16-Pin Cerdip, Commercial	Q-16
AD9300TE/883B[2]	−55°C to +125°C	20-Pin LCC, Military Temperature	E-20A
AD9300TQ/883B[2]	−55°C to +125°C	16-Pin Cerdip, Military Temperature	Q-16
AD9300KP	0 to +70°C	20-Pin PLCC, Commercial	P-20A

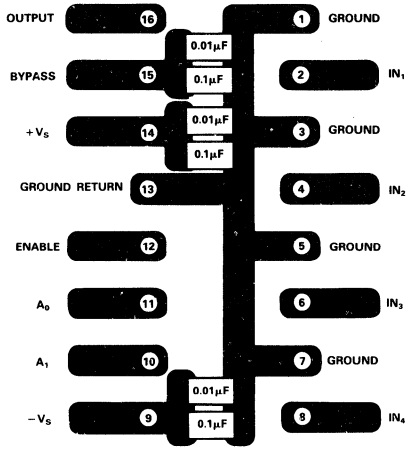
NOTES
[1]E = Ceramic Leadless Chip Carrier; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.
[2]For specifications, refer to Analog Devices *Military Products Databook*.

AD9300 BURN-IN DIAGRAM



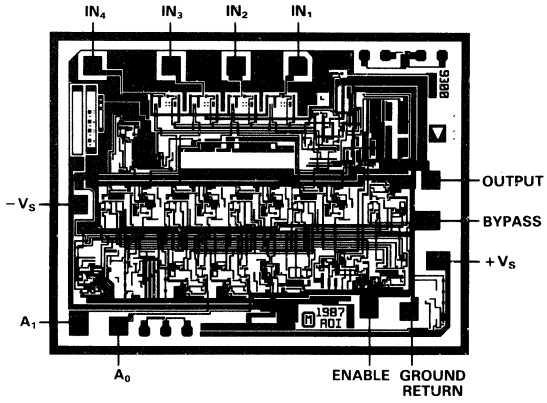
ALL RESISTORS ±5%
ALL CAPACITORS ±20%
ALL SUPPLY VOLTAGES ±5%

SUGGESTED LAYOUT OF AD9300 PC BOARD



Suggested Layout of AD9300 PC Board
(Bottom View – Not to Scale)
Component Side Should be Ground Plane

METALIZATION PHOTOGRAPH



MECHANICAL INFORMATION

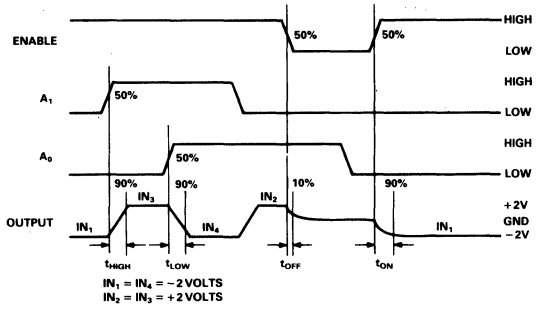
Die Dimensions	84 × 104 × 18 (max) mils
Pad Dimensions	4 × 4 (min) mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil, Aluminum; Ultrasonic Bonding or 1 mil, Gold; Gold Ball Bonding

FUNCTIONAL DESCRIPTION

$IN_1 - IN_4$	Four analog input channels.
GROUND	Analog input shielding grounds, not internally connected. Connect each to external low-impedance ground as close to device as possible.
A_0	One of two TTL decode control lines required for channel selection. See Logic Truth Table.
A_1	One of two TTL decode control lines required for channel selection. See Logic Truth Table.
ENABLE	TTL-compatible chip enable. In enabled mode (logic HIGH), output signal tracks selected input channel; in disabled mode (logic LOW), output is high impedance and no signal appears at output.
$-V_S$	Negative supply voltage; nominally − 10V dc to − 15V dc.
$+V_S$	Positive supply voltage; nominally + 10V dc to + 15V dc.
OUTPUT	Analog output. Tracks selected input channel when enabled.
BYPASS	Bypass terminal for internal bias line; must be decoupled externally to ground through 0.1μF capacitor.
GROUND RETURN	Analog signal and power supply ground return.

LOGIC TRUTH TABLE

ENABLE	A_1	A_0	OUTPUT
0	X	X	High Z
1	0	0	IN_1
1	0	1	IN_2
1	1	0	IN_3
1	1	1	IN_4



AD9300 Timing

THEORY OF OPERATION

Refer to the functional block diagram of the AD9300.

As shown on the drawing, this diagram is based on the pinouts of the DIP packaging of the models AD9300KQ and AD9300TQ. The AD9300KP and AD9300TE are packaged in 20-pin surface mount packages. The extra pins are used for ground connections; the theory of operation remains the same.

The AD9300 Video Multiplexer allows the user to connect any one of four analog input channels (IN_1 – IN_4) to the output of the device, and to switch between channels at megahertz rates.

The input channel which is connected to the output is determined by a 2-bit TTL digital code applied to A_0 and A_1. The selected input will not appear at the output unless a digital "1" is also applied to the ENABLE input pin; unless the output is enabled, it is a high impedance. Necessary combinations to accomplish channel selection are shown in the Logic Truth Table.

Bipolar construction used in the AD9300 insures that the input impedance of the device remains high, and will not vary with power supply voltages. This characteristic makes the AD9300, in effect, a switchable-input buffer. An on-board bias network makes the performance of the AD9300 independent of applied supply voltages, which can have any nominal value from ±10V dc to ±15V dc.

Although the primary application for the AD9300 is the routing of video signals, the harmonic and dynamic attributes of the device make it appropriate for other applications. The AD9300 has exceptional performance when switching video signals, but can also be used for switching other analog signals requiring greater dynamic range and/or precision than those in video.

As shown in Figure 1, Input and Output Equivalent Circuits, each analog input is connected to the base of a bipolar transistor. If Channel 1 is selected, a current switch is closed and routes current through the input transistor for Channel 1.

If Channel 2 is then selected by the digital inputs, the current switch for Channel 1 is opened and the current switch for Channel 2 is closed. This causes current to be routed away from the Channel 1 transistor and into the Channel 2 input transistor. Whenever a channel's input device is carrying current, the analog input applied to that channel is passed to the output stage.

The operation of the output stage is similar to that of the input stages. Whenever the output stage is enabled with a HIGH digital "1" signal at the ENABLE pin, the output transistor will carry current and pass the selected analog input.

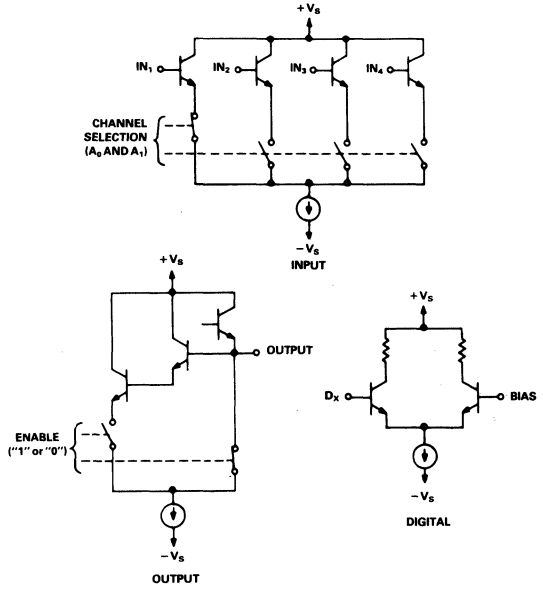


Figure 1. Input and Output Equivalent Circuits

When the output stage is disabled (by virtue of the ENABLE pin being driven LOW with a digital "0"), the output current switch is opened. This routes the current to other circuits within the AD9300 which keep the output transistor biased "off". These circuits require approximately 1μA of bias current from the load connected to the output of the multiplexer. In the absence of a terminating load and the resulting dc bias, the output of the AD9300 "floats" at −2.5V.

In summary, when the AD9300 is enabled by the ENABLE pin being driven HIGH with a digital "1", the selected analog input channel acts as a buffer for the input; and the output of the multiplexer is a low impedance. When the AD9300 is disabled with a digital "0" LOW signal, the selected channel acts as an open switch for the input; and the output of the unit becomes a high impedance. This characteristic allows the user to wire-or several AD9300 Analog Multiplexers together to form switch matrices.

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AD9300 APPLICATIONS

To ensure optimum performance from circuits using the AD9300, it is important to follow a few basic rules which apply to all high-speed devices.

A large, low-impedance ground plane under the AD9300 is critical. Generally, GROUND and GROUND RETURN connections should be connected solidly to this plane. GROUND pin connections are signal isolation grounds which are not connected internally; they can be left unconnected, but there may be some degradation in crosstalk rejection. GROUND RETURN, on the other hand, serves as the internal ground reference for the AD9300 and should be connected to the ground plane *without exception*.

The output stage of the unit is capable of driving a 2kΩ‖10pF load. Larger capacative loads may limit full power bandwidth and increase t_{OFF} (the interval between the 50% point of the ENABLE high-to-low transition and the instant the output becomes a high impedance.)

For applications such as driving cables (See Figure 2), output buffers are recommended.

It is recommended that the AD9300 be soldered directly into circuit boards, rather than using socket assemblies. If sockets must be used, individual pin sockets are the preferred choice, rather than a socket assembly. A second requirement for proper high-speed design involves decoupling the power supply and internal bias supply lines from ground to improve noise immunity. Chip capacitors are recommended for connecting 0.1μF and 0.01μF capacitors between ground and the $\pm V_S$ supplies (Pins 9 and 14), and the BYPASS connection (Pin 15).

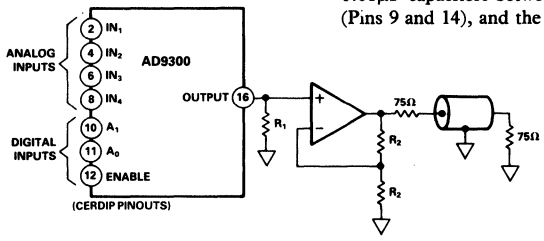


Figure 2. 4×1 AD9300 Multiplexer with Buffered Output Driving 75Ω Coaxial Cable

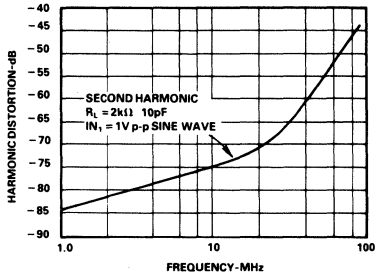


Figure 3. Harmonic Distortion vs. Frequency

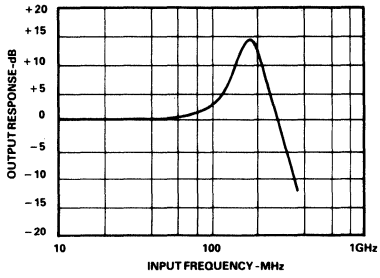


Figure 4. Output vs. Frequency

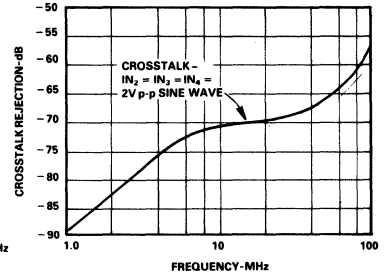


Figure 5. Crosstalk vs. Frequency

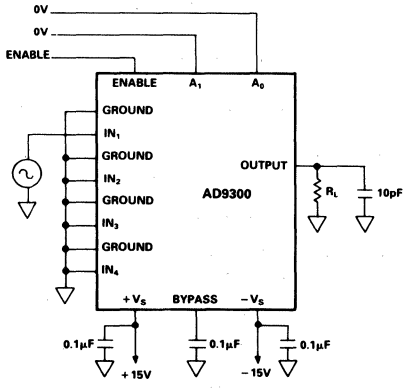


Figure 6. Test Circuit for Harmonic Distortion, Pulse Response, T-Step Response and Disable Characteristics

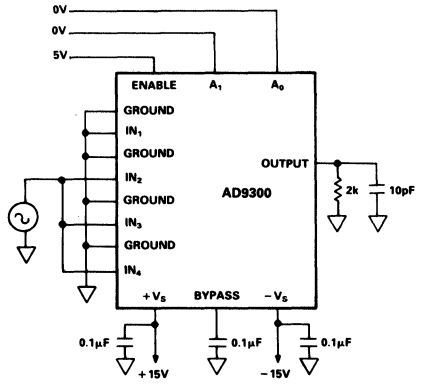


Figure 7. Crosstalk Rejection Test Circuit

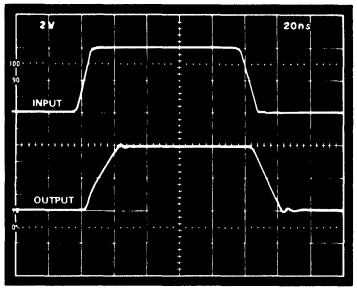


Figure 8. Pulse Response

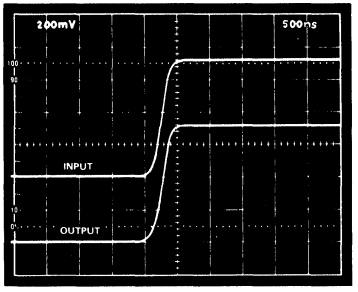


Figure 9. T-Step Response

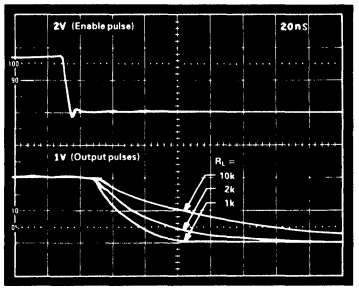
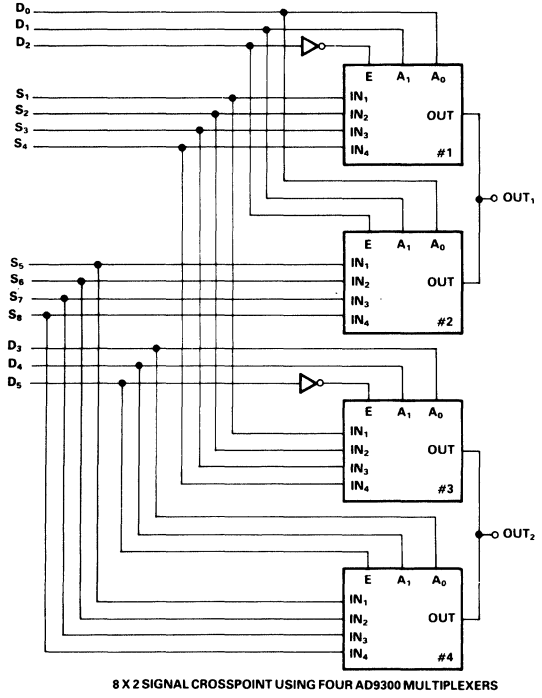


Figure 10. Enable to Channel "Off" Response

CROSSPOINT CIRCUIT APPLICATIONS

Four AD9300 multiplexers can be used to implement an 8 × 2 crosspoint, as shown in Figure 11. The circuit is modular in concept, with each pair of multiplexers (#1 and #2; #3 and #4) forming an 8 × 1 crosspoint. When the inputs to all four units are connected as shown, the result is an 8 × 2 crosspoint circuit.



8 X 2 SIGNAL CROSSPOINT USING FOUR AD9300 MULTIPLEXERS

Figure 11. 8 × 2 Signal Crosspoint Using Four AD9300 Multiplexers

The truth table describes the relationships among the digital inputs (D_0 – D_5) and the analog inputs (S_1 – S_8); and which signal input is selected at the outputs (OUT_1 and OUT_2). The number of crosspoint modules that can be connected in parallel is limited by the drive capabilities of the input signal sources. High input impedance (3MΩ) and low input capacitance (2pF) of the AD9300 help minimize this limitation.

8 × 2 Crosspoint Truth Table

D_2 or D_5	D_1 or D_4	D_0 or D_3	OUT_1 or OUT_2
0	0	0	S_1
0	0	1	S_2
0	1	0	S_3
0	1	1	S_4
1	0	0	S_5
1	0	1	S_6
1	1	0	S_7
1	1	1	S_8

Adding to the number of inputs applied to each crosspoint module is simply a matter of adding AD9300 multiplexers in parallel to the module. Eight devices connected in parallel result in a 32 × 1 crosspoint which can be used with input signals having 30MHz bandwidth and 1V peak-to-peak amplitude. Even more AD9300 units can be added if input signal amplitude and/or bandwidth are reduced; if they are not, distortion of the output signals can result.

When an AD9300 is enabled, its low output impedance causes the "off" isolation of disabled parallel devices to be greater than the crosstalk rejection of a single unit.

Quad 8-Bit Multiplying CMOS D/A Converter with Memory

DAC-8408

FEATURES

- Four DACs in a 28 Pin, 0.6 Inch Wide DIP or 28 Pin JEDEC Plastic Chip Carrier
- ±1/4 LSB End-Point Linearity
- Guaranteed Monotonic
- DACs Matched to Within 1%
- Microprocessor Compatible
- Read/Write Capability (with Memory)
- TTL/CMOS Compatible
- Four-Quadrant Multiplication
- Single-Supply Operation (+5V)
- Low Power Consumption
- Latch-Up Resistant
- Available In Die Form

ORDERING INFORMATION †

		PACKAGE		
		COMMERCIAL TEMPERATURE	EXTENDED INDUSTRIAL TEMPERATURE	MILITARY* TEMPERATURE
INL	DNL	0°C to +70°C	–40°C to +85°C	–55°C to +125°C
±1/4LSB	±1/2LSB	DAC8408GP	DAC8408ET	DAC8408AT
±1/2LSB	±1LSB	–	DAC8408FT	DAC8408BT
±1/2LSB	±1LSB	–	DAC8408FPC††	–
±1/2LSB	±1LSB	–	DAC8408FS	–
±1/2LSB	±1LSB	–	DAC8408FP	–

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

APPLICATIONS

- Voltage Set Points in Automatic Test Equipment
- Systems Requiring Data Access for Self-Diagnostics
- Industrial Automation
- Multi-Channel Microprocessor-Controlled Systems
- Digitally Controlled Op Amp Offset Adjustment
- Process Control
- Digital Attenuators

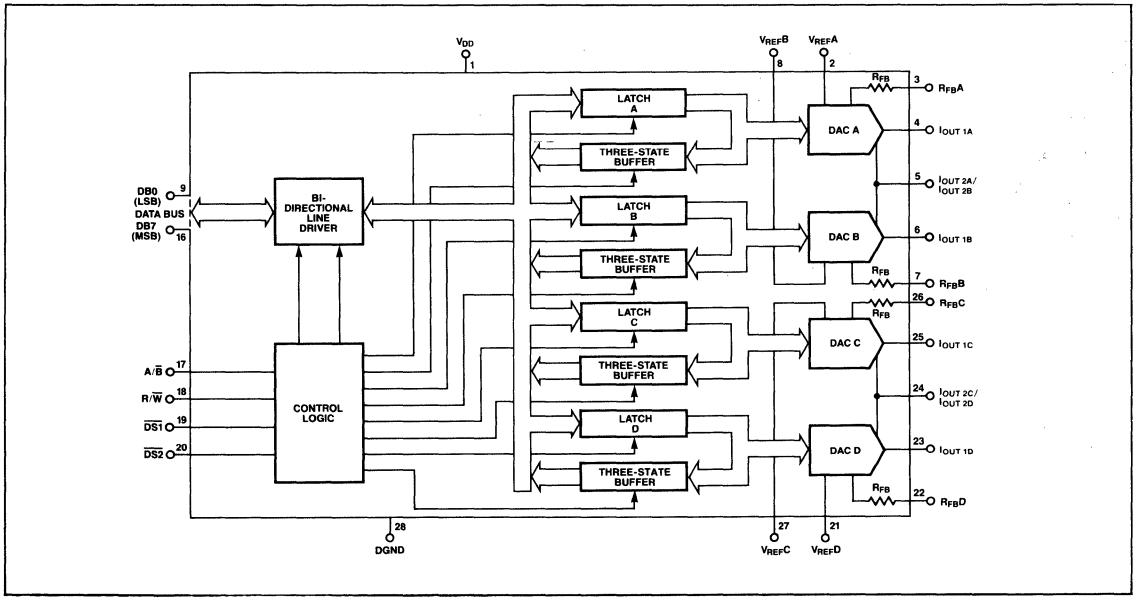
GENERAL DESCRIPTION

The DAC-8408 is a monolithic quad 8-bit multiplying digital-to-analog CMOS converter. Each DAC has its own reference input, feedback resistor, and on-board data latches that feature read/write capability. The readback function serves as memory for those systems requiring self-diagnostics.

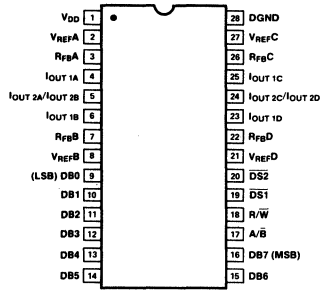
A common 8-bit TTL/CMOS compatible input port is used to load data into any of the four DAC data-latches. Control lines $\overline{DS1}$, $\overline{DS2}$, and A/$\overline{B}$ determine which DAC will accept data. Data loading is similar to that of a RAM's write cycle. Data can be read back onto the same data bus with control line R/$\overline{W}$. The DAC-8408 is bus compatible with most 8-bit microprocessors, including the 6800, 8080, 8085, and Z80. The DAC-8408 operates on a single +5 volt supply and dissipates less than 20mW. The DAC-8408 is manufactured using PMI's highly stable, thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS process. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

8

FUNCTIONAL DIAGRAM



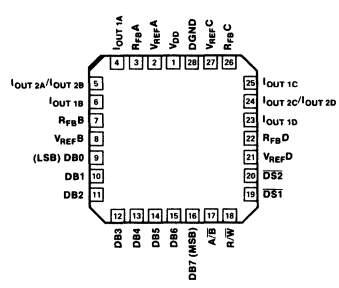
PIN CONNECTIONS



28-PIN
HERMETIC DIP
(T-Suffix)

28-PIN
EPOXY DIP
(P-Suffix)

28-PIN SOL
(S-Suffix)



28-PIN
PLASTIC LEADED
CHIP CARRIER
(PC-Suffix)

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

V_{DD} to $I_{OUT\ 2A}$, $I_{OUT\ 2B}$, $I_{OUT\ 2C}$, $I_{OUT\ 2D}$ ..... 0, +7V
V_{DD} to DGND ..... 0, +7V
$I_{OUT\ 1A}$, $I_{OUT\ 1B}$,
$I_{OUT\ 1C}$, $I_{OUT\ 1D}$ to DGND ..... –0.3V to V_{DD} + 0.3V
$R_{FB}A$, $R_{FB}B$, $R_{FB}C$, $R_{FB}D$ to I_{OUT} ..... ±25V
$I_{OUT\ 2A}$, $I_{OUT\ 2B}$,
$I_{OUT\ 2C}$, $I_{OUT\ 2D}$ to DGND .....–0.3V to V_{DD} + 0.3V
DB0 through DB7 to DGND .....–0.3V to V_{DD} + 0.3V
Control Logic
Input Voltage to DGND ..... –0.3V + V_{DD} + 0.3V
$V_{REF}A$, $V_{REF}B$, $V_{REF}C$, $V_{REF}D$ to
$I_{OUT\ 2A}$, $I_{OUT\ 2B}$, $I_{OUT\ 2C}$, $I_{OUT\ 2D}$ ..... ±25V
Operating Temperature Range
Commercial Grade (GP) ..... 0°C to +70°C
Industrial Grade (ET, FT, FP, FPC, FS) ..... –40°C to +85°C
Military Grade (AT, BT) ..... –55°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
28-Pin Hermetic DIP (T)	55	10	°C/W
28-Pin Plastic DIP (P)	53	27	°C/W
28-Pin SOL (S)	68	23	°C/W
28-Contact PLCC (PC)	66	29	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL and PLCC packages.

CAUTION:
1. Do not apply voltages higher than V_{DD} + 0.3V or less than –0.3V potential on any terminal except V_{REF} and R_{FB}.
2. The digital control inputs are diode-protected; however, permanent damage may occur on unconnected inputs from high-energy electrostatic fields. Keep in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = ±10V; V_{OUT}A, B, C, D = 0V; T_A = –55°C to +125°C apply for DAC-8408AT/BT, T_A = –40°C to +85°C apply for DAC-8408ET/FT/FP/FPC/FS; T_A = 0°C to +70°C apply for DAC-8408GP, unless otherwise noted. Specifications apply for DAC A, B, C, & D.

PARAMETER	SYMBOL	CONDITIONS	DAC-8408 MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution	N		8	—	—	Bits
Nonlinearity (Notes 1, 2)	INL	DAC-8408A/E/G	—	—	±1/4	LSB
		DAC-8408B/F/H	—	—	±1/2	
Differential Nonlinearity	DNL	DAC-8408A/E/G	—	—	±1/2	LSB
		DAC-8408B/F/H	—	—	±1	
Gain Error	G_{FSE}	(Using Internal R_{FB})	—	—	±1	LSB
Gain Tempco (Notes 3, 6)	TC_{GFS}		—	±2	±40	ppm/°C
Power Supply Rejection (ΔV_{DD} = ±10%)	PSR		—	—	0.001	%FSR/%
$I_{OUT\ 1A, B, C, D}$ Leakage Current (Note 13)	I_{LKG}	T_A = +25°C	—	—	±30	nA
		T_A = Full Temp. Range	—	—	±100	

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = ±10V; V_{OUT}A, B, C, D = 0V; T_A = –55°C to +125°C apply for DAC-8408AT/BT, T_A = –40°C to +85°C apply for DAC-8408ET/FT/FP/FPC/FS; T_A = 0°C to +70°C apply for DAC-8408GP, unless otherwise noted. Specifications apply for DAC A, B, C, & D. *Continued*

PARAMETER	SYMBOL	CONDITIONS	DAC-8408 MIN	TYP	MAX	UNITS
REFERENCE INPUT						
Input Voltage Range			—	—	±20	V
Input Resistance Match (Note 4)		$R_{A, B, C, D}$	—	—	±1	%
Input Resistance	R_{IN}		6	10	14	kΩ
DIGITAL INPUTS						
Digital Input Low	V_{IL}		—	—	0.8	V
Digital Input High	V_{IH}		2.4	—	—	V
Input Current (Note 5)	I_{IN}	T_A = +25°C T_A = Full Temp. Range	— —	±0.01 —	±1.0 ±10.0	μA
Input Capacitance (Note 6)	C_{IN}		—	—	8	pF
DATA BUS OUTPUTS						
Digital Output Low	V_{OL}	1.6mA Sink	—	—	0.4	V
Digital Output High	V_{OH}	400μA Source	4	—	—	V
Output Leakage Current	I_{LKG}	T_A = +25°C T_A = Full Temp. Range	— —	±0.005 ±0.075	±1.0 ±10.0	μA
DAC OUTPUTS (Note 6)						
Propagation Delay (Note 7)	t_{pD}		—	150	180	ns
Settling Time (Notes 11, 12)	t_s		—	190	250	ns
Output Capacitance	C_{OUT}	DAC Latches All "0's" DAC Latches All "1's"	— —	— —	30 50	pF
AC Feedthrough	FT	($20V_{p-p}$ @ F = 100kHz)	54	—	—	dB
SWITCHING CHARACTERISTICS (Notes 6, 10)						
Write to Data Strobe Time	t_{DS1} or t_{DS2}	T_A = +25°C T_A = Full Temp. Range	90 145	— —	— —	ns
Data Valid to Strobe Set-Up Time	t_{DSU}	T_A = +25°C T_A = Full Temp. Range	150 175	— —	— —	ns
Data Valid to Strobe Hold Time	t_{DH}		10	—	—	ns
DAC Select to Strobe Set-Up Time	t_{AS}		0	—	—	ns
DAC Select to Strobe Hold Time	t_{AH}		0	—	—	ns
Write Select to Strobe Set-Up Time	t_{WSU}		0	—	—	ns
Write Select to Strobe Hold Time	t_{WH}		0	—	—	ns

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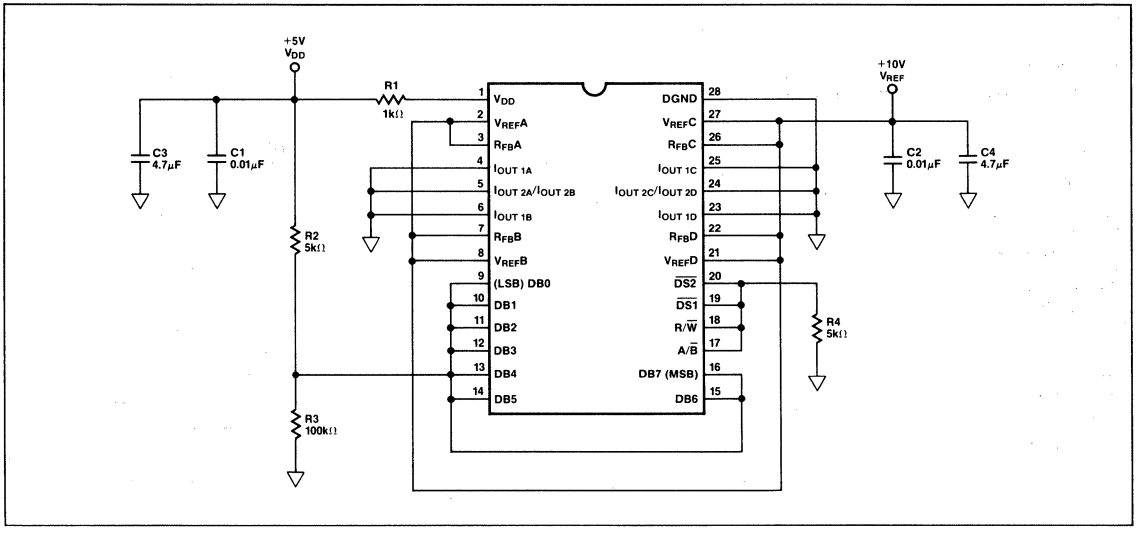
ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = ±10V; V_{OUT}A, B, C, D = 0V; T_A = –55°C to +125°C apply for DAC-8408AT/BT, T_A = –40°C to +85°C apply for DAC-8408ET/FT/FP/FPC/FS; T_A = 0°C to +70°C apply for DAC-8408GP, unless otherwise noted. Specifications apply for DAC A, B, C, & D. *Continued*

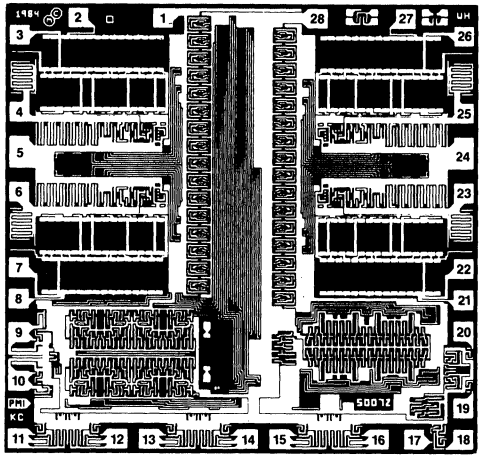
PARAMETER	SYMBOL	CONDITIONS	DAC-8408 MIN	TYP	MAX	UNITS
Read to Data Strobe Width	t_{RDS}	T_A = +25°C	220	—	—	ns
		T_A = Full Temp. Range	350	—	—	
Data Strobe to Output Valid Time	t_{CO}	T_A = +25°C	320	—	—	ns
		T_A = Full Temp. Range	430	—	—	
Output Data to Deselect Time	t_{OTD}	T_A = +25°C	200	—	—	ns
		T_A = Full Temp. Range	270	—	—	
Read Select to Strobe Set-Up Time	t_{RSU}		0	—	—	ns
Read Select to Strobe Hold Time	t_{RH}		0	—	—	ns
POWER SUPPLY						
Voltage Range	V_{DD}		4.5	—	5.5	V
Supply Current (Note 8)	I_{DD}		—	—	50	µA
Supply Current (Note 9)	I_{DD}	T_A = +25°C	—	—	1.0	mA
		T_A = Full Temp. Range	—	—	1.5	

NOTES:
1. This is an end-point linearity specification.
2. Guaranteed to be monotonic over the full operating temperature range.
3. ppm/°C of FSR (FSR = Full Scale Range = V_{REF} – 1 LSB.)
4. Input Resistance Temperature Coefficient = +300ppm/°C.
5. Logic Inputs are MOS gates. Typical input current at +25°C is less than 10nA.
6. Guaranteed by design.
7. From Digital Input to 90% of final analog output current.
8. All Digital Inputs "0" or V_{DD}.
9. All Digital Inputs V_{IH} or V_{IL}.
10. See Timing Diagram.
11. Digital Inputs = 0V to V_{DD} or V_{DD} to 0V.
12. Extrapolated: t_s (1/2 LSB) = t_{PD} + 6.2τ where τ = the measured first time constant of the final RC decay.
13. All Digital Inputs = 0V; V_{REF} = +10V.

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.130 × 0.124 inch, 16,120 sq. mils
(3.30 × 3.15 mm, 10.4 sq. mm)

1. V_{DD}
2. $V_{REF}A$
3. $R_{FB}A$
4. $I_{OUT\ 1A}$
5. $I_{OUT\ 2A}/I_{OUT\ 2B}$
6. $I_{OUT\ 1B}$
7. $R_{FB}B$
8. $V_{REF}B$
9. DB0 (LSB)
10. DB1
11. DB2
12. DB3
13. DB4
14. DB5
15. DB6
16. DB7 (MSB)
17. $A/\overline{B}$
18. $R/\overline{W}$
19. $\overline{DS1}$
20. $\overline{DS2}$
21. $V_{REF}D$
22. $R_{FB}D$
23. $I_{OUT\ 1D}$
24. $I_{OUT\ 2C}/I_{OUT\ 2D}$
25. $I_{OUT\ 1C}$
26. $R_{FB}C$
27. $V_{REF}C$
28. DGND

WAFER TEST LIMITS at $V_{DD} = +5V$; $V_{REF} = \pm 10V$; $V_{OUT}A, B, C, D = 0V$; $T_A = +25°C$, unless otherwise noted. Specifications apply for DAC A, B, C, & D.

PARAMETER	SYMBOL	CONDITIONS	DAC-8408G LIMITS	UNITS
STATIC ACCURACY				
Resolution	N		8	Bits MIN
Nonlinearity (Note 1)	INL		±1/2	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Gain Error	G_{FSE}	Using Internal R_{FB}	±1	LSB MAX
Power Supply Rejection ($\Delta V_{DD} = \pm 10\%$) (Note 2)	PSR	Using Internal R_{FB}	0.001	%FSR/% MAX
$I_{OUT\ 1A, B, C, D}$ Leakage Current	I_{LKG}	All Digital Inputs = 0V $V_{REF} = +10V$	±30	nA MAX
REFERENCE INPUT				
Reference Input Resistance (Note 3)	R_{IN}		6/14	kΩ MIN/MAX
Input Resistance Match	R_{IN}		±1	% MAX
DIGITAL INPUTS				
Digital Input Low	V_{IL}		0.8	V MAX
Digital Input High	V_{IH}		2.4	V MIN
Input Current (Note 4)	I_{IN}		±1.0	μA MAX

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WAFER TEST LIMITS at V_{DD} = +5V; V_{REF} = ±10V; V_{OUT}A, B, C, D = 0V; T_A = +25°C, unless otherwise noted. Specifications apply for DAC A, B, C, & D. (Continued)

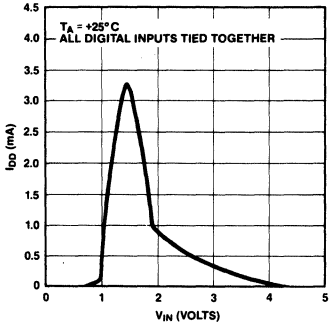
PARAMETER	SYMBOL	CONDITIONS	DAC-8408G LIMITS	UNITS
DATA BUS OUTPUTS				
Digital Output Low	V_{OL}	1.6mA Sink	0.4	V MAX
Digital Output High	V_{OH}	400μA Source	4	V MIN
Output Leakage Current	I_{LKG}		±1.0	μA MAX
POWER SUPPLY				
Supply Current (Note 5)	I_{DD}		50	μA MAX
Supply Current (Note 6)	I_{DD}		1.0	mA MAX

NOTES:
1. This is an endpoint linearity specification.
2. FSR is Full Scale Range = V_{REF} − 1 LSB.
3. Input Resistance Temperature Coefficient approximately equals +300ppm/°C.
4. Logic inputs are MOS gates. Typical input current at +25°C is less than 10nA.
5. All Digital Inputs are either "0" or V_{DD}.
6. All Digital Inputs are either V_{IH} or V_{IL}.

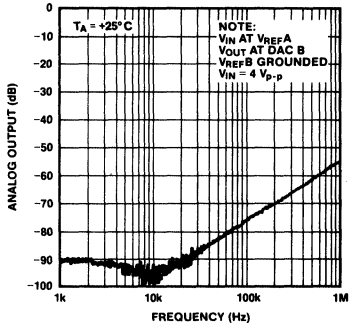
Electrical tests are performed at wafer probe to the limits shown, Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

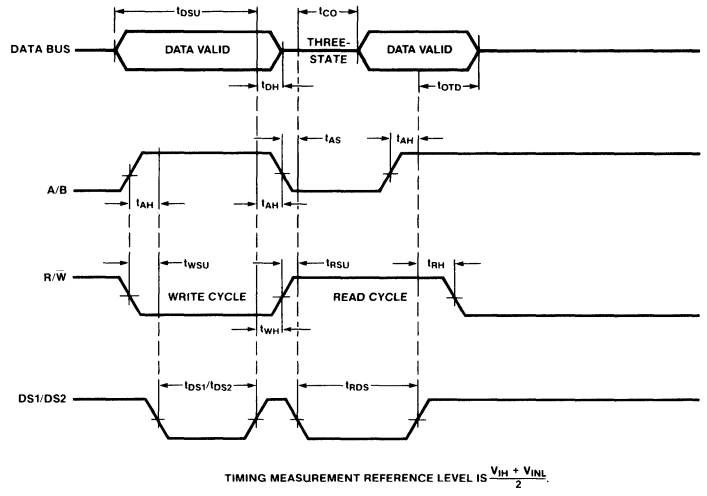
SUPPLY CURRENT vs LOGIC LEVEL



ANALOG CROSSTALK vs FREQUENCY



TIMING DIAGRAM



PARAMETER DEFINITIONS

RESOLUTION
Resolution is the number of states (2^n) that the full-scale range (FSR) of a DAC is divided (or resolved) into.

NONLINEARITY
Nonlinearity (Relative Accuracy) is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for ideal zero and full-scale and is expressed in LSB, %, or ppm of full-scale range.

DIFFERENTIAL NONLINEARITY
Differential Nonlinearity is the worst case deviation of any adjacent analog outputs from the ideal 1LSB step size. A specified differential nonlinearity of ±1 LSB maximum over the operating temperature range ensures monotonicity.

GAIN ERROR
Gain Error (full-scale error) is a measure of the output error between the ideal and actual DAC output. The ideal full-scale output is V_{REF} – 1 LSB.

OUTPUT CAPACITANCE
Output Capacitance is that capacitance between $I_{OUT\ 1A}$, $I_{OUT\ 1B}$, $I_{OUT\ 1C}$, or $I_{OUT\ 1D}$ and AGND.

AC FEEDTHROUGH ERROR
This is the error caused by capacitance coupling from V_{REF} to the DAC output with all switches off.

SETTLING TIME
Settling Time is the time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input signal.

PROPAGATION DELAY
This is a measure of the internal delays of the DAC. It is defined as the time from a digital input change to the analog output-current reaching 90% of its final value.

CHANNEL-TO-CHANNEL ISOLATION
This is the portion of input signal that appears at the output of a DAC from another DAC's reference input. It is expressed as a ratio in dB.

DIGITAL CROSSTALK
Digital Crosstalk is the glitch energy transferred to the output of one DAC due to a change in digital input code from other DACs. It is specified in nVs.

CIRCUIT INFORMATION

The DAC-8408 combines four identical 8-bit CMOS DACs onto a single monolithic chip. Each DAC has its own reference input, feedback resistor, and on-board data latches. It also features a read/write function that serves as an accessible memory location for digital-input data words. The DAC's three-state readback drivers place the data word back onto the data bus.

D/A CONVERTER SECTION

Each DAC contains a highly stable, silicon-chromium, thin-film, R-2R resistor ladder network and eight pairs of current steering switches. These switches are in series with each ladder resistor and are single-pole, double-throw NMOS transistors; the gates of these transistors are controlled by CMOS inverters. Figure 1 shows a simplified circuit of the R-2R resistor ladder section, and Figure 2 shows an approximate equivalent switch circuit. The current through each resistor leg is switched between $I_{OUT\,1}$ and $I_{OUT\,2}$. This maintains a constant current in each leg, regardless of the digital input logic states.

Each transistor switch has a finite "ON" resistance that can introduce errors to the DAC's specified performance. These resistances must be accounted for by making the voltage drop across each transistor equal to each other. This is done by binarily-scaling the transistor's "ON" resistance from the most significant bit (MSB) to the least significant bit (LSB). With 10 volts applied at the reference input, the current through the MSB switch is 0.5mA, the next bit is 0.25mA, etc.; this maintains a constant 10mV drop across each switch and the converter's accuracy is maintained. It also results in a constant resistance appearing at the DAC's reference input terminal; this allows the DAC to be driven by a voltage or current source, AC or DC of positive or negative polarity.

Shown in Figure 3 is an equivalent output circuit for DAC A. The circuit is shown with all digital inputs high. The leakage current source is the combination of surface and junction leakages to the substrate. The 1/256 current source represents the constant 1-bit current drain through the ladder terminating resistor. The situation is reversed with all digital inputs low, as shown in Figure 4. The output capacitance is code dependent, and therefore, is modulated between the low and high values.

FIGURE 1: Simplified D/A Circuit of DAC-8408

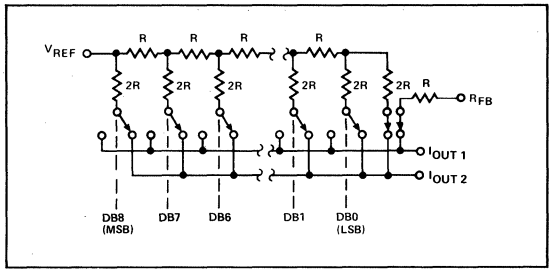


FIGURE 2: N-Channel Current Steering Switch

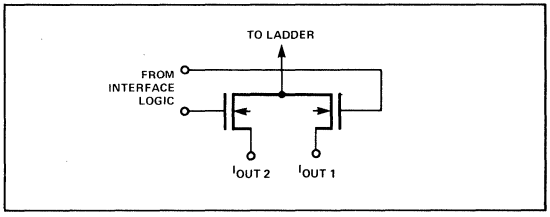


FIGURE 3: Equivalent DAC Circuit (All digital inputs HIGH)

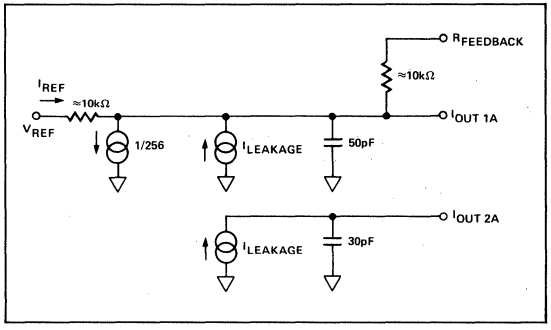
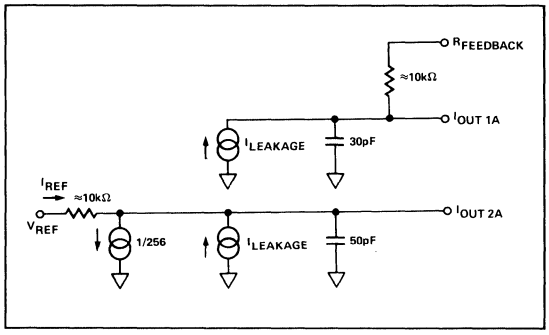


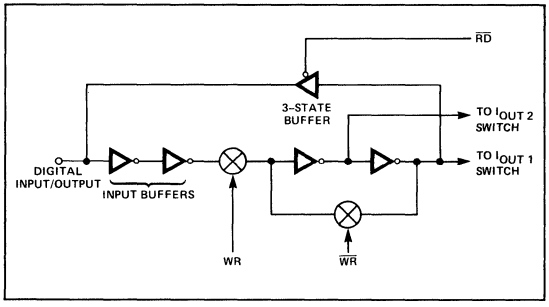
FIGURE 4: Equivalent DAC Circuit (All digital inputs LOW)



DIGITAL SECTION

Figure 5 shows the digital input/output structure for one bit. The digital WR, $\overline{WR}$, and $\overline{RD}$ controls shown in the figure are internally generated from the external A/$\overline{B}$, R/$\overline{W}$, $\overline{DS1}$, and $\overline{DS2}$ signals. The combination of these signals decide which DAC is selected. The digital inputs are CMOS inverters, designed such that TTL input levels (2.4V and 0.8V) are converted into CMOS logic levels. When the digital input is in the region of 1.2 to 1.8V, the input stages operate in their linear region and draw current from the +5V supply (see Typical Supply Current vs Logic Level curve on page 6). It is recommended that the digital input voltages be as close to V_{DD} and DGND as is practical in order to minimize supply currents. This allows maximum savings in power dissipation inherent with CMOS devices. The three-state readback digital output drivers (in the active mode) provide TTL-compatible digital outputs with a fan-out of one TTL load. The three-state digital readback leakage-current is typically 5nA.

FIGURE 5: Digital Input/Output Structure



INTERFACE LOGIC SECTION

DAC Operating Modes

- All DACs in HOLD MODE.
- DAC A, B, C, or D individually selected (WRITE MODE).
- DAC A, B, C, or D individually selected (READ MODE).
- DACs A and C simultaneously selected (WRITE MODE).
- DACs B and D simultaneously selected (WRITE MODE).

DAC Selection: Control inputs, $\overline{DS1}$, $\overline{DS2}$, and A/$\overline{B}$ select which DAC can accept data from the input port (see Mode Selection Table).

Mode Selection: Control inputs $\overline{DS}$ and R/$\overline{W}$ control the operating mode of the selected DAC.

Write Mode: When the control inputs $\overline{DS}$ and R/$\overline{W}$ are both low, the selected DAC is in the write mode. The input data latches of the selected DAC are transparent, and its analog output responds to activity on the data inputs DB0—DB7.

Hold Mode: The selected DAC latch retains the data that was present on the bus line just prior to $\overline{DS}$ or R/$\overline{W}$ going to a high state. All analog outputs remain at the values corresponding to the data in their respective latches.

Read Mode: When $\overline{DS}$ is low and R/$\overline{W}$ is high, the selected DAC is in the read mode, and the data held in the appropriate latch is put back onto the data bus.

MODE SELECTION TABLE

CONTROL LOGIC					
DS1	DS2	A/$\overline{B}$	R/$\overline{W}$	MODE	DAC
L	H	H	L	WRITE	A
L	H	L	L	WRITE	B
H	L	H	L	WRITE	C
H	L	L	L	WRITE	D
L	H	H	H	READ	A
L	H	L	H	READ	B
H	L	H	H	READ	C
H	L	L	H	READ	D
L	L	H	L	WRITE	A&C
L	L	L	L	WRITE	B&D
H	H	X	X	HOLD	A/B/C/D
L	L	H	H	HOLD	A/B/C/D
L	L	L	H	HOLD	A/B/C/D

L = LOW STATE H = HIGH STATE X = IRRELEVANT

8

BASIC APPLICATIONS

Some basic circuit configurations are shown in Figures 6 and 7. Figure 6 shows the DAC-8408 connected in a unipolar configuration (2-Quadrant Multiplication), and Table I shows the Code Table. Resistors R1, R2, R3, and R4 are used to trim full scale output. Full-scale output voltage = $V_{REF} - 1$ LSB = $V_{REF}(1-2^{-8})$ or $V_{REF} \times (255/256)$ with all digital inputs high. Low temperature coefficient (approximately 50ppm/°C) resistors or trimmers should be selected if used. Full scale can also be adjusted using V_{REF} voltage. This will eliminate resistors R1, R2, R3, and R4. In many applications, R1 through R4 are not required, and the maximum gain error will then be that of the DAC.

Each DAC exhibits a variable output resistance that is code-dependent. This produces a code-dependent, differential nonlinearity term at the amplifier's output which can have a maximum value of 0.67 × the amplifier's offset voltage. This differential nonlinearity term adds to the R-2R resistor ladder differential-nonlinearity; the output may no longer be monotonic. To maintain monotonicity and minimize gain and linearity errors, it is recommended that the op amp offset voltage be adjusted to less than 10% of 1 LSB (1 LSB = $2^{-8} \times V_{REF}$ or $1/256 \times V_{REF}$), or less than 3.9mV over the operating temperature range. Zero-scale output voltage (with all digital inputs low) may be adjusted using the op amp offset adjustment. Capacitors C1, C2, C3, and C4 provide phase compensation and help prevent overshoot and ringing when using high speed op amps.

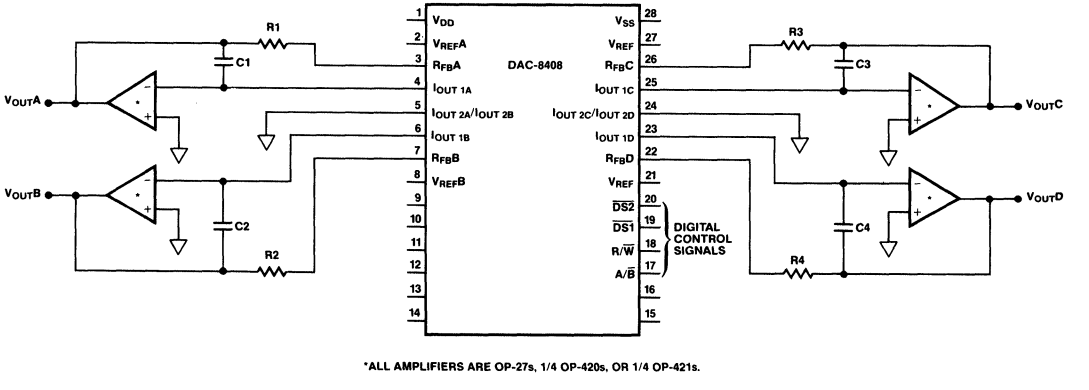
Figure 7 shows the recommended circuit configuration for the bipolar operation (4-quadrant multiplication), and Table II shows the Code Table. Trimmer resistors R17, R18, R19, and R20 are used only if gain error adjustments are required and range between 50 and 1000Ω. Resistors R21, R22, R23, and R24 will range betwen 50 and 500Ω. If these resistors are used, it is essential that resistor pairs R9—R13, R10—R14, R11—R15, R12—R16 are matched both in value and tempco. They should be within 0.01%; wire wound or metal foil types are preferred for best temperature coefficient matching. The circuits of Figure 6 and 7 can either be used as a fixed reference D/A converter, or as an attenuator with an AC input voltage.

TABLE I: Unipolar Binary Code Table (Refer to Figure 6.)

DAC DATA INPUT MSB							LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{255}{256}\right)$
1	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{129}{256}\right)$
1	0	0	0	0	0	0	0	$-V_{REF}\left(\frac{128}{256}\right) = \frac{-V_{IN}}{2}$
0	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{127}{256}\right)$
0	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{1}{256}\right)$
0	0	0	0	0	0	0	0	$-V_{REF}\left(\frac{0}{256}\right) = 0$

NOTE:
1 LSB = $(2^{-8})(V_{REF}) = \frac{1}{256}(V_{REF})$

FIGURE 6: Quad DAC Unipolar Operation (2-Quadrant Multiplication)



*ALL AMPLIFIERS ARE OP-27s, 1/4 OP-420s, OR 1/4 OP-421s.

FIGURE 7: Quad DAC Bipolar Operation (4-Quadrant Multiplication)

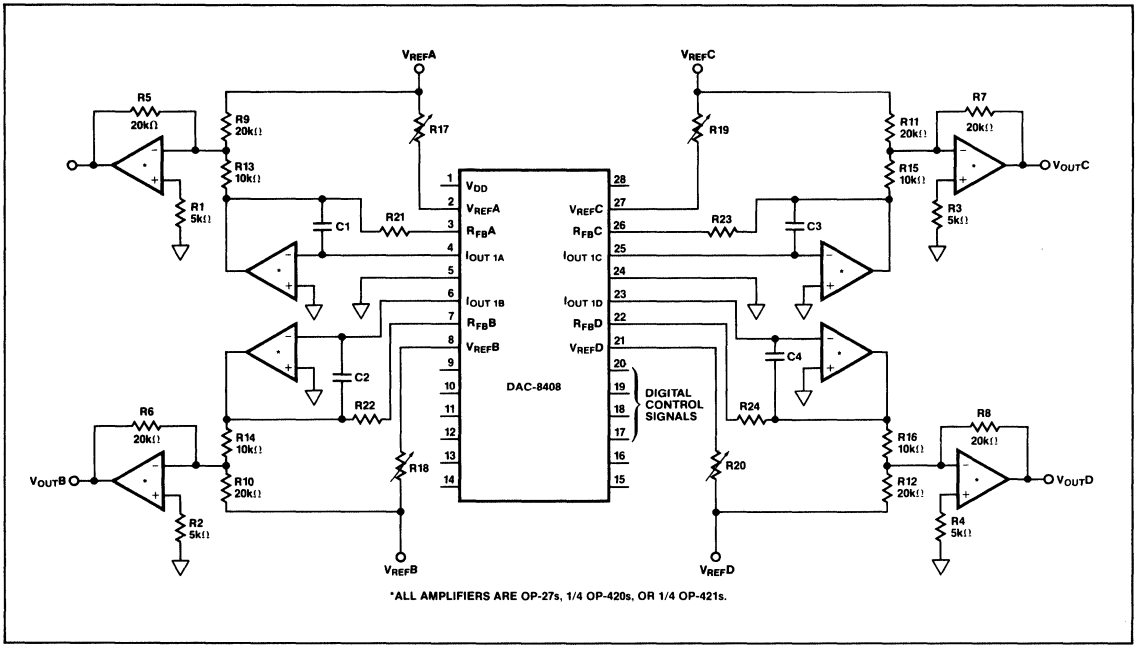


TABLE II: Bipolar (Offset Binary) Code Table (Refer to Figure 7.)

DAC DATA INPUT MSB							LSB	ANALOG OUTPUT (DAC A OR DAC B)
1	1	1	1	1	1	1	1	$+V_{REF}\left(\frac{127}{128}\right)$
1	0	0	0	0	0	0	1	$+V_{REF}\left(\frac{1}{128}\right)$
1	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{1}{128}\right)$
0	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{127}{128}\right)$
0	0	0	0	0	0	0	0	$-V_{REF}\left(\frac{128}{128}\right)$

NOTE:
1 LSB = (2^{-7}) $(V_{REF}) = \frac{1}{128}$ (V_{REF})

APPLICATION HINTS

General Ground Management: AC or transient voltages between AGND and DGND can appear as noise at the DAC-8408's analog output. Note that in Figures 5 and 6, $I_{OUT\,2A}/I_{OUT\,2B}$ and $I_{OUT\,2C}/I_{OUT\,2D}$ are connected to AGND. Therefore, it is recommended that AGND and DGND be tied together at the DAC-8408 socket. In systems where AGND and DGND are tied together on the backplane, two diodes (1N914 or equivalent) should be connected in inverse parallel between AGND and DGND.

Write Enable Timing: During the period when both $\overline{DS}$ and R/$\overline{W}$ are held low, the DAC latches are transparent and the analog output responds directly to the digital data input. To prevent unwanted variations of the analog output, the R/$\overline{W}$ should not go low until the data bus is fully settled (DATA VALID).

8

SINGLE SUPPLY, VOLTAGE OUTPUT OPERATION

The DAC-8408 can be connected with a single +5V supply to produce DAC output voltages from 0V to +1.5V. In Figure 8, the DAC-8408 R-2R ladder is inverted from its normal connection. A +1.500V reference is connected to the current output pin 4 ($I_{OUT\,1A}$), and the normal V_{REF} input pin becomes the DAC output. Instead of a normal current output, the R-2R ladder outputs a voltage. The OP-490, consisting of four precision low-power op amps that can operate its inputs and outputs to zero volts, buffers the DAC to produce a low-impedance output voltage from 0V to +1.5V full-scale. Table III shows the code table.

With the supply and reference voltages as shown, better than 1/2 LSB differential and integral nonlinearity can be expected. To maintain this performance level, the +5V supply must not drop below 4.75V. Similarly, the reference voltage must be no higher than 1.5V. This is because the CMOS switches require a minimum level of bias in order to maintain the linearity performance.

TABLE III: Single Supply Binary Code Table (Refer to Figure 8)

DAC DATA INPUT MSB							LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	$V_{REF}\left(\frac{255}{256}\right)$, +1.4941V
1	0	0	0	0	0	0	1	$V_{REF}\left(\frac{129}{256}\right)$, +0.7559V
1	0	0	0	0	0	0	0	$V_{REF}\left(\frac{128}{256}\right)$, +0.7500V
0	1	1	1	1	1	1	1	$V_{REF}\left(\frac{127}{256}\right)$, +0.7441V
0	0	0	0	0	0	0	1	$V_{REF}\left(\frac{1}{256}\right)$, +0.0059V
0	0	0	0	0	0	0	0	$V_{REF}\left(\frac{0}{256}\right)$, 0.0000V

FIGURE 8: Unipolar Supply, Voltage Output DAC Operation

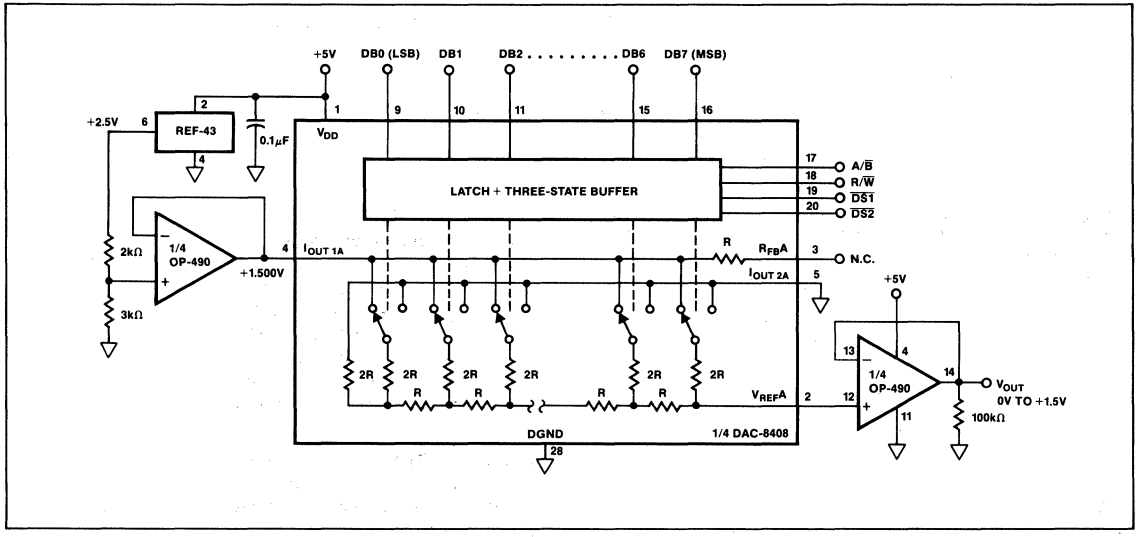
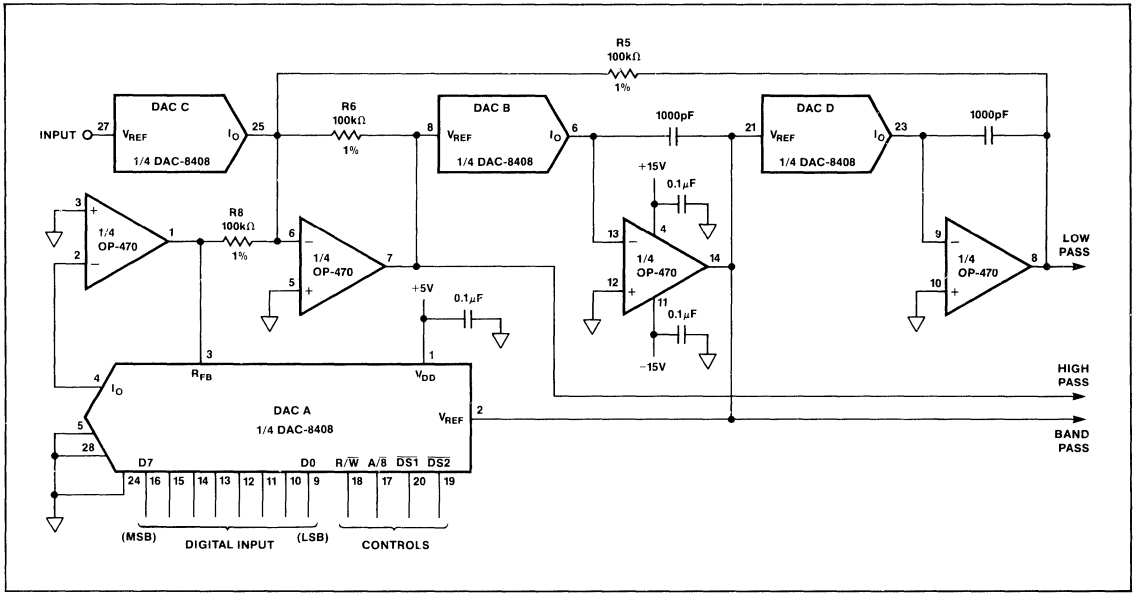


FIGURE 9: A Digitally Programmable Universal Active Filter

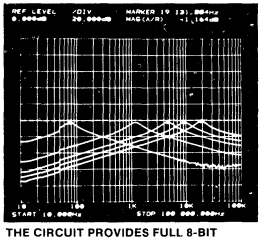


A DIGITALLY PROGRAMMABLE ACTIVE FILTER

A powerful D/A converter application is a programmable active filter design as shown in Figure 9. The design is based on the state-variable filter topology which offers stable and repeatable filter characteristics. DAC B and DAC D can be programmed in tandem with a single digital byte load which sets the center frequency of the filter. DAC A sets the Q of the filter. DAC C sets the gain of the filter transfer function. The unique feature of this design is that varying the gain of filter does not affect the Q of the filter. Similarly, the reverse is also true. This makes the programmability of the filter extremely reliable and predictable. Note that low-pass, high-pass, and bandpass outputs are available. This sophisticated function is achieved in only two IC packages.

The network analyzer photo shown in Figure 10 superimposes five actual bandpass responses ranging from the lowest frequency of 75Hz (1 LSB ON) to a full-scale frequency of 19.132kHz (all bits ON), which is equivalent to a 256 to 1 dynamic range. The frequency is determined by $f_C = 1/2\pi RC$ where R is the ladder resistance (R_{IN}) of the DAC -8408, and C is 1000pF. Note that from device to device, the resistance R_{IN} varies. Thus some tuning may be necessary.

FIGURE 10: Programmable Active Filter Band-Pass Frequency Response

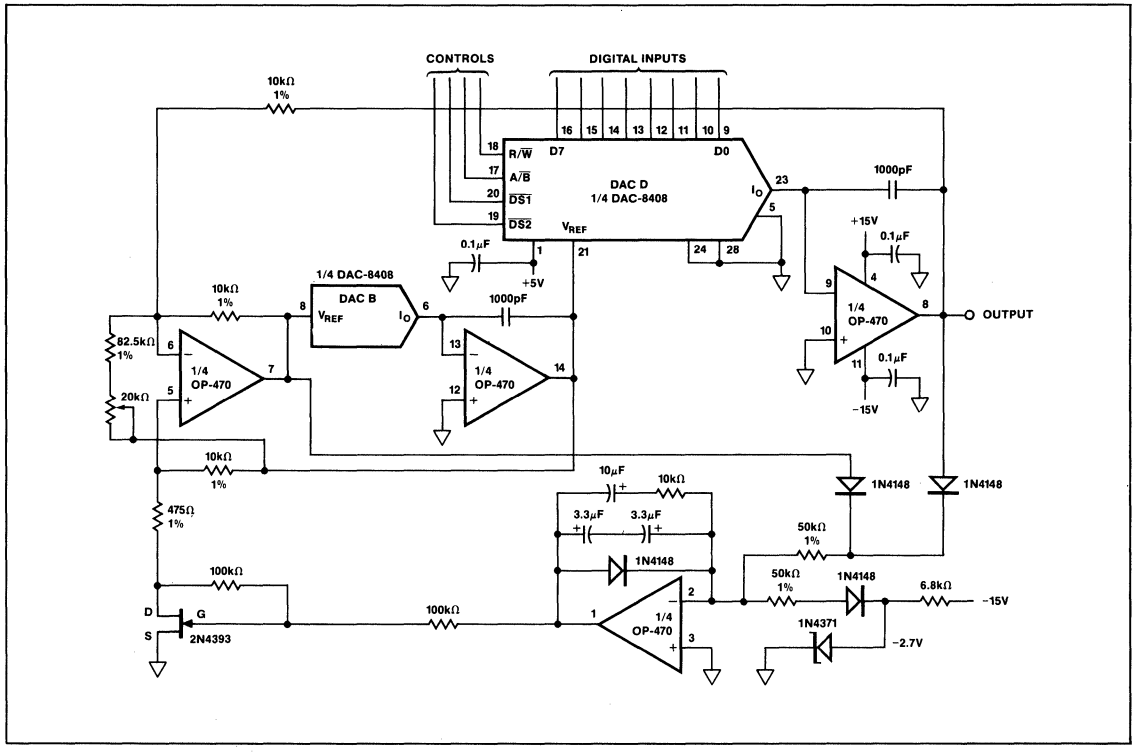


THE CIRCUIT PROVIDES FULL 8-BIT (> 2 DECADE) DYNAMIC RANGE OF FREQUENCY CONTROL

All components used are available off-the-shelf. Using low drift thin-film resistors, the DAC-8408 exhibits very stable performance over temperature. The wide bandwidth of the OP-470 produces excellent high frequency and high Q response. In addition, the OP-470's low input offset voltage assures an unusually low DC offset at the filter output.

8

FIGURE 11: A Digitally Programmable, Low-Distortion Sinewave Oscillator



A LOW-DISTORTION, PROGRAMMABLE SINEWAVE OSCILLATOR

By varying the previous state-variable filter topology slightly, one can obtain a very low distortion sinewave oscillator with programmable frequency feature as shown in Figure 11. Again, DAC B and DAC D in tandem control the oscillating frequency based on the relationship $f_c = 1/2\pi RC$. Positive feedback is accomplished via the 82.5kΩ and the 20kΩ potentiometer. The Q of the oscillator is determined by the ratio of 10kΩ and 475Ω in series with the FET transistor, which acts as an automatic gain control variable resistor. The AGC action maintains a very stable sinewave amplitude at any frequency. Again, only two ICs accomplish a very useful function.

At the highest frequency setting, the harmonic distortion level measures 0.016%. As the frequencies drop, distortion also drops to a low of 0.006%. At the lowest frequency setting, distortion came back up to a worst case of 0.035%.

ANALOG DEVICES

Octal 8-Bit CMOS D/A Converter

DAC-8800

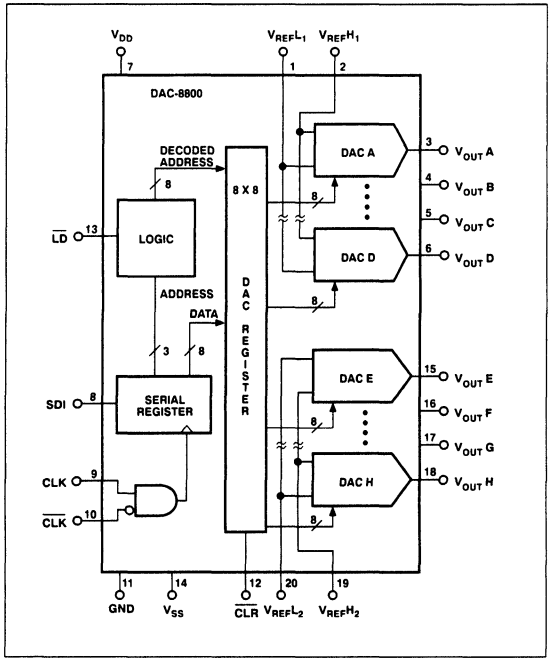
FEATURES

- ±1/2 LSB Total Unadjusted Error
- 2μs Settling Time
- Serial Data Input
- ±Full-Scale Output Set by $V_{REF}H$ and $V_{REF}L$
- Unipolar and Bipolar Operation
- TTL Input Compatible
- 20-Pin DIP or SOL Package
- Low Cost

APPLICATIONS

- Voltage Set Point Control
- Digital Offset & Gain Adjustment
- Microprocessor Controlled Calibration
- General Purpose Trimming Adjustments

FUNCTIONAL DIAGRAM



GENERAL DESCRIPTION

The DAC-8800 TrimDAC™ is designed to be a general purpose digitally controlled voltage adjustment device. The output voltage range can be independently set for each set of four D/A converters. In addition, both unipolar and bipolar output voltage ranges are easy to establish by external reference input high and low terminals. The digitally-programmed output voltages are ideal for op amp trimming, voltage-controlled amplifier gain setting and any general purpose trimming tasks.

A three-wire serial digital interface loads the contents of eight internal DAC registers which establish the output voltage levels. An asynchronous Clear ($\overline{CLR}$) input places all DACs in a zero code output condition, very handy for system power-up. An internal regulator provides TTL input compatibility over a wide range of V_{DD} supply voltages. Single supply operation is available by connecting V_{SS} to GND.

ORDERING INFORMATION †

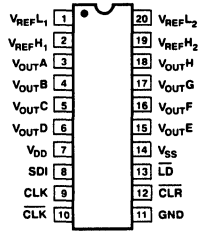
PACKAGE			OPERATING TEMPERATURE RANGE
CERDIP 20-PIN	PLASTIC 20-PIN	SO 20-PIN	
DAC8800BR*	–	–	–55°C to +125°C
DAC8800FR	DAC8800FP	DAC8800FS††	–40°C to +85°C

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP and plastic DIP packages.

†† For availability and burn-in information on SO package, contact your local sales office.

PIN CONNECTIONS



20-PIN CERDIP (R-Suffix)

20-PIN SOL (S-Suffix)

20-PIN EPOXY DIP (P-Suffix)

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ELECTRICAL CHARACTERISTICS: (Note 1) Unless otherwise noted, SINGLE SUPPLY: V_{DD} = +12V, V_{SS} = 0V, $V_{REF}H$ = +5V, $V_{REF}L$ = 0V; or DUAL SUPPLY: V_{DD} = +12V, V_{SS} = –5V, $V_{REF}H$ = +2.5V, $V_{REF}L$ = –2.5V; F GRADE: –40°C ≤ T_A ≤ +85°C; B GRADE: –55°C ≤ T_A ≤ +125°C.

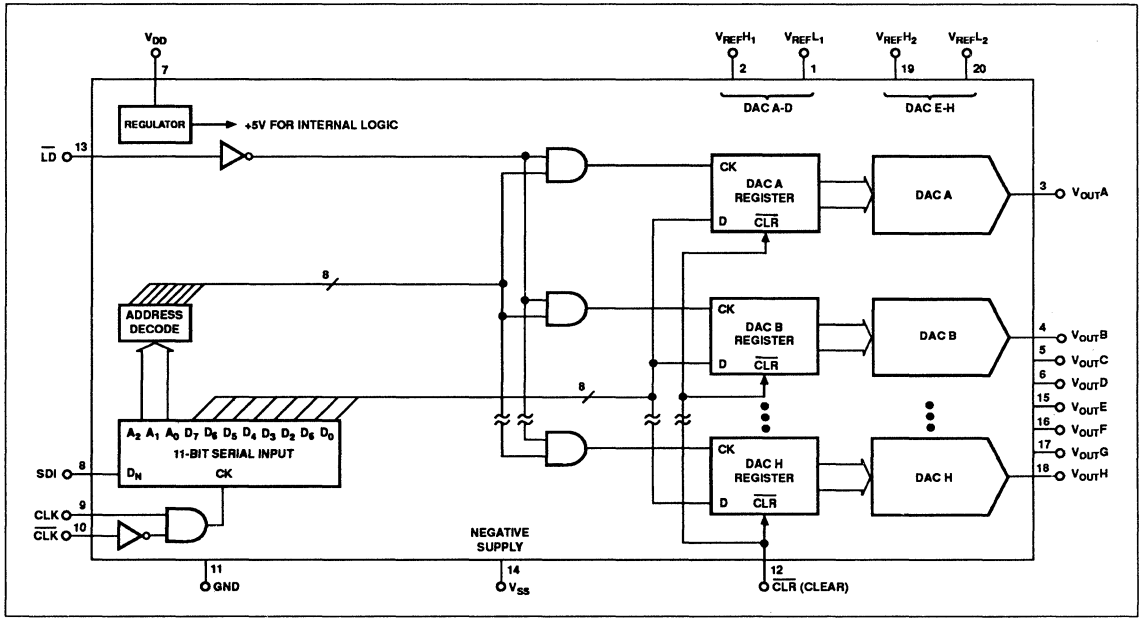
			DAC-8800			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
STATIC ACCURACY	All specifications apply for DACs A, B, C, D, E, F, G, H					
Resolution	N		8	–	–	Bits
Total Unadjusted Error (Note 2)	TUE		–	–	±1/2	LSB
Differential Nonlinearity (Note 3)	DNL		–	–	±1	LSB
Full Scale Error	G_{FSE}		–	–	±1/2	LSB
Zero Code Error	V_{ZSE}		–	–	±1/2	LSB
DAC Output Resistance	R_{OUT}		8	12	16	kΩ
DAC Output Resistance Match	$\Delta R_{OUT}/R_{OUT}$		–	0.5	–	%
REFERENCE INPUT						
Voltage Range (Note 5)	$V_{REF}H$	Pins 2 & 19	$V_{REF}L$	–	$(V_{DD}-4)$	V
	$V_{REF}L$	Pins 1 & 20	V_{SS}	–	$V_{REF}H$	
Input Resistance	$V_{REF}H$	Digital Inputs = 55_H	2	3	–	kΩ
Input Resistance Match	$\Delta R_{REF}H/R_{REF}H$	Digital Inputs = 55_H	–	0.5	–	%
Reference Input Capacitance (Note 4)	C_{REF}	Digital Inputs All Zeros Digital Inputs All Ones	– –	50 75	75 100	pF
DIGITAL INPUTS						
Logic High	V_{INH}		2.4	–	–	V
Logic Low	V_{INL}		–	–	0.8	V
Input Current	I_{IN}	V_{IN} = 0V or +5V	–	–	±1	µA
Input Capacitance (Note 4)	C_{IN}		–	4	8	pF
Input Coding				BINARY		
POWER SUPPLIES (Note 6)						
Positive Supply Current	I_{DD}	Dual Supply TTL Dual Supply CMOS	– –	1 0.2	2 0.4	mA
Negative Supply Current	I_{SS}	Dual Supply	–	0.01	0.2	mA
Power Dissipation	P_{DISS}	Single Supply Operation Dual Supply Operation	– –	12 12	24 25	mW
DC Power Supply Rejection Ratio	PSRR	ΔV_{DD} =±5%	–	0.001	0.01	%/%
DYNAMIC PERFORMANCE (Note 4)						
V_{OUT} Settling Time	t_S	±1/2 LSB Error Band	–	0.8	2	µs
Channel-to-Channel Crosstalk (Note 7)	CT	Measured Between Adjacent DAC Outputs	–	80	–	nVs

ELECTRICAL CHARACTERISTICS: (Note 1) Unless otherwise noted, SINGLE SUPPLY: V_{DD} = +12V, V_{SS} = 0V, $V_{REF}H$ = +5V, $V_{REF}L$ = 0V; or DUAL SUPPLY: V_{DD} = +12V, V_{SS} = –5V, $V_{REF}H$ = +2.5V, $V_{REF}L$ = –2.5V; F GRADE: –40°C ≤ T_A ≤ +85°C; B GRADE: –55°C ≤ T_A ≤ +125°C. *Continued*

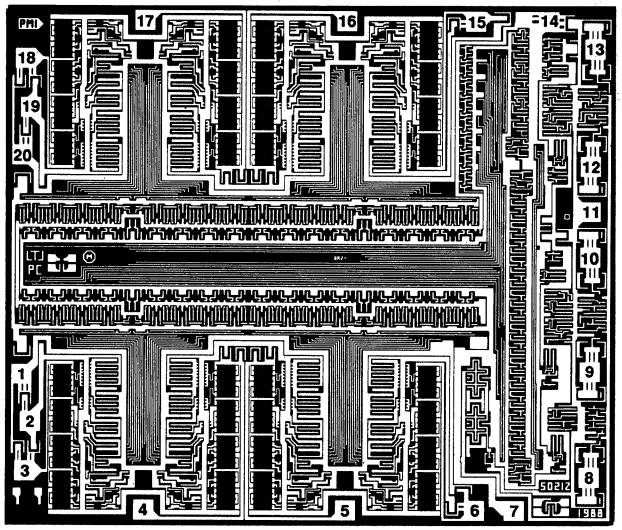
PARAMETER	SYMBOL	CONDITIONS	DAC-8800 MIN	DAC-8800 TYP	DAC-8800 MAX	UNITS
SWITCHING CHARACTERISTICS (Notes 4, 8)						
Input Clock Pulse Width	t_{CH}, t_{CL}	Clock Level High or Low	60	–	–	ns
Data Setup Time	t_{DS}		30	–	–	ns
Data Hold Time	t_{DH}		30	–	–	ns
DAC Register Load Pulse Width	t_{LD}		50	–	–	ns
Clear Pulse Width	t_{CLR}		50	–	–	ns
Clock Edge to Load Time	t_{CKLD}		50	–	–	ns
Load Edge to Next Clock Edge Time	t_{LDCK}		50	–	–	ns

NOTES:
1. Testing performed in SINGLE SUPPLY mode, except I_{DD}, I_{SS}, and PSRR which are tested in DUAL SUPPLY mode.
2. Includes Full Scale Error, Relative Accuracy, and Zero Code Error.
3. All devices guaranteed monotonic over the full operating temperature range.
4. Guaranteed by design and not subject to production test.
5. V_{DD} – 4 volts is the maximum reference voltage for the above specifications. Also $V_{REF}H \geq V_{REF}L$.
6. Digital Input voltages $V_{IN} = V_{INL}$ or V_{INH} for TTL condition; V_{IN} = 0V or +5V for CMOS condition. DAC outputs unloaded. P_{DISS} is calculated from $(I_{DD} \times V_{DD}) + (I_{SS} \times V_{SS})$.
7. Measured at V_{OUT} pin where an adjacent V_{OUT} pin is making a full-scale voltage change.
8. See timing diagram for location of measured values.

DETAILED DAC-8800 BLOCK DIAGRAM



DICE CHARACTERISTICS



1. $V_{REF}L_1$
2. $V_{REF}H_1$
3. $V_{OUT}A$
4. $V_{OUT}B$
5. $V_{OUT}C$
6. $V_{OUT}D$
7. V_{DD}
8. SDI
9. CLK
10. $\overline{CLK}$
11. GND
12. $\overline{CLR}$
13. $\overline{LD}$
14. V_{SS}
15. $V_{OUT}E$
16. $V_{OUT}F$
17. $V_{OUT}G$
18. $V_{OUT}H$
19. $V_{REF}H_2$
20. $V_{REF}L_2$

DIE SIZE 0.151 × 0.130 inch, 19,630 sq. mils
(3.8354 × 3.3033 mm, 12.664 sq. mm)

WAFER TEST LIMITS at V_{DD} = +12V, V_{SS} = 0V, $V_{REF}H$ = +5V, $V_{REF}L$ = 0V; T_A = +25°C unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		DAC-8800G LIMIT	UNITS
Total Unadjusted Error	TUE			±1/2	LSB MAX
Differential Nonlinearity	DNL			±1	LSB MAX
Full Scale Error	G_{FSE}			±1/2	LSB MAX
Zero Code Error	V_{ZSE}			±1/2	LSB MAX
DAC Output Resistance	R_{OUT}			8 16	kΩ MIN kΩ MAX
Reference Input Resistance	$R_{REF}H$	Digital Inputs = 55H		2	kΩ MIN
Digital Inputs High	V_{INH}			2.4	V MIN
Digital Inputs Low	V_{INL}			0.8	V MAX
Digital Input Current	I_{IN}	V_{IN} = 0V or +5V		±1	µA MAX
Positive Supply Current	I_{DD}	V_{SS} = −5V	TTL CMOS	2 0.4	mA MAX
Negative Supply Current	I_{SS}	V_{SS} = −5V		0.2	mA MAX
DC Power Supply Rejection Ratio	PSRR	ΔV_{DD} = ±5%		0.01	%/% MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted)

V_{DD} to V_{SS} ..... 0V, +20V
V_{DD} to GND ..... 0V, +20V
V_{SS} to GND ..... –20V, 0V
Digital Input Voltage to GND ..... GND – 0.3V, V_{DD} + 0.3V
$V_{REF}H$ to GND ..... $V_{REF}L$, V_{DD}
$V_{REF}L$ to GND ..... V_{SS}, $V_{REF}H$
V_{OUT} to GND ..... $V_{REF}L$, $V_{REF}H$
Operating Temperature Range
Military, DAC-8800BR ..... –55°C to +125°C
Extended Industrial, DAC-8800FR,FP,FS ...–40°C to +85°C
Maximum Junction Temperature (T_j Max) ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation ..... (T_j Max – T_A)/Θ_{JA}

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
20-Pin Hermetic DIP (R)	76	11	°C/W
20-Pin Plastic DIP (P)	69	27	°C/W
20-Pin SO (S)	88	25	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than V_{SS} potential on any terminal.
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets; remove power before insertion or removal.
4. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to device.

TABLE 1: PIN Function Description

PIN	MNEMONIC	DESCRIPTION
1	$V_{REF}L_1$	External DAC voltage reference input shared by DAC A, B, C, D. $V_{REF}L_1$ determines the lowest negative DAC output voltage. $V_{REF}L_1$ must be equal to or more positive than V_{SS}.
2	$V_{REF}H_1$	External DAC voltage reference input shared by DAC A, B, C, D. $V_{REF}H_1$ determines the highest positive DAC output voltage.
3	$V_{OUT}A$	DAC A Output } Output voltage determined by external $V_{REF}H_1$ and $V_{REF}L_1$.
4	$V_{OUT}B$	DAC B Output
5	$V_{OUT}C$	DAC C Output
6	$V_{OUT}D$	DAC D Output
7	V_{DD}	Positive supply, allowable input voltage range +4.5V to +16V.
8	SDI	Serial Data Input } TTL Input Compatible
9	CLK	Serial Clock Input, positive edge triggered
10	$\overline{CLK}$	Clock Enable or Serial Clock Input, negative edge triggered
11	GND	Ground
12	$\overline{CLR}$	Clear Input (Active Low), Asynchronous TTL compatible input that resets all DAC registers to zero code.
13	$\overline{LD}$	Load DAC Register Strobe, TTL compatible input that transfers data bits from serial input register into the decoded DAC register. See Table 2.
14	V_{SS}	Negative Supply, allowable input voltage range 0V to –12V.
15	$V_{OUT}E$	DAC E Output } Output voltage determined by external $V_{REF}H_2$ and $V_{REF}L_2$.
16	$V_{OUT}F$	DAC F Output
17	$V_{OUT}G$	DAC G Output
18	$V_{OUT}H$	DAC H Output
19	$V_{REF}H_2$	External DAC voltage reference input shared by DAC E, F, G, H. $V_{REF}H_2$ determines the highest positive DAC output voltage.
20	$V_{REF}L_2$	External DAC voltage reference input shared by DAC E, F, G, H. $V_{REF}L_2$ determines the lowest negative DAC output voltage. $V_{REF}L_2$ must be equal to or more positive than V_{SS}.

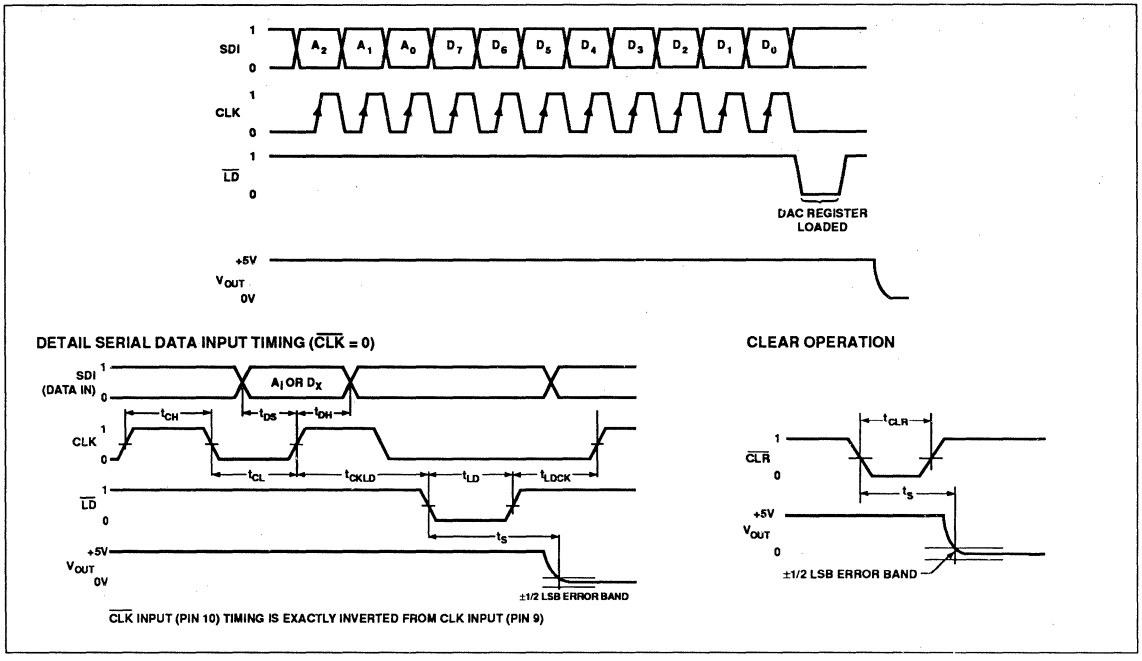


FIGURE 1: *Timing Diagrams*

TABLE 2: Serial Input Decode Table

LAST → FIRST

LSB D_0	D_1	D_2	D_3	D_4	D_5	D_6	MSB D_7	LSB A_0	A_1	MSB A_2

MSB D_7	D_6	D_5	D_4	D_3	D_2	D_1	LSB D_0	DAC OUTPUT VOLTAGE ($K = V_{REF}H - V_{REF}L$)
0	0	0	0	0	0	0	0	$V_{REF}L$
0	0	0	0	0	0	0	1	$(1/256) \times K + V_{REF}L$
⋮								
0	1	1	1	1	1	1	1	$(127/256) \times K + V_{REF}L$
1	0	0	0	0	0	0	0	$(128/256) \times K + V_{REF}L$
1	0	0	0	0	0	0	1	$(129/256) \times K + V_{REF}L$
⋮								
1	1	1	1	1	1	1	1	$(255/256) \times K + V_{REF}L$

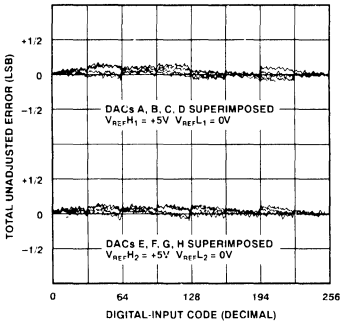
MSB A_2	A_1	LSB A_0	DAC UPDATED
0	0	0	DAC A
0	0	1	DAC B
0	1	0	DAC C
0	1	1	DAC D
1	0	0	DAC E
1	0	1	DAC F
1	1	0	DAC G
1	1	1	DAC H

TABLE 3: Logic Control Input Truth Table

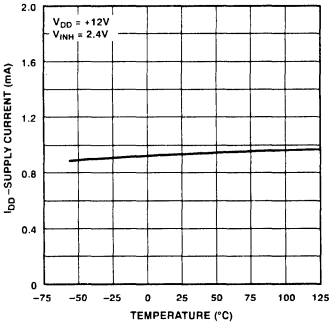
CLK	$\overline{CLK}$	INPUT SHIFT REGISTER OPERATON
↑	L	Shift Data
H	↓	Shift Data
L	X	No Operation
X	H	No Operation

TYPICAL PERFORMANCE CHARACTERISTICS

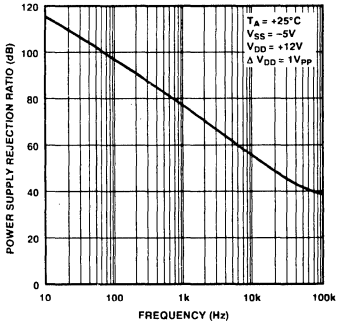
TOTAL UNADJUSTED ERROR vs DIGITAL INPUT CODE



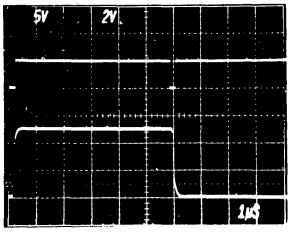
SUPPLY CURRENT vs TEMPERATURE



POWER SUPPLY REJECTION RATIO vs FREQUENCY

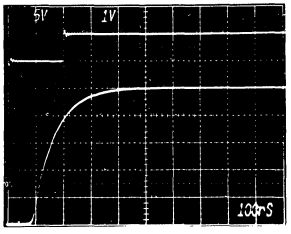


DAC OUTPUT SETTLING TIME POSITIVE & NEGATIVE TRANSITIONS



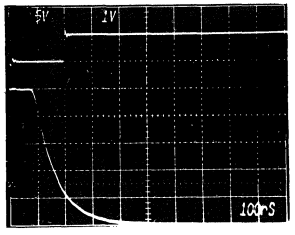
UPPER TRACE: t_{LD} INPUT (5V/DIV)
LOWER TRACE: $V_{OUT}A$ (2V/DIV)
CONDITIONS: V_{DD} = +12V, $V_{REF}H_1$ = +5V, $V_{REF}L_1$ = 0V, V_{SS} = 0V, R_L = 1MΩ, C_L = 3.4pF

EXPANDED DAC OUTPUT SETTLING TIME POSITIVE TRANSITION



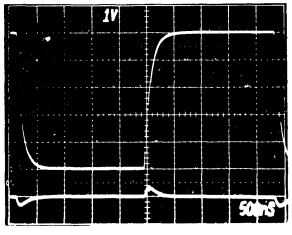
UPPER TRACE: t_{LD} INPUT (5V/DIV)
LOWER TRACE: $V_{OUT}A$ (1V/DIV)
CONDITIONS: V_{DD} = +12V, $V_{REF}H_1$ = +5V, $V_{REF}L_1$ = 0V, V_{SS} = 0V, R_L = 1MΩ, C_L = 3.4pF

EXPANDED DAC OUTPUT SETTLING TIME NEGATIVE TRANSITION



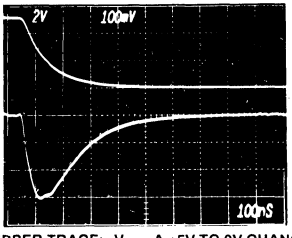
UPPER TRACE: t_{LD} INPUT (5V/DIV)
LOWER TRACE: $V_{OUT}A$ (1V/DIV)
CONDITIONS: V_{DD} = +12V, $V_{REF}H_1$ = +5V, $V_{REF}L_1$ = 0V, V_{SS} = 0V, R_L = 1MΩ, C_L = 3.4pF

DAC OUTPUT CHANNEL-TO-CHANNEL CROSSTALK BOTH TRANSITIONS



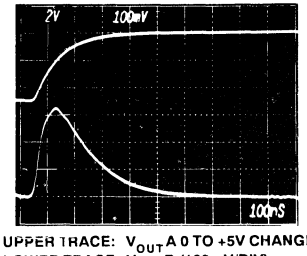
UPPER TRACE: $V_{OUT}A$ 0 TO +5V CHANGE
LOWER TRACE: $V_{OUT}B$ (1V/DIV)
CONDITIONS: V_{DD} = +12V, $V_{REF}H_1$ = +5V, $V_{REF}L_1$ = 0V, V_{SS} = 0V, R_L = 1MΩ, C_L = 3.4pF

EXPANDED DAC OUTPUT CHANNEL-TO-CHANNEL CROSS-TALK NEGATIVE TRANSITION



UPPER TRACE: $V_{OUT}A$ +5V TO 0V CHANGE
LOWER TRACE: $V_{OUT}B$ (100mV/DIV)
CONDITIONS: V_{DD} = +12V, $V_{REF}H_1$ = +5V, $V_{REF}L_1$ = 0V, V_{SS} = 0V, R_L = 1MΩ, C_L = 3.4pF

EXPANDED DAC OUTPUT CHANNEL-TO-CHANNEL CROSS-TALK POSITIVE TRANSITION



UPPER TRACE: $V_{OUT}A$ 0 TO +5V CHANGE
LOWER TRACE: $V_{OUT}B$ (100mV/DIV)
CONDITIONS: V_{DD} = +12V, $V_{REF}H_1$ = +5V, $V_{REF}L_1$ = 0V, V_{SS} = 0V, R_L = 1MΩ, C_L = 3.4pF

8

CIRCUIT OPERATION

The DAC-8800 provides a programmable voltage output adjustment capability. Changing the programmed output voltage of each DAC is accomplished by clocking in an 11-bit serial data word into pin SDI (Serial Data Input). The format of this data word is three address bits, MSB first, followed by 8 data bits, MSB first. Table 2 provides the serial input decode table for data loading. DAC outputs can be changed one at a time in random sequence. The fast serial-data clocking of 6.6MHz makes it possible to load all 8 DACs in as little time as 14 microseconds. The exact timing requirements are provided in Figure 1.

A clear ($\overline{CLR}$) input pin allows the circuit to be powered-up in the all zero state or a system reset pulse connected to $\overline{CLR}$ can asynchronously clear all data registers.

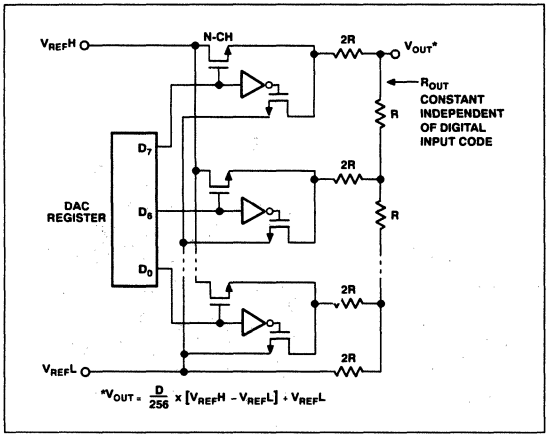


FIGURE 2: *DAC-8800 TrimDAC™ Equivalent DAC Circuit*

The output voltage range is determined by the external input voltages applied to $V_{REF}H$ and $V_{REF}L$. See Figure 2 for a simplified equivalent DAC circuit. If a negative supply is used on V_{SS} then $V_{REF}L$ may be set negative resulting in a programmable bipolar output voltage swing.

The actual output voltage, V_{OUT}, depends on $V_{REF}H$ and $V_{REF}L$ as follows:

$$V_{OUT}(D) = D \times (V_{REF}H - V_{REF}L)/256 + V_{REF}L$$

where D is a whole number binary digital input word loaded into the DAC register. For example, when $V_{REF}H = +5V$ and $V_{REF}L = 0V$ unipolar output operation results with the following binary digital inputs:

D	$V_{OUT}(D)$	$V_{REF}H = +5.00V$; $V_{REF}L = 0V$
255	4.98V	Full-Scale
128	2.50V	Half-Scale
1	0.02V	1 LSB
0	0.00V	Zero-Scale also generated When $\overline{CLR}$ Input Activated

Bipolar output operation is achieved when $V_{REF}H = +2.5V$ and $V_{REF}L = -2.5V$, also note V_{SS} must be equal to or more negative than $V_{REF}L$. $V_{SS} = -5V$ is a good choice for this example. The following example lists the actual bipolar output voltages produced by the binary digital input which would now be considered offset-binary coded:

D	$V_{OUT}(D)$	$V_{REF}H = +2.50V$; $V_{REF}L = -2.50V$
255	2.48V	Positive Full-Scale
129	0.02V	Positive 1 LSB
128	0.00V	Bipolar Zero-Scale
127	–0.02V	Negative 1 LSB
0	–2.50V	Negative Full-Scale

REFERENCE INPUTS ($V_{REF}H_1$, $V_{REF}L_1$, $V_{REF}H_2$, $V_{REF}L_2$)

The external voltages connected to the V_{REF} input pins determine the programmable output voltage ranges of the two sets of four DACs in the DAC-8800. Specifically, $V_{REF}H_1$ and $V_{REF}L_1$ are connected to DACs, A, B, C, D, and $V_{REF}H_2$ and $V_{REF}L_2$ are connected to DACs E, F, G, H.

Inspection of the DAC-8800 equivalent DAC circuit (Figure 2) shows the external $V_{REF}H$ and $V_{REF}L$ inputs connected to the internal DAC switches. During updating, the DAC switches produce transient current flowing from $V_{REF}H$ to $V_{REF}L$. It is recommended to place 0.01µF bypass capacitors across the $V_{REF}H$ and $V_{REF}L$ inputs to minimize the voltage transients.

A wide range of external voltage references can be used subject to the reference input voltage range boundary conditions. First $V_{REF}H$ should always be more positive than $V_{REF}L$. DC voltages are recommended. $V_{REF}L$ can be equal to the negative power supply V_{SS}. This feature results in single supply operation when V_{SS} is at ground. $V_{REF}H$ should not be closer than four volts to V_{DD}. This is due to the DAC-8800 NMOS only DAC switches which will no longer operate properly if $V_{REF}H$ is closer to V_{DD} than four volts. Total unadjusted error degrades when (V_{DD} – $V_{REF}H$) is less than four volts as shown in Figure 3.

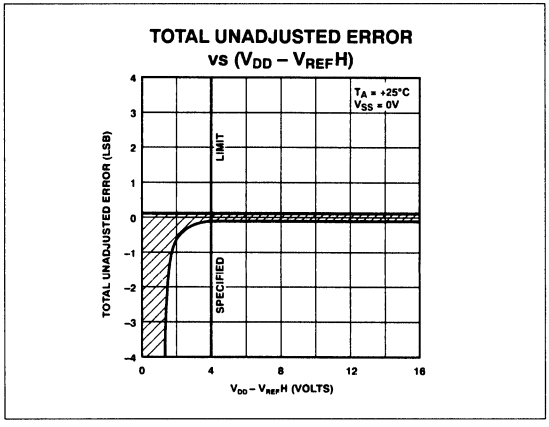


FIGURE 3: *Effect on TUE Operating Beyond (V_{DD} – $V_{REF}H$) > 4V Limit*

RECOMMENDED OPERATING POWER SUPPLY VOLTAGE RANGES

Although the DAC-8800 is thoroughly specified for operation with V_{DD} = +12V and V_{SS} = 0V or–5V, it will still function with the following recommended boundary conditions:

- (V_{DD} – V_{SS}) < 18V
- 4.5V < V_{DD} < 16V
- 0V > V_{SS} > –12V

In all cases the reference voltage boundary conditions still apply. The boundary conditions described here make it possible to use DAC-8800 with a wide variety of readily available supply voltages. Some choices include, but are not limited to:

V_{DD}/ V_{SS} = +15V/0V; +12V/0V; +12V/–5V; +5V/–5V; +5V/–12V

DAC OUTPUTS (V_{OUT} A, B, C, D, E, F, G, H)

The eight D/A converter voltage outputs have a constant output resistance independent of digital input code. The distribution of R_{OUT} from DAC to DAC within the DAC-8800 typically matches by 0.5%. Device to device R_{OUT} matching is process-lot to process-lot dependent having a ±20% variation. The change in R_{OUT} with temperature is very small as a result of PMI's low temperature coefficient SiCr thin-film resistor process.

The nominal DAC output capacitance measures three picofarads and has little variation with temperature.

One aspect of the nominal 12.5kΩ DAC output resistance is channel-to-channel crosstalk. Under a worst case condition of adjacent DAC outputs when DAC A makes a five volt output voltage change DAC B exhibits a 300mV voltage transient. See photograph in typical characteristics section of data sheet.

The channel-to-channel crosstalk is due to the 0.15pF inter-pin package capacitance. A FET probe with 3.4pF input capacitance was used to measure the DAC output channel-to-channel crosstalk characteristics shown. In voltage transient sensitive applications, minimization of crosstalk can be accomplished by placing ground traces between adjacent DAC output pins. DAC output bypass capacitors will also minimize voltage transients.

Output settling time has a dominant pole response as the photograph in the typical characteristics section shows. The output settling time characteristic consists of an 80 nanosecond propagation delay followed by a single RC decay waveform determined by the nominal R_{OUT} of 12.5kΩ times C_{OUT} plus C_{LOAD} which includes the oscilloscope probe.

The digital feedthrough from the serial data inputs (CLK, and SDI) to the DAC outputs measures less than 20mV.

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DIGITAL INTERFACING

The DAC-8800 contains a standard three-wire serial input control interface. The three inputs are clock (CLK), load ($\overline{LD}$), and serial data input (SDI). A $\overline{CLK}$ input pin is available for negative edge triggered data loading. The edge sensitive clock input pin requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. If mechanical switches are used for product evaluation they should be debounced by a flip-flop or other suitable means.

The logic control input truth table (Table 3) defines operation of the serial data input register.

The CLK input is used to place data in the serial data input register. The unused clock input (CLK or $\overline{CLK}$) should be tied to the active state (CLK = 1 or $\overline{CLK}$ = 0 for active). The load strobe ($\overline{LD}$) which must follow the eleventh active CLK edge transfers the

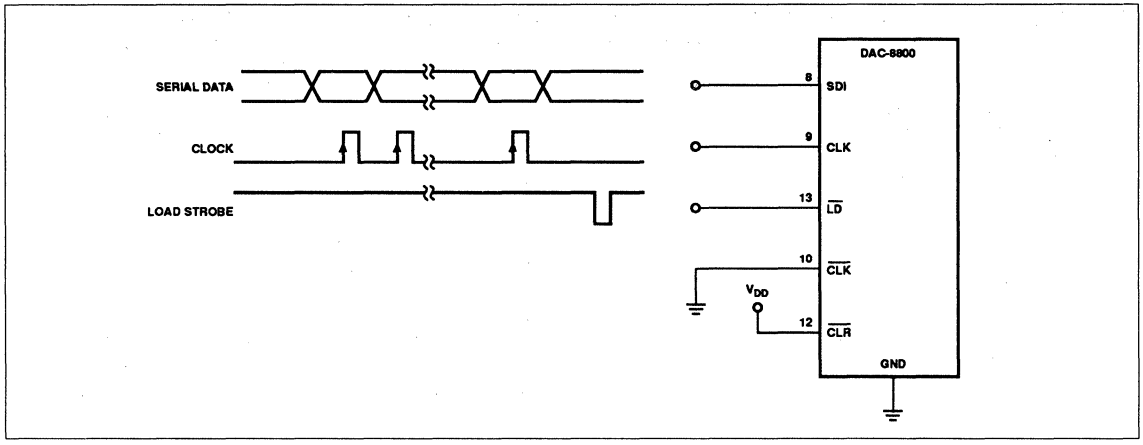

FIGURE 4: *Three-Wire Serial Interface Connections*

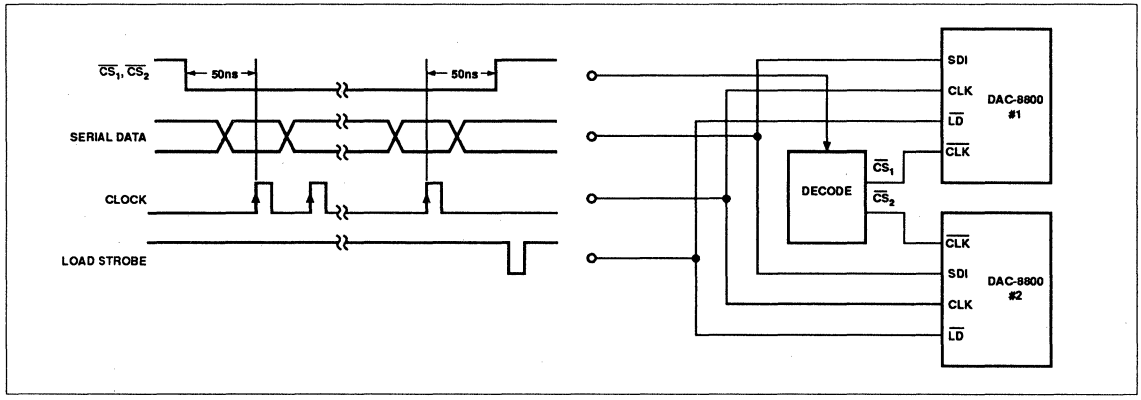

FIGURE 5a: *Decoding Multiple DAC-8800s*

data from the serial data input register to the DAC register decoded from the first three address bits clocked into the input register. Any extra CLK edges after the eleventh edge looses the first bits shifted in. See Table 2 for a complete description. See Figure 4 for an example using the CLK input pin to clock data into the SDI.

The unused clock input of Figure 4 can be used to provide a chip select ($\overline{CS}$) feature for applications using more than one DAC-8800. Figure 5a shows the proper connection and timing of the CLK inputs which assures that the $\overline{CLK}$ acting as a chip select ($\overline{CS}$) is taken to the active low state selecting the desired DAC-8800.

Another method of decoding multiple DAC-8800s is shown in Figure 5b. Here all the DAC serial input registers receive the same input data; however, only one of DAC's $\overline{LD}$ input is activated to transfer its serial input register contents into the destination DAC register. In this circuit the $\overline{LD}$ timing generated by the address decoder should follow the DAC-8800 standard timing requirements. Note the address decoder should not be activated by its $\overline{WR}$ input while the coded address inputs are changing.

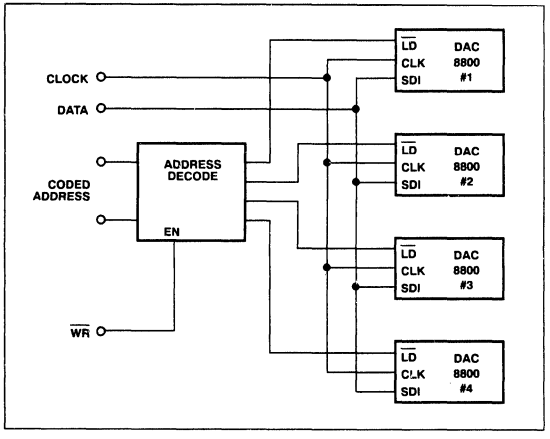

FIGURE 5b: *Decoding Multiple DAC-8800s Using the $\overline{LD}$ Input Pin*

APPLICATIONS

DIGITALLY PROGRAMMABLE AUDIO AMPLIFIER

The DAC-8800 is well suited to digitally control the gain or attenuation settings of eight voltage controlled amplifiers (VCAs). In professional audio mixing consoles, music synthesizers and other audio processor's VCAs, such as the SSM-2014, adjust audio channel gain and attenuation from front panel potentiometers. The VCA provides a clean gain transition control of audio level when the slew rate of the analog input control voltage (V_C) is properly chosen. Taking advantage of the 12.5kΩ nominal output resistance of the DAC-8800 it is very easy to control the slew rate of V_{OUT} by appropriate selection of C_{OUT}. Figure 6 shows one channel of a digitally programmable audio amplifier.

The reference high ($V_{REF}H$) and reference low ($V_{REF}L$) input voltages of the DAC-8800 provide a digitally programmable output voltage of −1.2V to +1.2V which is connected to the control voltage (V_C) input terminal of the SSM-2014 VCA. The gain of the SSM-2014 is guaranteed to change from −15dB to + 15dB for 1.2 to −1.2V input V_C voltage. A C_{OUT} of 0.1μF provides a control voltage transition time of 1.2ms which generates a click free change in audio channel gain.

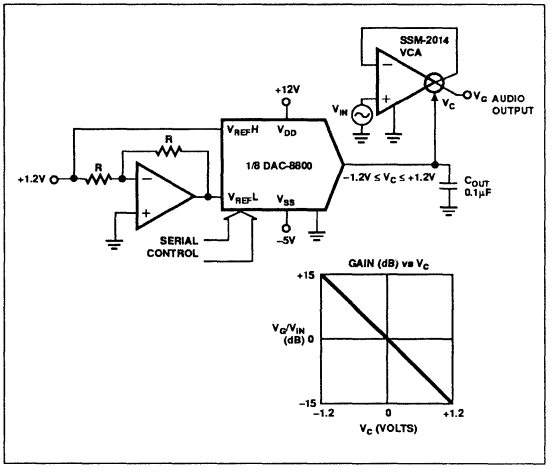

FIGURE 6: *Digitally Programmable Amplifier*

BUFFERING THE DAC-8800 OUTPUT

External op amps can be used to buffer the output of the DAC-8800's nominal 12.5kΩ output resistance. In Figure 7 a variety of possibilities are shown. The quad low power OP-420 is used as a simple buffer to reduce the output resistance of DAC A. The OP-420 was chosen for its wide operating supply range, both single and dual, low power consumption, and low cost.

The next two DACs, B and C, are configured in a summing arrangement where DAC C provides the course output voltage setting and DAC B can be used for fine adjustment. The insertion of R_1 in series with DAC B attenuates its contribution to the voltage sum node at the DAC C output.

DAC D in Figure 7 is in a noninverting gain of two configuration increasing the available output swing to 10V. Appropriate choice of external op amp gain can achieve output voltage swings beyond the range of the DAC-8800 if the external op amp power supply voltages are sufficiently high. In addition, the op amp feedback network termination could be a bias voltage which would provide an offset to the output signal swing.

SETTING COMPARATOR TRIP POINTS

The DAC-8800 is ideal to provide setpoints for voltage input comparators. In Figure 8 the very low power CMP-404 detects whether input voltage (V_{IN}) is higher or lower than the programmed limit values providing TTL compatible output signals. The compactness of the DAC-8800 makes it ideal for high density testing applications found in pin head electronics.

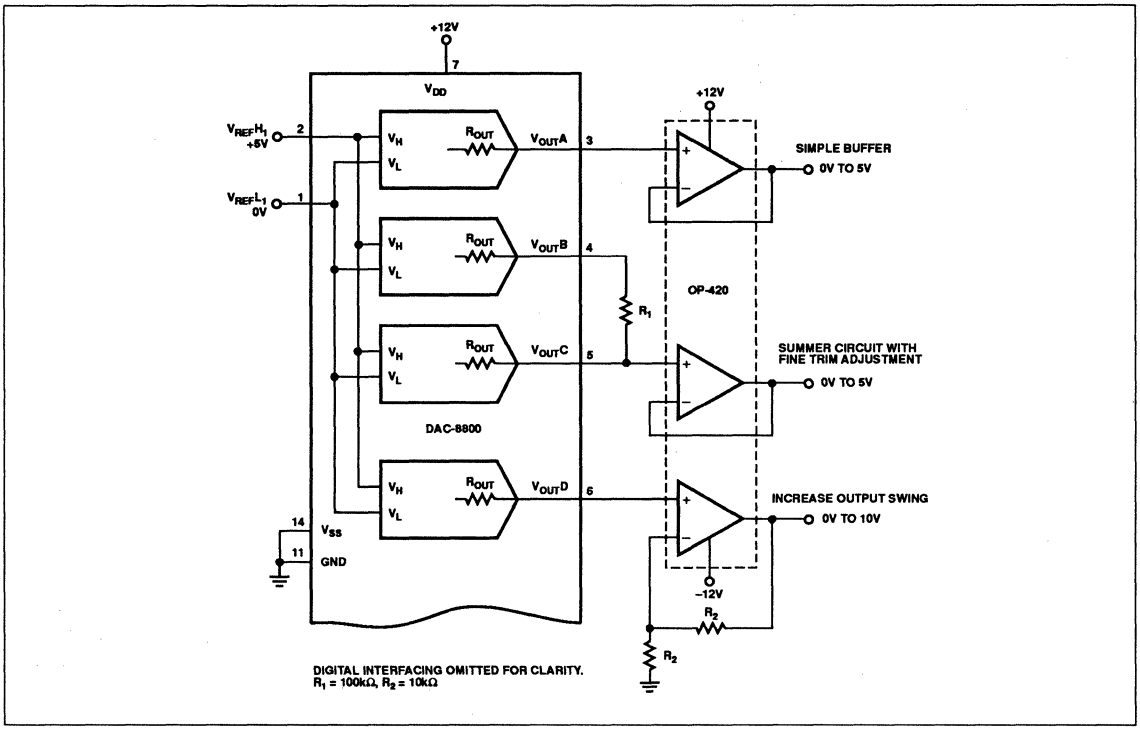

FIGURE 7: *Buffering the DAC-8800 Output*

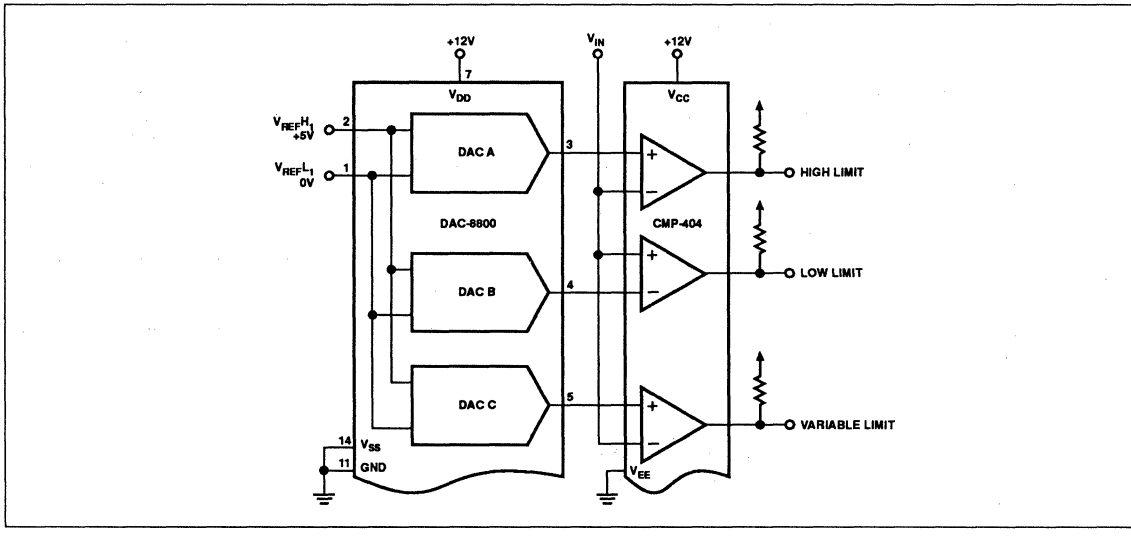

FIGURE 8: *Setting the Comparator Trip Points*

CURRENT SUMMING OUTPUT OPERATIONS

Since the DAC-8800 has a constant output resistance regardless of digital input code, it can be used in a current summing application. Figure 9 depicts the DAC output connected to the inverting input of an OP-20 low power consumption op amp. An external feedback resistor sets the output signal swing according to the formula given. The gain accuracy of this circuit has a wide variation due to the 30% output tolerance of the DAC-8800 R_{OUT} specification. A second DAC in the DAC-8800 could be used with an external resistor summed into the OP-20 current summing node to digitally adjust the full-scale swing.

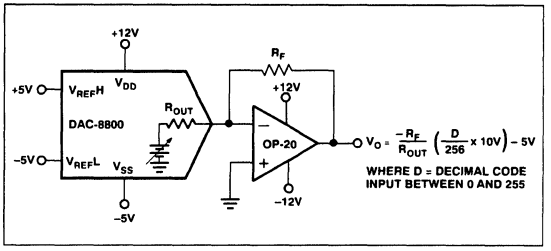

FIGURE 9: *Current Summing Output Operation*

OPTICALLY ISOLATED TWO-WIRE INTERFACE

Two-wire signal interfacing is often found in process control applications where electrical isolation of hazardous environments and minimization of wiring is necessary. Isolation transformers or optocouplers provide the high voltage isolation. Normally the DAC-8800 requires a three-wire interface to update the DAC contents. One technique which translates a two-wire interface into the three-wire signal control required by the DAC-8800 is shown in Figure 10. A single package CMOS-logic dual-retriggerable one-shot MC14538 provides the solution. At rest the optocouplers are both OFF allowing the pull-up resistors to sit at logic high. No undefined transients should occur on the control input line V_C to avoid inadvertently clocking incorrect data into the DAC-8800 serial input register. When it is time to update one of the DAC-8800 DACs, the CONTROL line will go

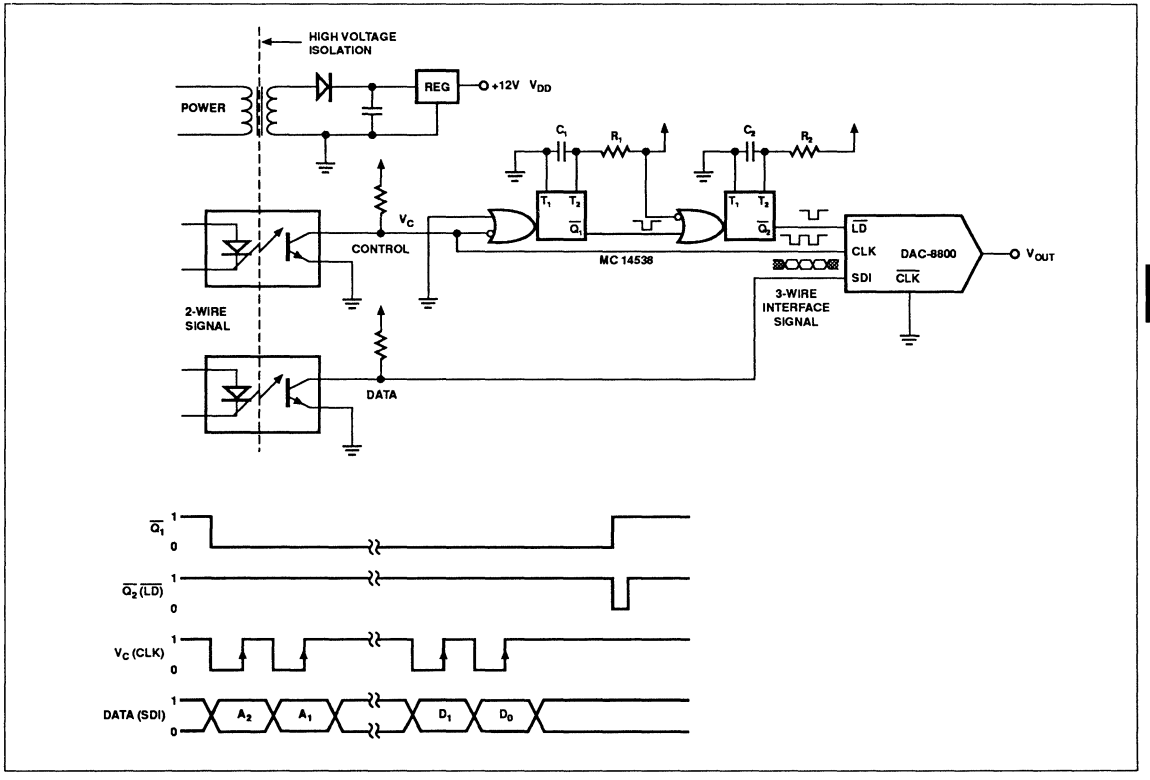

FIGURE 10: *Isolated Two-Wire Signal Interface for Serial Input DAC*

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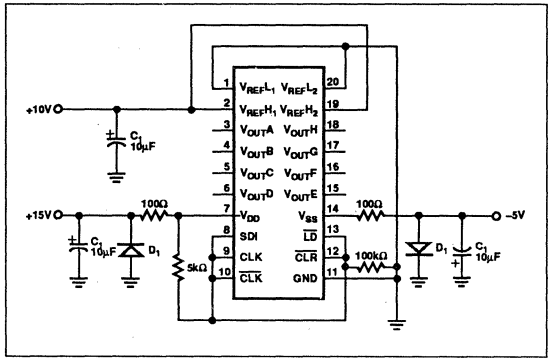
low, triggering the first one-shot ($\overline{Q_1}$). At this time valid data should also be applied to the DATA input optocoupler. Sufficient time must be allowed before the control (V_C) input returns to logic high to make sure the DAC-8800 input data is stabilized. When V_C changes to logic high, the first DATA bit shifts into the DAC-8800 serial data input register. The time constant of the first one-shot established by R_1 and C_1 should be at least twice as long as the basic CONTROL input clock period. This will prevent the $\overline{Q_1}$ output from returning to the high state. The next control input negative edge retriggers the first one-shot and sets up the DAC-8800 clock for the next DATA bit. All eleven positive clock edges will fill the DAC-8800 serial input register and each negative clock edge will retrigger the first one shot. As soon as the CONTROL line returns to the passive state, the first one shot will time out, triggering the second one shot ($\overline{Q_2}$), which will produce the required load $\overline{LD}$ pulse for the DAC-8800 to transfer its serial input register contents to the internal DAC register completing the DAC update. The R_1C_1 and R_2C_2 times need to be designed based on the system's CONTROL-input clock rate. The optocoupler clocking rate must also be considered in setting the system clock rate.

BURN-IN CIRCUIT



8-Bit, Octal, 4-Quadrant Multiplying, CMOS TrimDAC

DAC-8840

FEATURES
Replaces 8 Potentiometers
1 MHz 4-Quadrant Multiplying Bandwidth
No Signal Inversion
Low Zero Output Error
Eight Individual Channels
3-Wire Serial Input
500 kHz Update Data Loading Rate
±3 Volt Output Swing
Midscale Preset, Zero Volts Out

APPLICATIONS
Automatic Adjustment
Trimmer Replacement
Dynamic Level Adjustment
Special Waveform Generation and Modulation

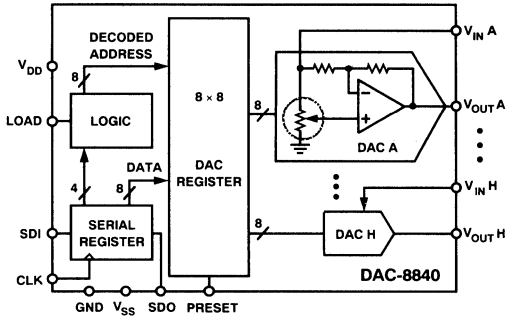
GENERAL DESCRIPTION

The DAC-8840 provides eight general purpose digitally controlled voltage adjustment devices. The TrimDAC™ capability allows replacement of the mechanical trimmer function in new designs. The DAC-8840 is ideal for ac or dc gain control of up to 1 MHz bandwidth signals. The 4-quadrant multiplying capability is useful for signal inversion and modulation often found in video convergence circuitry.

Internally the DAC-8840 contains eight voltage output CMOS digital-to-analog converters, each with separate reference inputs. Each DAC has its own DAC register which holds its output state. These DAC registers are updated from an internal serial-to-parallel shift register which is loaded from a standard 3-wire serial input digital interface. Twelve data bits make up the data word clocked into the serial input register. This data word is decoded where the first 4 bits determine the address of the DAC register to be loaded with the last 8 bits of data. A serial data output pin at the opposite end of the serial register allows simple daisy-chaining in multiple DAC applications without additional external decoding logic.

TrimDAC is a trademark of Analog Devices, Inc.

FUNCTIONAL BLOCK DIAGRAM



The DAC-8840 consumes only 190 mW from ±5 V power supplies. For single 5 V supply applications consult the DAC-8841.

The DAC-8840 is available in 24-pin plastic DIP, cerdip, and SOIC-24 packages. A separate MIL-STD/883 data sheet for −55°C to +125°C operation is available on request.

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DAC-8840—SPECIFICATIONS (V_{DD} = +5 V, V_{SS} = −5 V, All $V_{IN}X$ = +3 V, T_A = −40°C to +85°C apply for DAC-8840F, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC ACCURACY		All Specifications Apply for DACs A, B, C, D, E, F, G, H				
Resolution	N		8			Bits
Integral Nonlinearity	INL			±1/4	±1	LSB
Differential Nonlinearity	DNL	All Devices Monotonic			±1	LSB
Output Offset	V_{BZE}	$\overline{PR}$ = 0, Sets D = 80_H		3	25	mV
Output Offset Drift	TCV_{BZ}	$\overline{PR}$ = 0, Sets D = 80_H		10		µV/°C
REFERENCE INPUTS		Applies to All Inputs $V_{IN}X$				
Voltage Range	IVR	Note 1	±3			V
Input Resistance	R_{IN}	D = $2B_H$, Code Dependent	3	6		kΩ
Input Capacitance	C_{IN}	D = FF_H, Code Dependent		19	30	pF
DAC OUTPUTS		Applies to All Outputs $V_{OUT}X$				
Voltage Range	OVR	R_L = 10 kΩ	±3			V
Output Current	I_{OUT}	ΔV_{OUT} <1 LSB	±5	±10		mA
Capacitive Load	C_L	No Oscillation			200	pF
DYNAMIC PERFORMANCE		Applies to All DACs				
Multiplying Gain Bandwidth	GBW	$V_{IN}X$ = 100 mV p–p	1	2.5		MHz
Slew Rate		Measured 10% to 90%				
Positive	SR+	$\Delta V_{OUT}X$= +6 V	1.3	4.0		V/µs
Negative	SR−	$\Delta V_{OUT}X$ = −6 V	1.3	2.5		V/µs
Total Harmonic Distortion	THD	$V_{IN}X$ = 4 V p–p, D = FF_H, f = 1 kHz, f_{LP} = 80 kHz		0.01		%
Spot Noise Voltage	e_N	f = 1 kHz		0.17		µV/√Hz
Output Settling Time	t_S	±1 LSB Error Band, D = 0 to FF_H		3.5	6	µs
Channel-to-Channel Crosstalk	C_T	Measured Between Adjacent Channels, f = 100 kHz	60	80		dB
Digital Feedthrough	Q	V_{INX} = 0 V, D = 0 to 255_{10}		6		nVs
POWER SUPPLIES						
Power Supply Current	I_{DD}	$\overline{PR}$ = 0 V		19	26	mA
Negative Supply Current	I_{SS}	$\overline{PR}$ = 0 V		19	26	mA
Power Dissipation	P_{DISS}			190	260	mW
DC Power Supply Rejection Ratio	PSRR	$\overline{PR}$ = 0 V, ΔV_{DD} = ±5%		0.0002	0.01	%/%
Power Supply Range	PSR	V_{DD}, $\|V_{SS}\|$	4.75	5.00	5.25	V
DIGITAL INPUTS						
Logic High	V_{IH}		2.4			V
Logic Low	V_{IL}				0.8	V
Input Current	I_L				±10	µA
Input Capacitance	C_{IL}			7	10	pF
Input Coding			Offset Binary			
DIGITAL OUTPUT						
Logic High	V_{OH}	I_{OH} = −0.4 mA	3.5			V
Logic Low	V_{OL}	I_{OL} = 1.6 mA			0.4	V

NOTE
[1]Maximum input voltage is always 2 V less than V_{DD}.
Specifications subject to change without notice.

TIMING SPECIFICATIONS (V_{DD} = +5 V, V_{SS} = −5 V, All $V_{IN}X$ = +3 V, T_A = −40°C to +85°C apply for DAC-8840F, unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Clock Pulse Width	t_{CH}, t_{CL}	80		ns
Data Setup Time	t_{DS}	40		ns
Data Hold Time	t_{DH}	20		ns
CLK to SDO Propagation Delay	t_{PD}		120	ns
DAC Register Load Pulse Width	t_{LD}	70		ns
Preset Pulse Width	t_{PR}	50		ns
Clock Edge to Load Time	t_{CKLD}	30		ns
Load Edge to Next Clock Edge	t_{LDCK}	60		ns

WAFER TEST LIMITS: (V_{DD} = +5 V, V_{SS} = −5 V, All $V_{IN}X$ = +3 V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	DAC8840GBC Limits	Units
Integral Nonlinearity	INL		±1	LSB max
Differential Nonlinearity	DNL	All Devices Monotonic	±1	LSB max
Output Offset	V_{BZE}	$\overline{PR}$ = 0, Sets D = 80_H	25	mV max
Input Resistance ($V_{IN}X$)	R_{IN}	D = $2B_H$; Code Dependent	3	kΩ min
DAC Output Voltage Range	OVR	R_L = 10 kΩ	±3	V min
DAC Output Current	I_{OUT}	ΔV_{OUT} < 1 LSB	±5	mA min
Slew Rate		Measured 10% to 90%		
Positive	SR+	$\Delta V_{OUT}X$ = +6 V	1.3	V/µs min
Negative	SR−	$\Delta V_{OUT}X$ = −6 V	1.3	V/µs min
Positive Supply Current	I_{DD}	$\overline{PR}$ = 0 V	26	mA max
Negative Supply Current	I_{SS}	$\overline{PR}$ = 0 V	26	mA max
DC Power Supply Rejection Ratio	PSRR	$\overline{PR}$ = 0 V, ΔV_{DD} = ±5%	0.01	%/% max
Logic Input High	V_{IH}		2.4	V min
Logic Input Low	V_{IL}		0.8	V max
Logic Input Current	I_L		±10	µA max
Logic Output High	V_{OH}	I_{OH} = −0.4 mA	3.5	V min
Logic Output Low	V_{OL}	I_{OL} = 1.6 mA	0.4	V max

NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

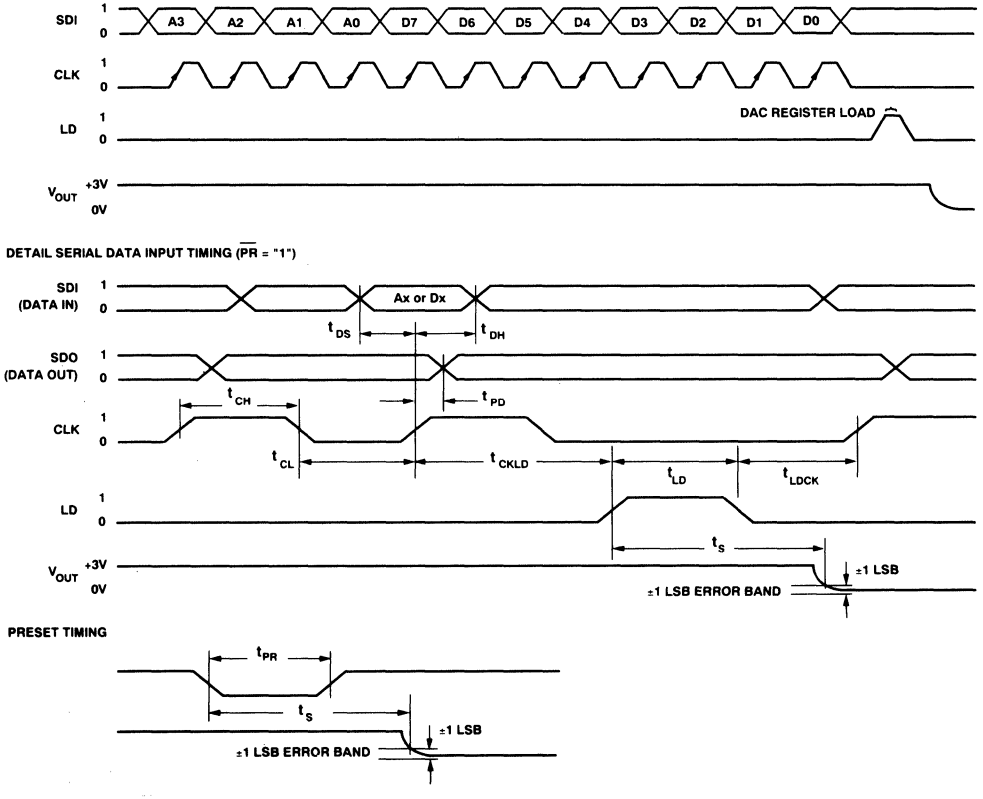
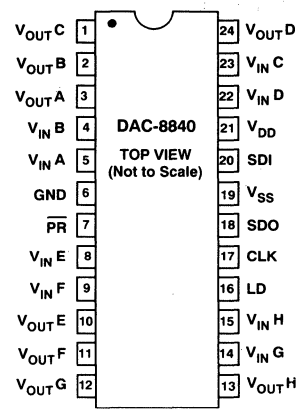


Figure 1. Timing Diagram

PIN DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	$V_{OUT}C$	DAC C Output
2	$V_{OUT}B$	DAC B Output
3	$V_{OUT}A$	DAC A Output
4	$V_{IN}B$	DAC B Reference Input
5	$V_{IN}A$	DAC A Reference Input
6	GND	Ground
7	$\overline{PR}$	Preset Input, Active Low, All DAC Registers = 80_H
8	$V_{IN}E$	DAC E Reference Input
9	$V_{IN}F$	DAC F Reference Input
10	$V_{OUT}E$	DAC E Output
11	$V_{OUT}F$	DAC F Output
12	$V_{OUT}G$	DAC G Output
13	$V_{OUT}H$	DAC H Output
14	$V_{IN}G$	DAC G Reference Input
15	$V_{IN}H$	DAC H Reference Input
16	LD	Load DAC Register Strobe, Active High Input That Transfers the Data Bits from the Serial Input Register into the Decoded DAC Register. See Table I.
17	CLK	Serial Clock Input, Positive Edge Triggered
18	SDO	Serial Data Output, Active Totem Pole Output
19	V_{SS}	Negative 5 V Power Supply
20	SDI	Serial Data Input
21	V_{DD}	Positive 5 V Power Supply
22	$V_{IN}D$	DAC D Reference Input
23	$V_{IN}C$	DAC C Reference Input
24	$V_{OUT}D$	DAC D Output

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted)

V_{DD} to GND . . . . . −0.3, +7 V
V_{SS} to GND . . . . . +0.3, −7 V
$V_{IN}X$ to GND . . . . . V_{DD}, V_{SS}
$V_{OUT}X$ to GND . . . . . V_{DD}, V_{SS}
Short Circuit $I_{OUT}X$ to GND . . . . . Continuous
Digital Input & Output Voltage to GND . . . . . V_{DD}, V_{SS}
Operating Temperature Range
Extended Industrial: DAC8840F . . . . . −40°C to +85°C
Maximum Junction Temperature (T_J max) . . . . . +150°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Package Power Dissipation . . . . . (T_J Max $-T_A$)/θ_{JA}
Thermal Resistance θ_{JA}
Cerdip . . . . . 64°C/W
P-DIP . . . . . 57°C/W
SOIC-24 . . . . . 70°C/W

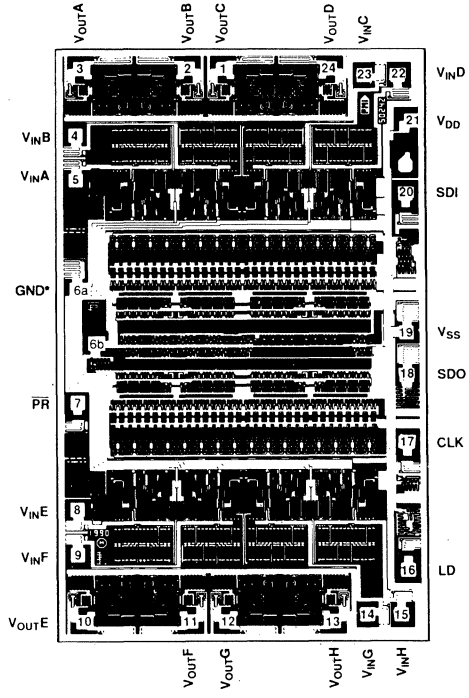
ORDERING GUIDE

Model	Temperature Range	Package Option
DAC8840FP	−40°C to +85°C	Plastic DIP
DAC8840FW	−40°C to +85°C	Cerdip
DAC8840FS	−40°C to +85°C	SOIC-24
DAC8840GBC	25°C	DICE

For devices processed in total compliance to MIL-STD 883, contact our local sales office for the DAC8840BW/883 datasheet.

DICE CHARACTERISTICS

DIE SIZE 0.117 × 0.185 inch, 21,645 sq. mils
(2.9718 × 4.699 mm, 13.964 sq. mm)
The die backside is electrically common to V_{DD}.



*BOTH GND PADS (6a, 6b) ARE BONDED TO PIN 6 OF PACKAGE.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

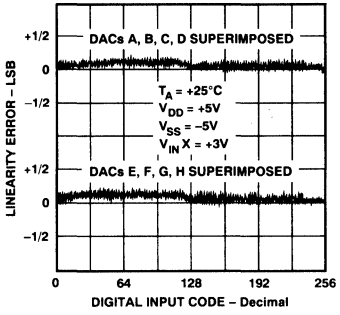


Figure 2. Linearity Error vs. Digital Input Code

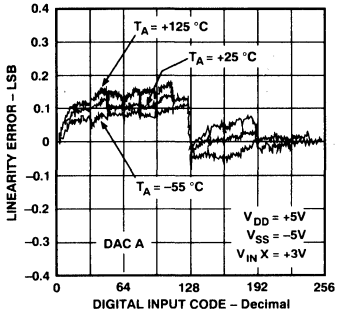


Figure 3. Linearity Error vs. Digital Code vs. Temperature

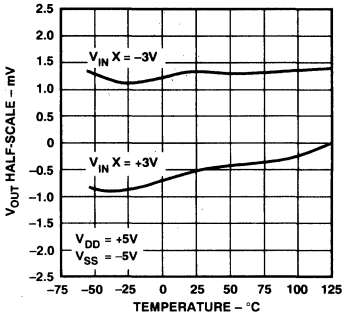


Figure 4. V_{OUT} Half-Scale (80_H) vs. Temperature

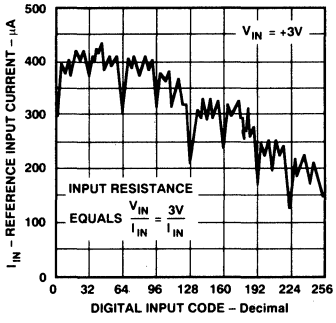


Figure 5. Input Resistance vs. Code

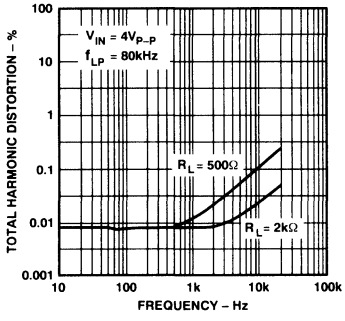


Figure 6. Total Harmonic Distortion vs. Frequency

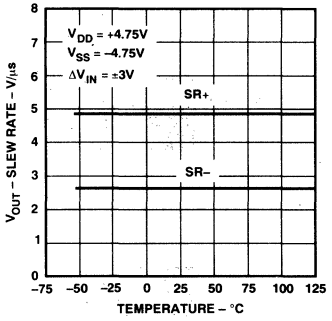


Figure 7. V_{OUT} Slew Rate vs. Temperature

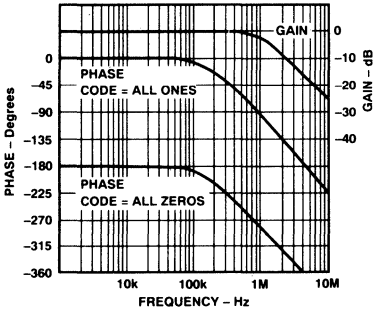


Figure 8. Gain and Phase vs. Frequency (Digital Input = 0 or 255_{10})

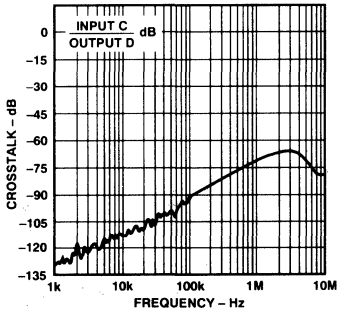


Figure 9. DAC Crosstalk vs. Frequency

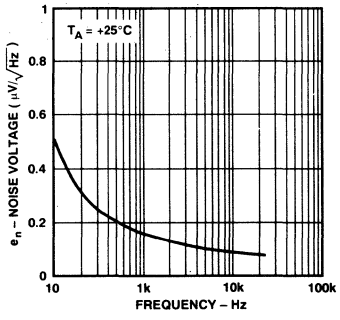


Figure 10. Voltage Noise Density vs. Frequency

8

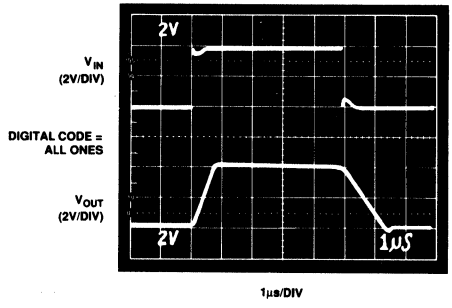


Figure 11. Pulse Response

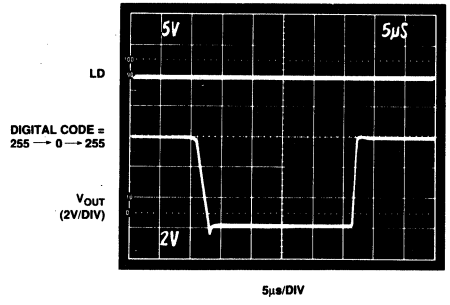


Figure 12. Settling Time

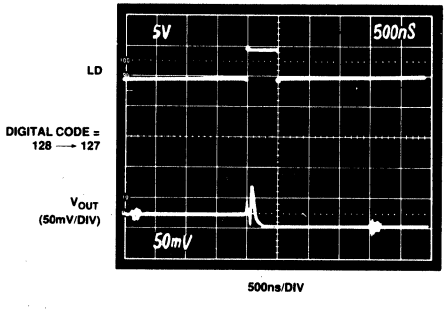


Figure 13. Worst Case 1 LSB Digital Step Change

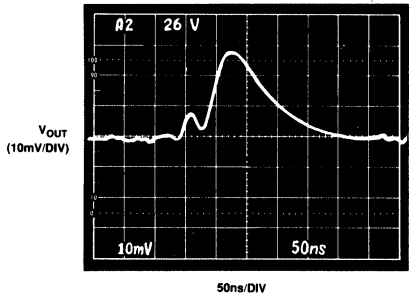


Figure 14. Digital Feedthrough

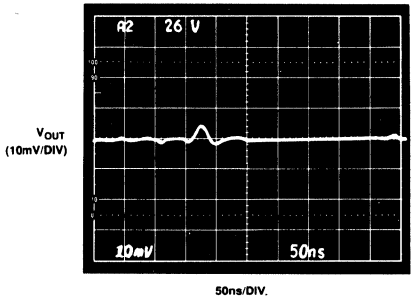


Figure 15. Digital Crosstalk

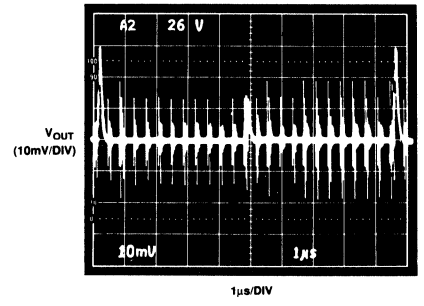


Figure 16. Clock Feedthrough

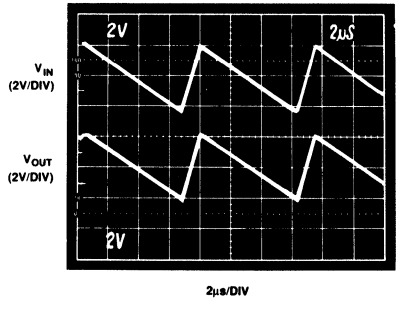


Figure 17. 128 kHz Sawtooth Waveform

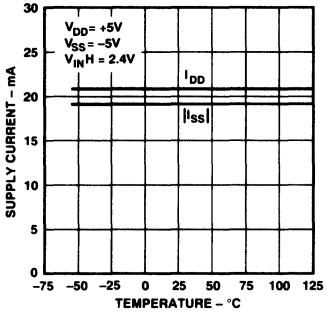


Figure 18. Supply Current vs. Temperature

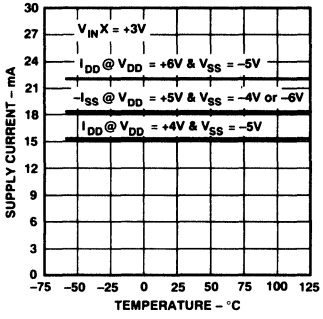


Figure 19. Supply Current vs. Supply Voltage vs. Temperature

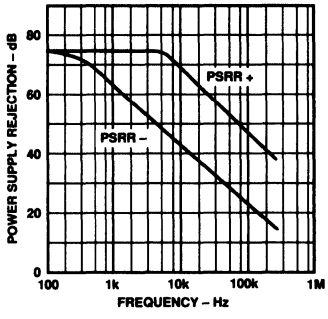


Figure 20. PSRR vs. Frequency

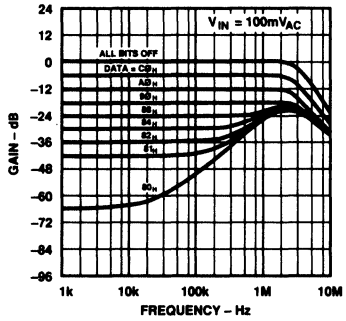


Figure 21. Gain (V_{OUT}/V_{IN}) and Feedthrough vs. Frequency

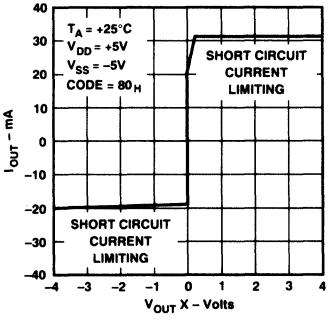


Figure 22. DAC Output Current vs. $V_{OUT}X$

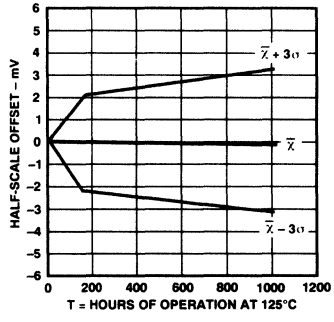


Figure 23. Output Drift Delta Accelerated by Burn-In

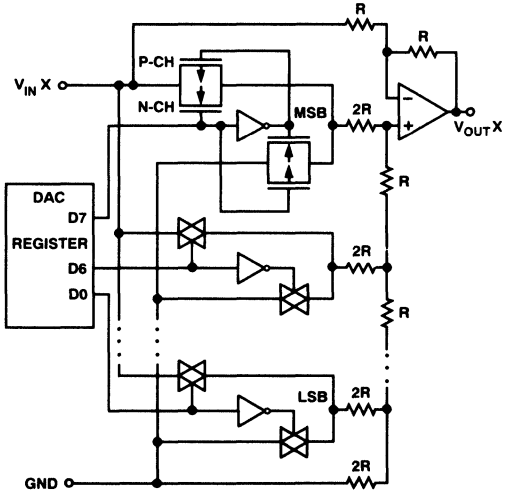


Figure 24. DAC-8840 TrimDAC Equivalent Circuit

Table I. Serial Input Decode

LAST → FIRST

LSB D0	D1	D2	D3	D4	D5	D6	MSB D7	LSB A0	A1	A2	MSB A3

DATA

ADDRESS

MSB A3	A2	A1	LSB A0	DAC Updated
0	0	0	0	No Operation
0	0	0	1	DAC A
0	0	1	0	DAC B
0	0	1	1	DAC C
0	1	0	0	DAC D
0	1	0	1	DAC E
0	1	1	0	DAC F
0	1	1	1	DAC G
1	0	0	0	DAC H
1	0	0	1	No Operation
⋮				⋮
1	1	1	1	No Operation

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	DAC Output Voltage VOUT = (D/128 –1) x VIN
0	0	0	0	0	0	0	0	–VIN
0	0	0	0	0	0	0	1	(1/128 –1) x VIN
				⋮				
0	1	1	1	1	1	1	1	(127/128 –1) x VIN
1	0	0	0	0	0	0	0	(128/128 –1) x VIN = 0V, (Preset Value)
1	0	0	0	0	0	0	1	(129/128 –1) x VIN
				⋮				
1	1	1	1	1	1	1	0	(254/128 –1) x VIN
1	1	1	1	1	1	1	1	(255/128 –1) x VIN = VIN

Table II. Logic Control Input Truth Table

SDI	CLK	LD	$\overline{PR}$	Input Shift Register Operation
X	L	L	H	No Operation
X		L	H	Shift One Bit In from SDI (Pin 20), Shift One Bit* Out from SDO (Pin 18)
X	X	L	L	All DAC Registers = 80_H
X	L	H	H	Load Serial Register Data into DAC(X) Register

*Data shifted into the SDI pin appears twelve clocks later at the SDO pin.

CIRCUIT OPERATION

The DAC-8840 is a general purpose multiple-channel ac or dc signal level adjustment device designed to replace potentiometers used in the three-terminal connection mode. Eight independent channels of programmable signal level control are available in this 24-pin package device. The outputs are completely buffered providing up to 5 mA of output drive-current to drive external loads. The DAC and amplifier combination shown in Figure 25 produces four-quadrant multiplication of the signal inputs applied to V_{IN} times the digital input control word. In addition, the DAC-8840 provides a 1 MHz gain-bandwidth product in the four-quadrant multiplying channel. Operating from plus and minus 5 V power supplies, analog inputs and outputs of ±3 V are easily accommodated.

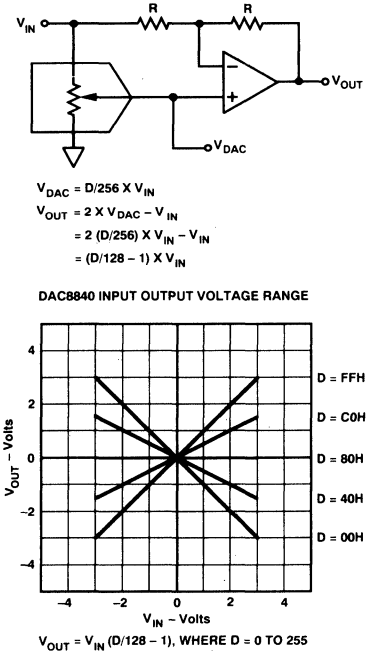


Figure 25. DAC Plus Amplifier Combine to Produce Four Quadrant Multiplication

In order to simplify use with a controlling microprocessor, a simple layout-efficient three-wire serial-data-interface was chosen. This interface can be easily adapted to almost all microcomputer and microprocessor systems. A clock (CLK), serial data input (SDI) and a load (LD) strobe pin make up the three-wire interface. The 12-bit input data word used to change the value of the internal DAC registers contains a 4-bit address and 8 bits of data. Using this word combination any DAC register can be changed at a given time without disturbing the other channels. A serial data output SDO pin simplifies cascading multiple DAC-8840s without adding address decoder chips to the system.

During system power up a logic low on the preset $\overline{PR}$ pin forces all DAC registers to 80_H which in turn forces all the buffer amplifier outputs to zero volts. This asynchronous input pin $\overline{PR}$ can be activated at any time to force the DAC registers to the half-scale code 80_H. This is generally the most convenient place to start general purpose adjustment procedures.

ADJUSTING AC OR DC SIGNAL LEVELS

The four quadrant multiplication operation of the DAC-8840 is shown in Figure 25. For dc operation the equation describing the relationship between V_{IN}, digital inputs and V_{OUT} is:

$$V_{OUT}(D) = (D/128 - 1) \times V_{IN} \quad (1)$$

where D is a decimal number between 0 and 255.

The actual output voltages generated with a fixed 3V dc input applied to V_{IN} are summarized in this table.

Table III.

Decimal Input (D)	V_{OUT}(D)	Comments (V_{IN} = 3 V)
0	−3.00 V	Inverted FS
1	−2.98	
127	−0.02	
128	0.00	Zero Output
129	0.02	
254	2.95	
255	2.98	Full Scale (FS)

Notice that the output polarity is the same as the input polarity when the DAC register is loaded with 255 (in binary = all ones). Also note that the output does not exactly equal the input voltage. This is a result of the R-2R ladder DAC architecture chosen. When the DAC register is loaded with 0, the output polarity is inverted and exactly equals the magnitude of the input voltage V_{IN}. The actual voltage measured when setting up a DAC in this example will vary within the ±1 LSB linearity error specification of the DAC-8840. The calculated voltage error would be ±0.023 V (= ±3 V/128).

If V_{IN} is an ac signal such as a sine wave then we can use equation 2 to describe circuit performance.

$$V_{OUT}(t,D) = (D/128 - 1) \times A \sin(\omega t) \quad (2)$$

where $\omega = 2\pi f$, A = sine wave amplitude, and D = decimal input code.

This transfer characteristic Equation 2 lends itself to amplitude and phase control of the incoming signal V_{IN}. When the DAC is loaded with all zeros, the output sine wave is shifted by 180° with respect to the input sine wave. This powerful multiplying capability can be used for a wide variety of modulation, waveform adjustment and amplitude control.

8

REFERENCE INPUTS (V_{IN}A, B, C, D, E, F, G, H)

The eight independent V_{IN} inputs have a code dependent input resistance whose worst case minimum value 3 kΩ is specified in the electrical characteristics table. The graph (Figure 5) titled "Reference Input Current versus Code" shown in the typical performance characteristics section displays the incremental changes. Use a suitable amplifier capable of driving this input resistance in parallel with the specified 19 pF typical input capacitance. These reference inputs are designed to receive not only dc, but ac input voltages. This results from the incorporation of a true bilateral analog switch in the DAC design (see Figure 24). The DAC switch operation has been designed to operate in the break-before-make format to minimize transient loading of the inputs. The reference input voltage range can operate from near the negative supply (V_{SS}) to within 2 V of the positive supply (V_{DD}). That is, the operating input voltage range is:

$$V_{SS} + 0.5\ V < V_{IN}X < (V_{DD}-2\ V) \qquad (3)$$

DAC OUTPUTS (V_{OUT}A, B, C, D, E, F, G, H)

The eight D/A converter outputs are fully buffered by the DAC-8840's internal amplifier. This amplifier is designed to drive up to 1 kΩ loads in parallel with 100 pF. However, in order to minimize internal device power consumption, it is recommended whenever possible to use larger values of load resistance. The amplifier output stage can handle shorts to GND; however, care should be taken to avoid continuous short circuit operation.

The low output impedance of the buffers minimizes crosstalk between analog input channels. A graph (Figure 9) of analog crosstalk between channels is provided in the typical performance characteristics section. At 1 MHz, 72 dB of channel-to-channel isolation exists. It is recommended to use good circuit layout practice such as guard traces between analog channels and power supply bypass capacitors. A 0.01 μF ceramic in parallel with a 1–10 μF tantulum capacitor provides a good power supply bypass for most frequencies encountered.

DIGITAL INTERFACING

The four digital input pins (CLK, SDI, LD, $\overline{PR}$) of the DAC-8840 were designed for TTL and 5 V CMOS logic compatibility. The SDO output pin offers good fanout in CMOS logic applications and can easily drive several DAC-8840s.

The Logic Control input Truth Table II describes how to shift data into the internal 12-bit serial input register. Note that the CLK is a positive edge sensitive input. If mechanical switches are used for breadboarding product evaluation, they should be debounced by a flipflop or other suitable means.

The required address plus data input format is defined in the serial input decode Table I. Note there are 8 address states that result in no operation (NOP) or activity in the DAC-8840 when the active high load strobe LD is activated. This NOP can be used in cascaded applications where only one DAC out of several packages needs updating. The packages not requiring data changes would receive the NOP address, that is, all zeros. It takes 12 clocks on the CLK pin to fully load the serial input shift register. Data on the SDI input pin is subject to the timing diagram (Figure 1) data setup and data hold time requirements. After the twelfth clock pulse the processor needs to activate the LD strobe to have the DAC-8840 decode the serial register contents and update the target DAC register with the 8-bit data word. This needs to be done before the thirteenth positive clock edge. The timing requirements are provided in the electrical characteristic table and in the Figure 1 timing diagram. After twelve clock edges, data initially loaded into the shift register at SDI appears at the shift register output SDO.

There is some digital feedthrough from the digital input pins. Operating the clock only when the DAC registers require updating minimizes the effect of the digital feedthrough on the analog signal channels. Measurements of DAC switch feedthrough shown in the electrical characteristics table were accomplished by grounding the V_{IN}X inputs and cycling the data codes between all zeros and all ones. Under this condition 6 nVs of feedthrough was measured on the output of the switched DAC channel. An adjacent channel measured less than 1 nVs of digital crosstalk. The digital feedthrough photographs shown in the typical performance characteristics section displays these characteristics (Figures 14, 15, and 16).

Figure 26 shows a three-wire interface for a single DAC-8840 that easily cascades for multiple packages.

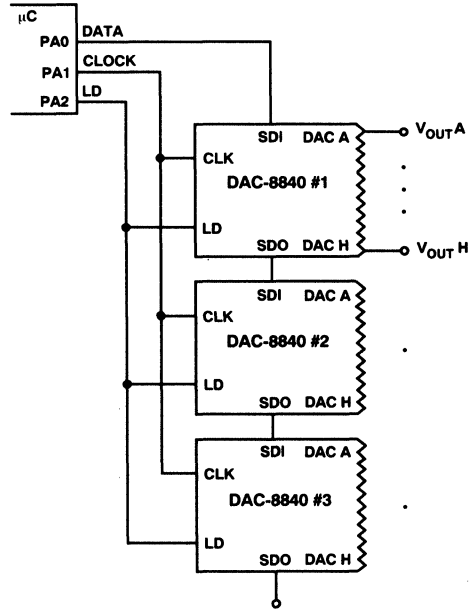


Figure 26. Three-Wire Interface Updates Multiple DAC-8840s

8-Bit Octal, 2-Quadrant Multiplying, CMOS TrimDAC

DAC-8841

FEATURES
Replaces 8 Potentiometers
Operates From Single +5 V Supply
1 MHz 2-Quadrant Multiplying Bandwidth
No Signal Inversion
Eight Individual Channels
3-Wire Serial Input
500 kHz Update Data Loading Rate
+3 Volt Output Swing
Midscale Preset
Low 95 mW Power Dissipation

APPLICATIONS
Trimmer Replacement
Dynamic Level Adjustment
Special Waveform Generation and Modulation
Programmable Gain Amplifiers

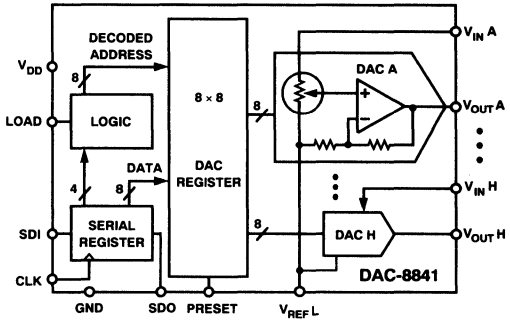
GENERAL DESCRIPTION

The DAC-8841 provides eight general purpose digitally controlled voltage adjustment devices. The TrimDAC™ capability replaces the mechanical trimmer function in new designs. It is ideal for ac or dc gain control of up to 1 MHz bandwidth signals.

Internally the DAC-8841 contains eight voltage output CMOS digital-to-analog converters, each with separate reference inputs. Each DAC has its own DAC register which holds its output state. These DAC registers are updated from an internal serial-to-parallel shift register which is loaded from a standard 3-wire serial input digital interface. Twelve data bits make up the data word clocked into the serial input register. This data word is decoded where the first 4 bits determine the address of the DAC register to be loaded with the last 8 bits of data. A serial data output pin at the opposite end of the serial register allows simple daisy-chaining in multiple DAC applications without additional external decoding logic.

TrimDAC is a trademark of Analog Devices, Inc.

FUNCTIONAL BLOCK DIAGRAM



The DAC-8841 consumes only 95 mW from a +5 V power supply. For dual polarity applications see the DAC-8840 which provides full 4-quadrant-multiplying ±3 V signal capability while operating from ±5 V power supplies.

The DAC-8841 is available in 24-pin plastic DIP, cerdip, and SOIC-24 packages. For MIL-STD/883 applications, contact ADI sales for the DAC-8841BW/883 data sheet which specifies operation over −55°C to +125°C.

8

DAC-8841—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{DD} = +5 V, All $V_{IN}X$ = +1.5 V, $V_{REF}L$ = 0V, T_A = −40°C to +85°C apply for DAC-8841F, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC ACCURACY		All Specifications Apply for DACs A, B, C, D, E, F, G, H				
Resolution	N		8			Bits
Integral Nonlinearity	INL	Note 1		±1/2	±1.5	LSB
Differential Nonlinearity	DNL	All Devices Monotonic, Note 1			±1	LSB
Half-Scale Output Voltage	V_{HS}	$\overline{PR}$ = 0 V, Sets D = 80_H	1.475	1.500	1.525	V
Zero-Scale Output Voltage	V_{ZS}	Digital Code = 00_H		20	100	mV
Output Voltage Drift	TCV_{HS}	$\overline{PR}$ = 0 V, Sets D = 80_H		10		μV/°C
SIGNAL INPUTS		Applies to All Inputs $V_{IN}X$ or $V_{REF}L$				
Input Voltage Range	IVR		0		1.5	V
Input Resistance	R_{IN}	D = 55_H; Code Dependent	4	10		kΩ
Input Capacitance	C_{IN}	Code Dependent		19	30	pF
REF Low Resistance	$R_{REF}L$	D = AB_H; Code Dependent	0.3	0.75		kΩ
REF Low Capacitance	$C_{REF}L$	Code Dependent		190	250	pF
DAC OUTPUTS		Applies to All Outputs $V_{OUT}X$				
Voltage Range	OVR	R_L = 10 kΩ	0		3	V
Output Current	I_{OUT}	ΔV_{OUT} < 25 mV, $V_{IN}X$ = 1.375V, $\overline{PR}$ = 0 V	±5	7		mA
Capacitive Load	C_L	No Oscillation			200	pF
DYNAMIC PERFORMANCE		Applies to All DACs				
Multiplying Gain Bandwidth	GBW	$V_{IN}X$ = 100 mV p-p + 1.0 V dc	1	2.5		MHz
Slew Rate		Measured 10% to 90%				
	+SR	$\Delta V_{OUT}X$ = +3 V	1.3	4.0		V/μs
	−SR	$\Delta V_{OUT}X$ = −3 V	1.3	2.5		V/μs
Total Harmonic Distortion	THD	$V_{IN}X$ = 1 V p-p + 1.0 V dc, D = FF_H, f = 1 kHz, f_{LP} = 80 kHz		0.01		%
Spot Noise Voltage	e_N	f = 1 kHz		0.17		μV/√Hz
Output Settling Time	t_S	±1 LSB Error Band, 8_{10} to 255_{10}		3.5	6	μs
Channel to Channel Crosstalk	C_T	Measured Between Adjacent Channels, f = 100 kHz	60	70		dB
Digital Feedthrough	Q	$V_{REF}L$ = +1.5 V, D = 0 to FF_H		6		nVs
POWER SUPPLIES						
Positive Supply Current	I_{DD}	$\overline{PR}$ = 0 V		19	26	mA
Power Dissipation	P_{DISS}			95	130	mW
DC Power Supply Rejection Ratio	PSRR	$\overline{PR}$ = 0 V			0.01	%/%
Power Supply Range	PSR	V_{DD}	4.75	5.00	5.25	V
DIGITAL INPUTS						
Logic High	V_{IH}		2.4			V
Logic Low	V_{IL}				0.8	V
Input Current	I_L				±10	μA
Input Capacitance	C_{IL}				8	pF
Input Coding				Binary		
DIGITAL OUTPUT						
Logic High	V_{OH}	I_{OH} = −0.4 mA	3.5			V
Logic Low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
TIMING SPECIFICATIONS						
Input Clock Pulse Width	t_{CH}, t_{CL}		80			ns
Data Setup Time	t_{DS}		40			ns
Data Hold Time	t_{DH}		20			ns
CLK to SDO Propagation Delay	t_{PD}				120	ns
DAC Register Load Pulse Width	t_{LD}		70			ns
Preset Pulse Width	t_{PR}		50			ns
Clock Edge to Load Time	t_{CKLD}		30			ns
Load Edge to Next Clock Edge	t_{LDCK}		60			ns

NOTE

[1]INL and DNL tests do not include operation at codes 0 thru 7 due to zero-scale output voltage. For bias voltages above 100 mV on $V_{REF}L$, INL and DNL are maintained over all codes.

Specifications subject to change without notice.

WAFER TEST LIMITS: V_{DD} = +5 V, All $V_{IN}X$ = +1.5 V, $V_{REF}L$ = 0 V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	DAC-8841GBC Limits	Units
Integral Nonlinearity	INL	Note 1	±1.5	LSB max
Differential Nonlinearity	DNL	All Devices Monotonic, Note 1	±1	LSB max
Half-Scale Output Voltage	V_{HS}	$\overline{PR}$ = 0 V, Sets D = 80_H	1.475/1.525	V min/max
Input Resistance ($V_{IN}X$)	R_{IN}	D = 55_H; Code Dependent	4	kΩ min
REF Low Resistance	$R_{REF}L$	D = AB_H; Code Dependent	0.3	kΩ min
DAC Output Voltage Range	OVR	R_L = 10 kΩ	3	V min
DAC Output Current	I_{OUT}	ΔV_{OUT} < 25 mV	±5	mA min
Slew Rate		Measured 10% to 90%		
Positive	SR+	$\Delta V_{OUT}X$ = +3 V	1.3	V/μs min
Negative	SR−	$\Delta V_{OUT}X$ = −3 V	1.3	V/μs min
Positive Supply Current	I_{DD}	$\overline{PR}$ = 0 V	26	mA max
DC Power Supply Rejection Ratio	PSRR	$\overline{PR}$ = 0 V, ΔV_{DD} = ±5%	0.01	%/% max
Logic Input High	V_{IH}		2.4	V min
Logic Input Low	V_{IL}		0.8	V max
Logic Input Current	I_L		±10	μA max
Logic Output High	V_{OH}	I_{OH} = −0.4 mA	3.5	V min
Logic Output Low	V_{OL}	I_{OL} = 1.6 mA	0.4	V max

NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

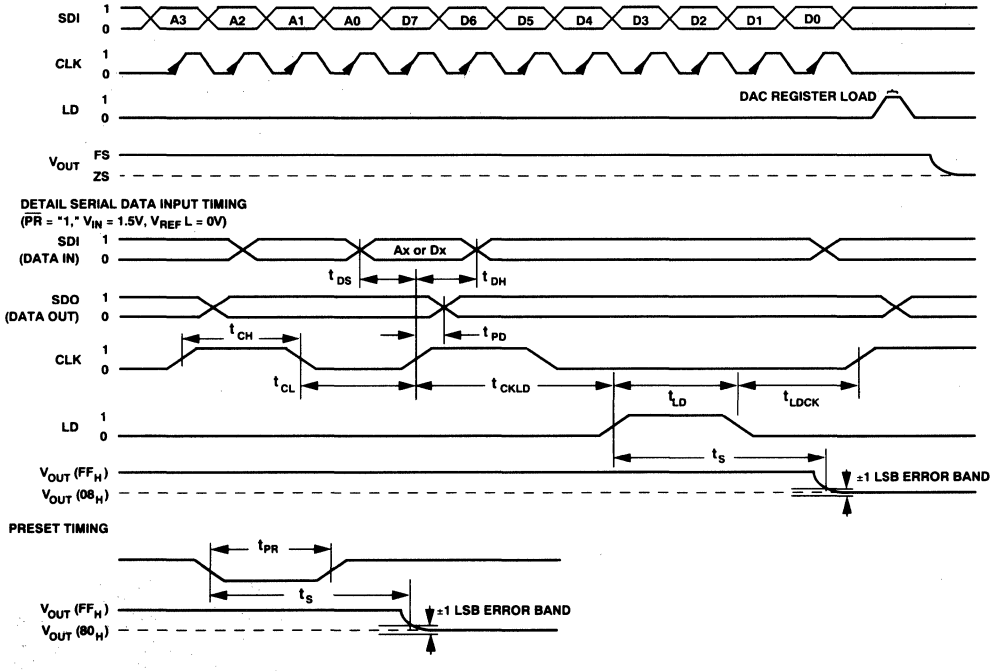


Figure 1. Timing Diagram

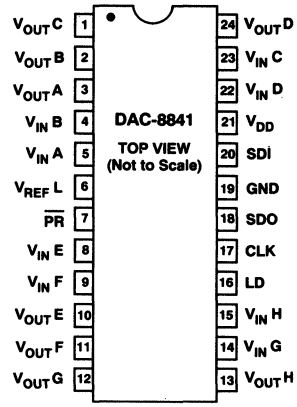
DAC-8841

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted)

V_{DD} to GND ..... −0.3 V, +7 V
V_{IN}X to GND ..... V_{DD}
V_{REF}L to GND ..... V_{DD}
V_{OUT}X to GND ..... V_{DD}
Short Circuit I_{OUT}X to GND ..... Continuous
Digital Input & Output Voltage to GND ..... V_{DD}
Operating Temperature Range
Extended Industrial: DAC-8841F ..... −40°C to +85°C
Maximum Junction Temperature (T_J max) ..... +150°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation ..... (T_J Max − T_A)/θ_{JA}
Thermal Resistance θ_{JA}
Cerdip ..... 64°C/W
P-DIP ..... 57°C/W
SOIC-24 ..... 70°C/W

PIN CONFIGURATIONS

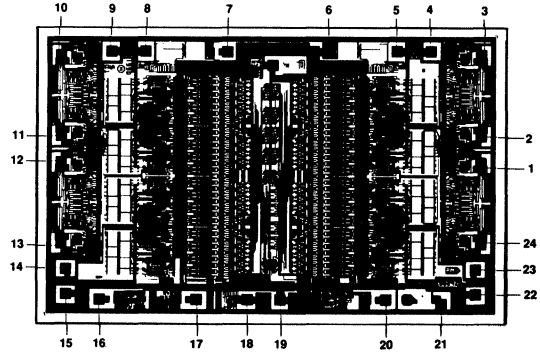


DAC-8841 PIN DESCRIPTION

Pin	Mnemonic	Description
1	V_{OUT}C	DAC C Output
2	V_{OUT}B	DAC B Output
3	V_{OUT}A	DAC A Output
4	V_{IN}B	DAC B Reference Input
5	V_{IN}A	DAC A Reference Input
6	$\overline{V_{REF}}$L	DAC Input Reference Low
7	$\overline{PR}$	Preset Input, Active Low, All DAC Registers = 80_H
8	V_{IN}E	DAC E Reference Input
9	V_{IN}F	DAC F Reference Input
10	V_{OUT}E	DAC E Output
11	V_{OUT}F	DAC F Output
12	V_{OUT}G	DAC G Output
13	V_{OUT}H	DAC H Output
14	V_{IN}G	DAC G Reference Input
15	V_{IN}H	DAC H Reference Input
16	LD	Load DAC Register Strobe, Active High Input that Transfers the Data Bits from the Serial Input Register into the Decoded DAC Register. See Table I
17	CLK	Serial Clock Input, Positive Edge Triggered
18	SDO	Serial Data Output, Active Totem Pole Output
19	GND	Ground
20	SDI	Serial Data Input
21	V_{DD}	Positive 5 V Power Supply
22	V_{IN}D	DAC D Reference Input
23	V_{IN}C	DAC C Reference Input
24	V_{OUT}D	DAC D Output

DICE CHARACTERISTICS

DIE SIZE 0.117 × 0.185 inch, 21,645 sq. mils
(2.9718 × 4.699 mm, 13.964 sq. mm)
The die backside is electrically common to V_{DD}.



1. V_{OUT}C	13. V_{OUT}H
2. V_{OUT}B	14. V_{IN}G
3. V_{OUT}A	15. V_{IN}H
4. V_{IN}B	16. LD
5. V_{IN}A	17. CLK
6. $\overline{V_{REF}}$L	18. SDO
7. PR	19. GND
8. V_{IN}E	20. SDI
9. V_{IN}F	21. V_{DD}
10. V_{OUT}E	22. V_{IN}D
11. V_{OUT}F	23. V_{IN}C
12. V_{OUT}G	24. V_{OUT}D

CAUTION

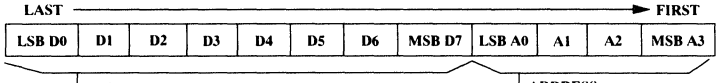
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

ORDERING GUIDE

Model	Temperature Range	Package Option
DAC8841FP	−40°C to +85°C	Plastic DIP
DAC8841FW	−40°C to +85°C	Cerdip
DAC8841FS	−40°C to +85°C	SOIC
DAC8841GBC	−25°C	Dice

For devices processed in total compliance to MIL-STD 883, contact your local sales office for the DAC8841BW/883 data sheet.

Table I. Serial Input Decode Table



MSB A3	A2	A1	LSB A0	DAC Updated
0	0	0	0	No Operation
0	0	0	1	DAC A
0	0	1	0	DAC B
0	0	1	1	DAC C
0	1	0	0	DAC D
0	1	0	1	DAC E
0	1	1	0	DAC F
0	1	1	1	DAC G
1	0	0	0	DAC H
1	0	0	1	No Operation
⋮				⋮
1	1	1	1	No Operation

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	DAC Output Voltage VOUT = D/128 (VIN – VREFL) + VREFL
0	0	0	0	0	0	0	0	VREFL
0	0	0	0	0	0	0	1	1/128 (VIN – VREFL) + VREFL
⋮								⋮
0	1	1	1	1	1	1	1	127/128 (VIN – VREFL) + VREFL
1	0	0	0	0	0	0	0	VIN (Preset Value)
1	0	0	0	0	0	0	1	129/128 (VIN – VREFL) + VREFL
⋮								⋮
1	1	1	1	1	1	1	0	254/128 (VIN – VREFL) + VREFL
1	1	1	1	1	1	1	1	255/128 (VIN – VREFL) + VREFL

Table II. Logic Control Input Truth Table

SDI	CLK	LD	$\overline{PR}$	Input Shift Register Operation
X	L	L	H	No Operation
X		L	H	Shift One Bit In from SDI (Pin 20), Shift One Bit* Out from SDO (Pin 18)
X	X	L	L	All DAC Registers = 80_H
X	L	H	H	Load Serial Register Data into DAC(X) Register

*Data shifted into the SDI pin appears twelve clocks later at the SDO pin.

8

DAC-8841—Typical Performance Characteristics

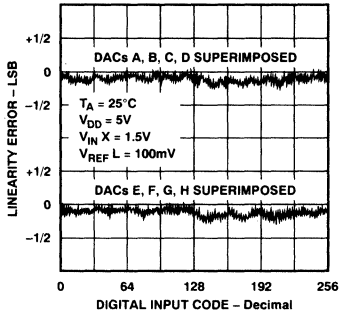


Figure 2. Linearity Error vs. Digital Input Code

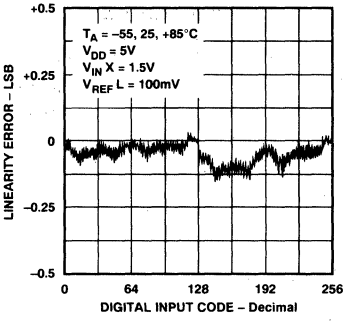


Figure 3. Linearity Error vs. Digital Code vs. Temperature

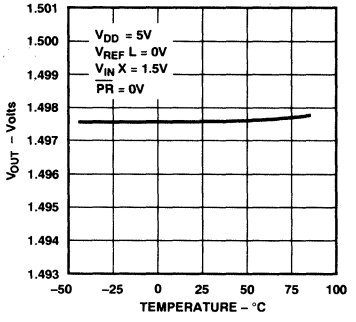


Figure 4. Half Scale vs. Temperature

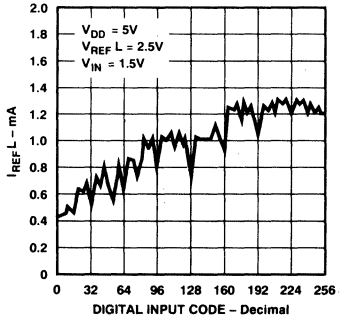


Figure 5. I_{REF}L Input Current vs. Digital Code

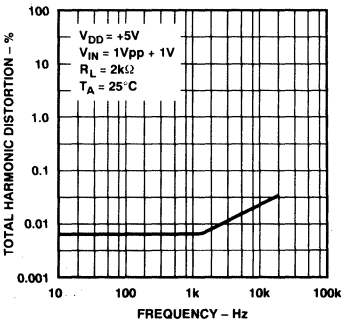


Figure 6. Total Harmonic Distortion vs. Frequency

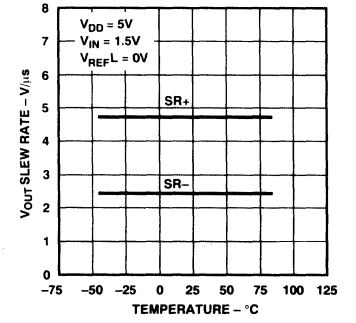


Figure 7. V_{OUT} Slew Rate vs. Temperature

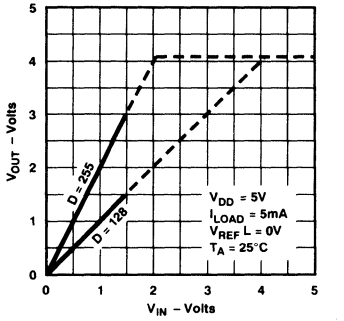


Figure 8. Full-Scale Output to Positive Saturation

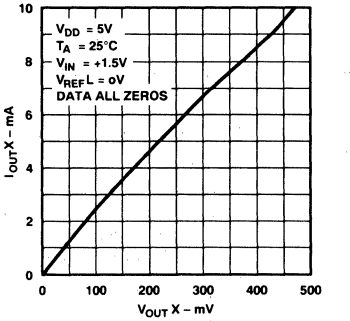


Figure 9. Zero-Scale Output Detail

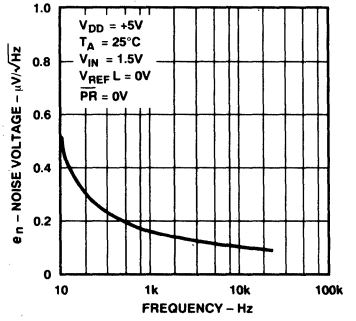


Figure 10. Voltage Noise Density vs. Frequency

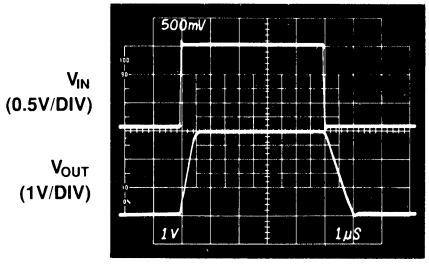


Figure 11. Pulse Response

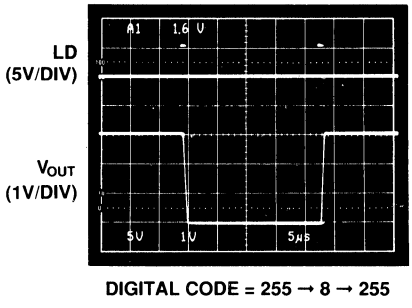


Figure 12. Settling Time

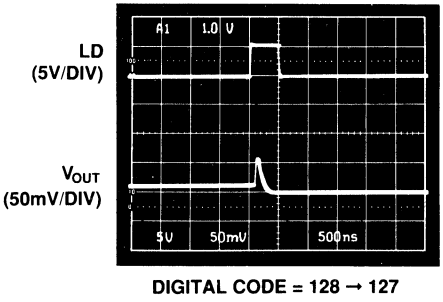


Figure 13. Worst Case 1 LSB Digital Step Change

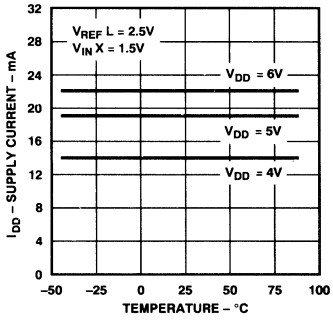


Figure 14. Supply Current vs. Temperature

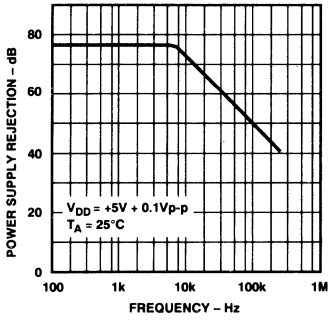


Figure 15. PSRR vs. Frequency

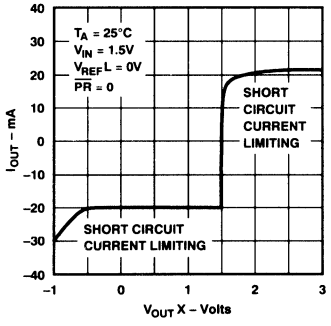


Figure 16. DAC Output Current vs. $V_{OUT}X$

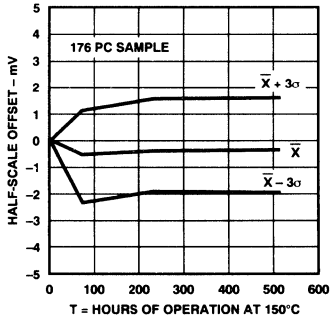


Figure 17. Output Drift Delta Accelerated by Burn-In

CIRCUIT OPERATION

The DAC-8841 is a general purpose multiple-channel ac or dc signal level adjustment device designed to replace potentiometers used in the three-terminal connection mode. Eight independent channels of programmable signal level control are available in this 24-pin package device. The outputs are completely buffered providing up to 5 mA of drive current to drive external loads. The DAC and amplifier combination shown in Figure 18 produces two-quadrant multiplication of the signal inputs applied to V_{IN} times the digital input control word. In addition the DAC-8841 provides a 1 MHz gain-bandwidth product in the two-quadrant multiplying channel. Operating from a 5 V power supply, analog inputs to +1.5 V which generate outputs to +3 V are easily accommodated.

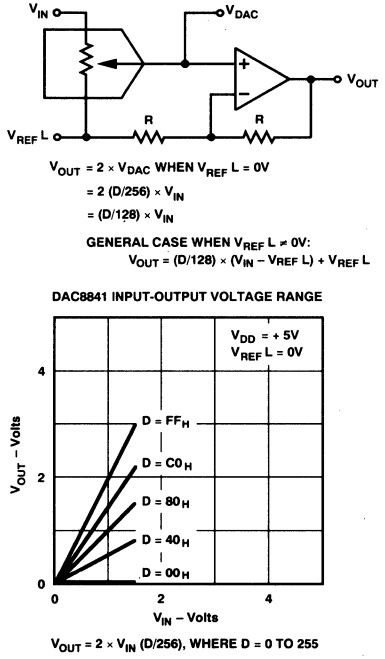


Figure 18. DAC Plus Amplifier Combine to Produce Two-Quadrant Multiplication

In order to be easy to use with a controlling microprocessor, a simple layout-efficient three-wire serial data interface was chosen. This interface can be easily adapted to almost all microcomputer and microprocessor systems. A clock (CLK), serial data input (SDI) and a load (LD) strobe pin make up the three-wire interface. The 12-bit input data word used to change the value of the internal DAC registers contains a 4-bit address and 8-bits of data. Using this combination, any DAC register can be changed without disturbing the other devices. A serial data output (SDO) pin simplifies cascading multiple DAC-8841s without adding address decoder chips to the system.

During system power up a logic low on the preset $\overline{PR}$ pin forces all DAC registers to 80_H which in turn forces all the buffer amplifier outputs to equal half-scale. The transfer equation (1) shows that in the preset condition (80_H) that V_{OUT} will equal V_{IN}. The asynchronous $\overline{PR}$ input pin can be activated at any time to force the DAC registers to the half-scale code 80_H. This is generally the most convenient place to start for general purpose adjustment applications.

ADJUSTING AC OR DC SIGNAL LEVELS

The two-quadrant multiplication operation of the DAC-8841 is shown in Figure 18. For dc operation the equation describing the relationship between V_{IN}, digital inputs and V_{OUT} is:

$$V_{OUT}(D) = (D/128) \times (V_{IN} - V_{REF}L) + V_{REF}L \qquad (1)$$

where D is a decimal number between 0 and 255.

The actual output voltages generated with a fixed 1.5 V dc input on V_{IN} and $V_{REF}L$ = 0 V are summarized in this table.

Decimal Input (D)	$V_{OUT}(D)$	Comments (V_{IN} = 1.5 V, $V_{REF}L$ = 0 V)
0	0.000 V*	Zero Scale
1	0.012*	
2	0.024*	
127	1.488	
128	1.500	Half Scale = V_{IN}
129	1.512	
254	2.976	
255	2.988	Full Scale (FS) ≈ 2 × V_{IN}

*See "Operation Near Ground."

Notice that the output polarity is the same as the input polarity when the DAC register is loaded with 255 (in binary = all ones). Also note that the output does not exactly equal two times the input voltage. This is a result of the R-2R ladder DAC chosen. When the DAC register is loaded with 0, the output is $V_{REF}L$. The actual voltage measured when setting up a DAC in this example will vary within the ±1 LSB linearity error specification of the DAC-8841. The actual voltage error would be ±0.012 V.

Operation Near ground – The input stage of the internal buffer amplifier functions down to ground, but the output stage cannot pull lower than the internal ground voltage. When a DAC output tries to output a voltage at or below the internal ground potential, it saturates and appears like a 50 Ω resistor to ground. The typical saturation voltage appearing at the output is 20 mV, see Figure 9. The 100 mV worst case zero-scale voltage specification reflects this saturation effect, including the worst case anticipated variation of the internal ground resistances, quiescent currents and buffer sinking current. Linearity is measured between code 8_{10} and code 255_{10} to avoid this saturation effect. In summary, the transfer function of each DAC will be a straight line from code 8 to code 255 when $V_{REF}L$ = 0 V. For input codes 0 to 7, some DAC outputs will be saturated in the zero-scale output voltage region; therefore, changing digital code 0 to 1 may not change the output voltage when $V_{REF}L$ = 0 V.

SIGNAL INPUTS (V_{IN}A, B, C, D, E, F, G, H)

The eight independent V_{IN} inputs have a code dependent input resistance whose worst case minimum value is specified in the electrical characteristics table. Use a suitable amplifier capable of driving this input resistance in parallel with the specified input capacitance. These reference inputs are designed to receive not only dc, but ac input voltages. This results from the incorporation of a true bilateral analog switch in the DAC design, see Figure 19. The DAC switch operation has been designed to operate in the break-before-make format to minimize transient loading of the inputs. The reference input voltage range can operate from ground (GND) to 1.5 V. That is, the operating input voltage range, when $V_{REF}L$ = 0 V, is:

$$0\ V < V_{IN}X < 1.5\ V \qquad (2)$$

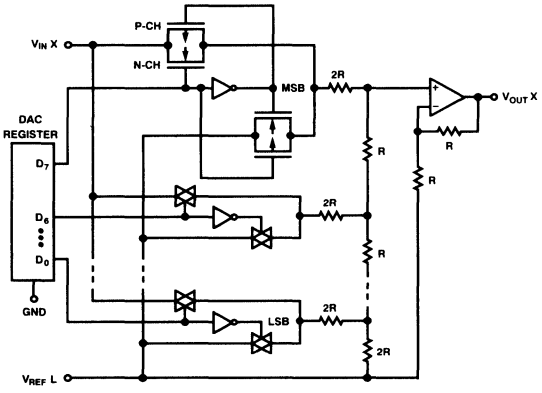


Figure 19. DAC-8841 TrimDAC Equivalent Circuit (One Channel)

The reference inputs can withstand input voltages up to V_{DD}; however due to the internal amplifier's gain of two configuration, the output voltage of the circuit reaches its maximum specified value of 3 V when the input voltage equals 1.5 V and $V_{REF}L$ = 0 V; see Figure 18.

The reference low input $V_{REF}L$ is the bottom end of the DAC (see Figure 18). This input is normally tied to ground; however it can be biased above ground. When $V_{REF}L$ is biased above ground, its value and that of $V_{IN}X$ should be chosen in agreement with Equation 3.

$$V_{OUT} \leq V_{DD} - 2\ V \qquad (3)$$

Also for the general case the headroom restriction to V_{DD} for $V_{IN}X$ and $V_{REF}L$ is given by Equation 4.

$$V_{IN}X,\ V_{REF}L \leq V_{DD} - 2\ V \qquad (4)$$

According to the above equations, the DAC-8841 can only be operated under certain combinations of $V_{IN}X$ and $V_{REF}L$. The shaded area in Figure 20 defines the theoretical allowable ranges of operation. Note that $V_{REF}L$ can be biased higher than $V_{IN}X$. Linearity will vary with the reference voltages and supply conditions. If a symmetrical output ac signal is desired, then the symmetrical ac input on $V_{IN}X$ should be offset to $V_{REF}L$. The output signal will then be with respect to $V_{REF}L$.

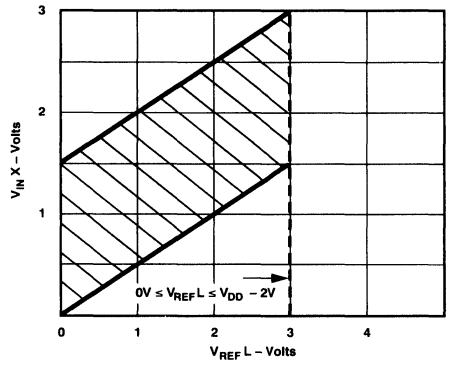


Figure 20. DAC-8841 Input Voltage Operating Boundaries

For example, biasing $V_{REF}L$ equal to one volt would accept a 1 V p–p ac input signal on V_{IN}. This input signal could then be attenuated or given a gain-of-two depending on the DAC data setting.

DAC OUTPUTS (V_{OUT}A, B, C, D, E, F, G, H)

The eight D/A converter outputs are fully buffered by the DAC-8841s internal amplifier. This amplifier is designed to drive up to 1 kΩ loads in parallel with 200 pF. However in order to minimize internal device power consumption, it is recommended whenever possible to use larger values of load resistance. The amplifier output stage can handle shorts to GND; however, care should be taken to avoid continuous short circuit operation. See Figure 16 "DAC output current versus $V_{OUT}X$" graph.

The amplifier output is guaranteed to operate to within 2 V of V_{DD} under all load conditions and temperature. Figure 8 shows typical operation to positive output saturation with a 5 mA load.

The low output impedance of the buffers minimizes crosstalk between analog input channels. At 100 kHz 70 dB of channel-to-channel isolation exists. It is recommended to use good circuit layout practice such as guard traces between analog channels and power supply bypass capacitors. A 0.01 μF ceramic in parallel with a 1–10 μF tantulum capacitor provides a good power supply bypass for most frequencies encountered.

DIGITAL INTERFACING

The four digital input pins (CLK, SDI, LD, $\overline{PR}$) of the DAC-8841 were designed for TTL and 5 V CMOS logic compatibility. The SDO output pin offers good fanout in CMOS logic applications and can easily drive several DAC-8841s.

The Logic Control Input Truth Table II describes how to shift data into the internal 12-bit serial input register. Note that the CLK is a positive edge-sensitive input. If mechanical switches are used for breadboard, product evaluation they should be debounced by a flipflop or other suitable means.

The required address plus data input format is defined in the Serial Input Decode Table I. Note there are 8 address states that result in no operation (NOP) or activity in the DAC-8841 when the active high load strobe LD is activated. This NOP can be used in cascaded applications where only one DAC out of several packages needs updating. It takes 12 clocks on the CLK

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pin to fully load the serial input shift register. Data on the SDI input pin is subject to the timing diagram (Figure 1) data setup and data hold time requirements. After the twelfth clock pulse, the processor needs to activate the LD strobe to have the DAC-8841 decode the serial register contents and update the target DAC register with the 8-bit data word. This needs to be done before the thirteenth positive clock edge. The timing requirements are in the electrical characteristic table and in the Figure 1 timing diagram. After twelve clock edges data initially loaded into the shift register at SDI appears at the shift register output SDO.

There is some digital feedthrough from the digital input pins. Operating the clock only when the DAC registers require updating minimizes the effect of the digital feedthrough on the analog signal channels.

Figure 21 shows a three-wire interface for a single DAC-8841 that easily cascades for multiple packages.

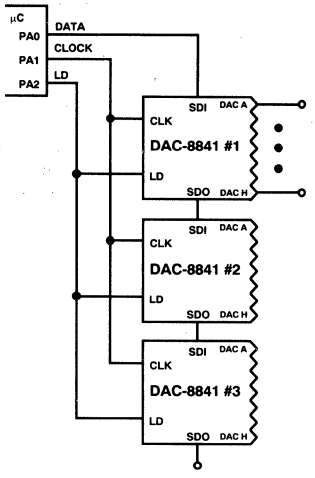

Figure 21. Three-Wire Interface

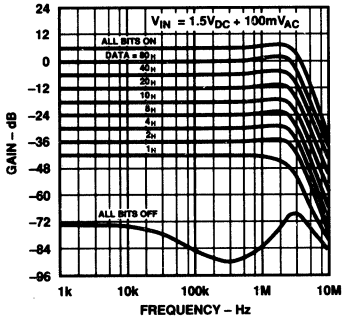

Figure 22. Gain (V_{OUT}/V_{IN}) and Feedthrough vs. Frequency

Digital Signal Processing Products
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Selection Guide
Digital Signal Processing Products

DSP Processor Key Feature Summary

Model	Instruction Cycle Time ns	Off-Chip Harvard Arch	Internal Program Memory RAM	Internal Data Memory RAM	Internal Program Cache Word	Program Memory Boot	Serial Ports	Programmable Timer	Ext Interrupts	Low Power Modes	Pin Count	Page
ADSP2100A	80	√			16 × 24				4		100	9-13
ADSP-2101	60		2K × 24	1K × 16		√	2	√	3	1	68	9-17
ADSP-2105	100		1K × 24	0.5K × 16		√	1	√	3	1	68	9-23
ADSP-2111	60		2K × 24	1K × 16		√	2	√	3	1	100	9-29
32/40-Bit Floating Point												
ADSP-21020	40	√			32 × 48				4	1	223	9-33

ANALOG DEVICES

In-Circuit Emulator

ADDS-2100A-ICE

FEATURES

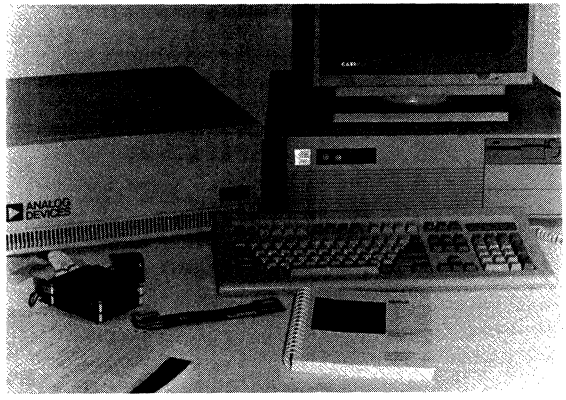
- **Interfaces to IBM PC Host via RS-232 Interface, at up to 57600 Baud**
- **Emulates 80 ns ADSP-2100A at Full Speed**
- **User Interface Similar to Simulators**
- **Custom Window Configuration and Command Aliasing**
- **Standalone Operation Allows Software Debugging Before Hardware Prototype**
- **Assembly and Disassembly of ADSP-2100A Instructions**
- **Single-Step as Well as Full-Speed Operation**
- **Overlay RAM Can Replace Target System Memory**
- **Trace Buffer Stores Up to 8K Frames of ADSP-2100A Activity**
- **Supports Software Breakpoints and Break Expressions**
- **Hardware Break and/or Trace Triggering on an Extensive Set of Bus Conditions**
- **Static User Control of Selected ADSP-2100A Inputs**
- **Software Support for Industry-Standard Mouse**
- **Optional Logic Module Probes Allow Tracing of Additional Signals**
- **Optional Probe-to-Target Umbilical Cord Facilitates Debug and Testing Work**

GENERAL DESCRIPTION

The ADSP-2100A Emulator is a hardware development tool that provides a controlled environment for observing, debugging, and testing activities in a target system. The emulator provides this control by replacing the target ADSP-2100A processor. While running at full speed, the emulator behaves like the processor in the target system. The emulator can monitor and record system behavior and lets you examine and alter memory locations as well as processor registers. Hardware events can be detected and used to trigger tracing.

The ADSP-2100A Emulator uses an emulator chassis manufactured by Microtek, Inc. The emulator consists of a control processor (CP) board, two real-time analyzer (RTA) boards, an ADSP-2100A personality board, and an ADSP-2100A in-circuit probe.

The emulator is operated through an IBM PC host computer. The interface software provided with the emulator is similar to the simulator of the ADSP-2100 Family Development Software.



TRACE SAMPLING RATE

Trace sampling occurs at the ADSP-2100A instruction rate, up to 12.5 MHz.

TRACE BUFFER SIZE

The trace memory buffer stores up to 8K × 144-bit frames of ADSP-2100A activity. Buffer data may be window displayed or written to a file.

OVERLAY RAM

Overlay RAM can replace program memory and/or data memory in the target system. Data memory space may be overlaid in 1K-word blocks. Program memory space may be overlaid in 2K-word blocks.

Overlay RAM size is equal to the ADSP-2100A's memory space. This includes 16K × 24-bit program memory and 16K × 16-bit data memory.

HARDWARE EVENT DETECT (TRIGGER)

Hardware events may be detected and used to break execution, start or stop tracing, or assert an instrumentation synchronization pulse. Break and/or trace triggering is possible on up to 8 bus condition sequences. Bus conditions and other signals may be logically combined to create more complex events.

ANALOG DEVICES

EZ-Tools Hardware Development Tools

ADDS-2101-EZ

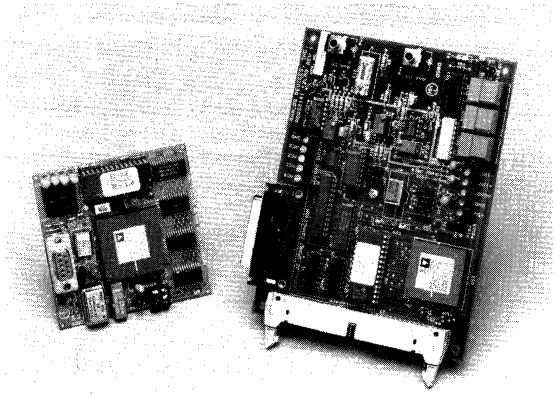
FEATURES

EZ-Tools Support Prototyping, Development and Debugging of ADSP-2101 and ADSP-2105 Systems

ADSP-2101 EZ-ICE™ IN-CIRCUIT EMULATOR
3.3" × 3.3" Surface-Mount Board with RS-232 Port
Plugs Directly into ADSP-2101 Socket on Target Board
Full Speed Emulation
Single Step Capability
Sixteen Breakpoints
Memory Upload/Download with a PC
Examine and Alter Registers, Program Memory and Data Memory
8 K × 24-Bit High Speed Program/Data Overlay Memory
12.288 MHz Oscillator, Socketed for Easy Change of Clock Speed
Memory Map (MMAP) Pin Control
Standalone Operation for Software Debugging without Target Board
Easy to Learn Menus and Displays

ADSP-2101 EZ-LAB™ DEMONSTRATION BOARD
12.5 MHz ADSP-2101 Microcomputer
64 K × 8-Bit Boot EPROM Preprogrammed with Demonstrations
Voice I/O Port with Microphone Input Jack and Speaker Output Jack
Four-Channel, 8-Bit Digital-to-Analog Converter (DAC) Port
Bus Expansion Connector Allows Additional I/O and Full Memory Expansion
Serial Port Expansion Available through SPORT Connector
12.288 MHz Crystal, Replaceable with Different Speed Crystals
Three Switches for User Control: Interrupt $\overline{IRQ2}$, Flag In and Reset

ADSP-2101 EZ-KIT STARTER PACKAGE
EZ-LAB Demonstration Board
Cross-Software (Assembler and Simulator)
DSP Textbook
Applications Handbook with Example Programs on Disk
Training Workshop Discount Coupon



GENERAL DESCRIPTION

The ADSP-2101 EZ-Tools support the prototyping, development and debugging in hardware of applications based on the ADSP-2101 or ADSP-2105 microcomputer.

EZ-ICE is a compact, easy-to-use in-circuit emulator for debugging code and testing ADSP-2101 or ADSP-2105 based systems. EZ-ICE consists of a board and an RS-232 cable. It is operated through a VT100-type terminal or through a PC running a terminal emulation program. The user interface is provided by an on-board microcontroller-based monitor.

EZ-LAB is a low cost evaluation and demonstration board for the ADSP-2101 DSP microcomputer. It allows you to test coded digital signal processing applications on the ADSP-2101. EZ-LAB comes equipped with an EPROM device containing prepared demonstrations, including speech and graphics applications. You can replace this EPROM with one containing your own programs. Upon reset, the processor reads in the contents of the EPROM, stores the code in its internal program memory, and begins execution.

EZ-Kit is a starter package consisting of:

- an ADSP-2101 EZ-LAB demonstration board,
- ADSP-2101 software development tools for the IBM* PC, including assembler and simulator,
- *Digital Signal Processing in VLSI*, a 575 page digital signal processing textbook featuring the ADSP-2100 family,
- a book of example applications with source code provided on disk, and
- a discount coupon for the ADSP-2100 processor family training workshop.

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EZ-ICE and EZ-LAB are trademarks of Analog Devices, Inc.
*IBM is a registered trademark of International Business Machines Corp.

ANALOG DEVICES

In-Circuit Emulator

ADDS-2101-ICE

FEATURES

- **Interfaces to IBM-PC Host via RS-232 Interface, at up to 57600 Baud**
- **Emulates 50 MHz ADSP-2101, with 12.5 MHz Instruction Rate**
- **User Interface Similar to ADSP-2101 Simulator**
- **Custom Window Configuration and Command Aliasing**
- **Simulator Configuration Files May Be Used**
- **Standalone Operation Allows Software Debugging Before Hardware Prototype**
- **Assembly and Disassembly of ADSP-2101 Instructions**
- **Single-Step As Well As Full-Speed Operation**
- **Overlay RAM Can Replace Target System Memory**
- **Interface Board Prevents Bus Contention Between Probe and Target**
- **Trace Buffer Stores up to 8K Frames of ADSP-2101 Activity at Full Speed**
- **Supports Software Breakpoints and Break Expressions**
- **Hardware Break and/or Trace Triggering on an Extensive Set of Bus Conditions**
- **Static User Control of Selected ADSP-2101 Inputs**
- **Software Support for Industry-Standard Mouse**
- **Optional PGA-PLCC Adaptor**
- **Optional Logic Module Probes Allow Tracing of Additional Signals**
- **Optional Probe-to-Target Umbilical Cord Facilitates Debug and Testing Work**

GENERAL DESCRIPTION

The ADSP-2101 Emulator is a hardware development tool that provides a controlled environment for observing, debugging, and testing activities in a target system. The emulator provides this control by replacing the target ADSP-2101 processor. While running at full speed, the emulator behaves like the processor in the target system. The emulator can monitor and record system behavior, and lets you examine and alter memory locations as well as processor registers. Hardware events can be detected and used to trigger tracing.

The ADSP-2101 Emulator user an emulator chassis manufactured by Microtek, Inc. The emulator consists of a VME-based chassis, a control processor (CP) board, two real-time analyzer (RTA) boards, an ADSP-2101 personality board, and an ADSP-2101 in circuit probe.

The emulator is operated through an IBM PC host computer. The interface software provided with the emulator is similar to the software simulator. If you are familiar with the simulator, the emulator requires little additional learning.

ANALOG DEVICES

ADSP-2100 Family Development Software

ADDS-21XX-SW

FEATURES

DSP PROCESSORS SUPPORTED
ADSP-2100
ADSP-2101/2102
ADSP-2105/2106
ADSP-2111
ADSP-21msp50

SYSTEM BUILDER
Architecture Description File Specifies Target Hardware

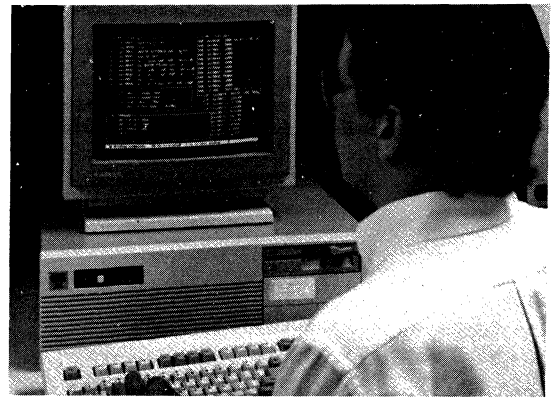
ASSEMBLER
C Preprocessor Supports High Level Constructs
Supports Flexible Macro Processing
Encourages Modular Code Development
Provides a Full Range of Diagnostics

LINKER
User-Defined Library Support
Maps Assembler Output to System Memory

PROM SPLITTER
Formats ROM Memory Image for Uploading to PROM Programmers

SIMULATORS
Reconfigurable Windowing Interface
Full Symbolic Disassembly
Simulates Hardware Configuration
Simulates Parallel and Serial Port I/O
Advanced Debugging Features
Profiling of Code Execution History

C COMPILER & RUNTIME LIBRARY
Allows Development of Applications Software in C Language
Supports In-Line Assembly Code
Incorporates Optimizing Algorithms
Produces ROMable Code
Floating-Point Emulation Support
Runtime Library with ANSI-Standard and DSP Library Functions
Simplified Interrupt Handling via Library Functions



GENERAL DESCRIPTION

The ADSP-2100 Family Development Software is a complete set of software design tools which allow the programming of applications for this family of DSP microprocessors. The development system includes C and assembly language programming tools as well as processor simulators to facilitate software design and debug.

The software development system includes several programs: System Builder, Assembler, Linker, PROM Splitter, Simulators and C Compiler. Release 3.0 of the software development system runs on the IBM (or IBM-compatible) PC under DOS 3.x, SUN3/SUN4 workstations, and VAX VMS.

The development process begins with the task of defining the target system hardware with the use of the system builder tool. The system builder generates an architecture description file which passes information about the target hardware to the linker, simulator, and emulator (if used).

Code generation is accomplished by writing C and/or assembly language source code modules. Each C and assembly module is compiled and/or assembled separately. Several modules are then linked together to form an executable program.

The simulator provides windows that display different portions of the hardware environment. To replicate the target hardware, the simulator configures memory according to the architecture description file generated by the system builder, and simulates I/O ports according to user-entered commands. This simulation allows the user to debug the system and analyze performance before committing to a hardware prototype.

ANALOG DEVICES ADSP-21000 Family Development Software

ADDS-210XX-SW

Supports the ADSP-21000 Family of Floating-Point DSP Processors

ASSEMBLER
High Level Algebraic Syntax
Extensive Set of Directives
Supports Macros & Conditional Assembly
Generates COFF Object FIles

LINKER
Combines Object and Library Files
Generates COFF Executable Files
Maps Assembler Output to Target Hardware
Generates Memory Map Listing

ASSEMBLY LIBRARY/LIBRARIAN
Powerful Set of Arithmetic and DSP Functions
Callable from Assembly Code
Can Incorporate User-Defined Routines

SIMULATOR
Window-Based Interface
Pull-Down Menus
Point-and-Click Mouse Operation
Full Symbolic Disassembly and On-Line Assembly
Simulates Memory and Ports
Flags Illegal Operations
Breakpoint Capability

PROM SPLITTER
Formats Executable File for Programming PROMs or Loading Target from a Microcontroller
Supports Motorola S Record, Intel Extended Hex, etc.

OPTIMIZING C COMPILER
ANSI C Compliant
C-Callable Library of ANSI-Standard and DSP Functions
Supports In-Line Assembly Code
Provides FRACT Data Type (1.31 Fixed-Point Format)

GENERAL DESCRIPTION

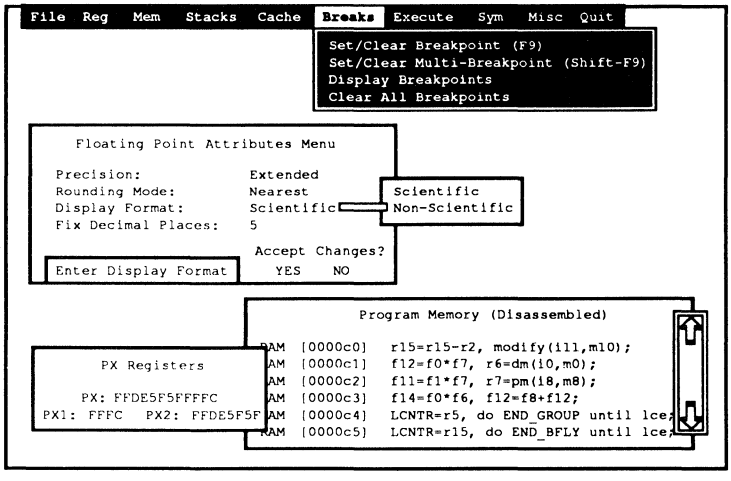
The ADSP-21000 Family Development Software is a set of tools for creating and debugging programs for the ADSP-21000 family of floating-point processors. These tools enable you to create, test, and debug ADSP-210XX programs.

The ADSP-21000 Development Software consists of several components described in the following sections.

OPTIMIZING C COMPILER

The C Compiler reads source files written in ANSI-standard C language. The compiler outputs ADSP-210XX assembly language files and comes with a standard library of C-callable routines.

ADSP-21020 SIMULATOR



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ASSEMBLER
The assembler inputs a file of ADSP-210XX source code and assembler directives and outputs a relocatable object file. The assembler supports standard C preprocessor directives as well as its own directives.

LINKER
The linker processes separately assembled object and library files to create a single executable program. It assigns memory locations to code and data in accordance with a user-defined architecture file, a text file that describes the memory configuration of the target system.

ASSEMBLY LIBRARY/LIBRARIAN
The assembly library contains standard arithmetic and DSP routines that you can call from your program, saving development time. You can add your own routines to this library using the librarian function.

SIMULATOR
The simulator executes an ADSP-210XX program in software in the same way that an ADSP-21000 family processor would in hardware. The simulator also simulates the memory and I/O devices specified in the architecture file. The window-based user interface supports a powerful debug environment that allows the developer to interactively observe and alter the data in the processor and in memory. Accurate simulation of chip functionality is assured.

PROM SPLITTER
The PROM splitter translates an ADSP-210XX executable program into one of several formats (Motorola S2 and S3, Intel Hex Record, etc.) that can be used to configure a PROM or be downloaded to a target from a microcontroller.

DEVELOPMENT PROCESS
Figure 1 shows the process of compiling, assembling, linking and simulating a program, indicating the input and output of each step. File name extensions (.asm, .obj, etc.) signify different types of files.

MINIMUM PC REQUIREMENTS
An IBM AT or 286/386-based PC (or compatible) and 640K of memory are required. A color monitor, mouse, and at least 2 MB of extended memory are recommended.

ORDERING INFORMATION

Part Number	Description
ADDS-210XX-DSW-PC	Assembler, Linker, Assembly Library/ Librarian. PROM Splitter, Simulator
ADDS-210XX-BUN-PC	Assembler, Linker, Assembly Library/ Librarian, PROM Splitter, Simulator, Optimizing C Compiler & Runtime Library
ADDS-210XX-C-UP-PC	Optimizing C Compiler & Runtime Library (Upgrade for Owners of the DSW Package)

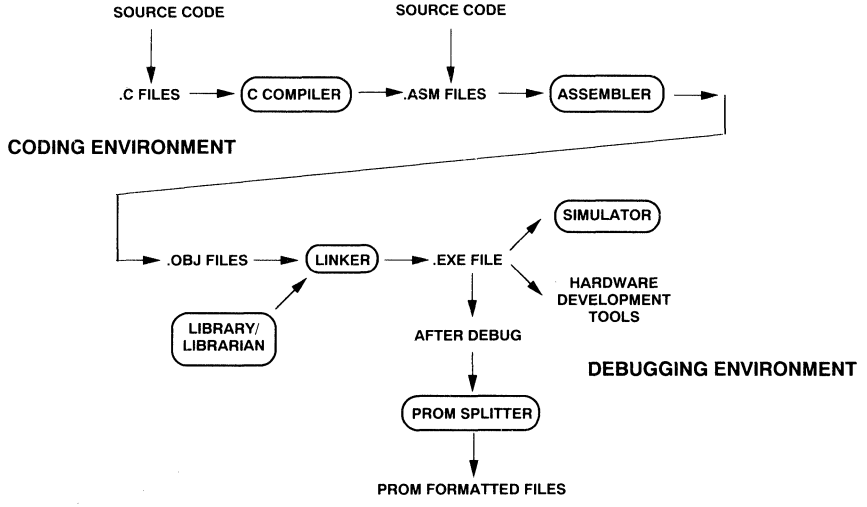


Figure 1. Program Development

ANALOG DEVICES

12.5 MIPS DSP Microprocessors

ADSP-2100/ADSP-2100A

FEATURES

Pin- and Code-Compatible DSP Microprocessors
ADSP-2100, 6.144MHz and 8.192MHz
ADSP-2100A, 10.24MHz and 12.5MHz
Separate Program and Data Buses, Extended Off-Chip
Single-Cycle Direct Access to 16K × 16 of Data Memory
Single-Cycle Direct Access to 32K × 24 of Program Memory
Dual Purpose Program Memory for Both Instruction and Data Storage
Three Independent Computational Units: ALU, Multiplier/Accumulator and Barrel Shifter
Two Independent Data Address Generators
Powerful Program Sequencer
Internal Instruction Cache
Provisions for Multiprecision Computation and Saturation Logic
Single-Cycle Instruction Execution
Multifunction Instructions
Four External Interrupts
80ns Cycle Time (ADSP-2100A)
790mW Maximum Power Dissipation (ADSP-2100A, J and K Grades)
100-Pin Grid Array, 100-Lead PQFP (JEDEC Style), 100-Lead CQFP

APPLICATIONS

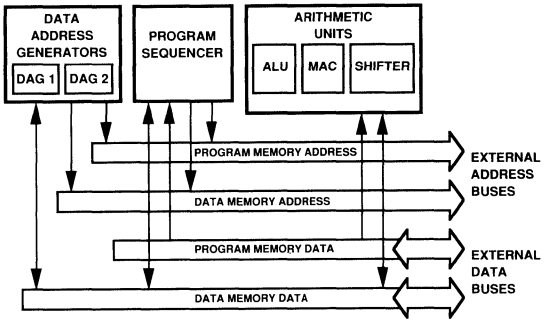
Optimized for DSP Algorithms Including
Digital Filtering
Fast Fourier Transforms
Applications Include
Image Processing
Radar, Sonar
Speech Processing
Telecommunications

GENERAL DESCRIPTION

The ADSP-2100 and ADSP-2100A are pin- and code-compatible single-chip microprocessors optimized for digital signal processing (DSP) and other high-speed numeric processing applications. The ADSP-2100 and ADSP-2100A are both fabricated in a low-power double-layer metal CMOS process. Together, they offer a span of performance from 6MHz to 12.5MHz. All descriptions of the ADSP-2100 in the text of this data sheet refer to both the ADSP-2100A and the ADSP-2100 versions since they have identical architectures and instruction sets. Timing and electrical specifications differ as shown in those sections of the data sheet.

Both processors integrate computational units, data address generators and a program sequencer in a single device. The ADSP-2100 architecture makes efficient use of external memories for program and data storage, freeing silicon area for increased processor performance. The resulting processor combines the functions and performance of a bit-slice/building block system with the ease of design and development support of a general purpose microprocessor.

FUNCTIONAL BLOCK DIAGRAM



The ADSP-2100A (K grade) operates at 12.5MHz. Every instruction executes in a single 80ns cycle. The ADSP-2100A (J and K grades) dissipates less than 790mW while the ADSP-2100 dissipates less than 475mW.

The ADSP-2100's flexible architecture and comprehensive instruction set support a high degree of operational parallelism. Because all instructions execute in a single cycle, MHz = MIPS. In one cycle the ADSP-2100 can:

- generate the next program address
- fetch the next instruction
- perform one or two data moves
- update one or two data address pointers
- perform a computational operation.

DEVELOPMENT SYSTEM

The ADSP-2100 and ADSP-2100A are supported by a complete set of tools for software and hardware system development. The Development-Software System provides a System Builder for defining the architecture of simulated systems under development, an Assembler, a Linker and a interactive Simulator. An ANSI (draft) Standard C Compiler supports program development in this widely used programming language, producing ADSP-2100 Assembly code which may be assembled, linked and simulated with the other development system tools. A PROM Splitter generates PROM burner compatible files. An In-Circuit Emulator is available for hardware debugging.

ADDITIONAL INFORMATION

For additional information on the architecture and instruction set of the processor, refer to the *ADSP-2100 User's Manual*. For more information about programming and the Development System, refer to the *ADSP-2100 Family Development Software Manual* and the *ADSP-2100 Emulator Manual*. Manuals are available only from your local Analog Devices sales office. There is also a quarterly newsletter, *DSPatch*™, supporting Analog Devices' digital signal processing customers.

ARCHITECTURE OVERVIEW

Figure 1 is an overall block diagram of the ADSP-2100. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC) and the Shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations. The Shifter performs logical and arithmetic shifts, normalization, denormalization and derive exponent operations. The Shifter can be used to efficiently implement any degree of numeric format control, up to and including full floating point representations. The computational units are arranged side-by-side instead of serially for flexible operation sequencing. The internal result (R) bus directly connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient use of these computational units. The program sequencer generates the next instruction address. To minimize overhead cycles, the sequencer supports conditional jumps, subroutine calls and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-2100 executes looped code with zero overhead; no explicit jump instructions are required to maintain the loop.

The data address generators (DAGs) handle address pointer updates. Each DAG keeps track of up to four address pointers. Whenever the pointer is used to access external data (indirect addressing), it is modified by a prespecified value. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers. With two independent DAGs, the processor can generate two addresses simultaneously for dual operand fetches.

Efficient data transfer is achieved with the use of five internal buses.

- Program Memory Address (PMA) bus
- Program Memory Data (PMD) bus
- Data Memory Address (DMA) bus
- Data Memory Data (DMD) bus
- Result (R) bus

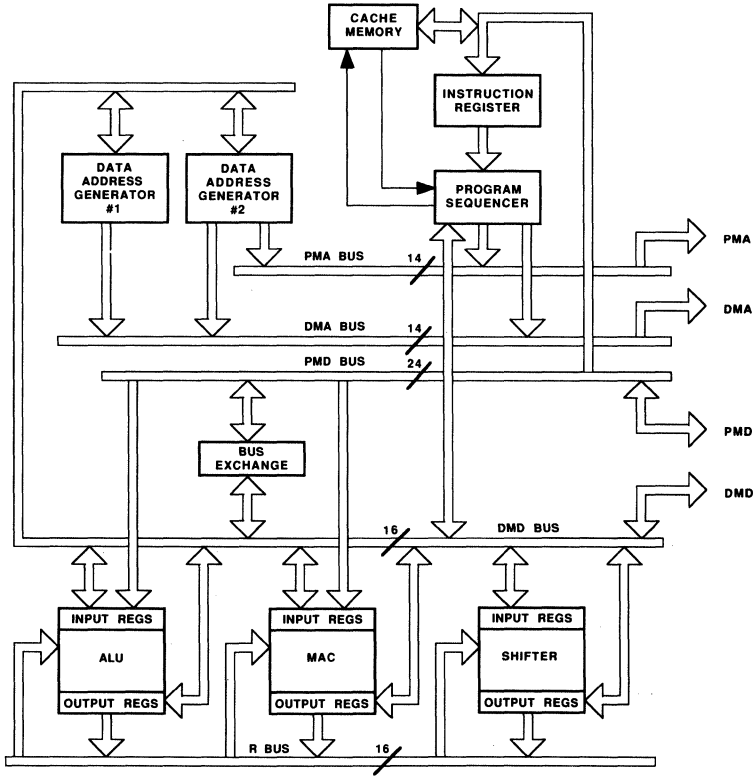


Figure 1. ADSP-2100 Block Diagram

DSPatch is a trademark of Analog Devices, Inc.

ADSP-2100A Data Memory Read	Test Code	AJ Grade Min	AJ Grade Max	AK Grade Min	AK Grade Max	AS Grade Min	AS Grade Max	AT Grade Min	AT Grade Max	AU Grade Min	AU Grade Max	Units	Derating Factor
Switching Characteristics													
67 $\overline{\text{DMRD}}$ Width Low	A	36		28		45		36		28		ns	4
68 DMA Valid to $\overline{\text{DMRD}}$ Low	A	6		4		14		6		4		ns	3
69 $\overline{\text{DMRD}}$ High to DMA Invalid	A	8		6		10		8		6		ns	1
70 $\overline{\text{DMS}}$ Valid to $\overline{\text{DMRD}}$ Low	A	18		14		27		18		14		ns	3
71 $\overline{\text{DMRD}}$ High to $\overline{\text{DMS}}$ Invalid	A	8		6		10		8		6		ns	1
Timing Requirements													
94 $\overline{\text{DMRD}}$ Low to DMD Input Valid	A		30		20		37		28		18	ns	4
95 DMA Valid to DMD Input Valid	A		48		32		59		46		32	ns	7
96 $\overline{\text{DMS}}$ Valid to DMD Input Valid	A		52		45		67		50		35	ns	7
98 $\overline{\text{DMRD}}$ High to DMD Input Invalid	A	0		0		0		0		0		ns	

NOTE ON GENERATING WAIT STATES

See the application note "Wait State Generation on the ADSP-2100/2100A" for information on using DMACK to generate wait states.

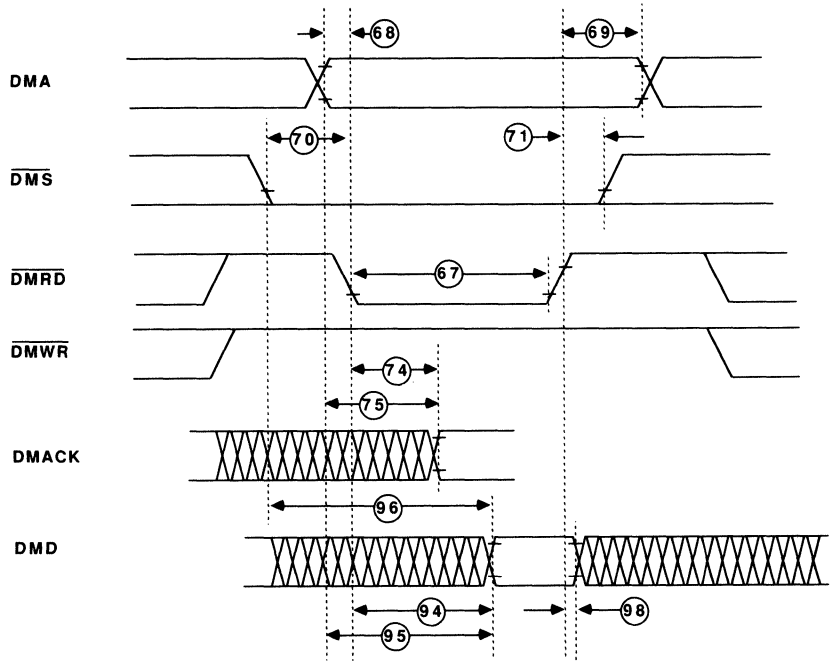


Figure 2. Data Memory Read

	ADSP-2100A Data Memory Write	Test Code	AJ Grade Min	AJ Grade Max	AK Grade Min	AK Grade Max	AS Grade Min	AS Grade Max	AT Grade Min	AT Grade Max	AU Grade Min	AU Grade Max	Units	Derating Factor
Switching Characteristics														
78	$\overline{DMWR}$ Width Low	A	36		28		45		36		28		ns	4
79	DMA Valid to $\overline{DMWR}$ Low	A	8		4		17		8		4		ns	3
80	$\overline{DMWR}$ High to DMA Invalid	A	8		6		10		8		6		ns	1
81	$\overline{DMS}$ Valid to $\overline{DMWR}$ Low	A	20		16		28		20		16		ns	3
82	$\overline{DMWR}$ High to $\overline{DMS}$ Invalid	A	6		4		8		6		4		ns	1
87	$\overline{DMWR}$ Low to DMD Out Enable	F	8		6		8		8		6		ns	1
88	$\overline{DMWR}$ High to DMD Out Disable	D		32		29		38		32		29	ns	1
89	$\overline{DMWR}$ Low to DMD Out Valid	A		29		26		32		29		26	ns	1
90	$\overline{DMWR}$ High to DMD Out Invalid	A	10		8		12		10		8		ns	1
91	DMD Out Valid to $\overline{DMWR}$ High	A	18		13		25		16		13		ns	3

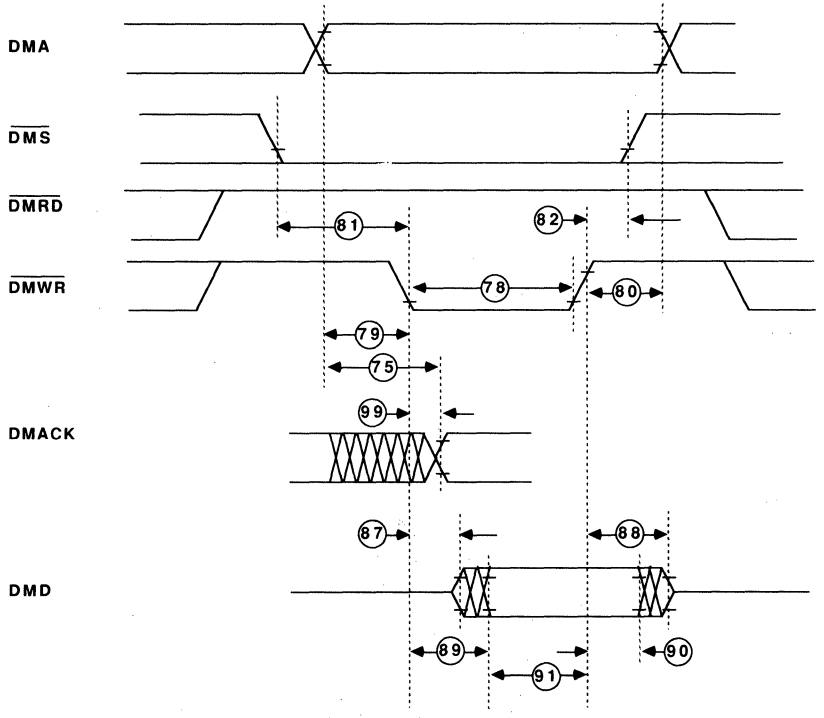


Figure 3. Data Memory Write

ANALOG DEVICES

DSP Microcomputer

ADSP-2101

FEATURES

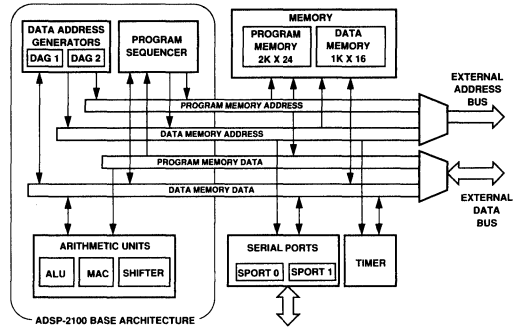
Complete DSP Microcomputer
80 ns Instruction Cycle Time from 12.5 MHz Crystal
ADSP-2100 Code & Function Compatible
2K Words of On-Chip Program Memory RAM
1K Word of On-Chip Data Memory RAM
Separate Program and Data Buses On-Chip
Dual Purpose Program Memory for Both Instruction and Data Storage
Three Independent Computational Units: ALU, Multiplier/Accumulator and Barrel Shifter
Two Independent Data Address Generators
Powerful Program Sequencer
Zero Overhead Looping
Conditional Arithmetic Instruction Execution
Two Double-Buffered Serial Ports with Companding Hardware and Automatic Data Buffering
Programmable 16-Bit Interval Timer with Prescaler
Programmable Wait State Generation
Automatic Booting of Internal Program Memory from Byte-Wide External Memory, e.g., EPROM
Provisions for Multiprecision Computation and Saturation Logic
Single-Cycle Instruction Execution
Single-Cycle Context Switch
Multifunction Instructions
Three Edge- or Level-Sensitive External Interrupts
80 mW Maximum Power Dissipation in Standby Mode
68-Pin PGA, 68-Lead PLCC and 80-Lead PQFP
MIL-STD-883 Compliant Versions Available

GENERAL DESCRIPTION

The ADSP-2101 is a single-chip microcomputer optimized for digital signal processing (DSP) and other high-speed numeric processing applications. Its instruction set is a fully compatible superset of the ADSP-2100 instruction set. It combines the complete ADSP-2100 architecture (three computational units, data address generators and a program sequencer) with two serial ports, a programmable timer, extensive interrupt capabilities and on-chip program and data memory RAM. The ADSP-2101 has 1K words of (16-bit) data memory RAM and 2K words of (24-bit) program memory RAM on chip.

Fabricated in a high-speed 1.0 micron double-layer metal CMOS process, the ADSP-2101 operates at an 80 ns instruction cycle time. Every instruction executes in a single cycle. Fabrication in CMOS results in low power requirements. The ADSP-2101 dissipates less than 1 W under all conditions and no more than 80 mW under standby conditions.

FUNCTIONAL BLOCK DIAGRAM



The ADSP-2101's flexible architecture and comprehensive instruction set support a high degree of operational parallelism. In one cycle the ADSP-2101 can:

- generate the next program address
- fetch the next instruction
- perform one or two data moves
- update one or two data address pointers
- perform a computational operation
- receive and transmit data via the two serial ports

Development System

The ADSP-2101 is supported by a complete set of tools for software and hardware system development. The Development Software is a set of modules that supports all ADSP-2100 family processors. The System Builder provides a high-level method for defining the architecture of systems under development. The Assembler produces object code and the Linker combines object modules and library calls into an executable file. The Simulator provides an interactive instruction-level simulation with a reconfigurable user interface. A PROM Splitter generates PROM burner compatible files. The C Compiler generates ADSP-2101 assembly source code.

Emulators aid in the hardware debugging of ADSP-2101 systems. The full featured emulator performs a full range of emulation functions including trace and triggering. EZ-Tools are low cost, easy-to-use hardware tools. The EZ-ICE™ emulator provides basic functions like changing register values and setting breakpoints. The EZ-LAB™ demonstration board is a complete ADSP-2101-based system that executes its own example programs. The EZ-Kit package is a starter kit that contains an EZ-LAB board, development software, books and example programs.

EZ-ICE and EZ-LAB are trademarks of Analog Devices, Inc.

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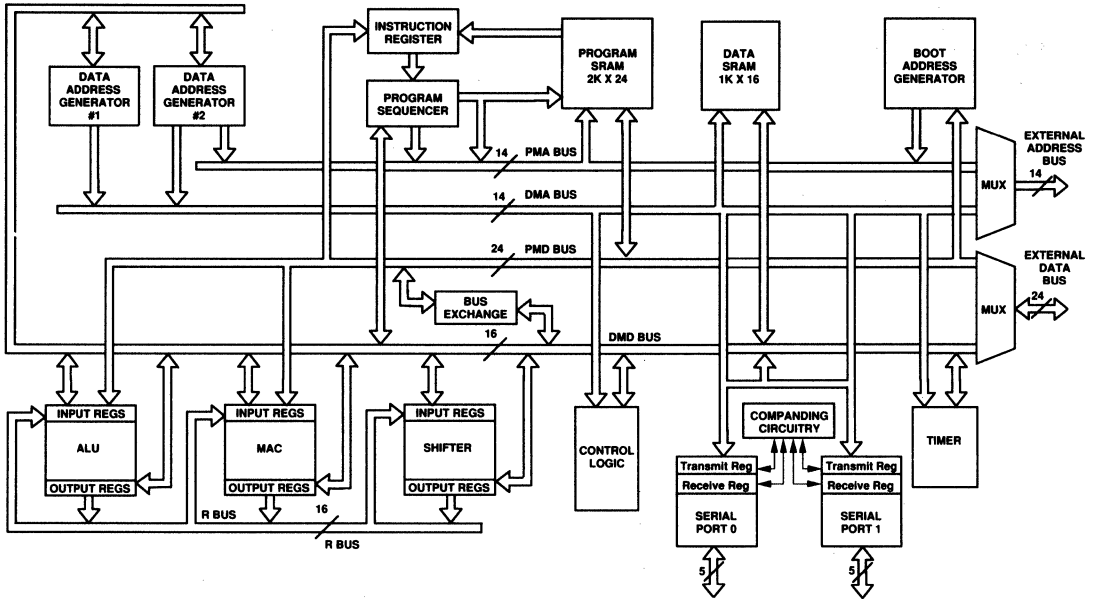


Figure 1. ADSP-2101 Block Diagram

Additional Information

This data sheet provides a general overview of ADSP-2101 functionality. For additional information on the architecture and instruction set of the processor, refer to the *ADSP-2101 User's Manual*. For more information about the Development System and ADSP-2101 programmer's reference information, refer to the *ADSP-2100 Family Development Software Manuals* and the *ADSP-2101 Emulator Manual*.

ARCHITECTURE OVERVIEW

Figure 1 is an overall block diagram of the ADSP-2101. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC) and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations. The shifter can be used to efficiently implement numeric format control including multiword floating-point representations.

The internal result (R) bus directly connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient use of these computational units. The sequencer supports conditional jumps, subroutine calls and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-2101 executes looped code with zero overhead; no explicit jump instructions are required to maintain the loop.

The data address generators (DAGs) handle address pointer updates. Each DAG maintains four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of a specified modify register. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers. With two data independent DAGs, the processor can generate two data addresses simultaneously for dual operand fetches. The circular buffering feature is also used by the serial ports for automatic data transfers; these are described in the section on serial ports.

Efficient data transfer is achieved with the use of five internal buses.

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

Parameter		ADSP-2101-40 Min	ADSP-2101-40 Max	ADSP-2101-50 Min	ADSP-2101-50 Max	Unit
Memory Read						
Timing Requirement:						
t_{RDD}	$\overline{RD}$ Low to Data Valid		$0.5t_{CK} - 15+w$		$0.5t_{CK} - 15+w$	ns
t_{AA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid		$0.75t_{CK} - 20+w$		$0.75t_{CK} - 20+w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		0		ns
Switching Characteristic:						
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 5+w$		$0.5t_{CK} - 5+w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{ASR}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 12$		$0.25t_{CK} - 12$		ns
t_{RDA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 10$		$0.25t_{CK} - 10$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		$0.5t_{CK} - 5$		ns
		w = wait states × (t_{CK})		w = wait states × (t_{CK})		

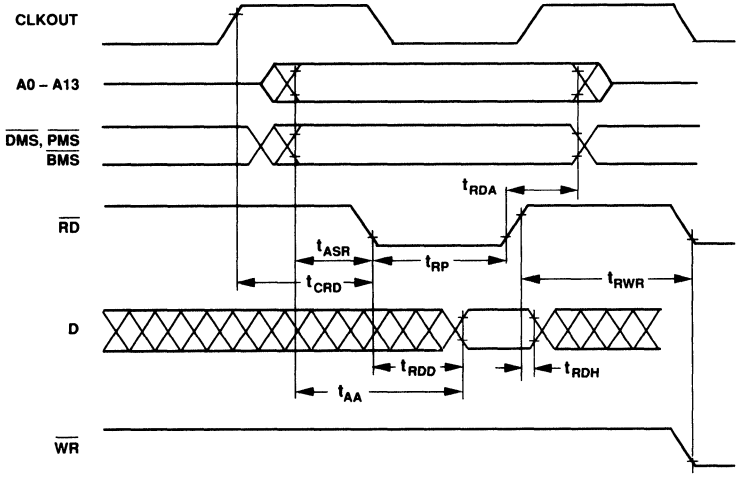


Figure 2. Memory Read

Parameter		ADSP-2101-40 Min	ADSP-2101-40 Max	ADSP-2101-50 Min	ADSP-2101-50 Max	Unit
Memory Write						
Switching Characteristic:						
t_{DW}	Data Setup before $\overline{WR}$ High	$0.5t_{CK} - 10+w$		$0.5t_{CK} - 10+w$		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK} - 10$		$0.25t_{CK} - 10$		ns
t_{WP}	$\overline{WR}$ Pulse Width	$0.5t_{CK} - 5+w$		$0.5t_{CK} - 5+w$		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		0		ns
t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	$0.25t_{CK} - 12$		$0.25t_{CK} - 12$		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK} - 10$		$0.25t_{CK} - 10$		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{AW}	A0–A13 Setup before $\overline{WR}$ Deasserted	$0.75t_{CK} - 15+w$		$0.75t_{CK} - 15+w$		ns
t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted	$0.25t_{CK} - 10$		$0.25t_{CK} - 10$		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		$0.5t_{CK} - 5$		ns
		w = wait states × (t_{CK})		w = wait states × (t_{CK})		

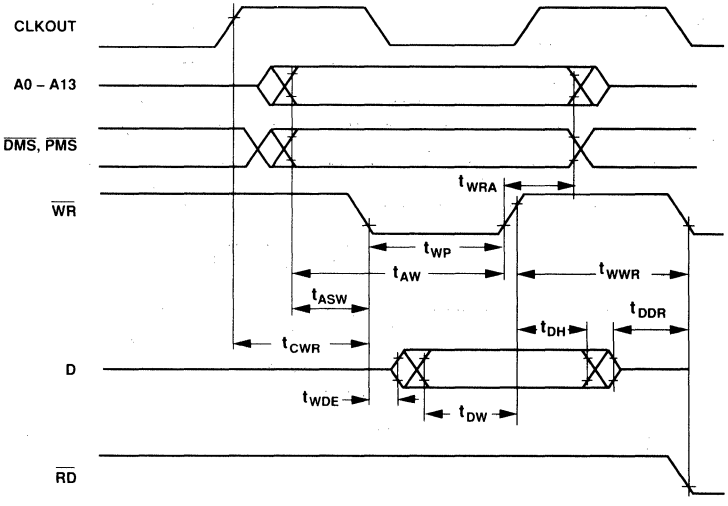


Figure 3. Memory Write

Parameter		ADSP-2101-40 Min	ADSP-2101-40 Max	ADSP-2101-50 Min	ADSP-2101-50 Max	Unit
Serial Ports						
Timing Requirement:						
t_{SCK}	SCLK Period	97.6		80		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	10		8		ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	10		10		ns
t_{SCP}	$SCLK_{in}$ Width	38		30		ns
Switching Characteristic:						
t_{CC}	CLKOUT High to $SCLK_{out}$	$0.25t_{CK}$	$0.25t_{CK}$ + 15	$0.25t_{CK}$	$0.25t_{CK}$ + 15	ns
t_{SCDE}	SCLK High to DT Enable	0		0		ns
t_{SCDV}	SCLK High to DT Valid		25		20	ns
t_{RH}	TFS/RFS_{out} Hold after SCLK High	0		0		ns
t_{RD}	TFS/RFS_{out} Delay from SCLK High		25		20	ns
t_{SCDH}	DT Hold after SCLK High	0		0		ns
t_{TDE}	TFS_{in} (alt) to DT Enable	0		0		ns
t_{TDV}	TFS_{in} (alt) to DT Valid		20		18	ns
t_{SCDD}	SCLK High to DT Disable		30		25	ns
t_{RDV}	RFS_{in} (multichannel, frame delay zero) to DT Valid		25		20	ns

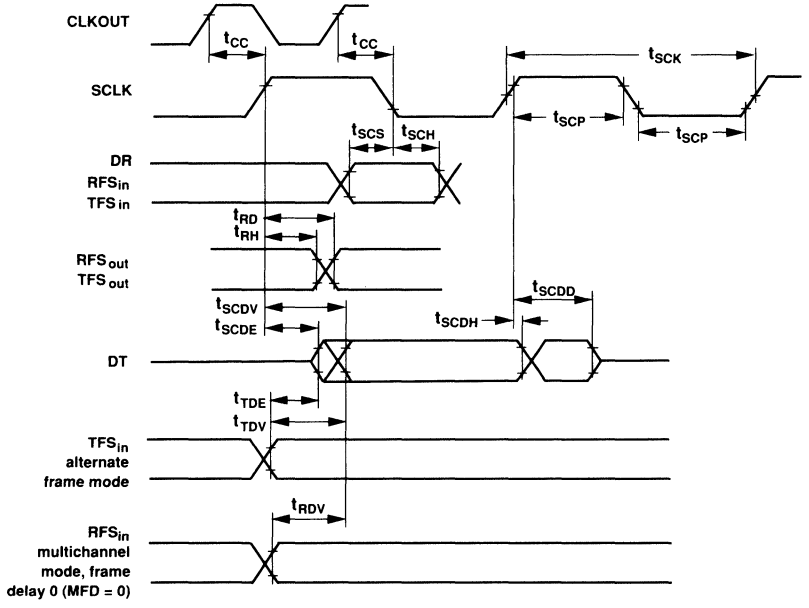


Figure 4. Serial Ports

ANALOG DEVICES

DSP Microcomputer

ADSP-2105

FEATURES

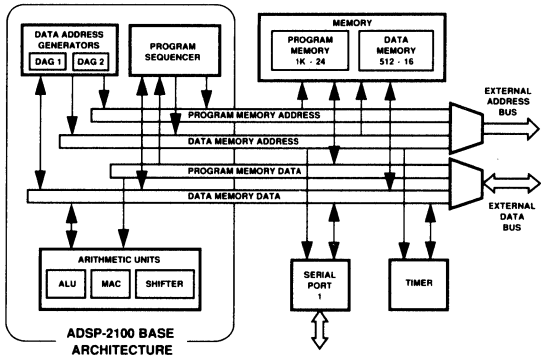
Complete DSP Microcomputer
100 ns Instruction Cycle Time from 10 MHz Crystal
ADSP-2100 Code- & Function-Compatible
ADSP-2101 Pin-Compatible
1K Words of On-Chip Program Memory RAM
512 Words of On-Chip Data Memory RAM
Dual Purpose Program Memory for Both Instruction and Data Storage
Separate Program and Data Buses On-Chip
Three Computation Units: ALU, Multiplier/ Accumulator and Barrel Shifter
Two Independent Data Address Generators
Powerful Program Sequencer
Zero Overhead Looping
Conditional Arithmetic Instruction Execution
Double-Buffered Serial Port with Companding Hardware and Automatic Data Buffering
Programmable 16-Bit Interval Timer with Prescaler
Programmable Wait State Generation
Automatic Boot of Internal Program Memory from Byte-Wide External Memory, e.g., EPROM
Provisions for Multiprecision Computation and Saturation Logic
Single-Cycle Instruction Execution
Single-Cycle Context Switch
Multifunction Instructions
Three Edge- or Level-Sensitive External Interrupts
80 mW Maximum Power Dissipation in Standby Mode
68-Lead PLCC

GENERAL DESCRIPTION

The ADSP-2105 is a single-chip microcomputer optimized for digital signal processing (DSP) and other high-speed numeric processing applications. Its instruction set is a fully compatible superset of the ADSP-2100 instruction set. It combines the complete ADSP-2100 architecture (three computational units, data address generators and a program sequencer) with a serial port, a programmable timer, extensive interrupt capabilities and on-chip program and data memory RAM. The ADSP-2105 has 512 words of (16-bit) data memory RAM and 1K words of (24-bit) program memory RAM on chip.

The ADSP-2105 is a pin-for-pin and code-compatible version of Analog Devices' ADSP-2101 DSP Microcomputer. The ADSP-2105 is the industry's leading cost/performance DSP. It is an ideal choice in applications needing the performance advantages of a DSP processor at the cost of today's standard microcontrollers.

FUNCTIONAL BLOCK DIAGRAM



The ADSP-2105 offers a direct upgrade path to more highly integrated and higher performance DSP processors. It is a subset of the ADSP-2101. Users selecting the ADSP-2105 will be able to preserve their investment in ADSP-21XX tools in future programs requiring the added features found on the ADSP-2101 and future members of the ADSP-2100 family.

The ADSP-2105 is feature- and instruction-set compatible with the ADSP-2101. The only differences are the sizes of on-chip memories (half the size of the ADSP-2101's), the number of serial ports (one instead of two) and processor speed. The ADSP-2105 serial port (SPORT) is identical to SPORT1 of the ADSP-2101. The specifics of these differences are documented at the end of this data sheet.

Fabricated in a high-speed 1.0 micron double-layer metal CMOS process, the ADSP-2105 operates with a 100 ns instruction cycle time. Every instruction executes in a single cycle. Fabrication in CMOS results in low power dissipation. The ADSP-2105 dissipates less than 1 W under all conditions and no more than 80 mW under standby conditions.

The ADSP-2105's flexible architecture and comprehensive instruction set support a high degree of operational parallelism. In one cycle the ADSP-2105 can:

- generate the next program address
- fetch the next instruction
- perform one or two data moves
- update one or two data address pointers
- perform a computational operation
- receive or transmit data via the serial port

9

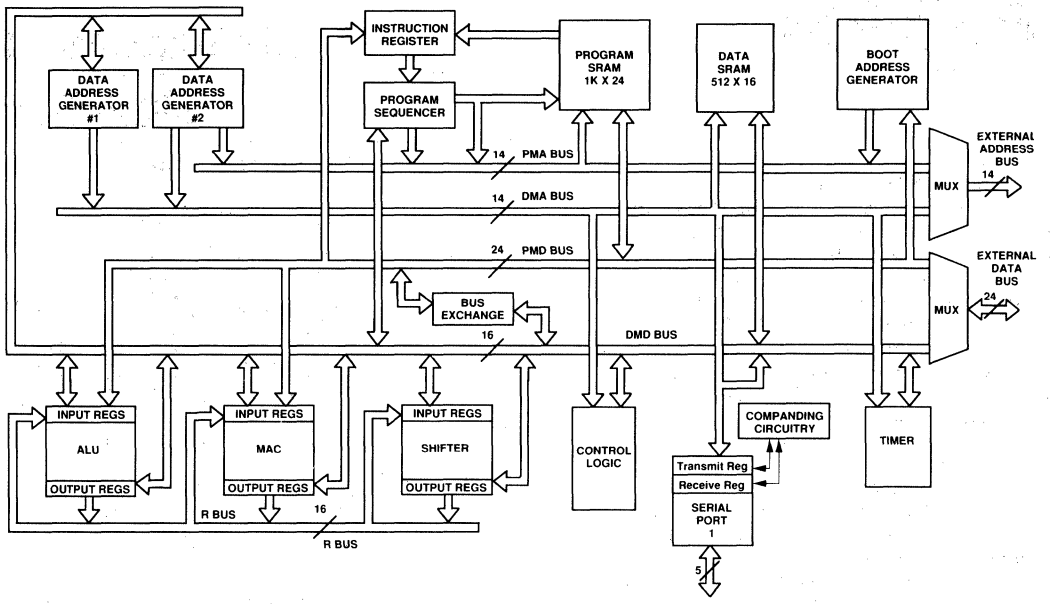


Figure 1. ADSP-2105 Block Diagram

Development System

The ADSP-2105 is supported by a complete set of tools for software and hardware system development. The development software is a set of modules that supports all the ADSP-2100 family processors. The System Builder provides a high-level method for defining the architecture of systems under development. The Assembler produces object code and the Linker combines object modules and library calls into an executable file. The Simulator provides an interactive instruction-level simulation with a reconfigurable user interface. A PROM Splitter generates PROM burner compatible files. The C Compiler generates ADSP-2105 assembly source code.

Emulators aid in the hardware debugging of ADSP-2105 systems. The full-featured emulator performs a full range of emulation functions including trace and triggering. EZ-Tools are low cost, easy-to-use hardware tools. The EZ-ICE™ emulator provides basic functions like changing register values and setting breakpoints. The EZ-LAB™ demonstration board is a complete ADSP-2101-based system that executes its own example programs. The EZ-Kit package is a starter kit that contains an EZ-LAB board, development software, books and example programs.

Additional Information

Because the ADSP-2105 is a subset of the ADSP-2101, the same publications and development tools support both devices.

For additional information on the architecture and instruction set of the processor, refer to the *ADSP-2101 User's Manual*. For more information about the Development System and ADSP-2105 programmer's reference information, refer to the *ADSP-2100 Family Development Software Manuals* and the *ADSP-2101 Emulator Manual*.

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ARCHITECTURE OVERVIEW

Figure 1 is an overall block diagram of the ADSP-2105.

The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC) and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations. The shifter can be used to efficiently implement numeric format control including multiword floating-point representations.

The internal result (R) bus directly connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient use of these computational units. The sequencer supports conditional jumps, subroutine calls and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-2105 executes looped code with zero overhead; no explicit jump instructions are required to maintain the loop.

The data address generators (DAGs) handle address pointer updates. Each DAG maintains four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of a specified modify register. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers. With two independent DAGs, the processor can generate two data addresses simultaneously for dual operand fetches. The circular buffering feature is also used by the serial port for automatic data transfers.

Efficient data transfer is achieved with the use of five internal buses.

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

Parameter		ADSP-2105-40 Min	Max	Unit
Memory Read				
Timing Requirement:				
t_{RDD}	$\overline{RD}$ Low to Data Valid		$0.5t_{CK} - 15+w$	ns
t_{AA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid		$0.75t_{CK} - 20+w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristic:				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 5+w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{ASR}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 12$		ns
t_{RDA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 10$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns
		w = wait states × (t_{CK})		

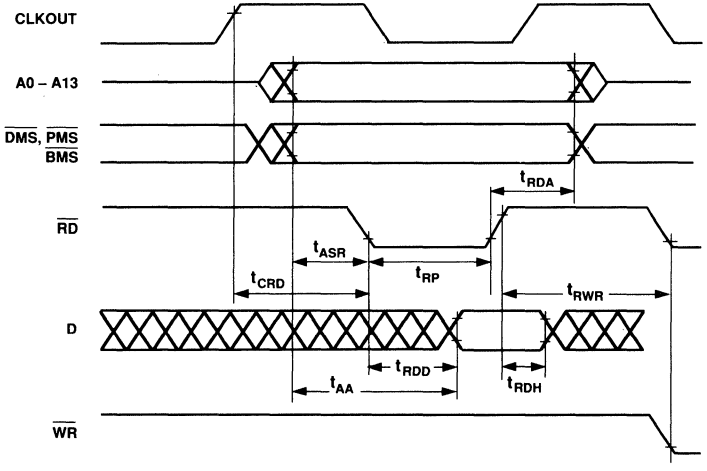


Figure 2. Memory Read

Parameter		ADSP-2105-40 Min	Max	Unit
Memory Write				
Switching Characteristic:				
t_{DW}	Data Setup before $\overline{WR}$ High	$0.5t_{CK} - 10+w$		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK} - 10$		ns
t_{WP}	$\overline{WR}$ Pulse Width	$0.5t_{CK} - 5+w$		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	$0.25t_{CK} - 12$		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK} - 10$		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{AW}	A0–A13 Setup before $\overline{WR}$ Deasserted	$0.75t_{CK} - 15+w$		ns
t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted	$0.25t_{CK} - 10$		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns
		w = wait states × (t_{CK})		

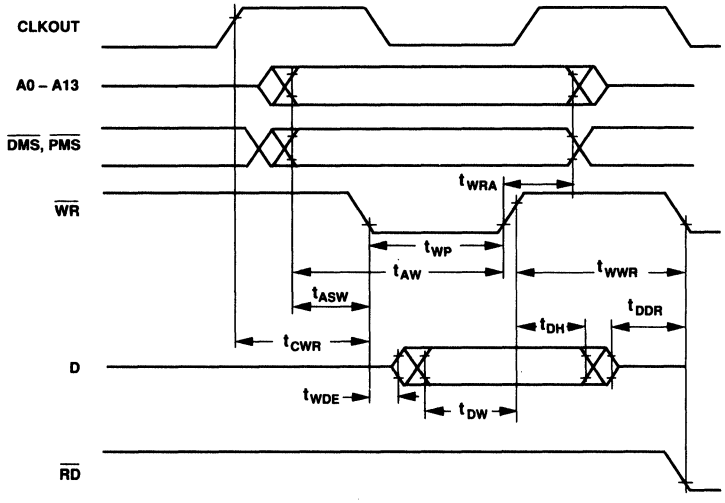


Figure 3. Memory Write

Parameter		ADSP-2105-40 Min	Max	Unit
Serial Port				
Timing Requirement:				
t_{SCK}	SCLK Period	97.6		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	10		ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	10		ns
t_{SCP}	$SCLK_{in}$ Width	38		ns
Switching Characteristic:				
t_{CC}	CLKOUT High to $SCLK_{out}$	$0.25t_{CK}$	$0.25t_{CK}$ + 15	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		25	ns
t_{RH}	TFS/RFS_{out} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{out} Delay from SCLK High		25	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS_{in} (alt) to DT Enable	0		ns
t_{TDV}	TFS_{in} (alt) to DT Valid		20	ns
t_{SCDD}	SCLK High to DT Disable		30	ns

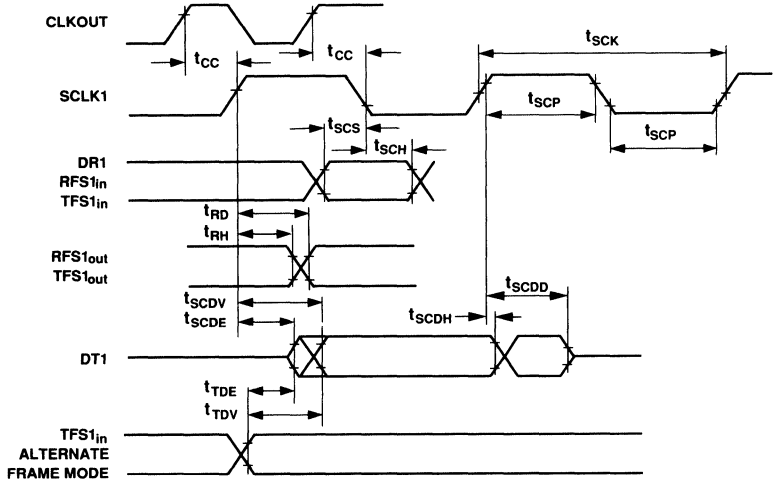


Figure 4. Serial Port

ANALOG DEVICES

DSP Microcomputer with Host Interface Port

ADSP-2111

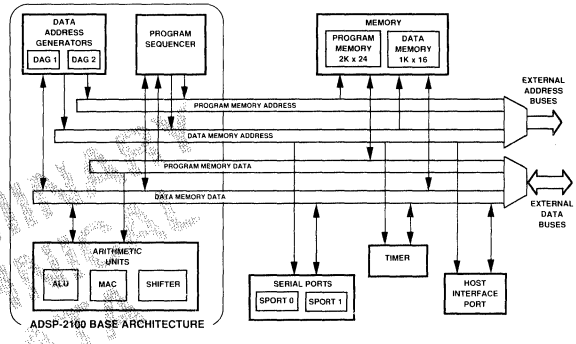
FEATURES

Complete DSP Microcomputer
60 ns Instruction Cycle Time from 16.67 MHz Crystal
ADSP-21XX Family Code & Function Compatible
2K Words of On-Chip Program Memory RAM
1K Word of On-Chip Data Memory RAM
Host Interface Port Provides Simple Interface to 68000, 80C51, ADSP-2101 and Others
Separate Program and Data Buses On-Chip
Dual Purpose Program Memory for Both Instruction and Data Storage
Three Independent Computational Units: ALU, Multiplier/Accumulator and Barrel Shifter
Two Independent Data Address Generators
Powerful Program Sequencer with: Zero Overhead Looping Conditional Arithmetic Instruction Execution
Two Double-Buffered Serial Ports with Companding Hardware and Automatic Data Buffering
Input and Output Flags
Programmable 16-Bit Interval Timer with Prescaler
Programmable Wait State Generation
Automatic Booting of Internal Program Memory from Byte-Wide External Memory, e.g., EPROM
Automatic Booting of Internal Program Memory from Host Port
Provisions for Multiprecision Computation and Saturation Logic
Single-Cycle Instruction Execution
Single-Cycle Context Switch
Multifunction Instructions
Three Edge- or Level-Sensitive External Interrupts
Low Power Dissipation in Standby Mode
100-Pin PGA and 100-Lead PQFP
MIL-STD-883 Compliant Version Available

GENERAL DESCRIPTION

The ADSP-2111 is a single-chip microcomputer optimized for digital signal processing (DSP) and other high-speed numeric processing applications. Its instruction set is a fully compatible superset of the ADSP-2100 instruction set. It combines the complete ADSP-2100 architecture (three computational units, data address generators and a program sequencer) with two serial ports, a host interface port, a programmable timer, extensive interrupt capabilities and on-chip program and data memory RAM. The ADSP-2111 has 1K words of (16-bit) data memory RAM and 2K words of (24-bit) program memory RAM on chip.

FUNCTIONAL BLOCK DIAGRAM



Fabricated in a high-speed, 1.0 micron, double-layer metal CMOS process, the ADSP-2111 operates with a 60 ns instruction cycle time. Every instruction executes in a single cycle. Fabrication in CMOS results in low power operation.

The ADSP-2111's flexible architecture and comprehensive instruction set support a high degree of operational parallelism. In one cycle the ADSP-2111 can:

- generate the next program address
- fetch the next instruction
- perform one or two data moves
- update one or two data address pointers
- perform a computational operation
- receive and transmit data via the two serial ports
- receive and/or transmit data via the host interface port

Development System

The ADSP-2111 is supported by a complete set of tools for software and hardware system development. The Development Software is a set of modules that supports all ADSP-2100 family processors. The System Builder provides a high-level method for defining the architecture of systems under development. The Assembler produces object code and the Linker combines object modules and library calls into an executable file. The Simulator provides an interactive instruction-level simulation with a reconfigurable user interface. A PROM Splitter generates PROM programmer compatible files. The C Compiler generates ADSP-2111 assembly source code.

9

Emulators aid in the hardware debugging of ADSP-2111 systems. The full featured emulator performs a full range of emulation functions including trace and triggering. EZ-Tools are low cost, easy-to-use hardware tools. The EZ-ICE™ emulator provides basic functions like changing register values and setting breakpoints. The EZ-LAB™ demonstration board is a complete ADSP-2111 system that executes EPROM-based programs.

Additional Information

This data sheet provides a general overview of ADSP-2111 functionality. For additional information on the architecture and instruction set of the processor, refer to the *ADSP-2111 User's Manual*. For more information about the Development System and ADSP-2111 programmer's reference information, refer to the *ADSP-2100 Family Development Software Manuals* and the *ADSP-2111 Emulator Manual*.

ARCHITECTURE OVERVIEW

Figure 1 is an overall block diagram of the ADSP-2111. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC) and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations. The shifter can be used to efficiently implement numeric format control including multiword floating-point representations.

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The internal result (R) bus directly connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient use of these computational units. The sequencer supports conditional jumps, subroutine calls and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-2111 executes looped code with zero overhead; no explicit jump instructions are required to maintain the loop.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers. The circular buffering feature is also used by the serial ports for automatic data transfers; these are described on the next page in "Serial Ports."

Efficient data transfer is achieved with the use of five internal buses.

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus allowing memory to expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. The $\overline{BMS}$, $\overline{DMS}$ and $\overline{PMS}$ signals indicate for which memory space the external buses are being used.

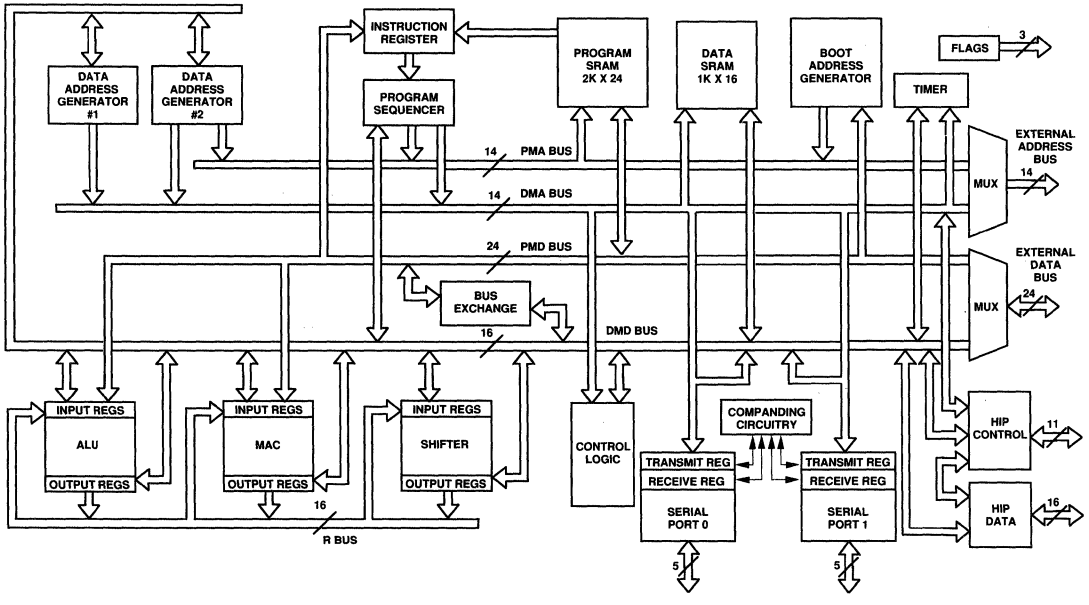


Figure 1. ADSP-2111 Block Diagram

Parameter		ADSP-2111-52 Min	Max	Unit
Memory Read				
Timing Requirement:				
t_{RDD}	$\overline{RD}$ Low to Data Valid		$0.5t_{CK} - 15+w$	ns
t_{AA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid		$0.75t_{CK} - 20+w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristic:				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 10+w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 10$	$0.25t_{CK} + 10$	ns
t_{ASR}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 15$		ns
t_{RDA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 10$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 10$		ns
		w = wait states × (t_{CK})		

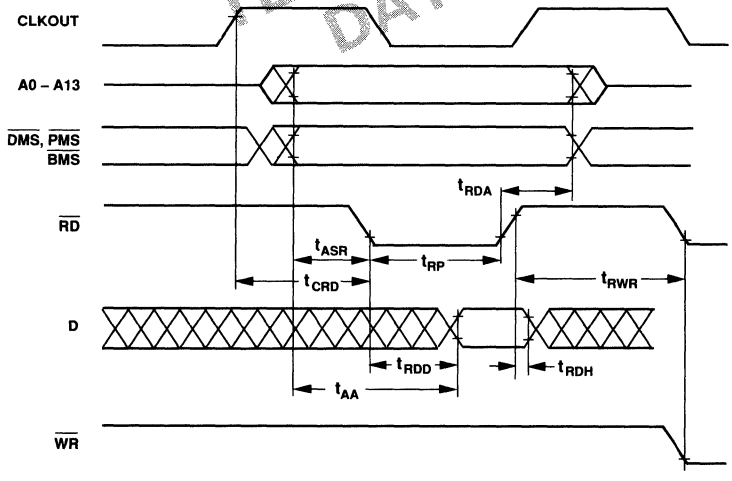


Figure 2. Memory Read

Parameter		ADSP-2111-52 Min	Max	Unit
Memory Write				
Switching Characteristic:				
t_{DW}	Data Setup before $\overline{WR}$ High	$0.5t_{CK} - 20+w$		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK} - 10$		ns
t_{WP}	$\overline{WR}$ Pulse Width	$0.5t_{CK} - 10+w$		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	$0.25t_{CK} - 15$		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK} - 10$		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK} - 10$	$0.25t_{CK} + 10$	ns
t_{AW}	A0–A13 Setup before $\overline{WR}$ Deasserted	$0.75t_{CK} - 25+w$		ns
t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted	$0.25t_{CK} - 10$		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 10$		ns
		w = wait states × (t_{CK})		

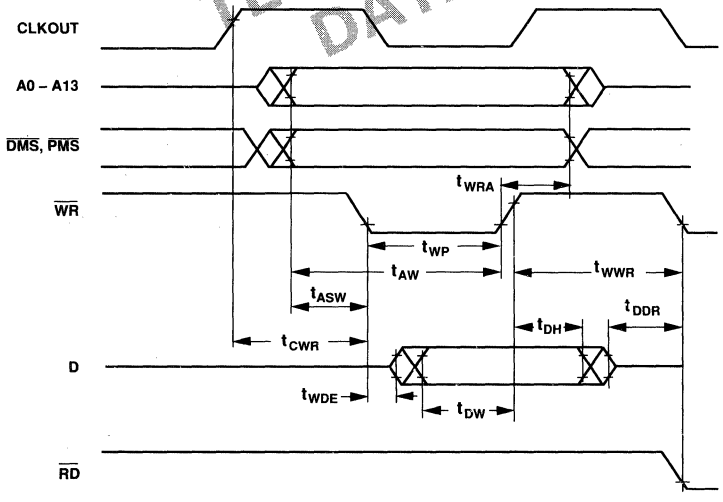


Figure 3. Memory Write

ANALOG DEVICES

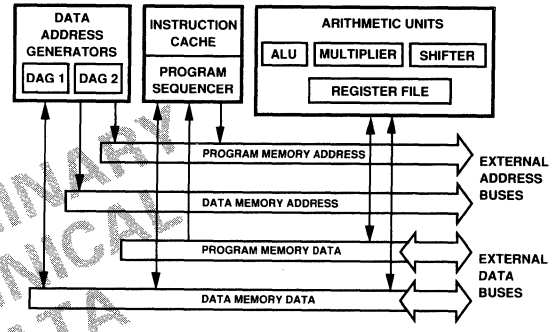
IEEE Floating-Point DSP Microprocessor

ADSP-21020

FEATURES

20 MHz IEEE Floating-Point Processor
IEEE 32-Bit Single-Precision and 40-Bit Extended Single-Precision Floating-Point Formats
32-Bit Fixed-Point Formats, Integer and Fractional
Separate Program and Data Buses Extended Off-Chip
Dual Purpose Program Memory Contains Both Instructions and Data
Three Independent Computation Units: ALU, Multiplier, Shifter
Single-Cycle Parallel Operation of Multiplier and ALU
Two Independent Address Generators
Addressing Support for Page-Mode DRAMs
Powerful Program Sequencer
Zero Overhead Loops
Conditional Execution
32-Word, High-Performance Instruction Cache
Programmable Interval Timer
Programmable and/or Hardware-Controlled Memory Wait States
Alternate Register Sets for Single-Cycle Context Switch
Large Instruction Set, Single-Cycle Instruction Execution
Four Edge- or Level-Sensitive External Interrupts
Four Input/Output Flags
50 ns Instruction Cycle Time
223-Pin PGA Package

SIMPLIFIED BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADSP-21020 is the first member of Analog Devices' family of single-chip, programmable, IEEE floating-point processors optimized for digital signal processing applications. Its architecture is similar to that of Analog Devices' ADSP-2100 family of fixed-point DSP processors.

The ADSP-21020 features:

- Independent Parallel Computation Units
  The arithmetic/logic unit (ALU), multiplier and shifter perform single-cycle instructions. The units are architecturally arranged in parallel, maximizing computational throughput. A single multifunction instruction executes parallel ALU and multiplier operations. These computation units support IEEE single-precision (32-bit) floating-point, extended 40-bit floating-point and 32-bit fixed-point data formats.
- Single-Cycle Fetch of Instruction and Two Operands
  The ADSP-21020 uses a modified Harvard architecture in which data memory stores data and program memory stores both instructions and data. Because of its separate program and data memory buses and its high-performance instruction cache, the processor can fetch an operand from data memory, an operand from program memory, and an instruction from the cache simultaneously.
- Hardware Circular Buffers
  The ADSP-21020 provides hardware to implement circular buffers in memory, which are common in digital filters and Fourier transform implementations. It handles address pointer wraparound, reducing overhead (thereby increasing performance) and simplifying implementation. Circular buffers can start and end at any location.
- Flexible Instruction Set
  The ADSP-21020's 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21020 can conditionally execute a computation, a data memory access and a branch in a single instruction.

9

ARCHITECTURE OVERVIEW

Figure 1 is a block diagram of the ADSP-21020. The processor features:

- Three Computation Units—ALU, Multiplier and Shifter —with a shared data register file
- Two Address Generators
- Program Sequencer with Instruction Cache
- Timer
- Memory Buses and Interface

Computation Units

The ADSP-21020 contains three independent computation units: an ALU, a multiplier with fixed-point accumulator and a shifter. For meeting a wide variety of processing needs, the computation units process data in three formats: 32-bit fixed-point, 32-bit floating-point and 40-bit floating-point. The floating-point operations are single-precision IEEE-compatible (IEEE Standard 754/854). The 32-bit floating-point format is the standard IEEE format, whereas the 40-bit IEEE extended-precision format has eight more LSBs of mantissa for additional accuracy.

The multiplier performs floating-point and fixed-point multiplication as well as fixed-point multiply/add and multiply/subtract operations. Integer products are 64 bits wide, and the accumulator is 80 bits wide. The ALU performs 45 standard arithmetic and logic operations, supporting both fixed-point and floating-point formats. The shifter performs 19 operations, including logical and arithmetic shifts, bit manipulation, field deposit, and extract and derive exponent operations, on 32-bit operands.

The computation units perform single-cycle operations; there is *no* computation pipeline. The units are connected in parallel rather than serially. The output of any unit may be the input of any unit on the next cycle.

In a *multifunction* computation, the ALU and multiplier perform independent simultaneous operations. A 10-port register file is used for transferring data between the computation units and the data buses, and for storing intermediate results. The register file has two sets (primary and alternate) of sixteen 40-bit registers each, for fast context switching. The primary or alternate set of each half of the register file (top eight or bottom eight registers) is selected independently.

Address Generators and Program Sequencer

Two dedicated address generators and a program sequencer supply addresses for memory accesses. Thus the computation units never need to be used to calculate addresses. Because of its instruction cache, the ADSP-21020 can simultaneously fetch an instruction and access data in both off-chip program memory and off-chip data memory in a single cycle. If the instruction is in the cache, there is no need to halt or wait for data.

The data address generators (DAGs) provide memory addresses when external memory data is transferred over the parallel memory ports to or from internal registers. Dual data address generators enable the processor to output two simultaneous addresses for dual operand reads and writes. DAG1 supplies 32-bit addresses to data memory. DAG2 supplies 24-bit addresses to program memory for program memory data accesses.

Each DAG keeps track of up to eight address pointers, eight modifiers, eight length values and eight base values. A pointer used for indirect addressing can be modified by a value in a specified register, either before (pre-modify) or after (post-modify) the access. To implement automatic modulo addressing for circular buffers, the ADSP-21020 provides length values that can be associated with each pointer. Base values for pointers allow relocatable data storage. Each DAG register has an alternate register that can be activated for fast context switching.

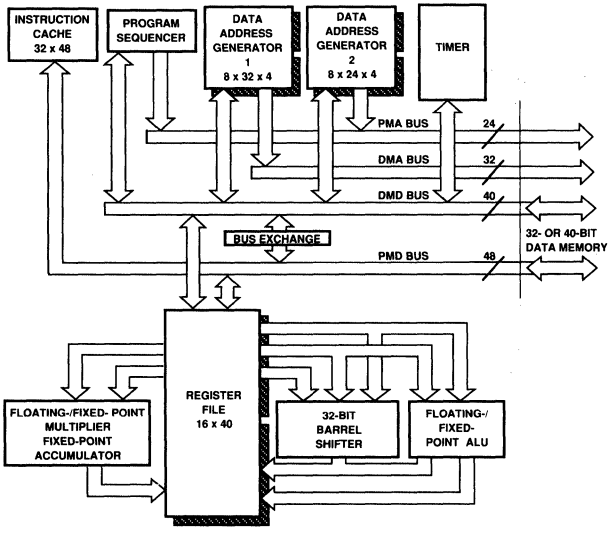


Figure 1. ADSP-21020 Block Diagram

The program sequencer supplies instruction addresses to the program memory. It controls loop iterations and evaluates conditional instructions. To execute looped code with zero overhead, the ADSP-21020 maintains an internal loop counter and loop stack. No explicit jump instructions are required to loop or to decrement and test the counter.

The ADSP-21020 derives its high clock rate from pipelined *fetch*, *decode* and *execute* cycles. External memories have more time to complete an access than if there were no decode cycle; consequently, ADSP-21020 systems can be built using slower and therefore less expensive memories.

The program sequencer includes a high-performance instruction cache. This 2-way, set associative cache holds 32 instructions. Only the instructions whose fetches conflict with program memory data accesses are cached, so the ADSP-21020 can perform a program memory data access and execute the corresponding instruction in the same cycle. The program sequencer fetches the instruction from the cache instead of program memory, and the ADSP-21020 can simultaneously access data in program memory.

Interrupts

The ADSP-21020 has four external hardware interrupts, nine internally generated interrupts and eight software interrupts. For the external user interrupts and the internal timer interrupt, the ADSP-21020 automatically stacks the arithmetic status and mode (MODE1) registers in parallel with servicing the interrupt, allowing four nesting levels of very fast service for these interrupts.

An interrupt can occur at any time while the ADSP-21020 is executing a program. Internal events that generate interrupts include arithmetic exceptions, allowing fast trap handling and recovery.

Development System

The ADSP-21020 is supported with a complete set of software and hardware development tools. The ADSP-21020 Development System includes development software for software design and an emulator for hardware debugging.

Parameter		Min	Max	Min	Max	Min	Max	Unit
Memory Read		**20 MHz (50 ns)**		**15 MHz (66 ns)**		**Frequency Dependency** t_{CK} = T ns; DT = T − 50 ns		
Switching Characteristic								
t_{DARL}	Address, Select valid to $\overline{xRD}$	11		17		11+3DT/8		ns
t_{DRHA}	$\overline{xRD}$ deasserted to Address, Select invalid	0		0		0		ns
t_{DCKA}	CLKIN rising edge to Address valid		18		16		18–DT/8	ns
t_{DAP}	Address valid to xPAGE valid		4		4		4	ns
t_{DCKP}	CLKIN rising edge to xPAGE valid		21		19		21–DT/8	ns
t_{DCKR}	CLKIN rising edge to $\overline{xRD}$ deasserted		11		9		11−DT/8	ns
Timing Requirement								
t_{RDDV}	Data Valid to CLKIN rising edge	4		6		4+DT/8		ns
t_{HRD}	CLKIN rising edge to Data invalid	8		6		8−DT/8		ns
t_{DAD}	Address, Select valid to external Data valid		36		53		36+DT	ns
t_{DRLD}	$\overline{xRD}$ asserted to external Data valid		25		27		25+5DT/8	ns
t_{DRHDZ}	$\overline{xRD}$ deasserted to Data high impedance	0	15	0	22	0	15+7DT/16	ns
t_{HDRH}	$\overline{xRD}$ deasserted to Data invalid	0		0		0		ns
t_{DAAK}	Address valid to xACK valid		21		36		21+7DT/8	ns
t_{DRAK}	$\overline{xRD}$ asserted to xACK valid		8		16		8+DT/2	ns
t_{SAK}	xACK valid to CLKIN rising edge	11		7		11−DT/4		ns
t_{HAK}	xACK invalid to CLKIN rising edge		2		−2		2−DT/4	ns

x = PM or DM; Select = $\overline{PMS1\text{-}0}$, $\overline{DMS3\text{-}0}$

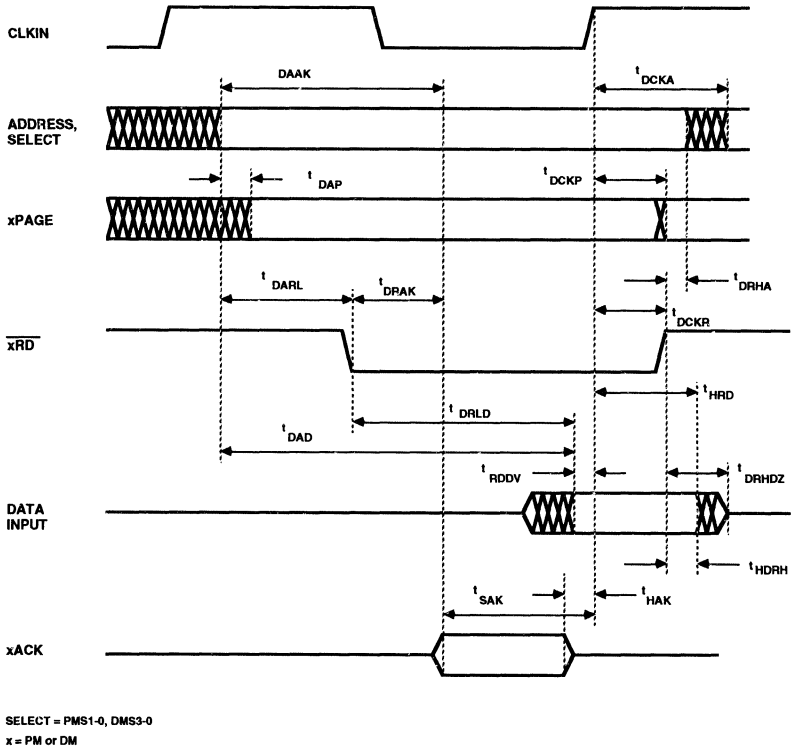


Figure 2. Memory Read Timing

Parameter		Min	Max	Min	Max	Min	Max	Unit
Memory Write		**20 MHz (50 ns)**		**15 MHz (66 ns)**		**Frequency Dependency** t_{CK} = T ns; DT = T − 50 ns		
Switching Characteristic								
t_{DAWH}	Address, Select valid to $\overline{xWR}$ deasserted	36		52		36+15DT/16		ns
t_{DAWL}	Address, Select valid to $\overline{xWR}$ asserted	10		16		10+3DT/8		ns
t_{WW}	$\overline{xWR}$ pulse width	25		34		25+9DT/16		ns
t_{DDWH}	Data valid to $\overline{xWR}$ deasserted	17		25		17+DT/2		ns
t_{WDDV}	CLKIN rising edge to Data valid		38		43		38+5DT/16	ns
t_{DDZL}	CLKIN rising edge to Data low impedance	18		23		18+5DT/16		ns
t_{DWHA}	$\overline{xWR}$ deasserted to Address, Select invalid	2		3		2+DT/16		ns
t_{DWHDZH}*	$\overline{xWR}$ deasserted to Data high impedance	4	15	5	16	4+DT/16	15+DT/16	ns
t_{DCKA}	CLKIN rising edge to Address valid		18		16		18−DT/8	ns
t_{DAP}	Address valid to xPAGE valid		4		4		4	ns
t_{DCKP}	CLKIN rising edge to xPAGE valid		21		19		21−DT/8	ns
t_{DCKW}	CLKIN rising edge to $\overline{xWR}$ deasserted		7		4		7−3DT/16	ns
Timing Requirement								
t_{DAAK}	Address valid to xACK valid		21		35		21+7DT/8	ns
t_{DWAK}	$\overline{xWR}$ valid to xACK valid		8		16		8+DT/2	ns
t_{SAK}	xACK enabled to CLKIN rising edge	11		15		11+DT/4		ns
t_{HAK}	xACK disabled to CLKIN rising edge		2		6		2+DT/4	ns

x = PM or DM; Select = $\overline{PMS1\text{-}0}$, $\overline{DMS3\text{-}0}$.

*t_{DWHDZH} is the time from the rising edge of $\overline{xWR}$ to when the ADSP-21020 stops driving the data bus, until the next write or read cycle. In between the two memory accesses, the data output remains valid on the output bus for a time determined by the system's total bus capacitance and the total leakage current.

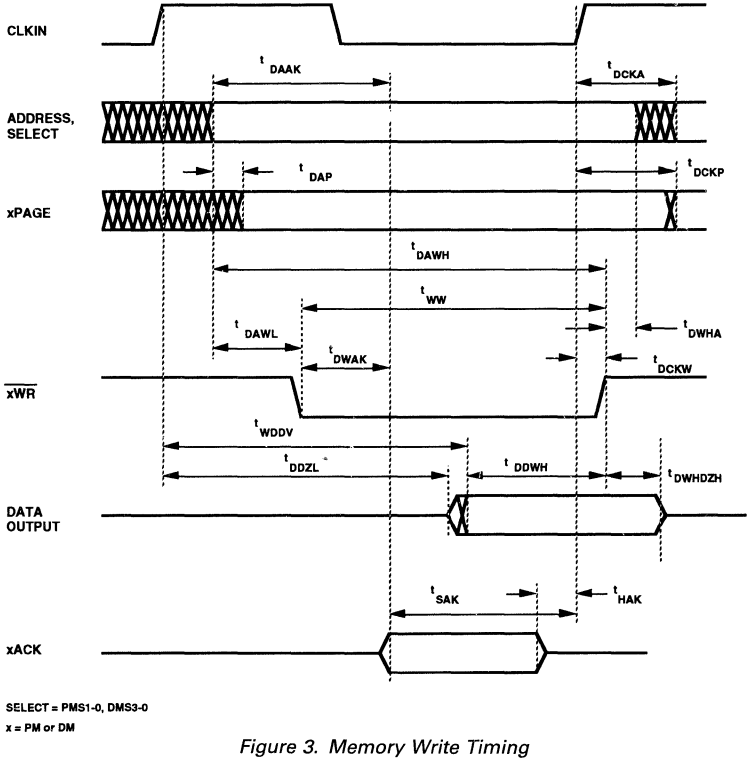


Figure 3. Memory Write Timing

Other Products
Contents

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Selection Guide
Analog-to-Digital Converters

Sampling Converters

Model	Res Bits	Through-put Rate kSPS max	SHA BW kHz typ[1]	Reference Volt Int/Ext[2]	Bus Interface Bits[3]	Package Options[4]	Temp Range[5]	Page[6]	Comments
AD7821	8	1000	100	0–5 V, Ext	8, µP	2, 3, 4, 5, 6	I, M	C II	CMOS, Bipolar or Unipolar Operation
AD7820	8	500	14	0-5 V, Ext	8, µP	2, 3, 4, 5, 6	I, M	C II	CMOS, 8-Bit Sampling ADC
AD7569	8	400	200	Int	8, µP	2, 3, 4, 5, 6	C, I, M	C II	CMOS, Complete I/O Port with DAC, ADC, SHA, Amps and Reference
AD7669	8	400	200	Int	8, µP	2, 5, 6	C, I, M	C II	CMOS, Complete I/O Port with 2 DACs, ADC, SHA, Amps and Reference
AD7769	8	400	200	Ext	8, µP	2, 5	C	C II	CMOS, Complete 2-Channel I/O Port with Input/Output Signal Conditioning
AD7824	8	400	10	0–5 V, Ext	8, µP	2, 3, 6	C, I, M	C II	CMOS, 4-Channel, 8-Bit Sampling ADC
AD7828	8	400	10	0–5 V, Ext	8, µP	2, 3, 4, 5	C, I, M	C II	CMOS, 8-Channel, 8-Bit Sampling ADC
AD7575	8	190	50	1.23 V, Ext	8, µP	2, 3, 4, 5	C, I, M	C II	CMOS, Low Cost
***AD7776**	10	500	50	2.0 V, Int/Ext	10, µP	2, 6	C, I	C II	CMOS, Single Channel Complete Sampling ADC, Single Supply, Twos Complement Output Code
***AD7777**	10	500	50	2.0 V, Int/Ext	10, µP	2, 6	C, I	C II	CMOS, 4-Channel Complete ADC for Single or Simultaneous Dual Channel Sampling, Single Supply
***AD7778**	10	500	50	2.0 V, Int/Ext	10, µP	10	C, I	C II	CMOS, 8-Channel Complete ADC for Single or Simultaneous Dual Channel Sampling, Single Supply
AD7579	10	50	25	2.5 V, Ext	8, µP	2, 3, 4, 5	C, I, M	C II	CMOS, Low Cost 10-Bit Sampling ADC
AD7580	10	50	25	2.5 V, Ext	10, µP	2, 3, 4, 5	C, I, M	C II	CMOS, Low Cost 10-Bit Sampling ADC
AD9003	12	1000	10000	Int	12	8	C	C II	12-Bit, 1 MSPS ADC, Single 40-Pin DIP
***AD1671**	12	1250	2000	2.5 V, Int	12	1, 2, 4, 5	C, I, M	C II	Complete, Monolithic 12-Bit, 1.25 MSPS ADC
***AD7886**	12	750	1000	5 V, Ext	12, µP	2, 3, 5	C, I	C II	CMOS, 12-Bit 750 kSPS Sampling ADC
AD678	12	200	1000	5 V, Int	8/12, µP	1, 2, 14	C, I, M	C II	BiMOS, High Impedance High Bandwidth Sampling Input, 10 V Range, AC/DC Tested
***AD1341**	12	150	150	10 V, Int	16, µP	12	C, M	C II	High Speed 8/16 Channel DAS
***AD7893**	12	140	70	2.5 V, Ext	Serial	2, 3, 6	I, M	C II	CMOS, Single Supply Sampling ADC in 8-Pin Package
***AD7892**	12	140	70	2.5 V, Ext	8/12/Serial, µP	2, 3, 6	I, M	C II	±10 V Input, Single Supply Sampling ADC
AD1332	12	125	125	−5 V, Int	12, µP	1	I, M	C II	Complete 12-Bit 125 kHz Sampling ADC for Digital Signal Processing, On-Chip FIFO
***AD7874**	12	29	500	Int (+3 V), Ext	12, µP	2, 3, 4, 6	C, I, M	C II	CMOS, Simultaneous Sampling 4-Channel ADC for ±10 V Input Signals
AD7870	12	100	500	3 V, Int	8/12/Serial, µP	2, 3, 4, 5	C, I, M	C II	CMOS, 100 kHz Throughput, ±3 V Input
***AD7875**	12	100	500	3 V, Int	8/12/Serial, µP	2, 3, 5	C, I, M	C II	CMOS 100 kHz Throughput, 0–5 V Input
***AD7876**	12	100	500	3 V, Int	8/12/Serial, µP	2, 3, 6	I, M	C II	CMOS, 100 kHz Throughput, ±10 V Input
AD7878	12	100	500	3 V, Int	12, µP	2, 3, 4, 5	C, I, M	C II	CMOS, 100 kHz Throughput, ±3 V Input, On-Chip FIFO
***AD1674**	12	100	500	10 V, Int	8/12, µP	1, 2, 6	C, I, M	C II	Complete AD574A Pinout Compatible, Sampling Input, AC/DC Tested
***AD7890**	12	100	50	2.5 V, Ext	Serial	2, 3, 6	I, M	C II	±10 V Input 8-Channel Single Supply Sampling ADC
***AD7891**	12	100	50	2.5 V, Ext	12, µP	10	I, M	C II	±10 V Input 8-Channel Single Supply Sampling ADC

Model	Res Bits	Through-put Rate kSPS max	SHA BW kHz typ[1]	Reference Volt Int/Ext[2]	Bus Interface Bits[3]	Package Options[4]	Temp Range[5]	Page[6]	Comments
***AD7868**	**12**	**83**	**500**	**3 V, Int**	**Serial, µP**	**2, 3, 6**	**I, M**	**C II**	**CMOS, Complete I/O Port with 12-Bit ADC and 12-Bit DAC**
AD1334	**12**	**67**	**235**	**−5 V, Int**	**12, µP**	**1**	**I, M**	**C II**	**Four- Channel 67 kHz 12-Bit Sampling ADC, On-Chip FIFO**
***AD7880**	**12**	**66**	**33**	**5 V, Ext**	**12, µP**	**2, 3, 6**	**I**	**C II**	**Single +5 V Supply, Low Power Shutdown**
AD368	12	50	40–1000	6.3 V, Int	12	1	I, M	C II	Complete 12-Bit ADC, PGA with Gains of 1, 8, 64, 512
AD369	12	50	40–1000	6.3 V, Int	12	1	I, M	C II	Complete 12-Bit ADC, PGA with Gains of 1, 10, 100, 500
AD363R	12	25		10 V, Int	12, µP	1	C, M	C II	16-Channel, 12-Bit DAS
AD364R	12	20		10 V, Int	12, µP	1	C, M	C II	High Speed, 16-Channel, 12-Bit DAS with Three-State Buffered Output
AD679	**14**	**128**	**1000**	**5 V, Int**	**8, µP**	**1, 2, 14**	**C, I, M**	**C II**	**BiMOS, High Impedance, High Bandwidth Sampling Input, 10 V Input Range, AC/DC Tested**
AD779	**14**	**128**	**1000**	**5 V, Int**	**14, µP**	**1, 2, 14**	**C, I, M**	**C II**	**BiMOS, High Impedance, High Bandwidth Sampling Input, 10 V Input Range, AC/DC Tested**
***AD7869**	**14**	**83**	**500**	**3 V, Int**	**Serial**	**2, 3, 6**	**C, I**	**C II**	**CMOS, Complete I/O Port with 14-Bit DAC and 14-Bit ADC**
AD7871	**14**	**83**	**500**	**3 V, Int**	**8/14/Serial, µP**	**2, 3, 5**	**C, I, M**	**C II**	**CMOS, Complete Sampling ADC, ±3 V Input**
AD7872	**14**	**83**	**500**	**3 V, Int**	**Serial, µP**	**2, 3, 6**	**C, I, M**	**C II**	**CMOS, Complete, Serial Interface, 16-Pin DIP/SOIC**
DAS1152	14	25	X	10 V, Int	14	Module	I	C II	14-Bit High Accuracy Sampling ADC
DAS1157	14	18	X	10 V, Int	14	Module	I	C II	Low Power Sampling ADC
DAS1153	15	20	X	10 V, Int	15	Module	I	C II	15-Bit High Accuracy Sampling ADC
DAS1158	15	18	X	10 V, Int	15	Module	I	C II	Low Power, 15-Bit Sampling ADC
***AD1382**	**16**	**500**	**2200**	**10 V, Int**	**8, µP**	**1**	**C**	**C II**	**High Speed, Guaranteed Dynamic Performance**
***AD1385**	**16**	**500**	**2200**	**10 V, Int**	**8, µP**	**1**	**C, M**	**C II**	**Similar to AD1382 with Autocalibration Ability, Guaranteed Dynamic Performance**
***AD7884**	**16**	**166**	**83**	**3 V, Ext**	**16, µP**	**2, 3, 5**	**I, M**	**C II**	**CMOS, Low Power (250 mW), 5.3 µs Conversion**
***AD7885**	**16**	**166**	**83**	**3 V, Ext**	**8, µP**	**2, 3, 5**	**I, M**	**C II**	**Similar to AD7884, 28-Pin Package, Byte Output**
***AD675**	**16**	**100**	**1000**	**3–10 V, Ext**	**8/Serial, µP**	**1, 2**	**C, I, M**	**C II**	**Autocalibrating, 24-Pin DIP ADC, AC/DC Tested**
***AD676**	**16**	**100**	**1000**	**3–10 V, Ext**	**16, µP**	**1, 2**	**C, I, M**	**C II**	**Similar to AD675 but in 28-Pin DIP, Parallel Output**
AD1380	**16**	**50**	**900**	**Int**	**16/Serial**	**1**	**C**	**C II**	**Low Cost, 16-Bit Sampling ADC**
DAS1159	16	18	X	10 V, Int	16	Module	I	C II	Low Power, 16-Bit Sampling ADC

[1]X indicates that the internal SHA bandwidth is not specified in kHz.

[2]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.

[3]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 13-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.

[4]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-In-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.

[5]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.

[6]C I = Data Converter Reference Manual, Volume I; C II = Data Converter Reference Manual, Volume II; D = Data sheet available, consult factory; L = Linear Products Databook; P = Precision Monolithics Division Databook.

Boldface Type: Product recommended for new design.

*New product.

Selection Guide
Analog-to-Digital Converters

Nonsampling Converters

Model	Res Bits	Conv Rate µs max	Reference Voltage Int/Ext[1]	Bus Interface Bits[2]	Package Options[3]	Temp Range[4]	Page[5]	Comments
ADC-908	8	6.0	−10 V, Ext	8, µP	2, 3, 4, 6	C, I, M	C II	CMOS, +5 V Operation, Fast
AD670	8	10	Int	8, µP	1, 2, 4, 5	C, I, M	C II	Single +5 V Supply, Including In-Amp and Reference
AD7576	8	10	1.23 V, Ext	8, µP	2, 3, 4, 5	C, I, M	C II	CMOS, Low Cost, Single Supply
PM-7574	8	15	−10 V, Ext	8, µP	2, 3, 4, 6	C, I, M	C II	CMOS, +5 V Operation
AD7574	**8**	**15**	**−10 V, Ext**	**8, µP**	**2, 3, 4**	**C, I, M**	**C II**	**CMOS, +5 V Operation**
AD570	8	25	Int	8	1	C, M	C II	
AD673	8	30	Int	8, µP	1, 2, 5	C, M	C II	
AD7581	8	66.7	−5 V to (−15 V), Ext	8, µP	2, 3, 5	C, I	C II	CMOS 8-Bit ADC
AD579	10	1.8	10 V, Int	10/Serial	1	C, M	C II	High Speed with Low Power
ADC-910	**10**	**6.0**	**2.5 V, Int**	**8, 10, µP**	**3**	**C, I, M**	**C II**	**Bipolar, Fast with Byte Output**
AD571	10	25	Int	10	1	C, M	C II	Complete 10-Bit ADC
AD573	**10**	**30**	**Int**	**8/10, µP**	**1, 2, 5**	**C, M**	**C II**	**Complete 10-Bit ADC, Byte or Parallel Interface**
AD575	10	30	Int	Serial	1, 2	C, M	C II	Complete 10-Bit ADC with Serial Interface
AD671-500	**12**	**0.5**	**5 V, Ext**	**12**	**1, 2**	**C, M**	**C II**	**12-Bit 500 ns Monolithic ADC**
AD671-750	**12**	**0.75**	**5 V, Ext**	**12**	**1, 2**	**C, M**	**C II**	**12-Bit 750 ns Monolithic ADC**
***AD7586**	**12**	**1**	**−4 V, Ext**	**12, µP**	**1, 2, 5**	**C, I**	**C II**	**CMOS 12-Bit, 1 MHz ADC**
AD578	12	3	10 V, Int	12	1	C, M	C II	Complete, 3 µs, 12-Bit ADC
***AD7572A**	**12**	**3**	**Int**	**8/12, µP**	**2, 3, 4, 6**	**C, I, M**	**C II**	**Improved Version of Industry Standard**
AD7672	12	3	−5 V, Ext	12, µP	2, 3, 4, 5	C, I, M	C II	CMOS, Unipolar or Bipolar, −12 V, +5 V Supply
AD5240	12	5	6.3 V, Int	12	1	C, M	C II	Industry Standard
AD7572	12	5	−5.25 V, Int	8/12, µP	2, 3, 4, 5	C, I, M	C II	CMOS 12-Bit ADC
***ADC-170**	**12**	**5.6**	**−5.25 V, Ext**	**Serial**	**2, 3, 6**	**I, M**	**C II**	**Complete, 5.6 µs, 12-Bit ADC in 8-Pin Mini-DIP**
***AD774B**	**12**	**8**	**10 V, Int**	**8/12, µP**	**1, 2, 6**	**C, I, M**	**C II**	**Faster Version of AD674B with 8 µs Conversion**
AD ADC84/85	12	10	6.3 V, Int	12	1	C, I, M	C II	Industry Standard
***ADC-912A**	**12**	**10**	**−5 V, Ext**	**12, µP**	**2, 3, 6**	**I, M**	**C II**	**CMOS, Improved Version of ADC-912**
ADC-912	12	12.5	−5 V, Ext	12, µP	2, 3, 6	C	C II	CMOS, Low Transition Noise
AD5210	12	13	−10 V, Int/Ext	12	1	I, M	C II	Industry Standard (AD5211/12/14/15)
AD674A	12	15	10 V, Int	8/12, µP	1	C, M	C II	Complete 12-Bit ADC, Industry Standard Pinout
***AD674B**	**12**	**15**	**10 V, Int**	**8/12, µP**	**1, 2, 6**	**C, I, M**	**C II**	**Improved Monolithic Version of AD674A and AD574A**
AD572	12	25	10 V, Int	12	1	I, M	C II	12-Bit Successive Approximation ADC
AD ADC80	12	30	6.3 V, Int	12	1	I	C II	Industry Standard
AD574A	**12**	**35**	**10 V, Int**	**8/12, µP**	**1, 2, 4, 5**	**C, M**	**C II**	**Complete ADC with Reference and Clock**
AD5200	12	50	−10 V, Int/Ext	12	1	I, M	C II	Industry Standard (AD5201/02/04/05)
AD7578	**12**	**100**	**5 V, Ext**	**8, µP**	**1, 2**	**C, I, M**	**C II**	**CMOS, 1 LSB Total Unadjusted Error**
AD7582	**12**	**100**	**5 V, Ext**	**8, µP**	**1, 2, 5**	**C, I, M**	**C II**	**CMOS, 4 Channel, 1 LSB Total Unadjusted Error**

Model	Res Bits	Conv Rate µs max	Reference Voltage Int/Ext[1]	Bus Interface Bits[2]	Package Options[3]	Temp Range[4]	Page[5]	Comments
AD1377	16	10	Int	16, Serial	1	C	C II	Complete, High Speed 16-Bit ADC Operation over −25°C to +85°C
AD1376	16	17	Int	16, Serial	1	C	C II	Complete 16-Bit Converter; Industry Standard Pinout
***AD1378**	**16**	**17**	**Int**	**16, Serial**	**1**	**M**	**C II**	**Complete 16-Bit Converter; MIL Temp Range; Industry Standard Pinout**
ADC1140	16	35	10 V, Int	16	Module	C	C II	16-Bit ADC, Operates over −25°C to +85°C Temperature Range
AD ADC71	16	50	6.3 V, Int	16	1	C	C II	Industry Standard
AD ADC72	16	50	6.3 V, Int	16	1	C, I	C II	Industry Standard
AD1170	**18**	**1000**	**5 V, Int**	**8**	**2**	**C**	**C II**	**7 to 22-Bit Programmable Integrating ADC**

[1]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.

[2]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 13-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.

[3]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-In-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.

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Boldface Type: Product recommended for new design.

*New product.

Selection Guide
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High Speed ADCs

Model	Res Bits	Through-put Rate MSPS min	Full Power BW MHz typ	Reference Voltage Int/Ext[1]	Bus Interface Bits[2]	Package Options[3]	Temp Range[4]	Page[5]	Comments
AD9006	6	470	550	±1 V, Ext	6, µP	4, 12	C, M	C II	470 MSPS, 6-Bit ADC; 8.0 pF Input Capacitance
AD9016	6	550		±1 V, Ext	Dual 6, µP	4, 12	C, M	C II	AD9006 with 1:2 Demultiplexed Data Output Demultiplexing Circuitry
AD9000	6	50	20	0.5–2 V, Ext	6	1, 3	C, M	C II	MIL-STD-883, Rev. C, Devices Available; Low Error Rate
AD9028	8	300	250	–2 V, Ext	8	4	C, M	C II	300 MSPS, 8-Bit ADC, Guaranteed Dynamic Performance
AD9038	8	300	250	–2 V, Ext	Dual 8	4	C, M	C II	AD9028 with On-Board 1:2 Demultiplexed Data Outputs
AD770	8	200	250	±2 V, Ext	8	1	C, M	C II	High Bandwidth, Error Correction
AD9002	8	125	160	0.1–(–2.1) Ext	8	1, 4	I, M	C II	Single Supply, Low Power, Low Input Capacitance, MIL-STD-883, Rev. C Device Available
AD9012	8	75	160	–2 V, Ext	8	3, 4	I, M	C II	TTL Outputs, Low Power, Low Input Cap
*AD9058	8	50	175	+2 V, Int	8	1, 5, 14	C, M	C II	Dual 8-Bit, TTL Output
*AD9040	10	40	50	+1.2 V	10	3, 4, 5	C, M	C II	Low Cost, High Performance 10-Bit TTL Monolithic
*AD9032	12	25	150	Int	12	8	C, M	C II	World's Fastest Complete 12-Bit ADC
*AD9034	12	20	150	Int	12	8	C, M	C II	20 Ms
*AD9005A	12	10	38	Int	12	8	C, M	C II	Complete 12-Bit ADC with T/H, Reference and Timing Circuitry
*AD1671	12	1.25	2	2.5 V, Int	12	1, 2, 4, 5	C, I, M	C II	Complete, Monolithic 12-Bit, 1.25 MSPS ADC
AD9003	12	1	10	Int	12	8	C	C II	12-Bit, 1 MSPS ADC, Single 40-Pin DIP
*AD7886	12	.75	1	+5 V, Ext	12, µP	1, 2, 5	C, I, M	C II	CMOS, 12-Bit 750 kSPS Sampling ADC
*AD9014	14	10	60	Int	14	Board	C	C II	Wide Spurious Free Dynamic Range

Sigma-Delta ADCs

Model	Res Bits	Input BW kHz	Through-put Rate kHz	Reference Voltage Int/Ext[1]	Bus Interface Bits[2]	Package Options[3]	Temp Range[4]	Page[5]	Comments
***AD776**	**16**	**50**	**100 to 400**	**2 V, Int**	**Serial**	**1, 2**	**C, I, M**	**C II**	**16-Bit 100 kSPS Oversampling ADC, Single Supply**
***AD7701**	**16**	**10 Hz**	**4**	**2.5 V, Ext**	**Serial, µP**	**2, 3, 6**	**I, M**	**C II**	**16-Bit Sigma-Delta ADC, 0.1–10 Hz Input Bandwidth**
***AD28msp02**	**16**	**4**	**8**	**2.5, Ext**	**Serial, µP**	**6**	**C**	**C I**	**Complete Voice Band Linear Codec with On-Chip Filtering, Single Supply**
***AD28msp01**	**16**	**3.4**	**7.2/8.0/9.6**	**2.5, Ext**	**Serial, µP**	**6**	**C**	**C I**	**Complete Analog Front End for High Performance, DSP-Based Modems, Single Supply**
***AD7716**	**20**	**18.5 to 300 Hz**	**0.075 to 1.145**	**2.5 V, Int**	**Serial**	**2, 6**	**C**	**C II**	**Quad 20-Bit Sigma Delta ADC, Low Power with BW up to 300 Hz**
***AD7703**	**20**	**10 Hz**	**4**	**2.5 V, Ext**	**Serial, µP**	**2, 3, 6**	**I, M**	**C II**	**20-Bit Sigma-Delta ADC, 0.1–10 Hz Input Bandwidth**
***AD7710**	**21**	**DC to 262 Hz**	**0.01 to 1.0**	**2.5 V, Int**	**Serial, µP**	**2, 3, 6**	**I, M**	**C II**	**21-Bit Sigma-Delta Signal Conditioning ADC for Thermocouple or mV Input**
***AD7711**	**21**	**DC to 262 Hz**	**0.01 to 1.0**	**2.5 V, Int**	**Serial, µP**	**2, 3, 6**	**I, M**	**C II**	**Similar to AD7710 but for RTD or mV Input**
***AD7712**	**21**	**DC to 262 Hz**	**0.01 to 1.0**	**2.5 V, Int**	**Serial, µP**	**2, 3, 6**	**I, M**	**C II**	**Similar to AD7710 with Higher Input Voltage Range, More General Purpose**
***AD7713**	**21**	**DC to 52.4 Hz**	**2.0 to 200 Hz**	**2.5 V, Ext**	**Serial, µP**	**2, 3, 6**	**I, M**	**C II**	**Loop Powered 21-Bit Sigma-Delta Signal Conditioning ADC**

[1]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.

[2]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 13-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.

[3]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-In-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.

[4]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.

[5]C I = Data Converter Reference Manual, Volume I; C II = Data Converter Reference Manual, Volume II; D = Data sheet available, consult factory; L = Linear Products Databook; P = Precision Monolithics Division Databook.

Boldface Type: Product recommended for new design.

*New product.

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Multiplexed ADCs

Model	Res Bits	# Chan	Conv Time µs	SHA BW kHz	Bus Interface Bits[1]	Reference Volt Int/Ext[2]	Package Options[3]	Temp Range[4]	Page[5]	Comments
AD7769	**8**	**2**	**2.5**	**200**	**8, µP**	**Ext**	**2, 5**	**C**	**C II**	**CMOS, Complete 2-Channel I/O Port with Input/Output Signal Conditioning**
AD7824	**8**	**4**	**2.5**	**10**	**8, µP**	**0–5 V, Ext**	**2, 3, 6**	**C, I, M**	**C II**	**CMOS, On-Chip Track-Hold**
AD7828	**8**	**8**	**2.5**	**10**	**8, µP**	**0–5 V, Ext**	**2, 3, 4, 5**	**C, I, M**	**C II**	**CMOS, On-Chip Track-Hold**
AD7581	8	8	66.7		8, µP	−10 V, Ext	2, 3, 5	C, I	C II	CMOS, 8-Channel DAS
***AD1341**	**12**	**8/16**	**6.67**		**16, µP**	**10 V, Int**	**12**	**C, M**	**C II**	**High Speed, 16-Channel Programmable 12-Bit DAS with 25 ns Bus Interface**
AD1334	**12**	**4**	**15**	**235**	**12, µP**	**−5 V, Int**	**1**	**I, M**	**C II**	**Four-Channel 65 kHz 12-Bit Sampling ADC for Digital Signal Processing, On-Chip FIFO**
***AD7874**	**12**	**4**	**32.5 (for 4 Channels)**	**500**	**12, µP**	**3 V Int**	**2, 3, 6**	**C, I, M**	**C II**	**CMOS, Simultaneous Sampling Four-Channel 29 kHz ADC for ±10 V Input Signals**
AD363R	12	8/16	40		12, µP	10 V, Int	1	C, M	C II	High Speed, 16-Channel, 12-Bit DAS
AD364R	12	8/16	50		12, µP	10 V, Int	1	C, M	C II	16-Channel, 12-Bit DAS with Three-State Buffers
AD7582	**12**	**4**	**100**		**12, µP**	**4 V–6 V, Ext**	**1, 2, 5**	**C, I, M**	**C II**	**CMOS, 1 LSB Total Unadjusted Error**
***AD7890**	**12**	**8**	**10**	**500**	**Serial, µP**	**2.5 V, Ext**	**2, 3, 6**	**I, M**	**C II**	**CMOS, 8-Channel Multiplexed ADC for ±10 V Input Signals**
***AD7891**	**12**	**8**	**10**	**500**	**12, µP**	**2.5 V, Ext**	**10**	**I, M**	**C II**	**CMOS, 8-Channel Multiplexed ADC for ±10 V Input Signals**

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Digital-to-Analog Converters

Single DACs, Current Output

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Volt Int/Ext (M)[2]	Package Options[3]	Temp Range[4]	Page[5]	Comments
AD9768	**8**	**0.005**	**8, µP**	**−1.26 V, Int**	**1, 4**	**C, M**	**C I**	**Ultrahigh Speed, ECL Compatible, 20 mA Output Current**
DAC-08	**8**	**0.085**	**8**	**Ext (M)**	**2, 3, 4, 6**	**C, I, M**	**C I**	**8-Bit High Speed Multiplying DAC**
DAC-20	8	0.085	8	10 V, Ext	2, 3	C	C I	2-Digit BCD High Speed Multiplying DAC
PM-7524	**8**	**0.10**	**8, µP**	**Ext (M)**	**2, 3, 4, 5, 6**	**C, I, M**	**C I**	**CMOS, Low Cost, 8-Bit Multiplying DAC with Latch**
AD7524	**8**	**0.10**	**8, µP**	**Ext (M)**	**2, 3, 4, 5, 6**	**C, I, M**	**C I**	**CMOS, Low Cost, 8-Bit Multiplying DAC with Latch**
DAC-1408A	8	0.25	8	Ext (M)	2, 3, 6	C, I	C I	8-Bit Multiplying DAC
DAC-1508A	8	0.25	8	Ext (M)	3	M	C I	8-Bit Multiplying DAC
DAC-888	8	0.30	8, µP	Ext (M)	3	I, M	C I	BYTEDAC 8-Bit High Speed Multiplying DAC
AD9720	**10**	**0.005**	**10**	**Int**	**2, 3, 5, 14**	**C, M**	**C I**	**Ultrahigh Speed, ECL Compatible, Low Power, Low Glitch**
AD9721	**10**	**0.005**	**10**	**Int**	**2, 3, 5, 14**	**C, M**	**C I**	**Ultrahigh Speed, TTL Compatible, Low Power, Low Glitch**
DAC-10	**10**	**0.085**	**10**	**Ext (M)**	**2, 3, 6**	**C, M**	**C I**	**10-Bit High Speed Multiplying DAC**
AD561	**10**	**0.25**	**10**	**Int**	**1, 2**	**C, M**	**C I**	**Industry Standard 10-Bit DAC, JAN Part Available**
DAC-100	10	0.300	10	6.6 V, Int	3	C, I, M	C I	10-Bit Current Output DAC
DAC-86	10	0.500	10	Ext (M)	3	I	C I	COMDAC Companding DAC (U-255 Law)
DAC-88	10	0.500	10	Ext (M)	3	I	C I	COMDAC Companding DAC (U-255 Law)
DAC-89	10	0.500	10	Ext (M)	3	I	C I	COMDAC Companding DAC (A-Law)
PM-7533	10	0.60	10	Ext (M)	2, 3, 5, 6	C, I, M	C I	CMOS, Low Cost, 10-Bit Multiplying DAC
AD7533	10	0.60	10	Ext (M)	2, 3, 4, 5, 6	C, I, M	C I	CMOS, Low Cost, 10-Bit Multiplying DAC
AD9712A	**12**	**0.022**	**12**	**Int**	**2, 3, 5, 14**	**C, M**	**C I**	**ECL Compatible, Low Glitch, 0.5 LSB DNL Typ**
AD9713A	**12**	**0.027**	**12**	**Int**	**2, 3, 5, 14**	**C, M**	**C I**	**TTL Compatible, Low Glitch, 0.5 LSB DNL Typ**
AD9712	12	0.030	12	−1.2 V, Int	2, 5	C, M	C I	ECL Compatible Inputs, Low Glitch
AD9713	12	0.030	12	−1.2 V, Int	2, 5	C, M	C I	TTL Compatible Inputs, Low Glitch
AD568	**12**	**0.035**	**12**	**Int**	**3, 4**	**C, M**	**C I**	**Highest Accuracy 12-Bit Ultrahigh Speed DAC**
AD668	**12**	**0.05**	**12**	**Ext (M)**	**3**	**C, M**	**C I**	**Multiplying 12-Bit Ultrahigh Speed DAC**
AD565A	**12**	**0.25**	**12**	**10 V, Int**	**1**	**C, M**	**C I**	**Industry Workhorse High Speed, JAN Part Available**

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Boldface Type: Product recommended for new design.
*New product.

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Single DACs, Current Output

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Volt Int/Ext (M)[2]	Package Options[3]	Temp Range[4]	Page[5]	Comments
DAC-8043	**12**	**0.25**	**Serial, µP**	**Ext (M)**	**2, 3**	**C, I, M**	**C I**	**8-Pin Serial Input 12-Bit CMOS Multiplying DAC**
PM-7542	**12**	**0.25**	**4, µP**	**Ext (M)**	**2, 3, 4, 6**	**C, I, M**	**C I**	**CMOS, Nibble Load 12-Bit Multiplying DAC**
AD7542	**12**	**0.25**	**4, µP**	**Ext (M)**	**1, 2, 3, 4, 5**	**C, I, M**	**C I**	**CMOS, Nibble Load 12-Bit Multiplying DAC**
***PM-6012**	**12**	**0.25**	**12**	**Ext (M)**	**2, 3, 6**	**I**	**C I**	**Low Cost, High Speed 12-Bit Multiplying DAC**
DAC-312	**12**	**0.25**	**12**	**Ext (M)**	**2, 3, 6**	**C, M**	**C I**	**12-Bit High Speed Multiplying DAC**
AD DAC80-I	12	0.30	12	6.3 V, Int	1	C	C I	Industry Standard, High Speed DAC
AD DAC85-I	12	0.30	12	6.3 V, Int	1	I, M	C I	Improved Industry Standard, High Speed DAC
AD DAC87-I	12	0.30	12	6.3 V, Int	1	I, M	C I	Improved Industry Standard, High Speed DAC
AD566A	**12**	**0.35**	**12**	**10 V, Ext**	**1**	**C, M**	**C I**	**High Speed DAC**
AD7543	**12**	**0.35**	**Serial, µP**	**Ext (M)**	**1, 2, 3, 4, 5, 6**	**C, I, M**	**C I**	**CMOS, Serial Load 12-Bit Multiplying DAC**
DAC-8143	**12**	**0.38**	**Serial, µP**	**Ext (M)**	**2, 3, 6**	**I, M**	**C I**	**12-Bit Serial Input DAC**
PM-7543	**12**	**0.38**	**Serial, µP**	**Ext (M)**	**2, 3, 5, 6**	**C, I, M**	**C I**	**CMOS, Serial Load 12-Bit Multiplying DAC, Daisy Chain**
PM-7541A	**12**	**0.60**	**12**	**Ext (M)**	**2, 3, 4, 5, 6**	**C, I, M**	**C I**	**CMOS, 12-Bit Multiplying DAC**
AD7541A	**12**	**0.60**	**12**	**Ext (M)**	**2, 3, 4, 5**	**C, I, M**	**C I**	**CMOS, 12-Bit Multiplying DAC**
DAC-8012	**12**	**1.0**	**12, µP**	**Ext (M)**	**2, 3, 5**	**C, I, M**	**C I**	**12-Bit CMOS DAC with Memory and Readback**
PM-7548	**12**	**1.0**	**8, µP**	**Ext (M)**	**2, 3, 5, 6**	**C, I, M**	**C I**	**CMOS, Byte Load 12-Bit DAC, Single or Dual Supply**
AD7548	**12**	**1.0**	**8, µP**	**Ext (M)**	**2, 3, 4, 5, 6**	**C, I, M**	**C I**	**CMOS, Byte Load 12-Bit DAC, Single or Dual Supply**
AD562	12	1.5	12	Ext	1	C, I, M	C I	Industry Standard, JAN Part Available
AD563	12	1.5	12	2.5 V, Int	1	C, M	C I	Industry Standard
AD7545A	**12**	**1.0**	**12, µP**	**Ext (M)**	**2, 3, 4, 5**	**C, I, M**	**C I**	**CMOS, Improved AD7545**
PM-7545	**12**	**1.0**	**12, µP**	**Ext (M)**	**2, 3, 4, 5, 6**	**C, I, M**	**C I**	**CMOS, Parallel Load 12-Bit Multiplying DAC**
PM-7645	**12**	**1.0**	**12, µP**	**Ext (M)**	**2, 3, 4**	**C, I, M**	**C I**	**PM-7545 Specified for +15 V Operation**
AD7545	**12**	**2.0**	**12, µP**	**Ext (M)**	**2, 3, 4, 5**	**C, I, M**	**C I**	**CMOS, Parallel Load 12-Bit Multiplying DAC**
AD7534	**14**	**1.5**	**8, µP**	**Ext (M)**	**2, 3, 5**	**C, I, M**	**C I**	**CMOS, Byte Load**
AD7535	**14**	**1.5**	**8/14, µP**	**Ext (M)**	**2, 3, 4, 5**	**C, I, M**	**C I**	**CMOS, Parallel or Byte Load**
AD7536	**14**	**1.5**	**8/14, µP**	**Ext (M)**	**2, 3, 4, 5**	**C, I, M**	**C I**	**CMOS, Parallel or Byte Load, Bipolar Output**
AD7538	**14**	**1.5**	**14, µP**	**Ext (M)**	**2, 3, 6**	**C, I, M**	**C I**	**CMOS, Parallel Load**
***DAC-16**	**16**	**0.5**	**16**	**Ext (M)**	**1, 2**	**I, M**	**C I**	**16-Bit High Speed Multiplying DAC**
AD DAC71-I	16	1.0	16	6.3 V, Int	1, 7	C	C I	High Resolution 16-Bit DAC
AD DAC72-I	16	1.0	16	6.3 V, Int	1, 7	C, I	C I	High Resolution 16-Bit DAC

Single DACs, Voltage Output

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Volt Int/Ext (M)[2]	Package Options[3]	Temp Range[4]	Page[5]	Comments
AD557	**8**	**0.8**	**8, µP**	**Int**	**2, 5**	**C**	**C I**	**Lowest Cost 8-Bit DACPORT™; Single +5 V Supply**
AD7569	**8**	**1.0**	**8, µP**	**Int**	**2, 3, 4, 5, 6**	**C, I, M**	**C II**	**CMOS, Complete 8-Bit DAC/ADC/SHA/ Reference**
AD558	**8**	**3.0**	**8, µP**	**Int**	**1, 2, 4, 5**	**C, M**	**C I**	**10 V Out DACPORT, Single or Dual Supply**
***PM7224**	**8**	**5.0**	**8, µP**	**2–12.5 V, Ext**	**2, 3, 4, 5, 6**	**C, I, M**	**C I**	**CMOS, Low Cost 8-Bit DAC**
AD7224	**8**	**5.0 (max)**	**8, µP**	**2–12.5 V, Ext**	**2, 3, 4, 5, 6**	**C, I, M**	**C I**	**CMOS, Low Cost 8-Bit DAC**
DAC-06	10	1.5	10	6.7 V, Int	1	C, M	C I	Twos Complement Input Coding
DAC-210	10	1.5	10	7.6 V, Int	1	C, I	C I	Sign-Magnitude/Internal Reference
DAC-05	10	2.0	10	6.7 V, Int	1	C, M	C I	Sign-Magnitude for Unipolar Output
DAC-02	10	2.0	10	6.7 V, Int	1	C, M	C I	Sign-Magnitude/Bipolar Output
AD7848	**12**	**2.5**	**12, µP**	**Int (+3 V), Ext**	**2, 3, 5**	**C, I**	**C I**	**CMOS, Complete 12-Bit DAC with 8-Word FIFO**
AD7845	**12**	**2.5**	**12, µP**	**Ext (M)**	**2, 3, 4, 5, 6**	**C, I, M**	**C I**	**CMOS, 12-Bit Multiplying DAC with Output Amplifier**
AD DAC80-V	12	3.0	12	6.3 V, Int	1	C	C I	Improved Industry Standard
AD DAC85-V	12	3.0	12	6.3 V, Int	1	I, M	C I	Improved Industry Standard
AD DAC87-V	12	3.0	12	6.3 V, Int	1	I, M	C I	Improved Industry Standard
AD667	**12**	**3.0**	**4/8/12, µP**	**10 V, Int**	**1, 2, 4, 5**	**C, I, M**	**C I**	**Highest Accuracy Complete 12-Bit DAC**
AD767	**12**	**3.0**	**12, µP**	**10 V, Int**	**1, 2**	**C, I, M**	**C I**	**Fastest Interface Complete 12-Bit DAC**
AD7233	**12**	**10 (max)**	**Serial, µP**	**Int**	**2**	**I**	**C I**	**Smallest 12-Bit Serial DACPORT (8-Pin) Bipolar ±5 V Output Range**
***AD7243**	**12**	**10 (max)**	**Serial**	**Int (+5 V), Ext**	**2, 3, 6**	**I, M**	**C I**	**Low Cost 12-Bit Serial DACPORT in 16-Pin Package**
AD7245A	**12**	**10 (max)**	**12, µP**	**5 V, Int**	**2, 3, 4, 5, 6**	**C, I, M**	**C I**	**Faster Interface, 12 V and 15 V AD7245**
AD7248A	**12**	**10 (max)**	**8, µP**	**5 V, Int**	**2, 3, 5, 6**	**C, I, M**	**C I**	**Faster Interface, 12 V and 15 V AD7248**
AD7245	12	10 (max)	12, µP	5 V, Int	2, 3, 4, 5	C, I, M	C I	CMOS, 12-Bit Complete DAC, Parallel Load
AD7248	12	10 (max)	8, µP	5 V, Int	2, 3, 4, 5	C, I, M	C I	CMOS, 12-Bit Complete DAC, Byte Load
AD7840	**14**	**2.0**	**14/Serial, µP**	**Int (+3 V), Ext**	**2, 3, 5**	**C, I, M**	**C I**	**CMOS, 14-Bit Complete DAC, Parallel or Serial Load**
***AD766**	**16**	**1.5**	**Serial, µP**	**Int**	**1, 2**	**C, I, M**	**C I**	**Zero-Chip Interface 16-Bit DSP DACPORT**
AD569	**16**	**3.0**	**8/16, µP**	**±5 V, Ext (M)**	**1, 2**	**I, M**	**C I**	**Monolithic, 16-Bit Monotonic DAC**
AD DAC71-V	16	5.0	16	6.3 V, Int	1, 7	C	C I	High Resolution 16-Bit DAC
AD DAC72-V	16	5.0	16	6.3 V, Int	1, 7	C, I	C I	High Resolution 16-Bit DAC
AD7846	**16**	**6**	**16, µP**	**Ext (M)**	**1, 2, 4, 5**	**C, I, M**	**C I**	**CMOS, 16-Bit Multiplying DAC with Readback Capability**

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Boldface type: Product recommended for new design.

*New product.

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Selection Guide
Digital-to-Analog Converters

Single DACS, Voltage Output

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Volt Int/Ext (M)[2]	Package Options[3]	Temp Range[4]	Page[5]	Comments
*AD669	16	8	16, µP	10 V, Int	2, 3, 6	I, M	C I	Monolithic, Complete 16-Bit DAC
DAC1136	16	8	16	6 V, Int	Module	C	C I	High Resolution and Accuracy
AD1147	16	20	16, µP	10 V, Int	2	I	C I	Internal 8-Bit Latched Input DACs for Offset and Gain Adjust
AD1148	16	20	16, µP	10 V, Int	2	I	C I	Separate 8-Bit Bus for Internal Offset and Gain Adjust DACs
DAC1138	18	10	18	6 V, Int	Module	C	C I	High Resolution and Accuracy
AD1139	18	40	18, µP	–10 V, Int	1	C	C I	True 18-Bit Accuracy

Video Graphics DACs

Model	Res Bits	Rate Update Rate MHz min	Palette Size	Reference	Package Options[3]	Temp Range[4]	Page[5]	Comments
*ADV477/ADV475	6/8	80, 66, 50, 35	256	V (Int.)	2, 5	C	C I	Low Power, Power Down RAM-DAC
*ADV473	8	100, 80, 66, 50, 35	256	V/I (Int.)	5	C	C I	True-Color Video RAM-DAC (Triple 8-Bit)
*ADV101	8	80, 50, 30	—	V	2, 5	C	C I	CMOS, Triple 8-Bit Video DAC
AD9701	8	225	—	—	1, 3, 4	I, M	C I	Single 8-Bit Video DAC
*ADV7150	10	170, 135, 110, 85	256	V	10	C	C I	High Speed, True-Color Video RAM-DAC, (Triple 10-Bit) 4 × 1 Multiplexing
*ADV7151	10	170, 135, 110, 85	256	V	10	C	C I	High Speed, Pseudo-Color Video RAM-DAC, (Triple 10-Bit)
*ADV7152	10	170, 135, 110, 85	256	V	10	C	C I	High Speed, Pseudo-Color Video RAM-DAC, (Triple 10-Bit) 2 × 1 Multiplexing

Multiple DACs, Voltage Output

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Voltage Int/Ext[2]	# of DACs	Package Options[3]	Temp Range[4]	Page[5]	Comments
AD7669	**8**	**1.0**	**8, µP**	**Int**	**2**	**2, 5, 6**	**C, I, M**	**C II**	**CMOS, Complete 8-Bit Dual DAC/ADC/SHA/Reference**
DAC-8228	**8**	**2.0**	**8, µP**	**Ext (M)**	**2**	**2, 3, 6**	**I, M**	**C I**	**CMOS, PM-7528 Pinout with Voltage Output**
DAC-8229	**8**	**2.0**	**8, µP**	**Ext (M)**	**2**	**2, 3, 6**	**I, M**	**C I**	**CMOS, Single or Dual Supply Operation**
AD7769	**8**	**2.5**	**8, µP**	**Ext**	**2**	**2, 5**	**C, I**	**C II**	**CMOS, Complete 8-Bit Dual DAC/ 2-Channel ADC**
DAC-8426	**8**	**3.0**	**8, µP**	**10 V, Int**	**4**	**2, 3, 6**	**I, M**	**C I**	**CMOS, Complete with 10 V Reference, Improved Timing**
PM-7226A	**8**	**3.0**	**8, µP**	**Ext (M)**	**4**	**2, 3, 6**	**I, M**	**C I**	**CMOS, Improved Timing, Specified for +5 V to +15 V Operation**
AD7226	**8**	**3.0**	**8, µP**	**2–12.5 V, Ext**	**8**	**2, 3, 4, 5, 6**	**C, I, M**	**C I**	**CMOS, No User Trims, Specified with Single or Dual Supplies**
AD7225	**8**	**5.0 (max)**	**8, µP**	**2–12.5 V, Ext**	**4**	**2, 3, 4, 5, 6**	**C, I, M**	**C I**	**CMOS, Separate References for Each DAC**
AD7228	8	5.0 (max)	8, µP	2–10 V, Ext	8	2, 3, 4, 5, 6	C, I, M	C I	CMOS, Specified for Single or Dual Supply, Skinny 20-Pin DIP
***AD7228A**	**8**	**5.0 (max)**	**8, µP**	**2–10 V, Ext**	**8**	**2, 3, 5, 6**	**C, I, M**	**C I**	**CMOS, Specified for Single or Dual Supply, Skinny 20-Pin DIP**
AD75004	**12**	**2**	**12, µP**	**5 V, Int**	**4**	**2, 5**	**C**	**C I**	**Fastest Quad 12-Bit Voltage Output DAC**
***AD7242**	**12**	**2**	**Serial, µP**	**3 V, Int**	**2**	**2, 3, 6**	**C, I**	**C I**	**Complete ±5 V 12-Bit Dual DAC**
AD392	12	4	12, µP	Int	4	8	C	C I	Fast Bus Access Time (<40 ns), Data Readback Capability
AD390	**12**	**4**	**12, µP**	**10 V, Int**	**4**	**1**	**C, M**	**C I**	**Double Buffered, Simultaneous Update**
***AD7837**	**12**	**5**	**8, µP**	**Ext (M)**	**2**	**2, 3, 6**	**C, I, M**	**C I**	**CMOS, MDAC, Byte Load, Double Buffered**
***AD7847**	**12**	**5**	**12, µP**	**Ext (M)**	**2**	**2, 3, 6**	**C, I, M**	**C I**	**CMOS MDAC, Parallel Load**
DAC-8412	**12**	**6**	**12, µP**	**Ext**	**4**	**1, 2, 4, 5**	**I, M**	**C I**	**Readback, Reset to Midscale, Low Power Quad DAC, +5 V to ±15 V Operation**
***DAC-8413**	**12**	**6**	**12, µP**	**Ext**	**4**	**1, 2, 4, 5**	**I, M**	**C I**	**Equivalent to DAC-8412 with Reset to Zero Scale**

[1]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 12-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.

[2]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.

[3]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-In-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/ Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.

[4]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.

[5]C I = Data Converter Reference Manual, Volume I; C II = Data Converter Reference Manual, Volume II; D = Data sheet available, consult factory; L = Linear Products Databook; P = Precision Monolithics Division Databook.

Boldface type: Product recommended for new design.

*New product.

Selection Guide
Digital-to-Analog Converters

Multiple DACs, Voltage Output

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Voltage Int/Ext[2]	# of DACs	Package Options[3]	Temp Range[4]	Page[5]	Comments
***AD7850**	**12**	**8**	**12, µP**	**5 V, Int**	**8**	**5**	**C, I**	**C I**	**Monolithic Octal 12-Bit Voltage Output DAC**
AD7237	**12**	**10 (max)**	**8, µP**	**Int (+5 V), Ext**	**2**	**2, 3, 6**	**C, I, M**	**C I**	**CMOS, Complete 12-Bit Dual DAC, Byte Load**
AD7247	**12**	**10 (max)**	**12, µP**	**Int (+5 V), Ext**	**2**	**2, 3, 6**	**C, I, M**	**C I**	**CMOS, Complete 12-Bit Dual DAC, Parallel Load**
AD664	**12**	**10**	**12, µP**	**Ext (M)**	**4**	**1, 2, 4, 5**	**C, I, M**	**C I**	**Readback, Reset, Low Power Quad DAC**
AD394	**12**	**10**	**12, µP**	**Ext (M)**	**4**	**1**	**C, M**	**C I**	**Four Independent Reference Inputs, Bipolar Outputs**
AD395	**12**	**10**	**12, µP**	**Ext (M)**	**4**	**1**	**C, M**	**C I**	**Four Independent Reference Inputs, Unipolar Outputs**
***AD7244**	**14**	**2**	**Serial, µP**	**+3 V, Int**	**2**	**2, 3, 6**	**C, I, M**	**C I**	**Complete ±5 V 14-Bit Dual DAC**
AD396	14	10	8, µP	Ext (M)	4	1	C, M	C I	Four Independent Reference Inputs, **Bipolar Output, Simultaneous Update**

Multiple DACs, Current Output

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Voltage Int/Ext[2]	# of DACs	Package Options[3]	Temp Range[4]	Page[5]	Comments
PM7528	**8**	**0.18**	**8, µP**	**Ext (M)**	**2**	**2, 3, 4, 5, 6**	**C, I, M**	**C I**	**CMOS, Single Supply Operation, TTL Compatible at V_{DD} = +5 V**
AD7528	**8**	**0.18**	**8, µP**	**Ext (M)**	**2**	**2, 3, 4, 5, 6**	**C, I, M**	**C I**	**CMOS, +5 V to +15 V Operation, TTL Compatible at V_{DD} = +5 V**
PM-7628	**8**	**0.20**	**8, µP**	**Ext (M)**	**2**	**2, 3, 4, 5, 6**	**I, M**	**C I**	**CMOS, +5 V or +15 V Operation, Improved Timing**
AD7628	**8**	**0.35**	**8, µP**	**Ext (M)**	**2**	**2, 3, 4, 5, 6**	**C, I, M**	**C I**	**CMOS, +12 V to +15 V Operation, TTL Compatible at V_{DD} = 12 V to 15 V**
DAC-8221	**12**	**0.45**	**12, µP**	**Ext (M)**	**2**	**2, 3, 4, 6**	**C, I, M**	**C I**	**CMOS, Buffered Inputs, +5 V Operation**
***AD7564**	**12**	**0.2**	**Serial, µP**	**Ext (M)**	**4**	**6**	**I**	**C I**	**Single +5 V Supply, Separate References, 28-Pin SOIC Package**
***AD7568**	**12**	**0.2**	**Serial, µP**	**Ext (M)**	**8**	**10**	**I**	**C I**	**Single +5 V Supply, Separate References, 44-Pin PQFP**
DAC-8212	12	1.0	12	Ext (M)	2	2, 3, 5	C, I, M	C I	CMOS, +5 V or +15 V Single Supply Operation
DAC-8222	**12**	**1.0**	**12, µP**	**Ext (M)**	**2**	**2, 3, 4, 6**	**C, I, M**	**C I**	**CMOS, Double Buffered Inputs, Parallel Load**
DAC-8248	**12**	**1.0**	**8, µP**	**Ext (M)**	**2**	**2, 3, 6**	**C, I, M**	**C I**	**CMOS, Double Buffered Inputs, Byte Load**
AD7537	**12**	**1.5 (max)**	**8, µP**	**Ext (M)**	**2**	**2, 3, 4, 5**	**C, I, M**	**C I**	**CMOS, Byte Load, Double Buffered**
AD7547	**12**	**1.5 (max)**	**12, µP**	**Ext (M)**	**2**	**2, 3, 4, 5, 6**	**C, I, M**	**C I**	**CMOS, Parallel Load**
AD7549	**12**	**1.5 (max)**	**4, µP**	**Ext (M)**	**2**	**2, 3, 4, 5**	**C, I, M**	**C I**	**CMOS, Nibble Load, Double Buffered**

[1]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 12-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.

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Boldface type: Product recommended for new design.

*New product.

Selection Guide
Operational Amplifiers

Low Noise Amplifiers

Model	Voltage Noise e_n typ 1 kHz $nV/\sqrt{Hz}$	Voltage Noise e_n typ 10 kHz $nV/\sqrt{Hz}$	Current Noise $I_n \pm I_{n-}$ typ 1 kHz $pA/\sqrt{Hz}$	I_B typ nA	V_{OS} mV typ	GBW MHz typ	SR V/µs typ	Settling Time ns to % typ	A_{CL} min V/V	Package Options[1]	Temp Range[2]	Page[3]	Comments
AD9610	1.6	0.7	32/32	5000	0.3	100	3500	1–0.1	1	2	I, M	L	Wide Bandwidth, Fast Settling
AD9617	2.0	1.3	32/32	12000	0.5	570	1400	10–0.1	±1	2, 3, 6, 12	C, I, M	L	Low Distortion, Wide Bandwidth
AD9618	2.0	1.3	32/32	10000	0.5	8000	1800	9–0.1	+5, −1	2, 3, 6, 12	C, I, M	L	Low Distortion, Wide Bandwidth
OP-227	3	3.5	0.4	10	0.02	8	2.8	—	1	3	C, I, M	P	Dual Matched Precision
*AD745	3.2	2.9	0.007	0.150	0.1	20	12.5	5000–0.01	5	2, 3, 6	C, I, M	D	Ultralow Noise, High Speed, BiFET Op Amp
AD743	3.2	2.9	0.007	0.15	0.1	4.5	2.8	—	1	2, 3, 6	C, I, M	L	Ultralow Noise FET Input
OP-270	3.2	3.6	0.6	5	0.01	5	2.4	—	1	2, 3, 4, 6	I, M	P	Dual Monolithic
OP-470	3.2	3.8	0.4	6	0.1	6	2	—	1	2, 3, 4, 6	I, M	P	Quad Monolithic, Low Noise
OP-50	4.5	5.5	0.23	1	0.01	25	3	—	5	3	I, M	P	High Output Current
AD645	9	8	0.6/0.6	0.0007	0.1	2	2	—	1	2, 7	C, I, M	L	FET Input, Low I_B

High Speed Amplifiers

Model	SR V/μs typ	GBW MHz typ	Settling Time ns to % typ	A_{CL} min V/V	V_{OS} mV typ	I_{OUT} mA min	Supply Current mA typ	Package Options[1]	Temp Range[2]	Page[3]	Comments
AD9610	3500	100	18–0.1	1	0.3	50	21	7	I, M	L	Wide Bandwidth, Fast Settling
AD9618	1800	8000	10–0.1	−1	0.2	60	31	2, 3, 6, 12	C, I, M	L	Low Distortion, Wideband, IMD ≤ −70 dBc at 20 MHz
AD9617	1600	570	10–0.1	1	0.4	60	34	2, 3, 6, 12	C, I, M	L	Low Distortion, Wide Bandwidth, IMD≤ −70 dBc at 20 MHz
OP-44	120	23	200–0.1	3	0.3–1.5	20	6.5	3, 7	I, M	P	High Speed, Precision
AD744	75	13	500–0.01	+2, −1	0.3	25	3.5	2, 3, 6, 7	C, I, M	L	FET Input, Fast Settling, High Speed, Custom Compensation
AD746	75	13	500–0.01	+2, −1	0.3	25	3.5	2, 3, 6, 7	C, I, M	L	Dual AD744
OP-17	60	30	600–0.1	1	0.2–0.5	5.5	4.6	2, 3, 6, 7	C, I, M	P	Precision, Low Power
OP-42	58	10	800–0.01	1	0.3–1.5	20	5.1	2, 3, 4, 6, 7	I, M	P	Precision, Fast Settling
PM-157A	45	20	4000–0.01	1	1	5	5	3, 7	C, M	P	Improved Industry Standard
OP-16	25	8	900–0.1	1	0.2–0.5	5.5	4.6	2, 3, 6, 7	C, I, M	P	Precision, Low Power
OP-01	18	2.5	700–0.1	1	0.3–2	6	1.6	2, 3, 7	C, M	P	Inverting, High Speed
OP-15	13	6	1200–0.1	1	0.2–0.5	5.5	2.7	2, 3, 6, 7	C, I, M	P	Precision, Low Power
***AD745**	12.5	2.0	5000–0.01	5	0.1–0.25	20	8	2, 3, 6	C, I, M	D	Ultralow Noise, High Speed, BiFET Op Amp
PM-156A	12	4.5	4000–0.01	1	1	5	5	3, 4, 7	C, M	P	Improved Industry Standard
***OP-282**	9.0	4	1500–0.01	1	1	10	0.5	2, 3, 6	I	D	Dual High Speed, Low Power
***OP-482**	9.0	4	1500–0.01	1	2	10	1.0	2, 3, 6	I	D	Quad High Speed, Low Power

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[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.

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Boldface Type: Product recommended for new design.

*New product.

Selection Guide
Operational Amplifiers

Precision Amplifiers

Model	V_{OS} μV max	V_{OS} TC μV/°C max	Noise μV p-p 0.1–10 Hz typ	GBW MHz typ	Slew Rate V/μs typ	I_B nA max	CMRR dB f = 1 kHz typ	Package Options[1]	Temp Range[2]	Page[3]	Comments
OP-177	10–60	0.1–1.2	0.35	0.6	0.3	1.5–2.8	110	2, 3, 6	I, M	P	Highest Precision
AD707	15–90	0.1–1.0	0.23	0.9	0.3	1.0–2.5	100	2, 3, 6, 7	C, I, M	L	High Precision
OP-77	25–100	0.3–1.2	0.35	0.6	0.3	2–2.8	105	2, 3, 4, 6, 7	C, I, M	P	Next Generation OP-07
OP-50	25–100	0.3–1	0.12	25	3	5–10	85	3	I, M	P	Low Noise, High Output Current $A_{VCL} \geq 5$
AD708	30–100	0.3–1.0	0.23	0.9	0.3	1.0–2.5	100	2, 3, 6, 7	C, I, M	L	Dual AD707
AD705	25–90	0.6–1.2	0.5	0.8	0.15	0.1–0.15	110	2, 3, 6	C, I, M	L	Low I_B Precision Bipolar
OP-97	25–75	0.6–2	0.5	0.9	0.2	0.1–0.15	100	2, 3, 4, 6, 7	I, M	P	Low Power OP-07
AD OP-27	25–100	0.6–1.8	0.08	8	2.8	40–80	123	2, 3, 7	C, I, M	L	Ultralow Noise
AD OP-37	25–100	0.6–1.8	0.08	63 (GBP)	17	40–80	123	2, 3, 7	C, I, M	L	Combines Precision and Speed
AD OP-07	25–150	0.6–2.5	0.35	0.6	0.17	2–12	95	2, 3, 6, 7	C, M	L	Improved Industry Standard
OP-07	25–150	0.6–2.5	0.35	0.6	0.3	2–12	98	2, 3, 4, 6, 7	C, I, M	P	Low Offset Voltage
PM-1012	35–50	1.5	0.5	0.5	0.2	0.1–0.15	100	2, 3, 6, 7	C, I, M	P	Low Power, Low I_B
AD706	50–100	0.6–1.5	0.5	0.8	0.15	0.15–0.25	110	2, 3, 6	C, I, M	L	Dual AD705
AD704	50–100	1.0–1.5	0.5	0.8	0.15	0.15–0.25	110	2, 3, 6	C, I, M	L	Quad AD705
AD517	50–100	1.3–3	2	0.25	0.1	0.25–2	94	7	C, M	L	
OP-297	50–200	0.6–2	0.3	0.5	0.15	0.1–0.2	105	2, 3, 6	I, M	P	Dual Precision, Low Power, Low I_B
*OP-497	50–150	0.5–1.5	0.3	0.5	0.15	0.1–0.2	130	2, 3, 4, 6	I, M	D	Quad Precision, Low I_B
OP-200	75–200	0.5–2	0.5	0.5	0.15	2–5	110	2, 3, 4, 6	I, M	P	Dual Monolithic, Precision
OP-270	75–250	1–3	0.08	5	2.4	20–60	115	2, 3, 4, 6	I, M	P	Dual Monolithic, Low Power
OP-227	80–180	1–1.8	0.08	8	2.8	40–80	125	3	I, M	P	Dual Matched, Low Noise
OP-207	100–200	1.3–1.8	0.35	0.6	0.2	3–7	98	3	C, M	P	Dual Matched, Precision
OP-21	100–500	1–5	—	0.6	0.25	100–150	60	2, 3, 6, 7	I, M	P	Low Power, Single Supply
PM-1008	120	1.5	0.5	0.5	0.2	0.1	100	2, 3, 7	C, M	P	Low I_B, Low Power
OP-400	150–300	1.2–2.5	0.5	0.5	0.15	3–7	110	2, 3, 4, 6	C, I, M	P	Quad, Monolithic, Precision
OP-90	150–450	2–5	3	—	—	15–25	80	2, 3, 4, 6	I, M	P	Micropower, Low Voltage, Single Supply
OP-221	150–500	1.5–3	—	0.6	0.3	80–120	60	2, 3, 6, 7	C, I, M	P	Dual Low Power, Single Supply
OP-220	150–750	1.5–3	—	0.2	0.05	20–30	30	2, 3, 6, 7	C, I, M	P	Dual Micropower, Single Supply
OP-290	200–500	3–5	3	0.02	—	15–25	100	2, 3, 4, 6	I, M	P	Dual Micropower, Low Voltage Single Supply

Model	V_{OS} μV max	V_{OS} TC μV/°C max	Noise μV p–p 0.1–10 Hz typ	GBW MHz typ	Slew Rate V/μs typ	I_B nA max	CMRR dB f = 1 kHz typ	Package Options[1]	Temp Range[2]	Page[3]	Comments
AD547	250–1000	1–5	2	1	3	0.025–0.05	60	7	C, M	L	Low Drift BiFET
AD647	250–1000	2.5–10	4	1	3	0.035	76	4, 7	C, M	L	Dual AD547
OP-20	**250–1000**	**1.5–7**	**—**	**0.1**	**0.05**	**25–40**	**30**	**2, 3, 6, 7**	**C, I, M**	**P**	**Micropower, Single Supply**
OP-43	**250–1500**	**5–10**	**—**	**2.4**	**6**	**0.005–0.02**	**100**	**2, 7**	**C, I, M**	**P**	**Low I_B, Fast**
AD548	**250–2000**	**2–20**	**2**	**1**	**1.8**	**0.03–0.015**	**83**	**2, 3, 6, 7**	**C, I, M**	**L**	**Low Power BiFET**
AD648	**100–2000**	**3–20**	**2**	**1**	**1.8**	**0.03–0.015**	**83**	**2, 3, 6, 7**	**C, I, M**	**L**	**Dual AD548**
OP-41	**250–2000**	**5–10**	**—**	**0.5**	**1.3**	**0.005–0.02**	**100**	**2, 6, 7**	**C, I, M**	**P**	**Low I_B**
OP-22	**300–1000**	**1.5–3**	**—**	**0.25**	**0.08**	**5–10**	**60**	**2, 3, 6, 7**	**C, I, M**	**P**	**Micropower, Programmable**
OP-32	**300–1000**	**1.5–3**	**—**	**4.5**	**1.5**	**5–10**	**90**	**2, 3**	**C, I, M**	**P**	**Micropower, Fast, Programmable**
OP-470	**400–1000**	**2–4**	**0.08**	**6**	**2**	**25–60**	**110**	**2, 3, 4, 6**	**C, I, M**	**P**	**Quad, Low Noise**

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-In-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.

[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.

[3]C I = Data Converter Reference Manual, Volume I; C II = Data Converter Reference Manual, Volume II; D = Data sheet available, consult factory; L = Linear Products Databook; P = Precision Monolithics Division Databook.

Boldface Type: Product recommended for new design.

*New product.

Selection Guide
Operational Amplifiers

Low Cost, General Purpose Amplifiers

Model	V_{OS} mV max	V_{OS} TC µV/°C max	I_B nA max	BW MHz typ[1]	SR V/µs typ	Settling Time µs 0.01% typ	Noise µV p-p 0.1–10 Hz typ	Package Options[2]	Temp Range[3]	Page[4]	Comments
OP-177	**0.01–0.06**	**0.1–1.2**	**1.5–2.8**	**0.6**	**0.3**	**—**	**0.35**	**2, 3, 6**	**I, M**	**P**	**Highest Precision Performance**
AD707	**0.015–0.09**	**0.1–1**	**1–2.5**	**0.9**	**0.15**	**—**	**0.23**	**2, 3, 6, 7**	**C, I, M**	**L**	**Very High DC Precision**
AD705	**0.025–0.09**	**0.6–2.0**	**0.1–0.15**	**0.8**	**0.15**	**—**	**0.5**	**2, 3, 6**	**C, I, M**	**L**	**Low I_B Precision Bipolar**
AD704	**0.05–0.10**	**0.6–1.5**	**0.15–0.25**	**0.8**	**0.15**	**8**	**0.5**	**2, 3, 6**	**C, I, M**	**L**	**Quad AD705**
AD706	**0.05–0.10**	**1.0–1.5**	**0.15–0.25**	**0.8**	**0.15**	**8**	**0.5**	**2, 3, 6**	**C, I, M**	**L**	**Dual AD705**
***OP-497**	**0.05–0.15**	**0.5–1.5**	**0.1–0.2**	**0.5**	**0.15**	**—**	**0.3**	**2, 3, 4, 6**	**I, M**	**D**	**Quad OP-97**
OP-77	**0.025–0.1**	**0.3–1.2**	**2–2.8**	**0.6**	**0.3**	**—**	**0.35**	**2, 3, 4, 6, 7**	**C, I, M**	**P**	**Next Generation OP-07**
AD OP-07	**0.025–0.15**	**0.6–2.5**	**3–12**	**0.6**	**0.17**	**—**	**0.35–0.38**	**2, 3, 6, 7**	**C, M**	**L**	**Improved Industry Standard**
OP-07	**0.025–0.15**	**0.6–2.5**	**2–12**	**0.6**	**0.3**	**—**	**0.35**	**2, 3, 4, 6, 7**	**C, I, M**	**P**	**Industry Standard Precision**
OP-97	**0.025–0.2**	**0.6–2**	**0.1–0.15**	**0.9**	**0.2**	**—**	**0.5**	**2, 3, 4, 6, 7**	**I, M**	**P**	**Low Power, Low I_B OP-07**
PM-1012	**0.035–0.05**	**1.5**	**0.1–0.15**	**0.5**	**0.2**	**—**	**0.5**	**2, 3, 6, 7**	**I, M**	**P**	**Low Power, Low I_B**
PM-1008	**0.12**	**1.5**	**0.1**	**0.5**	**0.2**	**—**	**0.5**	**2, 3, 7**	**C, M**	**P**	**Low Power Precision**
OP-05	**0.15–1.3**	**0.9–2**	**2–3**	**0.6**	**0.3**	**—**	**0.35**	**2, 3, 7**	**C, M**	**P**	**Instrumentation Operational Amplifier**
AD548	**0.25–2**	**2–20**	**0.01–0.02**	**1**	**1.8**	**8**	**2**	**2, 3, 6, 7**	**C, I, M**	**L**	**Low Power, High Performance**
AD542	0.5–2	5–20	0.025–0.05	1	3	—	2	7	C, M	L	High Performance BiFET
AD544	0.5–2	5–20	0.025–0.05	2	13	—	2	7	C, M	L	High Performance BiFET
OP-02	**0.5–5**	**8–10**	**30–100**	**1.3**	**0.5**	**—**	**0.65**	**2, 3, 7**	**C, M**	**P**	**Improved "741"**
OP-11	**0.5–5**	**10–15**	**300–500**	**3**	**1**	**—**	**0.7**	**2, 3, 4, 6**	**C, I, M**	**P**	**Improved Quad "741"**
OP-09	**0.5–5**	**10–15**	**300–500**	**3**	**1**	**—**	**0.7**	**3**	**C, M**	**P**	**Improved "4136," Quad**
OP-01	**0.7–5**	**8–20**	**30–100**	**2.5**	**18**	**—**	**—**	**2, 3, 7**	**C, M**	**P**	**Inverting, High Speed**
OP-04	**0.75–5**	**8–20**	**50–100**	**1.3**	**0.5**	**—**	**0.65**	**3, 7**	**I, M**	**P**	**Improved "747"**
OP-14	**0.75–5**	**8–20**	**50–100**	**1.3**	**0.5**	**—**	**0.65**	**2, 3, 6, 7**	**I, M**	**P**	**Improved "1458," Dual**
***OP-282**	**1.5**	**10**	**0.1**	**4**	**9**	**—**	**1.3**	**2, 3, 6**	**I**	**D**	**Dual, High Speed, Low Power**
***OP-482**	**2.5**	**10**	**0.1**	**4**	**9**	**—**	**1.3**	**2, 3, 6**	**I**	**D**	**Quad, High Speed, Low Power**
AD741	3–6	20	200–500	1	0.5	—	—	2, 7	C, I, M	L	Improved Second Source

Low Power/Micropower Amplifiers

Model	ISY max mA	V_{OS} max mV	I_B max nA	GBW typ MHz	SR typ V/μs	Package Options[2]	Temp Range[3]	Page[4]	Comments
OP-22	**0.0002–0.4**	**0.3–1**	**5–10**	**0.25**	**0.08**	**2, 3, 6, 7**	**I, M**	**P**	**Programmable, Single Supply**
OP-32	**0.0005–2**	**0.3–1**	**5–10**	**4.5**	**1.5**	**2, 3**	**I, M**	**P**	**Fast, Programmable $A_{VCL} \geq 10$, Single Supply**
OP-90	**0.02**	**0.15–0.45**	**15–25**	**0.02**	**—**	**2, 3, 4, 6**	**I, M**	**P**	**Micropower, Low Voltage Single Supply**
OP-290	**0.04**	**0.2–0.5**	**15–25**	**0.02**	**—**	**2, 3, 4, 6**	**I, M**	**P**	**Dual, Micropower, Low Voltage, Single Supply**
OP-20	**0.08**	**0.25–1**	**25–40**	**0.1**	**0.05**	**2, 3, 4, 6**	**I, M**	**P**	**Micropower, Single Supply, Low Cost**
OP-490	**0.08**	**0.5–1**	**15–25**	**0.02**	**—**	**2, 3, 4, 6**	**I, M**	**P**	**Quad, Micropower, Low Voltage, Single Supply**
OP-220	**0.17**	**0.15–0.75**	**20–30**	**0.2**	**0.05**	**2, 3, 6, 7**	**I, M**	**P**	**Dual, Low Cost, Micropower, Single Supply**
AD548	**0.2**	**0.25–0.2**	**0.01–0.02**	**1.0**	**1.8**	**2, 3, 7**	**C, I, M**	**L**	**Precision Low Power BiFET Op Amp**
OP-80	**0.325**	**1.5**	**0.00025–0.001**	**0.3**	**0.4**	**2, 6, 7**	**I, M**	**P**	**Low I_B, CMOS**
OP-420	**0.36**	**2.5–6**	**20–40**	**0.15**	**0.05**	**2, 3, 4, 6**	**I, M**	**P**	**Quad, Low Cost, Micropower, Single Supply**
OP-21	**0.3–0.4**	**0.1–0.5**	**100–150**	**0.6**	**0.25**	**2, 3, 6, 7**	**I, M**	**P**	**Low Cost, Low Power, Single Supply**
***OP-282**	**0.5**	**2.0**	**0.1**	**4**	**9**	**2, 3, 6**	**I**	**D**	**Dual, High Speed**
AD648	**0.4**	**0.4–2.0**	**0.005–.01**	**1.0**	**1.8**	**2, 3, 7**	**C, I, M**	**L**	**Dual, Precision Low Power BiFET Op Amp**
PM-1008	**0.6**	**0.12**	**0.1**	**3.5**	**0.2**	**2, 3, 6, 7**	**C, M**	**P**	**Low Power**
OP-97	**0.6**	**0.025–0.075**	**0.1–0.15**	**0.9**	**0.2**	**2, 3, 4, 6, 7**	**I, M**	**P**	**Precision, Low I_B**
AD705	**0.6**	**0.025–0.09**	**0.1–0.15**	**0.8**	**0.15**	**2, 3, 6**	**C, I, M**	**L**	**Picoampere Input Current Bipolar Op Amp**
PM-1012	**0.6**	**0.035–0.05**	**0.1–0.15**	**0.5**	**0.2**	**2, 3, 6, 7**	**C, I, M**	**P**	**Precision, Low I_B**
OP-221	**0.8**	**0.15–0.5**	**80–120**	**0.6**	**0.3**	**2, 3, 6, 7**	**I, M**	**P**	**Dual, Low Cost, Low Power, Single Supply**
OP-41	**1**	**0.25–2**	**0.005–0.02**	**0.5**	**1.3**	**2, 6, 7**	**I, M**	**P**	**Low Power, Low I_B**
***OP-482**	**1.0**	**3.0**	**0.1**	**4**	**9**	**2, 3, 6**	**I**	**D**	**Quad, High Speed**
OP-43	**1–1.2**	**0.25–1.5**	**0.005–0.025**	**2.4**	**6**	**2, 7**	**I, M**	**P**	**Fast, Low Power, Low I_B**
AD706	**1.2**	**0.05–0.1**	**0.11–0.2**	**0.8**	**0.15**	**2, 3, 6**	**C, I, M**	**L**	**Dual, Picoampere Input Current Bipolar Op Amp**
***OP-297**	**1.25**	**0.05–0.2**	**0.1–0.2**	**0.5**	**0.15**	**2, 3, 4, 6**	**I, M**	**D**	**Dual, Precision, Low I_B**
OP-200	**1.45**	**0.075–0.2**	**2–5**	**0.5**	**0.15**	**2, 3, 4, 6**	**I, M**	**P**	**Dual, Precision**
OP-421	**1.8**	**2.5–6**	**50–150**	**1.9**	**0.5**	**2, 3, 6**	**I, M**	**P**	**Quad, Low Cost, Low Power, Single Supply**
AD704	**2.4**	**0.075–0.150**	**0.15—0.17**	**1.0**	**0.15**	**2, 3, 6**	**C, I, M**	**D**	**Quad, Picoampere Input Current Bipolar Op Amp**
***OP-497**	**2.5**	**0.05–0.15**	**0.1–0.2**	**0.5**	**0.15**	**2, 3, 4, 6**	**I, M**	**D**	**Quad, Highest Precision, Low Power**
OP-400	**2.9**	**0.15–0.3**	**3–7**	**0.5**	**0.15**	**2, 3, 4, 6**	**C, I, M**	**P**	**Quad, Precision**

[1]Unity gain small signal bandwidth.
[2]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-In-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.
[3]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
[4]C I = Data Converter Reference Manual, Volume I; C II = Data Converter Reference Manual, Volume II; D = Data sheet available, consult factory; L = Linear Products Databook; P = Precision Monolithics Division Databook.
Boldface Type: Product recommended for new design.
*New product.

Selection Guide
Operational Amplifiers

Low Input Current Amplifiers

Model	I_B pA max	Input Impedance Differential Ω‖pF typ	Input Impedance Common Mode Ω‖pF typ	CMRR dB f=1 kHz typ	V_{OS} mV max	V_{OS} TC µV/°C max	BW MHz typ[1]	Package Options[2]	Temp Range[3]	Page[4]	Comments
AD549	**0.06–0.25**	**10^{13}‖1**	**10^{15}‖0.8**	**62**	**0.25–1**	**5–20**	**1**	**7**	**C, M**	**L**	**Monolithic, Lowest I_B**
AD515A	0.075–0.3	10^{13}‖1.6	10^{15}‖0.8	62	1–3	15–50	1	7	C	L	Lower Cost AD515 Replacement
OP-80	**0.25–1**	**—**		**90**	**1.5**	**—**	**0.3**	**2, 6, 7**	**I, M**	**P**	**Low Cost CMOS**
AD546	**0.5–1**	**10^{13}‖1**	**10^{15}‖0.8**	**62**	**1–2**	**20**	**1**	**2**	**C**	**L**	**Precision Low Cost Electrometer**
AD645	**1.5–3**	**10^{13}‖1**	**10^{14}‖3**	**94**	**0.25–0.5**	**1–5**	**2**	**2, 7**	**C, I, M**	**L**	**Low Noise, Precision BiFET**
AD545A	1–2	10^{13}‖1.6	10^{15}‖0.8	62	0.25–1	3–25	1	7	C	L	Lower Cost AD545 Replacement
OP-41	**5–20**	**—**		**98**	**0.25–2**	**5–10**	**0.5**	**2, 6, 7**	**C, I, M**	**P**	**High Stability JFET**
AD548	**10–20**	**10^{12}‖3**	**3×10^{12}‖3**	**84**	**0.25–2**	**2–20**	**1**	**2, 3, 6, 7**	**C, I, M**	**L**	**Low Power, Low Cost**
OP-43	**5–25**	**—**		**98**	**0.25–1.5**	**5–10**	**2.4**	**2, 7**	**I, M**	**P**	**Low I_B, Fast $A_{VCL} \geq 3$**
AD547	25–50	10^{12}‖6	10^{12}‖13	60	0.25–1	1–5	1	7	C, M	L	Low Drift
PM-155A	**50**	**—**		**90**	**2**	**5**	**2.5**	**3, 7**	**C, M**	**P**	**Improved Industry Standard**
PM-156A	**50**	**—**		**90**	**2**	**5**	**4.5**	**3, 7**	**C, M**	**P**	**Improved Industry Standard**
PM-157A	**50**	**—**		**90**	**2**	**5**	**20**	**3, 7**	**C, M**	**P**	**Improved Industry Standard**
OP-15	**50–200**	**—**		**90**	**0.5–3**	**5–15**	**6**	**2, 3, 6, 7**	**C, I, M**	**P**	**Precision BiFET**
OP-16	**50–200**	**—**		**90**	**0.5–3**	**5–15**	**8**	**2, 3, 6, 7**	**C, I, M**	**P**	**Precision BiFET**
OP-17	**50–200**	**—**		**90**	**0.5–3**	**5–15**	**30**	**2, 3, 6, 7**	**C, I, M**	**P**	**Fast, Precision BiFET**

Quad Operational Amplifiers

Model	V_{OS} mV max	V_{OS} TC µV/°C max	I_B pA max	BW MHz typ[1]	Slew Rate V/µs typ	Settling Time 0.01% to 0.01% µs typ	Package Options[2]	Temp Range[3]	Page[4]	Comments
AD704	**0.05–0.10**	**0.6–1.5**	**150–250**	**0.8**	**0.15**	**—**	**2, 3, 6**	**C, I, M**	**L**	**Quad AD705, Low I_B Precision Bipolar**
***OP-497**	**0.05–0.15**	**0.5–1.5**	**150–200**	**0.5**	**0.15**	**—**	**2, 3, 4, 6**	**I, M**	**D**	**Low Power, Low I_B Precision Bipolar**
OP-400	**0.15–0.3**	**1.2–2.5**	**3–7**	**0.5**	**0.15**	**—**	**2, 3, 4, 6**	**C, I, M**	**P**	**Quad Monolithic, Precision**
OP-470	**0.4–1**	**2–4**	**25–60**	**6**	**2**	**—**	**2, 3, 4, 6**	**C, I, M**	**P**	**Quad Monolithic, Low Noise**
OP-490	**0.5–1**	**5**	**15–25**	**0.02**	**—**	**—**	**2, 3, 4, 6**	**I, M**	**P**	**Micropower, Low Voltage, Single Supply**
OP-11	**0.5–5**	**10–15**	**300–500**	**3**	**1**	**—**	**2, 3, 4, 6**	**C, I, M**	**P**	**Improved Quad "741"**
***OP-482**	**3.0**	**10**	**0.1**	**4.0**	**9**	**1.5**	**3, 4, 6**	**I**	**D**	**High Speed, Low Power**
PM-148/248	**2.5**	**—**	**75**	**0.8**	**0.4**	**—**	**3**	**I, M**	**P**	**Improved Industry Standard**
OP-421	**2.5–6**	**10–15**	**50–150**	**1.9**	**0.5**	**—**	**2, 3, 6**	**I, M**	**P**	**Low Power, Low Cost, Single Supply**
OP-420	**2.5–6**	**10–25**	**20–40**	**0.15**	**0.05**	**—**	**2, 3, 4, 6**	**I, M**	**P**	**Micropower, Low Cost, Single Supply**

Dual Operational Amplifiers

Model	V_{OS} mV max	V_{OS} TC µV/°C max	I_B nA max	BW MHz typ[1]	Slew Rate V/µs typ	Settling Time to 0.01% µs typ	Package Options[2]	Temp Range[3]	Page[4]	Comments
AD708	**0.03–0.1**	**0.3–1.0**	**1–2.5**	**0.9**	**0.3**		**2, 3, 7**	**C, I, M**	**L**	**Highest DC Precision; Excellent Matching Between Amps, Dual AD707**
AD706	**0.05–0.10**	**0.6–1.5**	**0.15–0.25**	**0.8**	**0.15**	**—**	**2, 3, 6**	**C, I, M**	**L**	**Dual AD705, Low I_B Precision Bipolar**
***OP-297**	**0.05–0.2**	**0.6–2**	**0.1–0.2**	**0.5**	**0.15**	**—**	**2, 3, 6**	**I, M**	**D**	**Precision, Low Power, Low I_B**
OP-200	**0.075–0.2**	**0.5–2**	**2–5**	**0.5**	**0.15**	**—**	**2, 3, 4, 6**	**I, M**	**P**	**Dual Monolithic, Precision**
OP-270	**0.075–0.25**	**1–3**	**20–60**	**5**	**2.4**	**—**	**2, 3, 4, 6**	**I, M**	**P**	**Dual Monolithic, Low Noise**
OP-227	**0.08–0.18**	**1–1.8**	**40–80**	**8**	**2.8**	**—**	**3**	**I, M**	**P**	**Dual Matched, Low Noise**
OP-207	**0.1–0.2**	**1.3–1.8**	**3–7**	**0.6**	**0.2**	**—**	**3**	**C, M**	**P**	**Dual Matched, Precision**
OP-221	**0.15–0.5**	**1.5–3**	**80–120**	**0.6**	**0.3**	**—**	**2, 3, 6, 7**	**C, I, M**	**P**	**Low Power, Single Supply**
OP-220	**0.15–0.75**	**1.5–3**	**20–30**	**0.2**	**0.05**	**—**	**2, 3, 6, 7**	**C, I, M**	**P**	**Micropower, Single Supply**
OP-290	**0.2–0.5**	**3–5**	**15–25**	**0.02**	**—**	**—**	**2, 3, 4, 6**	**I, M**	**P**	**Micropower, Low Voltage Single Supply**
AD647	0.25–1	2.5–10	0.035–0.075	1	3	—	4, 7	C, M	L	Dual AD547
AD746	**0.25–1**	**3–20**	**0.15**	**13**	**75**	**0.5**	**2, 3, 7**	**C, I, M**	**L**	**Precision, Fast Settling, Dual AD744**
AD648	**0.3–2**	**3–20**	**0.01–0.02**	**1**	**1.8**	**8**	**2, 3, 7**	**C, I, M**	**L**	**Low Power, BiFET, Dual AD548**
OP-10	**0.5**	**2–4.5**	**3–7**	**0.6**	**0.17**	**—**	**3**	**C, M**	**P**	**Dual Matched, Precision**
AD642	0.5–2	—	0.035–0.075	1	3	—	7	C, M	L	Dual AD542
AD644	0.5–2	—	0.035–0.075	2	13	—	7	C, M	L	Dual AD544
OP-14	**0.75–5**	**8–20**	**50–100**	**1.3**	**0.5**	**—**	**2, 3, 6, 7**	**I, M**	**P**	**General Purpose, Low Cost**
OP-215	**1–4**	**10**	**0.1–0.3**	**5.7**	**18**	**0.9–0.1**	**2, 3, 4, 6, 7**	**C, I, M**	**P**	**High Speed, Precision**
***OP-282**	**2.0**	**10**	**0.1**	**4.0**	**9**	**1.5**	**3, 4, 6**	**I**	**D**	**High Speed, Low Power**

[1]Unity gain small signal bandwidth.
[2]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-In-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.
[3]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
[4]C I = Data Converter Reference Manual, Volume I; C II = Data Converter Reference Manual, Volume II; D = Data sheet available, consult factory; L = Linear Products Databook; P = Precision Monolithics Division Databook.
Boldface Type: Product recommended for new design.
*New product.

Selection Guide
Operational Amplifiers

Unity Gain Buffers

Model	−3 dB BW MHz typ	SR V/μs min	Settling Time to 0.02% ns typ	Rise Time 1V Step ns typ	I_{OUT} mA min	V_{OS} mV typ	I_{SS} mA max	Package Options[1]	Temp Range[2]	Page[3]	Comments
AD9630	**750**	**1800**	**8**	**0.9**	**50**	**3**	**26**	**2, 3, 6, 12**	**I, M**	**L**	**High Performance, Wideband Buffer**
AD9620	**600**	**2200**	**8**	**0.8**	**40**	**2**	**48**	**1**	**I, M**	**L**	**High Performance, Low Harmonic Distortion Buffer**

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-In-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.
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Boldface Type: Product recommended for new design.
*New product.

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Minimization of Noise in Operational Amplifier Applications

INTRODUCTION

Since operational amplifier specifications such as Input Offset Voltage and Input Bias Current have improved tremendously in the past few years, noise is becoming an increasingly important error consideration. To take advantage of today's high performance op amps, an understanding of the noise mechanisms affecting op amps is required. This paper examines noise contributions, both internal and external to an op amp, and provides practical methods for minimizing their effects.

BASIC NOISE PROPERTIES

Noise, for purposes of this discussion, is defined as any signal appearing in an op amp's output that could not have been predicted by DC and AC input error analysis. Noise can be random or repetitive, internally or externally generated, current or voltage type, narrowband or wideband, high frequency or low frequency; whatever its nature, it can be minimized.

The first step in minimizing noise is source identification in terms of bandwidth and location in the frequency spectrum; some of the more common sources are shown in Figure 1, an 11-decade frequency spectrum chart. Some preliminary observations can be made: noise is present from DC to VHF from sources which may be identified in terms of bandwidth and frequency. Noise source bandwidths overlap, making noise a composite quantity at any given frequency. Most externally caused noise is repetitive rather than random and can be found at a definite frequency. Noise effects from external sources must be reduced to insignificant levels to realize the full performance available from a low noise op amp.

EXTERNAL NOISE SOURCES

Since noise is a composite signal, the individual sources must be identified to minimize their effects. For example, 60Hz power line pickup is a common interference noise appearing at an op amp's output as a 16ms sine wave. In this and most other situations, the basic tool for external noise source frequency characterization is the oscilloscope sweep rate setting. Recognizing the oscilloscope's potential in this area, Tektronix® manufactures an oscilloscope vertical amplifier with variable upper and lower −3dB points, which allows quick noise source frequency identification. Another basic identification tool is the simple low pass filter as shown in Figure 2, where the bandpass is calculated by:

$$(1)\quad f_O \cong \frac{1}{2\pi RC}$$

With such a filter, measurement bandpass can be changed from 10Hz to 100kHz (C = 4.7μF to 470pF), attenuating higher frequency components while passing frequencies of interest. Once identified, noise from an external source may be minimized by the methods outlined in Table 1—the external noise source chart.

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FIGURE 1: Frequency Spectrum of Noise Sources Affecting Operational Amplifier Performance

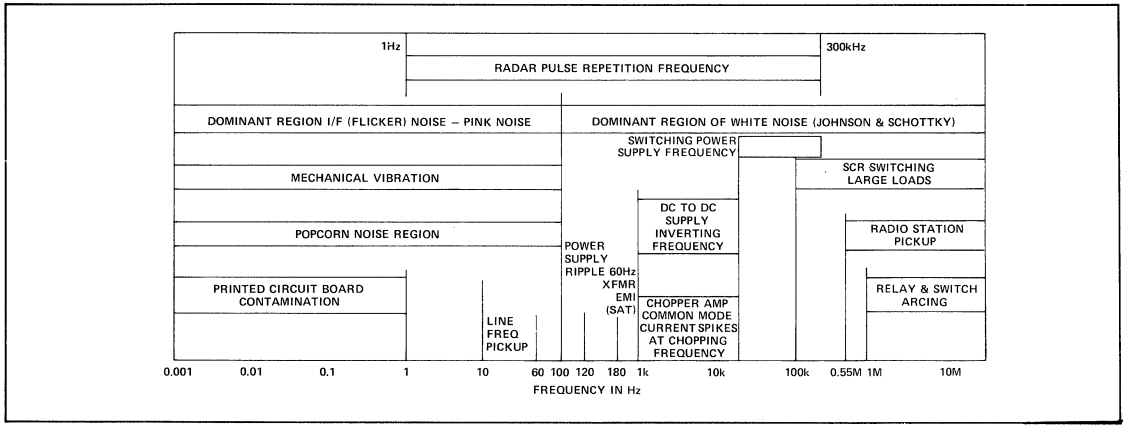

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TABLE 1: External Noise Source Chart

Source	Nature	Causes	Minimization Methods
60Hz	Repetitive Interference	Powerlines physically close to op amp inputs. Poor CMRR at 60Hz. Power transformer primary-to-secondary capacitive coupling.	Reorientation of power wiring. Shielded transformers. Single point grounding. Battery power.
120Hz Ripple	Repetitive	Full wave rectifier ripple on op amp's supply terminals. Inadequate ripple consideration. Poor PSRR at 120Hz.	Thorough design to minimize ripple. RC decoupling at the op amp. Battery power.
180Hz	Repetitive EMI	180Hz radiated from saturated 60Hz transformers.	Physical reorientation of components. Shielding. Battery power.
Radio Stations	Standard AM Broadcast Through FM	Antenna action anyplace in system.	Shielding. Output filtering. Limited circuit bandwidth.
Relay and Switch Arcing	High Frequency Burst At Switching Rate	Proximity to amplifier inputs, power lines, compensation terminals, or nulling terminals.	Filtering of HF components. Shielding. Avoidance of ground loops. Arc suppressors at switching source.
Printed Circuit Board Contamination	Random Low Frequency	Dirty boards or sockets.	Thorough cleaning at time of soldering followed by a bakeout and humidity sealant.
Radar Transmitters	High Frequency Gated At Radar Pulse Repetition Rate	Radar transmitters from long range surface search to short range navigational—especially near airports.	Shielding. Output filtering of frequencies ≫ PRR.
Mechanical Vibration	Random < 100Hz	Loose connections, intermittent contact in mobile equipment.	Attention to connectors and cable conditions. Shock mounting in severe environments.
Chopper Frequency Noise	Common Mode Input Current At Chopping Frequency	Abnormally high noise chopper amplifier in system.	Balanced source resistors. Use bipolar input op amps instead. Use premium low noise chopper.
Switching Power Supply	Repetitive High Frequency Glitches In Supply And Ground	Improper ground return. Radiated noise from switching circuit.	Analog ground return to AC return. Shield power supply. Liberal power supply bypass at the op amp.

FIGURE 2: Noise Frequency Analysis RC Low Pass Filter

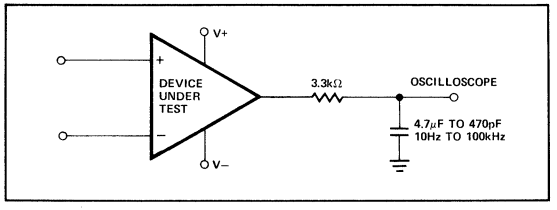
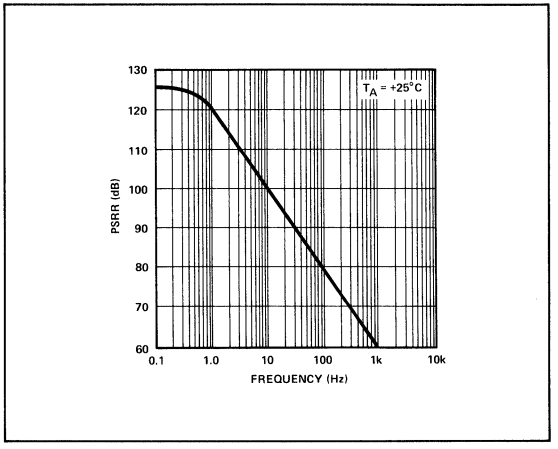


FIGURE 3: PSRR vs Frequency (OP-77)



Power Supply Ripple

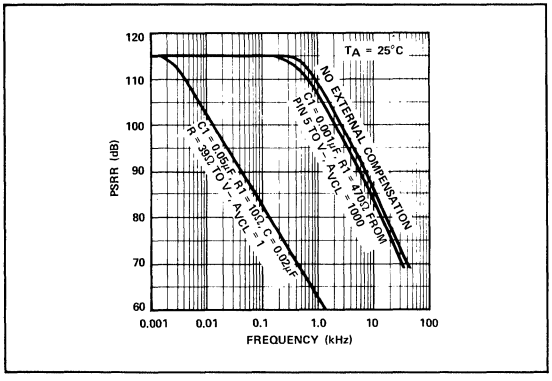
Power supply ripple at 120Hz is not usually thought of as a noise, but it should be. In an actual op amp application, it is quite possible to have a 120Hz noise component that is equal in magnitude to all other noise sources combined, and, for this reason, it deserves a special discussion.

To be negligible, 120Hz ripple noise should be between 10nV and 100nV referred to the input of an op amp. Achieving these low levels requires consideration of three factors: the op amp's 120Hz power supply rejection ratio (PSRR), the regulator's ripple rejection ratio, and finally, the regulator's input capacitor size.

PSRR at 120Hz for a given op amp may be found in the manufacturer's data sheet curves of PSRR versus frequency as shown in Figure 3. For the amplifier shown, 120Hz PSRR is about 76dB, and to attain a goal of 100nV referred to the input, ripple at the power terminals must be less than 0.6mV. Today's IC regulators provide about 60dB of ripple rejection; in this case the regulator input capacitor must be made large enough to limit input ripple to 0.6V.

Externally-compensated low noise op amps can provide improved 120Hz PSRR in high closed-loop gain configurations. The PSRR versus frequency curves of such an op amp are shown in Figure 4. When compensated for a closed-loop gain of 1000, 120Hz PSRR is 115dB. PSRR is still excellent at much higher frequencies allowing low ripple-noise operation in exceptionally severe environments.

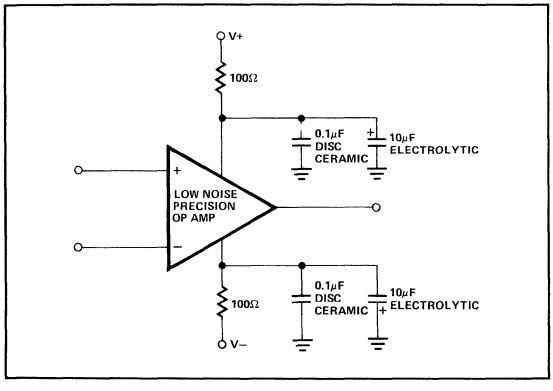
FIGURE 4: PSRR vs Frequency (OP-06)



Power Supply Bypassing

Usually, 120Hz ripple is not the only power supply associated noise. Series regulator output typically contain at least 150µV of noise in the 100Hz to 100kHz range; switching types contain even more. Unpredictable amounts of induced noise can also be present on power leads from many sources. Since high frequency PSRR decreases at 20dB/decade, these higher frequency supply noise components must not be allowed to reach the op amp's power terminals. RC decoupling, as shown in Figure 5, will adequately filter most wideband noise. Some caution must be exercised with this type of decoupling, as load current changes will modulate the voltage at the op amp's supply pins.

FIGURE 5: RC Decoupling



Power Supply Regulation

Any change in power supply voltage will have a resultant effect referred to an op amp's inputs. For the op amp of Figure 3, PSRR at DC is 126dB (0.5µV/V) which may be considered as a potential low frequency noise source. Power supplies for low noise op amp applications should, therefore, be both low in ripple and well-regulated. Inadequate supply regulation is often mistaken to be low frequency op amp noise.

When noise from external sources has been effectively minimized, further improvements in low noise performance are obtained by specifying the right op amp and through careful selection and application of the associated components.

OPERATIONAL AMPLIFIER INTERNAL NOISE

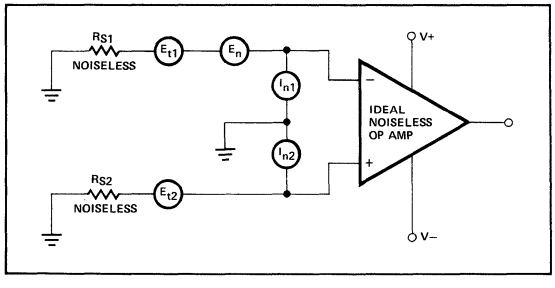
Most completely specified low-noise op amp data sheets specify current and voltage noises in a 1Hz bandwidth centered on 10Hz, 100Hz, and 1kHz, as well as low frequency noise over a range of 0.1Hz to 10Hz. To minimize total noise, a knowledge of the derivation of these specifications is useful. In this section, the reader is provided with an explanation of basic op amp-associated random noise mechanisms and introduced to a simplified method for calculating total input-referred noise in typical applications.

Op amp-associated noise currents and voltages are random in nature. They are aperiodic and uncorrelated to each other; and typically have Gaussian amplitude distributions, with the highest noise amplitudes having the lowest probability. There is a statistical relationship between the peak-to-peak value of random noise and its rms value. Where the amplitude distribution is Gaussian, the rms value may be multiplied by six to yield a peak-to-peak value that will not be exceeded 99.73% of the time (this is a handy rule-of-thumb for noise calculations).

Noise Model of Op Amps

In the calculation of op amp circuit noise, it is customary to refer all noise to the input. Figure 6 completely models the input-referred noise sources. In the model, the internal white and flicker noise sources are combined into three equivalent input noise generators, E_n, I_{n1}, and I_{n2}. The noise current generators produce noise voltage drops across their respective source resistors, R_{S1} and R_{S2}. The source resistors themselves generate thermal noise voltages, E_{t1} and E_{t2}. Total rms input-referred voltage noise, over a given bandwidth, is the square root of the sum of the squares of the five noise voltage generators over that bandwidth.

FIGURE 6: Op Amp Noise Model



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(2) $E_n(f_H, f_L) = \sqrt{E_n^2 + (I_{n1} \cdot R_{S1})^2 + (I_{n2} \cdot R_{S2})^2 + E_{t1}^2 + E_{t2}^2}$

Equation 2 describes, in total, all noise sources of an op amp circuit. It will be used throughout this application note.

Minimization of total noise requires an understanding of the mechanisms involved in each of the five generators. First, the white noise mechanisms, thermal and shot, are discussed, followed by other low frequency noise mechanisms, flicker and popcorn.

Noise Mechanisms of Op Amps

The two basic types of op amp-associated noises are white noise and flicker noise (1/f). White noise contains equal amounts of power in each hertz of bandwidth. Flicker noise is different in that it contains equal amounts of power in each decade of bandwidth. This is best illustrated by spectral noise density plots such as in Figures 7 and 8. Above a certain corner frequency, white noise dominates; below that frequency, flicker (1/f) noise is dominant. Low noise corner frequencies in conjunction with a low white noise magnitude distinguish low noise op amps from general purpose devices.

FIGURE 7: OP-77 Noise Voltage

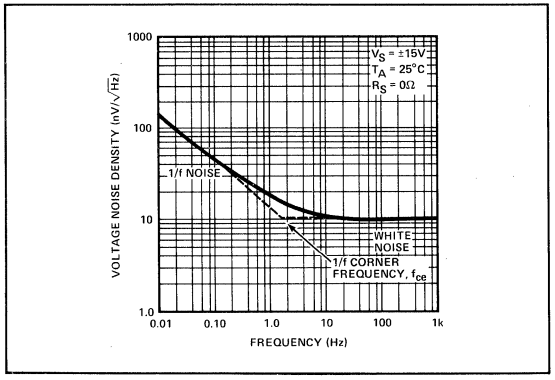
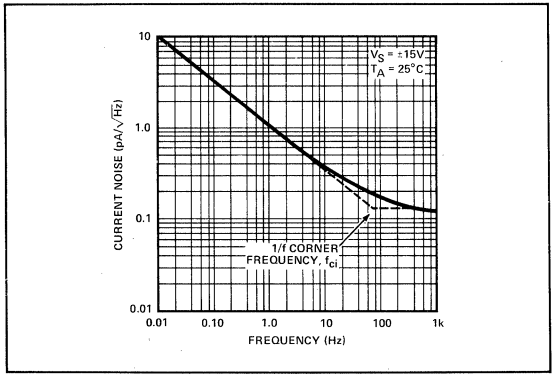


FIGURE 8: OP-77 Noise Current



Mathematically, noise spectral density may be expressed as:

(3a) $e_n^2 = \frac{E_n^2}{\Delta f}$ (3b) $i_n^2 = \frac{I_n^2}{\Delta f}$

Where: e_n, i_n = Spectral noise density of voltage and current, respectively

E_n, I_n = Total rms voltage and current noise in a frequency band, respectively

Δf = Bandwidth of 1Hz

From Equation 3, the total rms noise in a frequency band from f_L to f_H is then,

(4a) $E_n^2 = \int_{f_L}^{f_H} e_n^2 \, df$ (4b) $I_n^2 = \int_{f_L}^{f_H} i_n^2 \, df$

Where: f_H = Upper frequency limit of interest

f_L = Lower frequency limit of interest

Equation 4 means that three things must be known to evaluate total voltage noise (E_n) or current noise (I_n): f_H, f_L, and a knowledge of noise behavior over frequency.

White Noise

White noise contains many frequency components and is so named in analogy to white light which is made up of many colors. The important point to remember is that white noise has equal noise power in each hertz of bandwidth. In other words, the noise spectral density of white noise is **constant** with varying frequency. Thus, Equation 4 may be rewritten to describe white noise over a frequency band.

(5a) $E_{nW} = e_{nW}\sqrt{f_H - f_L}$ (5b) $I_{nW} = i_{nW}\sqrt{f_H - f_L}$

When $f_H \geq 10\,f_L$, the white noise expressions may be reduced to:

(6a) $E_{nW} = e_{nW}\sqrt{f_H}$ (6b) $I_{nW} = i_{nW}\sqrt{f_H}$

Flicker Noise

Unlike white noise, flicker (1/f) noise is not constant with respect to frequency, but has a power spectral density that is inversely proportional (K_e, K_i) to the frequency of interest as described in Equation 7.

(7a) $e_{nF}^2(f) = \frac{K_e^2}{f}$ (7b) $i_{nF}^2(f) = \frac{K_i^2}{f}$

or,

(8a) $e_{nF}(f) = \frac{K_e}{\sqrt{f}}$ (8b) $i_{nF}(f) = \frac{K_i}{\sqrt{f}}$

Where: K_e, K_i are constants of proportionality.

The constants of proportionality depend on a number of parameters internal to the amplifier. It will be shown later that the constants will drop out mathematically.

In order to calculate total voltage and current noise, the concept of corner frequency is useful. Referring to the graphs of e_n or i_n versus frequency as in Figures 7 and 8, we can see that it is a composite of a zero-slope line (white noise) summed with a line

of slope −1/2 (1/f noise, or flicker noise). The projected intersection of these lines occurs where the two noise powers are equal, at a frequency called the *corner frequency*. Therefore, it follows that at the corner frequency, f_{ce} or f_{ci},

(9a) $e_{nW}^2 = e_{nF}^2(f_{ce}) = \frac{K_e^2}{f_{ce}}$ (9b) $i_{nW}^2 = i_{nF}^2(f_{ci}) = \frac{K_i^2}{f_{ci}}$

rearranging,

(10a) $K_e^2 = e_{nW}^2 \cdot f_{ce}$ (10b) $K_i^2 = i_{nW}^2 \cdot f_{ci}$

substituting in Equation 7,

(11a) $e_{nF}^2(f) = e_{nW}^2 \cdot \frac{f_{ce}}{f}$ (11b) $i_{nF}^2(f) = i_{nW}^2 \cdot \frac{f_{ci}}{f}$

or,

(12a) $e_{nF}(f) = e_{nW}\sqrt{\frac{f_{ce}}{f}}$ (12b) $i_{nF}(f) = i_{nW}\sqrt{\frac{f_{ci}}{f}}$

We can find the rms flicker noise in a band as follows:

(13a) $E_{nF}^2 = \int_{f_L}^{f_H} e_{nF}^2(f)\, df$

$= e_{nW}^2 \cdot f_{ce} \cdot \ln\left(\frac{f_H}{f_L}\right)$

(13b) $I_{nF}^2 = \int_{f_L}^{f_H} i_{nF}^2(f)\, df$

$= i_{nW}^2 \cdot f_{ci} \cdot \ln\left(\frac{f_H}{f_L}\right)$

Typical bipolar op amp corner frequencies for voltage noise are in the range of 1 to 20Hz; and for current noise, 10 to 1,000Hz. In comparison, FET input op amps have voltage noise corner frequencies in the range of 100Hz to 500Hz. Still higher are CMOS op amps whose corner frequencies are typically on the order of 1kHz.

Now that we have the mathematical expressions describing white noise and flicker noise, we can sum (by root-sum-square method) the two components to yield a total spectral density expression.

(14a) $e_n^2 = e_{nW}^2 + e_{nF}^2(f)$ (14b) $i_n^2 = i_{nW}^2 + i_{nF}^2(f)$

substituting from Equation 11,

(15a) $e_n = e_{nW}\sqrt{1 + \frac{f_{ce}}{f}}$ (15b) $i_n = i_{nW}\sqrt{1 + \frac{f_{ci}}{f}}$

Equation 15 is an expression frequently used to describe noise (voltage and current) curves seen in op amp data sheets.

The rms noise in a band is then:

(16) $E_n(f_H, f_L) = e_{nW}\sqrt{f_{ce} \cdot \ln\left(\frac{f_H}{f_L}\right) + (f_H - f_L)}$

(17) $I_n(f_H, f_L) = i_{nW}\sqrt{f_{ci} \cdot \ln\left(\frac{f_H}{f_L}\right) + (f_H - f_L)}$

Where: e_{nW} = White noise voltage spectral density
i_{nW} = White noise current spectral density
f_{ce} = Voltage noise corner frequency
f_{ci} = Current noise corner frequency
f_H = Upper frequency limit of interest
f_L = Lower frequency limit of interest

The two most important internally-generated noise minimization rules are derived from Equation 16 and 17: a) limit the circuit bandwidth, and b) use operational amplifiers with low white noise specifications in conjunction with low corner frequencies. So far we have derived the noise voltage (E_n) and noise current (I_n) components (Equations 16 and 17) for the first three terms of Equation 2, which is reproduced below.

(2) $E_n(f_H, f_L) = \sqrt{E_n^2 + (I_{n1} \cdot R_{S1})^2 + (I_{n2} \cdot R_{S2})^2 + E_{t1}^2 + E_{t2}^2}$

In the next section, the last two terms of the equation, which are the thermal noise voltages generated by the external source resistances, are derived.

Thermal Noise

Thermal (Johnson) noise is a white noise voltage generated by random movement of thermally-charged carriers in a resistance; in op amp circuits, this is the type of noise produced by the source resistances in series with each input. Its rms value over a given bandwidth is calculated by:

(18) $E_t = \sqrt{4kTR \cdot (f_H - f_L)}$

Where: k = Boltzmann's constant = 1.38×10^{-23} joules/K
T = Absolute temperature, kelvin
R = Resistance in ohms
f_H = Upper frequency limit in hertz
f_L = Lower frequency limit in hertz

At room temperature, Equation 18 simplifies to:

(19) $E_t = 1.28 \times 10^{-10}\sqrt{R \cdot (f_H - f_L)}$

To minimize thermal noise (E_{t1} and E_{t2}) from R_{S1} and R_{S2}, large source resistors and excessive system bandwidth should be avoided.

Thermal noise is also generated inside the op amp, principally from r_{bb}', the base-spreading resistances in the input stage transistors. These noises are included in E_n, the total equivalent input voltage noise generator.

All the component noise sources of Equation 2 have now been derived. Total noise of an op amp circuit may be easily calculated using the equation. In the next sections, examples using several precision op amps will be calculated to illustrate the noise minimization techniques as well as to contrast the different noise performance of these devices.

TOTAL NOISE CALCULATION

With data sheet curves and specifications, and a knowledge of source resistance values, total input-referred noise may be calculated for a given application. To illustrate the method, noise information from the Precision Monolithics OP-77A and OP-27A data sheets are reproduced in Figure 9. The first step is to determine the current and voltage noise corner frequencies so that the E_n and I_n terms of Equation 2 may be calculated using Equations 16 and 17.

Corner Frequency Determination

In the input spot noise versus frequency curves of Figure 9, it may be seen that voltage noise ($R_S = 0$) begins to rise at about 3Hz. Lines projected from the horizontal (white noise) portion and the sloped (flicker noise) portion intersect at 2Hz, the voltage noise corner frequency (f_{ce}). In the center curve, excluding thermal noise from the source resistance, current noise multiplied by 200kΩ is plotted as a voltage noise. Lines projected from the horizontal portion and sloped portions intersect at 80Hz, the current noise corner frequency (f_{ci}).

FIGURE 9A: OP-77 Input Spot Noise Voltage vs Frequency

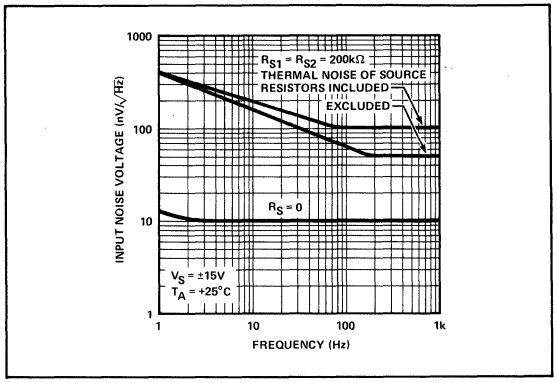


FIGURE 9B: OP-77/OP-27 Ultra-Low Offset Voltage Op Amps

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and $T_A = 25°C$, unless otherwise noted.

			OP-77A			OP-27A			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.35	0.6	—	0.08	0.18	μV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz	—	10.3	18.0	—	3.5	5.5	$nV/\sqrt{Hz}$
		f_O = 100Hz	—	10.0	13.0	—	3.1	4.5	
		f_O = 1000Hz	—	9.6	11.0	—	3.0	3.8	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	14	30	—	—	—	pA_{p-p}
Input Noise Current Density	i_n	f_O = 10Hz	—	0.32	0.80	—	1.7*	4.0	$pA/\sqrt{Hz}$
		f_O = 100Hz	—	0.14	0.23	—	1.0	2.3	
		f_O = 1000Hz	—	0.12	0.17	—	0.4	0.6	
Input Offset Voltage	V_{OS}		—	10	25	—	10	25	μV
Input Offset Voltage Drift	TCV_{OS}	$-55°C \le T_A \le +125°C$	—	0.1	0.3	—	0.2	0.6	$\mu V/°C$
Long Term Input Offset Voltage Stability	V_{OS}/Time		—	0.2	1.0	—	0.2	1.0	$\mu V/Mo$
Input Offset Current	I_{OS}		—	0.3	1.5	—	7	35	nA
Input Bias Current	I_B		—	±1.2	±2.0	—	±10	±40	nA

INPUT NOISE VOLTAGE (e_{np-p})
The peak-to-peak noise voltage in a specified frequency band.

INPUT NOISE VOLTAGE DENSITY(e_n)
The rms noise voltage in a 1Hz band surrounding a specified value of frequency.

INPUT NOISE CURRENT (i_{np-p})
The peak-to-peak noise current in a specified frequency band.

INPUT NOISE CURRENT DENSITY (i_n)
The rms noise current in a 1Hz band surrounding a specified value of frequency.

Equations 16 and 17 also require e_{nW} and i_{nW} for calculation of E_n and I_n. To find e_{nW} and i_{nW}, use the data sheet specifications a decade or more above the respective corner frequencies; in the case of the OP-77A, e_{nW} is $9.6V/\sqrt{Hz}$ (1,000Hz), and i_{nW} is $0.12pA/\sqrt{Hz}$ (1,000Hz). At this time, it should be noted that the noise current, $0.12pA/\sqrt{Hz}$, is a value that has been incorrectly derived from the standardized, commonly-used test method on virtually ALL commercially available op amps. The value is off by a factor of $\sqrt{2}$. Therefore, in order to calculate the correct total noise, the data sheet current noise value should be multiplied by a correction factor of $\sqrt{2}$. Thus, for the noise calculation of the OP-77A, the value e_{nW} is $9.6nV/\sqrt{Hz}$ (1,000Hz), and i_{nW} should be $0.17pA/\sqrt{Hz}$ (1,000Hz).

OP-77 Bandwidth of Interest

To be summed correctly, each of the five noise quantities must be expressed over the same bandwidth, f_H to f_L. For calculation purposes, assume f_H to be the highest frequency component that must be amplified without distortion. Note that e_n, i_n, corner frequencies are independent of actual circuit component values. When doing noise calculations for a large number of circuits using the same op amp, these numbers only have to be calculated once.

OP-77 Typical Application Example

Figure 10A shows a typical ×10 gain stage with a 10kΩ source resistance. In Figure 10B, the circuit is redrawn to show five noise voltage sources. To evaluate total input-referred noise, the values of each of the five sources must be determined.

FIGURE 10A: Noise Analysis Circuit

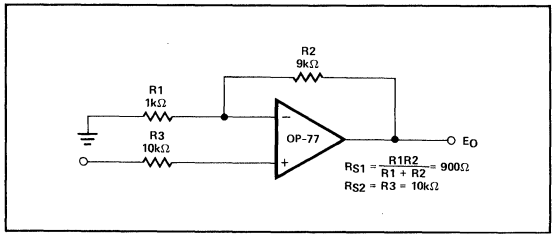
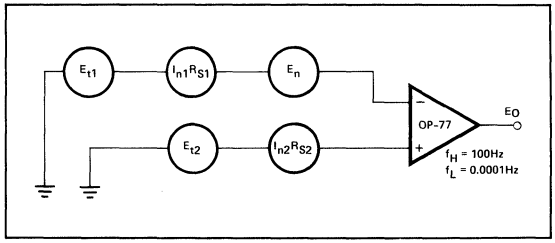


FIGURE 10B: Noise Analysis Equivalent Circuit



Using Equation 19: $E_t = 1.28 \times 10^{-10} \sqrt{R \cdot (f_H - f_L)}$

$E_{t1} = 1.28 \times 10^{-10} \sqrt{(900\Omega)\ (100Hz)} = 0.04\mu Vrms$

$E_{t2} = 1.28 \times 10^{-10} \sqrt{(10k\Omega)\ (100Hz)} = 0.128\mu Vrms$

Next, calculate I_n using Equation 17:

$$I_n = i_n \sqrt{f_{ci} \cdot \ln\left(\frac{f_H}{f_L}\right) + f_H - f_L}$$

$$= 0.17pA \sqrt{80 \cdot \ln\left(\frac{100Hz}{0.0001Hz}\right) + 100 - 0.0001}$$

$$= 5.9pArms$$

and:

$I_{n1} \cdot R_{S1} = 5.9pA \cdot (900\Omega) = 0.0053\mu Vrms$

$I_{n2} \cdot R_{S2} = 5.9pA \cdot (10k\Omega) = 0.059\mu Vrms$

Finally, E_n from Equation 16:

$$E_n = e_n \sqrt{f_{ce} \cdot \ln\left(\frac{f_H}{f_L}\right) + f_H - f_L}$$

$$= 9.6nV \sqrt{2 \cdot \ln\left(\frac{100Hz}{0.0001Hz}\right) + 100 - 0.0001}$$

$$= 0.108\mu Vrms$$

Substituting in Equation 2:

$$E_n(f_H - f_L) = \sqrt{E_n^2 + I_{n1}^2 R_{S1}^2 + I_{n2}^2 R_{S2}^2 + E_{t1}^2 + E_{t2}^2}$$

$$= \sqrt{(0.108\mu V)^2 + (0.0053\mu V)^2 + (0.059\mu V)^2 + (0.04\mu V)^2 + (0.128\mu V)^2}$$

$$= 0.18\mu Vrms$$

Total input-referred noise = 1.08μV peak-to-peak (0.0001Hz to 100Hz).

Notice that of the five terms in the equation, the first and the last terms dominate. Since the first term is the total rms noise voltage inherent of the amplifier, nothing can be done by the system designer to lower its noise other than to choose a device having inherently low noise characteristics. As can be seen in Equation 16, two key parameters determine the total rms noise of an amplifier—low white noise density and low noise corner frequency.

Notice that the thermal noise voltage (last term) of Equation 2 is determined by the 10kΩ value selected for R3. Had the value been reduced to 1kΩ, the thermal noise voltage would have been 0.04μVrms instead of 0.128μVrms. As a result, total rms noise voltage would have become 0.122μV, a remarkable 32% reduction in total noise.

Indeed, low noise design requires the system designer not only to choose an amplifier with low noise characteristics, but also to pay close attention in selecting appropriately low source resistances in the input circuit.

741 Calculation Example

The preceding calculation determined total noise in a given bandwidth using a low noise op amp. To place this level of performance into perspective, a calculation using the industry-standard 741 op amp in the circuit of Figure 10 is useful. Once again the starting point is corner frequency determination, using the data sheet curves of Figure 11: $f_{ce} = 200Hz$; $f_{ci} = 2kHz$; $e_n = 20nV/\sqrt{Hz}$; $i_n = (\sqrt{2}) \cdot (0.5pA/\sqrt{Hz}) = 0.71pA/\sqrt{Hz}$.

Using these corner frequencies and noise magnitudes, E_n and I_n are calculated to be 1.07μVrms and 118pArms, respectively. Multiplying this noise current by the source resistance gives terms 2 and 3 of Equation 2 as shown below:

$$(2)\quad E_n(f_H, f_L) = \sqrt{E_n^2 + I_{n1}^2 R_{S1}^2 + I_{n2}^2 R_{S2}^2 + E_{t1}^2 + E_{t2}^2}$$

substituting in the equation:

$$E_n(f_H, f_L) = \sqrt{(1.07\mu V)^2 + (0.106\mu V)^2 + (1.18\mu V)^2 + (0.04\mu V)^2 + (0.128\mu V)^2}$$

$$= 1.6\mu Vrms$$

Total input-referred noise = 9.6μV peak-to-peak (0.0001Hz to 100Hz). This is more than 8 times that of the low noise OP-77 example. Notice further in this example, the third term of the equation becomes an additional dominant term. It is due to a higher noise current flow in the 10kΩ source resistance.

The calculation examples illustrate four rules for minimizing noise in operational amplifier applications:

Rule 1. Use an op amp with low noise characteristics.

Rule 2. Use an op amp with low noise corner frequencies.

Rule 3. Keep source resistances as low as practical.

Rule 4. Limit circuit bandwidth to signal bandwidth.

FIGURE 11A: Input Noise Voltage as a Function of Frequency

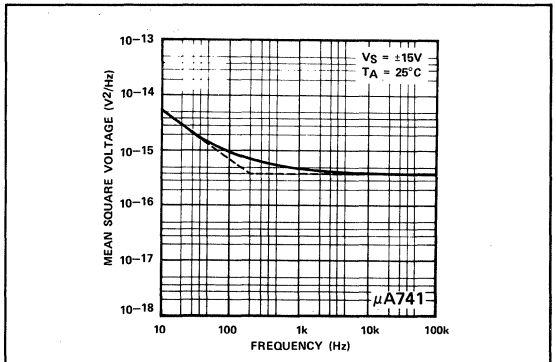


FIGURE 11B: Input Noise Current as a Function of Frequency

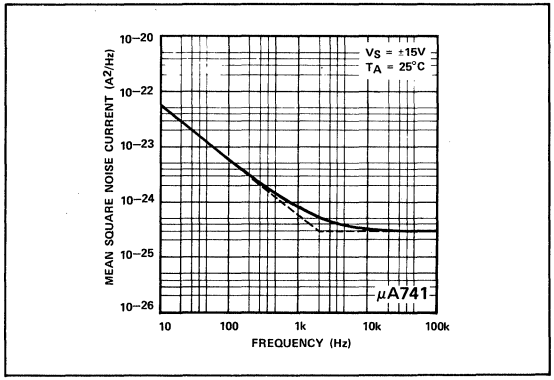
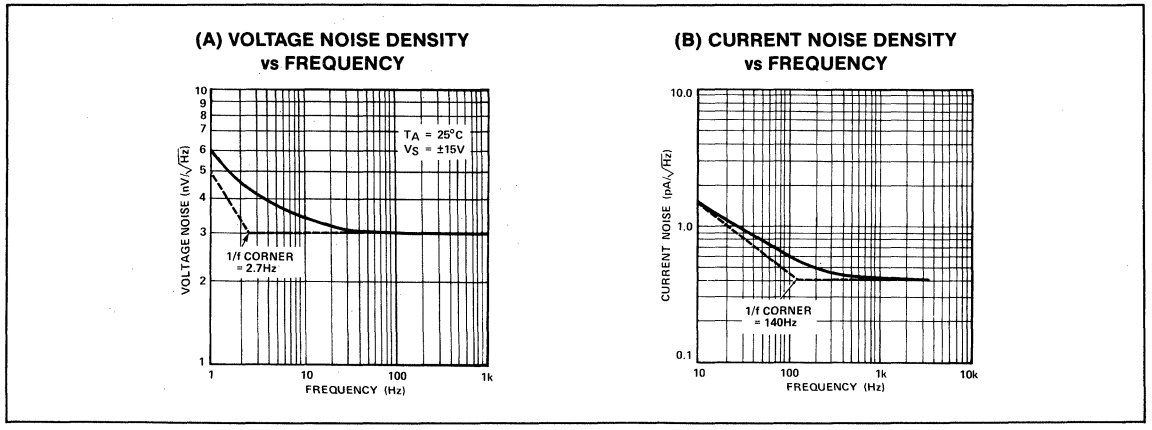


FIGURE 12: OP-27, OP-37, and OP-227 Noise Voltage and Current as a Function of Frequency



OP-27/OP-227/OP-37 Noise Optimization Design

In this example, a low noise, high speed op amp is examined. Using the circuits in Figures 10A and 10B, and using the data sheet curves of Figures 12A and 12B:

$f_{ce} = 2.7Hz$; $f_{ci} = 140Hz$; $e_n = 3.0nV/\sqrt{Hz}$;
$i_n = (\sqrt{2}) \cdot (0.4pA/\sqrt{Hz}) = 0.57pA/\sqrt{Hz}$

Using these corner frequencies and noise magnitudes, E_n and I_n are calculated to be 0.035μVrms and 25.7pArms, respectively. Multiplying the noise currents by the source resistances yield terms 2 and 3 of Equation 2 as shown below:

$$E_n(f_H, f_L) = \sqrt{E_n^2 + I_{n1}^2 R_{S1}^2 + I_{n2}^2 R_{S2}^2 + E_{t1}^2 + E_{t2}^2}$$

$$= \sqrt{(0.035\mu V)^2 + (0.023\mu V)^2 + (0.257\mu V)^2 + (0.04\mu V)^2 + (0.128\mu V)^2}$$

$$= 0.293\mu Vrms$$

Total input-referred noise = 1.76μV peak-to-peak (0.0001Hz to 100Hz).

Contrary to expectation, these supposedly lower noise amplifiers produce a circuit that has higher total noise than the previous OP-77 design. A closer analysis reveals again that the 10kΩ source resistance is the primary contributor to the two dominant terms (terms 3 and 5) of the total noise equation. The resulting noise generated swamped the excellent noise performance of these devices.

For the purpose of noise optimization, the 10kΩ source resistance is reduced to a balanced 910Ω resistance to preserve the inherently low input offset error of the amplifier. Recalculating Equation 2,

$$E_n(f_H, f_L) = \sqrt{(0.035\mu V)^2 + (0.023\mu V)^2 + (0.023\mu V)^2 + (0.04\mu V)^2 + (0.04\mu V)^2}$$

$$= 0.074\mu Vrms$$

Total input-referred noise is now a respectable 0.44μV peak-to-peak (0.0001Hz to 100Hz).

It is clear from this optimization that the system designer can achieve both a balance of low noise and low input offset voltage performance with these amplifiers. It is also obvious that one can optimize noise further by using, say, a 10Ω source resistance; in which case, the resulting total rms noise voltage is now 0.058μV, and a peak-to-peak noise is 0.35μV. This translates to a net noise reduction of 20% compared to the design using 1kΩ balance source resistance.

LIMITING BANDWIDTH TO MINIMIZE NOISE

Effective circuit bandwidth must not be much greater than signal bandwidth or amplification of undesirable high frequency noise components will occur. Throughout the preceding calculations, an assumption of "bandwidth-of-interest" was made, while in actual application the amplifier's bandwidth must be considered.

In Figure 13, the OP-77 frequency response curves show a rolloff of 20dB/decade; integration of the area under the curve will show the effective circuit noise bandwidth to be 1.57 times the 3dB bandwidth. In most closed-loop gain configurations, the amplifier's bandwidth may be greater than required, and output filtering, such as in Figure 14, could be used. As an alternate to output filtering, an integrating capacitor may be connected across the feedback resistor. Bandwidth may also be limited in some applications by overcompensating an externally-compensated low noise op amp, such as the OP-06.

FIGURE 13A: OP-77 Open-Loop Frequency Response

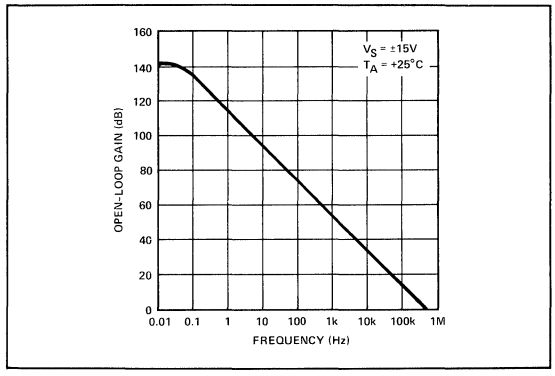


FIGURE 13B: OP-77 Closed-Loop Response for Various Gain Configurations

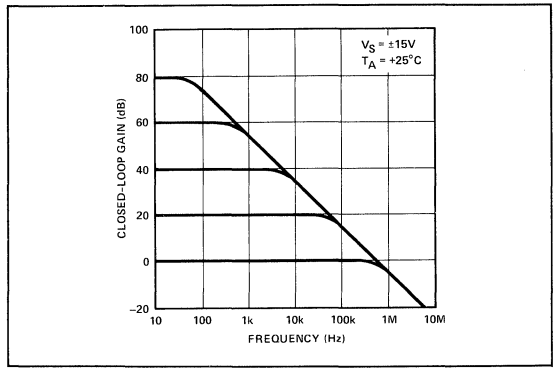
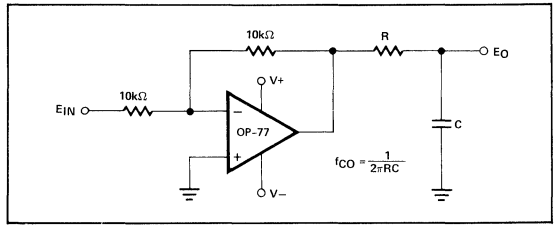


FIGURE 14: Output Filtering



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MISCELLANEOUS NOISE MINIMIZATION METHODS

Certain other noise mechanisms merit consideration: use metal film resistors; carbon resistors exhibit "excess noise," with both 1/f and white noise content being related to DC applied voltage. The use of balanced source resistors, while sometimes good for DC error purposes, will increase noise; the balancing resistor is not required for op amps such as the OP-07 and OP-77, since $I_{OS} \cong I_B$. Keep noise in its proper perspective; minimize it without introducing additional DC errors. Use low noise op amps with overall DC specifications that will satisfy the application.

OTHER NOISES

Shot noise (Schottky noise) is a white noise current associated with the fact that current flow is actually a movement of discrete charged particles (electrons) across a potential barrier, such as a PN junction of a transistor or diode. Shot noise is a component of i_n, and indirectly, e_n. In Figure 6, I_{n1} and I_{n2}, above the 1/f frequency, are shot noise currents which are related to the amplifier's DC input bias currents:

$$(20) \quad I_{sh} = \sqrt{2qI_{DC}(f_H - f_L)}$$

Where: I_{sh} = rms shot noise value in amps

q = Charge of an electron = 1.602×10^{-19} C

I_{DC} = DC bias current in amps

f_H = Upper frequency limit in hertz

f_L = Lower frequency limit in hertz

At room temperature Equation 20 simplifies to:

$$(21) \quad I_{sh} = 5.66 \times 10^{-10} \sqrt{I_{DC}(f_H - f_L)}$$

Shot noise currents also flow in the input-stage emitter dynamic resistances (r_e), producing input noise voltages. These voltages, along with the r_{bb}' thermal noise, make up the white noise portion of E_n; the total equivalent input noise voltage generator.

Shot noise can also be generated from external sources such as PIN photodiodes, zener diodes, and other semiconductor junction devices. Noise current from these sources may be calculated using Equation 20 or 21.

In limited bandwidth, very low frequency applications, *flicker* (1/f) noise is the most critical noise source. An op amp designer minimizes flicker noise by keeping current noise components in the input and second stages from contributing to input voltage noise. Equation 22 illustrates this relationship:

$$(22) \quad \frac{i_{n\ \text{second stage}}}{g_{m\ \text{first stage}}} = e_{n\ \text{input}}$$

Another critical factor is corner frequency. For minimum noise, the current and voltage noise corner frequencies must be low; this is crucial. As shown in Figure 15, low-noise corner frequencies distinguish low-noise op amps from ordinary industry-standard 741 types.

The photograph in Figure 16, taken using the test circuit of Figure 17, illustrates the flicker noise performance of the OP-77. This device demonstrates proper attention to low noise circuit design and wafer processing and achieves a remarkable 0.35μV peak-to-peak input voltage noise in the 0.1Hz to 10Hz bandwidth.

FIGURE 15: Noise Voltage Comparison

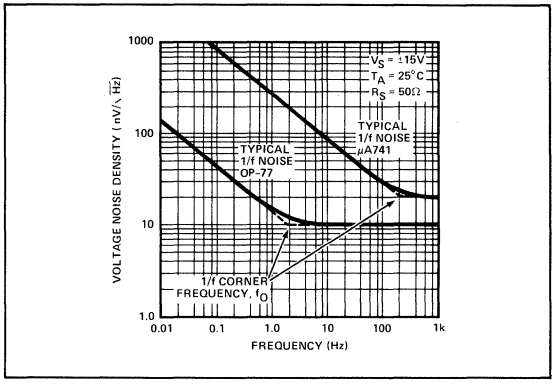


FIGURE 16: OP-77 Low Frequency Noise

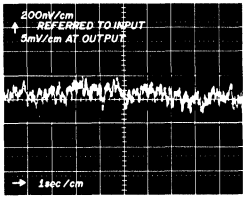
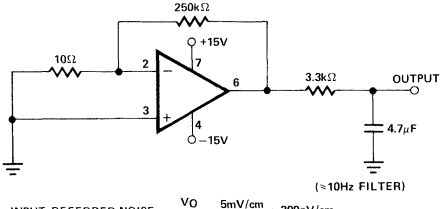


FIGURE 17: Low Frequency Noise Test Circuit

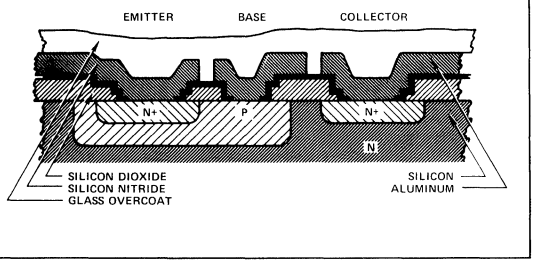


Popcorn noise (burst noise) is a momentary change in input bias current usually occurring below 100Hz, and is caused by imperfect semiconductor surface conditions incurred during wafer processing. Precision Monolithics minimizes this problem through careful surface treatment, general cleanliness, and a special three-step process known as "Triple Passivation."

To begin the process, a specially-treated thermal silicon dioxide layer is grown. This protects the junctions and also attracts any residual ionic impurities to the top surface of the oxide, where they are held fixed. Next, a layer of silicon nitride is applied to prevent the entry of any potential contamination or impurities.

The third step is the thick glass overcoat which leaves only the bonding pads exposed. A cutaway view of a finished device is shown in Figure 18.

FIGURE 18: Triple Passivated Integrated Circuit Process



Op amp manufacturers face a difficult decision in dealing with popcorn noise. Through careful low noise processing, it can be eliminated from almost all devices; alternatively, the processing may be relaxed, and finished devices must be individually tested for this parameter. Special noise testing takes valuable labor time, adds significant amounts to manufacturing cost, and ultimately increases the price a customer has to pay. At Precision Monolithics, the low noise process alternative is used to manufacture high volumes of cost-effective low noise op amps.

SUMMARY

A summary of the major points to consider is as follows:

1. Minimize externally-generated noise.
2. Choose an amplifier with low noise characteristics and low 1/f noise corner frequencies.
3. Limit the circuit bandwidth to signal bandwidth.
4. Eliminate excessive resistance in the input circuit.

CONCLUSION

Recent improvements in IC op amp DC specifications have made noise an important error consideration. From data sheet information and source resistance values, total input-referred noise over a given bandwidth can be easily calculated. Total noise can be minimized by a thorough understanding of the various noise-generation mechanisms.

NOISE BIBLIOGRAPHY

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Very Low Noise Operational Amplifier

APPLICATIONS

- High Precision Instrumentation
- Microphone Preamplifier
- Tape-Head Preamplifier
- Strain-Gage Amplifier

FEATURES

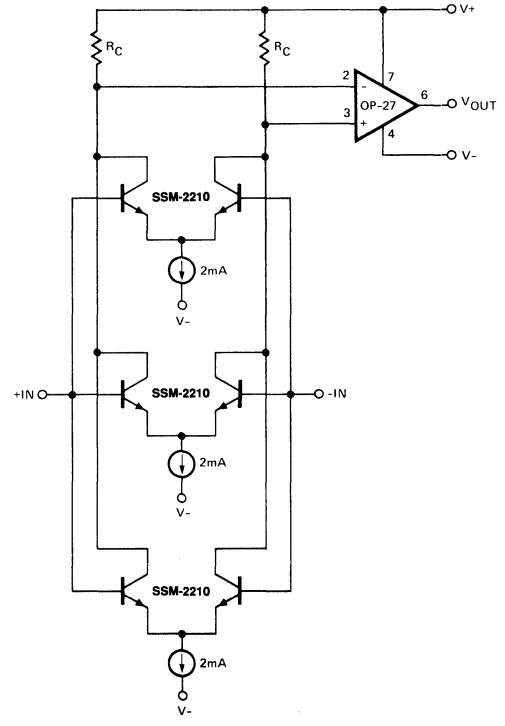
- Very Low Voltage Noise ..... 500pV/$\sqrt{Hz}$
- High Gain-Bandwidth Product 150MHz
- High Open-Loop Gain ..... 3×10^7
- High CMRR 130dB
- Very Low Offset Voltage Drift ..... <0.1μV/°C

GENERAL DESCRIPTION

In situations where low output, low-impedance transducers are used, amplifiers must have very low voltage noise to maintain a good signal-to-noise ratio. The design presented in this application note is an operational amplifier with only 500pV/$\sqrt{Hz}$ of broadband noise. The front end uses SSM-2210 low-noise dual transistors to achieve this exceptional performance. The op amp has superb DC specifications compatible with high-precision transducer requirements, and AC specifications suitable for professional audio work.

PRINCIPLE OF OPERATION

The design configuration in Figure 1 uses an OP-27 op amp (already a low-noise design) preceded by an amplifier consisting of three parallel-connected SSM-2210 dual transistors. Base spreading resistance (R_{bb}) generates thermal noise which is reduced by a factor of $\sqrt{3}$ when the input transistors are parallel connected. Schottky noise, the other major noise-generating mechanism, is minimized by using a relatively high collector current (1mA per device). High current ensures a low dynamic emitter resistance, but does increase the base current and its associated current noise. Higher current noise is relatively unimportant when low-impedance transducers are used.



Simplified Schematic for Very Low Noise Operational Amplifier

Figure 1: Simplified Schematic

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CIRCUIT DESCRIPTION

The detailed circuit is shown in Figure 2. A total input-stage emitter current of 6mA is provided by Q4. The transistor acts as a true current source to provide the highest possible common-mode rejection. R_1, R_2, and R_3 ensure that this current splits equally among the three input pairs. The constant current in Q4 is set by using the forward voltage of a GaAsP light-emitting diode as a reference. The difference between this voltage and the base-emitter voltage of a silicon transistor is predictable and constant (to within a few percent over the military temperature range. The voltage difference, approximately 1V, is impressed across the emitter resistor R_{12} which produces a temperature-stable emitter current.

R_6 and C_1 provide phase compensation for the amplifier and are sufficient to ensure stability at gains of ten and above.

R_7 is an input offset trim that provides approximately ±300μV trim range. The very low drift characteristics of the SSM-2210 make it possible to obtain drifts of less than 0.1μV/°C when the offset is nulled close to zero. If this trim is not required, the R_4, R_7, and R_8 network should be omitted and R_5/R_9 connected directly to V+.

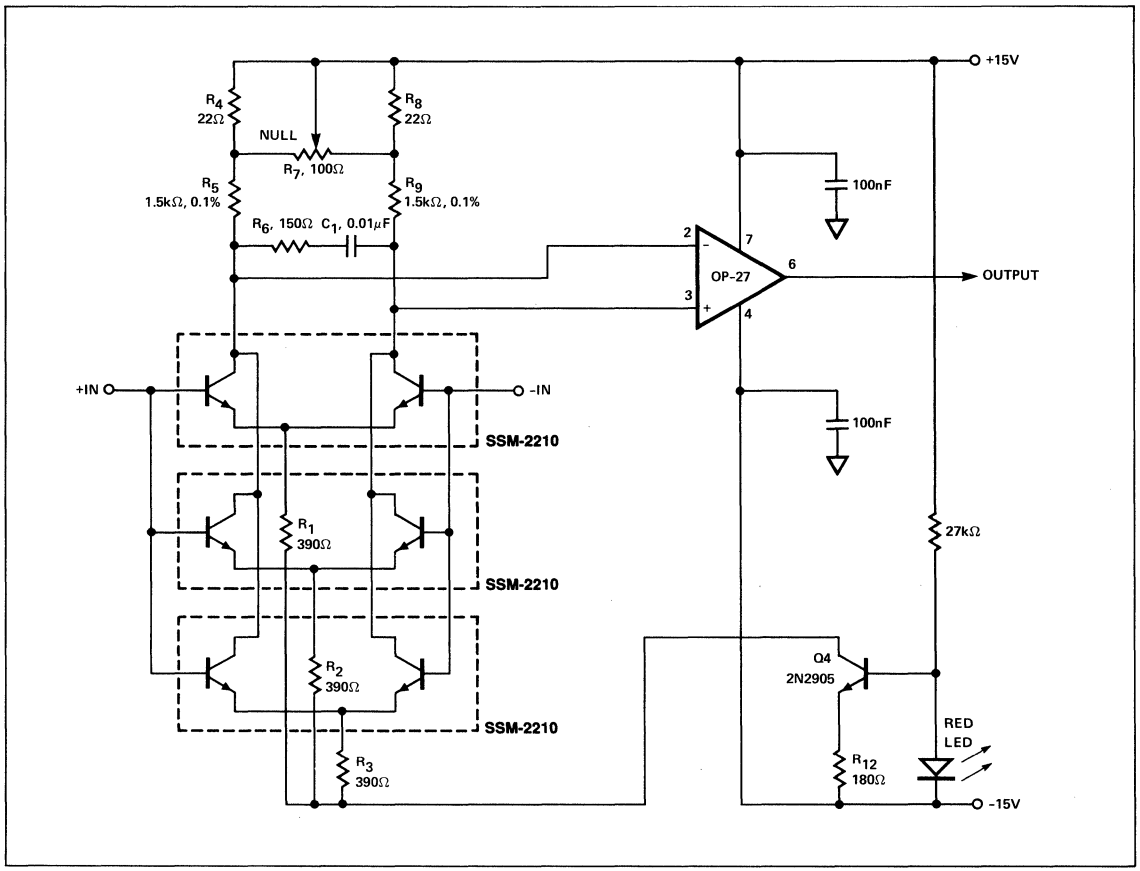


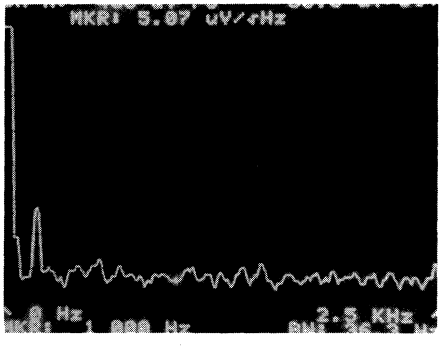
Figure 2: Complete Amplifier Schematic

AMPLIFIER PERFORMANCE

The measured performance of the op amp is summarized in Table 1. Figure 3 shows the broadband noise spectrum which is flat at about 500 pV/$\sqrt{Hz}$. Figure 4 shows the low-frequency spectrum which illustrates the low 1/f noise corner at 1.5Hz. The low-frequency characteristic in the time domain from 0.1Hz to 10Hz is shown in Figure 5; peak-to-peak amplitude is less than 40nV.

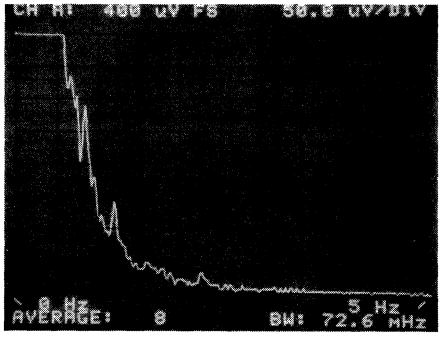
Table 1: Measured Performance of the Op Amp

Input Noise Voltage Density at 1kHz		500pV/$\sqrt{Hz}$
Input Noise Voltage from 0.1Hz to 10Hz		40nV$_{p-p}$
Input Noise Current at 1kHz		1.5pA/$\sqrt{Hz}$
Gain-Bandwidth	G = 10	3MHz
	G = 100	600kHz
	G = 1000	150kHz
Slew Rate		2V/μs
Open-Loop Gain		3×10^7
Common-Mode Rejection		130dB
Input Bias Current		3μA
Supply Current		10mA
Nulled TCV$_{OS}$		0.1μV/°C Max
T.H.D. at 1kHz	G = 1000	0.002%



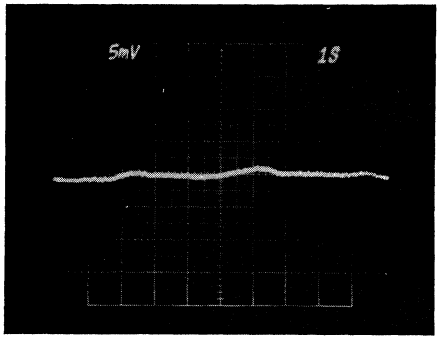
Spectrum analyzer display of broadband noise with a gain of 10,000.
Horizontal axis = 0 to 2.5kHz.
Normalized vertical axis = 830pV/$\sqrt{Hz}$ R.T.I.
e_n = 507pV/$\sqrt{Hz}$ at 1kHz.

Figure 3: Spectrum Analyzer Display — Broadband



Low frequency noise spectrum at a gain of 10,000 showing a low 1.5Hz noise corner.

Figure 4: Spectrum Analyzer Display — Low Frequency



Peak-to-peak noise from 0.1 to 10Hz.
Overall gain is 100,000.

Figure 5: Oscilloscope Display

CONCLUSION

Using SSM-2210 matched transistor pairs operating at a high current level, it is possible to construct a high-performance, low-noise operational amplifier. The circuit uses a minimum of components and achieves performance levels impractical with monolithic amplifiers.

ANALOG DEVICES

AN-105
APPLICATION NOTE

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Applications of the MAT-04
A Monolithic Matched Quad Transistor

The MAT-04 is a monolithic device containing four low-noise, tightly matched transistors, which dramatically improves the performance of many amplifier and analog computational circuits. This note describes several of these designs which capitalize on the superior characteristics and dynamic range of the MAT-04. These applications include a low-distortion voltage-controlled attenuator, a very low-noise ($1.2nV/\sqrt{Hz}$) high-speed instrumentation amplifier, a $900pV/\sqrt{Hz}$ ultra-low noise audio preamplifier, a vector summing amplifier, a squaring amplifier, and a square-root amplifier.

Discrete circuit designers repeatedly run into the problem of circuit component mismatches that limit performance. Passive component mismatching can be reduced by using tighter tolerance components, but active components present a more difficult problem. Discrete transistors exhibit poor beta and $V_{BE(ON)}$ matching, even within single transistor families, which severely degrade amplifier performance. Most available transistor arrays however, were developed to save board space rather than to provide accurate parametric matching. Only a few are designed to have tight matching tolerance.

The MAT-04 uses advanced layout and process techniques to guarantee that the offset voltage between **any** two transistors in the device will be no more than 200μV, and beta mismatch will not exceed 2%. Additionally, the MAT-04 transistors are designed for high beta (400 minimum) and 40V minimum breakdown. It exhibits a low 0.4Ω bulk resistance, which is important in logarithmic circuit applications. The MAT-04 uses a symmetrical quad transistor pinout (Figure 1) which allows incorrect orientation of pin 1 without damage. The base-emitter junctions are internally diode-protected against reverse zener breakdown, which protects against degradation of beta and matching characteristics.

VOLTAGE-CONTROLLED ATTENUATOR

A useful MAT-04 application is the Voltage-Controlled Attenuator (VCA) of Figure 2. This circuit, widely used in professional audio applications, is difficult to implement using discrete transistors due to distortion induced by transistor mismatching. The MAT-04 offers excellent matching which

FIGURE 1: Pin Connections

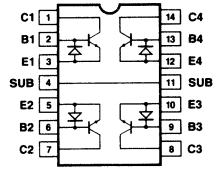
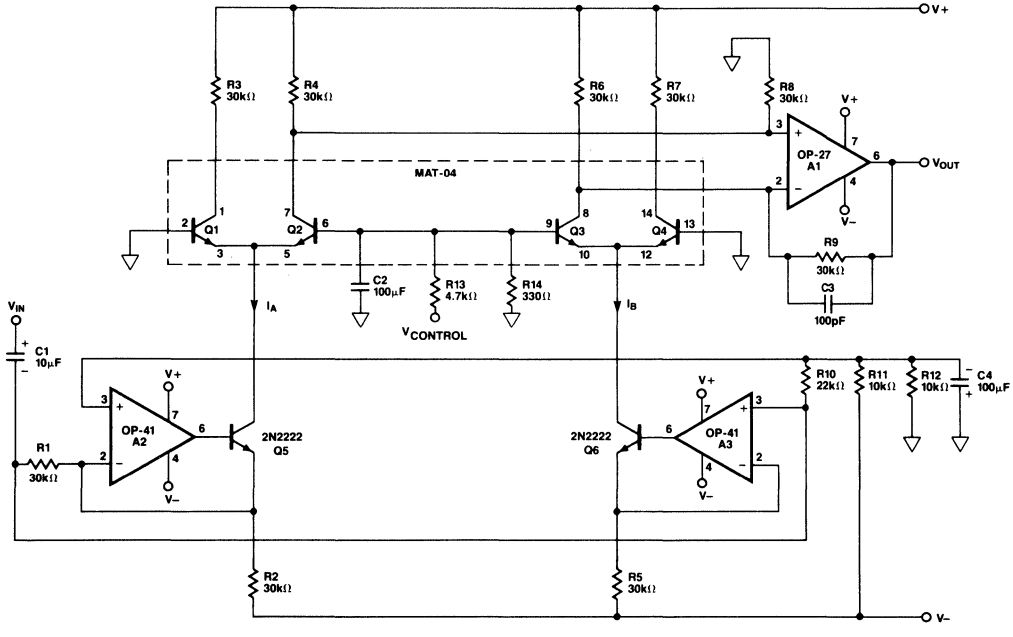


FIGURE 2: Voltage-Controlled Attenuator



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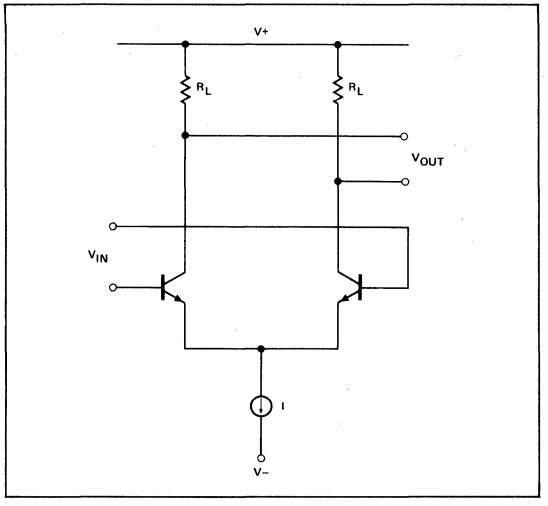
dramatically reduces distortion. The VCA provides low-distortion attenuation over a wide range of control voltages, and can be used as a low-distortion gain control in an audio amplifier.

The VCA design is based upon the amplifying characteristics of a differential pair. Figure 3 shows the classic differential pair. With zero volts between the inputs (V_{IN} = 0V), the current in each side of the differential pair is equal and therefore the output voltage equals zero. Small changes in V_{IN} unbalance the currents flowing in each side of the differential pair and produce an amplified differential output. The total stage current (I) of the differential pair is constant regardless of the input voltage. Matching of the transistors in a differential pair is critical, as any device mismatch will cause DC errors and upset linearity.

FIGURE 3: Classic Differential Pair



In the Voltage-Controlled Attenuator, the input signal modulates the stage currents of the two differential amplifier stages. Op amps A2 and A3, in conjunction with transistors Q5 and Q6, form two voltage-to-current converters that transform a single input voltage into differential currents, which form the stage currents I_A and I_B (see Figure 2) of each differential pair. The transfer function of the voltage-to-current converter is:

$$(1)\quad I_A = \frac{-V_{IN}}{R2}$$

$$(2)\quad I_B = \frac{V_{IN}}{R5}$$

Low-cost unmatched transistors can be used for Q5 and Q6, since they are inside the feedback loop of op amps A2 and A3. Their beta mismatch has minimal effect on output offset.

If all the bases of the MAT-04 are at ground potential, then the stage currents of each differential pair split equally among each transistor. The output is taken from one side of each differential pair (Q2 and Q3) and converted to a single-ended signal by op amp A1 which has a stage gain of 1. The gain of the overall circuit with the bases of the MAT-04 at ground potential is:

(3)

$$\frac{V_{OUT}}{V_{IN}} = \left[\left(\frac{1}{2}\right)(V_{IN})\left(\frac{R6}{R5}\right)\right] - \left[\left(-\frac{1}{2}\right)(V_{IN})\left(\frac{R4}{R2}\right)\right]$$

$$= V_{IN}\,\frac{(R2 \cdot R6 + R4 \cdot R5)}{(2R2 \cdot R5)}$$

and since R2 = R4 = R5 = R6, $\frac{V_{OUT}}{V_{IN}} = 1$

When a positive control voltage is applied, most of the stage current is diverted into transistors Q2 and Q3, resulting in an increase in circuit gain. However, when a negative control voltage is applied, most of the stage current is diverted through transistors Q1 and Q4, with a subsequent decrease in circuit gain.

The ideal transfer function for the Voltage-Controlled Attenuator is:

$$(4)\quad \frac{V_{OUT}}{V_{IN}} = \frac{2}{1 + \exp\left[\dfrac{(-V_{CONTROL})\left(\dfrac{R14}{R13 + R14}\right)}{\left(\dfrac{kT}{q}\right)}\right]}$$

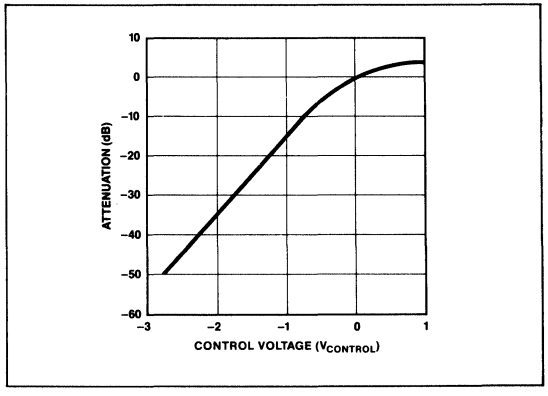
where k = Boltzmann constant = 1.38×10^{-23} J/°K

T = temperature in °K

q = electronic charge = 1.602×10^{-19} C

From the transfer function, it can be seen that the maximum gain of the circuit is 2 (6dB). Figure 4 shows the increase in attenuation as the control voltage becomes more negative.

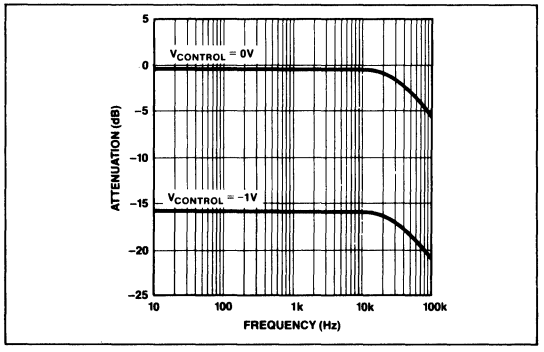
FIGURE 4: Voltage-Controlled Attenuator, Attenuation vs Control Voltage at 1kHz, 25°C



The Voltage-Controlled Attenuator accepts a 3Vrms input and easily handles the full 20Hz — 20kHz audio bandwidth as indicated in Figure 5. Distortion typically runs under 0.03% and the noise level is more than 110dB below maximum output.

To insure best performance, resistors R2 through R7 should be 1% metal film resistors. Since capacitor C2 can see a small amount of reverse bias when the control voltage is positive, a nonpolarized tantalum capacitor or two polarized capacitors connected back-to-back should be used.

FIGURE 5: Voltage-Controlled Attenuator, Attenuation vs Frequency



A LOW-NOISE, HIGH-SPEED INSTRUMENTATION AMPLIFIER

The circuit of Figure 6 has performance characteristics which make it ideal for use in high precision transducer and professional audio applications. The circuit uses a high-speed op amp, the OP-17, preceded by an input amplifier consisting of a precision matched dual transistor, the MAT-02, and a MAT-04. The arrangement of the MAT-04 is known as a "linearized cross quad" and acts as a voltage-to-current converter to provide feedback to the input stage. The OP-17 acts as an overall nulling amplifier to complete the feedback loop. Resistor pair R1 and R2, and resistor pair R3 and R4 form voltage dividers that attenuate the output feedback due to the limited input range of the "cross quad" arrangement. Biasing for the input stage is set by zener diode Z1. At low currents, the effective zener voltage is about 3.3V due to the soft knee characteristic of the zener diode. This results in a bias current of 530μA per side for the input stage.

The gain of the instrumentation amplifier, with the values shown in Figure 6, is:

$$(5)\quad \frac{V_{OUT}}{V_{IN}} = \frac{33{,}000}{R_G}$$

FIGURE 6: Low-Noise, High-Speed Instrumentation Amplifier

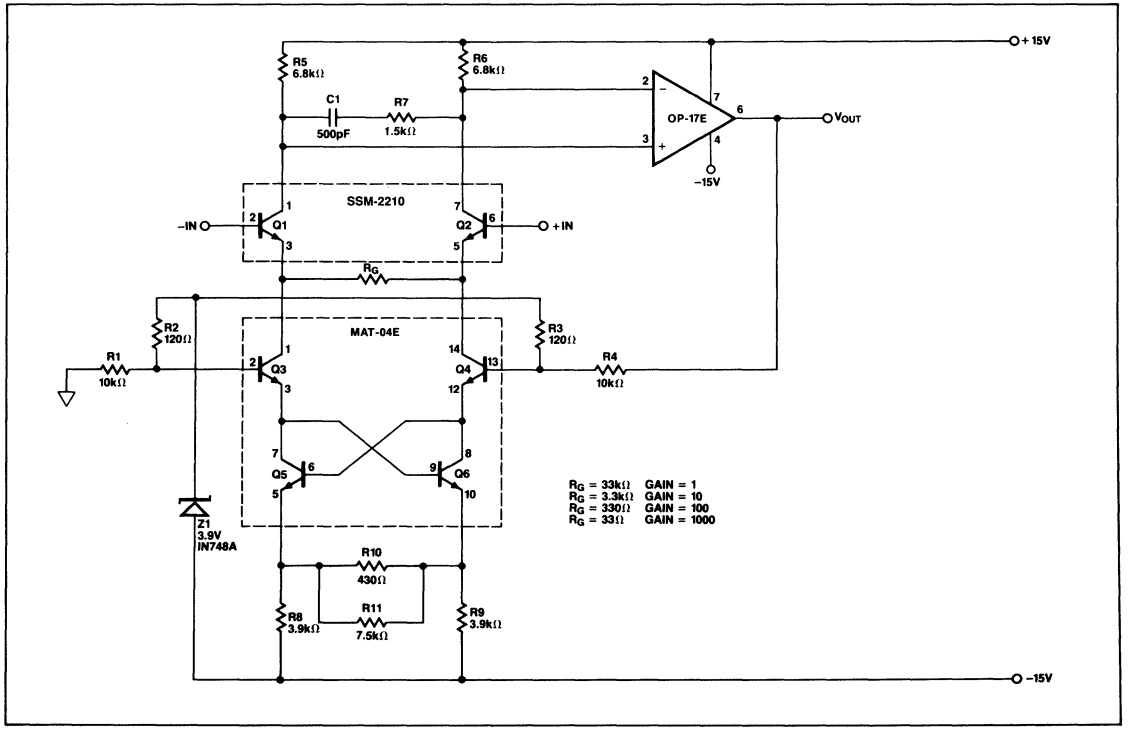


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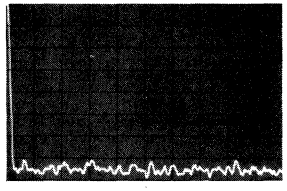
TABLE 1

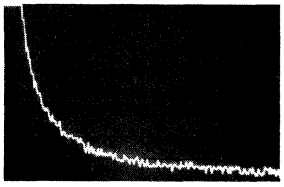
Input Noise Voltage Density	G = 1000 G = 100 G = 10	1.2nV/$\sqrt{Hz}$ 3.6nV/$\sqrt{Hz}$ 30nV/$\sqrt{Hz}$
Bandwidth	G = 500 G = 100 G = 10	400kHz 1MHz 1.2MHz
Slew Rate		40V/μs
Common-Mode Rejection	G = 1000	130dB
Distortion	G = 100 f = 20Hz to 20kHz	0.03%
Settling Time	G = 1000	10μs
Power Consumption		350mW

FIGURE 7: Spot Noise of Discrete Instrumentation Amplifier at Gain = 1000 from 0 to 25kHz



NORMALIZED VERTICAL AXIS = 2.6nV/$\sqrt{Hz}$ PER DIVISION
REFERENCED TO INPUT (R.T.I.).
e_n AT 10kHz = 1.2nV/$\sqrt{Hz}$

FIGURE 8: Low Frequency Noise Spectrum Showing Low 2Hz Noise Corner; Gain = 1000



HORIZONTAL AXIS = 0 TO 5Hz

The performance of the amplifier is summarized in Table 1. Figure 7 shows the input-referred spot noise to be flat at about 1.2nV/$\sqrt{Hz}$ over the 0 — 25kHz bandwidth. Figure 8 shows the low frequency noise spectrum which highlights the low 1/f noise corner at 2Hz.

In situations where small output, low impedance transducers are used, such as strain gages, amplifiers must have low voltage noise to maintain a good signal-to-noise ratio. The low voltage noise of 1.2nV/$\sqrt{Hz}$ suits this instrumentation amplifier for use in many low impedance transducer applications.

A LOW-NOISE HI-FI QUALITY PREAMPLIFIER

The AC-coupled preamplifier of Figure 9 exhibits an input-referred noise voltage density of only 900pV/$\sqrt{Hz}$ at a gain of 200. Preamplifier noise is minimized by using a single-ended input stage consisting of three transistors of a MAT-04 connected in parallel. This technique lowers the effective base-spreading resistance, reducing thermal noise from this source by a factor of $\sqrt{3}$. Tight matching of the three paralleled transistors is a critical requirement. If the matching is poor, one transistor will steal most of the stage current, effectively removing the two other transistors from the circuit. Noise reduction, achieved by paralleling the transistors, would therefore be lost. Schottky noise, or shot noise, is minimized by using a relatively high stage current of 2mA.

The fourth transistor (Q1) of the MAT-04 is used to bias the input stage. Op amp A1 forces the voltages across R1 and R2 to be equal, setting the bias current at 2mA. Overall feedback for the preamplifier is provided by resistors R7 and R8. Gain for this circuit is:

$$(6)\quad \frac{V_{OUT}}{V_{IN}} = \frac{R8 + 5\Omega}{5\Omega}$$

The circuit is characterized with the gain of 200. Compensation components R3 and C2 may need to be optimized for other values of gain. Open-loop gain of the preamplifier is over 10 million.

Figure 10 illustrates the wide bandwidth of the preamplifier. Figure 11 shows the broadband noise spectrum (0 — 25kHz) to be flat at 900pV/$\sqrt{Hz}$. Distortion of the preamplifier is 0.035% at V_{OUT} = 10V_{p-p}, f = 10kHz.

FIGURE 9: Low-Noise AC Preamplifier

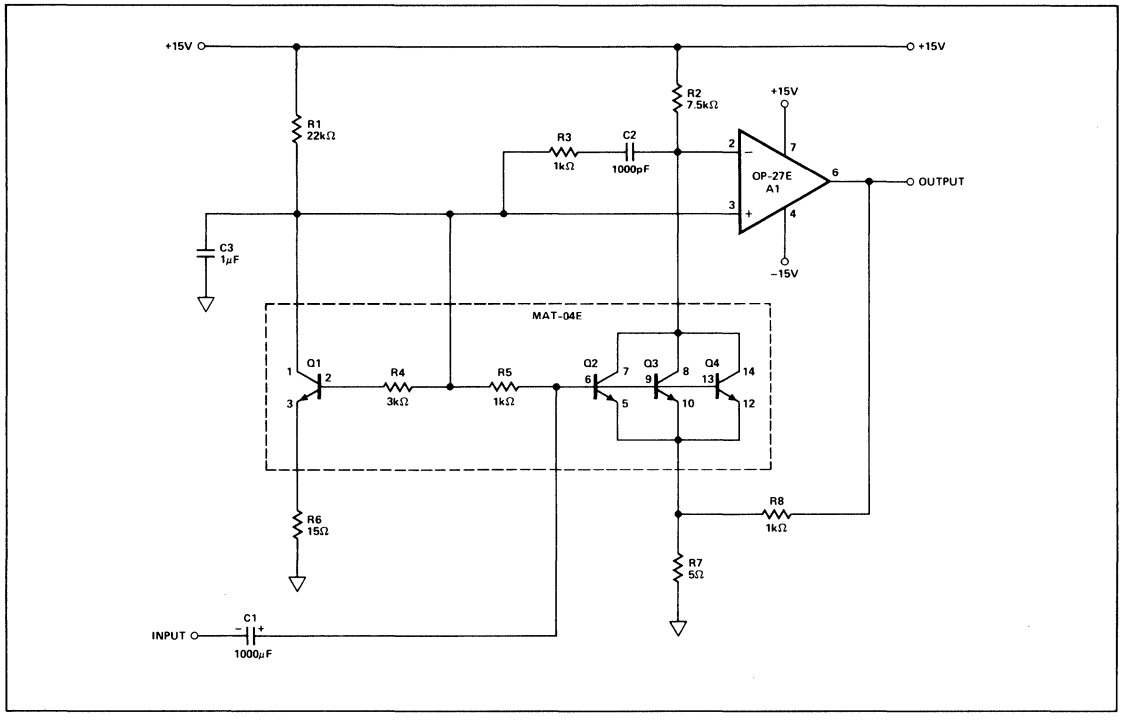


FIGURE 10: Low-Noise AC Preamplifier, Gain vs Frequency

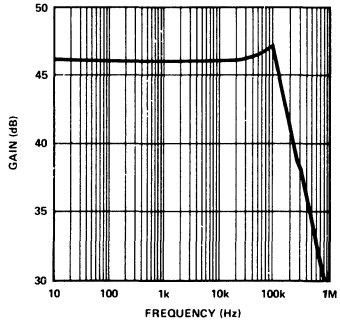
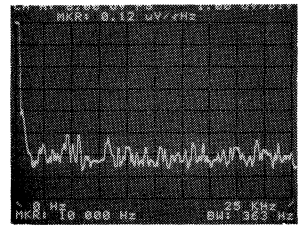


FIGURE 11: Spot Noise of AC Preamplifier at Gain = 200 from 0 to 25kHz



NORMALIZED VERTICAL AXIS = 260pV/$\sqrt{Hz}$ PER DIVISION REFERENCED TO INPUT.

e_n AT 10kHz = 600pV/$\sqrt{Hz}$

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NONLINEAR CIRCUIT APPLICATIONS

Another application area where precision matched transistors are a powerful tool is in the generation of nonlinear functions. These are based upon the transistor's logarithmic property which has the following form:

$$(7)\quad V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$$

where: $V_T = \frac{kT}{q}$

I_S = saturation current

The circuit of Figure 12 is a vector summing amplifier that has the following generalized transfer function:

(8) $V_{OUT} = k\sqrt{V_A^2 + V_B^2}$

where k is a scale factor

The circuit (see Figure 12) consists of two log amplifiers each using two transistors and an op amp. The voltage across the series transistors Q1 and Q2 is equal to the voltage across Q3 and the base-emitter of Q4. Summing this voltage loop leads to:

(9) $V_{T1} \ln\left(\frac{I_1}{I_{S1}}\right) + V_{T2} \ln\left(\frac{I_2}{I_{S2}}\right) = V_{T3} \ln\left(\frac{I_A}{I_{S3}}\right) + V_{T4} \ln\left(\frac{I_{OUT}}{I_{S4}}\right)$

All transistors are precisely matched and at the same temperature, therefore the I_S and V_T terms cancel. Equation 9 is simplified to:

(10) $2 \ln I_1 = \ln I_A + \ln I_O = \ln(I_A \cdot I_O)$

Exponentiating both sides yields:

(11) $I_1^2 = I_A \cdot I_O$

Similar analysis for transistors Q7, Q6, Q5, and Q4 leads to:

(12) $I_2^2 = I_B \cdot I_O$

Summing the currents at the emitter of Q4 gives:

(13) $I_O = I_A + I_B$

Solving equations (11) and (12) for I_A and I_B, and substituting into equation (13) yields:

(14) $I_O = \frac{I_1^2}{I_O} + \frac{I_2^2}{I_O} = \sqrt{I_1^2 + I_2^2}$

Op amp A3 forms a current-to-voltage converter giving $V_{OUT} = I_O \cdot R2$,

(15) $V_{OUT} = R2\sqrt{\left(\frac{V_A}{R1}\right)^2 + \left(\frac{V_B}{R3}\right)^2}$

For the circuit of Figure 12, R1 = R3, and $R2 = \frac{R1}{\sqrt{2}}$,

(16) $V_{OUT} = \left(\frac{1}{\sqrt{2}}\right)\sqrt{V_A^2 + V_B^2}$

A value of $R1/\sqrt{2}$ for resistor R2 builds in a scale factor of $1/\sqrt{2}$, which allows +10V to be applied to both inputs simultaneously without the danger of V_{OUT} exceeding the output range of op amp A3. The built-in protection diodes on the MAT-04 allow the input voltages to go negative without damaging the MAT-04. Under this condition, the output voltage is zero. The interconnections of the two MAT-04s in the circuit reduce errors due to inherent mismatching and temperature-induced differences between the two matched quad transistors. The accuracy of the vector summing amplifier is better than 0.5% over an input range of 10mV to 10V.

The MAT-04 can also be used to implement other nonlinear functions such as the square and square-root circuits shown in Figures 13 and 14 respectively. Similar to the vector summing amplifier, the analysis begins by summing the voltages across transistors Q1, Q2, Q3, and Q4 of the squaring circuit shown in Figure 13;

(17) $V_{T1} \ln\left(\frac{I_{IN}}{I_{S1}}\right) + V_{T2} \ln\left(\frac{I_{IN}}{I_{S2}}\right)$

$= V_{T3} \ln\left(\frac{I_O}{I_{S3}}\right) + V_{T4} \ln\left(\frac{I_{REF}}{I_{S4}}\right)$

FIGURE 12: Vector-Summing Amplifier

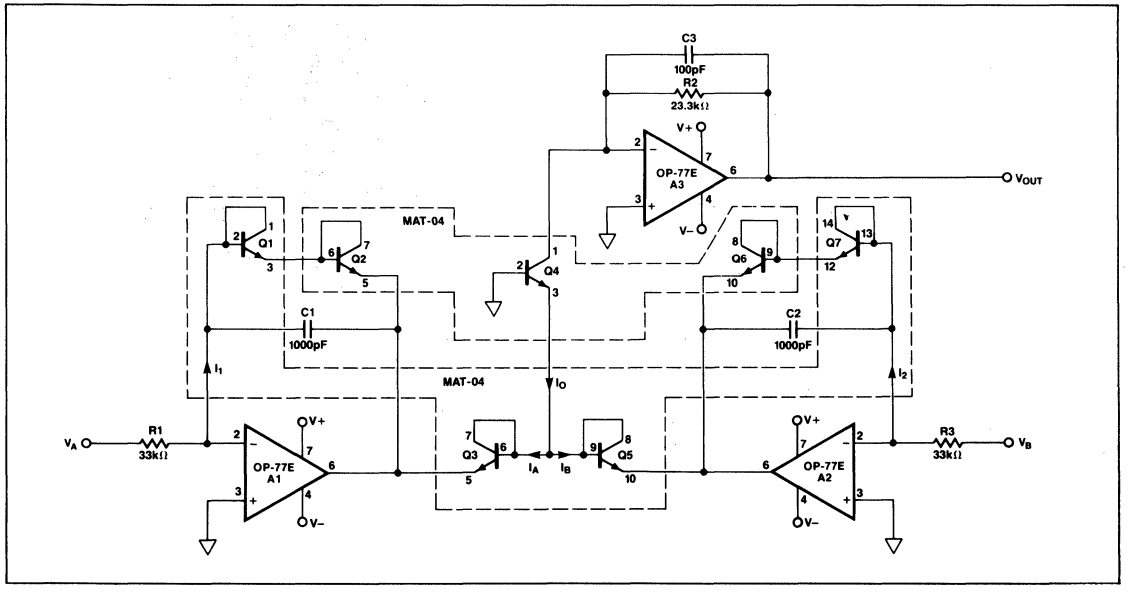


FIGURE 13: Squaring Amplifier

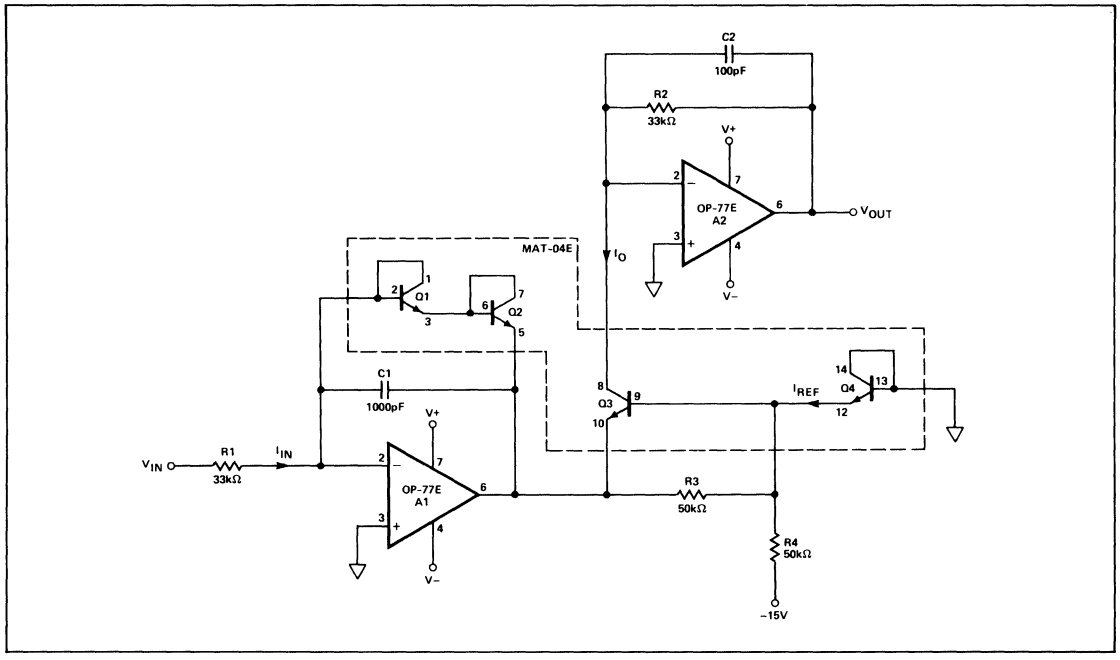
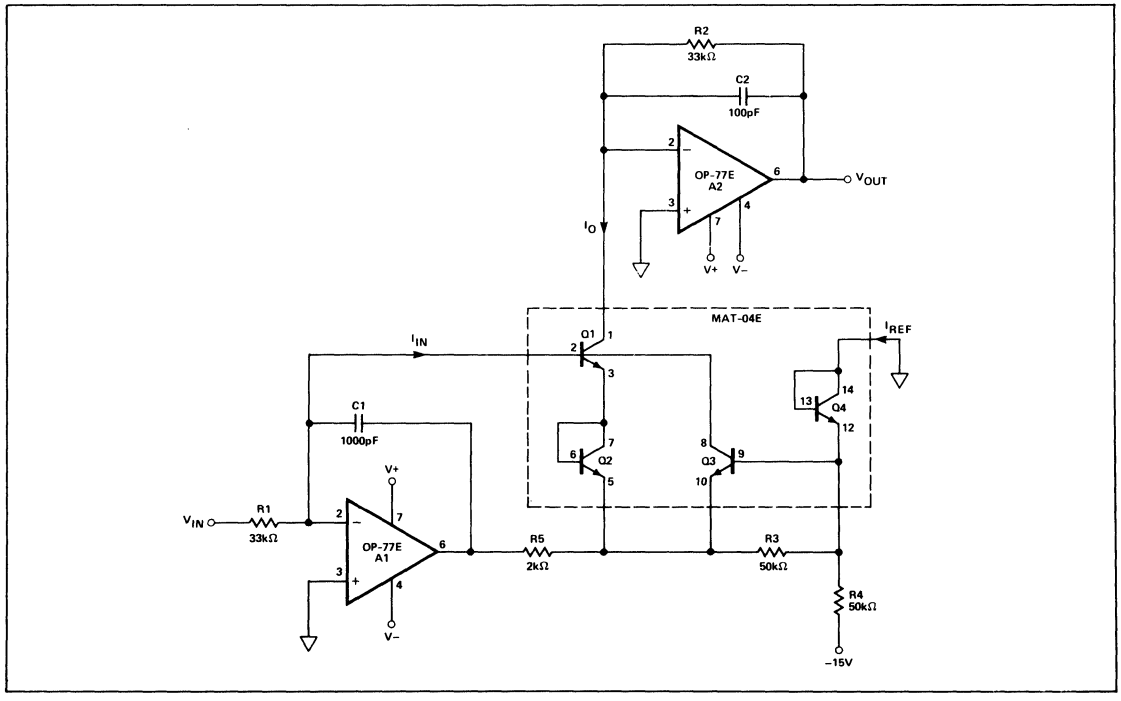


FIGURE 14: Square-Root Amplifier



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Once again, all the transistors are precisely matched and at the same temperature, so the I_S and V_T terms cancel giving:

$$(18)\quad 2\ln I_{IN} = \ln I_O + \ln I_{REF} = \ln(I_O \cdot I_{REF})$$

Exponentiating both sides of the equation leads to:

$$(19)\quad I_O = \frac{(I_{IN})^2}{I_{REF}}$$

Op amp A2 forms a current-to-voltage converter which gives $V_{OUT} = R2 \cdot I_O$. Substituting $(V_{IN}/R1)$ for I_{IN} and equation (19) for I_O yields:

$$(20)\quad V_{OUT} = \left(\frac{R2}{I_{REF}}\right)\left(\frac{V_{IN}}{R1}\right)^2$$

A similar analysis made for the square-root circuit of Figure 14 leads to its transfer function:

$$(21)\quad V_{OUT} = R2\sqrt{\frac{(V_{IN})(I_{REF})}{R1}}$$

In these circuits, I_{REF} is a function of the negative power supply. To maintain accuracy, the negative supply should be well regulated. For applications where very high accuracy is required, a voltage reference may be used to set I_{REF}. An important consideration for the squaring circuit is that a sufficiently large input voltage can force the output beyond the operating range of the output op amp. Resistor R4 can be changed to scale I_{REF}, or R1 and R2 can be varied to keep the output voltage within the usable range.

Unadjusted accuracy of the square-root circuit is better than 0.1% over an input voltage range of 100mV to 10V. For a similar input voltage range, the accuracy of the squaring circuit is better than 0.5%.

In summary, the accuracy of nonlinear circuits depends heavily upon the logarithmic conformance of the transistors used in the circuit. Extrinsic resistances and the Early effect cause a deviation from the ideal logarithmic transistor behavior. For small values of V_{CB}, the collector-base voltage, these effects can be lumped together as an effective bulk resistance, r_{BE}. The logarithmic transistor relationship of equation (7) changes to:

$$(22)\quad V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right) + (I_C\, r_{BE})$$

An obvious way to reduce r_{BE}-induced error in nonlinear circuits is to reduce the maximum collector currents, but the op amp offsets and leakage currents become a limiting factor at low input levels. An operating range of 10μA to 1mA is recommended. The MAT-04, which is specifically designed to have a low bulk resistance of 0.4Ω, further reduces r_{BE}-induced error in nonlinear circuits.

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A Balanced Summing Amplifier

The summing amplifier circuit shown in Figure 1 represents an excellent virtual ground summing amplifier using a balanced differential design that includes extremely low noise and wide bandwidth as featured by the SSM-2015. Any size audio mixing system can benefit from balanced virtual node mixing (summing). The low cost and exceptional performance of this design can be incorporated in any system with balanced or mixed balanced and unbalanced input sources.

IC_2, the PMI OP-41, serves as a DC servo-amplifier that is referenced to signal ground. The circuit functions as an integrator with a long time constant that retains the integrity of low frequency audio signals down to 5Hz, and keeps $e_{OUT} = 0V_{DC}$, ($\pm 10mV_{DC}$). The OP-41 is a FET input amplifier, with low input offset voltage (V_{OS}) and high input impedance. Although many low performance JFET/CMOS operational amplifiers can be employed, the summing output V_{DC} is a function of the servo's input offset voltage and its temperature coefficient ($\Delta V_{OS}/\Delta T$), which must be kept low for direct coupled summing applications.

In this design, the following facts predominate: $e_S = 0$, and $i_S = 0$. e_{IN} is the algebraic sum of the input(s) e_{IN1}, e_{IN2}, e_{IN3}, e_{INn} and etc. $e_{OUT} = [e_{IN1}(R_F/R_{IN1}) + e_{IN2}(R_F/R_{IN2}) + e_{IN3}(R_F/R_{IN3}) + e_{INn}(R_F/R_{INn})]$, etc. The input impedance therefore equals R_{IN1}, R_{IN2}, R_{IN3}, R_{INn}, etc. The overall gain of the circuit is set by R_F, and the gain of the individual channels can be adjusted independently by the values of R_{IN1}, R_{IN2}, R_{IN3}, R_{INn}, etc.

For individual source input(s), gain is $A_O = R_F/R_{IN}$.

The circuit configuration produces linear signal mixing at the summing nodes (IC_1 pins 10,11), whereas $e_S = 0$; therefore, no interaction occurs between the source inputs. Owing to the fact that the SSM-2015 is a bipolar transistor device, the noise is low ($1.3nV/\sqrt{Hz}$). The commonly used values of 10kΩ for R_F and R_{IN} are optimal for both minimum noise and previous stage loading, eliminating the need for buffer amplifiers and their noise contribution.

The input common-mode rejection for the SSM-2015 is typically 100dB as a result of true differential input topology. The differential thermal noise and DC offset drift is nearly eliminated by the common substrate construction employed. To exploit the high CMR of the SSM-2015, all signal resistors should be matched resistor networks or should employ 0.5% or better resistor tolerances.

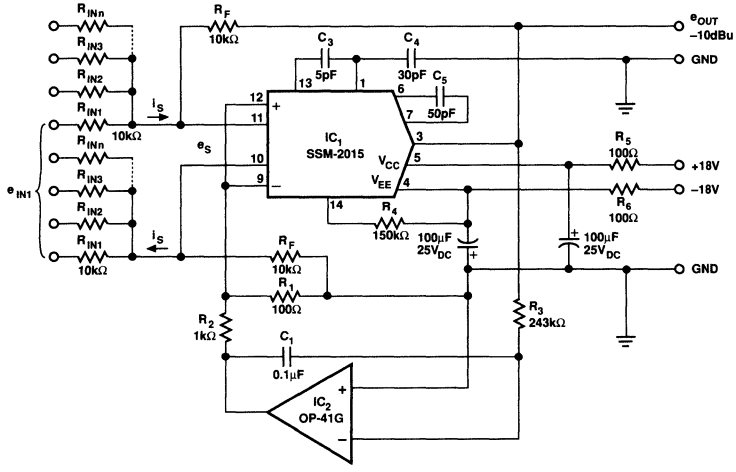

FIGURE 1

The output circuit topology of the SSM-2015 is complementary bipolar producing overall performance of 6V/μs slew rate, and is able to drive a 2kΩ unbalanced load. The circuit described can be directly coupled, eliminating coloration and distortion associated with coupling capacitors. The circuitry following this amplifier could be AC (capacitor) coupled if the DC servo IC_2 offset voltage of $\pm 10mV_{DC}$ is objectionable.

Audio performance challenges the best test equipment that might be used to measure high performance analog designs. For example: worst case THD for this circuit measures less than 0.008%, and IMD less than 0.02% over a band-width of 10Hz to 20kHz. See Table 1 for more performance details.

TABLE 1: Circuit Performance Specifications

Frequency Response (dB 20Hz to 20kHz)	±0.02
S/N Ratio @ +23dBu	103dB
TMD + Noise (@ +23dBu 20Hz to 20kHz)	0.008%
IMD (@ +23dBu SMPTE 60Hz & 4kHz, 4:1)	0.015%
CMRR (60Hz)	100dB
Slew Rate	6V/μs
Output Voltage (2kΩ load)	+23dBu or $11V_{RMS}$

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A Balanced Input High Level Amplifier

The balanced amplifier in Figure 1 utilizing the SSM-2015 features adjustable gain and can accept nominal audio signals from –27.5dBu to +0dBu with more than 30dB of headroom. The input terminals can tolerate common-mode voltages of 30 volts peak-to-peak. Common-mode noise rejection is greater than 100dB at 1,000Hz, while the EIN (Equivalent Input Noise) is a low –124dBu.

The IC_1 amplifier circuit is gain adjustable, and the design utilizes a 12-position switch with 2.5dB steps. Other resistor values can be calculated to accommodate custom gain requirements.

IC_1 is PMI's SSM-2015 true differential input IC amplifier. Its input circuit utilizes two identical low noise bipolar transistors, with access to the emitters that provide the gain adjustment. R_G (R_{14} through R_{24}) sets the amplifier's gain using the equation:

$$\text{Gain} = 3.5 + \left(\frac{20 \times 10^3}{R_G}\right) \text{ for } R_8, R_{18} = 10.0\text{k}\Omega$$

The emitter feedback design exhibits both minimum noise and maximum common-mode rejection while retaining a very high input impedance. The output circuit topology is complementary bipolar producing 6V/μs slew rate, and is able to drive a 2kΩ unbalanced load. The circuit described can be directly coupled eliminating the distortion associated with coupling capacitors. Circuitry following this amplifier could be AC (capacitor) coupled if input normal-mode DC voltages are expected at the input of this circuit. Worst case THD measures less than 0.008%, and IMD less than 0.015%.

Input components C_1, C_2, R_1, and R_2 constitute a single pole low-pass filter that limits the input voltage slew rate, curbs interface transient intermodulation distortion, and keeps the amplifier from slewing. The input network has little effect on phase response within the pass band of 20Hz to 20kHz. To maintain high frequency common-mode performance, capacitors C_1 and C_2 should be matched for 1% tolerance.

For an output voltage of –10dBu, the balanced input amplifier circuit has an input sensitivity range of 0.0dBu to –27.5dBu. The common-mode voltage trim is included for maximizing application common-mode noise reduction and also allows the use of low cost components.

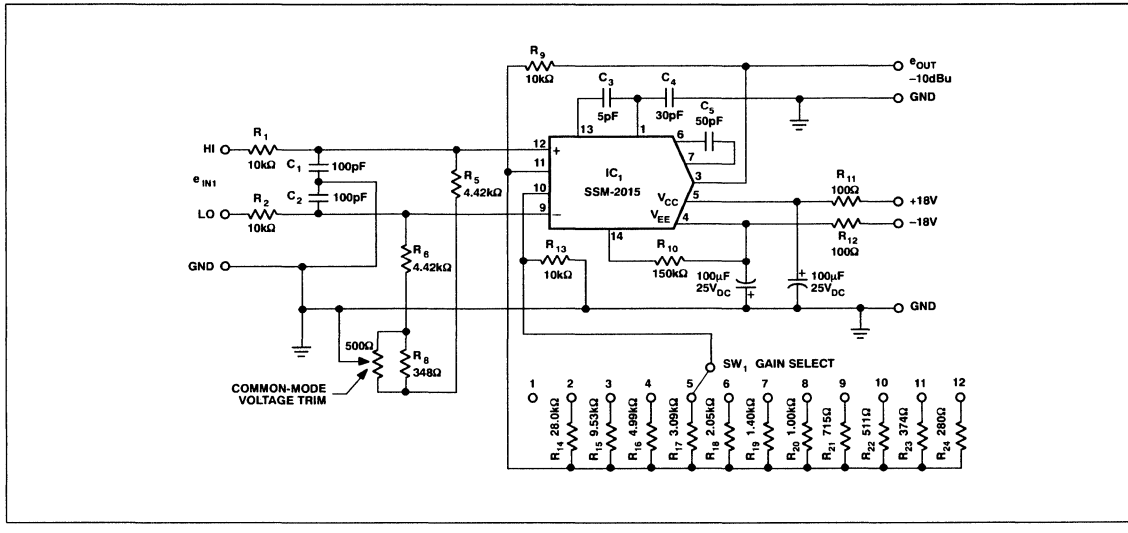

FIGURE 1

SW	G_{dB}	e_{IN}(dB)	R_G	VALUE (Ω)
1	10.0	0	R	ω
2	12.5	–2.5	R_{14}	28.0k
3	15.0	–5.0	R_{15}	9.53k
4	17.5	–7.5	R_{16}	4.99k
5	20.0	–10.0	R_{17}	3.09k
6	22.5	–12.5	R_{18}	2.05k
7	25.0	–15.0	R_{19}	1.40k
8	27.5	–17.5	R_{20}	1.00k
9	30.0	–20.0	R_{21}	715
10	32.5	–22.5	R_{22}	511
11	35.0	–25.0	R_{23}	374
12	37.5	–27.5	R_{24}	280

Specific gain can be calculated from the equation:

$$Gain_{dB} = 20 \log \left[3.5 + \left(\frac{20 \times 10^3}{R_G} \right) \right] \text{ for } R_8, R_{18} = 10.0k\Omega$$

TYPICAL APPLICATIONS

This design is ideal for use as the input amplifier in audio distribution amplifiers, for balanced input audio routing switchers, as the input buffer ahead of the A-to-D codec in digital recording and mixer equipment, or for the low noise high level input of mixing consoles.

TABLE 1: Circuit Performance Specifications

Frequency Response (dB 20Hz to 20kHz)	±0.1
S/N Ratio @ +23dBu	103dB
THD + Noise (20Hz to 20kHz) @ +23dBu	0.008%
IMD (SMPTE 60Hz & 4kHz, 4:1) @ +23dBu	0.015%
CMRR (60Hz)	100dB
Slew Rate	6V/μs
Output Voltage (2kΩ load)	+23dBu or $11V_{RMS}$

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An Unbalanced, Virtual Ground Summing Amplifier

The summing amplifier circuit shown in Figure 1 represents a splendid unbalanced virtual ground summing amplifier. The design utilizes the SSM-2134, PMI's superior version of the popular NE5534 bipolar operational amplifier. This low noise amplifier can now be implemented where most equipment manufacturers use FET input operational amplifiers. The circuit described features reduction in noise, temperature, and input impedance effects on static condition output voltages, and elimination of unity gain instability.

The SSM-2134 helps reduce wide-band noise figures by 3dB to 10dB, while improving the frequency and phase response performance. Only minimal value compensation (C_2) is required for the SSM-2134. In the feedback loop, C_1 improves stability while keeping the slew rate at 10V/μs and bandwidth greater than 100kHz.

In this circuit, note the following design facts: e_{OUT} is the algebraic sum of the input voltage(s) e_{IN1}, e_{IN2}, e_{IN3}, e_{INn} and etc. $e_{OUT} = (-) [e_{IN1} (R_F/R_{IN1}) + e_{IN2}(R_F/R_{IN2}) + e_{IN3}(R_F/R_{IN3}) + e_{INn}(R_F/R_{INn})]$, etc. The individual input impedance therefore equals R_{IN1}, R_{IN2}, R_{IN3}, R_{INn}, etc. The overall gain of the circuit is set by R_F, and the gain of the individual channels can be adjusted independently by the values of R_{IN1}, R_{IN2}, R_{IN3}, and R_{INn}.

For individual source input(s), voltage gain = R_F/R_{IN}.

The circuit configuration produces linear signal mixing at the summing node (common tie point C_1, R_F, R_{IN1}, R_{IN2}, R_{IN3}, and R_{INn}), whereas e_S = 0, there is no interaction between the source inputs. Owing to the fact that SSM-2134 is a bipolar device, noise is low ($2.8nV/\sqrt{Hz}$). The commonly used values of 10kΩ for R_F and R_{IN} are optimal for both minimum noise and previous stage loading, eliminating the need for buffer amplifiers and their noise contribution.

This design produces maximum amplifier bandwidth with unconditional circuit stability for both input and output impedance (reactive or not) variations.

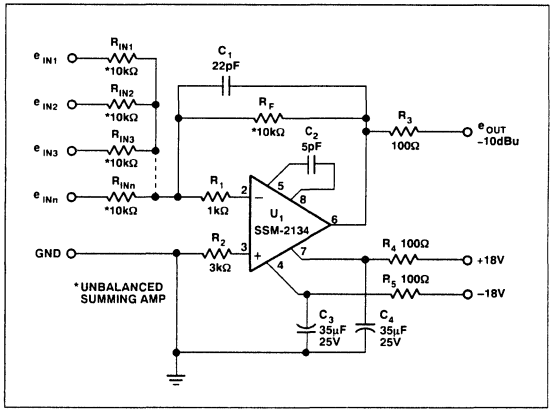

FIGURE 1

TABLE 1: Circuit Performance Specifications

Frequency Response (20Hz to 20kHz)	±0.02dB
S/N Ratio (@ +23dBu)	104dB
THD + Noise (@ +23dBu, 20Hz to 20kHz)	0.007%
IMD (SMPTE 60Hz and 4kHz, 4:1)	0.015%
Slew Rate	10V/μs
Output Voltage (2kΩ load)	+23.3dBu or 11.3V_{RMS}

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A High Performance Transformer-Coupled Microphone Preamplifier

The SSM-2015 or SSM-2016 low noise differential amplifier is utilized in a transformer-coupled microphone preamplifier. The circuit shown in Figure 1 represents a microphone preamplifier with high performance, wide dynamic range, and ultra low noise. The design features a Jensen transformer-coupled preamplifier circuit with balanced/floating input, 1500Ω input loading, three step input attenuator, phantom microphone powering, and twelve amplifier gain choices. Although the design shown includes a twelve position gain selector, fixed gain applications can utilize the component value calculations and formula provided.

The design provides microphone input loading of 1500Ω. Input loading is capacitive reactive, and at higher input voltage frequencies, the low-pass network and transformer characteristics help attenuate unwanted normal-mode RF and ultrasonic voltages that might be present at the input terminals.

The input circuit contains a three-position input attenuator used to optimize source levels versus amplifier headroom. As usual, it's a compromise of headroom and preamplifier signal-to-noise. The attenuation is 0dB, −10dB, and −20dB while maintaining an input impedance of 1500Ω.

A phantom microphone powering circuit is included for condenser microphones that require 24 to 48 volts DC power.

The common-mode voltage range is limited only by the transformer's primary-to-shield breakdown voltage. Common-mode rejection is a product of the primary-to-secondary isolation and provides detachment of the microphone wiring environment. Although the balanced single-pole low-pass filter at the input terminals provides protection from radio frequency interference, this network, along with the capacitive effect of the primary winding to the grounded shield, plus the phantom powering resistors present a circuit path for external RF voltages to enter the preamplifier's circuit ground. A carefully planned single point (power supply) grounding, and the true balanced and differential input topology of the SSM-2015/2016 amplifier will eliminate unwanted external noise signals.

The network composed of R_4 and C_6 at the transformer secondary serves two functions. It minimizes transformer rising secondary winding signal amplitude with rising input frequency and deters secondary ringing, while helping to prevent amplifier input slewing. The SSM-2015/2016 differential input improves transformer performance substantially as compared with the conventional unbalanced design.

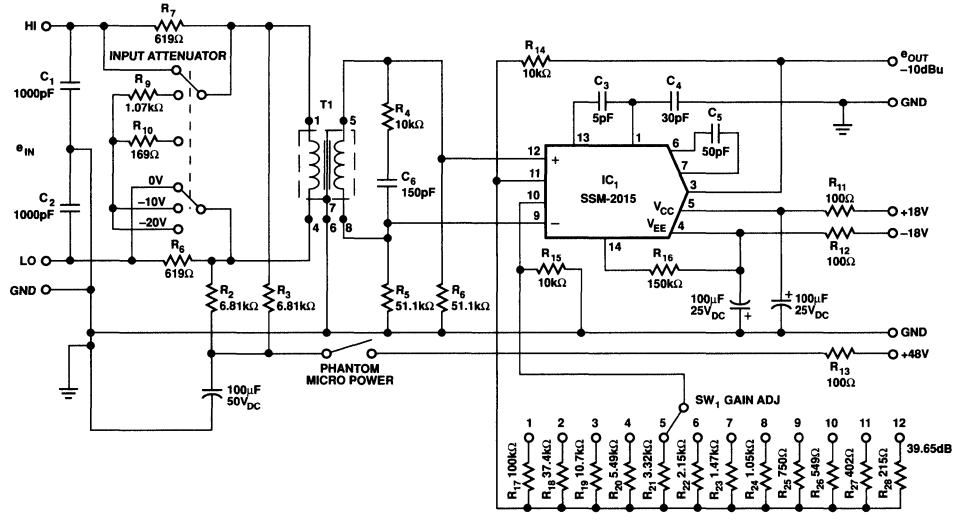

FIGURE 1

The circuit design incorporates a gain switch with twelve (12) calculated gain settings. The Jensen transformer, model JE-110K-HPC used in this application has a voltage gain of 17.9dB. For an output voltage of –10dBu, the microphone amplifier circuit has an input sensitivity range of –65dBu to –17.5dBu, with a typical output headroom of 33dB. The preamplifier circuit shown is gain adjustable from 9.6dB to 39.6dB in 2.5dB steps.

PMI's SSM-2015/2016 input circuit utilizes two identical low noise bipolar transistors, with access to the emitters, that provide the gain adjustment. The output circuit topology is complementary bipolar producing 6V/µs (2015) and 10V/µs (2016) slew rate into a 2kΩ unbalanced load.

R_G (R_{17} through R_{28}) sets the amplifier gain using the equation:

$$V_G = 3.5 + \left(\frac{20 \times 10^3}{R_G}\right)$$

for R_{14}, and R_{15} = 10.0kΩ.

SW	G_{dB}	*e_{IN}(dB)	R_G	VALUE (Ω)
1	9.6	–37.5	R_{17}	100k
2	12.1	–40.0	R_{18}	37.4k
3	14.6	–42.5	R_{19}	10.7k
4	17.1	–45.0	R_{20}	5.49k
5	19.6	–47.5	R_{21}	3.32k
6	22.1	–50.0	R_{22}	2.15k
7	24.6	–52.5	R_{23}	1.47k
8	27.1	–55.0	R_{24}	1.05k
9	29.6	–57.5	R_{25}	750
10	32.1	–60.0	R_{26}	549
11	34.6	–62.5	R_{27}	402
12	39.6	–65.0	R_{28}	215

*Input attenuator set to the 0dB position.

Unspecified overall circuit gain can be calculated from the equation:

$$G_{dB} = 20 \log\left[3.5 + \left(\frac{20 \times 10^3}{R_G}\right)\right] + 17.9$$

TYPICAL PERFORMANCE

Frequency response versus amplitude is ±0.2dB from 20 to 20,000Hz, and THD + noise is better than 0.03% over gain and frequency range described, with a typical EIN (Equivalent Input Noise) of –127dBu. See Table 1 for detailed performance specifications.

For applications where additional headroom is required, the SSM-2016 should be used. The SSM-2016 can be powered with up to ±36V_{DC} rails and drive 600Ω loads. If ±24V_{DC} rails are used, headroom increases to 35.7dB (typically), while the EIN remains at –127dB. As a consequence of the increased power supply voltage, the SSM-2016 package power dissipation will typically be 600mW with ±24V_{DC} rails (no signal), and will rise to 725mW with worst case signal conditions into 600Ω load.

For ±36V_{DC} power rails, although the headroom increases to 39.3dB, the SSM-2016 will dissipate 1.2 watts with no signal applied, and 1.5 watts worst case signal conditions into 600Ω load. Therefore, IC package cooling should be taken into consideration. Please see the SSM-2016 data sheet for IC pin-out connections and recommended compensation capacitor values. All other circuit component values shown here apply.

The transformer-coupled microphone preamplifier circuit described above demonstrates robust, real-world usage refinements, along with most operational features required by equipment designers to deliver the highest performance. It will handle the most hostile microphone environments without distress to either the circuit or the user.

TABLE 1: Circuit Performance Specifications

Frequency Response (20Hz to 20kHz, –60dBu, 50dB gain)	±0.15dB
THD + Noise (20Hz to 20kHz, –60dBu, 50db gain)	0.045%
IMD (+23dBu, SMPTE 60Hz and 4kHz, 4:1)	0.05%
EIN (Equivalent Input Noise, 150Ω source)	–127dB
Input Impedance (20Hz to 5kHz)	1500Ω
Source Impedance	150Ω
CMR at 1kHz (common-mode rejection at 1kHz)	120dB
CMVR (common-mode voltage range)	±150V_{DC}
Slew Rate (overall circuit)	6V/µs
Gain Range (overall circuit)	17.5dB to 36dB
Output Voltage	
SSM-2015 (±18V_{DC}, 2kΩ load)	+23dBu or 11V_{RMS}
SSM-2016 (±24V_{DC}, 2kΩ load)	+25.7dBu or 15V_{RMS}
Output Headroom (SSM-2015, 2kΩ load, –10dBu nominal)	33dB

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Balanced Low Noise Microphone Preamplifier Design

The SSM-2015 differential amplifier is utilized in a transformerless, active-balanced input amplifier. The circuit shown in Figure 1 provides a microphone preamplifier design with excellent performance and low noise. The design features a transformerless preamplifier circuit with true-balanced input, 1500Ω input loading, phantom microphone powering, and high common-mode rejection. The design shown also includes a twelve position gain selector, or for fixed gain usage, component value calculations.

The design includes microphone input loading of 1500Ω, but the load resistor can be changed to accommodate other applications. Input loading is capacitive reactive at higher frequencies to attenuate unwanted RF and ultrasonic voltages at the input terminals.

The phantom microphone powering circuit provides power for condenser microphones that require 24 to 48 volts DC. The zener diodes CR_1, CR_2, CR_3, and CR_4 protect the input transistors of the SSM-2015 when connecting the microphone to the preamplifier circuit.

The common-mode voltage range is ±5.5 volts. Its common-mode rejection is optimized for most applications by the true-balanced and differential input topology of the SSM-2015. A balanced single pole low-pass filter at the input terminals provides protection for the circuit from radio frequency interference and prevents slewing of the SSM-2015 amplifier. The output circuit topology is complementary bipolar producing 6V/μs slew rate, and able to drive a 2kΩ unbalanced load.

The circuit design incorporates a gain switch with twelve (12) calculated gain settings. For an output voltage of –10dBu, the microphone amplifier circuit has an input sensitivity range of –65dBu to –27.5dBu, and an output headroom of 33dB. The overall circuit gain is adjustable from 27.5dB to 55dB in 2.5dB steps.

SW	G_{dB}	e_{IN}(dB)	R_G	VALUE (Ω)
1	27.5	–37.5	R_{15}	1.00k
2	30	–40	R_{16}	715
3	32.5	–42.5	R_{17}	511
4	35	–45	R_{18}	374
5	37.5	–47.5	R_{19}	280
6	40	–50	R_{20}	205
7	42.5	–52.5	R_{21}	154
8	45	–55	R_{22}	115
9	47.5	–57.5	R_{23}	86.6
10	50	–60	R_{24}	63.4
11	52.5	–62.5	R_{25}	47.5
12	55	–65	R_{26}	35.7

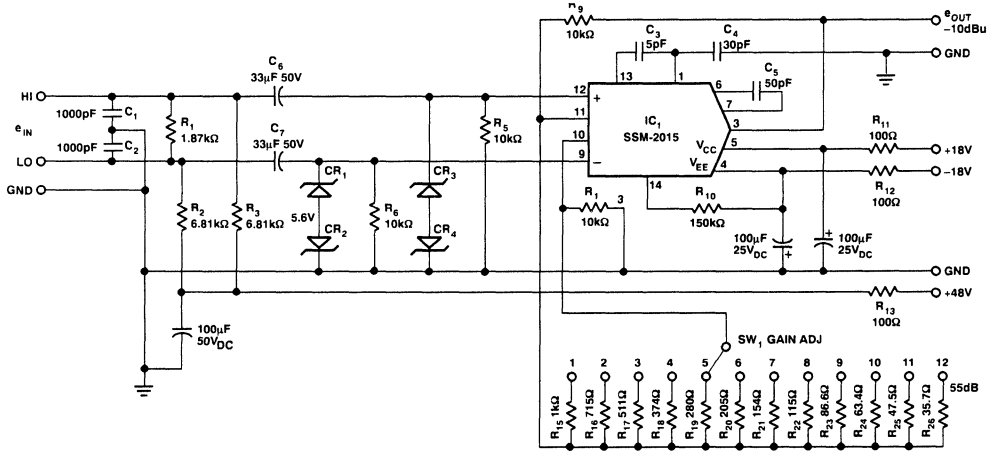

FIGURE 1

SSM-2015 input circuitry utilizes two identical low noise bipolar transistors, with access to the emitters that provide the gain adjustment. R_G (R_{15} through R_{26}) sets the amplifier's gain using the equation:

$$\text{Gain} = 3.5 + \left(\frac{20 \times 10^3}{R_G}\right) \quad \text{for } R_9, \& R_{13} = 10.0k\Omega$$

Unspecified gain can be calculated from the equation:

$$\text{Gain}_{dB} = 20 \log \left[3.5 + \left(\frac{20 \times 10^3}{R_G}\right)\right]$$

The frequency response amplitude is ±0.1dB from 20 to 20,000Hz, and THD + noise of better than 0.03% over the gain range described with a typical EIN (Equivalent Input Noise) of –124dBu.

The transformerless microphone preamplifier circuit described above demonstrates real-world usage refinements and includes most operational features required by equipment designers.

TABLE 1: Circuit Performance Specifications

Frequency Response (20Hz to 20kHz)		±0.1dB
THD + Noise (@ +23dBu, 20Hz to 20kHz)		0.03%
IMD (@ +23dBu, SMPTE 60Hz & 4kHz, 4:1)		0.05%
EIN (Equivalent Input Noise, 150Ω source)		–124dB
CMR (Common-Mode Rejection at 1kHz)		105dB
Slew Rate		6V/µs
Output Voltage (2kΩ load)	+23dBu or	$11V_{RMS}$
Output Headroom (2kΩ load, –10dBu nominal)		33dB

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AGC Amplifier Design with Adjustable Attack and Release Control

The automatic gain control (AGC) amplifier described below and shown in Figure 1, features selectable gain reduction compression ratios and time domain adjustable AGC attack and release. This design employs the SSM-2013 VCA , SSM-2110 precision level detector, two SSM-2134 low noise op amps, and an OP-215 FET input dual op amp.

The design features an inverting or noninverting input buffer amplifier, a voltage controlled amplifier with adjustable attack and recovery characteristics, driven by a true RMS level detector. Additionally, it provides selectable gain reduction compression, adjustable AGC output level, and maximum gain limit controls. Signal-to-noise ratio is better than 100dB and the RMS level detector allows the AGC amplifier to operate transparently throughout the audio spectrum. The gain recovery is linear and time adjustable, and has maximum gain limiting (gating) to preclude input source noise floor rise.

The input circuit includes a line level (–10dBu to 0dBu) buffer amplifier, that accepts inverting or noninverting inputs with greater than 10kΩ loading impedance. The buffer also isolates the input source from the compressor gain reduction ratio selector, and limits step function slewing voltage.

The six-position gain reduction selector that follows the input amplifier provides adjustable compression that smoothes the AGC action. Six GAIN REDUCTION slope ratios of 2 to 22 can be selected, thus reducing the irritating *"hole producing and pumping"* character of most AGC circuits. The SSM-2013 VCA is chosen for its predictable behavior and its high performance. The dynamic range exceeds 94dB over the frequency range 20Hz to 20kHz. Over this frequency range, the amplifier achieves typically less than 0.01% THD + noise, and 0.03% IMD.

The SSM-2110's precision rectifier circuit produces the true RMS output that comprises a level detector. It results in a consistent and precise AGC action that retains good signal dynamics while leveling the input signal. It responds to the audio signal power density in a manner similar to human hearing.

Following the precision RMS rectifier is the VCA control voltage conditioning circuits. Constructed around U_6 (OP-215), the FET-input amplifier forms an integrator while the other amplifier provides the VCA control port buffer. The AGC output level is set by the rectified signal voltage compared to the reference voltage from the OUTPUT LEVEL control.

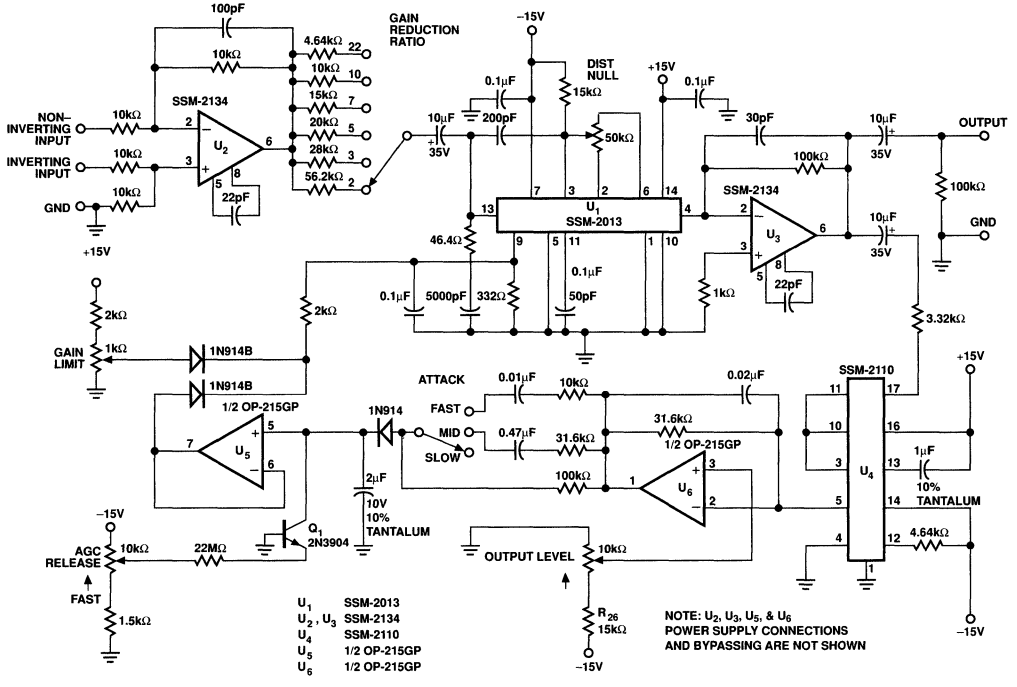

FIGURE 1

The AGC attack and compression response is altered by adjusting the integrator charging time constant or integrator wave shape current. The three-position ATTACK switch allows selection of fast, medium, and slow compression and AGC response. When the slow position is selected, an insignificant amount of compression will take place, while fast and medium combine compression with the AGC action. The AGC release rate is controlled by a constant current discharge of the integrator capacitor. The recovery time constant is linear and adjusted by changing the integrator discharge current supplied by Q_1 and regulated by the RELEASE rate control.

The SSM-2134 has been selected for its low noise and high performance characteristics. The AGC circuit described is of the feedback class, that is, the level detecting rectifier follows the voltage controlled amplifier stage. This class of AGC circuit combined with the complementary gain reduction compression, driven by RMS level detection, and adjustable attack and release AGC action, allows this circuit to be as unobtrusive or as conspicuous as desired.

The flexibility and high performance of this design, along with the simplicity and cost effectiveness, allows this design to be suitable for incorporating in mixing console designs, or in stand-alone products.

TABLE 1: Circuit Performance Specifications

Input Voltage Range (Nominal for 0dBu Out)	–26dBu to +10dBu (6mV to 2.45V_{RMS})
Rectifier Type	RMS
AGC Amplifier Class	Feedback
Attack Time	20 to 200ms
Recovery Time (6dB)	3 to 32 SEC
VCA Feedthrough (Trimmed)	–100dB
Gain Limit Range (Gain Reduction 22)	–26dBu to –12dBu
Frequency Response (20Hz to 20kHz)	±0.2dB
S/N Ratio (@ ±10dB Gain)	106dB
THD + Noise (@ +23dBu, 20Hz to 20kHz)	0.01%
IMD (@ + 23dBu, SMPTE 60Hz & 4kHz, 4:1)	0.02%
Output Voltage Slew Rate	6V/µs
Output Voltage (2kΩ Load)	+22dBu or 10V_{RMS}

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High Performance Stereo Routing Switcher

The SSM-2402 Dual Audio Switch comprises the nucleus for this 16 channels-to-one high performance stereo audio routing switcher, which features negligible noise and low distortion over the frequency range of 20Hz to 20kHz. This performance is achieved even while driving 600Ω loads at signal levels up to +30dBu.

The SSM-2402 affords a much simplified electrical design and printed circuit board layout, along with reduced manufacturing cost, when compared with discrete JFET circuits of similar performance. The electrical performance of the design described is vastly superior to CMOS switch designs, which are more prone to failure resulting from electrical static discharge.

The switching control of the SSM-2402 may be activated by conventional mechanical switches or 5 volt TTL or CMOS logic circuits. The application shown utilizes a simple mechanical control switch for illustration purposes only. Many diverse X/Y control schemes, destination control, or computer controlled designs can be utilized.

The "T" configuration of the SSM-2402 switch provides excellent ON-OFF isolation. The SSM-2402 also features 7ms ramped turn on and 4ms ramped turn off for click-free switching. Additionally, the switch has a break-before-make switching sequence. Both features become significant in large audio switching systems where the audio path can pass through multiple switching elements. Such controlled switching is very important in large systems used in broadcast program switching or in production work.

The application circuit design also employs the SSM-2015 balanced input amplifier (Figure 1). The input impedance is high (≈100kΩ), balanced or unbalanced. The input circuit incorporates a single pole RFI filter with a cutoff frequency set at 145kHz. In addition, the input circuit attenuates the signal by 25dB and extends the common-mode input voltage range to ±98 volts peak, with common-mode rejection greater than 70dB from 20Hz to 20kHz. The SSM-2015 is set to produce a 15dB gain. The signal drive level into the SSM-2402 switch is then

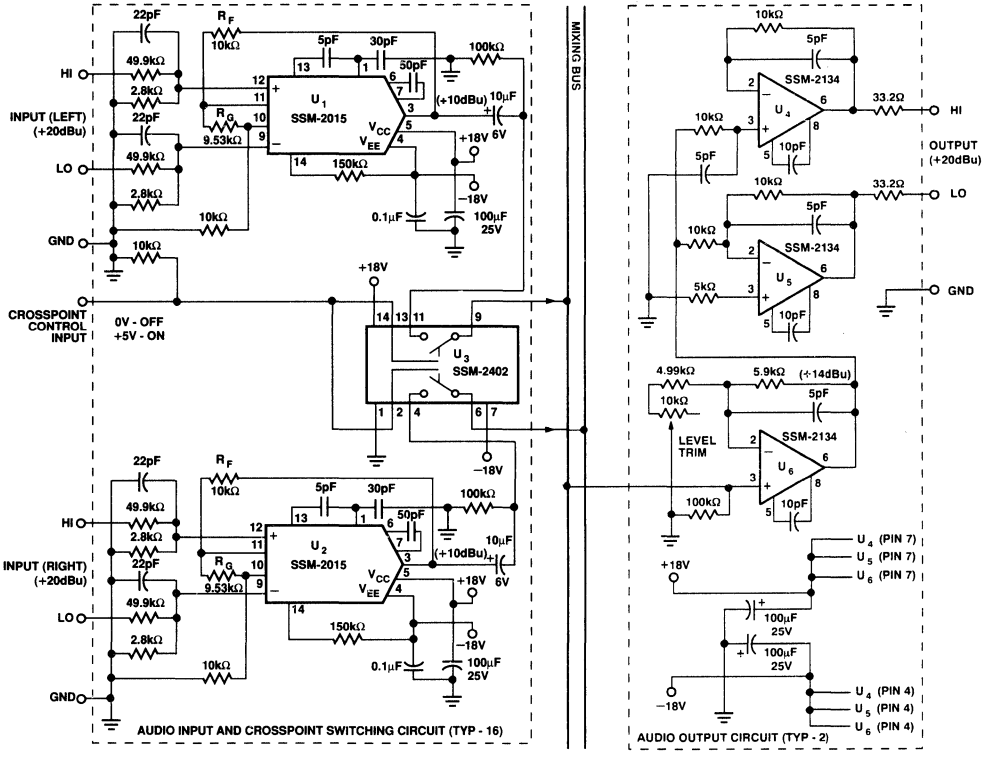

FIGURE 1: *Switcher Schematic*

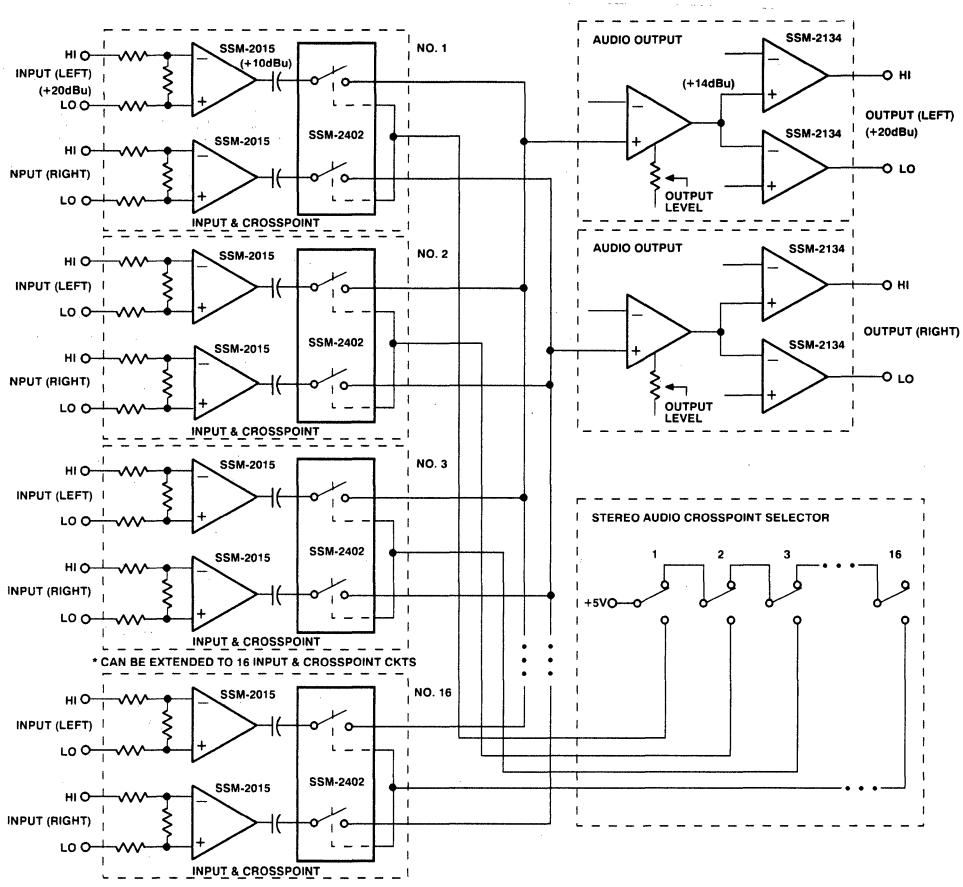

FIGURE 2: *Switcher Functional Block Diagram*

+10dBu with a +20dBu input level and +14dBu peak, well within ideal operating range. Good signal-to-noise is maintained, with generous head-room available by electing to use ±18VDC power supply voltages.

The routing switcher bus carries high level unbalanced audio, but is driven with low impedance sources. With the output impedance of the SSM-2015 at virtually 0Ω and the SSM-2402 switch ON, resistance is typically 60Ω. Bus-to-bus crosstalk is exceptionally low. For example, assuming 14pF coupling between buses and 20kHz signal, the crosstalk (isolation) exceeds 80dB. The 14pF would be representative for the 16 X 1 stereo design shown. Shielding of the buses with a printed circuit board ground plane and physically isolating the input and output circuits will reduce the crosstalk even further. The "T" configuration of the SSM-2402 switch virtually eliminates crosstalk between the various input signal sources.

The output amplifier incorporates a buffer amplifier that provides 4dB of gain (nominally), with adjustable output level trim control. The buffer also isolates the switching bus from the balanced output amplifier circuit. The balanced output is designed to drive 600Ω loads and utilizes two SSM-2134 IC amplifiers. The differential design increases drive capability, yet increases the heat dissipation surface area, and keeps IC package temperature well within safe operating limits, even when driving 600Ω loads. The SSM-2134 is recommended due to its low noise, wide frequency response, and output drive current capabilities.

Overall performance of the 16 X 1 stereo switcher is noteworthy. Input-to-output frequency response is flat to within 1dB over a 10Hz to 50kHz band. Total harmonic distortion plus noise is less than 0.03%, from 20Hz to 20kHz. SMPTE intermodulation distortion is less than 0.02%. The use of ±18VDC power supplies produces a +30dBm clip level, even when driving 600Ω loads.

TABLE 1: Circuit Performance Specifications

Max Input Level	+30dBu
Input Impedance, Unbalanced	100kΩ
Input Impedance, Balanced	200kΩ
Common-Mode Rejection (20Hz to 20kHz)	>70dB
Common-Mode Voltage Limit	±98V Peak
Max Output Level	+30dBu/dBm
Output Impedance	67Ω
Gain Control Range	±2dB
Output Voltage Slew Rate	6V/μs
Frequency Response (±0.05dB)	20Hz to 20kHz
Frequency Response (±0.5dB)	10Hz to 50kHz
THD + Noise (20Hz to 20kHz, +8dBu)	0.005%
THD + Noise (20Hz to 20kHz, +24dBu)	0.03%
IMD (SMPTE 60Hz & 4kHz, 4:1, +24dBu)	0.02%
Crosstalk (20Hz to 20kHz)	>80dB
S/N Ratio @ 0dB Gain	135dB

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A Balanced Mute Circuit for Audio Mixing Consoles

The SSM-2402 Dual Audio Switch enhances the performance and simplifies the design of balanced high level switching (Mute) circuits used in audio mixing consoles. The use of the SSM-2402 and SSM-2134 creates a design that has negligible transient noise (as a result of signal switching), and exceptionally low signal distortion over a wide dynamic range. The balanced high level voltage switch then drives a virtual ground summing bus through 10kΩ resistors. Also included is a design for a virtual ground summing amplifier.

The SSM-2402 is a monolithic dual audio switch that improves electrical performance and eases printed circuit board layout design. The design reduces manufacturing cost when compared with discrete JFET designs of similar performance. Electrical performance is measurably superior to CMOS switch designs, and will be less prone to failure from electrical static discharge.

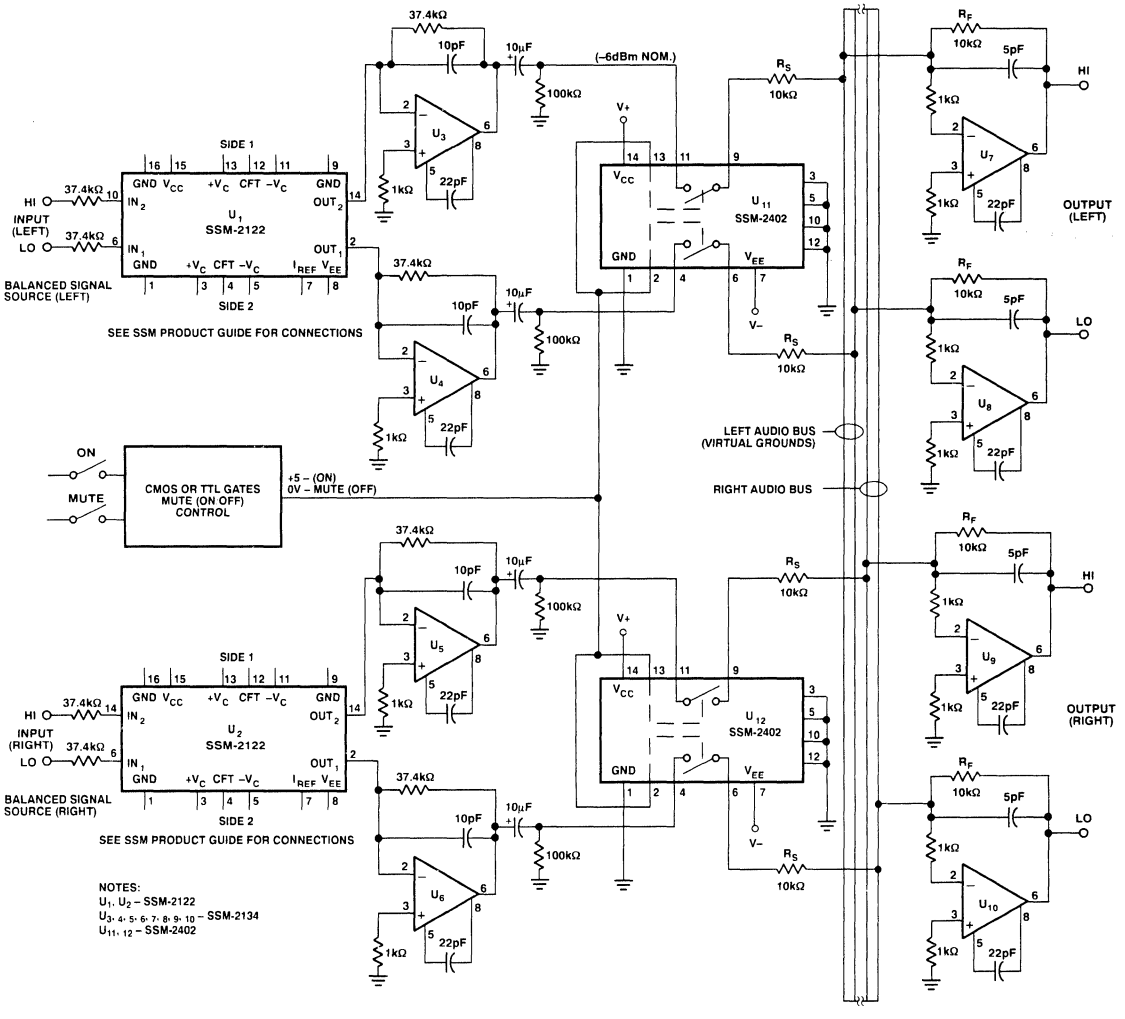

FIGURE 1: *Audio Mixer Channel Mute (On/Off) Circuit, a Balanced Design with High Level Bus Switching*

The "T" switch configuration of the SSM-2402 provides excellent ON-OFF isolation. The design shown further improves the ON-OFF isolation and left/right channel crosstalk figures by maintaining the common-mode rejection ratio of a fully balanced design. The switch features a 7ms ramped turn-on and 4ms ramped turn-off, and guaranteed break-before-make switching sequence for transient-free audio switching. The system performance is improved for large audio consoles that have multiple switches in the audio signal path.

The switch control ports are easily interfaced to conventional $5V_{DC}$ TTL or CMOS digital control circuits, further simplifying the control circuit design. Furthermore, product reliability and serviceability are improved by the simplified design. The application shown uses an elementary control circuit to functionally illustrate control voltage requirements. Customized logic gate control schemes or computer-controlled designs can be easily implemented.

The application circuit design employs dual audio switches driven by U_3, U_4, U_5 and U_6 inverting amplifiers. Their gain is controlled by two dual voltage controlled amplifier (VCA) elements U_1 and U_2. A simplified signal path is shown for application clarity. For additional design information of the SSM-2122 dual VCA, consult the data sheet.

The design shown in Figure 1 is signal phase noninverting, and incorporates a minimum number of components to minimize noise. The input signal source should be balanced to maximize separation and crosstalk isolation. PCB layout should also utilize equal inductance in each side of the signal path wiring, and include equal stray capacitance to ground and other signal paths to obtain maximum performance. The SSM-2122 VCA provides good gain tracking of the two audio channels, while maintaining accuracy in the balanced signal path.

U_{11} and U_{12} are utilized as high level switches so that other post-switching functions can be employed. A nominal drive level of 0dBu balanced (–6dBu unbalanced) is applied to the switch. This level is arbitrary, but will satisfy most signal-to-noise and headroom compromises. The output of amplifiers U_3, U_4, U_5, and U_6 are AC coupled prior to the switches to further minimize the switching transients caused by active component offset voltages. The balanced virtual ground mixing buses are current driven by R_S of 10kΩ. This value can affect overall system performance, and should be modified to suit the size of the mixing bus system. A greater number of input mixing channels will warrant lower bus drive current. Although the individual values of R_S and R_F can be altered, their values must be the same for a summing amplifier voltage gain of one (1).

TABLE 1: Circuit Performance Specifications

Max Input Level	+30dBu
Input Impedence, Balanced	75kΩ
Common-Mode Rejection (20Hz to 20kHz)	>70dB
Common-Mode Voltage Limit	±12V Peak
Max Output Level	+30dBu
Output Voltage Slew Rate	12V/µs
Frequency Response (±0.05dBu)	20Hz to 20kHz
Frequency Response (±0.5dBu)	10Hz to 50kHz
THD + Noise (20Hz to 20kHz, +8dBu)	0.005%
THD + Noise (20Hz to 20kHz, +24dBu)	0.03%
IMD (SMPTE 60Hz & 4kHz, 4:1, +24dBu)	0.02%
ON/MUTE Isolation (20Hz to 20kHz)	>85dB
S/N Ratio @ 0dB Gain	135dB

The active switches' ON resistances are typically 60Ω and are well matched. One should use 1% or better tolerance series resistor R_S (10kΩ) to minimize imbalance in the signal path. In the OFF state, the "T" configuration of the switch virtually eliminates leakage of the input source signal into the mixing bus(es). Greater than 100dB mute isolation at 1kHz can be obtained with prudent printed circuit board design since the SSM-2402 control inputs and switch terminals are separated by ground guards.

The use of $\pm 18V_{DC}$ power supplies allows a +30dBu (balanced) clipping level. All integrated circuit components mentioned will operate reliably at $\pm 18V_{DC}$, and noise contribution will be indiscernible, even in large mixing systems. The balanced input to balanced output frequency response is typically greater than 10Hz to 50kHz, within 1dB. Total harmonic distortion plus noise will measure less than 0.01%, from 20Hz to 20kHz at +30dBu, with SMPTE intermodulation distortion less than 0.02% under the same measurement conditions.

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A Constant Power "Pan" Control Circuit for Microphone Audio Mixing

The SSM-2134 permits the design of a constant power, transient-free "PAN" control circuit suitable for installation in the highest performance audio mixing consoles. The design incorporates unique and vital features. The PAN IN/OUT switch does not introduce transient type noise or interruptions in the audio when activated or deactivited, and when panning, an accurate constant power output is maintained between the sum of the two channels. The design allows "punching-in" and "punching-out" of the PAN circuit while mixing down or on-the-air, without transient clicks or holes in the mix.

The design utilizes conventional parts, e.g., a single SPST switch and a linear 10kΩ potentiometer. U_1 (SSM-2134) is used as a unity gain, inverting buffer with an input impedance of 37.4kΩ. The input source could be a VCA element or audio direct from the fader control. The values shown will allow a VCA, for example, the SSM-2013, to be used with only minor additions. The overall application circuit is noninverting from input to output.

The 15kΩ series input resistors R_S, plus the inverting input 15kΩ R_I in parallel with 5kΩ (1/2 of 10kΩ, with the PAN control in the center) forms an attenuator that has a 14dB loss. Rotating the PAN control in either direction decreases the attenuation to −11dB for one channel and maximum attenuation for the other.

$$\frac{1}{R_L} = \frac{1}{R_I} + \frac{1}{5k\Omega}, \qquad R_L = 3.75k\Omega$$

Attenuation is calculated as:

$$dB_{LOSS} = 20 \log \frac{R_L}{R_L + R_S} = 20 \log \frac{3.75k\Omega}{3.75k\Omega + 15k\Omega} = -14dB$$

Amplifier (U_2 & U_3) gain is:

$$dB_{GAIN} = 20 \log \frac{R_F}{R_I} = 20 \log \frac{75k\Omega}{15k\Omega} = +14dB$$

The frequency response is typically 10Hz to 50kHz, within 0.5dB. Total harmonic distortion plus noise will measure less than 0.007% from 20Hz to 20kHz, and SMPTE intermodulation distortion less than 0.01%. The amplifier clipping level is +24dBu with $\pm 18V_{DC}$ power supply rails. Headroom is nominally 30dB, and 27dB at full PAN for the operating channel.

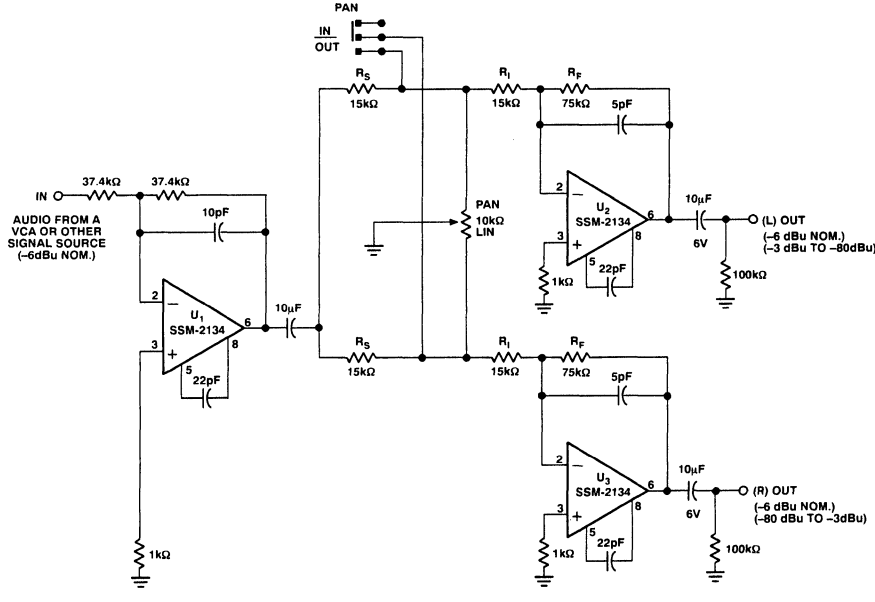

FIGURE 1: *Constant Power Type Control Circuit with Transient Free IN/OUT Switching*

TABLE 1: Circuit Performance Specifications

PAN Range, L ← C → R (L Out)	+3dB ← 0dB → –80dB
PAN Range, R ← C → L (R Out)	+3dB ← 0dB → –80dB
Max Input Level	+24dBu
Input Impedance, Balanced	37.4kΩ
Max Output Level (> 600Ω ±18V_{DC} PS)	+24dBu
Headroom	30dB
Output Voltage Slew Rate	<6V/μs
Frequency Response (±0.05dB)	20 Hz to 20kHz
Frequency Response (±0.5dB)	10 Hz to 50kHz
THD + Noise (20Hz to 20kHz, +8dBu)	0.005%
THD + Noise (20Hz to 20kHz, +24dBu)	0.03%
IMD (SMPTE 60Hz & 4kHz, 4:1, +24dBu)	0.02%
S/N Ratio	130dB

ANALOG DEVICES

AN-124
APPLICATION NOTE

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Three High Accuracy RIAA/IEC MC and MM Phono Preamplifiers

Although the digital compact disk is rapidly supplanting the vinyl disk as the popular media method for professional and consumer audio entertainment, the electro-mechanical recording and reproduction of audio signals has many more years of life. The group of phono preamplifier application designs below will make the future years with vinyl more productive and pleasant. The applications employ solid engineering concepts, and dismiss "golden ear" discussions.

One design includes an input scheme for both moving coil (MC) and moving magnet (MM) – or variable reluctance – transducers. All designs employ extremely low noise circuit topologies, high accuracy active and passive RIAA (Recording Industries Association of America) equalization with selectable old RIAA or RIAA/IEC (International Electro-Technical Commission) curves. The applications incorporate both consumer and balanced output circuit configurations.

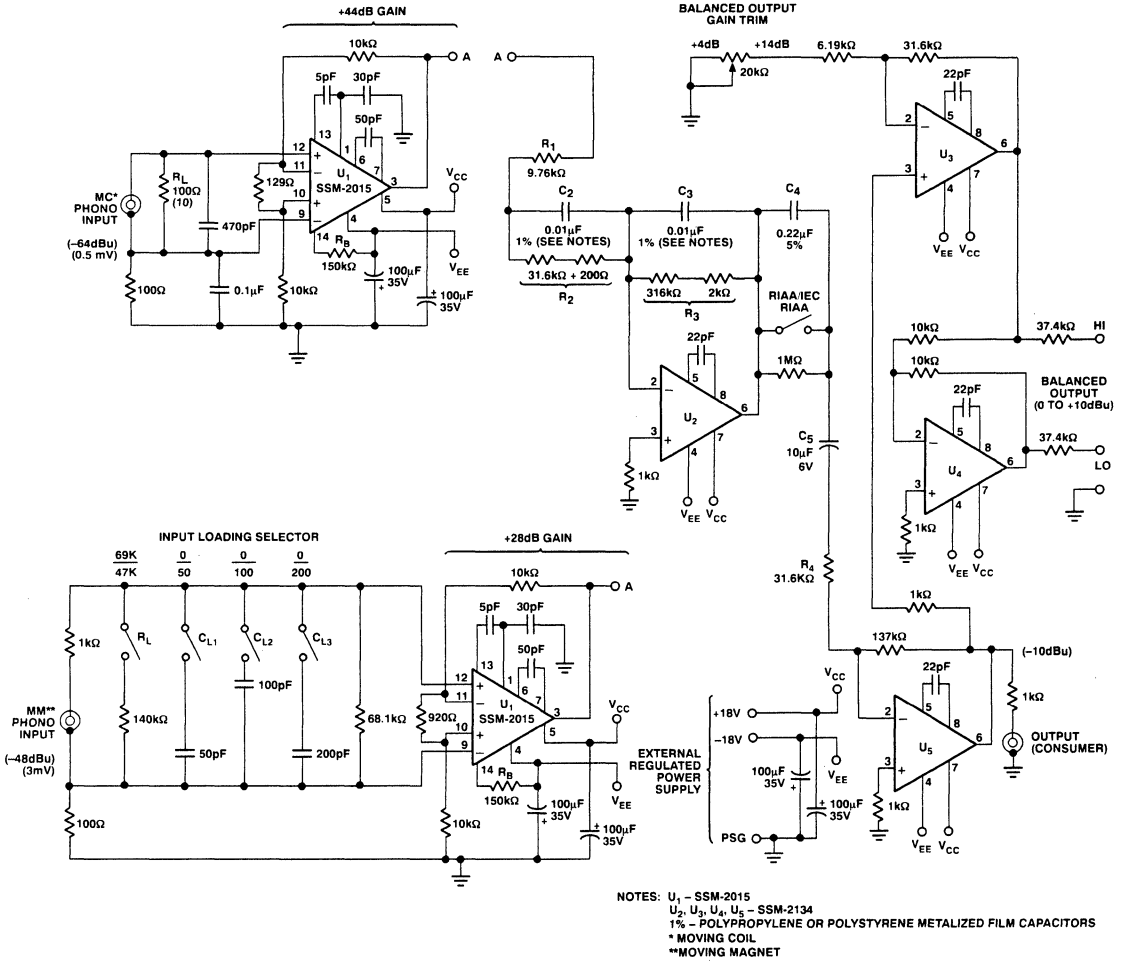

FIGURE 1: *High Accuracy RIAA/IEC MC or MM Phono Preamplifier*

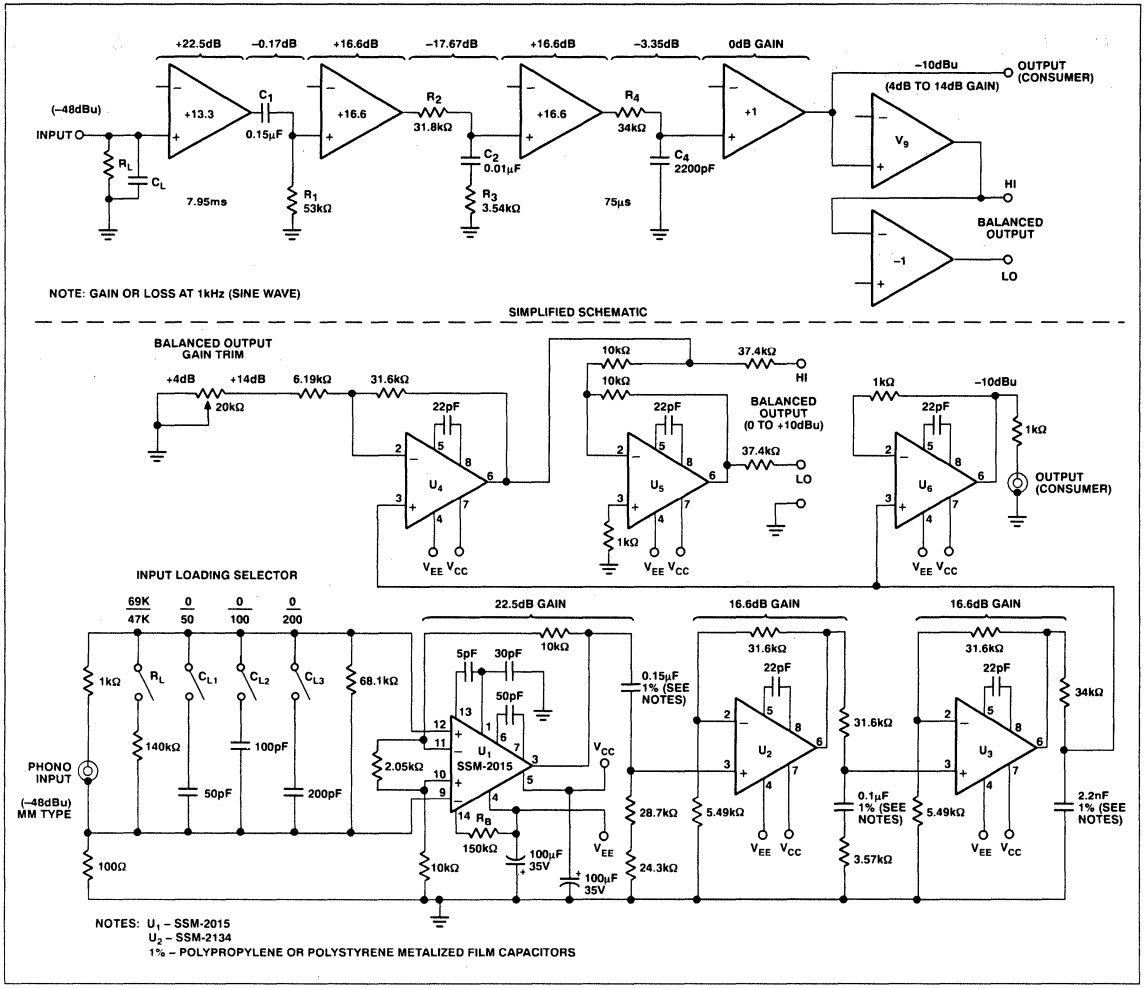

FIGURE 2: *Passive (Multi-Filter) RIAA/IEC Equalized Phono Preamplifier*

A HIGH ACCURACY DESIGN

In the High Accuracy RIAA/IEC Phono Preamplifier shown in Figure 1, both MC and MM transducer input configurations are presented. Both utilize the PMI SSM-2015 differential amplifier and take advantage of the high common-mode rejection it provides. The overall circuit structure *does not* incorporate any design compromises. It provides the lowest possible noise, adjustable MM input loading, highest accuracy RIAA filtering, and is completely devoid of transient and frequency dependent gain errors. The wide bandwidth stages minimize in-band phase shift, and provide exceptional phase and frequency response accuracy. This allows the RIAA/IEC filter to render the exact reciprocal of the recorded phase and frequency characteristics.

Referring to Figure 1, the MC input circuit has input loading (R_L) set at 100Ω. (Note: some MC transducers require 10Ω loading for maximum reproduction accuracy. For these, replace R_L with a 10Ω metal film resistor.) The input circuit gain is 44dB, and provides a −20dBu signal level at point A. 44dB gain should be adequate for most MC cartridges available. If U_1 gain requires adjusting, use the equation:

$$G_{dB} = 20 \log\left(3.5 + \frac{20 \times 10^3}{R_G}\right)$$

R_B sets the U_1 bias value and contributes to symmetrical amplifier slewing. The RIAA filter stage that follows U_1 stage(s) all but eliminates noise produced by the input amplifier.

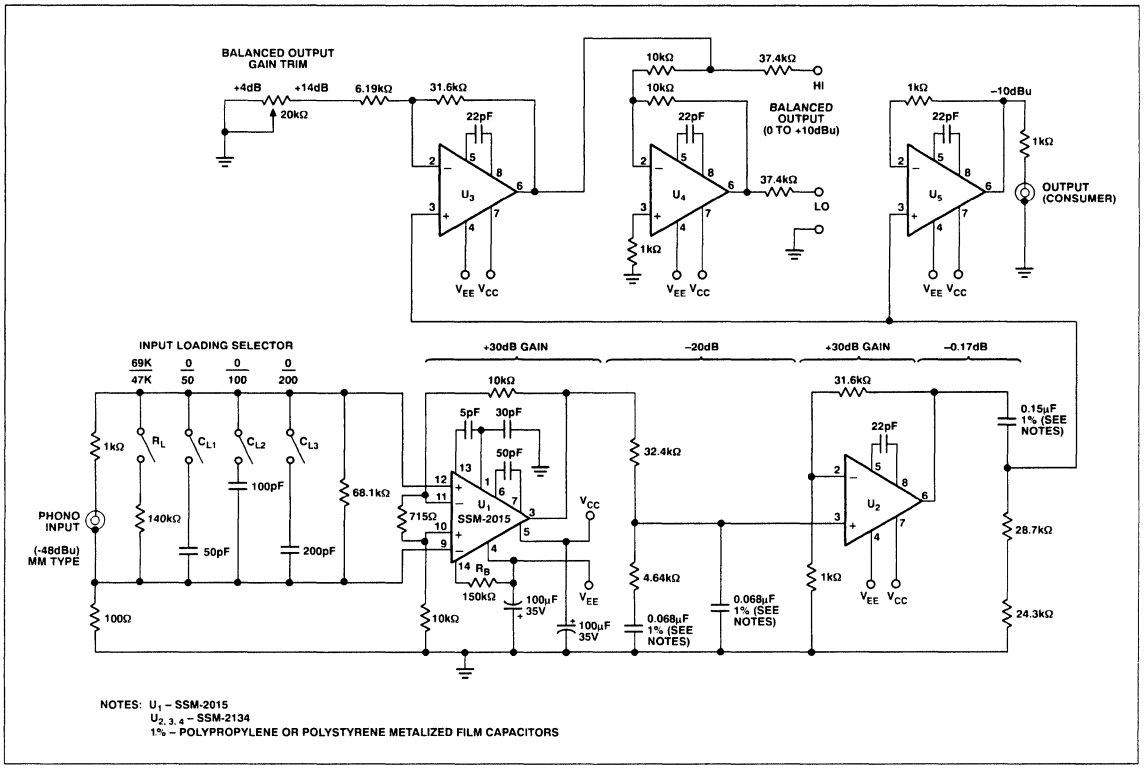

FIGURE 3: *Passive RIAA/IEC Equalized Phono Preamplifier*

The next stage contains the RIAA-RIAA/IEC equalization filter and is built around U_2, the SSM-2134 operational amplifier, and is an active feedback type filter. The overall gain of this circuit at 1,000Hz is –2.5dB. RIAA equalization requires a gain of 19.3dB at 20Hz, and attenuation of 19.6dB at 20,000Hz. The open-loop gain of U_2 is greater than 100dB at 20Hz, and 60dB at 20,000Hz, ensuring exceptional equalization accuracy.

Three filters make up the RIAA reproduction curve. The time constants are: 75µs, 318µs, and 3180µs, and a fourth time constant in the RIAA/IEC curve is 7960µs. The IEC filter was introduced to minimize warp and infrasonic signal interference while maintaining flat frequency response down to 40Hz.

- The 75µs filter is formed by resistors R_1 (9.76kΩ) and R_2 (31.8kΩ) in parallel with capacitor C_2 (0.01µF).
- The 318µs pre-emphasis filter is formed by R_2 (31.8kΩ) and C_2 (0.01µF).
- The 3180µs filter is formed by R_3 (318kΩ) and C_3 (0.01µF).
- The fourth pole, IEC 7960µs, a high pass filter is formed by R_4 (31.6kΩ) and C_4 (0.22µF), and provides 3dB attenuation at 20Hz rolling off at –6dB/octave thereafter.

Table 1 contains the complete RIAA and RIAA/IEC reproduction equalization characteristics. RIAA/IEC switching allows selection of either reproduction response curves. For the "audio purist," C_5 can be eliminated for a direct coupled design, thus reducing envelope and group delay distortions. All amplifier feedback circuits are direct coupled, and are referenced to circuit ground. The closed-loop gain is kept low to minimize input offset voltage. Therefore, only very small DC voltages can be expected at the output of the directly coupled version.

The high level amplifier, U_5, provides +12.7dB gain and feeds the unbalanced Consumer Output jack, with a nominal –10dBu level. U_5 is followed by balanced output buffer amplifier. The nominal output level is continuously adjustable from 0.0dBm to +10dBm at the balanced output terminals. The output source impedance is 75Ω, and will drive 600Ω loads to a maximum +30dBm clip point level. Table 2 shows circuit performance specifications.

TABLE 1: RIAA/IEC and RIAA Playback Characteristics

Frequency (Hz)	RIAA /IEC Relative Level (dB)	RIAA Relative Level (dB)
2.0	–0.2	
2.5	+1.8	
3.15	+3.7	
4.0	+5.7	
5.0	+7.6	
6.3	+9.4	
8.0	+11.2	
10.0	+12.8	
12.5	+14.1	
16.0	+15.4	
20.0	+16.3	+19.3
25.0	+16.8	+19.0
31.5	+17.0	+18.5
40.0	+16.8	+17.8
50.0	+16.3	+16.9
63.0	+15.4	+15.8
80.0	+14.2	+14.5
100	+12.9	+13.1
125	+11.5	+11.6
160	+9.7	+9.8
200	+8.2	+8.2
250	+6.7	+6.7
315	+5.2	+5.2
400	+3.8	+3.8
500	+2.6	+2.6
630	+0.8	+0.8
1,000	0.0	0.0
1,250	–0.8	–0.7
1,600	–1.6	–1.6
2,000	–2.6	–2.6
2,500	–3.7	–3.7
3,150	–5.0	–5.0
4,000	–6.6	–6.6
5,000	–8.2	–8.2
6,300	–10.0	–10.0
8,000	–11.9	–11.9
10,000	–13.7	–13.7
12,500	–15.6	–15.6
16,000	–17.7	–17.7
20,000	–19.6	–19.6

TABLE 2: High Accuracy Circuit Performance Specifications

MC Nominal Input Level	–64dBu (0.5mV)
MC Input Impedance	100Ω
MM Nominal Input Level	–48dBu (3.0mV)
MM Input Impedance, Resistive	69kΩ or 47kΩ
MM Input Impedance, Capacitive	50pF to 350pF
Common-Mode Rejection (20Hz to 20kHz)	>50dB
Common-Mode Voltage Limit	±10V Peak
Nominal Output Level, Balanced	+8dBu/dBm
Max Output Level, Balanced	+30dBu/dBm
Output Impedance, Balanced	70Ω
Gain Control Range, Balanced	0.0dBu to 10dBu/dBm
Nominal Output Level, Unbalanced	–10dBu
Max Output Level, Unbalanced	+24dBu
Output Impedance, Unbalanced	1,000Ω
Output Voltage Slew Rate	>6V/ µs
RIAA Reproduction Characteristics (20Hz to 20kHz)	±0.25dB
RIAA/IEC Reproduction Characteristic (2Hz to 20kHz)	±1.0dB
Wideband Frequency Response (±1.0dB)	0.0Hz to 70kHz
Signal-to-Noise Ratio (20Hz to 20kHz)	>90dB
THD + Noise (20Hz to 20kHz +8dBu, Any Output)	0.01%
IMD (SMPTE 60Hz & 4kHz, 4:1)	0.02%

A PASSIVE MULTI-FILTER DESIGN

The Passive Split Multi-Filter RIAA/IEC Preamplifier design, shown in Figure 2, is intended for moving magnet (MM) input phono transducers. The design has an extremely low noise circuit topology, high accuracy passive RIAA/IEC equalization filters, and both unbalanced consumer and balanced output circuits. The input configuration utilizes the SSM-2015. It provides the lowest possible noise, adjustable resistive and capacitive input loading, and high accuracy passive RIAA filtering totally devoid of transient and frequency dependent gain errors.

Referring to Figure 2, the following two stages contain the RIAA-RIAA/IEC passive equalization filters. All high pass and low pass filters are passive. The signal is amplified by U_2 and U_3 SSM-2134 op amps. The overall gain of the circuit at 1,000Hz is 38dB. RIAA equalization requires a gain of 19.3dB at 20Hz, and attenuation of 19.6dB at 20,000Hz. Open-loop gain of U_2 and U_3 is greater than 100dB at 20Hz, and 60dB at 20,000Hz. Closed-loop gain of U_1 is 22.5dB, and U_2, U_3 is 16.6dB, ensuring an extensive gain margin for phase accuracy. Refer to Table 3 for complete circuit specifications.

TABLE 3: Passive Multi-Filter Circuit Performance Specifications

MM Nominal Input Level	–48dBu (3.0mV)
MM Input Impedance, Resistive	69kΩ or 47kΩ
MM Input Impedance, Capacitive	50pF to 350pF
Common-Mode Rejection (20Hz to 20kHz)	> 50 dB
Common-Mode Voltage Limit	±10V Peak
Max Output Level, Balanced	+30dBu/dBm
Nominal Output Level, Balanced	+8dBu/dBm
Output Impedance, Balanced	70Ω
Gain Control Range, Balanced	0.0dBu to 10dBu/dBm
Nominal Output Level, Unbalanced	–10dBu
Max Output Level, Unbalanced	+24dBm
Output Impedance, Unbalanced	1,000Ω
Output Voltage Slew Rate	>6V/μs
RIAA Reproduction Characteristic (20Hz to 20kHz)	±0.25dB
RIAA/IEC Reproduction Characteristic (2Hz to 20kHz)	±0.5dB
Wideband Frequency Response (±1.0dB)	0.0Hz to 70kHz
Signal-to-Noise Ratio (20Hz to 20kHz)	>90dB
THD + Noise (20Hz to 20kHz +8dBu, Any Output)	0.01%
IMD (SMPTE 60Hz & 4kHz, 4:1)	0.02%

TABLE 4: Uncomplicated Passive Circuit Performance Specifications

MM Nominal Input Level	–48dBu (3.0mV)
MM Input Impedance, Resistive	69kΩ or 47kΩ
MM Input Impedance, Capacitive	50pF to 350pF
Common-Mode Rejection (20Hz to 20kHz)	> 50dB
Commom-Mode Voltage Limit	±10V Peak
Max Output Level, Balanced	+30dBu/dBm
Nominal Output Level, Balanced	+8dBu/dBm
Output Impedance, Balanced	70Ω
Gain Control Range, Balanced	0.0dBu to 10dBu/dBm
Nominal Output Level, Unbalanced	–10dBu
Max Output Level, Unbalanced	+24dBu
Output Impedance, Unbalanced	1,000Ω
Output Voltage Slew Rate	>6V/μs
RIAA Reproduction Characteristic (20Hz to 20kHz)	±0.5dB
RIAA/IEC Reproduction Characteristic (2Hz to 20kHz)	±1.0dB
Wideband Frequency Response (±1.0dB)	0.0Hz to 70kHz
Signal-to-Noise Ratio (20Hz to 20kHz)	>90dB
THD + Noise (20Hz to 20kHz, +8dBu, Any Output)	0.01%
IMD (SMPTE 60Hz & 4kHz, 4:1)	0.02%

AN ECONOMICAL APPROACH

An Uncomplicated Passive RIAA/IEC Preamplifier is shown in Figure 3. It is a low cost, practical design for a passively equalized RIAA/IEC phono preamplifier. The design shown is for moving magnet (MM) input. It also is an extremely low noise input circuit design, and includes both unbalanced consumer and balanced output circuit configurations. The input circuit also utilizes the SSM-2015, and provides adjustable resistive and capacitive input loading. Wide bandwidth stages minimize in-band phase shift, and provide exceptional phase and frequency response accuracy. Table 4 details circuit performance data.

SUMMARY

For a phono transducer cartridge to deliver the performance as intended, it should be loaded with proper resistance and capacitance. The MM input circuits have adjustable transducer loading. Most transducers currently available will be accommodated with resistive loading of 69kΩ or 47kΩ, and capacitive loading of a few pF (input wiring dependent) to 350pF, in 50pF steps.

If greater input common-mode noise rejection is required, it can be obtained in all input designs by increasing the value of the 100Ω resistor and 0.1μF capacitor connected between the input RCA jack shield connection and the main circuit ground point. The values shown satisfy most requirements for 1 meter cables supplied with the newer tone arms.

All circuits described are signal noninverting, and constructed with bipolar IC amplifiers for lowest noise. They are compensated for widest bandwidth and circuit stability.

To achieve optimum trouble-free performance, a few construction and manufacturing tips should be observed. For grounding to be truly effective, all grounded components must return to a single point. This technique is effective in minimizing ground current loops that can cause excessive noise, signal cross-talk, AC power line noise, and circuit instability, and permit external noise spikes to enter. The ground center should be as close to the input amplifier (U_1) as possible. All grounded components of U_2, U_3, U_4, U_5, the output jack grounds, and the power supply ground lead should be tied to the same U_1 ground point.

As long as the power supply leads are kept short, and adequately filtered and bypassed with polyester film capacitor at the regulators, there is no need for individual decoupling capacitors at U_2, U_3, U_4, and U_5. The power supply voltages should be regulated for $\pm 18V_{DC}$.

All signal filter components should be of the highest quality, i.e., metalized polypropylene or polystyrene film, 1% tolerance capacitors (except for C_5, 5% tolerance is OK) and metal film resistors, 1% or better tolerance.

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A Two-Channel Dynamic Filter Noise Reduction System

In this application, the SSM-2120 Dynamic Range Processor and SSM-2134 op amp are utilized in a dual-channel dynamic noise reduction circuit, where the input signal level and threshold control determine the corner frequency of a low-pass filter.

The SSM-2120 contains two class A VCAs (Voltage Controlled Amplifiers) that are used as the filter's control element, and two wide dynamic range full-wave rectifiers with control amplifiers. The VCA section or variable resistor is a current device con-

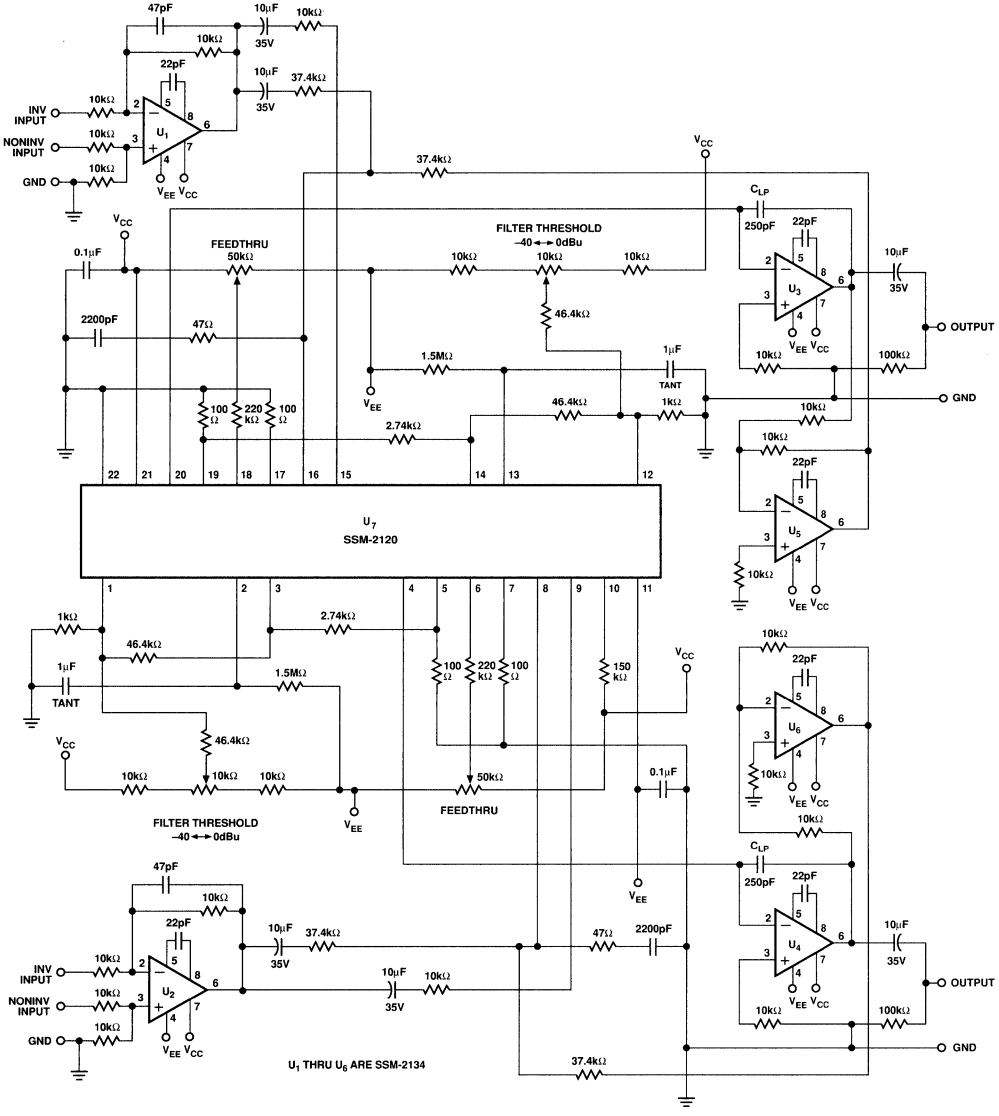

FIGURE 1: *Two-Channel Dynamic Filter Noise Reduction System*

trolled by the $+V_C$ voltage control ports. The VCAs are employed as variable resistor elements in a single-pole low-pass filter operating in a virtual ground configuration. The level detecting rectifier is a full-wave averaging type with more than 100dB dynamic range, followed by a LOG amp converter. The part also contains two operational amplifiers with PNP output transistors used to drive the $+V_C$ ports.

U_1 and U_2 (SSM-2134) are input amplifiers and source-load isolating buffers. They provide a choice of noninverting, inverting, or balanced inputs. Unbalanced loading is 10kΩ and balanced loading is 20kΩ. U_1 and U_2 gain is set at 0dB, with a –10dBu nominal input signal recommended using $\pm 18V_{DC}$ power supply rails. This configuration will provide an overall circuit headroom of more than 30dB. In less critical applications, the feedthrough trim controls and 220kΩ resistors can be eliminated.

DETAIL CIRCUIT DESCRIPTION FOR U_7 (SSM-2120), AND U_3 and U_4

The rectifier circuit is configured to provide a negative control voltage referenced to ground. The LOG amplifier's bias is set by the 1.5MΩ resistor. The 1.5MΩ resistor also provides the discharge path for the 1μF rectifier averaging capacitor. The discharge time constant controls the low-pass filter's action toward a lower corner frequency. The LOG amplifier provides a constant current charging for the 1μF averaging capacitor. It results in an attack (return to flat response) time constant T_{C0} of approximately 6ms, and a low-pass filter activation T_{C1} of 350ms.

The internal op amp of U_7 has the gain V_G set at 47. The potentiometer at the inverting input provides the adjustable threshold to activate the filter. The threshold adjustment ranges from –40dBu to 0dBu of input signal level. The output from the op amp drive transistor supplies only a negative control voltage to the VCA ($+V_C$) control port(s). For example, with the filter threshold control adjusted to 0dB and a –10dBu signal applied to the input, f_{C1} is ≈4kHz; or with –20dBu applied, f_{C2} is ≈1.2kHz, both rolling off at 6dB/Octave. With the input signal level exceeding the filter threshold setting (0V VCA control voltage present), the overall circuit frequency response is 20Hz to 16kHz, at ±1dB.

The VCA audio input current is limited by the 37.4kΩ resistor. The VCAs operate as current devices whose outputs feed the virtual ground of an amplifier loop. The feedback capacitor around the amplifier loop sets up a single-pole low-pass filter.

The SSM-2120 (U_7) inverts the signal current; therefore, U_5 and U_6 are required to invert the output signal that is summed at the input(s) of U_7.

The design is an effective single-ended noise reduction circuit with low distortion and noise. When utilized on a noisy signal source, it will attenuate high frequency noise with inconspicuous operation.

TABLE 1: Circuit Performance Specifications

Nominal Input Voltage (–10dBu Out)	–10dBu
Headroom (–10dBu Out)	+30dBu
Input Voltage Range	–20dBu to +10dBu
Input Type/Impedance, Balanced	20kΩ
Input Type/Impedance, Unbalanced	10kΩ
Dynamic Noise Reduction Class	Dynamic Low-Pass
Filter Activate Time Constant (6dB)	350ms
Threshold Range (Level)	–40dBu to 0dBu
Filter Deactivate Time Constant	6ms
Signal Rectifier Type	Full Wave Averaging
Modulation Feedthrough, Trimmed	–100dB
Frequency Response (20Hz to 16kHz)	±1dB
Filter Type, Low-Pass	Single Pole, 6dB/Oct
Input 10dB Below Threshold Setting	f_{C1} = 3,800Hz
Input 20dB Below Threshold Setting	f_{C2} = 1,400Hz
Dynamic Range	
@ 0dB Gain (Ref. +22dBu)	106dB
THD + Noise (20Hz to 20kHz)	0.02%
IMD (SMPTE 60Hz & 4kHz, 4:1)	0.05%
Output Voltage (2kΩ Load)	+22dBu
Output Type	Unbalanced
Power Supply	$\pm 18V_{DC}$ Regulated

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An Unbalanced Mute Circuit for Audio Mixing Channels

This application note describes a dual channel unbalanced analog audio mute switch, for use in audio console mute circuits. The SSM-2402 dual audio switch, when used in the virtual ground configuration, truly enhances any audio mute design. The application, as shown in Figure 1, incorporates unbalanced stereo input buffers, dual stereo electronic virtual ground switches (with simplified control circuit), and virtual ground summing amplifiers.

THE AUDIO SWITCH AS IMPLEMENTED

The design utilizes the SSM-2402 (U_1 and U_2) dual audio switch in a virtual ground switching configuration. This method of operation improves linearity over a wide dynamic range. The SSM-2402 utilizes JFET switching, with internal wide bandwidth integrated amplifiers applied in a unique configuration. The result is low transient intermodulation distortion, low THD, and low IMD, while essentially eliminating all audio switching

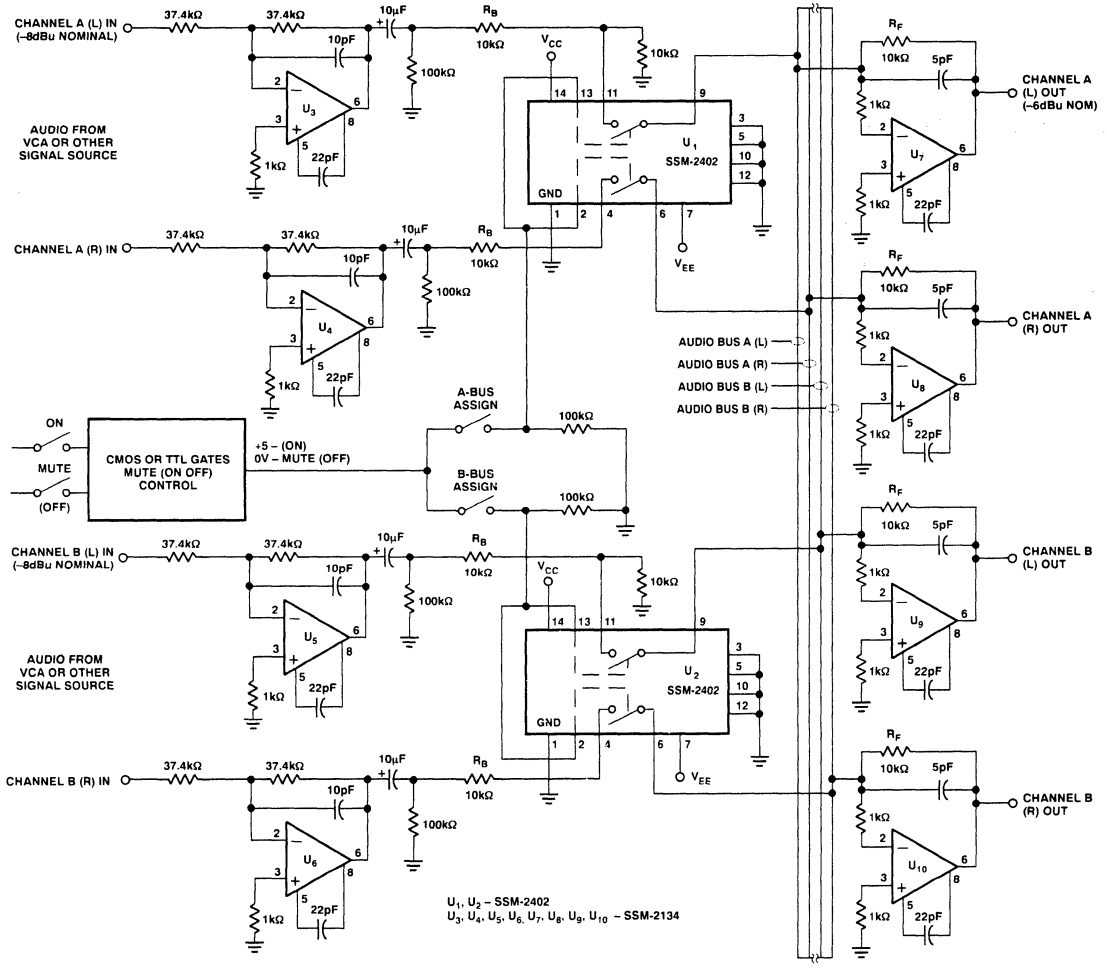

FIGURE 1: *Audio Mixer Channel Mute (On/Off) Circuit (Unbalanced Design with Virtual Ground Switching)*

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transients. The SSM-2402 switch closed (ON) resistance is typically 60Ω in series with R_B (10kΩ). As shown in this mixing system, the tolerance of the 60Ω contributes to less channel imbalance than the 1% resistor tolerance, thus eliminating the need for level trim adjustments.

The SSM-2402 employs a "T" switching configuration that yields superior ON-OFF signal isolation. In the OFF state, the "T" configuration of the SSM-2402 virtually eliminates leakage of the input signal (down more than 100dB at 1kHz with guard pins 3, 5, 10 and 12 grounded) onto the mixing bus(es). The part also features a 7ms ramped turn ON and 4ms ramped turn OFF, for transient free audio switching even with signal applied. The switch also operates with a break-before-make switching sequence. These properties are significant when many remotely controlled electronic switches are connected in series and controlled by a single device, as in large audio systems managed by an automation computer.

CONTROL INTERFACE

In this application note, the bus assignment (selection) switches are shown functionally for clarity. The control ports of the SSM-2402 can easily be interfaced to conventional 5V TTL or CMOS logic control circuits. $+5V_{DC}$ (logic high) closes the switch (ON), and $0V_{DC}$ (logic low) opens the switch (OFF). The common interface levels improve the reliability and serviceability of any products it's designed into. Diverse logic gate control designs or computer controlled schemes can easily be implemented.

DRIVE REQUIREMENTS – THE INPUT CIRCUIT

The application employs two SSM-2402 dual audio switches in a four-bus configuration (two stereo buses) driven by U_3, U_4 and U_5, U_6 bipolar amplifiers. The buffer amplifiers are signal inverting, with their gain set to 0dB ($A_V = 1$). The input amplifiers also serve as source signal level clippers that prevent the input signal from exceeding the input range of the switches, thus preventing the switches from passing a distorted signal when overdriven in the open (OFF) state. A nominal input drive level of –10dBu is applied to the switch and will maximize the signal-to-noise ratio, and optimize headroom. The output of U_3, U_4, U_5, and U_6 are AC coupled to further minimize the switching transient noise caused by signal path DC voltages from previous origins.

The virtual ground mixing buses are current driven by R_B (10.0kΩ) resistors. Once again, this is a compromise value that can be changed to accommodate the extent of the mixing bus implemented. A greater number of input mixing channels will warrant a lower bus drive current. Although other values can be used, the resistance values of R_B and R_F should be the same. As shown ($\pm 18V_{DC}$ power) R_B will apply approximately 1.7mA peak current to the mixing bus. This is well within SSM-2402 switching capabilities, as well as the SSM-2134 drive capabilities. The signal current is low enough to keep return ground currents low enough to prevent crosstalk resulting from the mechanical wiring constraints. Returning ground currents independently to the noninverting input of the summing amplifier is advised.

THE OUTPUT SUMMING AMPLIFIER

The design utilizes the SSM-2134, the PMI version of the popular NE5534 bipolar operational amplifier. The circuit features a significant reduction in summing amplifier noise, a decrease in temperature and bus impedance effects on the static output voltage as a result of using a bipolar amplifier. This design also balances the input circuit reflected source impedance of the bipolar IC amplifier, alleviating the unity-gain instability and eliminating the unbalanced input topology for inverting summing designs that could cause output offset.

The SSM-2134 has a noise voltage of $2.8nV/\sqrt{Hz}$, thus the noise floor is reduced by 3 to 10dB. Additionally, frequency and phase response performance have been improved. Only minimal compensation is required in the feedback loop of the SSM-2134 to maintain unconditional stability. The slew rate remains greater than 10V/μs, with bandwidth exceeding 50kHz.

SUMMARY

The design application shown in Figure 1 is signal noninverting, and utilizes a minimum number of noise generating elements. The circuit configuration produces linear signal mixing at the virtual ground summing node ($e_S = 0V_{AC}$); therefore, no reflected interaction occurs between the input sources. The signal input to any output frequency response is typically 10Hz to 50kHz, ±0.5dB. Total harmonic distortion plus noise will measure less than 0.01%, from 20Hz to 20kHz. SMPTE intermodulation distortion is less than 0.02%. With prudent printed circuit board design, a greater than 100dB mute isolation @ 1kHz can be obtained.

The application shown employs $\pm 18V_{DC}$ power supplies to produce a +24dBu audio output clip level. All SSM components will operate with equal reliability at $\pm 20V_{DC}$, producing approximately a 1dB increase in clip level. If the extra headroom is necessary, a $\pm 20V_{DC}$ power supply voltage is encouraged. The noise increase will be indiscernible, even in large mixing systems.

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A Two-Channel Noise Gate

This application applies the SSM-2120 as a dual-channel noise gate or adjustable threshold downward expander. A noise gate is a type of noise reduction system that fully attenuates a VCA when no audio signal is present. The SSM-2120 contains two class A VCAs (Voltage Controlled Amplifiers) and two wide dynamic range full-wave rectifiers and control amplifiers. The VCA section is a current amplifier device whose gain is controlled by two gain ports that have dB/V scaling. The VCAs are employed as wide bandwidth amplifiers with the current inputs and outputs operating in a virtual ground configuration. The rec-

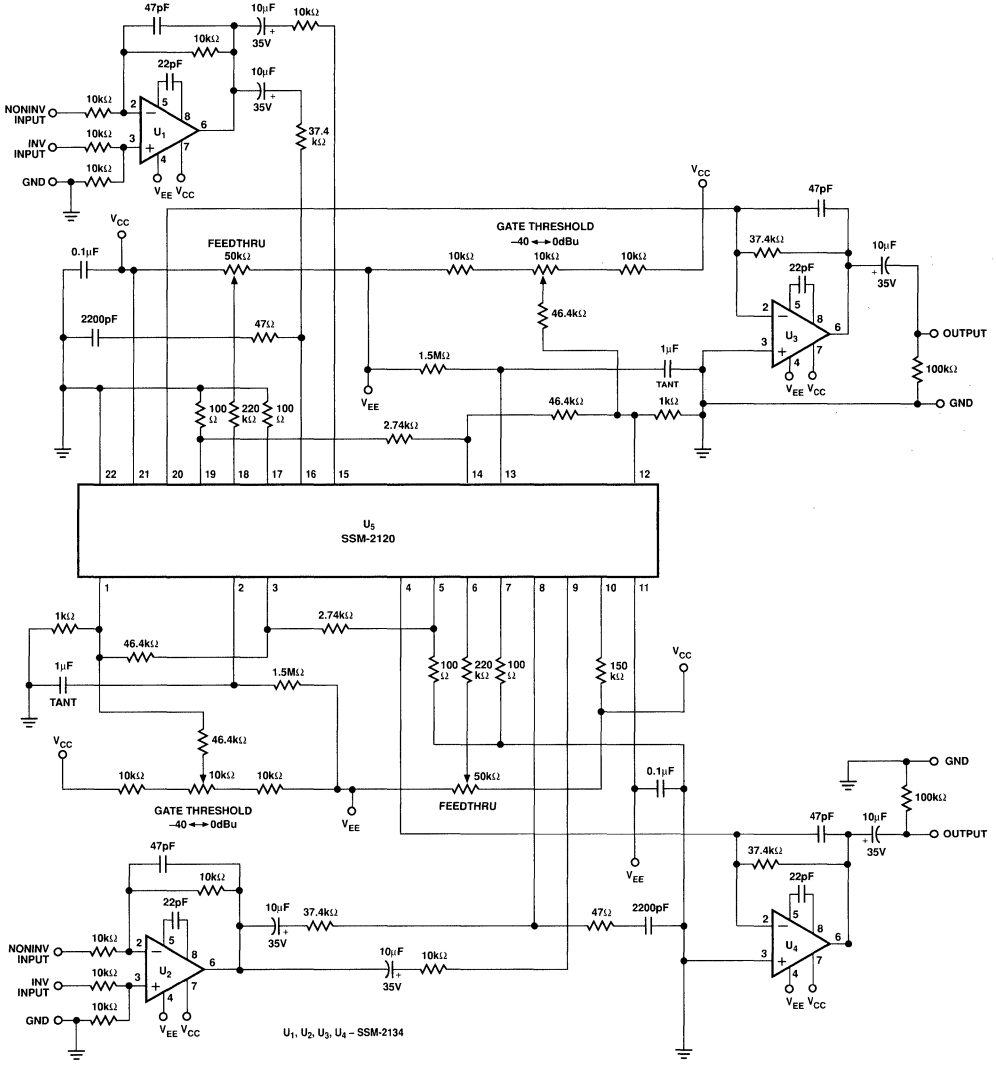

FIGURE 1: *Two-Channel Noise Gate*

tifiers are full-wave averaging type with 100dB dynamic range, followed by LOG converters. The part also contains two operational amplifiers with PNP output transistors connected in a common collector configuration.

Two SSM-2134s are used as input amplifiers, U_1 and U_2, to provide noninverting, inverting, or balanced inputs. Unbalanced loading is 10kΩ and balanced loading 20kΩ. U_1 and U_2 gain is set at 0dB, and with a –10dBu nominal input signal and $\pm 18V_{DC}$ power, will provide overall circuit headroom of 30dB. The VCA(s) could be DC coupled, although in this application they are AC coupled to reduce the dependence on trimming the side chain voltage modulation feedthrough. In critical applications the feedthrough trim controls and 220kΩ resistors should be added.

The SSM-2120's internal rectifier produces a negative DC voltage referenced to ground. The LOG amplifier bias is set by the 1.5MΩ resistor. The 1.5MΩ resistor also provides the discharge current path for the 1μF capacitor, that controls the gate's downward expansion time constant. The LOG amplifier provides a constant current capacitor charging value. It results in an attack (return 0dB gain) time constant T_C of approximately 6ms, and a downward expansion T_C of 350ms.

The internal op amp gain A_V is set at 47, with the inverting input also providing the reference voltage. The reference voltage range from the gate threshold control allows the gating to activate at any source signal level from –40dBu to 0dBu. The output from the op amp drive transistor supplies a negative control voltage to the VCA ($+V_C$) control port(s). The VCA(s) control ports have a sensitivity of 6mV/dB. As shown, the voltage divider provides a 2:1 downward expansion slope. Below the threshold level, the gain slope is $2dB_G/dB_{IN}$.

The VCAs are current output amplifiers that are designed to operate with virtual ground configurations such as U_3 and U_4. The VCA input current is supplied by the 37.4kΩ resistor and input voltage signal. The virtual ground amplifier feedback resistors are 37.4kΩ. With no VCA control voltage, the overall circuit voltage gain is 1 (0dB). Other non-gating gains can be attained by changing the output amplifiers feedback resistor value. The VCA input resistor should remain as shown for maximizing the performance of the VCA(s).

TABLE 1: Circuit Performance Specifications

Nominal Input Voltage (–10dBu Out)	–10dBu
Headroom (–10dBu Out)	+30dB
Input Type/Impedance, Balanced Unbalanced	20kΩ 10kΩ
Downward Expander Class	Feedthrough
Threshold Sense Time Constant (6dB)	350ms
Threshold Range (Level)	–40dBu to 0dBu
Gate Deactivate Time Constant	6ms
Signal Rectifier Type	Full-Wave Averaging
Modulation Feedthrough, Trimmed	< –60dBV
Gain Reduction Ratio, Downward Expansion	1 to 2 (–2dB/dB)
Frequency Response (20Hz to 20kHz)	±0.25dB
Dynamic Range	100dB
THD + Noise (20Hz to 20kHz)	0.02%
IMD (SMPTE 60Hz & 4kHz, 4:1)	0.05%
Output Voltage Slew Rate	6V/μs
Output Voltage (2kΩ Load)	+22dBu
Output Type	Unbalanced
Power Supply	$\pm$ 18V_{DC} Regulated

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A Precision Sum and Difference (Audio Matrix) Circuit

When constructing an accurate sum and difference signal from stereo left and right sources, amplitude and phase (delay) errors can contribute substantial amounts of crosstalk in the reconstructed left and right audio channels. A minor 1dB difference, or 6° phase error, will result in only 25dB stereo channel separation. The design presented has essentially no phase or group delay in the sum or difference outputs as measured over the audio spectrum, 20Hz to 20kHz. This circuit utilizes matched (laser trimmed) resistor networks combined with high open-loop gain differential amplifiers to guarantee virtually no phase and amplitude error in the sum and difference channels.

Amplifiers U_3 and U_4 (SSM-2134) are utilized as input signal buffers that provide a low source impedance (0Ω) to the 10kΩ summing resistors that feed the virtual ground current summing

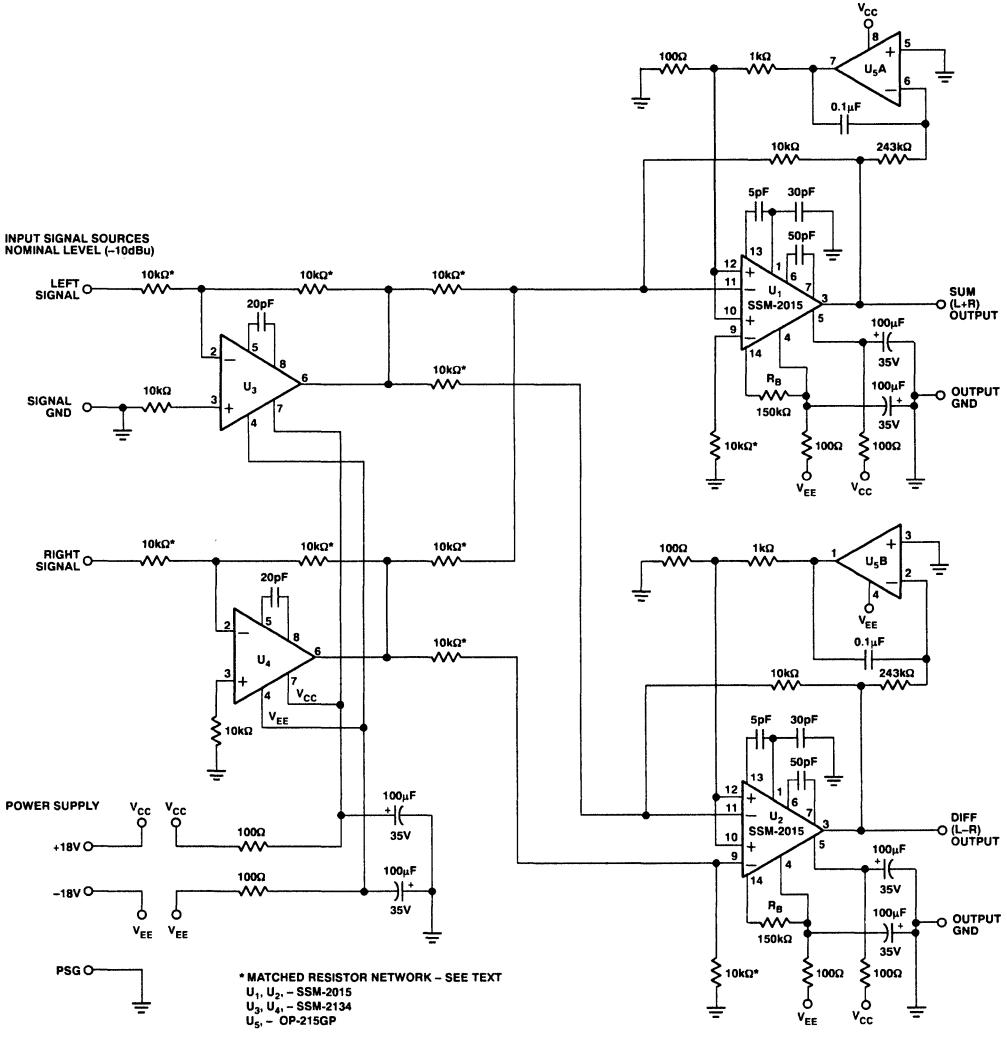

FIGURE 1: *Precision Sum and Difference (Audio Matrix) Circuit*

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nodes of U_1 and U_2. The overall gain of the buffer circuit is 0dB. The buffer amplifiers, U_3 and U_4, are compensated for a frequency response that extends to 100kHz at +24dBu. The buffers are configured as inverting amplifiers for lowest phase and group delay effects.

U_1 and U_2 (SSM-2015) are true differential input, high performance bipolar amplifiers. The current summing inputs have been employed for sum and difference operations. All bipolar and JFET op amps exhibit considerable propagation time differences between inverting and noninverting inputs, which result in phase and group delay errors. The SSM-2015 was selected because this device has practically equal propagation time between inverting and noninverting inputs (typically less than 10ns differential). This important characteristic produces high accuracy L + R and L – R signals. Because U_1 and U_2 are ultra-low noise audio preamplifiers, they contribute little noise and distortion to output signals.

U_5 (OP-215GP) is a dual JFET amplifier, and is utilized as a long time constant integrator, or DC servo amplifier. The noninverting input is referenced to ground ($0V_{DC}$) and will hold the output terminals of U_1 and U_2 at $0V_{DC}$. Capacitor (AC) coupling is not recommended as it would allow formation of envelope and low frequency group delay distortion.

CONSTRUCTION REQUIREMENTS

All 10kΩ resistors must be matched within 0.05% of each other, but can be 5% in value tolerance. The 0.1µF capacitor in the integrator circuit should be a metalized polyester film capacitor with 10% tolerance. The power supply rails are regulated at $\pm 18V_{DC}$.

TABLE 1: Circuit Performance Specifications

Frequency Response (± 0.02dB)	20Hz to 20kHz
Dynamic Range (20kHz Bandwidth)	104dB
THD + Noise (20Hz to 20kHz, +24dBu)	0.007%
IMD (SMPTE 60Hz & 4kHz, 4:1, +24dBu)	0.015%
Slew Rate	10V/µs
Nominal Signal Level	–10dBu
Maximum Output Voltage (2kΩ Load)	+23.3dBu or $11.3V_{RMS}$
Amplitude Accuracy	0.05%
Differential Error	<10ns

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A Two-Band Audio Compressor/Limiter

The two-band audio compressor amplifier shown in Figure 1 features separate and adjustable signal compression ratios and threshold levels. This design employs the SSM-2120 Dynamic Range Processor, and SSM-2134 low noise op amps.

The design features: an inverting or noninverting input buffer amplifier; high-pass and low-pass filters; and a voltage-controlled amplifier driven by a log-average level detector with a full-wave rectifier. Additionally, there are fully adjustable gain reduction controls, and adjustable compression threshold level controls. Signal-to-noise ratio exceeds 100dB, while the level detector allows the compressor to operate transparently throughout the audio spectrum without interaction between high and low bands.

The circuit includes a line level input (−10dBu to 0dBu nominal) buffer amplifier, with inverting or noninverting inputs that have 10kΩ input impedance. The buffer also limits step-function slewing voltages from entering the next stage and isolates the input source from the high-pass and low-pass filter stages.

Both high-pass and low-pass filters are of the single-pole type. This filter class eliminates combing effects in the stop bands, and compensates for compressor artifacts when the two bands are summed back together in the output amplifier stage. Such artifacts include the compressor's effect on the amplitude of each independent band, and the filter's effect on the summing influence has been taken into account in the design.

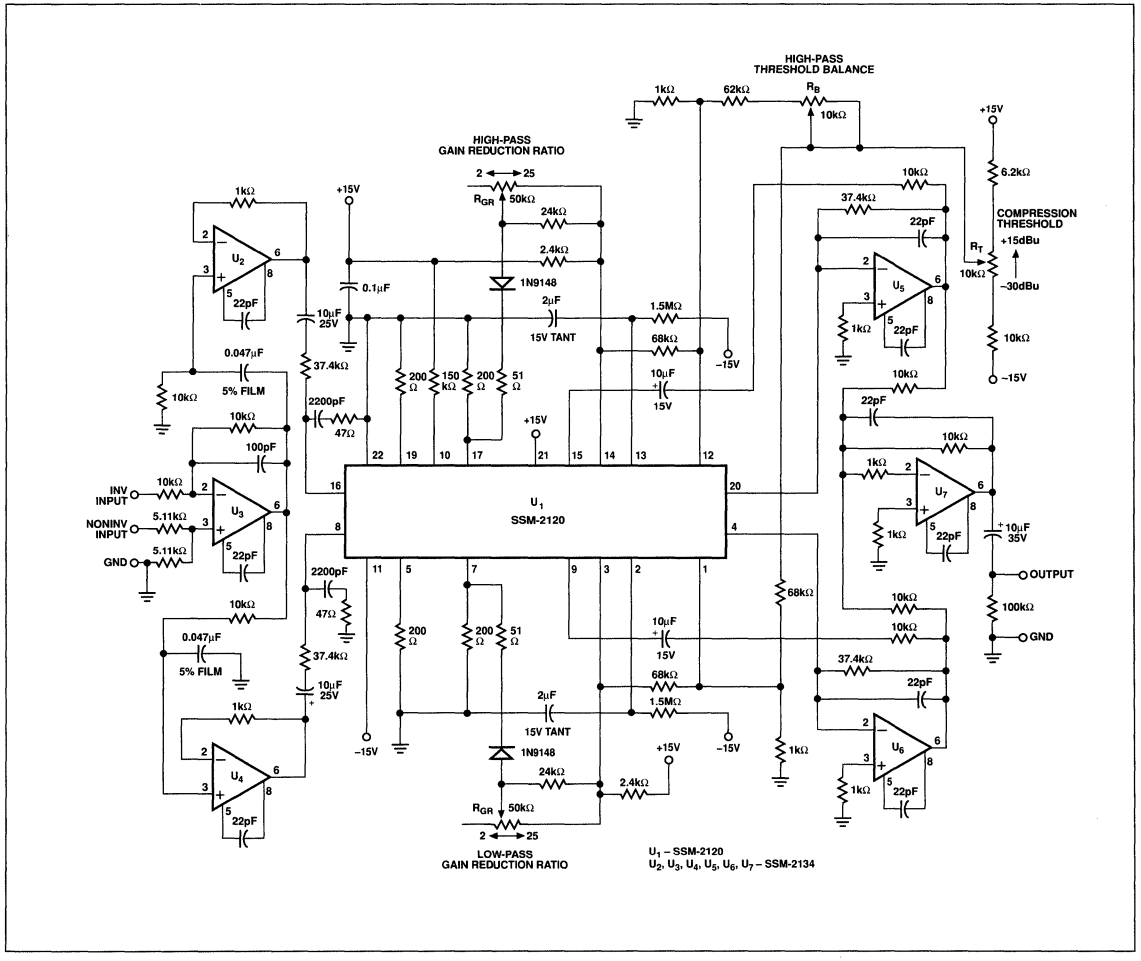

FIGURE 1: *Two-Band Audio Compressor*

Two continuously variable gain reduction controls (R_{GR}) in the VCA control circuit provide independent adjustment of compression gain slopes. The GAIN REDUCTION ratios are each adjustable from 2 to 25 for high-pass and low-pass bands. This range of adjustment provides mild compression to severe limiter/clipper action independently on each band. Thus the irritating "hole producing and pumping" character of single, wide-band compressor circuits can be reduced. The SSM-2120 provides a dynamic range of greater than 100dB over the frequency range of 20Hz to 20kHz with typically less than 0.02% THD + noise, and 0.05% IMD. Figure 2 shows THD+N vs. frequency, and Figures 3 and 4 provide compression and ratio characteristics.

The Compression Threshold control (R_T) allows the compressor to take effect from – 30dBu to +20dBu input levels. The SSM-2120's log-average precision rectifier is configured as a feedback-type level detector. The design produces consistent and precise compression profile of the input signal with no threshold level or compression drift over time and temperature.

The SSM-2120's full-wave log-averaging rectifier and control amplifier form an integrator and buffer circuit that isolates the low impedance VCA control port from the integrator timing circuit. This circuit senses the VCA output level and modifies its compression profile by feeding the averaged VCA signal plus the compression threshold control signal back into the VCA control ports. The control R_B balances the threshold amplitude between the two bands to pre-establish the compressor dynamics.

The small signal averaging time for the 2μF integration capacitor shown is 12ms. The attack time to 3dB of final value is about 6ms and is almost independent of signal level increase for level changes in excess of +10dB. The compression release rate is controlled by the 1.5MΩ discharge resistor in the integrator circuit. The recovery time constant is nearly linear since the discharge resistor returns to the $-15V_{DC}$ rail, and the rectifier produces a positive control voltage.

TABLE 1: Circuit Performance Specifications

Input Voltage Range (Nominal for 0dBu Out)	–10dBu to 0dBu 245mV to 755mV
Rectifier Type	Averaging
Compressor Amplifier Class	Feedback
Attack Time (+10dB or Greater Level Change)	6ms
Recovery Rate	1.67dB/ms
Feedthrough, Trimmed	–100dB
Gain Reduction Range	2 to 25
Frequency Response (20Hz to 20kHz)	0.2dB
Dynamic Range @ 0dB Gain	100dB
THD + Noise (20Hz to 20kHz)	0.02%
IMD (SMPTE 60Hz & 4kHz, 4:1)	0.05%
Output Voltage Slew Rate	6V/μs
Output Voltage (2kΩ Load)	+22dBu or $10V_{RMS}$

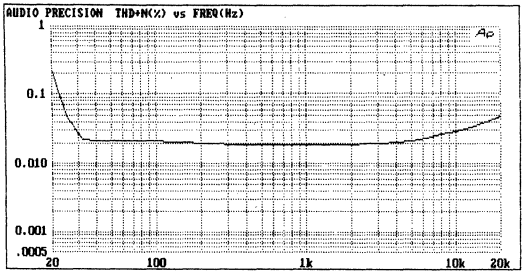

FIGURE 2: *THD+N vs. frequency ($V_{IN} = 2V_{RMS}$,using 80kHz low pass filter)*

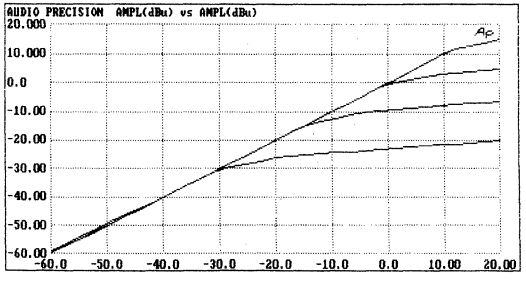

FIGURE 3: *Compression threshold variance characteristics (–30dBu to +15dBu)*

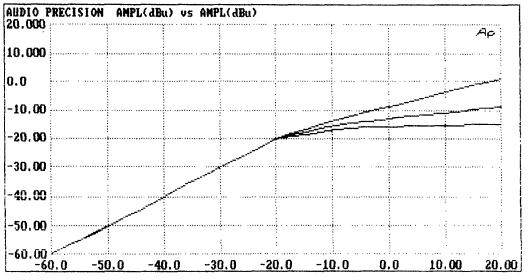

FIGURE 4: *Ratio characteristics (2:1 to 25:1)*

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A Two-Channel VCA Level (Volume) Control Circuit

The dual-channel voltage-controlled amplifier (VCA) level control circuit describes a useful application of the SSM-2122 dual VCA, SSM-2134 low noise op amp, and PMI's OP-215BP JFET/bipolar op amp. This circuit is very handy when extremely close gain matching of a stereo audio source is desired, such as in ON-AIR and production audio consoles.

The design features a balanced input buffer amplifier and VCA driven by a level shifting amplifier which is controlled by a single 10kΩ linear potentiometer. Additionally, there are fully adjustable and independent gain limit and maximum attenuation trim controls. The VCA circuit has a nominal attenuation range greater than 95dB and has input overdrive protection. The signal-to-noise ratio exceeds 100dB with a gain of 10dB, and headroom of 32dB. The amplitude varies less than ±0.1dB over the frequency range 20Hz to 20kHz. Typical THD and IMD are less than 0.005% and 0.02%, respectively.

As shown, the circuit includes two line-level inputs designed for a –10dBu input signal level. The SSM-2134 (U_2 and U_4) input buffer amplifiers can be connected for balanced or unbalanced inputs with inverting or noninverting inputs. The input loading impedance is 10kΩ unbalanced and 20kΩ balanced. The input buffer amplifier also limits step function slewing voltages from entering following stages. Other input levels can be accommodated by adjusting the feedback resistor R_{F2}. For example: for a nominal input level of 0dBu, R_{F2} should be changed to 3.16kΩ, or for a nominal input level of +10dBu, R_{F2} changed to 1kΩ to provide the optimal current drive to the VCA. C_F should also be changed to 68pF and 220pF, respectively, for both U_2 and U_3.

For other input levels, R_{F2} can be calculated:

$$R_{F2} = 10 \times 10^3 \times \text{EXP}\left(\frac{10 + \text{dBu}}{-20}\right)$$

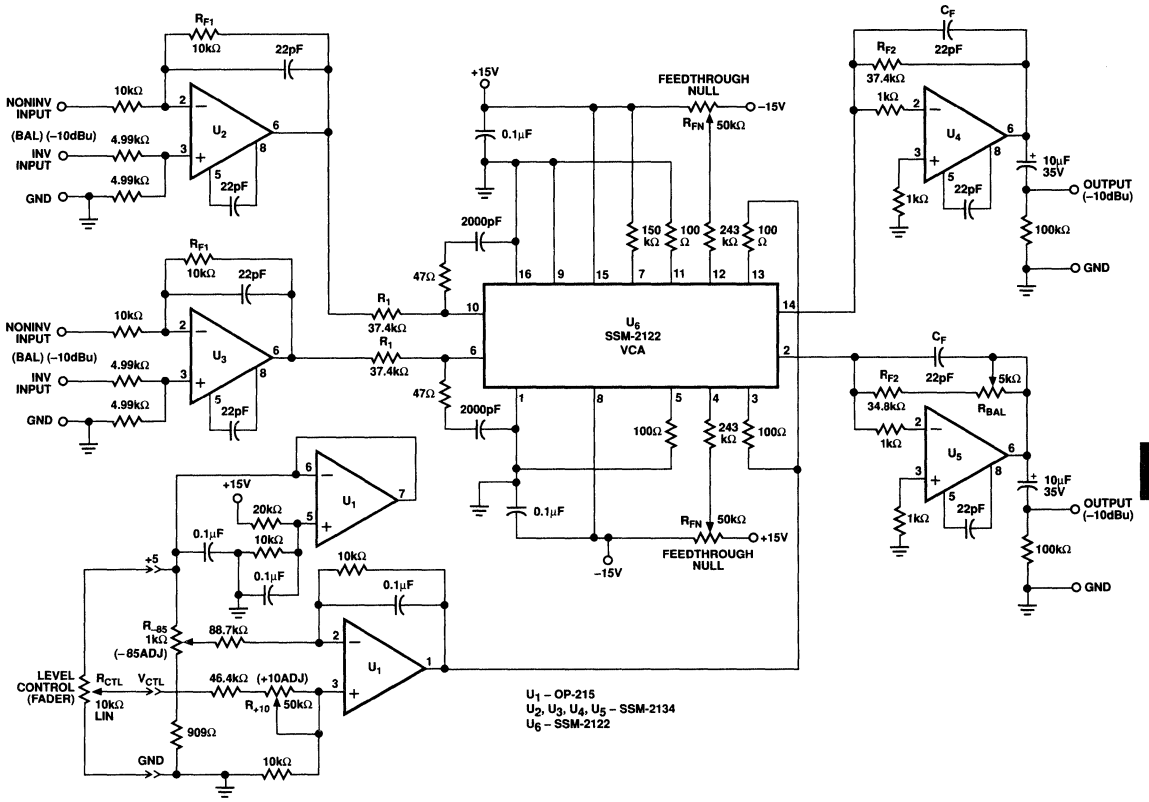

FIGURE 1: *Two-Channel VCA Level Control*

The SSM-2122 has a current-in and current-out structure. The input current is set by resistor R_1 and the virtual ground input of the SSM-2122. Similarly the transimpedance amplifier at the output converts the output current into a voltage. All devices in this design operate on $\pm 15V_{DC}$ power supply rails. The 37.4kΩ VCA input and output resistors optimize its dynamic range and minimize distortion. The SSM-2122 is a monolithic device, so the VCA gains remain uniform over a wide change in ambient temperature.

The SSM-2122 has two gain control ports that have a sensitivity of –6mV/dB. 0.0 volts at the gain control ports will yield 0dB overall gain; +60mV produces +10dB gain and –0.513V corresponds to a –85dB attenuation. The feedthrough trim null controls R_{FN} are not imperative for most applications. However, for very high performance requirements they will reduce attenuation control voltage feedthrough to less than 750μV. To adjust the null trim controls R_{FN}, inject a 100Hz sinewave into the control port through a 1kΩ resistor and a 100μF, 10V capacitor, and set the signal generator to 0.5 V_{RMS}. The control ports of U_6 are pins 3 and13. Adjust the level control R_{CTL} (fader) for 0dB gain, with the signal inputs shorted, then adjust R_{FN} for minimum 100Hz signal at the outputs.

The output amplifier(s) U_4 and U_5 are virtual ground connected current-to-voltage converters. The 37.4kΩ feedback resistors set the circuit voltage gain to 0dB with zero volts applied to the VCA control ports. Variable resistor R_{BAL} is used to balance the signal path gain of the two audio circuits. With the circuit gain set to 0dB and a test signal applied to the inputs, R_{BAL} is adjusted for equal output levels.

The VCA provides 10dB of additional gain at maximum level setting (+60mV at the VCA control ports). The THD is extremely low within the characteristic gain range of +10dB to –20dB.

The VCA control circuit is designed around U_1, the high input impedance OP-215 dual op amp. One half of U_1 is used to develop the 5V reference voltage for the level control element. This is a fail-safe design – with no voltage applied or an open connection at terminal V_{CTL}, the gain will descend to –85dB. Level control trimming is as follows: with the fader control set to minimum (0V), the trim control R_{-85} is adjusted for maximum attenuation of –85dB or $-0.513V_{DC}$ at pin 1 of U_1. Then with the fader set to its maximum (5V), trim control R_{+10} is adjusted for maximum circuit gain of +10dB or +60mV. Since there is no interaction when adjusting R_{+10} for +10dB gain, the setting for R_{-85} will remain unaffected. Other max-attenuation values can be used. R_{-85} has an attenuation range of –45dB(270mV) to –93dB (560mV).

TABLE 1: Circuit Performance Specifications

Input Voltage (Nominal for –10dBu Out)	–10dBu or $245mV_{RMS}$
Input Impedance, Unbalanced	10kΩ
Imput Impedance, Balanced	20kΩ
Headroom (Nominal for –10dBu In &Out)	32dB
Feedthrough, Trimmed	<750μV
Gain Control Range (Nominal)	+10dB to –85dB
Gain Control Voltage (+10dB to –85dB)	$5V_{DC}$ to $0V_{DC}$
Frequency Response (20Hz to 20kHz)	±0.1dB
S/N Ratio @ 10dB Gain	100dB
THD + Noise (20Hz to 20kHz, +22dBu)	0.005%
IMD (SMPTE 60Hz & 4kHz, 4:1, +22dBu)	0.02%
Output Voltage Slew Rate	6V/μs
Output Voltage (1kΩ Load)	+22dBu or $10V_{RMS}$
Output Impedance	<10Ω

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A High-Performance Compandor for Wireless Audio Systems

Wireless audio systems are finding increasing use in live performances, as well as in communications equipment where mobility is required. Designing such systems presents a difficult challenge: how to maintain adequate audio performance in view of power supply and current consumption limitations. To reduce transmission noise, the audio signal is usually compressed at

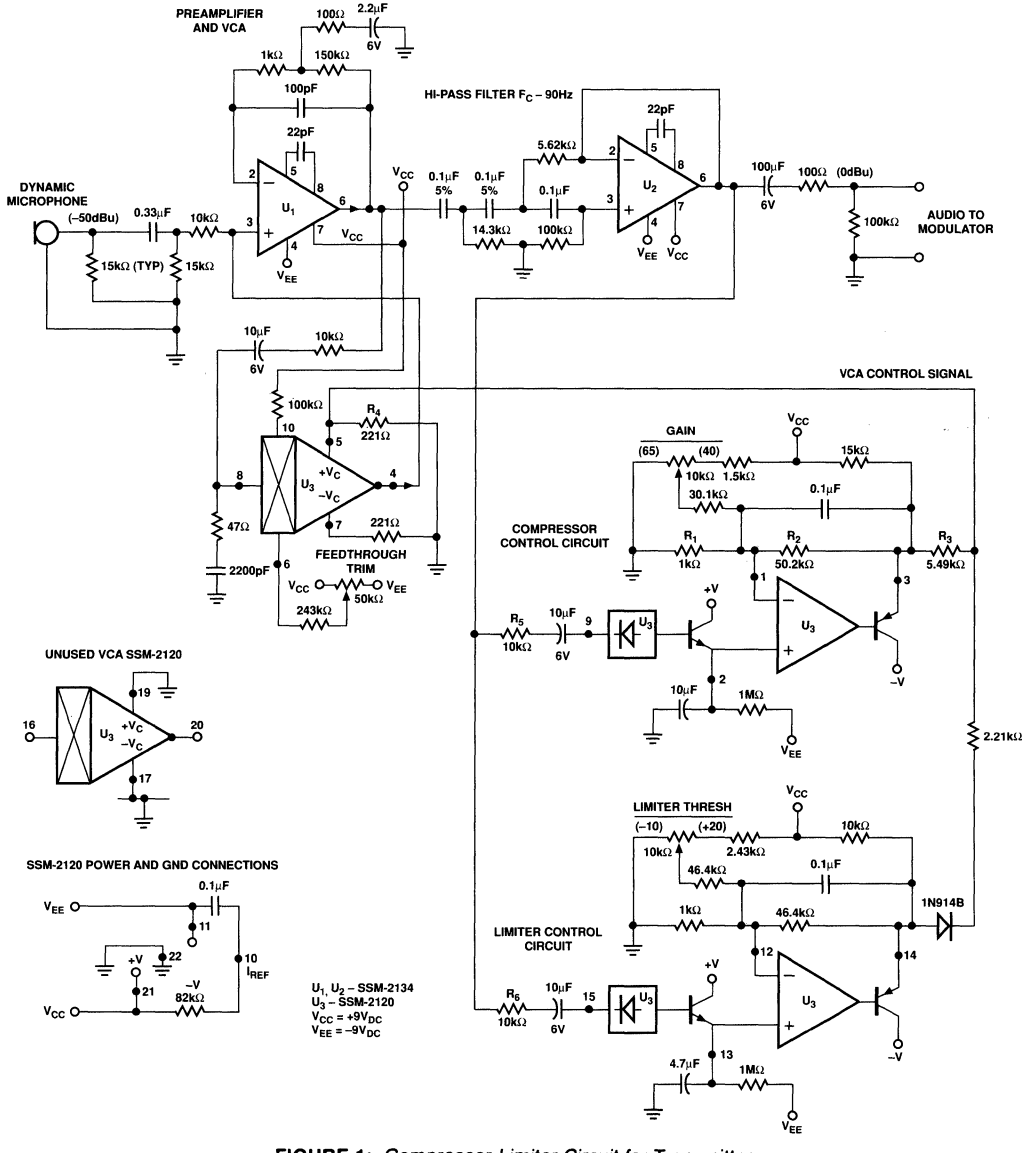

FIGURE 1: *Compressor-Limiter Circuit for Transmitter*

the transmitter and is expanded at the receiver by using a telecommunications industry-standard compandor IC, which has marginal audio performance as measured by professional standards. This application note describes a companding system utilizing the SSM-2120 Dynamic Range Processor, which permits considerable improvement over other techniques in terms of noise, distortion, feedthrough, and other key audio criteria.

Transmitters are battery powered and, hence, pose the most severe constraints on supply voltages and current consumption. Receivers are often AC powered, so bipolar supplies are more easily accommodated. Since the SSM-2120 requires split supplies, a voltage doubler circuit is necessary for the transmitter. In some cases, this may be considered unfeasible. In this event, however, the SSM-2120 is still very useful in the receiver expander circuit to complement any compressed signal, and to improve overall system performance. As a result, the compressor and expander sections of this application can be considered independently.

THE TRANSMITTER COMPRESSOR AND LIMITER CIRCUITS

COMPRESSOR

The design described is intended for $\pm 9V_{DC}$ battery operation, and includes a third-order high-pass filter for the elimination of subsonic noise and low frequency pops that would cause compandor overload or mistracking.

Figure 1 shows the connection of the SSM-2120 (U_3) VCA_1, rectifier, and control amplifier as a compressor. The VCA is connected in the feedback loop of the preamplifier U_1 to control the gain. The compressor is designed for a 2:1 compression characteristic. If the input rises 6dB, the output level will rise only 3dB. The gain compression expression is:

$$\text{Gain}_{\text{reduction ratio}} = \frac{R_2 \cdot R_4}{R_1 \cdot R_3}$$

as long as the rectifier input currents are limited by R_5, R_6 (10kΩ), and the rectifier has a ≈10μA reference current. The SSM-2120 rectifier and VCA have a dynamic range in excess of 100dB, resulting in exceptional tracking of the expander/compressor in the compandor system. High quality capacitors and resistors should be used to support the accuracy of the SSM-2120 elements. The small-signal averaging time for a 10μF integration capacitor is 25ms. The attack time to 3dB of final value is also about 26ms and is almost independent of signal level increases for level changes in excess of +10dB. The decay rate is 3ms per dB. The high-pass filter keeps frequencies below 90Hz from the input of the rectifier, reducing the low frequency distortion caused by the VCA control circuit.

DC and high-frequency feedback are provided for U_1 without sacrificing bandwidth or stability. The gain control is adjusted for 0dBu output with -50dBu applied to the microphone input terminals. The VCA is signal inverting. Its output current is summed, along with the microphone signal current, at the (virtual ground) noninverting input of preamplifier SSM-2134, U_1. The 10kΩ resistor at the input of the VCA limits the input current, iswhile the 2200pF, 47Ω network provides frequency compensation for the VCA, keeping it stable.

The 100kΩ resistor from V_{CC} to pin 10 of U_3 establishes the operating current for the VCA. To minimize power supply current, all pins of the unused VCA should be returned to ground. The FEEDTHROUGH trim control is optional, and it can be used to minimize the VCA control voltage from feeding through to the output.

PROTECTION LIMITER

The limiter uses the second rectifier and control amplifier for separate and independent attack and decay times, along with a steeper gain reduction slope. The limiter threshold control sets the predetermined gain limiting point for high input signal levels. The gain reduction ratio is 4.6:1 as shown in Figure 1. Typically, the onset of gain limiting should be set to +10dBu at the output.

As in the compressor control circuit, the rectifier input current is limited by R_6, 10kΩ, and the rectifier referenced to ≈10μA as well. Lower precision capacitors and resistors can be used here. Similar to the compressor, the attack time is much faster than the decay.

The VCA/Preamplifier was designed as a system. The VCA was put in the signal feedback loop of the preamplifier principally to prevent preamplifier overload, while keeping the overall noise low, and minimizing component count.

POWER SUPPLY

The application circuit requires two power supply voltages, $\pm 9V_{DC}$. The power consumption, for the circuit shown in Figure 1, is less than 15mA from each supply. The design described will operate properly with good dynamic range as the battery voltage begins to fall below the nominal $9V_{DC}$. It is assumed that two 9 volt batteries would be used, but for the smaller hand-held wireless microphones, a single 9 volt battery would be required. Figure 2 depicts a DC-to-DC converter that will supply the $-9V_{DC}$.

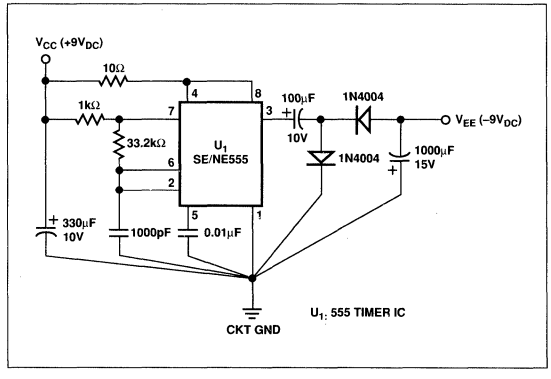

FIGURE 2: *DC-to-DC Converter for $+9V_{DC}$ to $-9V_{DC}$ at 15mA*

The converter circuit incorporates an astable oscillator running at 25kHz. It is followed by a capacitor-coupled level shifter and rectifier with a filter. A SE/NE555 timer is used in the "output sink" mode for maximum efficiency, and longest battery life.

THE RECEIVER EXPANDER SECTION

EXPANDER CONTROL

In Figure 3, the control connection of the SSM-2120 (U_3) VCA, rectifier, and control amplifier is shown. The control circuit connection to the VCA produces a 1:2 gain expansion curve. If the input rises 3dB, the output level will rise 6dB. The gain expansion ratio expression is:

$$\text{Gain}_{\text{expansion ratio}} = \frac{R_2 \cdot R_4}{R_1 \cdot R_3}$$

The rectifier input current is limited by a 10kΩ resistor connected to pin 9 of U_3, and the rectifier is biased at 10µA current through a 1.5MΩ resistor connected to V_{EE}. The SSM-2120 rectifier and VCA each have a 100dB dynamic range, resulting in accurate tracking of the compressor.

As with the compressor/limiter circuit, the small-signal averaging time for a 10µF integration capacitor is 26ms. The attack time to 3dB of final value is also about 26ms and is almost independent of signal level increases for level changes in excess of +10dB. The decay rate is 3ms per dB.

The control circuit gain values, as shown above, provide a control voltage to the VCA section $+V_C$ control port [U_3, pin 5(19)], which result in a 1:2 signal expansion characteristic. The LEVEL control sets the initial overall gain value, and is adjustable from −10dB to +20dB.

EXPANDER AUDIO

Input amplifier U_1 is a buffer between the input signal source (FM wireless receiver), the expander rectifier/control circuit, and the VCA audio signal input. If the signal source output impedance is below 100Ω, U_1 can be omitted. The nominal source signal level should be −10dBu. If signal gain or loss is required, U_1 gain structure should be modified to provide −10dBu to the VCA input current limiting resistor. The 37.4kΩ resistor ahead of the VCA input [pin 8,(16)] limits peak signal currents to avoid VCA distortion. The VCA signal input(s) are virtual ground current inputs. The 150kΩ resistor connected to V_{CC} and pin 10 of U_3 sets the VCA input/output current compliance range. A VCA input shunting capacitor shown from U_3 pin 8(16) to ground minimizes signal distortion and keeps the VCA stable by providing a high-frequency path to ground. The exact value is determined empirically. The output of the VCA feeds a virtual ground output amplifier, U_2. The overall audio path is signal noninverting, since the VCA is signal noninverting, and is combined with two inverting amplifiers U_1, and U_2.

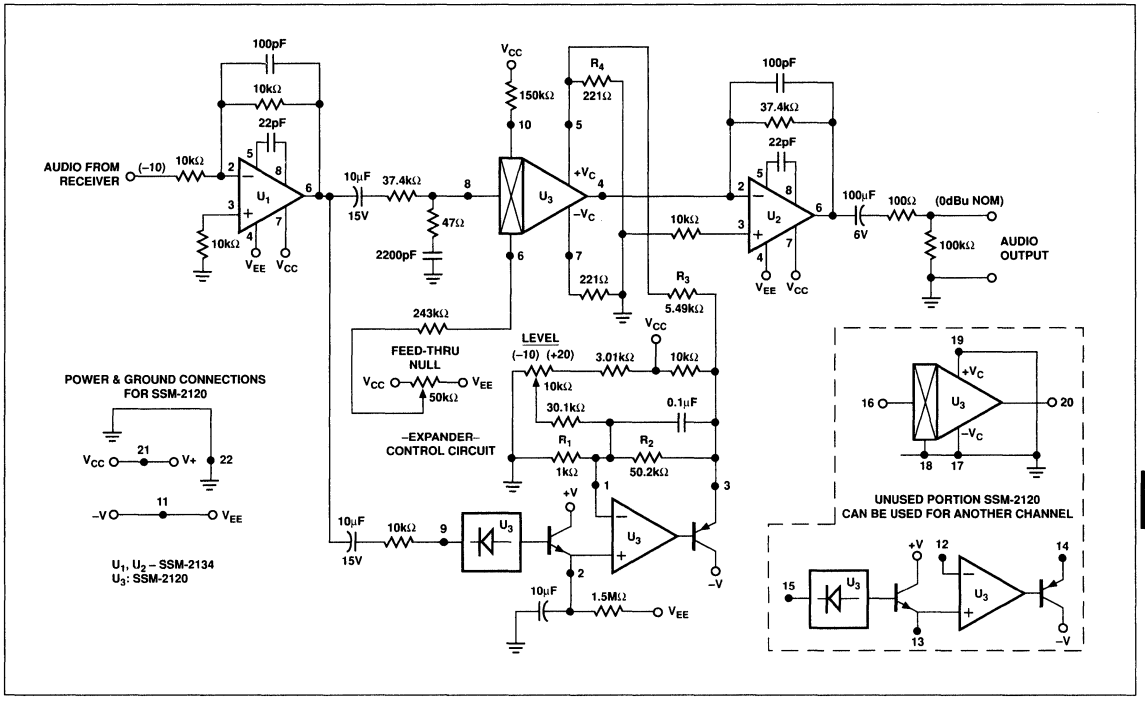

FIGURE 3: *Expander Circuit for Receiver Processor*

TABLE 1: Circuit Performance Specifications

Compressor/Limiter (Figure 1)	
Input Voltage Range (Nominal for 0dBu Out)	–65dBu to –40dBu
Compressor/Limiter Rectifier Type	Averaging
Compressor Amplifier Class	Feedback
Compressor Attack Time (to 3dB of Final Value)	26ms
Compressor Recovery Rate	3ms/dB
Feedthrough (Trimmed)	–70dBV
Compressor Gain Reduction Ratio	2:1
Limiter Attack Time (to 3dB of Final Value)	13ms
Limiter Recovery Rate	1.5ms/dB
Limiter Gain Reduction Ratio	4.6 to 1
High-Pass Filer, F_C	90Hz
High-Pass Filter Type	3rd Order Butterworth
Frequency Response (90Hz to 20kHz)	±0.5dB
S/N Ratio @ 0dB Gain	100dB
THD + Noise (% 1kHz to 20kHz)	0.05
IMD (% SMPTE 60Hz & 4kHz, 4:1)	0.05
Output Voltage Slew Rate	6V/µs
Power Supply, (Battery)	$\pm 9V_{DC}$
Output Voltage (2kΩ Load, $\pm 9V_{DC}$	+15dBu
Expander (Figure 3)	
Input Voltage Range (Nominal for 0dBu Out)	–10dBu
Expander Rectifier Type	Averaging
Expander Amplifier Class	Control Feed-Forward
Expander Attach Time (to 3dB of Final Value)	26ms
Expander Recovery Rate	3ms/dB
Feedthrough (Trimmed)	–70dBV
Gain Expander Ratio	1:2
Frequency Response (20Hz to 20kHz)	±1.0dB
S/N Ratio @ 0dB Gain (Dynamic Range)	100dB
THD + Noise (% 1kHz to 20kHz)	0.20%
IMD (% SMPTE 60Hz % 4kHz, 4:1)	0.25%
Output Voltage Slew Rate	6V/µs
Power Supply	$\pm 15V_{DC}$
Output Voltage (2kΩ Load)	+21dBu

AC coupling is not necessary but recommended. When the AC coupling is combined with feedthrough trimming, most of the unwanted sub-audible signals will be removed from the output signal. The unused portion of U_3 (SSM-2120) can be utilized in an identical second channel expander. The supply voltage should be held at ±15VDC to ±18VDC, to provide good dynamic range and circuit stability.

ANALOG DEVICES

AN-134
APPLICATION NOTE

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An Automatic Microphone Mixer

This application note describes an audio-signal activated microphone mixer, as shown, designed to accommodate eight input channels. The SSM-2120 Dynamic Range Processor is the nucleus of this design. The device includes two VCAs and two rectifier and control amplifier circuits. The application is designed for unattended microphone mixing functions, as would be used in a conference room that required sound reinforcement or conversation recording. The circuit provides automatic and transparent channel ON/OFF operation. The audio output automatically turns ON in less than 10ms and back OFF after 2 to 4 seconds of no audio. Each channel incorporates independent and automatic operation, with ON threshold sensitivity and level adjustment (trim) controls.

THE MICROPHONE PREAMPLIFIER CIRCUIT

For optimum circuit performance, the nominal output level from the microphone preamplifier or other audio source(s) should be –10dBu. The –10dBu level allows the SSM-2120 to provide the widest dynamic range and lowest noise, while optimizing the headroom of the automatic switch and the microphone preamplifier.

THE AUDIO SWITCH

Each audio signal is switched ON and OFF by a VCA (voltage controlled amplifier) element. By controlling the turn-ON and turn-OFF ramp time, the VCA produces transient-free switching. No distortion or "pops" are introduced using this technique. The turn-ON is ramped from a maximum of 90dB to 0dB attenuation in approximately 30ms. With the complete removal of the audio, the turn-OFF ramp of ≈100ms will begin after approximately three (3) seconds.

The VCA's input is a current input, virtual ground node. The design shown in Figure 1 assumes that $\pm 15V_{DC}$ will power the system. With this supply voltage, the 37.4kΩ input resistor(s) will keep the VCA operating at the optimum distortion and dynamic range. The 150kΩ resistor connected from V_{CC} ($+15V_{DC}$) to the reference current pin 10 of the 2120, sets the VCA bias operating point. The VCA's current output is then connected to a voltage by a transimpedance amplifier using a low noise SSM-2134 op amp. The VCA input(s) and output(s) are capacitively coupled to remove DC components from previous stages.

THE CONTROL CIRCUIT

The input signal is rectified and averaged before it is filtered by the integrator capacitor (10μF electrolytic). The small signal averaging time constant with this capacitor is approximately 60ms. The attack time is 30ms to 3dB of the final level, and is nearly independent of the magnitude of level increase. The discharge time is controlled by the 3.3MΩ resistor returned to V_{EE} ($-15V_{DC}$), which also sets the rectifier reference current.

The control circuit amplifier has a voltage gain of 217. The inverting input is used to set the ON/OFF threshold point, too, and allows for the ON Threshold level adjustment. The ON Threshold range is adjustable from -40dBu to 0dBu as referenced to the input of the VCA element. The control port +Vc of the VCA is used so that a negative control voltage applied will produce an attenuation effect. R_4 (221Ω) and R_5 (4.64kΩ) attenuate the control voltage by a factor of 22, resulting in a maximum attenuation value of 90dB with no audio signal present.

To minimize the effect of ON/OFF control voltage appearing in the output signal of the VCA, the Feedthrough null control circuit is recommended. It provides an external method for balancing the internal VCA currents and component values.

THE OUTPUT SECTION

The design incorporates a virtual ground current summing bus, that is fed by the individual mixing channel level control(s) and 10.0kΩ resistor(s). The Level control(s) provides 21dB attenuation range (0dB to –21dB), and is designed to balance the different inputs, but not turn them off fully. The 100kΩ (linear taper) level control(s), for a linear rotation produces a logarithmic attenuation curve.

The virtual ground summing amplifier establishes half of the balanced output circuit, with another inverting amplifier completing the balanced output circuit. The circuit is able to drive 600Ω loads to +24dBm levels with low distortion and high reliability.

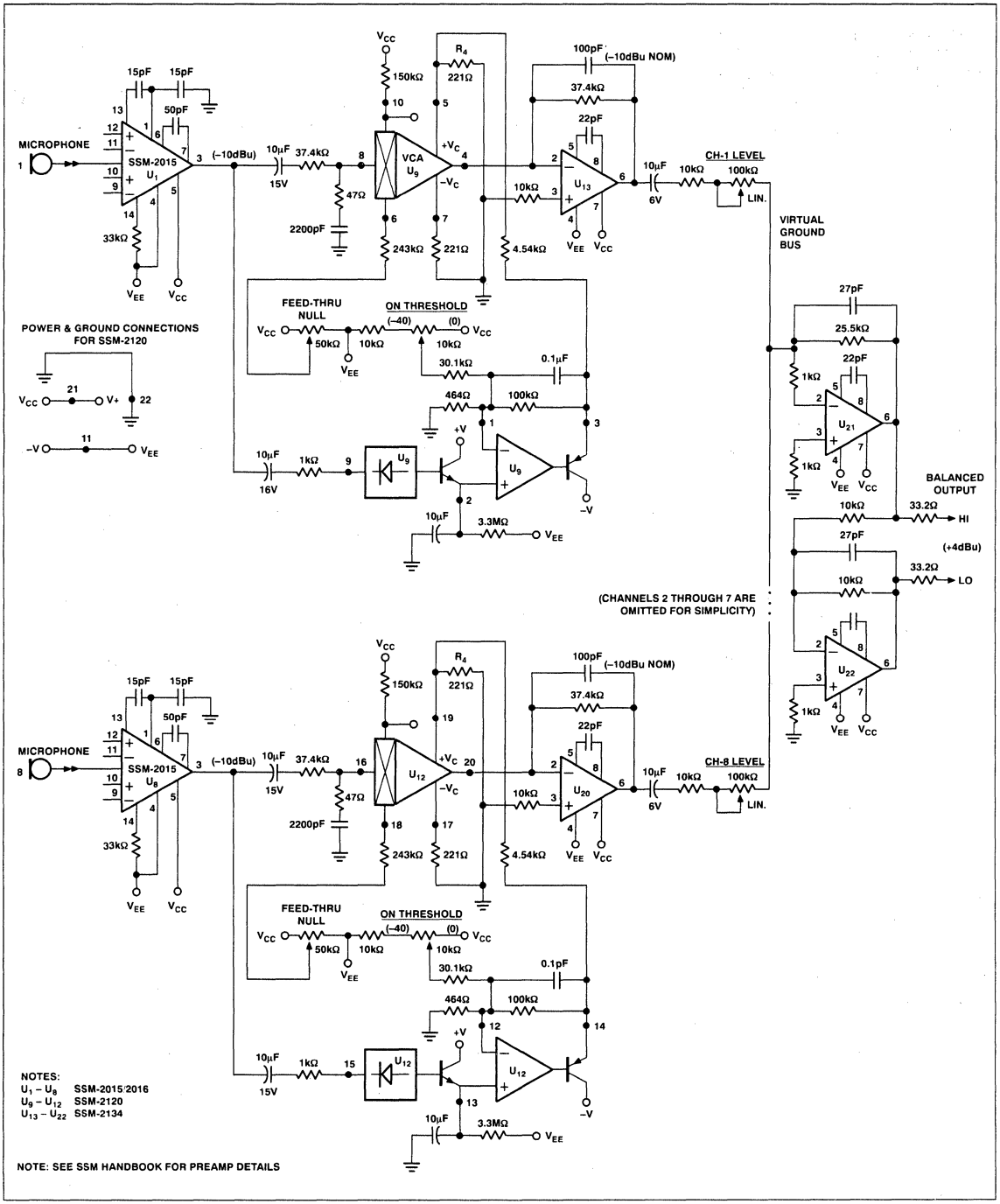

FIGURE 1: *Automatic Channel Activation Microphone Mixer Diagram Illustrates 8 Input Channels*

TABLE 1: Circuit Performance Specifications

Input Voltage, without Preamplifier, (for +4dBu Out)	−10dB
Input Impedance, Unbalanced	≈1kΩ
Headroom (Nominal for −10dBu In and Out)	32dB
Turn ON Time (to 3dB of Final Value)	30ms
Turn OFF Time (No Signal)	≈3sec
Turn OFF Ramp Time	100ms
Feedthrough (Trimmed)	>1mV
ON/OFF Threshold Range (Nominal)	0dBu to −40dBu
ON/OFF Gain Extent	0dB to −90dB
Frequency Response for ±0.1dB	20Hz to 20kHz
S/N Ratio @ 0dB Gain	110dB
THD + Noise (from 20Hz to 20kHz)	0.005%
IMD (SMPTE 60Hz and 4kHz, 4:1)	0.02%
Output Voltage Slew Rate	12V/μs
Rated Output Level (600Ω Load)	+24dBu
Output Impedance	68Ω
Output Type	Balanced
Power Supply Requirements	$\pm 15V_{DC}$ Regulated

ANALOG DEVICES

AN-135
APPLICATION NOTE

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The Morgan Compressor/Limiter

The following application was written by Michael Morgan, a consultant to PMI with extensive experience in the design of professional audio equipment, including high-performance dynamic range processors. While currently a freelance consultant, Mr. Morgan spent nine years at Valley International as a principal designer of their products.

This application note describes the configuration of a low cost, high quality compressor with variable attack time and ratio control using the SSM-2110 Level Detector and SSM-2014 VCA. The discussion begins with an overview of compressor/limiter fundamentals, and is followed by a description of the unique attributes of the integrated circuits and their implications for the design engineer.

COMPRESSOR/LIMITER FUNDAMENTALS

The function of the audio compressor is, of course, to compress the dynamic range of the processed audio signal by altering the gain of its signal path in response to the relative level of the signal as compared to an arbitrary setpoint called the threshold, thus adding gain to low-level signals and reducing gain in the presence of high-level signals.

An audio compressor consists primarily of two functional sections, one of which derives a control signal by measuring and otherwise manipulating the audio signal to produce a voltage suitable for the second functional section, which is the gain control element. The gain control element is a device which can alter its attenuation, gain, or resistance in response to an external signal, such as a voltage or current.

The audio compressor differs from a similar device, called a limiter, in that a compressor exhibits a rotation point which is independent of its threshold setting. The rotation point is the locus on a graph of the compressor's transfer function at which the gain control element exhibits unity gain, and through which all lines derived from data describing the device's output level as a function of input level will pass. A limiter, in the purest sense, adds no gain and has no rotation point.

The compressor's ratio is defined as the increase in input level, in decibels, above the threshold which will result in an increase of output level equal to 1dB, and is a function of control circuitry gain. For example, each increase of 1dB in signal level above the threshold may cause a corresponding decrease in gain equal to 1dB, thus keeping the output level constant for a ratio of infinity:1, or it may cause a 1/2 dB decrease in gain, thus allowing the output level to rise at a ratio of 2:1. A compressor may have a very high ratio, and conversely, a limiter may have a very low ratio.

SHAPING THE RESPONSE

Figures 1a and 1b illustrate the transfer function of an ideal compressor as the ratio is varied with a fixed threshold, and as the threshold is varied with a fixed ratio, respectively. Note that in both cases, the rotation point is easily identified at 0dB. Note also that the compressor operates as a limiter when the threshold is equal to, or higher than, the rotation point. For this reason, the device described in this application note may be considered as a "compressor/limiter," but because it possesses a rotation point, we shall refer to the device as a compressor.

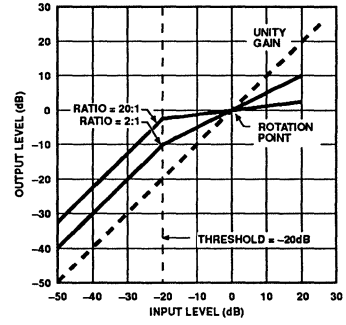

FIGURE 1a: *Output vs. Input Transfer Function of an Ideal Compressor*

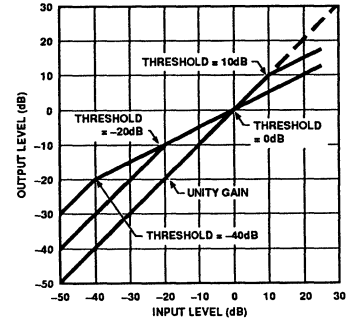

FIGURE 1b: *Output vs. Input Transfer Function of an Ideal Compressor Having a Fixed Ratio Showing the Effect of Threshold*

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Audio compressors use two types of circuit topologies. In a feedback, or closed-loop configuration, the control signal is derived by measuring the output level of the gain control element. In a feedforward, or open-loop configuration, the control signal is derived by measuring the level of audio present at the input of the gain control device. Each topology has its typical advantages and disadvantages. The most common type of audio compressor uses the feedback topology. Among its advantages are: low parts cost; ease of configuration; ability to use simple, "linear" control circuitry and gain control elements. The disadvantages of the feedback topology are numerous: inability to realize continuously variable parameters accurately; heavy dependence upon circuit trimming to assure consistency in performance from unit to unit; tendency toward overshoot in either control signal or processed signal; virtual inability to configure circuitry for performing arbitrary dynamic functions, such as program control of release times, equalized sidechain functions, and interactive processing having more than one control function per gain control element.

The feedforward topology has long been considered by equipment designers to be the more versatile method of configuring audio dynamics processors. Among its advantages are: precise control of dynamics; ability to accurately and continuously vary processor parameters, such as ratio and attack-and-release time constants; easy circuit trimming for unit-to-unit consistency; possibility to realize arbitrary types of dynamics alteration; ease in configuration of interactive processing schemes using multiple control signals to operate a single gain control element; and relative freedom from control and signal overshoot. The disadvantages of feedforward topology have traditionally been: dependence upon relatively expensive and little understood logarithmic circuitry in configuration; difficulty in sourcing high-quality, low cost log/linear multipliers (dB/volt VCAs); dependence upon expensive log/RMS detection schemes to achieve the required accuracy for wide range of control.

By using integrated building blocks, feedforward control technology can be realized by equipment designers by virtue of their ease of application and low cost. These readily available integrated circuits deliver performance equal to or surpassing complicated discrete circuits, and are more cost effective for general use by equipment manufacturers.

THE SSM-2110 MONOLITHIC LEVEL DETECTOR

The SSM-2110 level detector IC represents a significant advancement in low cost, high quality converter circuitry. The device greatly simplifies the design of feedforward dynamic processors since it produces an accurate output that is proportional to the log of the absolute value of its input, and the log of the rms value of its input, in addition to the corresponding linear values. Such versatility is unique among detector/converter configurations.

VARIABLE TIME INTEGRATOR

In this application, the SSM-2110 is used in the design of a feedforward compressor. The log of the absolute value of the input signal is extracted, then integrated by a E/I x C circuit which corresponds roughly to an RC network in the linear domain (see Figure 2).

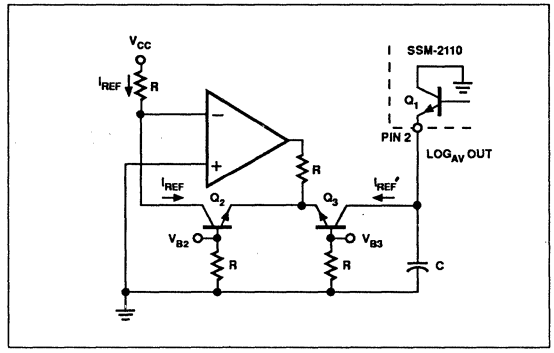

FIGURE 2: *Simplified Schematic of a Variable Time Constant Log of Average Integrator Using the SSM-2110*

The product of this operation is not, as one would expect, the average of the log of the absolute input value. During the integration process achieved by charging the integrator capacitor, C, the charging current is proportional to the antilog of the voltage appearing at the base of Q_1. Since the voltage at the base of Q_1 represents the log of the absolute value of the input, the log and anti-log terms cancel, thus leaving C to charge as a linear integrator with a current proportional to the absolute value of the input until the voltage across C approaches the voltage at the emitter of Q_1. In this manner, the order of the logging and averaging operations are reversed. This is a very important phenomenon which directly influences the audibility of the compression process, and will be discussed at length later.

The integration time of the circuit in Figure 2 is varied by changing the current through the collector of Q_3. This is accomplished by means of the multiplier circuit consisting of the operational amplifier, transistors Q_2 and Q_3, and their associated resistors.

Current I_{REF} is forced to flow through the collector of Q_2. The V_{be} of Q_2 is thus made to be proportional to the log of I_{REF} by virtue of the silicon transistor's intrinsic logarithmic property, idealized in the equation:

$V_{be} = kT/q \times \ln(I_c/I_s)$ where

k = Boltzman's constant (1.38×10^{-23}J/K)

T = Temperature in Kelvins

q = Charge on an electron (1.60×10^{-19}C)

I_c = Collector current

I_s = Reverse saturation current (extrapolated as $V_{be} \rightarrow 0$)

When transistors Q_2 and Q_3 are closely matched, V_{be} of Q_2, which appears also at Q_3's emitter, causes a current equal to I_c of Q_2 to flow through the collector of Q_3. This transistor collector current, I_{REF}, may be used to charge or discharge a capacitor, to cause a voltage drop across a resistor, or may be converted to a voltage at the output of an operational amplifier. The collector current of Q_3 may be varied by applying a voltage at the bases of Q_2 or Q_3, or both bases simultaneously. As a rule of thumb, at 25°C, each 60mV change in V_b will cause a corresponding ten-fold change in Q_3's I_c. By using the "shorthand" log relationship for gain in which a ten-fold change in voltage (or current) equals 20dB, we can say that the collector current of Q_3 can be made to vary antilogarithmically at a rate of 1 dB/3mV (20dB/60mV). In effect, the circuit generates a voltage at the emitter of Q_2 which corresponds to the log of the input current, I_{REF}, adds the control voltage, then generates a current at the collector of Q_3 which is proportional to the antilog of the sum. Thus the portion of the circuit formed by the operational amplifier, Q_2, Q_3, and their associated passive components form a two-quadrant multiplier whose output is a high compliance current sink.

A positive voltage applied to the base of Q_2 will cause a corresponding decrease in Q_3's collector current, while a positive voltage applied to the base of Q_3 has the opposite effect, causing an increase in I_c of Q_3. Both bases may be controlled by bipolar voltages, but I_{REF} must flow in the direction indicated by conventional current flow through the transistors (must be sourced from a voltage more positive than the noninverting input of the operational amplifier for NPN transistors).

In operation, varying the current which discharges C also causes a varying offset voltage at the collector of Q_3 which equals the change in V_b, and must be compensated for in order to derive a useful control voltage. Figure 3 shows the response to a +10 volt pulse input having a repetition frequency of approximately 4 pps and a duty cycle of 50%. Note that the X-axis corresponds also to increasing integration time (decreasing I_c of Q_3). The illustration is a composite of several sampled waveforms, thus, scalar references in the X-axis are valid only for each pulse.

As can be seen in Figure 3, in the log average detection mode, the response of the device to large level changes is relatively fast, while the last 50 to 100mV of change occurs at the characteristic integration time determined by the status of the charge on the capacitor, C, as it is discharged by the collector current of Q_3. As the voltage across C approaches the voltage at the emitter of Q_1, the transistor behaves less as an antilog element, and more as a linear resistance proportional to V_{be}/I_{REF}.

These attributes determine the detector circuit's response to complex waveforms, and directly affect the audibility of the compression process. Consider the following explanation: Humans respond to changes in audio signal level by perceiving volume as being proportional to the log of the acoustic power emitted by a source, thus the human listener perceives a source emitting 10 watts of "sound," (if the reader will permit such simplifications) to be roughly twice as loud as the same source emitting only 1 watt. This implies that one should be able to control audio levels logarithmically for a natural "sound" in the processed output. That is generally the case, but the principle does not extend, in a strict sense, to the control of a compressor.

If one accepts the premise that the most common uses of the audio compressor are to enhance the "loudness" of the processed material, or to "level" the apparent volume of the processed material, one should be aware of the effect of waveform complexity upon perceived loudness. A simple example is found in the case of a musician playing an instrument: when called upon to perform a solo, in order to "stand out" from the background music, the instrumentalist produces more complex sounds, in addition to producing sounds at a higher relative level. The increase in complexity provides a psychoacoustic "cue" which translates to the human listener as increased perceived loudness.

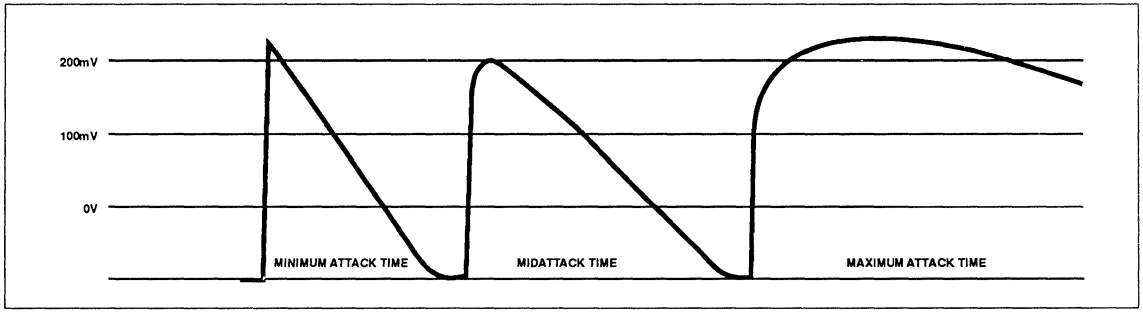

FIGURE 3: *Output Voltage Response of the Variable Time Constant Log of Average Integrator to a LF Square Wave Input*

During the compression process, if the detector circuitry produces a signal which calls for more gain reduction in response to the added harmonics in a sound which cause an increase in complexity, the gain control element will comply, thus making a solo instrumental exit the compressor at a lower level, foiling the intent of the performer. This is precisely what happens when using RMS detection – the detector circuit (correctly) assesses the increased complexity as an increase in sound energy, and calls for gain reduction.

The log averaging detector is relatively insensitive to increases in waveform complexity, and "ignores" the loudness cue thus provided. As a result, a complex waveform exits the compressor at a slightly higher level than it would if under the control of an rms detector. This rather unique "quirk" found in the log averaging process allows a solo instrumental or vocal to stand out in the processed signal, thus preserving the intent of the performer.

As a log averaging detector, the SSM-2110 exhibits remarkably little departure from an idealized log curve representing its input level throughout the entire range of the adjustable integration time, and offers superior performance to the equipment designer in this type of application. In addition, at higher input levels, the device does not compress the waveform at its output, thus under-reading the input value. In fact, the detector exhibits a gentle and quite predictable deviation from log conformity at high input current levels which results in the addition of a linear error term. This causes a slight over-reading of the input, and is quite useful for aficionados of "soft knee" limiting. It is unlikely that any real compressor design would require so wide a range of operation that this deviation might pose a problem (> 60 dB), but since the error term is so predictable and consistent, it can easily be corrected elsewhere in the control circuitry if necessary.

THE COMPRESSOR CONTROL CIRCUIT

Figure 4 illustrates a compressor control circuit incorporating the SSM-2110 as the detector element. Because the temperature compensation characteristics of the log recovery amplifier are not required in this application (control of a VCA having a complementary control sensitivity temperature coefficient) and to eliminate trimming of scale factor on a unit by unit basis, the log recovery amplifier is disabled by connecting its inputs to the IC's V_{REF} output. This step is necessary for proper operation of the IC when the log recovery amplifier is not used. The log recovery transistor is not used since offset is not a real concern in this circuit configuration.

The amplifier in the audio signal path, A_1, should be of a high quality, low noise type such as the SSM-2134. The remaining amplifiers may be general purpose types, preferably having FET input stages to minimize the effects of input bias currents on the accuracy of the multiplier circuits.

Amplifier A_2, and the SSM-2210 matched transistor pair Q_{1a}/Q_{1b} form the voltage-controlled current sink for the variable log averaging integrator. Amplifier A_4 boosts the output of the integrator to a usable level by increasing the nominal 6mV/dB scale factor of the signal at pin 2 to 1V/20dB, or 1V per decade. An offset corresponding to the change in voltage at pin 2 which results from varying the integration time is applied via R_{12}. Variable resistor VR_2 allows the adjustment of the compressor's rotation point, or that input level at which the output of A_4 will be 0V.

A pair of matching two-quadrant multipliers, which are configured using amplifiers A_6 and A_8 along with a four-transistor array Q_2 (MAT-04), allow adjustment of the compressor's ratio and adds sufficient gain as a function of both the threshold setting from VR_4 and A_9, and the ratio, as determined by VR_3 and A_5, to maintain the compressor's rotation point. Amplifier A_7 converts the current output of the ratio multiplier from Q_{2b} into a voltage which charges the holding capacitor C_8 via Q_{3a} to a voltage corresponding to the amount of gain reduction required of the VCA. Amplifier A_{12} converts the current output of the maintenance gain multiplier from Q_{2c} into a voltage corresponding to the quiescent gain required for the VCA to maintain the compressor rotation point, and adds or reduces gain at the VCA in response to the output gain control VR_7.

The release current sink is formed by amplifier A_{10}, and two sections of monolithic transistor array Q_3. Compensation for V_{be} of Q_{3a}, and for the quiescent change of voltage across C_8 caused by varying the release current through Q_{3c} are applied via R_{31} to A_7.

Amplifier A_9 and diode D_3 form a precision half-wave rectifier whose output is a positive voltage equal to the gain reduction signal. This point may also source a gain reduction indicator with intrinsic scaling of +1V = –20dB. Since metering is a matter of preference for the design engineer, no attempt has been made to include a gain reduction indicator as part of this circuit discussion.

Since it is possible for the inputs of both A_6 and A_8 to be negative voltages, it is wise to include germanium diodes D_1 and D_2 to prevent forward conduction of the internal base to emitter protective diodes in the MAT-04, thus eliminating the possibility of reverse leakage coupling between the multipliers. The existence of these diodes also prevents application of the MAT-04 as the charging transdiode Q_{3a}, since a voltage more negative than that across C_8 will frequently be present at the emitter of Q_{3a}.

Amplifier A_{13} outputs the algebraic sum of the various gain control signals for application to the compressor VCA section which will be described next.

Selection of the internal scale factor at 1V/decade, and inclusion of the –7.5V "math rail" are arbitrary choices made by the author in order to accommodate the use of the variable integrator, and to skew the control markings on the front panel controls, indicated by the enclosed names associated with those variable resistor potentiometers. Placing the rotation point, as determined by R_2, at the nominal operating line level, e.g., +4dB, etc., minimizes the effects of errors caused by the uncompensated temperature coefficient of the ratio multiplier, and any minor deviations in log conformity inherent in the detector circuitry or VCA sections of the compressor.

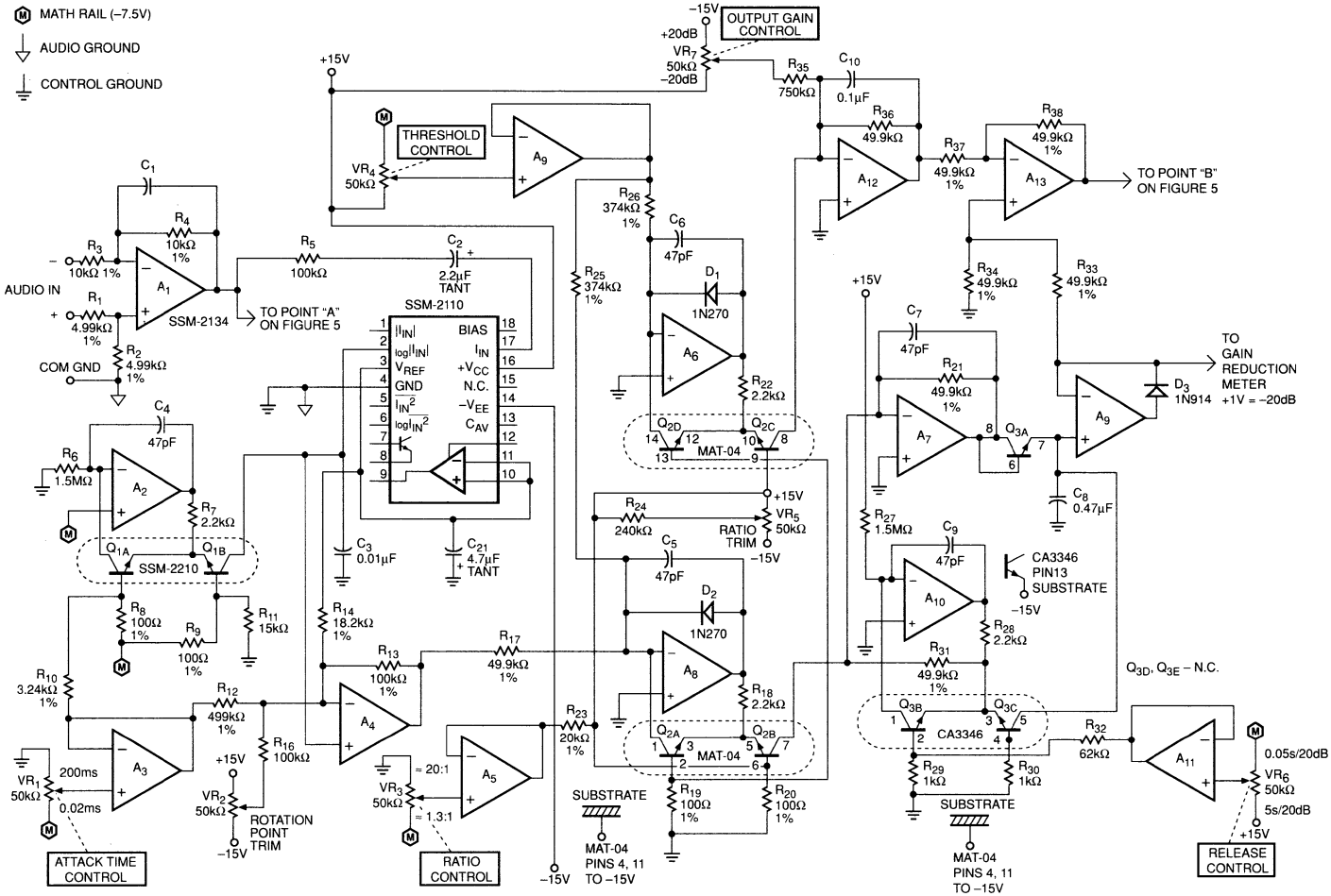

FIGURE 4: *Compressor Control Circuitry Schematic*

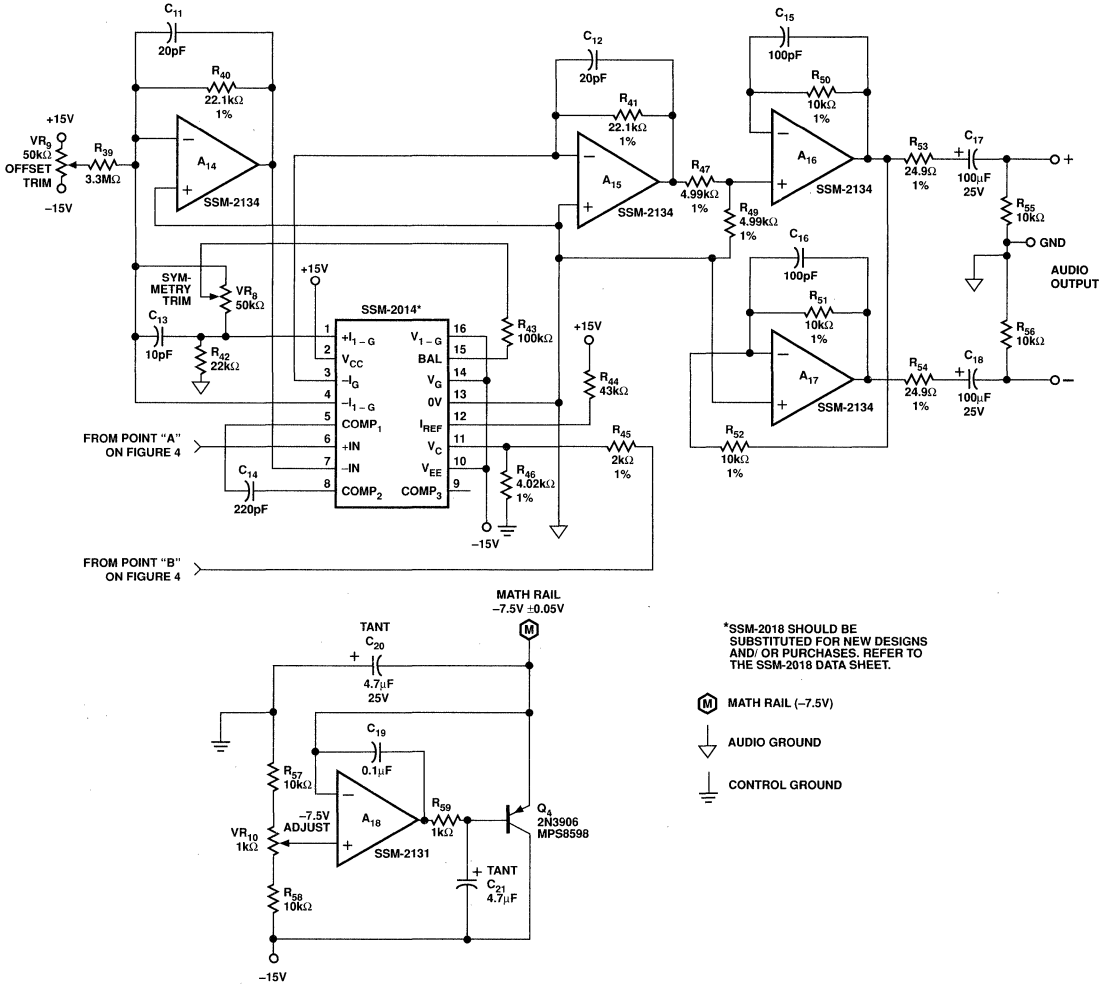

FIGURE 5: *VCA, Math Rail Regulator and Line Driver Schematic*

THE VCA SECTION

Figure 5 shows the VCA section of the compressor using the SSM-2014. The device is configured as an "outboard OVCE" in accordance with the literature supplied with the IC. Amplifiers A_{14}, A_{15}, A_{16}, and A_{17} should be high quality, low noise op amps such as the SSM-2134. A_{14} and A_{15} provide the necessary feedback and output buffers for this particular circuit. Resistive voltage divider R_{45}/R_{46} reduces the OVCE control port sensitivity to +1V/20dB attenuation to match the scale factor of the control circuitry. Variable resistor VR_8 is adjusted for lowest distortion products, preferrably at unity gain with a high level input. VR_9 is adjusted by applying a low frequency (<50Hz) signal at about $2V_{p\text{-}p}$ to pin 11, and setting for least low frequency output at A_{15} under a no-input signal or shorted-input condition. The stability of both these trims will be a welcomed surprise to the designer used to dealing with log/antilog VCAs.

A "quasi-balanced" line driver, consisting of A_{16}, A_{17}, and their associated passive components, completes the compressor

circuitry. The unit is capable of driving a 600Ω load at a sustained output level of +21dBm, and has a maximum output of +26dBm.

The SSM-2014 provides the designer a degree of flexibility in configuration which is not easily available using other VCA topologies. Chief among its attributes is the ability to select the operating bias current by applying current to a single port on the chip. This allows the user to select an operating point which is optimized for best noise performance vs. distortion for a given application.

In considering the normal operation of the compressor, the most common scenario is that the unit is used to "track" instruments or vocals. Of secondary, but no less important, concern is use for compressing mixed program material to enhance apparent loudness. In both applications, the trade-off between the residual noise floor and distortion at high-signal levels, both a function of operating bias, is somewhat arbitrary. Since it is likely that the dynamic distortion inherent in the compression process in normal operation would be at least equally as noticeable as moderate distortion at high-signal levels, the "intermediate" bias setting as described in the literature accompanying the device was chosen. This places the device bias at approximately 300μA, with a value of 43kΩ for R_{44}. As a result, the noise floor for the VCA circuit is –84dB (ref. $0.775V_{RMS}$) in a 20 kHz bandwidth at 0dB gain. The 1kHz THD+Noise measurements yielded figures consistent with the published data, and SMPTE IMD measurements disclosed worst-case distortion products in the 0.2% range, which is acceptable in all but the most critical applications. Should the designer wish to implement the sliding bias scheme, as described SSM-2014 data sheet, the output of the absolute value at pin 1 of the SSM-2110 (see Figure 4), or the rms computing loop (pin 5) may be used to drive a comparator with the appropriate time constants in order to switch to class A operation in the presence of high level inputs. In practice, this makes little difference in the transparency of the compressor in normal operation. Listening tests of the compressor demonstrated the smooth, precise control expected of the feedforward circuit topology. As the attack time (integration time) control is advanced from fast to slow settings, the low frequency content in mixed material becomes more solid and better defined, but the tendency to "squash" the lows is relatively absent at faster attack times as compared to other compressors having adjustable attack times with comparable settings.

The log averaging detector scheme really shines on vocals and horns, bringing a soloist "up-front" with moderate attack times. This is a noticeable difference when compared to any RMS-type compressor used for comparison in the listening tests.

ADJUSTING FOR BEST PERFORMANCE

As in any compressor or limiter whose ratio must be trimmed in its initial setup (see Figure 4, VR_5), the unit is sensitive to incorrect adjustment. One of the most distressing sounds which can be produced by a compressor is "over-compression," in which the control circuitry causes too much gain reduction at high ratios. For this reason, the compressor ratio trim should be set with the **Threshold** control at 0dB (0V at the wiper of VR_4), and with an input of +20dB, the trim should be adjusted so that with the **Attack**, **Release**, and **Output** gain controls centered, the maximum **Ratio** setting, fully clockwise, produces an output level equal to or slightly greater than the rotation point.

When laying out circuitry using the SSM-2014 and SSM-2110, care should be taken to keep traces to virtual grounds as short as possible, and a single point audio ground should be used. The control ground should connect to the audio ground at one point, pin 4 of the SSM-2110, and supply traces should be heavily decoupled with high quality capacitors. Traces carrying audio signal should be kept well away from control circuitry, and the detector IC and VCA should be located away from heat sources such as regulators or power supply transformers.

Since all parameter control is derived from DC levels produced by the front panel controls, high quality potentiometers need not be used. All the front panel control scales may be marked in equal intervals, and follow the antilog law, i.e., equal spacing per dB of gain or threshold setting, equal spacing per decade of attack and release times, etc. The sole exception is the ratio control, whose scale is skewed so that 2:1 appears near the middle of the control, as one normally would expect of a traditional feedback compressor.

The compressor control circuit described in this application note was configured using only four quad op amps in addition to the SSM-2110 and three matched transistor arrays. By providing the basic building blocks for an audio dynamic range processor in monolithic form, the SSM audio chip set greatly simplifies the implementation of an otherwise complex processor.

MEASURED PERFORMANCE:

SMPTE IMD @ Unity Gain, 0dBv in	0.009%
SMPTE IMD @ Unity Gain, +20dBv in	0.11%
SMPTE IMD @ 20dB Gain Reduction, 0dBv in	0.06%
SMPTE IMD @ 20dB Gain Reduction, +20dBv in	0.025%
Residual Noise and Hum @ Unity Gain, 20kHz BW	–84dBv
Maximum Output Level into 600Ω, Balanced	+21dBm
Maximum Input Level Before Clipping	+21dBv
Usable Dynamic Range, Unweighted in 20kHz BW	103dB
Threshold Range Ref. Rotation Point	–40 to +20dB
Useful Range of Rotation on Point Adj.	–10 to +4dBv
Nominal Attack (Integration) Time Range	0.02 to 200ms
Nominal Range of Ratio Adjustment	1.3:1 to 20:1
Range of Release Time Adjustment	0.05 to 5s/20dB
Range of Output Gain Adjustment	–20 to +20dB

NOTE: 0dBv refers to 0.775 V_{RMS}

ANALOG DEVICES

AN-136
APPLICATION NOTE

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An Ultra Low Noise Preamplifier

by M. Jachowski

Achieving the maximum usable dynamic range from low output level transducers such as audio microphones, magnetic pick-ups, or low impedance strain gauges requires a preamplifier with very low input-referred voltage noise. The circuit shown in Figure 1 has extremely low noise, 0.5nV/$\sqrt{Hz}$, and can provide a gain of 1000 over a 200kHz bandwidth.

This amplifier's low noise characteristics are attributable to the SSM-2220's matched PNP transistor pair. Operating with 2mA collector current in each transistor, the SSM-2220 forms a differential input stage with a DC gain of 385, approximately 50μV of offset voltage, and only 0.5nV/$\sqrt{Hz}$ of broadband noise. When multiplied by the stage gain of 385, the input noise of the SSM-2220 appears as 192.5nV/$\sqrt{Hz}$ differentially at the inputs of the OP-27. This makes the 3.8nV/$\sqrt{Hz}$ of the op amp an insignifi-cant contribution to the overall noise of the circuit. In this example, the input stage compensation, C_1 and R_7, optimizes noise performance over the audio frequency range by allowing the differential pair to have a flat frequency response to 20kHz before being rolled-off for stability criteria. Input stage gain is reduced 20dB from 20kHz to 200kHz and then remains constant until the SSM-2220's gain-bandwidth limit is reached at about 8MHz. This compensation ensures the preamplifier's stability for gains from 100 to over 2000. Gain is set with resistors R_5 and R_6 where $A_{VCL} = 1 + R_5/R_6$. To limit the thermal noise contributed by the feedback loop impedance, R_6 should be no more than 10Ω (a 10Ω resistor creates about 0.4nV/$\sqrt{Hz}$ at +25°C).

The input stage current, 4mA, is established by the current source of Q_2, R_1, and a GaAsP LED. The LED is used as a 1.6V "zener" whose temperature coefficient is nearly identical to that of Q_2's base-emitter junction. This produces a temperature stable 1V drop across R_1 forcing 4mA to flow from Q_2's collector. The 4mA splits to 2mA in each side of the differential pair. With $h_{fe} = 150$ in the SSM-2220, input bias current will be about 13μA. Because the bias current is relatively large, the offset voltage created as it flows through unbalanced source impedances will quickly surpass the differential pair's offset, making necessary the offset trim, R_8. Low source impedances will reduce the offset drift as h_{fe} changes over temperature.

A low source impedance is also critical to maintain a low overall input noise. The 0.5nV/ $\sqrt{Hz}$ noise of the SSM-2220 input is equivalent to the thermal noise of a 15Ω resistor at +25°C.

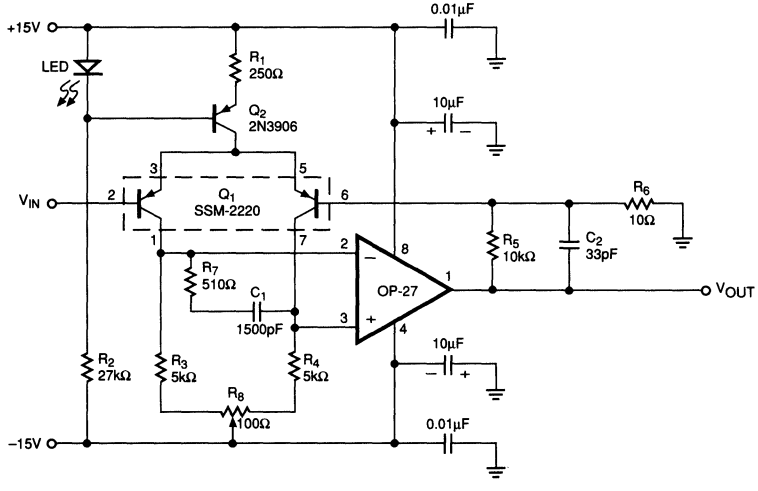

FIGURE 1: *This ultra low noise preamplifier shines new light on high-gain, low noise applications such as microphones, thermocouples, strain gauges, and magnetic pick-ups.*

Therefore, any transducer with a sourcing impedance greater than 15Ω will produce a noise which dominates that of the preamplifier. Figure 2 shows the total output noise of the preamplifier driven through a 10Ω source impedance. The analyzer displays total RMS noise voltage measured in a 0.03Hz bandwidth. The average broadband measurement is roughly 0.13μV on the vertical scale. Divided by the amplifier's closed-loop gain of 1000, this corresponds to 0.13nV at the preamp input, or expressed in nV/ $\sqrt{Hz}$,

$$e_n = \frac{0.13nV}{\sqrt{0.03Hz}} = 0.75nV/\sqrt{Hz}$$

Taking into account the noise of two 10Ω source resistors, the noise attributable to the SSM-2220 is then,

$$0.75nV/\sqrt{Hz} = \sqrt{(e_{SSM})^2 + (0.4nV/\sqrt{Hz})^2 + (0.4nV/\sqrt{Hz})^2}$$

$$e_{SSM} = 0.49nV/\sqrt{Hz}$$

The 1/f noise corner frequency is also remarkably low, only about 0.25Hz. In the 20kHz audio bandwidth, the total RMS input-referred noise voltage contributed by the SSM-2220 differential pair is,

$$e_n = (0.5nV/\sqrt{Hz})(\sqrt{20kHz - 20Hz}) = 70.5nV_{RMS}$$

The thermal noise of a 10Ω source impedance in the same bandwidth is,

$$e_t = 1.28 \times 10^{-10}\sqrt{(10\Omega)(20kHz - 20Hz)} = 57nV_{RMS}$$

The total input referred noise of the preamplifier with 10Ω source impedances on each input is,

$$e_{total} = \sqrt{(70.5nV)^2 + (57nV)^2 + (57nV)^2} + 106nV_{RMS}$$

This is lower than the thermal noise of a single 50Ω resistor over the same bandwidth, $126nV_{RMS}$.

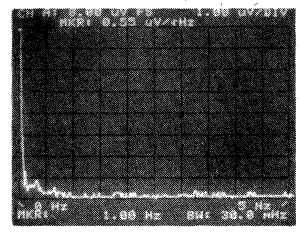

FIGURE 2: *The spectrum analyzer shows that, in a gain of 1000 with 10Ω source impedances, the SSM-2220 preamplifier has less than 0.5nV √Hz broadband noise and a 1/f noise corner of about 0.25Hz. Total harmonic distortion is less than 0.005% of a $10V_{p-p}$ signal from 20Hz to 20kHz.*

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Voltage Adjustment Applications of the DAC-8800 TrimDAC™ An Octal, 8-Bit D/A Converter

by Joe Buxton

The DAC-8800, a monolithic octal 8-bit digital-to-analog converter, is a digitally-controlled voltage adjustment device. The DAC's design makes it ideal for replacing trimming potentiometers in many applications. Not only does it replace potentiometers, but the DAC has many advantages over them, such as solid state reliability, very low drift over temperature and time, elimination of shifts due to vibrations, and automating the adjustment process. During manufacture of complex electrical systems, potentiometers must be manually adjusted taking considerable time and cost for labor, or expensive robotic systems must be developed for the same purpose. However, the DAC-8800 can automate the system's voltage adjustments so that a computer can now control the calibration.

This application note first describes the basic architecture and operating modes of the DAC-8800, including the reference input range limits, the load that the DAC places on the references, single supply operation, and serial interfacing. The last half of this note shows many basic circuits for using the DAC in a wide variety of applications, such as two wire interfaces and stand-alone operation for systems not based on digital controllers. Also included are techniques for adjusting the offset of operational amplifiers; using two DAC outputs together for coarse and fine control of a voltage; digitally changing the gain of a voltage-controlled amplifier; and trimming voltage references.

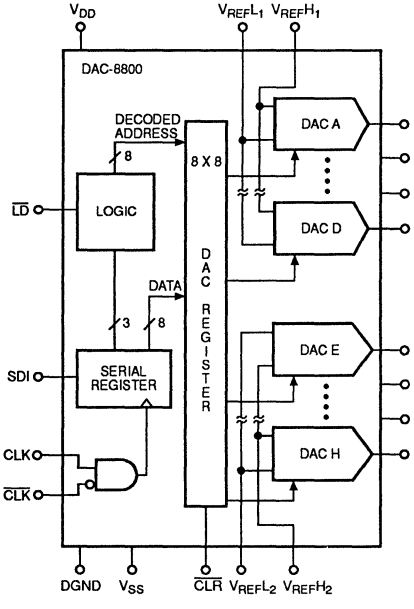

FIGURE 1: *DAC-8800 Block Diagram*

BASIC ARCHITECTURE

As the functional diagram shows in Figure 1, the DAC-8800 has eight individual DACs divided into two groups of four, each group having its own high and low reference inputs. Each DAC's output is independently controlled by a serial interface through which the 8-bit data word and 3-bit address are loaded.

Each of the DACs contains an R-2R ladder connected between the high and low reference inputs as shown in Figure 2. The output voltage is set by the position of the switches according to the formula below:

$$V_{OUT}(D) = D \times (V_{REF}H - V_{REF}L)/256 + V_{REF}L$$

where D is the digital code.

As this equation shows, the output can vary from $V_{REF}L$ to $V_{REF}H$ in 256 steps. It is significant that, while the output voltage can vary over this range, the DAC-8800's output impedance is always equal to a constant R_{OUT}, the characteristic resistance of the ladder. R_{OUT} is typically 12kΩ but can vary between 8kΩ and 16kΩ from device to device. The DAC's accuracy depends not on the absolute value of the ladder resistors but rather on the relative resistor matching. Thus, variations in output impedance do not

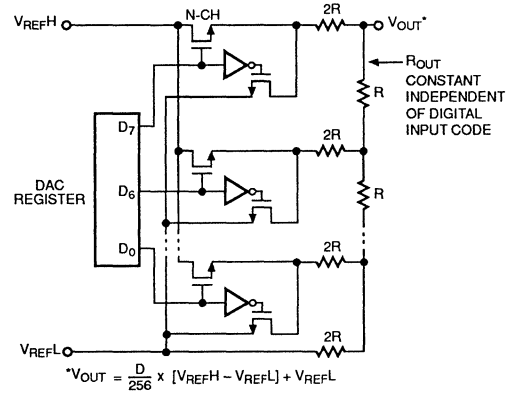

FIGURE 2: *DAC-8800 R-2R Ladder Network*

TrimDAC is a trademark of Analog Devices, Inc.

affect the linearity of the DAC. To easily understand the DAC, each output can be thought of as a Thevenin equivalent circuit of a voltage source in series with R_{OUT} as in Figure 3, where R_{OUT} is 12kΩ. The digital code then varies the voltage source between $V_{REF}L$ and $V_{REF}H$.

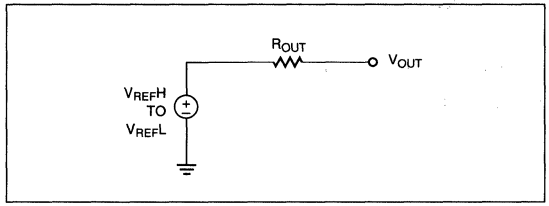

FIGURE 3: *Thevenin equivalent of each DAC output. R_{OUT} is typically 12kΩ.*

REFERENCE INPUT LIMITS

The switches in the R-2R ladder are N-channel enhancement MOSFETs with extremely low ON resistance. To ensure the DAC's linearity, the MOSFETs' gate-to-source voltage (V_{GS}) needs to be greater than the switches' intrinsic threshold voltage, which for the DAC-8800 is 2.5V. When the voltage falls below 2.5V the MOSFETs' ON resistance increases, which causes resistance mismatching in the R-2R ladder. Any mismatching degrades the precise R-2R ratios and thus decreases the linearity of the DAC.

In the DAC-8800, the gate-to-source voltage is equivalent to the voltage difference between V_{DD} and $V_{REF}H$, respectively. Figure 2 shows that $V_{REF}H$ is connected to the drain of the MOSFET switches, and, when the switches are on, the drain voltage is basically equivalent to the source voltage. The gate voltage is driven by CMOS logic, and when the switch is on, the logic connects the gate to V_{DD}. Thus, $V_{REF}H$ must be at least 2.5V below V_{DD}, as shown in Figure 3 of the DAC-8800's data sheet. However, to guarantee the data sheet error specifications over –55°C to +125°C, the gate-to-source voltage needs to be at least 4V. There is no similar limitation between the reference input and the negative supply, V_{SS}. Thus, the reference inputs can go to V_{SS}. An important note: because of internal protection diodes in the DAC, $V_{REF}L$ should not be allowed to go higher than $V_{REF}H$. Forward biasing these diodes allows large currents to flow between the two references, potentially resulting in permanent damage to the DAC-8800.

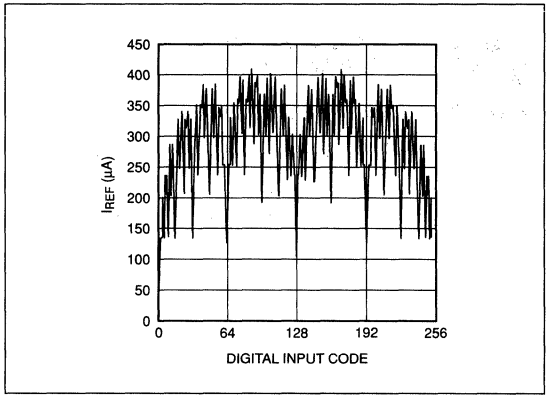

FIGURE 4: *$I_{REF}H$ variation versus digital code. One of four DACs connected to $V_{REF}H$. The other 3 DACs are loaded with zero code.*

REFERENCE INPUT CURRENT CHANGES WITH DIGITAL CODE

As the digital code changes, the resistance looking into the reference input changes significantly. Figure 4 shows the current demand into the $V_{REF}H$ pin as a function of the digital code for one of the four DACs referenced from that pin. This graph was generated with the following conditions: V_{DD} = +12V, V_{SS} = 0V, $V_{REF}H$ = +5V, and $V_{REF}L$ = 0V. As can be seen, the load on the reference varies from zero to 400µA. With all four DACs operating, the load current can go up to a maximum of 1.6mA. It is important to keep in mind that the current changes in abrupt steps. Thus, in applications where speed is important, any device driving the reference pin must be capable of handling these step current changes. A fast recovery op amp (such as the OP-42) or reference is recommended.

THE DAC-8800 CANNOT BE USED AS A VARIABLE RESISTOR

At first glance the DAC-8800 might appear to be ideal for use as a variable resistor from its output to $V_{REF}L$, where $V_{REF}L$ is tied to ground and $V_{REF}H$ left floating. However, its internal structure was not designed for this. The reason is twofold. First, the resistance from the DAC's output to $V_{REF}L$ does not vary linearly with

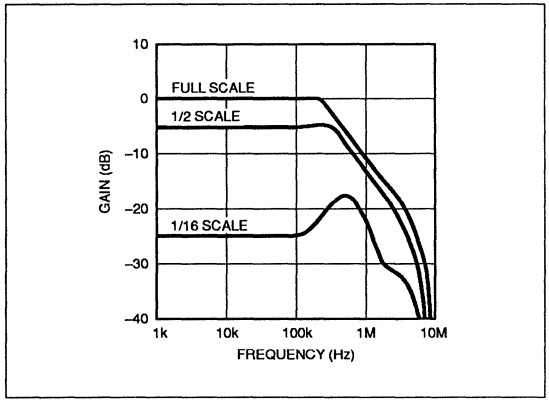

FIGURE 5: *DAC-8800 Bandwidth Under Different Gains*

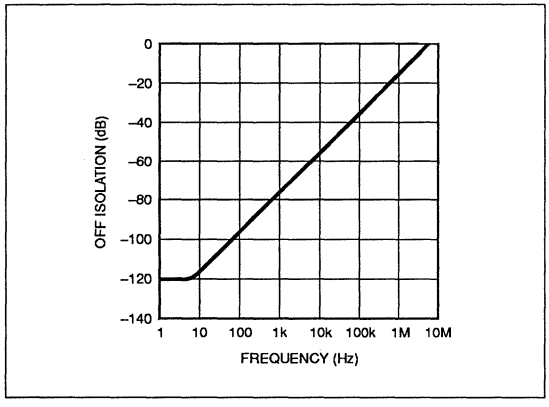

FIGURE 6: *DAC-8800 OFF Isolation*

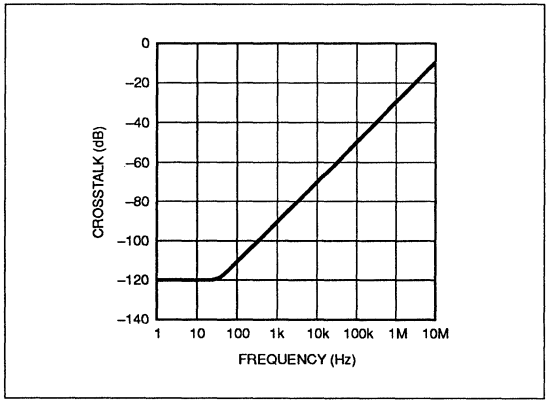

FIGURE 7: *DAC-8800 Crosstalk*

the digital code. Rather, it changes erratically, similar to the way the reference current changes in Figure 4. These seemingly random changes are due to various switches connected to $V_{REF}H$ turning on in binary fashion rather than sequentially and creating alternate current paths from the output to $V_{REF}L$.

Second, the NMOS switches are not bi-directional. In this variable resistor configuration, the switches connected to $V_{REF}H$ would actually have current flowing in reverse direction from the source to the drain. They maintain their low ON resistance only when current is flowing normally from the $V_{REF}H$ side (the drain) towards the output (the source). In backwards operation the source voltage causes changes in the ON resistance. Thus, any change of the voltage on the DAC's output will change the ON resistance and ultimately change the resistance to ground, even at the same digital code. Obviously, the DAC-8800 was designed to work as a voltage attenuator, and not as a variable resistor.

AC MULTIPLYING MODE OPERATION

The DAC-8800 is designed primarily as a DC adjustment device. However, it can also be used in multiplying mode by applying an AC signal to the reference input. In such applications, bandwidth, off-isolation, and crosstalk are important to the circuit's performance. The bandwidth of the DAC-8800 is limited by the ladder resistance and the internal capacitance, which are both specified in the data sheet. The typical resistance of 12kΩ, combined with the reference capacitance of 75pF, limits the bandwidth to 177kHz. Figure 5 shows actual network analyzer measurements of the –3dB bandwidth, which for this particular part occurs at 360kHz. The fact that the measured bandwidth is twice the typical points out how the bandwidth can vary due to varying capacitance and resistance from device to device. The worst case bandwidth is approximately 100kHz based on worst case resistor and capacitor values of 16kΩ and 100pF, respectively. Remember, as mentioned in the reference input limits section, $V_{REF}H$ cannot go below $V_{REF}L$. Any AC signal into $V_{REF}H$ must be biased to avoid this condition.

The off isolation of the DAC-8800, shown in Figure 6, was measured using an AC signal for $V_{REF}H$ and measuring an associated DAC output with all the bits off. The off isolation reveals how much of the input signal will feed through to the output. An interesting correlation can be made between this graph and the bandwidth graph of Figure 5, for the 1/16 scale measurement. The 1/16 scale shows a 10dB rise in the gain above 100kHz. This is actually due to the capacitive feedthrough of the DAC-8800.

The crosstalk versus frequency graph in Figure 7 was measured as the crosstalk from one set of four DACs to the other set of four DACs in the package. In other words, DACs A through D were set to full scale, and a frequency dependent signal was injected into their $V_{REF}H$ input. The crosstalk was then measured on the outputs of DACs E through H. The graph shows DC crosstalk of –120dB rising up to –50dB at 100kHz, revealing excellent performance for DC and low frequency AC signals.

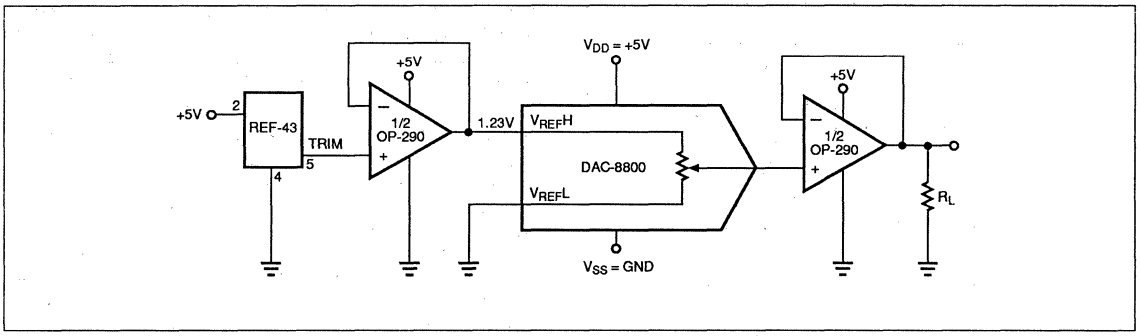

FIGURE 8: *DAC-8800 Single +5V Operation*

OUTPUT NOISE

The DAC-8800 exhibits basic broadband white noise of typically 18nV/$\sqrt{Hz}$. Its dominant noise source is the resistor ladder. Thus, the noise does not exhibit any measurable 1/f noise.

SINGLE +5V SUPPLY OPERATION OF THE DAC-8800

The DAC-8800 is ideal for single supply applications because its output range includes ground. In fact, the DAC-8800 can work well with a single +5V only. Even with this low of a supply voltage, $V_{REF}H$ can be connected to a 1.23V bandgap reference (Figure 8). Although the 1.23V bandgap reference violates the 4V of headroom requirement, the DAC is still within ±1/2 LSB of total unadjusted error. The 4V below the positive supply limit was set with a safety margin of about 0.5V to account for operation over the full operating temperature range.

The 1.23V bandgap reference voltage is derived from the TRIM pin of a precision 2.5V reference device, the REF-43. The buffer amplifier is needed because the TRIM pin's impedance is 50kΩ. The DAC-8800's reference inputs characteristically range from 12kΩ to 40kΩ depending on the digital code, which would load the trim pin excessively. The OP-290's low offset voltage of 75µV and low temperature drift characteristics maintain the reference's accuracy. The OP-290 also has the ability for its output to operate to ground with the addition of a load resistor; 10kΩ works well. The output amplifier is needed to buffer the DAC-8800's high output impedance when the output is connected to a low impedance load.

SERIAL INTERFACING

The digital control of the DAC-8800 is a standard three-wire serial interface with clock (CLK), load ($\overline{LD}$), and serial data input (SDI) (Figure 9). Additionally, an inverted $\overline{CLK}$ input pin is available for negative edge triggered data loading. Either CLK or $\overline{CLK}$ can also be used as a chip select pin. When loading data, 3 address bits are loaded, MSB first, followed by 8 bits of data, again MSB first. Thus 11 bits in all are loaded through the SDI pin to control each DAC. The DAC-8800 can run on a clock as fast as 6.6MHz making it possible to load all eight DACs in as little as 14 microseconds. Furthermore, the DAC-8800 maintains TTL compatibility for positive power supply voltages greater than or equal to +5V.

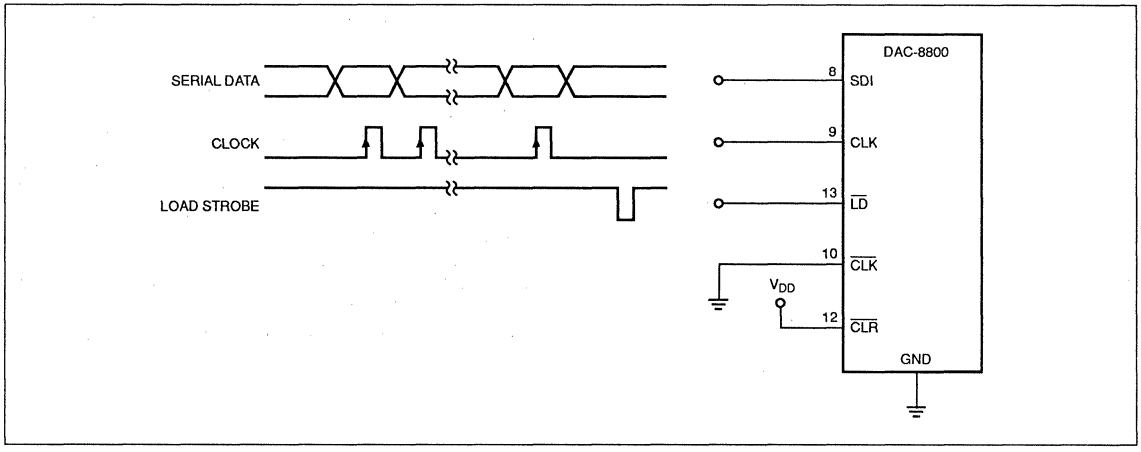

FIGURE 9: *DAC-8800 Serial Interfacing*

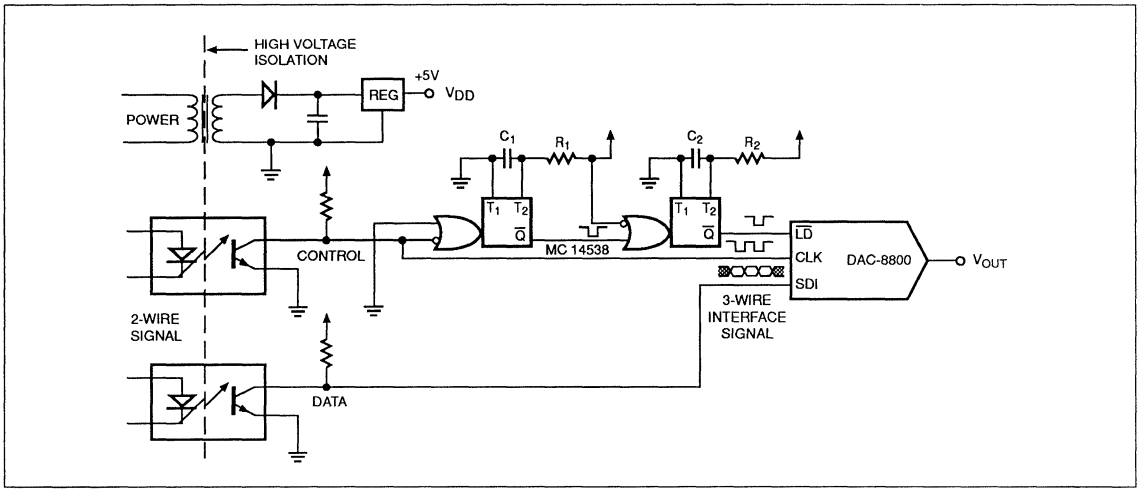

FIGURE 10: *Isolated Two-Wire Serial Interface for the DAC-8800*

TWO WIRE INTERFACES FOR PROCESS ENVIRONMENTS

High voltage isolation using opto-couplers is often necessary for serial interfaces found in process control applications. In these and other applications where minimizing the number of data lines is desirable, two-wire signal interfaces can be used (Figure 10). This simple circuit translates the two-wire interface into the three data lines required to load the DAC-8800. The $\overline{\text{LOAD}}$ signal is generated using two retriggerable one-shots. The first one-shot's timeout should be set longer than the clock period. Each succeeding clock pulse will retrigger the one-shot until all 11 bits are loaded into the DAC. Then the clock must pause long enough to allow the one-shot to time out. When the first one-shot's output goes low, it triggers the second one-shot, which produces the $\overline{\text{LOAD}}$ pulse, and finishes the loading cycle.

There are some common pitfalls when using one-shots. For example, the timeout set by the external resistor and capacitor can vary over temperature and from part to part. Even more significant is the variation due to resistor and capacitor tolerances. A typical capacitor can vary by ±10% which will cause an equivalent ±10% variation in the timing of the one-shot. To avoid the problems of one-shots, a second method using a counter is recommended (Figure 11a). The counter keeps track of the number of clock cycles and, when all the data has been input to the DAC, the external logic creates the $\overline{\text{LOAD}}$ pulse.

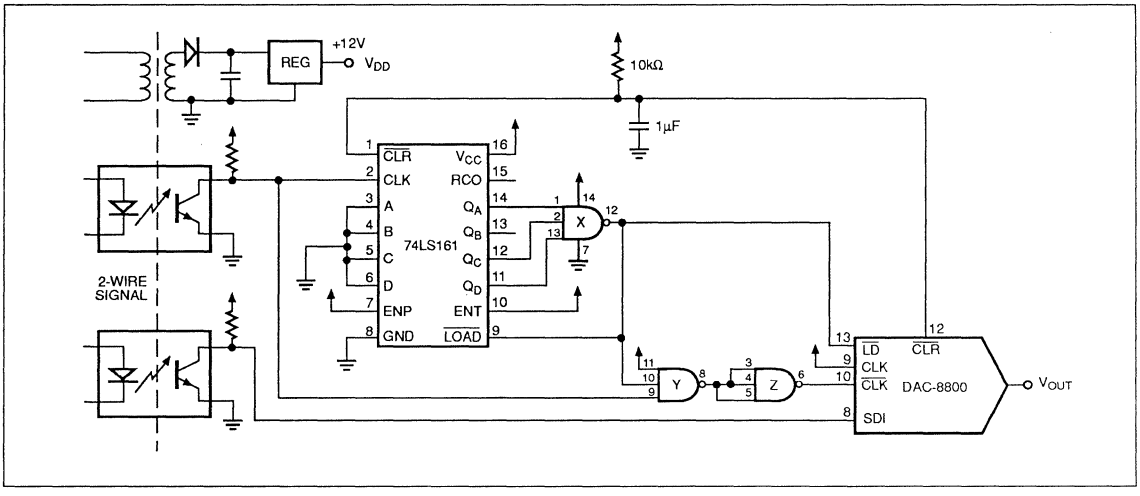

FIGURE 11a: *Isolated Two-Wire Serial Interface Using a Counter*

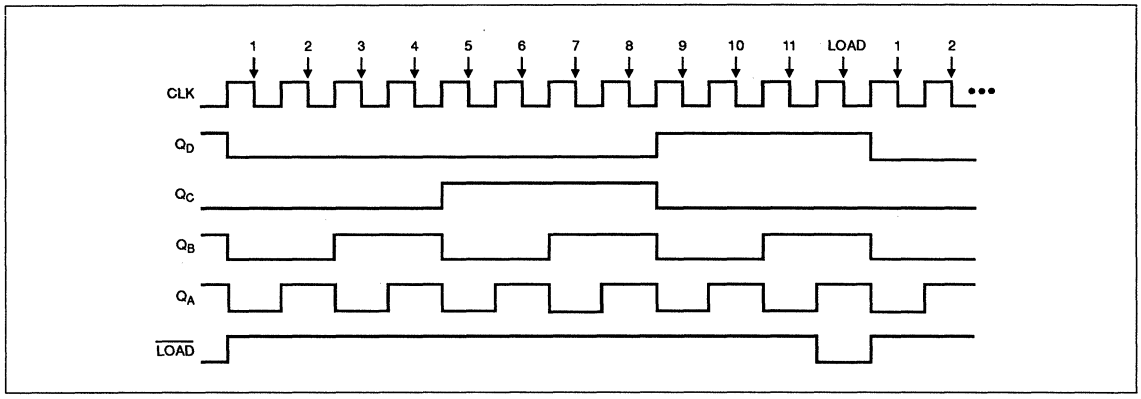

FIGURE 11b: *Isolated Two-wire Serial Interface Timing Diagram*

Referring to the timing diagram (see Figure 11b), the counter is incremented on every rising edge of the clock. Additionally, the data is loaded into the DAC-8800 on the falling edge of the clock by using the $\overline{CLK}$ input instead of the CLK input. The reason for using the $\overline{CLK}$ input becomes apparent after considering the $\overline{LOAD}$ pulse. The timing diagram shows that after the eleventh bit has been clocked, the output of the counter is binary 1010. On the following rising CLK edge the output of the counter changes to binary 1011, upon which NAND gate 'X' goes low to generate the $\overline{LOAD}$ pulse. The $\overline{LOAD}$ signal is connected to both the DAC's $\overline{LD}$ and the counter's $\overline{LOAD}$ pins. Since the counter has a synchronous clear, the $\overline{LOAD}$ pulse remains low until the next CLK pulse. NAND gates 'Y' and 'Z' prevent the twelfth falling CLK edge (labelled 'LOAD' in the timing diagram) from clocking the DAC, which would load false data into the DAC. Using the $\overline{CLK}$ input allows sufficient time from the CLK edge to the $\overline{LOAD}$ edge, and from the $\overline{LOAD}$ edge to the next CLK pulse, to satisfy the timing requirements for loading the DAC-8800.

After loading one address of the DAC, the entire process can be repeated to load another address. If the loading is complete then the CLK must stop after the twelfth pulse of the final load. The $\overline{CLK}$ input will be pulled high and the counter reset to zero. The timing requirements of the system are the same as for the DAC alone, and can be found in the DAC-8800's data sheet. Another feature of this circuit is the R and C on the CLR pins of both the DAC and the counter. This simple RC timing circuit will clear both chips upon system power-up. The 74LS161 was chosen because, like the DAC-8800, it has an asynchronous clear. The RC time constant should be set longer than the power supply turn-on time. The values shown in the circuit give a time constant of 10ms, which should be adequate for most systems. This same two-wire interface can be used for most three-input serial DACs.

STAND-ALONE OPERATION PROVIDING NONVOLATILE SETTINGS

Whenever a system with a DAC-8800 is powered on, the DAC-8800 needs to have all eight of its data words loaded to set the proper DC output voltages. In a system with a microprocessor or microcontroller, this is a straightforward operation. However, in some systems the DAC-8800 may be the only part with a digital interface. In this case, the circuit shown in Figure 12a will automatically load the DAC on system power-up. The core of the circuit is a serial input/output EEPROM device (U_2), preprogrammed with the appropriate data for the DAC. The counter labelled U_4 counts through 8 addresses, which are serially shifted into the EEPROM by U_3, a parallel to serial shift register. The EEPROM shifts out a 16-bit word associated with each address. Only 11 of the 16 bits are actually shifted into the DAC before the $\overline{LOAD}$ pulse arrives.

The second counter, U_7, in combination with the flip-flop U_6, counts the loading of the bits into the EEPROM and into the DAC-8800. When all the bits are loaded the logic sends a $\overline{LOAD}$ pulse which loads the DAC and increments the address on U_4. The timing diagram in Figure 12b gives a detailed description of the loading of one address. The CLK INH logic inhibits the shift register during certain CLK pulses because 9 bits need to be loaded into the EEPROM and only 8 bits are available in the register.

When the system is powered-up, R_1 and C_1 create a $\overline{PWRUP}$ pulse to asynchronously clear all of the counters and the DAC. After the $\overline{PWRUP}$ pulse goes high, the free running clock begins to load all 8 addresses. After the eighth address is loaded, the clock is disabled to remove any digital switching noise in the analog circuitry.

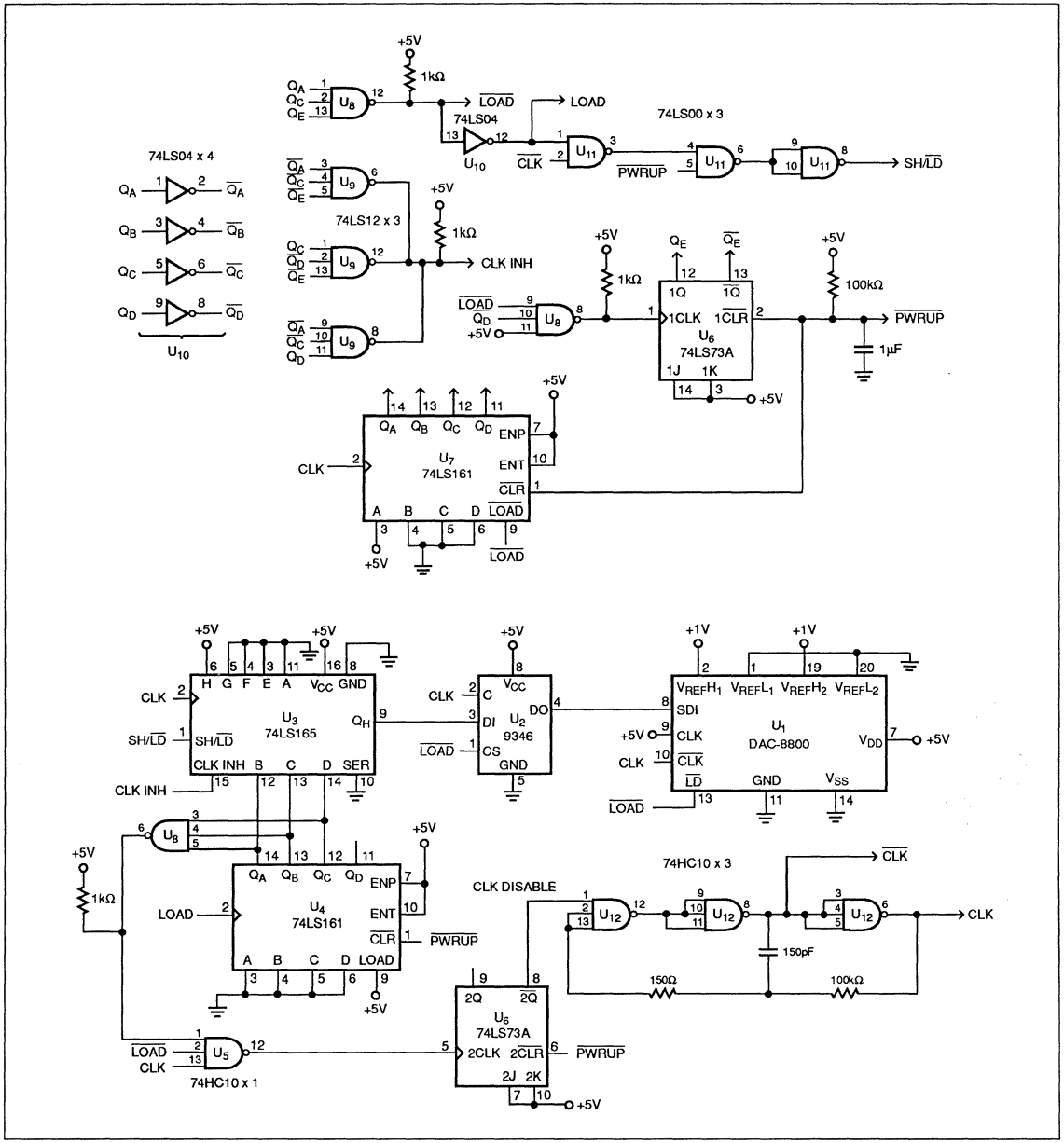

FIGURE 12a: *Stand-alone operation of the DAC-8800. The EEPROM stores data to set the DAC's output voltages on system power-up.*

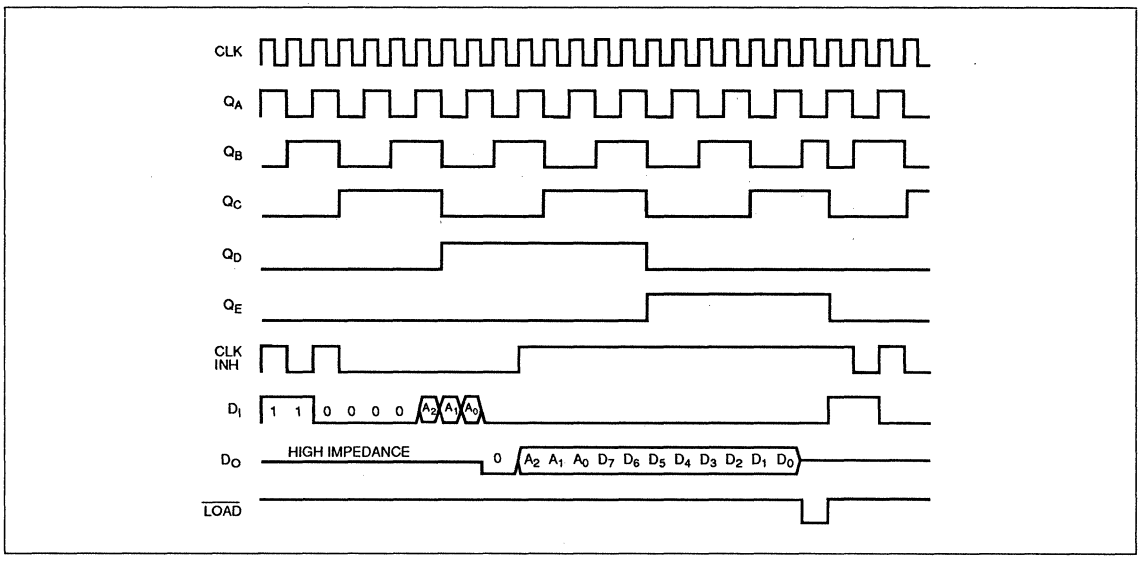

FIGURE 12b: *Stand-Alone Operation Timing Diagram*

DAC-8800 TEST FIXTURE

Figure 13 shows a fixture to test the DAC-8800. The circuit includes switches to set the address and data so that each DAC can be loaded with any digital word. After the switches are set, pressing the push-button activates the monostable multivibrator which generates the clock signal to load the DAC register. The counter selects the successive MUX channels, which switch the bits in proper loading order. After all eleven bits are loaded, the $\overline{LOAD}$ switch is manually toggled to generate a $\overline{LOAD}$ pulse. The $\overline{CLR}$ switch should be high at all times except to clear all eight DACs, in which case $\overline{CLR}$ needs to be switched low and then back to high. The CS switch should always be set low to keep the DAC selected at all times. The DAC-8800's outputs are buffered by OP-400 operational amplifiers; however, the outputs can be configured many different ways for the actual tests required.

CONDITIONS TO AVOID IN USING THE DAC-8800

The DAC-8800 is very resistant to the most common latch-up conditions.[1] For example, it does not latch-up when the digital inputs go high before the DAC is powered up. Nor is the DAC's own power supply sequencing significant. However, a few conditions still exist that are potentially destructive. In order to prevent damage from latch-up and ESD, the internal DAC-8800 design includes large body diodes placed from many of the pins to ground or either of the supplies, as shown in Figure 14. Looking at the placement of the diodes, it is easy to understand what conditions need to be avoided. The voltage across these diodes should be less than 0.3V, or they will start to turn on.

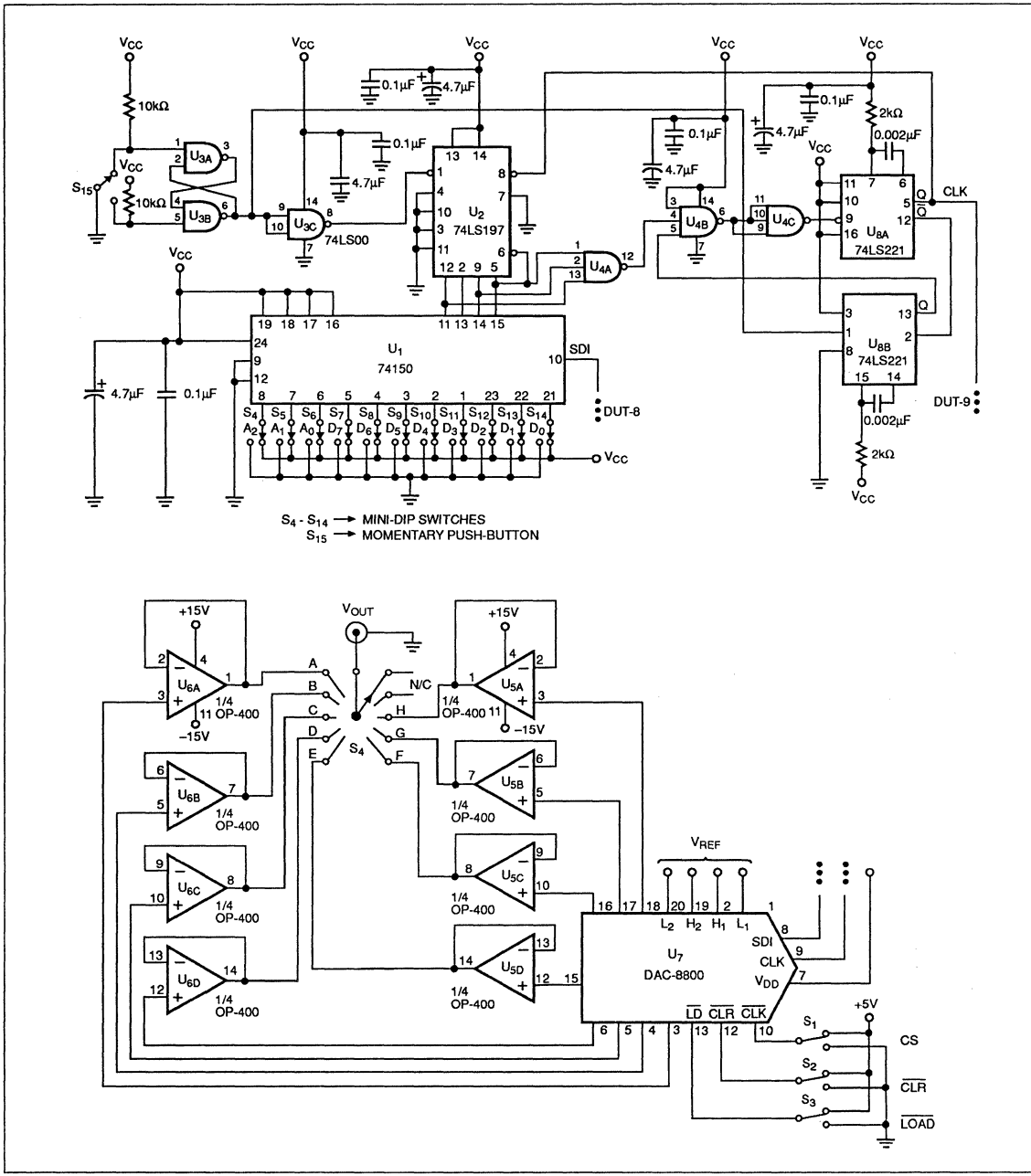

FIGURE 13: *DAC-8800 Test Fixture*

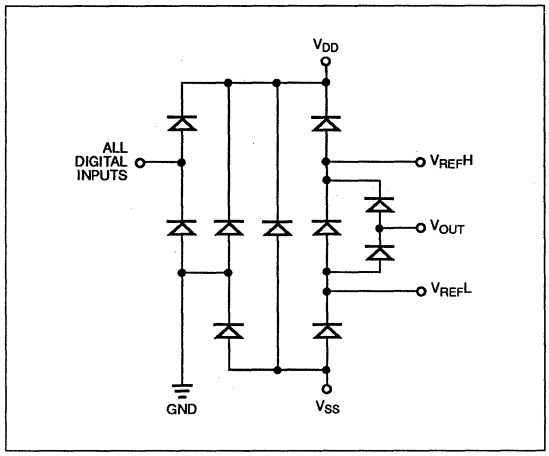

FIGURE 14: *Diagram of diodes in the DAC-8800 designed for ESD protection and latch-up prevention.*

Even if one of the diodes does turn on the condition is not necessarily destructive. For example, the diodes from the digital inputs to V_{DD}, and from ground to the inputs, were made large enough to handle in excess of 200mA of current without being damaged. All the other diodes can handle at least 100mA. Thus, if there is any chance of any of the diodes forward biasing, the pin should be current limited. In the case of the digital inputs, a small series resistor can easily prevent more than 200mA from flowing.

APPLICATION CIRCUIT COLLECTION FOR THE DAC-8800

The DAC-8800 can be used for a wide variety of DC adjustment applications. The main point that needs to be remembered is that the DAC-8800 output is basically a voltage source with a 12kΩ output impedance. Thus, a high impedance load can be directly connected to the DAC's output, however with a low impedance load, the DAC's output may need to be buffered.

Figure 15 suggests numerous basic trimming operations that the DAC-8800 can be used for. Setting comparator trip points is a prime example of using the DAC-8800 to directly drive a high impedance load. The comparator's trip point can be digitally altered for different signal conditions. Another example of a high impedance load is controlling the gain of a video Voltage Controlled Amplifier (VCA) by altering the collector current through the differential pair. The DAC-8800 adjusts the base voltage of the current source transistor thus changing the collector currents. This in turn changes the transconductance of the differential pair transistors, which directly changes the gain.

DIGITALLY-CONTROLLED VCA

The DAC-8800 can also be used in audio systems to control the gain of a low distortion audio VCA such as the SSM-2014 (Figure 16). The SSM-2014 has over 100dB of dynamic range, and its gain is logarithmically proportional to the control voltage, V_C. The DAC can be connected directly to the control port of the VCA, which has a gain sensitivity of –30mV/dB. A reference range from

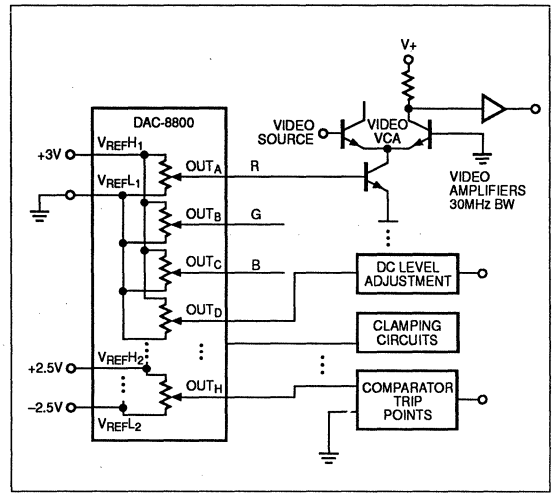

FIGURE 15: *Typical DC Adjustments Using the DAC-8800*

+2.5V to –1.2V will give a gain range of –80dB to +40dB, and the SSM-2014 maintains flat gain and phase response to well above the audio frequency range of 20kHz for all gains. The circuit has a typical control feedthrough of 1.3mV/V at 100Hz. To minimize this effect, capacitor C_S is used to slow down the DAC transitions. Using 1.0µF gives a pole at 13Hz, which will filter out most of the glitch energy and any high frequency noise.

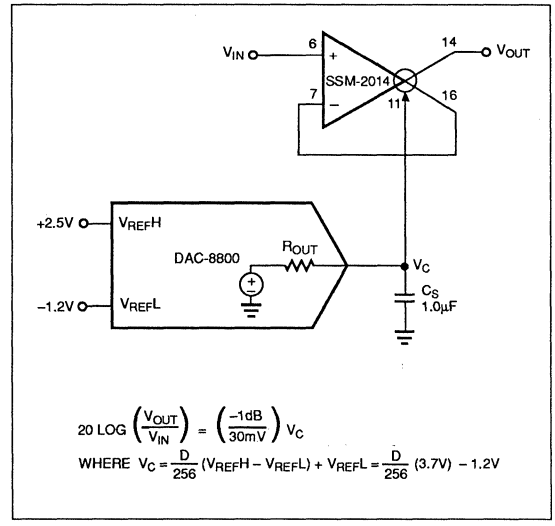

FIGURE 16: *Digital Gain Control Using a Voltage-Controlled Amplifier*

TRIMMING OP AMP OFFSET VOLTAGE

A frequently encountered DC adjustment application is trimming op amp offsets. There are many straightforward methods for trimming; one of which is connecting the DAC-8800 to the op amp's null pins. The DAC-8800 can directly null op amps to the negative supply, provided the supply is −12V or less in magnitude (Figure 17). This limit is because of the maximum 20V limit across the DAC. Since the positive supply needs to be at least +5V for logic interfacing, the DAC-8800's negative supply is safe to around −12V. The references used need to be near the voltage of the op amp's trim pins, which is typically a couple hundred millivolts above the negative rail. The figure shows reference values that work well for trimming the OP-42 over a ±40mV range. The actual voltages can be created using resistor dividers from the negative supply to ground and buffering the reference inputs with op amps. In cases where the op amp is adjusted from the positive rail, one of the alternative methods in the following paragraphs is needed. The reason for this is that the DAC-8800's output would need to be able to go up to the positive supply. However, $V_{REF}H$ is limited to 4V below the positive supply. Thus, the offset cannot be directly adjusted around the positive supply.

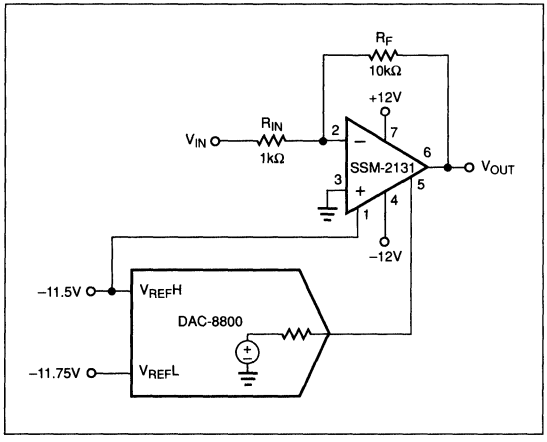

FIGURE 17: *Using the DAC-8800 for offset nulling directly on the op amp's null pins.*

A simpler method of offset nulling that gets around the supply voltage limitation is to connect the DAC-8800's output in series with a resistor to the summing node of the amplifier (Figure 18). This adds a small current that cancels the op amp's offset voltage. The series resistor should be large to provide a fine adjustment. The noise of the DAC and the series resistor might at first appear to be a problem, but it is actually attenuated by the 1kΩ input resistor. Therefore, the 1kΩ noise dominates. For the values in Figure 18, the adjustment range is ±50mV on the output. Figure

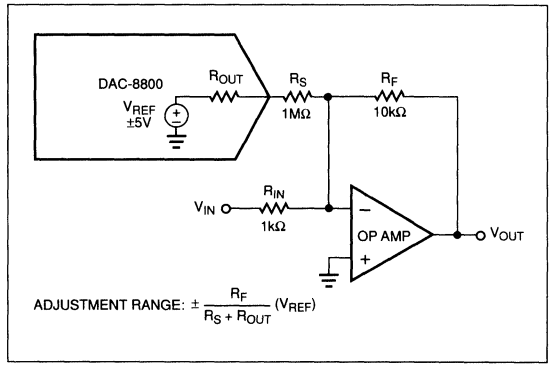

FIGURE 18: *Offset nulling by connecting the DAC-8800 to the summing node of an amplifier.*

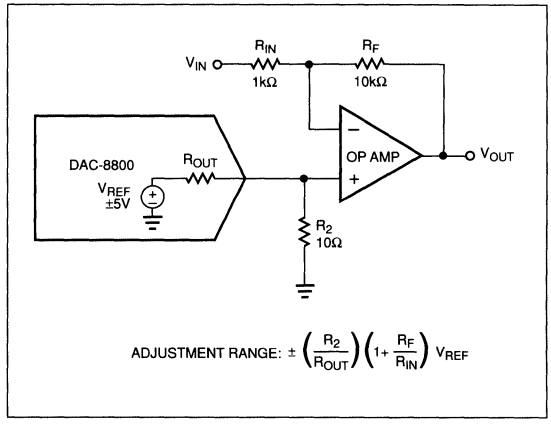

FIGURE 19: *Offset nulling by connecting the DAC-8800 to the noninverting node of an amplifier.*

19 shows an alternative method of offset nulling by adjusting the voltage at the amplifier's noninverting input. The resistor divider is recommended to provide for fine control of the offset. The adjustment range for the values in Figure 19 is ±42mV. The small resistor-to-ground also reduces the DAC's output noise to a point where it is insignificant compared to the op amp's own noise. With R_2 = 10Ω, the input noise caused by the DAC reduces to 15pV/$\sqrt{Hz}$; the noise of R_2 is much larger than this.

In both nulling applications shown, a positive and negative reference is required; however, in certain systems, only one reference may be available. Thus, the DAC-8800 can only adjust the offset in one direction. If this is the case, the amplifier can be forced to offset in either the positive or negative direction by connecting

one of the offset pins to the appropriate power supply voltage. Then the offset only needs to be adjusted in one direction, which the DAC-8800 can easily do with just one reference. Typical op amps have V_{OS} adjustment ranges on the order of ±5mV. Thus, the adjustment range of the DAC-8800 needs only to adjust the input offset by 10mV.

If the op amp is forced to offset in only one direction, the temperature coefficient of V_{OS} (TCV_{OS}) will almost certainly be affected. For a typical op amp, TCV_{OS} is directly proportional to the offset voltage. Thus, if the offset voltage is larger to start with, then TCV_{OS} will also be larger. For example, an op amp with a simple NPN input stage will exhibit a TCV_{OS} equal to V_{OS} divided by the temperature in degrees Kelvin at which that offset was measured. This translates to approximately 3µV/°C of TCV_{OS} for every millivolt of V_{OS}.

TRIMMING VOLTAGE REFERENCES

Figure 20 shows the DAC-8800 being used to trim a voltage reference such as PMI's REF-01. The output of the DAC is connected to the TRIM pin of the reference just as the wiper of a potentiometer would be connected. This entire circuit can easily be used in single supply applications because the DAC-8800's output can go to V_{SS}. Furthermore, this method can be used for all of PMI's references provided there is at least 4V of headroom between V_{DD} and V_{OUT}. The adjustment range of this circuit is the same as the ±300mV specified in the REF-01's data sheet.

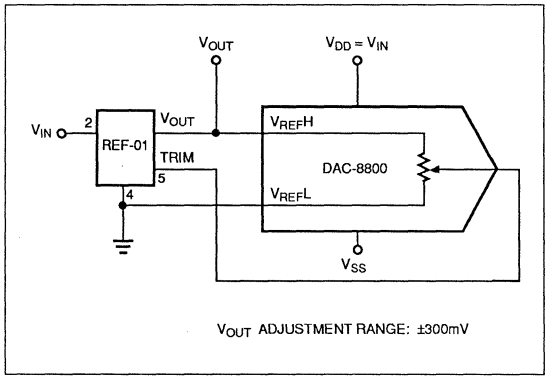

FIGURE 20: *Reference Trimming Using the DAC-8800*

COARSE-FINE CONTROL

Two of the DAC-8800's outputs can be connected together, and the resulting output is the average of the two unconnected outputs (Figure 21). This can easily be seen by thinking of the Thevenin equivalent circuit in Figure 3. The two output resistances in the same package are well matched so they form an accurate resistive divider, which averages the two DAC voltages. Such a circuit could be useful for performing a coarse-fine control, where one of the references is set to 1/10 the other reference. For example, setting $V_{REF}H_1$ to 1.0V, $V_{REF}L_1$ to –1.0V, $V_{REF}H_2$ to 100mV, and $V_{REF}L_2$ to –100mV gives an output adjustment range of ±0.5V ±0.05V.

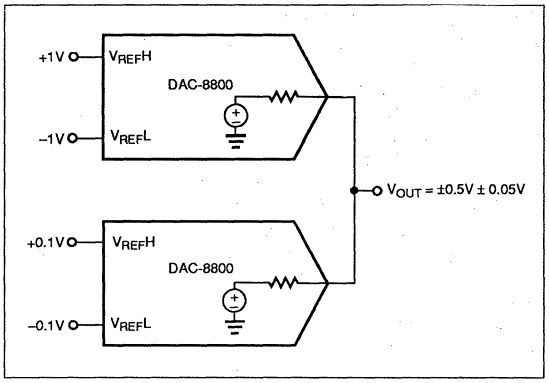

FIGURE 21: *Coarse-Fine Control by Averaging the DAC-8800 Outputs*

This application is limited by the voltage difference between the references. If $V_{REF}1$ is too much larger than $V_{REF}2$, the output voltage goes above $V_{REF}2$, and the switches in $V_{REF}2$ start to turn on independent of the digital code, which causes a significant error. It can even cause $V_{REF}2$ to increase by forcing current back into the reference, causing nonlinearities. The actual threshold for the switches turning on varies depending upon the common mode voltage of the two references, but the worst case is 1.5V between $V_{REF}1$ and $V_{REF}2$. Thus, the above example with $V_{REF}H_1$ = 1.0V and $V_{REF}H_2$ = 100mV works well, but increasing $V_{REF}H_1$ above 1.6V may cause the switches to start turning on. For unipolar applications, this problem can be avoided by connecting both the high references to ground and setting the low references to, for example, –10.0V and –1.0V. Configured this way, the output can never go above the high reference, and the switches will never turn on independent of digital code.

An alternative method that avoids the aforementioned problem is shown in Figure 22. Using this method, the output voltage can never be greater in magnitude than any of the references. To get the maximum output voltage, set both V_1 and V_2 to $V_{REF}H$, then the equation simplifies as follows:

$$V_O = V_{REF}H\,[\,(2R_{OUT} + R_S) / (2R_{OUT} + R_S)\,] = V_{REF}H$$

Thus, the maximum output voltage is equal to the reference of the DACs. Another advantage is that only half as many references are needed. One thing to be careful of is that the percentage adjustment range of each DAC output will vary with changing output resistances from device to device. In Figure 22, with R_{OUT} = 12kΩ, R_S = 96kΩ sets the output to be 10% of V_1 and 90% of V_2. However, if R_{OUT} changes to 8kΩ, then the percentages become 7% and 93%, respectively. If this is unacceptable, then R_S needs to be variable from at least 64kΩ to 128kΩ to cover the entire output resistance range of the DAC.

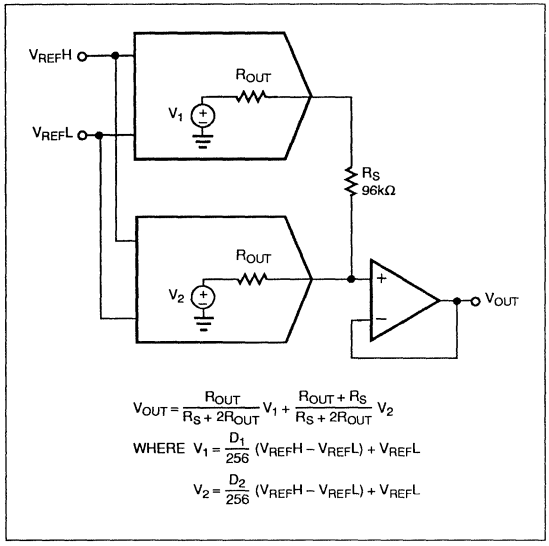

FIGURE 22: *Course-fine adjustment using the same reference for both DACs.*

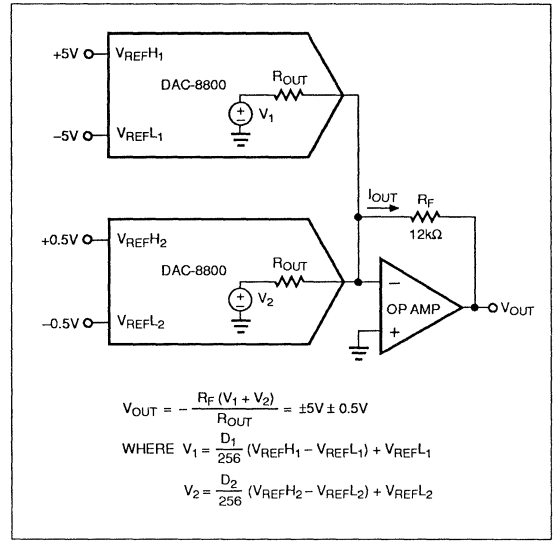

FIGURE 23: *Voltage summer by connecting the DAC-8800 outputs to the summing node of an amplifier.*

Another method, shown in Figure 23, is current summing. In this case, the DAC outputs are connected to the virtual ground of the op amp, avoiding the problem of the switches being forced on. The feedback resistor should be 12kΩ to match the output impedance of the DAC-8800. As in the above application, the feedback resistor may need to be varied from 8kΩ to 16kΩ depending on variations in the DAC-8800's output resistance. Also remember that the op amp inverts the DAC's reference voltages, so a 5V high reference gives –5V at the output of the op amp.

AN ADJUSTABLE REFERENCE FOR ANALOG-TO-DIGITAL CONVERTERS

In an analog-to-digital conversion circuit the DAC-8800 works well as a digitally-controlled reference (Figure 24). Using the DAC, the reference voltage can be adjusted for different ADC sensitivities. The DAC-8800 output may need to be buffered by an op amp because of the typical ADC's low reference input impedance. For flash converters the typical input impedance is usually well below 1kΩ, which is much too low for the DAC-8800's output impedance of 12kΩ. A separate DAC in the same package can provide the negative reference as well, but it too has to be buffered with an op amp.

As can be seen by the many different application circuits shown in the above section, the DAC-8800 is a very versatile device. Of course, the application examples shown here are only a small selection of the many different ways the DAC-8800 can be used.

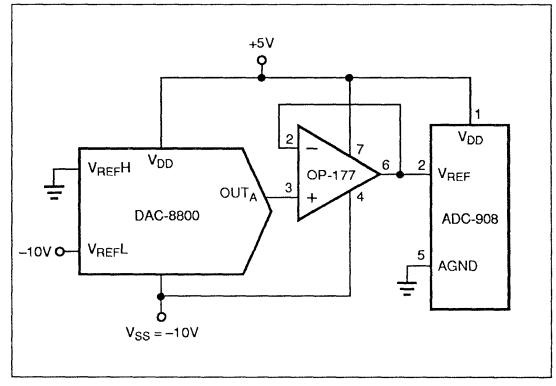

FIGURE 24: *The DAC-8800 as a digitally-controlled variable reference for ADCs. The DAC's output needs to be buffered by an op amp.*

References:

(1) *AN-109, Understanding and Preventing Latch-up in CMOS DACs,* Precision Monolithics Inc., January 1989.

ANALOG DEVICES

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How to Test Basic Operational Amplifier Parameters

THE REAL OP AMP

Input Imperfections

The characteristics of op amps are, of course, considerably more complicated than can be shown in Figure 1. The real op amp has a number of sources of error which must be tested independently to determine the true quality of the device. The active errors at the input can be modeled as a dc current source (I_B) and a series dc voltage source (V_{OS}). An impedance (Z_{IN} Diff) appears between the inputs, and another (Z_{INCM}) appears between the inputs and ground. These impedances usually consist of a resistance and capacitance in parallel, and the finite Z_{CM} will introduce errors due to common-mode input voltages.

There are two additional input error sources. In addition to the dc voltage and current sources, small ac sources representing the noise components must be included in the model.

Output Obstacles

The output side of the model is also nonideal. First, an output impedance, R_O, is added in series with the voltage source. The "A" term (infinite in the ideal model) is both finite and a function of frequency in a real amplifier A'(s). It is also obvious that the output voltage and current capabilities of a real op amp are bounded.

The real amplifier, thus, can be modeled as shown below.

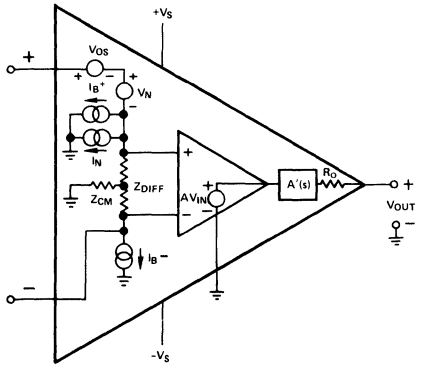

Figure 1. Real Op Amp

OP AMP SPECIFICATIONS

Offset Voltage

Each of these nonideal specifications should be examined in some detail. Consider first the dc errors. Offset voltage is the result of a mismatch in the base-emitter voltages of the differential input transistors (or gate-source voltage mismatch in FET-input amplifiers). This offset voltage is indistinguishable from an input signal as far as the amplifier is concerned. Usually this offset can be trimmed to zero by the user by means of an external potentiometer, which adjusts the balance of the operating currents in the input stage until the $V_{BE'S}$ (or $V_{GS'S}$) are equal. Of course, this trim will be effective only at one temperature, since offset voltage changes as a function of temperature.

Many circuits exist for testing offset voltage. If V_{OS} is redefined as the voltage at the op amp input which will drive the output to zero in an open-loop circuit, a servo loop can be built around the device under test to determine that voltage. In the circuit shown below, a second amplifier is used to provide feedback. This feedback amplifier must have very high gain and low offset. In operation, the control voltage, V_C, is set to zero. This forces the output of the device under test (D.U.T.) to also go to zero, because no dc current can flow through the amplifier's feedback capacitor. Since the output of the D.U.T. will only go to zero when a voltage equal to its input offset voltage is applied to its input, then V_A must equal V_{OS}. Thus, the output of the feedback amplifier is equal to $V_{OS} \times (1 + R_F/100\Omega)$.

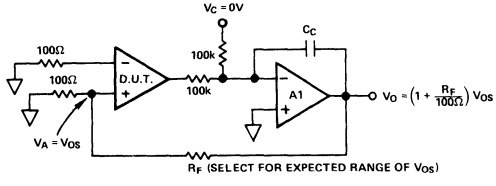

Figure 2. Op Amp Offset Voltage Test Circuit

An alternate method for offset voltage measurement can also be used. This alternate circuit is simpler to build and is only slightly less accurate. If it is assumed that V_{OS} can

be modeled as a source connected in series with one input, configuring the amplifier for a fairly high closed-loop gain will allow reasonably accurate measurement of offset voltage with an inexpensive voltmeter.

In order to maintain accuracy in this measurement, R_{IN} should be low enough that I_{OS} flowing through R_{IN} is at least ten times lower than the expected value of V_{OS}. R_C causes an equal voltage to be developed at each input due to I_B. This common-mode voltage effect can be neglected due to the common mode rejection of the op amp. Reasonable values for R_{IN}, R_C, and R_{FB} are 100Ω, 100Ω, and 9.9kΩ, respectively.

Another error arises in this circuit due to the finite open loop gain of the amplifier. Assuming a test circuit gain of 100, the amplifier must have a dc open-loop gain of at least 10,000 for a 1% accurate V_{OS} measurement.

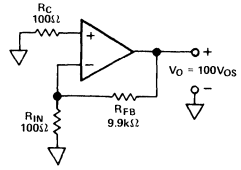

Figure 3. Simple V_{OS} Test Circuit

Input Bias Current

Another dc error term is the input bias current. As a consequence of the practical characteristics of transistors, base current must be supplied to the input transistors to bias them into their active operating region. This current must also return to its originating point through some dc path. Thus operational amplifiers cannot be used with input signal sources which are not referred to the same power source as the amplifier. It is possible to reduce bias current-induced errors by providing a source (other than the signal path) which can leak this current.

In many applications, the errors due to bias current are actually less annoying than the errors caused by the mismatch of the bias circuits of the two inputs. This difference between the bias currents is called the input offset current, and is usually specified along with the bias current.

Input currents, like input offset voltage, vary as a function of temperature. In the case of a bipolar-input amplifier, bias current decreases at elevated temperature. This is because the transistors' β increases, and since the emitter current is constant, the base current decreases. In the case of a FET-input amplifier, the bias current is due to JFET gate leakage, which is in reality a reverse-biased junction leakage current. Such currents have the characteristic of doubling for every 10°C rise in junction temperature.

It is important to consider the test conditions under which bias current is specified, particularly in the case of a FET-input op amp. Some manufacturers specify bias current at a junction temperature of 25°C. This corresponds roughly to the bias current immediately after power is applied to the amplifier. Unfortunately most circuits are not operated in a pulsed mode, and the effects of component self-heating must be considered. This effect is, in many cases, not trivial. For example, an amplifier which draws 5mA of supply current from ±15V supplies dissipates 150mW. The thermal resistance from junction to ambient for an 8-lead IC package is typically 150°C/W. This means that the junction temperature of the amplifier in question will be 22.5°C above ambient temperature, and the bias current will be over four times as high as a specification based on 25°C junction temperature.

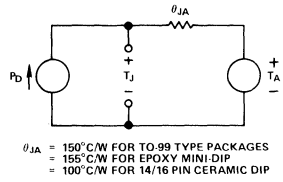

Figure 4. Thermal Circuit Model for IC Op Amp

Consider an op amp specified for 50pA I_B at T_J = 25°C. If the amplifier draws 5mA from ±15V, as in the previous example,

$P_D = 30V \times 5mA = 150mW$

$T_J = T_A + (150mW \times 150°C/W)$

$= 25°C + 22.5°C$

Therefore, I_B will be four times higher than the specification.

Bias current can be measured with essentially the same method used to measure offset voltage. The difference is that a large resistance is inserted in series with the input under test, creating an additional offset voltage equal to $I_B \times R_S$. Assuming the actual V_{OS} has been measured and recorded, the change in apparent V_{OS} due to the change in R_S can be determined and I_B easily computed. Offset current is tested by computing the difference between the bias current on the inverting input and the bias current on the noninverting input.

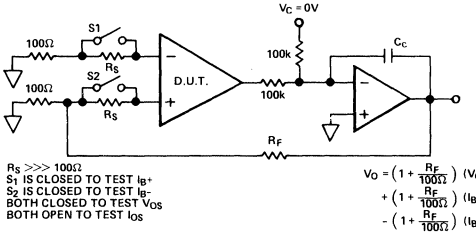

Figure 5. Bias/Offset Current Test Circuit

Open Loop Voltage Gain

Another op amp parameter which distinguishes a real amplifier from an ideal amplifier is open-loop gain. In the ideal op amp model, open loop gain is assumed to be infinite. The same assumption is also sometimes made when dealing with real amplifiers.

Open-loop gain of an operational amplifier is an interesting parameter to attempt to measure. It is generally not practical to measure open loop gain directly by applying a signal at the input and observing the output change. However, by using the device under test inside a feedback loop, it is possible to measure the change in input voltage required to produce a known change in output voltage.

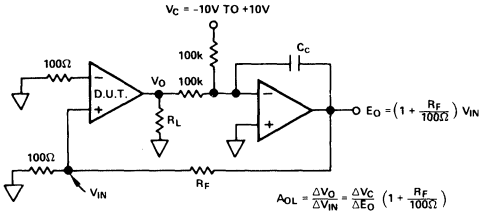

Figure 6. Open Loop Gain Test Circuit

In this circuit, the control voltage, V_C, is varied from −10V to +10V, causing the D.U.T. output, V_O, to vary from +10V to −10V. The D.U.T. output is varied by a change in V_{IN} produced by the second amplifier. Since V_{IN} is attenuated from E_O by the $R_F/100\Omega$ voltage divider, E_O is easily measured, and open-loop gain can readily be computed.

Common-Mode Rejection Ratio

The ideal operational amplifier is a pure differential amplifier and is insensitive to the absolute voltage on the inputs with respect to ground. The real amplifier has several nonideal characteristics associated with input levels. First, of course, is the allowable range of input voltage. Most IC op amps will only operate when the voltage on the input terminal is within the range bounded by the supply voltages. The second, and perhaps more subtle, characteristic is the common-mode rejection ratio (CMRR). CMRR is defined as the ratio of the change in common mode to the resulting change in input offset voltage. It is often convenient to specify this parameter logarithmically in dB: CMR = 20 log (CMRR).

Common-mode rejection can be measured several ways. One method uses four precision resistors to configure the op amp as a subtractor amplifier. The disadvantage inherent in this circuit is that the ratio match of the resistors also determines the subtractor's CMRR. A mismatch of 0.1% between resistor pairs will result in a CMR of only 60dB. Since most amplifiers exhibit CMR in excess of 80dB (some as high as 120dB), it is clear that this circuit is only marginally useful.

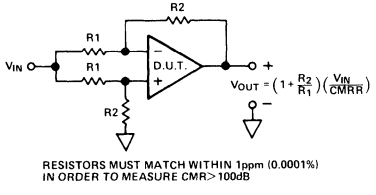

Figure 7. Simple CMR Test Circuit

A better circuit uses the same technique used for measuring offset voltage with one exception. Rather than applying a fixed zero volt input to the D.U.T. operating on ±15V supplies, the same input is applied to the D.U.T. with asymmetrical power supplies, such as +5V and −25V. The output of the amplifier is forced to remain centered between the supplies and the input voltage to the D.U.T. which forces this to occur is measured.

The change in V_{OS} can be readily translated into CMR. If this 10V change in CMV creates a 1mV change in V_{OS}, the CMRR is 10,000 and the CMR is 80dB.

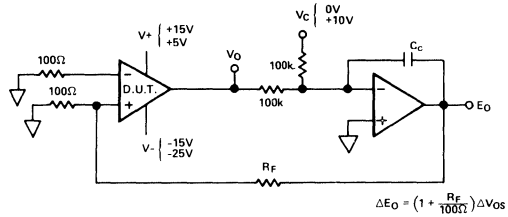

Figure 8. Common-Mode Rejection Test Circuit

Frequency Response

Open-loop gain versus frequency is another difficult-to-test specification. Bandwidth is usually specified in terms of gain-bandwidth product or unity-gain small signal bandwidth. It is assumed that the amplifier under test has an open-loop gain versus frequency plot which decreases with a −20dB/decade slope. It is therefore possible to measure the open-loop gain at some known frequency and predict the frequency at which the open-loop gain will be unity.

In the circuit shown, the D.U.T. dc output is held to 0V by V_C and the integrator amplifier. A low amplitude 10kHz ac input signal is applied to the D.U.T. Since the integrator has very low gain at 10kHz, the D.U.T. is effectively running open-loop for the ac signal. The ac output from the D.U.T. can be measured and the gain at 10kHz can be computed. For example, a 741-type amplifier has an open loop gain of approximately 100 at 10kHz. Thus, an easily generated 100mV input at the D.U.T. input will produce an easily measured 10V output. This corresponds to a 1MHz gain-bandwidth product.

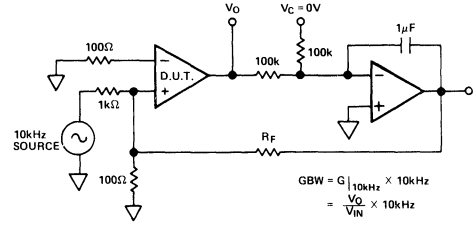

Figure 9. Gain-Bandwidth Product Test Circuit

In general, slew rate, settling time and noise measurements are performed on specialized test fixtures and the parametric data is observed on an oscilloscope. Slew rate can be measured in either the unity gain inverter or unity gain follower circuits. Typically it's measured in the unity gain follower circuit since this is usually the worst case condition due to the amplifier's common-mode swing limitation.

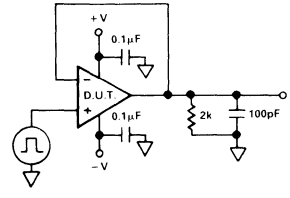

Figure 10. Slew Rate Test Circuit

The amplifier is driven by a high-frequency square wave of sufficient magnitude in both directions in order to remove any rounded peaks from the measurement interval as these portions are not slew rate limited. The slew rate is found as the slope of the transition between the rated output extremes. Frequently the positive and negative swings will have different slew rates, and both have to be monitored.

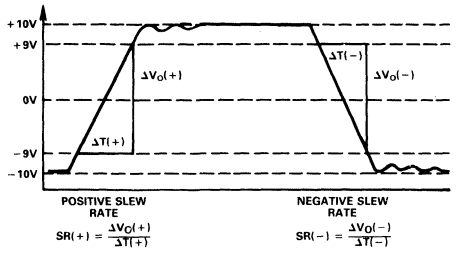

Figure 11. Slew Rate Test Output Waveform

Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value as shown in the following figure. Settling time, therefore, includes the time required for the amplifier to slew from the initial value, recover from slew rate limited overload, and settle to a given error in the linear range.

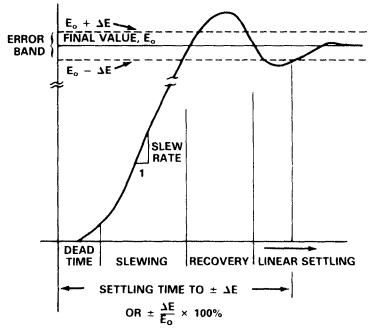

Figure 12. Typical Amplifier Settling Characteristic

To effectively measure settling time, the test fixture should be constructed with relatively low impedance levels, minimum stray capacitance and no load capacitance. A full scale step input is used to determine settling time and the step is usually unipolar. The settling time indicated is generally the longest time resulting from a step of either polarity and is given as a percentage of the full scale step transition.

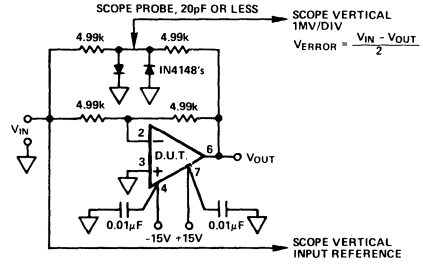

Figure 13. Settling Time Test Circuit

Low frequency noise is difficult to measure, since very long observation intervals are needed. In some cases, low frequency noise is measured by direct observation on a storage-type oscilloscope screen using very slow sweep periods.

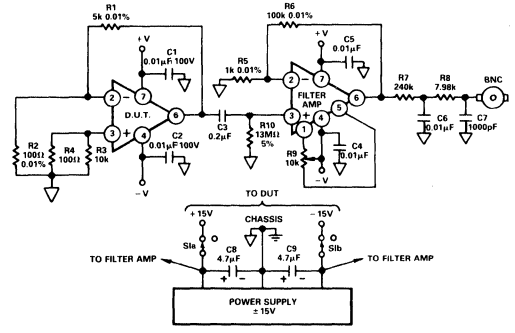

Figure 14. Noise Test Circuit

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An I.C. Amplifier Users' Guide To Decoupling, Grounding, and Making Things Go Right For a Change

by Paul Brokaw

"There once was a breathy baboon
Who always breathed down a bassoon,
For he said "It appears
that in billions of years
I shall certainly hit on a tune"
(Sir Arthur Eddington)

This quotation seemed a proper note with which to begin on a subject which has made monkeys of most of us at one time or another. The struggle to find a suitable configuration for system power, ground, and signal returns too frequently degenerates into a frustrating glitch hunt. While a strictly experimental approach can be used to solve simple problems, a little forethought can often prevent serious problems and provide a plan of attack if some judicious tinkering is later required.

The subject is so fragmented that a completely general treatment is too difficult for me to tackle. Therefore, I'd like to state one general principle and then look a bit more narrowly at the subject of decoupling and grounding as it relates to integrated circuit amplifiers.

. . . Principle: Think—where the currents will flow.

I suppose this seems pretty obvious, but all of us tend to think of the currents we're interested in as flowing "out" of some place and "through" some other place but often neglect to worry how the current will find its way back to its source. One tends to act as if all "ground" or "supply voltage" points are equivalent and neglect (for as long as possible) the fact that they are parts of a network of conductors through which currents flow and develop finite voltages.

In order to do some advance planning it's important to consider where the currents originate and to where they will return and to determine the effects of the resulting voltage drops. This in turn requires some minimum amount of understanding of what goes on inside the circuits being decoupled and grounded. This information may be lacking or difficult to interpret when integrated circuits are part of the design.

Operational amplifiers are one of the most widely used linear I.C.'s, and fortunately most of them fall into a few classes, so far as the problems of power and grounding are concerned. Although the configuration of a system may pose formidable problems of decoupling and signal returns, some basic methods to handle many of these problems can be developed from a look at op-amps.

OP AMPS HAVE FOUR TERMINALS

A casual look through almost any operational amplifier text might leave the reader with the impression that an ideal op-amp has three terminals: a pair of differential inputs and an output as shown in Figure 1. A quick review of fundamentals, however, shows that this can't be the case. If the amplifier has an output voltage it must be measured with respect to some point . . . a point to which the amplifier has a reference. Since the ideal op-amp has infinite common mode rejection, the inputs are ruled out as that reference so that there must be a fourth amplifier terminal. Another way of looking at it is that if the amplifier is to supply output current to a load, that current must get into the amplifier somewhere. Ideally, no input current flows, so again the conclusion is that a fourth terminal is required.

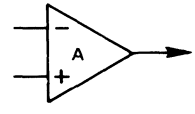

Figure 1. Conventional "Three Terminal" Op Amp

A common practice is to say, or indicate in a diagram, that this fourth terminal is "ground." Well, without getting into a discussion of what "ground" may be we can observe that most integrated circuit op-amps (and a lot of the modular ones as well) don't have a "ground" terminal. With these circuits the fourth terminal is one or both of the power supply terminals. There's a temptation here to lump together both supply voltages with the ubiquitous ground. And, to the extent that the supply lines really do present a low impedance at all frequencies within the amplifier bandwidth, this is probably reasonable. When the impedance requirement isn't satisfied, however, the door is left open to a variety of problems including noise, poor transient response, and oscillation.

DIFFERENTIAL TO SINGLE-ENDED CONVERSION:
One fundamental requirement of a simple op-amp is that an applied signal which is fully differential at the input must be converted to a single-ended output. Single ended, that is, with respect to the often neglected fourth terminal. To see how this can lead to difficulties, take a look at Figure 2.

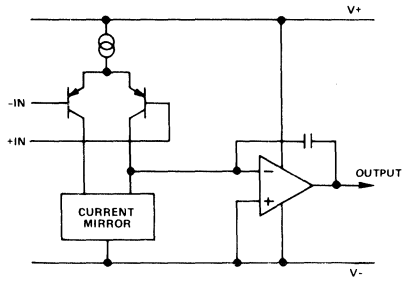

Figure 2. Simplified "Real" Op Amp

The signal flow illustrated by Figure 2 is used in several popular integrated circuit families. Details vary, but, the basic signal path is the same as the 101, 741, 748, 777, 4136, 503, 515, and other integrated circuit amplifiers. The circuit first transforms a differential input voltage into a differential current. This input stage function is represented by PNP transistors in Figure 2. The current is then converted from differential to single-ended form by a current mirror which is connected to the negative supply rail. The output from the current mirror drives a voltage amplifier and power output stage which is connected as an integrator. The integrator controls the open-loop frequency response, and its capacitor may be added externally, as in the 101, or may be self-contained, as in the 741. Most descriptions of this simplified model don't emphasize that the integrator has, of course, a differential input. It's biased positive by a couple of base emitter voltages, but, the non-inverting integrator input is referred to the negative supply.

It should be apparent that most of the voltage difference between the amplifier output and the negative supply appears across the compensation capacitor. If the negative supply voltage is changed abruptly the integrator amplifier will *force* the output to follow the change. When the entire amplifier is in a closed loop configuration the resulting error signal at its input will tend to restore the output, but, the recovery will be limited by the slew rate of the amplifier. As a result, an amplifier of this type may have outstanding low frequency power supply rejection, but, the negative supply rejection is fundamentally limited at high frequencies. Since it is the feedback signal to the input that causes the output to be restored, the negative supply rejection will approach zero for signals at frequencies above the *closed loop* bandwidth. This means that high-speed, high-level circuits can "talk to" low-level circuits through the common impedance of the negative supply line.

Note that the problem with these amplifiers is associated with the negative supply terminal. Positive supply rejection may also deteriorate with increasing frequency, but, the effect is less severe. Typically, small transients on the positive supply have only a minor effect on the signal output. The difference between these sensitivities can result in an apparent asymmetry in the amplifier transient response. If the amplifier is driven to produce a positive voltage swing across its rated load it will draw a current pulse from the positive supply. The pulse may result in a supply voltage transient, but, the positive supply rejection will minimize the effect on the amplifier output signal. In the opposite case, a negative output signal will extract a current from the negative supply. If this pulse results in a "glitch" on the bus, the poor negative supply rejection will result in a similar "glitch" at the amplifier output. While a positive pulse test may give the amplifier transient response, a negative pulse test may actually give you a pretty good look at your negative supply line transient response, instead of the amplifier response!

Remember that the impulse response of the power supply itself is not what is likely to appear at the amplifier. Thirty or forty centimeters of wire can act like a high Q inductor to add a high-frequency component to the normally overdamped supply response. A decoupling capacitor near the amplifier won't always cure the problem either, since the supply must be decoupled *to* somewhere. If the decoupled current flows through a long path, it can still produce an undesirable glitch.

Figure 3 illustrates three possible configurations for negative supply decoupling. In 3a the dotted line shows the negative signal current path through the decoupling and along the ground line. If the load "ground" and decoupled "ground" actually join at the power supply the "glitch" on the ground lines is similar to the "glitch" on the negative supply bus. Depending upon how the feedback and signal sources are "grounded" the effective disturbance *caused* by the decoupling capacitor may be larger than the disturbance which it was intended to prevent. Figure 3b shows how the decoupling capacitor can be used to minimize disturbance of V– and ground busses. The high-frequency component of the load current is confined to a loop which doesn't include any part of the ground path. If the capacitor is of sufficient size and quality, it will minimize the glitch on the negative supply without disturbing input or output signal paths. When the load situation is more complex, as in 3c, a little more thought is required. If the amplifier is driving a load that goes to a virtual ground, the actual load current does not return to ground. Rather, it must be supplied by the amplifier creating the virtual ground as shown in the figure. In this case, decoupling the negative supply of the first amplifier to the positive supply of the second amplifier closes the fast signal current loop without disturbing ground or signal paths. Of course, it's still important to provide a low impedance path from "ground" to V– for the second amplifier to avoid disturbing the input reference.

The key to understanding decoupling circuits is to note where the actual load and signal currents will flow. The key to optimizing the circuit is to bypass these currents around ground and other signal paths. Note, that as in figure 3a, "single point grounding" may be an oversimplified solution to a complex problem.

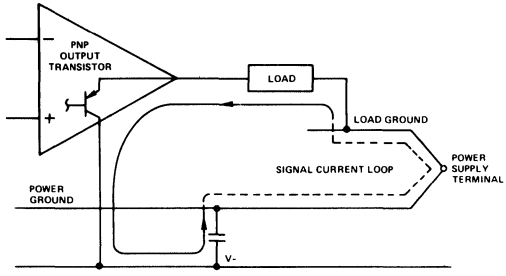

Figure 3a. Decoupling for Negative Supply Ineffective

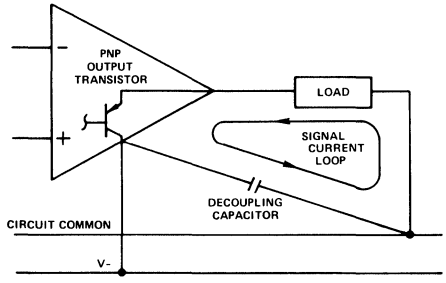

Figure 3b. Decoupling Negative Supply Optimized for "Grounded" Load

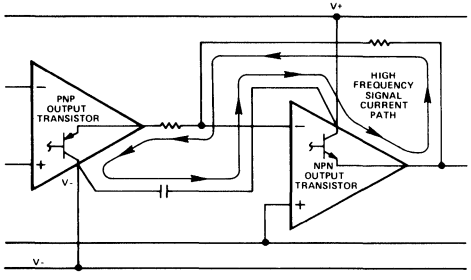

Figure 3c. Decoupling Negative Supply Optimized for "Virtual Ground" Load

Figure 3b and 3c have been simplified for illustrative purposes. When an entire circuit is considered conflicts frequently arise. For example, several amplifiers may be powered from the same supply, and an individual decoupling capacitor is required for each. In a gross sense the decoupling capacitors are all paralleled. In fact, however, the inductance of the interconnecting power and ground lines convert this harmless-looking arrangement into a complex L-C network that often rings like the "Avon Lady". In circuits handling fast signal wavefronts, decoupling networks paralleled by more than a few centimeters of wire generally mean trouble. Figure 4 shows how small resistors can be added to lower the Q of the undesired resonant circuits. The resistors can generally be tolerated since they convert a bad high-frequency jingle to a small damped signal at the op amp supply terminal. The residual has larger *low frequency* components, but, these can be handled by the op-amp supply rejection.

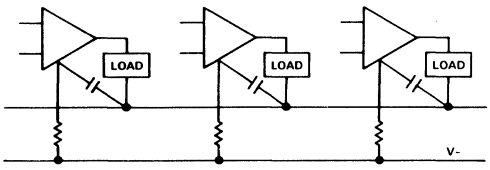

Figure 4. Damping Parallel Decoupling Resonances

FREQUENCY STABILITY

There's a temptation to forget about decoupling the negative supply when the system is intended to handle only low-frequency signals. Granted that decoupling may not be required to handle low-frequency signals, but it may still be required for frequency stability of the op-amps.

Figure 5 is a more-detailed version of Figure 2 showing the output stage of the I.C. separated from the integrator (since this is the usual arrangement) and showing the negative power supply and wiring impedance lumped together as a single constant. The amplifier is connected as a unity gain follower. This makes a closed-loop path from the amplifier output through the differential input to the integrator input. There is a second feedback path from the collector of the output PNP transistor back to the other integrator input. The net input to the integrator is the difference of the signals through these two paths. At low frequencies this is a net, negative feedback. The high-frequency feedback depends upon both the load reactance and the reactance of the V– supply.

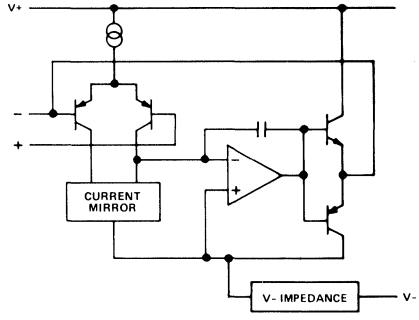

Figure 5. Instability Can Result from Neglecting Decoupling

When the supply lead reactance is inductive, it tends to destabilize the integrator. This situation is aggravated by a capacitive load on the amplifier. Although it's difficult to predict under exactly what circumstances the circuit will become unstable, it's generally wise to decouple the negative supply if there is any substantial lead inductance in the V– lead *or* in the common return to the load and amplifier input signal source. If the decoupling is to be effective, of course, it must be with respect to the *actual* signal returns, rather than to some vague "ground" connection.

POSITIVE SUPPLY DECOUPLING

Up to this point we haven't considered decoupling the positive supply line, and with amplifiers typified by Figures 2

and 5 there may be no need to. On the other hand, there are a number of integrated circuit amplifiers which refer the compensating integrator to the positive supply. Among these are the 108, 504, and 510 families. When these circuits are used, it's the positive supply which requires most attention. The considerations and techniques described for the class of circuits shown in Figure 2 apply equally to this second class, but, should be applied to the positive supply rather than the negative.

FEED-FORWARD

A technique which is most frequently used to improve bandwidth is called feed-forward. Generally, feed-forward is used to bypass an amplifier or level translator stage which has poor high frequency response. Figure 6 illustrates how this may be done. Each of the amplifiers shown is really a subcircuit, usually a single stage, in the overall amplifier. In the illustration, the input stage converts the differential input to a single-ended signal. The signal drives an intermediate stage (which in practice often includes level translator circuitry) which has low-frequency gain, but, limited bandwidth. The output of this stage drives an integrator-amplifier and output stage. The overall compensation capacitor feeds back to the input of the second stage and includes it in the integrator loop. The compromises necessary to obtain gain and level translation in the intermediate stage often limit its bandwidth and slow down the available integrator response. A feed-forward capacitor permits high-frequency signals to bypass this stage. As a result, the overall amplifier combines the low-frequency gain available from 3 stages with the improved frequency response available from a 2-stage amplifier. The feed-forward capacitor also feeds back to the non-inverting input of the intermediate stage. Note that the second stage is not an integrator, as it may appear at first glance, but actually has a positive feedback connection. Fed-forward amplifiers must be carefully designed to avoid internal oscillations resulting from this connection. Improper decoupling can upset this plan and permit this loop to oscillate.

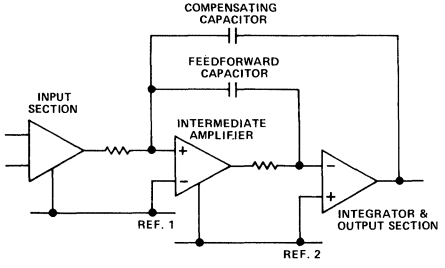

Figure 6. Fast Fed-Forward Amplifier

Note that the internal input stages are shown as being referred to separated reference points, Ideally, these will be the same reference so far as signals are concerned, although they may differ in bias level. In practice this may not be the case. Examples of fed-forward amplifiers are the AD518 and the AD707. In these amplifiers, signal Reference 1 is the positive supply, while signal Reference 2 is the negative supply. Signals appearing between the positive and negative supply terminals are effectively inserted inside the integrator loop!

Obviously, while feed-forward is a valuable tool for the high-speed amplifier designer, it poses special problems in application. A thoughtful approach to decoupling is required to maximize bandwidth and minimize noise, error, and the likelihood of oscillation.

Some fed-forward amplifiers have other arrangements, which include the "ground" terminal in inverting only amplifiers. Almost without exception, however, signals between some combination of the supply terminals get "inside" the amplifier. It is vital to proper operation that the involved supply terminals present a common low impedance at high frequencies. Many high-speed modular amplifiers include appropriate capacitive decoupling within the amplifier, but, with I.C. op amps this is impossible. The user must take care to provide a cleanly decoupled supply for fed-forward amplifiers. Figure 7 shows a decoupling method which may be applied to the AD518 as well as to other fast fed-forward amplifiers such as the 118. One capacitor is used to provide a low-impedance path between the supply terminals at high frequencies. The resistor in the V+ lead insures that noise on the supply lines will be rejected *and* prevents the establishment of resonances with other decoupling circuits. The second capacitor decouples the low side of the integrator to the load.

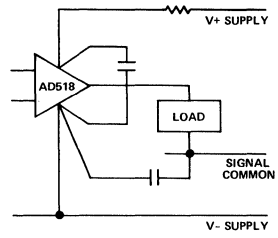

Figure 7. Decoupling for a Fed-Forward Amplifier

Alternatives include a resistor in both supply leads and/or decoupling from V+ to the load. In principle, the positive and negative supply should be tied in a "tight knot" with the signal return. To the extent that this cannot be done, there is a slight advantage to favoring the negative supply due to the high frequency limitations of PNP transistors used in junction-isolated I.C.'s.

OTHER COMPENSATION

While most integrated circuit amplifiers use one of the three compensation schemes already described, a significant fraction use some other plan. The 725 type amplifiers combine a V– referred integrator with a network which the manufacturers recommend to be connected from signal ground to the integrator input. This makes the circuit extremely liable to pick up noise between V– and ground. In many circumstances it may be wiser to connect the external compensation to the negative supply, rather than to signal ground.

One more class of amplifiers is typified by the Analog Devices AD507 and AD509. In these circuits, a single capaci-

tor may be used to induce a dominant pole of response without resorting to an integrator connection. The high-frequency response of the amplifier will appear with respect to the "ground" end of the compensation capacitor. In these amplifiers a small internal capacitance is connected between V+ and the compensation point. Unity gain compensation can be added in parallel and the pin-out is arranged to make this simple. The free end of the compensation capacitor can also be connected either to V– or signal common. It is extremely important that the signal common and the compensation connect directly or through a low-impedance decoupling.

Although the main signal path of these amplifiers can be compensated in a variety of ways, some care is required to insure the stability of internal structures. It's always wise to use extra care in decoupling wideband amplifiers to avoid problems with the output stage and other subcircuits which are similar to the main integrator problem illustrated by Figure 5. An effective compensation and decoupling circuit for the AD509 is shown in Figure 8. This arrangement is similar to Figure 7, and one of these two circuits is likely to be suitable for many types of wideband amplifier. Depending upon the power distribution, a small (10Ω to 50Ω) resistor may be appropriate in both of the supply leads to reduce power lead resonance and interference both to and from circuits sharing the power supply.

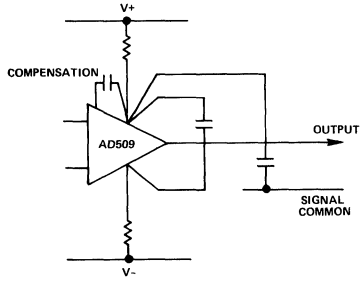

Figure 8. Decoupling a Wideband Amplifier

GROUNDING ERRORS

Ground in most electronic equipment is not an actual connection to earth ground, but a common connection to which signals and power are referred. It is frequently immaterial to the function of the equipment whether or not the point actually connects to earth ground. I myself prefer some distinguishing name or names for these common points to emphasize that they must be *made* common. The term "ground" too often seems to be associated with a sort of cure-all concept, like snake oil, money or motherhood. If you're one of those who regards ground with the same sort of irrational reverence that you hold for your mother, remember that while you can always trust your mother, you should *never* trust your "ground." Examine and think about it.

It's important to have a look at the currents which flow in the ground circuit. Allowing these currents to share a path with a low-level signal may result in trouble. Figure 9 illustrates how careless grounding can degrade the performance of a simple amplifier. The amplifier drives a load which is represented by the load resistor. The load current comes from the power supply and is controlled by the amplifier as it amplifies the input signal. This current must return to the supply by some path; suppose that points A and B are alternative power supply "ground" connections. Assuming that the figure represents the proper topology or ordering of connections along the "ground" bus, connecting the supply at A will cause the load current to share a segment of wire with the input signal connection. Fifteen centimeters of number 22 wire in this path will present about 8 milliohms of resistance to the load current. With a 2k load, a 10-volt output signal will result in about 40 microvolts between the points marked "ΔV." This signal acts in series with the non-inverting input and can result in significant errors. For example, the typical gain of an AD510 amplifier is 8 million so that only 1¼μV of input signal is required to produce a 10 volt output. The 40μV ground error signal will result in a 32 times increase in the circuit gain error! This degradation could easily be the most serious error in a high-gain precision application. Moreover, the error represents positive feedback so that the circuit will latch up or oscillate for large closed-loop gains with R_f/R_i greater than about 250k.

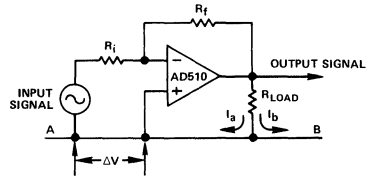

Figure 9. Proper Choice of Power Connections Minimizes Problems

Reconnecting the power supply to point B will correct the problem by eliminating the common impedance feedback connection. In a real system, the problem may be more complex. The input signal source, which is represented as floating in Figure 9, may also produce a current which must return to the power supply. With the supply at point B, any current which flows in additional loads (other than R_i) may interfere with the operation of the amplifier shown. Figure 10 illustrates how amplifiers can be cascaded and still drive auxiliary loads without common impedance coupling. The

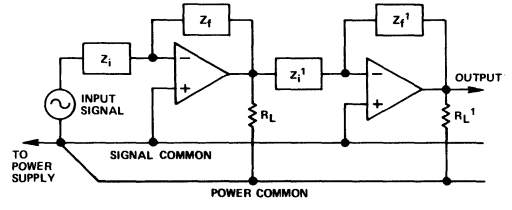

Figure 10. Minimizing Common Impedance Coupling

output currents flow through the auxiliary loads and back to the power supply through power common. The currents in the input and feedback resistors are supplied from

the power supply by way of the amplifiers as previously illustrated in Figure 3c. The only current flowing in signal common is the amplifier's input current, and its effect is generally negligibly small.

Having given an example of a simple "grounding error" and its solution, I will now get back on my soap box and say that grounding errors result from neglect based on the assumption that a ground, is a ground, is a ground. *Some* impedance will be present in any interconnection path, and its effect should be considered in the overall design of a system. Quantitative approaches are quite useful in specialized applications.' In fast TTL and ECL logic circuitry the characteristic impedance of interconnections is controlled so that proper terminations can reduce problems. In RF circuitry the unavoidable impedances are taken into account and incorporated into the design of the circuit. With op-amp circuitry, however, impedance levels do not lend themselves to transmission line theory, and the power and ground impedances are difficult to control or analyze. The most expedient procedure, short of difficult and restrictive quantitative analysis, seems to be to arrange the unavoidable impedances so as to minimize their effects and arrange the circuitry to overcome the effects. Figures 9 and 10 illustrate the sort of simple considerations which can substantially reduce practical ground problems. Figure 11 illustrates how circuitry can be used to reduce the effect of ground problems which can't be corrected by topological tricks.

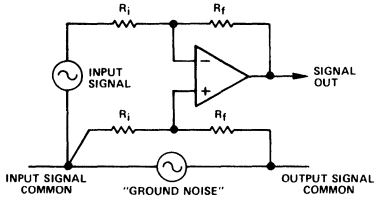

Figure 11. Subtractor Amplifier Rejects Common Mode Noise

GETTING AROUND THE PROBLEM

In Figure 11 a subtractor circuit is used to amplify a normal mode input signal and reject a ground noise signal which is common to both sides of the input signal. This scheme uses the common-mode rejection of the amplifier to reduce the noise component while amplifying the desired signal. An important aspect of this arrangement, which is often overlooked, is that the amplifier should be powered with respect to the *output* signal common. If its power pins are exposed to the high-frequency noise of the input common, the compensation capacitor will direct the noise right to the output and defeat the purpose of the subtractor. It's just this kind of effect which makes it important to use care in grounding and decoupling. A subtractor or dynamic bridge, like Figure 11, will be ineffective in correcting a grounding problem if the amplifier itself is carelessly decoupled. In general, an op-amp should be decoupled to the point which is the reference for measuring or using its output signal. In "single-ended" systems it should also be decoupled to the input signal return as well. When it is impossible to satisfy both these requirements at once, there's a high probability of either a noise or oscillation problem or both. Frequently the difficulty can be resolved with a subtractor, like Figure 11, where a network like the single-ended feedback network (which needn't be all resistive) joins the input and output signal reference points and provides a "clean" reference point for the non-inverting input of the amplifier.

A problem with the subtractor is that it uses a balanced bridge to reject the common mode signal between the input and output reference points. The arms of the network must be carefully balanced, since to the extent they don't match, the unwanted signal will be amplified. Although even a poorly matched network will probably eliminate oscillation problems, noise rejection will suffer in direct proportion to any mismatches. An easier way to reject large "ground noise" signals is to use a true instrumentation amplifier.

INSTRUMENTATION AMPLIFIERS

A true instrumentation amplifier has a very visible "fourth terminal." The output signal is developed with respect to a well defined reference point which is usually a "free" terminal that may be tied to the output signal common. The instrumentation amplifier also differs from an op amp in that the gain is fixed and well defined, but there is no feedback network coupling input and output circuits. Figure 12 shows how an instrumentation amplifier can be used to translate a signal from one "ground reference" to another. The normal mode input signal is developed with respect to one reference point which may be common to its generating circuits. The signal is to be used by a system which has an interfering signal between its own common and the signal source. The instrumentation amplifier has a high impedance differential input to which the desired signal is applied. Its high common mode rejection eliminates the unwanted signal and translates the desired signal to the output reference point. Unlike the dynamic bridge circuit, the gain and common mode rejection don't depend on a network connecting the input and output circuits. The gain is set, in Figure 12, by the ratio of a pair of resistors which are connected inside the amplifier. The amplifier has a very high input impedance, so that gain and common mode rejection are not greatly affected by variations or unbalance in source impedance.

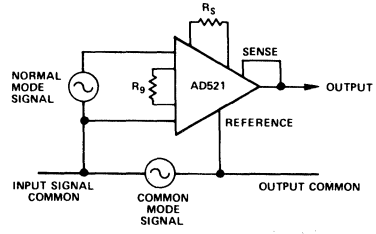

Figure 12. Applying an In-Amp

Since instrumentation amplifiers have a reference or "ground" terminal, they have the potential to be free of the power supply sensitivities of op amps. In practice, however, most instrumentation amplifiers have internal frequency

compensation which is referred to the power supply. In the case of the AD521, the compensation integrator is referred to the negative supply terminal. The decoupling of this terminal is particularly important, and it should be decoupled with respect to the output reference terminal, or actually to the point to which this terminal refers. The AD520 instrumentation amplifier, on the other hand, has an internal integrator which is referred to the positive supply terminal. For best results both the V+ and V– terminals should be decoupled to the output reference point.

THE "OTHER" INPUT

Most I.C. op-amps and in-amps include offset voltage nulling terminals. These terminals generally have a small voltage on them and by loading the terminals with a potentiometer the amplifier offset voltage can be adjusted. While their impedance level is much lower than the normal input, the null terminals can act as another differential input to the amplifier. Although the null terminals aren't generally looked at as inputs, most amplifiers are quite sensitive to signals applied here. For example, in 741 family amplifiers the output voltage gain from the null terminals is greater than the gain from the normal input!

An illustration of the type of problems that can arise with the "other" input is shown in Figure 13. The figure is an op-amp circuit with some of the offset null detail shown.

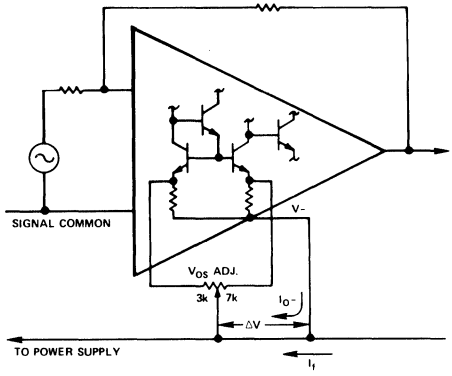

Figure 13. Details of V_{OS} Nulling – the "Other" Input

As it's drawn, the V_{OS} null pot wiper connects to a point along a V– "clothesline" which carries both the return current from the amplifier and currents from other circuits back to the power supply. These currents will develop a small voltage, ΔV, along the conductor between the amplifier V– terminal and the null pot wiper. If the null pot is set on center, the equal halves will form a balanced bridge with the resistors inside the amplifier. The effect of the voltage generated along the wire is balanced at the V_{OS} terminals and will have little effect on the amplifier output. On the other hand, if the null pot is unbalanced, to correct an amplifier offset, the bridge will no longer balance. In this case voltages developed along the "clothesline" will result in a difference voltage at the V_{OS} terminals. For instance, suppose that a 10k null pot balances out the op amp offset when it is set with 3k and 7k branches as shown in the figure. In a 741 the internal resistors are about 1k so that the difference signal at the V_{OS} terminals will be about 1/8 ΔV. The gain from these terminals is about twice the gain from the normal input, so that the disturbance acts as if it were an input signal of about 1/4 ΔV. Using the same assumptions as in the discussion of Figure 9. the current I_O– will result in a 10 microvolt input error signal. In this case, however, the error will appear *only* when the amplifier load current comes from the negative supply. When the load is driven positive the error will disappear. As a result, the V_{OS} input signal will result in distortion rather than a simple gain error!

An additional problem is created by I_f, a current returning to the power supply from other circuits. The current from other circuits is not generally related to the op amp signal, and the voltage developed by it will manifest itself as noise. This signal at the null terminals can easily be the dominant noise in the system. A few milliamps of V– current through a few centimeters of wire can result in interference which is orders of magnitude larger than the inherent input noise of the amplifier. The remedy is to make the connection from the null pot wiper direct to the V– pin of the amplifier, as shown in Figure 14. Some amplifiers such as the AD504 and AD510 refer to the null offset terminals to V+. Obviously, the pot wiper should go to the V+ terminal of this type of amplifier. It's important to connect the line directly to the op amp terminal so as to minimize the common impedance shared by the op amp current and the null pot connection.

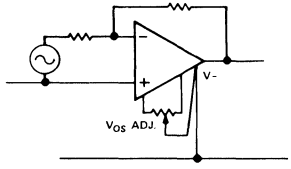

Figure 14. Connecting the Null Pot for Trouble Free Operation

The considerations for op-amp null pots also apply to the similar trimmers on almost all types of integrated circuits. For example, the AD521 In-Amp null terminals exhibit a gain of about 30 to the output. Although this is much less than in the case of most op-amps, it still warrants care in controlling the null pot wiper return. Table I lists the integrated circuits manufactured by Analog Devices, including some popular second-source families, and indicates how internal conversions from differential to single ended are referred. That is, the signals are made to appear with respect to the terminal(s) listed.

	Internal Integrator Referred to:	Comment
AD OP 07/ 27/37	V+, V−	Internal Feedforward Cap V+ to V− and Integrator V− to Output
AD380	V+	
AD390	V−	Output and Reference Amplifier
AD394/AD395	V−	Output Amplifiers
AD396	V−	Output Amplifiers
AD507	–	External Cap to Signal Common or V+
AD508	–	External Cap to Signal Common or V+
AD510	V+	
AD517	V+	
AD518	V+, V−	Internal Feedforward Cap V+ to V− and Integrator V− to Output
AD521	V−	Output Amplifier Integrator
AD524	V−	Output Amplifier Integrator
AD526	V−	Output Amplifier Integrator
AD532/AD533	V+	Multiplier Output Amplifier Integrator
AD534/AD535	V−	Output Amplifier
AD536A	V−, V+ Common	External Integrator to V+, Internal Feedforward V− to Common
AD538	V−	Internal Amplifiers
AD542/AD642	V−	
AD544/AD644	V−	
AD545A	V−	
AD546	V−	
AD547/AD647	V−	
AD548/AD648	V−	
AD549	V−	
AD557/AD558	Common	Output Amplifier and DAC Control Loop Integrator Referred to Common
AD561	V−, Common	DAC Control Loop Integrator and Ref. Amp Referred to Common and Ref. Bias Amplifier Referred to V−
AD565A/ AD566A	V−	DAC Control Loop Integrator Referred to V−. Reference Input Common to Control Loop Isolated from DAC Output Common
AD568	V+	Reference Amplifier
AD580	V−	Output Amplifier
AD581	V−	Output Amplifier
AD582	V−	Output Amplifier
AD584	V−	Output Amplifier
AD586/AD587	V−	Output Amplifier
AD588	V−	Output Amplifier
AD624/AD625	V−	Output Amplifier Integrator
AD636	V−, V+, Common	External Integrator to V+, Internal Feedforward V− to Common
AD637	V−, Common	Internal Feedforward V− to Common
AD645	V−	
AD650/AD652	V+	Internal Amplifier
AD662	Common	DAC Control Loop Integrator and Reference Amplifier Referred to Common
AD664	V−	Output Amplifiers
AD667	V−, Common	Output Amplifier Referred to V− and Reference Amplifier Referred to Common
AD668	V+	Reference Amplifier
AD688	V−	Output Amplifier
AD689	V−	Output Amplifier
AD704/AD705/ AD706	V+	
AD707/AD708	V+, V−	Internal Feedforward Cap V+ to V− and Integrator V− to Output
AD711/AD712/ AD713	V−	
AD736/ AD737	V−, Common	External Integrator to V− Internal Feedforward V− to Common
AD741	V−	
AD744/AD746	V−	
AD766	V−	Output and Reference Amplifier
AD767	V−, Common	Output Amplifier Referred to V− and Reference Amp Referred to Common
AD840/AD841/ AD842	V+, V−	
AD843	V+, V−	
AD844/AD846	V+, V−	
AD845	V+	
AD847/AD848/ AD849	V+, V−	
AD1856/AD1860	V−	Output and Reference Amplifier
AD1864	V−	Output and Reference Amplifier
AD2700/AD2710	Common	Output Amplifier
AD2701	V−	Output Amplifier
AD2702/ AD2712	V−, Common	Output Amplifiers
AD7224/AD7225	V−	Output Amplifiers
AD7226/AD7228	V−	Output Amplifiers
AD7237/ AD7247	V−, Common	Reference Amplifier to Common Output Amplifier to Both V− and Common
AD7245/ AD7248	V−, Common	Reference Amplifier to V− Output Amplifier to Both V− and Common
AD7569/AD7669	V−	All Amplifiers
AD7769	Common	All Amplifiers
AD7770	Common	All Amplifiers
AD7837/AD7847	V−	All Amplifiers
AD7840	V+, Common	Output Amplifiers to V− Reference Amplifier to Common
AD7845	V−	All Amplifiers
AD7846	V−	All Amplifiers
AD7848	V−, Common	Output Amplifier to V− Reference Amplifier to Common

Table I.

This collection of examples won't solve all your potential grounding problems. I hope that it will give you some good ideas how to prevent some of them, and it should also give you some of the "inside story" on I.C.'s which you can put to work in very practical ways. There is no general grounding method which will prevent all possible problems. The only generally applicable rule is attention to detail, and remember that you can always trust your mother, but . . . .

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Video Formats & Required Load Terminations

by Bill Slattery

A number of international standards exist for specifying video levels used in television and video monitors. This application note describes some of the more common standards and compares their similarities. It also details the required load terminations for Analog Devices video RAM-DACs and explains how alternate video standards can be implemented by altering the load termination.

VIDEO STANDARDS

The NTSC standard is the one most commonly used in North America and Japan, while Europe uses PAL and SECAM video standards. Figure 1 shows an RGB video waveform, and Table I shows the associated current, voltage and IRE relationships for the various video standards.

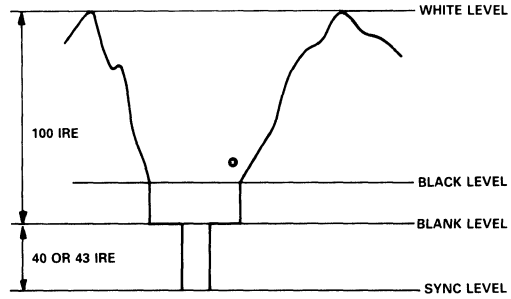

Figure 1. RGB Video Waveform

Table I. Levels Associated with Various Video Formats

	Video Output Levels	IRE Units	Volts	Singly Terminated Line mA (typ), 75Ω Monitor	Doubly Terminated Line mA (typ), 75Ω Monitor
NTSC RS-343A	Blank to White	100	0.714 ±0.1	9.52	19.04
	Blank to Black	7.5 ±5	0.054 (typ)	0.714	1.43
	Blank Level		0	0	0
	Blank to Sync	40 (typ)	−0.286 ±0.05	−3.81	−7.62
NTSC RS-170	Blank to White	100	1.0 ±0.05	13.33	26.67
	Blank to Black	7.5 ±2.5	0.075 (typ)	1	2
	Blank Level		0	0	0
	Blank to Sync	40 ±5	−0.4 (typ)	−5.33	−10.67
PAL	Blank to White	100	0.714 (typ)	9.52	19.04
	Blank to Black	0	0	0	0
	Blank Level		0	0	0
	Blank to Sync	43 (typ)	−0.307 (typ)	−4.09	−8.19
SECAM	Blank to White	100	0.714 (typ)	9.52	19.04
	Blank to Black	0 to 7	0 to 0.049	0	0
	Blank Level		0	0	0
	Blank to Sync	43 (typ)	−0.307 (typ)	−4.09	−8.19

NOTE
This table indicates the Blank Level as being the zero reference level while the Sync Level is given a negative value. In the case where composite sync is asserted using the DAC, Analog Devices video RAM-DACs have the Sync Level as the zero reference level; the Blank, Black and White Levels are all offset positively by the value of Sync Level. This will have no effect on the implementation of a particular standard as this is determined by the relative magnitude of the Blank Level relative to the White Level. The Blank to White Level remains unchanged whether or not sync is being asserted by the DAC.

The composite video waveform illustrates the relationship between the white level and blank level (gray scale or video portion) as well as the black and sync levels. The amplitude level between the blank level and white level is defined to be 100 IRE units. This corresponds to a voltage level of either 1V or 0.714V. The newer international standards specify the lower voltage level of 0.714V. The RS-343A, PAL and SECAM standards all specify a blank to white level of 0.714V, while RS-170 specifies a level of 1V. The blank to black level, also known as the setup or pedestal, is used to ensure a blacker than black beam level during retrace. The amplitude of the blank to black level varies between 0 and approximately 7.5 IRE units, depending on the video standard used. An additional 40 to 43 IRE units are required to drive the beam to the sync level. The sync levels of 40 IRE units for NTSC and 43 IRE units for both PAL and SECAM are close enough in tolerance to the 40 IRE levels of Analog Devices video RAM-DACs, thus enabling Analog Devices parts to output either NTSC, PAL or SECAM video formats. Table I illustrates the various amplitude levels and their tolerances for the video formats outlined above.

The most common of the four video standards used in computer graphics is RS-343A. The three RGB (red, green and blue) signals are individually generated, each one containing video, blanking and sync information. In many cases however, sync information is only encoded onto the green channel.

LOAD TERMINATIONS

Analog Devices video RAM-DACs are capable of driving 75Ω monitors using either doubly terminated or singly terminated loads. Table I shows the currents associated with the various video standards, for both 75Ω load termination and 37.5Ω (doubly terminated 75Ω) load termination. Figures 2 and 3 show the electrical connections between the video RAM-DAC and monitor. Any of the video standards listed in Table I can be implemented using either of these two terminations. Note that for singly terminated loads, I_{OUT} will have to be changed by adjusting I_{REF}.

IMPLEMENTATION OF RS-343A AND RS-170

Analog Devices video RAM-DACs can implement either RS-343A or RS-170. This is achieved, in the case of a doubly terminated configuration, by varying the value of the source termination resistance Z_S. Figures 4a to 4d show the required terminations as well as the associated RGB video waveforms for both RS-343A and RS-170 implementation when using the ADV478/ADV471. The assertion or nonassertion of sync is also distinguished in these diagrams. The advantage of using this technique to implement the different video standards lies in the fact that the output current level of the DAC need not be altered. The relationship between DAC output current, load termination resistance and voltage across the monitor is given by

$$V_L = \frac{I_{OUT} \cdot Z_S \cdot Z_L}{Z_S + Z_L}$$

V_L = voltage developed across monitor
I_{OUT} = DAC output current
Z_S = source termination resistance
Z_L = cable/monitor impedance

Since the relevant video standard is determined by the voltage developed across Z_L, altering the value of Z_S is a simple method of selecting any of the video standards.

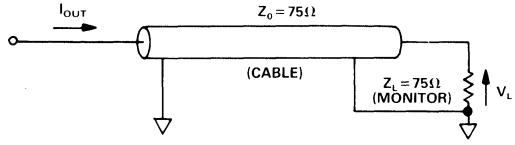

Figure 2. Singly Terminated 75Ω Load

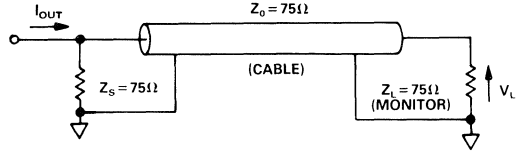

Figure 3. Doubly Terminated 75Ω Load

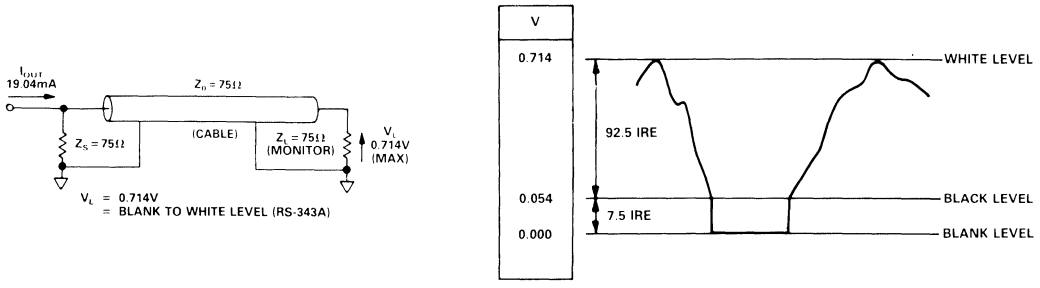

Figure 4a. RS-343A Load Termination & RGB Video Waveform (SYNC Not Asserted)

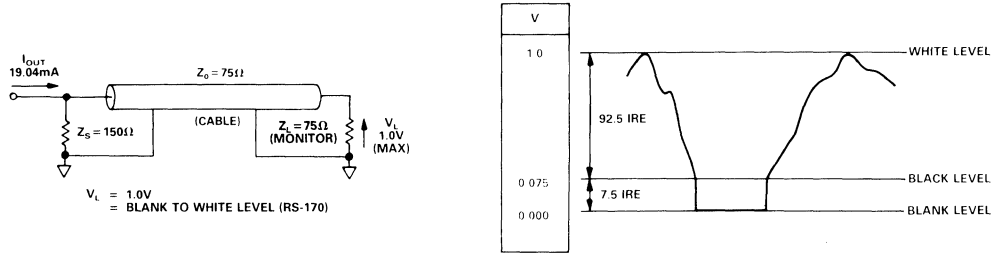

Figure 4b. RS-170 Load Termination & RGB Video Waveform (SYNC Not Asserted)

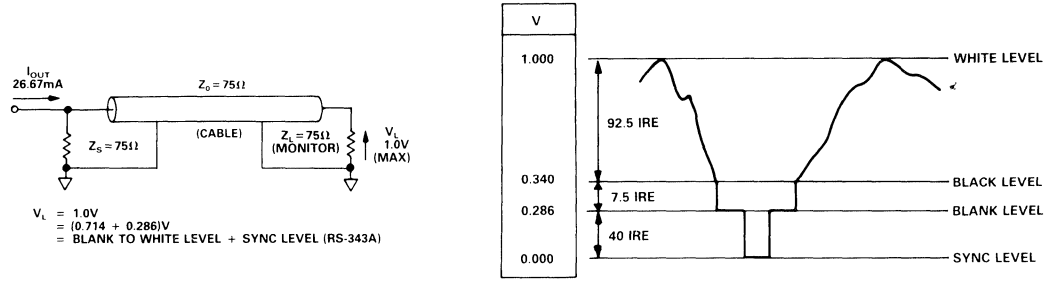

Figure 4c. RS-343A Load Termination & RGB Video Waveform (SYNC Asserted)

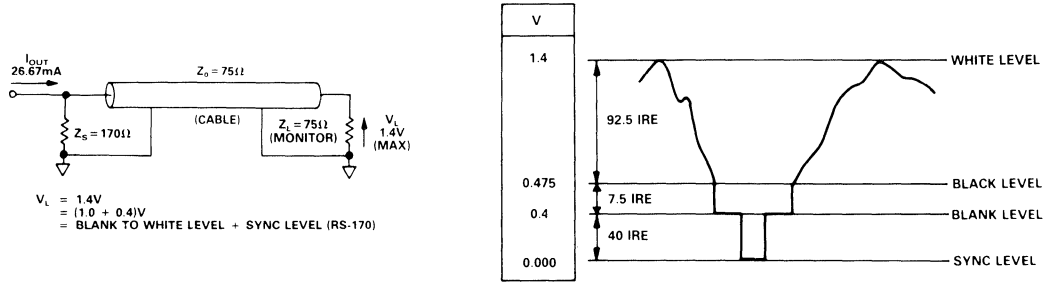

Figure 4d RS-170 Load Termination & RGB Video Waveform (SYNC Asserted)

SELECTABLE TERMINATION

Figures 5a and 5b illustrate an interesting load termination technique which allows the user to select either RS-343A or RS-170. If the switch is in the closed position, RS–343A is implemented. If the switch is in the open position, a blank to white voltage level of 1V is developed across the 75Ω monitor load, corresponding to RS-170. In the case where sync is not asserted by the DAC, the termination is as shown in Figure 5a. When sync is asserted by the DAC, the output must be terminated according to Figure 5b.

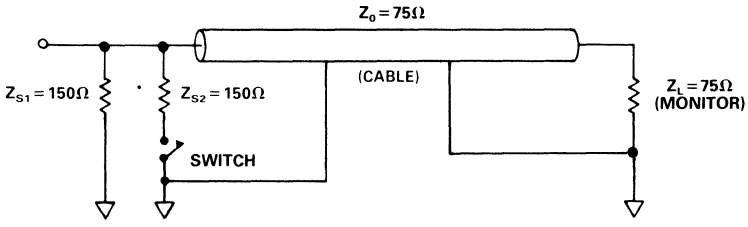

Figure 5a. RS-343A & RS170 Selectable Termination (SYNC Not Asserted)

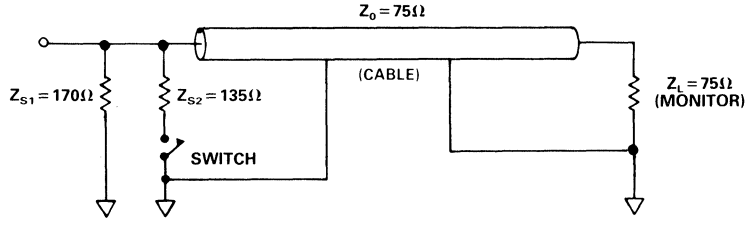

Figure 5b. RS-343A & RS170 Selectable Termination (SYNC Asserted)

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Analog Panning Circuit Provides Almost Constant Output Power

by John Wynne

In audio recording and playback it is often required to split or "pan" a single signal source into a two-channel signal for stereo effects. To locate the signal source as desired in the sound stage, the overall signal power is maintained constant while the relative levels in the derived channels are adjusted. This application note describes a circuit which limits variations in the total output power to ±0.1dB. It uses two CMOS Multiplying D/A Converters to control the signal levels in the derived channels. CMOS DACs are ideal in this application because of their low distortion. The DACs function as resistive attenuators using thin-film resistors which have low noise and very low voltage coefficient. Converters which are especially suitable for this application are Dual-DACs which contain two CMOS DACs on a monolithic substrate. These are available from Analog Devices with 8-bit resolution (AD7528) or 12-bit resolution (AD7537/47/49).

The simplest and most obvious circuit for panning is shown in Figure 1. The digital data N_B fed to DAC B is the 2's complement of the data N_A fed to DAC A. For n-bit converters the digital input codes, N_A & N_B, can be represented by fractional values, D_A & D_B respectively, where $D_A = N_A/2^n$ and $D_B = N_B/2^n$, with N_A and N_B in decimal format. Because of the 2's complement arrangement between the DACs, the all 0's code or full mute condition is not allowed – in theory at least. The relationship between the two fractional representations, D_A & D_B, is given as:

$$D_A + D_B = 1 \quad (1)$$

The output voltage expressions for the two channels in Figure 1 are as follows:

$$V_{OUTA} = -D_A \cdot V_{IN} \quad (2)$$

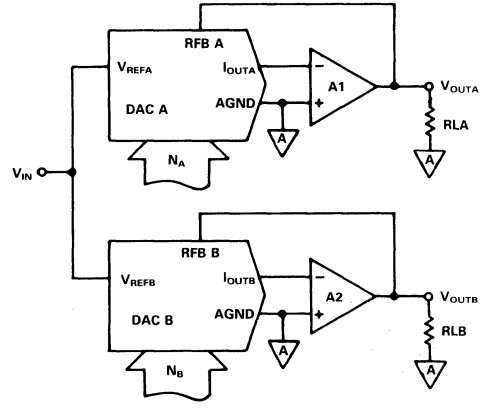

Figure 1. Simple Power Splitter Circuit

$$V_{OUTB} = -D_B \cdot V_{IN} \quad (3)$$

The performance of a 12-bit system is shown in Figure 2 where the total output power level is plotted versus N_A. The 0dB output power level used as the reference level in Figure 2 is the total output power available when $D_A = D_B = 0.5$, the balanced condition. With this simple panning circuit, the total output power level at either extreme of the allowable input code range has increased by 3dB (a doubling of the power) over the power output level at the balanced condition. Load impedances, RLA & RLB, are assumed equal for both channels.

11

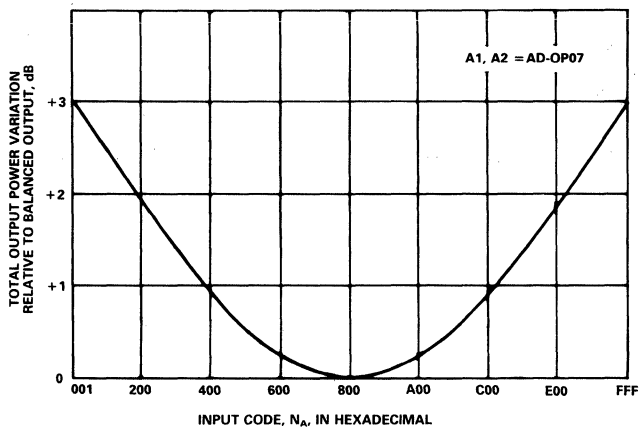

Figure 2. Response of Figure 1 Using 12-Bit DACs

A circuit which avoids this doubling in output power level is shown in Figure 3. The DACs are again driven with 2's complementary data. The output voltage expressions for the two channels are as follows:

$$V_{OUTA} = \frac{-D_A \cdot V_{IN}}{1 + D_A} \quad (4)$$

$$V_{OUTB} = \frac{-D_B \cdot V_{IN}}{1 + D_B} \quad (5)$$

Power splitter performance for this circuit when implemented with 12-bit DACs is shown in Figure 4. At the extremes of the input code range the total output power is now only 0.5dB greater with respect to its level at the balanced condition. This amount of output variation would be acceptable in many applications. Certain applications, however, may demand better performance than this.

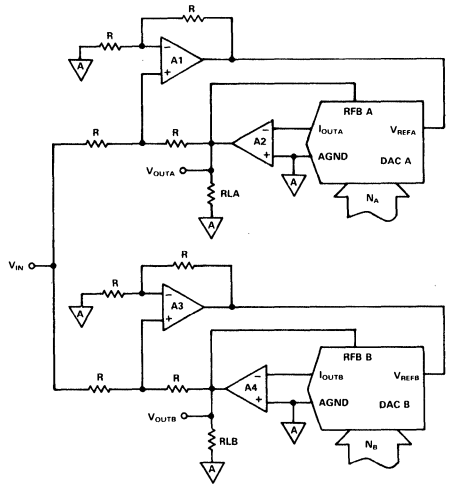

Figure 3. Improved Power Splitter Circuit

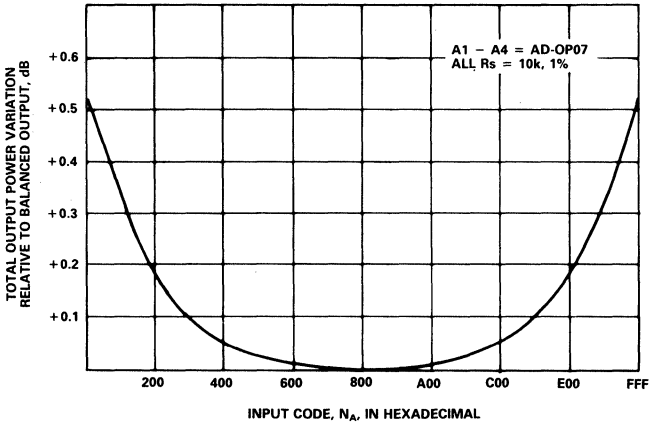

Figure 4. Response of Figure 3 Using 12-Bit DACs

HIGHER PERFORMANCE POWER SPLITTER

A higher performance power splitter circuit can be built by adding some gain around the CMOS DACs of Figure 3. The gain factor required is equal to $\sqrt{2}$.

In order to provide a DAC output voltage which is $\sqrt{2}$ times greater than normal, the effective value of the feedback resistor must be made equal to $\sqrt{2}$ times the DAC ladder impedance R_{DAC}. Reference 1 outlines how additional gain can be added to the standard configuration without requiring a large gain adjustment range or compromising the circuit's temperature coefficient. The circuit configuration of Figure 5 provides the additional $\sqrt{2}$ gain factor. Resistors R1, R2 and R3 should have similar temperature coefficients, but they need not match the temperature coefficient of the DAC. The three resistors are precision (0.1%) metal film resistors with standard EIA/MIL values. When both DAC circuits of Figure 3 are changed to include the gain resistors of Figure 5, the output voltage expressions for the two channels become:

$$V_{OUTA} = \frac{-\sqrt{2} \cdot D_A \cdot V_{IN}}{1 + \sqrt{2} \cdot D_A} \quad (6)$$

$$V_{OUTB} = \frac{-\sqrt{2} \cdot D_B \cdot V_{IN}}{1 + \sqrt{2} \cdot D_B} \quad (7)$$

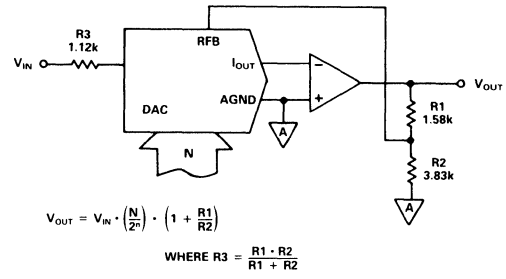

Figure 5. Additional Resistors to Provide $\sqrt{2}$ Gain Factor

The performance of the revised circuit is shown in Figure 6. The total power output at either extreme of the input code range is equal to the total power output at the balanced condition. The output power level remains constant within a ±0.1dB error band. With the exception of R1, R2 and R3, all resistors are metal film, 10kΩ, 1% tolerance.

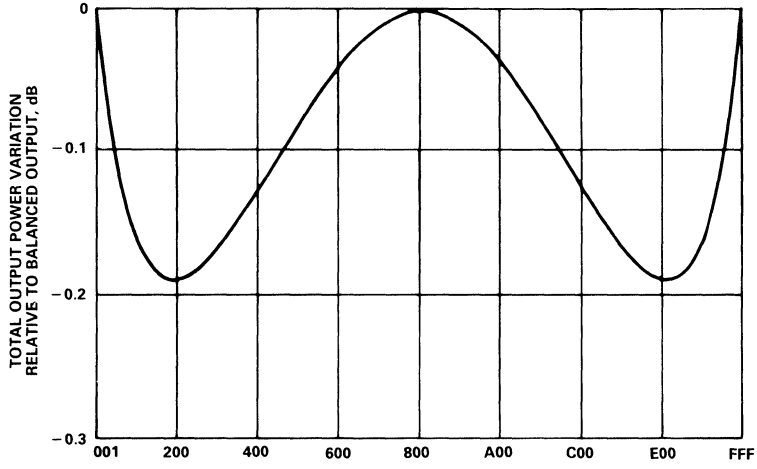

Figure 6. Response of Figure 3 Using $\sqrt{2}$ Gain Factor

STAND-ALONE APPLICATIONS

Many applications which are microprocessors-based will have no difficulty in generating the 2's complement data required for the previous power splitter circuits. It is also possible in non-microprocessor-based systems to perform the 2's complement operation with dedicated hardware. If either of these approaches are unsuitable, for whatever reason, it is still possible to build a power splitter circuit by rewiring one of the DAC channels and driving both DACs with identical data. Figure 7 shows the rewiring and the additional circuitry required to achieve this.

The output expressions for the two channels are now:

$$V_{OUTA} = \frac{-D \cdot V_{IN}}{1 + D} \quad (8)$$

$$V_{OUTB} = \frac{-(1-D) \cdot V_{IN}}{2 - D} \quad (9)$$

The performance of Figure 7 is identical to that of Figure 3. Additionally, the circuit performance can be upgraded in a similar fashion as previously described for Figure 5.

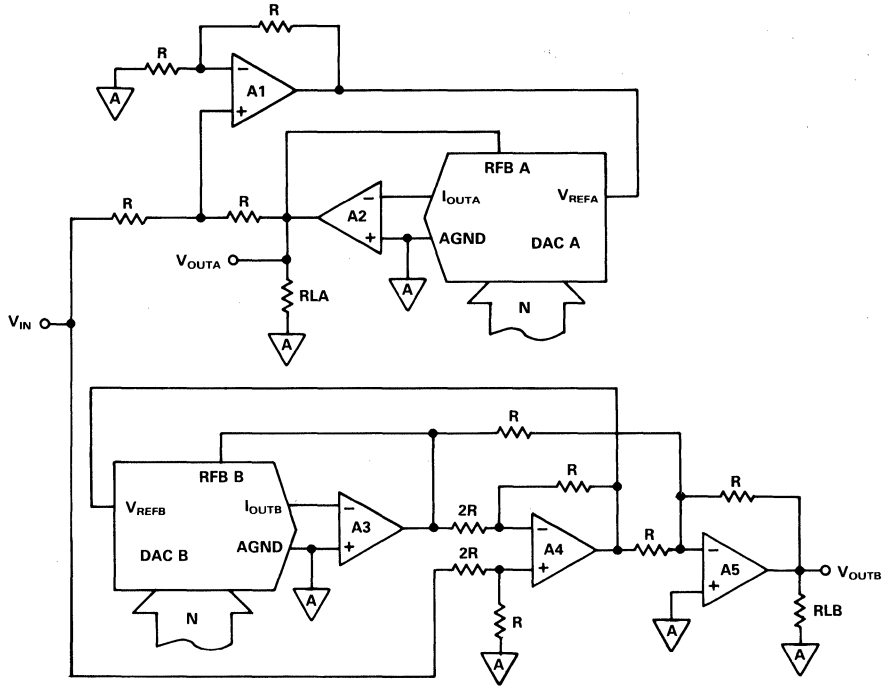

Figure 7. Power Splitter Circuit with Identical DAC Data, N

REFERENCES

1. Brokaw P., "Input Resistor Stabilizes MDACs Gain". EDN, January 7, 1981, pp.210-211.

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Interfacing Two 16-Bit AD1856 (AD1851) Audio DACs with the Philips SAA7220 Digital Filter

by Kevin Greene

INTRODUCTION

The AD1856 is a complete 16-bit DAC used primarily for digital audio applications. The AD1851 is a lower noise, second generation version of the AD1856. Each device provides a voltage output amplifier, 16-bit DAC, 16-bit serial-to-parallel input register, and voltage reference. The AD1856 is specified to operate with ±5 V to ±12 V supplies and achieves a *maximum* of 0.0025% total harmonic distortion (THD). The AD1851 operates with ±5 V supplies and has a *maximum* of 0.004% total harmonic distortion + noise (THD + N), and a signal-to-noise ratio (SNR) of at least 107 dB. Their performance and ease of use make the AD1856/AD1851 popular choices for 16-bit audio designs.

The Philips SAA7220 is a 4× oversampling digital interpolating filter. Some listeners prefer the sound quality of this filter over other digital filters on the market. The SAA7220 features attenuation correction in the audio passband. Other digital filters typically do not incorporate this feature making it difficult, if not impossible, to achieve a flat frequency response using a Butterworth or Bessel filter. These features make the SAA7220 a popular choice for system designers.

The combination of the AD1856/AD1851 with the SAA7220 yields a system with very low THD + N and an excellent SNR. If a Bessel (also known as Thompson) filter is used, the transient response will be exceptional as well. Figure 1 shows a block diagram of the system. Unfortunately, the output interface of the SAA7220 is compatible with I²S format, while the AD1856/AD1851 has a standard 3-line interface.

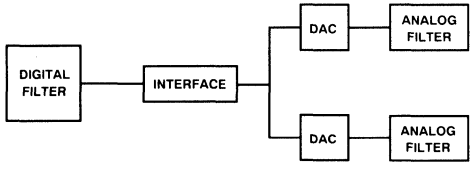

Figure 1. Block Diagram of System

INTERFACE

The interface needs to take the SAA7220 output, which conforms to I²S format (see Figure 2a), and modify it to match the input requirements of the AD1856/AD1851.

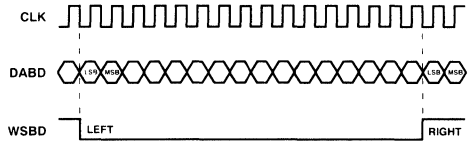

Figure 2a. Output of SAA7220

Three signals must be present for proper operation of the AD1856/AD1851: Data, Clock, and Latch Enable. These signals are shown in Figure 2b. Bringing Latch Enable low after the least significant bit of any word latches the previous 16 bits and starts the conversion.

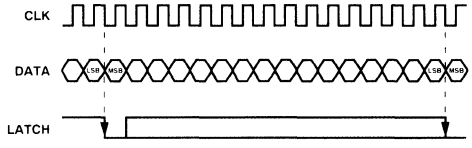

Figure 2b. Signal Requirements for AD1856 (AD1851)

In order for the AD1856/AD1851 to be compatible with the SAA7220, the interface must delay the WSBD line by one clock cycle, gate the clock on the left channel, and simultaneously latch both DACs to eliminate any phase shifts between channels. A quad NAND gate and a dual D flip-flop accomplish this as shown in Figure 3.

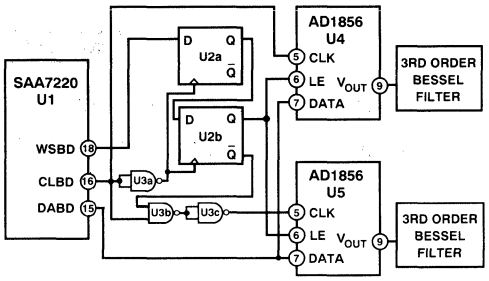

Figure 3. Interface of the SAA7220 and AD1856 (AD1851)

CIRCUIT DESCRIPTION

Data bits are valid on the negative edge of the clock. The D flip-flops are positive-edge triggered, therefore one NAND gate (U3a) is used to invert the clock to the flip-flops. Referring to Figure 2a, WSBD goes low one clock cycle prior to the LSB. Figure 2b shows LATCH going low after the LSB. The flip-flops delay WSBD by one clock cycle, similar to a shift register, to correct this mismatch. The other two NAND gates (U3b and U3c) are used to form an AND gate to gate the clock to the left channel DAC (U5). The SAA7220 transmits serial data, left channel first, followed by right data. WSBD is low during left data transmission. Using $\overline{Q}$ of U2b, the AND gate is "on" during the left data transmission. Therefore both DACs clock in the 16 left channel bits. During the transmission of right data, WSBD goes high ($\overline{Q}$ goes low), turning "off" the clock to U5. Only the right channel (U4) clocks in the right data. After the LSB of right data is clocked into U4, both DACs can be simultaneously latched from the Q output of U2b.

PASSBAND ATTENUATION

All ripple-free low-pass filters have attenuation in the passband similar to Figure 4a. Typically, the corner frequency is approximately 30 kHz for many audio circuits. This results in signal attenuation at 20 kHz. The SAA7220 provides 1.0 dB of digital pre-emphasis in the 20 kHz passband with attenuation in the stopband as shown in Figure 4b. If the analog filter is designed such that the magnitude is 1 dB down at 20 kHz, the combined response will theoretically be flat in the passband as shown in Figure 4c.

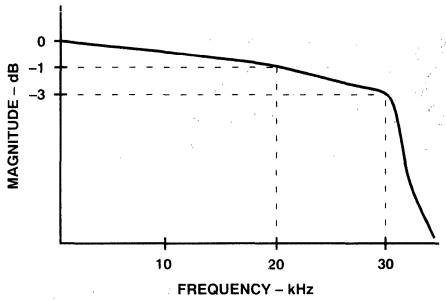

Figure 4a. Analog Filter Response

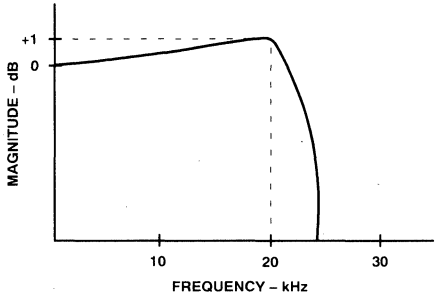

Figure 4b. Digital Filter Response

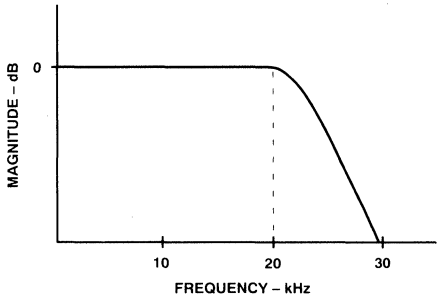

Figure 4c. Combined Response

Normally, Chebyshev or Elliptic filters, with very low ripple, would be required to achieve a flat response. However, these filters inherently have a poor transient response. A Bessel filter, which is optimized for linear phase, has essentially no overshoot or ringing associated with its step response. Additionally, the impulse response lacks oscillatory behavior. The Elliptic, Chebyshev, and even Butterworth filters all suffer from these shortcomings. The improvement in the transient response reduces the distortion of the overall circuit.

Figure 5 shows one such Bessel filter architecture. It's a 3rd order Sallen and Key filter with the −1 dB point of about 20 kHz. An advantage of this filter is that it uses only one op amp which reduces the component cost. A disadvantage is that the sensitivity (the change in magnitude to variations in the component values) increases dramatically as the order of the filter increases. The sensitivity of a third order filter is usually acceptable. Additionally, the capacitor values need to be modified to match available values. This causes the filter to roll-off slightly more than 1 dB at 20 kHz. Another design possibility is to use two op amps, cascading a two-pole filter and a one-pole filter. This would reduce the sensitivity of the filter and possibly achieve a more accurate −1 dB point.

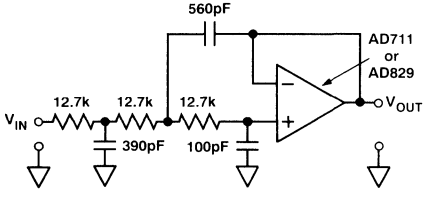

Figure 5. 3rd Order Bessel Filter

RESULTS

By combining the SAA7220's digital filter, the AD1856 (or even better, the AD1851), and a Bessel filter, an excellent system can be achieved. The result is a circuit with THD + N and SNR specifications comparable to the highest quality systems using Butterworth or Bessel filters, but additionally offering the flat frequency response of a system using a Chebyshev or Elliptic filter.

ACKNOWLEDGMENTS

To Bill Thompson for his input. To Steve Ruscak for his input and help throughout the project.

REFERENCES

1. L.P. Huelsman and P.E. Allen, *Introduction to the Theory and Design of Active Filters*, McGraw-Hill Publication Number: ISBN 0-07-030854-3.
2. Arthur B. Williams, *Electronic Filter Design Handbook*, McGraw-Hill Publication Number: ISBN 0-07-070430-9.

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Understanding LOGDACs™

by Jerry Whitmore

INTRODUCTION TO THE ANTILOG D/A CONVERTER

Analog Devices' AD7100 Series LOGDACs are CMOS multiplying DACs characterized by an exponential (antilogarithmic) digital-to-analog transfer function.

Perhaps the easiest way to visualize what a LOGDAC does is to compare it to two well-known circuits—the classic 3-terminal potentiometer and a CMOS multiplying DAC (digitally controlled potentiometer). As shown in Figure 1a through Figure 1c, the transfer function of all three circuits is of the form:

$$V_{OUT} = \alpha V_{IN} \qquad \text{EQN1}$$

WHERE:
α = attenuation factor
$0 \leq \alpha \leq 1$

In each case shown in Figure 1, α is a dimensionless number which can range from 0 (maximum attenuation) to approximately 1 (minimum attenuation). Additionally, each circuit has an analog input (V_{IN}), an analog output (V_{OUT}) and a mechanism for controlling the attenuation factor α.

The above in conjunction with Figure 1a through Figure 1c illustrates the similarity of the pot, M-DAC and LOGDAC functions. How, then does the LOGDAC *DIFFER* from the linear M-DAC?

The answer is resolution. The basic differentiating feature of the LOGDAC versus the linear multiplying DAC is the way resolution is specified.

RESOLUTION OF LOGDACs VERSUS LINEAR DACs

From Figure 1b, the attenuation factor α of a linear DAC is:

$$\alpha = \left(\frac{N}{2^n}\right) \qquad \text{EQN2}$$

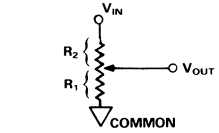
WHERE:
n = Number of digital input bits to the DAC
N = Integer value of DACs digital input

NOTE: Many treatments of multiplying DACs label the attenuation factor "D" where the digital input "D" is:

$$D = \alpha = \left(\frac{N}{2^n}\right) = \frac{\text{Bit 1}}{2^1} + \frac{\text{Bit 2}}{2^2} + \ldots \frac{\text{Bit n}}{2^n}$$

WHERE: Bit 1 through Bit n = 1 or 0
n = Number of bits

Since N was postulated to be an integer, the smallest possible change of N is plus or minus one count. The resolution of α is, therefore, ± 1 part in 2^n or 1 part in full scale. Important to realize is that the voltage resolution of a linear DAC is the same (barring differential nonlinearity effects) at all points on its transfer function.



$V_{OUT} = \left(\frac{R_1}{R_1 + R_2}\right)(V_{IN})$

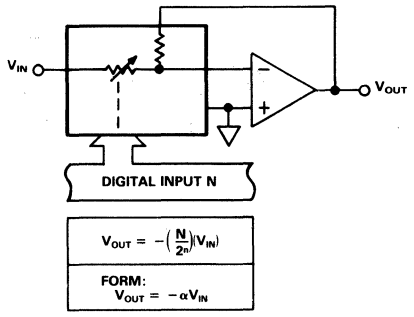
FORM:
$V_{OUT} = \alpha V_{IN}$

WHERE:
α = ATTENUATION FACTOR = $\left(\frac{R_1}{R_1 + R_2}\right)$

Figure 1a. Three Terminal Pot

The resolution of a LOGDAC is different, however. The following discussion shall endeavor to show that a LOGDAC's voltage resolution is different at all points on its transfer function, i.e., barring differential nonlinearity effects, the resolution expressed as a *percent of reading* (not percent of full scale) is constant throughout the LOGDACs range.

LOGDAC is a trademark of Analog Devices, Inc.

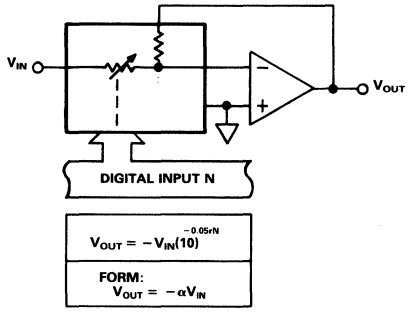


WHERE:
α = ATTENUATION FACTOR = $\left(\frac{N}{2^n}\right)$
n = NUMBER OF DIGITAL INPUT BITS
N = DIGITAL INPUT ($0 \cdot N \cdot 2^n-1$)

EXAMPLE: FOR 8-BIT DAC
$n = 8$, $2^n = 256$
$0 \cdot N \cdot 255$

$0 \cdot \alpha \cdot \left(\frac{255}{256}\right)$

Figure 1b. Linear Multiplying DAC (Digitally Controlled Pot)



WHERE:

α = ATTENUATION FACTOR = $10^{-0.05rN}$

N = DIGITAL INPUT
FOR AD7111: $0 \le N \le 239$
FOR AD7118: $0 \le N \le 59$
FOR AD7115: $0 \le N \le 199$

r = LOGDAC RESOLUTION IN dB

Figure 1c. LOGDAC (Digitally Controlled Pot)

From Figure 1c, the LOGDACs attenuation factor α is an exponential function (antilog) of the basic form:

$$y = a^{-x} \qquad \text{EQN3}$$

If base number 10 is chosen (other base numbers can be used, incidentally), the attenuation factor α for the LOGDAC of Figure 1c becomes:

$$\alpha = 10^{-\left(\frac{rN}{20}\right)} \qquad \text{EQN4}$$

WHERE:
N = Integer value of DACs digital input
for AD7115: $0 \le N \le 199$
for AD7111: $0 \le N \le 239$
for AD7118: $0 \le N \le 59$
r = LOGDAC resolution in dB
for AD7115: r = 0.1
for AD7111: r = 0.375
for AD7118: r = 1.5

Taking the LOG of both sides of EQN4 gives:

$$\log_{10}\alpha = -\left(\frac{rN}{20}\right)$$

$$20\log_{10}\alpha = -rN$$

$$\therefore \quad \alpha_{dB} = -rN \qquad \text{EQN5}$$

From EQN5, it is readily apparent that a plus one count change of N causes an attendant $-(r)$dB change in the attenuation factor α (and thus also a $-(r)$dB change in the DAC's output voltage).

Figure 2 is a graph of the general LOGDAC transfer function for the circuit of Figure 1c. It shows quite simply that increasing the digital input N causes a decrease in the output voltage V_{OUT}. Additionally, it shows the nonlinear relationship of V_{OUT} relative to N. Figure 3 is an expanded section of the transfer function shown in Figure 2. It illustrates the fact that the ratio of any two adjacent LOGDAC output voltage levels is the same throughout the transfer function. To further amplify the significance of this point, consider that a + one count change in the digital input N causes the output voltage to decrease in amplitude by a *fixed ratio relative to where it was before the change.* (At all points on its transfer function . . .) Thus, we have a DAC with *percent of reading* resolution as opposed to the linear DAC which defines resolution in terms of *percent of full scale.*

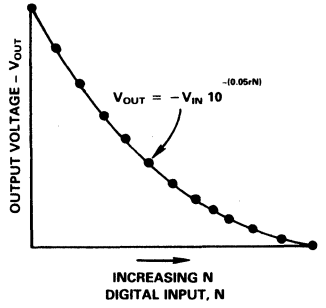


Figure 2. LOGDAC D/A Transfer Characteristic

To summarize, a linear DAC's voltage resolution is fixed throughout its transfer function. However, the LOGDAC

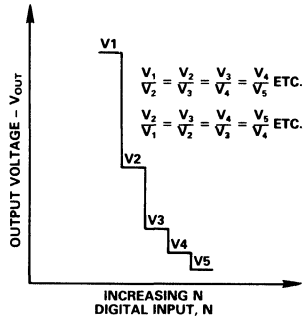


Figure 3. Expanded LOGDAC Transfer Function Illustrating the Concept of % of Reading Resolution

exhibits a continuously variable output voltage resolution throughout its transfer function range. The LOGDAC's voltage resolution is coarsest at or near full scale (0dB) and finest at or near 0 scale (mute). Table I shows the equivalent percent of reading resolution for various Analog Devices LOGDACs.

Model	dB Resolution ($\Delta N = \pm 1$ Count)	% of Reading Resolution ($\Delta N = +1$ Count)	($\Delta N = -1$ Count)
AD7118	±1.5dB	−15.9%	+18.9%
AD7111	±0.375dB	−4.2%	+4.4%
AD7115	±0.1dB	−1.1%	+1.2%

Table I.

BASIC CIRCUIT CONFIGURATIONS

ANTILOG DAC (Exponential with Negative Exponent)

The circuit of Figure 4 generates output voltage levels as determined by the equations:

$$V_{OUT} = -V_{IN}10^{\left(\frac{rN}{20}\right)} \quad \text{EQN6}$$

and/or

$$V_{OUT} = -V_{IN}e^{-(0.11512rN)} \quad \text{EQN7}$$

WHERE:

r = LOGDAC resolution in dB
- for AD7118: r = 1.5
- for AD7111: r = 0.375
- for AD7115: r = 0.1

N = Integer equivalent of digital input
- for AD7118: $0 \le N \le 59$
- for AD7111: $0 \le N \le 239$
- for AD7115: $0 \le N \le 199$

V_{IN} = ac or dc input voltage (nominal range ± 10V)

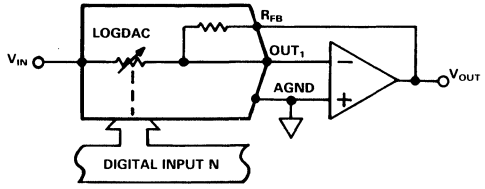


Figure 4. ANTILOG D/A Converter (Negative Exponent)

Features of the circuit of Figure 4 include:

1. It provides dB attenuation of V_{OUT} relative to V_{IN} as determined by the digital word N. (i.e., output range is 0dB to − dB)
2. The circuit provides % of *reading* resolution.
3. The analog input can be voltage or current, ac or dc, positive or negative polarity – i.e., the circuit is basically a CMOS multiplying DAC.

ANTILOG DAC (Exponential with Positive Exponent)

The circuit of Figure 5 is analogous to a multiplying DAC divider circuit. It provides signal gain of V_{OUT} relative to V_{IN} as determined by the equations:

$$V_{OUT} = -V_{IN}10^{+\left(\frac{rN}{20}\right)} \quad \text{EQN8}$$

and/or

$$V_{OUT} = -V_{IN}e^{+(0.11512rN)} \quad \text{EQN9}$$

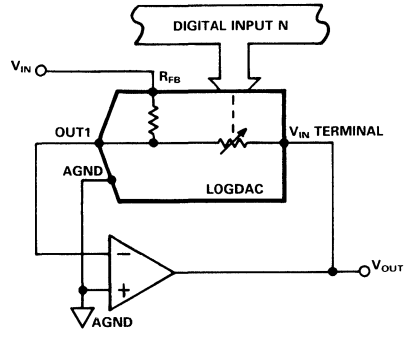


Figure 5. ANTILOG D/A Converter (Positive Exponent)

Basically, the analog input or reference voltage is applied to the on chip feedback resistor (RFB) and the amplifier output is connected to the V_{IN} terminal of the LOGDAC. The LOGDAC then ends up in the amplifier's feedback loop, thus the circuit provides *dB* gain of V_{OUT} relative to V_{IN} as determined by the digital input N (i.e., V_{OUT} range is 0dB to positive dB). As does the negative exponential DAC of Figure 4, this circuit provides % of *reading* resolution.

LOG OR LOG RATIO ADC

The circuit of Figure 6 provides an ADC function while performing a LOG compression. Its transfer function is:

$$N = \left(\frac{1}{-r}\right)\left(20\log_{10}\left|\frac{-V_{IN}}{V_{REF}}\right|\right) \qquad \text{EQN10}$$

OR

$$N = \left(\frac{8.68659}{-r}\right)\left(\ln\left|\frac{-V_{IN}}{V_{REF}}\right|\right) \qquad \text{EQN11}$$

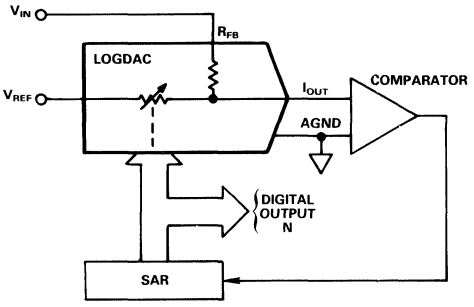


Figure 6. Log or Log Ratio A/D Converter

If the digital answer N (of EQN10) is multiplied by $-r$, the numerical value obtained is the dB value of the absolute value of V_{IN} relative to V_{REF} (answer 0dB to $-$dB).

If the digital answer N (of EQN11) is multiplied by $-r/8.68659$, the numerical value obtained is the natural log of the absolute value of V_{IN} relative to V_{REF}.

Circuit Constraints:

1. V_{IN} and V_{REF} must be of opposite polarity
2. $V_{IN} \leq V_{REF}$

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8th Order Programmable Low Pass Analog Filter Using Dual 12-Bit DACs

by Bill Slattery

INTRODUCTION

This application note describes the design of a low pass analog filter whose cutoff frequency can be programmed from 100Hz to 50kHz. The filter is designed as a plug in expansion board for IBM PC AT/XT* or compatibles. A high order filter function is implemented, giving a very fast roll-off in the transition band. This design realizes an 8th order function with a roll-off equalling 48dB/octave. The note also discusses some of the tradeoffs and practical limitations which must be considered when designing a filter.

The design is based on a 2nd order universal active filter, as shown in Figure 1. The required performance is achieved by cascading four of these 2nd order stages.

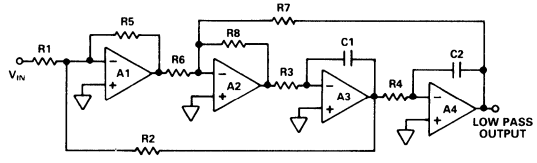


Figure 1. Universal Active Filter

The cutoff frequency of the filter is determined by R3, R4, C1 and C2. Digital control of the cutoff frequency is achieved by replacing resistors R3 and R4 in each stage by CMOS Multiplying Digital to Analog Converters (DACs). The DAC is in effect configured as a digitally programmable resistance.

To have accurate control of cutoff frequency, R3 and R4 within each stage must be closely matched. This is best achieved by replacing these two resistors with a monolithic dual 12-bit DAC. Analog Devices produces a range of suitable dual 12-bit DACs, the AD7537, AD7547 and AD7549. Since these have two DACs on one chip, DAC resistance matching will be in the order of 0.5%. Additionally, the use of 12-bit DACs ensures excellent resolution over the wide range of cutoff frequencies which can be programmed to the filter.

Applications for this filter include Industrial Process Control, Automatic Test Equipment (ATE), Sonar Signal Processing, Instrumentation, Audio Systems and Data Acquisition Systems. In Digital Signal Processing (DSP) applications, it can be used as the front end, low pass, anti-alias filter.

THE FILTER FUNCTION

A 2nd order low pass filter function is given by

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{A_O \omega_O^2}{s^2 + \frac{\omega_O}{Q} s + \omega_O^2} \quad (1)$$

where $s = j\omega$

ω_O = 3dB bandwidth (cutoff frequency)

Q = circuit Q factor

A_O = gain at $\omega = \omega_O$

The universal active filter shown in Figure 1 has a 2nd order low pass transfer function given by

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{\frac{R5\,R8}{R1\,R6}\left(\frac{1}{C1\ R3}\right)^2}{s^2 + \frac{R5\,R8}{R2\,R6}\left(\frac{1}{C1\ R3}\right)s + \left(\frac{1}{C1\ R3}\right)^2} \quad (2)$$

when $R3 = R4$

$R7 = R8$

and $C1 = C2$

By comparing coefficients between Equations (1) and (2) we see that

$$A_O = \frac{R5\,R8}{R1\,R6} \quad (3)$$

$$Q = \frac{R2\,R6}{R5\,R8} \quad (4)$$

$$\omega_O = \frac{1}{C1\,R3} \quad (5)$$

hence $$f_O = \frac{1}{2\pi\,C1\,R3} \text{ (filter cutoff frequency)} \quad (6)$$

*IBM PC AT/XT is a trademark of International Business Machines Corp.

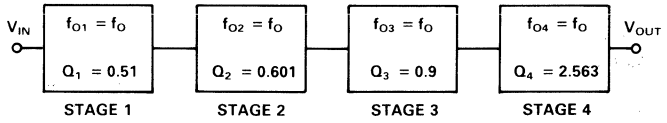


Figure 2. Block Diagram of 8th Order Butterworth Filter

8th Order Butterworth Filter Function

In realizing a particular 8th order filter function, each 2nd order stage is individually programmed to a specific cutoff frequency, f_O and Q. Values of f_O and Q for different filter types can be found using tables or software routines which are widely available (References 1 and 2).

The design discussed in this application note implements a unity gain, Butterworth filter function. The cutoff frequency which must be programmed to each stage is the same as the overall filter cutoff frequency f_O. The Qs of each stage, however are not the same. Figure 2 shows the required values of f_O and Q for each stage.

Since the gain of each stage is unity (A_O = 1), Equations (3) and (4) can now be solved using the values of Q given in Figure 2, to yield the required resistor values. Table I lists the required resistor values of each stage.

	Stage 1	Stage 2	Stage 3	Stage 4
R1	39k	150k	120k	12k
R2	20k	82k	82k	33k
R5	12k	82k	82k	3.9k
R6	10k	1.8k	2.7k	10k
R7	33k	3k	3k	33k
R8	33k	3k	3k	33k

1% tolerance resistors should be used.

Table I. Resistor Values for Each Stage of This 8th Order Butterworth Filter.

DIGITAL CONTROL OF CUTOFF FREQUENCY

The cutoff frequency of the filter is determined by C1, C2, R3 and R4. However, since C1 = C2 and R3 = R4, the cutoff frequency f_O can be expressed in the form shown in Equation (6).

Digital control over cutoff frequency is achieved by replacing R3 and R4 with one of the following configurations:

1. The AD7537 DAC.
2. The AD7537 DAC in series with a padding resistance R_{PAD}.

The principal difference between the AD7537, AD7547 and AD7549 is in their loading structure. The AD7537 is chosen for this design, see Figure 3. Its 2 byte (8 + 4) loading structure makes it ideal to use with a microprocessor based system which has an 8-bit data bus. The IBM PC AT/XT or compatible is just such a system.

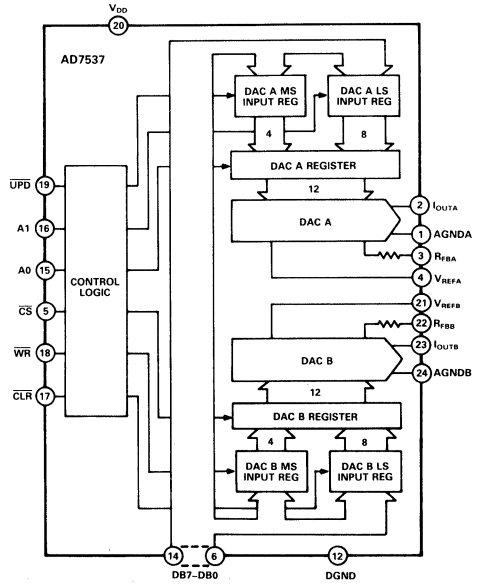


Figure 3. Functional Block Diagram of AD7537

The AD7537 is a dual 12-bit current output DAC which comes in a space saving 24-pin 0.3" wide package. The AD712 op amp is chosen for this design. It is a high performance, low-cost dual op amp. Its large Gain Bandwidth Product ensures excellent performance of the filter for cutoff frequencies up to and beyond 50kHz. (For more detailed information on the AD7537 and AD712 consult the relevant data sheets.)

Design (1)

Figure 4 shows how R3 and R4 are replaced by the AD7537 dual DAC. The AD7537 is now in effect a pair of programmable resistors.

The equivalent resistance of a DAC in this configuration is given by

$$R_{EQ} = \frac{R_{DAC}}{D} \quad (7)$$

where R_{DAC} is the DAC ladder resistance

and D is the digital fraction programmed to the DAC. D is given by

$$D = \frac{N}{2^n} \quad (8)$$

where n = resolution of DAC in bits (in this case n = 12)

N = DAC digital code (decimal 1 to 4095)

Since R3 is now replaced by R_{EQ} we can write

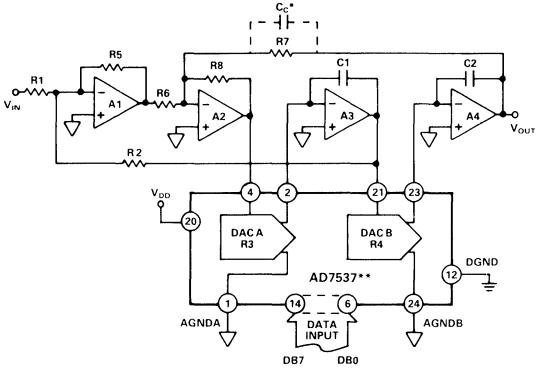
$$f_O = \frac{1}{2\pi C1 R_{EQ}} \quad (9)$$

Choosing C1 = 220pF and R_{DAC} = 14k

and solving between Equations (7), (8) and (9), the cutoff frequency can be written as a function of the decimal code N.

$$f_O = (0.01262 \cdot N)\ kHz \quad (10)$$

In practice the cutoff frequency can now be programmed between 100Hz and 50kHz with a resolution of 13Hz.



*See "GAIN BANDWIDTH PRODUCT SECTION".
**ADDITIONAL CIRCUITRY OMITTED FOR CLARITY.

Figure 4. Single Stage of Programmable Filter Using an AD7537

For a known DAC ladder resistance, a stage can be accurately programmed to a specific cutoff frequency. The two frequency controlling resistors are effectively matched to within 0.5%, since both are in one monolithic package. However, to achieve an overall accurate filter cutoff frequency, the DACs in each of the four stages must have similar DAC ladder resistances. DAC ladder resistance can vary between 9k and 20k with a typical value of 14k, for different AD7537s.

Design (2)

One solution that can be adopted to avoid using specially selected AD7537s is to use a padding resistance R_{PAD} in series with the DAC ladder resistance as shown in Figure 5. A large value of R_{PAD}, 100k, is used. This has the effect of desensitizing the variations in DAC ladder resistance. This means that the specified variation in DAC ladder resistance now has an insignificant effect on the overall filter performance.

The equivalent resistance of a DAC in this configuration is given by

$$R_{EQ} = \frac{R_{DAC} + R_{PAD}}{D} \quad (11)$$

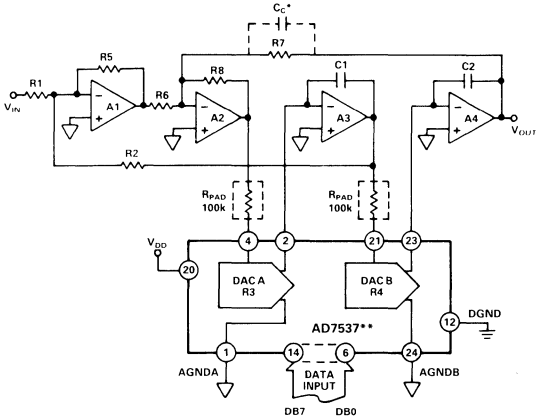
Choosing C1 = 22pF, R_{PAD} = 100k and R_{DAC} = 14k

and solving between Equations (8), (9) and (11), the cutoff frequency can be written as a function of the decimal code N.

$$f_O = (0.01549 \cdot N)\ kHz \quad (12)$$

The cutoff frequency can now be programmed between 100Hz and 50kHz with a resolution of 16Hz.

It should be noted that since we are using DACs whose ladder resistance can vary between 9k and 20k, the above expression for f_O will be accurate to within ±4.5%. If the padding resistance R_{PAD} was not used, f_O could vary by up to ±30% of the programmed value. Design 1 does not have this problem since DACs whose ladder resistance is known to be 14k are used. Cost and accuracy tradeoffs must be considered when choosing either of the two design options.



*See "GAIN BANDWIDTH PRODUCT SECTION".
**ADDITIONAL CIRCUITRY OMITTED FOR CLARITY.

Figure 5. Single Stage of Programmable Filter Using an AD7537 and Series Resistances R_{PAD}

GAIN BANDWIDTH PRODUCT

A compensation capacitor C_C must be used on the 4th Stage of the filter. This is required to reduce effects caused by Gain Bandwidth Product limitations. The value of capacitance depends on the type of function implemented and the design option choosen.

For this 8th Order Butterworth Filter, the value of the capacitor can vary between 15pF and 47pF

Design (1) – Use 15pF

Design (2) – Use 47pF.

DIGITAL INTERFACE

The filter circuit can be built on a standard IBM prototype card and plugged directly into the expansion slot on the main board of an IBM PC AT/XT or compatible. The prototype board basically consists of buffers and some circuitry which generates an enable line $\overline{EN}$. Figure 7 shows the interface layout used. Each AD7537 is addressed ($\overline{CS}$) using a 74LS138 (3 to 8 line decoder). Address lines A3 to A5 as well as the $\overline{EN}$ and $\overline{IOW}$ lines are used to decode each address. The valid addresses which can be used are HEX300 to HEX31F.

Since the AD7537 is a dual 12-bit DAC, data is loaded to each DAC with a 2-byte (8+4) loading instruction. Address lines A0 to A1 select DAC A and DAC B, see Figure 3, as well as selecting the low and high bytes of data. The address decoder also generates the $\overline{UPD}$ line which is used to update the data in all the DACs.

An IBM Basic program for this Butterworth filter is given in Table A1, Appendix 1. The program is run by inputting the required cutoff frequency in kHz as well as the values of R_{DAC}, R_{PAD}, and C1. The program calculates and outputs the relevant digital code to each of the DACs. Figure 6 gives a flow diagram representation of the program used.

PERFORMANCE

Plots of amplitude and phase response as well as a plot of the noise spectrum for the 8th Order Butterworth Filter are given in Appendix 2.

Figure A1 shows the amplitude response of the filter using Design 1. Plots for four different cutoff frequencies are given in this figure. The programmed cutoff frequency is found to be within 3% of the actual cutoff frequency achieved, for each of the four cases. Passband ripple is in the order of 0.2dB. Stop-band rejection is greater than 100dB, except for frequency components between 2kHz and 4kHz, and at 41kHz and 1MHz, where rejection is in the order of 90dB. The reduction in attenuation at lower frequencies is mainly due to the increased value of DAC equivalent resistance R_{EQ}. As the value of resistance increases, so too does the level of noise increase. In practice, frequencies below 500Hz should not be programmed to the filter with the component values used in this design option. Cutoff frequencies of less than 500Hz can however be achieved if larger values of capacitance C1 are used. This effectively reduces the range of selectable cutoff frequencies but allows lower cutoff frequencies with a reduced noise floor to be programmed to the filter. At high frequencies, greater than 10MHz, it is found that there is less attenuation; attenuation reduces below 90dB. This is due both to gain bandwidth limitations of the op amp and feedthrough across the system.

Figure A2 shows the amplitude response for various cutoff frequencies, using Design 2. Again we can see that the pass band ripple is less then 0.2dB. The accuracy of the cutoff frequency however will vary by about 4.5% from the programmed cutoff frequency. Also, it should be noted that in using Design 2 stopband rejection will be reduced to about 70dB. This is due to increased noise caused by the large value of padding resistance R_{PAD}. This can be reduced somewhat by using low noise resistors.

Figure A3 is a plot of the noise spectrum at the output of the filter, using Design 1. The cutoff frequency is programmed at 50kHz, and the input is grounded.The largest noise component in our system occurs at about 41kHz and has an amplitude of −54.8dBm* (0.4mV). Since the filter is present in a noisy environment, i.e., the board of an IBM PC AT/XT or compatible, it is not surprising that there should be noise present in the system. In practice, there is a minimum input signal level that can be applied to the filter to achieve a specific Signal-to-Noise Ratio (SNR) in the filter's pass band. In this design, using the noise component at 41kHz, an SNR greater than 90dB can be achieved by applying input signal levels of greater than 1.3V rms.

***Measured with respect to 50Ω.**

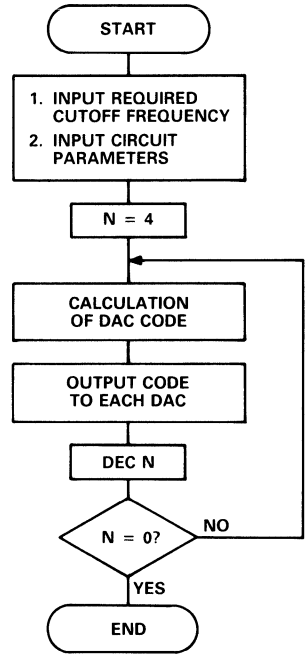


Figure 6. Flow Diagram Representation of Control Algorithm

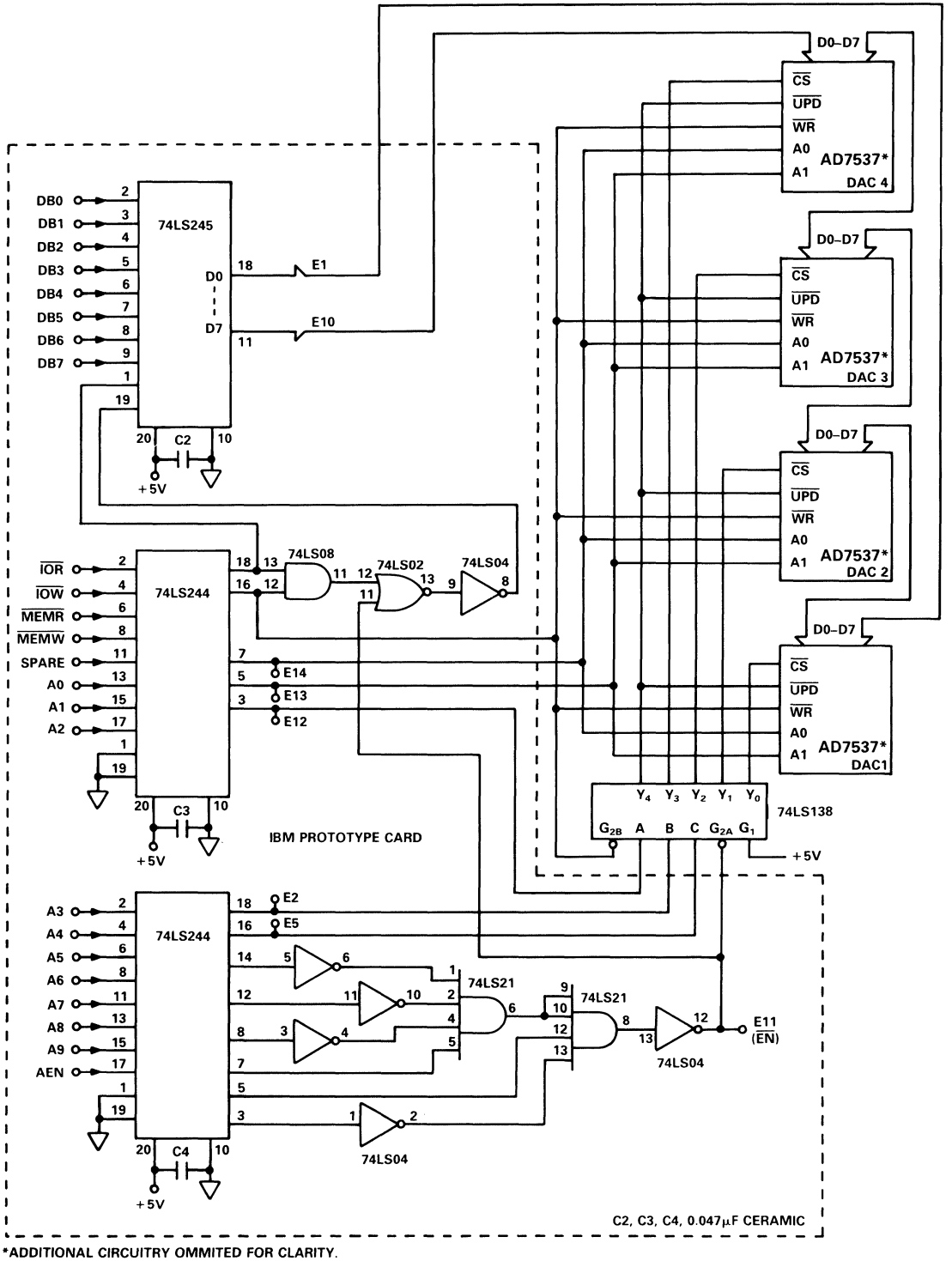
Figure A4 is a plot of the filter's phase response. The phase response of the system determines the Group Delay of the filter.

$$\text{Group Delay} = \frac{1}{2\pi}\frac{d\phi}{df}$$

Thus a linear phase response implies a constant group delay. The phase response plot shown exhibits some slight nonlinearity. This is as expected for a Butterworth filter function. If phase response is an important design consideration, a different filter function should be considered, eg., Bessel. (References 1 and 2.)

PERFORMANCE EXTENSION

1. The frequency range of this filter can be extended to 100kHz, using Design 1, by simply replacing the 220pF capacitors in each stage by 110pF capacitors. Stopband attenuation of 85dB and passband ripple of less than 0.2dB is achieved over the full range.
2. A Chebychev response can be achieved by using different values of R1 and R2 in each stage. R1 and R2 can be evaluated by solving Equations (3) and (4) for the values of Q given in Figure 8. Figure 8 gives the cutoff frequency f_O and Q for each stage of a 0.2dB ripple 8th Order Chebychev Filter. It should be noted that for a Chebychev filter the cutoff frequency of each stage is



*ADDITIONAL CIRCUITRY OMMITED FOR CLARITY.

Figure 7. IBM PC AT/XT Digital Interface

not the same as the overall filter cutoff frequency, as was the case with the Butterworth filter. The remainder of the design proceedure is the same as that outlined for the Butterworth filter. An IBM Basic program for this Chebychev filter is given in Table A2, Appendix 1. This program tunes each individual stage to its particular cutoff frequency so that a specified overall filter cutoff frequency is achieved.

3. Programmability over filter type (i.e., Butterworth, Chebychev, Bessel, etc.) as well as cutoff frequency can be achieved by replacing R1 and R2 of each stage by an AD7537. This gives us total software control over all the filter parameters.

CONCLUSION

Filtering in the analog domain has many inherent advantages over filtering in the increasingly popular digital domain. Analog filtering is a continuous time process whereas digital filtering is a sampled data process. Digital filters require extensive software routines to implement such algorithms as FIR and IIR filters. The analog filter utilizes digital processing power to control the filter while giving analog performance.

This application note deals with the IBM PC AT/XT or compatible as the digital controller for the analog filter. The filter could equally be controlled using any other microprocessor. Suggested microprocessor interfaces are given in the AD7537, AD7547 and AD7549 data sheets.

ACKNOWLEDGEMENTS

To Mike Curtin for suggesting the original design idea. To Sean Morley for his help in building and testing the circuit.

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1. L.P. Huelsman and P.E. Allen, "Introduction to the Theory and Design of Active Filters." McGraw-Hill Publication Number: ISBN 0-07-030854-3.
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3. A.D. Delagrange, "An Active Filter Primer, Mod 1" NSWC Publication Number: TR 82-552.
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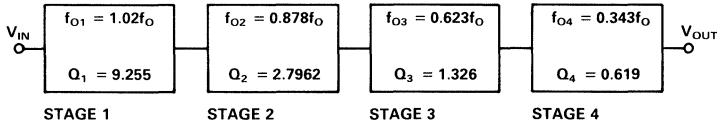

Figure 8. Block Diagram of 8th Order Chebychev Filter

```
10  CLS
20  PRINT "8th-Order Low-Pass Butterworth Filter"
30  PRINT
40  INPUT "F0 (kHz) (500Hz . . . . 48kHz)                    = ";FO
50  F0 = F0*1000
60  PRINT
70  INPUT "RDAC(Kohms) (14K TYPICALLY)                       = ";RDAC
80  RDAC = RDAC*1000
90  PRINT
100 INPUT "RPAD(Kohms) (0 FOR DES.1, 100K FOR DES.2)         = ";RPAD
110 RPAD = RPAD*1000
120 PRINT
130 INPUT "C(pFarads) (220pF FOR DES.1, 22pF FOR DES.2)       = ";C
140 C = C*1E-12
150 REQ = 1/2/22*7/FO/C
160 N = 4096*(RPAD + RDAC)/REQ
170 PRINT                                                     = ";HEX$(N);"H"
180 PRINT "CODE
190 N = INT (N)
200 N1 = INT(N/256)'   MSB
210 N2 = N-N1*256 '   LSB
220 ADDR = &H300
230 FOR C = 0 TO 3
240 OUT ADDR,N2
250 OUT ADDR + 1,N1
260 OUT ADDR + 2,N2
270 OUT ADDR + 3,N1
280 ADDR = ADDR + 4
290 NEXT C
300 OUT &H310,0 'UPDATE DACS
310 END
```

Table A1. IBM Basic Program for 8th Order Butterworth Filter

```
10  CLS
20  PRINT "8th-Order Low-Pass Chebychev Filter"
30  PRINT
40  INPUT "F0 (KHz)                                          = ";FO
50  F0 = F0*1000
60  PRINT
70  INPUT "RDAC (Kohms)  (14K TYPICALLY)                     = ";RDAC
80  RDAC = RDAC*1000
90  PRINT
100 INPUT "RPAD(Kohms)  (0 FOR DESIGN 1)                     = ";RPAD
110 RPAD = RPAD*1000
120 PRINT
130 INPUT "C(pFarads)  (220pF FOR DES. 1)                    = ";C
140 C = C*1E-12
150 FOR I = 0 TO 3
160 READ X
170 FC = X*FO
180 REQ = 1/2/22*7/FC/C
190 N = 4096*(RPAD + RDAC)/REQ
200 PRINT
210 PRINT "CODE" ;I;"                                        = ";HEX$(N);"H"
220 N = INT(N)
230 N1 = INT(N/256) '   MSB
240 N2 = N-N1*256 '   LSB
250 ADDR = &H300
260 ADDR = ADDR + I*4
270 OUT ADDR,N2
280 OUT ADDR + 1,N1
290 OUT ADDR + 2,N2
300 OUT ADDR + 3,N1
310 NEXT i
320 OUT &H310,0'UPDATE DACS
330 END
340 DATA 1.02,.878,.623,.343
```

Table A2. IBM Basic Program for 8th Order Chebychev Filter

APPENDIX 2

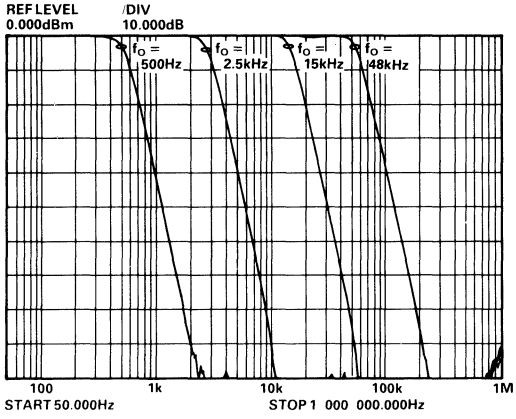

Figure A1. Amplitude Response of Butterworth Filter for Various Cutoff Frequencies Using Design 1.

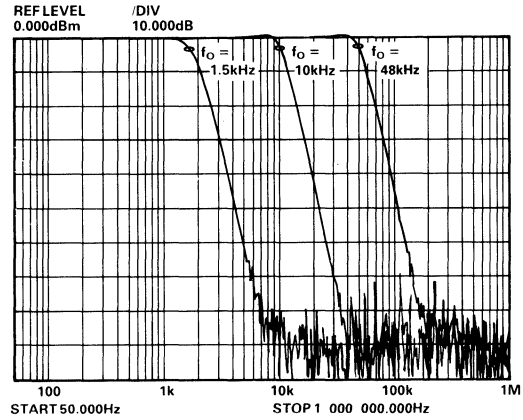

Figure A2. Amplitude Response of Butterworth Filter for Various Cutoff Frequencies Using Design 2.

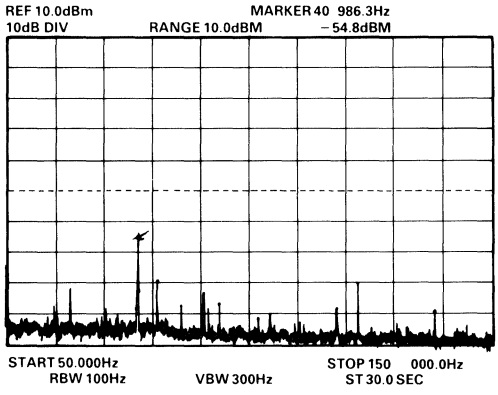

Figure A3. Noise Spectrum of Filter

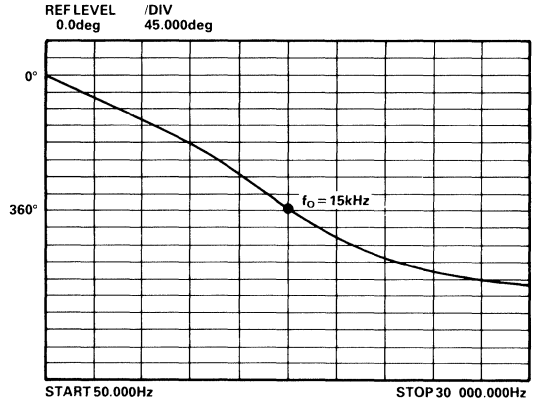

Figure A4. Typical Phase Response of Butterworth Filter

ANALOG DEVICES

AN-211
APPLICATION NOTE

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The Alexander Current-Feedback Audio Power Amplifier*

by Mark Alexander

This application note was written by Mark Alexander, who received his BSEE from the University of Toronto in 1981. As a consultant to Analog Devices, Mark describes a unique power amplifier topology that is the result of his long standing interest in audio power amplifier design and critical listening of audio systems.

The current-feedback approach presented here meets the traditional audio requirements of power amplifiers, but also adds the additional benefit of very high speed and bandwidth (200 V/μs slew rate, 1 MHz bandwidth) that results in excellent dynamic performance, and hence, sound quality.

INTRODUCTION

The subject of power amplifier design is one of those controversial areas of audio engineering that continues to receive intense debate, despite the fact that there are literally dozens of papers available to guide the designer. Many different topologies have evolved from the relatively modest beginnings of solid state power amplifier design in the late 1950s and early 1960s, and this has lead to a few very unique and original designs. A substantial number of transistorized amplifiers that were built during these early years were little more than redesigns of vacuum tube circuits with lower voltage supply rails, and often had performance levels that left a great deal to be desired. Quite a few of them sounded significantly worse than their thermionic predecessors. The "real revolution" in audio power amplifier design actually occurred during the 1970s and introduced such new innovations as direct coupling, fully complementary design, pseudo Class A biasing, and current dumping; not to mention the discovery of the importance of dynamic intermodulation distortion testing and its relationship to slew rate. Unfortunately, the plethora of so called "new" amplifier designs that have proliferated since this period are often variations of older circuits that originated during the 1970s, and generally feature only slight modifications to the input, output or gain stages.

Some designers have demonstrated rail-commutated output stages, which allow them to improve the operating efficiency of a big amplifier to such an extent that the huge amount of output transistor heat sinking usually necessary is reduced to that of a much lower power design. These can suffer from "switch over" distortion caused by the output stage switching between different supply rails, and can be quite objectionable. Certainly, high output power should not be obtained at the expense of inferior operating specifications, but this is indeed the case with certain types of amplifiers. Some clever design techniques do achieve quite impressive performance, however, albeit at the expense of greatly increased circuit complexity. Still other amplifiers dispense completely with the familiar principles of negative feedback, and their creators claim that their circuitry provides a sound more "open and lifelike," even though the distortion performance is usually poor. On the whole, though, most audio power amplifiers are essentially discrete copies of monolithic voltage feedback op amps, such as the 4136, but are invariably simplified to reduce the transistor count.

The purpose of this technical note is to introduce the audio designer to a truly new power amplifier topology, not an adaptation of an existing design, that offers exceptional performance on a par with the best of the available solid state designs (voltage feedback or otherwise). This new topology completely dispenses with the principles of global voltage feedback, so commonly used in most amplifiers, in favor of a design based instead on the principles of current feedback. In addition, this note addresses many of the important practical aspects of successfully getting a design off the ground, aside from choosing the basic core amplifier design. In almost all cases, having a good basic amplifier topology is not enough to guarantee that the final piece of equipment will perform to the original design expectations. Consequently, additional topics such as board layout,

***Patent pending. The amplifier described herein is for informational purposes only with restricted use and no licenses implied. Readers are permitted to construct one stereo amplifier for their own personal, noncommercial use. For other uses, contact Analog Devices for licensing details.**

component selection, paralleling output devices, placement of high current wiring, and thermal design are considered as well.

A LITTLE BACKGROUND ON FEEDBACK

Before dissecting the new audio amplifier circuit in detail, some background on the differences in operational characteristics between voltage feedback and current feedback amplifiers is appropriate. Since it is likely that the reader may not have been previously exposed to the latter, an overview of voltage feedback followed by a look at the advantages of current feedback is necessary. This discussion will allow one to understand why circuits that make use of this relatively new topology are so important. Because the bandwidth of an audio amplifier is usually one of the most important specifications, a relatively simple equation for the upper −3 dB point is essential. Simplifying the current feedback amplifier and its attendant feedback network into a representative circuit model for nodal analysis provides the key to arriving at a compact, but reasonably accurate, expression for the frequency response. Appendix A has complete details of the circuit analysis.

The theoretical analysis of a voltage feedback circuit that often accompanies its frequent criticism has been well described in other works,[1] and thus will not be reiterated here. Since the original impetus behind the development of this new power amplifier design was a general dissatisfaction with the performance achievable by voltage feedback circuits, some discussion of their disadvantages is worthwhile. This will serve to set the stage for the in-depth discussion of current feedback amplifier analysis, in Appendix A. Although the analysis section can be skipped without disrupting the continuity of this note, the reader is encouraged to review it.

Constant gain bandwidth characteristics, resulting from the application of voltage feedback, present a problem if one requires reasonably high gain while simultaneously achieving wide closed-loop bandwidth. Some very high voltage power amplifiers may require gains as high as 50, for example, plus a bandwidth of several hundred kilohertz which obviously means that a gain bandwidth product in the range of 10 MHz to 20 MHz is needed. This is not easy to achieve, especially in a high voltage design. An additional problem with voltage feedback amplifiers is that their slew rate is usually limited by the transconductance stage which has a finite maximum output current, normally equal to the tail current of the differential input transistor pair, available to charge the compensation capacitor. High slew rate is very desirable in a large-signal audio power amplifier and mandates the use of large input-stage tail currents and small compensation capacitor values. Unfortunately, in the interests of amplifier stability, reducing the value of the compensation capacitor requires some degeneration of the input stage (to reduce its transconductance) which thus reduces the open-loop gain. This action reduces the loop gain available in the audio band and causes an increase in THD products, since it is the loop gain that serves to reduce the open-loop amplifier distortion, most of which originates in the highly nonlinear output stage. What all this boils down to is the fact that a difficult trade-off has to be made between stability, open-loop gain, and slew rate without compromising the overall ac performance and transient response. Clearly, a global voltage feedback scheme may not necessarily be the optimum choice for ultrahigh performance audio power amplifiers, and in some cases it will not even be possible to meet all the design goals using this topology.

Current feedback operational amplifiers were originally introduced because they overcame the bandwidth variation, inversely proportional to closed-loop gain, exhibited by voltage feedback amplifiers. They still show a slight variation of bandwidth, however, as the gain is increased above unity, but it is much less significant than with the latter. In fact, current feedback amplifiers don't begin to behave like voltage feedback amplifiers until the closed-loop gain is made quite large (~50). The simplified model of a current feedback amplifier in Figure 1 shows that it uses a unity gain input buffer whose output current is fed, via a bidirectional current mirror, into a transimpedance gain stage. The voltage generated here is then buffered and fed to the output terminal. Typical values for R_T are quite high, usually several hundred kilohms or even a few megohms. R_{INV} is the output resistance of the input buffer, and feedback resistors R_1 and R_2 set the input-to-output voltage gain in a fashion somewhat similar to that of a conventional op amp. Here, however, it is an error current I_1 that sustains the output voltage and not an error voltage.

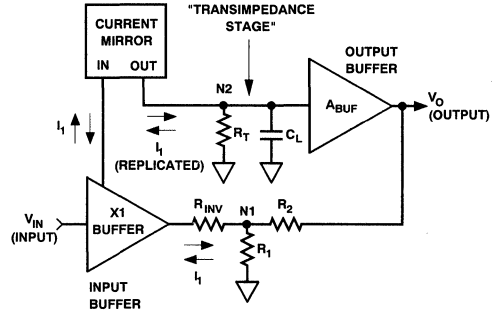


Figure 1. The Model of a Current Feedback Amplifier Shows that an Error Current, I_1, Determines the Overall Output Voltage.

The concept of a finite gain bandwidth product can also be applied to a current feedback amplifier as a measure of its performance, although it is only meaningful at high gains. Arguably, the most important attribute of this topology is that the amount of current available to charge the compensation capacitor during output slewing is proportional to the difference between the actual and final output voltages, just like a simple RC circuit. As such, there is theoretically no slew rate limit with this topology, which makes it very attractive for an audio power amplifier. Practical circuit limitations inevitably

impose a restriction on the maximum current level that can be handled in the gain stage of a current feedback amplifier, however, and it is this limiting that gives rise to a finite slew rate. Still, the slew rates achievable with these types of circuits are often higher by as much as a factor of 5 (or greater) than their voltage feedback counterparts, for a given quiescent supply current. Current feedback represents a much more logical choice for a power amplifier than voltage feedback, and this will be demonstrated.

POWER AMPLIFIER CIRCUIT TOPOLOGY

Prior to looking at the actual amplifier circuit, the simplified block diagram of Figure 2 will be considered to help understand how the overall design works on a system level. This will make the final amplifier circuit easier to follow. As may be gathered from Figure 2, this is a rather unconventional design, in which there are two op amp input stages feeding a single gain stage and power output buffer. By considering this design one block at a time, however, it is becomes easier to grasp the way in which each of the major sections interacts with one another.

The Input Stage

The input buffer used in this power amplifier is simply a conventional voltage feedback op amp chosen for its excellent audio characteristics, and reasonably high output current capability. This ensures that the limiting factor in terms of overall amplifier performance will be the current feedback gain block and not the input stage. The output current from input amplifier A_1 is taken from its power supply pins and fed to the emitters of a pair of common base cascode transistors that provide regulated dc voltages for the op amps. At first glance this might appear to be a very strange connection, because the power supply pins of A_1 are used as outputs and its output is used as an input. However, this is in accordance with the model shown in Figure 1 since the output current from the input buffer must be fed, via the bidirectional current mirror, into the transimpedance gain stage. It is here that the high output voltage is ultimately generated, prior to buffering by the unity gain output stage. The half-wave rectification action of A_1's output current, due to its class AB output stage, causes the two current mirrors to receive complementary input currents. When A_1 is sourcing output current, it causes a corresponding increase in the current of the upper mirror and a decrease in that of the lower mirror. This forces the voltage at the output of the transimpedance stage to swing positive. For cases where A_1 is sinking current, exactly the opposite is true. A current mode gain stage arrangement such as this is fully complementary and truly push-pull, which means it should exhibit low even-order distortion. Note that the quiescent supply current of A_1 conveniently serves to bias the two current mirrors that sit referenced to each power supply rail, thus providing an appropriate operating point for the transimpedance stage and bias voltage generator.

In most commercially available current feedback amplifiers, the input buffer stage has a gain of unity and is generally of an open-loop design. Here, an op amp is being used as the input stage instead and thus can be configured to provide some gain. This is extremely easy to do since it only involves tapping the shunt resistor to ground at the output of A_1. The overall amplifier midband gain is therefore:

$$A_V = \left(1 + \frac{R_7}{R_6}\right)\left(1 + \frac{R_8}{R_6 + R_7}\right) \qquad (1)$$

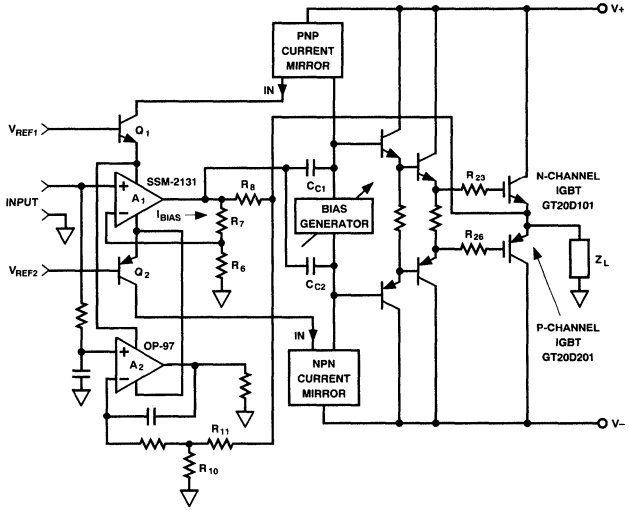


Figure 2. A Simplified Block Diagram of the Amplifier Shows that the Input Amplifiers, A_1 and A_2, Feed a Common Gain Stage and Output Buffer.

The Gain Stage and Frequency Compensation

The outputs of the two current mirrors that are connected to each supply rail feed an adjustable voltage bias generator which provides the necessary bias for class AB operation of the complementary MOS-IGBT (Metal-Oxide-Semiconductor Insulated-Gate-Bipolar-Transistor) output stage. The bias generator is designed to have very low output impedance over the operating frequency range of the amplifier. Compensation is provided by C_{C1} and C_{C2}; two capacitors are used instead of one to keep the structure of the gain stage symmetrical. Unlike the simplified current feedback model shown in Figure 1, this design has the compensation capacitors returned to the feedback summing node instead of ground. This alternate connection has a very beneficial effect on the amplifier step response when it is loaded by a fairly low value impedance such as a loudspeaker.

An IGBT emitter follower output stage, such as the one used in this amplifier, has a transfer function that contains two poles and a real zero plus the usual dc gain term of slightly less than unity. When the amplifier drives high values of load impedance, such as the feedback resistors alone, the two output stage poles are quite high in frequency (usually above 20 MHz), and contribute little excess phase shift within the amplifier's passband. Quite a different situation arises when a load is connected to the output of the amplifier. The two poles in the output stage now split apart, and the dominant one becomes sufficiently low in frequency that it contributes excess phase shift at lower frequencies within the amplifiers' passband. This can cause a considerable problem if the compensation scheme in Figure 1 is used since it may result in undesirable ringing on the edges of a square wave. The compensation scheme of Figure 2 overcomes this problem by inserting a high frequency closed-loop zero that tends to make the amplifier more stable. Also, this compensation arrangement allows the use of smaller capacitors than with the original scheme. Appendix A shows the complete response of the amplifier when this alternate compensation scheme is used. If we assume that the small signal transresistance, R_T, is quite high and also that the output buffer gain is near unity, then the closed-loop pole and zero will occur at frequencies given by:

$$f_{POLE} \cong \frac{1}{2\pi\left(2R_8 + \frac{R_8}{R_6 + R_7} R_{INV}\right) C_{C12}} \quad (2)$$

and

$$f_{ZERO} = \frac{\left(1 + \frac{R_8}{R_6 + R_7}\right)}{4\pi R_8 C_{C12}} \quad (3)$$

where C_{C12} is the sum of C_{C1} and C_{C2}. Notice that the frequency at which the zero occurs is approximately equal to the closed-loop bandwidth multiplied by the gain of the current feedback loop, if R_{INV} is fairly small in value. These equations, plus Equation (1), are the necessary design formulas needed to determine the gain and small signal bandwidth of this amplifier. Later on it will be demonstrated that the mathematical theory and actual measurements made on the circuit do indeed correlate very well with each other.

Driver and Output Stages

This part of the power amplifier design is quite conventional, relatively speaking, and no attempt was made to use error correction or pseudo class A biasing schemes to lower the output stage crossover distortion. Since the primary design objective for this amplifier was wide bandwidth and high slew rate, it was felt that any additional circuitry following the transimpedance gain stage might degrade the closed-loop stability. Besides, low crossover distortion can be achieved by running the output transistors at a sufficiently (but not excessively) high idling current. A simple double emitter follower driver stage, therefore, was chosen to buffer the voltage generated by the gain stage and feed it to the gates of the power IGBTs. This driver stage is capable of providing several hundred milliamps of charging current for the IGBT gate capacitances while the output is slewing, and is mandatory in a high speed design such as this.

DC Control Amplifier

The purpose of this additional input stage is to provide an accurate, low drift, dc gain path to the main output that is independent of the ac gain path and its poor dc characteristics. In the original version of this amplifier, expensive precision matched NPN and PNP dual transistors were used in the two current mirrors, but no dc control amplifier was used. It was incorrectly assumed that precise matching of the transistors in each mirror would result in very low output offset voltage, as long as the input buffer had reasonably low input offset voltage as well. As it happens, this is not the case with a current feedback amplifier. Any mismatch between the two current mirrors results in a finite amount of bias current appearing at the output terminal of the input buffer, which must flow through feedback resistor R_8 to the output. It cannot flow through R_6 and R_7 to ground, because the current in these resistors is set only by the voltage appearing at the output of the input buffer. The output offset voltage, without the dc control amplifier is thus:

$$V_{OOS} = V_{IOS\,(A1)}\left(1 + \frac{R_7}{R_6}\right)\left(1 + \frac{R_8}{R_6 + R_7}\right) + I_{BIAS} R_8 \quad (4)$$

Normally, V_{IOS} (A_1) can be made quite small by using a low offset op amp. Unfortunately, the output terminal bias current, I_{BIAS}, can be as large as 100 μA under static conditions and even larger if a thermal gradient exists between the two mirrors on the power amplifier driver board. This can easily lead to an output offset in excess of 100 mV, which changes as the amplifier warms up. A large offset like this is likely to cause an audible click when the relay that connects the loudspeakers to the amplifier is energized, and is generally undesirable.

The solution to these problems is a low frequency servo-loop that controls the dc output voltage, independently of any low frequency current or voltage fluctuations in

the main current feedback gain path. This is facilitated by the use of a second low power precision op amp, A_2, that is configured as an integrator with very low crossover frequency (less than 5 Hz). The low crossover frequency ensures that the integrator will not have any effect on the performance of the overall amplifier in the audio band. Voltage feedback is applied from the main output back to the input of the integrator through resistors R_{10} and R_{11}, which set the closed-loop dc gain. This gain is made equal to that given by equation (1). Since A_2 drives a resistor connected to ground, as shown in Figure 2, it behaves as an operational transconductance amplifier with the output current taken from its power supply terminals. This compensating output current is then fed to the two common-base regulator transistors where it is summed with the signal current from the power supply terminals of A_1. The output current of A_2 is thus forced to cancel I_{BIAS} almost exactly because the dc gain of the integrator, coupled with the additional gain produced by the transimpedance stage, is very high. Consequently, the integrating control loop completely overrides the current feedback loop at dc and the output offset is reduced from that given by Equation (4) to:

$$V_{OOS} = V_{IOS\,(A2)}\left(1 + \frac{R_{11}}{R_{10}}\right) \qquad (5)$$

This means that it can be made arbitrarily small through the choice of a low offset amplifier for A_2. Here the cost of an additional op amp is more than offset by not having to use expensive matched NPN and PNP dual transistors in the current mirrors.

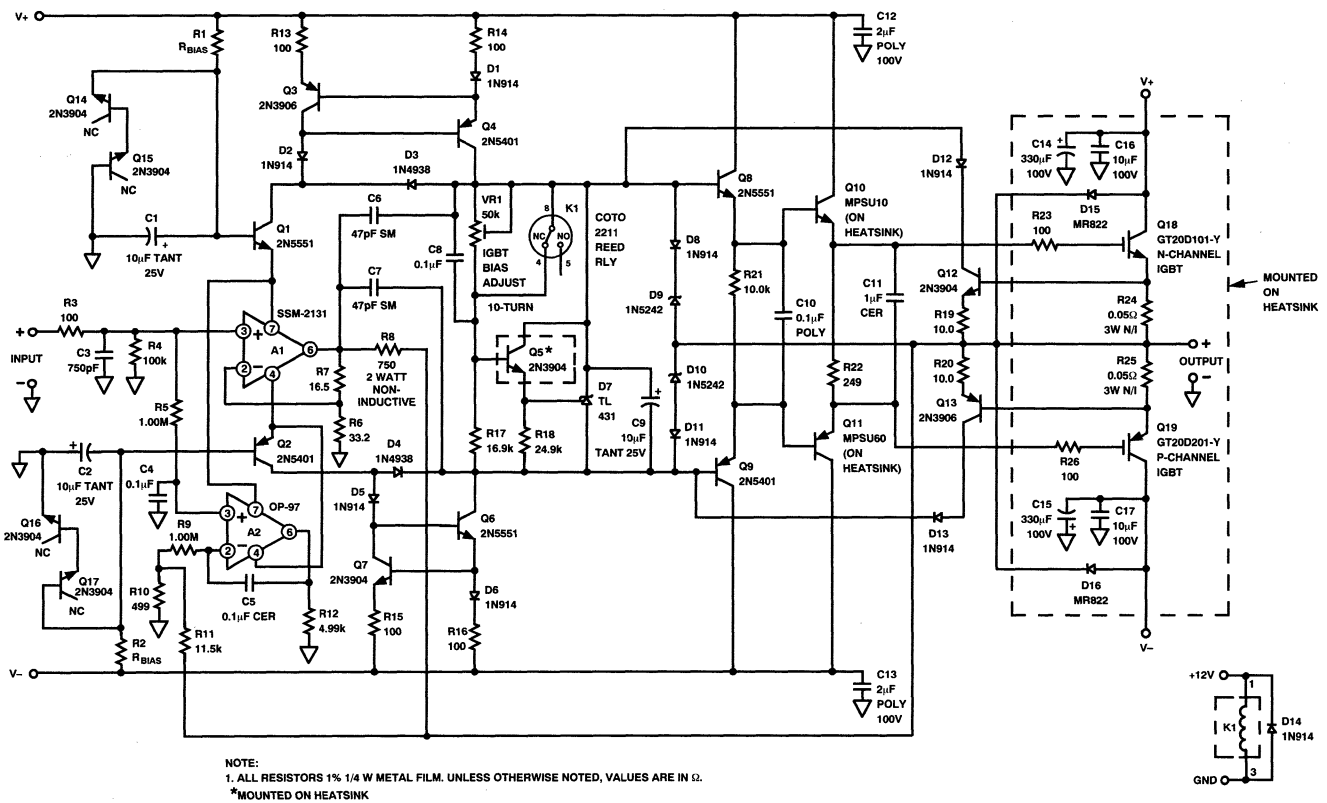
AMPLIFIER CIRCUIT DESIGN

The complete circuit diagram for one channel of the amplifier is shown in Figure 3, and an accompanying parts list is included in Appendix B. This design utilizes 2 IC op amps, 17 bipolar transistors in the gain and driver stages, and at least 2 complementary IGBT power transistors from Toshiba in the output stage. These recently introduced devices are essentially similar to power MOSFETs in that they have a very high impedance input terminal (the gate) and square-law transfer characteristics, but are manufactured using a slightly modified double diffused MOS process. Unlike power MOSFETs, however, they feature consistently higher current handling capability for N- and P-channel transistors of a given die size. This allows one to get by with a smaller die size IGBT output stage than one using MOSFETs, thus providing a fairly substantial cost savings (especially on the P-channel transistors). The driver stage in this amplifier can easily accommodate multiple pairs of power devices in the output stage, because of its high peak current drive capability, but just a single pair of 250 V, 20 A IGBTs was used in the version that was characterized here. Power supply voltages for the driver board and output stage may range from ±20 V to ±75 V. Most of the components that mount on the compact driver board, the layout of which is shown in Figure 4, are quite readily available and inexpensive.

An input filter with a cutoff frequency of approximately 2 MHz precedes the input stage. It was included to reduce the potential for RF interference problems, and to eliminate the possibility of the amplifier oscillating on power-up with the input left floating (something that was noticed during the original development of this topology). The filter is formed by the 100 Ω input resistor and 750 pF shunt capacitor. A 100 kΩ resistor is connected to ground at the input of A_1, and provides the necessary dc bias current path to ground if the input is inadvertently left open. The overall amplifier gain is set by R_6, R_7, and R_8, and substituting the values of these resistors into equation (1) yields a figure of 24.087 or 27.64 dB. If more gain from the circuit is desired, the values of R_6 and R_7 should be changed, but their sum should be kept approximately equal to 50 Ω so that the gain of the current feedback section stays constant (at about a factor of 16). By simply swapping the 16.5 Ω and 33.2 Ω resistors, for example, the gain of the input stage becomes approximately equal to 3, and the gain of the overall amplifier increases to a factor of 48.47 or 33.7 dB. In fact, the gain of the input stage can be made as large as 20 dB before its bandwidth drops below that of the rest of the amplifier.

The references for the two common-base regulator transistors (Q_1 and Q_2), which provide stable supply voltages for the op amps, are actually two pairs of standard NPN bipolar transistors (2N3904s) used as Zener diodes (Q_{14} through Q_{17}). They are connected in series (with their collector leads clipped off) to obtain a net breakdown voltage of around 15 V for the pair . There really is a good reason for using such an arrangement since it would obviously be easier to use a 15 V "Zener" diode, as opposed to this seemingly more complicated approach. In reality, the connection of two bipolar transistors in this manner exhibits significantly less low frequency noise than the 15 V "avalanche" diodes, as they are more appropriately called, and is actually more cost effective. The composite Zeners are bypassed with 10 μF 25 V tantalum capacitors, used mainly for reasons of economy and size, which filter out residual noise from the diodes as well as the power supply rails. Two resistors marked R_{BIAS} on the circuit diagram (R_1 and R_2), which are connected to each supply, serve to bias Zener connected transistors Q_{14} through Q_{17} and should be chosen such that with nominal power supply operating voltages (anywhere from 50 to 70 volts) about 1 mA of current will flow through them.

The two Wilson current mirrors connected to each rail, and fed from the collectors of Q_1 and Q_2, are formed from a low voltage transistor, a diode and a high voltage transistor (2N5551 or 2N5401). They are degenerated somewhat with 100 Ω 1% resistors to improve matching. Anti-saturation diodes (D_2 through D_5) have been included to prevent storage time problems with the cascode transistors (Q_4 and Q_6) in either of the two mirrors during clipping, and this results in extremely rapid recovery from overdrive. It should be noted that the onset of clipping in the transimpedance stage will occur at



NOTE:
1. ALL RESISTORS 1% 1/4 W METAL FILM. UNLESS OTHERWISE NOTED, VALUES ARE IN Ω.
*MOUNTED ON HEATSINK

Figure 3. The Complete Amplifier Circuit Diagram Shows that Inexpensive Small-Signal Silicon Is Used Throughout to Minimize Overall Cost.

about 2 V from either power supply rail for very small overdrive conditions, but hard clipping in this stage will actually be dependent on the current limit of the input amplifier A_1. This occurs because, during hard clipping, the current summing network connected to the output of A_1 is no longer balanced and significant current can flow in its output stage. Consequently, the current in the mirrors increases very rapidly up to the value of A_1's maximum output capability (usually 30 mA to 40 mA), causing a corresponding voltage drop across the aforementioned 100 Ω resistors. The effect of this excessive current in the mirrors is such that it causes the clipped signal to "pull in" slightly from the rails, as the amplifier is driven harder and harder into its overload region. It is very important not to let the circuit stay in this condition for any significant period of time, since the power dissipation in Q_1 and Q_2 will increase far beyond their nominally rated value of a few hundred milliwatts. Peak dissipation in these transistors can reach as much as 1.5 W to 2 W, with typical rail voltages of 50 to 70 volts; therefore, very large dc input signals or low frequency square waves should be avoided. If these operating conditions are anticipated, however, clip-on heat sinks for Q_1 and Q_2 are mandatory.

Frequency compensation in this particular design is provided by two 47 pF compensation capacitors that are connected to the feedback summing node (C_6 and C_7), as mentioned previously. This results in a total value of 94 pF. The reason such a large value of capacitance was chosen is quite simple: it completely swamps out any nonlinear voltage dependent capacitances that are present at the high impedance gain node, resulting in constant amplifier bandwidth as the supply voltage is varied. Concerns about too low a slew rate, with such large compensation capacitors, are usually justified in a voltage feedback amplifiers, but here there is as much as 30 mA of current available to charge them and slew rate limiting will not normally be encountered.

A calculation of the expected frequency response of the amplifier is now in order, and can be accomplished quite easily by substituting the value of 94 pF for C_{C12}, and the values of 750 Ω for R_8, 16.5 Ω for R_7, and 33.2 Ω for R_6 into Equation (2). The value for R_{INV} is a little more difficult to determine since we must know *a priori* what the value of the closed-loop output resistance of A_1 is, at the overall −3 dB point of the amplifier. The solution to this problem actually involves a little bit of circular reasoning, but the motive behind it is rather easy to see. If Equation (2) is evaluated initially without considering the effect of R_{INV}, a closed-loop bandwidth of 1.12 MHz is calculated. Since the effect of a finite R_{INV} is to lower the bandwidth somewhat, a prediction of the final amplifier closed-loop bandwidth will allow an initial guess for this parameter to be made. In this case a prediction of a final closed-loop bandwidth of 1 MHz is made. If we now take the open-loop output resistance of A_1 from its data sheet (about 70 Ω) and divide it by one plus the value of its loop gain at the predicted −3 dB point of 1 MHz (about 7.68), a value of 9.11 Ω is obtained. When this estimate for R_{INV} is included in Equation (2), an overall closed-loop bandwidth of 1.034 MHz is the final result. This is really very close to the original guess of 1 MHz, and it seems that no further iteration will be necessary to get closer to an acceptable answer. It should now be plainly apparent that extraordinarily wide closed-loop bandwidth seems rather easy to come by in a current feedback power amplifier, even when the compensation capacitors are quite large. For this reason, careful board layout and wiring techniques are of tantamount importance in actually getting a design such as this to work properly without oscillating.

The output stage bias voltage generator, connected between the collectors of Q_4 and Q_6, is formed from a programmable shunt regulator (D_7), with an NPN emitter-follower buffer (Q_5) driving its control input. This buffer is not normally required in most applications because the control input bias current of D_7 (a TL431) is only a few microamps, but it is included here for thermal compensation of the output stage idling current. A common problem with biasing output stages that use vertical DMOS devices (MOSFETs and IGBTs) is that at moderately low current levels, the decrease in V_{TH} of approximately 3 mV/°C causes the collector current to increase for a fixed gate-to-emitter bias voltage. If transistor Q_5 is securely mounted on the same heat sink as the power IGBT output stage, its V_{BE} will decrease as the output transistors heat up. This decrease in V_{BE} of about 2 mV/°C, which is multiplied up in the bias generator by approximately a factor of three, thus helps to stabilize the quiescent current in the IGBT output stage. A form-C relay can also be included across the 50 kΩ bias adjustment pot (VR_1), as shown, to allow the amplifier to be powered up with zero bias voltage on the output transistors. This feature, when used in conjunction with resistive surge protection schemes for the main filter capacitors (and bridge rectifiers) during power up, will prevent any static voltage drop across the current limiting resistor due to the amplifier class AB idling current.

Some means must be provided, as well, to protect the output transistors from any condition that could cause their gate-to-emitter voltages to exceed the maximum allowed value of ±20 V. Thus, Zener diodes D_9 and D_{10} are connected from either side of the bias generator to the main output, and prevent the voltage seen between the gain stage and the emitters of the IGBTs from exceeding more than about 12 V.

The IGBT output stage is operated in a complementary emitter-follower configuration running at an idling current of about 100 mA, and series gate resistors R_{23} and R_{26} are included to limit the frequency response. This mitigates any tendency, in the fairly wideband output stage, towards parasitic oscillation. Current in the output stage is sensed across two low value resistors, R_{24} and R_{25}, connected in series with the emitters of the IGBTs. As the voltage drop across either of these two resistors increases towards 0.7 V, Q_{12} or Q_{13} will begin to conduct current away from the gain stage and thus limit the

output voltage. This is a convenient way to limit the current in the output stage to a safe value. Emitter degeneration resistors (10 Ω) must be used in conjunction with the two limiter transistors, Q_{12} and Q_{13}, because this circuit has quite a bit of gain when active and tends to oscillate slightly at high frequencies. Since these transistors must sink or source all the current from the transimpedance stage (up to the current limit of A_1) when the output current is being limited, the voltage across the 10 Ω resistors will increase slightly as the amplifier is driven into hard limiting. This causes a corresponding increase in the actual value of limited current, resulting in a somewhat "soft" limiting curve.

Of course, current limiting alone is not enough to guarantee power transistor integrity if short circuits to ground at the output are anticipated. This results from the fact that excessive power dissipation in the output stage will still occur if the current limit is set fairly high (actually a very desirable attribute in a modern amplifier). Fusing the power supply feed to the output stage will usually be necessary for protection of the power transistors.

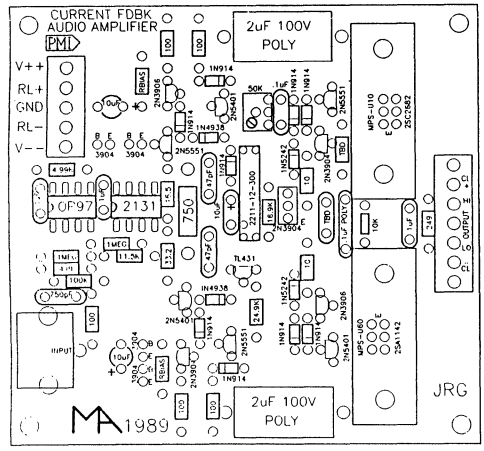
PRACTICAL CIRCUIT CONSIDERATIONS

It is often mistakenly assumed that once a respectable topology has been chosen for a power amplifier, it is a simple task to construct a completed unit that meets all the original design goals. In fact, getting the physical details of an amplifier's construction properly sorted out can be just as time consuming as the actual design of the driver electronics themselves.

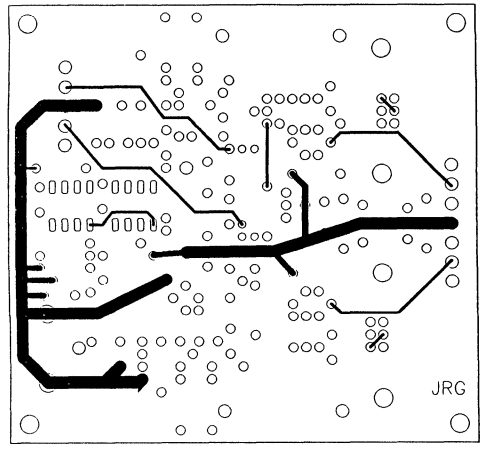
Circuit Board Layout

This is probably one of the most critical elements for a wide bandwidth audio power amplifier. The key to good board layout for this design is to keep trace lengths to an absolute minimum wherever possible, and to keep the overall layout very small in physical size. Figure 4 shows the layout of the board used to characterize this new topology, and as can be seen, the component packing density is reasonably high—it measures less than 9 cm on a side. The layout of the driver board actually follows the amplifier circuit diagram fairly closely in orientation, since it was begun on the left hand side where the input stage resides, and finished on the right where the output stage drivers are located.

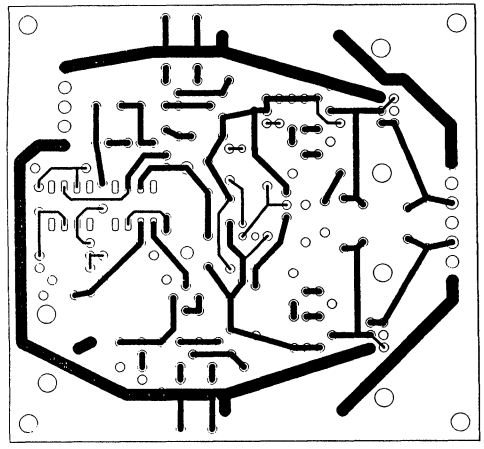
Power supply busses travel along the top and bottom edges of the board, thus providing a convenient means of picking off power for the various stages. The two polyfilm bypass capacitors on the board actually have their own ground return paths that are independently isolated from the signal ground bus near the input stage. This may seem a like a subtle refinement, but on the original layout the bypass capacitors shared the same ground bus as the input stage, and strange low level oscillations were noticed on the first prototypes. It turned out that the oscillation was occurring as a result of the discharging of the bypass capacitors into the driver transistors (and ultimately the gates of the output



a. Topside Silkscreening



b. Topside Layout



c. Bottomside Layout

Figure 4. A Compact Driver Board Contains All Amplifier Circuitry Except the IGBT Output Stage.

transistors) due to an initial perturbation in the circuit. This initial disturbance eventually lead to a self sustaining relaxation oscillation (of a few hundred hertz) because the ground bus surge, as the capacitors were discharging, was sufficiently large so as to be coupled back into the input stage of the amplifier. The improved layout of Figure 4 does not exhibit this anomaly.

Critical Component Selection

Some of the resistors in this design require great care in their selection, since the wrong type of resistive element will lead to unexpectedly poor performance. In particular, the 750 Ω feedback resistor R_8 should be an oversized completely noninductive metal film power resistor with a dissipation rating of at least 2 W (remember that the peak current in this component may be as high as 75 mA). Failure to use a resistor with a high enough power rating will very likely lead to thermal modulation of the actual resistance value and a corresponding increase in overall amplifier intermodulation distortion when large low frequency input signal components are present. Additionally, a low temperature coefficient of resistance is very desirable for this part. The current sensing resistors in the output stage (R_{24} and R_{25}) should also be of the low or noninductive variety. Since the short rise time of the amplifier (approximately 350 ns) means that a large di/dt in the load, and hence these resistors, can occur, any excessive inductance will cause the voltage across them to increase during fast edge transitions thus causing premature current limiting.

Input amplifier A_1 plays a significant role in the overall performance of the amplifier. It must possess all the desirable characteristics of a good line level audio op amp (namely low distortion, high slew rate and wide gain bandwidth product), plus it must have good output current capability as well. The SSM2131 BiFET audio op amp with a GBW of 10 MHz and slew rate of 40 V/μs more than meets the requirements for this design. Also, amplifier A_2 in the integrating dc control stage must have very low input offset current in addition to low offset voltage. This is because 1 MΩ resistors are used, in series with its input pins, to obtain the long time constant needed in this stage. Too large an input offset current would cause a sufficiently large differential dc error to appear across these resistors (many mV) and it would render a low input offset voltage op amp totally useless. The OP-97 adequately satisfies these requirements with an input offset current of only 30 pA and offset voltage of 30 μV.

Paralleling Output Transistors

This is an extremely important topic because most amplifiers will use more than one pair of output transistors per channel, so that low impedance loads can be accommodated without the output stage self-destructing. Since the maximum power dissipation in the output stage increases with decreasing load impedance, it is desirable to ensure adequate static and dynamic current sharing amongst all the output transistors. This will minimize the junction-to-case temperature rise in any one output device. Power MOSFET output stages can be effectively made to share current by means of tight thermal coupling between all transistors, and through the inclusion of appropriately valued series source-ballasting resistors. There is no reason to believe that power IGBT output stages, with their very similar square law transfer characteristics, will behave any differently if the same techniques are employed.

Typically for best current sharing in a MOSFET output stage, the value of the source resistors should be $>>1/gm$ of each transistor over its desired drain current range. Since the transconductance is lowest at the output stage quiescent point, using this value of gm should guarantee sharing over the full output current range. Unfortunately, in practice this may lead to rather large resistance values and correspondingly large voltage drops when high values of load current are being delivered. A better solution is to do a limited amount of prescreening on the N- and P-channel IGBTs to eliminate any devices with larger than average characteristic deviations in V_{TH} and gm (at the idling point). Once this is done, it becomes feasible to use series emitter resistors in the range of 0.2/gm to 0.5/gm, which will help to minimize the voltage drop. For the Toshiba IGBT output devices used in this design, the typical gm at an emitter current of around 100 mA is close to 1S. For example, if an eight transistor output stage is needed that must have a total idling current of 400 mA, series emitter resistors in the range of 0.2 Ω to 0.5 Ω are acceptable along with some limited screening of the output transistors prior to installation.

Wiring Techniques

Some amplifier designers relegate power supply and output terminal wiring to the lowest level of the design phase. However, since these wires may carry large pulsating currents with a harmonic content well above the audio band, it pays to devote some attention to this task. Wiring is probably one of the most critical things that must be accomplished successfully, if the final design is to get anywhere close to the performance measured on a prototype breadboard (where the wires are normally quite short). Usually the layout of the power supply wiring is not particularly well controlled, but some very simple rules should be observed that will maximize the likelihood of success at first power up.

One of the most important rules in wiring layout is to use twisted pairs for the forward and return currents paths in any loop. This minimizes the series inductance of the conductors, since inductance increases with cross sectional loop area. Thus all power supply wires from the filter capacitors to the amplifier output stage(s) (and driver boards) should be twisted together, as shown in the system connection diagram of Figure 5. Fuses are placed in series with the power rails to protect the output stage in the event that an accidental short circuit in the load occurs. They should be of the fast blow type, and must be rated appropriately so that they will not

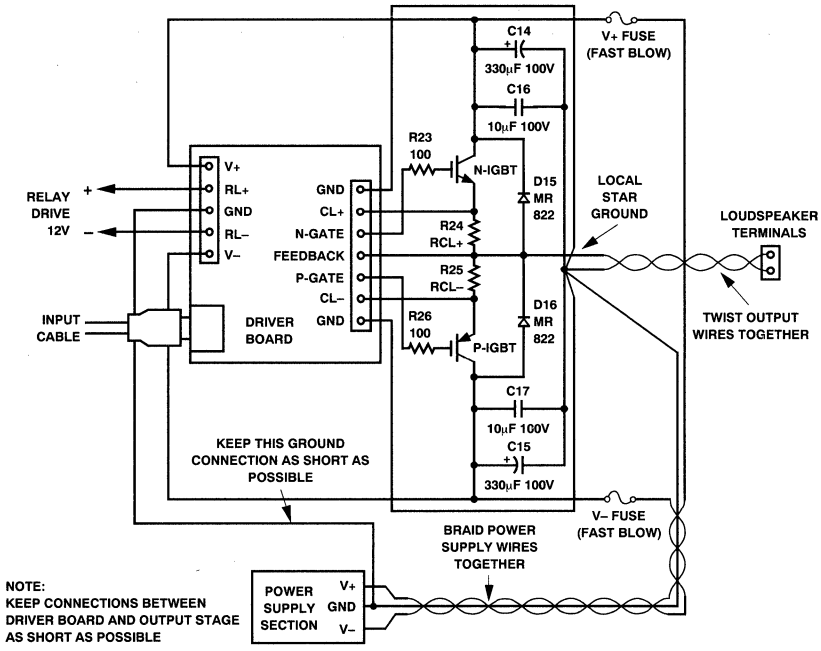


Figure 5. A Power Wiring Scheme Requires Proper Attention to Detail If Low Distortion Is to Be Achieved.

open up under peak output power levels. The wires that run from the output stage to the loudspeaker connectors should also be twisted together, as shown, to minimize their inductance. All interconnections between the driver boards and their respective output stages should be kept very short, in the interests of closed-loop stability. The series gate resistors for the IGBTs should be connected directly at the package terminals of these devices.

These tips are all a definite step in the right direction, but there is something else to consider that is decidedly not obvious. Since the positive and negative supply leads which feed the output stage(s) have half-wave rectified current waveforms, as shown in Figure 6, the harmonic current (occurring at even multiples of the fundamental output frequency) circulates in the loop formed between the power supply capacitors and the output transistors[2]. If there is any mutual inductance between these power supply leads and the output terminal loop, after the point at which negative feedback has been extracted, even order distortion components can be induced in the output that cannot be attenuated by the feedback action of the amplifier. For a typical amplifier with $R_L = 8\ \Omega$ and sinusoidal excitation, then at an output frequency f = 10 kHz, the induced second harmonic component in the output loop will be approximately 0.33% per μH of mutual inductance. It should be noted that the magnitude of the induced distortion components is proportional to the output frequency (i.e., they get larger as the frequency goes up), which can be minimized by keeping the power input and speaker wiring runs perpendicular to each other. Thus the output transistors should be physically connected to the power supply feed and output terminal cabling as shown in Figure 7. This approach minimizes the mutual coupling between the power input and output paths of the amplifier.

Heatsinking and Thermal Considerations

Heatsink selection should never be underestimated because it is one of those critical areas that, if neglected, will inevitably result in damage to the output transistors from excessive junction temperature. In most class AB power amplifiers, the total dissipation in the output stage is split equally between the two banks of output transistors (the N-channel units and the P-channel units). An equation that relates the power supply rail voltage and load impedance to the total maximum output stage power dissipation, under sinusoidal excitation, is given by:

$$P_{DISS}(max) = \frac{2\ V_{CC}^2}{\pi^2 |Z_L| \cos\theta} \qquad (6)$$

where θ is the phase angle of the load. As an example, consider the case of an amplifier with a two transistor output stage powered by ±60 V rails, and loaded by an impedance of 8 Ω with a phase angle of +30°. Under these conditions the maximum dissipated power will be 105.3 W. The Toshiba N- and P-channel IGBTs are rated for 180 W dissipation at a T_C of 25°C, but this is derated to zero at a T_C of 150°C. The junction-to-case thermal resistance ($R_{\theta JC}$) for these transistors is calculated by dividing the total difference in case temperature change (125°C) by that of the total change in power dissipation

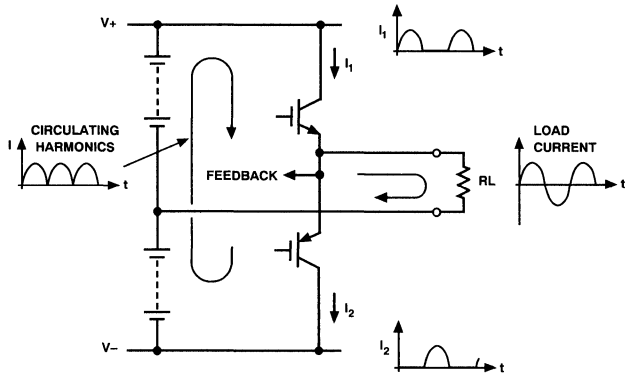


Figure 6. Harmonic Currents in a Power Amplifier Circulate Between the Supplies and the Class AB Output Stage.

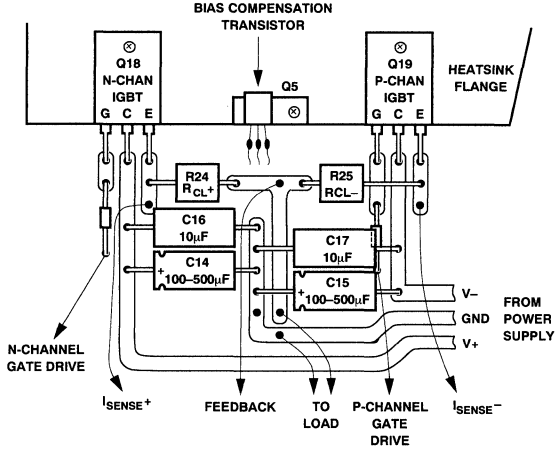


Figure 7. The Preferred Output Stage Layout and Component Placement

(180 W). This results in a figure of 0.694°C/W. Since the total power dissipated in the output stage is split equally between the two transistors, the effective $R_{\theta JC}$ is equal to 0.694/2 or 0.347°C/W. To ensure that the output stage transistors do not reach their maximum allowed junction temperature of 150°C, the total thermal resistance from junction-to-ambient (assuming T_A = 25°C) must not be greater than 125°C/105.3 W or 1.19°C/W. When the junction-to-case thermal resistance of the total output stage is subtracted from this number, we are left with the net allowed case-to-ambient thermal resistance ($R_{\theta CA}$) of 0.843°C/W. This value includes any thermal resistance due to the insulating washers that must be used to prevent the transistors from making electrical contact with the heat sink (often as much as 0.3°C/W per insulator). Thus in reality, some allowance for the interface materials must be made in the choice of the final extrusion which will provide heatsinking for the power transistors. In the example here, a large finned heatsink with a sink-to-ambient thermal resistance ($R_{\theta SA}$) of around 0.69°C/W is required. Of course, had two pairs of transistors been used in the output stage, the net $R_{\theta JC}$ would have been lower by a factor of two and a smaller extrusion could have been used for the heatsink. Thus there is a limited trade-off that can be made between the number of transistors and the size of the output stage heatsink, for a given power supply rail voltage and load impedance.

MEASURED PERFORMANCE

Table I provides a synopsis of the overall performance of the current feedback power amplifier using the new complementary IGBT output devices. Although this design does not achieve astoundingly low distortion levels typical of more complex topologies that employ linearization schemes in the output stage, the measurements made show that the THD and IMD generated by this circuit are still respectably low. Figure 8 shows that the overall harmonic distortion at 50 W output into an 8 Ω load is a minimal 0.001% at 1 kHz, rising to just under 0.009% at 20 kHz. This is a particularly good result considering that only one pair of output transistors has been used. Also, no low-pass LR isolation network has been used in series with the output that would tend to

attenuate the high frequency harmonics. This would artificially improve the amplifier performance in the vicinity of 20 kHz, and was deliberately excluded. SMPTE intermodulation distortion for 60 Hz and 7 kHz mixed 4:1 is plotted in Figure 9 as a function of the rms input level and, as the curve indicates, it is extremely low being just 0.0004% at 41.7 W into 8 Ω (0.92 V rms input). The absence of any significant upward slope in the curve of Figure 9, except where the amplifier is entering its overload region at about 0.95 V rms input, indicates a lack of thermal modulation effects on the 750 Ω feedback resistor.

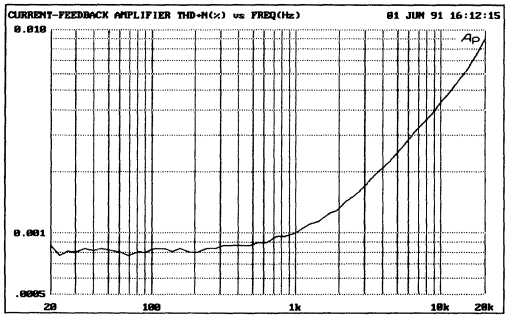


Figure 8. Amplifier THD Is Below 0.009% Throughout the Audio Band When Delivering 50 W to An 8 Ω Load.

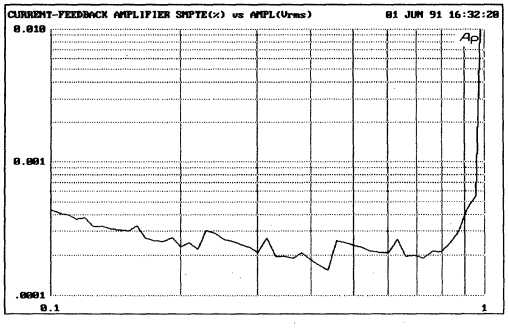


Figure 9. SMPTE Intermodulation Distortion (60 Hz/7 kHz 4:1, 40 W into 8 Ω) Is Exceptionally Low, Reaching Almost 0.0002% Before Rising as the Amplifier Enters its Overload Region.

Table 1. Summary of Amplifier Performance (V_{SUPPLY} = ±40 V, Current Limited to 2.5 A Average Per Rail, R_L = 8 Ω)

Sine Wave Power Output (Voltage Limited)	70 W
Total Harmonic Distortion at 1 kHz	0.001% at 50 W
Total Harmonic Distortion at 20 kHz (Depends Strongly on Idling Current Level in Output Stage)	0.009% at 50 W
SMPTE Intermodulation Distortion	0.0004% at 41.7 W
Dynamic Intermodulation Distortion (DIM-100)	0.0012% at 50 W
Frequency Response (−3 dB)	DC to 1 MHz
Slew Rate	>200 V/μs
Rise Time (Input Filter in Circuit)	400 ns
Total Quiescent Supply Current	130–150 mA

Static distortion measurements aside, what does put the current feedback topology into a class of its own is the dynamic performance. High slew rate is always critical in any large signal amplifier design, but proper waveform control during the reproduction of a square wave is just as important. Because of the nature of the gain stage arrangement in this amplifier, slew rate limiting occurs at a very large rate of change (typically 250 V/μs). Most normal program material is unlikely ever to cause slew limiting in this amplifier, even with large output swings. Consequently, the value measured for the DIM-100 dynamic intermodulation distortion test is a very low 0.0012% at 50 W output into 8 Ω, as shown in Figure 10.

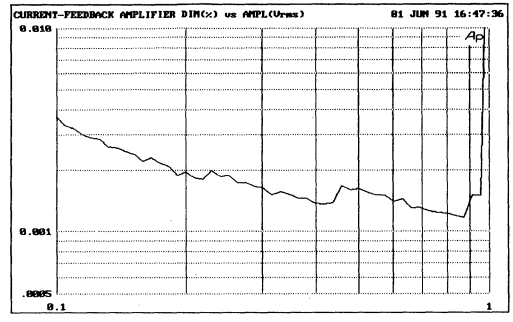


Figure 10. Low DIM-100 Transient Intermodulation Distortion (3.15 kHz/15 kHz 4.1, 50 W into 8 Ω) Results from the Clean Transient Response.

This is the lowest value of DIM-100 distortion that the author has ever seen reported for a solid-state power amplifier. In numerous listening tests, the "fast" sound of this amplifier and its tight LF performance have been commented upon. The large signal step response of the amplifier into an 8 Ω load at 100 kHz is shown in Figure 11, and the no load response with an 80 V p–p square-wave at the output is shown in Figure 12. Either photograph reveals that the amplifier is inherently stable and exhibits no trace of overshoot on fast edges.

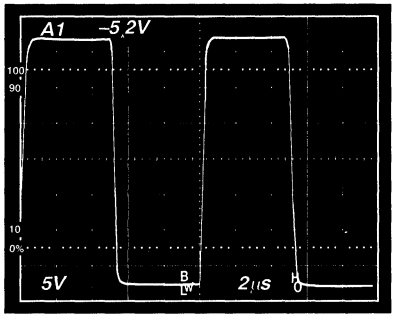


Figure 11. The Amplifier Exhibits Minimal Overshoot When Driving a High Frequency Square Wave into an 8 Ω Load.

Finally the frequency response, as shown in Figure 13, does indeed verify the somewhat overbearing calculations done earlier and proves that the closed-loop bandwidth extends all the way out to 1 MHz. Such a wide frequency response is definitely overkill for any audio power amplifier (200 kHz–300 kHz is probably more than adequate), but it does show what is achievable with a modern design.

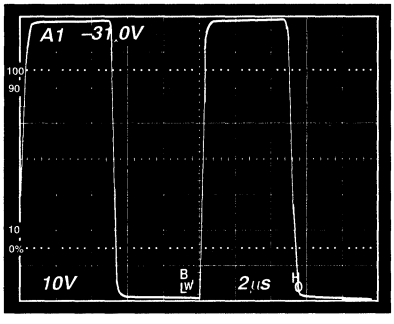


Figure 12. A Large Signal Square Wave at 100 kHz Shows that the IGBT Output Stage Is Inherently Stable Even Without a Load.

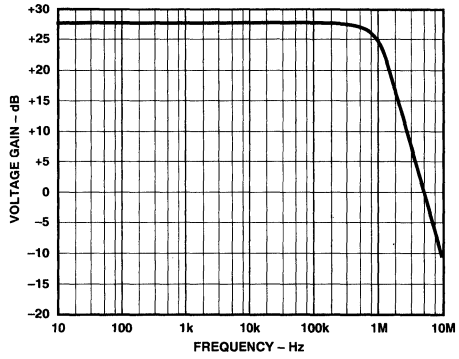


Figure 13. The Small-Signal Frequency Response Does Indeed Extend All the Way Out to 1 MHz, as Predicted by the Calculations.

CONCLUSION

Once in a while a new design comes along that offers a different way of doing an old job. The amplifier that has been presented here offers an evolutionary approach to the task of driving a loudspeaker. When proper attention is paid to all the details (and some of them are nontrivial indeed), current feedback amplifiers can offer superior sonic performance to all known topologies.

REFERENCES

[1]Mark Alexander, "A Current Feedback Audio Power Amplifier," 88th Convention of the Audio Eng. Soc., reprint #2902, March 1990.

[2]Edward M. Cherry, "A New Distortion Mechanism in Class B Amplifiers," Journal of the Audio Eng. Soc., Vol 29, No. 5, pp. 327-32 8, May 1981.

APPENDIX A: FREQUENCY RESPONSE OF CURRENT FEEDBACK AMPLIFIERS

To derive the input-to-output transfer function of a current feedback amplifier, the representative model shown in Figure 14 must be analyzed. Instead of a differential input stage, this topology utilizes a unity gain input buffer, driving a low impedance current summing node, which forces the inverting terminal to be at the same potential as the noninverting input. A nonzero input buffer output resistance, R_{INV}, is shown in series with the inverting terminal and must be included in the analysis of closed-loop gain versus frequency. Neglecting this resistance is a common oversight in simplified analyses, and leads to a transfer function that will not show any bandwidth variation with gain at all. Feedback is applied from the main amplifier output back to the inverting terminal through the current summing network that comprise of R_1 and R_2.

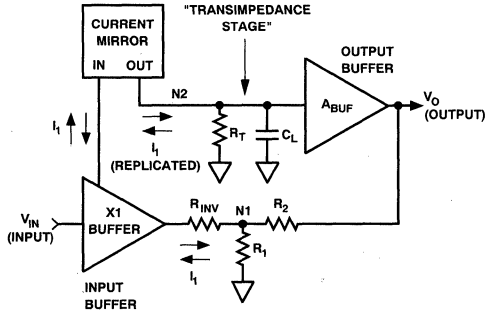


Figure 14.

The action of the input buffer is to force a finite current to flow through R_1 that must be balanced by an almost exactly equal but opposite current in R_2. Any difference between these two currents is an error current that flows into or out of the low impedance inverting terminal. This error current (as opposed to an error voltage in a conventional operational amplifier) is then mirrored and fed into a transimpedance stage, consisting of R_T and Cc, where current-to-voltage conversion takes place. The voltage generated here is buffered by another unity gain stage and is fed to the main amplifier output. Because the value of the small signal transresistance, R_T, is very high (normally several megohms) only minute error currents are needed to change the voltage at node 2 by several volts. Consequently, the amount of current that must flow into or out of the inverting terminal under steady state conditions is extremely small. The feedback network, even though it consists of fairly low value resistors, therefore presents a very light effective load on the output of the input buffer. To derive a transfer function for this amplifier, nodal equations must be written for nodes 1 and 2, and then combined in an appropriate way to obtain the final result:

$$\frac{V_O}{V_{IN}} = \frac{1+\frac{R_2}{R_1}}{1+\frac{R_2+\left(1+\frac{R_2}{R_1}\right)R_{INV}}{R_T A_{BUF}}+s\frac{\left(R_2+\left(1+\frac{R_2}{R_1}\right)R_{INV}\right)C_C}{A_{BUF}}} \quad (7)$$

This relationship is actually very similar to that of a voltage feedback amplifier, and it can be seen that the dc closed-loop gain is nearly equal to $1 + R_2/R_1$ (assuming that the product $R_T A_{BUF}$ is also reasonably large). The low frequency gain term is something with which most users of IC op amps should already be familiar. At a first glance the frequency dependent term might seem to be quite similar to that of a voltage feedback amplifier, but it is in fact very different. This can be seen more easily if the expression for the closed-loop pole frequency is written down:

$$f_{POLE} \cong \frac{A_{BUF}}{2\pi\left(R_2+\left(1+\frac{R_2}{R_1}\right)R_{INV}\right)C_C} \quad (8)$$

Interestingly, this result shows that the pole frequency now depends predominantly on the value of feedback resistor R_2 and the input buffer output resistance R_{INV} multiplied by the closed-loop gain. Normally the value of R_{INV} is made as low as possible to minimize the change in pole frequency with gain, and is typically less than one tenth that of the minimum recommended feedback resistor value. At high gains, as mentioned before, the closed-loop bandwidth starts to become inversely proportional to the gain because the term in the denominator of Equation (8) due to R_{INV} starts to become dominant. The gain bandwidth product is thus:

$$GBW = \frac{A_{BUF}}{2\pi R_{INV} C_C} \quad (9)$$

The gain of the output buffer, A_{BUF}, also plays its part in determining the closed-loop pole frequency. As the main amplifier output is loaded, this gain drops well below unity, and causes a reduction in closed-loop bandwidth as dictated by Equation (8). This actually tends to make the amplifier more stable since the high frequency nondominant poles contribute less additional phase shift at the lower closed-loop −3 dB point. In fact, many commercial current feedback amplifiers show significant gain peaking with light loads, and don't begin to behave acceptably until loaded fairly heavily. Another thing to remember is that the minimum recommended

value for feedback resistor R_2 must be strictly adhered because too low a value will result in an excessively high closed-loop pole frequency. This can result in severe gain peaking due to the higher order poles becoming more dominant, and is especially a problem at low gains when the multiplicative effect of R_{INV} on the closed-loop pole time constant is minimal.

During early development of the current feedback power amplifier it was noticed that instability appeared on the edges of square waves, using the ground referenced compensation scheme. Some experimentation revealed that connecting the compensation capacitors to the feedback summing node made the instability disappear. An analysis of the amplifier response using this new arrangement was undertaken, since something must have changed to make it more stable. Indeed, when the compensation capacitors are returned to the feedback summing node instead of ground, the transfer function of the circuit changes quite significantly. This modified compensation arrangement also allows one to get by with smaller capacitors than before, but without compromising closed-loop stability. To see this, the current feedback model must be analyzed again but this time the compensation capacitor C_C is returned to the summing node instead of ground:

$$\frac{V_O}{V_{IN}} = \frac{\left(1 + \frac{R_2}{R_1}\right)\left(1 + s\left(\frac{2R_1R_2C_C}{R_1 + R_2}\right)\right)}{1 + \frac{R_2 + \left(1 + \frac{R_2}{R_1}\right)R_{INV}}{R_TA_{BUF}} + s\left(\frac{2R_2C_C + \left(1 + \frac{R_2}{R_1} + \frac{R_2}{R_T}\right)R_{INV}C_C}{A_{BUF}} - R_{INV}C_C\right)} \quad (10)$$

The major difference between Equations (7) and (10) is the appearance of a zero in the numerator determined by the parallel combination of R_1 and R_2, and some additional terms in the denominator. The zero tends to partially cancel the second pole of the amplifier due to the IGBT output stage, resulting in greatly improved stability. Probably the most interesting thing to notice about Equation (10) however, is that the R_2C_C time constant is now multiplied by a factor of two instead of unity as before. Since it is this time constant that predominantly determines the closed-loop pole frequency, the original compensation capacitor value can thus be scaled down by a factor of one half.

APPENDIX B: AMPLIFIER COMPONENT LIST FOR A SINGLE CHANNEL

	Quantity	Designator
Integrated Circuits		
SSM-2131P BiFET Audio Op Amp	1	A_1
OP-97FP Precision DC Op Amp	1	A_2
TL431CP Programmable Shunt Regulator	1	D_7
Transistors		
2N3904 NPN, 40 V (4 Are Used as Zener diodes)	7	Q_5, Q_7, Q_{12}, Q_{14}–Q_{17}
2N3906 PNP, 40 V	2	Q_3, Q_{13}
2N5401 PNP, 150 V (or 2SC2682 from NEC)	3	Q_2, Q_4, Q_9
2N5551 NPN, 160 V	3	Q_1, Q_6, Q_8
MPS-U10 NPN, 300 V[1]	1	Q_{10}
MPS-U60 PNP, 300 V[2]	1	Q_{11}
GT20D101-Y N-CHAN IGBT 250 V, 20 A (Toshiba)	1	Q_{18}
GT20D201-Y P-CHAN IGBT 250 V, 20 A (Toshiba)	1	Q_{19}
Diodes		
1N914 100 V, 100 mA Small Signal Diode	9	D_1, D_2, D_5, D_6, D_8, D_{11}, D_{12}, D_{13}, D_{14}
1N5242B 12 V, 500 mW Zener Diode	2	D_9, D_{10}
1N4938 200 V, 100 mA Low t_{RR} Diode	2	D_3, D_4
MR822 200 V, 5 A Low t_{RR} Rectifier	2	D_{15}, D_{16}
Resistors		
(All Values Are in Ohms, and Are 1/4W 1% Metal Film Unless Otherwise Specified)		
0.05 Ω, 3 W, 5% Noninductive (Shallcross LO-3 Series)	2	R_{24}, R_{25}
10.0	2	R_{19}, R_{20}
16.5	1	R_7
33.2	1	R_6
100 (2 Are Used as Gate Resistors for the IGBTs)	7	R_3, R_{13}–R_{16}, R_{23}, R_{26}
249	1	R_{22}
499	1	R_{10}
750, 2-5 W, 1% Noninductive Metal Film	1	R_8
4.99 k	1	R_{12}
10.0 k	1	R_{21}
11.5 k	1	R_{11}
16.9 k	1	R_{17}
24.9 k	1	R_{18}
100 k	1	R_4
1.00 M	2	R_5, R_9
R_{BIAS} (49.9 k with ±65 V Power Rails)	2	R_1, R_2
50 kΩ Multiturn Trimpot (Helitrim 68WR503 or Equivalent)	1	VR_1
Capacitors		
47 pF 5% Silvered Mica (or Ceramic) 200 V	2	C_6, C_7
750 pF 5% Silvered Mica (or Ceramic) 200 V	1	C_3
0.1 μF 10% Ceramic or Mylar 63 V	4	C_4, C_5, C_8, C_{10}
1 μF 10% Ceramic 100 V	1	C_{11}
2 μF 10% Polyfilm 100 V (Electrocube 230B1B205K)	2	C_{12}, C_{13}
10 μF 10% Tantalum Electrolytic 25 V	3	C_1, C_2, C_9
2 to 10 μF 10% Polyfilm 100 V	2	C_{16}, C_{17}
220 or 330μF 10% Aluminum Electrolytic 100 V	2	C_{14}, C_{15}
Miscellaneous:		
Form-C Reed Relay (Coto 2211-12-300)	1	K_1
Thermalloy 6100B Heatsink for the Driver Transistors	2	
Extra Large Finned Heatsink for the IGBT Output Stage	1	
Insulating Pads for the IGBTs	2	
5-Pin Molex Header 0.156 Inch Pin Spacing	1	
7-Pin Molex Header 0.156 Inch Pin Spacing	1	
3-Pin Molex Header 0.100 Inch Pin Spacing	1	
Right Angle RCA Jack	1	
Amplifier evaluation PC Board[3]	1	

[1]First choice substitution is NEC 2SC2682; second choice Toshiba 2SC2238B. Note correct pinouts.
[2]First choice substitution is NEC 2SA1142; second choice Toshiba 2SA968B. Note correct pinouts.
[3]Available to qualified OEMs. Contact local ADI sales office for details.

ANALOG DEVICES

AN-212
APPLICATION NOTE

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Using the AD834 in DC to 500 MHz Applications: RMS-to-DC Conversion, Voltage-Controlled Amplifiers, and Video Switches

by Mark Elbert and Barrie Gilbert

INTRODUCTION

The AD834 is the fastest four quadrant multiplier available, having a useful bandwidth of 800 MHz, compared to the 60 MHz bandwidth of the AD539 two-quadrant multiplier, the 10 MHz bandwidth of the AD734 four-quadrant multiplier, or the 1 MHz bandwidth of the industry-standard AD534 four-quadrant multiplier. Its monolithic construction and high speed makes the AD834 a candidate for such HF applications as balanced modulation-demodulation, power measurement, gain control, and video switching, at frequencies that were previously beyond the scope of analog multipliers.

The AD834 does not sacrifice accuracy to achieve its speed. In common with all of the Analog Devices multipliers, laser trimming is used during manufacture to null input and output offsets and to establish precise scaling. In typical applications the total static error can be held to less than ±0.5%.

It is available in 8-pin plastic DIP, SOIC, and ceramic packages for the commercial, industrial, and military temperature ranges and operates from ±5 V supplies.

The main challenge in using the AD834 arises from its current-mode output stage. In order to maintain the highest possible bandwidth, the AD834's outputs are in the form of a pair of differential currents from open collectors. This is an inconvenience when a more conventional ground-referenced voltage output is needed. Thus, this application note discusses methods for the accurate conversion of these currents to a single-sided ground-referenced voltage.

These applications include a wideband mean-square detector, an rms-to-dc converter, two wideband voltage-controlled amplifiers, a high-speed video switch, and transformer-coupled output circuits. These applications provide the user with a complete and proven solution, in many cases including recommended sources for critical components.

OVERVIEW OF THE AD834

The AD834, shown in block schematic form in Figure 1, is the outcome of Analog Devices' continuing dedication to high-accuracy analog signal processing. In particular,

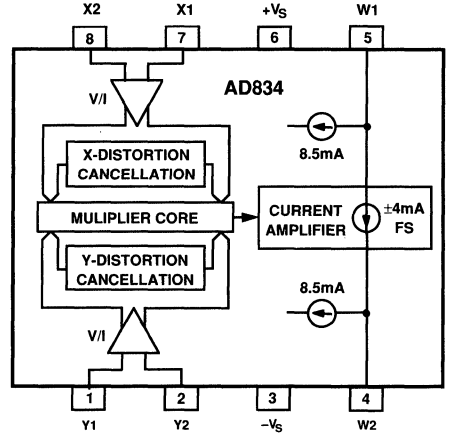


Figure 1. AD834 Block Diagram

it incorporates the experience gained in twenty years of manufacturing analog multipliers. The part is constructed on a 3 GHz epitaxial bipolar transistor process using laser-trimmed thin-film resistors. Attention to many subtle details has resulted in unusually low distortion and noise. Figure 2 shows a more detailed, but still simplified, circuit schematic.

The X- and Y-inputs are applied to high-speed voltage-to-current (V/I) converters, having a transresistance of 285 Ω and a small-signal input resistance of about 25 kΩ. The full-scale input voltage is ±1 V for both inputs. The input bias currents are typically 45 μA. Therefore, the dc resistance seen by both inputs of a differential pair must be equal to minimize offset voltages, just as for an op amp. Resistors at the inputs also minimize the risk of

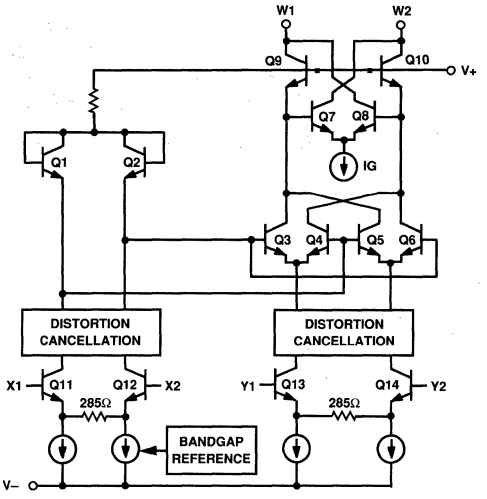


Figure 2. Simplified AD834 Schematic

high frequency oscillations. The V/I converters have a common-mode range of ±1.2 V, using the recommended supply voltages. Within that range, the differential inputs exhibit a common-mode rejection of 70 dB, conservatively specified for f < 100 kHz. Even-order distortion in the V/I converters is inherently low, while distortion cancellation circuitry is included to reduce odd order nonlinearity to typically ±0.05%.

The *multiplier core* is a well-known translinear circuit. The translinear principle [Ref. 1] exploits the precise logarithmic relationship between the base-emitter voltage (V_{BE}) and collector current (I_C) of a bipolar transistor. The input and output signals of translinear circuits are always in current form. Voltage swings at the internal nodes are very small, so that parasitic junction capacitances do not have to be charged and discharged, a common cause for bandwidth reduction and slew-rate limiting. Thus, translinear multiplier cells are inherently fast; they are also readily implemented in monolithic form. However, they can introduce distortion if not carefully designed.

This distortion is due primarily to emitter area mismatches and ohmic resistances in the core transistors (Ref. 2). Using the traditional convention in naming the channels, as shown in Figure 2, the X channel is susceptible to these effects, while the Y signal-path is essentially linear (the four output devices, Q3 through Q6, behaving in many respects like common-base stages, or cascodes). Therefore, the signal requiring the lowest possible distortion should always be handled by the Y channel. For example, in a balanced modulator application, the carrier (local oscillator voltage) should be applied to the X input and the baseband signal to the Y input.

The output from the core is in the form of a pair of differential currents. Now, the scaling of these currents is customarily controlled by adjustment of the bias currents in the V/I converter used on the X-input, which also determines the currents in the diode-connected transistors, Q1 and Q2.

In classical voltage-output multipliers, the range of adjustment needed to absorb the inevitable resistor mismatches is small, and this method of trimming the scaling factor is acceptable. In the AD834, however, the transfer function involves the two input voltages V_X and V_Y, the scaling voltage (generated in the band-gap reference circuit, and trimmed to an accurate value which is assumed here to be 1 V) and the output current, I_W:

$$I_W = \frac{V_X V_Y}{1V} \cdot \frac{I}{R} \qquad (1)$$

In this expression, the value of a resistance, R, determines the calibration of the output current. As fabricated, thin-film resistors have an initial uncertainty which can be as large as ±20%, and the customary methods of trimming the scale factor would result in other compromises (for example, erosion of the available signal range in the X-input V/I converter).

Therefore, the AD834 uses a "Gilbert gain-cell" [Reference 3] after the core to provide the needed adjustment of the effective value of R, which, in fact, is achieved by varying the current gain of this cell through trimming the current I_G. R, after the I_G trim, has an effective value of 250 Ω, resulting in a full-scale output current of ±4 mA when both inputs are at their full-scale value of ±1 V. The typical current-gain is 1.6, and because this type of amplifier is very fast and buffers the core outputs, the overall bandwidth of the multiplier is actually enhanced over that which would be obtained using the core outputs directly.

The bias currents from the core, and the gain-setting current I_G, result in a fairly large standing current—typically 8.5 mA—which flows into the outputs W1 and W2 (Pins 4 and 5). Only the *differential* output is precisely specified to be ±4 mA.

The output currents can be converted back to voltages in a variety of ways. In the simplest case, load resistors connected to the positive supply might be used, but these do not convert the (two) differential outputs to a single-sided voltage.

For the AD834 to operate properly, the output Pins (4 and 5) must be pulled above V+ to avoid saturation of Q7–Q10. To avoid using a separate supply to do this, several of the circuits included here use a voltage-dropping resistor in series with the positive supply Pin (6) of the AD834; this is a higher value than necessary for decoupling purposes.

This dropping resistor lowers the voltage at Pin 6 to provide an extra margin of bias for the output transistors. For example, in the mean-square circuit in Figure 3, 11 mA of quiescent current across the 169 Ω dropping resistor creates 1.86 V of headroom. The decoupling re-

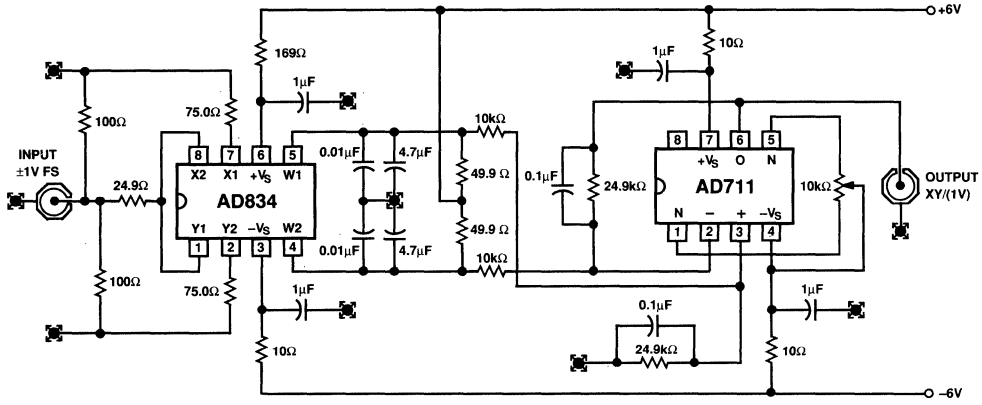


Figure 3. A DC to 500 MHz Mean Square Circuit

sistor in series with the negative supply to Pin 3 is only 10 Ω, since it is included just to decouple the supplies.

Much of this application note, however, is concerned with *more effective ways* of loading the outputs. For example, because they are fully calibrated, the outputs of two or more AD834's can be accurately summed by simply connecting them in parallel, as is done in the rms application discussed later in this application note.

MEAN-SQUARED DETECTOR

We will begin with a discussion of a mean square detector (Figure 3), whose output is a dc voltage proportional to the input power. This circuit is useful in that it requires only a calibrated signal generator and a dc voltmeter to demonstrate the very high speed of the AD834.

The input signal is applied to the X- and Y-inputs connected in parallel. The *instantaneous* output current is thus proportional to the square of the input voltage. The square of a sinusoidal input voltage of amplitude A is an offset cosine at twice the frequency:

$$A\,(sin\omega t)^2 = A^2\,(1 - cos\ 2\ \omega t)/2 \qquad (2)$$

If the input to the AD834 has this sinusoidal form, then the instantaneous output current (using Equation 1) is simply

$$I_W = 2A^2\,(1 - cos2\omega t)\ mA \qquad (3)$$

the average value of which is just 2 mA for the maximum 1 V amplitude sinusoid.

The full-scale differential voltage which would be measured across Pins 4 and 5 of the AD834 is, therefore, 2 mA × (50 Ω + 50 Ω), or 200 mV. This average is extracted by the low-pass filter formed by the 4.7 μF 22 μF (AVX part #SR505E475MMAA and #SR505a223JAA) capacitors in conjunction with the 50 Ω collector load resistors, having a −3 dB frequency of about 650 Hz.

Two capacitors are used in parallel since the 4.7 μF capacitor uses the compact but lossy Z5U dielectric material while the 22 μF capacitor uses a high Q NPO dielectric which ensures good filtering at the highest frequencies. Note that the 4.7 μF capacitors have a −20% to +80% tolerance, so their −3 dB frequency is not accurate, nor does it usually need to be. Further filtering is performed by the capacitors in shunt with the feedback resistors of the AD711 operational amplifier, configured to have a −3 dB frequency of 65 Hz.

Due to finite averaging of the circuit, there will be some ripple for low frequency inputs. For the circuit shown, a 1 kHz input will produce the mean-square plus a −42 dB 2 kHz ripple; for 100 kHz input, the ripple will be only −80 dB. Since the output is band limited, we can use a generic low speed op amp with ample common-mode range, obviating the need for level shifting. The differential gain of the amplifier can be chosen to provide a convenient scale factor.

The full-scale gain of the circuit in Figure 3 is calculated as follows. The average output current is ±2 mA for 1 V (peak) sinusoidal input, which creates ±100 mV across each 50 Ω output load resistor or 200 mV differential. The amplifier is configured for a differential gain of 2.5 (feedback resistance over source resistance), yielding a circuit gain of 0.5 V dc output for 1 V rms input.

The bandwidth of this circuit is limited by package capacitance and inductance. In the 8-pin cerdip, the multiplier's response normally starts to rise at 500 MHz due to package resonance and peaks at 800 MHz before rolling off. A 24.9 Ω resistor at the input dampens the resonance yielding an essentially flat response out to 800 MHz. (The package inductance will be different for a surface mount AD834.) Figure 4 shows the results over frequency for three different power levels using the test configuration shown in Figure 5.

Neglecting the 24.9 Ω in series with the high impedance inputs, the input resistance to the mean square circuit in Figure 3 is 50 Ω. Since the full-scale input range is ±1 V, the maximum measurable power with a 50 Ω input load is 10 mW (20 dBm), assuming a sinusoidal input.

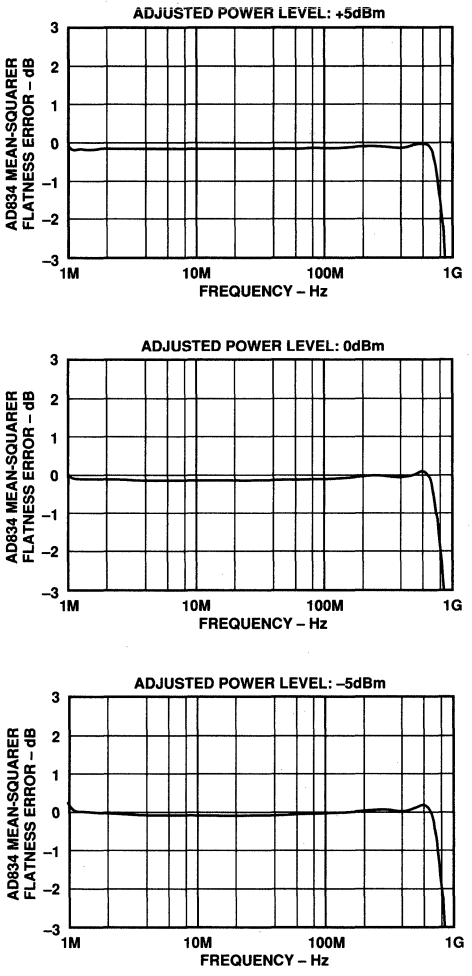


Figure 4. Frequency Response of Mean Square Circuit for Input Power Levels of −5 dBm, 0 dBm, and +5 dBm

For greater input ranges, a voltage divider with a series resistance of 50 Ω at the input will scale down the voltage seen by the AD834 while maintaining a proper termination resistance. For example, if the input signal is applied to a 45 Ω resistor in series with a 5 Ω resistor to ground, then taking the AD834's input from the middle node of the voltage divider provides 20 dB attenuation of the input signal, while maintaining a termination resistance of 50 Ω (45 Ω + 5 Ω).

Detection of low power signals is limited by dc offsets and the common-mode rejection of the op amp. For example, a −20 dBm signal, corresponding to 22.4 mV rms across 50 Ω, would result in a 4.5% error in the presence of only 1 mV of offset in the op amp. A 10% error can occur if the AD834's X channel offset is just 2 mV.

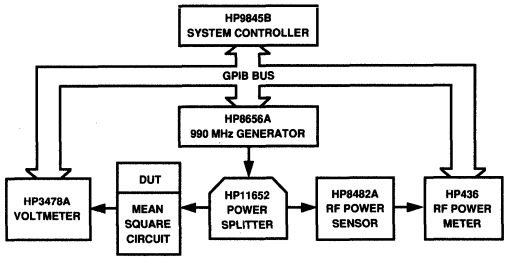


Figure 5. Test Configuration

RMS-TO-DC CONVERTER

The root mean square (rms) circuit (Figure 6) is little more than the mean square detector circuit described above followed by a square root circuit. The frequency response is determined by the front end squarer and output filter. From the mean-square discussion, the squarer functions well past 500 MHz, while the lower −3 dB frequency response is 340 Hz (100 Ω and 4.7 μF). Note that a resistor divider network at the input determines the full-scale input voltage to be ±2 V peak.

The square root function is performed by a squaring AD834 in the feedback loop of an AD711 operational amplifier. The 2N3904 transistor functions as a buffer. The resistive divider network (two 100 Ω) between the buffered output and the X and Y channel inputs of the AD834 used in the square root section determines the output scaling to be ±2 V full scale.

The outputs of the two AD834s are current-differenced. Accurate output differencing and summing is possible owing to the precision of the laser trimmed AD834 output signal current scaling. The AD711 forces the difference between the two AD834 signal current to zero. Any error in the nulling generates a voltage across the two 100 Ω pull-up resistors.

After additional filtering and level shifting by the 15 kΩ, 85 kΩ, and 0.1 μF network, the residual error is amplified by the full AD711 open loop gain. The amplified error signal forces the AD834 in the feedback loop to match its output to the mean-squaring AD834's output. The error is nulled when the rms circuit's output is equal to the square-root of the circuit's input mean-squared, hence the rms function.

The accuracy of the circuit at small signal levels is limited by inevitable offset voltages. While a nominal 0 V input with a 1 mV error to a mean-square function generates a 1 μV output error, the same input error generates a 31.6 mV output error through a square root circuit.

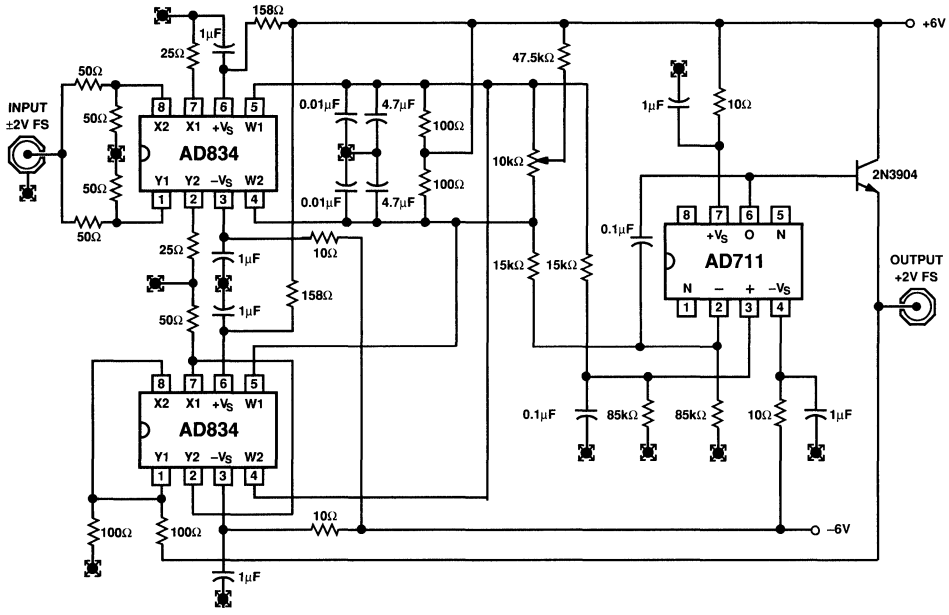


Figure 6. DC to 500 MHz RMS-to-DC Converter

DC COUPLED VCA APPLICATIONS

Where the dc response of the AD834 cannot be discarded, some form of level shifting, either passive or active must be employed, since high speed op amps often have inadequate common-mode range. The following applications show the use of active and passive level shifting circuits in the implementation of wideband voltage-controlled amplifiers.

A DC TO 60 MHz VOLTAGE-CONTROLLED AMPLIFIER USING PASSIVE LEVEL SHIFTING

Figure 7 shows the schematic of a circuit employing a passive network as a level shifter. The op amp chosen here is the AD5539.

The AD5539 is built on the same process as the AD834 and provides a 2 GHz gain-bandwidth product at high closed-loop gain. Unlike most op amps, the AD5539

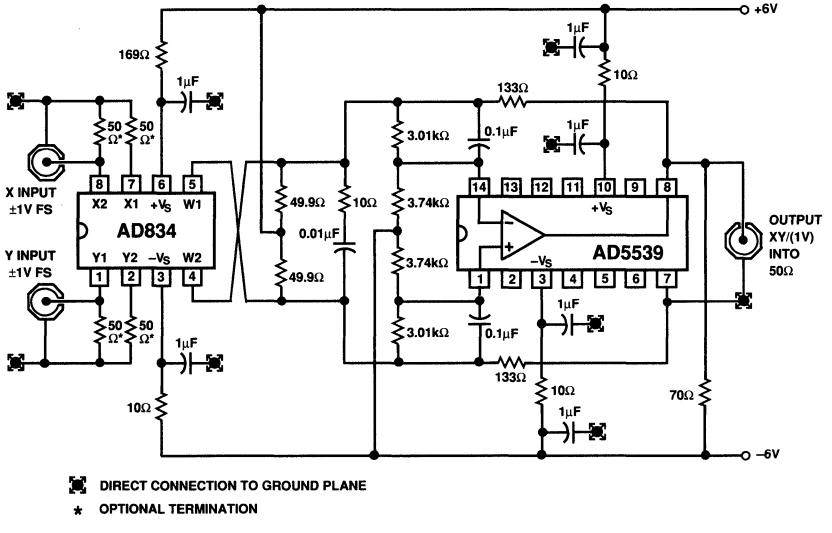


Figure 7. DC to 60 MHz Voltage-Controlled Amplifier Using Passive Level Shifting

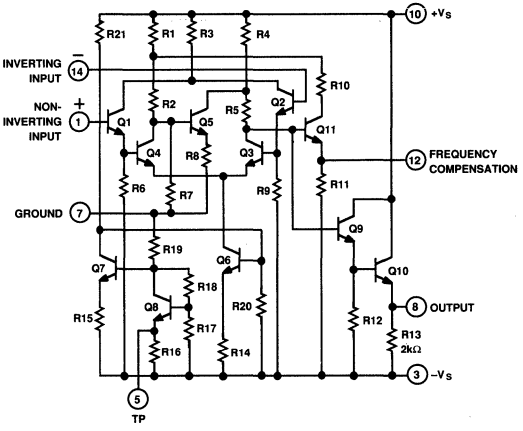


Figure 8. AD5539 Operational Amplifier Simplified Schematic

features a ground pin and an all-NPN output stage which operates in "Class A" to achieve the part's high speed (see Figure 8). Closer examination shows that there is a limited amount of "headroom" between the output node and the inputs, and between these voltages and ground. This, its high speed, and other unusual attributes of the AD5539 require special care in its use.

First, consider the consequences of its Class A output stage. In most op amps, the output can both "pull up" and "pull down" on the load, but the NPN emitter-follower output stage can only pull up. The AD5539 has an internal pull-down resistor (R11) of 2 kΩ, which can only supply two or three milliamps. A general-purpose high-speed multiplier must be able to swing to at least ±1 V while driving the minimum likely load resistance of 50 Ω. At this output level, the load current will be ±20 mA, which must therefore be supplied by an external pull-down resistor. In fact, the pull-down current must be considerably more than this, and requires careful consideration.

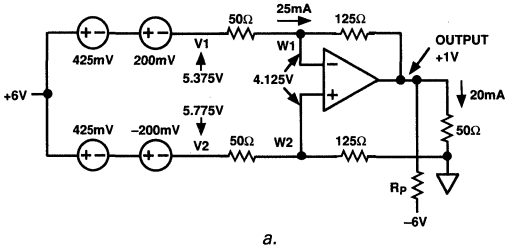
Figure 9 shows how the calculation is done. The 425 mV voltage sources are just "I_BR_C," that is, the standing current of 8.5 mA at the AD834 multiplied by the load resistor R_C, which we have here set to 50 Ω. The 200 mV sources in Figure 9 (a) are the "I_WR_C" generators when the full-scale output current is +4 mA. From here, we calculate V1 − 5.375 V and V2 − 5.775 V.

Next, we calculate the voltage at W2. Because the input current to an ideal op amp is zero, there is no loading at W2 and the voltage is simply V2 multiplied by the attenuation ratio 125/(125 + 50), or 4.125 V. Because the input voltage to an ideal op amp is zero, W1 is at the same voltage, so we can now calculate the current in the upper 50 Ω resistor as (5.375–4.125)/50 mA or 25 mA. Again, there is essentially no current at the input of the op amp, so the 25 mA all flows in the feedback resistor of 125 Ω, resulting in a voltage drop across it of 3.125 V. Finally, we calculate the output as the voltage at W1 (4.125 V) minus this drop; that is, the output is at +1 V.

Notice a somewhat surprising result at this point: although a current of 20 mA flows into the load, a larger current, 25 mA, flows in the feedback resistor! This unusual state of affairs is due to the very low value of the feedback resistor needed to reduce the scaling factor to the desired value, and the relatively large voltage needed at the output of the AD834 to ensure proper biasing of its outputs W1 and W2. Thus, even though the load needs to be sourced 20 mA, we still need to provide at least 5 mA in the pull-down resistor R_P to bias the output emitter-follower in the AD5539. The situation gets more severe when the output current of the AD834 is reversed, because we now need to sink 20 mA in the 50 Ω load and the voltage across the feedback resistor is now even higher.

This situation is shown in Figure 9(b). The calculation is exactly as before, and we discover that the current in the feedback resistor is now 39.7 mA. So R_P needs to provide the load current of 20 mA and an additional 40 mA or so in the feedback path, while the voltage across it is 5 V. This would require R_P = 83 Ω. In practice, it should be slightly lower to prevent slew rate limiting the fall time. Also, the feedback resistor will be raised from 125 Ω to 133 Ω to make up for the finite gain of the AD5539 under these heavily-loaded conditions. If we take the parallel sum of the 50 Ω load, the 70 Ω pull-down and about 150 Ω effective feedback resistance, the actual load on the amplifier is only 24 Ω!

The AD5539 is stable for uncompensated gains of greater than 5, and the AD5539 in this circuit is operating at a gain of just over 3. The 0.01 μF and 10 Ω network compensates by throwing away enough open loop gain to be stable when driving a 50 Ω load. For higher impedance loads, the 10 Ω compensation resistor may need to be reduced.



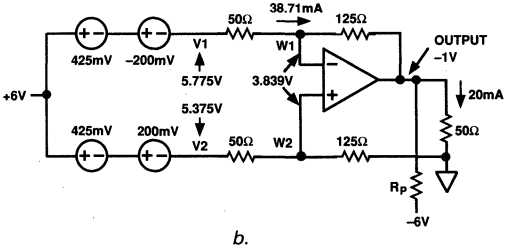


Figure 9. Equivalent Circuits for Calculating the Value of the Pull-Down Resistor

A level-shifting network is included between the nodes W1 and W2, whose average voltage is about +4 V, to the input of the AD5539 which must be close to ground. With the values shown, the op amp inputs are set slightly below ground (about −460 mV). This network halves the low frequency open-loop gain, which has some effect on the dc accuracy in the presence of offset voltages at the input to the AD5539. If output offset is important, a 500 Ω potentiometer should be inserted in series with the 3.74 kΩ resistors and its slider taken to −6 V. It is then adjusted for zero output with both X and Y inputs set to zero.

Note also that the "inner" Pins X1 and Y2 on the AD834 are grounded to minimize HF feedthrough; the resulting phase-reversal at the X input is corrected by swapping W1 and W2.

Figure 10 shows the pulse response with the input pulse applied to the X input and the Y input set to +1 V, indicating a rise time of 6 ns.

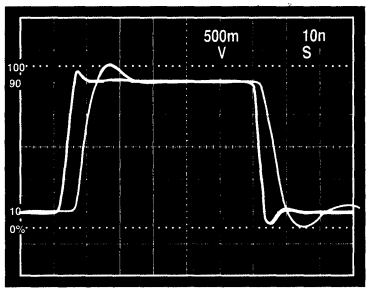


Figure 10. Pulse Response of the DC to 60 MHz Voltage-Controlled Amplifier

Figure 11 shows a set of frequency responses taken on an HP8753B network analyzer for Y inputs of +1 V, 316 mV, +100 mV, and 0 V. In the case of 0 V, the Y input is adjusted to null the input offsets. Note that the high frequency feedthrough is less than −65 dB of full scale (f < 3 MHz).

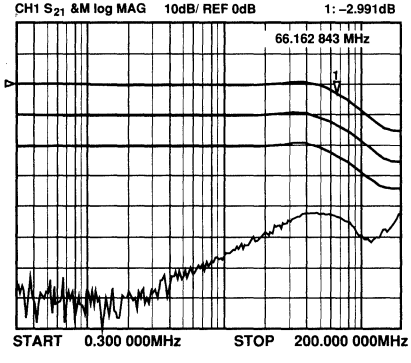


Figure 11. Frequency Response of the DC to 60 MHz Voltage-Controlled Amplifier

A DC TO 480 MHz VOLTAGE-CONTROLLED AMPLIFIER USING ACTIVE LEVEL SHIFTING

Figure 12 (a) shows an active level shifter, using a PNP transistor as a common base stage or cascode. Here, the AD834 is modeled by three ideal current sources, two for the 8.5 mA bias currents and one for the ±4 mA differential signal current. The transistors' bases are tied to +5 V, setting the emitter potential stays at 5.7 V resulting in a voltage of 3.3 V across the resistors R1 and R2 in the absence of signal. Figure 12 (b) shows an equivalent circuit.

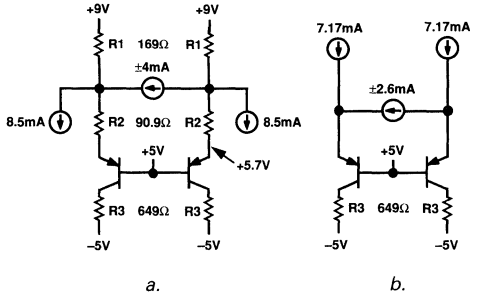


Figure 12. An AD834 Output Stage Using Active Level Shifting

The equivalent dc bias current of 7.17 mA is found by solving for the current flowing into the emitter when the signal current generator is zero. In the ac domain, the signal current generator sees R1 and R2 both tied to low impedance nodes. By inspection, the original signal current has been scaled by:

$$\pm 2.6mA = \pm 4\ mA \times \frac{R1}{R1 + R2} \quad (4)$$

Since AD834's outputs have very high output impedances, the equivalent series resistance can be ignored. The entire 7.17 mA flowing into the cascode's emitter flows out the cascode's collector, assuming a good α, and across R3. The voltage across R3 is:

$$4.65\ V = 7.17\ mA \times 649\ \Omega \quad (5)$$

The operational amplifier's inputs are 350 mV below ground and are within the common-mode range of a wideband amplifier.

The bandwidth of a transistor configured as a cascode is the unity gain frequency (f_T) of the transistor, provided that the user does not create any spurious poles. Choosing an R1 and R2 such that their parallel sum is too large for the transistor's parasitic emitter-base capacitance or an R3 too large for the transistor's parasitic collector-base capacitance will create unwanted poles that lower the frequency response of the circuit.

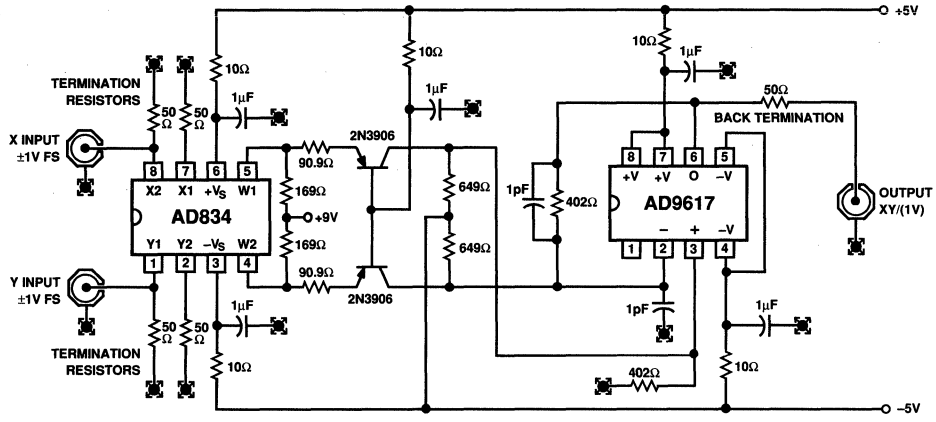


Figure 13. A DC to 480 MHz Voltage-Controlled Amplifier Using Active Level Shifting

Another potential pitfall when using the active PNP level shifter is oscillations at the cascode's emitter. The input impedance of a bipolar junction transistor's emitter is inductive at frequencies approaching its gain-bandwidth product (f_T), while the AD834's output is capacitive. Due to the high bandwidth of the system, these impedances can lead to oscillation.

To prevent such oscillations, the emitter in Figure 12 has been isolated from the AD834's output by R2. This prevents oscillations while providing signal attenuation (gain control) as related in Equation 4. The 2N3906s provide wideband level shifting without resonance or oscillation. Care must be taken when using alternative transistors.

The signal current at the cascodes' collectors is now fed to a wideband amplifier in a differential current to voltage converter configuration as shown in Figure 13. This configuration is similar to an op amp driven current-to-voltage converter which typically follows a current output multiplying digital-to-analog converter.

The AD9617 makes an excellent choice to drive the current to voltage converter. The AD9617 is a second-generation transimpedance amplifier (also known as a current feedback or TZ amplifier) with a fully complementary output stage (unlike the AD5539), and optimized for use with a 400 Ω feedback resistor.

The AD9617 inputs are tied directly to the collectors of the cascodes. The op amp creates a virtual short between the input nodes, forcing all the signal current to flow in the feedback paths. The differential transresistance of the convertor is 400 Ω. The desired scaling can be attained by means of the R1 and R2 attenuation network described above. The full-scale gain of the circuit (X = Y = 1 V) at the AD9617's output is calculated as:

$$2 \times 2.6\ mA \times 400\ \Omega = 2.08\ V \qquad (6)$$

or 1.04 V after the reverse termination resistor. The actual circuit shows a full-scale gain closer to unity.

Figure 14 shows the full-scale step response (−1 V to +1 V) applied to the X input and the Y input set to +1 V demonstrating the circuit's capabilities with a rise time of under 2 ns while exhibiting some overshoot, but no ringing. Note that the output slews at over 500 V/μs.

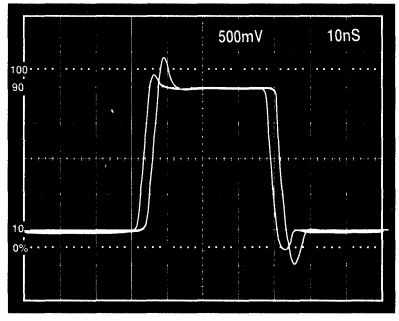


Figure 14. Step Response of the Wideband VCA

Figure 15 shows a set of frequency responses taken on the HP8753B network analyzer for Y inputs of +1 V, 316 mV, +100 mV, and 0 V. The Y input is actually adjusted to null the input offsets. Note that the circuit has a small-signal bandwidth of 500 MHz (at an input power level of 0 dBm). This bandwidth is possible with the two 1 pF capacitors at the inverting node. The high frequency feedthrough is less than −80 dB of full-scale (f < 2 MHz).

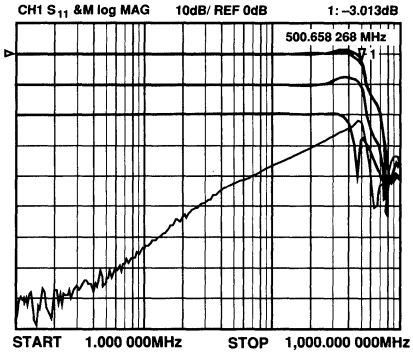


Figure 15. Frequency Response of the Wideband VCA

THE AD834 AS A VIDEO SWITCH

With 0 V or +1 V applied to the X channel as gate control and the video signal to the Y channel, the AD834 becomes a high-speed video switch. Figure 16 illustrates this idea with a high speed current switching circuit centered around an ECL switch. The current flows through either Q1 or Q2, depending on the input voltage. Current switching ensures fast and clean switching to determined levels (+1 V and ground), and allows the user to over- or under-drive the gate input.

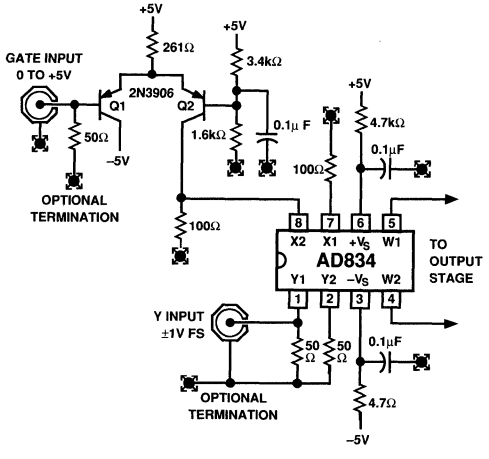


Figure 16. The AD834 as a High-Speed Video Switch

The AD834 switches on as the gate input rises from +1 V through +2 V at the gate circuit input. Below 1 V, Q1 absorbs almost all of the current from the 216 Ω resistor; the 2N3906 transistor is turned off. In this state, the 100 Ω resistor from the X2 input to ground accurately shuts the Y channel off, with Y channel feedthrough to the output measured at −50 dB. With the base of Q2 held at 1.6 V, the transistor's emitter potential is 2.35 V. A steady 10.2 mA (minus base current) from the 261 Ω resistor generates +1 V across the 100 Ω resistor at the X2 input independent of the exact high level of the gate input.

Figure 17 shows a scope photograph of a 1.5 ns rise-time pulse gating a 200 MHz signal. The resulting envelope rise time is 2.7 ns; it has a fall time of 3.0 ns. Although the switched signal may be much slower, the output stage from the AD834 should have a bandwidth greater than 100 MHz in order to maintain an envelope rise time of 3.5 ns.

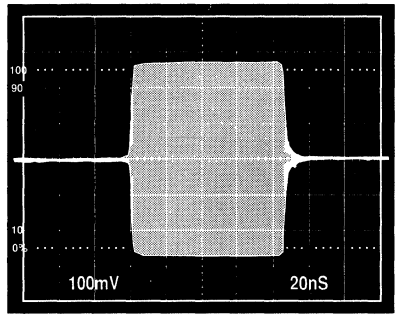


Figure 17. Rise Time of the Video Switch

AC OUTPUT-COUPLING METHODS

In many applications, the dc component at the output can be discarded. In such cases, a wideband buffer can easily ac couple to the AD834 output. The circuits below show the use of simple transformers and baluns for passive, ac coupled output circuits.

TRANSFORMER-COUPLED OUTPUT

Figure 18 shows the use of a center-tapped output transformer, which provides the necessary dc load condition at the outputs W1 and W2, and is designed to match into the desired load impedance by appropriate choice of turns ratio. The specific choice of the transformer design will depend entirely on the application. Transformers may also be used at the inputs. Center-tapped transformers can reduce high frequency distortion and lower HF feedthrough by driving the inputs with balanced signals. Suitable center-tapped transformers include the Coilcraft WB2010PC, which the manufacturer specifies for 0.04 MHz to 250 MHz operation.

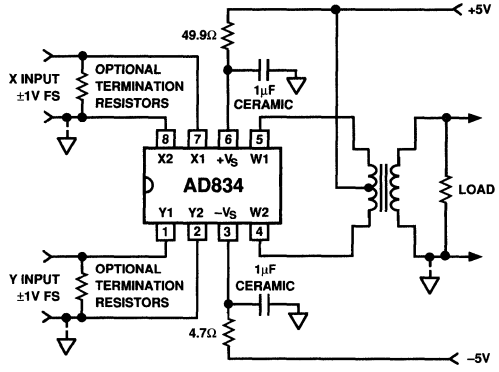


Figure 18. The AD834 with Transformer-Coupled Output

BALUN-COUPLED OUTPUT

Figure 19 shows a circuit which uses blocking capacitors to eliminate the dc offset, and a balun, a particularly effective type of transformer, to convert the differential (or balanced) signal to a single-sided (or unbalanced) output. A balun consists of a short length of transmission line wound on to a toroidal ferrite core, which converts the 'bal'anced output to an 'un'-balanced one (hence the use of the term).

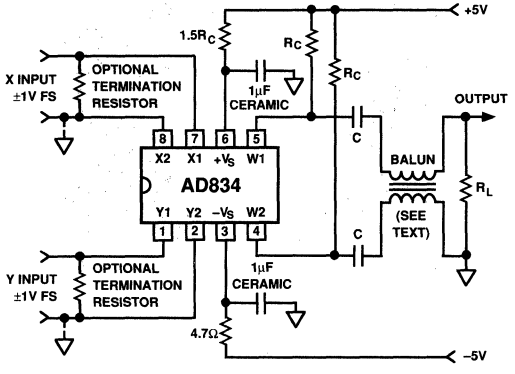


Figure 19. The AD834 with Balun-Coupled Output

Although the symbol used is identical to that for a transformer, the mode of operation is quite different. In the first place, the load should now be equal to the characteristic impedance of the line, although this will usually not be critical for short line lengths. The collector load resistors R_C may also be chosen to reverse-terminate the line, but again this will only be necessary when an electrically long line is used. In most cases, R_C will be made as large as the dc conditions allow, to minimize power loss to the load. The line may be a miniature coaxial cable or a twisted pair.

It is important to note that the upper bandwidth limit of the balun is determined only by the quality of the transmission line; hence, it will usually exceed that of the multiplier. This is unlike a conventional transformer, where the signal is conveyed as a flux in a magnetic core, and is limited by core losses and leakage inductance. The lower limit on bandwidth is determined by the series inductance of the line, taken as a whole, and the load resistance (if the blocking capacitors C are sufficiently large). In practice, a balun can provide excellent differential-to-single-sided conversion over much wider bandwidths than a transformer.

IMPLEMENTATION

Building these circuits requires good high frequency techniques. The circuit schematics suggest suitable layout. **Ground plane is essential for all of the circuits described in this applications brief.** It should cover as much of the component side of the PCB as possible, but not directly underneath the IC or encircling any individual pins. Sockets add to the pin capacitance and inductance, and should be avoided. If sockets are necessary, use individual pin sockets such as AMP p/n 6-330808-3. They contribute far less stray reactance than the molded socket assemblies. Each power trace should be decoupled at the IC with a 0.1 μF low inductance ceramic capacitor, in addition to the main decoupling capacitor. All lead lengths should be kept as short as possible. For lead lengths longer than an inch, stripline techniques should be used.

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[Ref. 2] Gilbert, Barrie, "A Precise Four-Quadrant Multiplier with Subnanosecond Response," *Journal of Solid-State Circuits*, Vol. SC-3, No. 4, pp. 365-373.

[Ref. 3] Gilbert, Barrie, "A New Wideband Amplifier Technique," *Journal of Solid-State Circuits*, Vol. SC-3, No. 4, pp. 353-365.

ANALOG DEVICES

AN-213
APPLICATION NOTE

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Low-Cost, Two-Chip Voltage-Controlled Amplifier and Video Switch

by Charles Kitchin, Andrew Wheeler, and Ken Weigel

INTRODUCTION

Historically, it has been very difficult to build wide bandwidth, high quality, voltage-controlled amplifiers. Discrete designs have required a great deal of design effort while monolithic or hybrid integrated circuit approaches to VCAs have been expensive, or they have suffered from poor performance.

With the introduction of the AD539JN, a 60MHz analog multiplier in a plastic package, wideband gain-control is now practical at low cost. Used in conjunction with the 5539N wideband op-amp available from either Analog Devices or Signetics Corp. (also in a plastic package), the two devices can be connected together to create a high-speed voltage-controlled amplifier (VCA) or Video Switch with outstanding performance. In addition to providing a 50MHz bandwidth, this combination also satisfies even the most stringent differential phase and differential gain requirements. The AD539/5539 VCA is able to drive a 75Ω terminated coaxial cable directly.

A REVIEW OF SOME BASICS

Before describing the complete circuit, some basic principles of analog multiplication, as well as the main features of the AD539, will be reviewed. Monolithic multipliers have been commercially available since 1970, following the discovery of an important circuit design technique based on the logarithmic relationship between the base-emitter voltage of a bipolar transistor and its collector current. All IC multipliers now use this concept, known as the translinear principle.

One-quadrant multipliers accept input voltages at V_X and V_Y of only one polarity; accordingly, their operation is confined to quadrant 1 of a 4-quadrant X, Y coordinate system. This type of multiplier is of most use in high-accuracy computational roles.

Two-quadrant multipliers can accept voltages of either polarity at one of their input ports, but they can accept only a single polarity voltage at the other input. In gain-control applications, the bipolar input is considered the "signal" input and the single polarity input is referred to as the "control" input; therefore, when V_X is restricted to positive values, multiplier operation is confined to Quadrants 1 and 4.

Four-quadrant multipliers allow operation in all four quadrants with any combination of input polarity. Since this variety always preserves the correct sign at the output, it may at first seem that the four-quadrant type would *always* be the most useful variety of multiplier. However, this is *not* the case.

Until recently, the main emphasis in improving multiplier performance was directed toward higher precision, and four-quadrant operation was standard. However, the introduction of the AD539 two-quadrant multiplier deviates from this trend, by providing a 50MHz low distortion device optimized for gain control applications.

SOME ADVANTAGES OF TWO-QUADRANT MULTIPLIERS OVER OTHER TYPES

Four-quadrant analog multipliers have often been used in fast computational applications, in correcting the distortion of wide-angle CRT deflection systems, and in performing modulation and demodulation operations. However, in gain-control applications a two-quadrant multiplier is the better choice because this device is optimized for AC signals. This type of multiplier is often used for precision AGC, for implementing voltage-controlled amplifiers, and for creating various types of programmable filters.

Two-quadrant multipliers such as the AD539 have important advantages in gain-control applications, where there is no need (and it is undesirable) to respond to a bipolar control input voltage. Therefore, one functional advantage of the two quadrant multiplier is that the control channel can be fully blocked for all values of V_X below zero. As a practical matter, the offset voltage of the control channel can be made to be about one-tenth that of a general-purpose four-quadrant multiplier; this also provides improved low level gain accuracy.

Other advantages relate to improvements made possible in the design of the IC when the four-quadrant requirement is removed. In the AD539, these result in higher

bandwidth (60MHz versus 1MHz for a general-purpose device) with much smaller signal feedthrough at low gains, better phase response, lower signal-path distortion (the AD539 will generate less than 0.05% THD at full output in most applications), higher control-channel linearity, and lower noise (particularly at low gains).

TWO-SIGNAL CHANNELS WITH COMMON CONTROL

A unique feature of the AD539 is its own separate signal input channels, V_{Y1} and V_{Y2}, each with a nominal full-scale voltage range of $\pm 2V$ and each simultaneously controlled by a common input, V_X. V_X has a range of zero to $+3V$ FS. All inputs are referred to a common (input) ground connection.

The two-signal channels may be used in many different ways. First, of course, they can be used to control the magnitude of a pair of separate input signals. The excellent gain-tracking and high separation between channels of the AD539 proves to be valuable in this application; in fact, the bandwidth, crosstalk and other limitations occurring at high frequencies are caused more by the PC board layout than by the IC itself.

In applications where only a single channel is involved, the signal inputs and outputs may be connected in parallel. When driving grounded resistive loads, this configuration has the advantage of increasing the load power by a factor of four. Alternatively, the two-signal channels may be driven from complementary (phase and antiphase) signals, to achieve distortion figures as low as 0.01%; this mode is generally of more utility in low-speed applications (those with less than 1MHz bandwidth).

The two-signal channels may also be connected in series, thus providing a $V_X^2 V_Y$ function. This results in a circuit which has higher gain with twice the gain-control range (up to 100dB is practical) or instead, to provide a circuit with a more constant bandwidth over a reduced control voltage range. With the constant bandwidth circuit, the gain now varies as the square of the control voltage, which in some applications is advantageous.

A 50MHz VOLTAGE-CONTROLLED AMPLIFIER

Figure 1 is a circuit for a 50MHz voltage-controlled amplifier (VCA) suitable for use in high-quality-video-speed applications. The outputs from the two-signal channels of the AD539 (see "Inside the AD539" for a more complete circuit analysis) are applied to the op-amp in a subtracting configuration. This connection has two main advantages: first, it results in better rejection of the control voltage, particularly when overdriven ($V_X<0$ or $V_X>3.3V$). Secondly, it provides a choice of either noninverting or inverting responses, using either inputs V_{Y1} or V_{Y2}, respectively. In this circuit, the output of the op amp will equal:

$$V_{OUT} = \frac{V_X (V_{Y1} - V_{Y2})}{2V} \text{ for } V_X > 0$$

Hence, the gain is unity at $V_X = +2V$. Since V_X can overrange to $+3.3V$, the maximum gain in this configuration is about 4.3dB. (Note: If pin 9 of the AD539 is grounded, rather than connected to the output of the 5539N, the maximum gain becomes 10dB.)

The bandwidth of this circuit is over 50MHz at full gain, and is not substantially affected at lower gains. Of course, when V_X is zero (or slightly negative, to override the residual input offset) there is still a small amount of capacitive feedthrough at high frequencies; therefore, *extreme* care is needed in laying out the PC board to minimize this effect. Also, for small values of V_X, the combination of this feedthrough with the multiplier output can cause a dip in the response where they are out of phase. Figure 2 shows the AC response from the non-inverting input, with the response from the inverting input, V_{Y2}, essentially identical. Test conditions: $V_{Y1} = 0.5V$ rms for values of V_X from $+10mV$ to $+3.16V$; this is with a 75Ω load on the output. The feedthrough at $V_X = -10mV$ is also shown.

The transient response of the signal channel at $V_X = +2V$, $V_Y = V_{OUT} = +$ or $-1V$ is shown in Figure 3; with the VCA driving a 75Ω load. The rise and fall times are both approximately 7ns.

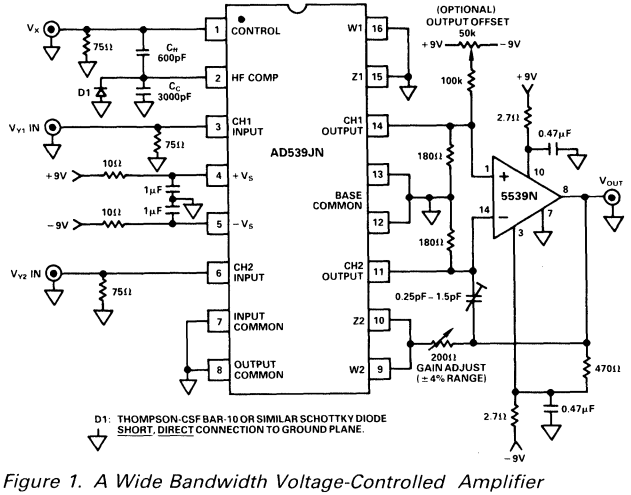

Figure 1. A Wide Bandwidth Voltage-Controlled Amplifier

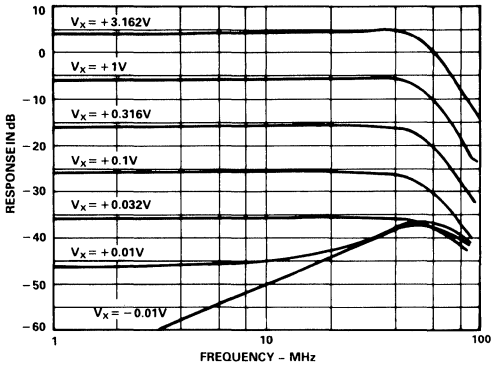

Figure 2. AC Response of the VCA at Different Gains $V_Y = 0.5V$ RMS

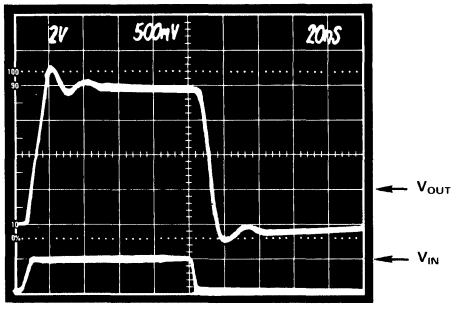

Figure 3. Transient Response of the Voltage-Controlled Amplifier $V_X = +2$ Volts, $V_Y = \pm 1$ Volt

In video applications, it is important that the gain and phase of the signal channels remain constant over the full-signal window. These aspects of the response are known as the differential-gain and differential-phase characteristics respectively, and are measured by superimposing a small AC signal at the subcarrier frequency (about 3.58MHz for NTSC systems) on top of a bias signal that modulates the channel over its nominal range, usually 0 to +1V. Figure 4 shows the variation in gain for $V_Y = -1V$ to +1V at a frequency of 3.58MHz, for three values of V_X. Figure 5 shows the phase variation under the same conditions. In most respects, this performance is similar to that which may be achieved using more expensive custom circuitry, although the control channel of the AD539 can be more easily overloaded by a rapidly changing step input.

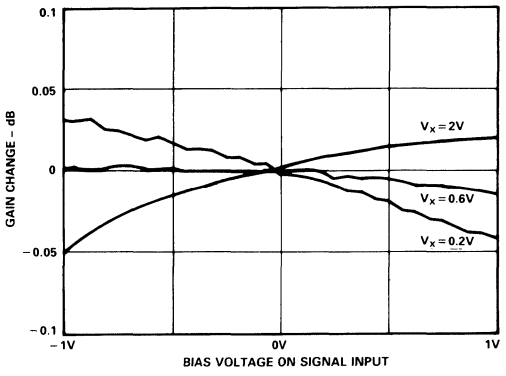

Figure 4. Differential Gain of the Voltage-Controlled Amplifier

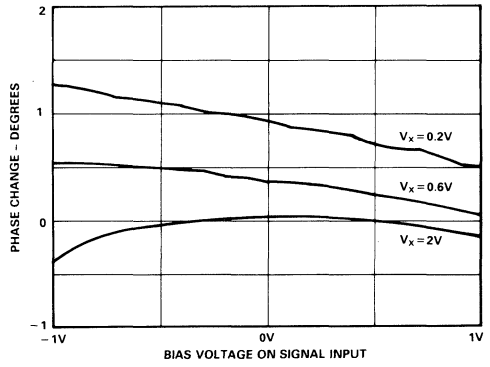

Figure 5. Differential Phase of the Voltage-Controlled Amplifier

A few final circuit details: in general, the control amplifier compensation capacitor for pin 2, C_C, must have a minimum value of 3000pF (3nF) to provide both circuit stability and maximum control bandwidth. However, if the *maximum* control bandwidth is not needed, then it is advisable to use a larger value of C_C, with typical values between 0.01 and 0.1μF. Like many aspects of design, the value of C_C will be a tradeoff: higher values of C_C will lower the high frequency distortion, reduce the high frequency crosstalk, and improve the signal channel phase response. Conversely, lower values of C_C will provide a higher control channel bandwidth at the expense of degraded linearity in the output response when amplitude modulating a carrier signal. The control channel bandwidth will vary in inverse proportion to the value of C_C, providing a typical bandwidth of 2MHz with a C_C of 0.01μF and a V_X voltage of +1.7 volts.

Both the bandwidth and pulse response of the control channel can be further increased by using a feedforward capacitor, C_{ff}, with a value between 5 and 20 percent of C_C. C_{ff} should be carefully adjusted to give the best pulse response for a particular step input applied to the control channel. Note that since C_{ff} is connected between a linear control input (pin 1) and a logarithmic node, the settling time of the control channel with a pulse input will vary with different control input step levels.

Diode D1 clamps the logarithmic control node at pin 2 of the AD539, (preventing this point from going too negative); this diode helps decrease the circuit recovery time when the control input goes below ground potential.

THE AD539/5539 COMBINATION AS A FAST, LOW FEEDTHROUGH, VIDEO SWITCH

Figure 6 shows how the AD539/5539 combination can be used to create a fast video speed switch suitable for many high frequency applications including color key switching. It features both inverting and noninverting inputs and can provide an output of ±1V into a reverse-terminated 75Ω load (or ±2V into 150Ω). An optional output offset adjustment is provided. The input range of the video switch is the same as the output range: ±1V at either input generates ±1V (noninverting) or ∓1V (inverting) across the 75Ω load. The circuit provides a dimensionless gain of about 1, when "ON," or zero when "OFF."

The differential configuration uses both channels of the AD539 not only to provide alternative input phases, but also to eliminate the switching pedestal due to step-changes in the output current as the AD539 is gated on or off.

The waveforms shown in Figures 7 and 8 were taken across a 75Ω termination; in both photos, the signal of 0 to +1V (in this case, an offset sine wave at 1MHz) was applied to the noninverting input. In Figure 7, the envelope response shows the output being fully switched in about 50ns. Note that the output is ON when the control input is zero (or more negative) and OFF for a control input of +1V or more. There is very little control-signal breakthrough.

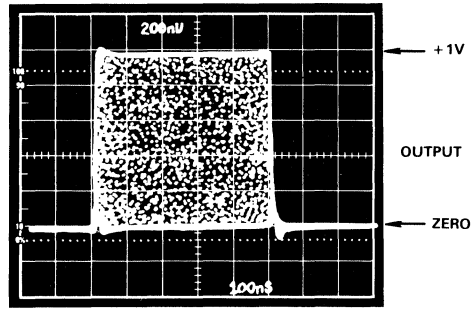

Figure 7. The Control Response of the Video Switcher

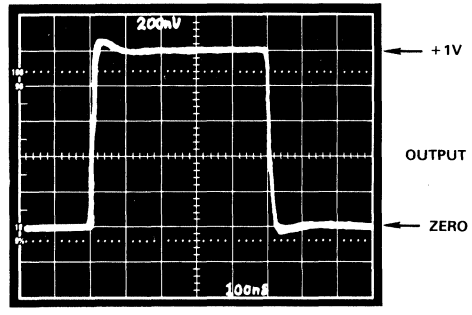

Figure 8. The Signal Response of the Video Switcher

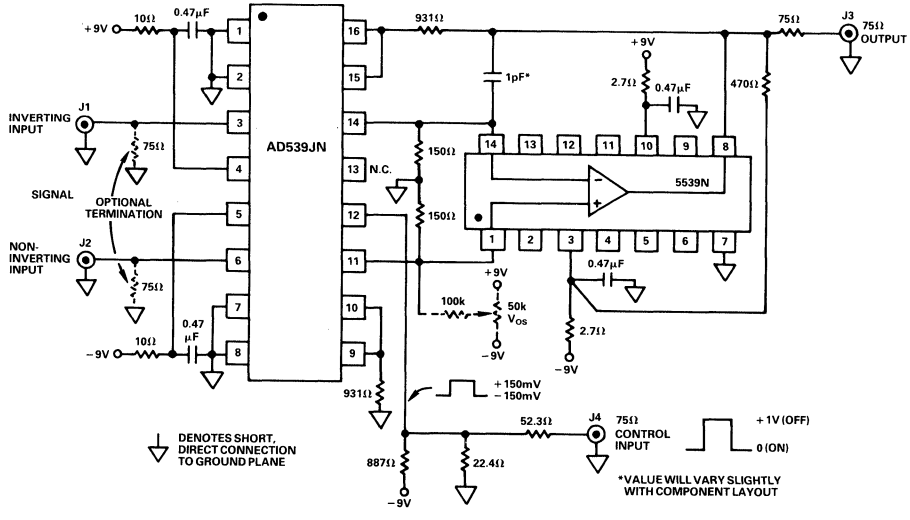

Figure 6. An Analog Multiplier Video Switch

Figure 8 shows the response to a pulse of 0V to +1V on the signal channel. With the control input held at zero, the rise-time is under 10ns. The response from the inverting input is similar.

The differential-gain and differential-phase characteristics of this switch are compatible with video applications. The incremental gain changes less than 0.05dB over a signal window of 0V to +1V, with a phase variation of less than 0.5 degree at the subcarrier frequency of 3.58MHz. The noise level of this circuit measured at the 75Ω load is typically 200μV in a 0 to 5MHz bandwidth or approximately 100nV per root hertz. The noise spectral density is essentially flat to 40MHz.

INSIDE THE AD539

Figure 9 is a simplified schematic outlining the main design features of the AD539 multiplier. Q1 through Q6, which form the translinear core of the multiplier, are multi-emitter NPN transistors having a very low base resistance, to minimize noise and distortion; emitter area scaling is also used in optimizing this crucial section of the circuit. Each of the pairs Q1-Q2, Q3-Q4, and Q5-Q6 form what is called a "controlled cascode" circuit; this is basically a grounded-base transistor to which has been added another device which removes some of the signal from the emitter. This alters the gain of the cascode, from almost unity (when *no* current is removed) to zero (when *all* the signal is removed). The "controlled cascode" configuration has very desirable characteristics for use in two-quadrant multiplication.

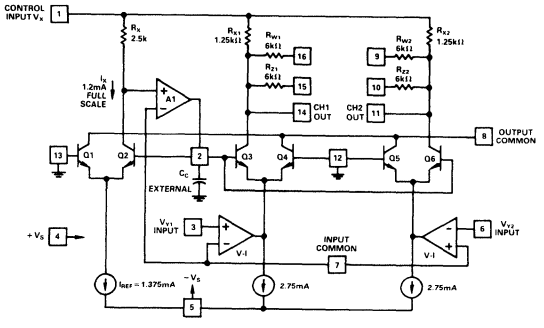

Figure 9. A Simplified Schematic of the AD539 Analog Multiplier

A stable 1.375mA reference current (which determines the multiplier scaling) is supplied to the common emitters of the controlled-cascode Q1-Q2, whose bases are biased by the control amplifier (a high speed op amp). When the control input V_X is zero, Q2 is biased off. This bias voltage is conveyed to Q3 and Q6, which are likewise turned off; signal transmission to the outputs is thus blocked. As V_X increases, the current through R_X (I_X) is forced to flow in the collector of Q2; this current only represents a fractional part of the 1.375mA reference current. When $V_X = 3V$ (its nominal full-scale value), 1.2mA flows in R_X and Q2; this is 0.873 (or 87.3%) of the reference current. Correspondingly, the *same fraction* of the signal and bias-currents that is supplied to the common emitter nodes of controlled cascodes Q3-Q4 and Q5-Q6 is conveyed to the two outputs.

Now consider the signals paths. The voltages V_{Y1} and V_{Y2} are converted to currents by V-I converters which have a transresistance of 1.74kΩ. At full-scale input of ±2V, the signal current supplied to the cascodes is ±1.15mA; this is superimposed on a bias current of 2.75mA. Thus, when $V_X = +3V$, the collector currents of either Q3 or Q6 will consist of a signal component of ±1mA (0.873 × 1.15mA) and a DC component of 2.4mA, both of these currents being proportionally less for other values of V_X. The DC component is removed by resistors R_{X1} and R_{X2}, driven directly from V_X. The final output is thus a current of value:

$$I_W = \frac{V_X}{1V} \times \frac{V_Y}{6k\Omega}$$

Note that the peak value of V_Y can be ±4.2V (using a $-V_S$ supply of at least −7.5V) and V_X can overrange by 10% to +3.3V, so the *peak* output current of each channel can be slightly more than ±2mA, for a maximum of ±4mA when the channels are used in parallel. These currents may be delivered directly to grounded load resistors or to terminated coaxial cables. With coaxial cables, the full 60MHz bandwidth of the AD539 can be realized, but the peak signal amplitude will be quite limited (to only ±330mV using a 75Ω load). Clearly, some additional gain is needed.

Unfortunately, the amplifiers necessary for additional gain could not be included on the AD539, due mainly to power dissipation considerations. Also, gain errors (of up to ±1.5dB) will occur using a simple load resistor, because of the 20 percent tolerance of the thin-film resistors. Fortunately, by using external op amps, the output currents may be converted to much larger voltages, using on-chip applications resistors R_W and R_Z provided for this purpose. These resistors have a nominal value of 6kΩ, but they are laser-trimmed during manufacture so as to result in high gain accuracy when used as the feedback resistors around an inverting op amp. When using just R_W (R_{W1} for CH1, R_{W2} for CH2), the transfer characteristic becomes:

$$V_W = I_W \times R_W = \frac{V_X}{1V} \times \frac{V_Y}{6k\Omega} \times 6k\Omega = \frac{V_X V_Y}{1V} \text{ for } V_X > 0$$

When R_W and R_Z are used in parallel, the gain is halved, that is:

$$V_W = \frac{V_X V_Y}{2V}$$

The bandwidth is now largely determined by the op amp. For wideband applications, the 5539N is an ideal low-cost complement to the AD539; this combination is capable of providing ±1V into a 75Ω load with only a very small degradation of the 60MHz bandwidth achieved by the AD539 alone.

LAYOUT OF VIDEO-BANDWIDTH CIRCUITRY

Careful component layout, adequate power supply bypassing, and proper coaxial cable termination are all very important in the implementation of video-bandwidth circuits in general. Unfortunately, even when these precautions are taken, some added difficulties can still arise in the case of voltage-controlled amplifiers. This can happen when leakage of the input signal to the output occurs when the gain should be zero. This feedthrough will cause ghost images which are generated by the high-frequency components of the unwanted signal.

A good ground plane is essential! To help assure this, it is recommended that part of this ground be run between the rows of the pins of both chips, on both the upper and lower surfaces of the PC board. The ground plane for a typical AD539/5539 layout is shown in Figure 10. In addition, all decoupling capacitors must have *minimum* lead lengths to this ground plane. Also, the input and output connections *must* be kept short, and should be physically separated as far as possible from each other. Separate power supply decoupling for the AD539JN and 5539N is also recommended.

Proper cable termination is also essential for adequate high-frequency performance. One-quarter-watt carbon resistors are well suited for this function since they are noninductive and quite inexpensive; one-percent-metal film resistors may also be used, although their inductance should be measured first (since this property of the resistor may vary with each manufacturer). Avoid using wirewound resistors for termination!

The VCA described in this application note was designed to operate directly into a 75Ω load; therefore, "back-termination" (i.e., a series resistor which halves the load voltage) was not used. In most cases, the weak reflection from a short (up to 6 feet) directly driven cable will not cause any visible effects. However, when using very long cables, it may be necessary to insert a 75Ω resistor in series with the output of the 5539N to absorb these reflections.

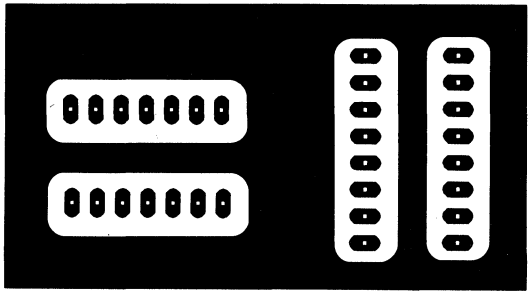

Figure 10. Layout of a Typical AD539/5539 Ground Plane

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Ground Rules for High-Speed Circuits

Layout and Wiring Are Critical in Video-Converter Circuits

How to Keep Interference to a Minimum

by Don Brockman and Arnold Williams

In recent issues, **Analog Dialogue** *has dealt extensively with topics in shielding and grounding,[1, 2] emphasizing the techniques needed to protect the integrity and precision of analog signals in the dc and audio-frequency domain from interfering signals, whether at line frequency or at much higher frequencies. To complement those articles, we suggest here the elements of good practice for high-resolution "video speed" converters, i.e., converters of 10-bit or greater resolution, operating at word rates above 1 MHz.*

Electronics may be frustrating for designers who cross the threshold from low-resolution-low-speed to high-resolution-high-speed designs, or from digital to analog-signal-conditioning circuits. For them, it often seems the "ground rules" have changed.

Experienced designers can readily attest to the difficulty of obtaining consistent grounds. They can relate stories about the ground that wasn't where they thought it was, or the ground that wasn't there at all, despite a conviction that "it has to be." On printed-circuit (p-c) boards, wires and/or runs that seemed to be perfectly good grounds are transformed into inductors or worse in high-speed or high-frequency circuits.

At ADI's Computer Labs Division, where high-speed circuits are its bread and butter, applications engineers have found that grounding is the focus of a large percentage of questions from designers making their initial foray into high-speed circuits. In most cases, the designers encountered difficulties as the result of being unaware of—or ignoring—certain basic ground rules.

BASIC PC-CARD RULES

Knowledgeable high-speed circuit designers have learned that *every* square inch of a printed-circuit board which doesn't contain circuits or conducting runs should be ground plane. Violating that simple rule invites disaster. But sometimes, strict adherence to the rule is still no guarantee of success if circuit density is too high; then one must reduce the density and create more "real estate" for the ground plane.

Our applications engineers strongly recommend that all bread-board designs be done on double-sided copper-clad boards. Although this is not a sure cure for ground problems, it improves the designer's chances.

Another basic rule for working with high-speed and/or high-frequency printed-circuit-board designs is to connect analog ground and digital ground together within the PC board. This technique is used, for example, in Analog Devices card-level high-speed a/d converters (e.g., MOD-1005, MOD-1020, MOD-1205, CAV-0920, and CAV-1210). Connecting the two grounds enhances the performance of the converters when they are operated either by themselves or as tightly knit subsystems. However, it can raise some system-level problems, to be discussed below.

Another rule for printed-circuit-board designs containing analog and digital circuitry is to use every available spare pin for making ground connections, and to use those pins to separate the analog and digital signals entering or leaving the board.

Avoid using purely insulating (e.g., "Vector") bread-boards and small-diameter hookup wire (e.g., #24) for connections, including supply voltages and grounds. The approach will create ground and noise problems if the circuit is intended to operate at 1 MHz or more (it will probably lead to problems at even slower speeds).

To summarize: Use double-sided copper-clad boards with maximum ground area and heavy, well-located power-supply and ground-return leads. Tie rounds together locally.

[1]Alan Rich, "Understanding Interference-Type Noise," *Analog Dialogue* 16-3, 1982, pages 16-19.
[2]Alan Rich, "Shielding and Guarding," *Analog Dialogue* 17-1, 1983, pages 8-13.

GENERAL CIRCUIT PRACTICE

Any subsystem or circuit layout operating at high speeds with both analog and digital signals needs to have those signals physically separated as much as possible to prevent possible crosstalk between the two. Digital signals leaving or entering the layout should use runs that have minimum length. The shorter the digital runs, the lower the likelihood of coupling to the analog circuits.

Analog signals should be routed as far from digital signals as size constraints allow; and the two, ideally should never closely parallel one another's paths. If they must cross, they should do so at right angles to minimize interference. Coaxial cables may be necessary for analog inputs or outputs—a demanding condition mechanically, but sometimes the only solution electrically.

When combining track-and-hold and a/d-converter hybrids or modules on the same board, keep them as close together as is practical. All grounds need to be connected to the single, low-impedance ground plane: and the connections should be made right at the units themselves (another argument for having large amounts of good, solid ground plane available all over the p-c board).

A suggested practical approach for accomplishing this is illustrated in Figure 1, which shows a flow-chart layout, as the preferred method for combining high-speed analog and digital circuits on a p-c board.

If one assumes a 10-volt input range on the 12-bit a/d converter, the least-significant bit (LSB) of the ADC will have a value of 2.5 mV (10 V/4,096). Assume that a single pin of the p-c connector, which is used for ground, has a resistance of 0.05 ohm—and that the p-c card draws a total of 1.5 amperes.

The voltage drop at the ground pin could be 75 millivolts in these circumstances. If only digital logic were used, this voltage drop would be minuscule, hardly worth considering. However, the hypothetical real-world situation being considered here is a mixture of both analog and digital circuits, and the 75 mV can have a significant impact on the subsystem's performance.

In this example, the digital circuits are TTL. Since TTL is a saturated logic, ground currents vary widely, and varying current flowing through the ground often produces noise signals which modulate the ground plane. This noise, created by digital switching, can couple into the analog portion of the circuit and have an important effect on performance, even at low digital levels. For example, if only 10% of the 75-millivolt I-R drop cited here couples into the analog signal, that would represent 3 LSBs.

The result? The circuit intended for operation as a 12-bit system is now reduced to a system of 10 to 11 bits, because of noise masking the 2.5-millivolt level of the desired 12-bit LSB. The recommended solution? Assign multiple pins for ground connections, to reduce the total contact resistance. As Figure 1 shows, those pins are also used to separate the analog and digital signals.

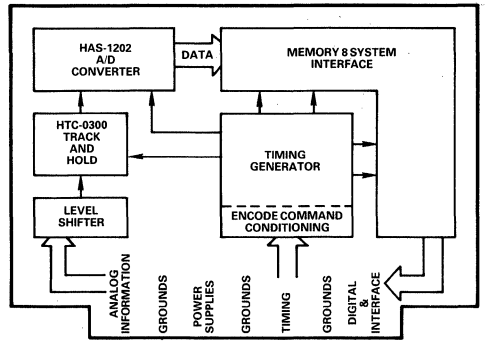

Figure 1. "Flow Chart" Layout for Logical Separation of Functions.

This design approach may seem unnecessarily rigorous and time-consuming but can prove rewarding when the p-c board is installed in its final system location.

Locate the timing circuits near the center of the board (Figure 1) because the timing is at the heart of the circuit, being connected to all of the major circuit components of the board. A central location helps assure minimum paths for the digital signals.

Variations of this theme may not use the exact same components or functions, but the same basic techniques should be applied in any design containing analog and digital circuits. For cards with all connections at one end, avoid configurations which have analog circuits near the p-c connector, and digital signals at the opposite end of the card—or vice versa; either situation will cause analog and digital paths to pass in close proximity to one another.

SYSTEM GROUNDING

Although local ties for analog and digital grounds help the performance of a card, they can cause problems for the system designer using ADCs and DACs. In systems, data converters should be considered as *analog* (not digital) components; the system design must be assigned to experienced and capable analog engineers, who are used to defending millivolt signals against interference.

Place ADCs and DACs (like other analog devices) near other parts of the analog section, because: (1) reflections make it hard to transmit analog signals more than a short distance without loss of bandwidth and amplitude; and (2) noise generated by the digital section can couple into the analog through the ground plane or power supplies, or radiate to nearby analog components.

Each card in the system should be returned directly to the power supply common, using heavy wire. Where it is mandatory that a card's analog and digital grounds be separated, each should be separately returned to the power supply; don't connect the two grounds and return a single ground line to the power supply.

POWER SUPPLIES

Besides ground rules, designers of high-speed circuits must also consider the rules about power supplies to obtain best results.

Every power-supply line leading into a high-speed p-c card or data-acquisition circuit must be carefully bypassed to its ground return to prevent noise from entering the card. Ceramic capacitors, ranging in value from 0.01 to 0.1 μF, should be used generously in the layout, mounted as closely as possible to the device or circuit being bypassed; and at least one good-quality tantalum capacitor of 3 to 20 μF should be assigned to each power-supply voltage, mounted as near as possible to the incoming power pins to keep potentially high levels of low-frequency ripple off the card.

To some extent, the p-c's power-supply connector pins can introduce noise problems. If their contact resistance is sufficiently high, and a varying current is flowing, the varying IR drop which results is noise and can be coupled into parts of the card. This caution applies especially to +5-volt supplies used to power TTL systems, but the problem can be alleviated with a variation of the rule about multiple pins for making ground connections. Parallel the I-R drops by also using multiple pins for power connections.

Low-noise, low-ripple temperature-stable linear power supplies are the preferred choices for high-speed circuits. Switching power supplies often seem to meet those criteria, including ripple specifications. *But ripple specs are generally expressed in terms of rms*—and the spikes generated in switchers may often produce hard-to-filter, uncontrollable noise peaks with amplitudes of several hundred millivolts. Their high-frequency components may be extremely difficult to keep out of the ground system.

If switchers cannot be avoided for high-speed designs, they should be carefully shielded and located as far away from the "action" as possible, and their outputs should be filtered heavily.

ABOUT IC DESIGNS

There is often a difference in implementing designs using high-precision IC circuits vis-à-vis p-c card designs using modules or hybrids. Some ICs are specifically designed to keep analog and digital grounds separated within the device, because they would be unable to perform their functions properly without the separation.

Recognizing this, IC manufacturers are generally very careful in detailing how to obtain optimum performance from their devices. Those details of the application notes frequently instruct the user to connect analog and digital grounds for the device together externally; when they do, the connection needs to be made as closely as possible to the device. In other, much rarer, instances, the characteristics of an individual device—or system—may require some remote connection of the grounds.

The best approach for getting optimum performance from any device is to follow diligently the recommendations of the manufacturer. If the recommendations are missing or vague, ask for them.

Logical signal flow generates logical treatment of ground paths and ground connections— a logical way to prevent potential problems.

ANALOG DEVICES

AN-215A
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Designer's Guide to Flash-ADC Testing

Part 1
Flash ADCs Provide the Basis for High Speed Conversion

by Walt Kester

Building high-performance circuits that take advantage of the high sampling rates of flash ADCs requires a knowledge of these converters' many intricacies. Part 1 of this 3-part series discusses the pitfalls of designing with flash ADCs, how to evaluate certain data-sheet specifications, and how to choose external components that complement your particular converter. Parts 2 and 3 will explore test and measurement methods that you can use to verify a converter's performance in your system.

Walt Kester, *Computer Labs Div, Analog Devices*

To digitize analog signals whose bandwidths exceed 1 MHz, you'll probably need flash ADCs. Many flash converters with 4 to 10 bits of resolution are now available, thanks to recent advances in VLSI process technology and design techniques. However, to use these converters successfully at the high sampling rates that they provide, you must take into account and compensate for a variety of flash-converter characteristics.

The basic features of most flash converters are shown in **Fig 1.** A flash ADC simultaneously applies an analog-input signal to $2^N - 1$ latched comparators, where N is the number of the converter's output bits. A resistive voltage divider generates each comparator's reference voltage and sets each reference level 1 LSB higher than the level of the comparator immediately below it. Comparators that have a reference voltage below the input-signal level will assume a logic 1. The comparators with a reference voltage above the level of the input signal will produce a logic 0. A secondary logic stage decodes the thermometer code that results from the $2^N - 1$ comparisons. An optional output register latches the decoding stage's digital output for one clock cycle.

Timing is everything

One of the first difficulties you'll encounter when using flash converters is removing valid data from the converter. In practice, the comparator bank has two states controlled by a conversion-command signal. Various converters call this command the convert, the encode, or simply the clock command. When this signal is in its convert-command state, the comparators track the analog-input signal, and during this time the output data is invalid. When the command line changes state, it latches the comparator outputs. Valid output data is now available for transfer to an external register. You'll find most flash converters somewhat sensitive to the duty cycle and frequency of this command pulse. In other words, the performance of the converter, specifically its differential and integral nonlinearity performance, is related to the clock's duty cycle and frequency. Performance degradation is especially pronounced when you run the device at or near its maximum sampling rate.

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Because of recent advances in VLSI processing and design techniques, many flash converters that have from 4 to 10 bits of resolution are available.

The way you handle the binary output depends on whether the converter has an internal output latch. Without a latch, the data will be invalid for a period equal to the sampling clock's pulse width. At high sample rates, the data-invalid time will impinge on the data-valid time, making it difficult for you to strobe the flash converter's output into an external register. For instance, if you operate a flash converter at 100M samples/sec with a 50%-duty-cycle sampling clock, the output data will be valid for only 5 nsec. When you consider the finite rise and fall time of the output binary bits, this short time doesn't leave you much leeway, even if you use the fastest external logic. In fact, you may ultimately lose data. The addition of an internal output latch simplifies clocking of the output data, because the output data is valid for approximately the entire clock cycle. In return for a longer data-valid time, you'll have to accept an inherent 1-cycle or more pipeline delay—an acceptable compromise in most systems applications.

Try to place an appropriate buffer register next to the flash converter. If you route the converter's digital output directly to a backplane data bus through a card-edge connector, signal coupling between the digital-output signals and analog input will degrade the S/N ratio and harmonic performance.

In many high-speed data-acquisition designs, you'll need a large and fast buffer memory to store the output data. A 500M-sample/sec converter can fill 1M byte of memory in 2 msec. To reduce the required speed—and thus the cost—of the memory, you can demultiplex the high-speed data stream (**Fig 2**), which slows it to frequencies compatible with cost-efficient CMOS RAMs. **Fig 2**'s circuit clocks the two output registers at half the sample rate, and it latches data in each register 180x out of phase from the other. Some flash converters that operate in excess of 200 MHz have onboard demultiplexing for added convenience.

All that sparkles isn't gold

So far, these timing difficulties refer to how you deal with the converter's output data. But flash converters can have internal problems as well. Low input frequencies can cause comparator metastability, and

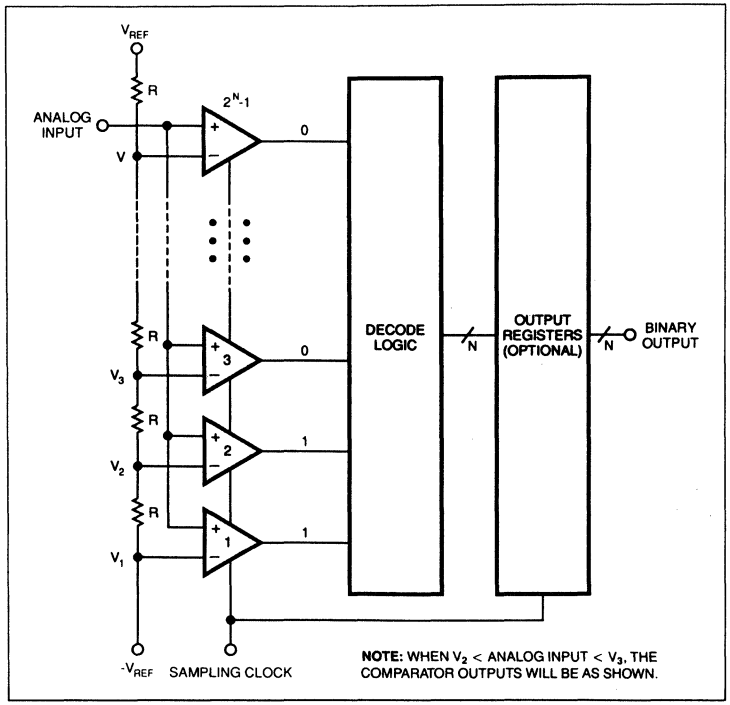


***Fig 1—Flash converters contain a bank** of 2^N-1 comparators, where N is the number of output bits. Decoding logic transforms the comparator outputs into the appropriate N-bit result. Timing and input characteristics of the converter, such as mismatched comparator delays, mismatched ladder resistors, and nonlinear input capacitances, are just a few sources of converter errors.*

high input frequencies can lead to errors caused by slew-rate and delay mismatches. All of these errors may manifest themselves as sparkle codes in a poorly designed flash converter.

Sparkle codes are random errors whose magnitude may approach the full-scale range of the converter. The term refers to the white dots or "sparkles" that appear against a gray background when the ADC output drives a video display. There are two sources of sparkle codes: comparator metastable states and thermometer-code bubbles.

A comparator metastable state occurs if the comparator output falls between the logic-0 and logic-1 threshold of the digital decoding logic. If the threshold uncertainty region has a width of ΔV_L and the comparator has a gain of A, then the error probability P_m is a uniformly distributed value that's equal to

$$P_m = \frac{\Delta V_L}{Aq},$$

where q is the weight of the LSB.

A latched comparator in a flash converter has a regenerative gain of

$$A = A_0 e^{t/\tau}$$

when $t>0$, and

$$A = A_0$$

when $t \leq 0$. τ equals the regeneration-time constant, and t is the time after the application of a latch command. The probability of a metastable state, P_m, for a regenerative comparator bank driving decoding logic is

$$P_m = \frac{\Delta V_L}{A_0 q} e^{-t/\tau}.$$

The magnitude of the sparkle code depends on the location of the metastable comparator in the comparator bank and on the logic-decoding scheme. For instance, the 128th comparator determines the MSB of an 8-bit flash converter with straight binary decoding logic. If this comparator's output is in a metastable state, the decoding logic may mistakenly convert the input voltage whose correct binary representation is 01111111 to 11111111, producing a full-scale error. If the comparator bank's thermometer-code output is first decoded into Gray code, latched, and then converted into binary code, the metastable error is reduced to 1 LSB, regardless of the comparator in error. Flash converters, however, rarely use this scheme because of the ripple-through time and the increased logic density of the Gray-to-binary circuitry. Instead, converter designers often use "pseudo-Gray" decoding techniques to eliminate the delay time associated with traditional Gray-to-binary circuits.

Note that the probability of a metastable-state error increases as the time-after-latch, t, decreases (assum-

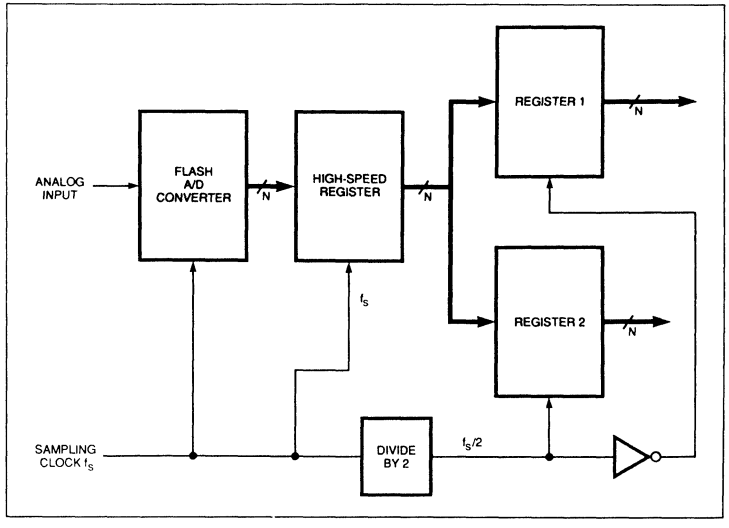
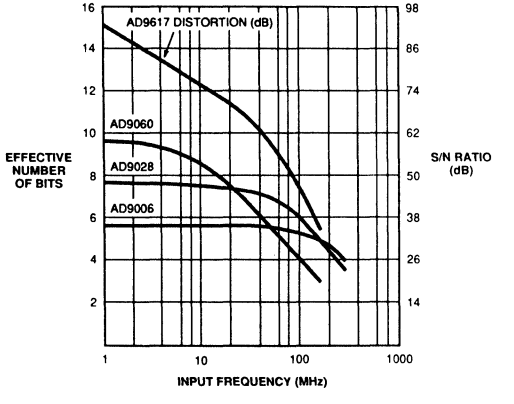


***Fig 2—Flash converters can operate** at extremely high sample rates. Thus, you must have an output register that can handle this fast data. By demultiplexing the converter's outputs, you can slow the data to a rate that's compatible with standard CMOS memory.*

One of the first difficulties you'll encounter when using flash converters is removing valid data from the converter.

ing a constant value of τ). This implies that the flash converter is more apt to produce metastable-state errors as you increase the sampling rate, because t must decrease correspondingly. Most manufacturers reduce metastable comparator states by minimizing the regeneration-time constant, τ. Lower regeneration-time constants result in higher power dissipation, which is one reason why many high-speed flash converters are power-hungry devices.

Thermometer-code bubbles are another potential source of sparkle codes. A well-behaved flash converter's comparator bank produces a specific sequence of ones up to a certain point in the input range of the converter, and it produces a sequence of zeros beyond that point. The decoding logic then assigns a binary number to the thermometer code. For low-frequency inputs, most flash converters' comparator banks are well behaved. At high speeds, however, delay mismatches among comparators may produce out-of-sequence ones and zeros in the thermometer code. The decoding logic then assigns an error binary code to these out-of-sequence points, or bubbles, which also result in sparkle codes. Again, proper comparator design and more sophisticated decoding-logic circuitry



FLASH ADC	RESOLUTION (BITS)	MAXIMUM SAMPLING RATE (M SAMPLES/SEC)	TEST SAMPLING RATE (M SAMPLES/SEC)
AD9060	10	75	60
AD9028	8	300	250
AD9006	6	500	400

***Fig 3—Theoretically, a flash converter should maintain its performance** across the full Nyquist bandwidth. But as the curves in this figure illustrate, the S/N ratio starts to degrade well below each device's maximum sampling rate. (Note that these curves are based on test sampling rates that are somewhat lower than each device's maximum possible rate.)*

within the ADC itself can reduce these errors to acceptable levels.

These comparator-timing errors degrade both the differential and integral linearity of a flash ADC as the input slew rate increases. In addition to static errors, such as missing codes and sparkle-code errors, slew-rate limitations manifest themselves as dynamic errors, such as increased harmonic distortion and degradation in the S/N ratio. Ideally, a flash converter should maintain its static performance specifications across the full Nyquist bandwidth, and certain applications demand full performance beyond the Nyquist bandwidth. The theoretical, rms S/N ratio for an N-bit ADC is given by the well-known equation

$$\text{S/N ratio} = 6.02N + 1.76 \text{ dB}.$$

However, as shown in a typical plot of S/N ratio versus input frequency for actual flash converters (**Fig 3**), the S/N ratio degrades as the input frequency increases. This degradation starts well below these converters' maximum sampling rates. The left vertical axis of **Fig 3** shows the S/N ratio in another term: effective number of bits. The effective number of bits is simply the value of N when you solve the above equation using a specific value for the S/N ratio. Aperture jitter (sample-to-sample variations in the effective-sampling instant) can also cause degradation in the overall S/N ratio for high-slew-rate inputs. Jitter can be internal or external to the converter. Part 3 of this series will cover this topic in more detail. To minimize externally produced jitter components, you should always practice proper grounding, power-supply-decoupling, and pc-board-layout techniques.

Watch for dangerous data-sheet territory

Most of the timing difficulties and error sources discussed so far are common to all flash converters. However, each converter features its own unique design and specifications; thus the data sheets require scrutiny. Don't be fooled into believing that sampling rate and input bandwidth are interchangeable; they're different specifications. It wasn't until recently that you'd even find input bandwidth specified for an ADC. Even now, no accepted industry-wide definition exists for a flash converter's full-power-bandwidth specification. Scrutinize the data sheet carefully and make sure you understand the manufacturer's definition and test method. The full-power bandwidth of a traditional op amp is the maximum frequency at which the amplifier

can produce the specified p-p output voltage at a specified level of distortion. Another commonly used definition calculates the full-power bandwidth by dividing the amplifier's slew rate by $2\pi V_O$, where the output-voltage range of the amplifier is $\pm V_O$.

When you apply traditional analog-bandwidth definitions to flash converters, the results can be misleading. The dynamic-error sources previously discussed may become predominant long before the comparator front end approaches its maximum bandwidth. If you use a common definition of full-power bandwidth as the frequency at which the p-p reconstructed-sine-wave output is reduced by 3 dB for a full-scale input, then the effective number of bits (S/N ratio) at this input frequency may render the flash converter useless in your system. Thus, to get a true idea of a converter's performance, you must consider both the full-power bandwidth and the effective number of bits (S/N ratio) at a specific sampling rate.

Another definition you'll encounter occasionally for full-power bandwidth is the maximum, full-scale input signal at a specified sampling rate that produces no missing codes. Using this definition always gives the most pessimistic number, so specifications based on this definition appear on only a few data sheets. The following is a recently proposed definition for full-power bandwidth (courtesy Chris Manglesdorf, a senior scientist at Analog Devices): the frequency at which the fundamental component of the reconstructed FFT output—excluding harmonics—is reduced by 3 dB from full scale.

Just when you think you've mastered the intricacies of flash ADCs, you'll realize that you have another component to worry about: the input buffer amplifier. Fortunately (or unfortunately depending upon your perspective), the flash converter—not the amplifier—usually limits the converter's dynamic performance. A flash converter typically digitizes a signal from a 50, 75, or 93Ω bipolar or unipolar source. If the input range of the flash converter is incompatible with the signal, then you'll clearly need a wideband op amp to generate the required gain and offset (**Fig 4**). In addition, the input capacitance of some flash converters may vary as a function of the analog input's signal amplitude. Therefore, so that the nonlinear capacitance doesn't produce undesirable harmonics in the digitized signal, you'll need to use a buffer amplifier for isolation. For certain flash converters, the input capacitance is so high that a buffer amplifier is needed just to preserve the signal bandwidth.

A good choice for the buffer is a high-speed transimpedance amplifier. These amplifiers have high bandwidths and flat frequency responses over a broad range of input frequencies. Also, many transimpedance amplifiers exhibit extremely low distortion. Pairing the right amplifier with your converter is important. For instance, **Fig 3** shows the S/N ratio of various converters plotted along with the harmonic distortion of the AD9617. Since the THD of the amplifier is better than the S/N ratio of the converters, the amplifier won't degrade the flash converters' performance over the major portion of their usable bandwidth.

Another factor to consider when driving the input of flash converters is the input-signal polarity. Positive input signals, which forward bias the substrate diode, can damage a converter that has a unipolar, negative input-voltage range. Installing an external Schottky diode provides effective protection.

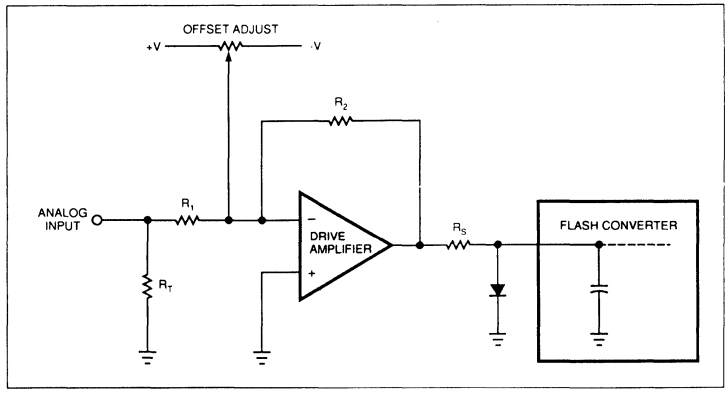


***Fig 4—If the voltage range of the analog signal** and the input range of the ADC aren't compatible, you'll have to adjust the gain using R_1 and R_2 and also adjust the input signal's offset. Because of the substantial value and the often nonlinear nature of a flash converter's input capacitance, you must choose an appropriate drive amplifier and value for R_S.*

Ideally, a flash converter should maintain its static-performance specifications across the full Nyquist bandwidth, but in reality ADCs fall far short of this ideal.

The flash converter's input capacitance and the drive amplifier's isolation resistor, R_S, form a lowpass filter. Typical series-resistor and input-capacitance values of 10Ω and 20 pF create a single-pole lowpass filter that has a bandwidth of 800 MHz. However, if the input capacitance changes from 20 to 15 pF over the input range of the converter, then an attenuation error of 1.4% occurs for a 50-MHz input signal. This 1.4% nonlinearity will produce 37 dBc of harmonics. (The unit dBc refers to the number of dB between the signal you're measuring and the carrier frequency). If you minimize the value of R_S and still maintain op-amp stability, you can reduce the attenuation error caused by these lowpass filtering effects. The signal dependence of input capacitance is rarely specified, but as converters move toward higher bandwidths, you can expect to see this parameter on more data sheets.

Few, if any, flash converters contain an internal voltage reference, so in addition to an external drive amplifier, you must also design your own voltage-reference generator. **Fig 5** illustrates a typical −2V, unipolar reference-voltage circuit for a flash converter. A buffer transistor is necessary because the resistance of the converter's ladder string is usually fairly low. The total reference-ladder resistance of a flash converter depends heavily on the fabrication process and may vary considerably from device to device. Also, the ladder's resistance may exhibit a large temperature coefficient.

If the flash converter allows bipolar operation, then you'll have to generate two reference voltages. The circuit in **Fig 6** allows great flexibility in setting both the gain and the offset of a bipolar flash converter, and it operates on ±5V power supplies. A few flash converters provide a sense pin for the voltage reference. You can use this pin to compensate for the voltage drop caused by the package's pin and bond-wire resistances, as shown in the bipolar-reference circuit in **Fig 6**. In addition, some ADCs give you access to one or more taps along the internal, reference-ladder resistor string. To achieve better integral linearity, you can drive these taps from low-impedance sources.

Improve dynamics with T/H amplifiers

As previously discussed, the effective-sample time-delay variations among the latched comparators degrade the S/N ratio and the harmonic performance. You can visualize the individual comparators within an array as having variable delay lines in series with their latch-strobe inputs. To understand the effect of this delay on performance, consider an 8-bit, 100M-sample/sec flash converter that's digitizing a full-scale, 50-MHz sine-wave input. You can express the sine wave as

$$v(t)=V_P\sin 2\pi ft.$$

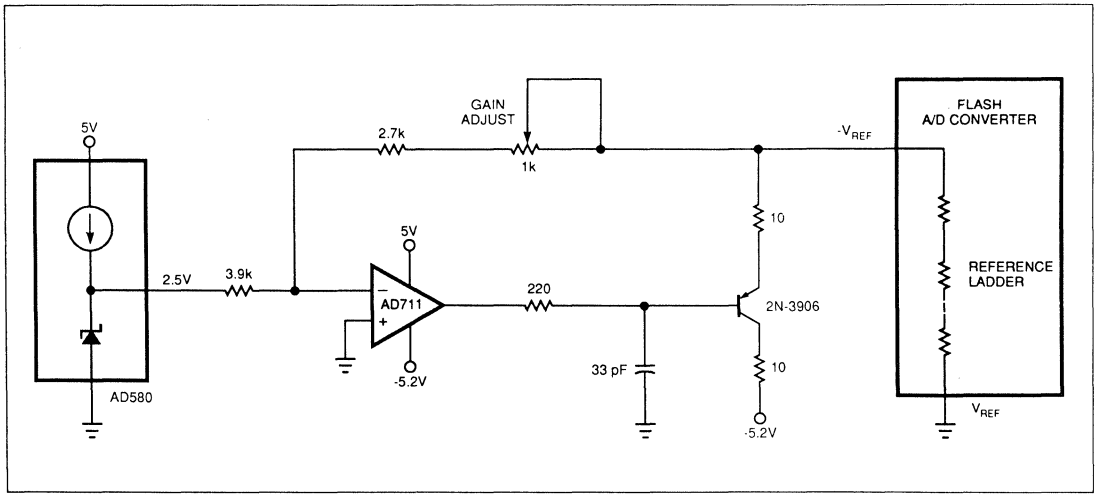


Fig 5—Flash converters don't have internal references, *so you must design them externally. This particular circuit provides a stable −2V reference for a unipolar converter.*

To improve flash-converter performance at sampling rates as high as 25 MHz, you can use front-end T/H amplifiers to implement a "track-and-slow-down" approach.

The maximum rate-of-change of this signal occurs at the zero-crossing point and is equal to

$$\left.\frac{dv}{dt}\right|_{max}=2\pi f V_P=\left.\frac{\Delta v}{\Delta t}\right|_{max}.$$

By solving this equation for Δt_{max}, you obtain

$$\Delta t_{max}=\frac{\Delta V}{2\pi f V_P}.$$

If the input-voltage range of the flash converter is 2V, or $V_P=1V$, then the LSB weight is 8 mV for an 8-bit ADC. For the flash converter's error to be less than 1 LSB, Δt_{max} must equal 25 psec. The effective-sample delay mismatch between comparators can't exceed this value. If the mismatch is greater, a 50-MHz, full-scale sine-wave input will produce missing codes in the converter's output.

Placing an ideal track-and-hold (T/H) amplifier ahead of the flash converter theoretically would eliminate this problem, because the flash converter basically would be digitizing a dc input. In actual practice, T/H amplifiers aren't ideal, especially at high speeds. The signal presented to the flash converter is still changing, although at a slower rate. Nevertheless, this "track-and-slow-down" approach can improve the flash-converter performance at sampling rates as high as approximately 25 MHz. At sampling rates above 25 MHz, the T/H circuit needs to be mounted on the same substrate as the flash converter in a suitable hybrid package. Monolithic T/H amplifiers in hybrid packages with 8-bit flash converters have successfully achieved 7 effective bits at Nyquist inputs and at sampling rates of 250 MHz. These hybrid packages exact a penalty of higher cost and power consumption, however.

You'll find it difficult to select an appropriate discrete T/H amplifier, because the interaction between the T/H amplifier and the flash ADC is hard to predict. You should evaluate key T/H amplifier specifications such as acquisition time, full-power bandwidth, slew rate, and harmonic distortion. Harmonic-distortion specifications typically are provided for the track mode. The T/H amplifier's performance may be considerably

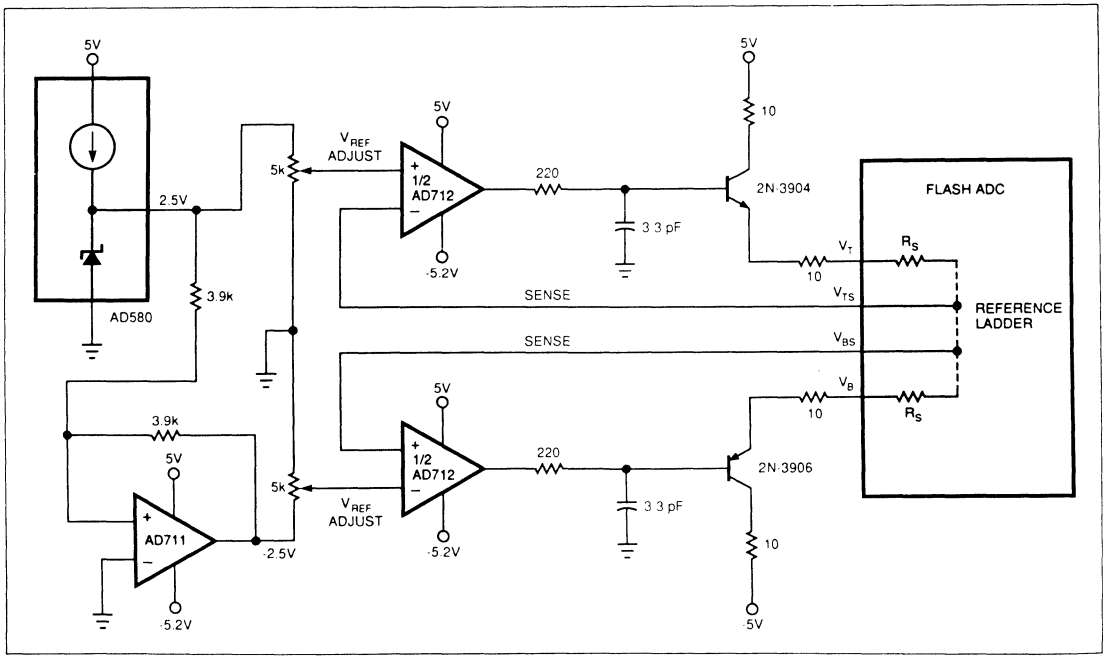


Fig 6—This reference generator *for a bipolar flash converter uses the sense pins provided by the resistor ladder to compensate for the voltage drops in the package's pin and bond-wire resistances.*

worse than the stated specifications when the amplifier is in the hold mode and actually driving a flash converter. Also, the loading effects of the converter may degrade the T/H amplifier's performance. In addition, obtaining the optimum relationship between the various timing pulses that drive the T/H amplifier and the flash converter may require considerable experimentation.

Because of these many difficulties, the current goal of many ADC manufacturers is either to provide flash converters whose dynamic performance is acceptable without a T/H function, or to integrate the T/H function and converter on the same chip. In either case, manufacturers can fully specify the ADC for dynamic performance and spare you the somewhat difficult design problems associated with interfacing the T/H amplifier to the converter.

The knowledge of internal ADC features and the requirements these ADCs place on external circuits should guide your initial design efforts. But once you finish the design and build your circuit, you'll want to ensure that the combined performance of your converter and its support circuits meets your requirements. Part 2 will discuss various DSP-based test methods that are particularly effective in flash-converter testing. EDN

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Designer's Guide to Flash-ADC Testing

Part 2
DSP Test Techniques Keep Flash ADCs in Check

by Walt Kester

By testing your flash A/D converter, you can ensure that it's faithful to all the specifications listed on its data sheet. Part 2 of this 3-part series presents a number of methods, including sine-wave curve fitting and the FFT, that you can use to test flash converters. Readily available benchtop instruments or personal computers are the only equipment that you'll need to use these methods.

Walt Kester, *Computer Labs Div, Analog Devices*

It's important to know how your flash A/D converter will perform in real-world applications. Therefore, you may want to perform any one of a variety of tests on your converter to determine its deviation from ideal performance. As Part 1 of this series discussed, flash ADCs exhibit errors due to static and dynamic nonlinearities, and these errors increase as the input signal's slew rate increases. Thus, the actual S/N ratio will fall short of the converter's theoretical value. Even if you don't apply these tests yourself, becoming familiar with them will help you evaluate data-sheet specifications more accurately, because many manufacturers use these same methods.

Another reason you may want to test your flash converter is to gain information that the manufacturer doesn't provide. Specifications such as S/N ratio and its related effective number of bits are key in all applications and are normally specified, but other specifications that are more important for your particular application may not be included on the data sheet. For example, video designs typically require that you know a converter's differential phase and gain (**Ref 1**). Communications systems may even depend on esoteric specifications such as the spurious-free dynamic range, which isn't available on many data sheets.

For a full-scale sine-wave input, the theoretical rms-signal to rms-quantization noise ratio is

$$\text{S/N RATIO} = 6.02N + 1.76 \text{ dB},$$

where N equals the number of bits (**Ref 2**). The rms quantization-noise voltage for an ideal ADC within the Nyquist bandwidth is $q/\sqrt{12}$, where q is the weight of the LSB expressed in volts.

The most popular method for extracting a flash converter's S/N ratio and effective number of bits is through discrete Fourier transforms (DFTs). Today, you can perform sophisticated DSP tests with PC-based test systems and standard software packages. The test system in **Fig 1**, for example, can execute a 1024-point FFT in less than one second. Most of the hardware you'll need is available as plug-in boards for the PC. However, you'll have to do a fair amount of work before you can begin to use a PC-based test system. First, you'll need to design a high-speed buffer-memory board to capture the data from the flash ADC. Typically, you'll need to use high-speed static CMOS or ECL RAMs. Second, plan to design an appropriate logic interface to connect this buffer memory to the digital I/O card of the PC.

Another hardware feature you might consider is an evaluation board, which certain manufacturers of video-speed ADCs supply to ease design testing. Many evaluation boards contain reference voltages, power-supply decoupling, timing circuits, output registers, and connectors. The evaluation boards usually have a

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DSP test techniques determine your converter's deviation from ideal performance, and they even tell you certain specifications that the ADC's data sheet doesn't.

matching reconstruction DAC. In most cases, the manufacturer has optimized the design of these boards so that your ADC test won't be corrupted by faulty or poorly designed support circuits.

Your software must include a program to capture the data and then load it into the memory of the PC. If you plan to use FFT analysis, you must link a standard FFT software package to your test program. You may also have to generate a look-up table to store any special weighting functions required by your particular sampling scheme. Also, adding a coprocessor card will speed up the thousands of multiplications that FFT-based analysis requires.

If you don't have the time or the energy to build your own test system, consider one of the benchtop instruments available from a number of instrumentation manufacturers. These turnkey systems typically utilize a high-speed logic analyzer to capture data. Because menu-driven software allows you to select from a variety of tests, you incur practically no hardware or software development time.

To test a flash ADC using Fourier analysis, you must apply a spectrally pure sine wave to the converter and store a number of contiguous output data samples. Then, using DFT techniques, your test program calculates the rms-signal and rms-noise content and determines the ratio of the two. Noise calculations using DFT techniques include not only the converter's quantization noise but also the harmonics of the input sine wave. In addition, harmonics that fall outside the Nyquist bandwidth are aliased back into the Nyquist bandwidth because of the sampling process. Thus, to achieve accurate and repeatable results, the purity of the sampling clock and the input sine wave is critical.

You can use either coherent or noncoherent sampling to evaluate the ADC performance. Coherent sampling simply means that your record of samples contains an integer number of sine-wave input cycles. Alternatively, noncoherent sampling produces a record that contains noninteger multiples of the input. You must choose between these sampling schemes based on the type of input data you expect. Coherent testing is more suited to a laboratory environment when you know the precise frequency content of an input signal, and it requires careful attention in the selection of the input and sampling frequencies. Noncoherent testing yields a better representation of ADC performance in a real-world application such as spectral analysis, because the precise frequency content of the signal being digitized is a mystery.

However, whenever the number of time samples doesn't contain an integer number of input cycles (noncoherent testing), you'll have to time-weight the samples to reduce frequency side lobes. Without weighting, discontinuities will cause the main lobe's energy—the fundamental—to leak into many other frequency bins. The term "bins" refers to the spaces between spectral lines or spectral peaks. The number of bins for a particular spectrum equals the sampling fre-

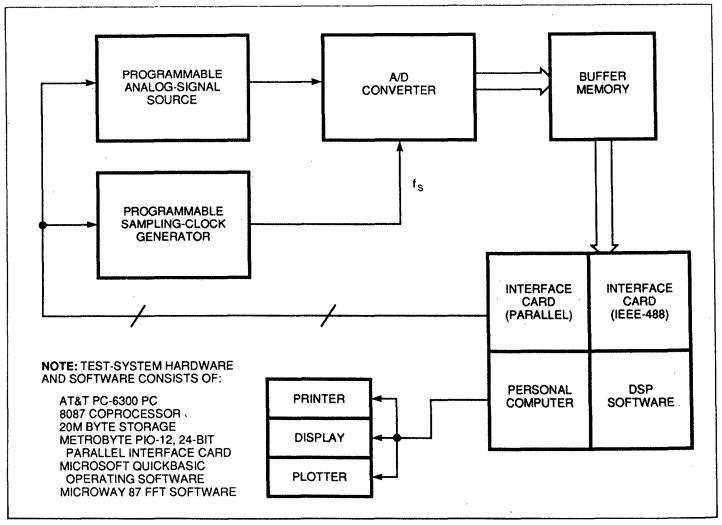

***Fig 1—This DSP test system for a flash ADC** can execute a 1024-point FFT in less than one second, but the system requires a significant design effort. Hardware requirements include a high-speed buffer memory and logic interface between this memory and your PC. Software requirements include a program to capture the data and load it into the memory of the PC, as well as a link between your test program and a standard FFT software package.*

quency divided by the record length, or f_S/M. The leakage of the signal from the central bin to side-lobe bins makes accurate spectral measurements impossible—you simply can't distinguish the frequency bins that contain actual signal information from those that contain noise. Another reason to time-weight the samples is that the end user of your A/D-conversion system may be interested in the performance of the ADC using an identical or similar window.

Noncoherent sampling involves fewer input- and sampling-frequency restrictions than coherent sampling does, but it requires careful attention in the selection and use of the weighting function. Also, to prevent masking out harmonics of the fundamental, avoid using inputs that are integer submultiples of the sampling frequency. If your input frequency is an integer submultiple of the sampling frequency, the quantization noise, $q/\sqrt{12}$, will be concentrated in the harmonics of the input frequency rather than uniformly distributed across the Nyquist bandwidth. Ultimately, this condition leads to incorrect harmonic-distortion test results.

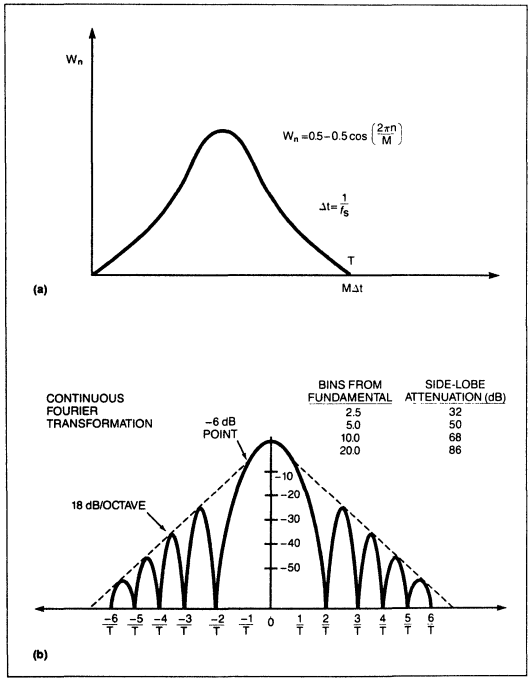

***Fig 2—When the record of samples doesn't contain an integer number of input cycles**—that is, when you're using noncoherent sampling—you must precondition the data with a weighting function. The Hanning window shown here in the time domain **(a)** and the sampled-frequency domain **(b)** is a popular weighting function.*

One popular weighting function is the Hanning window (**Ref 3**), which is described by the equation

$$W_n = 0.5 - 0.5\cos\left(\frac{2\pi n}{M}\right),$$

where W_n is the weighting coefficient for the nth data sample, and M is the total number of samples. **Fig 2** graphically depicts the Hanning window in both the time and the frequency domains.

To calculate the S/N ratio, you have to decide the number of frequency bins to include in the fundamental and the number of bins to consider as noise. As **Fig 2** shows, you can correlate the amount of side-lobe attenuation with the lobe's distance, in terms of bins, from the fundamental bin. **Fig 2b** includes a table that lists some of these values. You'll have to make your decision based on the theoretical S/N ratio of the converter you're testing.

For example, an 8-bit converter has a theoretical, maximum S/N ratio of approximately 50 dB. In order to ensure that the side-lobe energy doesn't cause an artificially high noise measurement (and hence an artificially low S/N-ratio measurement), you should include at least 10 frequency bins on either side of the fundamental when calculating the signal level. (Simply take the square root of the sum of the squares of all 21 bins as your signal level.) Now, any side-lobe energy outside this region will be at least 68 dB below the fundamental signal level (18 dB below the theoretical, 8-bit quantization noise floor of 50 dB), and side-lobe leakage won't significantly affect the accuracy of your S/N-ratio measurement.

Other weighting functions may better suit your application. For example, **Fig 3** compares the popular Hanning window's spectral representation with the more sophisticated, minimum 4-term, Blackman-Harris type. For the same record length, the Blackman-Harris window provides better spectral resolution than the Hanning window, making it more suitable for critical spectral analysis, such as measuring 2-tone, third-order intermodulation-distortion products. The extra computations for the Blackman-Harris window don't lengthen processing time, because you calculate them only once and store them in a look-up table.

As previously stated, you can use coherent sampling if you know the characteristics of your input signal and if you choose the sampling rate accordingly. Coherent

Today, you can perform sophisticated DSP tests with PC-based test systems and standard software packages.

sampling eliminates leakage and the need for windowing (**Ref 4**); the spectral result of a coherently sampled signal is simply a single-frequency peak. Certain restrictions apply to the choice of the sampling rate and the sine-wave frequency, however. First, you must observe the following ratio:

$$\frac{f_{in}}{f_S}=\frac{M_C}{M}.$$

M_C equals the number of integer cycles of the sine wave during the record period. For a whole number of cycles, M_C must be an integer. To ensure that you don't take repetitive data, M_C should also be a prime number: 1, 3, 5, 7, 11, 13, 17, etc. By using prime numbers, you ensure that all samples during the record period are unique. When using coherent sampling, it's mandatory that the ratio M_C/M be constant. This requirement implies that you derive f_S and f_{in} from two locked frequency synthesizers.

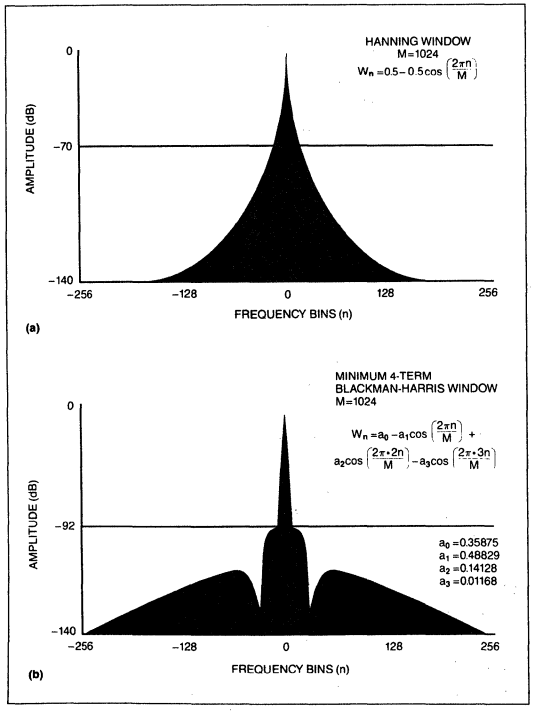

Fig 3—The Blackman-Harris windowing function (b) resolves closer peaks in a frequency spectrum than does the Hanning window (a). The mathematical expression for the Blackman-Harris window is more complex, but you only need to calculate the terms once and then store them in a look-up table.

Calculate the DFT

After selecting the record length and determining the weighting function (for noncoherent sampling), you must write your DFT test program. Your program must find the DFT of the sequence of weighted data samples for M/2 frequencies (the Nyquist frequency). Thus, the program should solve the following two equations for the kth frequency:

$$A_k=\frac{1}{M}\sum_{n=1}^{M} W_nD_n\cos\left[\frac{2\pi k(n-1)}{M}\right]$$

$$B_k=\frac{1}{M}\sum_{n=1}^{M} W_nD_n\sin\left[\frac{2\pi k(n-1)}{M}\right].$$

In these equations, A_k and B_k represent the magnitudes of the cosine and sine parts of the kth spectral line; n is the number of time samples; W_n is the weighting function; D_n is the amplitude of the time-function data point; and k is the number of a spectral line. The total magnitude of the kth spectral line is

$$\text{MAGNITUDE}_K=\sqrt{A_k^2+B_k^2}.$$

The program's results yield M/2 components, which are the frequency-domain representation of the M time samples. The resolution or spacing between the spectral lines, Δf, equals f_S/M and is the bin size or bin width.

Typically, you should select the number of time samples (M) to be between 256 and 4096, depending on the desired resolution and the size of the buffer memory. M must be equal to an integer that's a power of two. If you're using noncoherent sampling, you can compress leakage around the main lobe by using a larger record length, thereby leaving a larger percentage of the Nyquist spectrum uncontaminated. For example, the Hanning weighting leakage is ±10 bins from the fundamental for 68-dB side-lobe suppression. If the record length is 256, then the leaky fundamental occupies 20 bins out of 128 spectral components, or 16% of the digital spectrum. When M equals 1024, the percentage reduces to 20/512, or 4%.

In practice, you can use one of the many FFT algorithms to simplify and speed the DFT calculations (**Ref 5**). An FFT algorithm will produce the same results as the DFT equations above, and the computation time is much faster.

The discrete Fourier transform is the most popular method for determining a converter's true S/N ratio and effective number of bits.

Verify the FFT

Consider the noise floor when verifying the FFT. Assuming that the round-off error contributed by the DSP-noise calculation (the error caused by using a finite number of bits in the FFT multiplications and additions) is negligible, the rms-signal to rms-noise level in a single frequency bin of width Δf is

$$\text{S/N RATIO}_{FFT}=6.02N+1.76\text{ dB}+10\text{ LOG}_{10}\left(\frac{M}{2}\right).$$

This equation represents the FFT noise floor. You should choose M so that any spurious components you want to resolve lie at least 10 dB above this floor.

Basic software can easily generate an ideal N-bit sine wave by using the Integer (INT) function to truncate the value to the proper resolution. For instance, an input signal of frequency f_{in} is equal to

$$V_q=V_0\sin\left(\frac{2\pi nf_{in}}{f_S}\right),$$

where n is the nth time sample for an ADC that has infinite resolution. You can calculate the corresponding quantized value using

$$V_q(n)=\text{INT}\left(\frac{V_0\sin\dfrac{2\pi f_{in}}{f_S}}{q}\right),$$

where $q=2V_0/2^N$. Substituting this expression for q in the above equation yields

$$V_q(n)=\text{INT}\left[2^{N-1}\sin\left(\frac{2\pi nf_{in}}{f_S}\right)\right].$$

The INT function simply truncates the fractional portion of $V_q(n)$.

To check the dynamic range of the FFT, calculate the S/N ratio by using 6.02N + 1.76 dB for increasing values of N and observing the point at which the S/N ratio no longer increases by 6.02 dB/bit. The sine-wave input to the weighting function and the FFT are more ideal as N approaches infinity. By making N arbitrarily large, you can greatly reduce quantization-error effects and analyze the true noise floor of the FFT. You can also examine the characteristics of the weighting function.

Match the sine wave to a curve

Another test method to use with flash ADCs is sine-wave curve fitting. You perform this test after the ADC digitizes the sine wave and after your test system stores the data in its memory. A record length of 1024 samples is usually sufficient. The software then calculates the best-fit, ideal N-bit sine wave to match the data points, based on the sine wave's amplitude, offset, frequency, and phase required to minimize the rms error between the actual and the ideal sine wave (**Refs 6** and **7**). This method also requires that the input sine-wave frequency contains no subharmonics of the sampling rate. If you know the precise sine-wave frequency, the curve-fit algorithm is much simpler than the FFT method, and the probability that the algorithm will converge is higher.

After the software computes the rms error, Q_A, between the ideal sine wave and the actual sine wave, you can calculate the effective number of bits by using

$$\text{EFFECTIVE NUMBER OF BITS}=N-\text{LOG}_2\left(\frac{Q_A}{Q_T}\right),$$

where Q_T is the theoretical rms quantization error, $q/\sqrt{12}$. This measurement includes errors due to differential nonlinearity, integral nonlinearity, missing codes, aperture jitter, and noise, in addition to the quantization noise.

The effective number of bits that you calculate using the sine-wave curve-fitting method correlates with the value of the full-scale, FFT S/N-ratio measurement obtained using the equation

$$\text{EFFECTIVE NUMBER OF BITS}=\frac{\text{S/N RATIO}_{ACTUAL}-1.76\text{ dB}}{6.02}.$$

However, if you measure the effective bits of a sine-wave input signal whose amplitude is less than full scale, you must include the following correction factor in the above equation to achieve correlation between the two methods:

$$\text{EFFECTIVE NUMBER OF BITS}=\frac{\text{S/N RATIO}_{ACTUAL}-1.76\text{ dB}}{6.02}$$

$$+\frac{\text{LEVEL OF SIGNAL BELOW FULL SCALE (dB)}}{6.02}.$$

One useful method for reducing the effects of the D/A converter in making gross back-to-back measurements on an ADC is the beat-frequency method. **Fig 4** illustrates a basic test setup. This test method stresses the converter with a near-Nyquist signal and drives the converter at its maximum sampling rate. Thus, the analog-input sine wave should be slightly lower in frequency than half the sampling frequency. The test system updates the registers that drive the DAC at an even submultiple of the sampling rate, f_S/N,

Coherent testing is more suited to a laboratory environment; noncoherent testing more closely represents ADC performance in the real world.

where N is a power of 2. (N is not the ADC's resolution.) The resulting signal from the DAC is a low-frequency sine wave whose exact frequency equals the difference between half the sampling rate and the analog-input frequency. As **Fig 4** shows, you should clock the DAC at a much lower rate, f_S/N—known as the decimation rate—thereby reducing the effects of glitches and other dynamic errors.

You can use the beat-frequency method to make signal-to-noise measurements over the Nyquist bandwidth, $f_S/2N$. You also can examine the low-frequency beat on an oscilloscope for missing codes and other nonlinearities. To measure the harmonic content of the beat frequency, you can use a low-frequency spectrum analyzer. The harmonics of the low-frequency beat are directly related to the harmonics of the analog-input frequency. A beat frequency of a few hundred kilohertz works well. To prevent jitter on the low-frequency beat signal, you must derive both the analog-input sine wave and the sampling frequency from frequency synthesizers or crystal oscillators.

This beat-frequency test is also effective in measuring the flash converter's performance for input signals near the sampling frequency. The performance under these conditions is useful for radar in-phase and quadrature-phase systems and in IF-to-digital conversion. To perform this test, set the ADC's analog-input frequency to slightly less than the sampling rate. The circuit generates a low-frequency beat even if the DAC updates at the sampling rate. However, updating the DAC at f_S/N reduces the effects of DAC dynamic errors on the measurements.

You can use DSP techniques and FFTs to analyze **Fig 4**'s decimated data for a wide range of input frequencies. You do have to remember the rules of aliasing, however, to know where to expect the fundamental signal to show up in the FFT output spectrum. You may think your FFT is sampling your signal at a rate of f_S/N, but the converter is actually sampling at a rate of f_S.

Once you understand how to use these various techniques, you can start to probe your particular converter to measure its real performance. Part 3 will discuss how you apply these techniques to actually test an ADC in your system and determine a number of static and dynamic specifications. EDN

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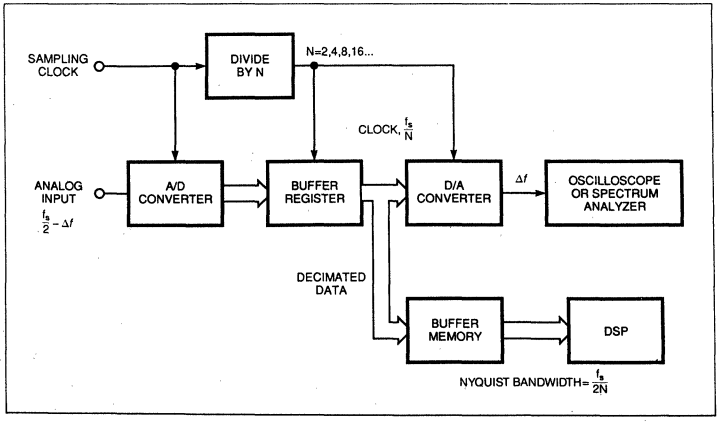

Fig 4—The beat-frequency test stresses the converter with a near-Nyquist input signal, *and it drives the converter at its maximum sampling rate. You can then examine the low-frequency beat on an oscilloscope and search for missing codes and other nonlinearities.*

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Designer's Guide to Flash-ADC Testing

Part 3
Measure Flash-ADC Performance for Trouble-Free Operation

by Walt Kester

The first two parts of this series described the subtleties of flash A/D converters and the test methods used to evaluate these devices. Part 3 concludes the series with a discussion of the actual measurements you'll need to fully characterize flash A/D converters.

Walt Kester, *Analog Devices*

Although manufacturers have expanded the number of guaranteed specifications they put on their data sheets, the test conditions often won't match those of your system design. You can use the methods described in Part 2 of this series to test a flash A/D converter, but the measurements you need to perform depend on the converter's primary application. This final part of the series provides information on important measurements you'll need to characterize your converter's performance, including total harmonic distortion (THD), differential and integral nonlinearity, and noise power ratio. You'll probably want to start with the S/N ratio, a measurement that's common to most A/D converter applications.

The S/N ratio is the ratio of the rms fundamental to the rms quantization noise. As described in Part 2, you can measure this parameter by digitizing a pure sine wave and performing Fourier transformations on the data. The rms energy contained in the fundamental sine wave is equal to the square root of the sum of the squares of the peak value and the values of the appropriate number of samples, or bins, located on either side of the peak. The converter's resolution and its side-lobe roll-off characteristics determine the number of samples you'll need. For a detailed explanation of sampling requirements, see Part 2.

The rms energy in the remaining frequency bins represents the noise due to theoretical quantization, the converter's harmonic distortion and excess noise, and the FFT round-off error. Take the square root of the sum of the squares of the remaining samples (excluding the dc components) to determine the rms energy. The overall S/N ratio of the A/D converter is

$$\text{S/N ratio} = 20 \log(\text{rms signal level/rms noise level}).$$

You can measure harmonic distortion in a similar manner. The test program (described in Part 2) examines the FFT frequency spectrum for the proper location of the desired harmonic (harmonics above $f_S/2$ will be aliased into the baseband) and determines the rms energy in that harmonic. The following equation calculates the harmonic distortion:

$$\text{Harmonic distortion} = 20 \log(\text{rms signal level/rms harmonic level}).$$

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The S/N ratio and harmonic distortion are key specifications in evaluating the performance of A/D converters.

The total harmonic distortion (THD) is the root-sum-square of the first five harmonics of the fundamental. Use this number in place of the rms harmonic level in the above formula.

Two-tone intermodulation tests using FFTs

In many applications, you don't have the simple case of a single input frequency. For example, in communication applications that multiplex several frequencies onto a single carrier, you need to measure intermodulation products. You determine this parameter by applying two sine waves of different frequencies (f_1 and f_2) to an A/D converter. You then measure the amplitudes of the third-order intermodulation products, which occur at frequencies $2f_1+f_2$, $2f_1-f_2$, $2f_2+f_1$, and $2f_2-f_1$.

Although it's possible to filter out most intermodulation distortion if the two tones are of similar frequencies, the third-order products will be very close to the fundamental frequencies and thus difficult to remove.

To avoid clipping-induced distortion, the amplitudes of the individual tones should be at least 6 dB below the full-scale range of the flash converter. In addition, the frequency separation of the two tones should be consistent with the resolution of the FFT. As discussed in Part 2, the spectral resolution of the FFT is a function of record length M, coherence vs noncoherence, and the properties of the windowing function that you choose.

In receiver applications, you often want to know the maximum ratio between the amplitude of a single-tone input signal and the amplitude of its maximum spurious component. For an ideal A/D converter, this ratio occurs for a full-scale input sinusoid. In a practical A/D converter, however, spurious content is a function of slew rate. Therefore, the maximum spurious-free dynamic range for a given input frequency will probably occur at a level somewhat below full scale. Because the spurious-free dynamic range is slew-rate dependent, it's a function of input frequency and amplitude.

Fig 1 is a plot of the typical maximum spurious level vs input signal level. Also shown is a plot of the corresponding spurious-free dynamic range. The plot demonstrates that the maximum spurious-free dynamic range of 38 dB occurs for an input signal that's about 3 dB below full scale.

The data you need to generate these plots is readily available from the family of FFTs calculated for the different input amplitudes. By knowing the input signal level that gives the highest spurious-free dynamic range at frequencies close to the Nyquist frequency, it's possible to set the gain of the system to take maximum advantage of the A/D converter's spectral characteristics.

Histograms are helpful

Differential and integral nonlinearity are also important measurements of converter performance. Try a histogram test to obtain these measurements. To make a histogram analysis, digitize a known periodic input at a rate that's asynchronous relative to the input signal. To gather the sample data for the histogram, you'll need a buffer memory and a test system, as described

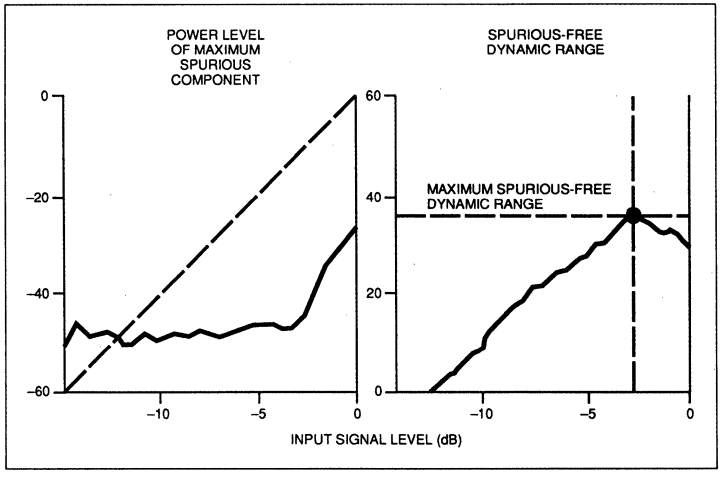

***Fig 1—These dynamic-range plots** show the power levels of spurious frequencies and the maximum spurious-free dynamic range. In this example, the maximum spurious-free dynamic range occurs at an input signal level that's 3 dB below full scale.*

in Part 2. The buffer memory will probably be too small to hold a statistically significant number of samples from a single run (several hundred thousand are usually required). For this reason, run several tests to acquire the data and load the contents of the buffer into the main memory of your test system after each run. Benchtop test systems from Hewlett Packard and Tektronix also provide histogram test capability.

After the test system accumulates a statistically significant number of samples, it can determine the relative number of occurrences of each digital code (the code density). This test routine then normalizes the data based upon the input signal and analyzes the results for linearity errors.

For an ideal A/D converter with a full-scale triangular-wave input, you'd expect an equal number of codes in each bin. The number of counts in the nth bin, H(n), divided by the total number of samples taken, M, is the bin width as a fraction of full scale. The ratio of the actual bin width to the ideal bin width, P(n), is the differential linearity. Ideally, this ratio should be unity. Subtracting 1 LSB gives you the differential nonlinearity.

You can determine integral nonlinearity with a cumulative histogram; the cumulative bin widths are the transition levels. However, the cumulative effects of errors can make the integral-nonlinearity measurement inaccurate. Histograms are used more often in evaluating differential nonlinearity.

High-speed, high-accuracy triangular waves are difficult to generate, so use a sine wave. All codes aren't equally probable with a sine-wave input, however, and you should normalize the histogram data using the probability density function for a sine wave, as shown in **Fig 2.**

To obtain accurate results, you need to take a large number of samples. For example, to determine the differential nonlinearity for an 8-bit flash converter to within 0.1 bit with 99-percent confidence, you'll need 268,000 samples. You can use hardware to count these samples, thus speeding up the software processing time. For high-speed sampling, decimate the output data to clock rates that are compatible with a slower-speed memory.

Using noise-power-ratio tests

You can use noise-power-ratio (NPR) tests to measure the transmission characteristics of frequency-division-multiplexed (FDM) communications links. In a typical FDM system, 4-kHz-wide voice channels are "stacked" in frequency for transmission over coaxial, microwave, or satellite equipment. At the receiving end, the FDM equipment demultiplexes the data and returns it to individual, 4-kHz baseband channels. In an FDM system that has 100 channels or more, Gaussian noise with the appropriate bandwidth approximates the FDM signal.

The test setup of **Fig 3** measures an individual 4-kHz channel for quietness by using a narrow-band notch (bandstop) filter and a tuned receiver (**Ref 4**), both of which measure the noise power inside this 4-kHz notch. The NPR measurements are straightforward. With the

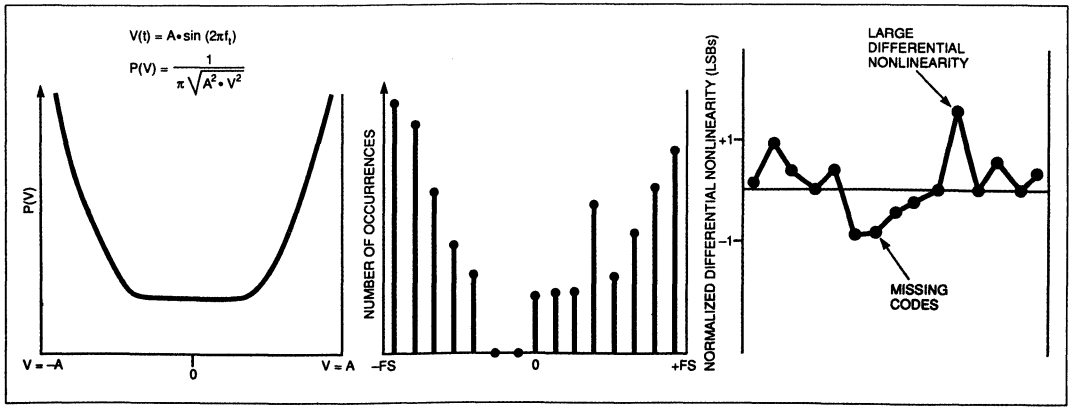

Fig 2—Histograms are often used to plot differential nonlinearity. *Shown here is a curve for the probability density function of a sine wave, which is used to normalize histogram data to produce a plot of differential nonlinearity.*

Where multiple frequencies exist on a single carrier, you need to measure intermodulation distortion as well as harmonic distortion.

notch filter out, the receiver determines the rms noise power of the signal inside the notch. The notch filter is then switched in, and the receiver determines the residual noise inside the 4-kHz slot. The ratio of the two readings, expressed in dB, is the NPR. You should test several slot frequencies across the noise bandwidth—low, midband, and high.

The NPR is usually plotted on an NPR curve as a function of rms noise level referred to the peak range of the system. For very low noise levels, the undesired noise is primarily thermal noise and is independent of the input noise level. Over this region of the curve, a 1-dB increase in the noise level causes a 1-dB increase in the NPR. As the noise level increases, the amplifiers in the system begin to overload, creating intermodulation products that cause the noise floor of the system to rise. As the input noise increases further, the effects of overload noise predominate, reducing the NPR dramatically. FDM systems are usually operated at a noise-loading level a few decibels below the point of maximum NPR.

In a digital system containing an A/D converter, the noise within the slot is primarily quantizing noise when low values of noise input signals are applied. The NPR curve is linear in this region. As the noise input level increases, the hard-limiting action of the converter causes clipping noise to dominate.

In a practical A/D converter, any dc or ac nonlinearities cause a departure from the theoretical NPR. Although the peak value of NPR occurs at a fairly low input noise level (rms noise = 1/4 V_O, where $\pm V_O$ is the range of the A/D converter), the broadband nature of the noise signal stresses the device, and the test provides a good indication of its dynamic performance.

Theoretically, NPR readings should be independent of any particular slot frequency. However, because of increased nonlinearities for the higher input frequencies, the NPR readings in the higher slots tend to be lower.

NPR testing using DSP techniques

Using FFT analysis techniques, you'll find NPR measurements a real challenge. Consider the case where the record length is 1024 and the sampling rate is 20 MHz. The FFT of 1024 contiguous time samples would place a spectral component every 19.53 kHz (20 MHz/1024). Because the notch-filter slot width is approximately 4 kHz, the probability of a spectral component falling within the notch is very low.

To achieve reasonable data stability in the FFT NPR analysis, a number of samples must fall within the notch. If ten samples are within the 4-kHz notch, then the resolution of the FFT would need to be 400 Hz, necessitating a record length of 50,000 for a sampling

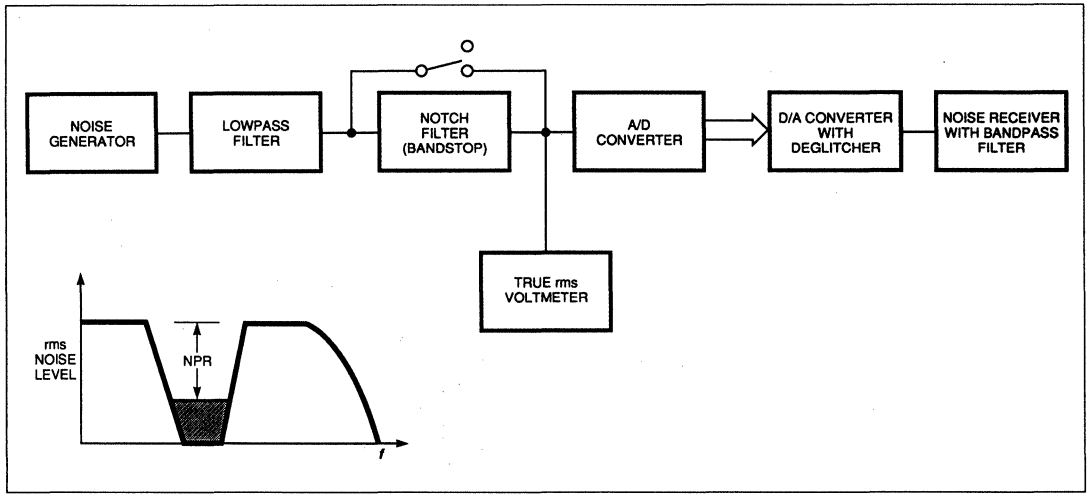

Fig 3—You can use this test setup to measure noise power ratio (NPR). *With the notch filter out, the receiver determines the noise power of the signal inside the notch. With the notch filter switched in, the receiver measures the residual noise inside the typical 4-kHz slot. The ratio of the two readings (in decibels) is the NPR.*

rate of 20 MHz. To avoid an extremely large buffer memory (and hence more demands on the FFT processor), you need to make the notch filter wider. For 20-MHz sampling and a 1024-word buffer memory, a notch filter that has a width of 200 kHz will provide ten frequency bins inside the notch. Even under these conditions, however, you should average the NPR calculations for several records to provide reasonable data stability.

Transient-response testing

The response of a flash converter to a transient input such as a square wave is often critical in radar applications. The major difficulty in implementing this test is obtaining a flat pulse that's commensurate with the converter's resolution.

A test setup for measuring the transient response of an A/D converter is shown in **Fig 4**. If you mount the Schottky-diode flat-pulse generator as close as possible to the analog input of the A/D converter, you can apply a signal to the A/D converter that's flat to at least 10-bit accuracy a few nanoseconds after it reverse biases the Schottky diodes.

You can use the same test setup to measure overvoltage recovery time. The amount of overvoltage is generally specified as a percentage of the A/D converter's range. For a converter with a 2V input range, 50% overvoltage corresponds to 1V above or below the nominal 2V input range. You make the starting point of the flat pulse correspond to the desired overvoltage condition. The actual recovery time is referenced to the time the input signal re-enters the A/D-converter input range. As in the transient-response test, you must consider the sampling (aperture) time delay when making this measurement.

The aperture-time and -jitter specifications of video A/D converters have probably been the least understood and most misused specifications in the entire field. The original concept of aperture time is centered around the classic S/H circuit of **Fig 5**. In an ideal S/H circuit, the switch has zero resistance when closed and opens instantly on receipt of an encode command. In practice, the sampling switch changes from a low to a high resistance over a certain finite time interval. An error occurs because the circuit tends to average the input signal over the finite time interval required to open the switch. As a result, the sampled voltage varies from the voltage at the instant the switch starts to open. The time required to open the switch is the aperture time. The error is determined by $E_a = t_a\ dV/dt$, where E_a is the aperture error, t_a is the aperture time, and dV/dt is the rate at which the input signal changes.

A simple first-order analysis, which neglects nonlinear effects, shows that no real error exists for such a switch. As long as the switch opens in a repeatable fashion, there is an effective sampling time that will cause an ideal S/H amplifier to produce the same hold voltage. The difference between this effective sampling point and the leading edge of the sampling clock is a fixed delay, which doesn't constitute an error. This effective aperture delay is the period from the leading edge of the sampling clock to the instant when the input signal equals the hold value. This specification

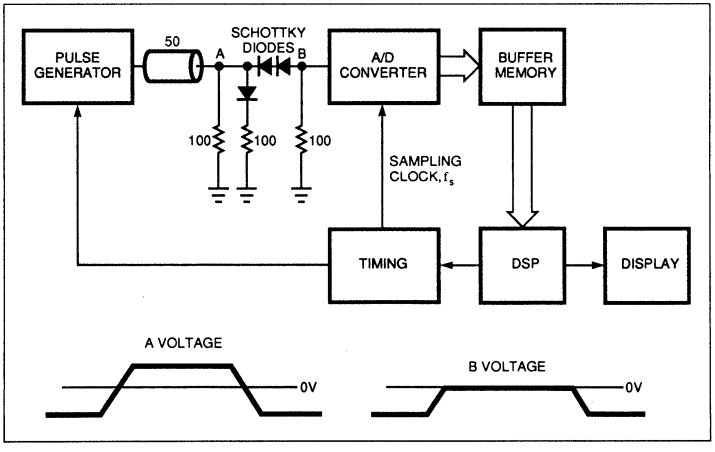

Fig 4—This test setup measures the transient response of an A/D converter. *The Schottky-diode network, located between points A and B in the circuit, generates a flat pulse for the input of the converter.*

In a practical A/D converter, the spurious-free dynamic range is a function of the converter's slew rate and can occur at a level below full scale.

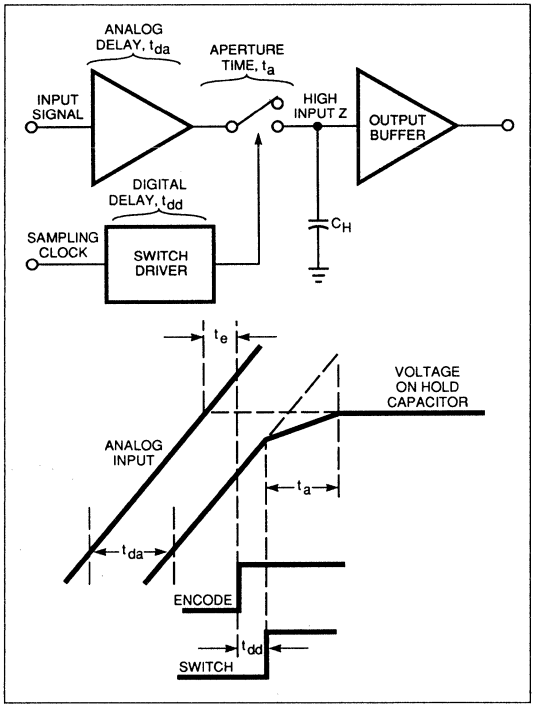

Fig 5—The concept of aperture time centers around the S/H circuit. *In practice, the sampling switch generates an error because of input-signal averaging over the finite time interval needed to open the switch. The aperture time is the time needed to open the switch.*

is important because it helps you determine when to apply the sampling clock with respect to the input signal timing.

The variation in effective aperture delay is important in simultaneous S/H applications. For example, in both I (in-phase) and Q (quadrature) radar receivers you may have to provide adjustable delays in the sampling clock to match the effective aperture delay times of several A/D converters. You should also consider delay-time tracking over a range of temperatures, especially in military systems where the specified operating temperature ranges from −55 to +125°C.

True aperture errors, however, do result from variable time delays. In a practical A/D converter, the sampling clock is often phase-modulated by some unwanted source; the source can be wideband random noise, power-line frequency, or digital noise due to poor grounding techniques. Phase jitter on the input sine wave can produce the same effect as jitter on the sampling clock. The resulting error is called aperture jitter. The corresponding rms voltage error caused by the rms aperture jitter qualifies as a valid aperture error.

The aperture-jitter specification is sometimes interpreted as a measure of the converter's ability to accurately digitize rapidly changing input signals. An A/D converter with an impressive aperture-jitter specification still may lose effective bits when digitizing a sine wave that has a maximum slew rate calculated from the aperture formula $E_a = t_a\, dV/dt$.

For example, assume that a 20-MHz, 8-bit flash converter has a bipolar input range of $\pm V_0$ ($2V_0$ p-p) and an aperture jitter specification of 20 psec rms. To calculate the maximum aperture-jitter error, convert the rms aperture jitter into a maximum value. If you consider that aperture jitter follows a Gaussian distribution similar to white noise, the rms aperture jitter, t_a, corresponds to the sigma (σ) of the distribution. The 2σ point on the distribution is a good place to set the maximum value, and the maximum aperture jitter becomes is $2t_a$.

If the corresponding maximum voltage error (ΔV) at the zero crossing of a full-scale sine wave is set to ½ LSB (½ LSB $= 2V_0/2^{N+1}$, where N equals the resolution of the A/D converter), then you can calculate the maximum full-scale sine-wave frequency, f_{max}, which will produce the ½ LSB aperture error, by using the following equations:

$$V(t) = V_0 \cdot \sin(2\pi f_t),$$

$$\frac{dV}{dt} = 2\pi f V_0 \cdot \cos(2\pi f_t),$$

$$\left.\frac{dV}{dt}\right|_{max} = \frac{\Delta V}{2t_a} = \left|2\pi V_0 f_{max}\right|, \text{ and}$$

$$f_{max} = \frac{\Delta V}{4\pi V_0 t_a} = 2\pi t_a \cdot 2^{N+1}.$$

For $t_a = 20$ psec rms and $N = 8$, f_{max} is 16 MHz. These calculations imply that a 20-MHz flash converter can accurately digitize a full-scale sine wave of 16 MHz. In actual practice, however, the device may begin to suffer from skipped codes, decreased effective bits and S/N ratio, and ac nonlinearities at much lower frequencies.

You can calculate the effects of aperture jitter on

Histograms are useful in evaluating the differential nonlinearity of an A/D converter.

the full-scale sine-wave S/N ratio as follows:

$$V(t) = V_0 \cdot \sin(2\pi f_t),$$

$$\frac{dV}{dt} = 2\pi f V_0 \cdot \cos(2\pi f_t), \text{ and}$$

$$\frac{dV}{dt}_{rms} = \frac{2\pi f V_0}{\sqrt{2}}.$$

For an rms error voltage, ΔV_{rms}, and an rms aperture jitter of t_a,

$$\frac{\Delta V_{rms}}{t_a} = \frac{2\pi f V_0}{\sqrt{2}}, \text{ and}$$

$$\Delta V_{rms} = \frac{2\pi f V_0 t_a}{\sqrt{2}}.$$

The rms-signal to rms-noise ratio, expressed in decibels, is

$$\text{S/N ratio} = 20 \log \left[\frac{V_0/\sqrt{2}}{\Delta V_{rms}}\right]$$

$$= 20 \log \left[\frac{1}{2\pi f t_a}\right] \text{dB}.$$

The S/N ratio that's due exclusively to aperture jitter in the above equation is plotted in **Fig 6** as a function of the full-scale input-sine-wave frequency for various values of aperture jitter.

Consider an 8-bit, 20-MHz A/D converter with an rms aperture jitter of 20 psec. For an 8-MHz full-scale input, the S/N ratio due only to aperture jitter is 60 dB, as calculated from the equation. The theoretical S/N ratio due to quantizing noise in an 8-bit flash converter is 50 dB. When you combine the S/N ratio of 60 dB with the S/N ratio of 50 dB, you obtain a theoretical S/N ratio of 49.6 dB, which encompasses both the ideal quantizing noise and the noise due to aperture jitter. A practical 8-bit device that has an rms aperture-jitter specification of 20 psec may, however, only achieve an S/N ratio of 40 dB under these conditions.

Therefore, to accurately evaluate the A/D converter's dynamic performance, you must carefully examine the S/N ratio, effective number of bits, and aperture-jitter specifications.

Try measuring the aperture jitter of an A/D converter using the test setup shown in **Fig 7**. The low-

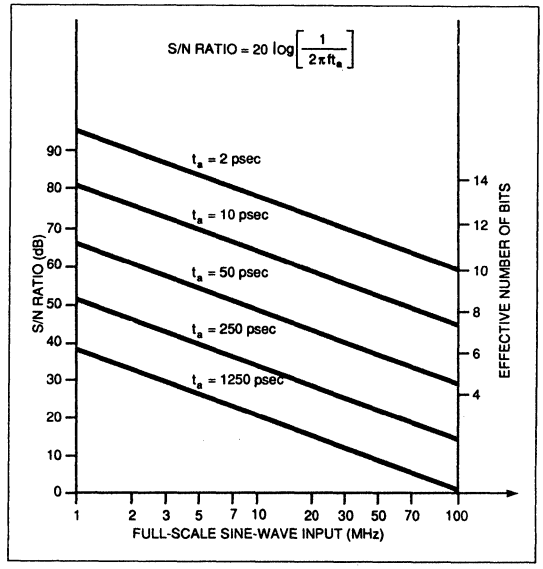

Fig 6—This plot compares the S/N ratio to the full-scale sine-wave input frequency for various values of aperture jitter.

jitter pulse generator produces both the sampling clock and the analog input signal to minimize the phase jitter between them. Adjust the phase shifter until the A/D converter repetitively samples the sine wave at its point of maximum slew rate at midscale. Then take a histogram on the digitized A/D-converter output data.

An ideal A/D converter with no aperture jitter would have only one code present on the histogram. A practical converter gives a distribution of codes that you can fit to the normal distribution. The sigma (Σ) of the distribution corresponds to the rms error voltage, ΔV_{rms}, produced by the rms aperture jitter. Calculate the aperture jitter, t_a, from the formula

$$t_a = \frac{\Delta V_{rms}}{\frac{dV}{dt}}$$

where dV/dt is the rate-of-change of the sine wave at zero crossing.

If you sufficiently attenuate the input sine wave, any spreading of the distribution around the nominal code is due to intrinsic A/D-converter noise. As the input sine wave increases in amplitude, the slew rate, dV/dt, becomes proportionally greater, and the distri-

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Noise-power-ratio tests are useful in determining the transmission characteristics of frequency-division-multiplexed communications links.

bution begins to spread because of the aperture jitter. Because high slew rates can affect the ac differential linearity of the converter, you should exercise caution when interpreting the histogram for high slew-rate inputs.

The offset adjustment shown in **Fig 7** lets you position the sine wave at different points on the A/D-converter range. In this way, you can see variations attributed to range-dependent differential-linearity characteristics. When offsetting the sine wave, make sure you don't exceed the A/D converter's input range.

It's also possible to measure effective aperture delay by using the locked-sine-wave technique. Adjust the phase shifter until the output reads midscale. Use a dual-trace scope to determine the difference between the leading edge of the sampling-clock pulse and the actual zero crossing of the sine-wave input. This difference is the effective aperture delay, which can be either negative or positive, depending on the values of the internal analog and digital delays in the S/H portion of the A/D converter.

At present, no industry standard exists for either the definition or the test for A/D-converter error rates. In flash converters, comparator metastable states can occur for low- or high-frequency input signals. At high frequencies, bubbles in the thermometer code of the comparator-bank output can also produce erroneous output codes.

Because error rates less than 1×10^{-16} are typical for well-behaved A/D converters, you need to take a large number of samples to properly measure the error rate. You must also take great care in the test-set layout, grounding, shielding, and power-supply decoupling so that 60-Hz, EMI, or RFI glitches don't create erroneous errors.

Use the circuit in **Fig 8** to measure the error rate for low-frequency input signals. Apply a low-frequency, full-scale sine wave (or triangle wave) to the A/D converter so that its rate of change is less than 1 LSB/sample. This step ensures that the transition zones between codes are all adequately exercised. An error amplitude of X LSBs is established as the lower limit for the definition of a qualified error. Usually, you select X to be several LSBs so that random noise doesn't produce errors. The software or hardware then examines the difference between each adjacent sample and records the number of times this difference exceeds the error threshold, X. If NQ is the number of qualified errors that occur, and NT is the total number of samples taken, then the error rate, ER, is given by the equation $ER = NQ/2{\cdot}NT$.

As an example, consider an 8-bit, 100M-sample/sec flash converter designed to take at least ten samples at each code level. For one slope of the triangle-wave input, the number of samples required is $10\times256=2560$ samples. The frequency of the triangle wave is

$$f_t = \frac{1}{2560 \cdot 2 \cdot 10\ \text{nsec}} = 19.5\ \text{kHz}.$$

At a 100-MHz sampling rate, the average time required to make an error for an error rate of 1×10^{-9} is 10 seconds.

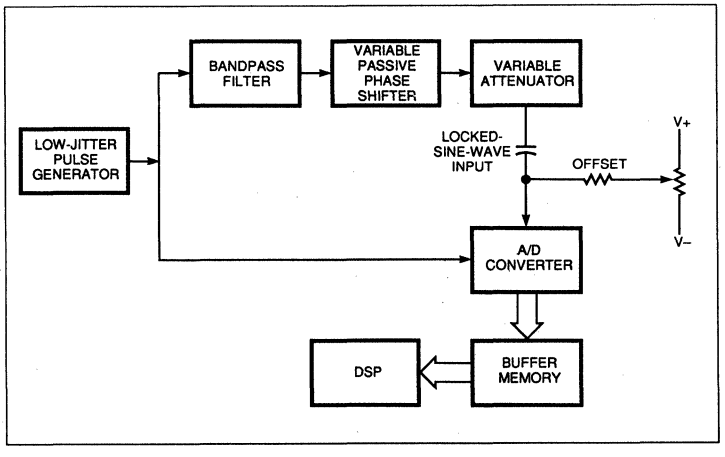

Fig 7—In this test setup for measuring aperture jitter, *you adjust the phase shifter until the A/D converter repetitively samples the sine wave at its point of maximum slew rate. You then take a histogram of the digitized A/D-converter output data. The offset adjustment lets you position the sine wave at different points on the converter's range.*

Aperture time and aperture jitter for A/D converters are probably the most misunderstood and misused specifications.

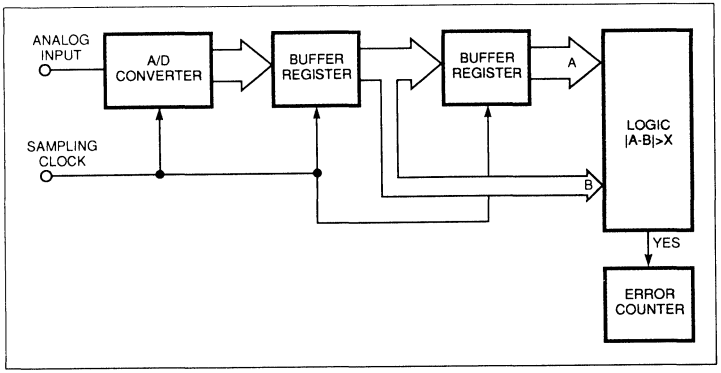

Fig 8—The effective aperture delay *is the time difference between the leading edge of the sampling-clock pulse and the actual zero crossing of the sine-wave input.*

In a similar manner, you can measure dynamic errors caused by fast input signals by using the beat-frequency approach. You choose the low-frequency beat frequency to give the proper number of samples per code level, and then you examine the decimated digital outputs for adjacent sample differences that exceed the allowable error amplitude.

In summary, determining appropriate error-rate criteria for an A/D converter depends upon both the application and the characteristics of the converter under consideration. Flash converters that use straight binary decoding with no additional correction logic are most subject to large metastable errors at midscale. For this situation, a low-amplitude dither signal centered on the midscale code transition might be an appropriate stimulus. In a more well-behaved flash converter, a full-scale signal that exercises all codes might be desirable.

If you plan to digitize composite video signals, you'll need to measure the differential-gain and -phase performance of the flash A/D converter. Differential gain is the percentage difference between the digitized amplitudes of two signals. Likewise, differential phase is the phase difference between the digitized values of the same two input signals. The input signals are typically a high-frequency low-level sine wave representing the color subcarrier frequency, superimposed on a low-frequency sine wave. Distortion-free processing of the color signal requires that the flash converter alters neither the amplitude nor the phase of the chrominance signal as a function of the luminance-signal level.

The best method for performing composite video tests is to use an A/D converter back-to-back with a D/A converter. Connect a TV test signal to the A/D converter and use the output of the D/A converter to drive a vectorscope. To ensure that the test accurately measures the A/D converter's performance, use a low-glitch D/A converter followed by a track-and-hold deglitcher. In addition, the dc accuracy of the D/A converter should exceed that of the A/D converter. When testing an 8-bit flash converter, use a D/A converter with at least 10 bits of accuracy. EDN

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Video VCAs and Keyers Using the AD834 and AD811

by Eberhard Brunner, Bob Clarke, and Barrie Gilbert

INTRODUCTION

Voltage-controlled amplifiers (VCAs) built from analog multipliers take one of two forms. In the first, the multiplier acts as a voltage-controlled attenuator ahead of a fixed-gain amplifier. This type of VCA is used in applications where only a moderate maximum gain, but a fairly high maximum loss, are needed. In the second, the variable attenuation is placed in the feedback path around an op amp, which, in fact, implements an analog divider, more suitable for applications requiring high gains.

This application note describes practical circuits in which the wide bandwidth of the Analog Devices AD834 Four-Quadrant Multiplier and the AD811 Current-Feedback Op Amp are exploited to provide a video-quality VCA with a maximum gain of 12 dB (×4) or 20 dB (×10), based on the first of the above methods. A slightly modified form of this VCA, using two multipliers whose outputs are summed, provides the first of two video keyer designs; a second design uses global negative feedback around the multipliers to achieve improved accuracy and some simplification.

A VIDEO-QUALITY VCA

The VCA is shown in Figure 1. The AD834 multiplies the signal input by the control voltage. Its outputs are in the form of differential currents from a pair of open collectors, ensuring that the full bandwidth of the multiplier (which exceeds 500 MHz) is available for certain applications. In this case, more moderate bandwidth is obtained using current-to-voltage conversion, provided by the AD811 op amp, to realize a practical amplifier with a single-sided ground-referenced output. Using feedback resistors R8 and R9 of 511 Ω the overall gain ranges from −70 dB for V_G ~0 to +12 dB (a numerical gain of four) when V_G = +1 V.

The −3 dB bandwidth is 90 MHz (Figure 2) and is essentially independent of gain. The response can be maintained flat to within ±0.1 dB from dc to 40 MHz at full gain (Figure 3) with the addition of an optional capacitor of about 0.3 pF across the feedback resistor R8. The circuit produces a full-scale output of ±4 V for a ±1 V input, and can drive a reverse-terminated load of 50 Ω or 75 Ω to ±2 V. Figure 4 shows the typical pulse response.

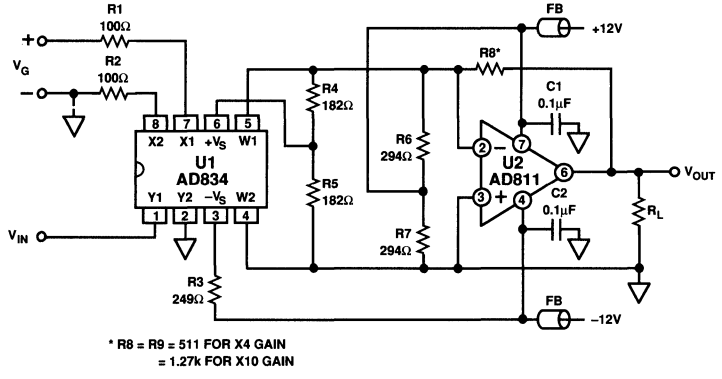


Figure 1. Complete VCA Provides Up to 20 dB of Gain (G = BW = 25 MHz) and a Bandwidth of Over 90 MHz (G = 12 dB)

The gain can be increased to 20 dB (×10) by raising R8 and R9 to 1.27 kΩ, with a reduction of the −3 dB bandwidth to about 25 MHz (also shown in Figure 2) and a maximum output voltage of ±9 V using the ±12 V supplies. It is not necessary to alter R6 and R7 for the high gain version of the amplifier, although an optimized design would raise these slightly to restore the common-mode voltage at the input of the AD811 to +5 V.

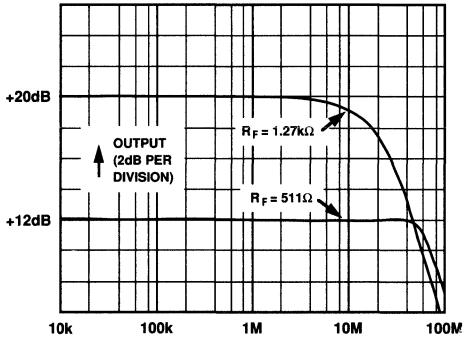


Figure 2. Small-Signal Response of the VCA Shows a −3 dB Bandwidth of 90 MHz for the 12 dB Version and 25 MHz for the 20 dB Version

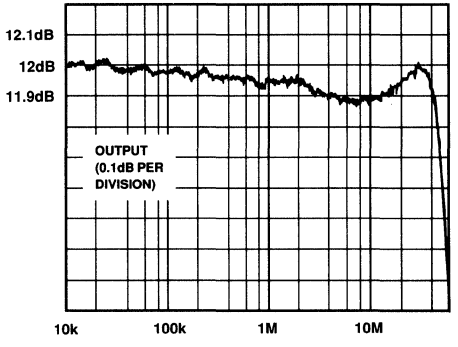


Figure 3. AC Response Can Be Held Flat to Within ±0.1 dB from DC to 40 MHz by Addition of a 0.1 pF Capacitor Across R8

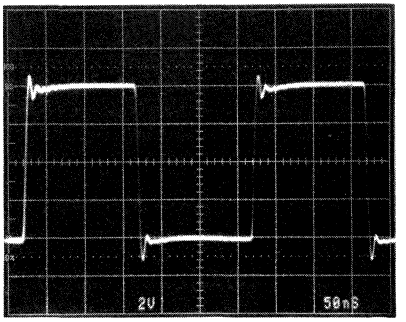


Figure 4. Full-Output Pulse Response for the 12 dB Amplifier

The gain-control input may be a positive or negative ground-referenced voltage, or fully differential, depending on the user's choice of connections at Pins 7 and 8. As shown, a positive value of V_G results in an overall noninverting response. Reversing the sign of V_G simply causes the sign of the overall response to invert. In fact, although we have called this a voltage-controlled amplifier, it can just as well be used as a general-purpose four-quadrant multiplier with good load-driving capabilities and fully symmetrical responses from X- and Y-inputs.

We have used the Y-input of the multiplier for the signal, since this port is slightly more linear than the X-input, and have shown X2 and Y2 grounded. These inputs each draw about 45 μA of bias current, so the grounded (unused) inputs should be terminated preferably in the same resistance as the source, in each case, to minimize offset voltages. The resistance of the signal source may in some cases be essentially zero (as in the case of a transformer-coupled input, or certain signal generators); note that a doubly terminated cable line of impedance Z_O will present a dc resistance of $Z_O/2$ at the input. Resistors R1 and R2 have been included in Figure 1 to minimize the likelihood of small aberrations arising in the signal path in those cases where V_G is derived from a source having poor HF characteristics; they may be omitted in the four-quadrant multiplier application.

High-frequency circuits such as those described herein are sensitive to component layout, stray capacitance, and lead lengths. Use a ground plane and make short, direct connections to ground. Bypass the power-supply connections—inductance in the power-supply leads can form resonant circuits that produce response peaking or even sustained oscillations.

Circuit Analysis

To understand the operation of the VCA, we need first to consider the scaling properties of the AD834, which is actually an accurate nonlinear (two-input) voltage-controlled current source. Figure 5 shows a simplified schematic of the whole VCA.

The exact transfer function for the AD834 would show that the differential voltage inputs at X1, X2 and Y1, Y2 are first multiplied together, divided by the scaling voltage of 1 V (determined by the on-chip bandgap reference) and the resulting voltage is then divided by an accurate 250 Ω resistor to generate the output current. A simplified form of this transfer function is

$$I_W = (X_1 - X_2)(Y_1 - Y_2) \times 4mA \quad (1)$$

where I_W is the differential current output from W1 to W2 and it is understood that the inputs X_1, X_2, Y_1, and Y_2 are expressed in volts. Thus, when both differential inputs are 1 V, I_W is 4 mA; this current is laser-calibrated to close tolerance, which simplifies the use of the AD834 in many applications. Note carefully the direction of this current in determining the correct polarity of the output connections.

It is easy to show that the output of the AD811 is

$$V_{OUT} = 2 \times I_W \times R_F \quad (2)$$

where R_F is the feedback resistor. For R_F = 500 Ω (499 Ω is the nearest standard resistor value), the overall transfer function of the VCA becomes

$$V_{OUT} = 4(X_1 - X_2)(Y_1 - Y_2) \quad (3)$$

which reduces to $V_{OUT} = 4\,V_G\,V_{IN}$ using the labeling conventions shown in Figure 1. As noted, the phase of the output reverses when V_G is negative. A slightly higher value of R_F is used to compensate for the finite gain of the AD811.

Both the AD811 and the AD834 can operate individually from power-supply voltages of ±5 V. However, to ensure proper operation of the AD811's input stage, the common-mode voltage at W1 and W2 must be within the common-mode range of these inputs. There are several ways to do this. We can use separate supplies of ±5 V for the AD834 and ≥ ±9 V for the AD811. Here, we have chosen to show how the VCA can be biased from one dual supply of nominally ±12 V. Figure 5 also helps to understand the dc biasing design.

We begin by deciding to place the AD834's outputs at about +5 V (a little higher than they operate in the other published applications of this product). Under dc conditions, the high open-loop gain of the op amp forces W1 and W2 to assume the same potential. We calculate the values of R_A to introduce the required 7 V drop, by considering the components of the total current in each of these resistors for the zero-signal condition.

First, when V_{OUT} = 0, the current in resistors R_F must be 10 mA (5 V/ 500 Ω). Second, the standing current into W1 and W2, due to the AD834's internal biasing, is 8.5 mA per side. Third, in this application we provide the positive supply voltage for the AD834 (at Pin 6) via resistors R_B which each carry one-half of the total supply current of 11 mA. Thus, the total current in resistors R_A is 24 mA (10 + 8.5 + 5.5 mA) and a value of 294 Ω is chosen (the closest standard value to 7 V/24 mA) for these resistors. Finally, we choose R_B to set the voltage at Pin 6 to +4 V, which is high enough to ensure accurate operation of the AD834 over the full signal and temperature ranges; the nearest standard resistor value is 182 Ω (1 V/ 5.5 mA).

The presence of these resistors (whose parallel sum is 112 Ω on each side) at the input of the op amp causes it to operate at a "noise gain" of 4.45 (499 Ω/112 Ω), but this neither has any significant effect on the dc scaling of the system, nor does it lower the closed-loop bandwidth (as would be the case for a conventional voltage-feedback op amp).

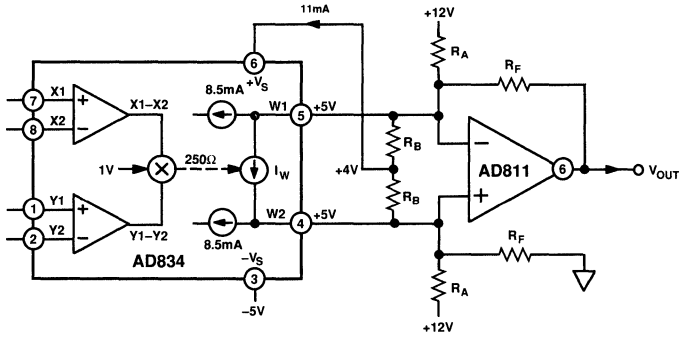


Figure 5. Simplified Schematic of the VCA for Analysis Purposes

A VIDEO KEYER BASED ON THE VCA

Using two AD834s and adding a 1 V dc source, a special form of a two-input VCA called a video keyer (Figure 6) can be assembled. Keying is the term used in reference to blending two or more video sources under the control of a further signal or signals to create such special effects as dissolves and overlays. The circuit described here is a two-input keyer, with video inputs V_A and V_B, and a control input V_G. The output at the load is given by

$$V_{OUT} = GV_A + (1 - G)V_B \quad (4)$$

where G is a dimensionless variable (actually, just the gain of the "A" signal path) that ranges from 0 when $V_G = 0$, to 1 when $V_G = +1$ V. Thus, V_{OUT} varies continuously between V_A and V_B as G varies from 0 to 1.

The operation is straightforward. Consider first the signal path through U1, which handles video input V_A. Its gain is clearly zero when $V_G = 0$ and the scaling we have chosen ensures that it is unity when $V_G = +1$ V; this takes care of the first term in Equation 4. On the other hand, the V_G input to U2 is taken to the *inverting* input X2 while X1 is biased at an accurate +1 V. Thus, when $V_G = 0$, the response to video input V_B is already at its full-scale value of unity, whereas when $V_G = +1$ V, the differential input $X_1 - X_2$ is zero. This generates the second term in Equation 4.

To generate the 1 V dc needed for the "1–G" term, an AD589 reference supplies 1.225 V ±25 mV to a voltage divider consisting of resistors R2 through R4. Potentiometer R3 should be adjusted to provide exactly +1 V at the X1 input.

In this case, we have shown an alternative arrangement using dual supplies of ±5 V for the AD834 and ±12 V for the AD811. Also, the overall gain in this case is arranged to be unity *at the load*, when it is driven from a reverse-terminated 75 Ω line. This means that the "dual VCA" has to operate at a maximum gain of ×2, rather than ×4 as in Figure 1. However, this cannot be achieved by lowering the feedback resistor, since below a critical value (not much less that 500 Ω) the AD811 will become unstable. This is because the dominant pole in the closed-loop ac response of a current-feedback amplifier is controlled by this feedback resistor. It would be possible to operate at a gain of ×4 and then attenuate the signal at the output. Instead, we have chosen to attenuate the signals by 6 dB at the input to the AD811; this is the function of R8 through R11.

The −3dB bandwidth is about 85 MHz and the gain is flat within ±0.1 dB to 30 MHz (Figure 7). Output noise and signal isolation with either channel fully off and the other fully on is about −60 dB to 20 MHz. The feedthrough at 100 MHz is limited primarily by board layout.

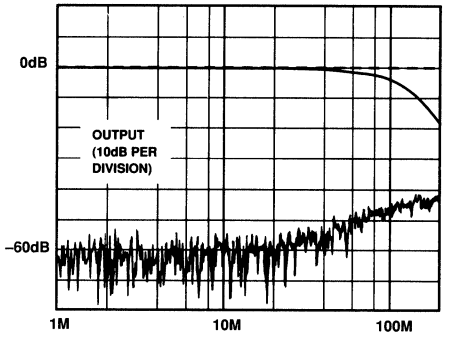


Figure 7. AC Response of the Video Keyer, at V_G = Zero and +1 V; Feedthrough Is About −60 dB

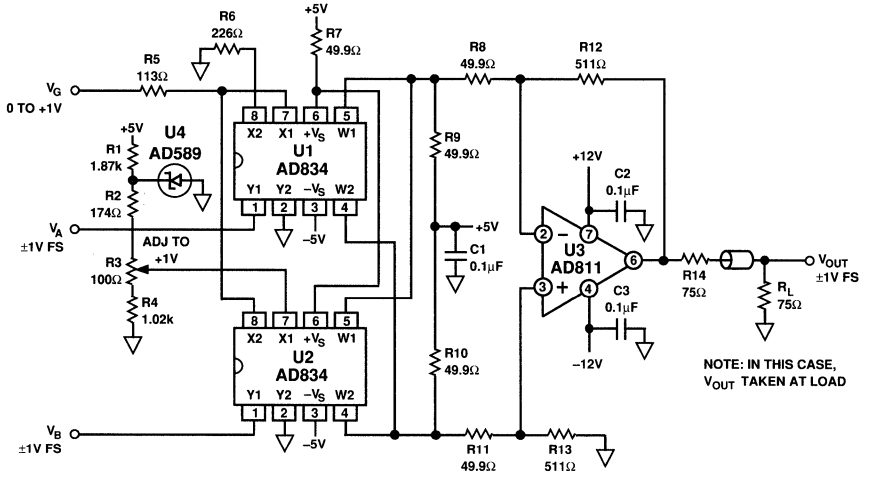


Figure 6. A Two-Input Video Keyer Based on the VCA

A FEEDBACK KEYER

The gain accuracy of the "VCA-based" keyer is dependent on the feedback resistor, R_F. Also, any nonlinearity in the multipliers will show up as a differential gain error. Using an alternative technique, in which the feedback is routed back to unused signal inputs on the AD834s, we can eliminate the feedback resistor and achieve higher accuracy. In the design shown here, we have also used a level-shifting network between the AD834 and the AD811 that eliminates the need for separate power supplies for the two ICs. (In fact, this technique can also be used in the VCAs.)

The basic idea is shown in Figure 8. Note first that V_{OUT} is returned to the inverting inputs Y2 of the multipliers and that their outputs are added. The sum is forced to zero by the assumed high open-loop gain of the op amp. Multiplier M1 produces an output $G(V_A–V_{OUT})$, while M2 produces an output $(1–G)(V_B–V_{OUT})$, where G is $V_G/(1\ V)$ and ranges from 0 to 1. Therefore, the complete system is described by the limiting condition

$$G(V_A–V_{OUT}) + (1–G)(V_B–V_{OUT}) \rightarrow 0 \qquad (5)$$

which requires that

$$V_{OUT} = GV_A + (1–G)V_B \qquad (6)$$

exactly as required for a two-input keyer. The summation of the differential current-mode outputs of the two AD834s is simply achieved by connecting together their respective W1 and W2 nodes. The resulting signal—essentially the loop error represented by the left-hand side of Equation 5—is forced to zero by the high gain of an AD811 op amp.

Figure 9 provides a practical embodiment of these ideas. The gain-control details to provide G and (1–G) terms

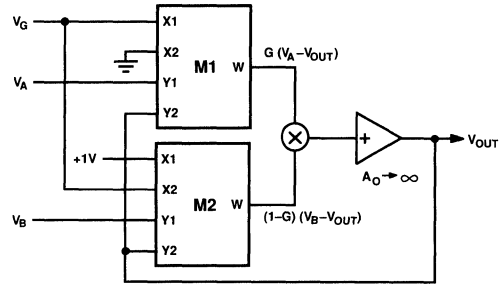


Figure 8. Elements of a Feedback Keyer

are identical to those used previously. The bias currents required at the output of the multipliers are provided by R8 and R9. A dc-level-shifting network comprising R10/R12 and R11/R13 ensures that the input nodes of the AD811 are positioned within an acceptable common-mode range for this IC. At high frequencies, C1 and C2 bypass R10 and R11, respectively.

R14 is included to lower the HF loop gain, and is needed because the voltage-to-current conversion in the AD834s, via the Y2 inputs, results in an effective value of the feedback resistance of 250 Ω (see Figure 5); this is only half the minimum value of 500 Ω required for HF stability of the AD811. (Note that this resistance is unaffected by G: when G = 1, all the feedback is via U1, while when G = 0 it is all via U2.) Resistor R14 reduces the fractional amount of output current from the multipliers into the current-summing inverting input of the AD811, by sharing it with R8. This resistor can be used to adjust the bandwidth and damping factor to best suit the application.

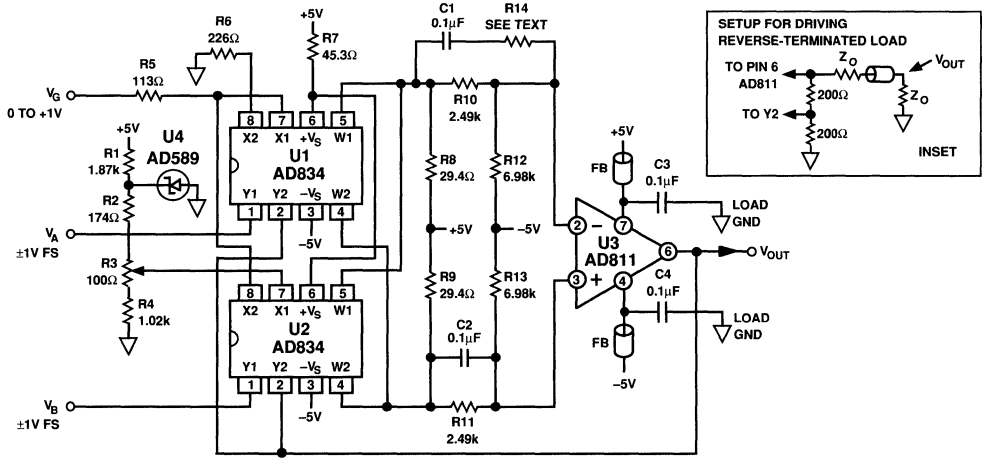


Figure 9. A Practical Embodiment of a Feedback Keyer. The Inset Shows the Feedback Configuration (Gain of ×2) for Driving a Reverse-Terminated Load.

Figure 10 shows the small-signal ac response of this system of the "A" channel at unity gain and zero gain; as is inevitably the case, there is a small amount of feedthrough at the highest frequencies. Two representative values of R14 are shown; using 402 Ω, the pulse response is considerably overdamped, resulting in a −3 dB bandwidth of 15 MHz, while a value of 107 Ω provides a maximally flat response with a −3 dB bandwidth of 70 MHz.

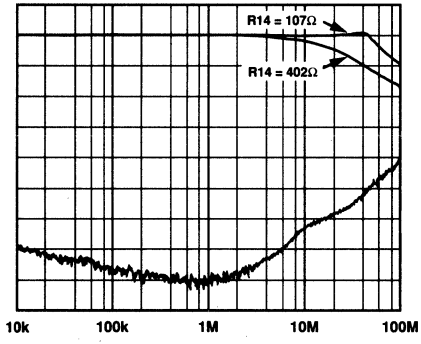
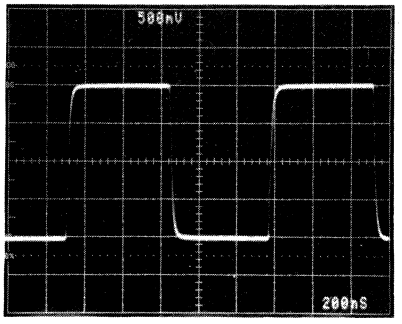
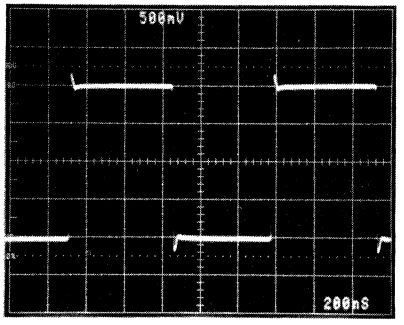


Figure 10. AC Response of the Feedback Keyer. For V_G = +1 V, the −3 dB Bandwidth Is 15 MHz Using R14 = 402 Ω and 70 MHz with R14 = 107 Ω. For These Measurements, R_L = 50 Ω

Figure 11 shows the pulse response at unity gain: in (a) R14 = 402 Ω, while in (b) R14 = 107 Ω. The frequency and pulse responses of the "B" channel, and of the gain-control input are the same, being limited by the output amplifier rather than the AD834s. Likewise, the differential gain and phase behavior will be determined primarily by the AD811; the data sheet should be consulted for more information. The feedthrough at 1 MHz is about −80 dB and −64 dB at 10 MHz and, as before, is eventually limited by board layout. All of these results used a 50 Ω load at the output.



a.



b.

Figure 11. Pulse Response of the Feedback Keyer. In (a), R14 = 402 Ω While in (b), R14 = 107 Ω. For These Measurements, R_L = 50 Ω

Unlike Figure 6's circuit, this keyer provides unity-gain operation. In applications where a reverse-terminated line (50+50 Ω or 75+75 Ω) is to be driven, the gain can be doubled by the inclusion of a resistive divider between V_{OUT} and the Y2 pins; equal resistors of 200 Ω can be used (see the inset in Figure 9). This halving of the feedback voltage also lowers the bandwidth, which can now be restored by reducing, or even eliminating, R14. Figures 12 and 13 show the modified circuit's performance when driving a 50 Ω reverse-terminated line.

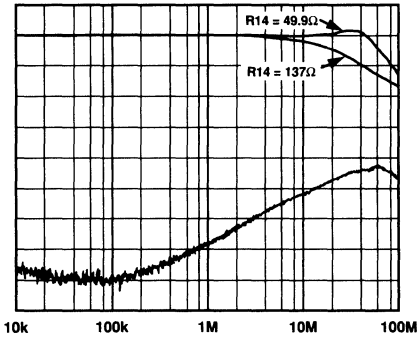
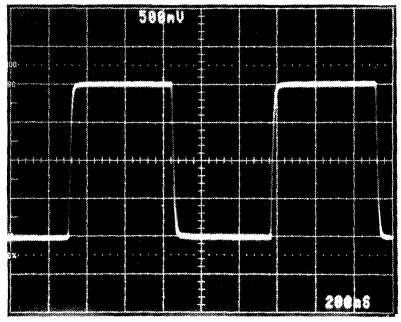
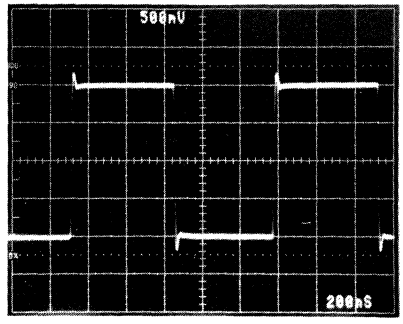


Figure 12. AC Response of the Feedback Keyer, Now Configured for a Gain of ×2. For V_G = + 1 V, the −3 dB Bandwidth Is 15 MHz Using R14 = 137 Ω and 70 MHz with R14 = 49.9 Ω. For These Measurements, R_L = 50 Ω



a.



b.

Figure 13. Pulse Response of the Feedback Keyer Now Configured for a Gain of ×2. In (a), R14 = 137 Ω While in (b), R14 = 49.9 Ω. For These Measurements, R_L = 50 Ω

ANALOG DEVICES

AN-217
APPLICATION NOTE

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Audio Applications of the ADSP Family (IIR Filters)

INFINITE IMPULSE RESPONSE (IIR) FILTERS

Compared to the FIR filter, an IIR filter can often be much more efficient in terms of attaining certain performance characteristics with a given filter order. This is because the IIR filter incorporates feedback and is capable of realizing both poles and zeros of a system transfer function, whereas the FIR filter is only capable of realizing the zeros (although the FIR filter is still more desirable in many applications, because of features such as stability and the ability to realize exactly linear phase responses).

Direct Form IIR Filter

The IIR filter can realize both the poles and zeros of a system because it has a rational transfer function, described by polynomials in z in both the numerator and the denominator:

$$H(z) = \frac{\sum_{k=0}^{M} b_k z^{-k}}{1 - \sum_{k=1}^{N} a_k z^{-k}}$$

The difference equation for such a system is described by the following:

$$y(n) = \sum_{k=0}^{M} b_k x(n-k) + \sum_{k=1}^{N} a_k y(n-k)$$

In most applications, the order of the two polynomials M and N are the same.

The roots of the denominator determine the pole locations of the filter, and the roots of the numerator determine the zero locations. There are, of course, several means of implementing the above transfer function with an IIR filter structure. The "direct form" structure presented in Listing 1 implements the difference equation above.

Note that there is a single delay line buffer for the recursive and nonrecursive portions of the filter (Oppenheim and Schafer's Direct Form II). The sum-of-products of the a values and the delay line values are first computed, followed by the sum-of-products of the b values and the delay line values.

```
.MODULE  diriir_sub;

{
   Direct Form II IIR Filter Subroutine

   Calling Parameters
            MR1 = Input sample (x[n])
            MR0 = 0
            I0 → Delay line buffer current location (x[n–1])
            L0 = Filter length
            I5 → Feedback coefficients (a[1], a[2], . . . a[N])
            L5 = Filter length – 1
            I6 → Feedforward coefficients (b[0], b[1], . . . b[N])
            L6 = Filter length
            M0 = 0
            M1,M4 = 1
            CNTR = Filter length – 2
            AX0 = Filter length – 1

   Return Values
            MR1 = output sample (y[n])
            I0 → delay line current location (x[n–1])
            I5 → feedback coefficients
            I6 → feedforward coefficients

   Altered Registers
            MX0,MY0,MR

   Computation Time
            ((N – 2) + (N – 1)) + 10 + 4 cycles (N = M = Filter order)

   All coefficients and data values are assumed to be in 1.15 format.

}

.ENTRY diriir;

diriir:     MX0=DM(I0,M1), MY0=PM(I5,M4);
            DO poleloop UNTIL CE;
poleloop:   MR=MR+MX0*MY0(SS), MX0=DM(I0,M1), MY0=PM(I5,M4);
            MR=MR+MX0*MY0(RND);
            CNTR=AX0;
            DM(I0,M0)=MR1;
            MR=0, MX0=DM(I0,M1), MY0=PM(I6,M4);
            DO zeroloop UNTIL CE;

zeroloop:   MR=MR+MX0*MY0(SS), MX0=DM(I0,M1), MY0=PM(I6,M4);
            MR=MR+MX0*MY0(RND);
            MODIFY (I0,M2);
            RTS;

.ENDMOD;
```

Listing 1. Direct Form IIR Filter

11

Cascaded Biquad IIR Filter

A second-order biquad IIR filter section is shown on Figure 1. Its transfer function in the z-domain is:

$$H(z) = Y(z)/X(z) = (B_0 + B_1 z^{-1} + B_2 z^{-2})/(1 + A_1 z^{-1} + A_2 z^{-2})$$

where A_1, A_2, B_0, B_1 and B_2 are coefficients that determine the desired impulse response of the system H(z). Furthermore, the corresponding difference equation for a biquad section is:

$$Y(n) = B_0 X(n) + B_1 X(n-1) + B_2 X(n-2) - A_1 Y(n-1) - A_2 Y(n-2)$$

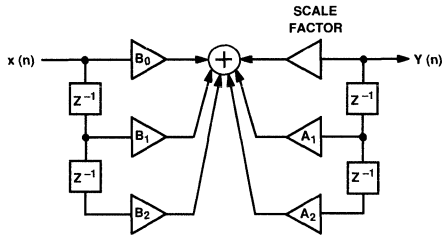

Figure 1. Second-Order Biquad IIR Filter Section

Higher-order filters can be obtained by cascading several biquad sections with appropriate coefficients. Another way to design higher-order filters is to use only one complicated single section. This approach is called the direct form implementation. The biquad implementation executes slower but generates smaller numerical errors than the direct form implementation. The biquads can be scaled separately and then cascaded to minimize the coefficient quantization and the recursive accumulation errors. The coefficients and data in the direct form implementation must be scaled all at once, which gives rise to larger errors. Another disadvantage of the direct form implementation is that the poles of such single-stage high-order polynomials get increasingly sensitive to quantization errors. The second-order polynomial sections (i.e., biquads) are less sensitive to quantization effects.

An ADSP-2100 subroutine that implements a high-order filter is shown in Listing 2. The subroutine is arranged as a module and is labeled *biquad_sub*. There are a number of registers that need to be initialized in order to execute this subroutine. It may be sufficient to do this initialization only once (e.g., at power-up) if other executed algorithms do not need these registers. In most typical cases, however, some of these registers may need to be set every time the *biquad_sub* routine is called. It may sometimes be beneficial, from a modular software point of view, always to initialize all the setup registers as a part of this subroutine.

The *biquad_sub* routine takes its input from the SR1 register. This register must contain the 16-bit input X(n). X(n) is assumed to be already computed before this subroutine is called. The output of the filter is also made available in the SR1 register.

After the initial design of a high-order filter, all coefficients must be scaled down separately in each biquad stage. This is necessary in order to conform to the 16-bit fixed-point fractional number format as well as to ensure that overflows will not occur in the final multiply-accumulate operations in each stage. The scaled-down coefficients are the ones that get stored in the processor's memory. The operations in each biquad are performed with scaled data and coefficients and are eventually scaled up before being output to the next one. The choice of a proper scaling factor depends greatly on the design objectives, and in some cases it may even be unnecessary. The filter coefficients are usually designed with a commercial software package in higher than 16-bit precision arithmetic. System performance deviates from ideal when such high precision coefficients are quantized to 16 bits and further scaled down. In systems that require stringent specifications, careful simulations of quantization and scaling effects must be performed.

During the initialization of the *biquad_sub* routine, the index register I0 points to the data memory buffer that contains the previous error inputs and the previous biquad section outputs. This buffer must be initialized to zero at powerup unless some nonzero initial condition is desired. The index register I1 points to another buffer in data memory that contains the individual scale factors for each biquad. The buffer length register L1 is set to zero if the filter has only one biquad section. In the case of multiple biquads, L1 is initialized with the number of biquad sections. The index register I4, on the other hand, points to the circular program memory buffer that contains the scaled biquad coefficients. These coefficients are stored in the order: B_2, B_1, B_0, A_2 and A_1 for each biquad. All of the individual biquad coefficient groups must be stored in the same order in which the biquads are cascaded, such as: B_2, B_1, B_0, A_2, A_1, B_2*, B_1*, B_0*, A_2*, A_1*, B_2**, etc. The buffer length register L4 must be set to the value of (5 × number of biquad sections). Finally, the loop counter register CNTR must be set to the number of biquad sections, since the filter code will be executed as a loop.

The core of the *biquad_sub* routine starts its execution at the *biquad* label. The routine is organized in a looped fashion where the end of the loop is the instruction labeled *sections*. Each iteration of the loop executes the computations for one biquad. The number of loops to be executed is determined by the CNTR register contents. The SE register is loaded with the appropriate scaling factor for the particular biquad at the beginning of each loop iteration. After this operation, the coefficients and the data values are fetched from memory in the sequence in which they have been stored. These numbers are multiplied and accumulated until all of the values for a particular biquad have been accessed. The result of the last multiply/accumulate is rounded to 16 bits and upshifted by the scaling value. At this point, the *biquad* loop is executed again, or the filter computations are completed by doing the final update to the delay line.

The delay lines for data values are always being updated within the *biquad* loop as well as outside of it.

The filter coefficients must be scaled appropriately so that no overflows occur after the upshifting operation between the biquads. If this is not ensured by design, it may be necessary to include some overflow checking between the biquads.

The execution time for an Nth order *biquad_sub* routine can be calculated as follows (assuming that the appropriate registers have been initialized and N is a power of 2):

ADSP-2101/2102: $(8 \times N/2) + 4$ processor cycles
ADSP-2100/2100A: $(8 \times N/2) + 4 + 5$ processor cycles

It may take up to a maximum of 12 cycles to initialize the appropriate registers every time the filter is called, but typically this number will be lower.

```
.MODULE biquad_sub;

{ Nth order cascaded biquad filter subroutine

  Calling Parameters:

        SR1 = input X(n)
        I0 → delay line buffer for X(n-2), X(n–1),
             Y(n-2), Y(n-1)
        L0 = 0
        I1 → scaling factors for each biquad section
        L1 = 0 (in the case of a single biquad)
        L1 = number of biquad sections
             (for multiple biquads)
        I4 → scaled biquad coefficients
        L4 = 5 × [number of biquads]
        M0, M4 = 1
        M1 = –3
        M2 = 1 (in the case of multiple biquads)
        M2 = 0 (in the case of a single biquad)
        M3 = (1 – length of delay line buffer)

  Return Value:
        SR1 = output sample Y(n)

  Altered Registers:
        SE, MX0, MX1, MY0, MR, SR

  Computation Time (with N even):
        ADSP-2101/2102: (8 × N/2) + 5 cycles
        ADSP-2100/2100A: (8 × N/2) + 5 + 5 cycles

  All coefficients and data values are assumed to be in 1.15 format

}

.ENTRY biquad;

biquad: CNTR = number_of_biquads
        DO sections UNTIL CE;
          SE=DM(I1,M2);
          MX0=DM(I0,M0), MY0=PM(I4,M4);
          MR=MX0*MY0(SS), MX1=DM(I0,M0), MY0=PM(I4,M4);
          MR=MR+MX1*MY0(SS), MY0=PM(I4,M4);
          MR=MR+SR1*MY0(SS), MX0=DM(I0,M0), MY0=PM(I4,M4);
          MR=MR+MX0*MY0(SS), MX0=DM(I0,M1), MY0=PM(I4,M4);
          DM(I0,M0)=MX1, MR=MR+MX0*MY0(RND);
sections: DM(I0,M0)=SR1, SR=ASHIFT MR1 (HI);
        DM(I0,M0)=MX0;
        DM(I0,M3)=SR1;
        RTS;

.ENDMOD;
```

Listing 2. Cascaded Biquad IIR Filter

ANALOG DEVICES

AN-218
APPLICATION NOTE

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DSP Multirate Filters

MULTIRATE FILTERS

Multirate filters are digital filters that change the sampling rate of a digitally represented signal. These filters convert a set of input samples to another set of data that represents the same analog signal sampled at a different rate. A system incorporating multirate filters (a multirate system) can process data sampled at various rates.

Some examples of applications for multirate filters are:

- Sample-rate conversion between digital audio systems
- Narrow-band low-pass and band-pass filters
- Sub-band coding for speech processing in vocoders
- Transmultiplexers for TDM (time-division multiplexing) to FDM (frequency-division multiplexing) translation
- Quadrature modulation
- Digital reconstruction filters and antialias filters for digital audio, and
- Narrow-band spectra calculation for sonar and vibration analysis.

The two types of multirate filtering processes are decimation and interpolation. Decimation reduces the sample rate of a signal. It eliminates redundant or unnecessary information and compacts the data, allowing more information to be stored, processed, or transmitted in the same amount of data. Interpolation increases the sample rate of a signal. Through calculations on existing data, interpolation fills in missing information between the samples of a signal. Decimation reduces a sample rate by an integer factor M, and interpolation increases a sample rate by an integer factor L. Non-integer rational (ratio of integers) changes in sample rate can be achieved by combining the interpolation and decimation processes.

The ADSP-2100 programs in this application note demonstrate decimation and interpolation as well as efficient rational changes in sample rate. Cascaded stages of decimation and interpolation, which are required for large rate changes (large values of L and M) and are useful for implementing narrow-band low-pass and band-pass filters, are also demonstrated.

Decimation

Decimation is equivalent to sampling a discrete-time signal. Continuous-time (analog) signal sampling and discrete-time (digital) signal sampling are analogous.

Decimation Filter Structure

The decimation algorithm can be implemented in an FIR (Finite Impulse Response) filter structure. The FIR filter has many advantages for multirate filtering including: linear phase, unconditional stability, simple structure, and easy coefficient design. Additionally, the FIR structure in multirate filters provides for an increase in computational efficiency over IIR structures. The major difference between the IIR and the FIR filter is that the IIR filter must calculate all outputs for all inputs. The FIR multirate filter calculates an output for every Mth input. For a more detailed description of the FIR and IIR filters, refer to Crochiere and Rabiner, 1983.

The impulse response of the anti-imaging low-pass filter is h(n). A time-series equation filtering x(n) is the convolution

$$w(n) = \sum_{k=0}^{N-1} h(k)\, x(n-k)$$

where N is the number of coefficients in h(n). N is the order, or number of taps, in the filter. The application of this equation to implement the filter response $H(e^{jw})$ results in an FIR filter structure.

Figure 1a, shows the signal flowgraph of an FIR decimation filter. The N most recent input samples are stored in a delay line; $z-1$ is a unit sample delay. N samples from the delay line are multiplied by N coefficients and the resulting products are summed to form a single output sample w(n). Then w(n) is down-sampled by M using the rate compressor.

It is not necessary to calculate the samples of w(n) that are discarded by the rate compressor. Accordingly, the rate compressor can be moved in front of the multiply/accumulate paths, as shown in Figure 1b. This change reduces the required computation by a factor of M. This

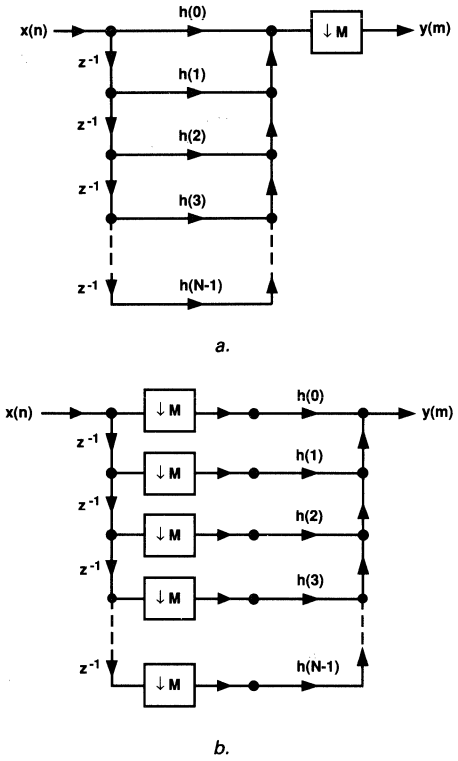


Figure 1. FIR Form Decimation Filter

filter structure can be implemented by updating the delay line with M inputs before each output sample is calculated.

Substitution of the relationship between w(n) and y(m) into the convolution results in the decimation filtering equation

$$y(m) = \sum_{k=0}^{N-1} h(k)\, x(Mm-k)$$

Some of the implementations shown in textbooks on digital filters take advantage of the symmetry in transposed forms of the FIR structure to reduce the number of multiplications required. However, such a reduction of multiplications results in an increased number of additions. In this application, because the ADSP-2100 is capable of both multiplying and accumulating in one cycle, trading off multiplication for addition is a useless technique.

ADSP-2100 Decimation Algorithm

Figure 2 shows a flowchart of the decimation filter algorithm used for the ADSP-2100 routine. The decimator calculates one output for every M inputs to the delay line.

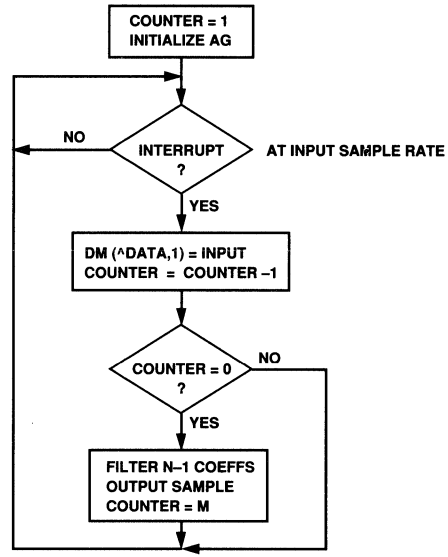


Figure 2. Decimator Flowchart

External hardware causes an interrupt at the input sample rate F_S, which triggers the program to fetch an input data sample and store it in the *data* circular buffer. The index register that points into this data buffer is then incremented by one, so that the next consecutive input sample is written to the next address in the buffer. The counter is then decremented by one and compared to zero. If the counter is not yet zero, the algorithm waits for another input sample. If the counter has decremented to zero, the algorithm calculates an output sample, then resets the counter to M so that the next output will be calculated after the next M inputs.

The output is the sum of products of N data buffer samples in a circular buffer and N coefficients in another circular buffer. Note that M input samples are written into the data buffer before an output sample is calculated. Therefore, the resulting output sample rate is equal to the input rate divided by the decimation factor: $F_S' = F_S/M$.

For additional information on the use of the ADSP-2100's address generators for circular buffers, see the *ADSP-2100 User's Manual,* Chapter 2.

The ADSP-2100 program for the decimation filter is shown in Listing 1. Inputs to this filter routine come from the memory-mapped port *adc,* and outputs go to the memory-mapped port *dac.* The filter's I/O interfacing hardware is described in more detail later in this application note.

```
{DECIMATE.dsp
Real time Direct Form FIR Filter, N taps, decimates by M for a decrease of 1/M times the input sample rate.

  INPUT: adc
  OUTPUT: dac

}
.MODULE/RAM/ABS=0   decimate;
.CONST              N=300;
.CONST              M=4;                    {decimate by factor of M}
.VAR/PM/RAM/CIRC    coef [N];
.VAR/DM/RAM/CIRC    data [N];
.VAR/DM/RAM         counter;
.PORT               adc;
.PORT               dac;
.INIT               coef:<coef.dat>;
                    RTI;                    {interrupt 0}
                    RTI;                    {interrupt 1}
                    RTI;                    {interrupt 2}
                    JUMP sample;            {interrupt 3= input sample rate}
initialize:         IMASK=b#0000;           {disable all interrupts}
                    ICNTL=b#01111;          {edge sensitive interrupts}
                    SI=M;                   {set decimation counter to M}
                    DM(counter)= SI;        {for first input data sample}
                    I4=^coef;               {setup a circular buffer in PM}
                    L4=%coef;
                    M4=1;                   {modifier for coef is 1}
                    I0=^data;               {setup a circular buffer in DM}
                    L0=%data;
                    M0=1;                   {modifier for data is 1}
                    IMASK=b#1000;           {enable interrupt 3}
wait_interrupt:     JUMP wait_interrupt;    {infinite wait loop}
{_________Decimator, code executed at the sample rate_________________}
sample:             AY0=DM(adc);
                    DM(I0,M0)=AY0;          {update delay line with newest}
                    AY0=DM(counter);
                    AR=AY0-1;               {decrement and update counter}
                    DM(counter)=AR;
                    IF NE RTI;              {test and return if not M times}
{_____   code below executed at 1/M times the sample rate_____________}
do_fir:             AR=M;                   {reset the counter to M}
                    DM(counter)=AR;
                    CNTR=N - 1;
                    MR=0, MX0=DM(I0,M0), MY0=PM(I4,M4);
                    DO taploop UNTIL CE;    {N-1 taps of FIR}
taploop:              MR=MR+MX0*MY0(SS), MX0=DM(I0,M0), MY0=PM(I4,M4);
                    MR=MR+MX0*MY0(RND);     {last tap with round}
                    IF MV SAT MR;           {saturate result if overflow}
                    DM(dac)=MR1;            {output data sample}
                    RTI;
.ENDMOD;
```

Listing 1. Decimation Filter

The routine uses two circular buffers, one for data samples and one for coefficients, that are each N locations long. The *coef* buffer is located in program memory and stores the filter coefficients. Each time an output is calculated, the decimator accesses all these coefficients in sequence, starting with the first location in *coef*. The I4 index register, which points to the coefficient buffer, is modified by one (from modify register M0) each time it is accessed. Therefore, I4 is always modified back to the beginning of the coefficient buffer after the calculation is complete.

The FIR filter equation starts the convolution with the most recent data sample and accesses the oldest data sample last. Delay lines implemented with circular buffers, however, access data in the opposite order. The oldest data sample is fetched first from the buffer and the newest data sample is fetched last. Therefore, to keep the data/coefficient pairs together, the coefficients must be stored in memory in reverse order.

The relationship between the address and the contents of the two circular buffers (after N inputs have occurred) is shown in the table below. The *data* buffer is located in data memory and contains the last N data samples input to the filter. Each pass of the filter accesses the locations of both buffers sequentially (the pointer is modified by one), but the first address accessed is not always the first location in the buffer, because the decimation filter inputs M samples into the delay line before starting each filter pass. For each pass, the first fetch from the data buffer is from an address M greater than for the previous pass. The data delay line moves forward M samples for every output calculated.

Data		*Coefficient*	
DM(0)	= x(n−(N−1)) oldest	PM(0)	= h(N−1)
DM(1)	= x(n−(N−2))	PM(1)	= h(N−2)
DM(2)	= x(n−(N−3))	PM(2)	= h(N−3)
	●		●
	●		●
	●		●
DM(N−3)	= x(n−2)	PM(N−3)	= h(2)
DM(N−2)	= x(n−1)	PM(N−2)	= h(1)
DM(N−1)	= x(n−0) newest	PM(N−1)	= h(0)

A variable in data memory is used to store the decimation counter. One of the processor's registers could have been used for this counter, but using a memory location allows for expansion to multiple stages of decimation.

The number of cycles required for the decimation filter routine is shown below. The ADSP-2100 takes one cycle to calculate each tap (multiply and accumulate), so only 18+N cycles are necessary to calculate one output sample of an N-tap decimator. The 18 cycles of overhead for each pass is just six cycles greater than the overhead of a non-multirate FIR filter.

Interrupt Response	2 Cycles
Fetch Input	1 Cycle
Write Input to Data Buffer	1 Cycle
Decrement and Test Counter	4 Cycles
Reload Counter with M	2 Cycles
FIR Filter Pass	7+N Cycles
Return from Interrupt	1 Cycle
Maximum Total	18+N Cycles/Output

A More Efficient Decimator

The routine in Listing 1 requires that the 18+N cycles needed to calculate an output occur during the first of the M input sample intervals. No calculations are done in the remaining M−1 intervals. This limits the number of filter taps that can be calculated in real time to:

$$N = \frac{1}{F_S\, t_{CLK}} - 18$$

where t_{CLK} is the instruction cycle time of the processor.

An increase in this limit by a factor of M occurs if the program is modified so that the M data inputs overlap the filter calculations. This more efficient version of the program is shown in Listing 2.

In this example, a circular buffer *input_buf* stores the M input samples. The code for loading *input_buf* is placed in an interrupt routine to allow the input of data and the FIR filter calculations to occur simultaneously.

A loop waits until the input buffer is filled with M samples before the filter output is calculated. Instead of counting input samples, this program determines that M samples have been input when the input buffer's index register I0 is modified back to the buffer's starting address. This strategy saves a few cycles in the interrupt routine.

After M samples have been input, a second loop transfers the data from *input_buf* to the data buffer. An output sample is calculated. Then the program checks that at least one sample has been placed in *input_buf*. This check prevents a false output if the output calculation occurs in less than one sample interval. Then the program jumps back to wait until the next M samples have been input.

This more efficient decimation filter spreads the calculations over the output sample interval $1/F_S'$ instead of the input interval $1/F_S$. The number of taps that can be calculated in real time is:

$$N = \frac{M}{F_S\, t_{CLK}} - 20 - 2M - 6(M-1)$$

which is approximately M times greater than for the first routine.

{DEC_EFF.dsp
Real time Direct Form FIR Filter, N taps, decimates by M for a decrease of 1/M times the input sample rate. This version uses an input buffer to allow the filter computations to occur in parallel with inputs. This allows larger order filter for a given input sample rate. To save time, an index register is used for the input buffer as well as for a decimation counter.

```
  INPUT: adc
  OUTPUT: dac
}
.MODULE/RAM/ABS=0          eff_decimate;
.CONST                     N=300;
.CONST                     M=4;                    {decimate by factor of M}
.VAR/PM/RAM/CIRC           coef[N];
.VAR/DM/RAM/CIRC           data[N];
.VAR/DM/RAM/CIRC           input_buf[M];
.PORT                      adc;
.PORT                      dac;
.INIT                      coef:<coef.dat>;
      RTI;                      {interrupt 0}
      RTI;                      {interrupt 1}
      RTI;                      {interrupt 2}
      JUMP sample;              {interrupt 3= input sample rate}
initialize:                IMASK=b#0000;           {disable all interrupts}
                           ICNTL=b#01111;          {edge sensitive interrupts}
                           I4=^coef;               {setup a circular buffer in PM}
                           L4=%coef;
                           M4=1;                   {modifier for coef is 1}
                           I0=^data;               {setup a circular buffer in DM}
                           L0=%data;
                           M0=1;                   {modifier for data is 1}
                           I1=^input_buf;          {setup a circular buffer in DM}
                           L1=%input_buf;
                           IMASK=b#1000;           {enable interrupt 3}
wait_M:                    AX0=I1;                 {wait for M inputs}
                           AY0=^input_buf;
                           AR=AX0-AY0;             {test if pointer is at start}
                           IF NE JUMP wait_M;
{_____code below executed at 1/M times the sample rate_____}
                           CNTR=M;
                           DO load_data UNTIL CE;
                              AR=DM(I1,M0);
load_data:                    DM(I0,M0)=AR;
fir:                       CNTR=N - 1;
                           MR=0, MX0=DM(I0,M0), MY0=PM(I4,M4);
                           DO taploop UNTIL CE;    {N-1 taps of FIR}
taploop:                      MR=MR+MX0*MY0(SS), MX0=DM(I0,M0), MY0=PM(I4,M4);
                           MR=MR+MX0*MY0(RND);     {last tap with round}
                           IF MV SAT MR;           {saturate result if overflow}
                           DM(dac)=MR1;            {output data sample}
wait_again:                AX0=I1;
                           AY0=^input_buf;
                           AR=AX0-AY0;             {test and wait if i1 still}
                           IF EQ JUMP wait_again;  {points to start of input_buf}
                           JUMP wait_M;
{_____sample input, code executed at the sample rate_____}
sample:                    ENA SEC_REG;            {so no registers will get lost}
                           AY0=DM(adc);            {get input sample}
                           DM(I1,M0)=AY0;          {load in M long buffer}
                           RTI;
.ENDMOD;
```

Listing 2. Efficient Decimation Filter

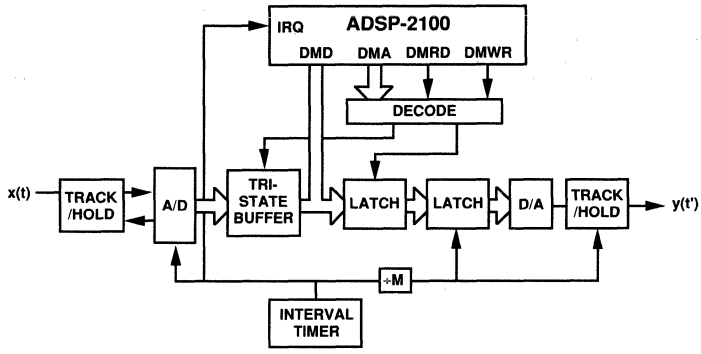


Figure 3. Decimator Hardware

Decimator Hardware Configuration

Both decimation filter programs assume an ADSP-2100 system with the I/O hardware configuration shown in Figure 3. The processor is interrupted by an interval timer at a frequency equal to the input sample rate F_S and responds by inputting a data value from the A/D converter. The track/hold (sampler) and the A/D converter (quantizer) are also clocked at this frequency. The D/A converter on the filter output is clocked at a rate of F_S/M, which is generated by dividing the interval timer frequency by M.

To keep the output signal jitter-free, it is important to derive the D/A converter's clock from the interval timer and not from the ADSP-2100. The sample period of the analog output should be disassociated from writes to the D/A converter. If an instruction-derived clock is used, any conditional instructions in the program could branch to different length program paths, causing the output samples to be spaced unequally in time. The D/A converter must be double-buffered to accommodate the interval-time-derived clock. The ADSP-2100 outputs data to one latch. Data from this latch is fed to a second latch that is controlled by an interval-timer-derived clock.

Interpolation

The process of recreating a continuous-time signal from its discrete-time representation is called reconstruction. Interpolation can be thought of as the reconstruction of a discrete-time signal from another discrete-time signal, just as decimation is equivalent to sampling the samples of a signal. Continuous-time (analog) signal reconstruction and discrete-time (digital) signal reconstruction are analogous.

Interpolation Filter Structure

Figure 4a shows a block diagram of an interpolation filter. The two major differences from the decimation filter are that the interpolator uses a sample rate expander instead of the sample rate compressor and that the interpolator's low-pass filter is placed after the rate expander instead of before the rate compressor. The rate expander, which is the block labeled with an up-arrow and L, inserts L−1 zero-valued samples after each input sample. The resulting w(m) is low-pass filtered to

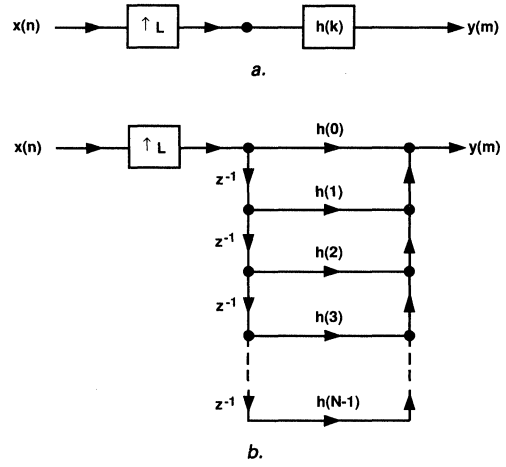


Figure 4. Interpolation Filter Block Diagram

produce y(m), a smoothed, anti-imaged version of w(m). The transfer function of the interpolator H(k) incorporates a gain of 1/L because the L−1 zeros inserted by the rate expander cause the energy of each input to be spread over L output samples.

The low-pass filter of the interpolator uses an FIR filter structure for the same reasons that an FIR filter is used in the decimator, notably computational efficiency. The convolution equation for this filter is

$$y(m) = \sum_{k=0}^{N-1} h(k)\, w(m-k)$$

N−1 is the number of filter coefficients (taps) in h(k), w(m−k) is the rate expanded version of the input x(n), and w(m−k) is related to x(n) by

$$w(m-k) = \begin{cases} x((m-k)/L) & \text{for } m-k = 0, \pm L, \pm 2L, \ldots \\ 0 & \text{otherwise} \end{cases}$$

The signal flowgraph that represents the interpolation filter is shown in Figure 4b. A delay line of length N is loaded with an input sample followed by L−1 zeros,

then the next input sample and L−1 zeros, and so on. The output is the sum of the N products of each sample from the delay line and its corresponding filter coefficient. The filter calculates an output for every sample, zero or data, loaded into the delay line.

An example of the interpolator operation is shown in the signal flowgraph in Figure 5. The contents of the delay line for three consecutive passes of the filter are highlighted. In this example, the interpolation factor L is 3. The delay line is N locations long, where N is the number of coefficients of the filter; N=9 in this example. There are N/L or 3 data samples in the delay line during each pass. The data samples x(1), x(2), and x(3) in the first pass are separated by L−1 or 2 zeros inserted by the rate expander. The zero-valued samples contribute (L−1)N/L or 6 zero-valued products to the output result. These (L−1)N/L multiplications are unnecessary and waste processor capacity and execution time.

A more efficient interpolation method is to access the coefficients and the data in a way that eliminates wasted calculations. This method is accomplished by removing the rate expander to eliminate the storage of the zero-valued samples and shortening the data delay line from N to N/L locations. In this implementation, the data delay line is updated only after L outputs are calculated. The same N/L (three) data samples are accessed for each set of L output calculations. Each output calculation accesses every Lth (third) coefficient, skipping the coefficients that correspond to zero-valued data samples.

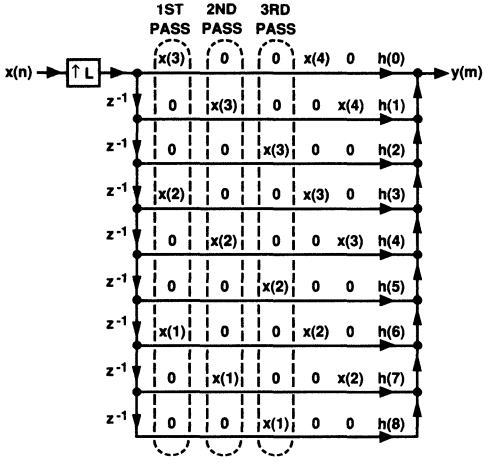


Figure 5. Example Interpolator Flowgraph

Crochiere and Rabiner refer to this efficient interpolation filtering method as *polyphase filtering*, because a different phase of the filter function h(k) (equivalent to a set of interleaved coefficients) is used to calculate each output sample.

ADSP-2100 Interpolation Algorithm

A circular buffer of length N/L located in data memory forms the data delay line. Although the convolution equation accesses the newest data sample first and the oldest data sample last, the ADSP-2100 fetches data samples from the circular buffer in the opposite order: oldest data first, newest data last. To keep the data/coefficient pairs together, the coefficients are stored in program memory in reverse order, e.g., h(N−1) in PM(0) and h(0) in PM(N−1).

Figure 6 shows a flowchart of the interpolation algorithm. The processor waits in a loop and is interrupted at the output sample rate (L times the input sample rate). In the interrupt routine, the coefficient address pointer is decremented by one location so that a new set of interleaved coefficients will be accessed in the next filter pass. A counter tracks the occurrence of every Lth output; on the Lth output, an input sample is taken and the coefficient address pointer is set forward L locations, back to the first set of interleaved coefficients. The output is then calculated with the coefficient address pointer incremented by L locations to fetch every Lth coefficient. One restriction in this algorithm is that the number of filter taps must be an integral multiple of the interpolation factor; N/L must be an integer.

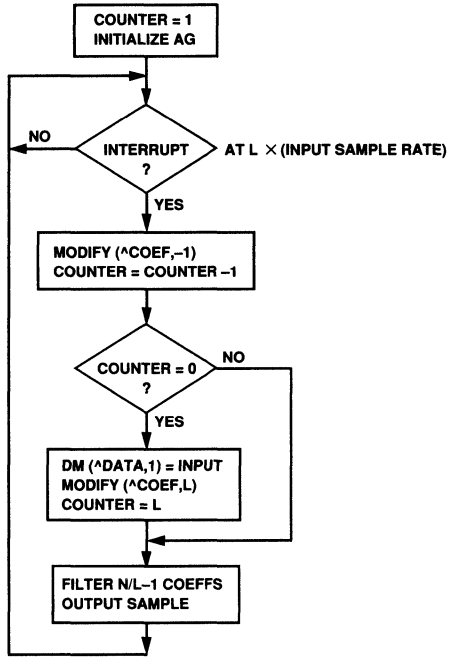


Figure 6. Interpolation Flowchart

Listing 3 is an ADSP-2100 program that implements this interpolation algorithm. The ADSP-2100 is capable of calculating each filter pass in ((N/L)+17) processor instruction cycles. Each pass must be calculated within the period between output samples, equal to $1/F_S L$. Thus the maximum number of taps that can be calculated in real time is:

$$N = \frac{1}{F_S\, t_{CLK}} - 17L$$

where t_{CLK} is the processor cycle time and F_S is the input sampling rate.

The interpolation filter has a gain of 1/L in the passband. One method to attain unity gain is to premultiply (offline) all the filter coefficients by L. This method requires the maximum coefficient amplitude to be less than 1/L, otherwise the multiplication overflows the 16-bit coefficient word length. If the maximum coefficient amplitude is not less than 1/L, then you must multiply each output result by 1/L instead. The code in Listing 4 performs the 16-by-32 bit multiplication needed for this gain correction. The MY1 register should be initialized to L at the start of the routine, and the last multiply/accumulate of the filter should be performed with (SS) format, not the rounding option. This code multiplies a filter output sample in 1.31 format by the gain L, in 16.0 format, and produces in a 1.15 format corrected output in the SR0 register.

```
{INTERPOLATE.dsp
Real time Direct Form FIR Filter, N taps, uses an efficient algorithm to interpolate
by L for an increase of L times the input sample rate. A restriction on the number
of taps is that N/L be an integer.

    INPUT: adc
    OUTPUT: dac
}
.MODULE/RAM/ABS=0 interpolate;
.CONST          N=30;
.CONST          L=4;                        {interpolate by factor of L}
.CONST          NoverL=75;
.VAR/PM/RAM/CIRC coef[N];
.VAR/DM/RAM/CIRC data[NoverL];
.VAR/DM/RAM     counter;
.PORT           adc;
.PORT           dac;
.INIT           coef:<coef.dat>;
                RTI;                        {interrupt 0}
                RTI;                        {interrupt 1}
                RTI;                        {interrupt 1}
    JUMP sample;                            {interrupt 3 at (L*input rate)}
initialize:     IMASK=b#0000;               {disable all interrupts}
                ICNTL=b#01111;              {edge sensitive interrupts}
                SI=1;                       {set interpolate counter to 1}
                DM(counter)=SI;             {for first data sample}
                I4=^coef;                   {setup a circular buffer in PM}
                L4=%coef;
                M4=L;                       {modifier for coef is L}
                M5=-1;                      {modifier to shift coef back -1}
                I0=^data;                   {setup a circular buffer in DM}
                L0=%data;
                M0=1;
                IMASK=b#1000;               {enable interrupt 3}
wait_interrupt: JUMP wait_interrupt;        {infinite wait loop}
{_____Interpolate_____}
sample:         MODIFY(I4,M5);              {shifts coef pointer back by -1}
                AY0=DM(counter);
                AR=AY0-1;                   {decrement and update counter}
                DM(counter)=AR;
                IF NE JUMP do_fir;          {test and input if L times}
{_____input data sample, code executed at the sample rate_____}
do_input:       AY0=DM(adc);                {input data sample}
                DM(I0,M0)=AY0;              {update delay line with newest}
                MODIFY(I4,M4);              {shifts coef pointer up by L}
                DM(counter)=M4;             {reset counter to L}
{_____filter pass, occurs at L times the input sample rate_____}
do_fir:         CNTR=NoverL - 1;            {N/L-1 since round on last tap}
                MR=0, MX0=DM(I0,M0), MY0=PM(I4,M4);
                DO taploop UNTIL CE;        {N/L-1 taps of FIR}
taploop:          MR=MR+MX0*MY0(SS), MX0=DM(I0,M0), MY0=PM(I4,M4);
                MR=MR+MX0*MY0(RND);         {last tap with round}
                IF MV SAT MR;               {saturate result if overflowed}
                DM(dac)=MR1;                {output sample}
                RTI;
.ENDMOD;
```

Listing 3. Efficient Interpolation Filter

```
MX1= MR1;
MR= MR0*MY1 (UU);
MR0= MR1;
MR1= MR2;
MR= MR+MX1*MY1 (SU);
SR= LSHIFT MR0 BY -1 (LO);
SR= SR OR ASHIFT MR1 BY -1 (HI);
```

Listing 4. Extended Precision Multiply

Interpolator Hardware Configuration

The I/O hardware required for the interpolation filter is the same as that for the decimation filter with the exception that the interval timer clocks the output D/A converter, and the input A/D converter is clocked by the interval counter signal divided by L. The interval timer interrupts the ADSP-2100 at the output sample rate. This configuration is shown in Figure 7.

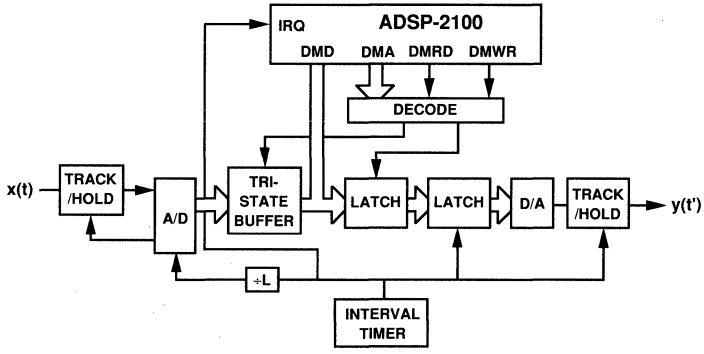


Figure 7. Interpolation Filter Hardware

ANALOG DEVICES

AN-219
APPLICATION NOTE

ONE TECHNOLOGY WAY • P.O. BOX 9106 • NORWOOD, MASSACHUSETTS 02062-9106 • 617/329-4700

Electronic Adjustment Made Easy with the TrimDAC™

by Walter Heinzer and Joe Buxton

The TrimDAC™ is a multi-channel d/a converter designed specifically for adjusting gains and dc levels in electronic circuits digitally and without moving parts. It combines many of the properties of the adjusting pot(entiometer) with the prospect of hands-off automatic adjustment and high reliability. The highly desirable attributes of TrimDACs include small package size, many devices per package, serial interface (reduces pin count) and low power dissipation. TrimDACs in electronic adjustment reduce cost in two ways: the higher speed of adjustment under software control saves time and capital investment; and the device itself is quite cheap.

Most designers of new circuit designs would like to avoid the once-ubiquitous variable resistor because of its mechanical sensitivity, relatively wide absolute tolerances, and high labor cost. But there is generally a need for factory adjustments and calibrations in electronic equipment. Even digital products need a power supply adjusted or calibrated to a specified tolerance. And many electronic systems are connected to real world sensors or output devices in *systems* that need calibration. A key issue facing engineers who design such systems is cost reduction of factory calibration and field maintenance.

Electronic factory-calibration of chips by semiconductor manufacturers is already widely used; calibration and adjustment problems are solved on (and with) integrated circuits by autozero, self-calibration, Zener-zap, fuse link, EPROM and laser trim. Something akin to this in larger-scale real-world systems is highly desirable.

Recognizing this problem, we sought to design products to fill the need for digitally adjustable electronic devices to automate, speed up, and eliminate manual and mechanical adjustments.

For example, consider the CRT display; curvature aberrations in the manufacturing of glass tubes require that the elements of focus (convergence & color purity) be individually adjusted, especially for high-resolution displays. Since the convergence adjustment of CRT display systems with resolutions of more than 1,000 lines requires that 6 to 8 variable-resistor adjustments be made in high-volume production—currently by robot-controlled screwdrivers—displays are ideal candidates for electronically controlled adjustment devices. The TrimDAC™ offers an attractive alternative to this mechanical adjustment approach. Previously a labor- (human or robot) intensive process taking minutes, the operation now can be done in seconds.

VOLTAGE ADJUSTMENT, THE FIRST GENERATION

The first TrimDAC, the DAC-8800, is a monolithic CMOS IC with all the ingredients necessary for general-purpose dc voltage setting. It contains eight unbuffered voltage-output d/a converters in a 20-pin skinny DIP package (Figure 1). The output voltage range, unipolar or bipolar, can be independently set for each group of four DACs. Output voltage ranges are established by the choice of high- and low- external-reference inputs. The 8-bit DACs provide 256 voltage levels within each range.

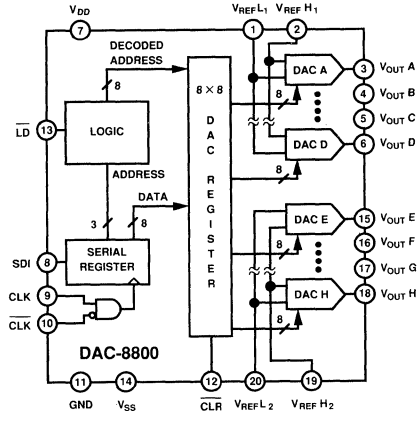


Figure 1. DAC-8800 Block Diagram. Shared References Determine Output Voltage Range.

TrimDAC is a trademark of Analog Devices, Inc.

A TTL-compatible 3-wire serial interface loads the contents of the eight internal DAC registers. These can all be set to zero by an asynchronous Clear (CLR) input, very handy for system power-up. An internal regulator provides TTL compatibility over a wide range of V_{DD} supply voltages. Single-supply operation is available by connecting V_{SS} to GND. The device achieves its performance and flexibility with a low 24 mW of dissipation.

The output voltage of each DAC is changed by clocking an 11-bit word (3 address bits, 8 data bits) into the serial shift register. The internal logic decodes the three address bits to establish which internal DAC register will receive the 8 bits of data from the serial register during the Load (LD) strobe. One DAC is updated with each LD strobe. At the maximum clock rate of 6.6 MHz, all eight d/a converters can be loaded in as little as 14 microseconds.

The output voltage range is determined by the external input voltages applied to V_{REFH} and V_{REFL} (Figure 2). If V_{SS} is negative, V_{REFL} may be set to a negative value; this results in a programmable bipolar range of output voltages. The relationship between V_{OUT}, and V_{REFH}, V_{REFL}, and the digital input, D (a base-10 integer between 0 and 255), is:

$$V_{OUT}(D) = (D/256)(V_{REFH} - V_{REFL}) + V_{REFL}$$

The DAC-8800 is tested for operation with V_{DD} = 12 V and V_{SS} = 0 V or –5 V. However, it was designed to operate from a wide variety of available supply-voltage combinations. Here are some typical pairings: V_{DD}, V_{SS} = *+15 V, 0 V; +12 V, 0 V; +12 V, –5 V; +5 V,–5 V; +5 V, –12 V; +5 V, 0 V.*

The primary application of the DAC-8800 is with fixed reference inputs for dc voltage setting. Outputs may be applied directly to high-impedance circuits—or to external op amps for buffering.

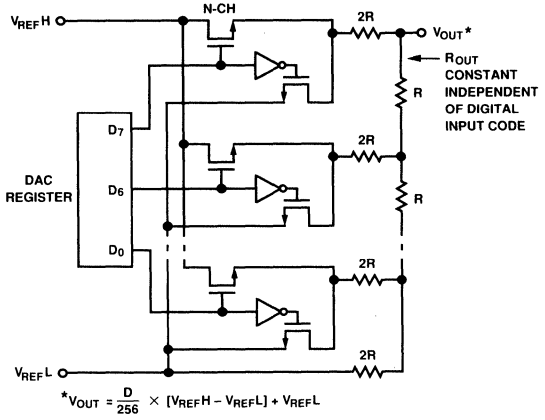


Figure 2. Simplified Equivalent Voltage-Switching DAC Circuit. The Output Resistance Remains Constant at a Nominal 11 kΩ.

ADDING GAIN: THE SECOND GENERATION

Second-generation TrimDACs, such as the DAC-8840 and DAC-8841, solve the problem of replacing variable resistors for adjusting ac or varying dc voltages—for example, in audio volume control. Other common applications where ac signals must be attenuated include some circuits found in video displays, projection-TV displays, instrumentation, oscilloscopes, medical gear, modulation circuits, modems, and so on.

The DAC-8840 contains a multiplying DAC structure with four-quadrant multiplying capability. Figure 3 shows the connection of one of the eight independent channels of the DAC-8840. This multiplying channel has a 1-MHz

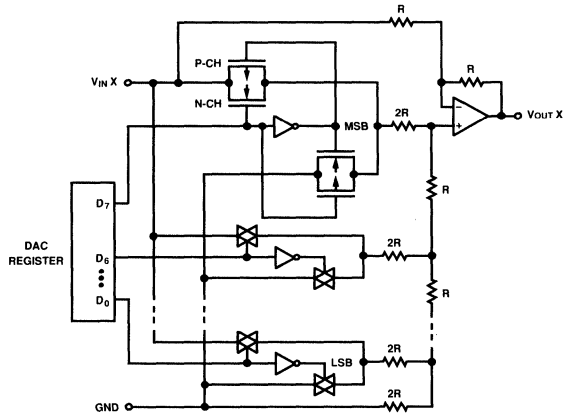


Figure 3. One Channel of the Four-Quadrant Multiplying DAC-8840.

bandwidth for ±3-V input signal levels while operating from ±5-V supplies. A typical signal channel has 0.01% total harmonic distortion and can slew at 2.5 V/μs. Because the output amplifier is connected in a differencing (push-pull) configuration, the gain for signals applied to V_{IN} can range from full-scale positive to full-scale negative, depending on the applied digital (offset binary) word. The magnitude of the binary word corresponds to the wiper position of a pot, with zero output at half-scale; a Preset control input sets all DACs to this "zero" position. Figure 4 describes this serial input CMOS octal D/A converter in greater detail.

The gain transfer function of a DAC-8840 channel is:

$$V_{OUT}(D) = (D/128 - 1)\ V_{IN}$$

where D is the value of the binary input, a decimal integer between 0 and 255. At full-scale, V_{OUT} = 127/128 × V_{IN}; when D = 128 (also the Preset condition), V_{OUT} equals zero volts; and when D = zero, $V_{OUT} = -V_{IN}$.

In the DAC-8840, eight DAC registers store the output state; they are updated from an internal serial-to-parallel shift register loaded from a standard 3-wire serial-input

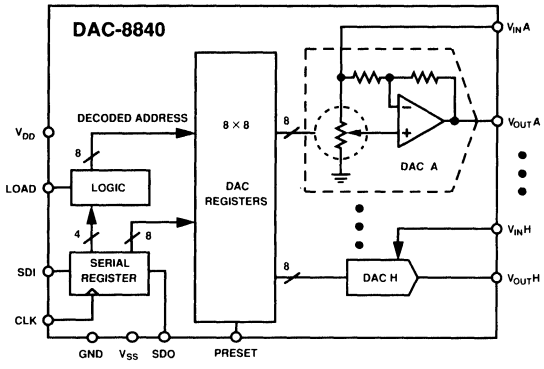


Figure 4. DAC-8840 Block Diagram. Note the 3-Wire Input and Serial Data Output Pin (SDO) for Daisy-Chaining Additional Packages.

digital interface. The data word clocked into the serial-input register (SDI) consists of 12 bits; the first four determine the address of the DAC register to be loaded with the 8 data-bits. A serial data output pin at the other end of the shift register (SDO) allows simple daisy-chaining in multiple DAC applications without additional external decoding logic (Figure 5). The fourth address bit, which decodes as a NOP for the package, makes it possible to select a single DAC in one of the packages to be updated when all the packages receive the common LD DAC strobe signal.

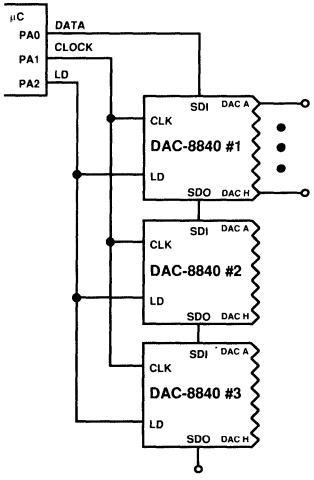


Figure 5. DAC-8840s in a Serial Daisy Chain Minimize Chip Decoders.

The DAC-8841, a mask option of the DAC-8840, offers an ideal octal DAC for +5-V single-supply applications. The DAC and amplifier of each channel are configured as shown in Figure 6, with the amplifier connected for a non-inverting gain of two. This configuration is a 2-quadrant multiplying arrangement with a 1-MHz bandwidth. AC signals applied to the V_{IN} terminal can be attenuated to zero or amplified by a factor of up to two, with 256 possible level settings from zero to 2 × (255/256) V_{IN}:

$$V_{OUT}(D) = 2 \times (D/256) \times (V_{IN} - V_{REFL}) + V_{REFL}$$

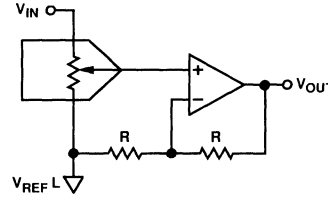


Figure 6. Internal Connections of the +5-V-only DAC-8841.

VARIABLE RESISTORS VERSUS TRIMDACS

From the above overview of the DAC-8800 and DAC-8840/41 TrimDACs, we can compare them to mechanically variable resistors (pots), reviewing the strengths and weaknesses of each.

Advantages of TrimDACs over Potentiometers: Better mechanical stability, improved product life, improved temperature coefficients, smaller size; computer control can eliminate technician costs; remote operation, constant output resistance, and low output resistance with low power dissipation.

Advantages of Potentiometers over TrimDACs: Voltage range usually much greater, no separate power supply required, simple human interface, no memory required, no "zipper noise" (the sound heard when using a DAC to adjust audio levels).

Another useful advantage of the potentiometer at present is a nonvolatile memory. That is, in a vibration-free environment, the wiper of the potentiometer stays where it was last set, even with the power off. The TrimDAC™ devices described here do not contain nonvolatile memory; for them, the required memory is generally supplied by system E^2PROM. Since in many of today's systems a low-cost high-density E^2PROM holds system set points for current time, date, mode, parameters and so on, it is an easy matter to share this nonvolatile memory with the TrimDAC calibration set points; they are reloaded at system powerup.

TYPICAL APPLICATIONS

In professional audio equipment, voltage-controlled amplifiers (VCA) are used to set gain, fade, pan and mix signals. The dc control inputs of these VCAs are ideally controlled by the DAC-8800 (Figure 7). The addition of the capacitor at the VCA voltage control port, VC, helps to limit the slew rate, reducing the clicking to a subaudible level. One DAC-8800 can control 8 channels of logarithmically set gain and attenuation levels.

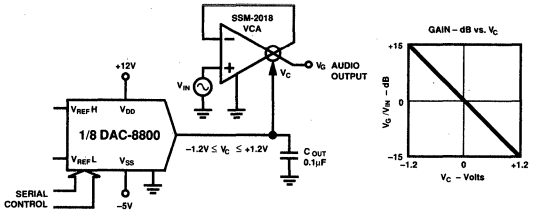


Figure 7. Setting Gain of a Voltage-Controlled Amplifier in Professional Audio Equipment. One DAC-8800 Can Serve 8 Channels. The Damping Capacitor at the Voltage-Control Point Minimizes Zipper Noise by Slowing Rates of Gain Change to Subaudio Frequencies.

Figure 8 shows a selection of output configurations of a DAC-8800, including simple buffers, summing circuits with coarse/fine control, and adding gain for increased output swing. A DAC-8800 can be used in system offset nulling by connecting its output to the summing node of any convenient op amp, using an appropriate value of summing resistance or a T-network.

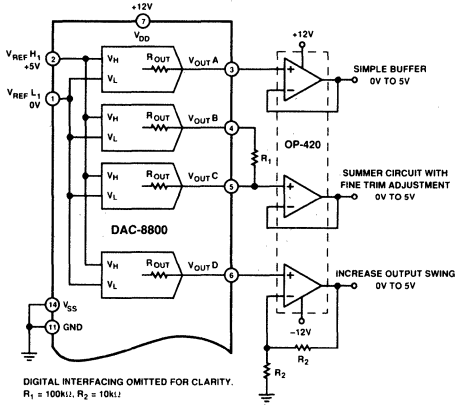


Figure 8. Some Ways of Buffering the DAC-8800 Output.

For video convergence and deflection control, especially in multi-sync displays, the DAC-8840 can be used to adjust the sawtooth waveform amplitudes, their reference bias voltages, and the parabolic waveforms used to linearize them as they are summed together to drive the CRT deflection. Figure 9 shows a block diagram of a typical arrangement.

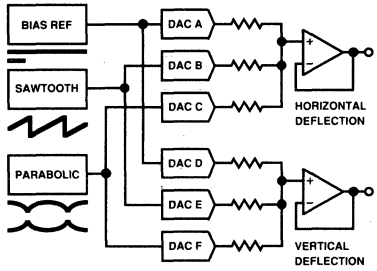


Figure 9. DAC-8840's Four-Quadrant Multiplying Capability Simplifies Amplitude Adjustment of Waveform Components in Video Deflection.

Availability

The 20-pin DAC-8800, and the 24-pin DAC-8840 and DAC-8841 are available for two temperature ranges—extended industrial (−40°C to +85°C) and military (−55°C to +125°C). Packaging includes plastic and ceramic DIPs and SOL surface-mount packages.

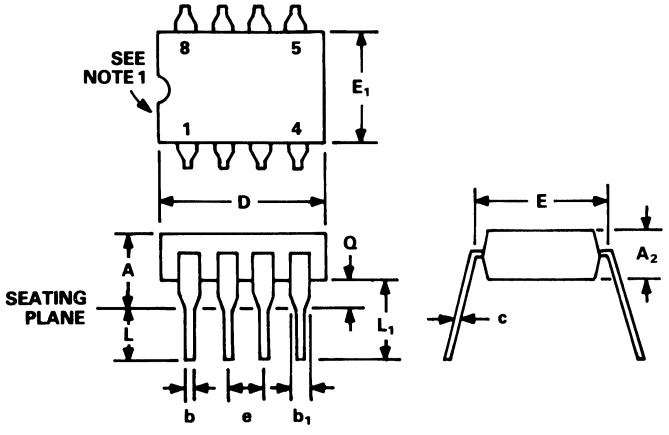
The DAC-8800 was designed by Patrick Copley, who also—with Jim Brubaker—designed the DAC-8840 & DAC-8841 at the Precision Monolithics Division of Analog Devices, Santa Clara, CA.

Package Information
Contents

12

ADI Letter Designator	PMI Letter Designator	Package Description	MIL-M38510 Applicable Configuration	Page
J-Leaded Chip Carrier				
J-28		28-Lead		12-38
Side Brazed DIP (Ceramic)				
D-28A		28-Lead		12-39
Pin Grid Array				
G-68A		68-Lead		12-40
G-100A		100-Lead		12-41
G-223		223-Lead		12-42
Plastic Quad Flat Pack				
P-100		100-Lead		12-43
Ceramic Quad Flat Pack				
Z-100		100-Lead		12-44
Plastic Pin Grid Array				
223		223-Lead		12-45

N-8
8-Lead Plastic DIP

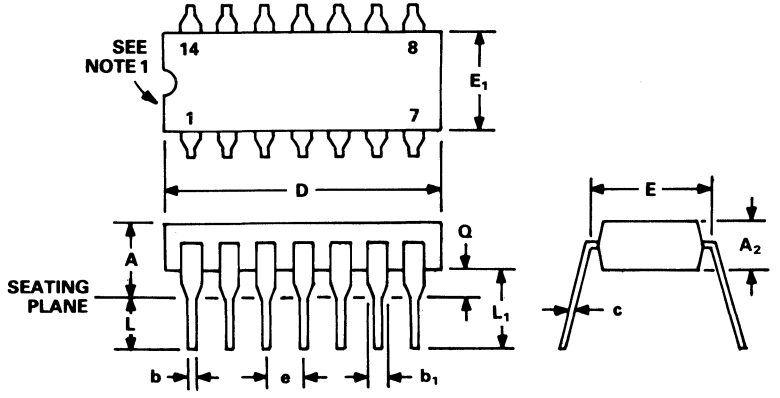


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.348	0.430	8.84	10.92	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

12

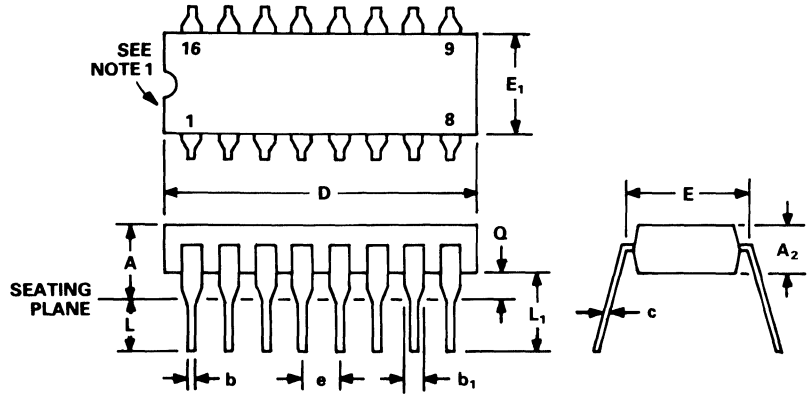
N-14
14-Lead Plastic DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.725	0.795	18.42	20.19	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

N-16
16-Lead Plastic DIP



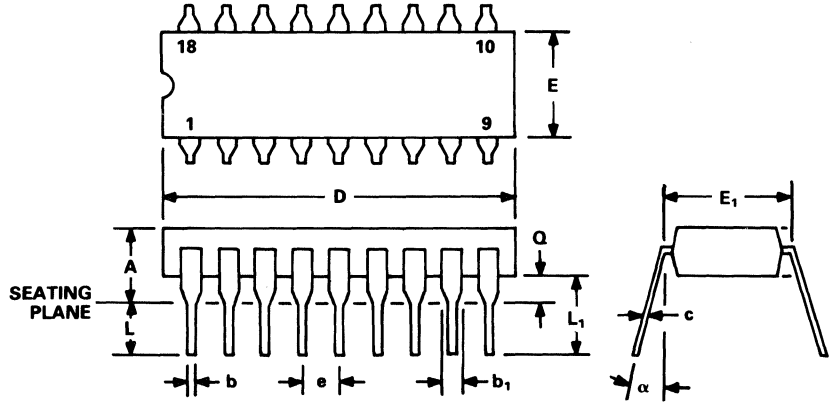
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.745	0.840	18.93	21.33	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

12

18-Lead Epoxy DIP

(P) Suffix

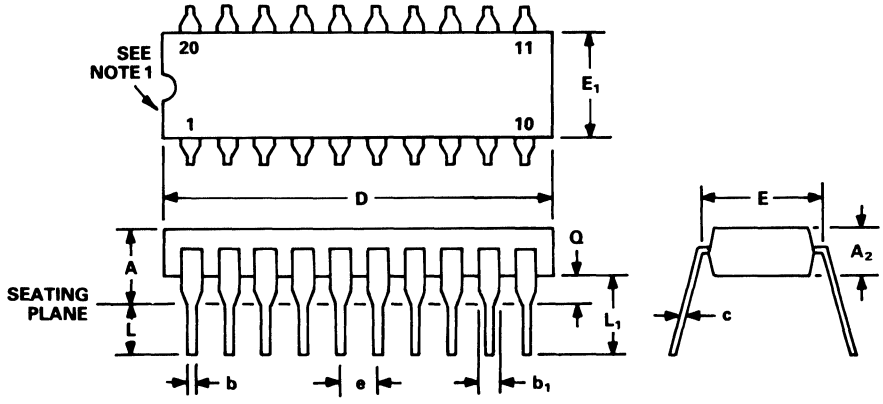


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.20	0.38	
D	0.845	0.925	21.46	23.49	3
E	0.240	0.280	6.10	7.11	3
E_1	0.300	0.325	7.62	8.25	2
e	0.100 BSC		2.54 BSC		
L	0.115	0.160	2.92	4.06	
L_1	0.130		3.30		
Q	0.015		0.38		
α	0°	15°	0°	15°	

NOTES

1. Minor changes in dimensions may occur without advance notice.
2. Dimensions "E_1" to center of leads when formed parallel.
3. D and E dimensions do not include mold flash or protrusion.

N-20
20-Lead Plastic DIP

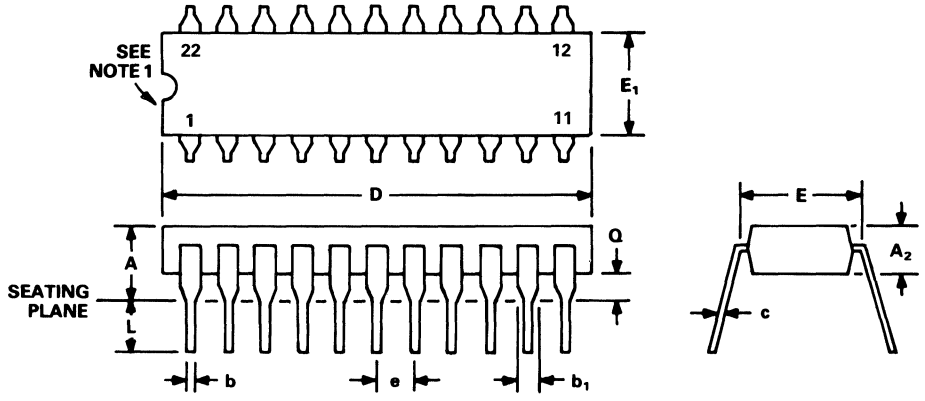


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.925	1.060	23.50	26.90	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

12

22-Pin Plastic DIP

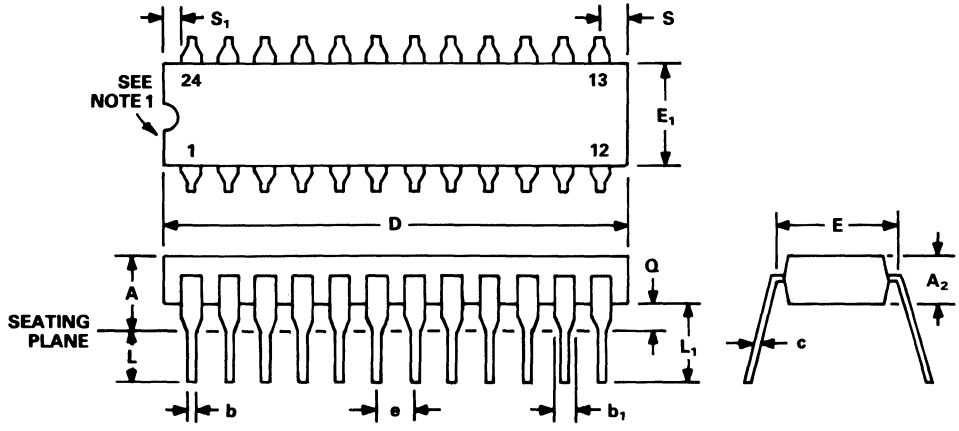


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.210		5.33
A_2	0.115	0.195	2.93	4.95
b	0.014	0.022	0.356	0.558
b_1	0.045	0.070	1.15	1.77
C	0.008	0.015	0.204	0.381
D	1.020	1.080		
E	0.300	0.325	7.62	8.25
E_1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
L	0.115	0.160	2.93	4.06
Q	0.015		0.38	

NOTES

1. **Index area; a notch or a lead one identification mark is located adjacent to lead one.**
2. **The dimension does not include mold flash or protrusions.**

N-24
24-Lead Plastic DIP

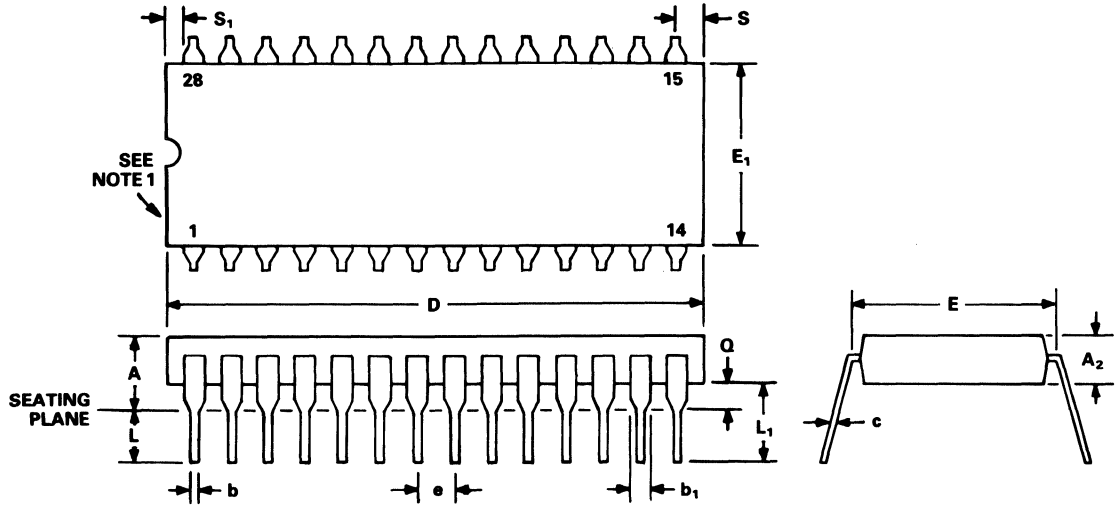


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	1.125	1.275	28.60	32.30	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

12

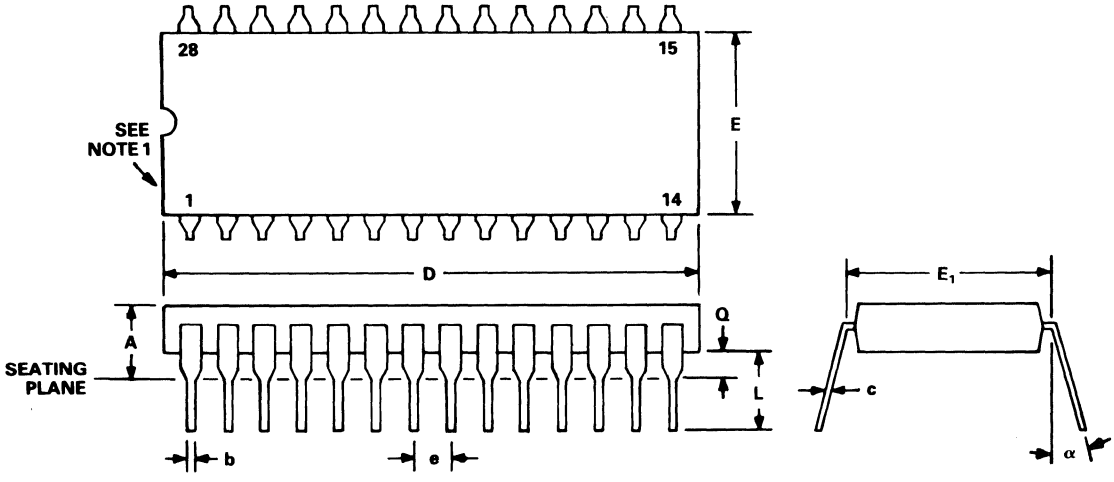
N-28
28-Lead Plastic DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.250		6.35	
A_2	0.125	0.195	3.18	4.95	
b	0.014	0.022	0.356	0.558	
b_1		0.070		1.77	
c	0.008	0.015	0.204	0.381	
D	1.380	1.565	35.10	39.70	2
E	0.600	0.625	15.24	15.87	
E_1	0.485	0.580	12.32	14.73	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

N-28A
28-Pin Plastic DIP

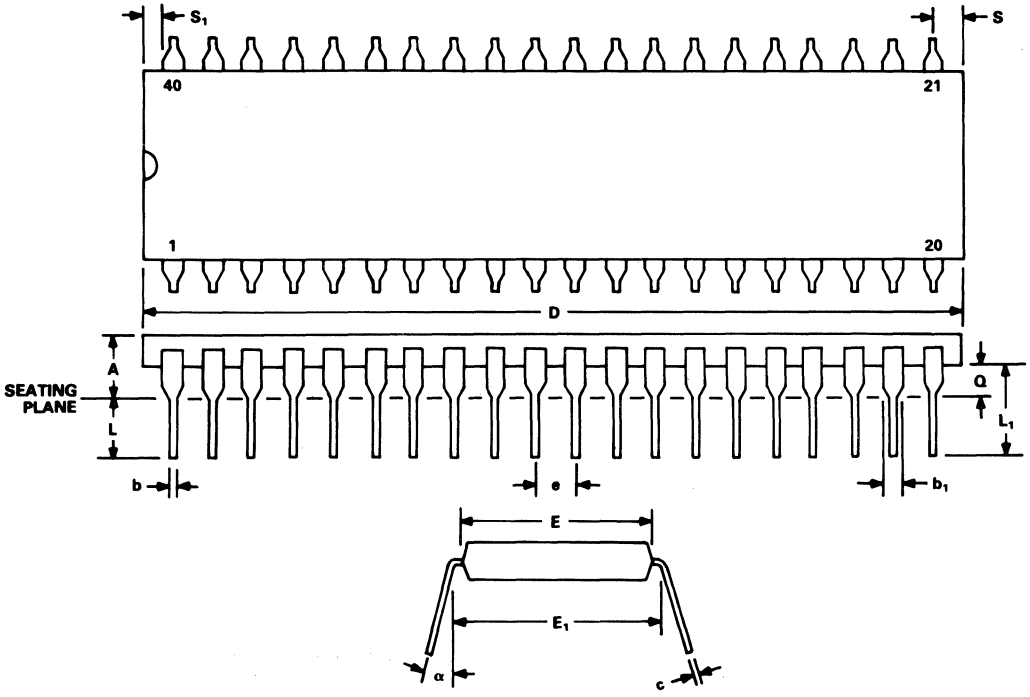


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.200		5.080	
b	0.015	0.020	0.381	0.508	3
c	0.008	0.012	0.203	0.305	3
D	1.440	1.450	35.580	36.830	
E	0.530	0.550	13.470	13.970	
E_1	0.594	0.606	15.090	15.400	2
e	0.096	0.105	2.420	2.670	4
L	0.120	0.175	3.050	4.450	
Q	0.020	0.060	0.560	1.580	
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
3. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
4. Twenty-six spaces.

12

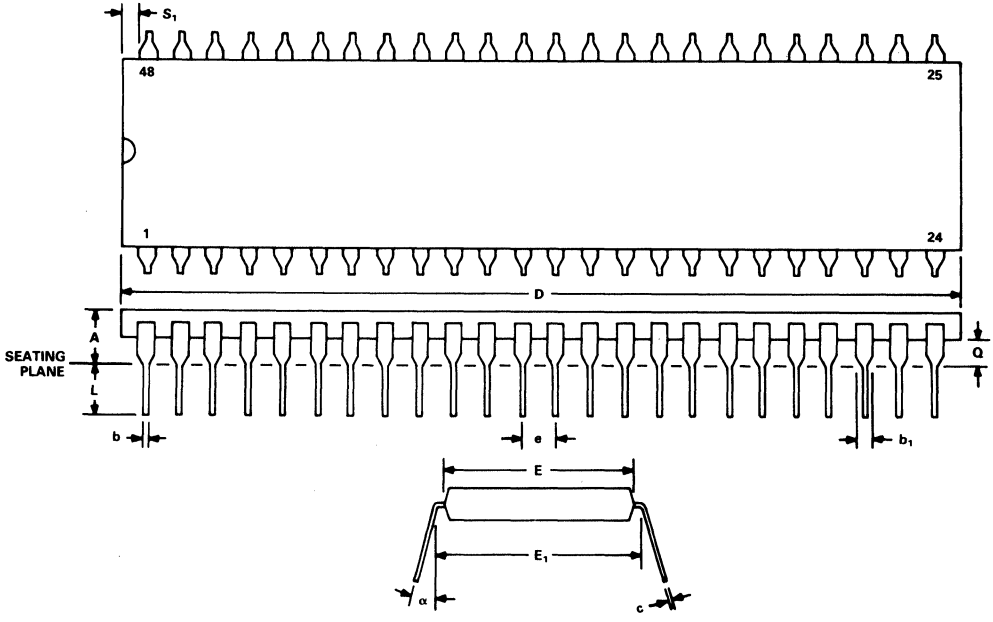
N-40A
40-Pin Plastic DIP



NOTE:
LEADS ARE SOLDER-PLATED KOVAR OR ALLOY 42

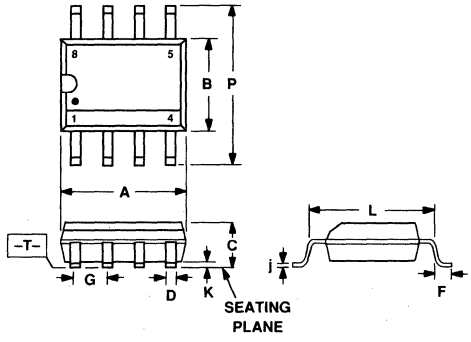
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
b	0.015	0.025	0.38	0.64
b_1	0.040	0.060	1.02	1.52
c	0.008	0.015	0.20	0.38
D	–	2.08	–	52.83
E	0.550	0.550	13.46	13.97
E_1	0.580	0.620	14.73	15.75
e	0.100 BSC		2.54 BSC	
L	0.120	0.175	3.05	4.45
L_1	0.140	–	3.56	–
Q	0.015	0.060	0.38	1.52
S	–	0.110	–	2.79
S_1	0.005	–	0.13	–
α	0°	15°	0°	15°

48-Pin Plastic DIP



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.25		6.35
b	0.014	0.022	0.36	0.59
b_1	0.030	0.070	0.77	1.77
C	0.008	0.015	0.20	0.38
D	2.385	2.480	60.7	63.1
E	0.485	0.580	12.32	14.73
E_1	0.590	0.630	15.0	16.0
e	0.100 BSC		2.54 BSC	
L	0.115	0.200	2.93	5.08
Q	0.015		0.39	
S_1	0.005		0.13	
α	0°	15°	0°	15°

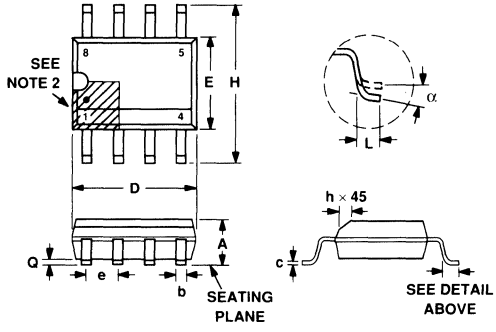
R-8
8-Lead Small Outline (SOIC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.188	0.198	4.77	5.03
B	0.150	0.158	3.81	4.01
C	0.089	0.107	2.26	2.72
D	0.014	0.022	0.36	0.56
F	0.018	0.034	0.46	0.86
G	0.050 BSC		1.27 BSC	
J	0.007	0.015	0.18	0.38
K	0.005	0.011	0.125	0.275
L	0.195	0.205	4.95	5.21
P	0.224	0.248	5.69	6.29

SO-8

8-Lead Narrow-Body SO
(S-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	
b	0.0138	0.0192	0.35	0.49	
c	0.0075	0.0098	0.19	0.25	
D	0.1890	0.1968	4.80	5.00	
E	0.1497	0.1574	3.80	4.00	
H	0.2284	0.2440	5.80	6.20	
e	0.0500 BSC		1.27 BSC		
h	0.0099	0.0196	0.25	0.50	
L	0.0160	0.0500	0.41	1.27	
Q	0.0040	0.0098	0.10	0.25	
α	0°	8°	0°	8°	

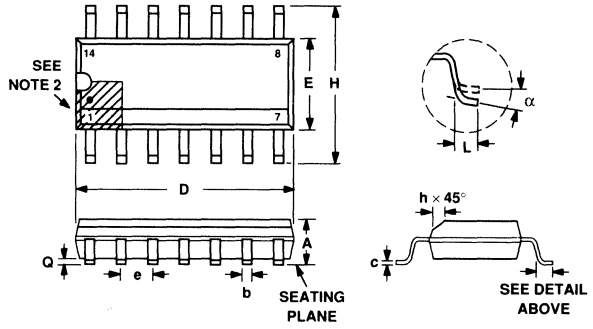
NOTES

1. Package dimensions conform to JEDEC specification MS-012-AA (Issue A, June 1985).
2. Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.

12

SO-14

14-Lead Narrow-Body SO
(S-Suffix)



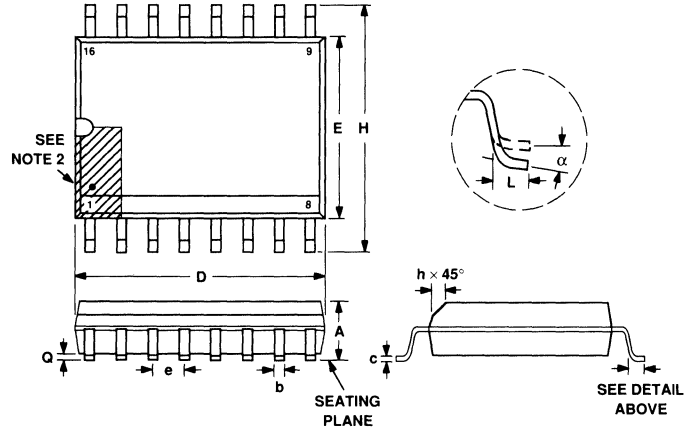
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	
b	0.0138	0.0192	0.35	0.49	
c	0.0075	0.0098	0.19	0.25	
D	0.3367	0.3444	8.55	8.75	
E	0.1497	0.1574	3.80	4.00	
H	0.2284	0.2440	5.80	6.20	
e	0.0500 BSC		1.27 BSC		
h	0.0099	0.0196	0.25	0.50	
L	0.0160	0.0500	0.41	1.27	
Q	0.0040	0.0098	0.10	0.25	
α	0°	8°	0°	8°	

NOTES

1. Package dimensions conform to JEDEC specification MS-012-AB (Issue A, June 1985).
2. Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.

R-16 (S-Suffix)

16-Lead Wide-Body SO
(SOL-16)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	
b	0.0138	0.0192	0.35	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.3977	0.4133	10.10	10.50	
E	0.2914	0.2992	7.40	7.60	
H	0.3937	0.4193	10.00	10.65	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

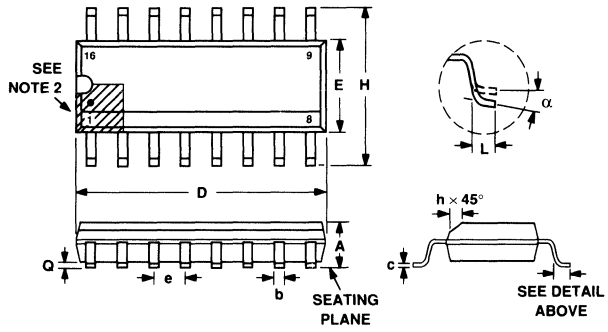
NOTES

1. Package dimensions conform to JEDEC specification MS-013-AA (Issue A, June 1985).
2. Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.

12

R-16A (S-Suffix)

16-Lead Narrow Body SO
(SO-16)



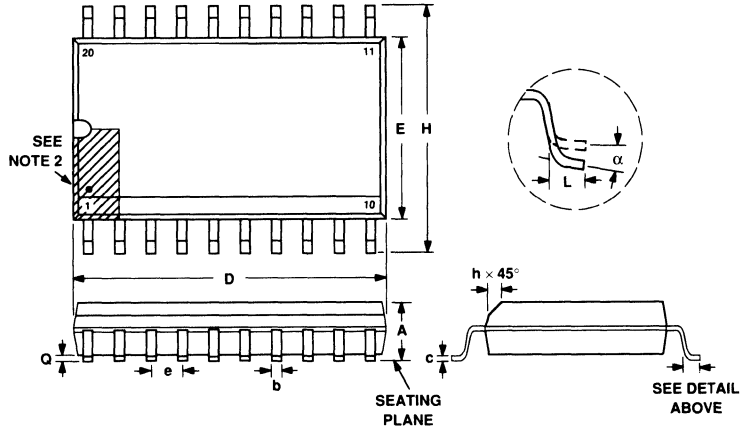
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	
b	0.0138	0.0192	0.35	0.49	
c	0.0075	0.0099	0.19	0.25	
D	0.3859	0.3937	9.80	10.00	
E	0.1497	0.1574	3.80	4.00	
H	0.2284	0.2440	5.80	6.20	
e	0.0500 BSC		1.27 BSC		
h	0.0099	0.0196	0.25	0.50	
L	0.0160	0.0500	0.41	1.27	
Q	0.0040	0.0098	0.10	0.25	
α	0°	8°	0°	8°	

NOTES

1. Package dimensions conform to JEDEC specification MS-012-AC (Issue A, June 1985).
2. Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.

R-20 (S-Suffix)

20-Lead Wide-Body SO
(SOL-20)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	
b	0.0138	0.0192	0.35	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.4961	0.5118	12.60	13.00	
E	0.2914	0.2992	7.40	7.60	
H	0.3937	0.4193	10.00	10.65	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

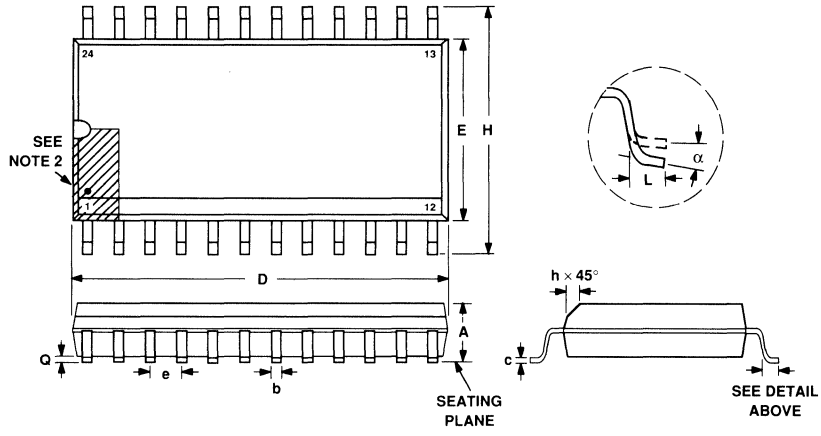
NOTES

1. Package dimensions conform to JEDEC specification MS-013-AC (Issue A, June 1985).
2. Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.

12

R-24 (S-Suffix)

24-Lead Wide-Body SO
(SOL-24)



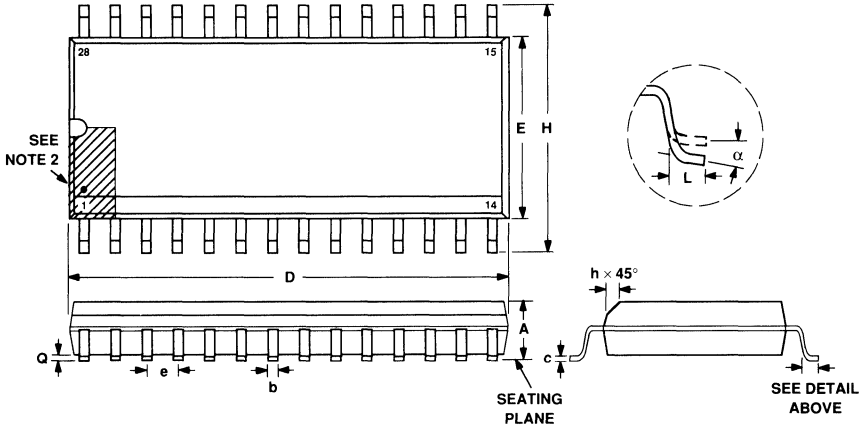
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	
b	0.0138	0.0192	0.35	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.5985	0.6141	15.20	15.60	
E	0.2914	0.2992	7.40	7.60	
H	0.3937	0.4193	10.00	10.65	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

NOTES

1. Package dimensions conform to JEDEC specification MS-013-AD (Issue A, June 1985).
2. Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.

R-28 (S-Suffix)

28-Lead Wide-Body SO
(SOL-28)

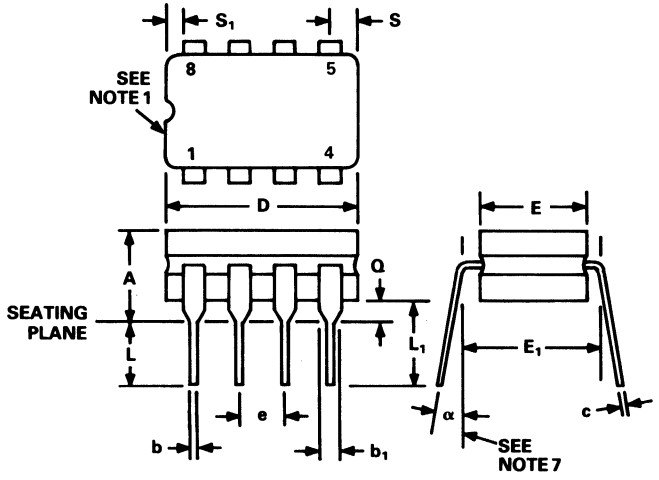


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	
b	0.0138	0.0192	0.35	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.6969	0.7125	17.70	18.10	
E	0.2914	0.2992	7.40	7.60	
H	0.3937	0.4193	10.00	10.65	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

NOTES

1. Package dimensions conform to JEDEC specification MS-013-AE (Issue A, June 1985).
2. Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.

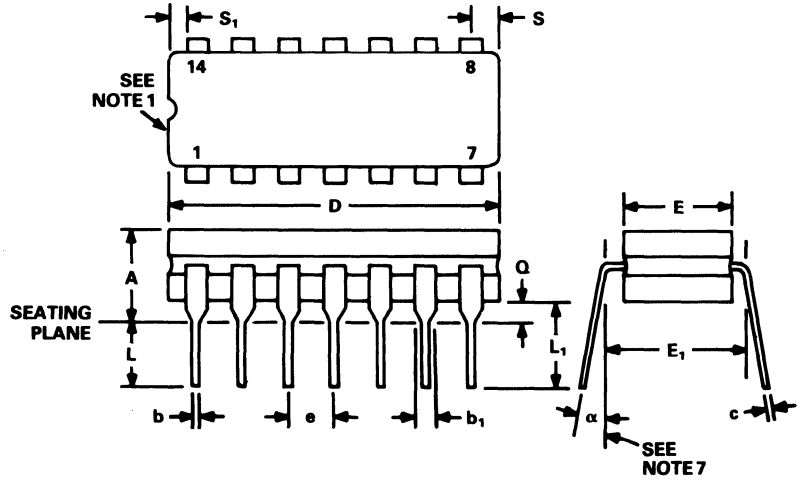
Q-8
8-Lead Cerdip



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		0.405		10.29	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.055		1.35	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Six spaces.

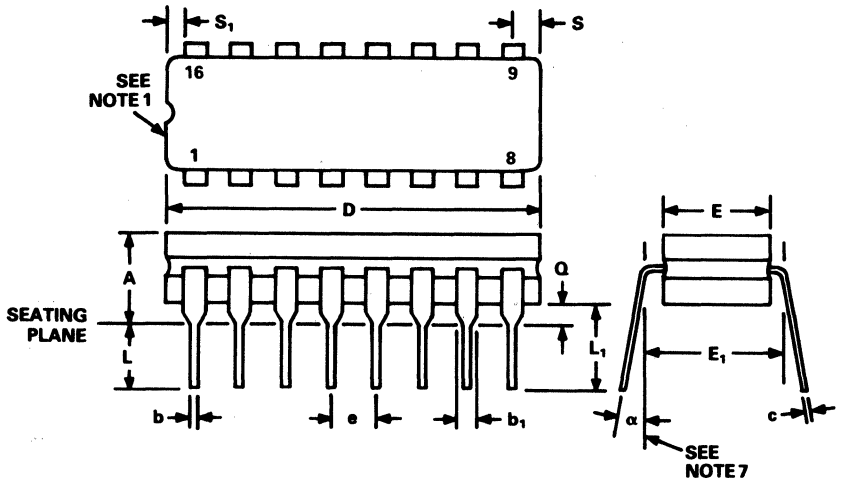
Q-14
14-Lead Cerdip



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		0.785		19.94	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Twelve spaces.

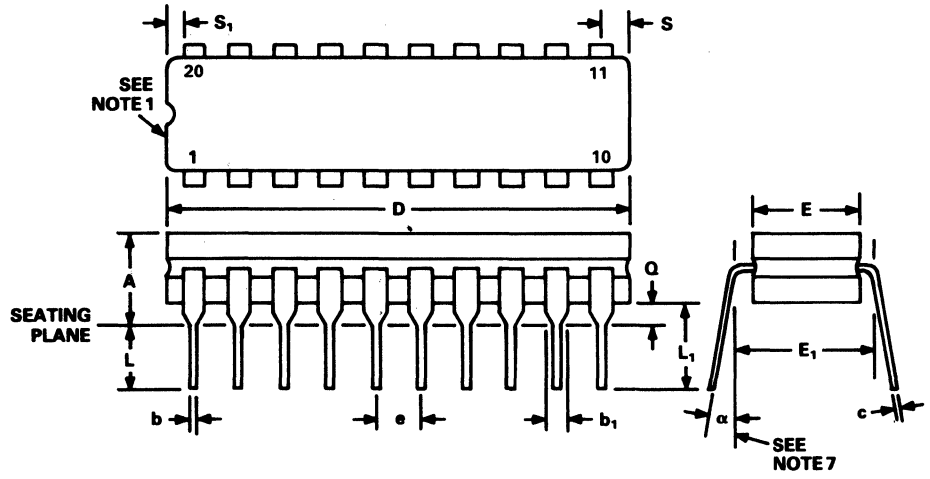
Q-16
16-Lead Cerdip



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		0.840		21.34	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Fourteen spaces.

Q-20
20-Lead Cerdip

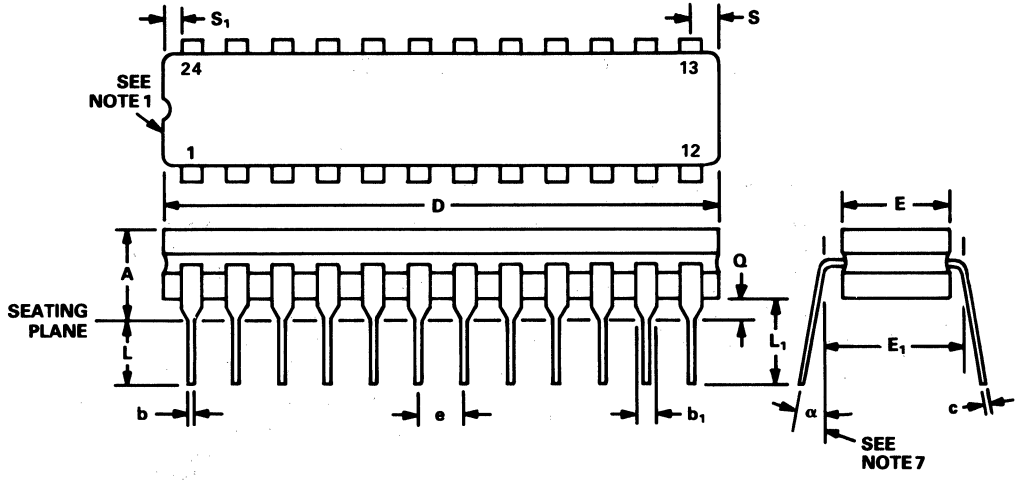


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		1.060		26.92	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	.0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Eighteen spaces.

12

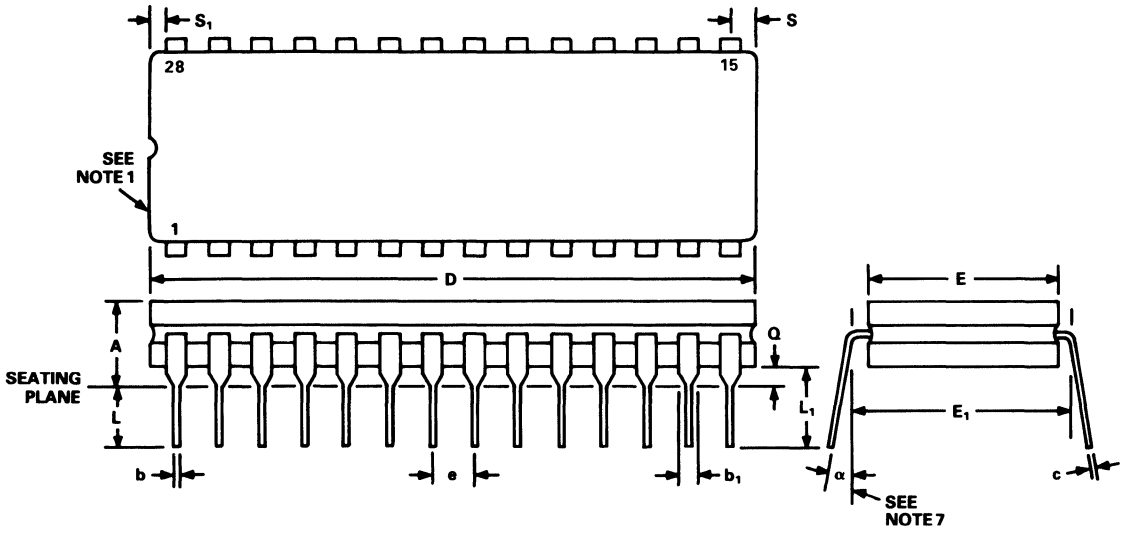
Q-24
24-Lead Cerdip



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		1.280		32.51	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Twenty-two spaces.

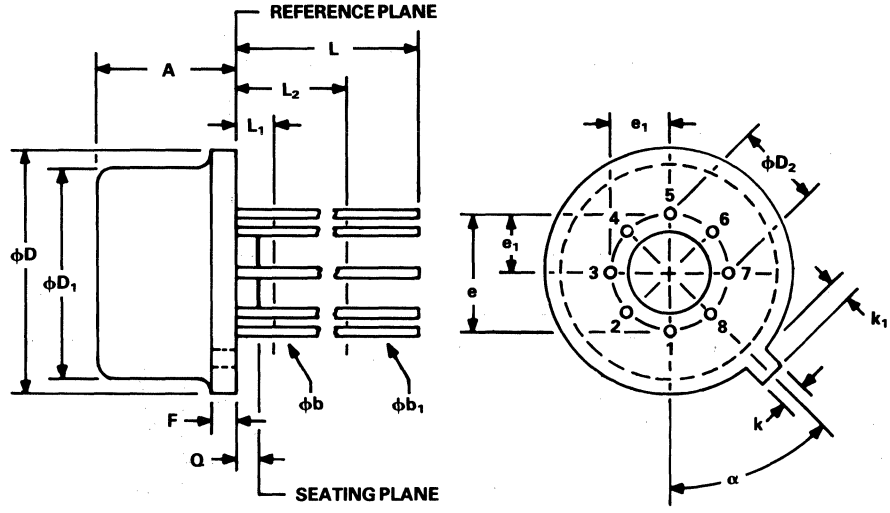
Q-28
28-Lead Cerdip



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.225		5.72	
b	0.014	0.026	0.36	0.66	7
b_1	0.030	0.070	0.76	1.78	2, 7
c	0.008	0.018	0.20	0.46	7
D		1.490		37.85	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015		0.38		3
S		0.100		2.54	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Twenty-six spaces.

H-08A
8-Lead Metal Can (TO-99)

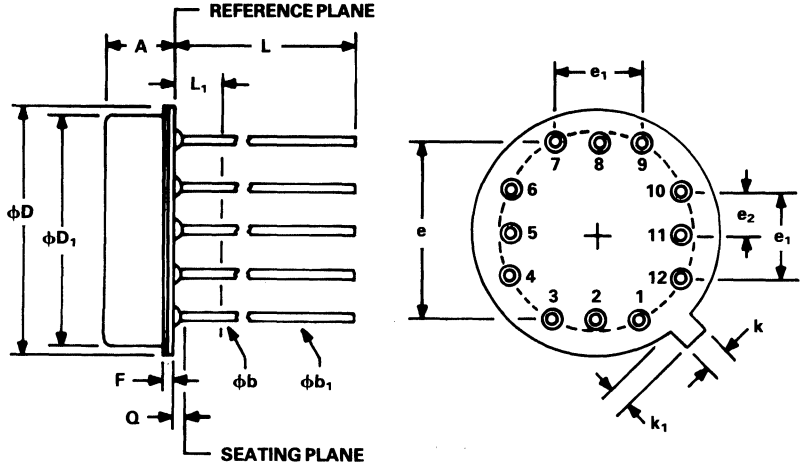


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.019	0.41	0.48	1,4
ϕb_1	0.016	0.021	0.41	0.53	1,4
ϕD	0.335	0.370	8.51	9.40	
ϕD_1	0.305	0.335	7.75	8.51	
ϕD_2	0.110	0.160	2.79	4.06	
e	0.200 BSC		5.08 BSC		3
e_1	0.100 BSC		2.54 BSC		3
F		0.040		1.02	
k	0.027	0.034	0.69	0.86	
k_1	0.027	0.045	0.69	1.14	
L	0.500	0.750	12.70	19.05	
L_1		0.050		1.27	
L_2	0.250		6.35		
Q	0.010	0.045	0.25	1.14	
α	45° BSC		45° BSC		3

NOTES
1. (All leads) ϕb applies between L_1 and L_2. ϕb_1 applies between L_2 and 0.500" (12.70mm) from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter 0.019" (0.48mm) measued in gauging plane 0.054" (1.37mm) + 0.001" (0.03mm) – 0.000" (0.00mm) below the base plane of the product are within 0.007" (0.18mm) of their true position relative to the maximum width tab.
4. All leads – increase maximum limit 0.003" (0.08mm) when hot solder dip finish is applied.

H-12A

12-Lead Metal Can (TO-8 Style)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.148	0.181	3.76	4.60	
ϕb	0.016	0.019	0.41	0.48	1
ϕb_1	0.016	0.021	0.41	0.53	1
ϕD	0.592	0.610	15.04	15.44	
ϕD_1	0.545	0.555	13.84	14.10	
e	0.400 BSC				3
e_1	0.200 BSC				3
e_2	0.100 BSC				3
F		0.040		1.02	
k	0.026	0.036	0.66	0.91	
k_1	0.026	0.036	0.66	0.91	2
L	0.375		9.50		1
L_1		0.050		1.27	1
Q	0.010	0.045	0.25	1.14	

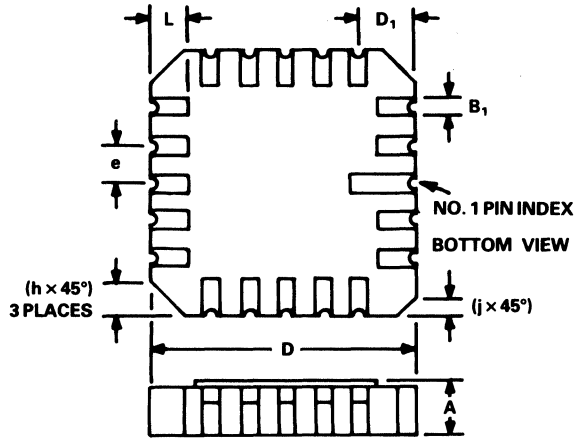
NOTES

1. (All leads) ϕb applies between L and L_1. ϕb_1 applies between L_1 and 0.375" (9.50mm) from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.375" (9.50mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter 0.019" (0.48mm) measued in gauging plane 0.054" (1.37mm) + 0.001" (0.03mm) – 0.000" (0.00mm) below the base plane of the product is within 0.007" (0.18mm) of their true position relative to the maximum width tab.

12

E-20A

20-Terminal Leadless Ceramic Chip Carrier

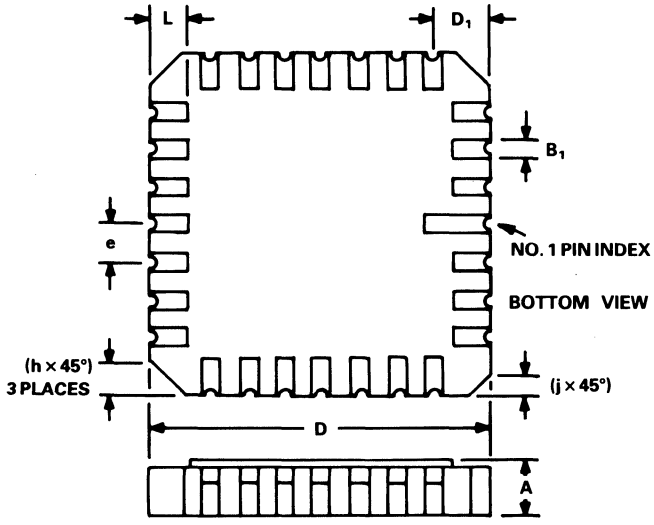


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.100	1.63	2.54	1
B_1	0.022	0.028	0.56	0.71	
D	0.342	0.358	8.69	9.09	2
D_1	0.075 REF		1.91 REF		
e	0.050 BSC		1.27 BSC		
j	0.020 REF		0.51		
h	0.040 REF		1.02		
L	0.045	0.055	1.14	1.40	

NOTES
1. Dimension A controls the overall package thickness.
2. Applies to all 4 sides.
3. All terminals are gold plated.

E-28A

28-Terminal Leadless Ceramic Chip Carrier

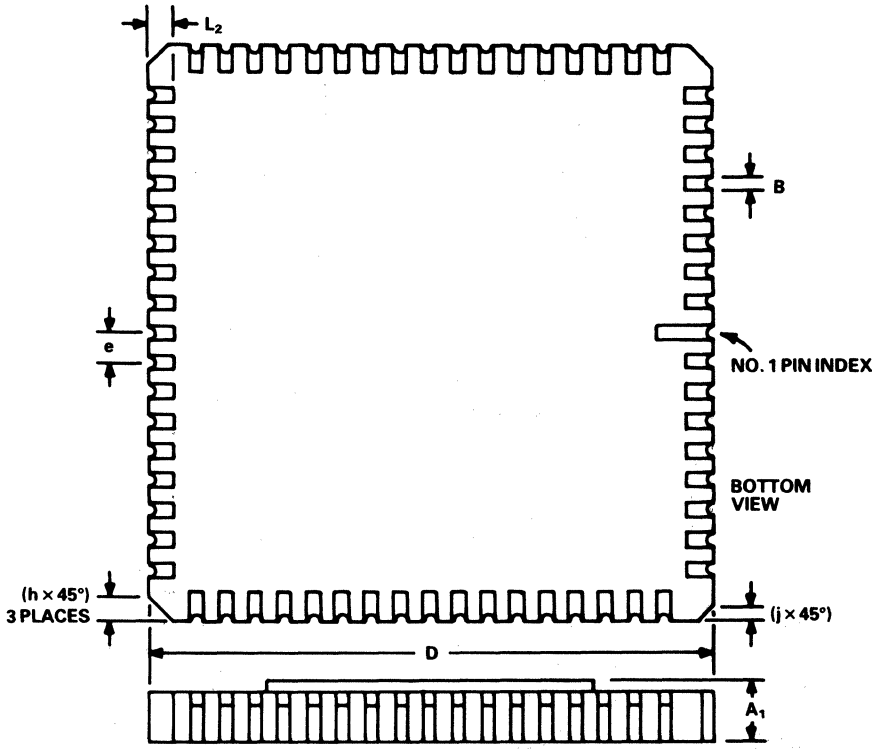


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.100	1.63	2.54	1
B_1	0.022	0.028	0.56	0.71	
D	0.442	0.458	11.23	11.63	2
D_1	0.075 REF		1.91 REF		
e	0.050 BSC		1.27 BSC		
j	0.020 REF		0.51		
h	0.040 REF		1.02		
L	0.045	0.055	1.14	1.40	

NOTES
1. Dimension A controls the overall package thickness.
2. Applies to all 4 sides.
3. All terminals are gold plated.

12

E-68A
68-Terminal Leadless Chip Carrier

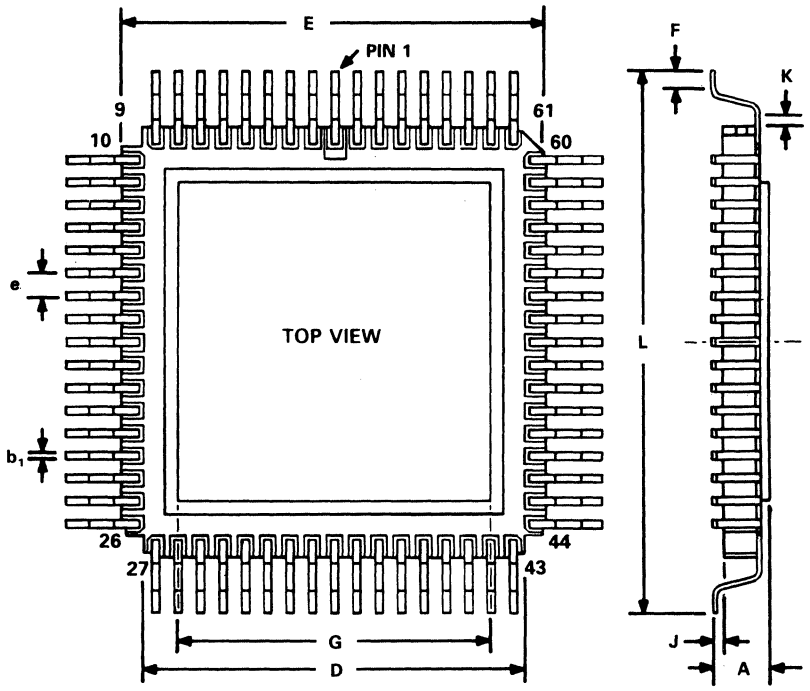


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A_1	0.065	0.103	1.65	2.62	1
B	0.020	0.030	0.51	0.76	
D	0.940	0.965	23.88	24.51	2
e	0.045	0.055	1.14	1.40	
h	0.040 TYP		1.02 TYP		
j	0.020 TYP		0.51 TYP		
L_2	0.045	0.055	1.14	1.40	

NOTES
1. Dimension controls the overall package thickness.
2. Applies to all 4 sides.
3. All terminals are gold plated.

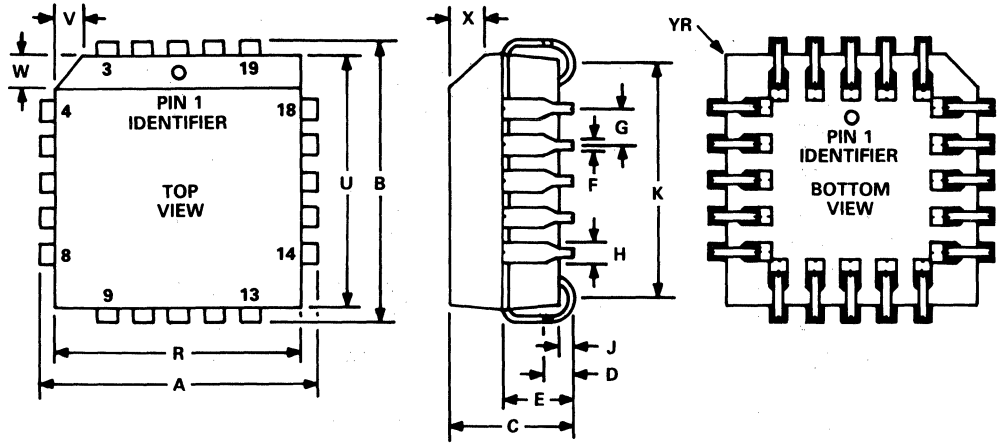
Z-68

68-Lead Leaded Chip Carrier (Ceramic)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.092	0.118	2.337	2.997
b_1	0.016	0.020	0.452	0.462
D	0.841	0.859	21.361	21.819
e	0.050 BSC		1.27 BSC	
E	0.940	0.960	23.876	24.384
F	0.040		1.016	
G	0.695	0.705	17.653	17.907
K	0.025		0.625	
L	1.200	1.220	30.476	30.984

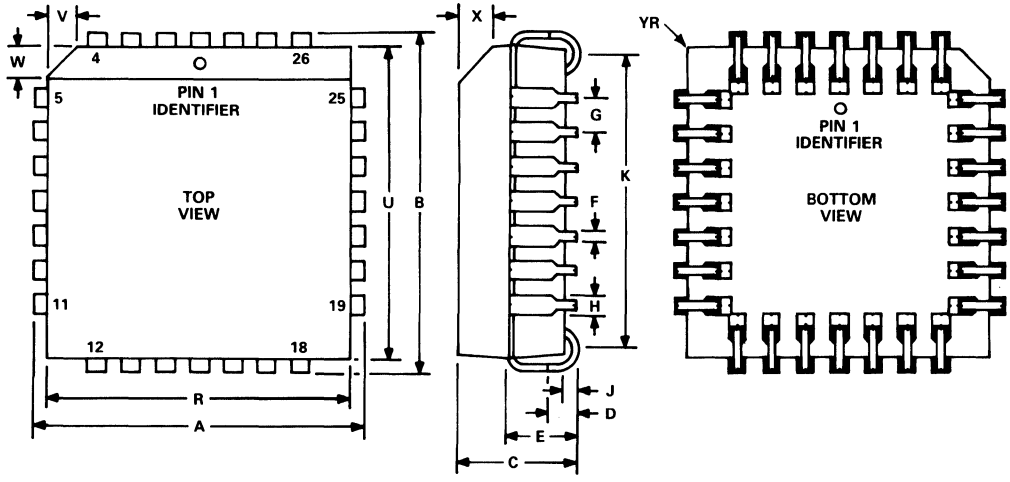
P-20A
20-Lead Plastic Leaded Chip Carrier (PLCC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.02
B	0.385	0.395	9.78	10.02
C	0.165	0.180	4.19	4.57
D	0.025	0.040	0.64	1.01
E	0.085	0.110	2.16	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.015	0.025	0.38	0.63
K	0.290	0.330	7.37	8.38
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50

P-28A

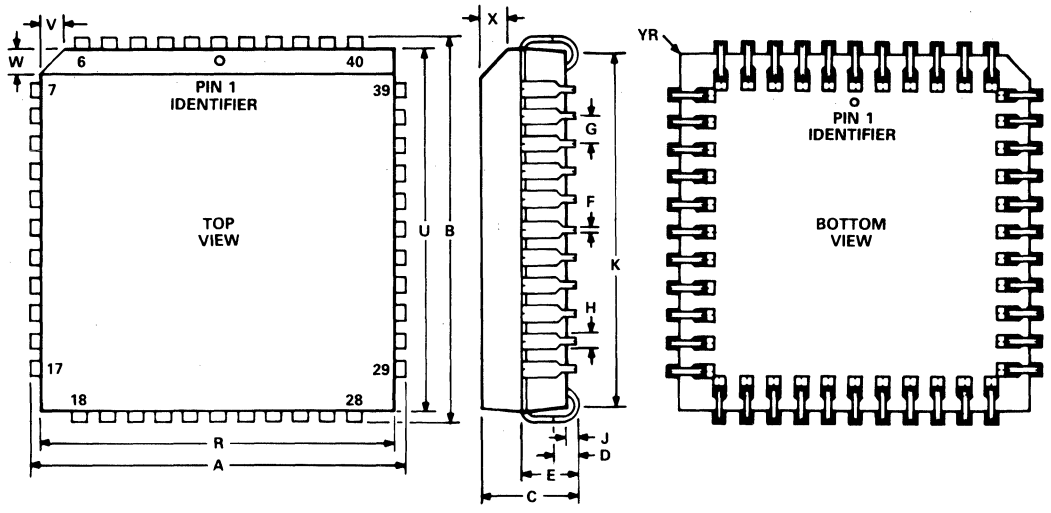
28-Lead Plastic Leaded Chip Carrier (PLCC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.19	4.57
D	0.025	0.040	0.64	1.01
E	0.085	0.110	2.16	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.015	0.025	0.38	0.63
K	0.390	0.430	9.91	10.92
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50

P-44A

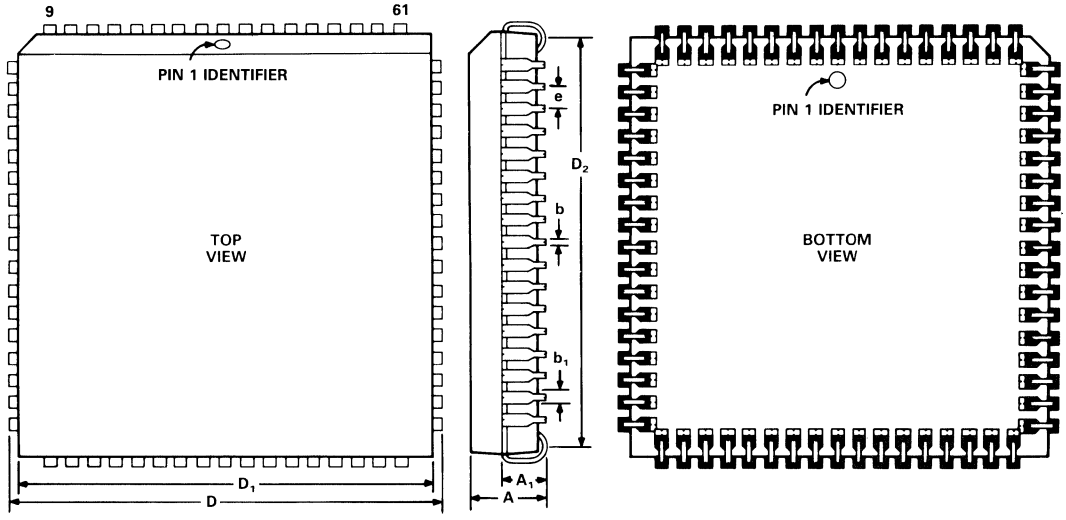
44-Lead Plastic Leaded Chip Carrier (PLCC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.19	4.57
D	0.025	0.040	0.64	1.01
E	0.085	0.110	2.16	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.015	0.025	0.38	0.63
K	0.650	0.656	16.51	16.66
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50

P-68A

68-Lead Plastic Leaded Chip Carrier

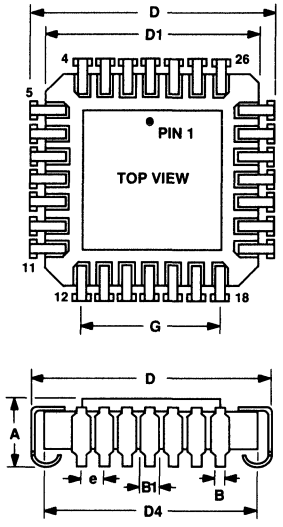


	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.169	0.175	4.29	4.45
A_1	0.104 TYP		2.64 TYP	
b	0.017	0.019	0.43	0.48
b_1	0.027	0.029	0.69	0.74
D	0.885	0.995	22.48	25.27
D_1	0.950	0.954	24.13	24.23
D_2	0.895	0.925	22.73	23.50
e	0.050 TYP		1.27 TYP	

12

J-28

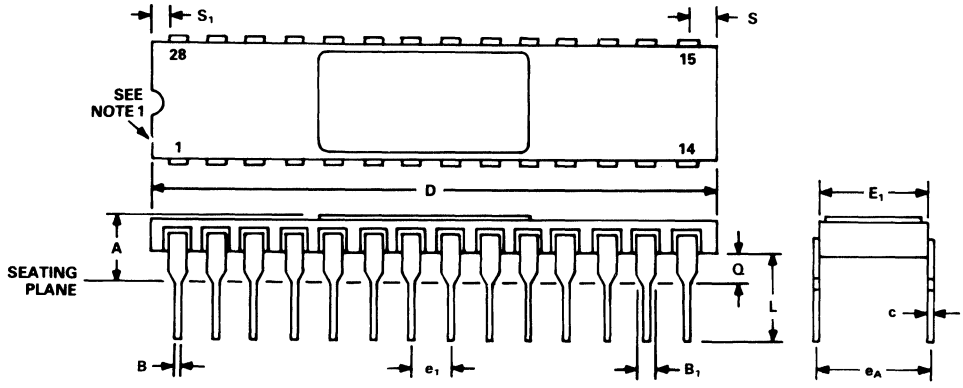
28-Lead J-Leaded Chip Carrier



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.125		3.175
B	0.013	0.021	0.330	0.534
B_1	0.017		0.432	
D	0.489	0.491	12.196	12.704
D_1	0.440	0.460	11.176	11.684
D_4	0.428	0.432	10.412	11.428
e	0.050 BSC		1.27 BSC	
G	0.280	0.310	2.366	2.874

D-28A

28-Lead Side Brazed Ceramic DIP (Single Width)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		1.480		37.59	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	
S_1	0.005		0.13		5

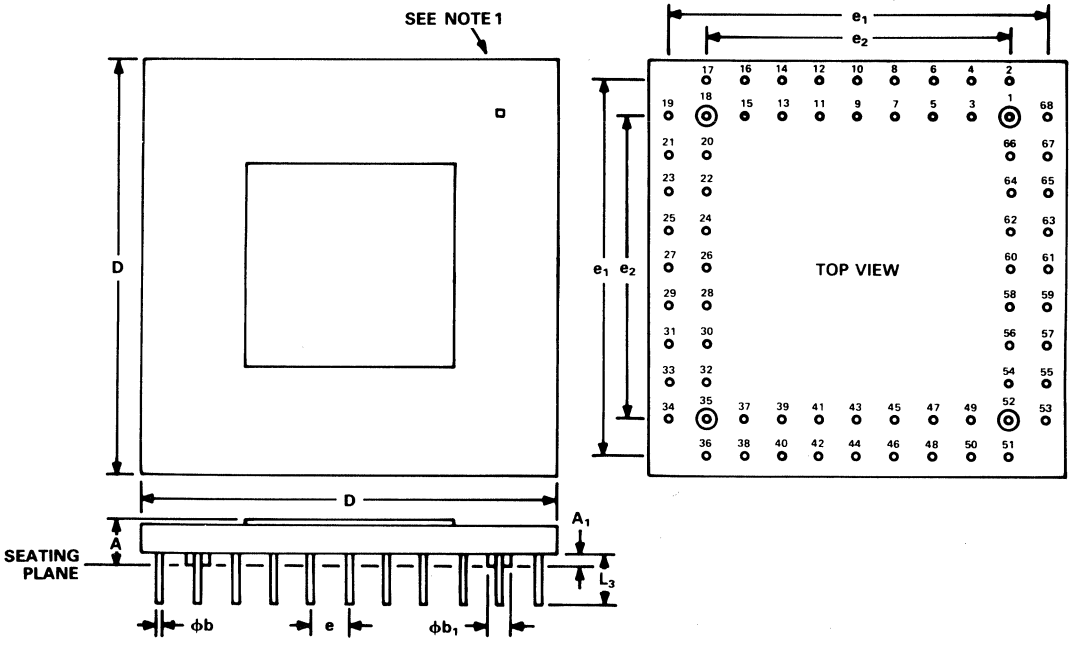
NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Twenty-six spaces.

12

G-68A

68-Pin Grid Array



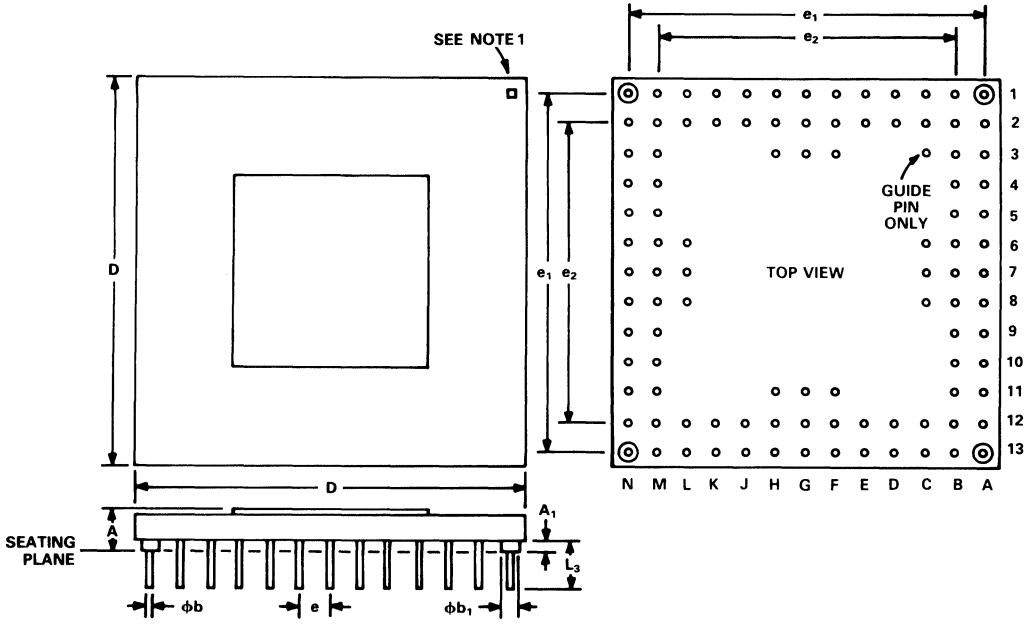
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.123	0.164	3.12	4.17	3
A_1	0.035	0.055	0.89	1.40	3
ϕb	0.016	0.021	0.41	0.53	
ϕb_1	0.045	0.060	1.14	1.52	2
D	1.080	1.110	27.43	28.19	6
e_1	0.988	1.012	25.10	25.70	5
e_2	0.788	0.812	20.02	20.62	5
e	0.095	0.105	2.41	2.67	4
L_3	0.145	0.190	3.68	4.83	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead A1.
2. The minimum limit for dimension ϕb_1 may be 0.023″ (0.58 mm) for all four corner leads only.
3. Dimension shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100″ (2.54 mm) between centerlines.
5. Lead center when α is 0°; e_1 shall be measured at the centerline of the leads.
6. All four sides.

G-100A

100-Pin Grid Array



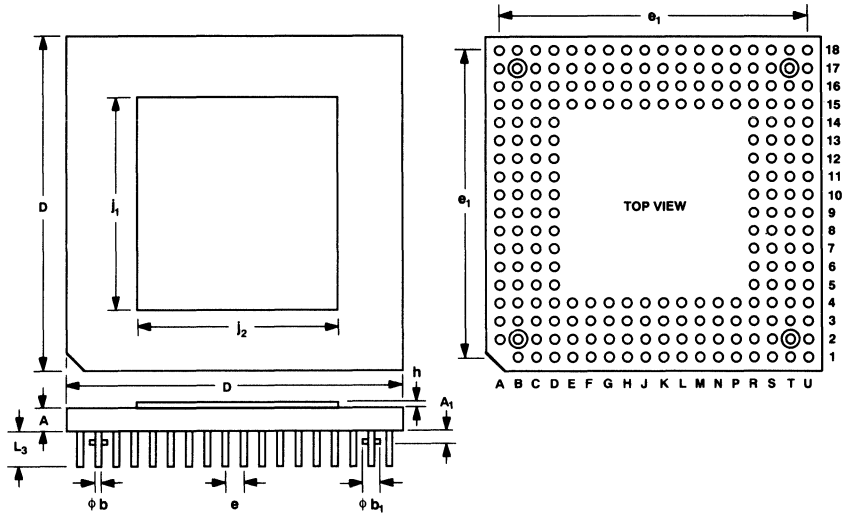
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.169		4.29	3
A_1	0.025	0.055	0.64	1.40	3
ϕb	0.016	0.020	0.41	0.51	
ϕb_1	0.040	0.055	1.02	1.40	2
D	1.308	1.332	33.22	33.83	6
e_1	1.188	1.212	30.18	30.78	5
e_2	0.988	1.024	25.10	26.01	5
e	0.095	0.105	2.41	2.67	4
L_3	0.165	0.190	4.19	4.83	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead A1.
2. The minimum limit for dimension ϕb_1 may be 0.023″ (0.58 mm) for all four corner leads only.
3. Dimension shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100″ (2.54 mm) between centerlines.
5. Lead center when α is 0°; e_1 shall be measured at the centerline of the leads.
6. All four sides.
7. Gold plating a minimum of 50μ inches over 100μ inches ref. Thickness of nickel.

12

223-Pin Ceramic Pin Grid Array

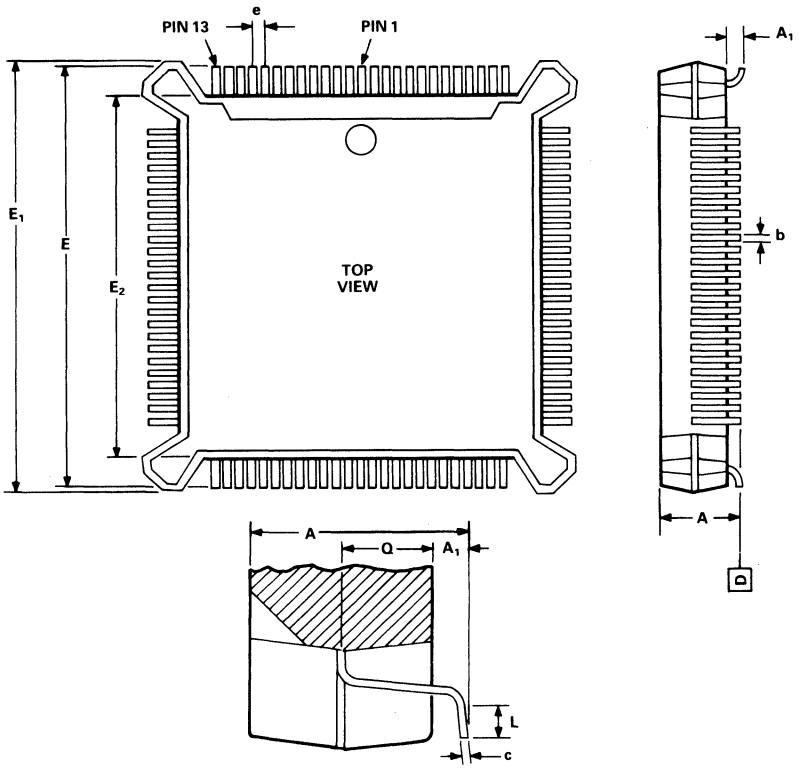


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.073	0.089	1.86	2.26
A_1	0.045	0.055	1.14	1.40
ϕb	0.018 TYP		0.46 TYP	
ϕb_1	0.050 TYP		0.27 TYP	
D	1.844	1.876	46.84	47.64
e_1	1.700 TYP		43.18 TYP	
e	0.100 TYP		2.54 TYP	
L_3	0.174	0.186	4.42	4.72
h	0.020 TYP		0.500 TYP	
j_1	1.209	1.225	30.71	31.91
j_2	1.134	1.150	28.80	29.20

NOTE
When socketing the CPGA Package, use of a low insertion force socket is recommended.

P-100

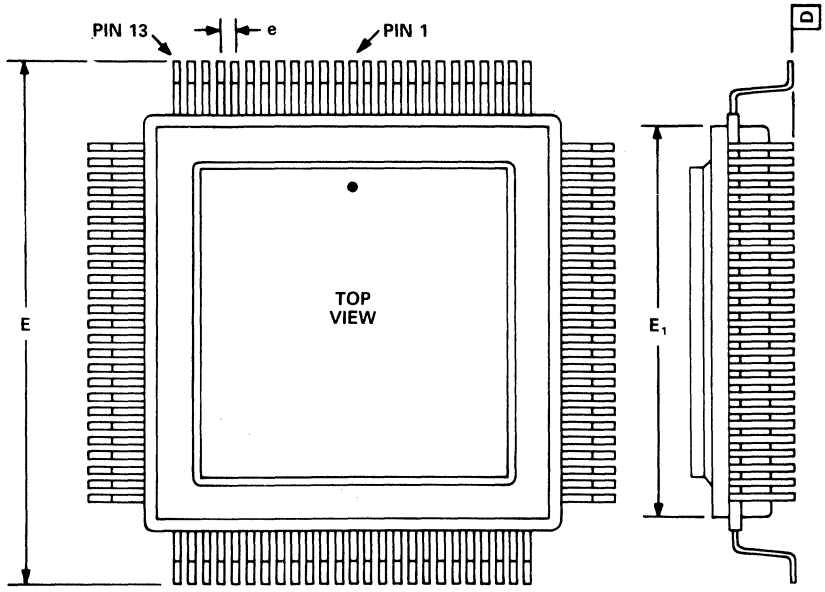
100-Lead Plastic Quad Flat Pack

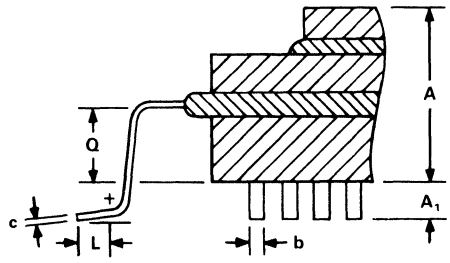


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.160	0.180	4.06	4.57
A_1	0.020	0.040	0.51	1.02
b	0.010	0.013	0.25	0.33
c	0.006	0.008	0.15	0.20
E	0.875	0.885	22.23	22.48
E_1	0.897	0.903	22.78	22.94
E_2	0.747	0.753	18.97	19.13
e	0.020	0.030	0.51	0.76
L	0.020	0.030	0.51	0.76
Q	0.065	0.075	1.65	1.91
⌭		0.008		0.20

Z-100

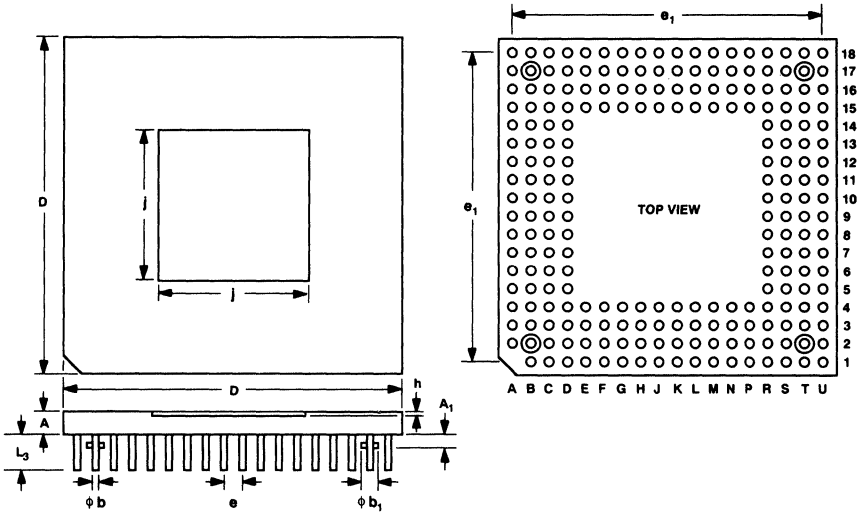
100-Lead Ceramic Quad Flat Pack





SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.114	0.174	2.91	4.41
A_1	0.020	0.040	0.51	1.02
b	0.008	0.013	0.20	0.33
c	0.004	0.006	0.10	0.15
E	0.875	0.885	22.23	22.48
E_1	0.660	0.700	16.76	17.78
e	0.023	0.027	0.58	0.69
L	0.020	0.030	0.51	0.76
Q	0.055	0.075	1.40	1.91
D		0.008		0.20

223-Pin Plastic Pin Grid Array



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.065	0.089	1.65	2.25
A_1	0.065	0.077	1.65	1.95
ϕb	0.0164	0.0196	0.42	0.50
ϕb_1	0.046	0.054	1.17	1.37
D	1.856	1.864	47.14	47.34
e_1	1.688	1.712	42.88	43.48
e	0.088	0.112	2.24	2.84
L_3	0.197 TYP		5.0 TYP	
h	0.012	0.020	0.3	0.5
j	0.803	0.811	20.4	20.6

NOTE
When socketing the PPGA package, use of a low insertion force socket is recommended.

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Appendix Contents

13

Ordering Guide

INTRODUCTION

This Ordering Guide should make it easy to order Analog Devices products, whether you're buying one IC op amp, a multi-option subsystem, or 1000 each of 15 different items. It will help you:

1. Find the correct part number for the options you want.
2. Get a price quotation and place an order with us.
3. Know our warranty for components and subsystems.

For answers to further questions, call the nearest sales office (listed at the back of the book) or our main office in Norwood, Mass. U.S.A. (617-329-4700).

MODEL NUMBERING

In this reference manual many of the data sheets for products having a number of standard options contain an Ordering Guide. Use it to specify the correct part number for the exact combination of options you want. Two model numbering schemes are used by Analog Devices. The first model numbering scheme is used for designating standard Analog Devices monolithic and hybrid products. The second scheme is used by our Precision Monolithics Division (formerly PMI) as designators for its product line.

Figure 1 shows the form of model number used for our proprietary standard monolithic ICs and many of our hybrids. It consists of an "AD" (Analog Devices) prefix, a 3-to-5-digit number,* an alphabetic performance/temperature-range designator and a package designator. One or two additional letters may immediately follow the digits ("A" for second-generation redesigned ICs, "DI" for dielectrically isolated CMOS switches, e.g., AD536AJH, AD7512DIKD).

Figure 2 shows a different numbering scheme used by our Precision Monolithics Division. This numbering scheme starts with a prefix which designates the device type and model number. It is then followed by a suffix consisting of alphabetic designators (as applicable) to indicate additional functional designations or options and packaging options.

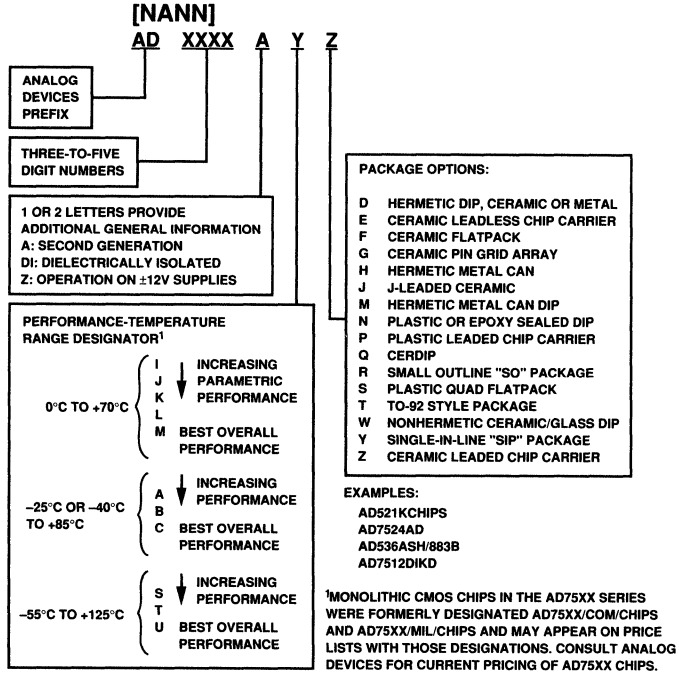

Figure 1. Model-Number Designations for Standard Analog Devices Monolithic and Hybrid IC Products. S, T and U Grades have the Added Suffix, /883B for Devices that Qualify to the Latest Revision of MIL-STD-883, Level B.

***For some models, the combination [digit][letter] [two or three digits] is used instead of ADXXXX, e.g., 2S80.**

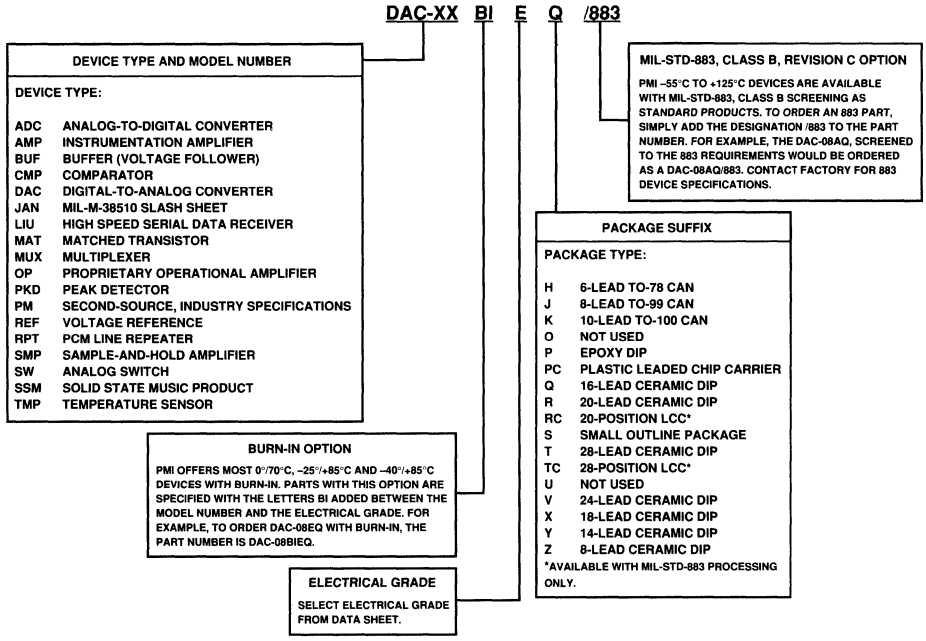

Figure 2. Precision Monolithics Division's Product Designations

ORDERING FROM ANALOG DEVICES

When placing an order, please provide specific information regarding model type, number, option designations, quantity, ship-to and bill-to address. Prices quoted are list; they do not include applicable taxes, customs, or shipping charges. All shipments are F.O.B. factory. Please specify if air shipment is required.

Place your orders with our local sales office or representative, or directly with our customer service group located in the Norwood facility. Orders and requests for quotations may be telephoned, sent via fax or telex, or mailed. Orders will be acknowledged when received; billing and delivery information is included.

Payments for new accounts, where open-account credit has not yet been established, will be C.O.D. or prepaid. Analog Devices' minimum order value is two hundred fifty dollars ($250.00).

When prepaid, orders should include $2.50 additional for packaging and postage (and a 5% sales tax on the price of the goods if you are ordering for delivery to a destination in Massachusetts).

You may also order Analog Devices parts through distributors. For information on distributors, please see pages 13–8 and 13–9 at the back of this volume.

WARRANTY AND REPAIR CHARGE POLICIES

All Analog Devices, Inc., products are warranted against defects in workmanship and materials under normal use and service for one year from the date of their shipment by Analog Devices, Inc., except that components obtained from others are warranted only to the extent of the original manufacturers' warranties, if any, except for component test systems, which have a 180-day warranty, and μMAC and MACSYM systems, which have a 90-day warranty. This warranty does not extend to any products which have been subjected to misuse, neglect, accident, or improper installation or application, or which have been repaired or altered by others. Analog Devices' sole liability and the Purchaser's sole remedy under this warranty is limited to repairing or replacing defective products. (The repair or replacement of defective products does not extend the warranty period. This warranty does not apply to components which are normally consumed in operation or which have a normal life inherently shorter than one year.) Analog Devices, Inc., shall not be liable for consequential damages under any circumstances.

THE FOREGOING WARRANTY AND REMEDY ARE IN LIEU OF ALL OTHER REMEDIES AND ALL OTHER WARRANTIES, WRITTEN OR ORAL, STATUTORY, EXPRESS, OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

Technical Publications

Analog Devices provides a wide array of FREE technical publications. These include Data Sheets, Catalogs, Application Notes and Guides and four serial publications: *Analog Productlog*, a digest of new-production information; *DSPatch*™, a newsletter about digital signal-processing (applications); *Analog Briefings*®, current information about products for military/avionics and the status of reliability at ADI; and *Analog Dialogue*, our technical magazine, with in-depth discussions of products, technologies and applications.

In addition to the free publications, a group of technical reference books are available at reasonable cost. Subsystem products are supported with hardware, software, and user documentation, at prices related to content.

Brief descriptions of typical publications appear below. For copies of any items, to subscribe to any of our free serials or to request any other publications, please get in touch with Analog Devices or the nearest sales office.

CATALOGS

Data Acquisition Products Databooks. Contain selection guides, data sheets and other useful information about all Analog Devices ICs, hybrids, modules and subsystem components recommended for new designs. The current series consists of:

DATA CONVERTER REFERENCE MANUAL—1992: Volumes 1 and 2. Data sheets and selection guides on A/D and D/A Converters, V/F and F/V Converters, Synchro/Resolver-to-Digital Converters, Sample/Track-Hold Amplifiers, Switches and Multiplexers, Voltage References, Data-Acquisition Subsystems, Analog I/O Ports, Communications Products, Bus Interface and I/O Products, Application-Specific ICs, Digital Panel Meters, Power Supplies. (Available FREE)

LINEAR PRODUCTS DATABOOK—1990/1991. Data Sheets and Selection Guides on Op Amps, Instrumentation Amplifiers, Isolators, RMS-to-DC Converters, Multipliers/Dividers, Log/Antilog Amplifiers, Comparators, Temperature-Measuring Components and Transducers, Special Function Components, Digital Panel Instruments, Signal-Conditioning Components and Subsystems, Mass Storage Components, ATE Components, Automotive Components, Bus Interface and Serial I/O Products, Application Specific ICs. (Available FREE.)

AUDIO/VIDEO REFERENCE MANUAL—SSM Audio Products from ADI's PMI Division: VCAs, Surround-Sound Decoder, Audio Preamplifiers, Audio Switches, Line Driver/Receiver, Audio Op Amps, Matched Transistors, Level Detection System, Voltage-Controlled Filters, Log Conversion Amplifier, Multiplexed Sample/Hold, plus 19 Application Notes.

MILITARY PRODUCTS DATABOOK—1990 (in two volumes) Information and data on products available with processing in accordance with MIL-STD-883.

Volume 2: PMI Division products—including Class S
Volume 1: All other Analog Devices products

DATA-ACQUISITION AND CONTROL CATALOG—1990. Tutorial and Configuration Guide, with Product Reference and Index. Bus-Compatible I/O Boards for: IBM PS/2,* IBM PC/XT/AT,* STD Bus, VMEbus, MULTIBUS.† Distributed I/O Subsystems—fixed-function front ends, programmable units, and distributed control systems. Modular Signal Conditioners—analog and digitizing. Analog Signal-Conditioning Panels—isolated and nonisolated. Digital Subsystems—16- and 24/32-channel. Software—DOS drivers and applications packages.

POWER SUPPLIES‡–Linear Supplies•DC-DC Converters. 12-page Short-Form Catalog listing AC/DC Power Supplies, Modular DC/DC Converters, Power-Supply Test Procedures, Transients, Thermal Derating, Mechanical Outlines of Packages and Sockets.

APPLICATION NOTES

Available individually upon request:

A/D Converters

"AD671 12-Bit, 2-MHz ADC Digitizes CCD Outputs for Imaging Applications" [E1455]
"AD7672 Converter Delivers 12-Bit 200-kHz Sampling Systems" [E1313]
"Asynchronous Clock Interfacing with the AD7878" [E1334]
"Bipolar Operations with the AD7572" [E1010]
"Evaluation Board for the AD7701/AD7703 Sigma-Delta A/D Converters" [E1483]
"FIFO Operation and Boundary Conditions in the AD1332 and AD1334" [E1355]
"How to Obtain the Best Performance from the AD7572" [E1038]
"Implement Infinite Sample-and-Hold Circuits Using Analog Input/Output Ports" [E1359]
"Simple Circuit Provides Ratiometric Reference Levels for AD782X Family of Half-Flash ADCs" [E1412]
"Simultaneous and Independent Sampling of Analog Signals with the AD1334" [E1358]
"The AD7574 Analog-to-Microprocessor Interface" [E694]
"Using Multiple AD1334s in Many-Channel Synchronous Sampling Applications" [E1435]

Amplifiers

"A Balanced-Input High-Level Amplifier" [AN-112]
"Active Feedback Improves Amplifier Phase Accuracy" [AN-107]
"AD9617/AD9618 Current-Feedback Amplifier Macro-Models" [E1460]
"An IC Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change" [AN-202]
"An Ultralow-Noise Preamplifier" [AN-136]
"An Unbalanced Virtual-Ground Summing Amplifier" [AN-113]
"Applications of High-Performance BiFET Op Amps" [E727]
"CMOS DACs and Operational Amplifiers Combine to Build Programmable-Gain Amplifiers" (in 2 parts: I and II) [E1073A and E1110]

"How to Test Basic Operational Amplifier Parameters" [AN-201]
"JFET-Input Amps Are Unrivalled for Speed and Accuracy" [AN-108]
"Low-Cost Two-Chip Voltage-Controlled Amplifier and Video Switch" (AD539) [AN-213]
"Using the AD9610 Transimpedance Amplifier" [E1097]
"Very Low-Noise Operational Amplifier" (OP-27) [AN-102]

Analog Signal-Processing and Measurement

"A Function Generator and Linearization Circuit Using the AD7569" [E1369]
"Precision Surface Measurements Using the AD2S58" [E1486]
"RMS-to-DC Converters Ease Measurement Tasks" [E1519]
"Understanding and Applying the AD7341/AD7371 Switched-Capacitor Filters" [E1373]

Audio

"A Balanced Mute Circuit for Audio Mixing Consoles" [AN-122]
"A Constant-Power 'Pan' Control Circuit for Microphone Audio Mixing" [AN-123]
"A High-Performance Compandor for Wireless Audio Systems" [AN-133]
"An Automatic Microphone Mixer" [AN-134]
"An Ultralow Noise Preamplifier" [AN-136]
"A Precision Sum and Difference (Audio Matrix) Circuit" [AN-129]
"A Two-Band Audio Compressor/Limiter" [AN-130]
"A Two-Channel Dynamic Filter Noise Reduction System" [AN-125]
"High Performance Stereo Routing Switcher" [AN-121]
"Interfacing Two 16-Bit AD1856 (AD1851) Audio DACs with the Philips SAA7220 Digital Filter" [AN-207]
"Three High-Accuracy RIAA/IEC MC and MM Phono Preamplifiers" [AN-124]

D/A Converters

"AD7528 Dual 8-Bit CMOS DAC" [E757]
"Analog Panning Circuits Provide Almost Constant Output Power" [AN-206]
"Circuit Applications of the AD7226 Quad CMOS DAC" [E873]
"CMOS DACs and Operational Amplifiers Combine to Build Programmable-Gain Amplifiers" (in 2 parts: I and II) [E1073A and E1110]
"Dynamic Performance of CMOS DACs in Modem Applications" [E1172]
"8th Order Programmable Low-Pass Filter Using Dual 12-Bit DACs" [AN-209]
"Exploring the AD667 12-Bit Analog Output Port" [E875]
"14-Bit DACs Maintain High Performance Over Extended Temperature Range" [E987]
"Gain Error and Tempco of CMOS Multiplying DACs" [E630C]
"Generate 4 Channels of Analog Output Using AD7542 12-Bit D/A Converters and Control the Lot with Only Two Wires" [E909]
"Interfacing the AD7549 Dual 12-Bit DAC to the MCS-48 and MCS-51 Microcomputer Families" [E941]
"Replacing the AD1145 with the AD7846" [E1467]
"Simple Interface Between D/A Converter and Microcomputer Leads to Programmable Sine-Wave Oscillator" (AD7542) [E889]
"The AD7224 DAC Provides Programmable Voltages Over Varying Ranges" [E910]
"Three-Phase Sine-Wave Generation Using the AD7226 Quad DAC" [E924]
"Understanding and Preventing Latchup in CMOS DACs" [AN-109]
"Voltage Adjustment Applications of the DAC-8800 TrimDAC™, an Octal 8-Bit D/A Converter" [AN-142]

Digital Signal-Processing

"Considerations for Selecting a DSP Processor" (ADSP-2100A vs. TMS320C25) [E1306]
"Considerations for Selecting a DSP Processor" (ADSP-2101 vs. WE DSP16A) [E1446]
"Considerations for Selecting a DSP Processor" (ADSP-2101 vs. TMS320C50) [E1558]
"Implement a Cache Memory in Your Word-Slice® System" [E1062]
"Sharing the Output Bus of the ADSP-1401 Microprogram Sequencer" [E1059]
"Using Digitally Programmable Delay Generators" [E1518a]
"Variable-Width Bit Reversing with the ADSP-1410 Address Generator" [E1061]

Disk-Drive Electronics

"Microstepping Drive Circuits for Single Supply Systems" [E1229A]
"Simple DAC-Based Circuit Implements Constant Linear Velocity (CLV) Motor Speed Control" [E1236]

Modelling

"AD9617/AD9618 Current-Feedback Amplifier Macro-Models" [E1460]
"OP-42 Advanced SPICE Macro-Model" [AN-117]
"OP-64 Advanced SPICE Macro-Model" [AN-110]
"OP-260 Advanced SPICE Macro-Model" [AN-126]
"OP-400 SPICE Macro-Model" [AN-120]
"OP-470 SPICE Macro-Model" [AN-132]
"SPICE-Compatible Op Amp Macro-Models" [AN-138]

Power Supply

"A Low-Voltage Power Supply Watchdog Monitor Circuit" [AN-139]

Practice

"An IC Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change" [AN-202]
"How to Reliably Protect CMOS Circuits Against Power-Supply Overranging" [C1499]

Repeater Circuits

"Improved T148 (CEPT) PCM Repeater for #22AWG (0.7mm) Unshielded Twisted-Pair Wire" [AN-119]

Resolver (Synchro) to Digital Conversion

"Circuit Applications of the 2S81 and 2S80 Resolver-to-Digital Converters" [E1140]

"Dynamic Characteristics of Tracking Converters" [E1141]
"Dynamic Resolution-Switching on the 1S74 Resolver-to-Digital Converter" [E919]
"Using the 2S80 Series Resolver-to-Digital Converters with Synchros: Solid-State Scott-T Circuit" [E1361]
"Why the Velocity Output of the 1S74 and 1S64 Series R/D Converters is Continuous and Step-Free Down to Zero Speed" [E893]

Sample-Holds

"Applying IC Sample-Hold Amplifiers" [E931]
"Generate 4 Channels of Analog Output Using AD7542 12-Bit D/A Converters and Control It All with Only Two Wires" [E909]
"Implement Infinite Sample-and-Hold Circuits Using Analog Input/Output Ports" [E1359]

Switches and Multiplexers

"ADG201A/202A and ADG221/222 Performance with Reduced Power Supplies" [E1052]
"Bandwidth, OFF Isolation, and Crosstalk Performance of the ADG5XXAA Multiplexer Series" [E1340]
"Overvoltage Protection for the ADG5XXA Multiplexer Series" [E1237]
"R_{ON} Modulation in CMOS Switches and Multiplexers; What it Is and How to Predict its Effect on Signal Distortion" [E1470]

Temperature Measurement

"A Cost-Effective Approach to Thermocouple Interfacing in Industrial Systems" [E730]
"Use of the AD590 Temperature Sensor in a Remote Sensing Application" [E920]

V/F Converters

"Analog-to-Digital Conversion Using Voltage-to-Frequency Converters" [E994A]
"Operation and Applications of the AD654 IC V-to-F Converter" [E923]
"Using the AD650 Voltage-to-Frequency Converter as a Frequency-to-Voltage Converter" [E1539]

Video Applications

"Animation Using the Pixel Read Mask Register of the ADV47X Series of Video RAM-DACs" [E1316]
"Changing Your VGA Design from a 171/176 to an ADV471" [E1260]
"Design and Layout of a Video Graphics System for Reduced EMI" [E1309]
"Improved PCB Layouts for Video RAM-DACs Can Use Either PLCC or DIP Package Types" [E1225]
"Low Cost Two-Chip Voltage-Controlled Amplifier and Video Switch." (AD539) [AN-213]
"The AD9502 Video Signal Digitizer and Its Applications" [E1173]
"Video Formats & Required Load Terminations." [AN-205]

APPLICATION GUIDES

Analog CMOS Switches and Multiplexers. A 16-page short-form guide to high-speed CMOS switches, CMOS switches with dielectric isolation and CMOS multiplexers. Also included are reliability data and information on single-supply operation.

Applications Guide for Isolation Amplifiers and Signal Conditioners. A 20-page guide to specifications and applications of galvanically isolated amplifiers and signal conditioners for industrial, instrumentation and medical applications.

CMOS DAC Application Guide 3rd Edition by Phil Burton (1989—64 pages). Introduction to CMOS DACs, Inside CMOS DACs, Basic Application Circuits in Current-Steering Mode, Single-Supply Operation Using Voltage-Switching Mode, The Logic Interface, Applications.

ESD Prevention Manual – Protecting ICs from electrostatic discharges. Thirty pages of information that will assist the reader in implementing an appropriate and effective program to assure protection against electrostatic discharge (ESD) failures.

High-Speed Data Conversion – A 24-page short-form guide to video and other high-speed A/D and D/A converters and accessories, in forms ranging from monolithic ICs to card-level products.

RMS-to-DC Conversion Application Guide 2nd Edition by C. Kitchin and L. Counts (1986—61 pages). RMS-DC Conversion: Theory, Basic Design Considerations; RMS Application Circuits; Testing Critical Parameters; Input Buffer Amplifier Requirements; Programs for Computing Errors, Ripple and Settling Time.

Surface Mount IC‡—A 28-page guide to ICs in SO and PLCC packages. Products include op amps, rms-to-dc converters, DACs, ADCs, VFCs, sample-holds and CMOS switches.

DIGITAL SIGNAL PROCESSING MANUALS

Available at no charge for single copies; write on letterhead.

ADSP-2101/ADSP-2102 USER'S MANUAL—Architecture. [Fixed-point processor] Introduction; Computational Units; Data Moves, Program Control; Timer; Serial Ports; System Interface; Memory Interface; Instruction Set Overview; Appendixes; Index. 190 pages.

ADSP-2111 USER'S MANUAL—Architecture. [Fixed-point processor] Introduction; Computational Units; Data Moves; Program Control; Timer; Host Interface Port; Serial Ports; System Interface; Memory Interface; Instruction Set Overview; Appendixes; Index. 218 pages.

ADSP-21020 USER'S MANUAL. [Floating-point processor] Introduction; Computational Units; Program Sequencing; Data Addressing; Timer; Memory Interface; Instruction Summary; Assembly Programmer's Tutorial; Hardware System Configuration; Appendixes; Index. 394 pages.

TECHNICAL REFERENCE BOOKS

Can be purchased from Analog Devices, Inc., at the prices shown. If more than one book is ordered, deduct a discount of $1.00 from the price of each book. Price of the entire set of 9 books is $166.00—a bargain for your department's library (in effect, the nonlinear, transducer, and high-speed books come free). VISA and MasterCard are welcome; phone (617) 461-3392 or FAX (617)821-4273. Or send your check for the indicated amount to Analog Devices, Inc., P.O. Box 9106, Norwood, MA 02062-9106.

‡This publication is available in North America only.

ANALOG-DIGITAL CONVERSION HANDBOOK: Third Edition, by the Engineering Staff of Analog Devices, edited by Daniel H. Sheingold. Englewood Cliffs, NJ: Prentice Hall (1986). A comprehensive guide to A/D and D/A converters and their applications. This third edition of our classic is in hardcover and has more than 700 pages, an Index, a Bibliography, and much new material, including: video-speed, synchro-resolver, V/F, high-resolution, and logarithmic converters, ICs for DSP, and a "Guide for the Troubled." Seven of its 22 chapters are totally new. $32.95

DIGITAL SIGNAL-PROCESSING APPLICATIONS USING THE ADSP-2100 FAMILY, by the Applications Staff of Analog Devices, DSP Division; edited by Amy Mar (628 pages). Englewood Cliffs NJ: Prentice Hall (1990). Bridge the gap between DSP algorithms and their real-world implementation on state-of-the-art signal processors. Each chapter tackles a specific application topic, briefly describing the algorithm and discussing its implementation on the ADSP-2100 family of DSP chips. Comprehensive source-code listings are complete with comments and accompanied by explanatory text. Programs are listed on a pair of supplementary diskettes—furnished with the book. Application areas include fixed- and floating-point arithmetic, function approximation, digital filters, one- and two-dimensional FFTs, image processing, graphics, LP speech coding, PCM, ADPCM, high-speed modem algorithms, DTMF coding, sonar beamforming. Additional topics include memory interface, multiprocessing, and host interface. The book can serve as a companion to *Digital Signal Processing in VLSI*. Price includes diskettes. $38.00

DIGITAL SIGNAL PROCESSING IN VLSI, by Richard J. Higgins. Englewood Cliffs NJ: Prentice Hall (1990). An introductory 614-page guide for the engineer and scientist who needs to understand and use DSP algorithms and special-purpose DSP hardware ICs—and the software tools developed to carry them out efficiently. Real-World Signal Processing; Sampled Signals and Systems; The DFT and the FFT Algorithm; Digital Filters; The Bridge to VLSI; Real DSP Hardware; Software Development for the DSP System; DSP Applications; plus Bibliography and Index. $38.00

NEW—*DIGITAL SIGNAL PROCESSING LABORATORY Using the ADSP-2101 Microcomputer*, by Vinay K. Ingle and John G. Proakis (Northeastern University). Englewood Cliffs NJ: Prentice Hall (1991). Contents: Introduction to the ADSP-2100/2101 family; ADSP-2101 instruction set overview; Overview of development tools; Getting started with the ADSP-2101; Laboratory experiments using the ADSP-2101; FIR filter implementation; IIR filter implementation; Fast Fourier transform implementation; Applications in communications; Adaptive filters and their applications; References; Index. $24.00

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