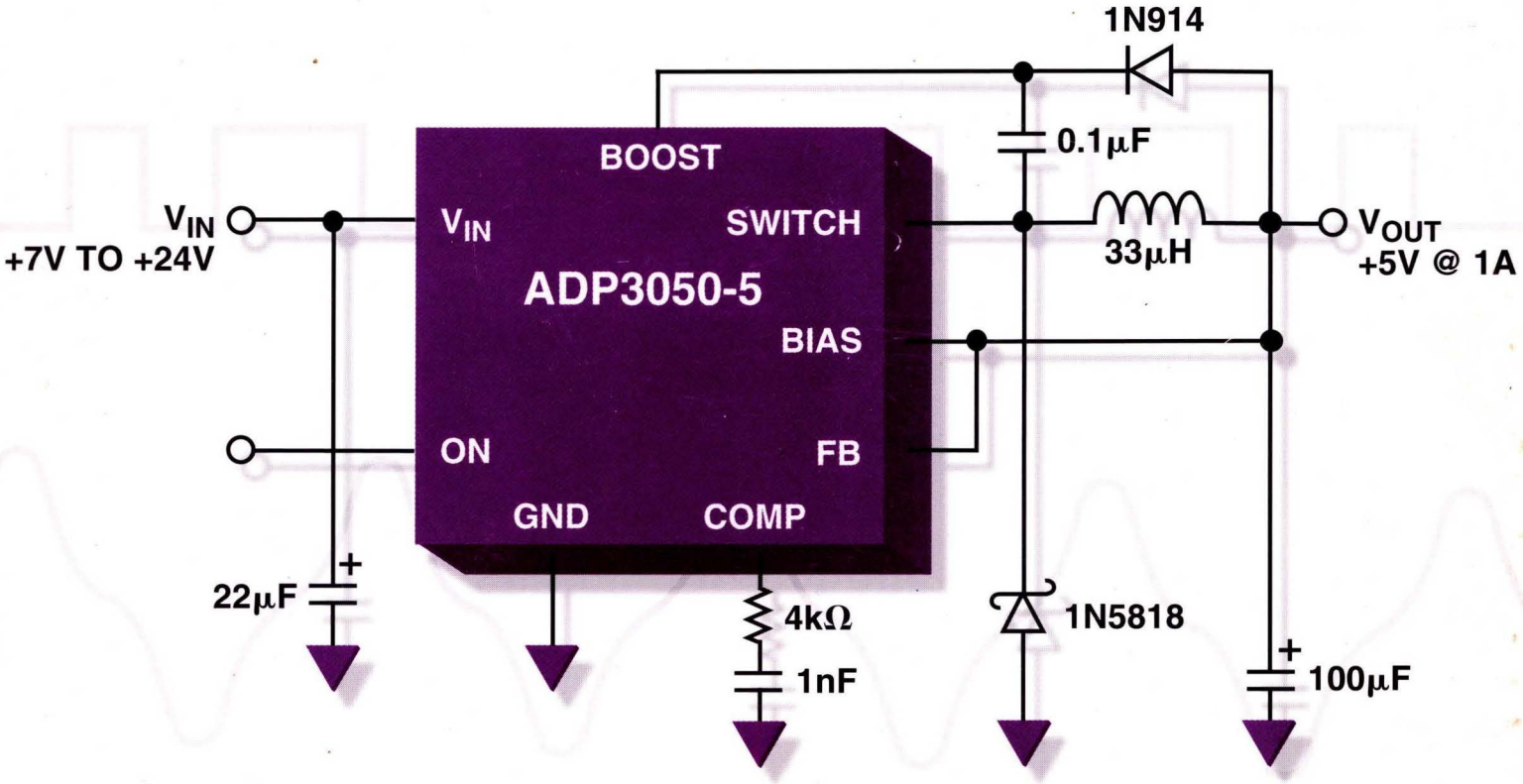
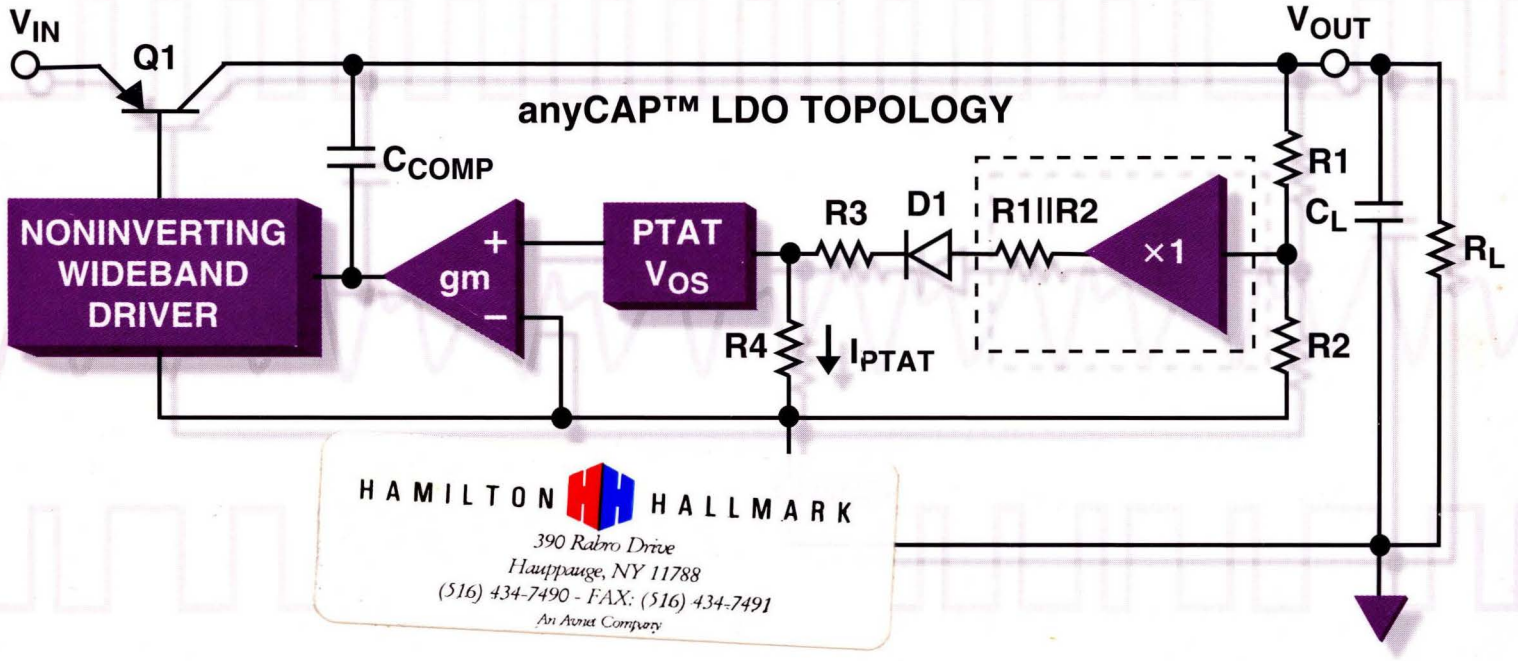
PRACTICAL DESIGN TECHNIQUES FOR POWER AND THERMAL MANAGEMENT





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PRACTICAL DESIGN TECHNIQUES FOR POWER AND THERMAL MANAGEMENT

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Walt Kester
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PRACTICAL DESIGN TECHNIQUES FOR POWER AND THERMAL MANAGEMENT

SECTION 1

INTRODUCTION

SECTION 1

INTRODUCTION
Walt Kester

This book focuses on three rather broad and inter-related topics: *power management*, *thermal management*, and *hardware monitoring*. We will discuss them in terms of the various design and application issues associated with each and show how modern ICs allow cost effective and efficient solutions.

Power management broadly refers to the generation and control of regulated voltages required to operate an electronic system. It encompasses much more than just power supply design. Today's systems require that power supply design be integrated with the system design in order to maintain high efficiency. In addition, distributed power supply systems require localized regulators at the PC board level, thereby requiring the design engineer to master at least the basics of switching and linear regulators.

Integrated circuit components such as switching regulators, linear regulators, switched capacitor voltage converters, and voltage references are typical elements of power management. Battery charging is also an important portion of power management.

Closely related to power management is *thermal management*. In addition to traditional applications of temperature sensors in industrial process control, today's systems require accurate control of monitoring and control of temperature, airflow, etc.

Today's computers require that hardware as well as software operate properly, in spite of the many things that can cause a complex high performance system to crash or lock up. The purpose of *hardware monitoring* is to monitor the critical items in a computing system and take corrective action should problems occur.

Microprocessor supply voltage and temperature are two critical parameters. If the supply voltage drops below a specified minimum level, further operations should be halted until the voltage returns to acceptable levels. In some cases, it is desirable to reset the microprocessor under "brownout" conditions. It is also common practice to reset the microprocessor on power-up or power-down. Switching to a battery backup may be required if the supply voltage is low. Under low voltage conditions it may also be desirable to inhibit the microprocessor from writing to external CMOS memory by inhibiting the Chip Enable signal to the memory.

A summary of the concepts of power management, thermal management, and hardware monitoring is shown in Figure 1.1.

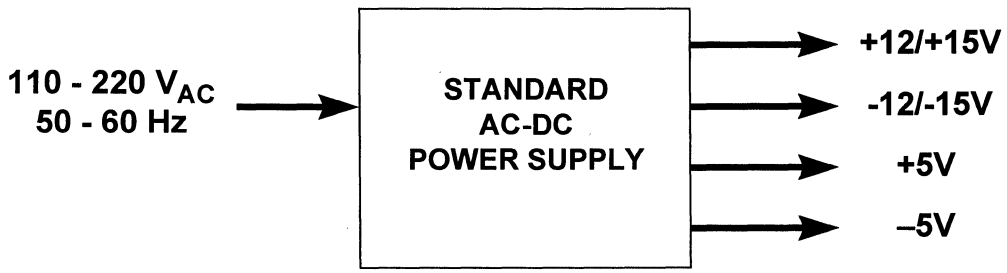
POWER MANAGEMENT, THERMAL MANAGEMENT AND HARDWARE MONITORING OVERVIEW

- **Power Management**
  - **Switching Supplies**
  - **Switched Capacitor Voltage Converters**
  - **Battery Chargers**
  - **Linear Low Dropout Regulators**
  - **Voltage References**
- **Thermal Management**
  - **Temperature Sensing**
  - **Temperature Control**
- **Hardware Monitoring**
  - **µP Supervision**
  - **Supply Voltages**
  - **Temperature**

Figure 1.1

In order to understand power management better, we will consider a few typical applications. Consider the traditional desktop PC power supply shown in Figure 1.2. This approach suffers from a number of disadvantages including inefficiency (all the voltages are on all the time - which is probably not necessary), multiple high-current distribution busses, etc.

CLASSICAL POWER SUPPLY SYSTEM e.g. TRADITIONAL DESKTOP PCs



Major Disadvantages of the Traditional PS System Include:

- **Inefficiency : Output Voltages Are Always Turned On**
- **Cable Lengths**
- **Inductance**

Figure 1.2

The trend in today's systems is to make use of the distributed power approach as shown in Figure 1.3. The AC input is rectified, filtered, and converted into an unregulated intermediate voltage which is distributed throughout the system. Each subsystem uses localized voltage regulators (usually switching-types for high efficiency) for generating required voltages. This simplifies the power distribution problem and also allows individual voltages to be shutdown if they are not in use.

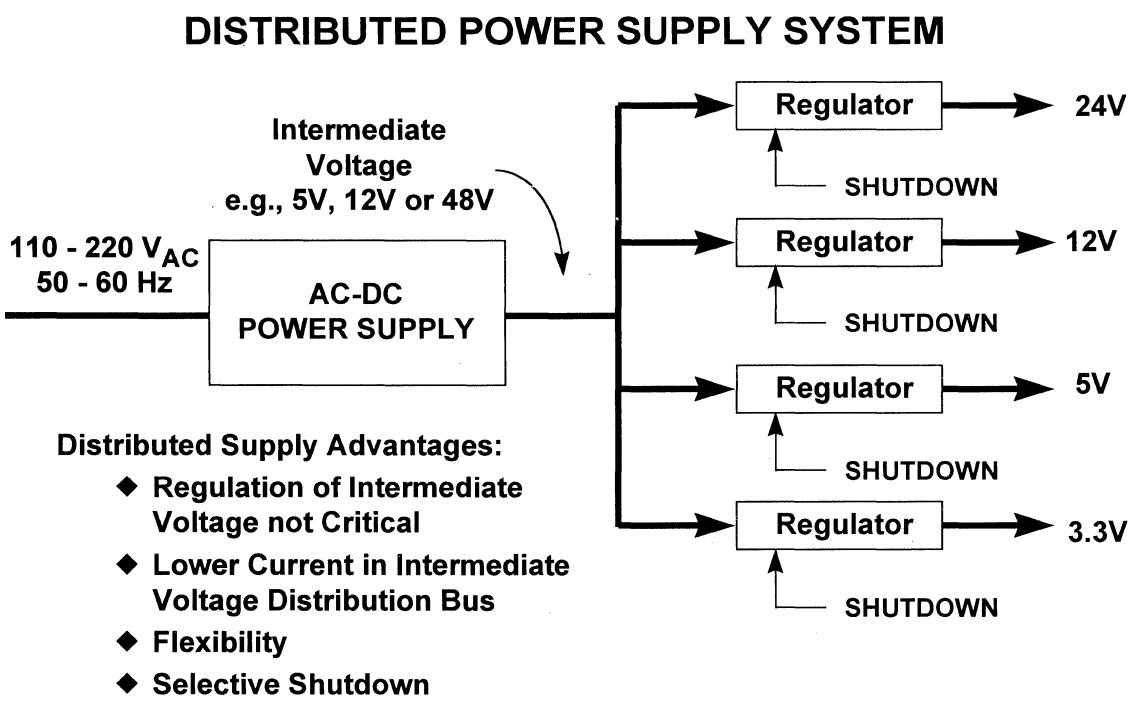


Figure 1.3

To see how this concept is extended to the PC board level design, Figure 1.4 shows a simplified block diagram of a data acquisition board. The unregulated intermediate voltage enters the board and drives the switching regulators. In the example shown, one switching regulator is dedicated to the processor, and the other drives a low dropout linear regulator. The critical analog circuits on the board, including the signal conditioning and A/D converter, are supplied from the output of the linear regulator. This ensures that the analog circuits operate with a well-regulated and low noise supply voltage. A separate low noise voltage reference is used in conjunction with the 16 bit A/D converter for even lower noise and higher accuracy.

The hardware monitoring circuits monitor the processor power supply voltages to ensure the processor functions properly. Airflow and heat sinking is often required with modern high-speed DSPs or microprocessors because of their high power dissipation. Therefore a temperature sensor monitors the processor temperature and works in conjunction with the temperature monitoring and control circuit to regulate the airflow.

Figure 1.5 summarizes some of the trends in digital and analog signal processing.

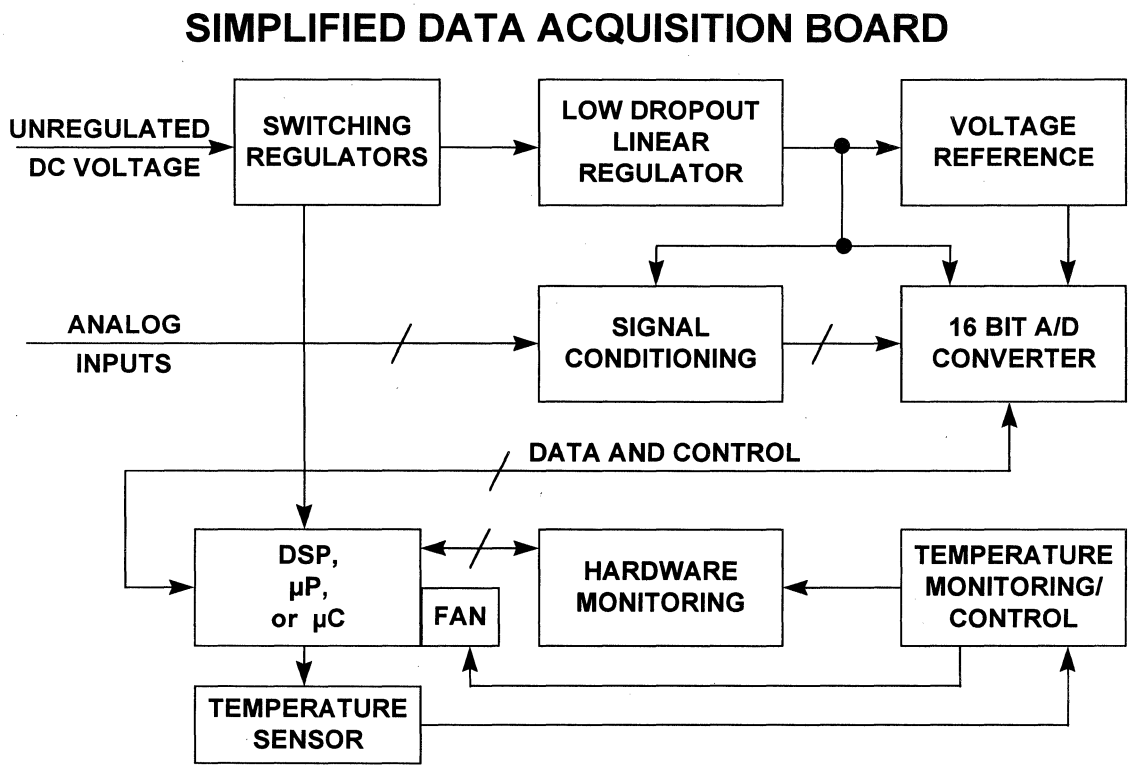


Figure 1.4

TRENDS IN DIGITAL AND ANALOG SIGNAL PROCESSING

- **Faster Digital and Analog Signal Processing**
- **Higher Power - Requires Thermal Management**
- **Distributed Power Systems vs. Single Power Supply- Implies On-Board Regulation**
- **Energy Efficient - Requires Switching Regulators and Low Dropout Linear Regulators**
- **16+ Bit ADCs Require Precision Voltage References**

Figure 1.5

Portable electronic equipment such as laptop computers and cell phones require other types of hardware monitoring as well as power and thermal management circuits. Today's laptop computers are replacing the traditional desktop systems in many companies (see Figure 1.6). Laptops, however, present a large number of design challenges because of the emphasis on performance, light weight, low power, and long battery life. Battery charging circuits are quite complex, and battery voltage and temperature must be monitored and controlled during the charging

cycle. Redundancy must be built into these circuits in order to prevent damage to the battery or dangerous outgassing.

Thermal and power management is therefore critical to laptop computers, not only relating to the high-power microprocessor, but also with respect to the battery charging function (see Figure 1.7). Most laptops have internal fans to cool the microprocessor when the internal temperature exceeds safe levels, but the fan should only operate when necessary to conserve battery life.

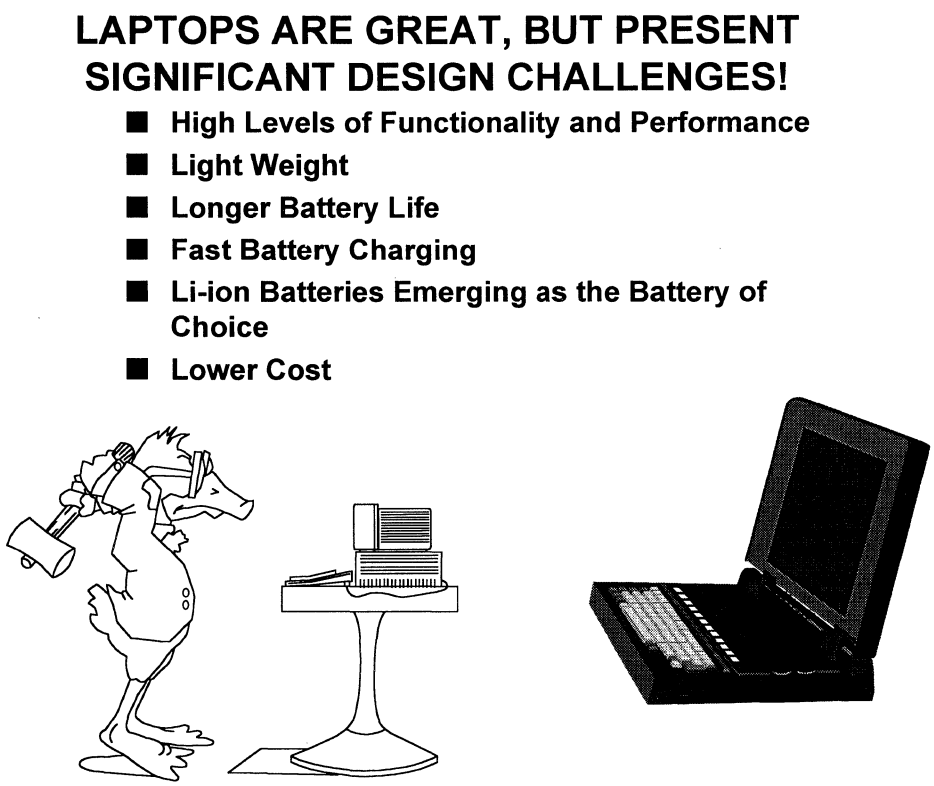


Figure 1.6

Cell phones and other types of hand-held electronic equipment make wide use of power management techniques (see Figure 1.8). Certain critical parts of a cell phone such as the oscillator and frequency synthesis circuits are generally powered by low dropout linear regulators for low noise and accuracy, while high efficiency switching regulators are most often used in the high-power transmitter circuits. Shutdown features are also vital to preserve battery life while the phone is idle.

LAPTOP COMPUTERS REQUIRE

- Battery Charger Circuits
- Switching Regulators
- Low Dropout Linear Regulators
- Temperature Sensors and Control
- µP Supervisory Circuits
- Airflow (Fan) Control

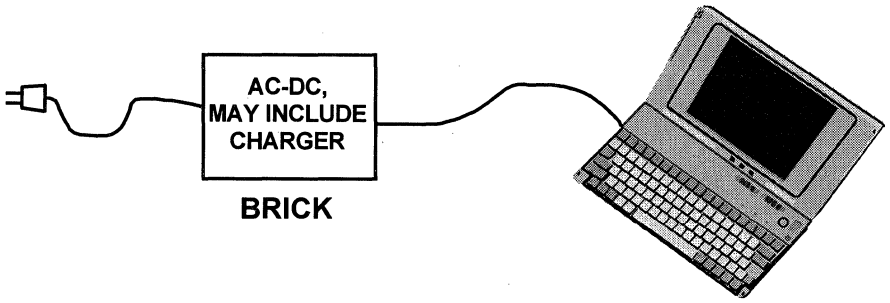
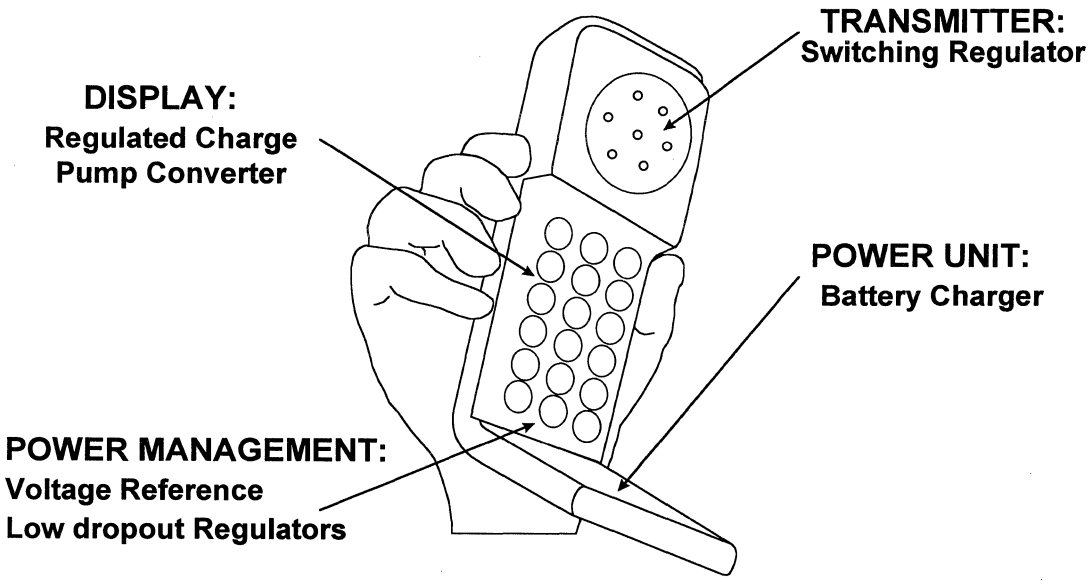


Figure 1.7

CELL PHONES



- High Performance and Functionality
- Small Size, Light Weight
- Long Battery Life, Fast Charging
- Low Cost

Figure 1.8

Temperature sensors and temperature control circuits are widespread in industrial applications such as process control. In many cases, the output signal levels are low level ones (as in a thermocouple), and low noise high gain conditioning is required before further processing. Semiconductor temperature sensors are useful in many applications and offer high-level output signals which reduces the burden on the signal conditioning circuitry (see Figure 1.9). In addition, semiconductor sensors are ideally suited to applications such as PCs, because their operating temperature range, power supply requirements, and packaging closely match the other types of ICs in the system.

APPLICATIONS OF THERMAL MANAGEMENT

- **Instrumentation**
- **Process Control**
- **IC Temperature Monitoring**
- **Airflow Control**
- **Battery Charging**
- **Heat Sink Design**

Figure 1.9

Finally, proper hardware design techniques are critical to all modern systems. Layout, grounding, and decoupling are extremely critical to successful system design as well as controlling EMI and RFI. Also an understanding of thermal techniques for maintaining safe junction temperatures is critical due to the high power dissipated in many digital ICs. Discussions regarding these practical issues conclude the book (see Figure 1.10).

HARDWARE DESIGN TECHNIQUES

- **Verifying the Design**
  - **Simulation**
  - **Prototyping**

- **Minimizing Noise**
  - **Layout**
  - **Grounding**
  - **Decoupling and Filtering**
  - **Shielding**

- **Thermal Management**
  - **Temperature Sensing**
  - **Airflow Control**
  - **Heat Sinks**

- **EMI / RFI Qualification**

Figure 1.10

SECTION 2

REFERENCES AND LOW DROPOUT LINEAR REGULATORS

- Precision Voltage References
- Low Dropout Regulators

SECTION 2

REFERENCES AND LOW DROPOUT LINEAR REGULATORS

Walt Jung

Reference circuits and linear regulators actually have much in common. In fact, the latter could be functionally described as a reference circuit, but with greater current (or power) output. Accordingly, almost all of the specifications of the two circuit types have great commonality (even though the performance of references is usually tighter with regard to drift, accuracy, etc.). This chapter is broadly divided into an initial discussion on voltage references, followed by a concluding discussion on linear regulators, with emphasis on their low dropout operation for highest power efficiency.

PRECISION VOLTAGE REFERENCES

Walt Jung, Walt Kester, James Bryant

Voltage references have a major impact on the performance and accuracy of analog systems. A ±5mV tolerance on a 5V reference corresponds to ±0.1% absolute accuracy–only 10-bits. For a 12-bit system, choosing a reference that has a ±1mV tolerance may be far more cost effective than performing manual calibration, while both high initial accuracy and calibration will be necessary in a system making absolute 16-bit measurements. Note that many systems make *relative* measurements rather than absolute ones, and in such cases the absolute accuracy of the reference is not important, although noise and short-term stability may be. Figure 2.1 summarizes some key points of the reference selection process.

Temperature drift or drift due to aging may be an even greater problem than absolute accuracy. The initial error can always be trimmed, but compensating for drift is difficult. Where possible, references should be chosen for temperature coefficient and aging characteristics which preserve adequate accuracy over the operating temperature range and expected lifetime of the system.

Noise in voltage references is often overlooked, but it can be very important in system design. It is generally specified on data sheets, but system designers frequently ignore the specification and assume that voltage references do not contribute to system noise.

There are two dynamic issues that must be considered with voltage references: their behavior at start-up, and their behavior with transient loads. With regard to the first, always bear in mind that voltage references *do not power up instantly* (this is true of references inside ADCs and DACs as well as discrete designs). Thus it is rarely possible to turn on an ADC and reference, whether internal or external, make

a reading, and turn off again within a few microseconds, however attractive such a procedure might be in terms of energy saving.

Regarding the second point, a given reference IC may or may not be well suited for pulse-loading conditions, dependent upon the specific architecture. Many references use low power, and therefore low bandwidth, output buffer amplifiers. This makes for poor behavior under fast transient loads, which may degrade the performance of fast ADCs (especially successive approximation and flash ADCs). Suitable decoupling can ease the problem (but some references oscillate with capacitive loads), or an additional external broadband buffer amplifier may be used to drive the node where the transients occur.

References, like almost all other ICs today, are fast migrating to such smaller packages such as SO-8, and the even more tiny SOT-23, enabling much higher circuit densities within a given area of real estate. In addition to the system size reductions these steps bring, there are also tangible reductions in standby power and cost with the smaller and less expense ICs.

CHOOSING VOLTAGE REFERENCES FOR HIGH PERFORMANCE SYSTEMS

- **Tight Tolerance Improves Accuracy, Reduces System Costs**
- **Temperature Drift Affects Accuracy**
- **Long-Term Stability, Low Hysteresis Assures Repeatability**
- **Noise Limits System Resolution**
- **Dynamic Loading Can Cause Errors**
- **Power Consumption is Critical to Battery Systems**
- **Tiny Low Cost Packages Increase Circuit Density**

Figure 2.1

TYPES OF VOLTAGE REFERENCES

In terms of the functionality of their circuit connection, standard reference ICs are often only available in *series*, or *three-terminal* form (V_{IN}, Common, V_{OUT}), and also in positive polarity only. The series types have the potential advantages of lower and more stable quiescent current, standard pre-trimmed output voltages, and relatively high output current without accuracy loss. *Shunt*, or *two-terminal* (i.e., diode-like) references are more flexible regarding operating polarity, but they are also more restrictive as to loading. They can in fact eat up excessive power with widely varying resistor-fed voltage inputs. Also, they sometimes come in non-standard voltages. All of these various factors tend to govern when one functional type is preferred over the other.

Some simple diode-based references are shown in Figure 2.2. In the first of these, a current driven forward biased diode (or diode-connected transistor) produces a voltage, $V_f = V_{REF}$. While the junction drop is somewhat decoupled from the raw supply, it has numerous deficiencies as a reference. Among them are a strong TC of about –0.3%/°C, some sensitivity to loading, and a rather inflexible output voltage: it is only available in 600mV jumps.

By contrast, these most simple references (as well as all other shunt-type regulators) have a basic advantage, which is the fact that the polarity is readily reversible by flipping connections and reversing the drive current. However, a basic limitation of all shunt regulators is that load current must always be less (usually appreciably less) than the driving current, I_D.

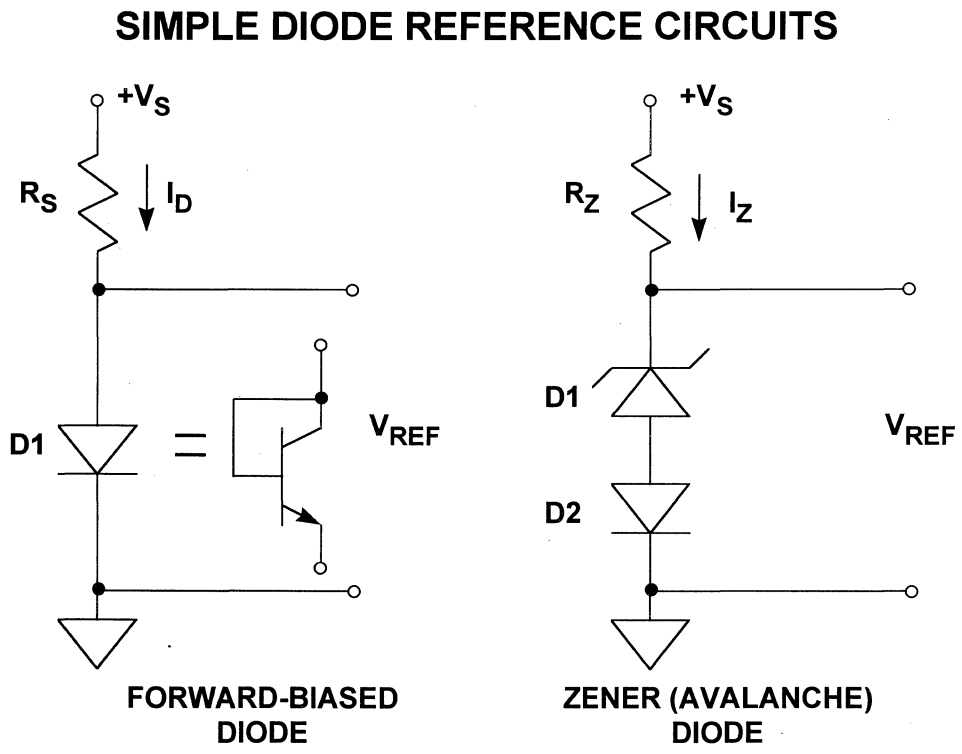


Figure 2.2

In the second circuit of Figure 2.2, a zener or avalanche diode is used, and an appreciably higher output voltage realized. While true *zener* breakdown occurs below 5V, *avalanche* breakdown occurs at higher voltages and has a positive temperature coefficient. Note that diode reverse breakdown is referred to almost universally today as *zener*, even though it is usually avalanche breakdown. With a D1 breakdown voltage in the 5 to 8V range, the net positive TC is such that it equals the negative TC of forward-biased diode D2, yielding a net TC of 100ppm/°C or less with proper bias current. Combinations of such carefully chosen diodes formed the basis of the early single package "temperature-compensated zener" references, such as the 1N821-1N829 series.

The temperature-compensated zener reference is limited in terms of initial accuracy, since the best TC combinations fall at odd voltages, such as the 1N829's 6.2V. And, the scheme is also limited for loading, since for best TC the diode current must be carefully controlled. Unlike a fundamentally lower voltage (<2V) reference, zener diode based references must of necessity be driven from voltage sources appreciably higher than 6V levels, so this precludes operation of zener references from 5V system supplies. References based on low TC zener (avalanche) diodes also tend to be noisy, due to the basic noise of the breakdown mechanism. This has been improved greatly with *monolithic* zener types, as is described further below.

At this point, we know that a reference circuit can be functionally arranged into either a series or shunt operated form, and the technology within may use either bandgap based or zener diode based circuitry. In practice there are all permutations of these available, as well as a third major technology category. The three major reference technologies are now described in more detail.

BANDGAP REFERENCES

The development of low voltage (<5V) references based on the bandgap voltage of silicon led to the introductions of various ICs which could be operated on low voltage supplies with good TC performance. The first of these was the LM109 (Reference 1), and a basic bandgap reference cell is shown in Figure 2.3.

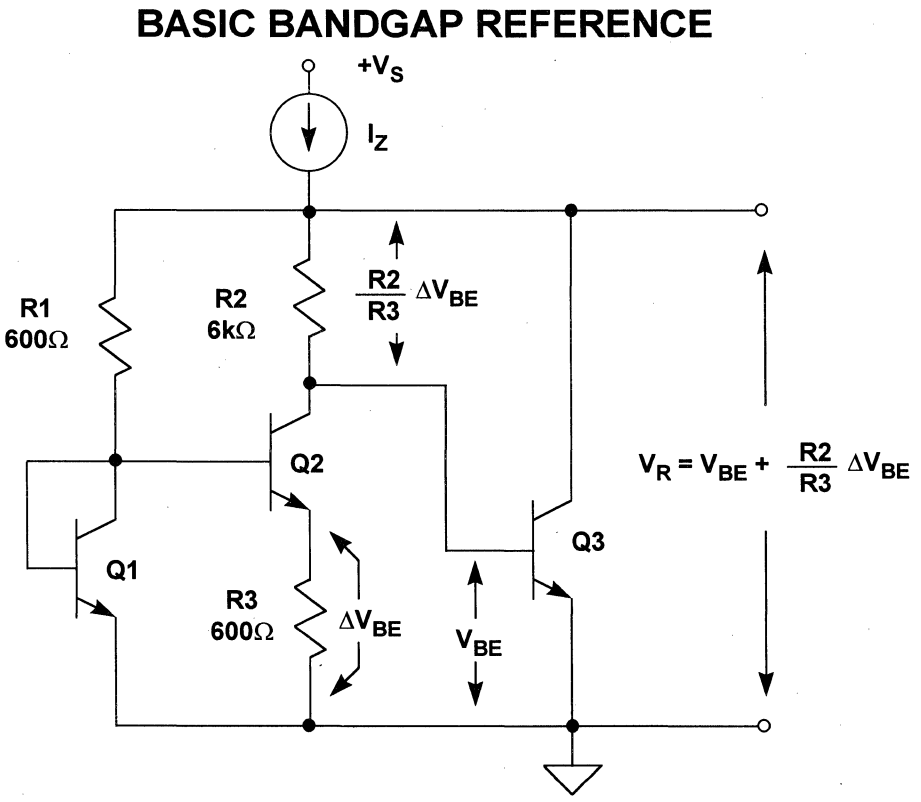


Figure 2.3

This circuit is also called a "ΔV_{BE}" reference because the differing current densities between matched transistors Q1-Q2 produces a ΔV_{BE} across R3. It works by summing the V_{BE} of Q3 with the amplified ΔV_{BE} of Q1-Q2, developed across R2. The ΔV_{BE} and V_{BE} components have opposite polarity TCs; ΔV_{BE} is proportional-to-absolute-temperature (PTAT), while V_{BE} is complementary-to-absolute-temperature (CTAT). The summed output is V_R, and when it is equal to 1.205V (silicon bandgap voltage), the TC is a minimum.

The bandgap reference technique is attractive in IC designs because of several reasons; among these are the relative simplicity, and the avoidance of zeners and their noise. However, very important in these days of ever decreasing system supplies is the fundamental fact that bandgap devices operate at low voltages, i.e., <5V. Not only are they used for stand-alone IC references, but they are also used within the designs of many other linear ICs such as ADCs, DACs, and op-amps.

Buffered forms of 1.2V two terminal bandgap references, such as the AD589 IC, remain stable under varying load currents. The H-02A metal can AD589, a 1.235V reference, handles 50μA to 5mA with an output impedance of 0.6Ω, and TCs ranging between 10 and 100ppm/°C. The more recent and functionally similar AD1580, a 1.225V reference, is in the tiny SOT-23 package and handles the same nominal currents as the AD589, with TCs of 50 and 100ppm/°C.

However, the basic designs of Figure 2.3 suffer from load and current drive sensitivity, plus the fact that the output needs accurate scaling to more useful levels, i.e., 2.5V, 5V, etc. The load drive issue is best addressed with the use of a buffer amplifier, which also provides convenient voltage scaling to standard levels.

An improved three-terminal bandgap reference, the AD580, is shown in Figure 2.4. Popularly called the "Brokaw Cell" (see References 2 and 3), this circuit provides on-chip output buffering, which allows good drive capability and standard output voltage scaling. The AD580 was the first precision bandgap based IC reference, and variants of the topology have influenced further generations of both industry standard references such as the REF01 and REF02 series, as well as more recent ADI parts such as the REF195 series, the AD680, AD780, and the AD1582-85 series.

The AD580 has two 8:1 emitter-scaled transistors Q1-Q2 operating at identical collector currents (and thus 1/8 current densities), by virtue of equal load resistors and a closed loop around the buffer op-amp. Due to the resultant smaller V_{BE} of the 8× area Q2, R2 in series with Q2 drops the ΔV_{BE} voltage, while R1 (due to the current relationships) drops a PTAT voltage V1:

$$V_1 = 2 \times \frac{R1}{R2} \times \Delta V_{BE} \ .$$

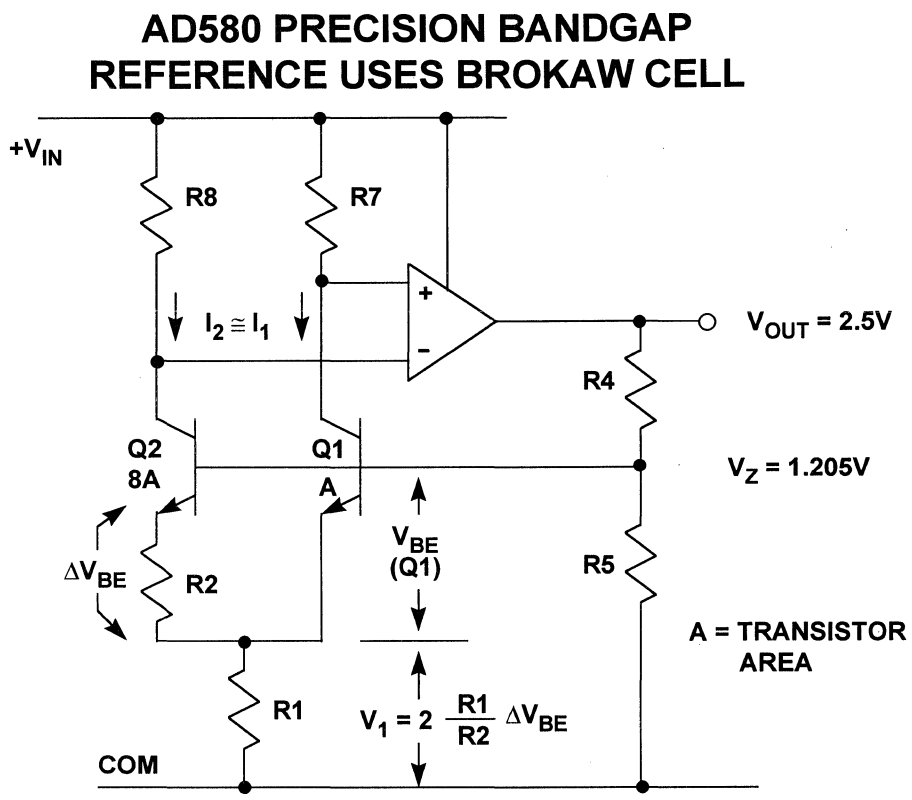


Figure 2.4

The bandgap cell reference voltage V_Z appears at the base of Q1, and is the sum of $V_{BE}(Q1)$ and V1, or 1.205V, the bandgap voltage:

$$
\begin{aligned}
V_Z &= V_{BE(Q1)} + V_1 \\
&= V_{BE(Q1)} + 2 \times \frac{R1}{R2} \times \Delta V_{BE} \\
&= V_{BE(Q1)} + 2 \times \frac{R1}{R2} \times \frac{kT}{q} \times \ln\frac{J1}{J2} \\
&= V_{BE(Q1)} + 2 \times \frac{R1}{R2} \times \frac{kT}{q} \times \ln 8 \\
&= 1.205V\,.
\end{aligned}
$$

Note that J1 = current density in Q1, J2 = current density in Q2, and J1/J2 = 8.

However, because of the presence of the R4/R5 (laser trimmed) thin film divider and the op-amp, the actual voltage appearing at V_{OUT} can be scaled higher, in the AD580 case 2.5V. Following this general principle, V_{OUT} can be raised to other practical levels, such as for example in the AD584, with taps for precise 2.5, 5, 7.5, and 10V operation. The AD580 provides up to 10mA output current while operating from supplies between 4.5 and 30V. It is available in tolerances as low as 10mV, with TCs as low as 10ppm/°C.

Many of the recent developments in bandgap references have focused on smaller package size and cost reduction, to address system needs for smaller, more power efficient and less costly reference ICs. Among these are several recent bandgap based IC references.

The AD1580 is a shunt mode IC reference which is functionally quite similar to the classic shunt IC reference, the AD589 mentioned above. A key difference is the fact that the AD1580 uses a newer, small geometry process, enabling its availability within the tiny SOT-23 package. The very small size of this package allows use in a wide variety of space limited applications, and the low operating current lends itself to portable battery powered uses. The AD1580 circuit is shown in simplified form in Figure 2.5.

AD1580 1.2V SHUNT TYPE BANDGAP REFERENCE HAS TINY SIZE IN SOT-23 FOOTPRINT

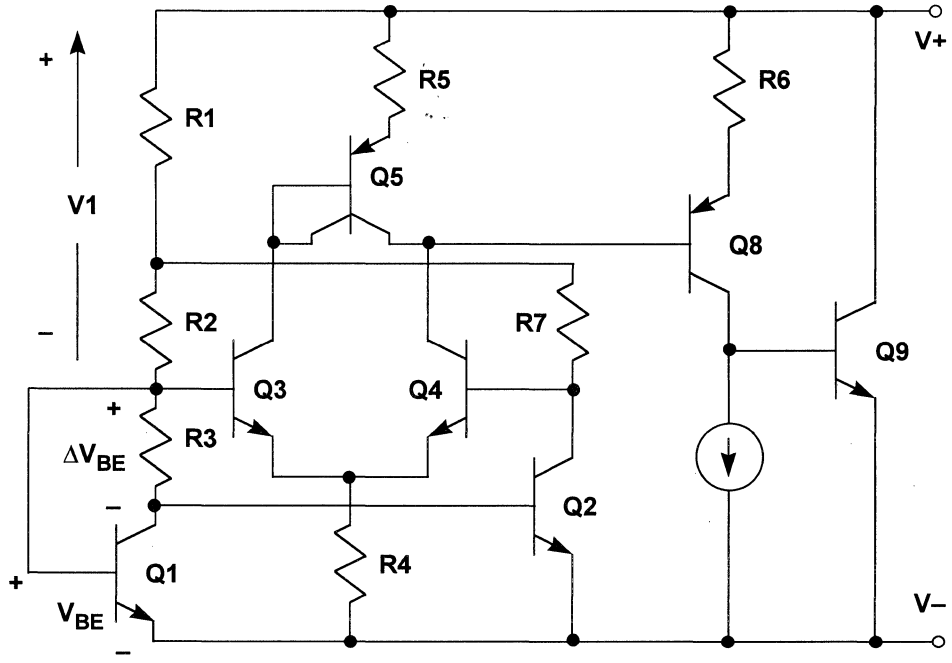


Figure 2.5

In this circuit, like transistors Q1 and Q2 form the bandgap core, and are operated at a current ratio of 5 times, determined by the ratio of R7 to R2. An op amp is formed by the differential pair Q3-Q4, current mirror Q5, and driver/output stage Q8-Q9. In closed loop equilibrium, this amplifier maintains the bottom ends of R2-R7 at the same potential.

As a result of the closed loop control described, a basic ΔV_{BE} voltage is dropped across R3, and a scaled PTAT voltage also appears as V1, which is effectively in series with V_{BE}. The nominal bandgap reference voltage of 1.225V is then the sum of Q1's V_{BE} and V1. The AD1580 is designed to operate at currents as low as 50 μA, also handling maximum currents as high as 10 mA. It is available in grades with voltage tolerances of ±1 or ±10 mV, and with corresponding TC's of 50 or 100 ppm/°C.

The AD1582-AD1585 series comprises a family of series mode IC references, which produce voltage outputs of 2.5, 3.0, 4.096 and 5.0V. Like the AD1580, the series uses a small geometry process to allow packaging within an SOT-23. The AD1582 series specifications are summarized in Figure 2.6.

AD1582-AD1585 2.5-5V SERIES TYPE BANDGAP SERIES SPECIFICATIONS

- **V_{OUT} : 2.500, 3.000, 4.096, & 5.000V**
- **2.7V to 12V Supply Range**
- **Supply Current : 65µA max**
- **Initial Accuracy: ±0.1% max**
- **Temperature Coefficient: 50 ppm/°C max**
- **Noise: 50µV rms (10Hz - 10kHz)**
- **Long-Term Drift: 100ppm/1khrs**
- **High Output Current: ±5mA min**
- **Temperature Range –40°C to +85°C**
- **Low Cost SOT-23 Package**

Figure 2.6

The circuit diagram for the series, shown in Figure 2.7, may be recognized as a variant of the basic Brokaw bandgap cell, as described under Figure 2.4. In this case Q1-Q2 form the core, and the overall loop operates to produce the stable reference voltage V_{BG} at the base of Q1. A notable difference here is that the op amp's output stage is designed with push-pull common-emitter stages. This has the effect of requiring an output capacitor for stability, but it also provides the IC with relatively low dropout operation. The low dropout feature means essentially that V_{IN} can be lowered to as close as several hundred mV above the V_{OUT} level without disturbing operation. The push-pull operation also means that this device series can actually both sink and source currents at the output, as opposed to the classic reference operation of sourcing current (only). For the various output voltage ratings, the divider R5-R6 is adjusted for the respective levels.

The AD1582 series is designed to operate with quiescent currents of only 65µA (maximum), which allows good power efficiency when used in low power systems with varying voltage inputs. The rated output current for the series is 5 mA, and they are available in grades with voltage tolerances of ±0.1 or ±1% of V_{OUT}, with corresponding TC's of 50 or 100ppm/°C.

Because of stability requirements, devices of the AD1582 series must be used with both an output and input bypass capacitor. Recommended worst case values for these are shown in the hookup diagram of Figure 2.8. For the electrical values noted, it is likely that tantalum chip capacitors will be the smallest in size.

AD1582-AD1585 2.5-5V SERIES TYPE BANDGAP REFERENCES HAVE TINY SIZE IN SOT-23 FOOTPRINT

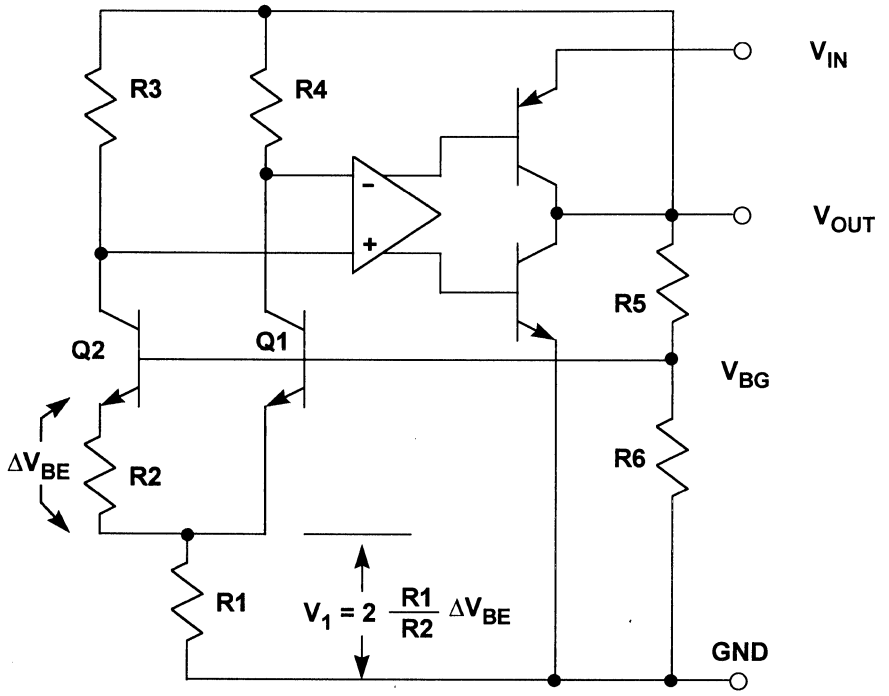


Figure 2.7

AD1582-AD1585 SERIES CONNECTION DIAGRAM

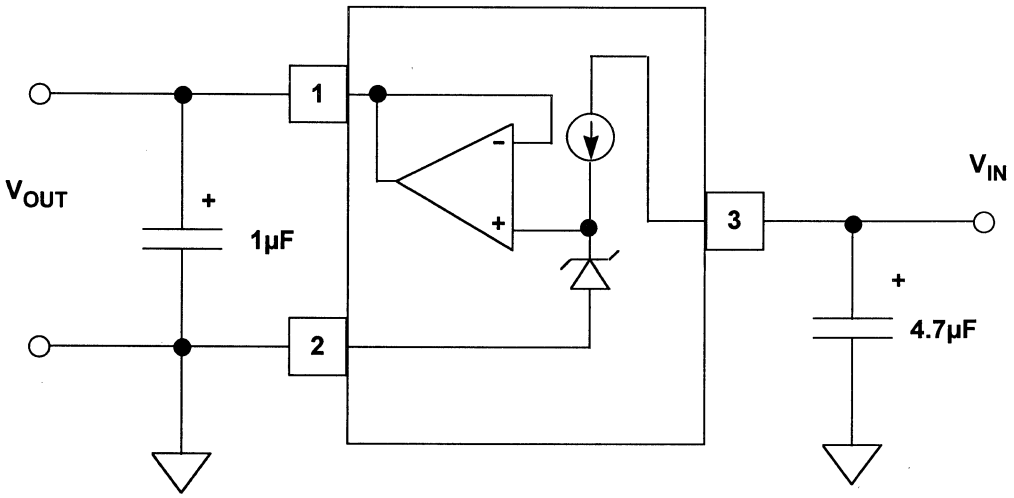


Figure 2.8

BURIED ZENER REFERENCES

In terms of the design approaches used within the reference core, the two most popular basic types of IC references consist of the bandgap and buried zener units. Bandgaps have been discussed, but zener based references warrant some further discussion.

In an IC chip, surface operated diode junction breakdown is prone to crystal imperfections and other contamination, thus zener diodes formed at the surface are more noisy and less stable than are *buried* (or sub-surface) ones. ADI zener based IC references employ the much preferred buried zener. This improves substantially upon the noise and drift of surface-mode operated zeners (see Reference 4). Buried zener references offer very low temperature drift, down to the 1-2ppm/°C (AD588 and AD586), and the lowest noise as a percent of full-scale, i.e., 100nV/√Hz or less. On the downside, the operating current of zener type references is usually relatively high, typically on the order of several mA.

An important general point arises when comparing noise performance of different references. The best way to do this is to compare the ratio of the noise (within a given bandwidth) to the DC output voltage. For example, a 10V reference with a 100nV/√Hz noise density is 6dB more quiet in relative terms than is a 5V reference with the same noise level.

XFET™ REFERENCES

A third and brand new category of IC reference core design is based on the properties of junction field effect (JFET) transistors. Somewhat analogous to the bandgap reference for bipolar transistors, the JFET based reference operates a pair of junction field effect transistors with different pinchoff voltages, and amplifies the differential output to produce a stable reference voltage. One of the two JFETs uses an extra ion implantation, giving rise to the name XFET™ (eXtra implantation junction Field Effect Transistor) for the reference core design.

The basic topology for the XFET™ reference circuit is shown in Figure 2.9. J1 and J2 are the two JFET transistors, which form the core of the reference. J1 and J2 are driven at the same current level from matched current sources, I1 and I2. To the right, J1 is the JFET with the extra implantation, which causes the difference in the J1-J2 pinchoff voltages to differ by 500mV. With the pinchoff voltage of two such FETs purposely skewed, a differential voltage will appear between the gates for identical current drive conditions and equal source voltages. This voltage, ΔV_P, is:

$$\Delta V_P = V_{P1} - V_{P2},$$

where V_{P1} and V_{P2} are the pinchoff voltages of FETs J1 and J2, respectively.

ADR290-ADR293 2.048-5V XFET™ REFERENCE TOPOLOGY FEATURES HIGH STABILITY AND LOW POWER

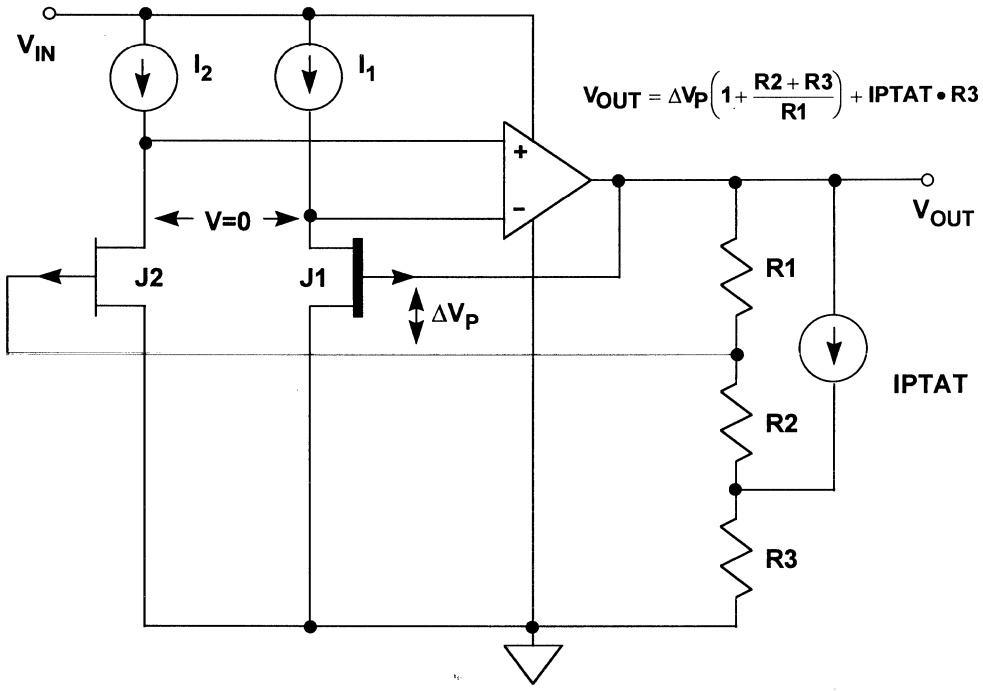


Figure 2.9

Note that, within this circuit, the voltage ΔV_P exists between the *gates* of the two FETs. We also know that, with the overall feedback loop closed, the op amp axiom of zero input differential voltage will hold the sources of the two JFET at same potential. These source voltages are applied as inputs to the op amp, the output of which drives feedback divider R1-R3. As this loop is configured, it stabilizes at an output voltage from the R1-R2 tap which does in fact produce the required ΔV_P between the J1-J2 gates. In essence, the op amp amplifies ΔV_P to produce V_{OUT},where

$$V_{OUT} = \Delta V_P\left(1 + \frac{R2 + R3}{R1}\right) + (I_{PTAT})(R3).$$

As can be noted, this expression includes the basic output scaling (leftmost portion of the right terms), plus a rightmost temperature dependent term including I_{PTAT}. The I_{PTAT} portion of the expression compensates for a basic negative temperature coefficient of the XFET™ core, such that the overall net temperature drift of the reference is typically in a range of 3 to 8ppm/°C.

During manufacture, the R1-R3 scaling resistance values are adjusted to produce the different voltage output options of 2.048, 2.5, 4.096 and 5.0V for the ADR290, ADR291, ADR292 and ADR293 family (ADR29X). This ADR29X family of series mode references is available in 8 pin packages with a standard footprint, as well as a TO-92 3 lead format. They operate from supplies of V_{OUT} plus 200mV to 15V, with a typical quiescent current of 12 μA, and output currents of up to 5 mA. A summary of specifications for the family appears in Figure 2.10.

ADR290-ADR293 XFET™ SERIES SPECIFICATIONS

- **V_{OUT} : 2.048, 2.500, 4.096, & 5.000V**
- **2.7V to 15V Supply Range**
- **Supply Current : 12µA max**
- **Initial Accuracy: ±2 mV max**
- **Temperature Coefficient: 8 ppm/°C max**
- **Low-Noise: 6µVp-p (0.1 - 10Hz)**
- **Wideband Noise: 420nV/√Hz @ 1kHz**
- **Long-Term Drift: 0.2ppm/1khrs**
- **High Output Current: 5mA min**
- **Temperature Range –40°C to +125°C**
- **Standard REF02 Pinout**
- **8-Lead Narrow Body SOIC, 8-Lead TSSOP, and 3-Lead TO-92**

Figure 2.10

The XFET™ architecture offers performance improvements over bandgap and buried zener references, particularly for systems where operating current is critical, yet drift and noise performance must still be excellent. XFET™ noise levels are lower than bandgap based bipolar references operating at an equivalent current, the temperature drift is low and linear at 3-8 ppm/°C (allowing easier compensation when required), and the series has lower hysteresis than bandgaps. Thermal hysteresis is a low 50ppm over a –40 to +125°C range, less that half that of a typical bandgap device. Finally, the long-term stability is excellent, typically only 0.2ppm/1000 hours.

Figure 2.11 summarizes the pro and con characteristics of the three reference architectures; bandgap, buried zener, and XFET™.

Modern IC references come in a variety of styles, but series operating, fixed output positive types do tend to dominate. These devices can use bandgap based bipolars, JFETs, or buried zeners at the device core, all of which has an impact on the part's ultimate performance and application suitability. They may or may not also be low power, low noise, and/or low dropout, and be available within a certain package. Of course, in a given application, any single one of these differentiating factors can drive a choice, thus it behooves the designer to be aware of all the different devices available.

CHARACTERISTICS OF REFERENCE ARCHITECTURES

BANDGAP	BURIED ZENER	XFET™
< 5V Supplies	> 5V Supplies	< 5V Supplies
High Noise @ High Power	Low Noise @ High Power	Low Noise @ Low Power
Fair Drift and Long Term Stability	Good Drift and Long Term Stability	Excellent Drift and Long Term Stability
Fair Hysteresis	Fair Hysteresis	Low Hysteresis

Figure 2.11

STANDARD POSITIVE OUTPUT THREE TERMINAL REFERENCE HOOKUP (8-PIN DIP PINOUT)

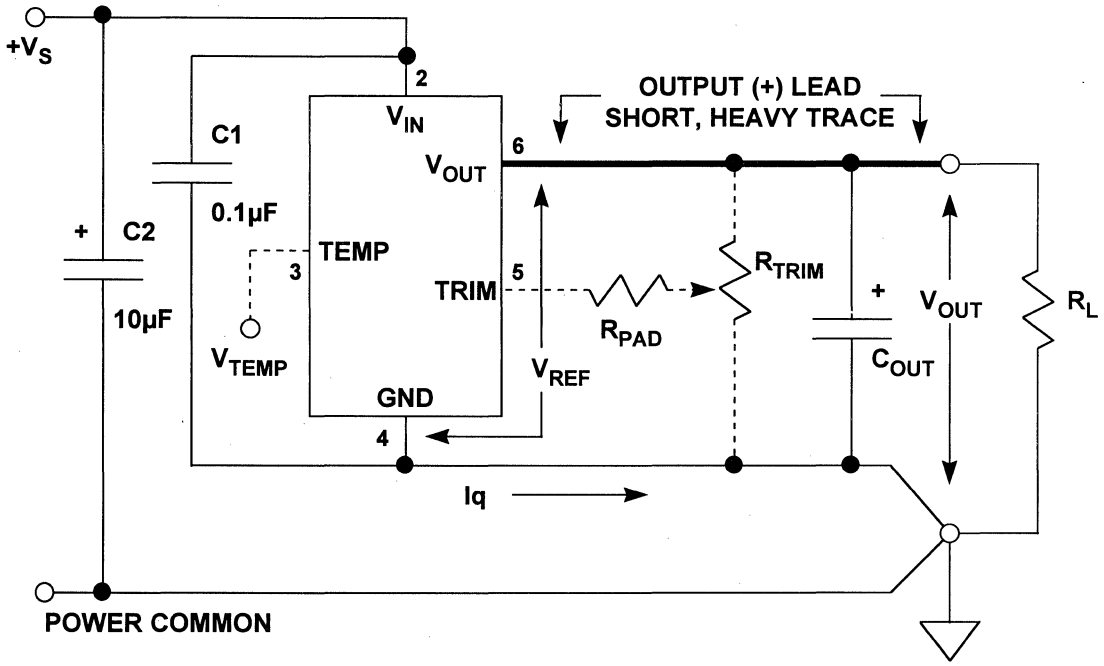


Figure 2.12

Figure 2.12 shows the standard footprint for such a series type IC positive reference in an 8 pin package (Note that "(x)" numbers refer to the standard pin for that function). There are several details which are important. Many references allow optional trimming by connecting an external trim circuit to drive the references' *trim* input pin (5). Some bandgap references also have a high impedance PTAT output (V_{TEMP}) for temperature sensing (3). The intent here is that no appreciable current be drawn from this pin, but it can be useful for such non-loading types of connections as comparator inputs, to sense temperature thresholds, etc.

All references should use decoupling capacitors on the input pin (2), but the amount of decoupling (if any) placed on the output (6) depends upon the stability of the reference's output op-amp with capacitive load. Simply put, there is no hard and fast rule for capacitive loads here. For example, some three terminal types *require* the output capacitor (i.e., REF19X and AD1582-85 series), while with others it is optional for performance improvement (AD780, REF43). The safest rule then is that you should verify what are the specific capacitive loading ground rules for the reference you intend to use, for the load conditions your circuit presents.

VOLTAGE REFERENCE SPECIFICATIONS

TOLERANCE

It is usually better to select a reference with the required value and accuracy and to avoid external trimming and scaling if possible. This allows the best TCs to be realized, as tight tolerances and low TCs usually go hand-in-hand. Tolerances as low as 0.04% can be achieved with the AD586, AD780, REF195, while the AD588 is 0.01%. If and when trimming must be used, be sure to use the recommended trim network with no more range than is absolutely necessary. When/if additional external scaling is required, a precision op-amp should be used, along with ratio-accurate, low TC tracking thin film resistors.

DRIFT

The XFET™ and buried zener reference families have the best long term drift and TC performance. TCs as low as 1-2ppm/°C are available with the AD586 and AD588, and the AD780 bandgap reference is almost as good at 3ppm/°C. The XFET™ series achieve long terms drifts of 0.2 ppm/1000 hours, while the buried zener types come in at 25ppm/1000 hours. Note that where a figure is given for long term drift, it is usually drift expressed in ppm/1000 hours. There are 8766 hours in a year, and many engineers multiply the 1000 hour figure by 8.77 to find the annual drift - this is not correct, and can in fact be quite pessimistic. Long term drift in precision analog circuits is a "random walk" phenomenon and increases with the *square root* of the elapsed time (this supposes that drift is due to random micro-effects in the chip and not some over-riding cause such as contamination). The 1 year figure will therefore be about $\sqrt{8.766} \approx 3$ times the 1000 hour figure, and the ten year value will be roughly 9 times the 1000 hour value. In practice, things are a little better even than this, as devices tend to stabilize with age.

The accuracy of an ADC or DAC can be no better than that of its reference. Reference temperature drift affects fullscale accuracy as shown in Figure 2.13. This table shows system resolution and the TC required to maintain 1/2 LSB error over an operating temperature range of 100°C. For example, a TC of about 1ppm/°C is required to maintain 1/2LSB error at 12-bits. For smaller operating temperature ranges, the drift requirement will be less. The last three columns of the table show the voltage value of 1/2 LSB for popular full scale ranges.

REFERENCE TEMPERATURE DRIFT REQUIREMENTS FOR VARIOUS SYSTEM ACCURACIES (1/2 LSB CRITERIA, 100°C SPAN)

		½ LSB WEIGHT (mV) 10, 5, AND 2.5V FULLSCALE RANGES		
BITS	REQUIRED DRIFT (ppm/°C)	10V	5V	2.5V
8	19.53	19.53	9.77	4.88
9	9.77	9.77	4.88	2.44
10	4.88	4.88	2.44	1.22
11	2.44	2.44	1.22	0.61
12	1.22	1.22	0.61	0.31
13	0.61	0.61	0.31	0.15
14	0.31	0.31	0.15	0.08
15	0.15	0.15	0.08	0.04
16	0.08	0.08	0.04	0.02

Figure 2.13

SUPPLY RANGE

IC reference supply voltages range from about 3V (or less) above rated output, to as high as 30V (or more) above rated output. Exceptions are devices designed for low dropout, such as the REF195 and the AD1582-AD1585 series. At low currents, the REF195 can deliver 5V with an input as low as 5.1V (100mV dropout). Note that due to process limits, some references may have more restrictive maximum voltage input ranges, such as the AD1582-AD1585 series (12V), or the ADR29X series (18V).

LOAD SENSITIVITY

Load sensitivity (or output impedance) is usually specified in μV/mA of load current, or mΩ. While figures of 100μV/mA (100mΩ) or less are quite good (AD780, REF43, REF195), it should be noted that external wiring drops can produce comparable errors at high currents, without care in layout. Load current dependent errors are minimized with short, heavy conductors on the (+) output and on the ground return.

For the highest precision, buffer amplifiers and Kelvin sensing circuits (AD588 and AD688) are used to ensure accurate voltages at the load.

The output of a buffered reference is the output of an op amp, and therefore the source impedance is a function of frequency. Typical reference output impedance rises at 6dB/octave from the DC value, and is nominally about 10Ω at a few hundred kHz. This impedance can be lowered with an external capacitor, provided the op-amp within the reference remains stable for such loading.

LINE SENSITIVITY

Line sensitivity (or regulation) is usually specified in μV/V of input change, and is lower than 50μV/V (–86dB) in the REF43, REF195, AD680, and AD780. For DC and very low frequencies, such errors are easily masked by noise.

As with op-amps, the line sensitivity (or power supply rejection) of references degrades with increasing frequency, typically 30 to 50dB at a few hundred kHz. For this reason, the reference input should be highly decoupled (LF and HF). Line rejection can also be increased with a low dropout pre-regulator, such as one of the ADP3300 series parts.

Figure 2.14 summarizes the major reference specifications.

VOLTAGE REFERENCE DC SPECIFICATIONS (TYPICAL VALUES AVAILABLE)

- **Tolerance:**
  - **AD588:** **0.01%**
  - **AD586, AD780, REF195:** **0.04%**
- **Drift (TC):**
  - **AD586, AD588:** **1-2ppm/°C**
  - **AD780, ADR29X** **3 ppm/°C**
- **Drift (long term):**
  - **AD29X:** **0.2 ppm/1000 hours**
  - **AD588:** **25 ppm/1000 hours**
- **Supply Range:**
  - **REF19X, AD1582-AD1585:** **V_{OUT} plus ~0.5 V**
- **Load Sensitivity:** **100μV/mA (100mohm)**
- **Line Sensitivity:** **50μV/V (-86 dB)**

Figure 2.14

NOISE

Reference noise is not always specified, and when it is, there is not total uniformity on how. For example, some devices are characterized for peak-to-peak noise in a 0.1

to 10Hz bandwidth, while others are specified in terms of wideband rms or peak-to-peak noise over a specified bandwidth. The most useful way to specify noise (as with op-amps) is a plot of noise voltage spectral density (nV/√Hz) versus frequency.

Low noise references are important in high resolution systems to prevent loss of accuracy. Since white noise is statistical, a given noise density must be related to an equivalent peak-to-peak noise in the relevant bandwidth. Strictly speaking, the peak-to-peak noise in a gaussian system is infinite (but its probability is infinitesimal). Conventionally, the figure of 6.6 × rms is used to define a practical peak value - statistically, this occurs less than 0.1% of the time. This peak-to-peak value should be less than 1/2LSB in order to maintain required accuracy. If peak-to-peak noise is assumed to be 6 times the rms value, then for an N-bit system, reference voltage fullscale V_{REF}, reference noise bandwidth (BW), the required noise voltage spectral density E_n (V/√Hz) is given by:

$$E_n \leq \frac{V_{REF}}{12 \cdot 2^N \cdot \sqrt{BW}}.$$

For a 10V, 12-bit, 100kHz system, the noise requirement is a modest 643nV/√Hz. Figure 2.15 shows that increasing resolution and/or lower fullscale references make noise requirements more stringent. The 100kHz bandwidth assumption is somewhat arbitrary, but the user may reduce it with external filtering, thereby reducing the noise. Most good IC references have noise spectral densities around 100nV/√Hz, so additional filtering is obviously required in most high resolution systems, especially those with low values of V_{REF}.

REFERENCE NOISE REQUIREMENTS FOR VARIOUS SYSTEM ACCURACIES (1/2 LSB / 100kHZ CRITERIA)

	NOISE DENSITY (nV/√Hz) FOR 10, 5, AND 2.5V FULLSCALE RANGES		
BITS	10V	5V	2.5V
12	643	322	161
13	322	161	80
14	161	80	40
15	80	40	20
16	40	20	10

Figure 2.15

Some references, for example the AD587 buried zener type have a pin designated as the *noise reduction pin* (see data sheet). This pin is connected to a high impedance node preceding the on-chip buffer amplifier. Thus an externally connected capacitor C_N will form a low pass filter with an internal resistor, to limits the effective noise bandwidth seen at the output. A 1μF capacitor gives a 3 dB bandwidth of 40 Hz. Note that this method of noise reduction is by no means universal, and other devices may implement noise reduction differently, if at all.

There are also general purpose methods of noise reduction, which can be used to reduce the noise of any reference IC, at any standard voltage level. The reference circuit of Figure 2.16 (References 5 and 6) is one such example. This circuit uses external filtering and a precision low-noise op-amp to provide both very low noise and high DC accuracy. Reference U1 is a 2.5, 3.0, 5, or 10V reference with a low noise buffered output. The output of U1 is applied to the R1-C1/C2 noise filter to produce a corner frequency of about 1.7 Hz. Electrolytic capacitors usually imply DC leakage errors, but the bootstrap connection of C1 causes its applied bias voltage to be only the relatively small drop across R2. This lowers the leakage current through R1 to acceptable levels. Since the filter attenuation is modest below a few Hertz, the reference noise still affects overall performance at low frequencies (i.e., <10 Hz).

COMBINING LOW-NOISE AMPLIFIER WITH EXTENSIVE FILTERING YIELDS EXCEPTIONAL REFERENCE NOISE PERFORMANCE (1.5 TO 5nV/√Hz @ 1kHZ)

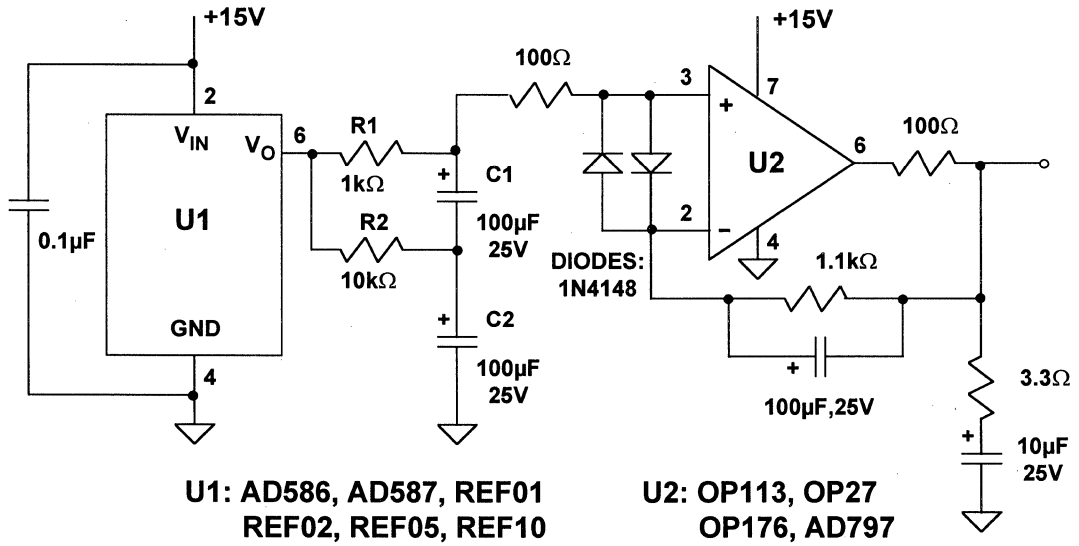


Figure 2.16

The output of the filter is then buffered by a precision low noise unity-gain follower, such as the OP113EP. With less than ±150μV of offset error and under 1μV/°C drift, the buffer amplifier's DC performance will not seriously affect the accuracy/drift of most references. For example, an ADR292E for U1 will have a typical drift of 3ppm/°C, equivalent to 7.5μV/°C, higher than the buffer amplifier. Almost any op amp will have a current limit higher than a typical IC reference. Further, even lower noise op-amps are available for 5-10V use. The AD797 offers 1kHz noise

performance less than 2nV/√Hz in this circuit, compared to about 5nV/√Hz for the OP113. With any amplifier, Kelvin sensing can be used at the load point, a technique which can eliminate I×R related output voltage errors.

SCALED REFERENCES

A useful approach when a non-standard reference voltage is required is to simply buffer and scale a basic low voltage reference diode. With this approach, a potential difficulty is getting an amplifier to work well at such low voltages as 3V. A workhorse solution is the low power reference and scaling buffer shown in Figure 2.17. Here a low current 1.2V two terminal reference diode is used for D1, which can be either a 1.235V AD589, or the 1.225V AD1580. Resistor R1 sets the diode current in either case, and is chosen for 50μA at a minimum supply of 2.7V (a current suitable for either diode). Obviously, loading on the unbuffered diode must be minimized at the V_{REF} node.

RAIL-TO-RAIL OUTPUT OP AMPS ALLOW GREATEST FLEXIBILITY IN LOW DROPOUT REFERENCES

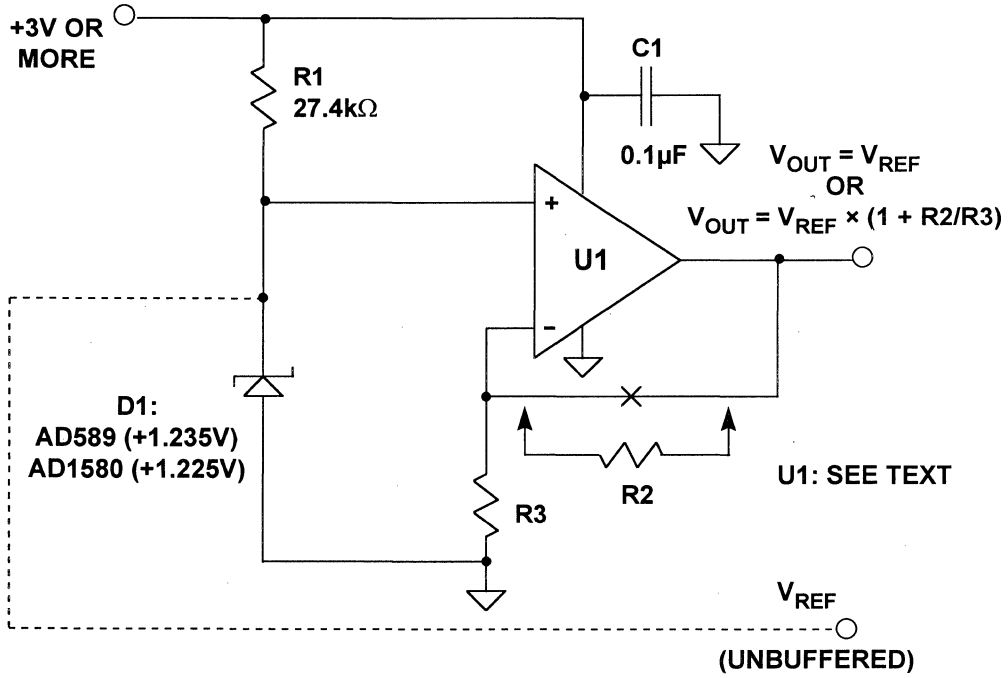


Figure 2.17

The amplifier U1 both buffers and optionally scales up the nominal 1.2V reference, allowing much higher source/sink output currents. Of course, a higher op amp quiescent current is expended in doing this, but this is a basic tradeoff of the approach. Quiescent current is amplifier dependent, ranging from 45μA/channel with the OP196/296/496 series to 1000-2000μA/channel with the OP284 and OP279. The former series is most useful for very light loads (<2mA), while the latter series provide device dependent outputs up to 50mA. Various devices can be used in the circuit as shown, and their key specs are summarized in Figure 2.18.

OP AMPS USEFUL IN LOW VOLTAGE RAIL-RAIL REFERENCES AND REGULATORS

DEVICE*	Iq, mA per channel	Vsat (+) V (min @ mA)	Vsat (–) V (max @ mA)	Isc, mA min
OP181/281/481	0.003	4.93 @ 0.05	0.075 @ 0.05	± 3.5
OP193/293/493	0.017	4.20 @ 1	0.280 @ 1 (typ)	± 8
OP196/296/496	0.045	4.30 @ 1	0.400 @ 1	± 4 (typ)
OP295/495	0.150**	4.50 @ 1	0.110 @ 1	± 11
OP191/291/491	0.300	4.80 @ 2.5	0.075 @ 2.5	± 8.75
AD820/822	0.620	4.89 @ 2	0.055 @ 2	± 15
OP184/284/484	1.250**	4.85 @ 2.5	0.125 @ 2.5	± 7.5
AD8531/32/34	1.400	4.90 @ 10	0.100 @ 10	± 250
OP279	2.000	4.80 @ 10	0.075 @ 10	± 45

*** Typical device specifications @ Vs = +5V, TA = 25°C, unless otherwise noted**
**** Maximum**

Figure 2.18

In Figure 2.17, without gain scaling resistors R2-R3, V_{OUT} is simply equal to V_{REF}. With the use of the scaling resistors, V_{OUT} can be set anywhere between a lower limit of V_{REF}, and an upper limit of the positive rail, due to the op amp's rail-rail output swing. Also, note that this buffered reference is inherently low dropout, allowing a +4.5V (or more) reference output on a +5V supply, for example. The general expression for V_{OUT} is shown in the figure, where V_{REF} is the reference voltage.

Amplifier standby current can be further reduced below 20μA, if an amplifier from the OP181/281/481 or the OP193/293/493 series is used. This choice will be at some expense of current drive, but can provide very low quiescent current if necessary. All devices shown operate from voltages down to 3V (except the OP279, which operates at 5V).

REFERENCE PULSE CURRENT RESPONSE

The response of references to dynamic loads is often a concern, especially in applications such as driving ADCs and DACs. Fast changes in load current invariably perturb the output, often outside the rated error band. For example, the reference input to a sigma-delta ADC may be the switched capacitor circuit shown in Figure 2.19. The dynamic load causes current spikes in the reference as the capacitor C_{IN} is charged and discharged. As a result, noise may be induced on the ADC reference circuitry.

SWITCHED CAPACITOR INPUT OF SIGMA-DELTA ADC PRESENTS A DYNAMIC LOAD TO THE VOLTAGE REFERENCE

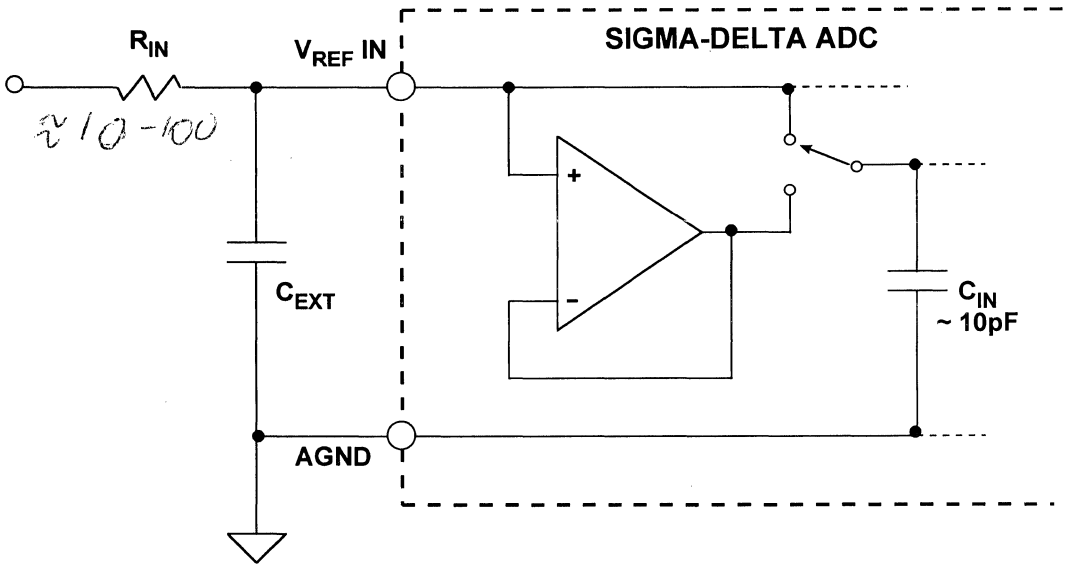


Figure 2.19

Although sigma-delta ADCs have an internal digital filter, transients on the reference input can still cause appreciable conversion errors. Thus it is important to maintain a low noise, transient free potential at the ADC's reference input. Be aware that if the reference source impedance is too high, dynamic loading can cause the reference input to shift by more than 5mV.

A bypass capacitor on the output of a reference may help it to cope with load transients, but many references are unstable with large capacitive loads. Therefore it is quite important to verify that the device chosen will satisfactorily drive the output capacitance required. In any case, the input to references should always be decoupled - with at least 0.1µF, and with an additional 5-50µF if there is any LF ripple on its supply. See Figure 2.12 (again).

Since some references misbehave with transient loads, either by oscillating or by losing accuracy for comparatively long periods, it is advisable to test the pulse response of voltage references which may encounter transient loads. A suitable circuit is shown in Figure 2.20. In a typical voltage reference, a step change of 1mA produces the transients shown. Both the duration of the transient, and the amplitude of the ringing *increase* when a 0.01µF capacitor is connected to the reference output.

MAKE SURE REFERENCE IS STABLE WITH LARGE CAPACITIVE LOADS

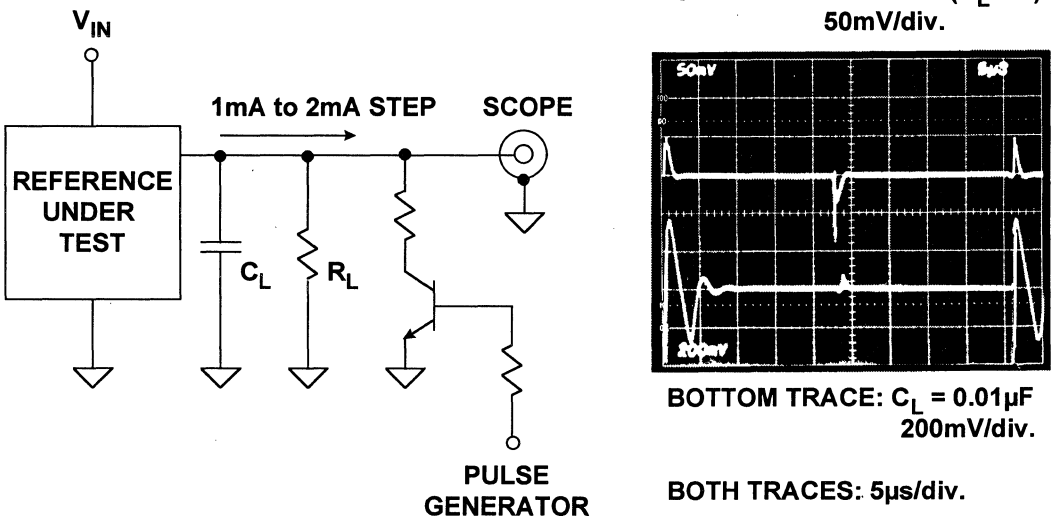


Figure 2.20

Where possible, a reference should be designed to drive large capacitive loads. The AD780 is designed to drive unlimited capacitance without oscillation, it has excellent drift and an accurate output, in addition to relatively low power consumption. Other references which are useful with output capacitors are the REF19X and AD1582-AD1585 series.

As noted above, reference bypass capacitors are useful when driving the reference inputs of successive-approximation ADCs. Figure 2.21 illustrates reference voltage settling behavior immediately following the "Start Convert" command. A small capacitor (0.01µF) does not provide sufficient charge storage to keep the reference voltage stable during conversion, and errors may result. As shown by the bottom trace, decoupling with a ≥1µF capacitor maintains the reference stability during conversion.

Where voltage references are required to drive large capacitances, it is also critically important to realize that their turn-on time will be prolonged. Experiment may be needed to determine the delay before the reference output reaches full accuracy, but it will certainly be much longer than the time specified on the data sheet for the same reference in a low capacitance loaded state.

SUCCESSIVE APPROXIMATION ADCs CAN PRESENT A DYNAMIC TRANSIENT LOAD TO THE REFERENCE

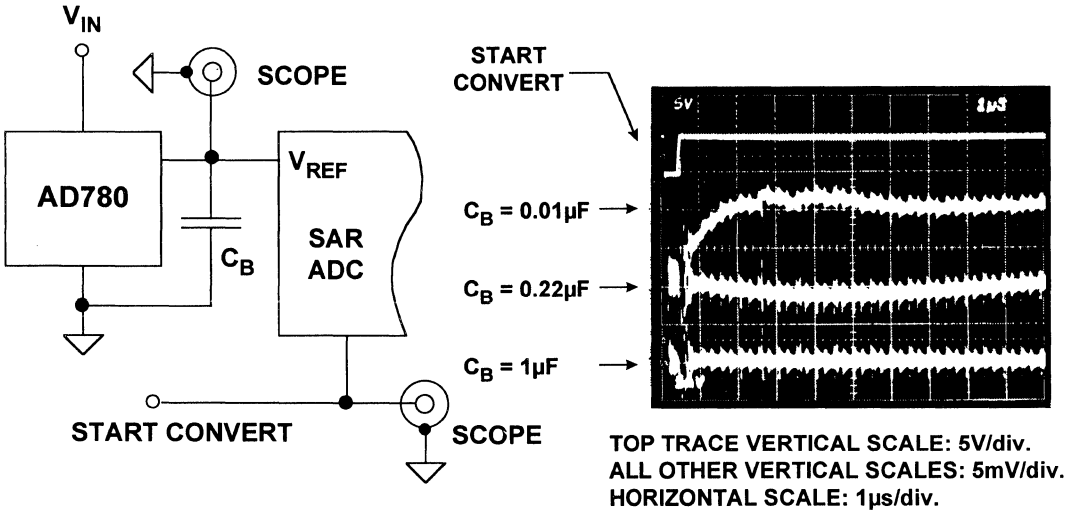


Figure 2.21

LOW NOISE REFERENCES FOR HIGH RESOLUTION CONVERTERS

High resolution converters (both sigma-delta and high speed ones) can benefit from recent improvements in IC references, such as lower noise and the ability to drive capacitive loads. Even though many data converters have internal references, the performance of these references is often compromised because of the limitations of the converter process. In such cases, using an external reference rather than the internal one often yields better overall performance. For example, the AD7710-series of 22-bit ADCs has a 2.5V internal reference with a 0.1 to 10Hz noise of 8.3µV rms (2600nV/√Hz), while the AD780 reference noise is only 0.67µV rms (200nV/√Hz). The internal noise of the AD7710-series in this bandwidth is about 1.7µV rms. The use of the AD780 increases the effective resolution of the AD7710 from about 20.5-bits to 21.5 bits.

Figure 2.22 shows the AD780 used as the reference for the AD7710-series ADCs. The use of the AD780's optional 3V scaling enhances the dynamic range of the ADC, while lowering overall system noise as described above. In addition, the AD780 allows a large decoupling capacitor on its output thereby minimizing conversion errors due to transients.

There is one possible but yet quite real problem when replacing the internal reference of a converter with a higher precision external one. The converter in question may have been trimmed during manufacture to deliver its specified performance with a relatively inaccurate internal reference. In such a case, using a more accurate external reference with the converter may actually introduce additional gain error! For example, the early AD574 had a guaranteed uncalibrated gain accuracy of 0.125% when using an internal 10V reference (which itself had a

specified accuracy of only ±1%). It is obvious that if such a device, having an internal reference which is at one end of the specified range, is used with an external reference of exactly 10V, then its gain will be about 1% in error.

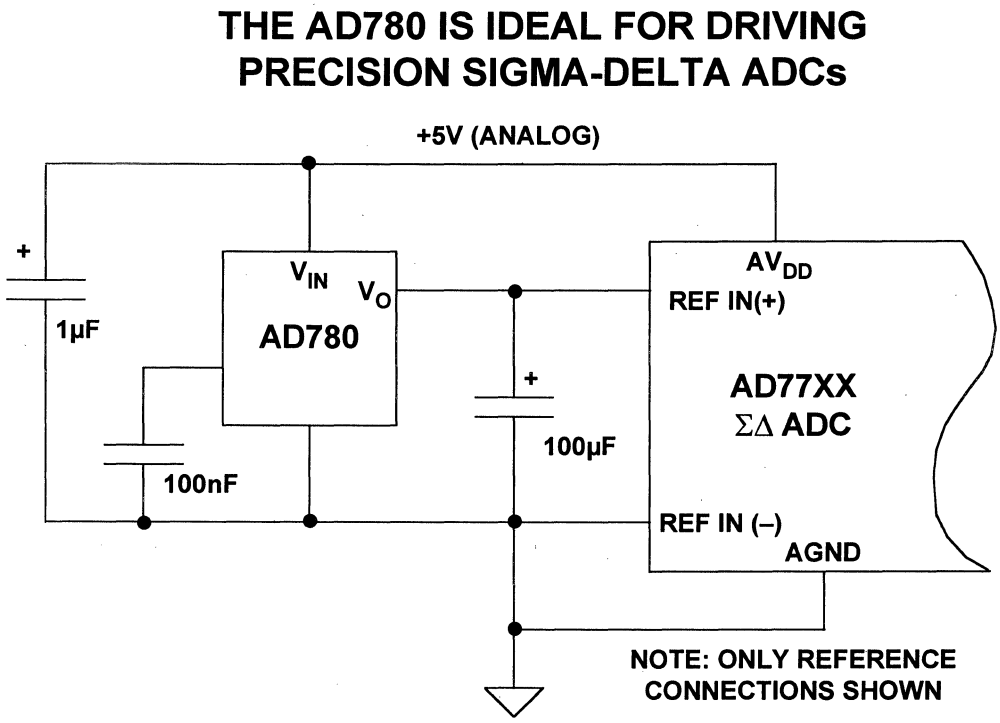


Figure 2.22

REFERENCES (Voltage References)

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2. Paul Brokaw, *A Simple Three-Terminal IC Bandgap Voltage Reference*, **IEEE Journal of Solid State Circuits**, Vol. SC-9, December, 1974.

3. Paul Brokaw, *More About the AD580 Monolithic IC Voltage Regulator*, **Analog Dialogue**, 9-1, 1975.

4. Dan Sheingold, Section 20.2 within ***Analog-Digital Conversion Handbook, 3d. Edition***, Prentice-Hall, 1986.

5. Walt Jung, *Build an Ultra-Low-Noise Voltage Reference*, **Electronic Design Analog Applications Issue**, June 24, 1993.

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LOW DROPOUT REGULATORS

Walt Jung

INTRODUCTION

Linear IC voltage regulators have long been standard power system building blocks. After an initial introduction in 5 V logic voltage regulator form, they have since expanded into other standard voltage levels spanning from 3 to 24 V, handling output currents from as low as 100 mA (or less) to as high as 5 A (or more). For several good reasons, linear style IC voltage regulators have been valuable system components since the early days. One reason is the relatively low noise characteristic vis-à-vis the switching type of regulator. Others are a low parts count and overall simplicity compared to discrete solutions. But, because of their power losses, these linear regulators have also been known for being relatively inefficient. Early generation devices (of which many are still available) required 2V or more of unregulated input above the regulated output voltage, making them lossy in power terms.

More recently however, linear IC regulators have been developed with more liberal (i.e., lower) limits on minimum input-output voltage. This voltage, known more commonly as *dropout* voltage, has led to what is termed the Low DropOut regulator, or more popularly, the LDO. Dropout voltage (V_{MIN}) is defined simply as that minimum input-output differential where the regulator undergoes a 2% reduction in output voltage. For example, if a nominal 5.0V LDO output drops to 4.9V (-2%) under conditions of an input-output differential of 0.5V, by this definition the LDO's V_{MIN} is 0.5V.

As will be shown in this section, dropout voltage is extremely critical to a linear regulator stage's power efficiency. The lower the voltage allowable across a regulator while still maintaining a regulated output, the less power the regulator dissipates as a result. A low regulator dropout voltage is the key to this, as it takes this lower dropout to maintain regulation as the input voltage lowers. In performance terms, the bottom line for LDOs is simply that more useful power is delivered to the load and less heat is generated in the regulator. LDOs are key elements of power systems that must provide stable voltages from batteries, such as portable computers, cellular phones, etc. This is simply because they maintain their regulated output down to lower points on the battery's discharge curve. Or, within classic mains-powered raw DC supplies, LDOs allow lower transformer secondary voltages, reducing system susceptibility to shutdown under brownout conditions as well as allowing cooler operation.

LINEAR VOLTAGE REGULATOR BASICS

A brief review of three terminal linear IC regulator fundamentals is necessary to understanding the LDO variety. As it turns out, almost all LDOs available today, as well as many of the more general three terminal regulator types, are *positive leg, series style* regulators. This simply means that they control the regulated voltage

output by means of a pass element which is in series with the positive side of unregulated input.

This is shown more clearly in Figure 2.23, which is a hookup diagram for a hypothetical three terminal style regulator. To re-iterate what was said earlier in the chapter about reference ICs, in terms of their basic functionality, many standard voltage regulator ICs are available in the series three-terminal form as is shown here (V_{IN}, GND or Common, V_{OUT}).

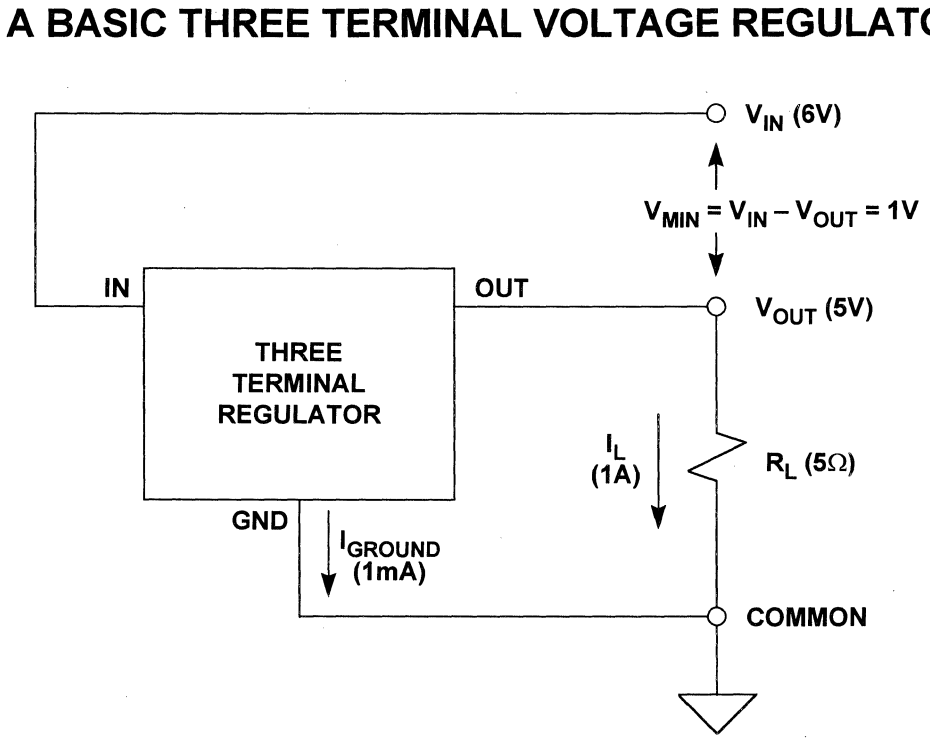

Figure 2.23

This diagram also allows some statements to be made about power losses in the regulator. There are two components to power which are dissipated in the regulator, one a function of $V_{IN} - V_{OUT}$ and I_L, plus a second which is a function of V_{IN} and Iground. If we call the total power P_D, this then becomes:

$$P_D = (V_{IN} - V_{OUT})(I_L) + (V_{IN})(\text{Iground}).$$

Obviously, the magnitude of the load current and the regulator dropout voltage both greatly influence the power dissipated. However, it is also easy to see that for a given I_L, as the dropout voltage is lowered, the first term of P_D is reduced. With an intermediate dropout voltage rating of 1V, a 1A load current will produce 1W of heat in this regulator, which may require a heat sink for continuous operation. It is this first term of the regulator power which usually predominates, at least for loaded regulator conditions.

The second term, being proportional to Iground (typically only 1-2 mA, sometimes even less) usually only becomes significant when the regulator is unloaded, and the regulator's quiescent or standby power then produces a constant drain on the source V_{IN}.

However, it should be noted that in some types of regulators (notably those which have very low β pass devices such as lateral PNP transistors) the Iground current under load can actually run quite high. This effect is worst at the onset of regulation, or when the pass device is in saturation, and can be noted by a sudden Iground current "spike", where the current jumps upward abruptly from a lower low level. All LDO regulators using bipolar transistor pass devices which can be saturated (such as PNPs) can show this effect. It is much less severe in PNP regulators using vertical PNPs (since these have a higher intrinsic β) and doesn't exist to any major extent in PMOS LDOs (since PMOS transistors are controlled by voltage level, not current).

In the example shown, the regulator delivers 5V × 1A, or 5W to the load. With a dropout voltage of 1V, the input power is 6V times the same 1A, or 6W. In terms of power efficiency, this can be calculated as:

$$P_{EFF(\%)} = 100 \times \frac{P_{OUT}}{P_{IN}},$$

where P_{OUT} and P_{IN} are the total output and input powers, respectively.

In these sample calculations, the relatively small portion of power related to Iground will be ignored for simplicity, since this power is relatively small. In an actual design, this simplifying step may not be justified.

In the case shown, the efficiency would be 100 × 5/6, or about 83%. But by contrast, if an LDO were to be used with a dropout voltage of 0.1V instead of 1V, the input voltage can then be allowed to go as low as 5.1V. The new efficiency for this condition then becomes 100 × 5/5.1, or 98%. It is obvious that an LDO can potentially greatly enhance the power efficiency of linear voltage regulator systems.

A more detailed look within a typical regulator block diagram reveals a variety of elements, as is shown in Figure 2.24.

In this diagram virtually all of the elements shown can be considered to be fundamentally necessary, the exceptions being the shutdown control and saturation sensor functions (shown dotted). While these are present on many current regulators, the shutdown feature is relatively new as a standard function, and certainly isn't part of standard three-terminal regulators. When present, shutdown control is a logic level controllable input, whereby a digital HIGH (or LO) is defined as regulation active (or vice-versa). The error output, $\overline{ERR}$, is useful within a system to detect regulator overload, such as saturation of the pass device, thermal overload, etc. The remaining functions shown are always part of an IC power regulator.

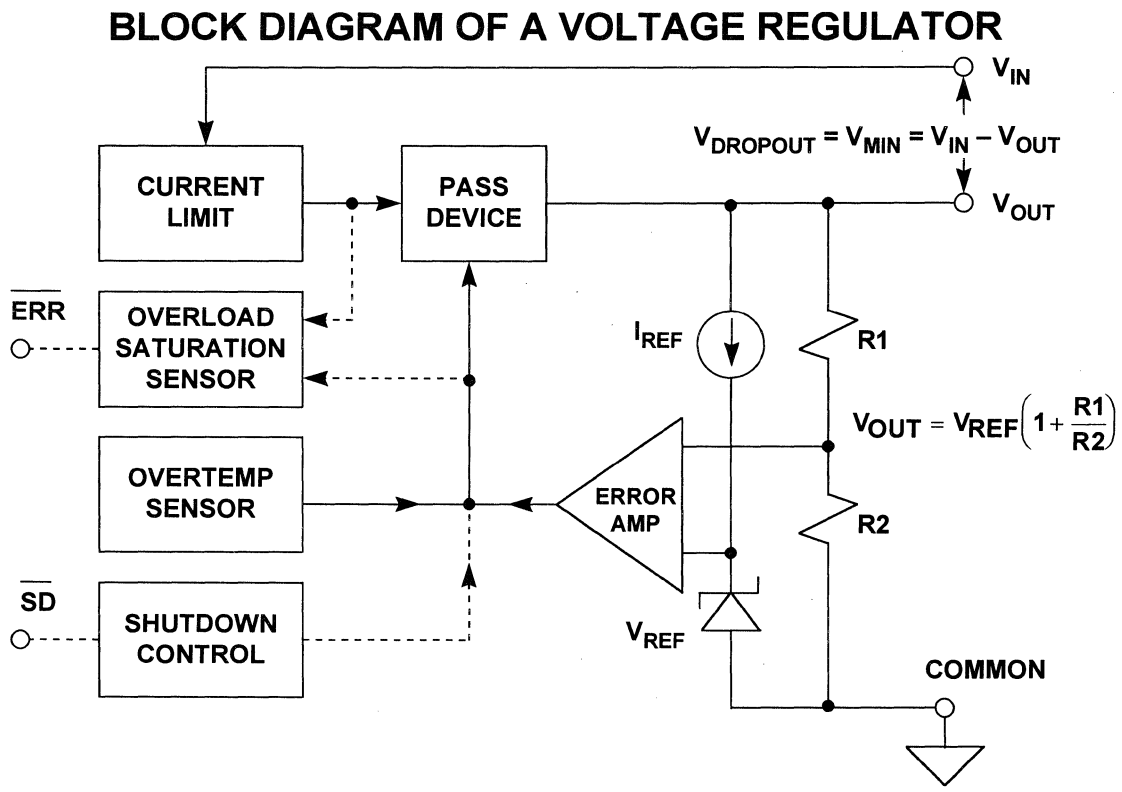

Figure 2.24

In operation, a voltage reference block produces a stable voltage V_{REF}, which is almost always a bandgap based voltage, typically ~1.2V, which allows output voltages of 3V or more from supplies as low as 5V. This voltage is presented to one input of an error amplifier, with the other input connected to the V_{OUT} sensing divider, R1-R2. The error amplifier drives the pass device, which in turn controls the output. The resulting regulated voltage is then simply:

$$V_{OUT} = V_{REF}\left(1 + \frac{R1}{R2}\right).$$

With a typical bandgap reference voltage of 1.2V, the R1/R2 ratio will be approximately 3/1 for a 5V output. When standby power is critical, several design steps will be taken. The resistor values of the divider will be high, the error amplifier and pass device driver will be low power, and the reference current I_{REF} will also be low. By these means the regulator's unloaded standby current can be reduced to a mA or less using bipolar technology, and to only a few μA in CMOS parts. In regulators which offer a shutdown mode, the shutdown state standby current will be reduced to a μA or less.

Nearly all regulators will have some means of current limiting and over temperature sensing, to protect the pass device against failure. Current limiting is usually by a series sensing resistor for high current parts, or alternately by a more simple drive current limit to a controlled β pass device (which achieves the same end). For higher voltage circuits, this current limiting may also be combined with

voltage limiting, to provide complete load line control for the pass device. All power regulator devices will also have some means of sensing over-temperature, usually by means of a fixed reference voltage and a V_{BE}-based sensor monitoring chip temperature. When the die temperature exceeds a dangerous level (above ~150°C), this can be used to shutdown the chip, by removing the drive to the pass device. In some cases an error flag output may be provided to warn of this shutdown (and also loss of regulation from other sources).

PASS DEVICES AND THEIR ASSOCIATED TRADEOFFS

The discussion thus far has not treated the pass device in any detail. In practice, this major part of the regulator can actually take on quite a number of alternate forms. Precisely which type of pass device is chosen has a major influence on almost all major regulator performance issues. Most notable among these is the dropout voltage, V_{MIN}.

Figure 2.25a through 2.25e illustrates a number of pass devices which are useful within voltage regulator circuits, shown in simple schematic form. On the figure is also listed the salient V_{MIN} for the device as it would typically be used, which directly indicates its utility for use in an LDO. Not shown in these various mini-figures are the remaining circuits of a regulator.

It is difficult to fully compare all of the devices from their schematic representations, since they differ in so many ways beyond their applicable dropout voltages. For this reason, the chart of Figure 2.26 is useful.

This chart compares the various pass elements in greater detail, allowing easy comparison between the device types, dependent upon which criteria is most important. Note that columns A-E correspond to the schematics of Figure 2.25a-2.25e. Note also that the pro/con comparison items are in *relative* terms, as opposed to a hard specification limit for any particular pass device type.

For example, it can be seen that the all NPN pass devices of columns A and B have the attributes of a follower circuit, which allows high bandwidth and provides relative immunity to cap loading because of the characteristic low Z_{OUT}. However, neither the single NPN nor the Darlington NPN can achieve low dropout, for any load current. This is because the V_{BE}(s) of the pass device appears in series with the input, preventing its saturation, and thus setting a V_{MIN} of about 1 or 2V.

By contrast, the inverting mode device connections of both columns C and E do allow the pass device to be effectively saturated, which lowers the associated voltage losses to a minimum. This single factor makes these two pass device types optimum for LDO use, at least in terms of power efficiency.

PASS DEVICES USEFUL IN VOLTAGE REGULATORS

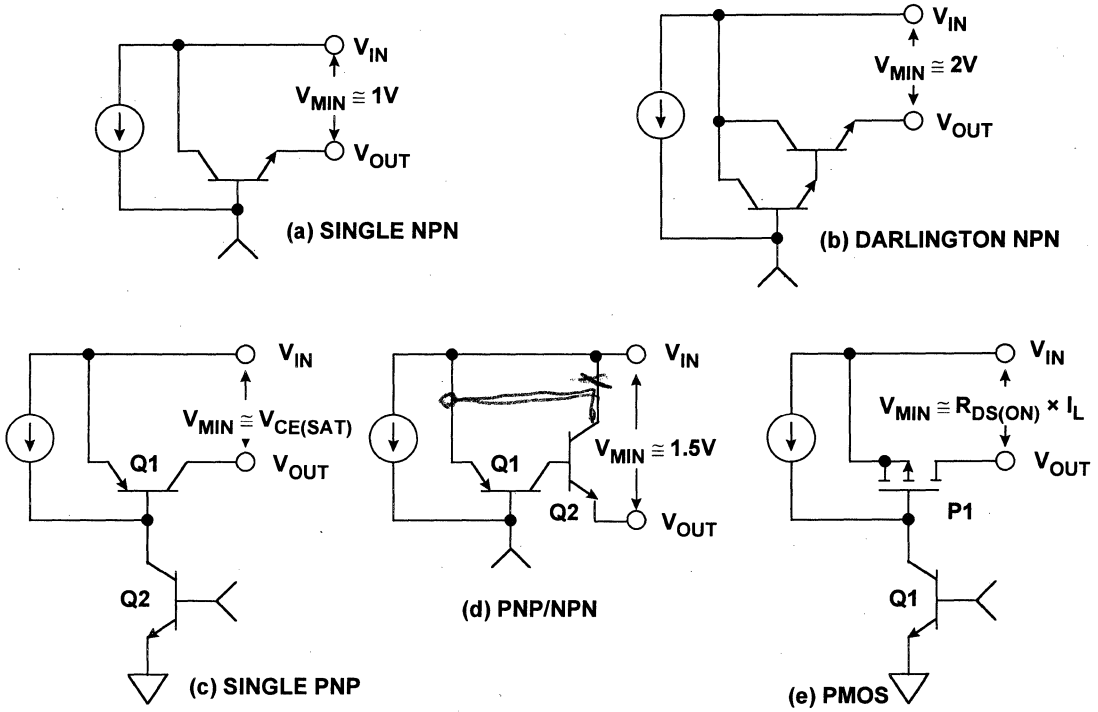

Figure 2.25

PROS AND CONS OF VOLTAGE REGULATOR PASS DEVICES

A SINGLE NPN	B DARLINGTON NPN	C SINGLE PNP	D PNP/NPN	E PMOS
V_{MIN} ~ 1V	V_{MIN} ~ 2V	V_{MIN} ~ 0.1V	V_{MIN} ~ 1.5V	$V_{MIN} \sim R_{DS(ON)} \times I_L$
I_L < 1A	I_L > 1A	I_L < 1A	I_L > 1A	I_L > 1A
Follower	Follower	Inverter	Inverter	Inverter
Low Z_{OUT}	Low Z_{OUT}	High Z_{OUT}	High Z_{OUT}	High Z_{OUT}
Wide BW	Wide BW	Narrow BW	Narrow BW	Narrow BW
C_L Immune	C_L Immune	C_L Sensitive	C_L Sensitive	C_L Sensitive

Figure 2.26

For currents below 1A, either a single PNP or a PMOS pass device is most useful for low dropout, and they both can achieve a V_{MIN} of 0.1V or less at currents of 100mA. The dropout voltage of a PNP will be highly dependent upon the actual device used and the operating current, with vertical PNP devices being superior for saturation losses, as well as minimizing the Iground spike when in saturation. PMOS pass devices offer the potential for the lowest possible V_{MIN}, since the actual dropout voltage will be the product of the device $R_{DS(ON)}$ and I_L. Thus a low $R_{DS(ON)}$ PMOS device can always be chosen to minimize V_{MIN} for a given I_L. PMOS pass devices are typically *external* to the LDO IC, making the IC actually a controller (as opposed to a complete and integral LDO). PMOS pass devices can allow currents up to several amps or more with very low dropout voltages. The PNP/NPN connection of column D is actually a hybrid hookup, intended to boost the current of a single PNP pass device. This it does, but it also adds the V_{BE} of the NPN in series (which cannot be saturated), making the net V_{MIN} of the connection about 1.5V.

All of the three connections C/D/E have the characteristic of high output impedance, and require an output capacitor for stability. The fact that the output cap is part of the regulator frequency compensation is a most basic application point, and one which needs to be clearly understood by the regulator user. This factor, denoted by "C_L sensitive", makes regulators using them generally critical as to the exact C_L value, as well as its ESR (equivalent series resistance). Typically this type of regulator must be used only with a specific size as well as type of output capacitor, where the ESR is controlled with respect to both time and temperature to fully guarantee regulator stability. Fortunately, some recent Analog Devices LDO IC circuit developments have eased this burden on the part of the regulator user a great deal, and will be discussed below in further detail.

Some examples of standard IC regulator architectures illustrate the points above regarding pass devices, and allow an appreciation of regulator developments leading up to more recent LDO technologies.

The classic LM309 5V/1A three-terminal regulator (see Reference 1) was the originator in a long procession of regulators. This circuit is shown in much simplified form in Figure 2.27, with current limiting and over temperature details omitted. This IC type is still in standard production today, not just in original form, but in family derivatives such as the 7805, 7815 etc., and their various low and medium current alternates. Using a Darlington pass connection for Q18-Q19, the design has never been known for low dropout characteristics (~1.5V typical), or for low quiescent current (~5mA). It is however relatively immune to instability issues, due to the internal compensation of C1, and the buffering of the emitter follower output. This helps make it easy to apply.

The LM109/309 bandgap voltage reference actually used in this circuit consists of a more involved scheme, as opposed to the basic form which was described with Figure 2.3. Resistor R8 drops a PTAT voltage, which drives the Darlington connected error amplifier, Q9-Q10. The negative TC V_{BE}s of Q9-Q10 and Q12-Q13 are summed with this PTAT voltage, and this sum produces a temperature-stable 5V output voltage. Current buffering of the error amplifier Q10 is provided by PNP Q11, which drives the NPN pass devices.

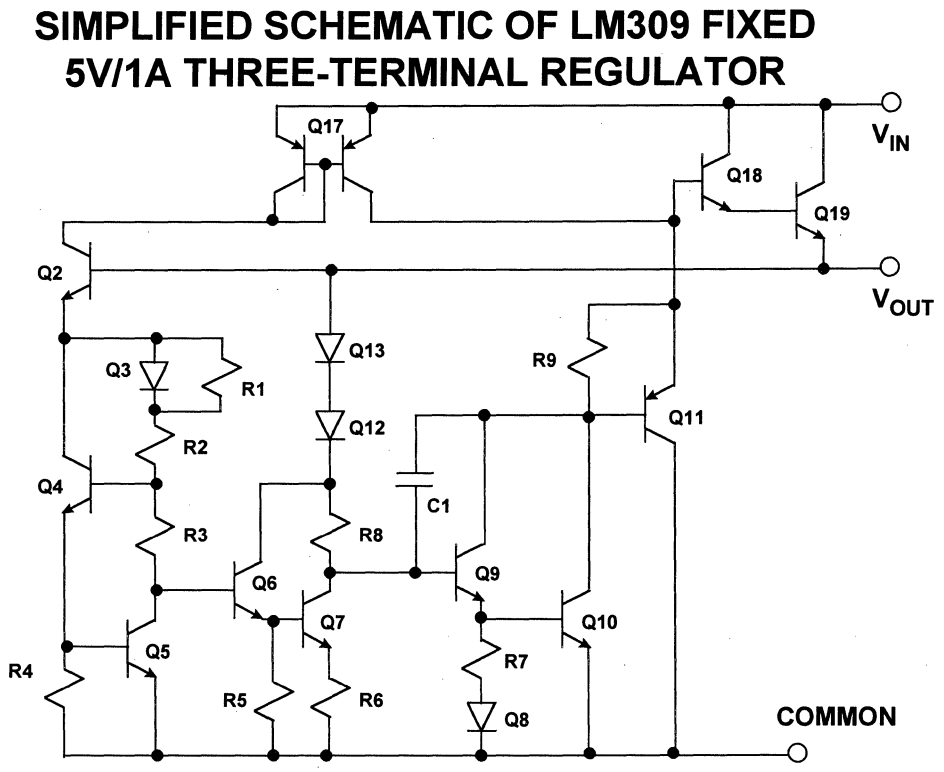

Figure 2.27

Later developments in references and three-terminal regulation techniques led to the development of the voltage adjustable regulator. The original IC to employ this concept was the LM317 (see Reference 2), which is shown in simplified schematic form in Figure 2.28. Note that this design does not use the same ΔV_{BE} form of reference as in the LM309. Instead, Q17-Q19, etc. are employed as a form of a Brokaw bandgap reference cell (see Figure 2.4 again, and Reference 3).

This adjustable regulator bootstraps the reference cell transistors Q17-Q19 and the error amplifier transistors Q16-Q18. The output of the error amplifier drives Darlington pass transistors Q25-Q26, through buffer Q12. The basic reference cell produces a fixed voltage of 1.25V, which appears between the V_{OUT} and ADJ pins of the IC as shown. External scaling resistors R1 and R2 set up the desired output voltage, which is:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + 50\mu A \times R2 .$$

SIMPLIFIED SCHEMATIC OF LM317 ADJUSTABLE THREE-TERMINAL REGULATOR

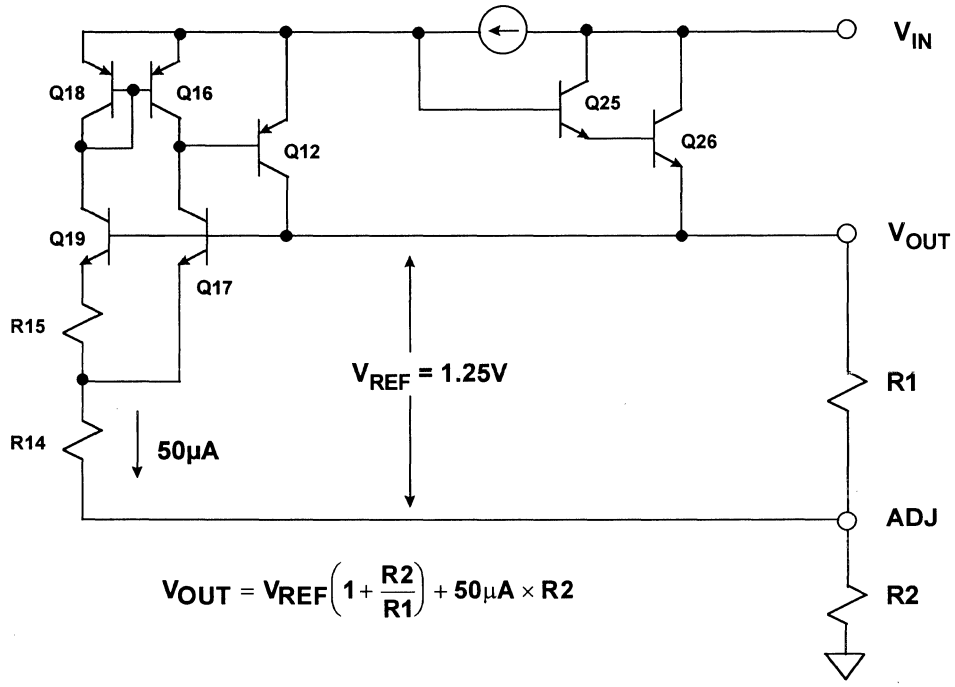

Figure 2.28

As can be noted, the voltage output is a scaling of V_{REF} by R2-R1, plus a small voltage component which is a function of the 50μA reference cell current. Typically, the R1-R2 values are chosen to draw >5mA, making the rightmost term relatively small by comparison. The design is internally compensated, and in many applications will not necessarily need an output bypass capacitor.

Like the LM309 fixed voltage regulator, the LM317 series has relatively high dropout voltage, due to the use of Darlington pass transistors. It is also not a low power IC (quiescent current typically 3.5mA). The strength of this regulator lies in the wide range of user voltage adaptability it allows.

Subsequent variations on the LM317 pass device topology modified the method of output drive, substituting a PNP/NPN cascade for the LM317's Darlington NPN pass devices. This development achieves a lower V_{MIN}, 1.5V or less (see Reference 4). The modification also allows all of the general voltage programmability of the basic LM317, but at some potential increase in application sensitivity to output capacitance. This sensitivity is brought about by the fundamental requirement for an output capacitor for the IC's frequency compensation, which is a differentiation from the original LM317.

LOW DROPOUT REGULATOR ARCHITECTURES

As has been shown thus far, all LDO pass devices have the fundamental characteristics of operating in an inverting mode. This allows the regulator circuit

to achieve pass device saturation, and thus low dropout. A by-product of this mode of operation is that this type of topology will necessarily be more susceptible to stability issues. These basic points give rise to some of the more difficult issues with regard to LDO performance. In fact, these points influence both the design and the application of LDOs to a very large degree, and in the end, determine how they are differentiated in the performance arena.

A traditional LDO architecture is shown in Figure 2.29, and is generally representative of actual parts employing either a PNP pass device as shown, or alternately, a PMOS device. There are both DC and AC design and application issues to be resolved with this architecture, which are now discussed.

TRADITIONAL LDO ARCHITECTURE

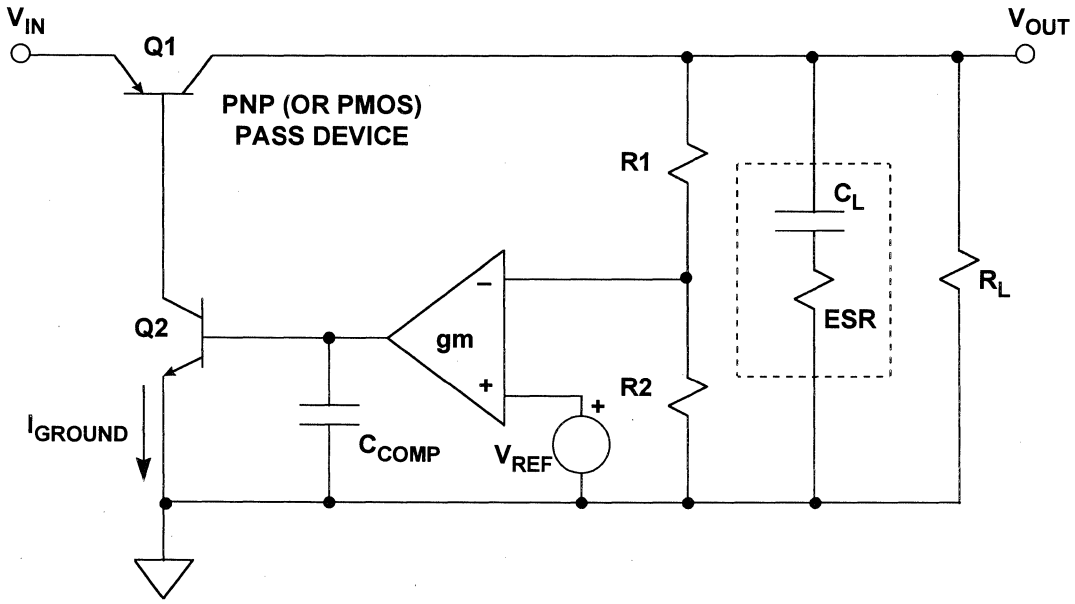

Figure 2.29

In DC terms, perhaps the major issue is the type of pass device used, which influences dropout voltage and ground current. If a lateral PNP device is used for Q1, the β will be low, sometimes only on the order or 10 or so. Since Q1 is driven from the collector of Q2, the relatively high base current demanded by a lateral PNP results in relatively high emitter current in Q2, or a high Iground. For a typical lateral PNP based regulator operating with a 5V/150mA output, Iground will be typically ~18mA, and can be as high as 40mA. To compound the problem of high Iground in PNP LDOs, there is also the "spike" in Iground, as the regulator is operating within its dropout region. Under such conditions, the output voltage is out of tolerance, and the regulation loop forces higher drive to the pass device, in an attempt to maintain loop regulation. This results in a substantial spike upward in Iground, which is typically internally limited by the regulator's saturation control circuits.

PMOS pass devices do not demonstrate a similar current spike in Iground, since they are voltage controlled. But, while devoid of the Iground spike, PMOS pass

devices do have some problems of their own. Problem number one is that high quality, low R_{ON}, low threshold PMOS devices generally aren't compatible with many IC processes. This makes the best technical choice for a PMOS pass device an external part, driven from the collector of Q2 in the figure. This introduces the term "LDO controller", where the LDO architecture is completed by an external pass device. While in theory NMOS pass devices would offer lower R_{ON} choice options, they also demand a boosted voltage supply to turn on, making them impractical for a simple LDO. PMOS pass devices are widely available in low both R_{ON} and low threshold forms, with current levels up to several amperes. They offer the potential of the lowest dropout of any device, since dropout can always be lowered by picking a lower R_{ON} part.

The dropout voltage of lateral PNP pass devices is reasonably good, typically around 300mV at 150mA, with a maximum of 600mV. These levels are however considerably bettered in regulators using vertical PNPs, which have a typical β of ~150 at currents of 200mA. This leads directly to an Iground of 1.5mA at the 200mA output current. The dropout voltage of vertical PNPs is also an improvement vis-à-vis that of the lateral PNP regulator, and is typically 180mV at 200mA, with a maximum of 400mV.

There are also major AC performance issues to be dealt with in the LDO architecture of Fig. 2.29. This topology has an inherently high output impedance, due to the operation of the PNP pass device in a common-emitter (or common-source with a PMOS device) mode. In either case, this factor causes the regulator to appear as a high source impedance to the load.

The internal compensation capacitor of the regulator, C_{COMP}, forms a fixed frequency pole, in conjunction with the g_m of the error amplifier. In addition, load capacitance C_L forms an output pole, in conjunction with R_L. This particular pole, because it is a second (and sometimes variable) pole of a two-pole system, is the source of a major LDO application problem. The C_L pole can strongly influence the overall frequency response of the regulator, in ways that are both useful as well as detrimental. Depending upon the relative positioning of the two poles in the frequency domain, along with the relative value of the ESR of capacitor C_L, it is quite possible that the stability of the system can be compromised for certain combinations of C_L and ESR. Note that C_L is shown here as a real capacitor, which is actually composed of a pure capacitance plus the series parasitic resistance ESR.

Without a heavy duty exercise into closed-loop stability analysis, it can safely be said that LDOs, like other feedback systems, need to satisfy certain basic stability criteria. One of these is the gain-versus-frequency rate-of-change characteristic in the region approaching the system's unity loop gain crossover point. For the system to be closed loop stable, the phase shift must be less than 180° at the point of unity gain. In practice, a good feedback design needs to have some phase margin, generally 45° or more to allow for various parasitic effects. While a single pole system is intrinsically stable, two pole systems are *not* necessarily so—they may in fact be stable, or they may also be unstable. Whether or not they are stable for a given instance is highly dependent upon the specifics of their gain-phase characteristics.

If the two poles of such a system are widely separated in terms of frequency, stability may not be a serious problem. The emitter-follower output of a classic regulator like the LM309 is an example with widely separated pole frequencies, as the very low Z_{OUT} of the NPN follower pushes the output pole due to load capacitance far out in frequency, where it does little harm. The internal compensation capacitance (C1 of Fig. 2.27, again) then forms part of a *dominant pole*, which reduces loop gain to below unity at the much higher frequencies where the output pole does occur. Thus stability is not necessarily compromised by load capacitance in this type of regulator.

Figure 2.30 summarizes the various DC and AC design issues of LDOs.

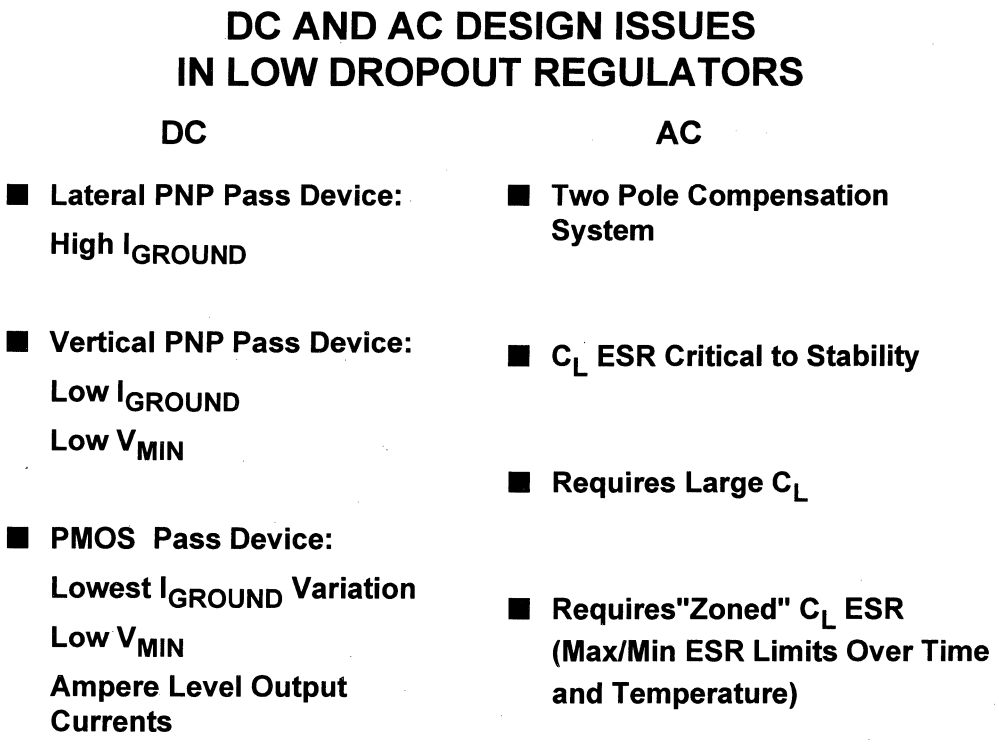

Figure 2.30

By their nature however, LDOs simply can't afford the luxury of emitter follower outputs, they must instead operate with pass devices capable of saturation. Thus, given the existence of two or more poles (one or more internal and a second formed by external loading) there is the potential for the cumulative gain-phase to add in a less than satisfactory manner. The potential for instability under certain output loading conditions is, for better or worse, a fact-of-life for most LDO topologies.

However, the output capacitor which gives rise to the instability can, for certain circumstances, also be the solution to the same instability. This seemingly paradoxical situation can be appreciated by realizing that almost all practical capacitors are actually as shown in Fig. 2.29, a series combination of the capacitance C_L and a parasitic resistance, ESR. While load resistance R_L and C_L do form a pole, C_L and its ESR also form a zero. The effect of the zero is to mitigate the de-stabilizing effect of C_L for certain conditions. For example, if the pole and zero in

question are appropriately placed in frequency relative to the internal regulator poles, some of the deleterious effects can be made to essentially cancel, leaving little or no problematic instability (see Reference 5). The basic problem with this setup is simply that the capacitor's ESR, being a parasitic term, is not at all well controlled. As a result, LDOs which depend upon output pole-zero compensation schemes must very carefully limit the capacitor ESR to certain *zones*, such as shown by Figure 2.31.

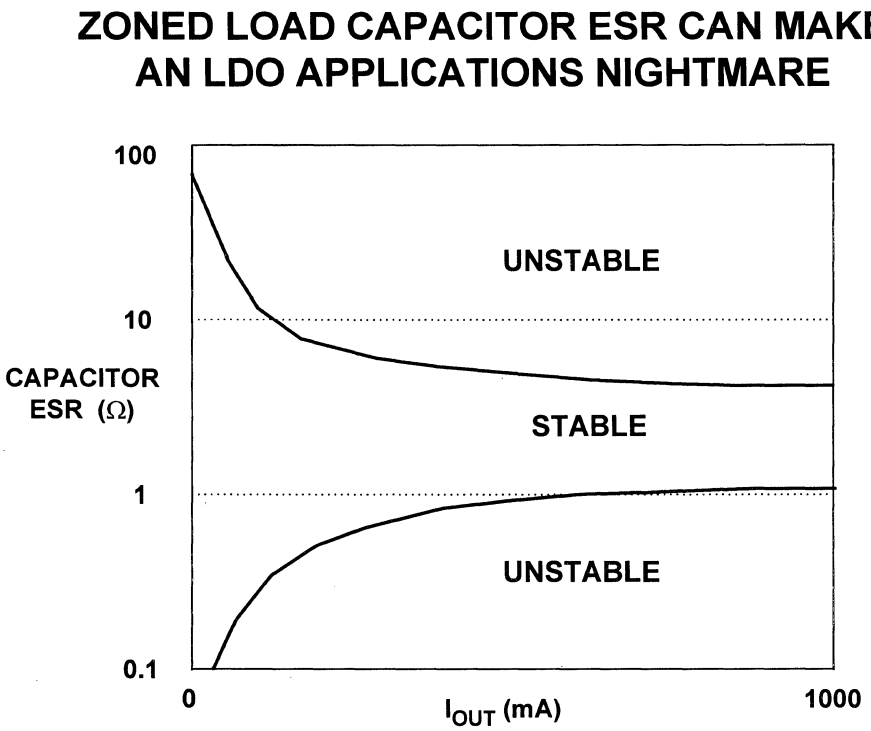

Figure 2.31

A zoned ESR chart such as this is meant to guide the user of an LDO in picking an output capacitor which confines ESR to the stable region, i.e., the central zone, for all operating conditions. Note that this generic chart is not intended to portray any specific device, just the general pattern. Unfortunately, capacitor facts of life make such data somewhat limited in terms of the real help it provides. Bearing in mind the requirements of such a zoned chart, it effectively means that general purpose aluminum electrolytic are prohibited from use, since they deteriorate in terms of ESR at cold temperatures. Very low ESR types such as OS-CON or multi-layer ceramic units have ESRs which are too low for use. While they could in theory be padded up into the stable zone with external resistance, this would hardly be a practical solution. This leaves tantalum types as the best all around choice for LDO output use. Finally, since a large capacitor value is likely to be used to maximize stability, this effectively means that the solution for an LDO such as Fig. 2.29 must use a more expensive and physically large tantalum capacitor. This is not desirable if small size is a major design criteria.

THE anyCAP™ LOW DROPOUT REGULATOR FAMILY

Some novel modifications to the basic LDO architecture of Fig. 2.29 allow major improvements in terms of both DC and AC performance. These developments are shown schematically in Figure 2.32, which is a simplified diagram of the Analog Devices ADP330X series LDO regulator family. These regulators are also known as the anyCAP™ family, so named for their relative insensitivity to the output capacitor in terms of both size and ESR. They are available in power efficient packages such as the Thermal Coastline (discussed below), in both stand-alone LDO and LDO controller forms, and also in a wide span of output voltage options.

ADP330X anyCAP™ TOPOLOGY FEATURES IMPROVED DC & AC PERFORMANCE OVER TRADITIONAL LDOs

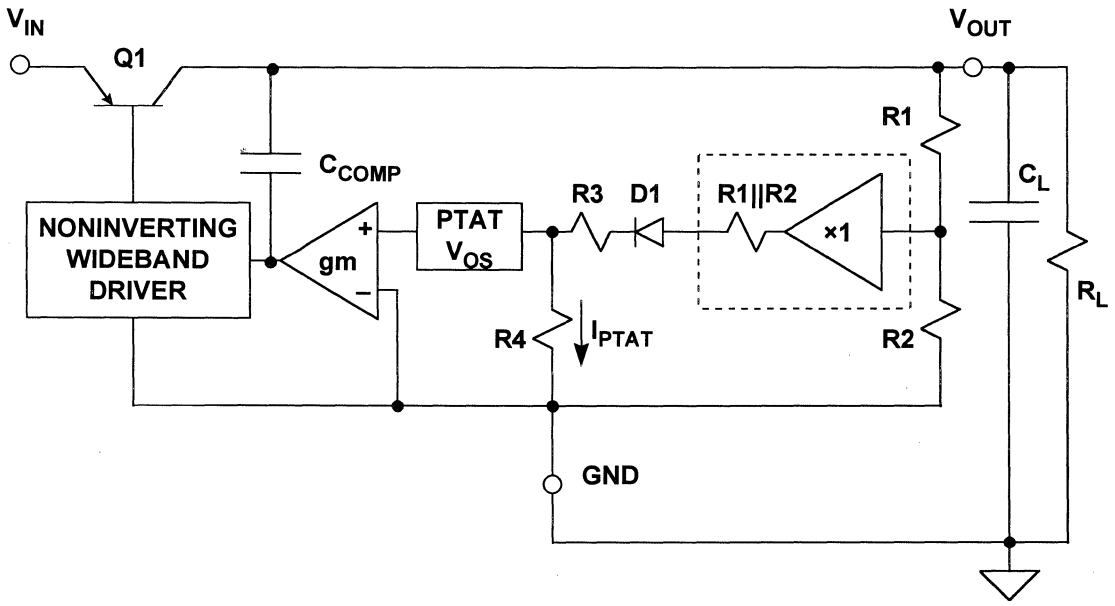

Figure 2.32

Design Features Related to DC Performance

One of the key differences in the ADP330X series is the use of a high gain vertical PNP pass device, with all of the advantages described above with Figs. 2.29 and 2.30 (also, see Reference 6). This allows the typical dropout voltages for the series to be on the order of 1mV/mA for currents of 200mA or less.

It is important to note that the topology of this LDO is distinctly different from that of the generic form in Fig. 2.29, as there is no obvious V_{REF} block. The reason for this is the fact that the ADP330X series uses what is termed a "merged" amplifier-reference design. The operation of the integral amplifier and reference scheme illustrated in Fig. 2.32 can be described as follows.

In this circuit, V_{REF} is defined as a reference voltage existing at the output of a zero impedance divider of ratio R1/R2. In the figure, this is depicted symbolically by the (dotted) unity gain buffer amplifier fed by R1/R2, which has an output of V_{REF}. This reference voltage feeds into a series connection of (dotted) R1 | | R2, then actual components D1, R3, R4, etc.

The error amplifier, shown here as a gm stage, is actually a PNP input differential stage with the two transistors of the pair operated at different current densities, so as to produce a predictable PTAT offset voltage. Although shown here as a separate block V_{OS}, this offset voltage is inherent to a bipolar pair for such operating conditions. The PTAT V_{OS} causes a current I_{PTAT} to flow in R4, which is simply:

$$I_{PTAT} = \frac{V_{OS}}{R4}.$$

Note that this current also flows in series connected R4, R3, and the Thevenin resistance of the divider, R1 | | R2, so:

$$V_{PTAT} = I_{PTAT}\,(R3 + R4 + R1||R2).$$

The *total* voltage defined as V_{REF} is the sum of two component voltages:

$$V_{REF} = V_{PTAT} + V_{D1},$$

where the I_{PTAT} scaled voltages across R3, R4, and R1 | | R2 produce a net PTAT voltage V_{PTAT}, and the diode voltage V_{D1} is a CTAT voltage. As in a standard bandgap reference, the PTAT and CTAT components add up to a temperature stable reference voltage of 1.25V. In this case however, the reference voltage is not directly accessible, but instead it exists in the virtual form described above. It acts as it would be seen at the output of a zero impedance divider of a numeric ratio of R1/R2, which is then fed into the R3-D1 series string through a Thevenin resistance of R1 | | R2 in series with D1.

With the closed loop regulator at equilibrium, the voltage at the virtual reference node will be:

$$V_{REF} = V_{OUT}\left(\frac{R2}{R1+R2}\right).$$

With minor re-arrangement, this can be put into the standard form to describe the regulator output voltage, as:

$$V_{OUT} = V_{REF}\left(1 + \frac{R1}{R2}\right).$$

In the various devices of the ADP330X series, the R1-R2 divider is adjusted to produce standard output voltages of 2.7, 3.0, 3.2, 3.3, and 5.0V.

As can be noted from this discussion, unlike a conventional reference setup, there is no power wasting reference current such as used in a conventional regulator topology (I_{REF} of Fig. 2.24). In fact, the Fig. 2.32 regulator behaves as if the entire error amplifier has simply an offset voltage of V_{REF} volts, as seen at the output of a conventional R1-R2 divider.

Design Features Related to AC Performance

While the above described DC performance enhancements of the ADP330X series are worthwhile, the most dramatic improvements come in areas of AC related performance. These improvements are in fact the genesis of the anyCAP™ series name.

Capacitive loading and the potential instability it brings is a major deterrent to easily applying LDOs. While low dropout goals prevent the use of emitter follower type outputs, and so preclude their desirable buffering effect against cap loading, there is an alternative technique of providing load immunity. One method of providing a measure of insusceptibility against variation in a particular amplifier response pole is called *pole splitting* (see Reference 8). It refers to an amplifier compensation method whereby two response poles are shifted in such a way so as to make one a dominant, lower frequency pole. In this manner the secondary pole (which in this case is the C_L related output pole) becomes much less of a major contributor to the net AC response. This has the desirable effect of greatly de-sensitizing the amplifier to variations in the output pole.

A Basic Pole-Splitting Topology

A basic LDO topology with frequency compensation as modified for pole splitting is shown in Figure 2.33. Here the internal compensation capacitor C_{COMP} is connected as an integrating capacitor, around pass device Q1 (C1 is the pass device input capacitance). While it is true that this step will help immunize the regulator to the C_L related pole, it also has a built in fatal flaw. With C_{COMP} connected directly to the Q1 base as shown, the line rejection characteristics of this setup will be quite poor. In effect, when doing it this way one problem (C_L sensitivity) will be exchanged for another (poor line rejection).

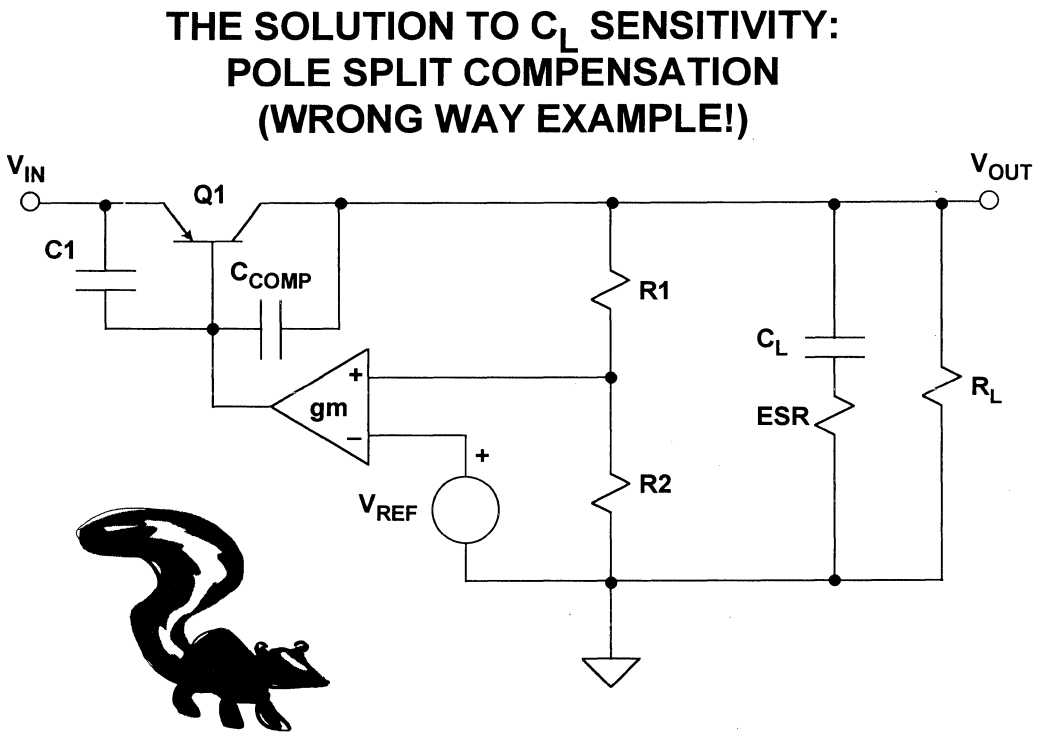

Figure 2.33

The anyCAP™ Pole-Splitting Topology

Returning to the anyCAP™ series topology, (Fig. 2.32, again) it can be noted that in this case C_{COMP} is isolated from the pass device's base (and thus input ripple variations), by the wideband non-inverting driver. But insofar as frequency compensation is concerned, because of this buffer's isolation, C_{COMP} still functions as a modified pole splitting capacitor (see Reference 9), and it does provide the benefits of a buffered, C_L independent single-pole response. The regulator's frequency response is dominated by the internal compensation, and becomes relatively immune to the value and ESR of load capacitor C_L. Thus the name anyCAP™ for the series is apt, as the design is tolerant of virtually any output capacitor type.

The benefits of the anyCAP™ topology are summarized by Figure 2.34. As can be noted, C_L can be as low as 0.47μF, and it can also be a multi-layer ceramic capacitor (MLCC) type. This allows a very small physical size for the entire regulation function, such as when a SOT-23 packaged anyCAP™ LDO is used, for example the ADP3300 device. Because of the in-sensitivity to C_L, the designer needn't worry about such things as ESR zones, and can better concentrate on the system aspects of the regulator application.

BENEFITS OF anyCAP™ LDO TOPOLOGY

- Internal C_{COMP} Dominates Response Rolloff
- C_L Can Range from 0.47µF(min) to Infinity
- Low and Ultra-Low C_L ESR is OK
- MLCC Types for C_L Work, is Physically Smallest Solution
- No ESR Exclusion Zones
- Fast Load Transient Response and Good Line Rejection

Figure 2.34

The anyCAP™ LDO series devices

The major specifications of the anyCAP™ series of LDO regulators are summarized in Figure. 2.35. The devices include both single and dual output parts, with current capabilities ranging from 50 to 200mA. Rather than separate individual specifications for output tolerance, line and load regulation, plus temperature, the anyCAP™ series devices are rated simply for a combined total accuracy figure. This accuracy is either 0.8% at 25°C, or 1.4% over the temperature range with the device operating over an input range of V_{OUT} +0.3 (or 0.5V), up to 12V. With total accuracy being covered by one clear specification, the designer can then achieve a higher degree of confidence. It is important to note that this method of specification also includes operation within the regulator dropout range (unlike some LDO parts specified for higher input-output voltage difference conditions).

anyCAP™ SERIES LDO REGULATOR DEVICES

Part Number	V_{MIN} @ I_L (V, typ/max)	I_L (mA)	Accuracy (±% @ 25°C / ±% Full)	Package (All SO-8 are Thermal coastline)	Comment (Singles have NR, SD, ERR; Dual no NR)
ADP3300	0.08 / 0.17	50	0.8 / 1.4	SOT-23-6	Single
ADP3301	0.10 / 0.2	100	0.8 / 1.4	SO-8	Single
ADP3302	0.10 / 0.2	100	0.8 / 1.4	SO-8	Dual
ADP3303	0.18 / 0.4	200	0.8 / 1.4	SO-8	Single
ADP3307	0.13 / 0.22	100	0.8 / 1.4	SOT-23-6	Single

Figure 2.35

Functional Diagram and Basic 50 mA LDO Regulator

A functional diagram common to the various devices of the ADP330X series LDO regulators is shown by Figure 2.36. Operation of the various pins and internal functions is discussed below.

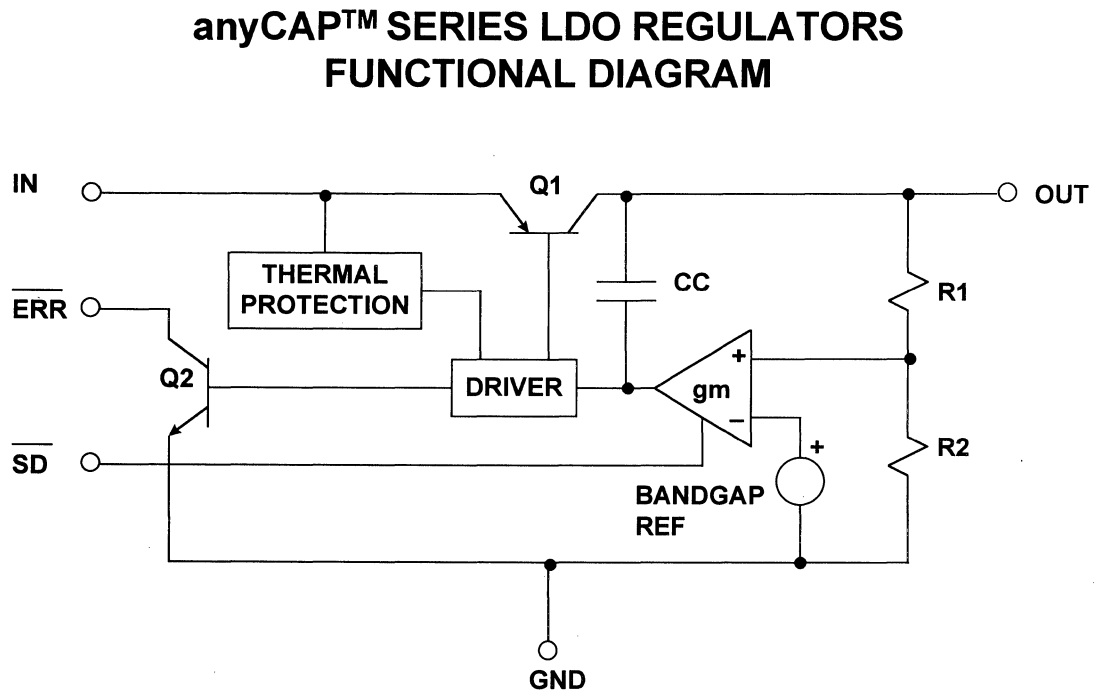

Figure 2.36

In application, the use of the anyCAP™ series of LDOs is simple, as shown by a basic 50mA ADP3300 regulator, in Figure 2.37. This circuit is a general one, to illustrate points common to the entire device series. The ADP3300 is a basic LDO regulator device, designed for fixed output voltage applications while operating from sources over a range of 3 to 12V and a temperature range of –40 to +85°C. The actual ADP3300 device ordered would be specified as ADP3300ART-YY, where the "YY" is a voltage designator suffix such as 2.7, 3, 3.2, 3.3, or 5, for those respective voltages. The "ART" portion of the part number designates the SOT23 6-lead package. The example circuit shown produces 5.0V with the use of the ADP3300-5.

In operation, the circuit will produce its rated 5V output for loads of 50mA or less, and for input voltages above 5.3V (V_{OUT} + 0.3V), when the shutdown input is in a HIGH state. This can be accomplished either by a logic HIGH control input to the $\overline{SD}$ pin, or by simply tying this pin to V_{IN}. When $\overline{SD}$ is LOW (or tied to ground), the regulator shuts down, and draws a quiescent current of 1μA or less.

A BASIC ADP3300 50mA LDO REGULATOR CIRCUIT

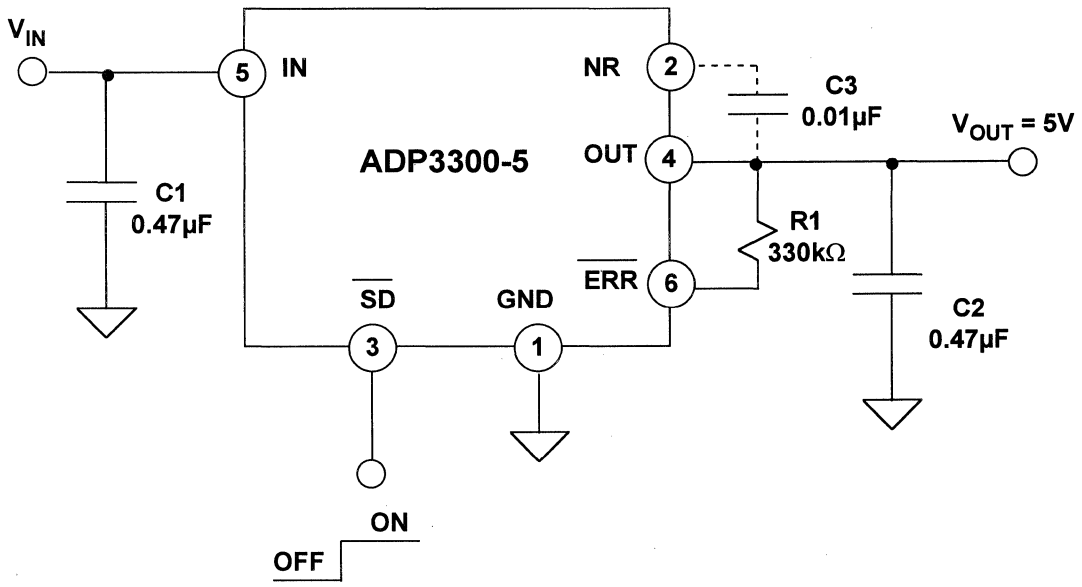

Figure 2.37

The ADP3300 and other anyCAP™ series devices maintain regulation over a wide range of load, input voltage and temperature conditions. However, when the regulator is overloaded or entering the dropout region (for example, by a reduction in the input voltage) the open collector $\overline{\text{ERR}}$ pin becomes active, by going to a LOW or conducting state. Once set, the $\overline{\text{ERR}}$ pin's internal hysteresis keeps the output low, until some margin of operating range is restored. In the circuit of Fig. 2.37, R1 is a pullup resistor for the $\overline{\text{ERR}}$ output, E_{OUT}. This resistor can be eliminated if the load being driven provides a pullup current.

The $\overline{\text{ERR}}$ function can also be activated by the regulator's over temperature protection circuit, which trips at 165°C. These internal current and thermal limits are intended to protect the device against accidental overload conditions. For normal operation, device power dissipation should be externally limited by means of heat sinking, air flow, etc. so that junction temperatures will not exceed 125°C.

A capacitor, C3, connected between pins 2 and 4, can be used for an optional noise reduction (NR) feature. This is accomplished by AC-bypassing a portion of the regulator's internal scaling divider, which has the effect of reducing the output noise ~10 dB. When this option is exercised, only low leakage 10 -100nF capacitors should be used. Also, input and output capacitors should be changed to 1 and 4.7µF values respectively, for lowest noise and the best overall performance. Note that the noise reduction pin is internally connected to a high impedance node, so connections to it should be carefully done to avoid noise. PC traces and pads connected to this pin should be as short and small as possible.

LDO Regulator Thermal Considerations

To determine a regulator's power dissipation, calculate it as follows:

$$P_D = (V_{IN} - V_{OUT})(I_L) + (V_{IN})(\text{Iground}),$$

where I_L and Iground are load and ground current, and V_{IN} and V_{OUT} are the input and output voltages respectively. Assuming I_L= 50mA, Iground = 0.5mA, V_{IN} = 8V, and V_{OUT} = 5V, the device power dissipation is:

$$P_D = (8 - 5)(0.05) + (8)(0.0005) = 0.150 + .004 = 0.154 \text{ W}.$$

To determine the regulator's temperature rise, ΔT, calculate it as follows:

$$\Delta T = T_J - T_A = P_D \times \theta_{JA} = 0.154\text{W} \times 165°\text{C/W} = 25.4°\text{C}.$$

With a maximum junction temperature of 125°C, this yields a calculated maximum safe ambient operating temperature of 125 – 25.4°C, or just under 100°C. Since this temperature is in excess of the device's rated temperature range of 85°C, the device will then be operated conservatively at an 85°C (or less) maximum ambient temperature.

These general procedures can be used for other devices in the series, substituting the appropriate θ_{JA} for the applicable package, and applying the remaining operating conditions. For reference, a complete tutorial section on thermal management is contained in Chapter 8.

In addition, layout and PCB design can have a significant influence on the power dissipation capabilities of power management ICs. This is due to the fact that the surface mount packages used with these devices rely heavily on thermally conductive traces or pads, to transfer heat away from the package. Appropriate PC layout techniques should then be used to remove the heat due to device power dissipation. The following general guidelines will be helpful in designing a board layout for lowest thermal resistance in SOT-23 and SO-8 packages:

1. *PC board traces with large cross sectional areas remove more heat. For optimum results, use large area PCB patterns with wide and heavy (2 oz.) copper traces, placed on the uppermost side of the PCB.*

2. *Electrically connect dual V_{IN} and V_{OUT} pins in parallel, as well as to the corresponding V_{IN} and V_{OUT} large area PCB lands.*

3. *In cases where maximum heat dissipation is required, use double-sided copper planes connected with multiple vias.*

4. *Where possible, increase the thermally conducting surface area(s) openly exposed to moving air, so that heat can be removed by convection (or forced air flow, if available).*

5. *Do* not *use solder mask or silkscreen on the heat dissipating traces, as they increase the net thermal resistance of the mounted IC package.*

A real life example visually illustrates a number of the above points far better than words can do, and is shown in Figure 2.38, a photo of the ADP3300 1.5" square evaluation PCB. The boxed area on the board represents the actual active circuit area.

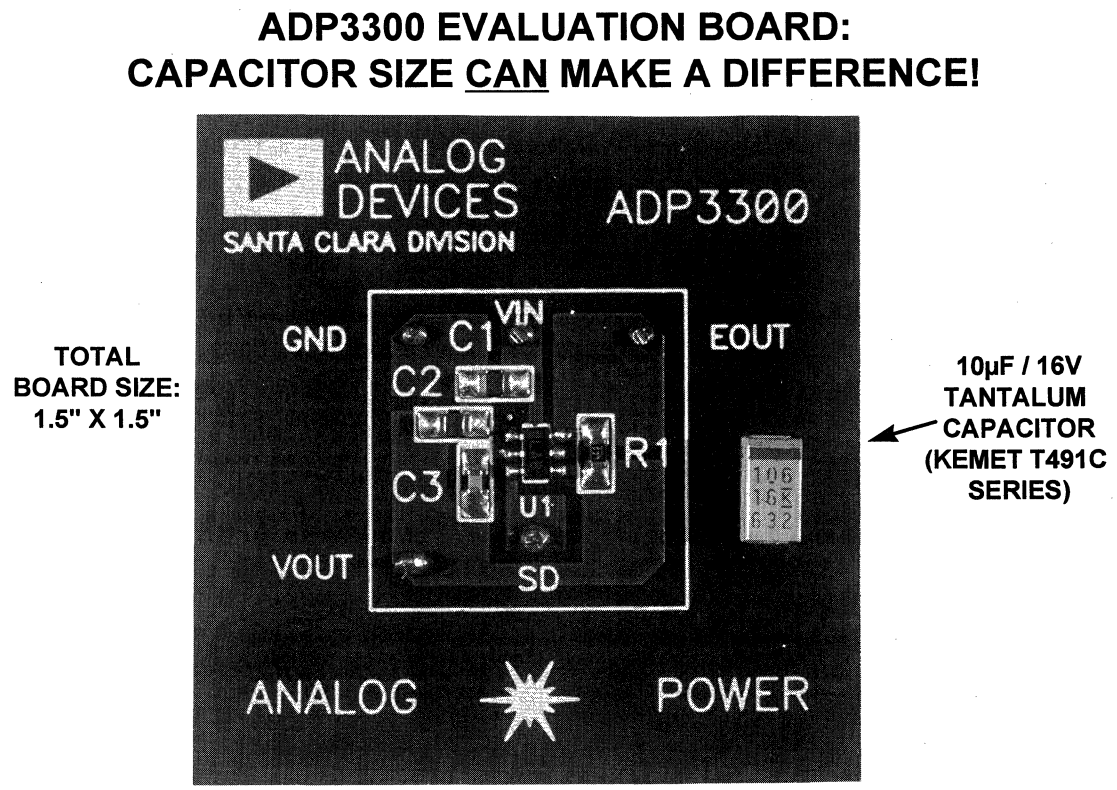

Figure 2.38

In this figure, a large cross section conductor area can be seen associated with pin 4 and V_{OUT}, the large "U" shaped trace at the lower part within the boxed outline.

Also, the effect of the anyCAP™ design on capacitor size can be noted from the tiny size of the C1 and C2 0.47µF input and output capacitors, near the upper left of the boxed area. For comparison purposes, a 10µF/16V tantalum capacitor (Kemet T491C-series) is also shown outside the box, as it might be used on a more conventional LDO circuit. It is several times the size of output capacitor C2.

Recent developments in packaging have led to much improved thermal performance for power management ICs. The anyCAP™ LDO regulator family capitalizes on this most effectively, using a thermally improved leadframe as the basis for all 8 pin devices. This package is called a "Thermal Coastline" design, and is shown in Figure. 2.39. The foundation of the improvement in heat transfer is related to two key parameters of the leadframe design, distance and width. The payoff comes in the reduced thermal resistance of the leadframe based on the Thermal Coastline,

only 90°C/W versus 160°C/W for a standard SO-8 package. The increased dissipation of the Thermal Coastline allows the anyCAP™ series of SO-8 regulators to support more than one watt of dissipation at 25°C.

anyCAP™ SERIES REGULATORS IN SO-8 USE THERMAL COASTLINE PACKAGES

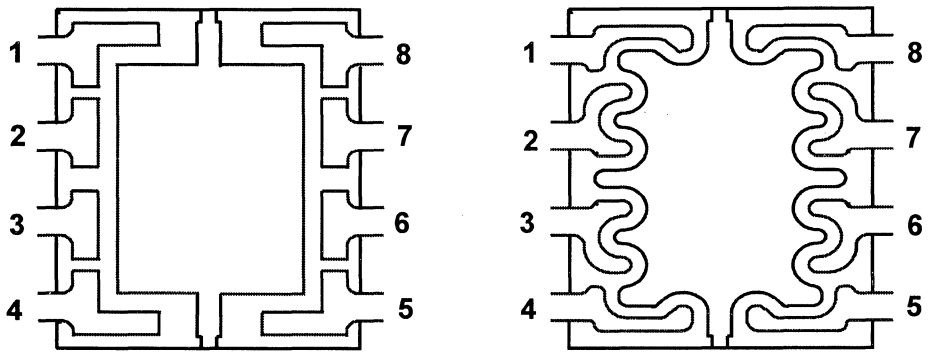

Figure 2.39

Additional insight into how the new leadframe increases heat transfer can be appreciated by Figure. 2.40. In this figure, it can be noted how the spacing of the Thermal Coastline paddle and leads shown on the right is reduced, while the width of the lead ends are increased, versus the standard leadframe, on the left.

DETAILS OF THERMAL COASTLINE PACKAGE

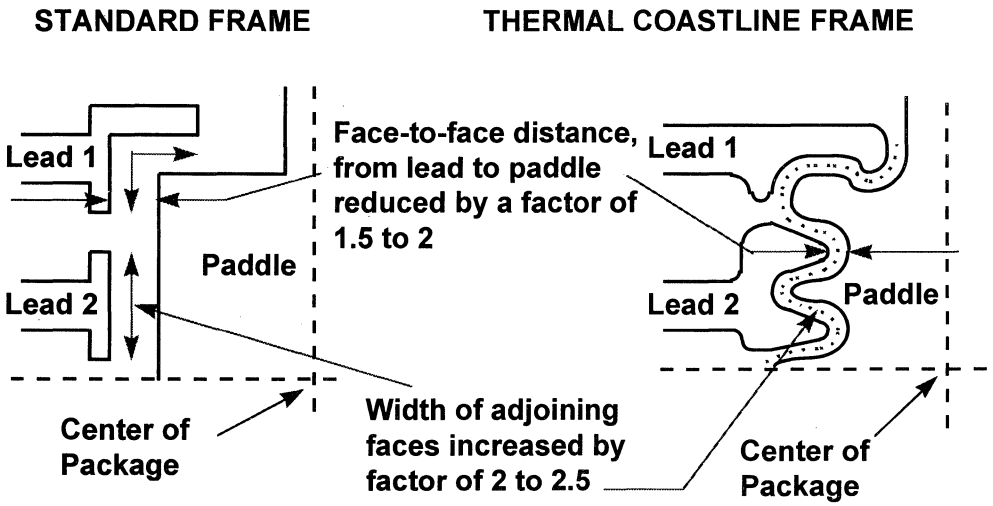

Figure 2.40

LDO REGULATOR CONTROLLERS

To complement the anyCAP™ series of standalone LDO regulators, there is also the LDO *regulator controller*. The regulator controller IC picks up where the standalone regulator IC is no longer useful in either load current or power dissipation terms, and uses an external PMOS FET for the pass device. The ADP3310 is a basic LDO regulator controller device, designed for fixed output voltage applications while operating from sources over a range of 3.8 to 15V and a temperature range of –40 to +85°C. The actual ADP3310 device ordered would be specified as ADP3310AR-YY, where the "YY" is a voltage designator suffix such as 2.8, 3, 3.3, or 5, for those respective voltages. The "AR" portion of the part number designates the SO-8 Thermal Coastline 8-lead package. A summary of the main features of the ADP3310 device is listed in Figure 2.41.

anyCAP™ ADP3310 LDO REGULATOR CONTROLLER FEATURES

- **Controller drives external PMOS power FETs**
  - **User FET choice determines I_L and V_{MIN} performance**
  - **Small, 2 chip regulator solution handles up to 10A**
- **Advantages compared to integrated solutions**
  - **High accuracy (1.5%) fixed voltages; 2.8, 3, 3.3, or 5V**
  - **User flexibility (selection of FET for performance)**
  - **Small footprint with anyCAP™ controller and SMD FET**
  - **Kelvin output sensing possible**
  - **Integral, low-loss current limit sensing for protection**

Figure 2.41

Regulator Controller Differences

An obvious basic difference of the regulator controller versus a stand alone regulator is the removal of the pass device from the regulator chip. This design step has both advantages and disadvantages. A positive is that the external PMOS pass device can be chosen for the exact size, package, current rating and power handling which is most useful to the application. This approach allows the same basic controller IC to be useful for currents of several hundred mA to more than 10A, simply by choice of the FET. Also, since the regulator controller IC's Iground of 800μA results is very little power dissipation, its thermal drift will be enhanced. On the downside, there are two packages now used to make up the regulator function. And, current limiting (which can be made completely integral to a standalone IC LDO regulator) is now a function which must be split between the regulator controller IC and an external sense resistor. This step also increases the dropout voltage of the LDO regulator controller somewhat, by about 50mV.

A functional diagram of the ADP3310 regulator controller is shown in Figure 2.42. The basic error amplifier, reference and scaling divider of this circuit are similar to the standalone anyCAP™ regulator, and will not be described in detail. The regulator controller version does share the same cap load immunity of the standalone versions, and also has a shutdown function, similarly controlled by the EN (enable) pin.

The main differences in the regulator controller IC architecture is the buffered output of the amplifier, which is brought out on the GATE pin, to drive the external PMOS FET. In addition, the current limit sense amplifier has a built in 50mV threshold voltage, and is designed to compare the voltage between the V_{IN} and IS pins. When this voltage exceeds 50mV, the current limit sense amplifier takes over control of the loop, by shutting down the error amplifier and limiting output current to the preset level.

FUNCTIONAL BLOCK DIAGRAM OF anyCAP™ SERIES LDO REGULATOR CONTROLLER

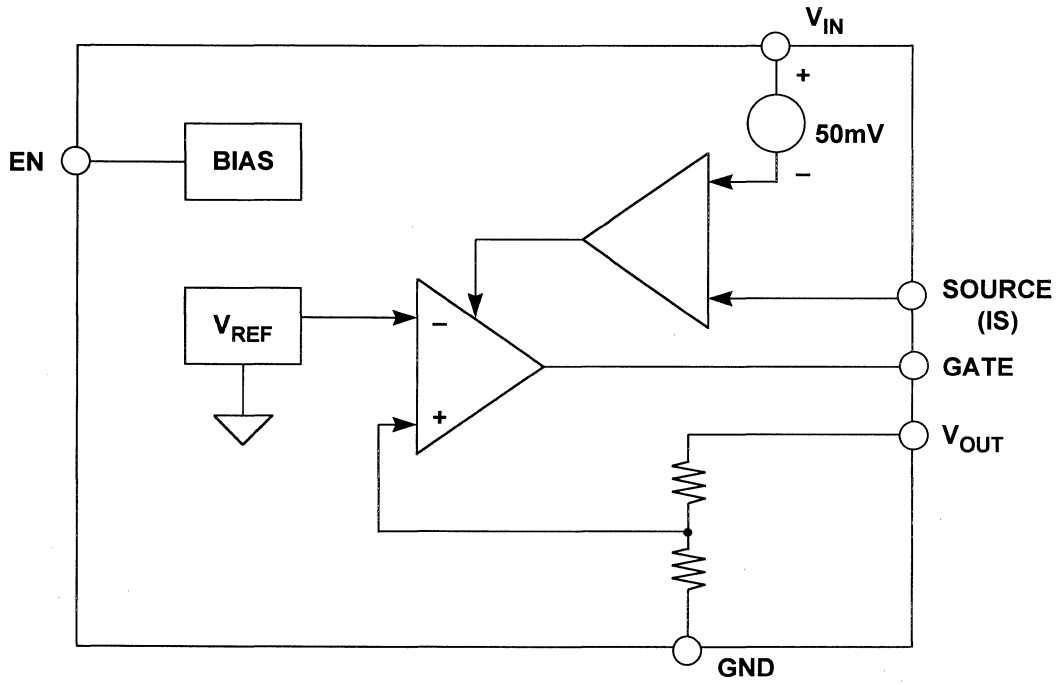

Figure 2.42

A Basic 5V/1A LDO Regulator Controller

An LDO regulator controller is easy to use, since a PMOS FET, a resistor and two relatively small capacitors (one at the input, one at the output) is all that is needed to form an LDO regulator. The general configuration is shown by Figure 2.43, an LDO suitable as a 5V/1A regulator operating from a V_{IN} of 6V, using the ADP3310-5 controller IC.

This regulator is stable with virtually any good quality output capacitor used for C_L (as is true with the other anyCAP™ devices). The actual C_L value required and its associated ESR depends on the gm and capacitance of the external PMOS device. In general, a 10µF capacitor at the output is sufficient to ensure stability for load currents up to 10A. Larger capacitors can also be used, if high output surge currents are present. In such cases, low ESR capacitors such as OS-CON electrolytics are preferred, because they offer lowest ripple on the output. For less demanding requirements, a standard tantalum or aluminum electrolytic can be adequate. When an aluminum electrolytic is used, it should be qualified for adequate performance over temperature. The input capacitor, C_{IN}, is only necessary when the regulator is several inches or more distant from the raw DC filter capacitor. However, since it is a small type, it is usually prudent to use it in most instances, located close to the V_{IN} pin of the regulator.

A BASIC ADP3310 PMOS FET 1A LDO REGULATOR CONTROLLER CIRCUIT

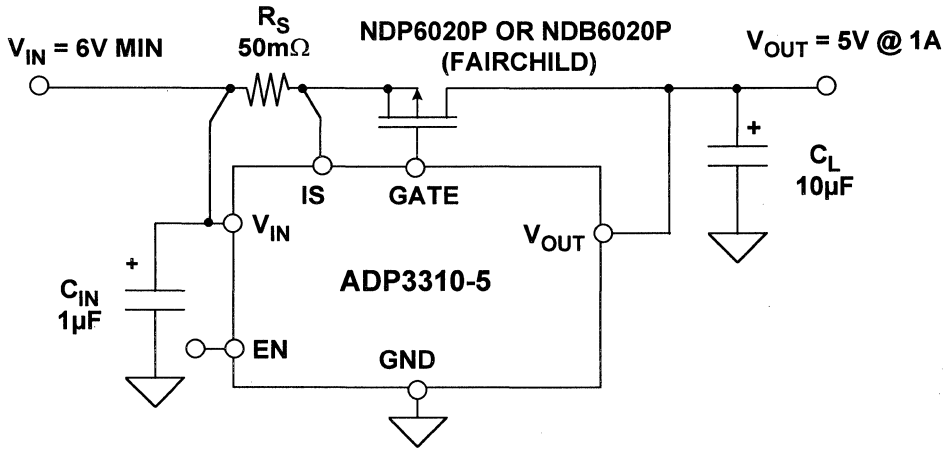

Figure 2.43

Selecting the Pass Device

The type and size of the pass transistor are determined by a set of requirements for threshold voltage, input-output voltage differential, load current, power dissipation, and thermal resistance. An actual PMOS pass device selected must satisfy all of these electrical requirements, plus physical and thermal parameters. There are a number of manufacturers offering suitable devices in packages ranging from SO-8 up through TO-220 in size.

To ensure that the maximum available drive from the controller will adequately drive the FET under worst case conditions of temperature range and manufacturing tolerances, the maximum drive from the controller ($V_{GS(DRIVE)}$) to the pass device must be determined. This voltage is calculated as follows:

$$V_{GS(DRIVE)} = V_{IN} - V_{BE} - \left(I_{L(MAX)}\right)\left(R_S\right),$$

where V_{IN} is the minimum input voltage, $I_{L(MAX)}$ is the maximum load current, R_S the sense resistor, and V_{BE} is a voltage internal to the ADP3310 (~ 0.5 @ high temp, 0.9 cold, and 0.7V at room temp). Note that since $I_{L(MAX)} \times R_S$ will be no more than 75mV, and V_{BE} at cold temperature ≅0.9V, this equation can be further simplified to:

$$V_{GS(DRIVE)} \cong V_{IN} - 1V .$$

In the Figure 2.43 example, V_{IN} = 6V and V_{OUT} = 5V, so $V_{GS(DRIVE)}$ is 6 – 1 = 5V.

It should be noted that the above two equations apply to FET drive voltages which are *less* than the typical gate-to-source clamp voltage of 8V (built into the ADP3310, for the purposes of FET protection).

An overall goal of the design is to then select an FET which will have an $R_{DS(ON)}$ sufficiently low so that the resulting dropout voltage will be less than $V_{IN} - V_{OUT}$, which in this case is 1V. For the NDP6020P used in Fig. 2.43 (see Reference 10), this device achieves an $R_{DS(ON)}$ of 70 milliohms (max) with a V_{GS} of 2.7V, a voltage drive appreciably less than the ADP3310's $V_{GS(DRIVE)}$ of 5V. The dropout voltage V_{MIN} of this regulator configuration is the sum of two series voltage drops, the FET's drop plus the drop across R_S, or:

$$V_{MIN} = I_{L(MAX)} \left(R_{DS(ON)} + R_S\right).$$

In the design here, the two resistances are roughly comparable to one another, so the net V_{MIN} will be 1A × (50+70 milliohms) = 120mV.

For a design safety margin, use a FET with a rated V_{GS} at the required R_{DS}, with a substantial headroom between the applicable ADP3310 $V_{GS(DRIVE)}$ and the applicable V_{GS} rating for the FET. In the case here, there is ample margin, with 5V of drive and a V_{GS} of 2.7V. It should be borne in mind that the FET's V_{GS} and $R_{DS(ON)}$ will change over temperature, but for the NDP6020P device even these variations and a V_{GS} of 4.5V are still possible with the circuit as shown. With a rated minimum DC input of 6V, this means that the design is conservative with 5V output. In practice, the circuit will typically operate with input voltage minimums on the order of V_{OUT} plus the dropout of 120mV, or ~ 5.12V. Since the NDP6020P is also a fairly low threshold device, it will typically operate at lower output voltages, down to about 3V.

In the event the output is shorted to ground, the pass device chosen must be able to conduct the maximum short circuit current, both instantaneously and longer term.

Thermal Design

The maximum allowable thermal resistance between the FET junction and the highest expected ambient temperature must be taken into account, to determine the type of FET package and heat sink used (if any).

Whenever possible to do so reliably, the FET pass device can be directly mounted to the PCB, and the available PCB copper lands used as an effective heat sink. This heat sink philosophy will likely be adequate when the power to be dissipated in the FET is on the order of 1-2W or less. Note that the very nature of an LDO helps this type of design immensely, as the lower voltage drop across the pass device reduces the power to be dissipated. Under normal conditions for example, Q1 of Figure 2.43 dissipates less than 1W at a current of 1A, since the drop across the FET is less than 1V.

To use PCB lands as effective heat sinks with SO-8 and other SMD packages, the pass device manufacturer's recommendations for the lowest θ_{JA} mounting should be followed (see References 11 and 12). In general these suggestions will likely parallel the 5 rules noted above, under "LDO regulator thermal considerations" for SO-8 and SOT-23 packaged anyCAP™ LDOs. For lowest possible thermal resistance, also connect multiple FET pins together, as follows:

Electrically connect multiple FET source and drain pins in parallel, as well as to the corresponding R_S and V_{OUT} large area PCB lands.

Using 2 oz. copper PCB material and one square inch of copper PCB land area as a heatsink, it is possible to achieve a net thermal resistance, θ_{JA}, for mounted SO-8 devices on the order of 60°C/W or less. Such data is available for SO-8 power FETs (see Reference 11). There are also a variety of larger packages with lower thermal resistance than the SO-8, but still useful with surface mount techniques. Examples are the DPAK and D²PAK, etc.

For higher power dissipation applications, corresponding to thermal resistance of 50°C/W or less, a bolt-on external heat sink is required to satisfy the θ_{JA} requirement. Compatible package examples would be the TO-220 family, which is used with the NDP6020P example of Fig. 2.43.

Calculating thermal resistance for V_{IN} = 6.7V, V_{OUT} = 5V, and I_L = 1A:

$$\theta_{JA} = \frac{T_J - T_{A(MAX)}}{V_{DS(MAX)} \cdot I_L},$$

where T_J is the pass device junction temperature limit, $T_{A(MAX)}$ is the maximum ambient temperature, $V_{DS(MAX)}$ is the maximum pass device drain-source voltage, and $I_{L(MAX)}$ is the maximum load current.

Inserting some example numbers of 125°C as a max. junction temp for the NDP6020P, a 75°C expected ambient, and the $V_{DS(MAX)}$ and $I_{L(MAX)}$ figures of 1.7V and 1A, the required θ_{JA} works out to be 125 – 75/1.7 = 29.4°C/W. This can be met with a very simple heat sink, which is derived as follows.

The NDP6020P in the TO-220 package has a junction-case thermal resistance, θ_{JC}, of 2°C/W. The required external heatsink's thermal resistance, θ_{CA}, is determined as follows:

$$\theta_{CA} = \theta_{JA} - \theta_{JC},$$

where θ_{CA} is the required heat sink case-to-ambient thermal resistance, θ_{JA} is the calculated *overall* junction-to-ambient thermal resistance, and θ_{JC} is the pass device junction-to-case thermal resistance, which in this case is 2°C/W typical for TO-220 devices, and NDP6020P.

$$\theta_{CA} = 29.4°C/W - 2°C/W = 27.4°C/W.$$

For a safety margin, select a heatsink with a θ_{CA} *less* than the results of this calculation. For example, the Aavid TO-220 style clip on heat sink # 576802 has a θ_{CA} of 18.8°C/W, and in fact many others have performance of 25°C/W or less. As an alternative, the NDB6020P D²PAK FET pass device could be used in this same design, with an SMD style heat sink such as the Aavid 573300 series used in conjunction with an internal PCB heat spreader.

Note that many LDO applications like the above will calculate out with very modest heat sink requirements. This is fine, as long as the output never gets shorted! With a shorted output, the current goes to the limit level (as much as 1.5A in this case), while the voltage across the pass device goes to V_{IN} (which could also be at a maximum). In this case, the new pass device dissipation for short circuit conditions becomes 1.5A × 6.7V, or 10W. Supporting this level of power continuously will require the entire heat sink situation to be re-evaluated, as what was adequate for 1.7W will simply not be adequate for 10W. In fact, the required heat sink θ_{CA} is about 3°C/W to support the 10W safely on a continuous basis, which requires a much larger heat sink.

Note that a general overview of thermal design and heat sink selection is included in section 8.

Sensing Resistors for LDO Controllers

Current limiting in the ADP3310 controller is achieved by choosing an appropriate external current sense resistor, R_S, which is connected between the controller's V_{IN} and IS (source) pins. An internally derived 50 mV current limit threshold voltage appears between these pins, to establish a comparison threshold for current limiting. This 50mV determines the threshold where current limiting begins. For a continuous current limiting, a foldback mode is established, with dissipation controlled by reducing the gate drive. The net effect is that the ultimate current limit level is a factor of 2/3 of maximum. The foldback limiting reduces the power dissipated in the pass transistor substantially.

To choose a sense resistor for a maximum output current I_L, R_S is calculated as follows:

$$R_S = \frac{0.05}{K_F \cdot I_L}.$$

In this expression, the nominal 50mV current limit threshold voltage appears in the numerator. In the denominator appears a scaling factor K_F, which can be either 1.0 or 1.5, plus the maximum load current, I_L. For example, if a scaling factor of 1.0 is

to be used for a 1A I_L, the R_S calculation is straightforward, and 50 milliohms is the correct R_S value.

However, to account for uncertainties in the threshold voltage and to provide a more conservative output current margin, a scaling factor of $K_F = 1.5$ can alternately be used. When this approach is used, the same 1A I_L load conditions will result in a 33 milliohm R_S value. In essence, the use of the 1.5 scaling factor takes into account the foldback scheme's reduction in output current, allowing higher current in the limit mode.

The simplest and least expensive sense resistor for high current applications such as Figure 2.43 is a copper PCB trace controlled in both thickness and width. Both the temperature dependence of copper and the relative size of the trace must be taken into account in the resistor design. The temperature coefficient of resistivity for copper has a positive temperature coefficient of +0.39%/°C. This natural copper TC, in conjunction with the controller's PTAT based current limit threshold voltage, can provide for a current limit characteristic which is simple and effective over temperature.

The table of Figure 2.44 provides resistance data for designing PCB copper traces with various PCB copper thickness (or weight), in ounces of copper per square foot area. To use this information, note that the center column contains a resistance coefficient, which is the conductor resistance in milliohms/inch, divided by the trace width, W. For example, the first entry, for 1/2 ounce copper is 0.983 milliohms/inch/W. So, for a reference trace width of 0.1", the resistance would be 9.83 milliohms/inch. Since these are all linear relationships, everything scales for wider/skinnier traces, or for differing copper weights. As an example, to design a 50 milliohm R_S for the circuit of Fig. 2.43 using 1/2 ounce copper, a 2.54" length of a 0.05" wide PCB trace could be used.

PRINTED CIRCUIT COPPER RESISTANCE DESIGN FOR LDO CONTROLLERS

Copper Thickness	Resistance Coefficient, Milliohms / inch/ W (trace width W in inches)	Reference 0.1 Inch wide trace, Milliohms / inch
1/2 oz / ft^2	0.983 / W	9.83
1 oz / ft^2	0.491 / W	4.91
2 oz / ft^2	0.246 / W	2.46
3 oz / ft^2	0.163 / W	1.63

Figure 2.44

To minimize current limit sense voltage errors, the two connections to R_S should be made four-terminal style, as is noted in Figure 2.43 (again). It is not absolutely necessary to actually use four-terminal style resistors, except for the highest current levels. However, as a minimum, the heavy currents flowing in the source circuit of the pass device should not be allowed to flow in the ADP3310 sense pin traces. To minimize such errors, the V_{IN} connection trace to the ADP3310 should connect close to the body of R_S (or the resistor's input sense terminal), and the IS connection trace should also connect close to the resistor body (or the resistor's output sense terminal). Four-terminal wiring is increasingly important for output currents of 1A or more.

Alternately, an appropriate selected sense resistor such as surface mount sense devices available from resistor vendors can be used (see Reference 13). Sense resistor R_S may not be needed in all applications, if a current limiting function is provided by the circuit feeding the regulator. For circuits that don't require current limiting, the IS and V_{IN} pins of the ADP3310 must be tied together.

PCB-Layout Issues

For best voltage regulation, place the load as close as possible to the controller device's V_{OUT} and GND pins. Where the best regulation is required, the V_{OUT} trace from the ADP3310 and the pass device's drain connection should connect to the positive load terminal via separate traces. This step (Kelvin sensing) will keep the heavy load currents in the pass device's drain out of the feedback sensing path, and thus maximize output accuracy. Similarly, the unregulated input common should connect to the common side of the load via a separate trace from the ADP3310 GND pin.

These points are summarized in the "Techniques" discussion of section 8, around Figures. 8.10 and 8.11 specifically.

A 2.8V/8A LDO Regulator Controller

With seemingly minor changes to the basic 1A LDO circuit used in Fig. 2.43, an 8A LDO regulator controller can be configured, as shown in Figure 2.45. This circuit uses an ADP3310- 2.8, to produce a 2.8V output. The sense resistor is dropped to 5 milliohms, which supports currents of up to 10A (or about 6.7A, with current limiting active). Four-terminal wiring should be used with the sense resistor to minimize errors.

The most significant change over the more generic schematic of Fig. 2.43 is the use of multiple, low ESR input and output bypass capacitors. At the output, C2 is a bank of 4 × 220µF OS-CON type capacitors, in parallel with 2 × 10µF MLCC chip type capacitors. These are located right at the load point with minimum inductance wiring, plus separate wiring back to the V_{OUT} pin of the ADP3310 and the drain of the pass device. This wiring will maximize the DC output accuracy, while the multiple capacitors will minimize the transient errors at the point-of-load. In addition, multiple bypasses on the regulator input in the form of C1 minimizes the transient errors at the regulator's V_{IN} pin.

A 2.8V/8A LDO REGULATOR CONTROLLER

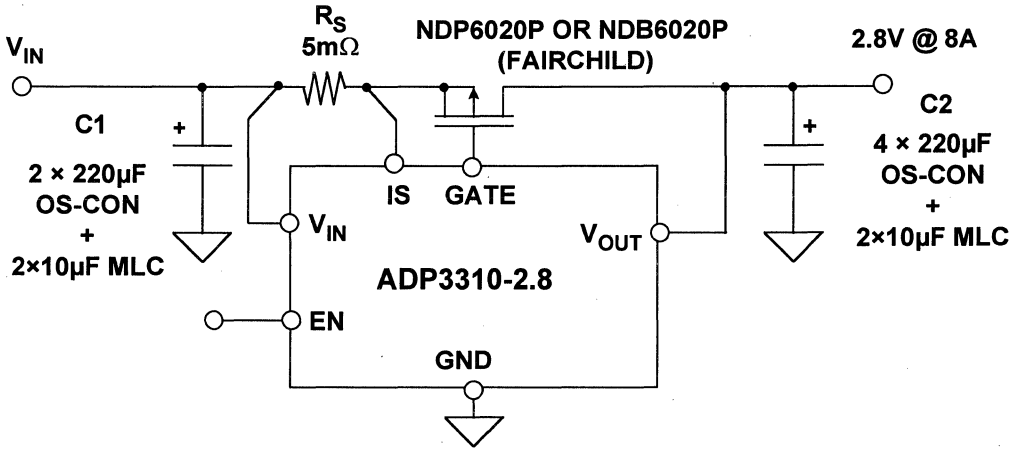

Figure 2.45

Heat sink requirements for the pass device in this application will be governed by the loading and input voltage, and should be calculated by the procedures discussed above.

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SECTION 3

SWITCHING REGULATORS

- Applications of Switching Regulators
- Inductor and Capacitor Fundamentals
- Ideal Step-Down (Buck) Converter
- Ideal Step-Up (Boost) Converter
- Buck-Boost Topologies
- Other Non-Isolated Switcher Topologies
- Isolated Switching Regulator Topologies
- Switch Modulation Techniques
- Control Techniques
- Diode and Switch Considerations
- Inductor Considerations
- Capacitor Considerations
- Input and Output Filtering

SECTION 3
SWITCHING REGULATORS
Walt Kester, Brian Erisman

INTRODUCTION

Virtually all of today's electronic systems require some form of power conversion. The trend toward lower power, portable equipment has driven the technology and the requirement for converting power efficiently. Switchmode power converters, often referred to simply as "switchers", offer a versatile way of achieving this goal. Modern IC switching regulators are small, flexible, and allow either step-up (boost) or step-down (buck) operation.

When switcher functions are integrated and include a switch which is part of the basic power converter topology, these ICs are called "switching regulators". When no switches are included in the IC, but the signal for driving an external switch is provided, it is called a "switching regulator controller". Sometimes - usually for higher power levels - the control is not entirely integrated, but other functions to enhance the flexibility of the IC are included instead. In this case the device might be called a "controller" of sorts - perhaps a "feedback controller" if it just generates the feedback signal to the switch modulator. It is important to know what you are getting in your controller, and to know if your switching regulator is really a regulator or is it just the controller function.

Also, like switchmode power conversion, linear power conversion and charge pump technology offer both regulators and controllers. So within the field of power conversion, the terms "regulator" and "controller" can have wide meaning.

The most basic switcher topologies require only one transistor which is essentially used as a switch, one diode, one inductor, a capacitor across the output, and for practical but not fundamental reasons, another one across the input. A practical converter, however, requires several additional elements, such as a voltage reference, error amplifier, comparator, oscillator, and switch driver, and may also include optional features like current limiting and shutdown capability. Depending on the power level, modern IC switching regulators may integrate the entire converter except for the main magnetic element(s) (usually a single inductor) and the input/output capacitors. Often, a diode, the one which is an essential element of basic switcher topologies, cannot be integrated either. In any case, the complete power conversion for a switcher cannot be as integrated as a linear regulator, for example. The requirement of a magnetic element means that system designers are not inclined to think of switching regulators as simply "drop in" solutions. This presents the challenge to switching regulator manufacturers to provide careful design guidelines, commonly-used application circuits, and plenty of design assistance and product support. As the power levels increase, ICs tend to grow in complexity because it becomes more critical to optimize the control flexibility and precision. Also, since the switches begin to dominate the size of the die, it becomes more cost effective to remove them and integrate only the controller.

The primary limitations of switching regulators as compared to linear regulators are their output noise, EMI/RFI emissions, and the proper selection of external support components. Although switching regulators do not necessarily require transformers, they do use inductors, and magnetic theory is not generally well understood. However, manufacturers of switching regulators generally offer applications support in this area by offering complete data sheets with recommended parts lists for the external inductor as well as capacitors and switching elements.

One unique advantage of switching regulators lies in their ability to convert a given supply voltage with a known voltage range to virtually any given desired output voltage, with no "first order" limitations on efficiency. This is true regardless of whether the output voltage is higher or lower than the input voltage - the same or the opposite polarity. Consider the basic components of a switcher, as stated above. The inductor and capacitor are, ideally, reactive elements which dissipate no power. The transistor is effectively, ideally, a switch in that it is either "on", thus having no voltage dropped across it while current flows through it, or "off", thus having no current flowing through it while there is voltage across it. Since either voltage or current are always zero, the power dissipation is zero, thus, ideally, the switch dissipates no power. Finally, there is the diode, which has a finite voltage drop while current flows through it, and thus dissipates *some* power. But even that can be substituted with a synchronized switch, called a "synchronous rectifier", so that it ideally dissipates no power either.

Switchers also offer the advantage that, since they inherently require a magnetic element, it is often a simple matter to "tap" an extra winding onto that element and, often with just a diode and capacitor, generate a reasonably well regulated additional output. If more outputs are needed, more such taps can be used. Since the tap winding requires no electrical connection, it can be isolated from other circuitry, or made to "float" atop other voltages.

Of course, nothing is ideal, and everything has a price. Inductors have resistance, and their magnetic cores are not ideal either, so they dissipate power. Capacitors have resistance, and as current flows in and out of them, they dissipate power, too. Transistors, bipolar or field-effect, are not ideal switches, and have a voltage drop when they are turned on, plus they cannot be switched instantly, and thus dissipate power while they are turning on or off.

As we shall soon see, switchers create ripple currents in their input and output capacitors. Those ripple currents create voltage ripple and noise on the converter's input and output due to the resistance, inductance, and finite capacitance of the capacitors used. That is the *conducted* part of the noise. Then there are often ringing voltages in the converter, parasitic inductances in components and PCB traces, and an inductor which creates a magnetic field which it cannot perfectly contain within its core - all contributors to *radiated* noise. Noise is an inherent by-product of a switcher and must be controlled by proper component selection, PCB layout, and, if that is not sufficient, additional input or output filtering or shielding.

INTEGRATED CIRCUIT SWITCHING REGULATORS

- **Advantages:**
  - **High Efficiency**
  - **Small**
  - **Flexible - Step-Up (Boost), Step-Down (Buck), etc.**

- **Disadvantages**
  - **Noisy (EMI, RFI, Peak-to-Peak Ripple)**
  - **Require External Components (L's, C's)**
  - **Designs Can Be Tricky**
  - **Higher Total Cost Than Linear Regulators**

- **"Regulators" vs. "Controllers"**

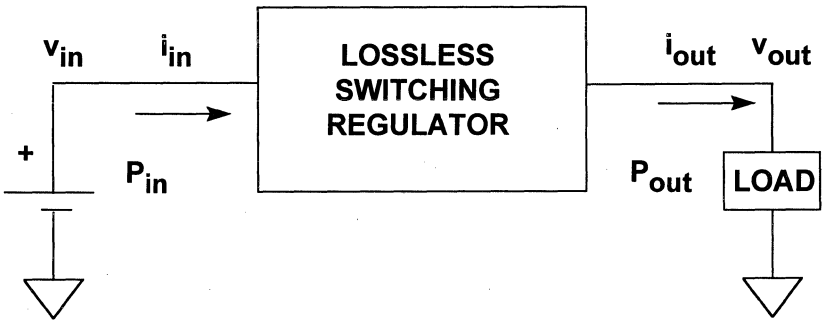
Figure 3.1

Though switchers can be designed to accommodate a range of input/output conditions, it is generally more costly in non-isolated systems to accommodate a requirement for both voltage step-up and step-down. So generally it is preferable to limit the input/output ranges such that one or the other case can exist, but not both, and then a simpler converter design can be chosen.

The concerns of minimizing power dissipation and noise as well as the design complexity and power converter versatility set forth the limitations and challenges for designing switchers, whether with regulators or controllers.

The ideal switching regulator shown in Figure 3.2 performs a voltage conversion and input/output energy transfer without loss of power by the use of purely reactive components. Although an actual switching regulator does have internal losses, efficiencies can be quite high, generally greater than 80 to 90%. Conservation of energy applies, so the input power equals the output power. This says that in step-down (buck) designs, the input current is lower than the output current. On the other hand, in step-up (boost) designs, the input current is greater than the output current. Input currents can therefore be quite high in boost applications, and this should be kept in mind, especially when generating high output voltages from batteries.

THE IDEAL SWITCHING REGULATOR



- $P_{in} = P_{out}$
- Efficiency = $P_{out} / P_{in} = 100\%$
- $v_{in} \cdot i_{in} = v_{out} \cdot i_{out}$
- $\frac{v_{out}}{v_{in}} = \frac{i_{in}}{i_{out}}$
- Energy Must be Conserved!

Figure 3.2

Design engineers unfamiliar with IC switching regulators are sometimes confused by what exactly these devices can do for them. Figure 3.3 summarizes what to expect from a typical IC switching regulator. It should be emphasized that these are typical specifications, and can vary widely, but serve to illustrate some general characteristics.

Input voltages may range from 0.8 to beyond 30V, depending on the breakdown voltage of the IC process. Most regulators are available in several output voltage options, 12V, 5V, 3.3V, and 3V are the most common, and some regulators allow the output voltage to be set using external resistors. Output current varies widely, but regulators with internal switches have inherent current handling limitations that controllers (with external switches) do not. Output line and load regulation is typically about 50mV. The output ripple voltage is highly dependent upon the external output capacitor, but with care, can be limited to between 20mV and 100mV peak-to-peak. This ripple is at the switching frequency, which can range from 20kHz to 1MHz. There are also high frequency components in the output current of a switching regulator, but these can be minimized with proper external filtering, layout, and grounding. Efficiency can also vary widely, with up to 95% sometimes being achievable.

WHAT TO EXPECT FROM A SWITCHING REGULATOR IC

- **Input Voltage Range: 0.8V to 30V**
- **Output Voltage:**
  - **"Standard": 12V, 5V, 3.3V, 3V**
  - **"Specialized": VID Programmable for Microprocessors**
  - **(Some are Adjustable)**
- **Output Current**
  - **Up to 1.5A, Using Internal Switches of a Regulator**
  - **No Inherent Limitations Using External Switches with a Controller**
- **Output Line / Load Regulation: 50mV, typical**
- **Output Voltage Ripple (peak-peak) :**
  20mV - 100mV @ Switching Frequency
- **Switching Frequency: 20kHz - 1MHz**
- **Efficiency: Up to 95%**

Figure 3.3

POPULAR APPLICATIONS OF SWITCHING REGULATORS

For equipment which is powered by an AC source, the conversion from AC to DC is generally accomplished with a switcher, except for low-power applications where size and efficiency concerns are outweighed by cost. Then the power conversion may be done with just an AC transformer, some diodes, a capacitor, and a linear regulator. The size issue quickly brings switchers back into the picture as the preferable conversion method as power levels rise up to 10 watts and beyond. Off-line power conversion is heavily dominated by switchers in most modern electronic equipment.

Many modern high-power off-line power supply systems use the distributed approach by employing a switcher to generate an intermediate DC voltage which is then distributed to any number of DC/DC converters which can be located near to their respective loads (see Figure 3.4). Although there is the obvious redundancy of converting the power twice, distribution offers some advantages. Since such systems require isolation from the line voltage, only the first converter requires the isolation; all cascaded converters need not be isolated, or at least not to the degree of isolation that the first converter requires. The intermediate DC voltage is usually regulated to less than 60 volts in order to minimize the isolation requirement for the cascaded converters. Its regulation is not critical since it is not a direct output. Since it is typically higher than any of the switching regulator output voltages, the distribution current is substantially less than the sum of the output currents, thereby reducing I^2R losses in the system power distribution wiring. This also allows the use of a smaller energy storage capacitor on the intermediate DC supply output. (Recall that the energy stored in a capacitor is $\frac{1}{2}CV^2$).

Power management can be realized by selectively turning on or off the individual DC/DC converters as needed.

POWER DISTRIBUTION USING LINEAR AND SWITCHING REGULATORS

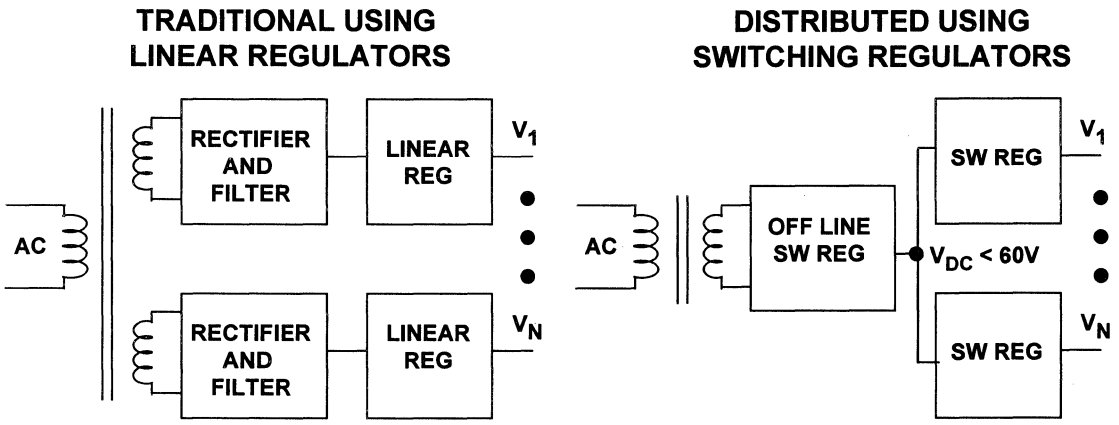


Figure 3.4

ADVANTAGES OF DISTRIBUTED POWER SYSTEMS USING SWITCHING REGULATORS

- **Higher Efficiency with Switching Regulators than Linear Regulators**
- **Use of High Intermediate DC Voltage Minimizes Power Loss due to Wiring Resistance**
- **Flexible (Multiple Output Voltages Easily Obtained)**
- **AC Power Transformer Design Easier (Only One Winding Required, Regulation Not Critical)**
- **Selective Shutdown Techniques Can Be Used for Higher Efficiency**
- **Eliminates Safety Isolation Requirements for DC/DC Converters**

Figure 3.5

Batteries are the primary power source in much of today's consumer and communications equipment. Such systems may require one or several voltages, and they may be less or greater than the battery voltage. Since a battery is a self-contained power source, power converters seldom require isolation. Often, then, the basic switcher topologies are used, and a wide variety of switching regulators are

available to fill many of the applications. Maximum power levels for these regulators typically can range up from as low as tens of milliwatts to several watts.

Efficiency is often of great importance, as it is a factor in determining battery life which, in turn, affects practicality and cost of ownership. Often of even greater importance, though often confused with efficiency, is quiescent power dissipation when operating at a small fraction of the maximum rated load (e.g., standby mode). For electronic equipment which must remain under power in order to retain data storage or minimal monitoring functions, but is otherwise shut down most of the time, the quiescent dissipation is the largest determinant of battery life. Although efficiency may indicate power consumption for a specific light load condition, it is not the most useful way to address the concern. For example, if there is no load on the converter output, the efficiency will be zero no matter how optimal the converter, and one could not distinguish a well power-managed converter from a poorly managed one by such a specification.

The concern of managing power effectively from no load to full load has driven much of the technology which has been and still is emerging from today's switching regulators and controllers. Effective power management, as well as reliable power conversion, is often a substantial factor of quality or noteworthy distinction in a wide variety of equipment. The limitations and cost of batteries are such that consumers place a value on not having to replace them more often than necessary, and that is certainly a goal for effective power conversion solutions.

TYPICAL APPLICATION OF A BOOST REGULATOR IN BATTERY OPERATED EQUIPMENT

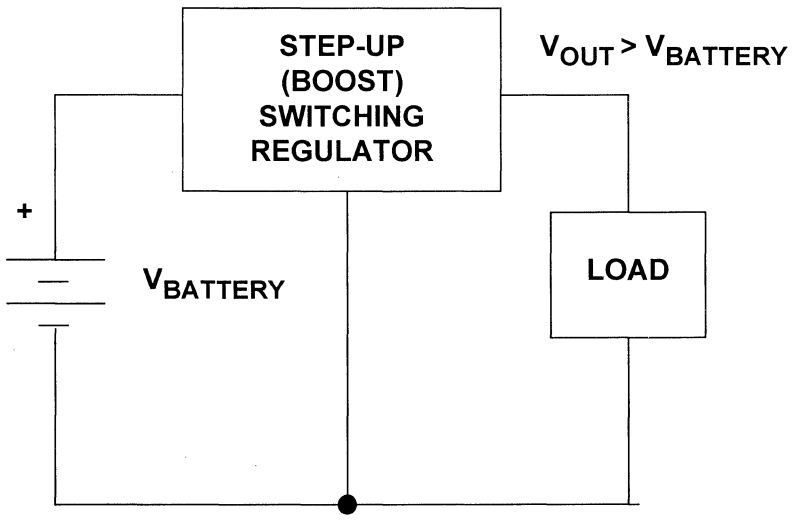


Figure 3.6

INDUCTOR AND CAPACITOR FUNDAMENTALS

In order to understand switching regulators, the fundamental energy storage capabilities of inductors and capacitors must be fully understood. When a voltage is applied to an ideal inductor (see Figure 3.7), the current builds up linearly over time at a rate equal to V/L, where V is the applied voltage, and L is the value of the inductance. This energy is stored in the inductor's magnetic field, and if the switch is opened, the magnetic field collapses, and the inductor voltage goes to a large instantaneous value until the field has fully collapsed.

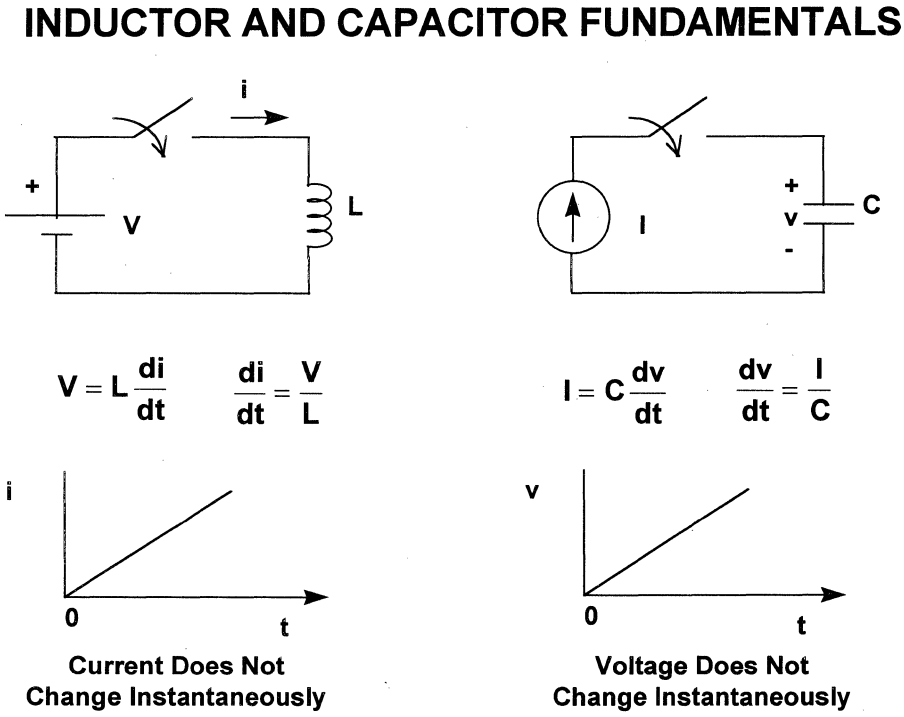


Figure 3.7

When a current is applied to an ideal capacitor, the capacitor is gradually charged, and the voltage builds up linearly over time at a rate equal to I/C, where I is the applied current, and C is the value of the capacitance. Note that the voltage across an ideal capacitor cannot change instantaneously.

Of course, there is no such thing as an ideal inductor or capacitor. Real inductors have stray winding capacitance, series resistance, and can saturate for large currents. Real capacitors have series resistance and inductance and may break down under large voltages. Nevertheless, the fundamentals of the ideal inductor and capacitor are critical in understanding the operation of switching regulators.

An inductor can be used to transfer energy between two voltage sources as shown in Figure 3.8. While energy transfer could occur between two voltage sources with a resistor connected between them, the energy transfer would be inefficient due to the power loss in the resistor, and the energy could only be transferred from the higher to the lower value source. In contrast, an inductor ideally returns all the energy that

is stored in it, and with the use of properly configured switches, the energy can flow from any one source to another, regardless of their respective values and polarities.

ENERGY TRANSFER USING AN INDUCTOR

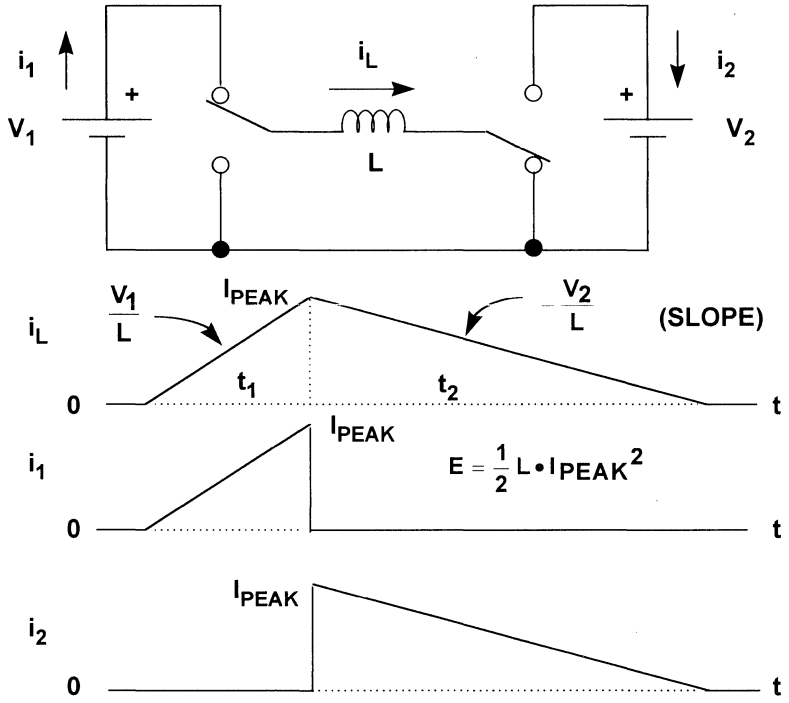


Figure 3.8

When the switches are initially placed in the position shown, the voltage V_1 is applied to the inductor, and the inductor current builds up at a rate equal to V_1/L. The peak value of the inductor current at the end of the interval t_1 is

$$I_{PEAK} = \frac{V_1}{L} \bullet t_1.$$

The average power transferred to the inductor during the interval t_1 is

$$P_{AVG} = \frac{1}{2} I_{PEAK} \bullet V_1.$$

The energy transferred during the interval t_1 is

$$E = P_{AVG} \bullet t_1 = \frac{1}{2} I_{PEAK} \bullet V_1 \bullet t_1.$$

Solving the first equation for t_1 and substituting into the last equation yields

$$E = \frac{1}{2} L \bullet I_{PEAK}^2.$$

When the switch positions are reversed, the inductor current continues to flow into the load voltage V_2, and the inductor current decreases at a rate $-V_2/L$. At the end of the interval t_2, the inductor current has decreased to zero, and the energy has been transferred into the load. The figure shows the current waveforms for the inductor, the input current i_1, and the output current i_2. The ideal inductor dissipates no power, so there is no power loss in this transfer, assuming ideal circuit elements. This fundamental method of energy transfer forms the basis for all switching regulators.

IDEAL STEP-DOWN (BUCK) CONVERTER

The fundamental circuit for an ideal step-down (buck) converter is shown in Figure 3.9. The actual integrated circuit switching regulator contains the switch control circuit and may or may not include the switch (depending upon the output current requirement). The inductor, diode, and load bypass capacitor are external.

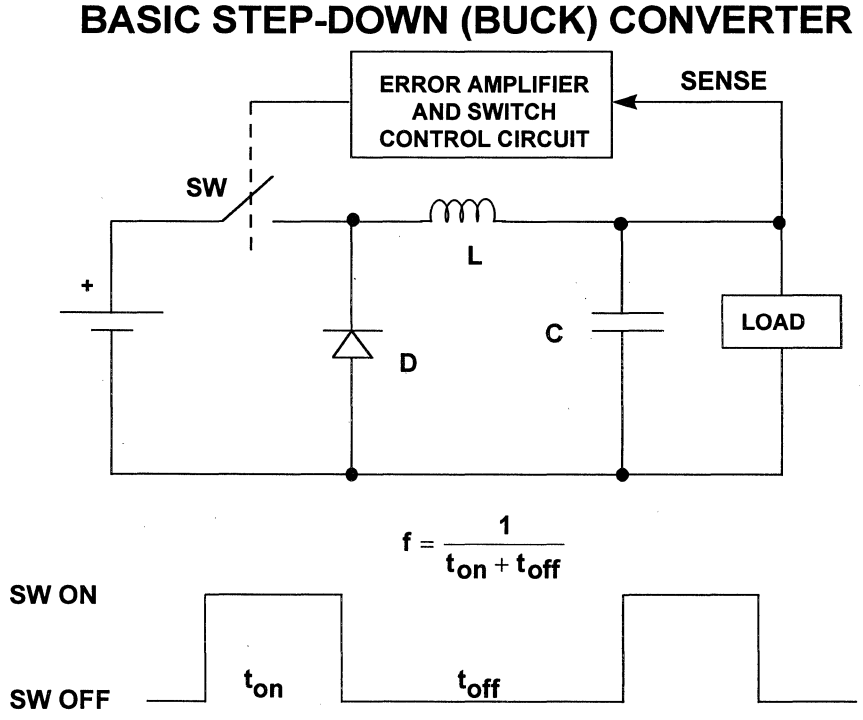


Figure 3.9

The output voltage is sensed and then regulated by the switch control circuit. There are several methods for controlling the switch, but for now assume that the switch is controlled by a pulse width modulator (PWM) operating at a fixed frequency, f.

The actual waveforms associated with the buck converter are shown in Figure 3.10. When the switch is on, the voltage $V_{IN}-V_{OUT}$ appears across the inductor, and the inductor current increases with a slope equal to $(V_{IN}-V_{OUT})/L$ (see Figure 3.10B). When the switch turns off, current continues to flow through the inductor and into the load (remember that the current cannot change instantaneously in an inductor), with the ideal diode providing the return current path. The voltage across the

inductor is now V_{OUT}, but the polarity has reversed. Therefore, the inductor current decreases with a slope equal to $-V_{OUT}/L$. Note that the inductor current is equal to the output current in a buck converter.

The diode and switch currents are shown in Figures 3.10C and 3.10D, respectively, and the inductor current is the sum of these waveforms. Also note by inspection that the instantaneous input current equals the switch current. Note, however, that the average input current is less than the average output current. In a practical regulator, both the switch and the diode have voltage drops across them during their conduction which creates internal power dissipation and a loss of efficiency, but these voltages will be neglected for now. It is also assumed that the output capacitor, C, is large enough so that the output voltage does not change significantly during the switch on or off times.

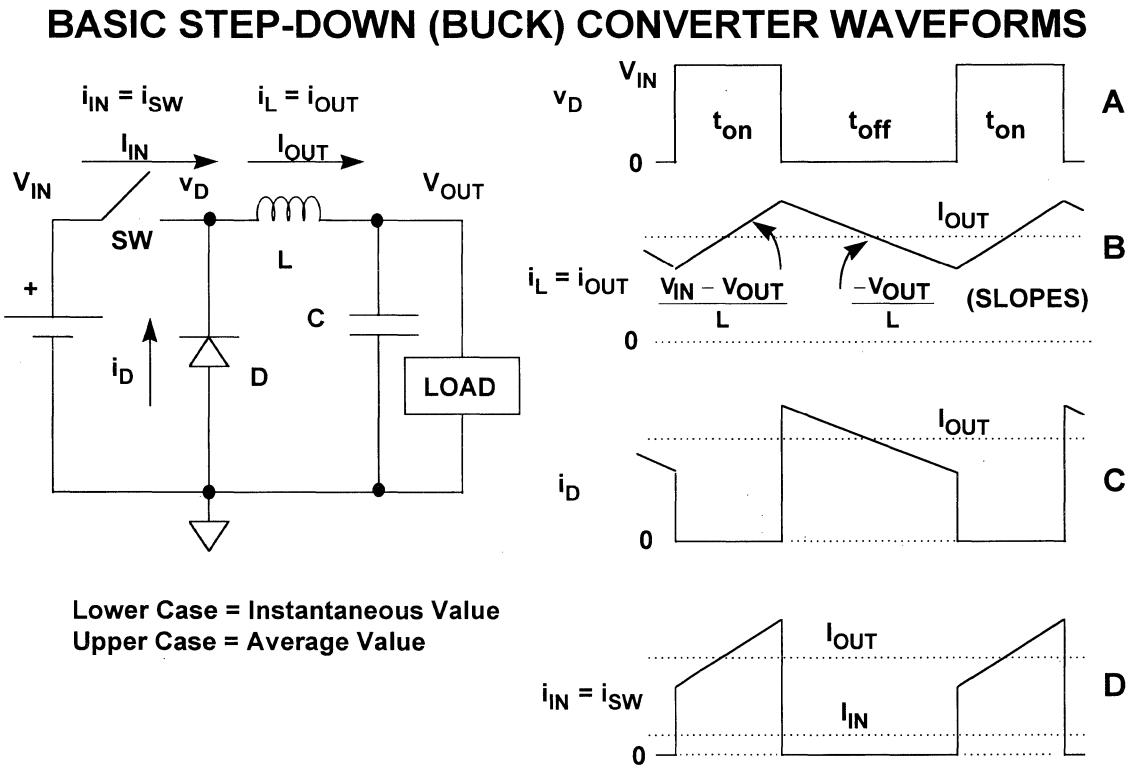


Figure 3.10

There are several important things to note about these waveforms. The most important is that ideal components have been assumed, i.e., the input voltage source has zero impedance, the switch has zero on-resistance and zero turn-on and turn-off times. It is also assumed that the inductor does not saturate and that the diode is ideal with no forward drop.

Also note that the output current is continuous, while the input current is pulsating. Obviously, this has implications regarding input and output filtering. If one is concerned about the voltage ripple created on the power source which supplies a buck converter, the input filter capacitor (not shown) is generally more critical that the output capacitor with respect to ESR/ESL.

If a steady-state condition exists (see Figure 3.11), the basic relationship between the input and output voltage may be derived by inspecting the inductor current waveform and writing:

$$\frac{V_{IN} - V_{OUT}}{L} \bullet t_{on} = \frac{V_{OUT}}{L} \bullet t_{off}.$$

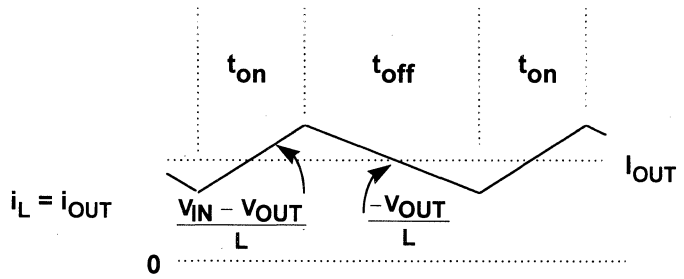
Solving for V_{OUT}:

$$V_{OUT} = V_{IN} \bullet \frac{t_{on}}{t_{on} + t_{off}} = V_{IN} \bullet D,$$

where D is the switch *duty ratio* (more commonly called *duty cycle*), defined as the ratio of the switch on-time (t_{on}) to the total switch cycle time ($t_{on} + t_{off}$).

This is the classic equation relating input and output voltage in a buck converter which is operating with *continuous* inductor current, defined by the fact that the inductor current never goes to zero.

INPUT/OUTPUT RELATIONSHIP FOR BUCK CONVERTER



- **Write by Inspection from Inductor/Output Current Waveforms:**
- $\frac{V_{IN} - V_{OUT}}{L} \bullet t_{on} = \frac{V_{OUT}}{L} \bullet t_{off}$
- **Rearrange and Solve for V_{OUT}:**
- $V_{OUT} = V_{IN} \bullet \frac{t_{on}}{t_{on} + t_{off}} = V_{IN} \bullet D$

Figure 3.11

Notice that this relationship is independent of the inductor value L as well as the switching frequency $1/(t_{on} + t_{off})$ and the load current. Decreasing the inductor value, however, will result in a larger peak-to-peak output ripple current, while increasing the value results in smaller ripple. There are many other tradeoffs involved in selecting the inductor, and these will be discussed in a later section.

In this simple model, line and load regulation (of the output voltage) is achieved by varying the duty cycle using a pulse width modulator (PWM) operating at a fixed frequency, f. The PWM is in turn controlled by an error amplifier - an amplifier which amplifies the "error" between the measured output voltage and a reference voltage. As the input voltage increases, the duty cycle decreases; and as the input voltage decreases, the duty cycle increases. Note that while the average inductor current changes proportionally to the output current, the duty cycle does not change. Only dynamic changes in the duty cycle are required to modulate the inductor current to the desired level; then the duty cycle returns to its steady state value. In a practical converter, the duty cycle might increase slightly with load current to counter the increase in voltage drops in the circuit, but would otherwise follow the ideal model.

This discussion so far has assumed the regulator is in the *continuous-mode* of operation, defined by the fact that the inductor current never goes to zero. If, however, the output load current is decreased, there comes a point where the inductor current will go to zero between cycles, and the inductor current is said to be *discontinuous*. It is necessary to understand this operating mode as well, since many switchers must supply a wide dynamic range of output current, where this phenomenon is unavoidable. Waveforms for discontinuous operation are shown in Figure 3.12.

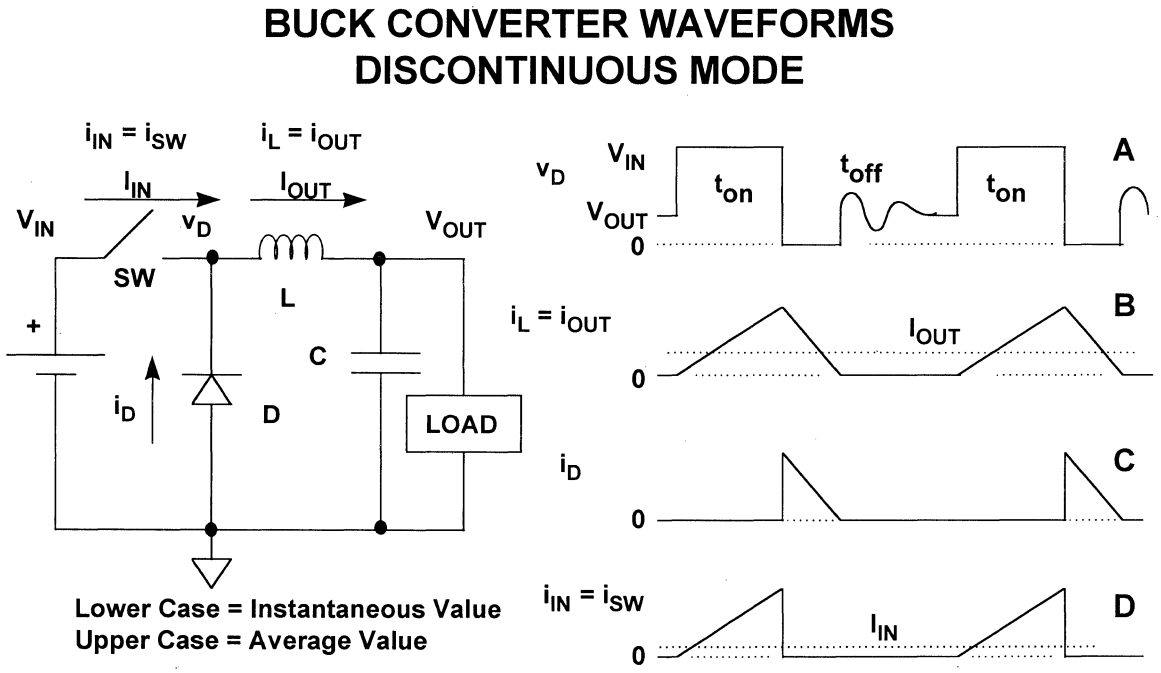


Figure 3.12

Behavior during the switch on-time is identical to that of the continuous mode of operation. However, during the switch off-time, there are two regions of unique behavior. First, the inductor current ramps down at the same rate as it does during continuous mode, but then the inductor current goes to zero. When it reaches zero, the current tries to reverse but cannot find a path through the diode any longer. So the voltage on the input side of the inductor (same as the diode and switch junction)

jumps up to V_{OUT} such that the inductor has no voltage across it, and the current can remain at zero.

Because the impedance at diode node (v_D) is high, ringing occurs due to the inductor, L, resonating with the stray capacitance which is the sum of the diode capacitance, C_D, and the switch capacitance, C_{SW}. The oscillation is damped by stray resistances in the circuit, and occurs at a frequency given by

$$f_o = \frac{1}{2\pi \sqrt{L(C_D + C_{SW})}}.$$

A circuit devoted simply to dampening resonances via power dissipation is called a *snubber*. If the ringing generates EMI/RFI problems, it may be damped with a suitable RC snubber. However, this will cause additional power dissipation and reduced efficiency.

If the load current of a standard buck converter is low enough, the inductor current becomes discontinuous. The current at which this occurs can be calculated by observing the waveform shown in Figure 3.13. This waveform is drawn showing the inductor current going to exactly zero at the end of the switch off-time. Under these conditions, the average output current is

$$I_{OUT} = I_{PEAK}/2.$$

We have already shown that the peak inductor current is

$$I_{PEAK} = \frac{V_{IN} - V_{OUT}}{L} \bullet t_{on}.$$

Thus, discontinuous operation will occur if

$$I_{OUT} < \frac{V_{IN} - V_{OUT}}{2L} \bullet t_{on}.$$

However, V_{OUT} and V_{IN} are related by:

$$V_{OUT} = V_{IN} \bullet D = V_{IN} \bullet \frac{t_{on}}{t_{on} + t_{off}}.$$

Solving for t_{on}:

$$t_{on} = \frac{V_{OUT}}{V_{IN}} \bullet (t_{on} + t_{off}) = \frac{V_{OUT}}{V_{IN}} \bullet \frac{1}{f}.$$

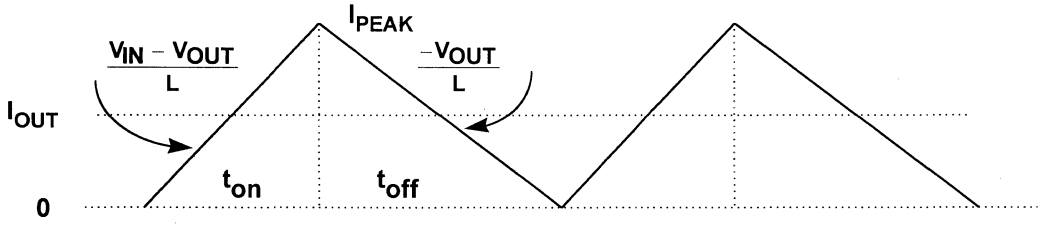
Substituting this value for t_{on} into the previous equation for I_{OUT}:

$$I_{OUT} < \frac{V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{2Lf}$$

(Criteria for discontinuous operation - buck converter)

BUCK CONVERTER POINT OF DISCONTINUOUS OPERATION

INDUCTOR CURRENT AND OUTPUT CURRENT



DISCONTINUOUS MODE IF:

$$I_{OUT} < \frac{1}{2} I_{PEAK} = \frac{V_{IN} - V_{OUT}}{2L} \cdot t_{on}$$

$$I_{OUT} < \frac{V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{2Lf}, \quad f = \frac{1}{t_{on} + t_{off}}$$

Figure 3.13

IDEAL STEP-UP (BOOST) CONVERTER

The basic step-up (boost) converter circuit is shown in Figure 3.14. During the switch on-time, the current builds up in the inductor. When the switch is opened, the energy stored in the inductor is transferred to the load through the diode.

The actual waveforms associated with the boost converter are shown in Figure 3.15. When the switch is on, the voltage V_{IN} appears across the inductor, and the inductor current increases at a rate equal to V_{IN}/L. When the switch is opened, a voltage equal to $V_{OUT} - V_{IN}$ appears across the inductor, current is supplied to the load, and the current decays at a rate equal to $(V_{OUT} - V_{IN})/L$. The inductor current waveform is shown in Figure 3.15B.

BASIC STEP-UP (BOOST) CONVERTER

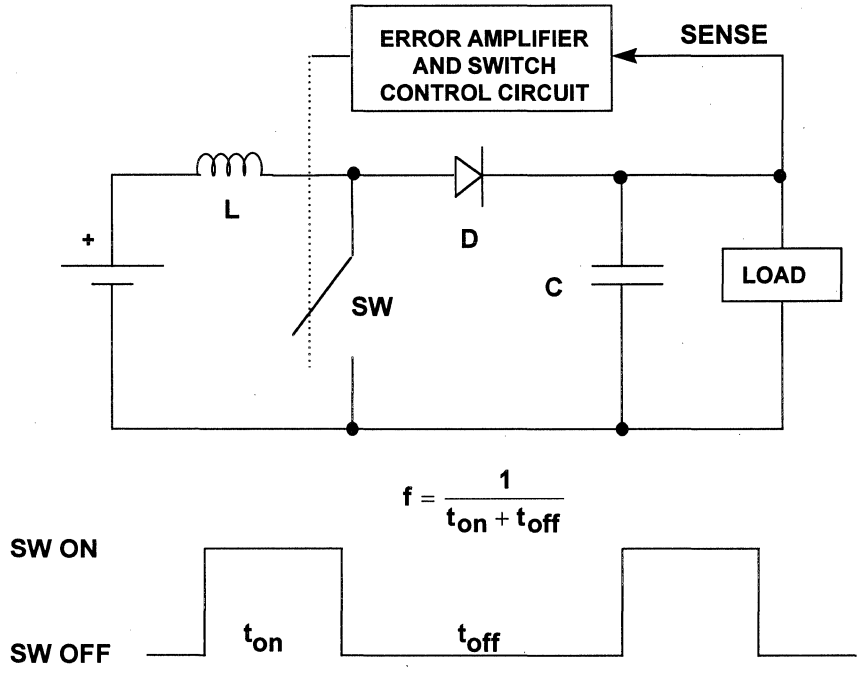


Figure 3.14

BASIC STEP-UP (BOOST) CONVERTER WAVEFORMS

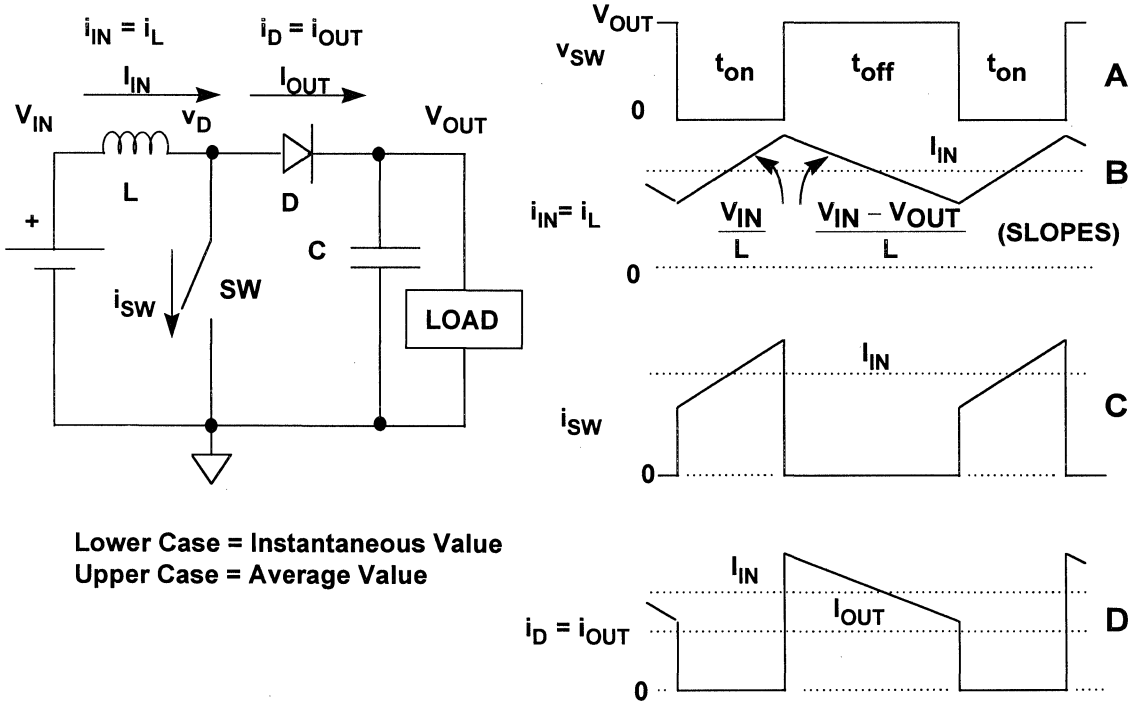


Figure 3.15

Note that in the boost converter, the input current is continuous, while the output current (Figure 3.15D) is pulsating. This implies that filtering the output of a boost converter is more difficult than that of a buck converter. (Refer back to the previous discussion of buck converters). Also note that the input current is the sum of the switch and diode current.

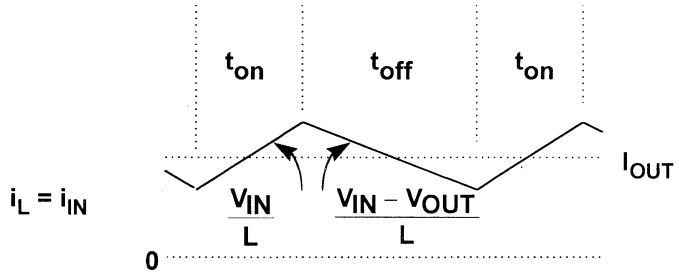
If a steady-state condition exists (see Figure 3.16), the basic relationship between the input and output voltage may be derived by inspecting the inductor current waveform and writing:

$$\frac{V_{IN}}{L} \bullet t_{on} = \frac{V_{OUT} - V_{IN}}{L} \bullet t_{off}.$$

Solving for V_{OUT}:

$$V_{OUT} = V_{IN} \bullet \frac{t_{on} + t_{off}}{t_{off}} = V_{IN} \bullet \frac{1}{1 - D}.$$

INPUT/OUTPUT RELATIONSHIP FOR BOOST CONVERTER



- **Write by Inspection from Inductor/Input Current Waveforms:**
- $\frac{V_{IN}}{L} \bullet t_{on} = \frac{V_{OUT} - V_{IN}}{L} \bullet t_{off}$
- **Rearrange and Solve for V_{OUT}:**
- $V_{OUT} = V_{IN} \bullet \frac{t_{on} + t_{off}}{t_{off}} = V_{IN} \bullet \frac{1}{1 - D}$

Figure 3.16

This discussion so far has assumed the boost converter is in the *continuous-mode* of operation, defined by the fact that the inductor current never goes to zero. If, however, the output load current is decreased, there comes a point where the inductor current will go to zero between cycles, and the inductor current is said to be *discontinuous*. It is necessary to understand this operating mode as well, since many switchers must supply a wide dynamic range of output current, where this phenomenon is unavoidable.

Discontinuous operation for the boost converter is similar to that of the buck converter. Figure 3.17 shows the waveforms. Note that when the inductor current goes to zero, ringing occurs at the switch node at a frequency f_0 given by:

$$f_0 = \frac{1}{2\pi\sqrt{L(C_D + C_{SW})}}.$$

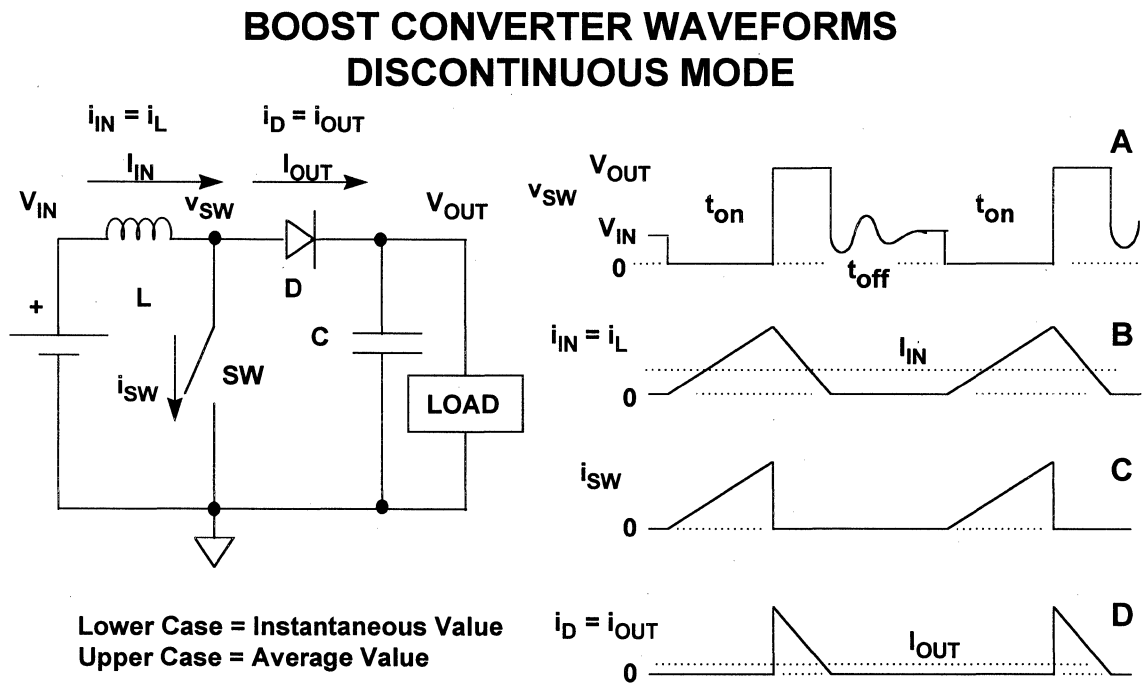


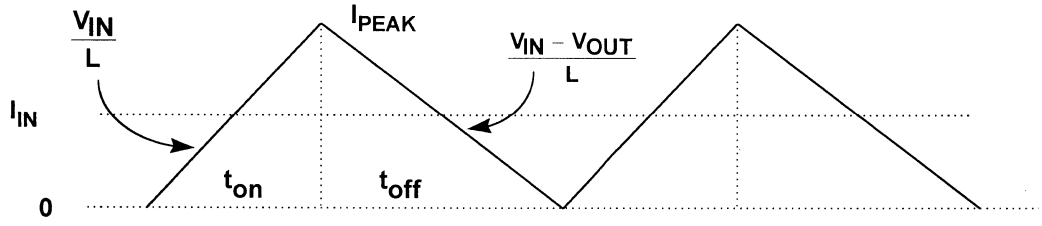
Figure 3.17

The inductor, L, resonates with the stray switch capacitance and diode capacitance, $C_{SW} + C_D$ as in the case of the buck converter. The ringing is dampened by circuit resistances, and, if needed, a snubber.

The current at which a boost converter becomes discontinuous can be derived by observing the inductor current (same as input current) waveform of Figure 3.18.

BOOST CONVERTER POINT OF DISCONTINUOUS OPERATION

INDUCTOR CURRENT AND INPUT CURRENT



DISCONTINUOUS MODE IF:

$$I_{IN} < \frac{1}{2} I_{PEAK} = \frac{V_{OUT} - V_{IN}}{2L} \bullet t_{off}$$

$$I_{OUT} < \frac{V_{IN}^2 (V_{OUT} - V_{IN})}{V_{OUT}^2 \bullet 2Lf}, \quad f = \frac{1}{t_{on} + t_{off}}$$

3

Figure 3.18

The average input current at the point of discontinuous operation is

$$I_{IN} = I_{PEAK}/2.$$

Discontinuous operation will occur if

$$I_{IN} < I_{PEAK}/2.$$

However,

$$I_{IN} = \frac{I_{PEAK}}{2} = \frac{V_{OUT} - V_{IN}}{2L} \bullet t_{off}.$$

Also,

$$V_{IN} \bullet I_{IN} = V_{OUT} \bullet I_{OUT}, \text{ and therefore}$$

$$I_{OUT} = \frac{V_{IN}}{V_{OUT}} \bullet I_{IN} = \frac{V_{IN}}{V_{OUT}} \bullet \frac{(V_{OUT} - V_{IN})}{2L} \bullet t_{off}.$$

However,

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 - D} = \frac{1}{1 - \frac{t_{on}}{t_{on} + t_{off}}} = \frac{t_{on} + t_{off}}{t_{off}}.$$

Solving for t_{off}:

$$t_{off} = \frac{V_{IN}}{V_{OUT}}(t_{on} + t_{off}) = \frac{V_{IN}}{f \bullet V_{OUT}}.$$

Substituting this value for t_{off} into the previous expression for I_{OUT}, the criteria for discontinuous operation of a boost converter is established:

$$I_{OUT} < \frac{V_{IN}^2(V_{OUT} - V_{IN})}{V_{OUT}^2 \bullet 2Lf}. \qquad \text{(Criteria for discontinuous operation - boost converter).}$$

The basic buck and boost converter circuits can work equally well for negative inputs and outputs as shown in Figure 3.19. Note that the only difference is that the polarities of the input voltage and the diode have been reversed. In practice, however, not many IC buck and boost regulators or controllers will work with negative inputs. In some cases, external circuitry can be added in order to handle negative inputs and outputs. Rarely are regulators or controllers designed specifically for negative inputs or outputs. In any case, data sheets for the specific ICs will indicate the degree of flexibility allowed.

NEGATIVE IN, NEGATIVE OUT BUCK AND BOOST CONVERTERS

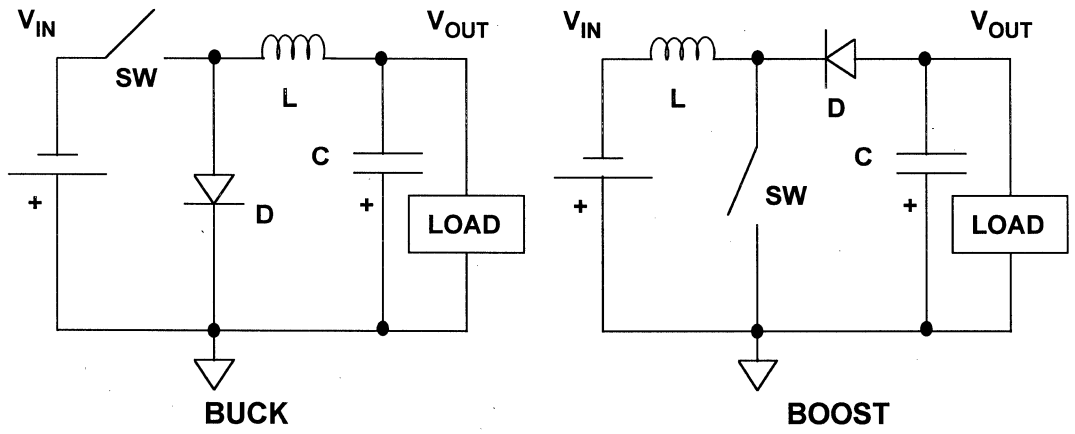


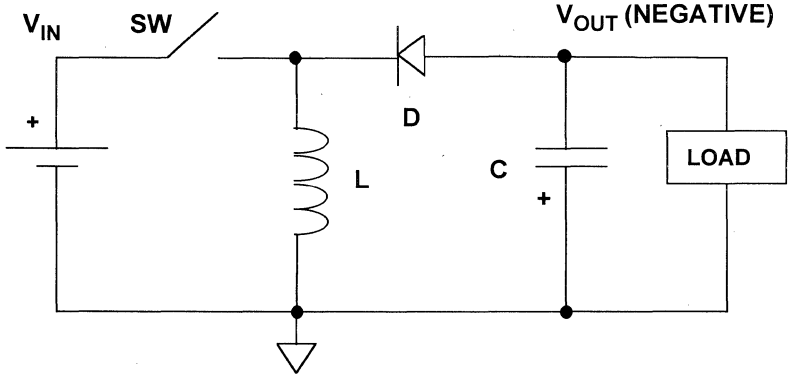
Figure 3.19

BUCK-BOOST TOPOLOGIES

The simple buck converter can only produce an output voltage which is less than the input voltage, while the simple boost converter can only produce an output voltage greater than the input voltage. There are many applications where more flexibility is required. This is especially true in battery powered applications, where the fully charged battery voltage starts out greater than the desired output (the converter must operate in the buck mode), but as the battery discharges, its voltage becomes less than the desired output (the converter must then operate in the boost mode).

A *buck-boost* converter is capable of producing an output voltage which is either greater than or less than the absolute value of the input voltage. A simple buck-boost converter topology is shown in Figure 3.20. The input voltage is positive, and the output voltage is negative. When the switch is on, the inductor current builds up. When the switch is opened, the inductor supplies current to the load through the diode. Obviously, this circuit can be modified for a negative input and a positive output by reversing the polarity of the diode.

BUCK-BOOST CONVERTER #1,
$+V_{IN}$, $-V_{OUT}$

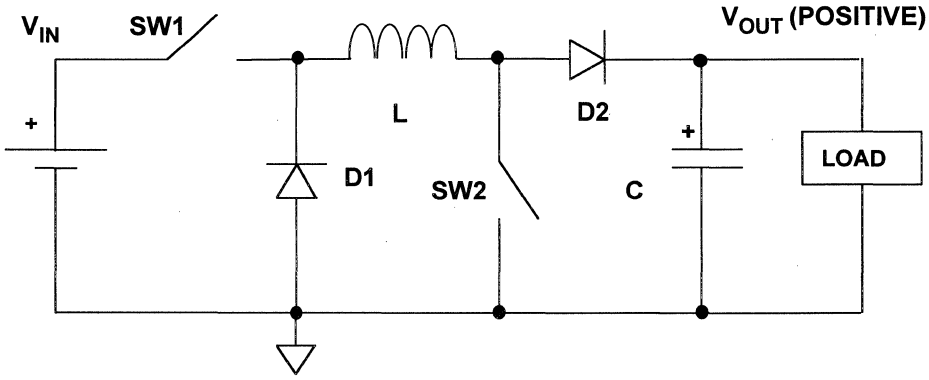


The Absolute Value of the Output Can Be Less Than Or Greater Than the Absolute Value of the Input

Figure 3.20

A second buck-boost converter topology is shown in Figure 3.21. This circuit allows both the input and output voltage to be positive. When the switches are closed, the inductor current builds up. When the switches open, the inductor current is supplied to the load through the current path provided by D1 and D2. A fundamental disadvantage to this circuit is that it requires two switches and two diodes. As in the previous circuits, the polarities of the diodes may be reversed to handle negative input and output voltages.

BUCK-BOOST CONVERTER #2
$+V_{IN}$, $+V_{OUT}$



The Absolute Value of the Output Can Be Less Than Or Greater Than the Absolute Value of the Input

Figure 3.21

Another way to accomplish the buck-boost function is to cascade two switching regulators; a boost regulator followed by a buck regulator as shown in Figure 3.22. The example shows some practical voltages in a battery-operated system. The input from the four AA cells can range from 6V (charged) to about 3.5V (discharged). The intermediate voltage output of the boost converter is 8V, which is always greater than the input voltage. The buck regulator generates the desired 5V from the 8V intermediate voltage. The total efficiency of the combination is the product of the individual efficiencies of each regulator, and can be greater than 85% with careful design.

An alternate topology is use a buck regulator followed by a boost regulator. This approach, however, has the disadvantage of pulsating currents on both the input and output and a higher current at the intermediate voltage output.

CASCADED BUCK-BOOST REGULATORS (EXAMPLE VOLTAGES)

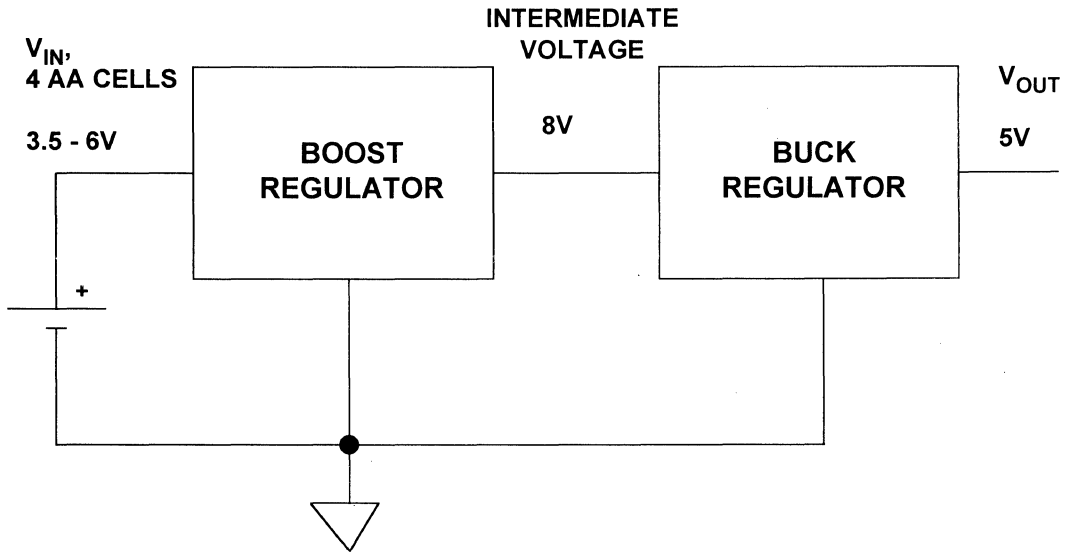


Figure 3.22

OTHER NON-ISOLATED SWITCHER TOPOLOGIES

The coupled-inductor single-ended primary inductance converter (SEPIC) topology is shown in Figure 3.23. This converter uses a transformer with the addition of capacitor C_C which couples additional energy to the load. If the turns ratio (N = the ratio of the number of primary turns to the number of secondary turns) of the transformer in the SEPIC converter is 1:1, the capacitor serves only to recover the energy in the leakage inductance (i.e., that energy which is not perfectly coupled between the windings) and delivering it to the load. In that case, the relationship between input and output voltage is given by

$$V_{OUT} = V_{IN} \bullet \frac{D}{1-D}.$$

For non-unity turns ratios the input/output relationship is highly nonlinear due to transfer of energy occurring via both the coupling between the windings and the capacitor C_C. For that reason, it is not analyzed here.

SINGLE-ENDED PRIMARY INDUCTANCE CONVERTER (SEPIC)

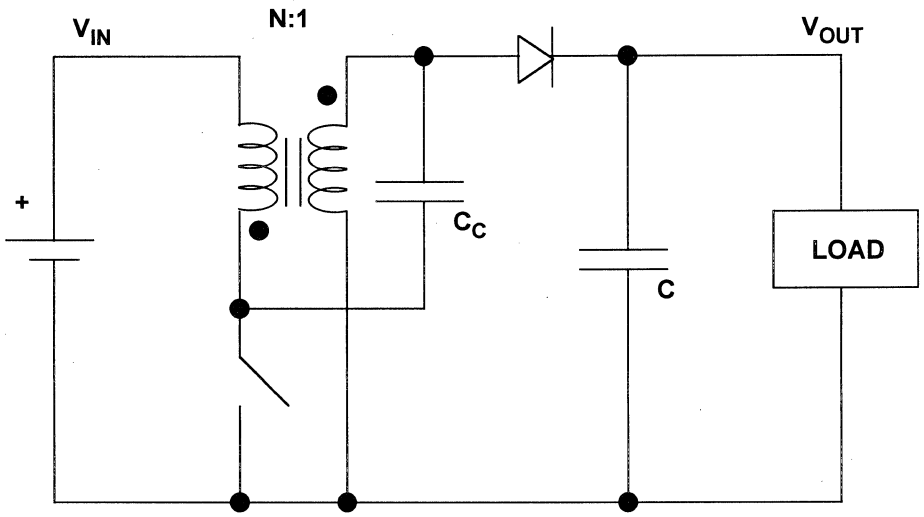


Figure 3.23

This converter topology often makes an excellent choice in non-isolated battery-powered systems for providing both the ability to step up or down the voltage, and, unlike the boost converter, the ability to have zero voltage at the output when desired.

The Zeta and Cük converters, not shown, are two examples of non-isolated converters which require capacitors to deliver energy from input to output, i.e., rather than just to store energy or deliver only recovered leakage energy, as the SEPIC can be configured via a 1:1 turns ratio. Because capacitors capable of delivering energy efficiently in such converters tend to be bulky and expensive, these converters are not frequently used.

ISOLATED SWITCHING REGULATOR TOPOLOGIES

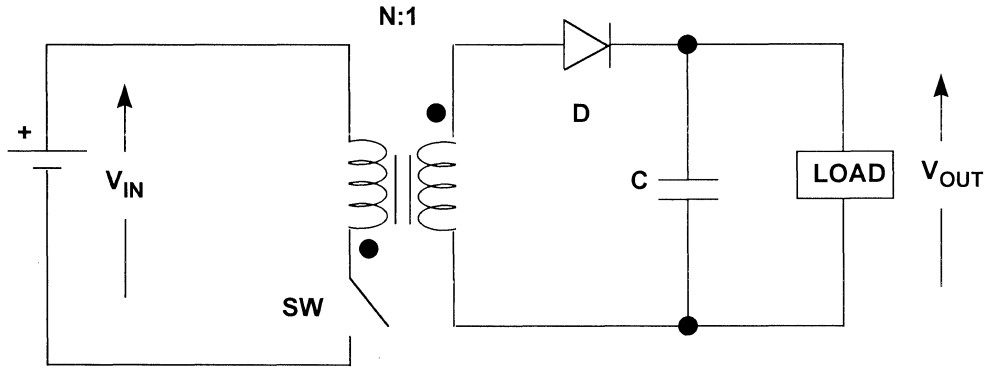
The switching regulators discussed so far have direct galvanic connections between the input and output. Transformers can be used to supply galvanic isolation as well as allowing the buck-boost function to be easily performed. However, adding a transformer to the circuit creates a more complicated and expensive design as well as increasing the physical size.

The basic *flyback* buck-boost converter circuit is shown in Figure 3.24. It is derived from the buck-boost converter topology. When the switch is on, the current builds up in the primary of the transformer. When the switch is opened, the current reverts to the secondary winding and flows through the diode and into the load. The relationship between the input and output voltage is determined by the turns ratio, N, and the duty cycle, D, per the following equation:

$$V_{OUT} = \frac{V_{IN}}{N} \bullet \frac{D}{1-D}.$$

A disadvantage of the flyback converter is the high energy which must be stored in the transformer in the form of DC current in the windings. This requires larger cores than would be necessary with pure AC in the windings.

ISOLATED TOPOLOGY: FLYBACK CONVERTER



(BUCK-BOOST DERIVED)

$$V_{OUT} = \frac{V_{IN}}{N} \bullet \frac{D}{1-D}$$

D = Duty Cycle

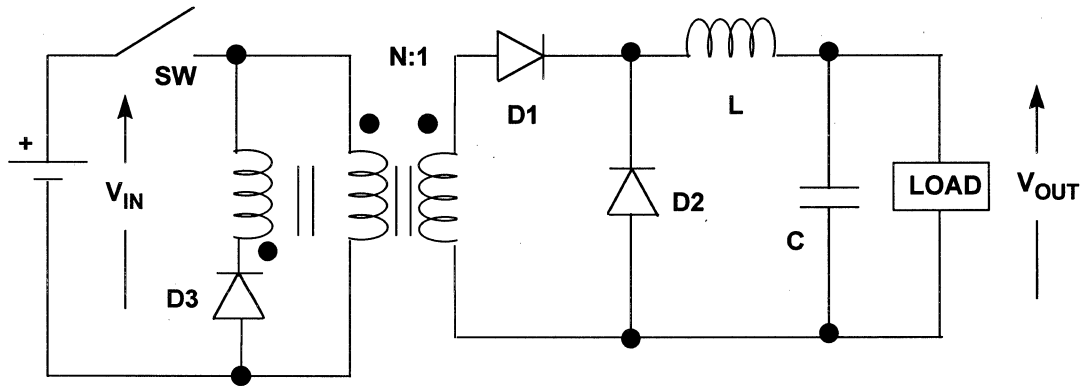
Figure 3.24

The basic *forward* converter topology is shown in Figure 3.25. It is derived from the buck converter. This topology avoids the problem of large stored energy in the transformer core. However, the circuit is more complex and requires an additional magnetic element (a transformer), an inductor, an additional transformer winding, plus three diodes. When the switch is on, current builds up in the primary winding and also in the secondary winding, where it is transferred to the load through diode D1. When the switch is on, the current in the inductor flows out of D1 from the transformer and is reflected back to the primary winding according to the turns ratio. Additionally, the current due to the input voltage applied across the primary inductance, called the *magnetizing current*, flows in the primary winding. When the switch is opened, the current in the inductor continues to flow through the load via the return path provided by diode D2. The load current is no longer reflected into the transformer, but the magnetizing current induced in the primary still requires a return path so that the transformer can be *reset*. Hence the extra *reset* winding and diode are needed.

The relationship between the input and output voltage is given by:

$$V_{OUT} = \frac{V_{IN}}{N} \bullet D.$$

ISOLATED TOPOLOGY: FORWARD CONVERTER



(BUCK DERIVED)

$$V_{OUT} = \frac{V_{IN}}{N} \bullet D$$

D = Duty Cycle

Figure 3.25

There are many other possible isolated switching regulator topologies which use transformers, however, the balance of this section will focus on non-isolated topologies because of their wider application in portable and distributed power systems.

SWITCH MODULATION TECHNIQUES

Important keys to understanding switching regulators are the various methods used to control the switch. For simplicity of analysis, the examples previously discussed used a simple fixed-frequency pulse width modulation (PWM) technique. There can be two other standard variations of the PWM technique: variable frequency constant on-time, and variable frequency constant off-time.

In the case of a buck converter, using a variable frequency constant off-time ensures that the peak-to-peak output ripple current (also the inductor current) remains constant as the input voltage varies. This is illustrated in Figure 3.26, where the output current is shown for two conditions of input voltage. Note that as the input voltage increases, the slope during the on-time increases, but the on-time decreases, thereby causing the frequency to increase. Constant off-time control schemes are popular for buck converters where a wide input voltage range must be accomodated. The ADP1147 family implements this switch modulation technique.

CONTROL OF BUCK CONVERTER USING CONSTANT OFF-TIME, VARIABLE FREQUENCY PWM

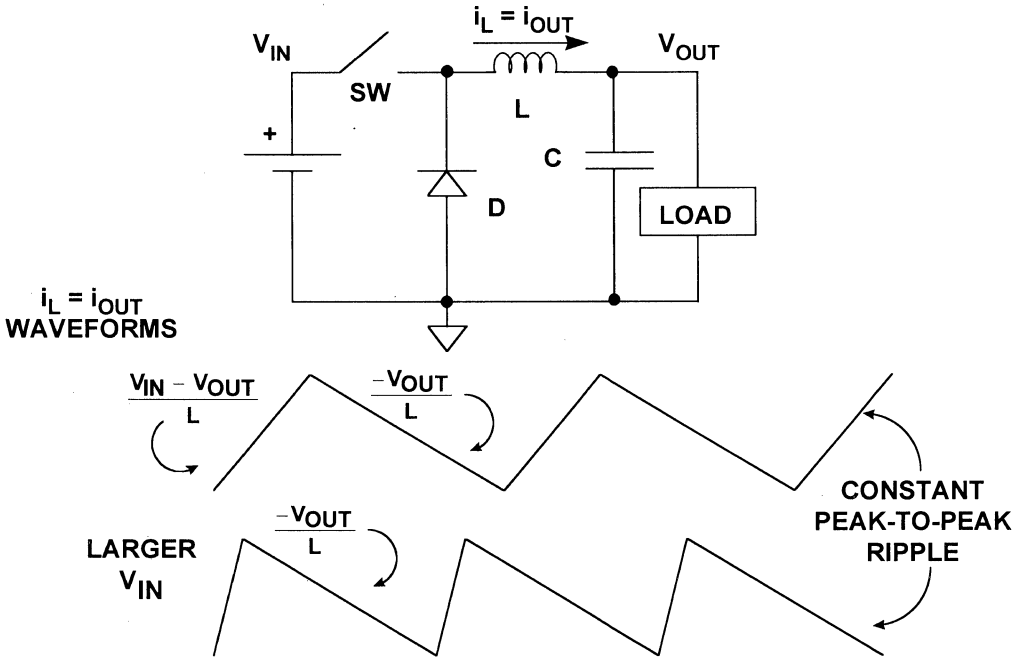


Figure 3.26

In the case of a boost converter, however, neither input ramp slopes nor output ramp slopes are solely a function of the output voltage (see Figure 3.15), so there is no inherent advantage in the variable frequency constant off-time modulation method with respect to maintaining constant output ripple current. Still, that modulation method tends to allow for less ripple current variation than does fixed frequency, so it is often used.

In the case where very low duty cycles are needed, e.g., under short circuit conditions, sometimes the limitation of a minimum achievable duty cycle is encountered. In such cases, in order to maintain a steady-state condition and prevent runaway of the switch current, a pulse skipping function must be implemented. This might take the form of a current monitoring circuit which detects that the switch current is too high to turn the switch on and ramp the current up any higher. So either a fixed frequency cycle is skipped without turning on the switch, or the off-time is extended in some way to delay the turn-on.

The pulse skipping technique for a fixed frequency controller can be applied even to operation at *normal* duty cycles. Such a switch modulation technique is then referred to as *pulse burst modulation* (PBM). At its simplest, this technique simply gates a fixed frequency, fixed duty cycle oscillator to be applied to the switch or not. The duty cycle of the oscillator sets the maximum achievable duty cycle for the converter, and smaller duty cycles are achieved over an average of a multiplicity of pulses by skipping oscillator cycles. This switch modulation method accompanies a simple control method of using a hysteretic comparator to monitor the output voltage versus a reference and decide whether to use the oscillator to turn on the switch for that cycle or not. The hysteresis of the comparator tends to give rise to

several cycles of switching followed by several cycles of not switching. Hence, the resulting switching signal is characterized by pulses which tend to come in bursts - hence the name for the modulation technique.

There are at least two inherent fundamental drawbacks of the PBM switch modulation technique. First, the constant variation of the duty cycle between zero and maximum produces high ripple currents and accompanying losses. Second, there is an inherent generation of subharmonic frequencies with respect to the oscillator frequency. This means that the noise spectrum is not well controlled, and often audible frequencies can be produced. This is often apparent in higher power converters which use pulse skipping to maintain short-circuit current control. An audible noise can often be heard under such a condition, due to the large magnetics acting like speaker coils. For these reasons, PBM is seldom used at power levels above ~10 Watts. But for its simplicity, it is often preferred below that power level, but above a power level or with a power conversion requirement where charge pumps are not well suited.

CONTROL TECHNIQUES

Though often confused with or used in conjunction with discussing the switch modulation technique, the control technique refers to what parameters of operation are used and how they are used to control the modulation of the switch. The specific way in which the switch is modulated can be thought of separately, and was just presented in the previous section.

In circuits using PBM for switch modulation, the control technique typically used is a voltage-mode hysteretic control. In this implementation the switch is controlled by monitoring the output voltage and modulating the switch such that the output voltage oscillates between two hysteretic limits. The ADP3000 switching regulator is an example of a regulator which combines these modulation and control techniques.

The most basic control technique for use with PWM is *voltage-mode (VM) control* (see Figure 3.27). Here, the output voltage is the only parameter used to determine how the switch will be modulated. An error amplifier (first mentioned in the Buck Converter section) monitors the output voltage, its error is amplified with the required frequency compensation for maintaining stability of the control loop, and the switch is modulated directly in accordance with that amplifier output.

The output voltage is divided down by a ratio-matched resistor divider and drives one input of an amplifier, G. A precision reference voltage (V_{REF}) is applied to the other input of the amplifier. The output of the amplifier in turn controls the duty cycle of the PWM. It is important to note that the resistor divider, amplifier, and reference are actually part of the switching regulator IC, but are shown externally in the diagram for clarity. The output voltage is set by the resistor divider ratio and the reference voltage:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right).$$

The internal resistor ratios and the reference voltage are set to produce standard output voltage options such as 12V, 5V, 3.3V, or 3V. In some regulators, the resistor divider can be external, allowing the output voltage to be adjusted.

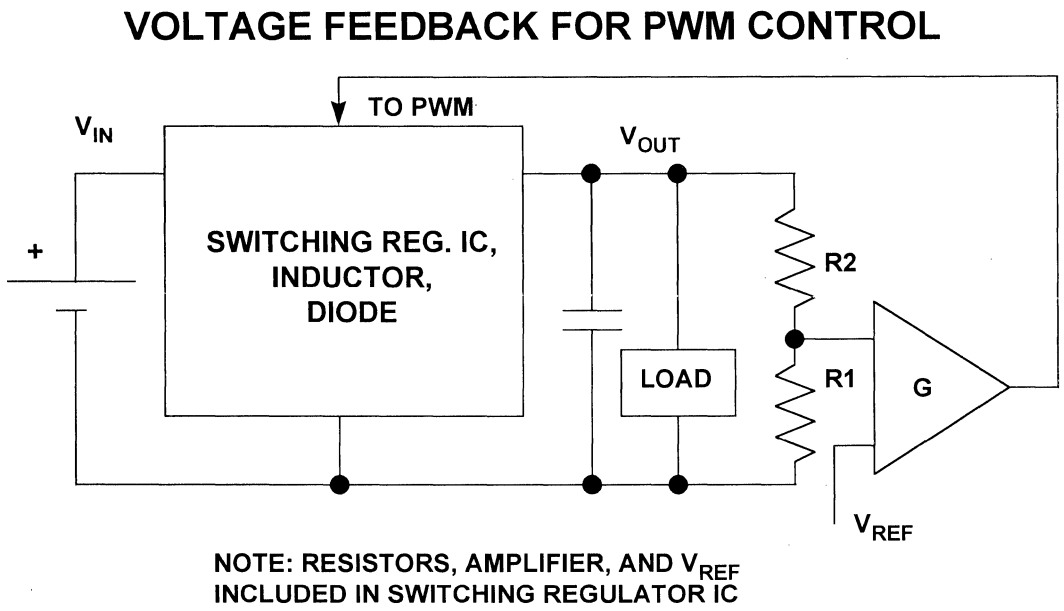


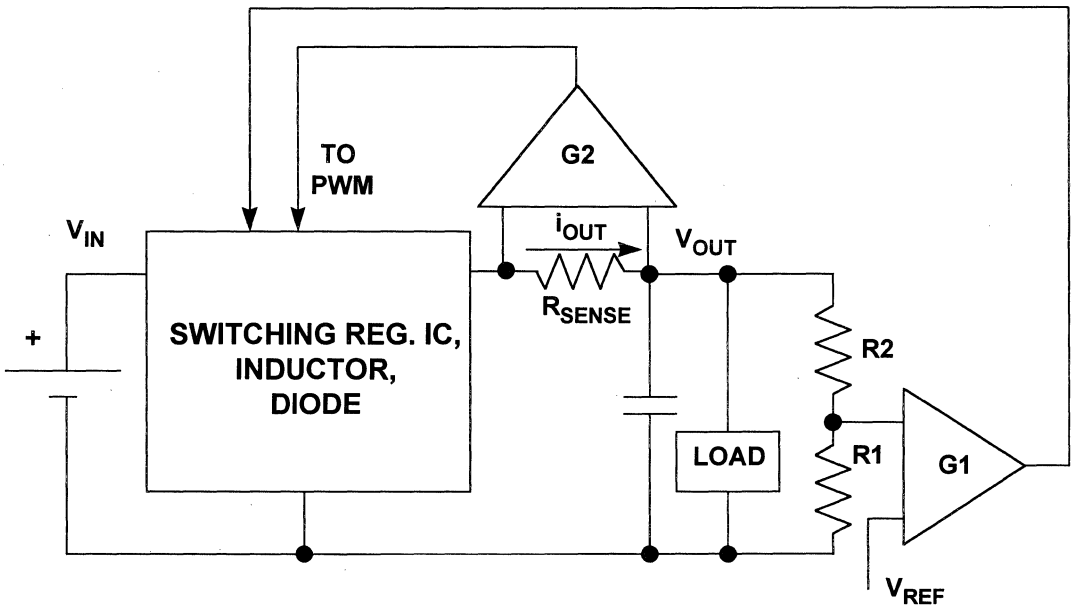
Figure 3.27

A simple modification of VM control is voltage *feedforward*. This technique adjusts the duty cycle automatically as the input voltage changes so that the feedback loop does not have to make an adjustment (or as much of an adjustment). Voltage feedforward can even be used in the simple PBM regulators. Feedforward is especially useful in applications where the input voltage can change suddenly or, perhaps due to current limit protection limitations, it is desirable to limit the maximum duty cycle to lower levels when the input voltage is higher.

In switchers, the VM control loop needs to be compensated to provide stability, considering that the voltage being controlled by the modulator is the average voltage produced at the switched node, whereas the actual output voltage is filtered through the switcher's LC filter. The phase shift produced by the filter can make it difficult to produce a control loop with a fast response time.

A popular way to circumvent the problem produced by the LC filter phase shift is to use current-mode (CM) control as shown in Figure 3.28. In current-mode control, it is still desirable, of course, to regulate the output voltage. Thus, an error amplifier (G1) is still required. However, the switch modulation is no longer controlled directly by the error amplifier. Instead, the inductor current is sensed, amplified by G2, and used to modulate the switch in accordance with the command signal from the [output voltage] error amplifier. It should be noted that the divider network, V_{REF}, G1 and G2 are usually part of the IC switching regulator itself, rather than external as shown in the simplified diagram.

CURRENT FEEDBACK FOR PWM CONTROL



NOTE: RESISTORS, AMPLIFIERS, AND V_{REF} INCLUDED IN SWITCHING REGULATOR IC

Figure 3.28

The CM control system uses feedback from both the output voltage and output current. Recall that at the beginning of each PWM cycle, the switch turns on, and the inductor current begins to rise. The inductor current develops a voltage across the small sense resistor, R_{SENSE}, which is amplified by G2 and fed back to the PWM controller to turn off the switch. The output voltage, sensed by amplifier G1 and also fed back to the PWM controller, sets the level at which the peak inductor current will terminate the switch on-time. Since it is inductor current that turns off the switch (and thereby sets the duty cycle) this method is commonly referred to as *current-mode* control, even though there are actually two feedback control loops: the fast responding current loop, and the slower responding output voltage loop. Note that inductor current is being controlled on a pulse-by-pulse basis, which simplifies protection against switch over-current and inductor saturation conditions.

In essence, then, in CM control, rather than controlling the average voltage which is applied to the LC filter as in VM control, the inductor current is controlled directly on a cycle-by-cycle basis. The only phase shift remaining between the inductor current and the output voltage is that produced by the impedance of the output capacitor(s). The correspondingly lower phase shift in the output filter allows the loop response to be faster while still remaining stable. Also, instantaneous changes in input voltage are immediately reflected in the inductor current, which provides excellent line transient response. The obvious disadvantage of CM control is the requirement of sensing current and, if needed, an additional amplifier. With increasingly higher performance requirements in modern electronic equipment, the performance advantage of CM control typically outweighs the cost of

implementation. Also, some sort of current limit protection is often required, whatever the control technique. Thus it tends to be necessary to implement some sort of current sensing even in VM-controlled systems.

Now even though we speak of a CM controller as essentially controlling the inductor current, more often than not the switch current is controlled instead, since it is more easily sensed (especially in a switching regulator) and it is a representation of the inductor current for at least the on-time portion of the switching cycle. Rather than actually controlling the average switch current, which is not the same as the average inductor current anyway, it is often simpler to control the peak current - which is the same for both the switch and the inductor in all the basic topologies. The error between the average inductor current and the peak inductor current produces a non-linearity within the control loop. In most systems, that is not a problem. In other systems, a more precise current control is needed, and in such a case, the inductor current is sensed directly and amplified and frequency-compensated for the best response.

Other control variations are possible, including *valley* rather than peak control, *hysteretic current* control, and even *charge* control - a technique whereby the integral of the inductor current (i.e., charge) is controlled. That eliminates even the phase shift of the output capacitance from the loop, but presents the problem that instantaneous current is not controlled, and therefore short-circuit protection is not inherent in the system. All techniques offer various advantages and disadvantages. Usually the best tradeoff between performance and cost/simplicity is peak-current control - as used by the ADP1147 family. This family also uses the current-sense output to control a *sleep, or power saving mode* of operation to maintain high efficiency for low output currents.

GATED OSCILLATOR (PULSE BURST MODULATION) CONTROL EXAMPLE

All of the PWM techniques discussed thus far require some degree of feedback loop compensation. This can be especially tricky for boost converters, where there is more phase shift between the switch and the output voltage.

As previously mentioned, a technique which requires no feedback compensation uses a fixed frequency gated oscillator as the switch control (see Figure 3.29). This method is often (incorrectly) referred to as the Pulse Frequency Modulation (PFM) mode, but is more correctly called *pulse burst modulation (PBM)* or *gated-oscillator* control.

The output voltage (V_{OUT}) is divided by the resistive divider (R1 and R2) and compared against a reference voltage, V_{REF}. The comparator hysteresis is required for stability and also affects the output voltage ripple. When the resistor divider output voltage drops below the comparator threshold (V_{REF} minus the hysteresis voltage), the comparator starts the gated oscillator. The switcher begins switching again which then causes the output voltage to increase until the comparator threshold is reached (V_{REF} plus the hysteresis voltage), at which time the oscillator is turned off. When the oscillator is off, quiescent current drops to a very low value

(for example, 95μA in the ADP1073) making PBM controllers very suitable for battery-powered applications.

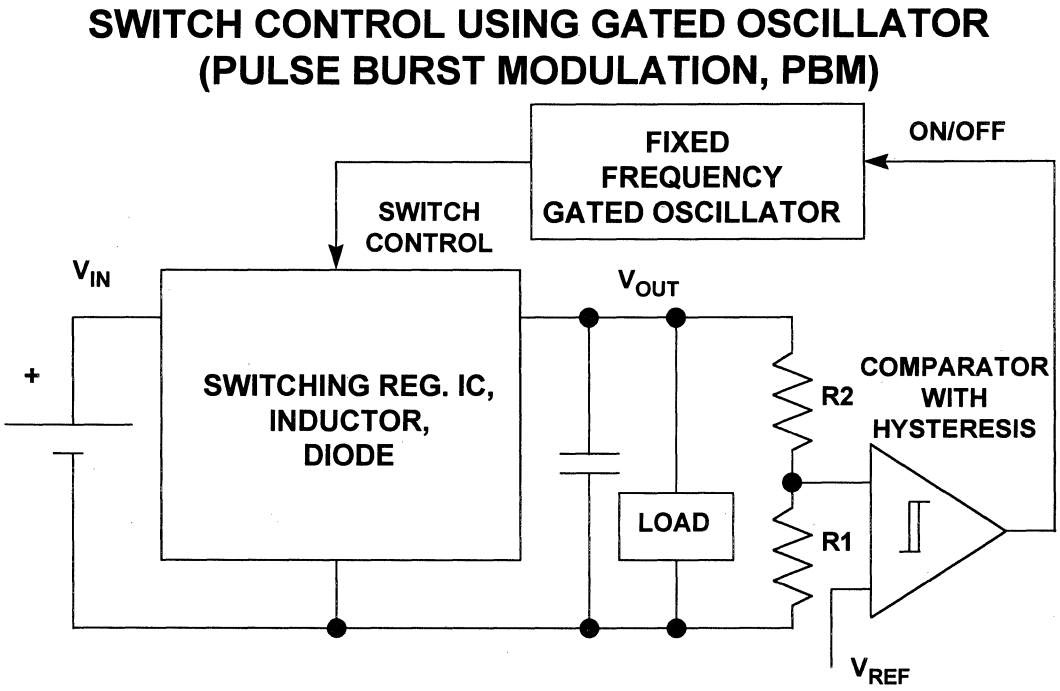


Figure 3.29

A simplified output voltage waveform is shown in Figure 3.30 for a PBM buck converter. Note that the comparator hysteresis voltage multiplied by the reciprocal of the attenuation factor primarily determines the peak-to-peak output voltage ripple (typically between 50 and 100mV). It should be noted that the actual output voltage ripple waveform can look quite different from that shown in Figure 3.30 depending on the design and whether the converter is a buck or boost.

A practical switching regulator IC using the PBM approach is the ADP3000, which has a fixed switching frequency of 400kHz and a fixed duty cycle of 80%. This device is a versatile step-up/step-down converter. It can deliver an output current of 100mA in a 5V to 3V step-down configuration and 180mA in a 2V to 3.3V step-up configuration. Input supply voltage can range between 2V and 12V in the boost mode, and up to 30V in the buck mode. It should be noted that when the oscillator is turned off, the internal switch is opened so that the inductor current does not continue to increase.

REPRESENTATIVE OUTPUT VOLTAGE WAVEFORM FOR GATED OSCILLATOR CONTROLLED (PBM) BUCK REGULATORS

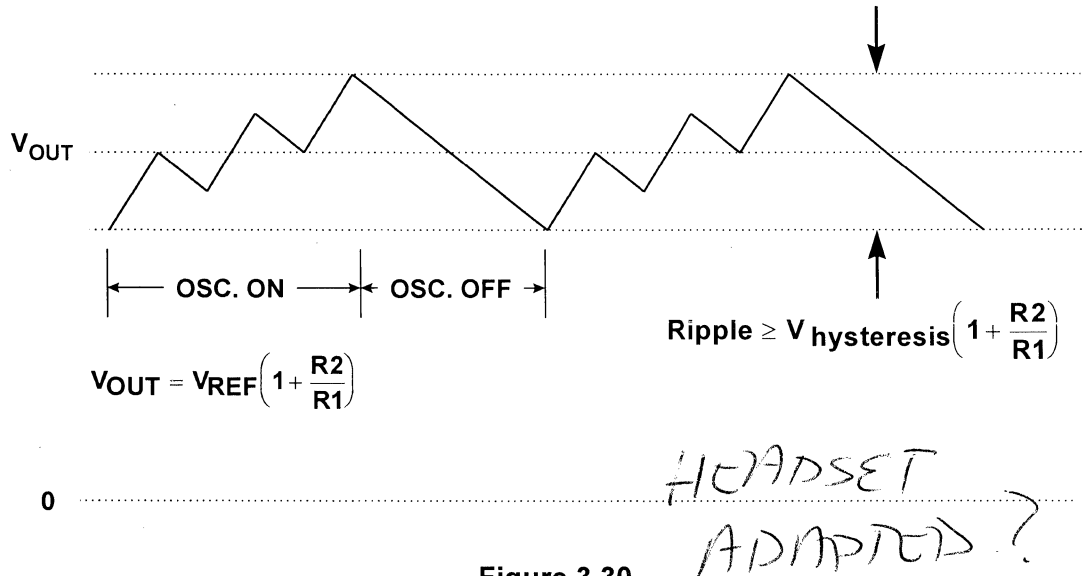


Figure 3.30

In the gated-oscillator method, the comparator hysteresis serves to stabilize the feedback loop making the designs relatively simple. The disadvantage, of course, is that the peak-to-peak output voltage ripple can never be less than the comparator hysteresis multiplied by the reciprocal of the attenuation factor:

$$\text{Output Ripple} \geq V_{hysteresis}\left(\frac{R2}{R1}\right).$$

Because the gated-oscillator (PBM) controlled switching regulator operates with a fixed duty cycle, output regulation is achieved by changing the number of "skipped pulses" as a function of load current and voltage. From this perspective, PBM controlled switchers tend to operate in the "discontinuous" mode under light load conditions. Also, the maximum average duty cycle is limited by the built-in duty cycle of the oscillator. Once the required duty cycle exceeds that limit, no pulse skipping occurs, and the device will lose regulation.

One disadvantage of the PBM switching regulator is that the frequency spectrum of the output ripple is "fuzzy" because of the burst-mode of operation. Frequency components may fall into the audio band, so proper filtering of the output of such a regulator is mandatory.

Selection of the inductor value is also more critical in PBM regulators. Because the regulation is accomplished with a burst of fixed duty cycle pulses (i.e., higher than needed on average) followed by an extended off time, the energy stored in the inductor during the burst of pulses must be sufficient to supply the required energy to the load. If the inductor value is too large, the regulator may never start up, or may have poor transient response and inadequate line and load regulation. On the other hand, if the inductor value is too small, the inductor may saturate during the

charging time, or the peak inductor current may exceed the maximum rated switch current. However, devices such as the ADP3000 incorporate on-chip overcurrent protection for the switch. An additional feature allows the maximum peak switch current to be set with an external resistor, thereby preventing inductor saturation. Techniques for selecting the proper inductor value will be discussed in a following section.

DIODE AND SWITCH CONSIDERATIONS

So far, we have based our discussions around an ideal lossless switching regulator having ideal circuit elements. In practice, the diode, switch, and inductor all dissipate power which leads to less than 100% efficiency.

Figure 3.31 shows typical buck and boost converters, where the switch is part of the IC. The process is bipolar, and this type of transistor is used as the switching element. The ADP3000 and its relatives (ADP1108, ADP1109, ADP1110, ADP1111, ADP1073, ADP1173) use this type of internal switch.

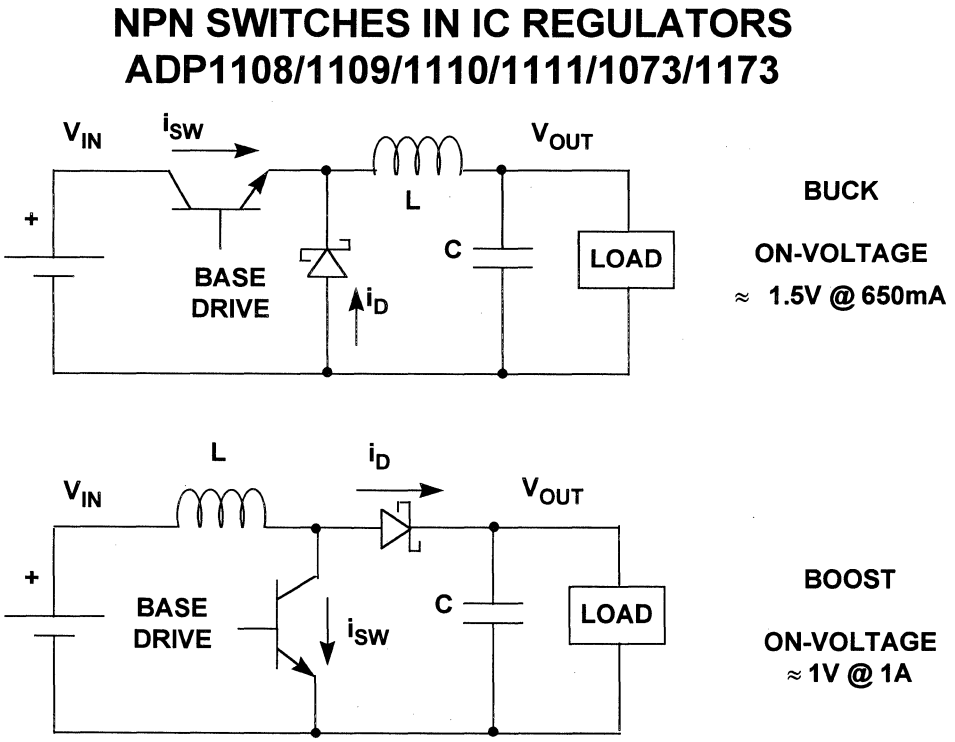


Figure 3.31

The diode is external to the IC and must be chosen carefully. Current flows through the diode during the off-time of the switching cycle. This translates into an average current which causes power dissipation because of the diode forward voltage drop. The power dissipation can be minimized by selecting a Schottky diode with a low forward drop (0.5V),such as the 1N5818-type. It is also important that the diode capacitance and recovery time be low to prevent additional power loss due to charging current, and this is also afforded by the Schottky diode. Power dissipation

can be approximated by multiplying the average diode current by the forward voltage drop.

The drop across the NPN switch also contributes to internal power dissipation. The power (neglecting switching losses) is equal to the average switch current multiplied by the collector-emitter on-state voltage. In the case of the ADP3000 series, it is 1.5V at the maximum rated switch current of 650mA (when operating in the buck mode).

In the boost mode, the NPN switch can be driven into saturation, so the on-state voltage is reduced, and thus, so is the power dissipation. Note that in the case of the ADP3000, the saturation voltage is about 1V at the maximum rated switch current of 1A.

In examining the two configurations, it would be logical to use a PNP switching transistor in the buck converter and an NPN transistor in the boost converter in order to minimize switch voltage drop. However, the PNP transistors available on processes which are suitable for IC switching regulators generally have poor performance, so the NPN transistor must be used for both topologies.

In addition to lowering efficiency by their power dissipation, the switching transistors and the diode also affect the relationship between the input and output voltage. The equations previously developed assumed zero switch and diode voltage drops. Rather than re-deriving all the equations to account for these drops, we will examine their effects on the inductor current for a simple buck and boost converter operating in the continuous mode as shown in Figure 3.32.

EFFECTS OF SWITCH AND DIODE VOLTAGE ON INDUCTOR CURRENT EQUATIONS

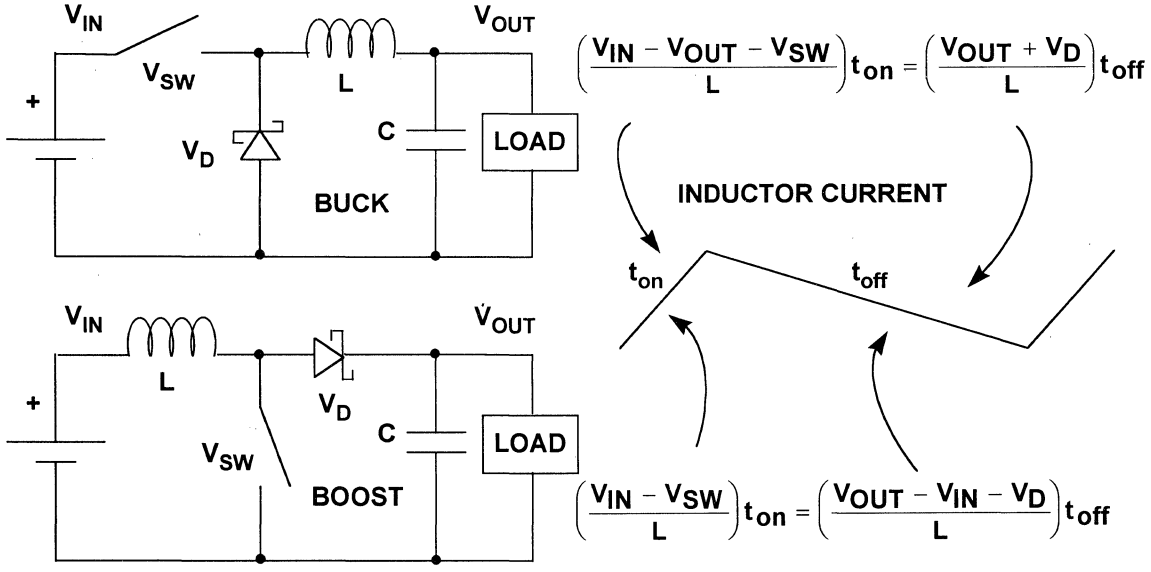


Figure 3.32

In the buck converter, the voltage applied to the inductor when the switch is on is equal to $V_{IN} - V_{OUT} - V_{SW}$, where V_{SW} is the approximate average voltage drop across the switch. When the switch is off, the inductor current is discharged into a voltage equal to $V_{OUT} + V_D$, where V_D is the approximate average forward drop across the diode. The basic inductor equation used to derive the relationship between the input and output voltage becomes:

$$\left(\frac{V_{IN} - V_{OUT} - V_{SW}}{L}\right)t_{on} = \left(\frac{V_{OUT} + V_D}{L}\right)t_{off}.$$

In the actual regulator circuit, negative feedback will force the duty cycle to maintain the correct output voltage, but the duty cycle will also be affected by the switch and the diode drops to a lesser degree.

When the switch is on in a boost converter, the voltage applied to the inductor is equal to $V_{IN} - V_{SW}$. When the switch is off, the inductor current discharges into a voltage equal to $V_{OUT} - V_{IN} - V_D$. The basic inductor current equation becomes:

$$\left(\frac{V_{IN} - V_{SW}}{L}\right)t_{on} = \left(\frac{V_{OUT} - V_{IN} - V_D}{L}\right)t_{off}.$$

From the above equations, the basic relationships between input voltage, output voltage, duty cycle, switch, and diode drops can be derived for the buck and boost converters.

The ADP3000 is a switching regulator that uses the NPN-type switch just discussed. A block diagram is shown in Figure 3.33 and key specifications are given in Figure 3.34.

ADP3000 SWITCHING REGULATOR BLOCK DIAGRAM

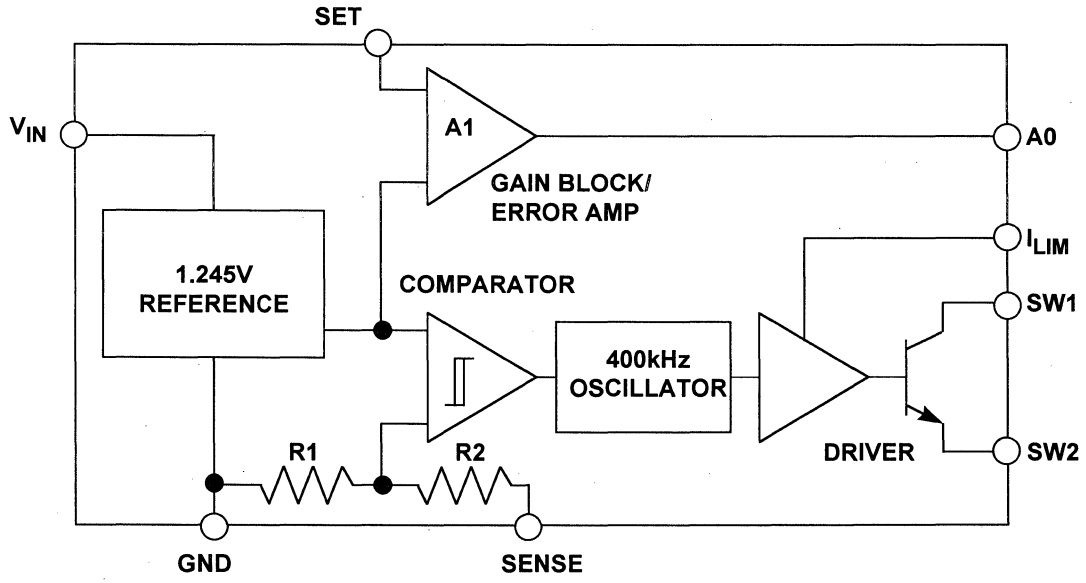


Figure 3.33

ADP3000 SWITCHING REGULATOR KEY SPECIFICATIONS

- **Input Voltages from 2V to 12V (Step-Up), 2V to 30V (Step-Down)**
- **Fixed 3.3V, 5V, 12V and Adjustable Output Voltage**
- **Step-Up or Step-Down Mode**
- **PBM (Gated Oscillator) Control Simplifies Design**
- **50mV Typical Output Ripple Voltage (5V Output)**
- **400kHz Switching Frequency Allows Low Value Inductors**
- **80% Duty Cycle**
- **500µA Quiescent Current**
- **Output Drive Capability:**
  - **100mA @ 3V from 5V Input in Step-Down Mode**
  - **180mA @ 3.3V from 2V Input in Step-Up Mode**
- **8-Pin DIP or SOIC Package**

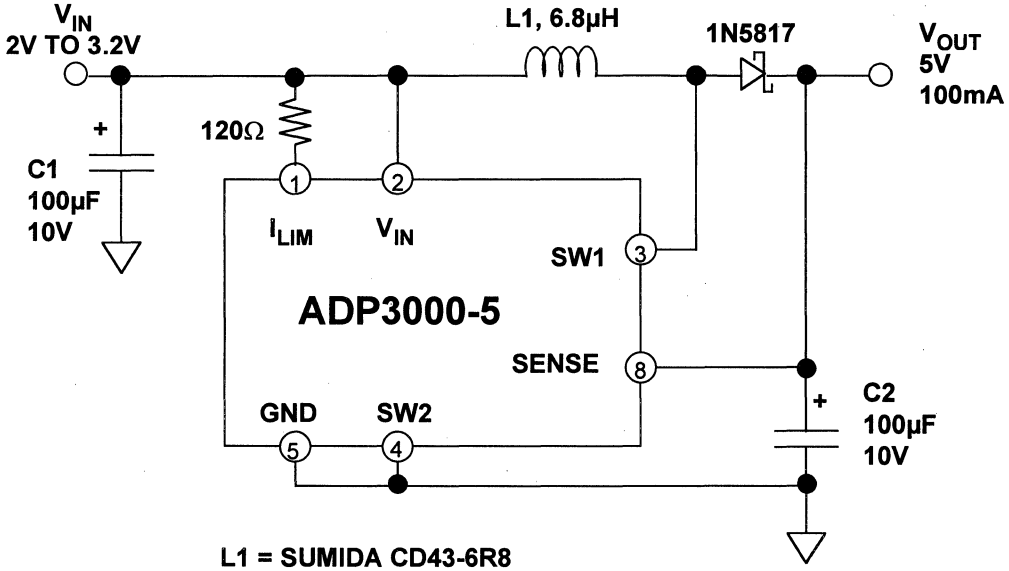
Figure 3.34

The device uses the gated oscillator, or pulse burst modulation (PBM) feedback control scheme. The internal oscillator operates at a frequency of 400kHz allowing the use of small value inductors and capacitors. The internal resistors, R1 and R2, set the output voltage to 3.3V, 5V, or 12V, depending upon the option selected. A completely adjustable version is also available where the comparator input is brought out directly to the "SENSE" pin, and the user provides the external divider resistors. Total quiescent current is only 500µA. The uncommitted gain block, A1, can be used as a low-battery detector or to reduce output hysteretic ripple limits by adding gain in the feedback loop. A current-limit pin, I_{LIM}, allows switch current to be limited with an external resistor. Limiting the switch current on a cycle by cycle basis allows the use of small inductors with low saturation current. It also allows physically small tantalum capacitors with a typical ESR of 0.1Ω to achieve an output ripple voltage as low as 40 to 80mV, as well as low input ripple current.

A typical ADP3000 boost application circuit is shown in Figure 3.35. The input voltage can range from +2V to +3.2V. The output is +5V and supplies a load current of 100mA. Typical efficiency for the circuit is 80%. All components are available in surface mount.

The ADP3000 can also be used in the buck configuration as shown in Figure 3.36. The input voltage to the regulator is between 5V and 6V, and the output is 3V at 100mA. Note that in this case, the adjustable version of the ADP3000 is used. The external divider resistors, R1 and R2, are chosen to set the nominal output voltage to 3V. All components are available in surface mount, and the efficiency of the circuit is approximately 75%.

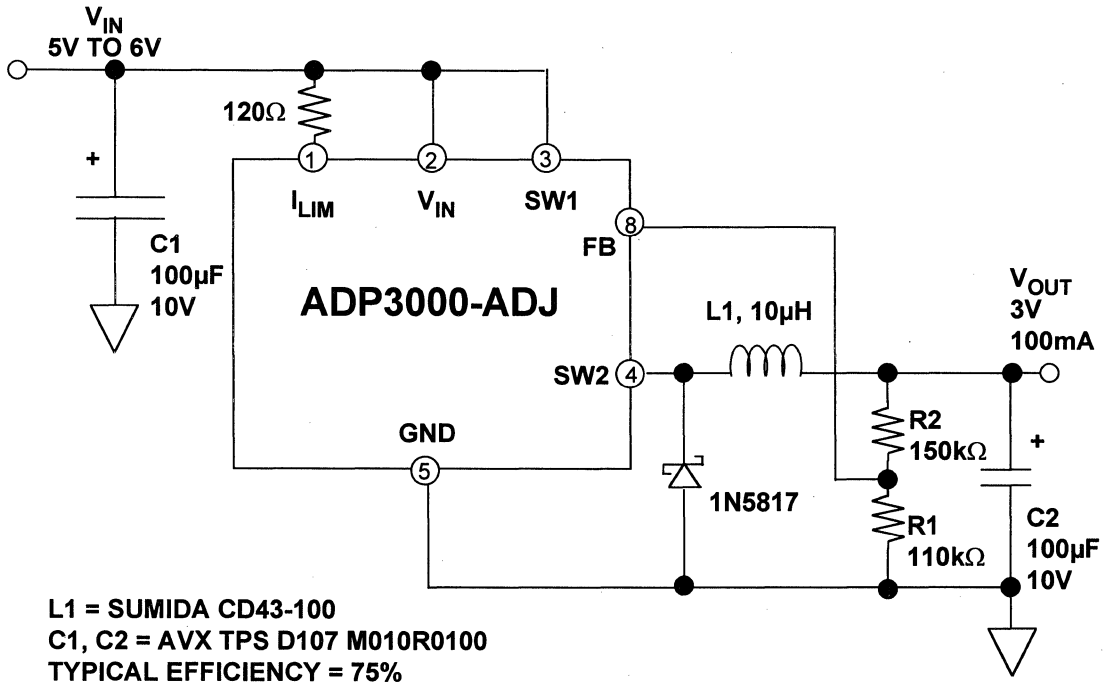
ADP3000 2V TO 5V BOOST APPLICATION



L1 = SUMIDA CD43-6R8
C1, C2 = AVX TPS D107 M010R0100
TYPICAL EFFICIENCY = 80%

Figure 3.35

ADP3000 5V TO 3V BUCK APPLICATION



L1 = SUMIDA CD43-100
C1, C2 = AVX TPS D107 M010R0100
TYPICAL EFFICIENCY = 75%

Figure 3.36

The ADP3050 is a 1.5A buck converter with an internal saturable NPN switch. It utilizes PWM current-mode control and operates at a fixed 250kHz switching frequency. An application circuit for the device is shown in Figure 3.37 and key specifications are summarized in Figure 3.38. A special boosted drive stage is used to saturate an NPN power switch, providing a system efficiency higher than conventional bipolar buck switchers. An external diode and capacitor provide the boosted voltage to the drive stage that is higher than the input supply voltage. A shutdown signal places the device in a low power mode, reducing the supply current to under 15μA. The ADP3050 provides excellent line and load regulation, maintaining ±2.5% output voltage accuracy over an ambient operating range of –40°C to +85°C. The ADP3050 package (8-pin SOIC footprint) is thermally enhanced and has a junction-to-ambient thermal resistance of approximately 90°C/W.

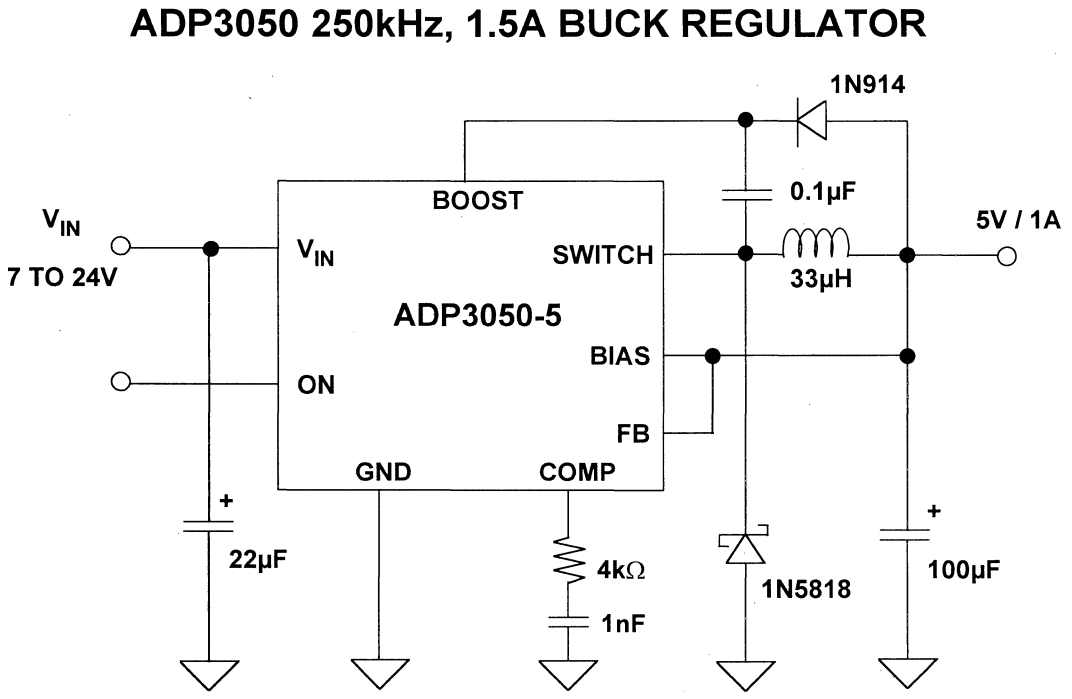


Figure 3.37

For high current output switchers, external power MOSFETs are often used as switches. The basic buck and boost converter circuits using MOSFETs are shown in Figure 3.39. On-resistances are typically 0.006Ω - 0.1Ω, depending upon power and efficiency requirements. The MOSFETs are generally discrete devices and are rarely integrated onto the IC regulator. The regulator generates the appropriate gate drive signal to the MOSFET.

ADP3050 BUCK REGULATOR KEY SPECIFICATIONS

- **Input Voltage Range: 3.6V to 24V**
- **3.3V, 5V, and Adjustable Output Versions**
- **0.5Ω Saturating NPN Switch**
- **250kHz Switching Frequency**
- **Current-Mode Control**
- **Cycle-by-Cycle Current Limit**
- **Shutdown Feature Reduces Current to 15μA**
- **8-Pin SOIC Thermally Enhanced Package,**
  $\theta_{JA} \approx$ 90°C/W

Figure 3.38

The main selection criteria for the power MOSFET is the peak current rating, threshold voltage, and the on-resistance. The minimum regulator input voltage determines whether a standard threshold or logic-level threshold MOSFET must be used. For input voltages greater than 8V, a standard threshold MOSFET with a threshold voltage of less than 4V can be used. If the input voltage is expected to drop below 8V, a logic-level MOSFET is recommended. In applications involving high current outputs and input voltages less than 8V, it may be necessary to drive the MOSFET gates with circuits which operate on a higher voltage, such as 12V. If this voltage is not available in the system, it can be derived from the input voltage using charge pump techniques (described in a later section) since the current requirements of the drive circuits are typically fairly low.

The I^2R loss in this type of regulator can be quite low because of the low MOSFET on-resistance, however one source of internal power dissipation which must not be overlooked is the gate charge required to turn the MOSFET on and off. The gate drive signal must overcome the gate capacitance (typically 1000 to 3000pF, and is directly proportional to physical size and the current-handling capability of the MOSFET). This current must be supplied by the input power supply and adds to the overall regulator power dissipation. It can be a significant contributor to efficiency reduction, up to 2 or 3% for output currents of 100 to 200mA.

Note that gate charge loss increases directly with both input voltage and operating frequency. This is the principal reason why highest efficiency circuits which utilize this topology operate at moderate frequencies of 200kHz or less. Furthermore, it argues against using a larger MOSFET than necessary to control on-resistance I^2R loss at the maximum expected output current.

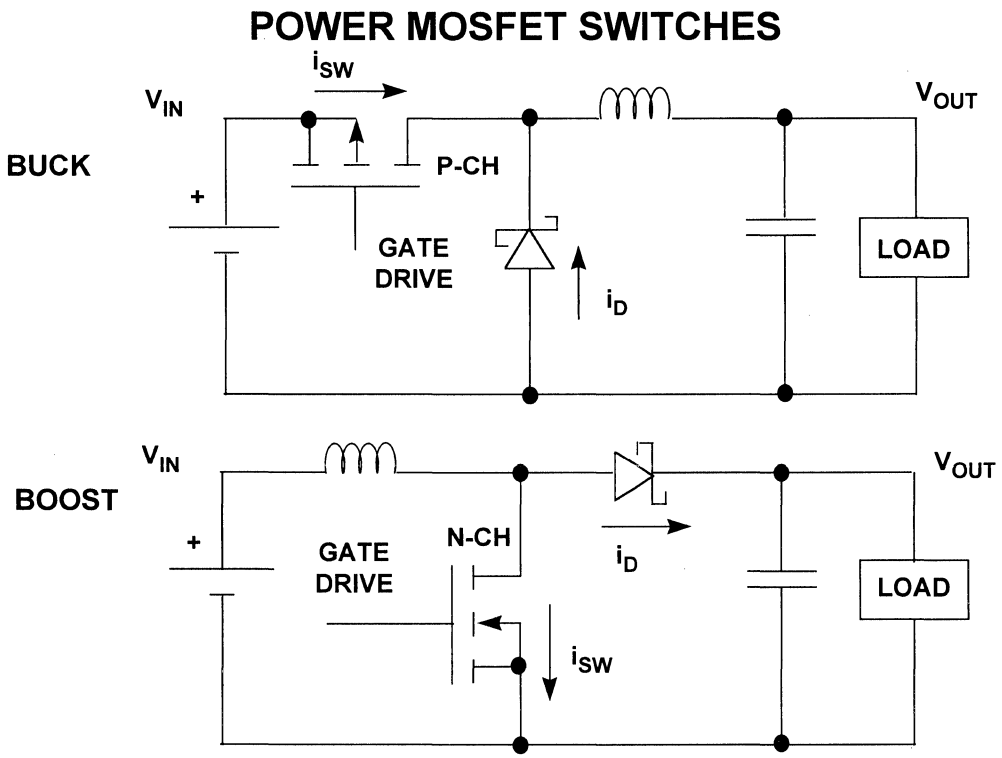


Figure 3.39

Power MOSFET switches allow current levels greater than 1A at high efficiencies (greater than 90%) using ICs such as the ADP1147 buck converter controller. The input voltage for the ADP1147 can range from 3.5V to 14V. Two output voltage versions are available : 3.3V (ADP1147-3.3) and 5V (ADP1147-5). The ADP1147 regulator controller operates in a constant off-time, variable frequency control mode with current-mode control. Operating in the constant off-time mode maintains constant inductor ripple current, thereby easing the output filter design. High efficiency is maintained at low output currents by switching automatically into a power-saving (PBM) mode.

A typical step-down application of the ADP1147 is shown in Figure 3.40. Input voltage in the circuit can range from 5.2V to 14V, and the output is 5V at 2A. The external resistor (R_C) and capacitor (C_C) connected to the I_{TH} pin serves to control the frequency response of the voltage feedback loop. The off-time of the regulator is determined by the external C_T capacitor. Current feedback is obtained from the voltage developed across the external R_{SENSE} resistor.

Typical efficiency is shown in the composite Figure 3.41, where the contributions of each source of efficiency loss are given (switch I^2R loss, gate charge loss, quiescent power loss, and Schottky diode loss). The lower curve represents the total efficiency. Note that for output currents between about 100mA and 1A, the power required to drive the MOSFET gate (gate charge) is the largest contributor to efficiency loss. At the higher current levels, the I^2R loss due to MOSFET on resistance dominates. Key specifications for the ADP1147 are summarized in Figure 3.42.

HIGH EFFICIENCY STEP DOWN REGULATOR USING THE ADP1147 CONTROLLER

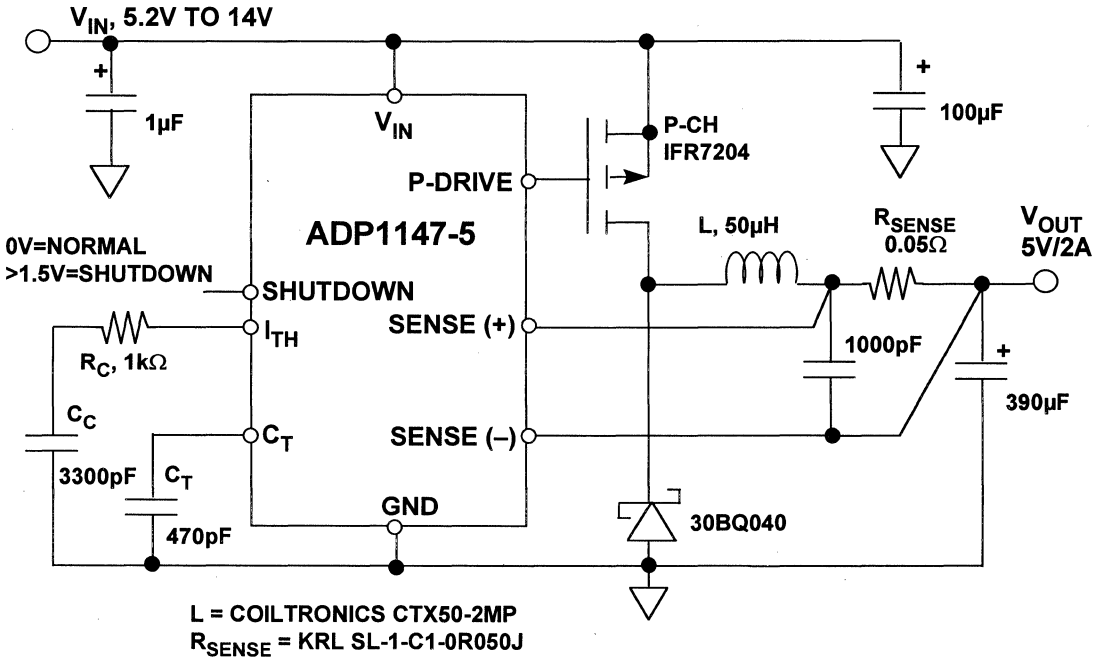


Figure 3.40

ADP1147 TYPICAL EFFICIENCY LOSSES

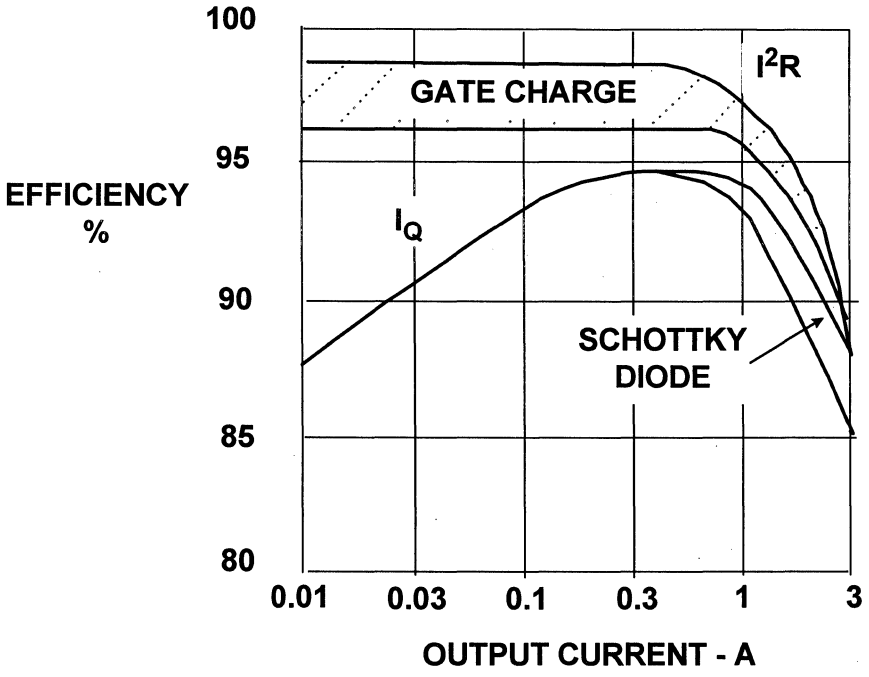


Figure 3.41

ADP1147 STEP-DOWN REGULATOR CONTROLLER KEY SPECIFICATIONS

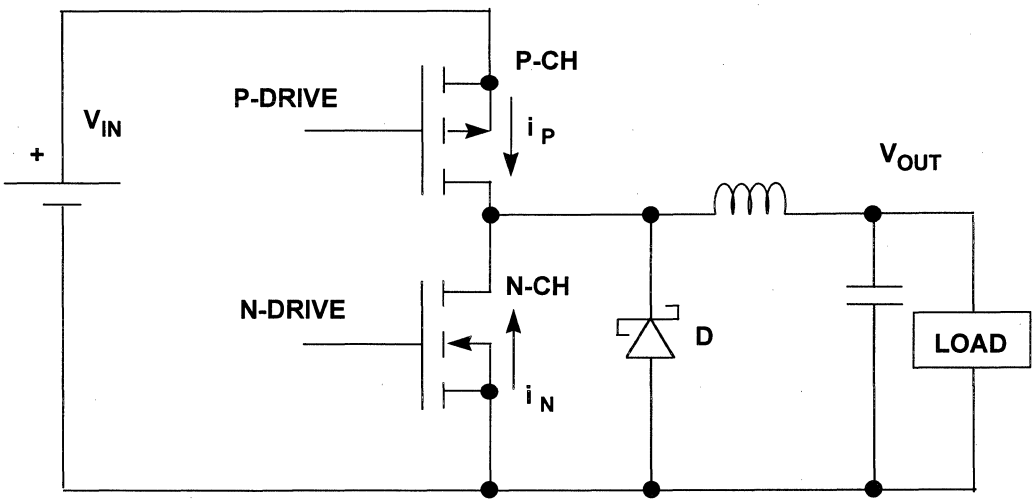
- **Input Voltage Range: 3.5V to 14V (16V Max.)**
- **Output Voltage Options: 3.3V, 5V**
- **Current-Mode Control Circuit**
- **Constant Off-Time (5μs), Variable Frequency**
- **P-Channel MOSFET Gate Drive Output**
- **Power Saving Mode: 160μA Typical**
- **Up to 95% Efficiency**
- **8-Pin SOIC and DIP Packages**

Figure 3.42

In order to achieve even higher efficiency, the Schottky diode can be replaced with an N-channel MOSFET switch as shown in Figure 3.43. This configuration is referred to as a *synchronous rectifier*, or *synchronous switch*, because the switching of the N-channel MOSFET switch must be synchronized to the switching of the P-channel MOSFET switch so that it essentially passes the current in one direction and blocks it in the other direction, just like a rectifier or diode. This terminology does not imply that the switching *frequency* of the regulator is synchronized to an external clock.

The gate drive signals from the controller must be non-overlapping to prevent cross-conduction current spikes in the switches. This means that there is a period of time when both switches are off. The external Schottky diode prevents the body diode of the N-channel MOSFET from conducting during this time. It is not always necessary to add the Schottky diode, but it will increase overall efficiency slightly even if not required.

BUCK CONVERTER WITH SYNCHRONOUS SWITCH USING P AND N-CHANNEL MOSFETS



SCHOTTKY DIODE PREVENTS BODY DIODE OF N-CHANNEL MOSFET FROM CONDUCTING DURING "DEADTIME"

Figure 3.43

The ADP1148 is a high efficiency synchronous step-down switching regulator controller with an input voltage range of 3.5V to 18V. It utilizes a constant off-time, variable frequency current-mode control topology and is available in three versions: the ADP1148-3.3 (3.3V output), the ADP1148-5 (5V output), and the ADP1148 (adjustable output). At low output currents, the device switches into a power-saving mode to maintain high efficiency.

An application circuit for the ADP1148 synchronous step-down regulator controller is shown in Figure 3.44. Operation of the ADP1148 is similar to the ADP1147 with the addition of the drive circuitry for the synchronous N-channel MOSFET. The input voltage can range from 5.2V to 18V, and the output is 5V at 2A. A breakdown of the ADP1148 efficiency losses is shown in Figure 3.45, where the lower curve represents the total efficiency. Key specifications for the device are given in Figure 3.46.

HIGH EFFICIENCY STEP-DOWN REGULATOR USING THE ADP1148 CONTROLLER

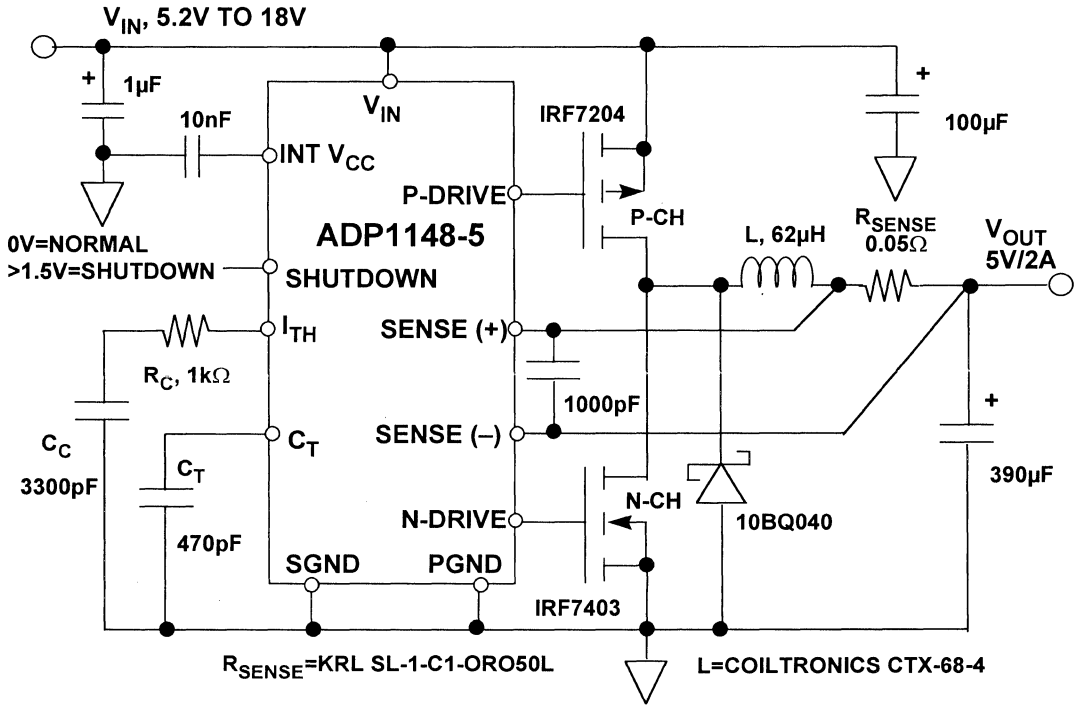


Figure 3.44

ADP1148 TYPICAL EFFICIENCY LOSSES

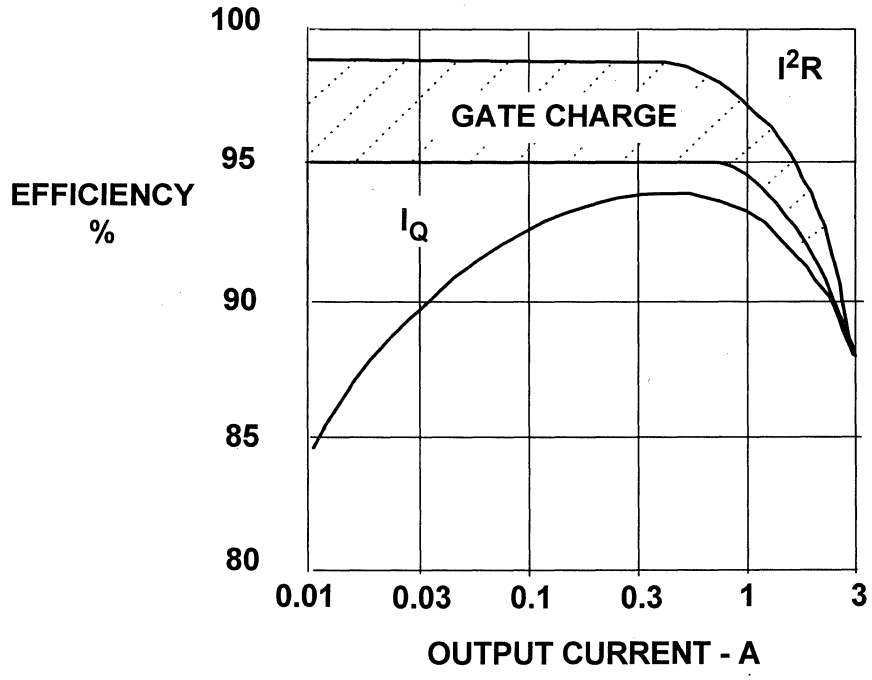


Figure 3.45

ADP1148 HIGH EFFICIENCY SYNCHRONOUS SWITCH REGULATOR CONTROLLER KEY SPECIFICATIONS

- **Input Voltage Range: 3.5V to 18V (20V Max.)**
- **Output Voltage Options: 3.3V, 5V, and Adjustable**
- **Current-Mode Control Circuit**
- **Non-Overlapping P and N-Channel MOSFET Gate Drive Outputs**
- **Constant Off-Time (5μs), Variable Frequency**
- **Power Saving Mode: 160μA Typical**
- **Up to 95% Efficiency Possible**
- **14-Pin SOIC and DIP Packages**

Figure 3.46

The ADP3153 is a 5-bit programmable synchronous switching regulator controller suitable for the Pentium II processor. An application circuit is shown in Figure 3.47, and key specifications are given in Figure 3.48. The ADP3153 is optimized for applications where 5V is stepped down to a digitally controlled output voltage between 1.8V and 3.5V. Using a 5-bit DAC to read a voltage identification (VID) code directly from the processor, the ADP3153 generates the precise output voltage by using a current mode constant off-time topology to drive two N-channel MOSFETs at a nominal switching frequency of 250kHz. The constant off-time topology maintains constant inductor ripple current, and current mode operation together with an optimal compensation design provide excellent line and load transient response. The current limit level is user programmable with an external current sense resistor.

ADP3153 POWER SUPPLY CONTROLLER FOR PENTIUM II (SIMPLIFIED SCHEMATIC)

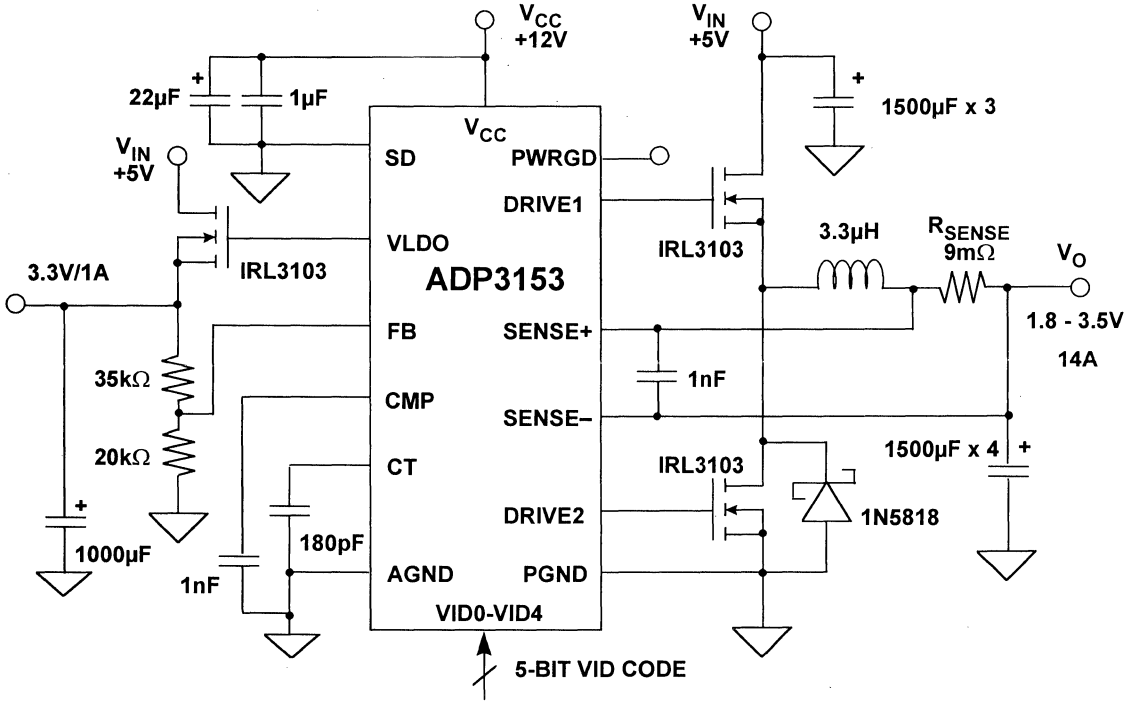


Figure 3.47

ADP3153 VID-PROGRAMMABLE MICROPROCESSOR CONTROLLER KEY SPECIFICATIONS

- 5-Bit Digitally Programmable 1.8V to 3.5V Output Voltage
- Dual N-Channel Driver Outputs
- Output Accuracy: ±1% (0°C to +70°C)
- Constant Off-Time, Variable Frequency Current-Mode Control
- On-Chip Adjustable Linear Regulator Controller
- 20-Lead TSSOP Package
- Suitable for Pentium II, Pentium Pro, AMD-K6 Processors

Figure 3.48

INDUCTOR CONSIDERATIONS

The selection of the inductor used in a switching regulator is probably the most difficult part of the design. Fortunately, manufacturers of switching regulators supply a wealth of applications information, and standard off-the-shelf inductors from well-known and reliable manufacturers are quite often recommended on the switching regulator data sheet. However, it is important for the design engineer to understand at least some of the fundamental issues relating to inductors. This discussion, while by no means complete, will give some insight into the relevant magnetics issues.

Selecting the actual value for the inductor in a switching regulator is a function of many parameters. Fortunately, in a given application the exact value is generally not all that critical, and equations supplied on the data sheets allow the designer to calculate a minimum and maximum acceptable value. That's the easy part.

Unfortunately, there is more to a simple inductor than its inductance! Figure 3.49 shows an equivalent circuit of a real inductor and also some of the many considerations that go into the selection process. To further complicate the issue, most of these parameters interact, thereby making the design of an inductor truly more of an art than a science.

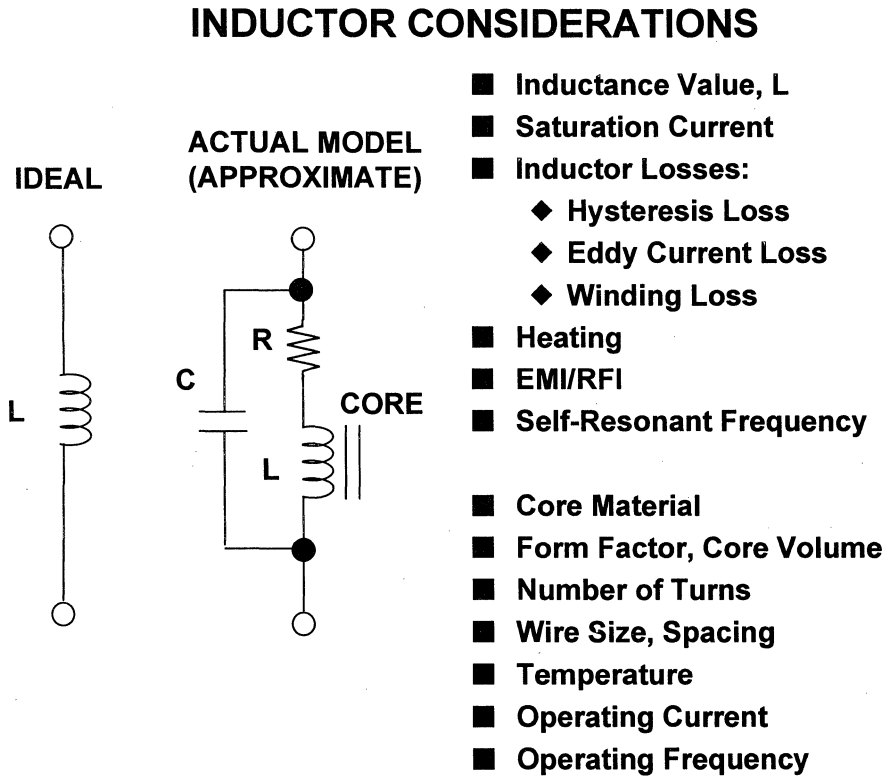


Figure 3.49

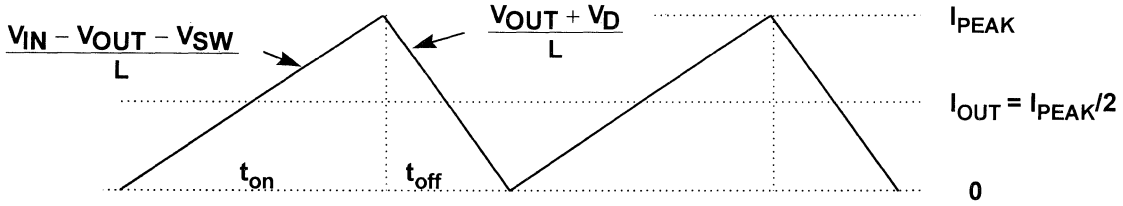
Probably the easiest inductor problem to solve is selecting the proper value. In most switching regulator applications, the exact value is not very critical, so approximations can be used with a high degree of confidence.

The heart of a switching regulator analysis involves a thorough understanding of the inductor current waveform. Figure 3.50 shows an assumed inductor current waveform (which is also the output current) for a buck converter, such as the ADP3000, which uses the gated-oscillator PBM switch modulation technique. Note that this waveform represents a worst case condition from the standpoint of storing energy in the inductor, where the inductor current starts from zero on each cycle. In high output current applications, the inductor current does not return to zero, but ramps up until the output voltage comparator senses that the oscillator should be turned off, at which time the current ramps down until the comparator turns the oscillator on again. This assumption about the worst case waveform is necessary because in a simple PBM regulator, the oscillator duty cycle remains constant regardless of input voltage or output load current. Selecting the inductor value using this assumption will always ensure that there is enough energy stored in the inductor to maintain regulation.

It should be emphasized that the following inductance calculations for the PBM buck and boost regulators should be used only as a starting point, and larger or smaller values may actually be required depending on the specific regulator and the input/output conditions.

CALCULATING L FOR BUCK CONVERTER: GATED OSCILLATOR (PBM) TYPE

OUTPUT AND INDUCTOR CURRENT:



$$I_{PEAK} = \left(\frac{V_{IN} - V_{OUT} - V_{SW}}{L}\right) t_{on}$$

$$L = \left(\frac{V_{IN} - V_{OUT} - V_{SW}}{2\, I_{OUT}}\right) t_{on}$$

USE MINIMUM V_{IN}

Figure 3.50

The peak current is easily calculated from the slope of the positive-going portion of the ramp:

$$I_{PEAK} = \left(\frac{V_{IN} - V_{OUT} - V_{SW}}{L}\right) t_{on} .$$

This equation can then be solved for L:

$$L = \left(\frac{V_{IN} - V_{OUT} - V_{SW}}{I_{PEAK}}\right) t_{on} .$$

However, the average output current, I_{OUT} is equal to $I_{PEAK}/2$, and therefore $I_{PEAK}=2I_{OUT}$. Substituting this value for I_{PEAK} into the previous equation yields:

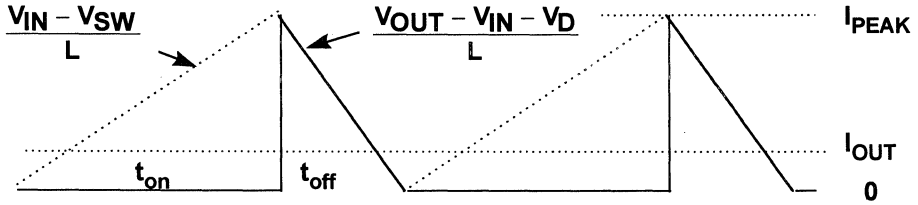
$$L = \left(\frac{V_{IN} - V_{OUT} - V_{SW}}{2I_{OUT}}\right) t_{on} . \quad \text{[L for buck PBM Converter]}$$

The minimum expected value of V_{IN} should be used in order to minimize the inductor value and maximize its stored energy. If V_{IN} is expected to vary widely, an external resistor can be added to the ADP3000 to limit peak current and prevent inductor saturation at maximum V_{IN}.

A similar analysis can be carried out for a boost PBM regulator as shown in Figure 3.51.

CALCULATING L FOR BOOST CONVERTER: GATED OSCILLATOR (PBM) TYPE

OUTPUT CURRENT:



$$DC = \frac{1}{t_{on} + t_{off}}$$

$$I_{OUT} = \frac{I_{PEAK}}{2}(1 - D) \qquad I_{PEAK} = \frac{2 I_{OUT}}{1 - D}$$

$$I_{PEAK} = \left(\frac{V_{IN} - V_{SW}}{L}\right) t_{on}$$

$$L = \left(\frac{V_{IN} - V_{SW}}{I_{PEAK}}\right) t_{on} = \left(\frac{V_{IN} - V_{SW}}{2 I_{OUT}}\right)(1 - D) t_{on}$$

USE MINIMUM V_{IN}

Figure 3.51

We make the same assumptions about the inductor current, but note that the output current shown on the diagram is pulsating and not continuous. The output current, I_{OUT}, can be expressed in terms of the peak current, I_{PEAK}, and the duty cycle, D, as:

$$I_{OUT} = \frac{I_{PEAK}}{2}(1 - D).$$

Solving for I_{PEAK} yields:

$$I_{PEAK} = \frac{2I_{OUT}}{1 - D}.$$

However, I_{PEAK} can also be expressed in terms of V_{IN}, V_{SW}, L, and t_{on}:

$$I_{PEAK} = \left(\frac{V_{IN} - V_{SW}}{L}\right)t_{on}, \text{ which can be solved for L:}$$

$$L = \left(\frac{V_{IN} - V_{SW}}{I_{PEAK}}\right)t_{on}.$$

Substituting the previous expression for I_{PEAK} yields:

$$L = \left(\frac{V_{IN} - V_{SW}}{2I_{OUT}}\right)(1 - D)t_{on}. \qquad \text{[L for boost PBM Converter]}$$

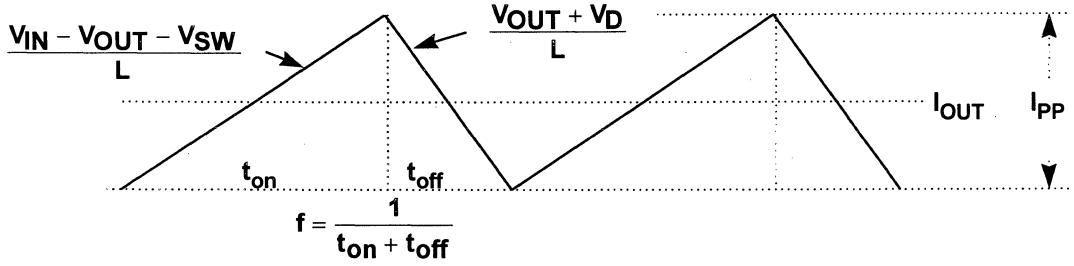
The minimum expected value of V_{IN} should be used in order to ensure sufficient inductor energy storage under all conditions. If V_{IN} is expected to vary widely, an external resistor can be added to the ADP3000 to limit peak current and prevent inductor saturation at maximum V_{IN}.

The above equations will only yield approximations to the proper inductor value for the PBM-type regulators and should be used only as a starting point. An exact analysis is difficult and highly dependent on the regulator and input/output conditions. However, there is considerable latitude with this type of regulator, and other analyses may yield different results but still fall within the allowable range for proper regulator operation.

Calculating the proper inductor value for PWM regulators is more straightforward. Figure 3.52 shows the output and inductor current waveform for a buck PWM regulator operating in the continuous mode. It is accepted design practice to design for a peak-to-peak ripple current, I_{pp}, which is between 10% and 30% of the output current, I_{OUT}. We will assume that $I_{pp}=0.2I_{OUT}$.

CALCULATING L FOR BUCK CONVERTER: CONSTANT FREQUENCY PWM TYPE

OUTPUT AND INDUCTOR CURRENT, CONTINUOUS MODE:



$$L = \left(\frac{1}{f}\right)\left(\frac{V_{IN} - V_{OUT} - V_{SW}}{V_{IN} - V_{SW} + V_D}\right)\left(\frac{V_{OUT} + V_D}{I_{PP}}\right)$$

NOMINALLY, MAKE $I_{PP} = 0.2\ I_{OUT}$

Figure 3.52

By inspection, we can write:

$$\left(\frac{V_{IN} - V_{OUT} - V_{SW}}{L}\right)t_{on} = \left(\frac{V_{OUT} + V_D}{L}\right)t_{off}\text{, or}$$

$$t_{off} = \left(\frac{V_{IN} - V_{OUT} - V_{SW}}{V_{OUT} + V_D}\right)t_{on}.$$

However, the switching frequency, f, is given by

$$f = \frac{1}{t_{on} + t_{off}}\text{, or} \qquad t_{off} = \frac{1}{f} - t_{on}.$$

Substituting this expression for t_{off} in the previous equation for t_{off} and solving for t_{on} yields:

$$t_{on} = \frac{1}{f}\left(\frac{V_{OUT} + V_D}{V_{IN} - V_{SW} + V_D}\right).$$

However,

$$I_{pp} = \left(\frac{V_{IN} - V_{OUT} - V_{SW}}{L}\right)t_{on}.$$

Combining the last two equations and solving for L yields:

$$L = \left(\frac{1}{f}\right)\left(\frac{V_{IN} - V_{OUT} - V_{SW}}{V_{IN} - V_{SW} + V_D}\right)\left(\frac{V_{OUT} + V_D}{I_{pp}}\right). \quad \text{[L for buck PWM converter, constant frequency]}$$

As indicated earlier, choose I_{pp} to be nominally $0.2I_{OUT}$ and solve the equation for L. Calculate L for the minimum and maximum expected value of V_{IN} and choose a value halfway between. System requirements may dictate a larger or smaller value of I_{pp}, which will inversely affect the inductor value.

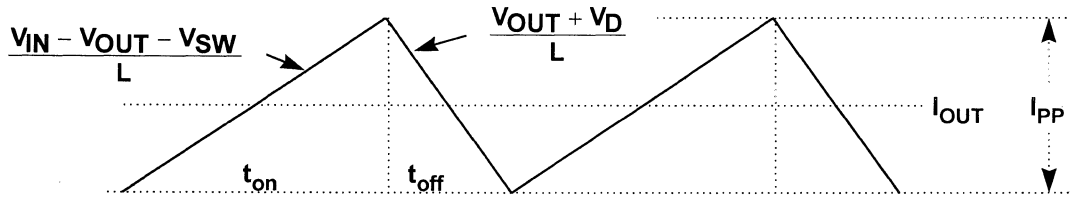
A variation of the buck PWM constant frequency regulator is the buck PWM regulator with variable frequency and constant off-time (e.g., ADP1147, ADP1148).

A diagram of the output and inductor current waveform is shown in Figure 3.53 for the continuous mode.

3

CALCULATING L FOR BUCK CONVERTER: CONSTANT OFF-TIME, VARIABLE FREQUENCY PWM TYPE

OUTPUT AND INDUCTOR CURRENT, CONTINUOUS MODE:



$$\left(\frac{V_{OUT} + V_D}{L}\right) t_{off} = I_{PP}$$

$$L = \left(\frac{V_{OUT} + V_D}{I_{PP}}\right) t_{off}$$

NOMINALLY, MAKE $I_{PP} = 0.2\ I_{OUT}$

Figure 3.53

The calculations are very straightforward, since the peak-to-peak amplitude of the ripple current is constant:

$$I_{pp} = \left(\frac{V_{OUT} + V_D}{L}\right) t_{off}.$$

Solving for L:

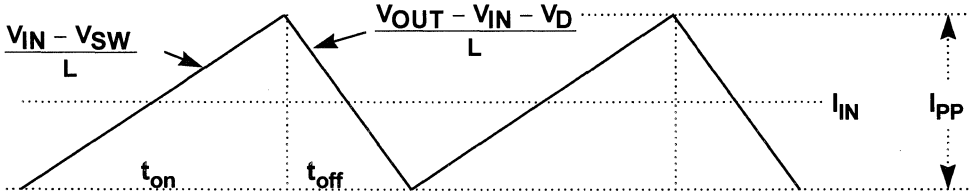
$$L = \left(\frac{V_{OUT} + V_D}{I_{pp}}\right) t_{off} . \qquad \text{[L for buck PWM constant off-time, variable frequency converter]}$$

Again, choose $I_{pp} = 0.2 I_{OUT}$, or whatever the system requires.

The final example showing the inductance calculation is for the boost PWM constant frequency regulator. The inductor (and input) current waveform is shown in Figure 3.54.

CALCULATING L FOR BOOST CONVERTER: CONSTANT FREQUENCY PWM TYPE

INPUT AND INDUCTOR CURRENT, CONTINUOUS MODE:



$$f = \frac{1}{t_{on} + t_{off}}$$

$$L = \left(\frac{1}{f}\right)\left(\frac{V_{OUT} - V_{IN} - V_D}{V_{OUT} - V_{SW} - V_D}\right)\left(\frac{V_{IN} - V_{SW}}{I_{PP}}\right)$$

$$I_{IN} = \left(\frac{V_{OUT}}{V_{IN}}\right) I_{OUT}$$

NOMINALLY, MAKE $I_{PP} = 0.2\ I_{IN}$

Figure 3.54

The analysis is similar to that of the constant frequency buck PWM regulator.

By inspection of the inductor current, we can write:

$$\left(\frac{V_{IN} - V_{SW}}{L}\right) t_{on} = \left(\frac{V_{OUT} - V_{IN} - V_D}{L}\right) t_{off} , \text{ or}$$

$$t_{off} = \left(\frac{V_{IN} - V_{SW}}{V_{OUT} - V_{IN} - V_D}\right) t_{on} .$$

However, the switching frequency, f, is given by

$$f = \frac{1}{t_{on} + t_{off}}, \text{ or } \quad t_{off} = \frac{1}{f} - t_{on}.$$

Substituting this expression for t_{off} in the previous equation for t_{off} and solving for t_{on} yields:

$$t_{on} = \frac{1}{f}\left(\frac{V_{OUT} - V_{IN} - V_D}{V_{OUT} - V_{SW} - V_D}\right).$$

However,

$$I_{pp} = \left(\frac{V_{IN} - V_{SW}}{L}\right)t_{on}.$$

Combining the last two equations and solving for L yields:

$$L = \left(\frac{1}{f}\right)\left(\frac{V_{OUT} - V_{IN} - V_D}{V_{OUT} - V_{SW} - V_D}\right)\left(\frac{V_{IN} - V_{SW}}{I_{pp}}\right). \quad \text{[L for boost PWM, constant frequency converter]}$$

For the boost converter, the inductor (input) current, I_{IN}, can be related to the output current, I_{OUT}, by:

$$I_{IN} = \left(\frac{V_{OUT}}{V_{IN}}\right)I_{OUT}.$$

Nominally, make $I_{pp} = 0.2I_{IN}$.

Note that for the boost PWM, even though the input current is continuous, while the output current pulsates, we still base the inductance calculation on the peak-to-peak inductor ripple current.

As was previously suggested, the actual selection of the inductor value in a switching regulator is probably the easiest part of the design process. Choosing the proper type of inductor is much more complicated as the following discussions will indicate.

Fundamental magnetic theory says that if a current passes through a wire, a magnetic field will be generated around the wire (right-hand rule). The strength of this field is measured in ampere-turns per meter, or *oersteds* and is proportional to the current flowing in the wire. The magnetic field strength produces a *magnetic flux density* (B, measured in webers per square meter, or *gauss*).

Using a number of turns of wire to form a coil increases the magnetic flux density for a given current. The effective inductance of the coil is proportional to the ratio of the magnetic flux density to the field strength.

This simple air core inductor is not very practical for the values of inductance required in switching regulators because of wiring resistance, interwinding capacitance, sheer physical size, and other factors. Therefore, in order to make a reasonable inductor, the wire is wound around some type of ferromagnetic core having a high *permeability*. Core permeability is often specified as a relative permeability which is basically the increase in inductance which is obtained when the inductor is wound on a core instead of just air. A relative permeability of 1000, for instance, will increase inductance by 1000:1 above that of an equivalent air core.

Figure 3.55 shows magnetic flux density (B) versus inductor current for the air core and also ferromagnetic cores. Note that B is linear with respect to H for the air core inductor, i.e., the inductance remains constant regardless of current.

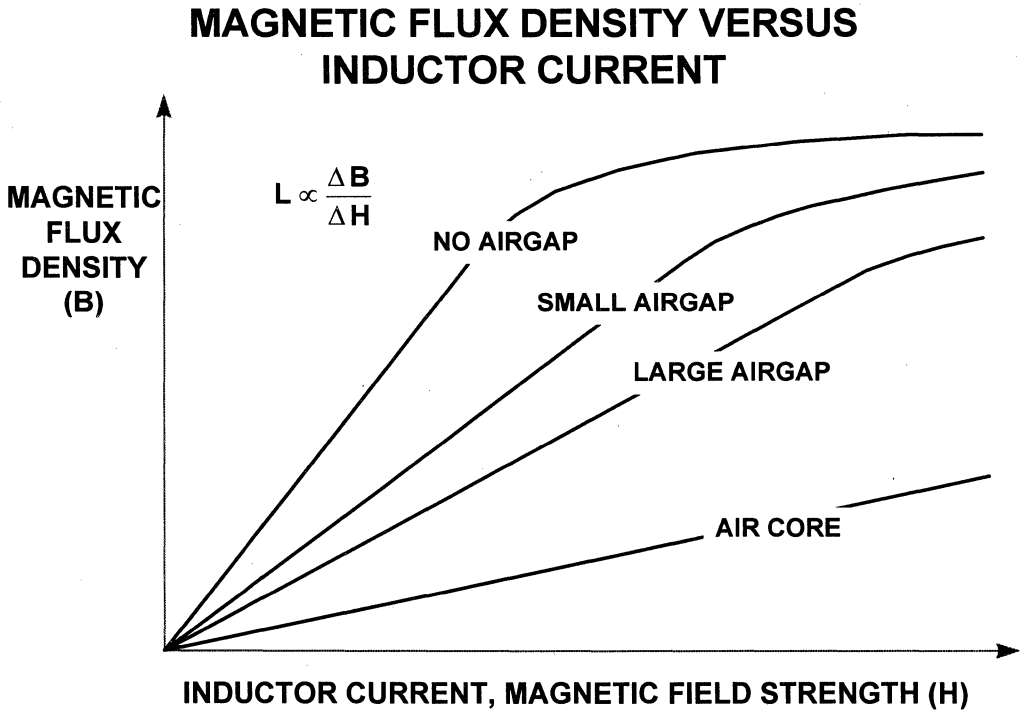


Figure 3.55

The addition of a ferromagnetic core increases the slope of the curve and increases the effective inductance, but at some current level, the inductor core will saturate (i.e., the inductance is drastically reduced). It is obvious that inductor saturation can wreck havoc in a switching regulator, and can even burn out the switch if it is not current-limited.

This effect can be reduced somewhat while still maintaining higher inductance than an air core by the addition of an air gap in the ferromagnetic core. The air gap reduces the slope of the curve, but provides a wider linear operating range of inductor current. Air gaps do have their problems, however, and one of them is the

tendency of the air-gapped inductor to radiate high frequency energy more than a non-gapped inductor. Proper design and manufacturing techniques, however, can be used to minimize this EMI problem, so air-gapped cores are popular in many applications.

The effects of inductor core saturation in a switcher can be disastrous to the switching elements as well as lowering efficiency and increasing noise. Figure 3.56 shows a normal inductor current waveform in a switching regulator as well as a superimposed waveform showing the effects of core saturation. Under normal conditions the slope is linear for both the charge and discharge cycle. If saturation occurs, however, the inductor current increases exponentially, corresponding to the drop in effective inductance. It is therefore important in all switching regulator designs to determine the peak inductor current expected under the worst case conditions of input voltage, load current, duty cycle, etc. This worst case peak current must be less than the peak-current rating of the inductor. Notice that when inductor literature does not have a "DC-current" rating, or shows only an "AC amps" rating, such inductors are often prone to saturation.

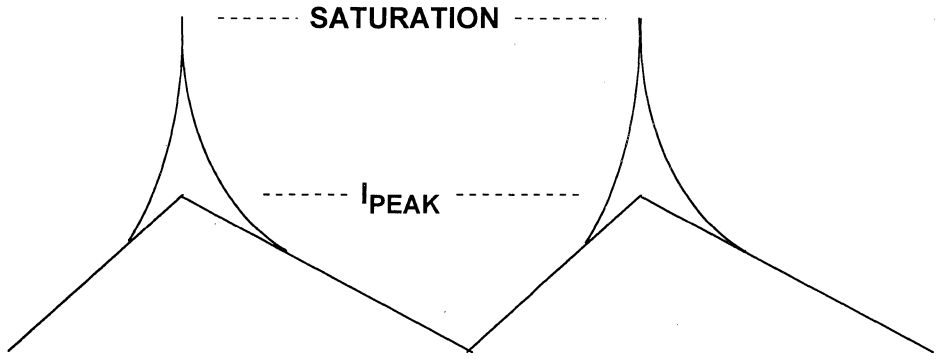


Figure 3.56

From a simplified design standpoint, the effects or presence of inductor saturation can best be observed with a scope and a current probe. If a current probe is not available, a less direct but still effective method is to measure the voltage across a small sense resistor in series with the inductor. The resistor value should be 1Ω or less (depending on the inductor current), and the resistor must be sized to dissipate the power. In most cases, a 1Ω, 1W resistor will work for currents up to a few hundred mA, and a 0.1Ω, 10W resistor is good for currents up to 10A.

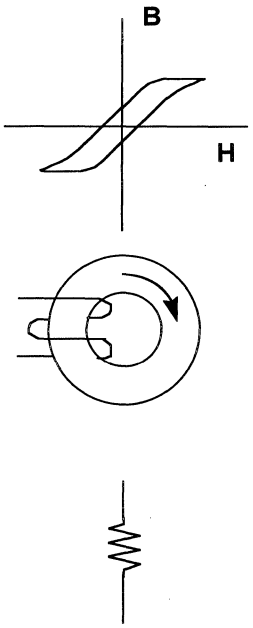
Another inductor consideration is its loss. Ideally, an inductor should dissipate no power. However, in a practical inductor, power is dissipated in the form of hysteresis loss, eddy-current loss, and winding loss. Figure 3.57 shows a typical B/H curve for an inductor. The enclosed area swept out by the B/H curve during one complete operating cycle is the hysteresis loss exhibited by the core during that cycle. Hysteresis loss is a function of core material, core volume, operating

frequency, and the maximum flux density during each cycle. The second major loss within the core is eddy-current loss. This loss is caused by the flow of circulating magnetic currents within the core material caused by rapid transitions in the magnetic flux density. It is also dependent on the core material, core volume, operating frequency, and flux density.

In addition to core loss, there is winding loss, the power dissipated in the DC resistance of the winding. This loss is a function of the wire size, core volume, and the number of turns.

In a switching regulator application, excessive loss will result in a loss of efficiency and high inductor operating temperatures.

INDUCTOR POWER LOSSES



LOSS	FUNCTION OF
■ Magnetic Hysteresis	◆ Core Material ◆ Core Volume ◆ Flux Density ◆ Frequency
■ Eddy Currents	◆ Core Material ◆ Core Volume ◆ Flux Density ◆ Frequency
■ Winding Resistance	◆ Wire Size ◆ Number of Turns ◆ Core Volume

■ Figure of Merit: "Q" = $\frac{2\pi fL}{R}$

Figure 3.57

Fortunately, inductor manufacturers have simplified the design process by specifying maximum peak current, maximum continuous current, and operating frequency range and temperature for their inductors. If the designer derates the maximum peak and continuous current levels by a factor of 20% or so, the inductor should be satisfactory for the application. If these simple guidelines are observed, then the designer can be reasonable confident that the major sources of efficiency losses will be due to other parts of the regulator, i.e., the switch (I^2R, gate charge, on-voltage), the diode (on-voltage), and the quiescent power dissipation of the regulator itself.

One method to ensure that the inductor losses do not significantly degrade the regulator performance is to measure the Q of the inductor at the switching frequency. If the Q is greater than about 25, then the losses should be insignificant.

There are many possible choices in inductor core materials: ferrite, molypermalloy (MPP) ferrite, powdered iron, etc. High efficiency converters generally cannot accommodate the core loss found in the low-cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy (MPP), or "Kool Mμ"® cores.

Ferrite core material saturates "hard", which causes the inductance to collapse abruptly when the peak current is exceeded. This results in a sharp increase in inductor ripple current.

Molypermalloy from Magnetics, Inc., is a very good, low loss core material for toroids, but is more expensive than ferrite. A reasonable compromise from the same manufacturer is "Kool Mμ".

The final consideration is the inductor self-resonant frequency. A practical example would be an inductor of 10μH which has an equivalent distributed capacitance of 5pF. The self-resonant frequency can be calculated as follows:

$$f_{resonance} = \frac{1}{2\pi}\sqrt{\frac{1}{LC}} = 22MHz.$$

The switching frequency of the regulator should be at least ten times less than the resonant frequency. In most practical designs with switching frequencies less than 1MHz this will always be the case, but a quick calculation is a good idea.

CAPACITOR CONSIDERATIONS

Capacitors play a critical role in switching regulators by acting as storage elements for the pulsating currents produced by the switching action. Although not shown on the diagrams previously, all switching regulators need capacitors on their inputs as well as their outputs for proper operation. The capacitors must have very low impedance at the switching frequency as well as the high frequencies produced by the pulsating current waveforms.

Recall the input and output current waveforms for the simple buck converter shown in Figure 3.58. Note that the input current to the buck converter is pulsating, while the output is continuous. Obviously, the input capacitor C_{IN} is critical for proper operation of the regulator. It must maintain the input at a constant voltage during the switching spikes. This says that the impedance of the capacitor must be very low at high frequencies, much above the regulator switching frequency. The load capacitor is also critical in that its impedance will determine the peak-to-peak output voltage ripple, but its impedance at high frequencies is not as critical due to the continuous nature of the output current waveform.

The situation is reversed in the case of the boost converter shown in Figure 3.59. Here the input waveform is continuous, while the output waveform is pulsating. The output capacitor must have good low and high frequency characteristics in order to minimize the output voltage ripple. Boost converters are often followed by a post filter to remove the high frequency switching noise.

BUCK CONVERTER
INPUT AND OUTPUT CURRENT WAVEFORMS

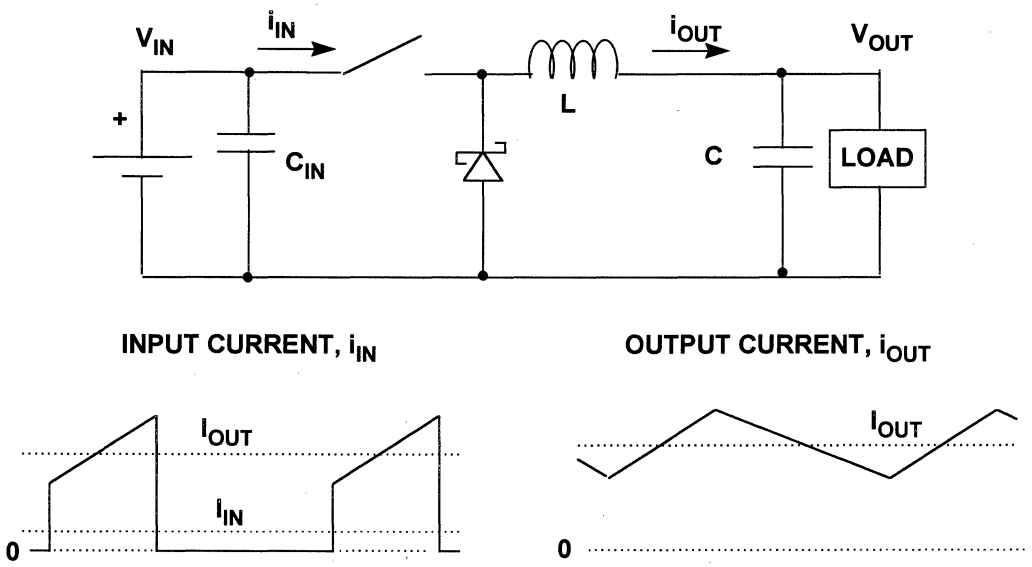


Figure 3.58

BOOST CONVERTER
INPUT AND OUTPUT CURRENT WAVEFORMS

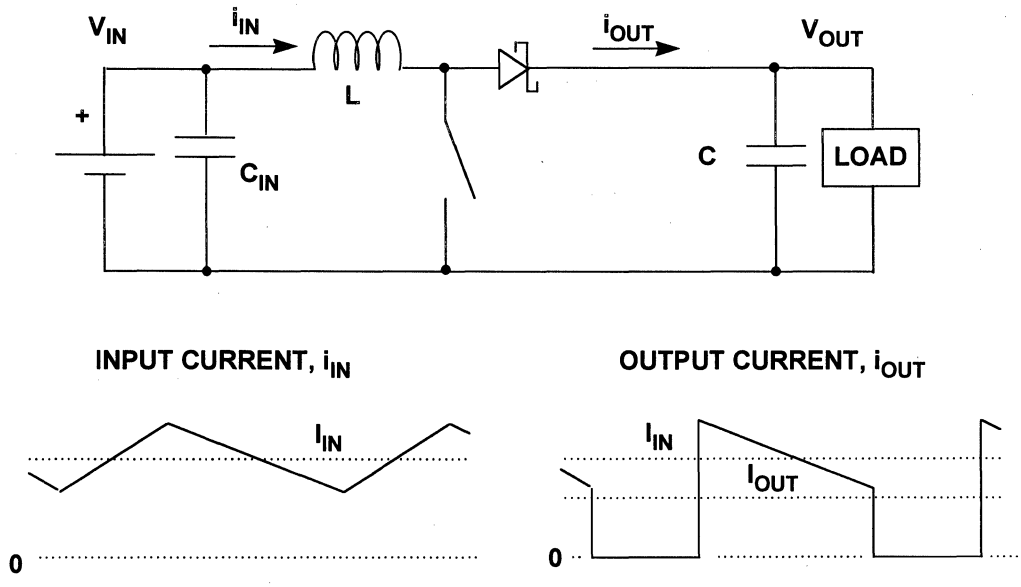


Figure 3.59

Switching regulator capacitors are generally of the electrolytic type because of the relatively large values required. An equivalent circuit for an electrolytic capacitor is shown in Figure 3.60. In addition to the capacitance value itself, the capacitor has some equivalent series resistance (ESR) and equivalent series inductance (ESL). It is useful to make a few assumptions and examine the approximate response of the capacitor to a fast current step input. For the sake of the discussion, assume the input current switches from 0 to 1A in 100ns. Also, assume that the ESR is 0.2Ω and that the ESL is 20nH. ESR and ESL vary widely between manufacturers and are also dependent upon body style (through-hole vs. surface mount), but these values will serve to illustrate the point.

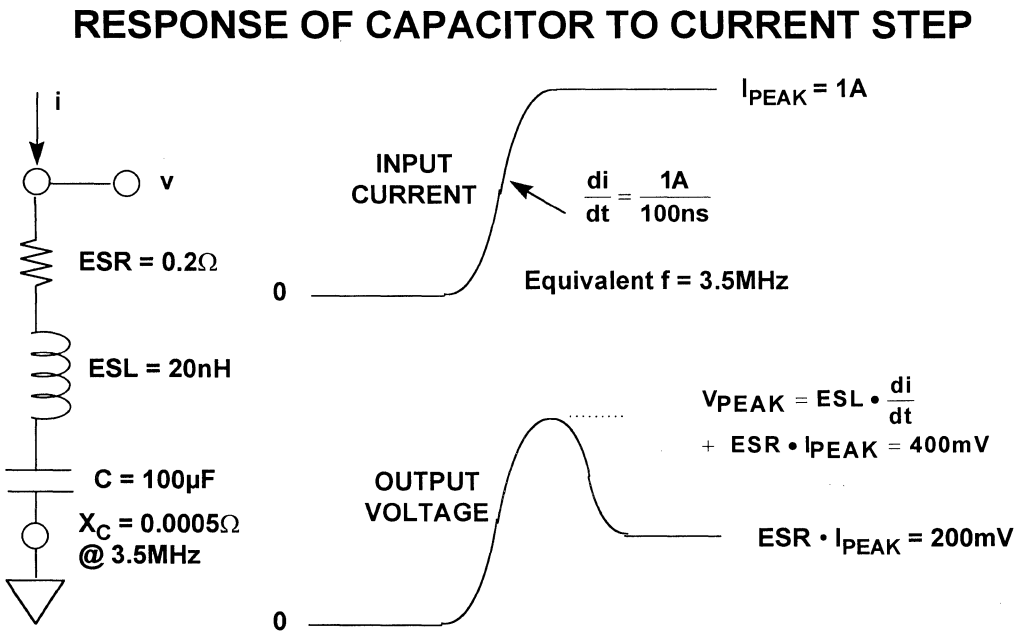


Figure 3.60

Assume that the actual value of the capacitor is large enough so that its reactance is essentially a short circuit with respect to the step function input. For example, 100µF at 3.5MHz (the equivalent frequency of a 100ns risetime pulse) has a reactance of $1/2\pi fC = 0.0005\Omega$. In this case, the output voltage ripple is determined exclusively by the ESR and ESL of the capacitor, not the actual capacitor value itself.

These waveforms show the inherent limitations of electrolytic capacitors used to absorb high frequency switching pulses. In a practical system, the high frequency components must be attenuated by low-inductance ceramic capacitors with low ESL or by the addition of an LC filter.

Figure 3.61 shows the impedance versus frequency for a typical 100µF electrolytic capacitor having an ESR of 0.2Ω and an ESL of 20nH. At frequencies below about 10kHz, the capacitor is nearly ideal. Between 10kHz and 1MHz (the range of switching frequencies for most IC switching regulators!) the impedance is limited by the ESR to 0.2Ω. Above about 1MHz the capacitor behaves like an inductor due to the ESL of 20nH. These values, although they may vary somewhat depending upon

the actual type of electrolytic capacitor (aluminum general purpose, aluminum switching type, tantalum, or organic semiconductor), are representative and illustrate the importance of understanding the limitations of capacitors in switching regulators.

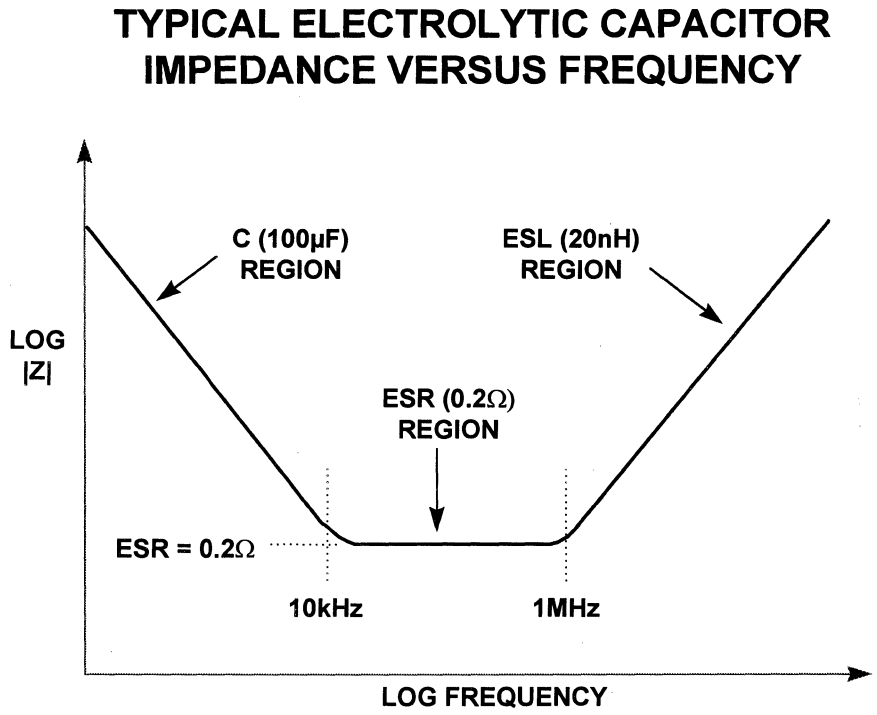


Figure 3.61

From the electrolytic capacitor impedance characteristic, it is clear that the ESR and ESL of the output capacitor will determine the peak-to-peak output voltage ripple caused by the switching regulator output ripple current.

In most electrolytic capacitors, ESR degrades noticeably at low temperature, by as much as a factor of 4-6 times at –55°C vs. the room temperature value. For circuits where ESR is critical to performance, this can lead to problems. Some specific electrolytic types do address this problem, for example within the HFQ switching types, the –10°C ESR at 100kHz is no more than 2× that at room temperature. The OS-CON electrolytics have a ESR vs. temperature characteristic which is relatively flat.

There are generally three classes of capacitors useful in 10kHz-100MHz frequency range, broadly distinguished as the generic dielectric types; *electrolytic*, *film*, and *ceramic*. These can in turn can be further sub-divided. A thumbnail sketch of capacitor characteristics is shown in the chart of Figure 3.62.

CAPACITOR SELECTION

	Aluminum Electrolytic (General Purpose)	Aluminum Electrolytic (Switching Type)	Tantalum Electrolytic	OS-CON Electrolytic	Polyester (Stacked Film)	Ceramic (Multilayer)
Size	100 µF	120 µF	120 µF	100 µF	1 µF	0.1 µF
Rated Voltage	25 V	25 V	20 V	20 V	400 V	50 V
ESR	0.6 Ω @ 100 kHz	0.18 Ω @ 100 kHz	0.12 Ω @ 100 kHz	0.02 Ω @ 100 kHz	0.11 Ω @ 1 MHz	0.12 Ω @ 1 MHz
Operating Frequency (*)	≅ 100 kHz	≅ 500 kHz	≅ 1 MHz	≅ 1 MHz	≅ 10 MHz	≅ 1 GHz

(*) Upper frequency strongly size and package dependent

Figure 3.62

The *electrolytic* family provides an excellent, cost-effective low-frequency component, because of the wide range of values, a high capacitance-to-volume ratio, and a broad range of working voltages. It includes *general purpose aluminum electrolytic* types, available in working voltages from below 10V up to about 500V, and in size from 1 to several thousand µF (with proportional case sizes). All electrolytic capacitors are polarized, and thus cannot withstand more than a volt or so of reverse bias without damage. They also have relatively high leakage currents (up to tens of µA, and strongly dependent upon design specifics).

A subset of the general electrolytic family includes *tantalum* types, generally limited to voltages of 100V or less, with capacitance of 500µF or less[Reference 8]. In a given size, tantalums exhibit a higher capacitance-to-volume ratio than do general purpose electrolytics, and have both a higher frequency range and lower ESR. They are generally more expensive than standard electrolytics, and must be carefully applied with respect to surge and ripple currents.

A subset of aluminum electrolytic capacitors is the *switching* type, designed for handling high pulse currents at frequencies up to several hundred kHz with low losses [Reference 9]. This capacitor type competes directly with tantalums in high frequency filtering applications, with the advantage of a broader range of values.

A more specialized high performance aluminum electrolytic capacitor type uses an organic semiconductor electrolyte [Reference 10]. The *OS-CON* capacitors feature appreciably lower ESR and higher frequency range than do other electrolytic types, with an additional feature of low low-temperature ESR degradation.

Film capacitors are available in very broad value ranges and different dielectrics, including polyester, polycarbonate, polypropylene, and polystyrene. Because of the low dielectric constant of these films, their volumetric efficiency is quite low, and a 10μF/50V polyester capacitor (for example) is actually a handful. Metalized (as opposed to foil) electrodes does help to reduce size, but even the highest dielectric constant units among film types (polyester, polycarbonate) are still larger than any electrolytic, even using the thinnest films with the lowest voltage ratings (50V). Where film types excel is in their low dielectric losses, a factor which may not necessarily be a practical advantage for filtering switchers. For example, ESR in film capacitors can be as low as 10mΩ or less, and the behavior of films generally is very high in terms of Q. In fact, this can cause problems of spurious resonance in filters, requiring damping components.

Typically using a wound layer-type construction, film capacitors can be inductive, which can limit their effectiveness for high frequency filtering. Obviously, only non-inductively made film caps are useful for switching regulator filters. One specific style which is non-inductive is the *stacked-film* type, where the capacitor plates are cut as small overlapping linear sheet sections from a much larger wound drum of dielectric/plate material. This technique offers the low inductance attractiveness of a plate sheet style capacitor with conventional leads [see References 9, 10, 11]. Obviously, minimal lead length should be used for best high frequency effectiveness. Very high current polycarbonate film types are also available, specifically designed for switching power supplies, with a variety of low inductance terminations to minimize ESL [Reference 12].

Dependent upon their electrical and physical size, film capacitors can be useful at frequencies to well above 10MHz. At the highest frequencies, only stacked film types should be considered. Some manufacturers are now supplying film types in leadless surface mount packages, which eliminates the lead length inductance.

Ceramic is often the capacitor material of choice above a few MHz, due to its compact size, low loss, and availability up to several μF in the high-K dielectric formulations (X7R and Z5U), at voltage ratings up to 200V [see ceramic families of Reference 8]. NP0 (also called COG) types use a lower dielectric constant formulation, and have nominally zero TC, plus a low voltage coefficient (unlike the less stable high-K types). NP0 types are limited to values of 0.1μF or less, with 0.01μF representing a more practical upper limit.

Multilayer ceramic "chip caps" are very popular for bypassing/ filtering at 10MHz or more, simply because their very low inductance design allows near optimum RF bypassing. For smaller values, ceramic chip caps have an operating frequency range to 1GHz. For high frequency applications, a useful selection can be ensured by selecting a value which has a self-resonant frequency *above* the highest frequency of interest.

The *ripple-current* rating of electrolytic capacitors must not be ignored in switching regulator applications because, unlike linear regulators, switching regulators subject capacitors to large AC currents. AC currents can cause heating in the dielectric material and change the temperature-dependent characteristics of the capacitor. Also, the capacitor is more likely to fail at the higher temperatures

produced by the ripple current. Fortunately, most manufacturers provide ripple-current ratings, and this problem can be averted if understood.

Calculating the exact ripple current can be tedious, especially with complex switching regulator waveforms. Simple approximations can be made, however, which are sufficiently accurate. Consider first the buck converter input and output currents (refer to Figure 3.63). The rms input capacitor ripple current can be approximated by a square wave having a peak-to-peak amplitude equal to I_{OUT}. The rms value of this square wave is therefore $I_{OUT}/2$. The output capacitor current waveform can be approximated by a sawtooth waveform having a peak-to-peak amplitude of $0.2I_{OUT}$. The rms value of this sawtooth is therefore approximately $0.2I_{OUT}/\sqrt{12}$, or $0.06I_{OUT}$.

BUCK CONVERTER INPUT AND OUTPUT CAPACITOR RMS RIPPLE CURRENT APPROXIMATIONS

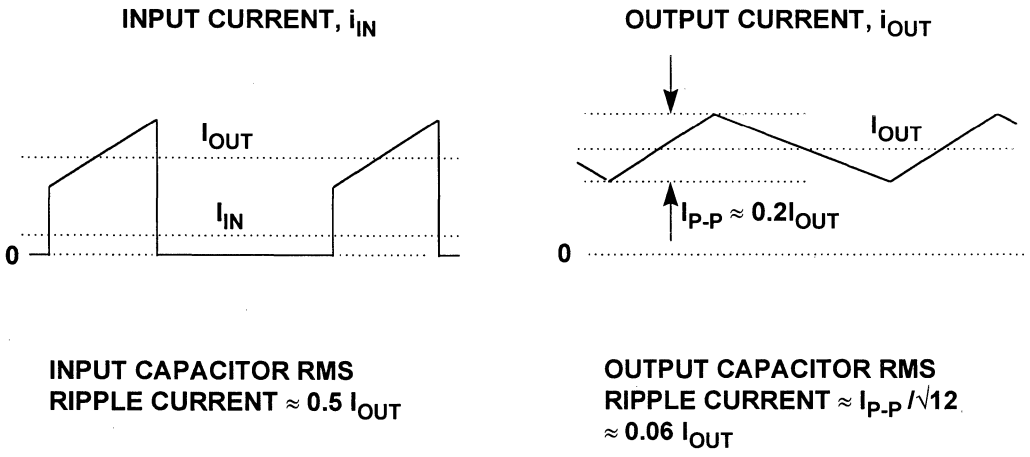


Figure 3.63

Similarly for a boost converter (see waveforms shown in Figure 3.64), the input capacitor rms ripple current is $0.06I_{IN}$, and the rms output current ripple is $0.5I_{IN}$. These boost converter expressions can also be expressed in terms of the output current, I_{OUT}, using the relationship, $I_{IN} = I_{OUT}(V_{OUT}/V_{IN})$. In any case, the minimum expected value of input voltage should be used which will result in the largest value of input current.

In practice, a safety factor of 25% should be added to the above approximations for further derating. In practical applications, especially those using surface mount components, it may be impossible to meet the capacitance value, ESR, and ripple current requirement using a single capacitor. Paralleling a number of equal value capacitors is a viable option which will increase the effective capacitance and reduce ESR, ESL. In addition, the ripple current is divided between the individual capacitors.

BOOST CONVERTER INPUT AND OUTPUT CAPACITOR RMS RIPPLE CURRENT APPROXIMATIONS

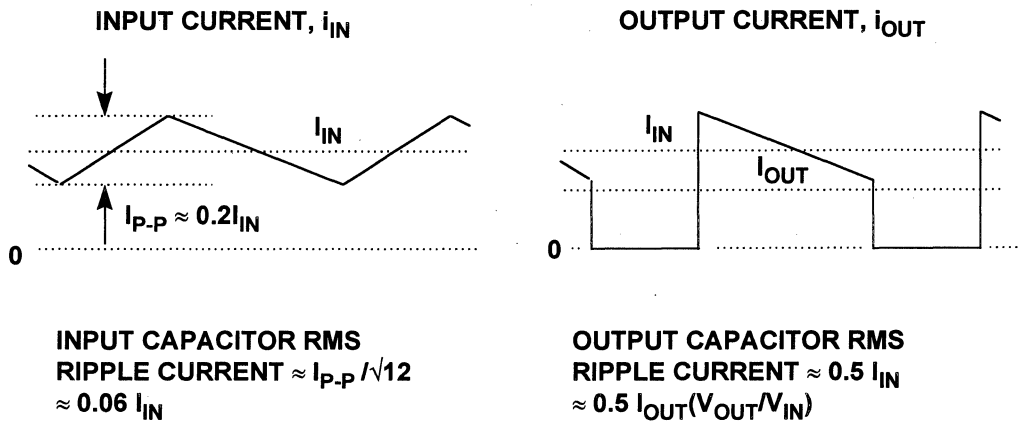


Figure 3.64

Several electrolytic capacitor manufacturers offer low ESR surface mount devices including the AVX TPS-series [Reference 14], and the Sprague 595D-series [Reference 15]. Low ESR through-hole electrolytic capacitors are the HFQ-series from Panasonic [Reference 16] and the OS-CON-series from Sanyo [Reference 17].

SWITCHING REGULATOR OUTPUT FILTERING

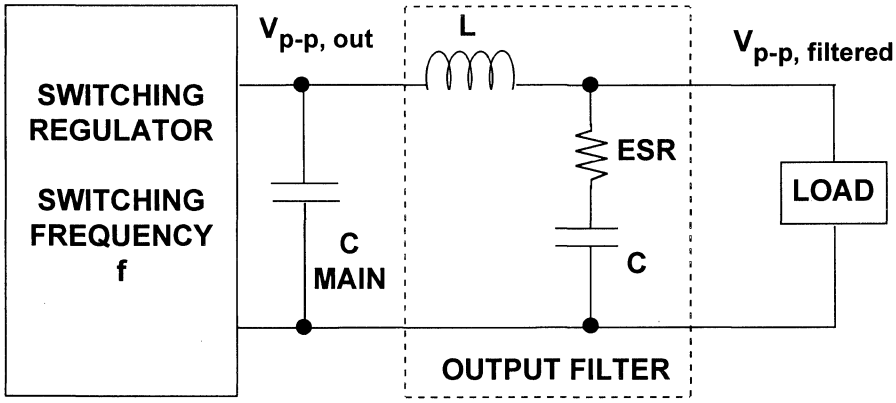
In order to minimize switching regulator output voltage ripple it is often necessary to add additional filtering. In many cases, this is more efficient than simply adding parallel capacitors to the main output capacitor to reduce ESR.

Output ripple current in a boost converter is pulsating, while that of a buck converter is a sawtooth. In any event, the high frequency components in the output ripple current can be removed with a small inductor (2 to 10μH or so followed by a low ESR capacitor). Figure 3.65 shows a simple LC filter on the output of a switching regulator whose switching frequency is f. Generally the actual value of the filter capacitor is not as important as its ESR when filtering the switching frequency ripple. For instance, the reactance of a 100μF capacitor at 100kHz is approximately 0.016Ω, which is much less than available ESRs.

The capacitor ESR and the inductor reactance attenuate the ripple voltage by a factor of approximately $2\pi fL/ESR$. The example shown in Figure 3.65 uses a 10µH inductor and a capacitor with an ESR of 0.2Ω. This combination attenuates the output ripple by a factor of about 32.

The inductor core material is not critical, but it should be rated to handle the load current. Also, its DC resistance should be low enough so that the load current does not cause a significant voltage drop across it.

SWITCHING REGULATOR OUTPUT FILTERING



$$\text{ATTENUATION} \approx \frac{2\pi fL}{ESR}$$

Example: ESR = 0.2Ω , L = 10µH , f = 100kHz

ATTENUATION = 32

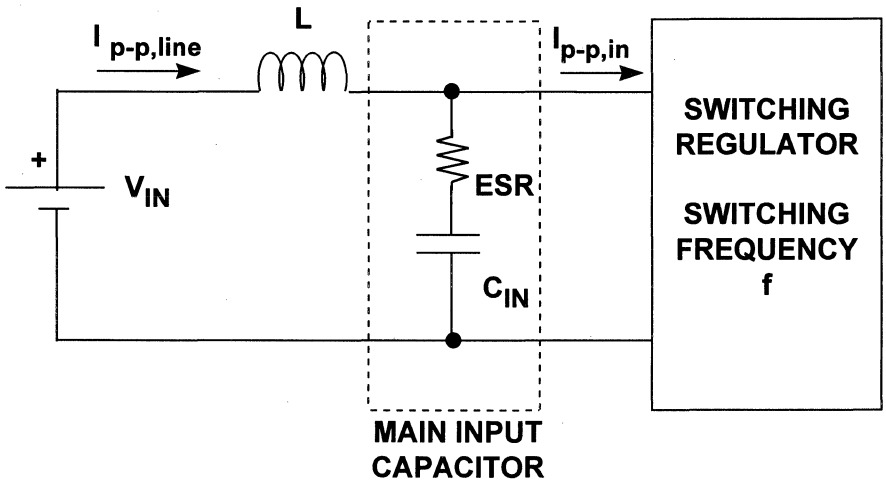
Figure 3.65

SWITCHING REGULATOR INPUT FILTERING

The input ripple current in a buck converter is pulsating, while that of a boost converter is a sawtooth. Additional filtering may be required to prevent the switching frequency and the other higher frequency components from affecting the main supply ripple current.

This is easily accomplished by the addition of a small inductor in series with the main input capacitor of the regulator as shown in Figure 3.66. The reactance of the inductor at the switching frequency forms a divider with the ESR of the input capacitor. The inductor will block both low and high frequency components from the main input voltage source. The attenuation of the ripple current at the switching frequency, f, is approximately $2\pi fL/ESR$.

SWITCHING REGULATOR INPUT FILTERING



$$\text{ATTENUATION} \approx \frac{2\pi fL}{ESR}$$

Figure 3.66

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17. Sanyo Corporation, 2001 Sanyo Ave., San Diego, CA 92173, 619-661-6835

18. Kemet Electronics, Box 5828, Greenville, SC 29606, 803-963-6300

Inductor Manufacturers:

19. Coiltronics, 6000 Park of Commerce Blvd., Boca Raton, FL 33487, 407-241-7876.

20. Sumida, 5999 New Wilke Rd. Suite 110, Rolling Meadow, IL. 60008, 847-956-0666.

21. Pulse Engineering, 12220 World Trade Drive, San Diego, CA 92128, 619-674-8100.

22. Gowanda Electronics, 1 Industrial Place, Gowanda, NY 14070, 716-532-2234.

23. Coilcraft, 1102 Silver Lake Rd., Cary, IL 60013, 847-639-2361.

24. Dale Electronics, Inc., E. Highway 50, P.O. Box 180, Yankton, SD 57078, 605-665-9301.

25. Hurricane Electronics Lab, 331 N. 2260 West, P.O. Box 1280, Hurricane, UT 84737, 801-635-2003.

Core Manufacturers:

26. Magnetics, P.O. Box 391, Butler, PA 16003, 412-282-8282.

MOSFET Manufacturers:

27. International Rectifier, 233 Kansas Street, El Segundo, CA 90245, 310-322-3331.

28. Motorola Semiconductor, 3102 North 56th Street, MS56-126, Phoenix, AZ 85018, 800-521-6274.

29. Siliconix Inc., 2201 Laurelwood Road, P.O. Box 54951, Santa Clara, CA 95056, 408-988-8000.

Schottky Diode Manufacturers:

30. General Instrument, Power Semiconductor Division, 10 Melville Park Road, Melville, NY 11747, 516-847-3000.

31. International Rectifier, 233 Kansas Street, El Segundo, CA 90245, 310-322-3331.

32. Motorola Semiconductor, 3102 North 56th Street, MS56-126, Phoenix, AZ 85018, 800-521-6274.

SECTION 4

SWITCHED CAPACITOR VOLTAGE CONVERTERS

- Charge Transfer Using Capacitors
- Unregulated Switched Capacitor Inverter and Doubler Implementations
- Voltage Inverter and Doubler Dynamic Operation
- Switched Capacitor Voltage Converter Power Losses
- Unregulated Inverter/Doubler Design Example
- Regulated Output Switched Capacitor Voltage Converters

SECTION 4
SWITCHED CAPACITOR VOLTAGE CONVERTERS

Walt Kester, Brian Erisman, Gurjit Thandi

INTRODUCTION

In the previous section, we saw how inductors can be used to transfer energy and perform voltage conversions. This section examines switched capacitor voltage converters which accomplish energy transfer and voltage conversion using capacitors.

The two most common switched capacitor voltage converters are the *voltage inverter* and the *voltage doubler* circuit shown in Figure 4.1. In the voltage inverter, the charge pump capacitor, C1, is charged to the input voltage during the first half of the switching cycle. During the second half of the switching cycle, its voltage is inverted and applied to capacitor C2 and the load. The output voltage is the negative of the input voltage, and the average input current is approximately equal to the output current. The switching frequency impacts the size of the external capacitors required, and higher switching frequencies allow the use of smaller capacitors. The duty cycle - defined as the ratio of charging time for C1 to the entire switching cycle time - is usually 50%, because that generally yields the optimal charge transfer efficiency.

After initial start-up transient conditions and when a steady-state condition is reached, the charge pump capacitor only has to supply a small amount of charge to the output capacitor on each switching cycle. The amount of charge transferred depends upon the load current and the switching frequency. During the time the pump capacitor is charged by the input voltage, the output capacitor C2 must supply the load current. The load current flowing out of C2 causes a droop in the output voltage which corresponds to a component of output voltage ripple. Higher switching frequencies allow smaller capacitors for the same amount of droop. There are, however, practical limitations on the switching speeds and switching losses, and switching frequencies are generally limited to a few hundred kHz.

The voltage doubler works similarly to the inverter; however, the pump capacitor is placed in series with the input voltage during its discharge cycle, thereby accomplishing the voltage doubling function. In the voltage doubler, the average input current is approximately twice the average output current.

The basic inverter and doubler circuits provide no output voltage regulation, however, techniques exist to add regulated capability and have been implemented in the ADP3603/3604/3605/3607.

BASIC SWITCHED CAPACITOR VOLTAGE INVERTER AND VOLTAGE DOUBLER

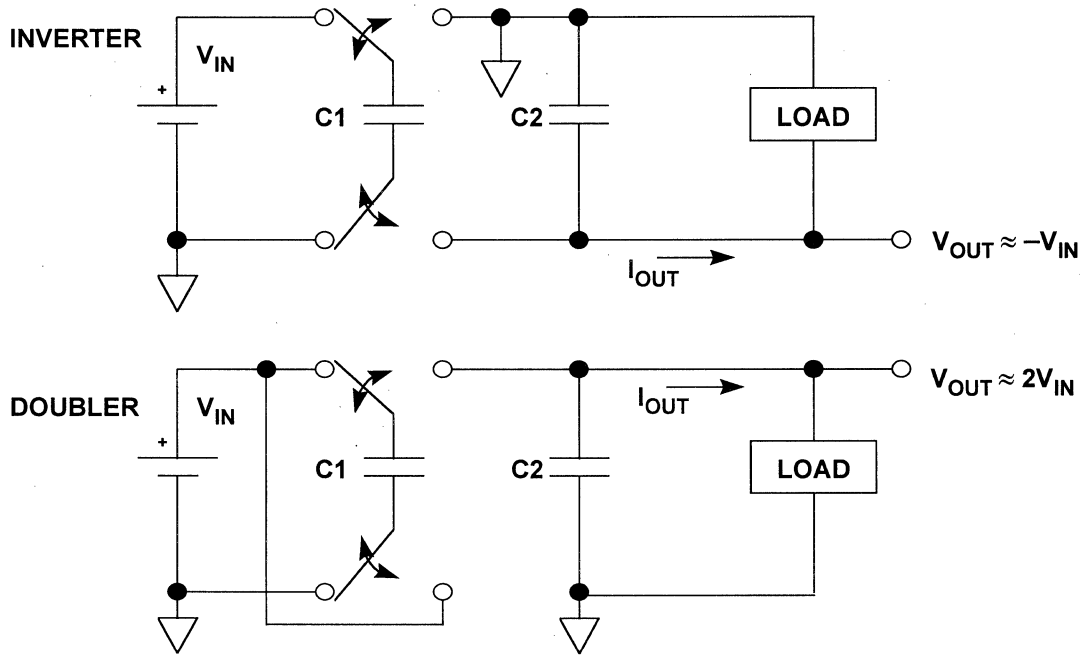


Figure 4.1

There are certain advantages and disadvantages of using switched capacitor techniques rather than inductor-based switching regulators. An obvious key advantage is the elimination of the inductor and the related magnetic design issues. In addition, these converters typically have relatively low noise and minimal radiated EMI. Application circuits are simple, and usually only two or three external capacitors are required. Because there is no need for an inductor, the final PCB component height can generally be made smaller than a comparable switching regulator. This is important in many applications such as display panels.

Switched capacitor inverters are low cost and compact and are capable of achieving efficiencies greater than 90%. Obviously, the current output is limited by the size of the capacitors and the current carrying capacity of the switches. Typical IC switched capacitor inverters have maximum output currents of about 150mA maximum.

Switched capacitor voltage converters do not maintain high efficiency for a wide range of ratios of input to output voltages, unlike their switching regulator counterparts. Because the input to output current ratio is scaled according to the basic voltage conversion (i.e., doubled for a doubler, inverted for an inverter) regardless of whether or not regulation is used to reduce the doubled or inverted voltage, any output voltage magnitude less than $2V_{IN}$ for a doubler or less than $|V_{IN}|$ for an inverter will result in additional power dissipation within the converter, and efficiency will be degraded proportionally.

SWITCHED CAPACITOR VOLTAGE CONVERTERS

- **No Inductors!**
- **Minimal Radiated EMI**
- **Simple Implementation: Only 2 External Capacitors (Plus an Input Capacitor if Required)**
- **Efficiency > 90% Achievable**
- **Optimized for Doubling or Inverting Supply Voltage - Efficiency Degrades for Other Output Voltages**
- **Low Cost, Compact, Low Profile (Height)**

- **Parts with Voltage Regulation are Available:**

  ADP3603/ADP3604/ADP3605/ADP3607

Figure 4.2

The voltage inverter is useful where a relatively low current negative voltage is required in addition to the primary positive voltage. This may occur in a single supply system where only a few high performance parts require the negative voltage. Similarly, voltage doublers are useful in low current applications where a voltage greater than the primary supply voltage is required.

CHARGE TRANSFER USING CAPACITORS

A fundamental understanding of capacitors (theoretical and real) is required in order to master the subtleties of switched capacitor voltage converters. Figure 4.3 shows the theoretical capacitor and its real-world counterpart. If the capacitor is charged to a voltage V, then the total charge stored in the capacitor, q, is given by $q = CV$. Real capacitors have equivalent series resistance (ESR) and inductance (ESL) as shown in the diagram, but these parasitics do not affect the ability of the capacitor to store charge. They can, however, have a large effect on the overall efficiency of the switched capacitor voltage converter.

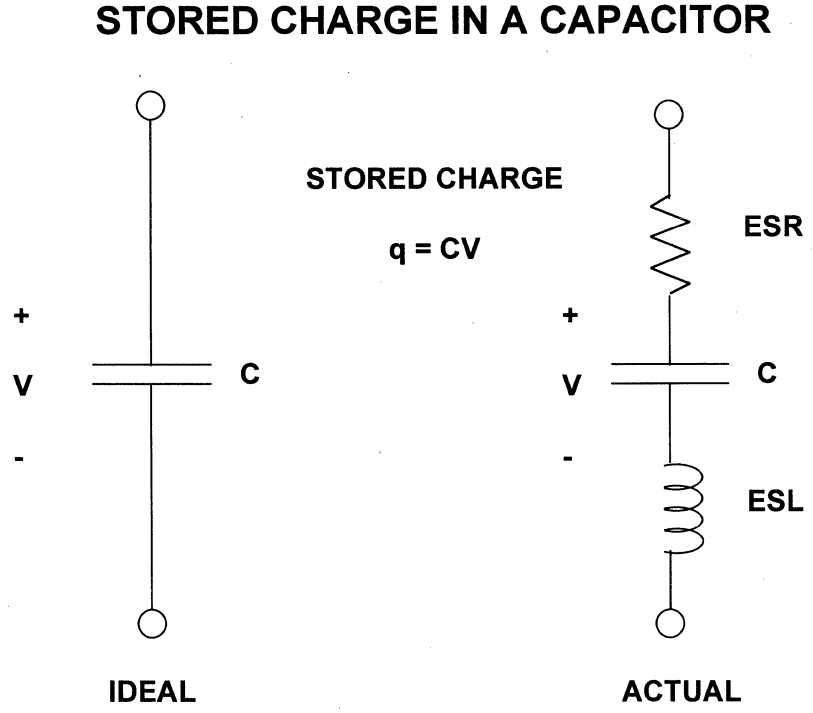


Figure 4.3

If an ideal capacitor is charged with an ideal voltage source as shown in Figure 4.4(A), the capacitor charge buildup occurs instantaneously, corresponding to a unit impulse of current. A practical circuit (Figure 4.4 (B)) will have resistance in the switch (R_{SW}) as well as the equivalent series resistance (ESR) of the capacitor. In addition, the capacitor has an equivalent series inductance (ESL). The charging current path also has an effective series inductance which can be minimized with proper component layout techniques. These parasitics serve to limit the peak current, and also increase the charge transfer time as shown in the diagram. Typical switch resistances can range from 1Ω to 50Ω, and ESRs between 50mΩ and 200mΩ. Typical capacitor values may range from about 0.1μF to 10μF, and typical ESL values 1 to 5nH. Although the equivalent RLC circuit of the capacitor can be underdamped or overdamped, the relatively large switch resistance generally makes the final output voltage response overdamped.

CHARGING A CAPACITOR FROM A VOLTAGE SOURCE

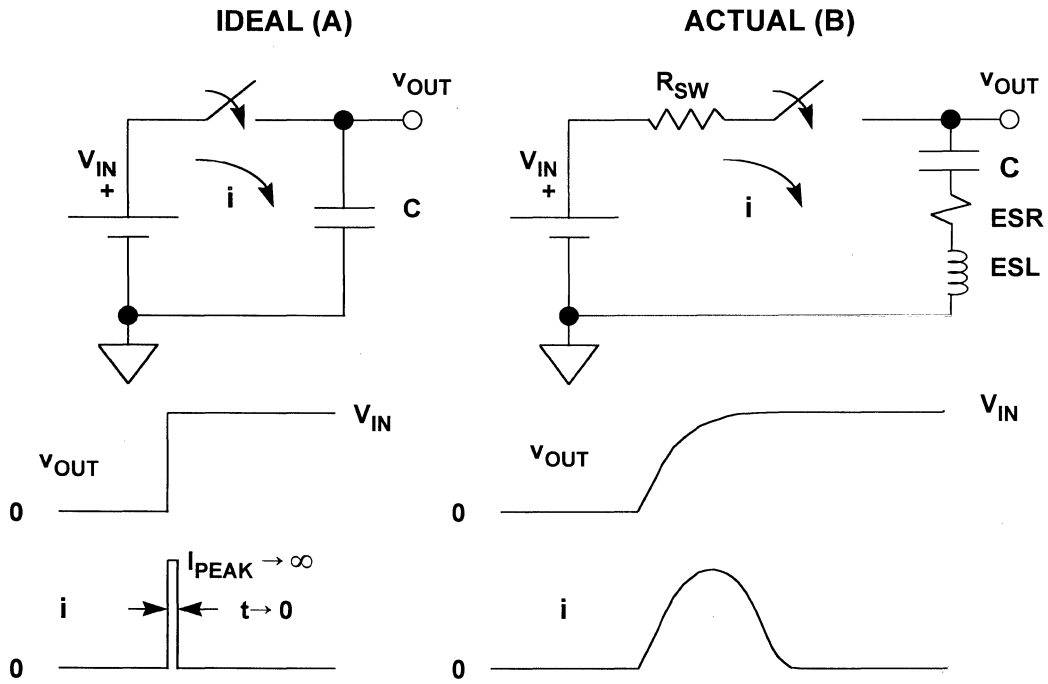


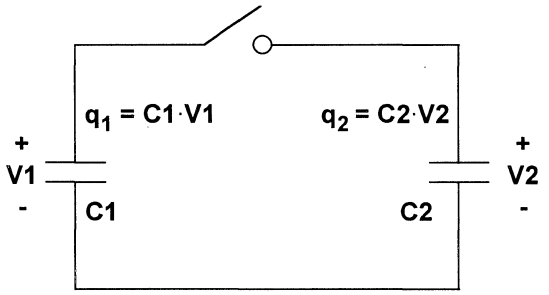
Figure 4.4

The law of conservation of charge states that if two capacitors are connected together, the total charge on the parallel combination is equal to the sum of the original charges on the capacitors. Figure 4.5 shows two capacitors, C1 and C2, each charged to voltages V1 and V2, respectively. When the switch is closed, an impulse of current flows, and the charge is redistributed. The total charge on the parallel combination of the two capacitors is $q_T = C1 \cdot V1 + C2 \cdot V2$. This charge is distributed between the two capacitors, so the new voltage, V_T, across the parallel combination is equal to qT/(C1 + C2), or

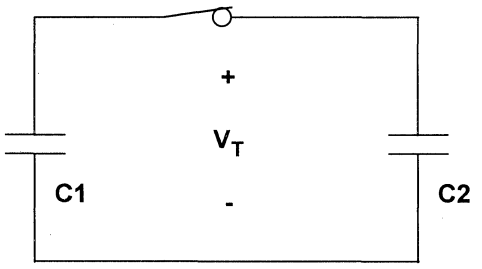
$$V_T = \frac{qT}{C1 + C2} = \frac{C1 \cdot V1 + C2 \cdot V2}{C1 + C2} = \left(\frac{C1}{C1 + C2}\right) V1 + \left(\frac{C2}{C1 + C2}\right) V2 .$$

This principle may be used in the simple charge pump circuit shown in Figure 4.6. Note that this circuit is neither a doubler nor inverter, but only a voltage replicator. The pump capacitor is C1, and the initial charge on C2 is zero. The pump capacitor is initially charged to V_{IN}. When it is connected to C2, the charge is redistributed, and the output voltage is $V_{IN}/2$ (assuming C1 = C2). On the second transfer cycle, the output voltage is pumped to $V_{IN}/2 + V_{IN}/4$. On the third transfer cycle, the output voltage is pumped to $V_{IN}/2 + V_{IN}/4 + V_{IN}/8$. The waveform shows how the output voltage exponentially approaches V_{IN}.

CHARGE REDISTRIBUTION BETWEEN CAPACITORS



CONSERVATION OF CHARGE:



$$q_T = C1 \cdot V1 + C2 \cdot V2$$

$$V_T = \frac{q_T}{C1 + C2}$$

$$V_T = \frac{C1}{C1 + C2} \cdot V1 + \frac{C2}{C1 + C2} \cdot V2$$

Figure 4.5

CONTINUOUS SWITCHING

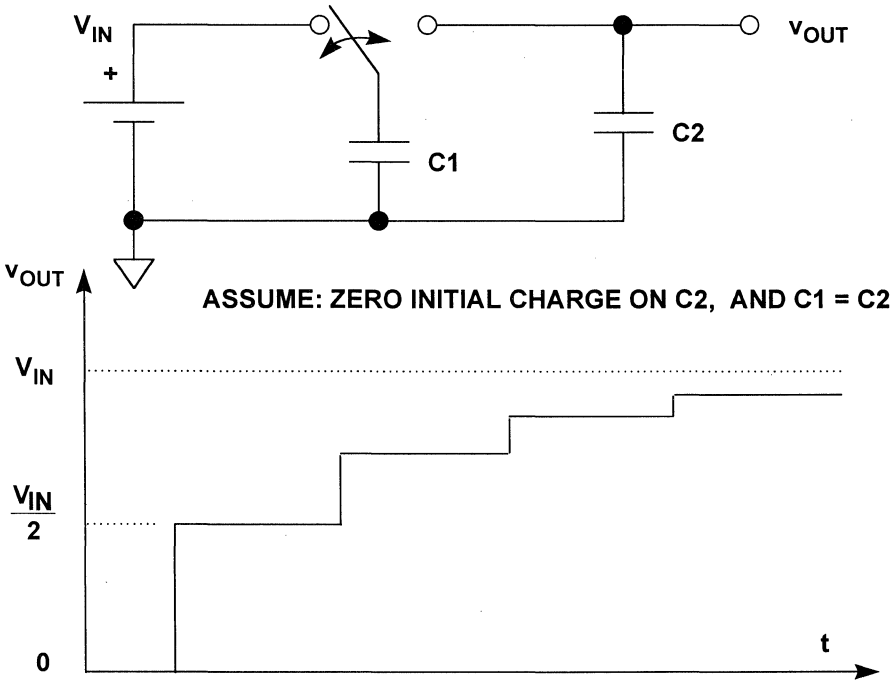


Figure 4.6

Figure 4.7 shows a pump capacitor, C1, switched continuously between the source, V1, and C2 in parallel with the load. The conditions shown are after a steady state condition has been reached. The charge transferred each cycle is $\Delta q = C1(V1 - V2)$. This charge is transferred at the switching frequency, f. This corresponds to an average current (current = charge transferred per unit time) of

$$I = f\,\Delta q = f \cdot C1(V1 - V2), \text{ or}$$

$$I = \frac{V1 - V2}{1/f \cdot C1}.$$

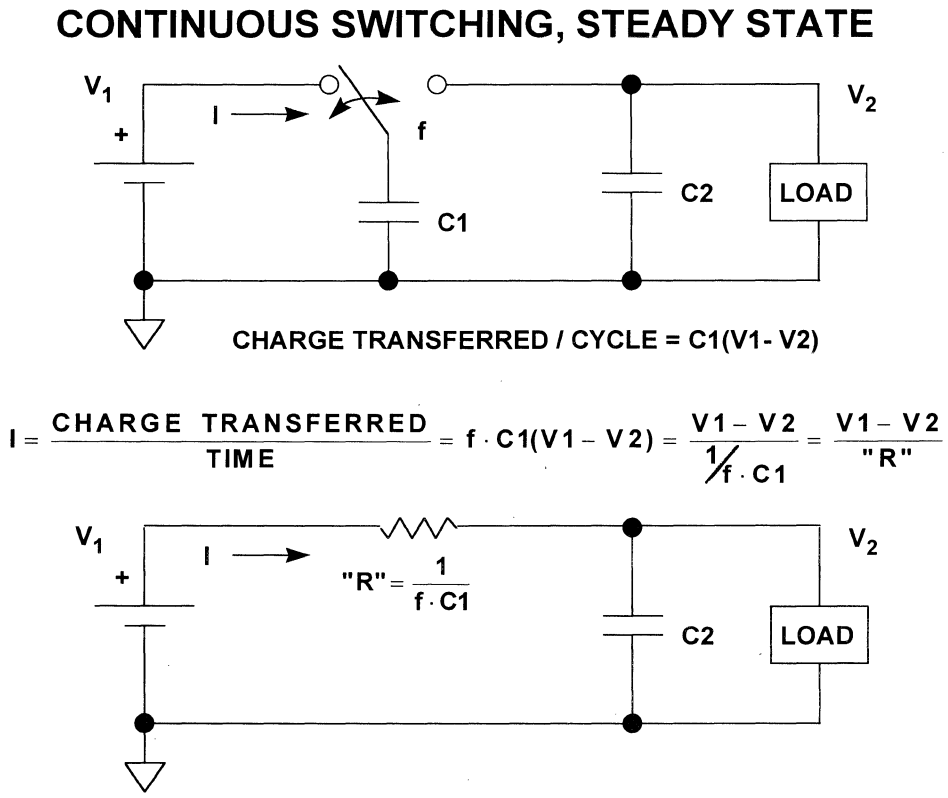


Figure 4.7

Notice that the quantity, 1/f·C1, can be considered an equivalent resistance, "R", connected between the source and the load. The power dissipation associated with this virtual resistance, "R", is essentially forced to be dissipated in the switch on resistance and the capacitor ESR, regardless of how low those values are reduced. (It should be noted that capacitor ESR and the switch on-resistance cause additional power losses as will be discussed shortly.)

In a typical switched capacitor voltage inverter, a capacitance of 10μF switched at 100kHz corresponds to "R" = 1Ω. Obviously, minimizing "R" by increasing the frequency minimizes power loss in the circuit. However, increasing switching frequency tends to increase switching losses. The optimum switched capacitor operating frequency is therefore highly process and device dependent. Therefore, specific recommendations are given in the data sheet for each device.

UNREGULATED SWITCHED CAPACITOR INVERTER AND DOUBLER IMPLEMENTATIONS

An unregulated switched capacitor inverter implementation is shown in Figure 4.8. Notice that the SPDT switches (shown in previous diagrams) actually comprise two SPST switches. The control circuit consists of an oscillator and the switch drive signal generators. Most IC switched capacitor inverters and doublers contain all the control circuits as well as the switches and the oscillator. The pump capacitor, C1, and the load capacitor, C2, are external. Not shown in the diagram is a capacitor on the input which is generally required to ensure low source impedance at the frequencies contained in the switching transients.

The switches used in IC switched capacitor voltage converters may be CMOS or bipolar as shown in Figure 4.9. Standard CMOS processes allow low on-resistance MOSFET switches to be fabricated along with the oscillator and other necessary control circuits. Bipolar processes can also be used, but add cost and increase power dissipation.

SWITCHED CAPACITOR VOLTAGE INVERTER IMPLEMENTATION

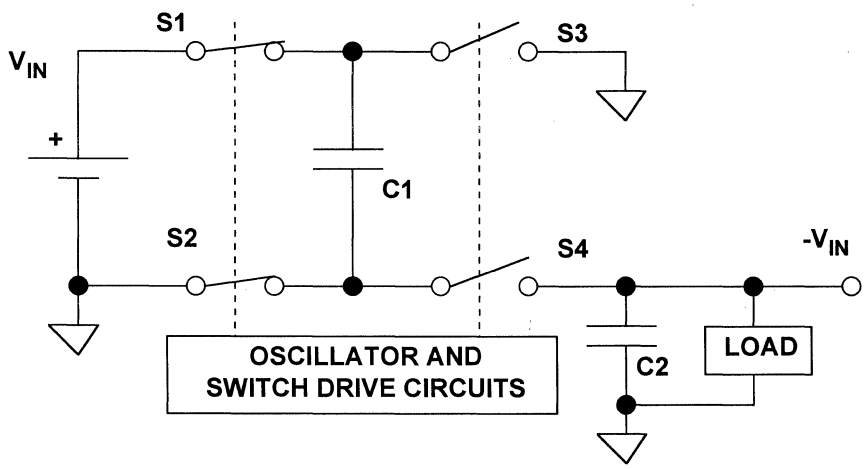


Figure 4.8

SWITCHES USED IN VOLTAGE CONVERTERS

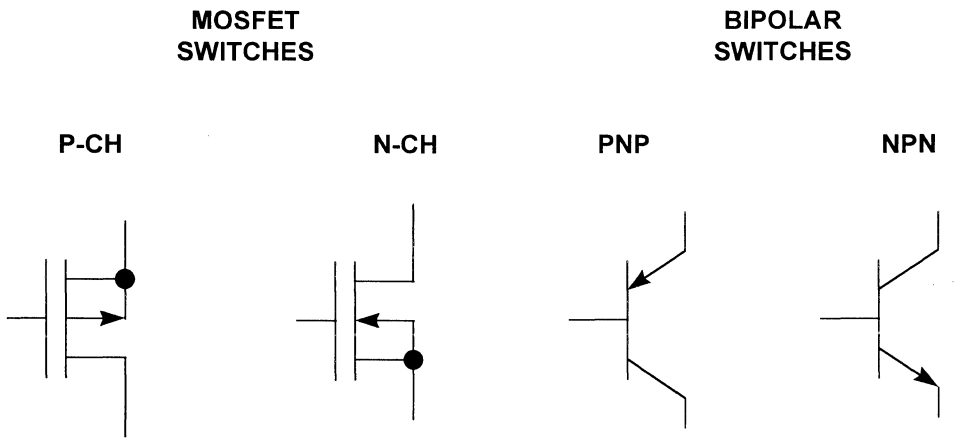


Figure 4.9

VOLTAGE INVERTER AND DOUBLER DYNAMIC OPERATION

The steady-state current and voltage waveforms for a switched capacitor voltage inverter are shown in Figure 4.10. The average value of the input current waveform (A) must be equal to I_{OUT}. When the pump capacitor is connected to the input, a charging current flows. The initial value of this charging current depends on the initial voltage across C1, the ESR of C1, and the resistance of the switches. The switching frequency, switch resistance, and the capacitor ESRs generally limit the peak amplitude of the charging current to less than $2.5I_{OUT}$. The charging current then decays exponentially as C1 is charged. The waveforms in Figure 4.10 assume that the time constant due to capacitor C1, the switch resistance, and the ESR of C1 is several times greater than the switching period (1/f). Smaller time constants will cause the peak currents to increase as well as increase the slopes of the charge/discharge waveforms. Long time constants cause longer start-up times and require larger and more costly capacitors. For the conditions shown in Figure 4.10 (A), the peak value of the input current is only slightly greater than $2I_{OUT}$.

The output current waveform of C1 is shown in Figure 4.10 (B). When C1 is connected to the output capacitor, the step change in the output capacitor current is approximately $2I_{OUT}$. This current step therefore creates an output voltage step equal to $2I_{OUT} \times ESR_{C2}$ as shown in Figure 4.10(C). After the step change, C2 charges linearly by an amount equal to $I_{OUT}/2f \cdot C2$. When C1 is connected back to the input, the ripple waveform reverses direction as shown in the diagram. The total peak-to-peak output ripple voltage is therefore:

$$V_{RIPPLE} \approx 2I_{OUT} \cdot ESR_{C2} + \frac{I_{OUT}}{2f \cdot C2}.$$

VOLTAGE INVERTER WAVEFORMS

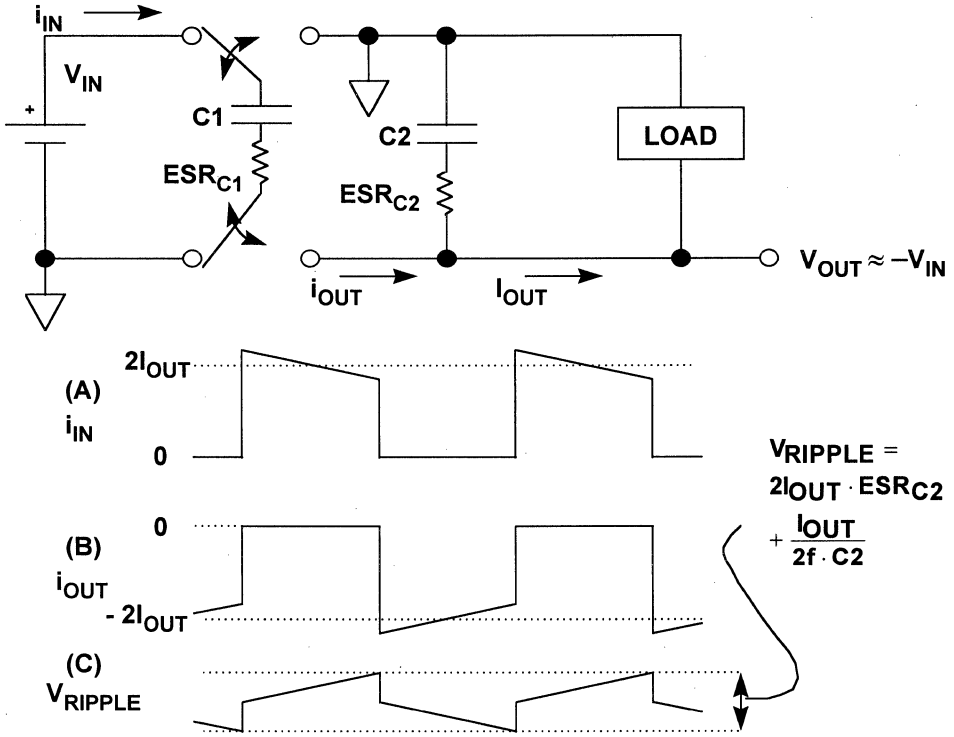


Figure 4.10

VOLTAGE DOUBLER WAVEFORMS

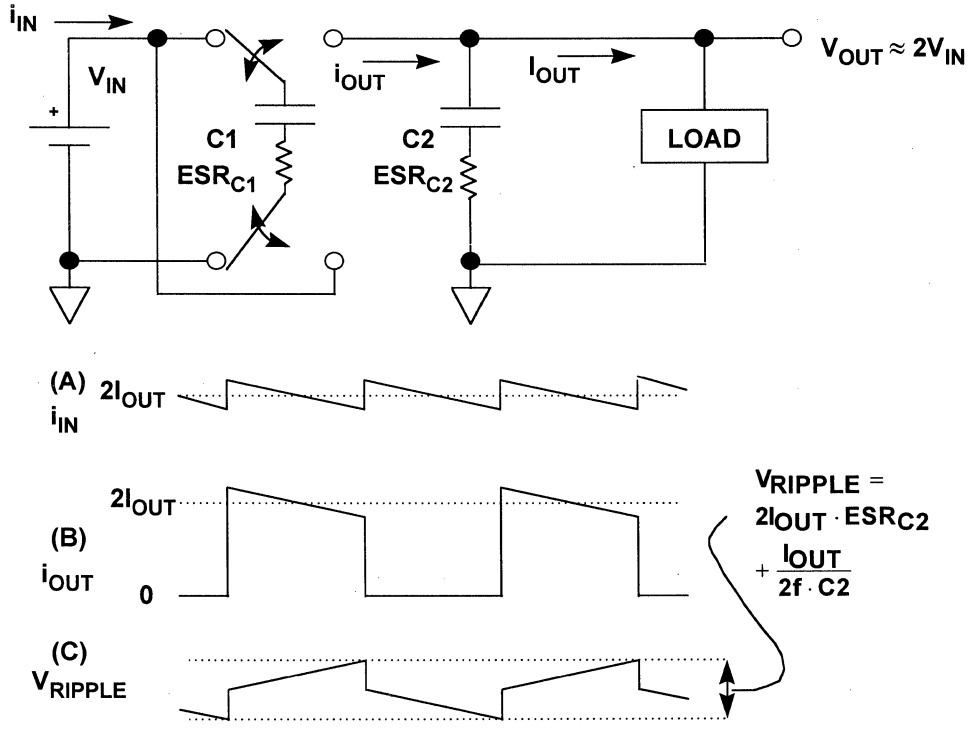


Figure 4.11

The current and voltage waveforms for a simple voltage doubler are shown in Figure 4.11 and are similar to those of the inverter. Typical voltage ripple for practical switched capacitor voltage inverter/doublers range from 25mV to 100mV, but can be reduced by filtering techniques as described in Section 8 of this book.

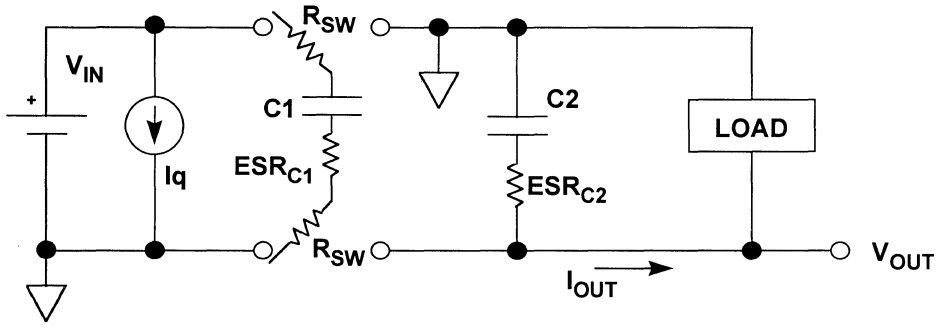
Note that the input current waveform has an average value of $2I_{OUT}$ because V_{IN} is connected to C1 during C1's charge cycle and to the load during C1's discharge cycle. The expression for the ripple voltage is identical to that of the voltage inverter.

SWITCHED CAPACITOR VOLTAGE CONVERTER POWER LOSSES

The various sources of power loss in a switched capacitor voltage inverter are shown in Figure 4.12. In addition to the inherent switched capacitor resistance, "R" = 1/f·C1, there are resistances associated with each switch, as well as the ESRs of the capacitors. The quiescent power dissipation, $I_q \cdot V_{IN}$, must also be included, where I_q is the quiescent current drawn by the IC itself.

4

VOLTAGE INVERTER POWER LOSSES



$$P_{LOSS} = I_{OUT}(V_{IN} - |V_{OUT}|) + I_q V_{IN}$$
$$= I_{OUT}^2 \cdot R_{OUT} + I_q V_{IN}$$

$$R_{OUT} \approx 8R_{SW} + 4ESR_{C1} + \frac{1}{f \cdot C1} + ESR_{C2}$$

Figure 4.12

The power dissipated in the switching arm is first calculated. When C1 is connected to V_{IN}, a current of $2I_{OUT}$ flows through the switch resistances ($2R_{SW}$) and the ESR of C1, ESR_{C1}. When C1 is connected to the output, a current of $2I_{OUT}$ continues to flow through C1, $2R_{SW}$, and ESR_{C1}. Therefore, there is always an rms current of $2I_{OUT}$ flowing through these resistances, resulting in a power dissipation in the switching arm of:

$$P_{SW} = (2I_{OUT})^2 \times (2R_{SW} + ESR_{C1}) = I_{OUT}^2 \times (8R_{SW} + 4ESR_{C1}).$$

In addition to these purely resistive losses, an rms current of I_{OUT} flows through the "resistance" of the switched capacitor, C1, yielding an additional loss of:

$$"P_{C1}" = I_{OUT}^2 \times "R_{C1}" = I_{OUT}^2 \times \frac{1}{f \cdot C1}.$$

The rms current flowing through ESR_{C2} is I_{OUT}, yielding a power dissipation of:

$$P_{ESR_{C2}} = I_{OUT}^2 \times ESR_{C2}.$$

Adding all the resistive power dissipations to the quiescent power dissipation yields:

$$P_{LOSS} = I_{OUT}^2 \times \left(8R_{SW} + 4ESR_{C1} + ESR_{C2} + \frac{1}{f \cdot C1}\right) + IqV_{IN}.$$

All of the resistive losses can be grouped into an equivalent R_{OUT} as shown in the diagram.

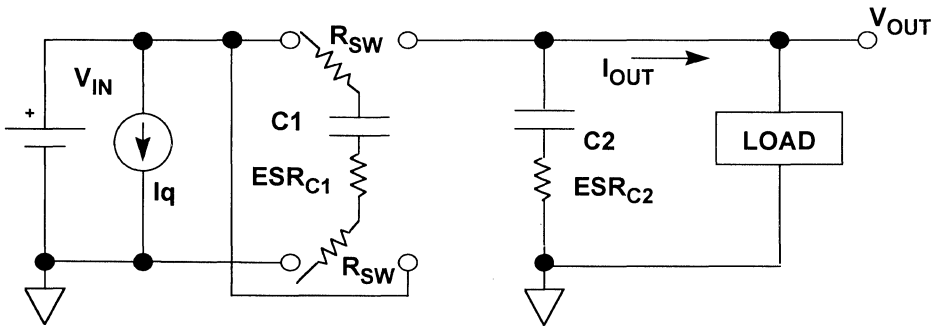
$$R_{OUT} \approx 8R_{SW} + 4ESR_{C1} + 1/f \cdot C1 + ESR_{C2}.$$

Typical values for switch resistances are between 1 - 20Ω, and ESRs between 50 and 200mΩ. The values of C1 and f are generally chosen such that the term, $1/f \cdot C1$, is less than 1Ω. For instance, 10μF @ 100kHz yields "R" = 1Ω. The dominant sources of power loss in most inverters are therefore the switch resistances and the ESRs of the pump capacitor and output capacitor.

The ADP3603/3604/3605/3607 series regulators have a shutdown control pin which can be asserted when load current is not required. When activated, the shutdown feature reduces quiescent current to a few tens of microamperes.

Power losses in a voltage doubler circuit are shown in Figure 4.13, and the analysis is similar to that of the inverter.

VOLTAGE DOUBLER POWER LOSSES



$$P_{LOSS} = I_{OUT}(2V_{IN} - V_{OUT}) + I_q V_{IN}$$
$$= I_{OUT}^2 \cdot R_{OUT} + I_q V_{IN}$$

$$R_{OUT} \approx 8R_{SW} + 4ESR_{C1} + \frac{1}{f \cdot C1} + ESR_{C2}$$

Figure 4.13

4

UNREGULATED INVERTER/DOUBLER DESIGN EXAMPLE

The ADM660 is a popular switched capacitor voltage inverter/doubler IC (see Figure 4.14). Switching frequency is selectable (25kHz/120kHz) using the FC input. When the FC input is open, the switching frequency is 25kHz. When it is connected to V+, the frequency increases to 120kHz. Only two external electrolytic capacitors (ESR should be less than 200mΩ) are required for operation (see Figure 4.14). The choice of the value of these capacitors is somewhat flexible. For a 25kHz switching frequency 10µF is recommended, and for 120kHz operation 2.2µF provides comparable performance.

If frequencies less than the selected output frequency are desired, an external capacitor can be placed between the OSC input and ground. The internal oscillator can also be overridden by driving the OSC input with an external logic signal, in which case the internal charge pump frequency is one-half the external clock frequency.

The ADM8660 is similar to the ADM660, however it is optimized for inverter operation and includes a "shutdown" feature which reduces the quiescent current to 5µA. Shutdown recovery time is 500µs. Key specifications for the ADM660/ADM8660 series are given in Figure 4.15.

Efficiency for the ADM660/ADM8660 is greater than 90% for output currents up to 50mA and greater than 80% for output currents to 100mA (see Figure 4.16).

ADM660 SWITCHED CAPACITOR VOLTAGE CONVERTER

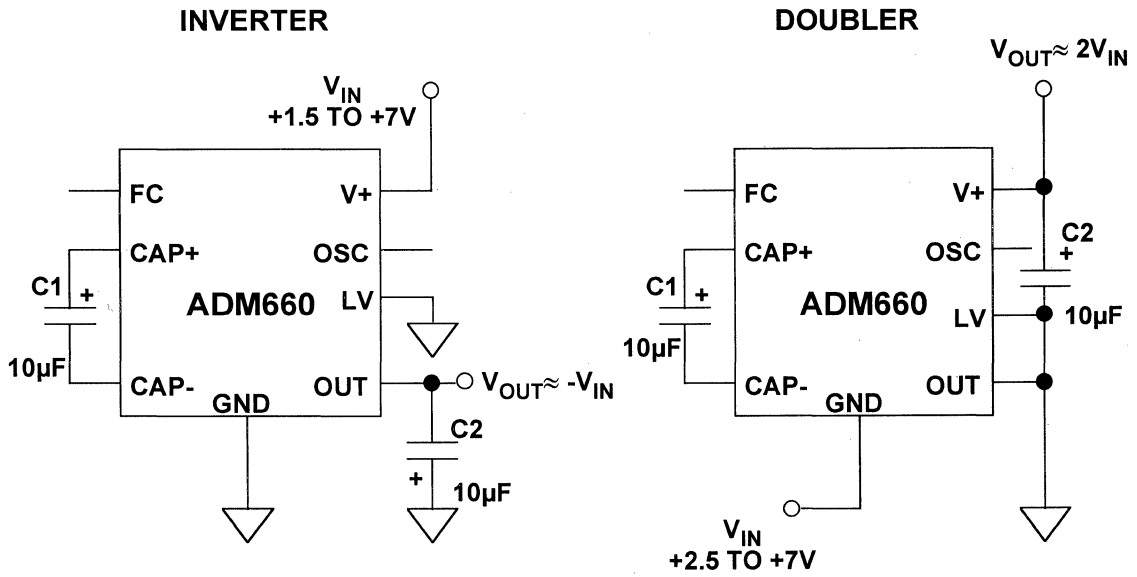


Figure 4.14

ADM660 / ADM8660 KEY SPECIFICATIONS

- ADM660: Inverts or Doubles Input Supply Voltage
- ADM8660: Inverts Input Supply Voltage
- Input Range Inverting: +1.5V to +7V
- Input Range Doubling: +2.5 to +7V (ADM660)
- 100mA Output Current
- Selectable Switching Frequency: 120kHz or 25kHz
- 2.2µF or 10µF External Capacitors (120kHz / 25kHz)
- 600µA Quiescent Current
- Shutdown Function (ADM8660), 5µA Shutdown Current
- 500µs Shutdown Recovery Time
- 8-Pin SOIC

Figure 4.15

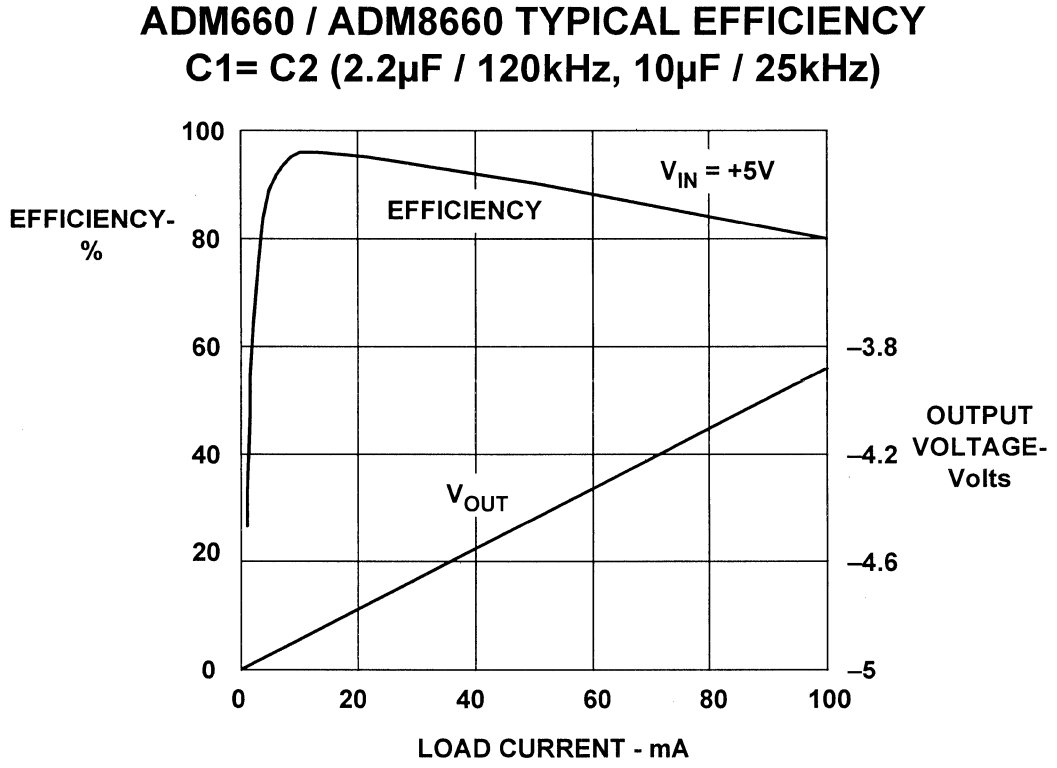


Figure 4.16

REGULATED OUTPUT SWITCHED CAPACITOR VOLTAGE CONVERTERS

Adding regulation to the simple switched capacitor voltage converter greatly enhances its usefulness in many applications. There are three general techniques for adding regulation to a switched capacitor converter. The most straightforward is to follow the switched capacitor inverter/doubler with a low dropout (LDO) linear regulator. The LDO provides the regulated output and also reduces the ripple of the switched capacitor converter. This approach, however, adds complexity and reduces the available output voltage by the dropout voltage of the LDO.

Another approach to regulation is to vary the duty cycle of the switch control signal with the output of an error amplifier which compares the output voltage with a reference. This technique is similar to that used in inductor-based switching regulators and requires the addition of a PWM and appropriate control circuitry. However, this approach is highly nonlinear and requires long time constants (i.e., lossy components) in order to maintain good regulation control.

By far the simplest and most effective method for achieving regulation in a switched capacitor voltage converter is to use an error amplifier to control the on-resistance of one of the switches as shown in Figure 4.17, a block diagram of the ADP3603/3604/3605 voltage inverters. These devices offer a regulated –3V output for an input voltage of +4.5V to +6V. The output is sensed and fed back into the device via the V_{SENSE} pin. Output regulation is accomplished by varying the on-resistance of one of the MOSFET switches as shown by control signal labeled "R_{ON} CONTROL" in the diagram. This signal accomplishes the switching of the MOSFET as well as controlling the on-resistance.

Key features of the ADP3603/3604/3605 series are shown in Figure 4.18. Note that the output regulation of the ADP3605 is ±2%, and the switching frequency is 250kHz. All three devices have a shutdown feature and a turn-on, turn-off time of about 5ms.

A typical application circuit for the ADP3603/3604/3605 series is shown in Figure 4.19. In the normal mode of operation, the SHUTDOWN pin should be connected to ground. The 10µF capacitors should have ESRs of less than 150mΩ, and values of 4.7µF can be used at the expense of slightly higher output ripple voltage. The equations for ripple voltage shown in Figure 4.10 also apply to the ADP3603/3604/3605. Using the values shown, typical ripple voltage ranges from 25mV to 60mV as the output current varies over its allowable range.

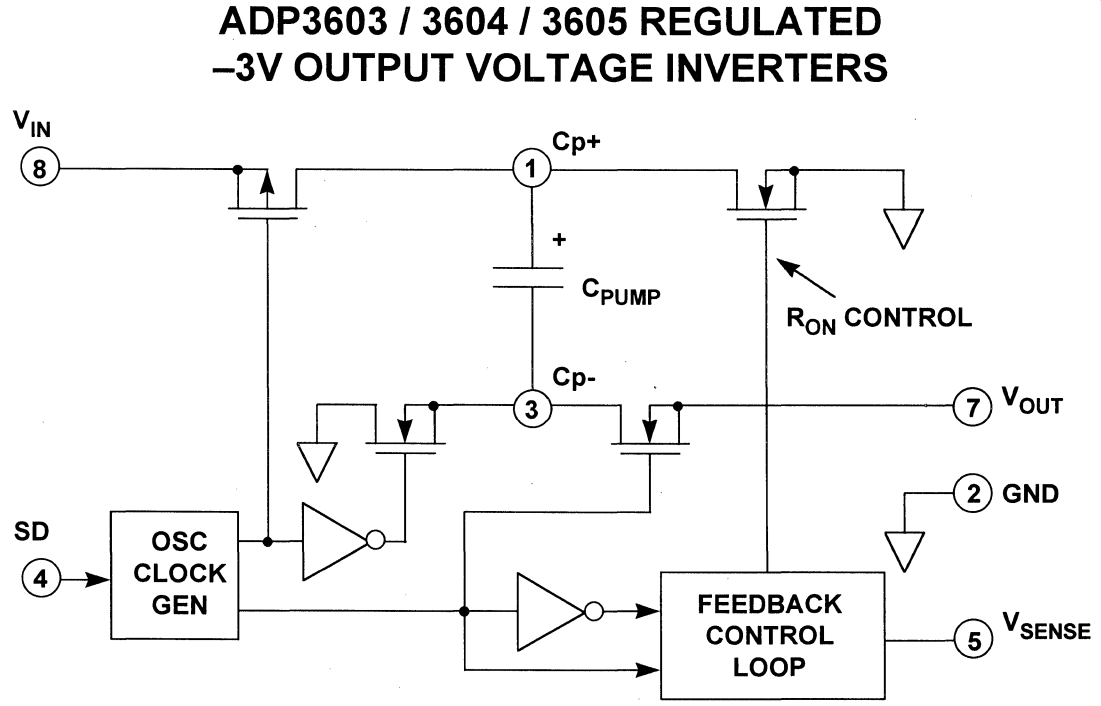


Figure 4.17

ADP3603 / ADP3604 / ADP3605 REGULATED INVERTERS - KEY SPECIFICATIONS

	ADP3603 / 3604	ADP3605
Output Accuracy	±3%	±2%
Switching Frequency	120kHz	250kHz
Turn-On, Turn-Off Time	5ms	5ms
Shutdown Current	1.4mA	10µA
Output Current	50mA / 120mA	120mA
Quiescent Current	2.4mA	2mA
Input Voltage	4.5V to 6V	4.5V to 6V
Nominal Output	–3V	–3V
Package	SO-8	SO-8

Figure 4.18

ADP3603 / 3604 / 3605 APPLICATION CIRCUIT FOR –3V OUTPUT

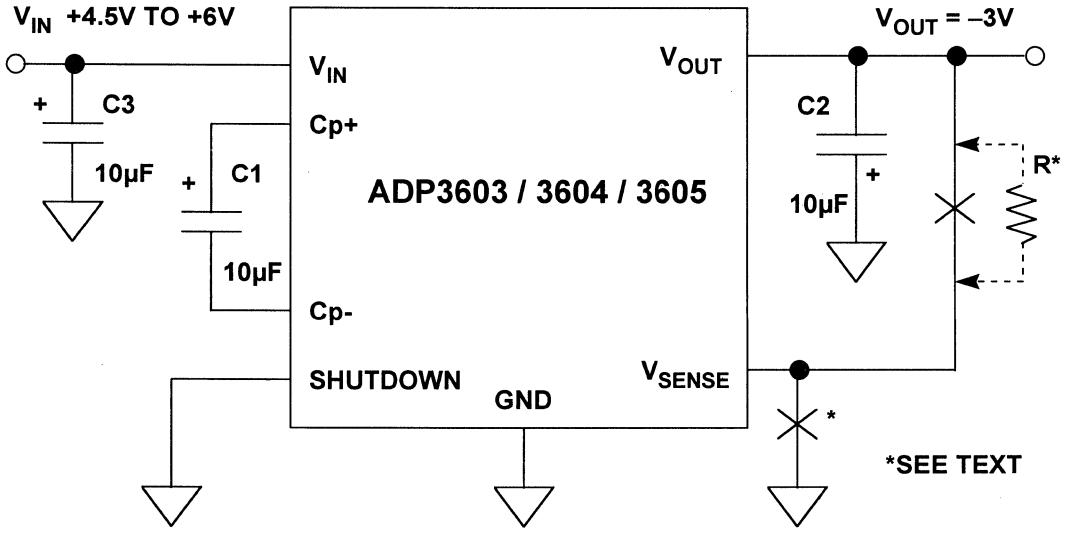


Figure 4.19

The regulated output voltage of the ADP3603/3604/3605 series can varied between –3V and $-V_{IN}$ by connecting a resistor between the output and the V_{SENSE} pin as shown in the diagram. Regulation will be maintained for output currents up to about 30mA. The value of the resistor is calculated from the following equation:

$$V_{OUT} = -\left(\frac{R}{5k\Omega} + 3V\right).$$

The devices can be made to operate as standard inverters providing an unregulated output voltage if the V_{SENSE} pin is simply connected to ground.

The ADP3607/ADP3607-5 are boost switched capacitor voltage regulators based on a regulated voltage doubling topology. The ADP3607-5 is optimized for an output voltage of +5V for inputs between +3V and +5V. The ADP3607 output is adjustable with an external resistor. A block diagram is shown in Figure 4.20 and key specifications in Figure 4.21. The device uses a feedback control scheme similar to the ADP3603/3604/3605 to maintain output voltage regulation for $V_{OUT} < 2V_{IN}$.

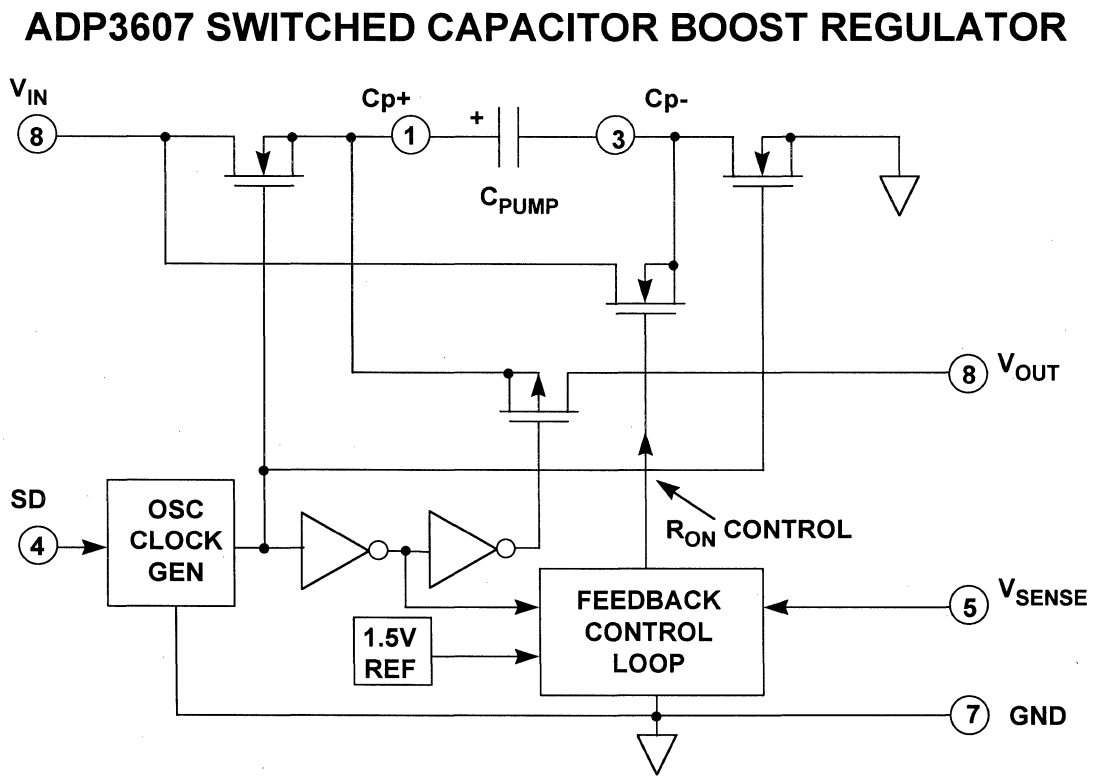


Figure 4.20

ADP3607/ADP3607-5 BOOST REGULATOR KEY SPECIFICATIONS

- **Input Voltage Range: +3V to +5V**
- **Output Voltage: +5V (ADP3607-5)**
- **Adjustable Output Voltage (ADP3607), $V_{OUT} < 2V_{IN}$**
- **Output Current: 50mA**
- **Accuracy: ± 2%**
- **Switching Frequency: 250kHz**
- **Quiescent Current: 2mA**
- **Shutdown Current: 10µA**
- **Turn-On, Turn-Off Time: 50µs**
- **Package: 8-Pin SOIC**

Figure 4.21

A typical application circuit is shown in Figure 4.22. The Schottky diode connecting the input to the output is required for proper operation during start-up and shutdown. If V_{SENSE} is connected to ground, the devices operate as unregulated voltage doublers.

The output voltage of each device can be adjusted with an external resistor. The equation which relates output voltage to the resistor value for the ADP3607 is given by:

$$V_{OUT} = \frac{R}{9.5k\Omega} + 1V, \text{ for } V_{OUT} < 2V_{IN}.$$

The ADP3607 should be operated with an output voltage of at least 3V in order to maintain regulation.

Although the ADP3607-5 is optimized for an output voltage of 5V, its output voltage can be adjusted between 5V and $2V_{IN}$ with an external resistor using the equation:

$$V_{OUT} = \frac{2R}{9.5k\Omega} + 5V, \text{ for } V_{OUT} < 2V_{IN}.$$

ADP3607/ADP3607-5 APPLICATION CIRCUIT

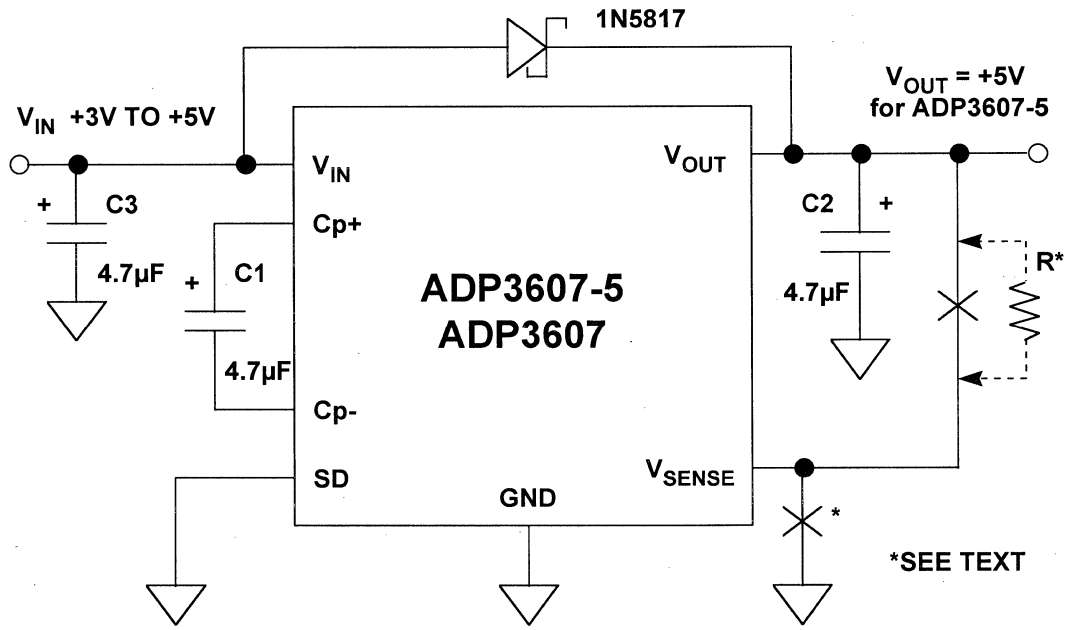


Figure 4.22

When using either the ADP3607 or the ADP3607-5 in the adjustable mode, the output current should be no greater than 30mA in order to maintain good regulation.

The circuit shown in Figure 4.23 generates a regulated 12V output from a 5V input using the ADP3607-5 in a voltage tripler application. Operation is as follows. First assume that the V_{SENSE} pin of the ADP3607-5 is grounded and that the resistor R is not connected. The output of the ADP3607-5 is an unregulated voltage equal to $2V_{IN}$. The voltage at the Cp+ pin of the ADP3607-5 is a square wave with a minimum value of V_{IN} and a maximum value of $2V_{IN}$. When the voltage at Cp+ is V_{IN}, capacitor C2 is charged to V_{IN} (less the D1 diode drop) from V_{OUT1} via diode D1. When the voltage at Cp+ is $2V_{IN}$, the output capacitor C4 is charged to a voltage $3V_{IN}$ (less the diode drops of D1 and D2). The final unregulated output voltage of the circuit, V_{OUT2}, is therefore approximately $3V_{IN} - 2V_D$, where V_D is the Schottky diode voltage drop.

The addition of the feedback resistor, R, ensures that the output is regulated for values of V_{OUT2} between $2V_{IN} - 2V_D$ and $3V_{IN} - 2V_D$. Choosing R = 33.2kΩ yields an output voltage V_{OUT2} of +12V for a nominal input voltage of +5V. Regulation is maintained for output currents up to approximately 20mA.

REGULATED +12V FROM A +5V INPUT USING THE ADP3607-5

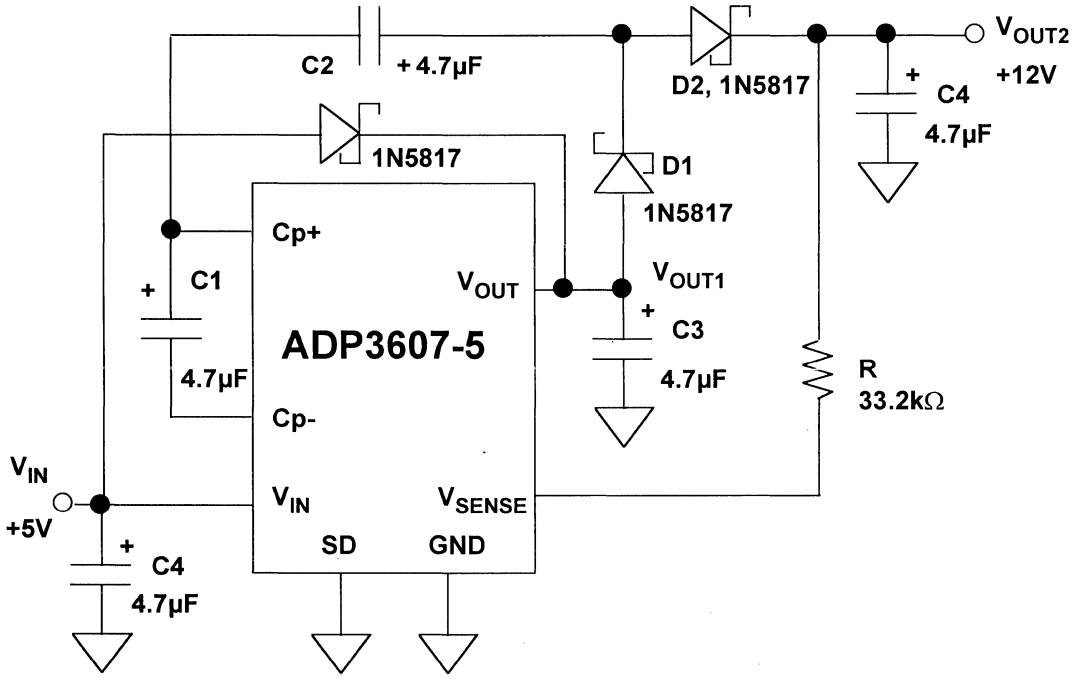


Figure 4.23

SECTION 5

BATTERY CHARGERS

- Battery Fundamentals
- Battery Charging
- Linear Battery Charger
- Switch Mode Dual Charger for Li-Ion, NiCd, and NiMH Batteries
- Universal Charger for Li-Ion, NiCd, and NiMH

SECTION 5
BATTERY CHARGERS
Walt Kester, Joe Buxton

INTRODUCTION

Rechargeable batteries are vital to portable electronic equipment such as laptop computers and cell phones. Fast charging circuits must be carefully designed and are highly dependent on the particular battery's chemistry. The most popular types of rechargeable batteries in use today are the Sealed-Lead-Acid (SLA), Nickel-Cadmium (NiCd), Nickel-Metal-Hydride (NiMH), and Lithium-Ion (Li-Ion). Li-Ion is fast becoming the chemistry of choice for many portable applications because it offers a high capacity-to-size (weight) ratio and a low self-discharge characteristic.

RECHARGEABLE BATTERY CONSIDERATIONS IN PORTABLE EQUIPMENT

- **Amp-Hour Capacity (C) and Cell Voltage**
- **Multiple Cell Configurations: Series/Parallel Combinations, Matching Requirements**
- **Weight and Volume**
- **Cost of Battery Pack**
- **Battery Chemistry**
  - **Sealed Lead Acid (SLA)**
  - **Nickel-Cadmium (NiCd)**
  - **Nickel-Metal Hydride (NiMH)**
  - **Lithium-Ion (Li-Ion)**
  - **Lithium-Metal (Relatively New)**
- **Discharge Characteristics**
- **Charge Characteristics**
- **Cost and Complexity of "Fast Charging" Circuits**

Figure 5.1

There are an enormous number of tradeoffs to be made in selecting the battery and designing the appropriate charging circuits. Weight, capacity, and cost are the primary considerations in most portable electronic equipment. Unfortunately, these considerations are not only interacting but often conflicting. While slow-charging (charging time greater than 12 hours) circuits are relatively simple, fast-charging circuits must be tailored to the battery chemistry and provide both reliable charging and charge termination. Overcharging batteries can cause reduced battery life, overheating, the emission of dangerous corrosive gasses, and sometimes total destruction. For this reason, fast-charging circuits generally have built-in backup means to terminate the charge should the primary termination method fail.

Understanding battery charger electronics requires a knowledge of the battery charge and discharge characteristics as well as charge termination techniques.

BATTERY FUNDAMENTALS

Battery capacity, C, is expressed in Amp hours, or mA hours and is a figure of merit of battery life between charges. Battery current is described in units of *C-Rate*. For instance, a 1000mA-h battery has a C-Rate of 1000mA. The current corresponding to 1C is 1000mA, and for 0.1C, 100mA. For a given cell type, the behavior of cells with varying capacity is similar at the same C-Rate.

"C-RATE" DEFINITION

- **Battery Charge and Discharge Currents are Expressed (Normalized) in Terms of "C-Rate"**
- **C-Rate = C / 1 hour, Where C is the Battery Capacity Expressed in A-hour, or mA-hour**
- **Example:**
  - **A 1000 mA-h Battery has a "C-Rate" of 1000mA**
  - **The Current Corresponding to 1C is 1000mA**
  - **The Current Corresponding to 0.1C is 100mA**
  - **The Current Corresponding to 2C is 2000mA**
- **For a Given Cell Type, the Behavior of Cells with Varying Capacity is Similar at the same C-rate**

Figure 5.2

There are a number of other figures of merit used to characterize batteries which are summarized in Figure 5.3. These figures of merit are used to characterize various battery chemistries as shown in Figure 5.4. Note that in Figure 5.4, the approximate chronology of battery technology is from left to right.

A few terms relating to batteries deserve further clarification. *Self-discharge* is the rate at which a battery discharges with no load. Li-Ion batteries are a factor of two better than NiCd or NiMH in this regard. The *discharge rate* is the maximum allowable load or discharge current, expressed in units of C-Rate. Note that all chemistries can be discharged at currents higher than the battery C-Rate. The number of *charge and discharge cycles* is the average number of times a battery can be discharged and then recharged and is a measure of the battery's service life.

RECHARGEABLE BATTERY FIGURES OF MERIT

- Cell Voltage
- Capacity: C, Measured in Amp-hours (A-h) or mA-hours (mA-h)
- Energy Density (Volume): Measured in Watt-hours/liter (Wh/l)
- Energy Density (Weight): Measured in Watt-hours/kilogram (Wh/kg)
- Cost: Measured in $/Wh
- Memory Effect?
- Self-Discharge Rate: Measured in %/month, or %/day
- Operating Temperature Range
- Environmental Concerns

Figure 5.3

RECHARGEABLE BATTERY TECHNOLOGIES

	Sealed Lead-Acid	Nickel Cadmium*	Nickel Metal Hydride*	Lithium Ion*	Lithium Metal*
Average Cell Voltage (V)	2	1.20	1.25	3.6	3.0
Energy Density (Wh/kg)	35	45	55	100	140
Energy Density (Wh/l)	85	150	180	225	300
Cost ($/Wh)	0.25 - 0.50	0.75 - 1.5	1.5 - 3.0	2.5 - 3.5	1.4 - 3.0
Memory Effect?	No	Yes	No	No	No
Self-Discharge (%/month)	5 - 10	25	20 - 25	8	1 - 2
Discharge Rate	<5C	>10C	<3C	<2C	<2C
Charge/Discharge Cycles	500	1000	800	1000	1000
Temperature Range (°C)	0 to +50	–10 to +50	–10 to +50	–10 to +50	–30 to +55
Environmental Concerns	Yes	Yes	No	No	No

* Based on AA-Size Cell

Figure 5.4

Memory occurs only in NiCd batteries and is relatively rare. It can occur during cyclic discharging to a definite fixed level and subsequent recharging. Upon discharging, the cell potential drops several tenths of a volt below normal and remains there for the rest of the discharge. The total ampere-hour capacity of the cell is not significantly affected. Memory usually disappears if the cell is almost fully discharged and then recharged a time or two. In practical applications, memory is not often a problem because NiCd battery packs are rarely discharged to the same level before recharging.

Environmental concerns exist regarding the proper disposal of sealed-lead-acid and NiCd batteries because of hazardous metal content. NiMH and Li-Ion batteries do not contain significant amounts of pollutant, but nevertheless, some caution should be used in their disposal.

The discharge profiles of these four popular type of batteries are shown in Figure 5.5. A discharge current of 0.2C was used in each case. Note that NiCd, NiMH, and SLA batteries have a relatively flat profile, while Li-Ion batteries have a nearly linear discharge profile.

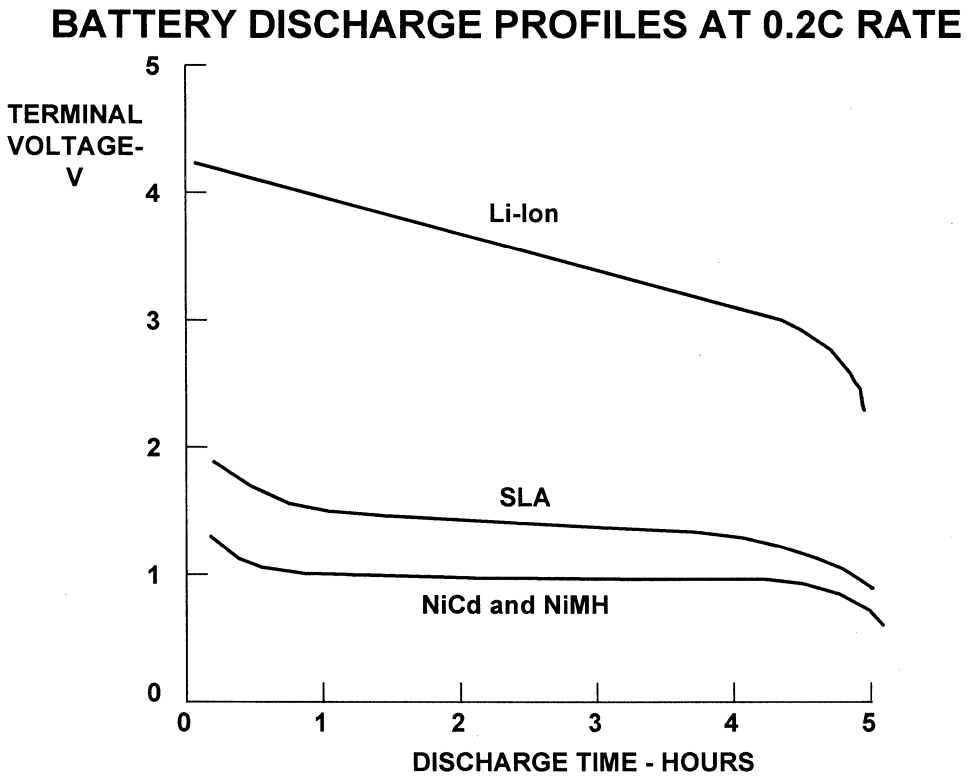


Figure 5.5

BATTERY CHARGING

A generalized battery charging circuit is shown in Figure 5.6. The battery is charged with a constant current until fully charged. The voltage developed across the R_{SENSE} resistor is used to maintain the constant current. The voltage is continuously monitored, and the entire operation is under the control of a microcontroller which may even have an on-chip A/D converter. Temperature sensors are used to monitor battery temperature and sometimes ambient temperature.

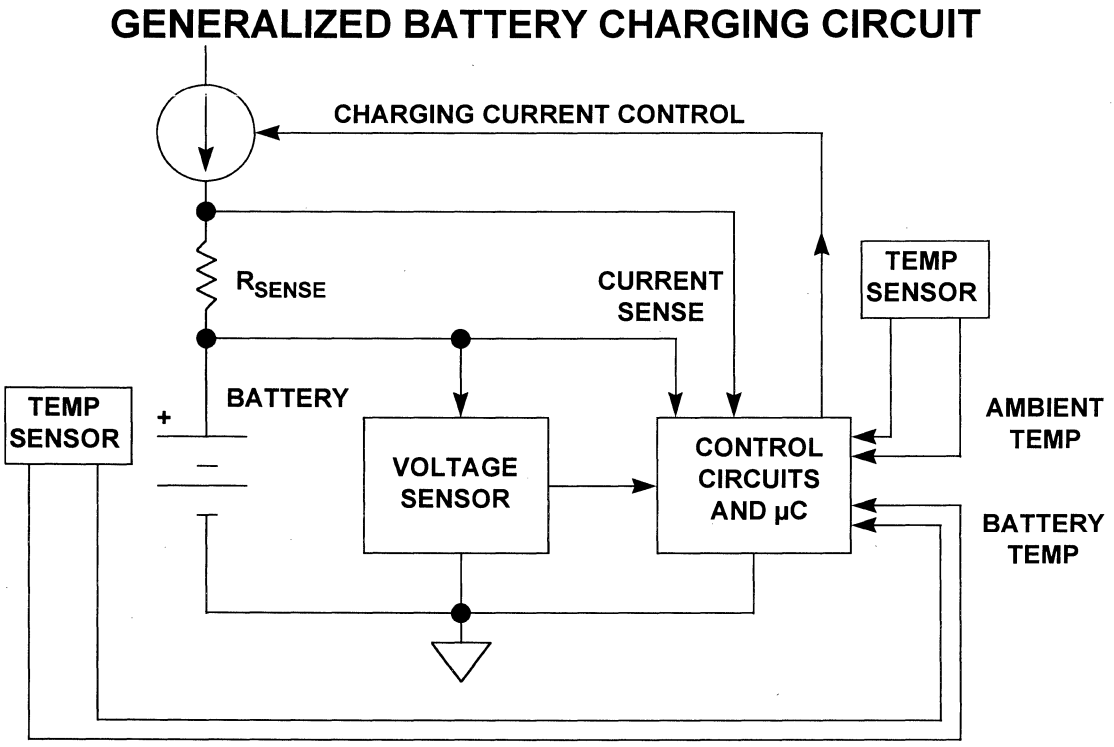


Figure 5.6

This type of circuit represents a high level of sophistication and is primarily used in fast-charging applications, where the charge time is less than 3 hours. Voltage and sometimes temperature monitoring is required to accurately determine the state of the battery and the end-of-charge. Slow charging (charge time greater than 12 hours) requires much less sophistication and can be accomplished using a simple current source. Typical characteristics for slow charging are shown in Figure 5.7. Charge termination is not critical, but a timer is sometimes used to end the slow charging of NiMH batteries. If no charge termination is indicated in the table, then it is safe to *trickle charge* the battery at the slow-charging current for indefinite periods of time. *Trickle charge* is the charging current a cell can accept continually without affecting its service life. A safe trickle charge current for NiMH batteries is typically 0.03C. For example, for an NiMH battery with C = 1A-hr, 30mA would be safe. Battery manufacturers can recommend safe trickle charge current limits for specific battery types and sizes.

BATTERY CHARGING CHARACTERISTICS FOR SLOW CHARGING

	SLA	NiCd	NiMH	Li-Ion
Current	0.25C	0.1C	0.1C	0.1C
Voltage (V/cell)	2.27	1.50	1.50	4.1 or 4.2
Time (hr)	24	16	16	16
Temp. Range	0°/45°C	5°/45°C	5°/40°C	5°/40°C
Termination	None	None	Timer	Voltage Limit

Figure 5.7

Fast-charging batteries (charge time less than 3 hours) requires much more sophisticated techniques. Figure 5.8 summarizes fast-charging characteristics for the four popular battery types. The most difficult part of the process is to correctly determine when to terminate the charging. Undercharged batteries have reduced capacity, while overcharging can damage the battery, cause catastrophic outgassing of the electrolyte, and even explode the battery.

BATTERY CHARACTERISTICS FOR FAST CHARGING (<3HOURS)

	SLA	NiCd	NiMH	Li-Ion
Current	≥1.5C	≥1C	≥1C	1C
Voltage (V/cell)	2.45	1.50	1.50	4.1 or 4.2 ± 50mV
Time (hours)	≤1.5	≤3	≤3	2.5
Temp. Range (°C)	0 to 30	15 to 40	15 to 40	10 to 40
Primary Termination	I_{min}, ΔTCO	−ΔV, dT/dt	dT/dt, dV/dt = 0	I_{min} @ Voltage Limit
Secondary Termination	Timer, ΔTCO	TCO, Timer	TCO, Timer	TCO, Timer

C = Normal Capacity, I_{min} = Minimum Current-Threshold Termination
TCO = Absolute Temperature Cutoff, ΔTCO = Temperature Rise Above Ambient

Figure 5.8

Because of the importance of proper charge termination, a primary and secondary method is generally used. Depending on the battery type, the charge may be terminated based on monitoring battery voltage, voltage change vs. time, temperature change, temperature change vs. time, minimum current at full voltage, charge time, or various combinations of the above.

Battery voltage and temperature are the most popular methods of terminating the charge of NiCd and NiMH batteries. Figure 5.9 shows the cell voltage and temperature as a function of charge time for these two types of batteries (charging at the 1C-rate). Note that NiCd has a distinct peak in the cell voltage immediately preceding full charge. NiMH has a much less pronounced peak, as shown in the dotted portion of the curve. A popular method of charge termination for NiCd is the $-\Delta V$ method, where the charge is terminated after the cell voltage falls 10 to 20mV after reaching its peak.

Note that for both types the temperature increases rather suddenly near full charge. Because of the much less pronounced voltage peak in the NiMH characteristic, the change in temperature with respect to time (dT/dt) is most often used as a primary charge termination method.

NiCd/NiMH BATTERY TEMPERATURE AND VOLTAGE CHARGING CHARACTERISTICS

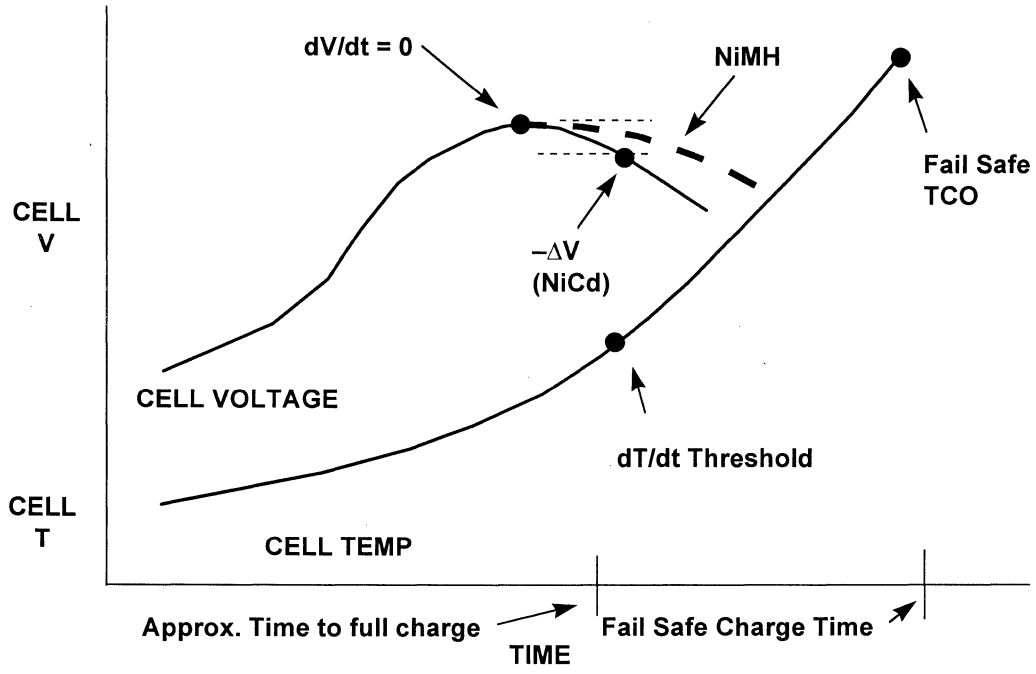


Figure 5.9

In addition to the primary termination, secondary terminations are used as backups for added protection. The primary and secondary termination methods for NiCd and NiMH cells are summarized in Figure 5.10. All these termination methods are generally controlled by a microcontroller. After proper signal conditioning, the cell

voltage and temperature are converted into digital format using 8 or 10-bit A/D converters which may be located inside the microcontroller itself.

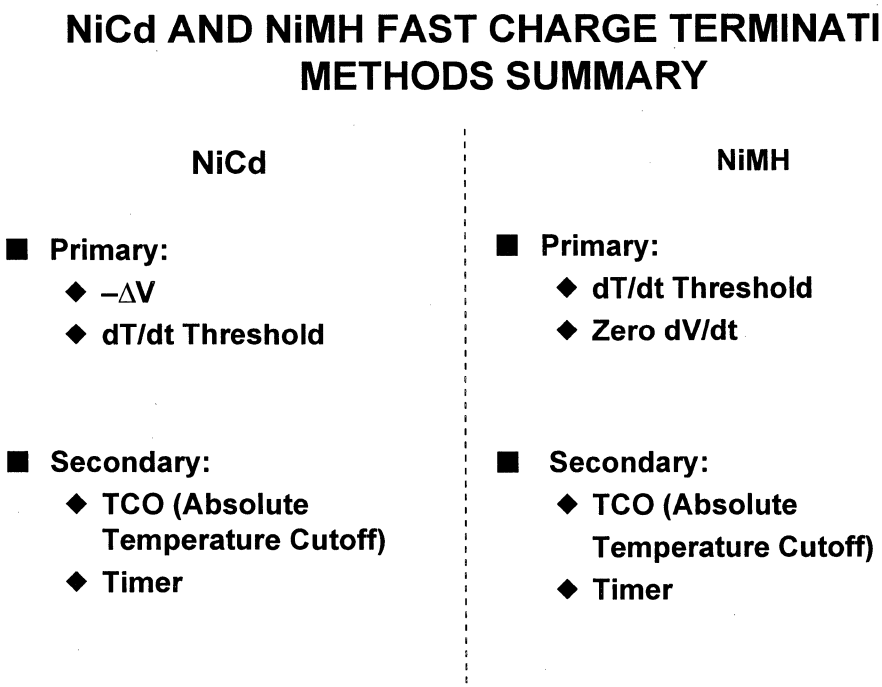


Figure 5.10

Li-Ion cells behave quite differently from the other chemistries in that there is a gradual rise to the final cell voltage when charged from a constant current source (see Figure 5.11). The ideal charging source for Li-Ion is a current-limited constant voltage source (sometimes called constant-current, constant-voltage, or CC-CV). A constant current is applied to the cell until the cell voltage reaches the final battery voltage (4.2V ±50mV for most Li-Ion cells, but a few manufacturers' cells reach full charge at 4.1V). At this point, the charger switches from constant-current to constant-voltage, and the charge current gradually drops. The gradual drop in charge current is due to the internal cell resistance. Charge is terminated when the current falls below a specified minimum value, I_{MIN}. It should be noted that approximately 65% of the total charge is delivered to the battery during the constant current mode, and the final 35% during the constant voltage mode.

Secondary charge termination is usually handled with a timer or if the cell temperature exceeds a maximum value, TCO (absolute temperature cutoff).

It should be emphasized that Li-Ion batteries are extremely sensitive to overcharge! Even slight overcharging can result in a dangerous explosion or severely decrease battery life. For this reason, it is critical that the final charge voltage be controlled to within about ±50mV of the nominal 4.2V value.

Li-Ion FAST CHARGING CHARACTERISTICS

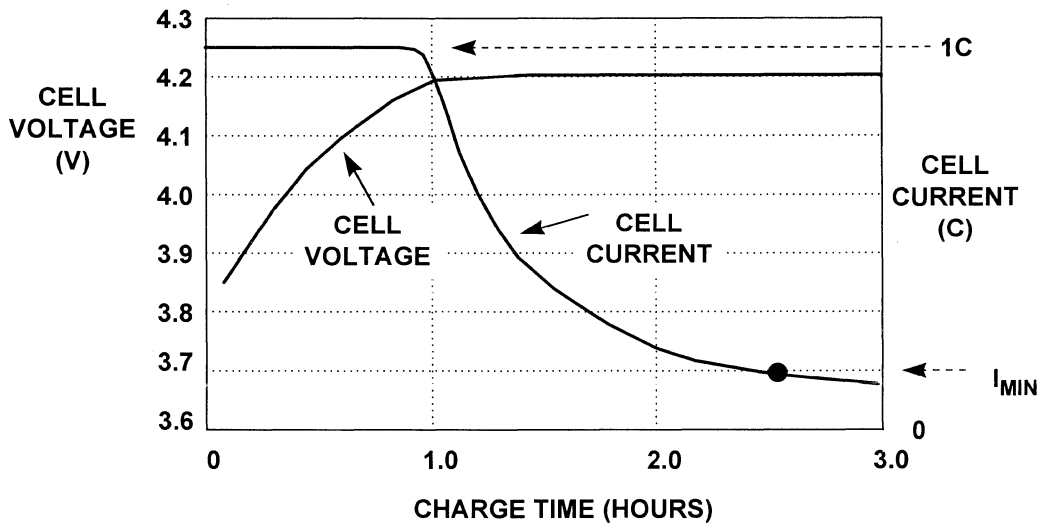


Figure 5.11

Battery packs which contain multiple Li-Ion cells are generally manufactured with matched cells and voltage equalizers. The external charging circuitry controls the charging current and monitors the voltage across the entire battery pack. However, the voltage across each cell is also monitored within the pack, and cells which have higher voltage than others are discharged through shunt FETs. If the voltage across any cell exceeds 4.2V, charging must be terminated.

5

Li-Ion CHARGE TERMINATION TECHNIQUES

- **Primary:**
  - **Detection of Minimum Threshold Charging Current with Cell Voltage Limited to 4.2V**
- **Secondary:**
  - **TCO (Absolute Temperature Cutoff)**
  - **Timer**
- **Accurate Control (± 50mV) of Final Battery Voltage Required for Safety!**
- **Multiple-Cell Li-Ion Battery Packs Require Accurate Cell Matching and/or Individual Cell Monitors and Charge Current Shunts for Safety**

Figure 5.12

Under no circumstances should a multiple-cell Li-Ion battery pack be constructed from individual cells without providing this voltage equalization function!

While the dangers of overcharging cannot be overstated, undercharging a Li-Ion cell can greatly reduce capacity as shown in Figure 5.13. Notice that if the battery is undercharged by only 100mV, 10% of the battery capacity is lost. For this reason, accurate control of the final charging voltage is mandatory in Li-Ion chargers.

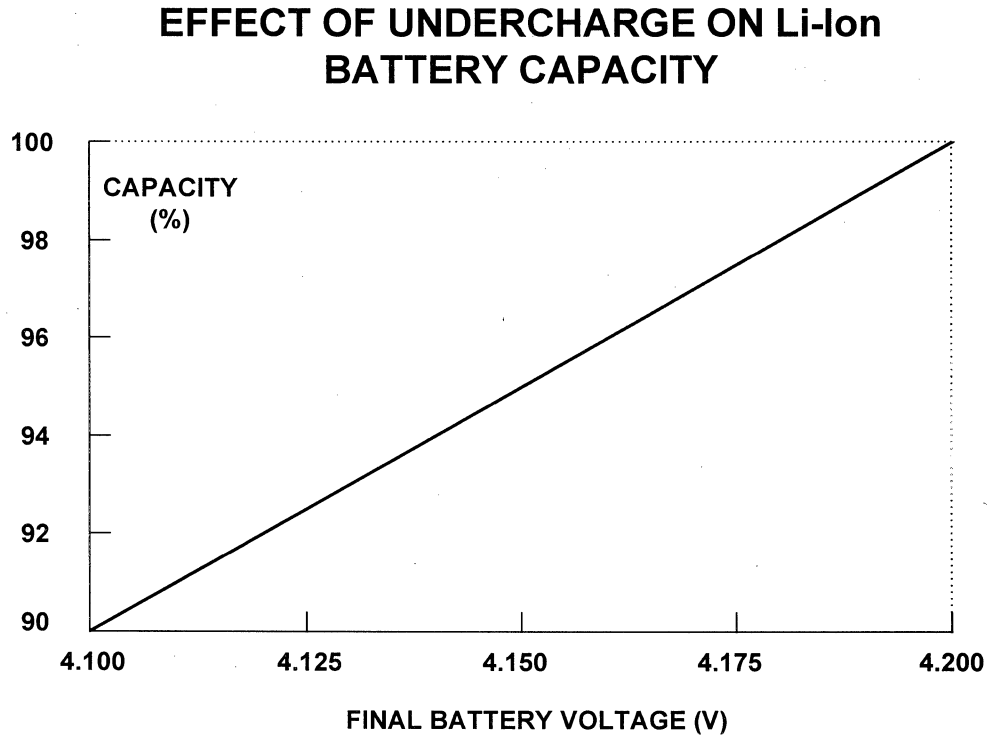


Figure 5.13

From the above discussion, it is clear that accurate control of battery voltage and current is key to proper charging, regardless of cell chemistry. The ADP3810/3811-series of ICs makes this job much easier to implement. A block diagram of the IC is shown in Figure 5.14. Because the final voltage is critical in charging Li-Ion cells, the ADP3810 has precision resistors (R1 and R2) which are accurately trimmed for the standard Li-Ion cell/multiple cell voltages of 4.2V (1 cell), 8.4V (2 cells), 12.6V (3 cells), and 16.8V (4 cells). The value of the charging current is controlled by the voltage applied to the V_{CTRL} input pin. The charging current is constantly monitored by the voltage at the V_{CS} input pin. The voltage is derived from a low-side sense resistor placed in series with the battery. The output of the ADP3810 (OUT pin) is applied to external circuitry, such as a PWM, which controls the actual charging current to the battery. The output is a current ranging from 0 to 5mA which is suitable for driving an opto-isolator in an isolated system.

ADP3810/3811 BLOCK DIAGRAM

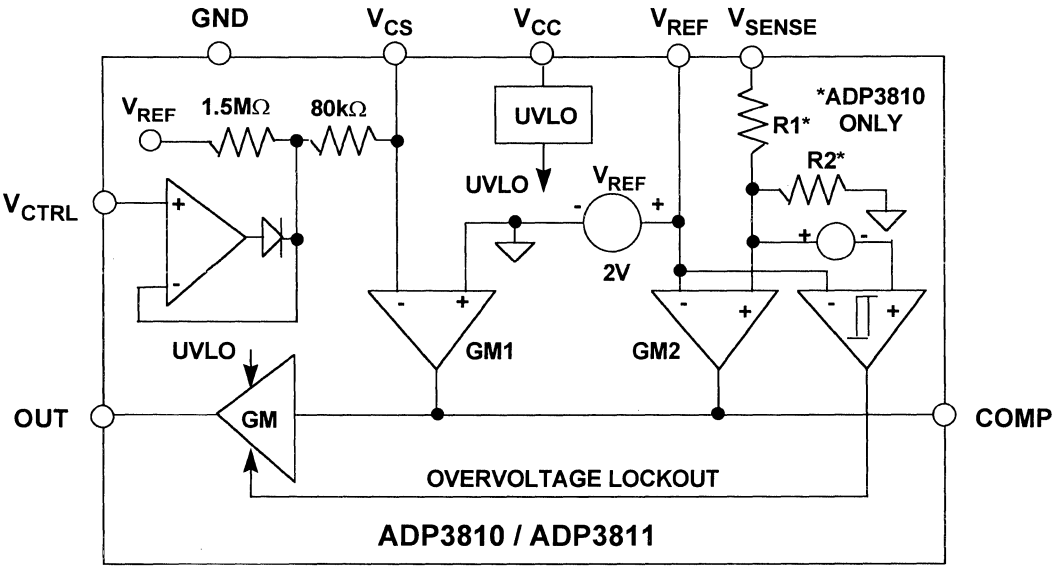


Figure 5.14

5

ADP3810/3811 BATTERY CHARGER CONTROLLER KEY FEATURES

- Programmable Charge Current
- Battery Voltage Limits
  - (4.2V, 8.4V, 12.6V, 16.8V) ± 1%, ADP3810
  - Adjustable, ADP3811
- Overvoltage Comparator (6% Over Final Voltage)
- Input Supply Voltage Range 2.7V to 16V
- Undervoltage Shutdown for V_{CC} less than 2.7V
- Sharp Current to Voltage Control Transition Due to High Gain GM Stages
- SO-8 Package with Single Pin Compensation

Figure 5.15

The charging current is held constant until the battery voltage (measured at the V_{SENSE} input) reaches the specified value (i.e. 4.2V per cell). The voltage control loop has an accuracy of ±1%, required by Li-Ion batteries. At this point, the control switches from the current control loop (V_{CS}) to the voltage control loop (V_{SENSE}), and the battery is charged with a constant voltage until charging is complete. In addition, the ADP3810 has an overvoltage comparator which stops the charging process if the battery voltage exceeds 6% of its programmed value. This function protects the circuitry should the battery be removed during charging. In addition, if the supply voltage drops below 2.7V, the charging is stopped by the undervoltage lockout (UVLO) circuit.

The ADP3811 is identical to the ADP3810 except that the V_{SENSE} input ties directly to the GM2 stage input, and R1/R2 are external, allowing other voltages to be programmed by the user for battery chemistries other than Li-Ion.

A simplified functional diagram of a battery charger based on the ADP3810/3811 battery charger controller is shown in Figure 5.16. The ADP3810/3811 controls the DC-DC converter which can be one of many different types such as a buck, flyback, or linear regulator. The ADP3810/3811 maintains accurate control of the current and voltage loops.

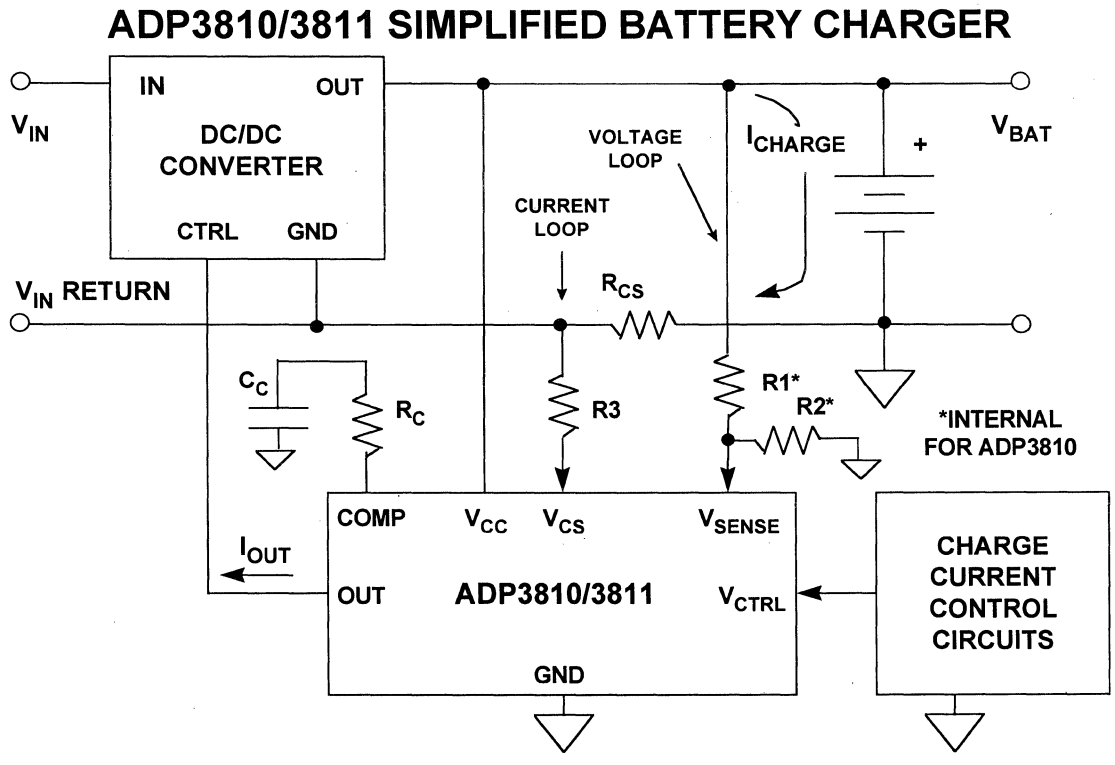


Figure 5.16

The value of the charge current is controlled by the feedback loop comprised of R_{CS}, R3, GM1, the external DC-DC converter, and the DC voltage at the V_{CTRL} input. The actual charge current is set by the voltage, V_{CTRL}, and is dependent upon the choice for the values of R_{CS} and R3 according to:

$$I_{CHARGE} = \frac{1}{R_{CS}} \cdot \frac{R3}{80k\Omega} \cdot V_{CTRL} \cdot$$

Typical values are $R_{CS} = 0.25\Omega$ and $R3 = 20k\Omega$, which result in a charge current of 1.0A for a control voltage of 1.0V. The 80kΩ resistor is internal to the IC, and it is trimmed to its absolute value. The positive input of GM1 is referenced to ground, forcing the V_{CS} point to a virtual ground.

The low-side sense resistor, R_{CS}, converts the charging current into a voltage which is applied to the V_{CS} pin. If the charge current increases above its programmed value, the GM1 stage forces the current, I_{OUT}, to increase. The higher I_{OUT} decreases the duty cycle of the DC-DC converter, reducing the charging current and balancing the feedback loop.

As the battery approaches its final charge voltage, the voltage control loop takes over. The system becomes a voltage source, floating the battery at constant voltage, thereby preventing overcharging. The voltage control loop is comprised of R1, R2, GM2, and the DC-DC converter. The final battery voltage is simply set by the ratio of R1 to R2 according to:

$$V_{BAT} = 2.000V \cdot \left(\frac{R1}{R2} + 1\right).$$

If the battery voltage rises above its programmed voltage, V_{SENSE} is pulled high causing GM2 to source more current, thereby increasing I_{OUT}. As with the current loop, the higher I_{OUT} reduces the duty cycle of the DC-DC converter and causes the battery voltage to fall, balancing the feedback loop.

Notice that because of the low-side sensing scheme, the ground of the circuits in the system must be isolated from the ground of the DC-DC converter.

Further design details for specific applications are given in the ADP3810/3811 data sheet (Reference 7), including detailed analysis and computations for compensating the feedback loops with resistor R_C and capacitor C_C.

The ADP3810/3811 does not include circuitry to detect charge termination criteria such as $-\Delta V$ or dT/dt, which are common for NiCd and NiMH batteries. If such charge termination schemes are required, a low cost microcontroller can be added to the system to monitor the battery voltage and temperature. A PWM output from the microcontroller can subsequently program the V_{CTRL} input to set the charge current. The high impedance of V_{CTRL} enables the addition of an RC filter to integrate the PWM output into a DC control voltage.

OFF-LINE, ISOLATED, FLYBACK BATTERY CHARGER

The ADP3810/3811 are ideal for use in isolated off-line chargers. Because the output stage can directly drive an optocoupler, feedback of the control signal across an isolation barrier is a simple task. Figure 5.17 shows a simplified schematic of a flyback battery charger with isolation provided by the flyback transformer and the optocoupler. For details of the schematic, refer to the ADP3810/3811 data sheet (Reference 7).

Caution: This circuit contains lethal AC and DC voltages, and appropriate precautions must be observed!! Please refer to the data sheet text and schematic if building this circuit!!

The operation of the circuit is similar to that of Figure 5.16. The DC-DC converter block is comprised of a primary-side PWM circuit and flyback transformer, and the control signal passes through the optocoupler to the PWM.

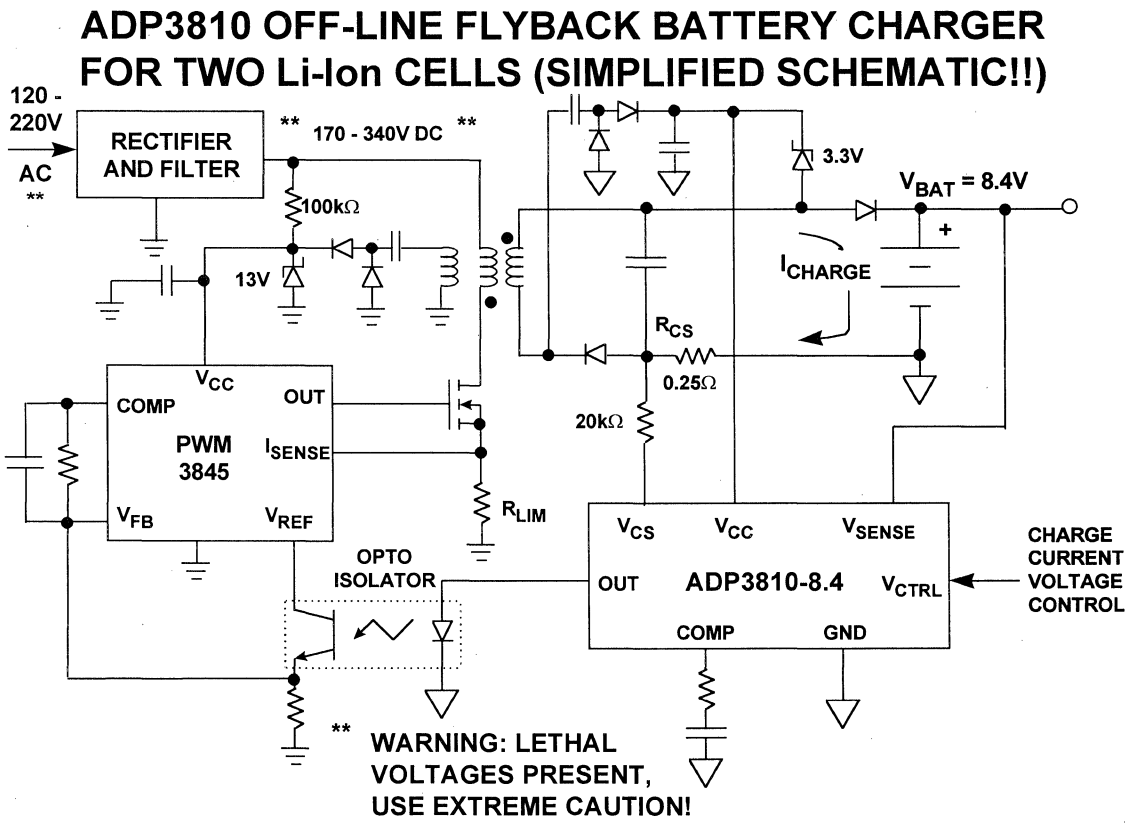


Figure 5.17

A typical current-mode flyback PWM controller (3845-series) was chosen for the primary control for several reasons. First and most importantly, it is capable of operating from very small duty cycles to near the maximum desired duty cycle. This makes it a good choice for a wide input AC supply voltage variation requirement, which is usually between 70V and 270V for world-wide applications. Add to that the additional requirement of 0% to 100% current control, and the PWM duty cycle

must have a wide range. This charger achieves these ranges while maintaining stable feedback loops.

The detailed operation and design of the primary side PWM is widely described in the technical literature and is not detailed here. However, the following explanation should make clear the reasons for the primary-side component choices. The PWM frequency is set to around 100kHz as a reasonable compromise between inductive and capacitive component sizes, switching losses, and cost.

The primary-side PWM-IC derives its starting V_{CC} through a 100kΩ resistor directly from the rectified AC input. After start-up, a simple rectifier circuit driven from a third winding on the transformer charges a 13V zener diode which supplies the V_{CC} to the 3845 PWM.

While the signal from the ADP3810/3811 controls the average charge current, the primary side should have cycle by cycle limit of the switching current. This current limit has to be designed so that, with a failed or malfunctioning secondary circuit or optocoupler, the primary power circuit components (the MOSFET and the transformer) won't be overstressed. In addition, during start-up or for a shorted battery, V_{CC} to the ADP3810/3811 will not be present. Thus, the primary side current limit is the only control of the charge current. As the secondary side V_{CC} rises above 2.7V, the ADP3810/3811 takes over and controls the average current. The primary side current limit is set by the R_{LIM} resistor.

The current drive of the ADP3810/3811's output stage directly connects to the photodiode of an optocoupler with no additional circuitry. With 5mA of output current, the output stage can drive a variety of optocouplers.

A current-mode flyback converter topology is used on the secondary side. Only a single diode is needed for rectification, and no filter inductor is required. The diode also prevents the battery from back driving the charger when input power is disconnected. The R_{CS} resistor senses the average current which is controlled via the V_{CS} input.

The V_{CC} source to the ADP3810/3811 can come from a direct connection to the battery as long as the battery voltage remains below the specified 16V operating range. If the battery voltage is less than 2.7V (e.g., with a shorted battery, or a battery discharged below its minimum voltage), the ADP3810/3811 will be in Undervoltage Lock Out (UVLO) and will not drive the optocoupler. In this condition, the primary PWM circuit will run at its designed current limit. The V_{CC} of the ADP3810/3811 is boosted using the additional rectifier and 3.3V zener diode. This circuit keeps V_{CC} above 2.7V as long as the battery voltage is at least 1.5V with a programmed charge current of 0.1A. For higher programmed charge current, the battery voltage can drop below 1.5V, and V_{CC} is still maintained above 2.7V.

The charge current versus charge voltage characteristics for three different charge current settings are shown in Figure 5.18. The high gain of the internal amplifiers ensures the sharp transition between current-mode and voltage-mode regardless of the charge current setting. The fact that the current remains at full charging until the battery is very close to its final voltage ensures fast charging times. It should be noted, however, that the curves shown in Figure 5.18 reflect the performance of only

the charging circuitry and not the I/V characteristics when charging an actual battery. The internal battery resistance will cause a more gradual decrease in charge current when the final cell voltage is reached (see Figure 5.11, for example).

A detailed description of this off-line charging circuit is contained in the ADP3810/3811 data sheet (Reference 7) along with design examples for those interested.

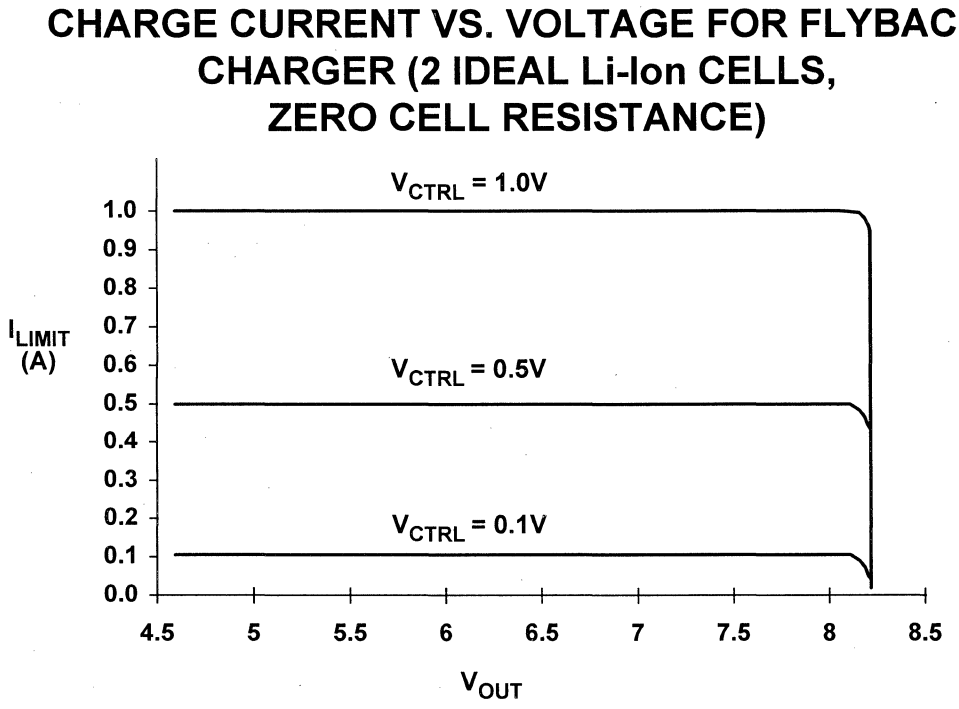


Figure 5.18

Off-line chargers are often used in laptop computers as shown in Figure 5.19. Here, there are many options. The "brick" may consist of a simple AC/DC converter, and the charger circuit put inside the laptop. In some laptops, the charger circuit is part of the brick. Ultimately, the entire AC/DC converter as well as the charger circuit can be put inside the laptop, thereby eliminating the need for the brick entirely. There are pros and cons to all the approaches, and laptop computer designers wrestle with these tradeoffs for each new design.

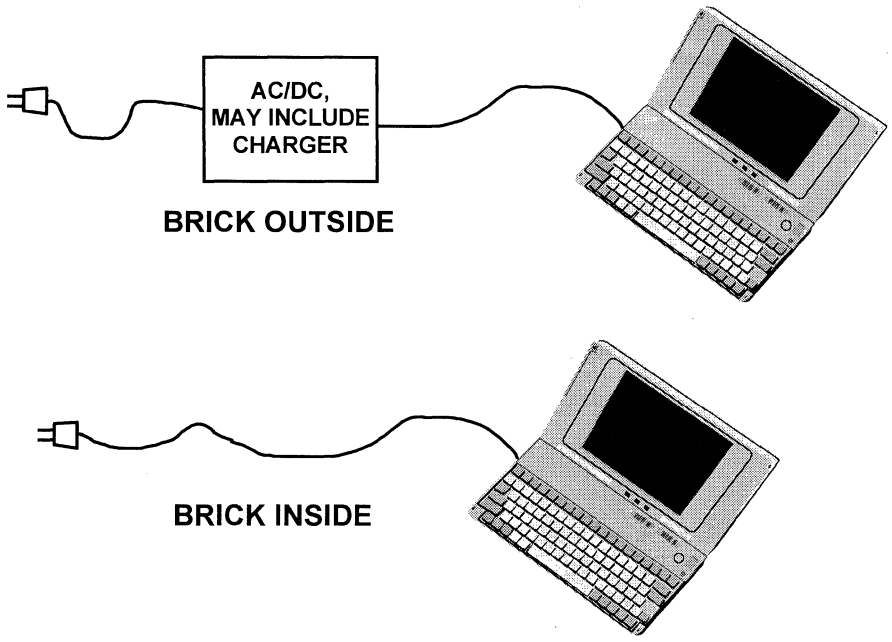


Figure 5.19

LINEAR BATTERY CHARGER

In some applications where efficiency and heat generation is not a prime concern, a low cost linear battery charger can be an ideal solution. The ADP3820 linear regulator controller is designed to accurately charge single cell Li-Ion batteries as shown in Figure 5.20. Its output directly controls the gate of an external p-channel MOSFET. As the circuit shows, a linear implementation of a battery charger is a simple approach. In addition to the IC and the MOSFET, only an external sense resistor and input and output capacitors are required. The charge current is set by choosing the appropriate value of sense resistor, R_S. The ADP3820 includes all the components needed to guarantee a system level specification of ±1% final battery voltage, and it is available with either a 4.2V or 4.1V final battery voltage. The ADP3820 has an internal precision reference, low offset amplifier, and trimmed thin film resistor divider to guarantee Li-Ion accuracy. In addition, an enable (EN) pin is available to place the part in low current shutdown.

If a linear charger is needed for higher Li-Ion battery voltages such as 8.4V, 12.6V, or 16.8V, the ADP3810 with an external MOSFET can also be used. Refer to the ADP3810 data sheet for more details.

The tradeoff between using a linear regulator as shown versus using a flyback or buck-type of charger is efficiency versus simplicity. The linear charger of Figure 5.20 is very simple, and it uses a minimal amount of external components. However, the efficiency is poor, especially when there is a large difference between the input and output voltages. The power loss in the power MOSFET is equal to $(V_{IN}-V_{BAT})\cdot I_{CHARGE}$. Since the circuit is powered from a wall adapter, efficiency may not be a big concern, but the heat dissipated in the pass transistor could be excessive.

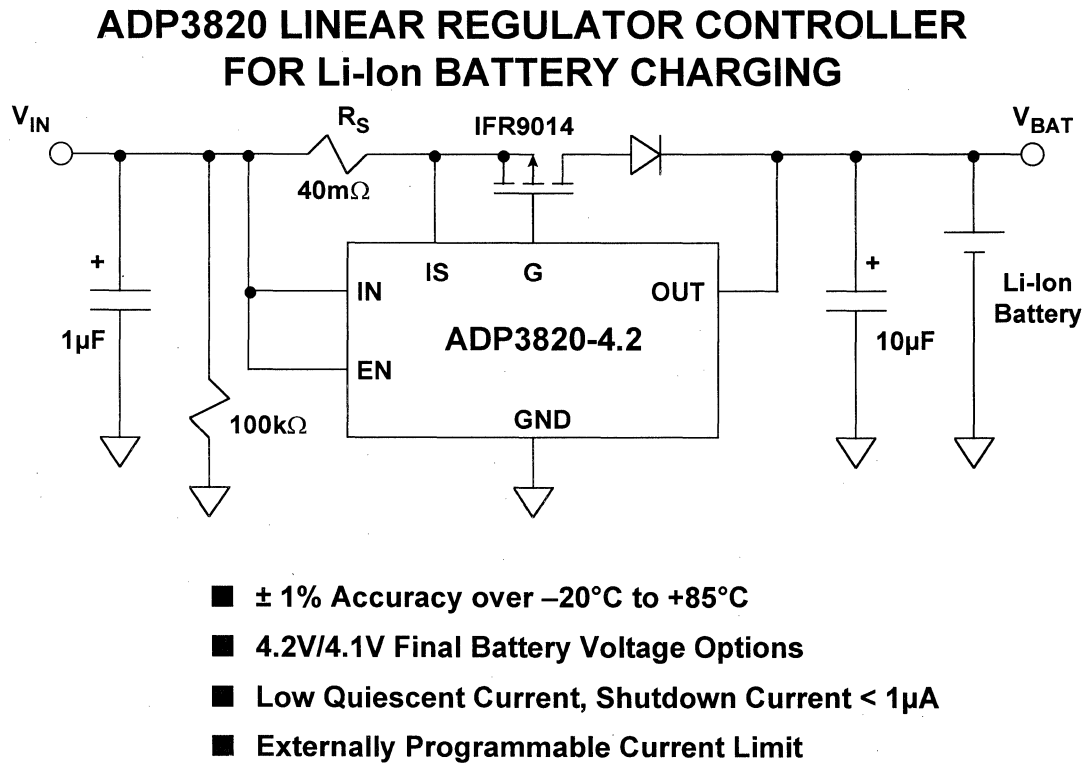


Figure 5.20

SWITCH MODE DUAL CHARGER FOR LI-ION, NICD, AND NIMH BATTERIES

The ADP3801 and ADP3802 are complete battery charging ICs with on-chip buck regulator control circuits. The devices combine a high accuracy, final battery voltage control with a constant charge current control, and on-chip 3.3V Low Drop-Out Regulator. The accuracy of the final battery voltage control is ±0.75% to safely charge Li-Ion batteries. An internal multiplexer allows the alternate charging of two separate battery stacks. The final voltage is pin programmable to one of six options: 4.2V (one Li-Ion cell), 8.4V (two Li-Ion cells), 12.6V (three Li-Ion cells), 4.5V (three NiCd/NiMH cells), 9.0V(six NiCd/NiMH cells), or 13.5V (nine NiCd/NiMH cells). In addition, a pin is provided for changing the final battery voltage by up to ±10% to adjust for variations in battery chemistry from different Li-Ion manufacturers. A functional diagram along with a typical application circuit is shown in Figure 5.21.

The ADP3801 and ADP3802 directly drive an external PMOS transistor. Switching frequencies of the family are 200kHz (ADP3801), and 500kHz (ADP3802). An on-chip end of charge comparator indicates when the charging current drops to below 80mA (50mA of hysteresis prevents comparator oscillation).

ADP3801/ADP3802 BUCK BATTERY CHARGER

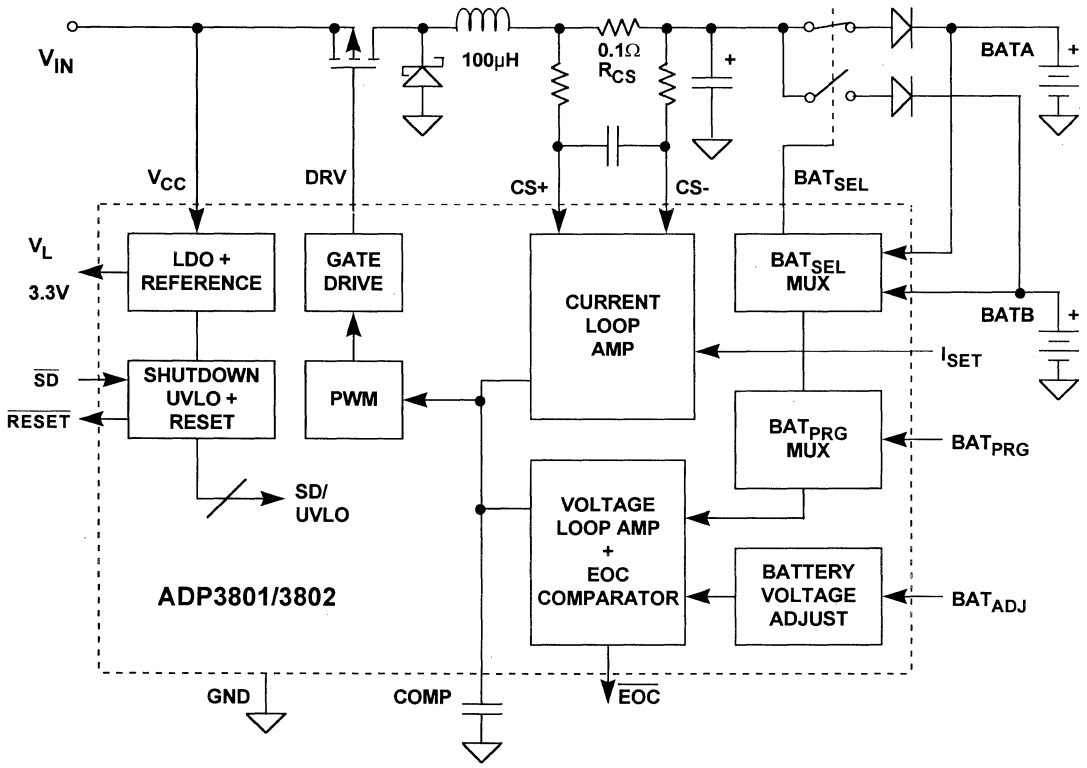


Figure 5.21

ADP3801/ADP3802 SWITCH MODE BATTERY CHARGER KEY SPECIFICATIONS

- Programmable Charge Current with High-Side Sensing
- ± 0.75% End-of-Charge Voltage
- Pin Programmable Battery Chemistry and Cell Number Select
- On Chip LDO Regulator (3.3V)
- Drives External PMOS Transistor
- PWM Oscillator Frequency:
  - ADP3801: 200kHz
  - ADP3802: 500kHz
- End-of-Charge Output Signal
- SO-16 Package

Figure 5.22

Both devices offer a 3.3V LDO. The LDO can deliver up to 20mA of current to power external circuitry such as a microcontroller. An Under Voltage Lock-Out (UVLO) circuit is included to safely shut down the charging circuitry when the input voltage drops below its minimum rating. A shutdown pin is also provided to turn off the charger when, for example, the battery has been fully charged. The LDO remains active during shutdown, and the UVLO circuit consumes only 100μA of quiescent current.

During charging, the ADP3801/3802 maintains a constant, programmable charge current. The high-side, differential to single-ended current sense amplifier has low offset allowing the use of a low voltage drop sense resistor of 100mΩ. The input common mode range extends from ground to V_{CC} – 2V ensuring current control over the full charging voltage of the battery, including a short circuit condition. The output of the current sense amp is compared to a high impedance, DC voltage input, ISET. V_{ISET} sets the charge current is as follows:

$$I_{CHARGE} = \frac{V_{ISET}}{10 \cdot R_{CS}}$$

For R_{CS} = 100mΩ, an input voltage of V_{ISET} = 1.0V gives a charge current of 1.0 Amp.

When the battery voltage approaches its final limit, the device naturally transfers to voltage control mode. The charge current then decreases gradually as was shown in Figure 5.11. The BAT_{PRG} pin is used to program one of the six available battery voltages. This pin controls a six channel multiplexer that selects the proper tap on a resistor divider as shown in Figure 5.23. The output of the MUX is connected to an error amplifier that compares the divided down battery voltage to a 1.65V reference. The accuracy of the final battery voltage is dependent upon the major functions shown in Figure 5.23. The accuracy of the reference, the resistor divider, and the amplifier must all be well controlled to give an overall accuracy of ±0.75%.

The ADP3801 and 3802 are designed to charge two separate battery packs. These batteries can be of different chemistries and have a different number of cells. At any given time, only one of the two batteries is being charged. To select which battery is being monitored, and therefore, which battery is being charged, the devices include a battery selector multiplexer as is shown in Figure 5.23. This two channel mux is designed to "break before make" to ensure that the two batteries are not shorted together momentarily when switching from one to the other.

An important feature for Li-Ion battery chargers is an end-of-charge detect (EOC). The $\overline{EOC}$ signal operation is shown in Figure 5.24. When the charge current drops below 80mA (for R_{CS} = 0.1Ω), the $\overline{EOC}$ output pulls low. The EOC threshold current, I_{MIN}, is given by the equation:

$$I_{MIN} = \frac{8mV}{R_{CS}}.$$

INTERNAL MUX SELECTS FINAL BATTERY VOLTAGE

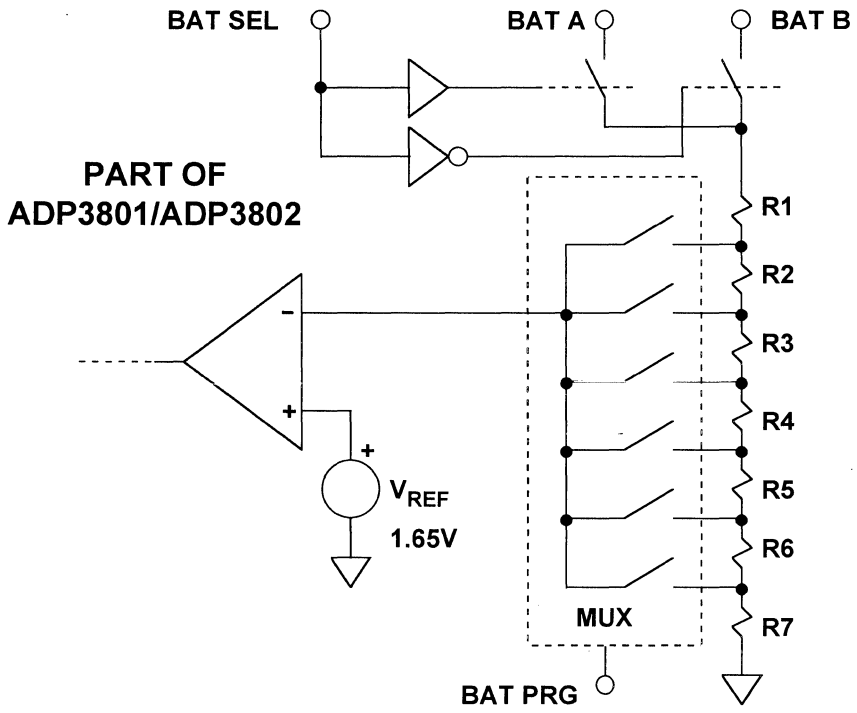


Figure 5.23

END-OF-CHARGE (EOC) DETECTION IN THE ADP3801/ADP3802

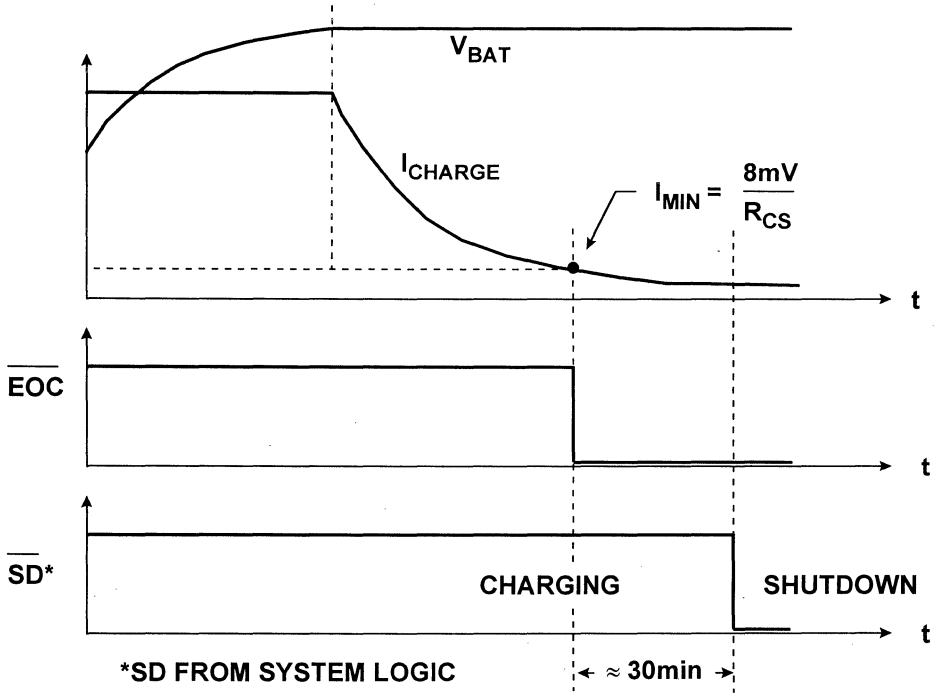


Figure 5.24

The internal EOC comparator actually monitors the voltage across CS+ and CS– (V_{CS}). When V_{CS} drops to 8mV, the $\overline{EOC}$ comparator trips. Thus, the actual current level for detecting the end of charge can be adjusted by changing the value of R_{CS}. This may be useful when more than one cell is charged in parallel. For example, two parallel cells may use an end of charge current of 160mA, so R_{CS} should be 0.05Ω. This results in a total charging current of 2A (1A/cell) for V_{ISET} = 1V. It should be noted, however, that changing the value of R_{CS} in order to change I_{MIN} also requires a change in V_{ISET} in order to maintain the same charging current.

To prevent false triggering of $\overline{EOC}$ during start-up, the internal comparator is gated by a second comparator that monitors the battery voltage. The $\overline{EOC}$ comparator is only enabled when V_{BAT} is at least 95% of its final value. Because of the soft start, the charge current is initially zero when the power is applied. If the $\overline{EOC}$ comparator was not gated by the battery voltage, it would initially signal the $\overline{EOC}$ until the charge current rose above 80mA, which could cause incorrect battery charging.

Typically system operation is to continue charging for 30 minutes after the $\overline{EOC}$ signal and then shutdown the charger using the $\overline{SD}$ pin. Li-Ion manufacturers recommend that the battery should not be left in trickle charge mode indefinitely. Thus, the ADP3801/3802 $\overline{EOC}$ signal makes the charger design simpler. Periodically, the system can remove the $\overline{SD}$ signal, wait until the switching regulator output settles, check the status of the $\overline{EOC}$ signal, and then decide to resume charging if necessary. This operation maintains a fully charged battery without having to resort to trickle charging.

The output stage of the ADP3801/3802 is designed to directly drive an external PMOS transistor. Some discrete logic level PMOS transistors have a low V_{GS} breakdown voltage specification. To prevent damage, the output swing is limited to approximately 8V below VCC.

For further details on specific design issues, consult the ADP3801/3802 product data sheet (Reference 9).

UNIVERSAL CHARGER FOR LI-ION, NICD, AND NIMH

Many applications only require the charger to charge one specific battery. The form factor (physical dimensions) of the battery pack is usually unique to prevent other battery types from being plugged in. However, some applications require the charger to handle multiple battery types and chemistries. The design for these universal chargers is fairly complicated because the charger must first identify the type of battery, program the charge current and voltage, and choose the proper charge termination scheme. Clearly, such a charger requires some sort of microcontroller intelligence. Figure 5.25 shows a simplified block diagram for a universal charger using a microcontroller with the ADP3801.

UNIVERSAL BATTERY CHARGER - SIMPLIFIED

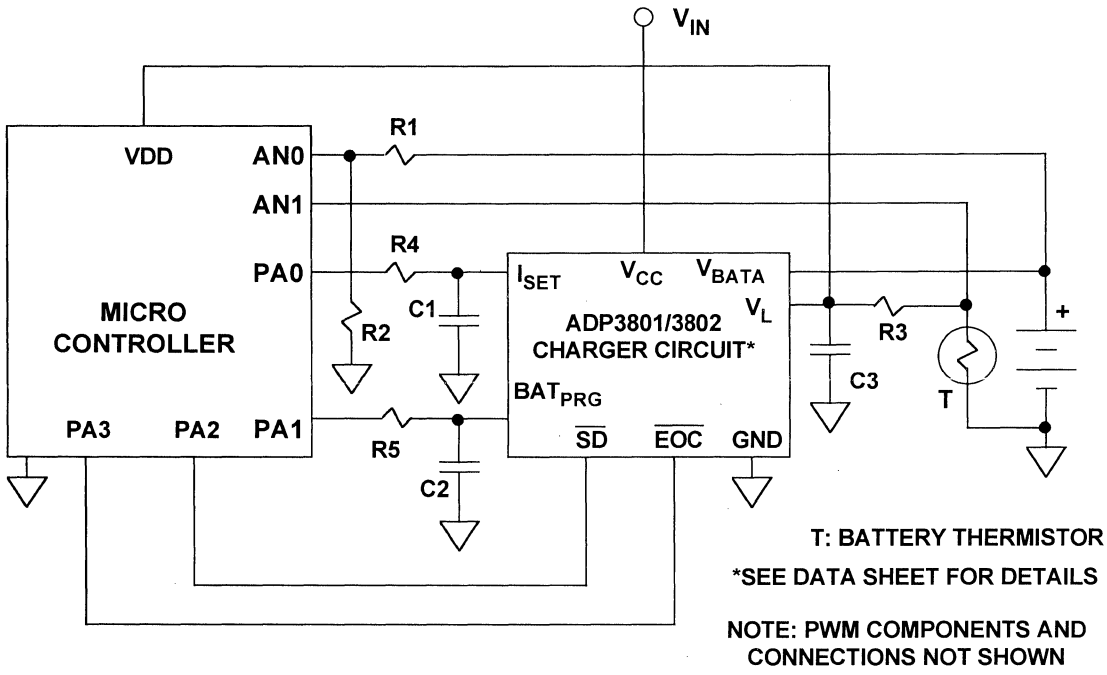


Figure 5.25

The microcontroller is used to monitor the battery voltage and temperature via its internal 8-bit ADC and multiplexer input. It also keeps track of the overall charge time. It may also monitor the ambient temperature via a thermistor or an analog temp sensor. The ADP3801's LDO makes an ideal supply for the microcontroller and the RESET pin generates the necessary power on reset signal. The LDO can also be used as a ±1% reference for the ADC.

The first step when a battery is inserted into the charger is to identify the type of battery placed in the charger. The most common method of doing this is reading the value of the in-pack thermistor. Different values of thermistors are used to identify if the battery is Li-Ion or if it is NiCd/NiMH. This thermistor is also used to monitor the temperature of the battery. A resistor from the ADP3801's LDO to the battery's thermistor terminal forms a resistor divider and generates a voltage across the thermistor for the microcontroller to read. During this time, the ADP3801 should be in shutdown, which the µC controls via the $\overline{SD}$ pin.

When the battery has been identified, the microcontroller can do a pre-qualification of the battery to make sure its voltage and temperature are within the charging range. Assuming that the battery passes, the $\overline{SD}$ pin is taken high, and the charging process begins. To program the charge voltage and charge current, two digital outputs from the µC can be used in PWM mode with an RC filter on the BAT_{PRG} and I_{SET} pins. A connection should also be made between the $\overline{EOC}$ pin of the ADP3801 and a digital input on the µC.

If the battery has been identified as NiCd/NiMH, then the µC must monitor the voltage and temperature to look for $-\Delta V$ or dT/dt criteria to terminate charging.

After this point has been reached the charge current can be set to trickle charge. A timer function is needed to terminate charge if the charge time exceeds an upper limit, which is usually a sign that the battery is damaged and the normal termination methods will not work. The ADP3801's final battery voltage should be programmed to a higher voltage than the maximum expected charging voltage. Doing so prevents interference with the NiCd/NiMH charging, yet still provides a limited output voltage in case the battery is removed. Meanwhile, the ADP3801 maintains a tightly regulated charge current.

If the battery has been identified as a Li-Ion battery, then the ADP3801 is used to terminate charge. The μC should monitor the $\overline{EOC}$ pin for the charge completion signal. In some cases, the charge is continued for 30-60 minutes after $\overline{EOC}$ to top off the battery. If this is desired, the timer function should be started upon receiving the $\overline{EOC}$. After the allotted time, the ADP3801 should be placed in shutdown to prevent constant trickle charging. By using the high accuracy final battery voltage limit of the ADP3801, the circuit can guarantee safe Li-Ion charging without requiring an expensive reference and amplifier.

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SECTION 6

TEMPERATURE SENSORS

- Thermocouple Principles and Cold-Junction Compensation
- Resistance Temperature Detectors (RTDs)
- Thermistors
- Semiconductor Temperature Sensors

SECTION 6
TEMPERATURE SENSORS
Walt Kester

INTRODUCTION

Measurement of temperature is critical in modern electronic devices, especially expensive laptop computers and other portable devices with densely packed circuits which dissipate considerable power in the form of heat. Knowledge of system temperature can also be used to control battery charging as well as prevent damage to expensive microprocessors.

Compact high power portable equipment often has fan cooling to maintain junction temperatures at proper levels. In order to conserve battery life, the fan should only operate when necessary. Accurate control of the fan requires a knowledge of critical temperatures from the appropriate temperature sensor.

APPLICATIONS OF TEMPERATURE SENSORS

- **Monitoring**
  - **Portable Equipment**
  - **CPU Temperature**
  - **Battery Temperature**
  - **Ambient Temperature**
- **Compensation**
  - **Oscillator Drift in Cellular Phones**
  - **Thermocouple Cold-Junction Compensation**
- **Control**
  - **Battery Charging**
  - **Process Control**

Figure 6.1

Accurate temperature measurements are required in many other measurement systems such as process control and instrumentation applications. In most cases, because of low-level nonlinear outputs, the sensor output must be properly conditioned and amplified before further processing can occur.

Except for IC sensors, all temperature sensors have nonlinear transfer functions. In the past, complex analog conditioning circuits were designed to correct for the sensor nonlinearity. These circuits often required manual calibration and precision resistors to achieve the desired accuracy. Today, however, sensor outputs may be

digitized directly by high resolution ADCs. Linearization and calibration is then performed digitally, thereby reducing cost and complexity.

Resistance Temperature Devices (RTDs) are accurate, but require excitation current and are generally used in bridge circuits. Thermistors have the most sensitivity but are the most non-linear. However, they are popular in portable applications such as measurement of battery temperature and other critical temperatures in a system.

Modern semiconductor temperature sensors offer high accuracy and high linearity over an operating range of about –55°C to +150°C. Internal amplifiers can scale the output to convenient values, such as 10mV/°C. They are also useful in cold-junction-compensation circuits for wide temperature range thermocouples. Semiconductor temperature sensors can be integrated into multi-function ICs which perform a number of other hardware monitoring functions.

Figure 6.2 lists the most popular types of temperature transducers and their characteristics.

TYPES OF TEMPERATURE SENSORS

THERMOCOUPLE	RTD	THERMISTOR	SEMICONDUCTOR
Widest Range: –184°C to +2300°C	Range: –200°C to +850°C	Range: 0°C to +100°C	Range: –55°C to +150°C
High Accuracy and Repeatability	Fair Linearity	Poor Linearity	Linearity: 1°C Accuracy: 1°C
Needs Cold Junction Compensation	Requires Excitation	Requires Excitation	Requires Excitation
Low-Voltage Output	Low Cost	High Sensitivity	10mV/K, 20mV/K, or 1µA/K Typical Output

Figure 6.2

THERMOCOUPLE PRINCIPLES AND COLD-JUNCTION COMPENSATION

Thermocouples are small, rugged, relatively inexpensive, and operate over the widest range of all temperature sensors. They are especially useful for making measurements at extremely high temperatures (up to +2300°C) in hostile environments. They produce only millivolts of output, however, and require precision amplification for further processing. They also require cold-junction-compensation (CJC) techniques which will be discussed shortly. They are more linear than many other sensors, and their non-linearity has been well characterized. Some common thermocouples are shown in Figure 6.3. The most common metals

used are Iron, Platinum, Rhodium, Rhenium, Tungsten, Copper, Alumel (composed of Nickel and Aluminum), Chromel (composed of Nickel and Chromium) and Constantan (composed of Copper and Nickel).

COMMON THERMOCOUPLES

JUNCTION MATERIALS	TYPICAL USEFUL RANGE (°C)	NOMINAL SENSITIVITY (μV/°C)	ANSI DESIGNATION
Platinum (6%)/ Rhodium-Platinum (30%)/Rhodium	38 to 1800	7.7	B
Tungsten (5%)/Rhenium - Tungsten (26%)/Rhenium	0 to 2300	16	C
Chromel - Constantan	0 to 982	76	E
Iron - Constantan	0 to 760	55	J
Chromel - Alumel	–184 to 1260	39	K
Platinum (13%)/Rhodium-Platinum	0 to 1593	11.7	R
Platinum (10%)/Rhodium-Platinum	0 to 1538	10.4	S
Copper-Constantan	–184 to 400	45	T

Figure 6.3

Figure 6.4 shows the voltage-temperature curves of three commonly used thermocouples, referred to a 0°C fixed-temperature reference junction. Of the thermocouples shown, Type J thermocouples are the most sensitive, producing the largest output voltage for a given temperature change. On the other hand, Type S thermocouples are the least sensitive. These characteristics are very important to consider when designing signal conditioning circuitry in that the thermocouples' relatively low output signals require low-noise, low-drift, high-gain amplifiers.

To understand thermocouple behavior, it is necessary to consider the non-linearities in their response to temperature differences. Figure 6.4 shows the relationships between sensing junction temperature and voltage output for a number of thermocouple types (in all cases, the reference *cold* junction is maintained at 0°C). It is evident that the responses are not quite linear, but the nature of the non-linearity is not so obvious.

Figure 6.5 shows how the Seebeck coefficient (the *change* of output voltage with *change* of sensor junction temperature - i.e., the first derivative of output with respect to temperature) varies with sensor junction temperature (we are still considering the case where the reference junction is maintained at 0°C).

When selecting a thermocouple for making measurements over a particular range of temperature, we should choose a thermocouple whose Seebeck coefficient varies as little as possible over that range.

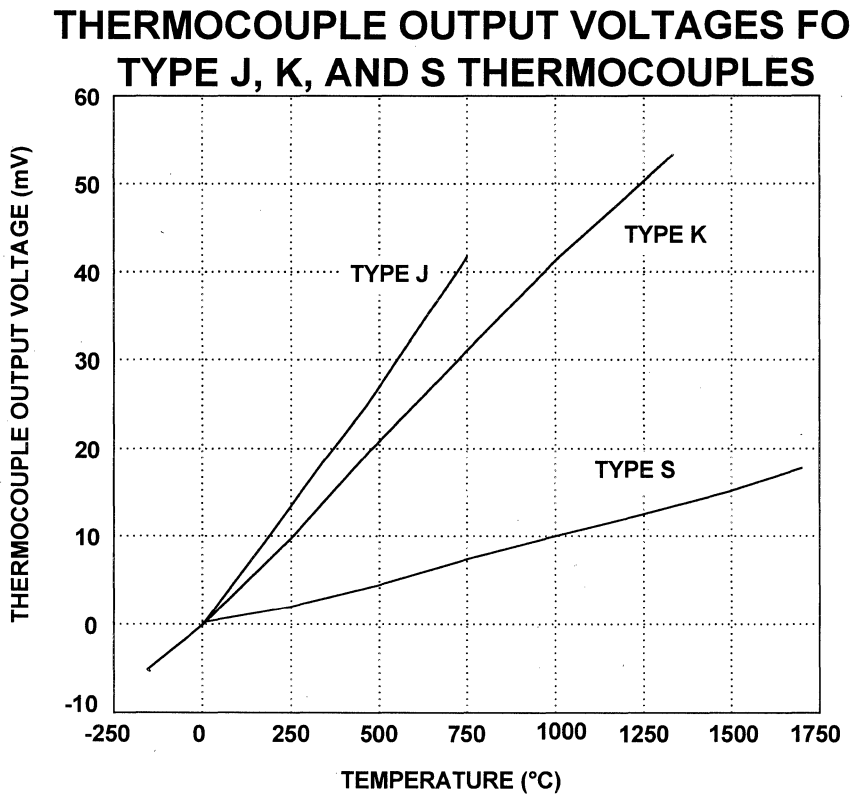


Figure 6.4

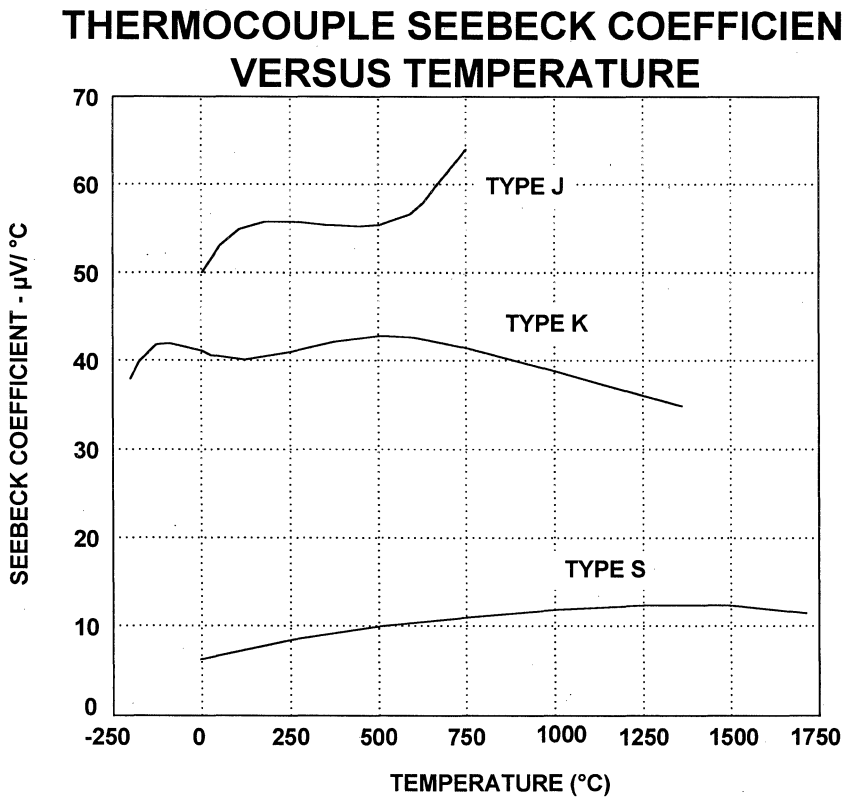


Figure 6.5

For example, a Type J thermocouple has a Seebeck coefficient which varies by less than 1μV/°C between 200 and 500°C, which makes it ideal for measurements in this range.

Presenting these data on thermocouples serves two purposes: First, Figure 6.4 illustrates the range and sensitivity of the three thermocouple types so that the system designer can, at a glance, determine that a Type S thermocouple has the widest useful temperature range, but a Type J thermocouple is more sensitive. Second, the Seebeck coefficients provide a quick guide to a thermocouple's linearity. Using Figure 6.5, the system designer can choose a Type K thermocouple for its linear Seebeck coefficient over the range of 400°C to 800°C or a Type S over the range of 900°C to 1700°C. The behavior of a thermocouple's Seebeck coefficient is important in applications where variations of temperature rather than absolute magnitude are important. These data also indicate what performance is required of the associated signal conditioning circuitry.

To use thermocouples successfully we must understand their basic principles. Consider the diagrams in Figure 6.6.

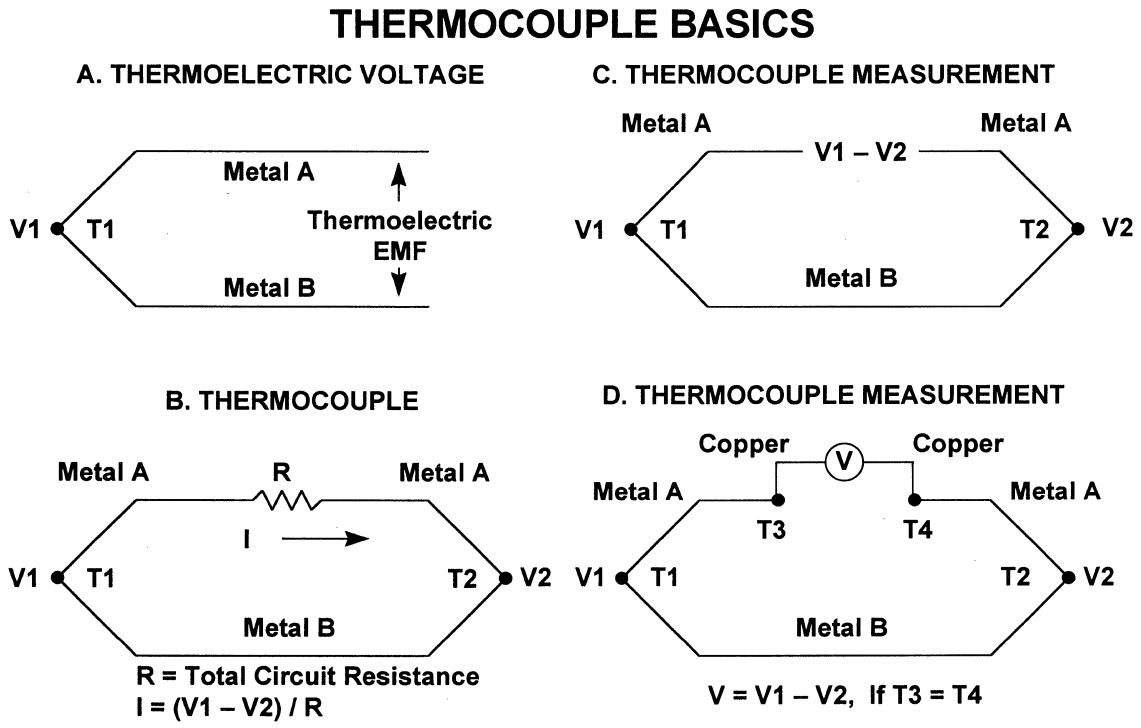


Figure 6.6

If we join two dissimilar metals at any temperature above absolute zero, there will be a potential difference between them (their "thermoelectric e.m.f." or "contact potential") which is a function of the temperature of the junction (Figure 6.6A). If we join the two wires at two places, two junctions are formed (Figure 6.6B). If the two junctions are at different temperatures, there will be a net e.m.f. in the circuit, and a current will flow determined by the e.m.f. and the total resistance in the circuit (Figure 6.6B). If we break one of the wires, the voltage across the break will

be equal to the net thermoelectric e.m.f. of the circuit, and if we measure this voltage, we can use it to calculate the temperature difference between the two junctions (Figure 6.6C). *We must always remember that a thermocouple measures the temperature difference between two junctions, not the absolute temperature at one junction.* We can only measure the temperature at the measuring junction if we know the temperature of the other junction (often called the "reference" junction or the "cold" junction).

But it is not so easy to measure the voltage generated by a thermocouple. Suppose that we attach a voltmeter to the circuit in Figure 6.6C (Figure 6.6D). The wires attached to the voltmeter will form further thermojunctions where they are attached. If both these additional junctions are at the same temperature (it does not matter what temperature), then the "Law of Intermediate Metals" states that they will make no net contribution to the total e.m.f. of the system. If they are at different temperatures, they will introduce errors. Since *every pair of dissimilar metals in contact generates a thermoelectric e.m.f.* (including copper/solder, kovar/copper [kovar is the alloy used for IC leadframes] and aluminum/kovar [at the bond inside the IC]), it is obvious that in practical circuits the problem is even more complex, and it is necessary to take extreme care to ensure that all the junction pairs in the circuitry around a thermocouple, except the measurement and reference junctions themselves, are at the same temperature.

Thermocouples generate a voltage, albeit a very small one, and do not require excitation. As shown in Figure 6.6D, however, two junctions (T1, the measurement junction and T2, the reference junction) are involved. If T2 = T1, then V2 = V1, and the output voltage V = 0. Thermocouple output voltages are often defined with a reference junction temperature of 0°C (hence the term *cold* or *ice point* junction), so the thermocouple provides an output voltage of 0V at 0°C. To maintain system accuracy, the reference junction must therefore be at a well-defined temperature (but not necessarily 0°C). A conceptually simple approach to this need is shown in Figure 6.7. Although an ice/water bath is relatively easy to define, it is quite inconvenient to maintain.

Today an ice-point reference, and its inconvenient ice/water bath, is generally replaced by electronics. A temperature sensor of another sort (often a semiconductor sensor, sometimes a thermistor) measures the temperature of the cold junction and is used to inject a voltage into the thermocouple circuit which compensates for the difference between the actual cold junction temperature and its ideal value (usually 0°C) as shown in Figure 6.8. Ideally, the compensation voltage should be an exact match for the difference voltage required, which is why the diagram gives the voltage as f(T2) (a *function* of T2) rather than KT2, where K is a simple constant. In practice, since the cold junction is rarely more than a few tens of degrees from 0°C, and generally varies by little more than ±10°C, a linear approximation (V=KT2) to the more complex reality is sufficiently accurate and is what is often used. (The expression for the output voltage of a thermocouple with its measuring junction at T°C and its reference at 0°C is a polynomial of the form $V = K_1T + K_2T^2 + K_3T^3 + ...$, but the values of the coefficients K_2, K_3, etc. are very small for most common types of thermocouple. References 8 and 9 give the values of these coefficients for a wide range of thermocouples.)

CLASSICAL COLD-JUNCTION COMPENSATION USING AN ICE-POINT (0°C) REFERENCE JUNCTION

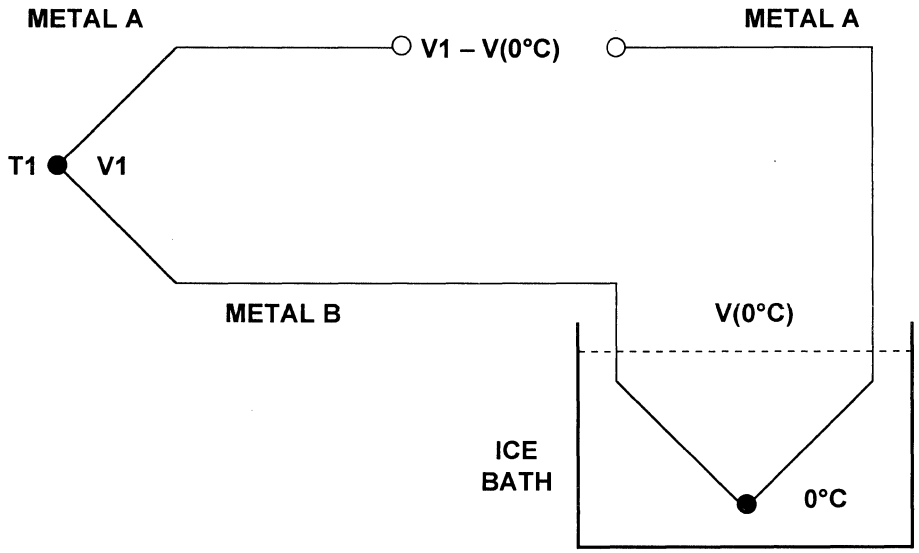
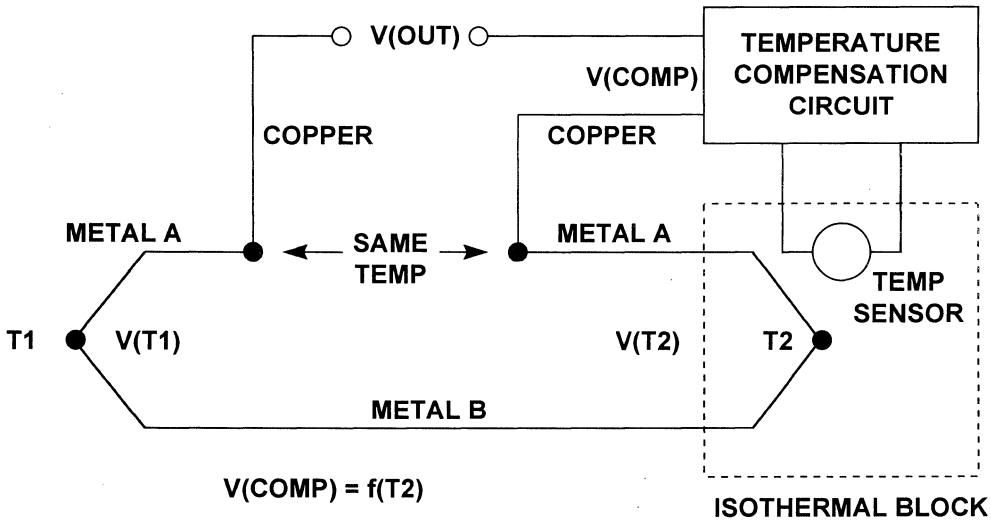


Figure 6.7

USING A TEMPERATURE SENSOR FOR COLD-JUNCTION COMPENSATION



V(COMP) = f(T2)

V(OUT) = V(T1) – V(T2) + V(COMP)

IF V(COMP) = V(T2) – V(0°C), THEN

V(OUT) = V(T1) – V(0°C)

Figure 6.8

When electronic cold-junction compensation is used, it is common practice to eliminate the additional thermocouple wire and terminate the thermocouple leads in the isothermal block in the arrangement shown in Figure 6.9. The Metal A-Copper and the Metal B-Copper junctions, if at the same temperature, are equivalent to the Metal A-Metal B thermocouple junction in Figure 6.8.

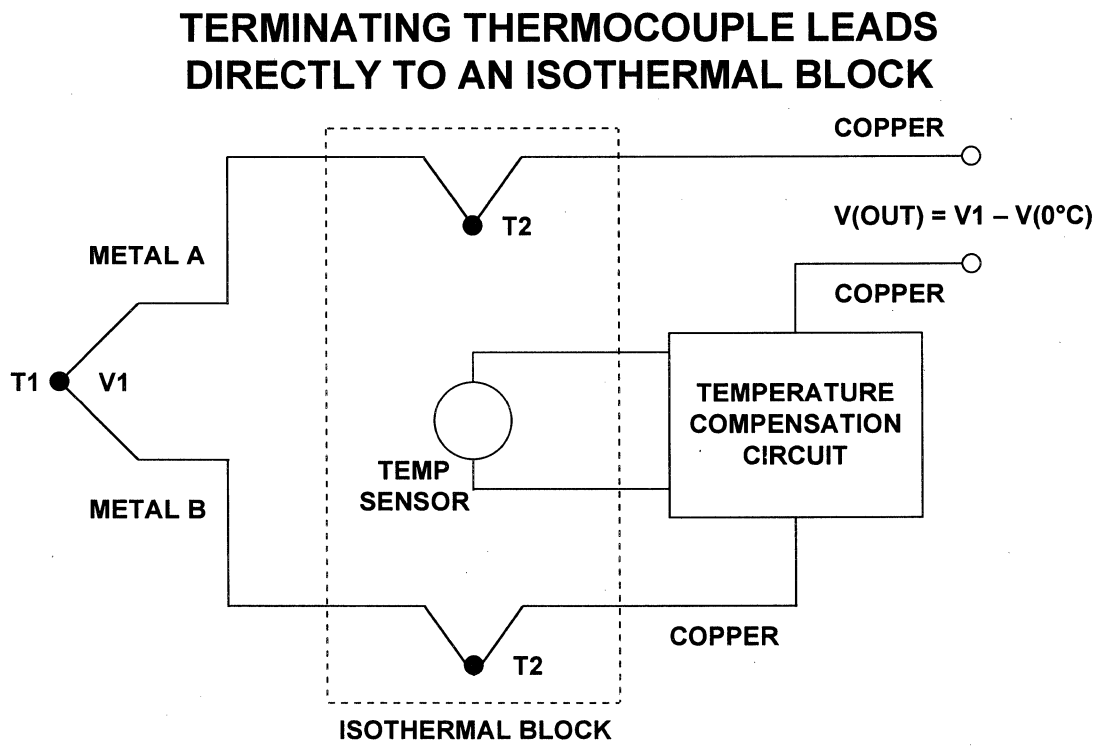


Figure 6.9

The circuit in Figure 6.10 conditions the output of a Type K thermocouple, while providing cold-junction compensation, for temperatures between 0°C and 250°C. The circuit operates from single +3.3V to +12V supplies and has been designed to produce an output voltage transfer characteristic of 10mV/°C.

A Type K thermocouple exhibits a Seebeck coefficient of approximately 41μV/°C; therefore, at the cold junction, the TMP35 voltage output sensor with a temperature coefficient of 10mV/°C is used with R1 and R2 to introduce an opposing cold-junction temperature coefficient of –41μV/°C. This prevents the isothermal, cold-junction connection between the circuit's printed circuit board traces and the thermocouple's wires from introducing an error in the measured temperature. This compensation works extremely well for circuit ambient temperatures in the range of 20°C to 50°C. Over a 250°C measurement temperature range, the thermocouple produces an output voltage change of 10.151mV. Since the required circuit's output full-scale voltage change is 2.5V, the gain of the circuit is set to 246.3. Choosing R4 equal to 4.99kΩ sets R5 equal to 1.22MΩ. Since the closest 1% value for R5 is 1.21MΩ, a 50kΩ potentiometer is used with R5 for fine trim of the full-scale output voltage. Although the OP193 is a single-supply op amp, its output stage is not rail-to-rail, and will only go down to about 0.1V above ground. For this reason, R3 is added to the circuit to supply an output offset voltage of about 0.1V for a nominal supply

voltage of 5V. This offset (10°C) must be subtracted when making measurements referenced to the OP193 output. R3 also provides an open thermocouple detection, forcing the output voltage to greater than 3V should the thermocouple open. Resistor R7 balances the DC input impedance of the OP193, and the 0.1µF film capacitor reduces noise coupling into its non-inverting input.

USING A TEMPERATURE SENSOR FOR COLD-JUNCTION COMPENSATION (TMP35)

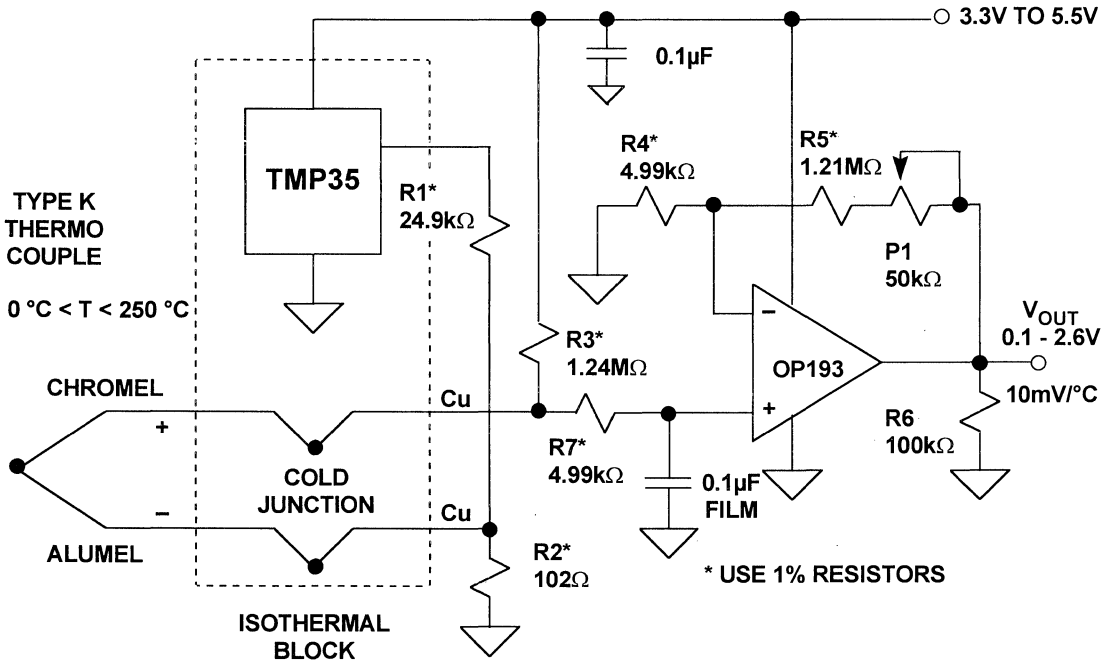


Figure 6.10

The AD594/AD595 is a complete instrumentation amplifier and thermocouple cold junction compensator on a monolithic chip (see Figure 6.11). It combines an ice point reference with a precalibrated amplifier to provide a high level (10mV/°C) output directly from the thermocouple signal. Pin-strapping options allow it to be used as a linear amplifier-compensator or as a switched output set-point controller using either fixed or remote set-point control. It can be used to amplify its compensation voltage directly, thereby becoming a stand-alone Celsius transducer with 10mV/°C output. In such applications it is very important that the IC chip is at the same temperature as the cold junction of the thermocouple, which is usually achieved by keeping the two in close proximity and isolated from any heat sources.

The AD594/AD595 includes a thermocouple failure alarm that indicates if one or both thermocouple leads open. The alarm output has a flexible format which includes TTL drive capability. The device can be powered from a single-ended supply (which may be as low as +5V), but by including a negative supply, temperatures below 0°C can be measured. To minimize self-heating, an unloaded AD594/AD595 will operate with a supply current of 160µA, but is also capable of delivering ±5mA to a load.

The AD594 is precalibrated by laser wafer trimming to match the characteristics of type J (iron/constantan) thermocouples, and the AD595 is laser trimmed for type K (chromel/alumel). The temperature transducer voltages and gain control resistors are available at the package pins so that the circuit can be recalibrated for other thermocouple types by the addition of resistors. These terminals also allow more precise calibration for both thermocouple and thermometer applications. The AD594/AD595 is available in two performance grades. The C and the A versions have calibration accuracies of ±1°C and ±3°C, respectively. Both are designed to be used with cold junctions between 0 to +50°C. The circuit shown in Figure 6.11 will provide a direct output from a type J thermocouple (AD594) or a type K thermocouple (AD595) capable of measuring 0 to +300°C.

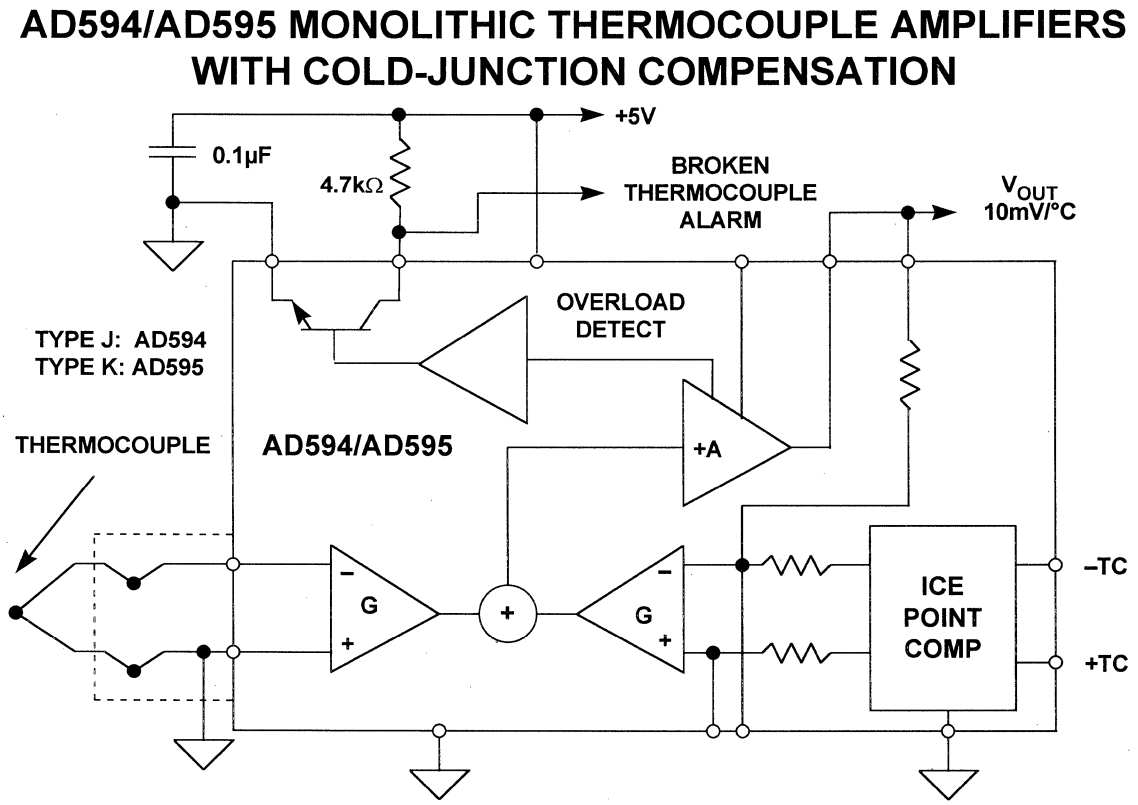


Figure 6.11

The AD596/AD597 are monolithic set-point controllers which have been optimized for use at elevated temperatures as are found in oven control applications. The device cold-junction compensates and amplifies a type J/K thermocouple to derive an internal signal proportional to temperature. They can be configured to provide a voltage output (10mV/°C) directly from type J/K thermocouple signals. The device is packaged in a 10-pin metal can and is trimmed to operate over an ambient range from +25°C to +100°C. The AD596 will amplify thermocouple signals covering the entire –200°C to +760°C temperature range recommended for type J thermocouples while the AD597 can accommodate –200°C to +1250°C type K inputs. They have a calibration accuracy of ±4°C at an ambient temperature of 60°C and an ambient temperature stability specification of 0.05°C/°C from +25°C to +100°C.

None of the thermocouple amplifiers previously described compensate for thermocouple non-linearity, they only provide conditioning and voltage gain. High resolution ADCs such as the AD77XX family can be used to digitize the thermocouple output directly, allowing a microcontroller to perform the transfer function linearization as shown in Figure 6.12. The two multiplexed inputs to the ADC are used to digitize the thermocouple voltage and the cold-junction temperature sensor outputs directly. The input PGA gain is programmable from 1 to 128, and the ADC resolution is between 16 and 22 bits (depending upon the particular ADC selected). The microcontroller performs both the cold-junction compensation and the linearization arithmetic.

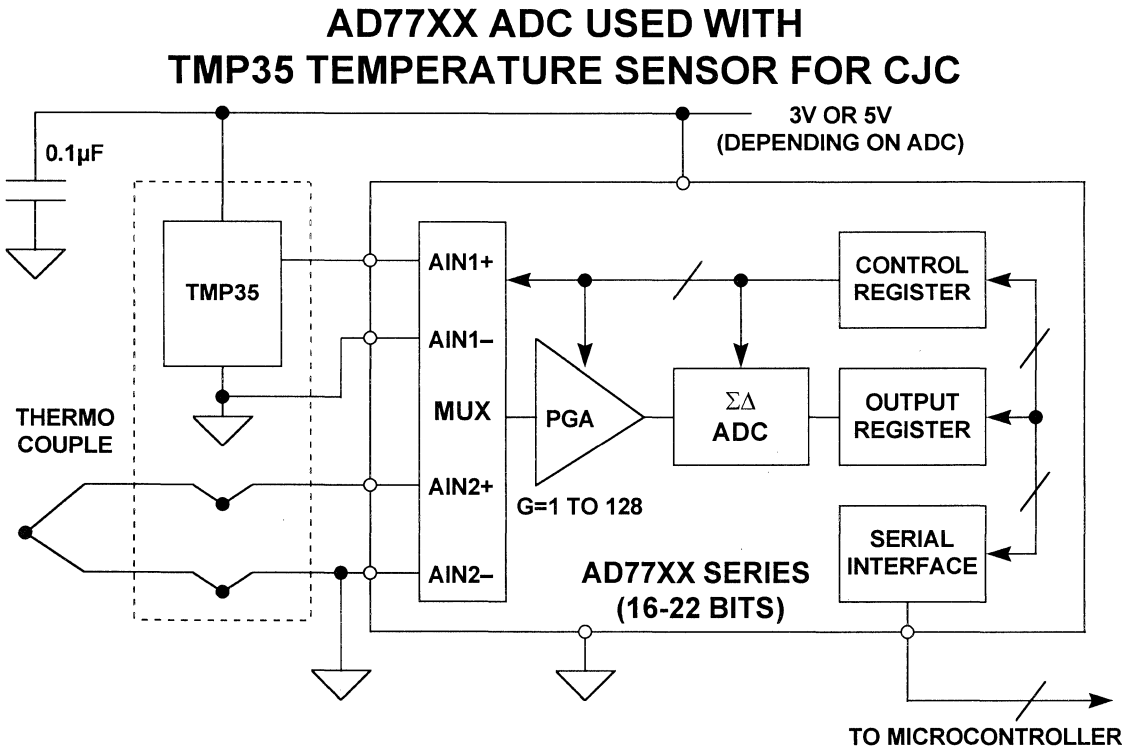


Figure 6.12

RESISTANCE TEMPERATURE DETECTORS (RTDS)

The Resistance Temperature Detector, or the RTD, is a sensor whose resistance changes with temperature. Typically built of a platinum (Pt) wire wrapped around a ceramic bobbin, the RTD exhibits behavior which is more accurate and more linear over wide temperature ranges than a thermocouple. Figure 6.13 illustrates the temperature coefficient of a 100Ω RTD and the Seebeck coefficient of a Type S thermocouple. Over the entire range (approximately –200°C to +850°C), the RTD is a more linear device. Hence, linearizing an RTD is less complex.

RESISTANCE TEMPERATURE DETECTORs (RTD)

- **Platinum (Pt) the Most Common**
- **100Ω, 1000Ω Standard Values**
- **Typical TC = 0.385% / °C,**
  0.385Ω / °C for 100Ω Pt RTD
- **Good Linearity - Better than Thermocouple,**
  Easily Compensated

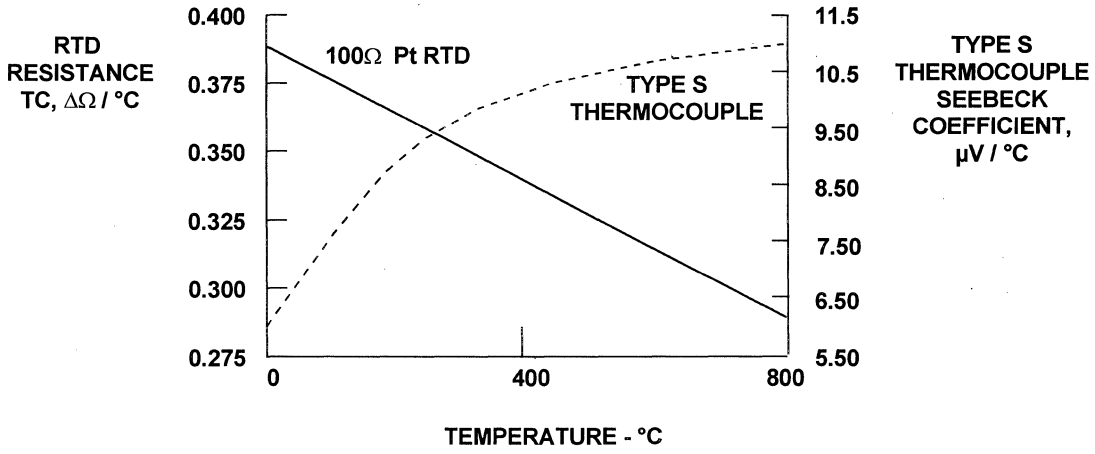


Figure 6.13

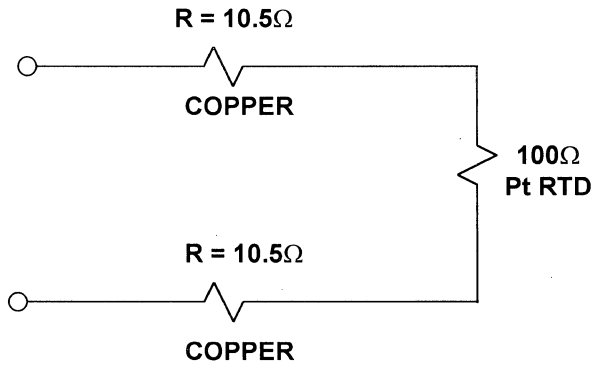
Unlike a thermocouple, however, an RTD is a passive sensor and requires current excitation to produce an output voltage. The RTD's low temperature coefficient of 0.385%/°C requires similar high-performance signal conditioning circuitry to that used by a thermocouple; however, the voltage drop across an RTD is much larger than a thermocouple output voltage. A system designer may opt for large value RTDs with higher output, but large-valued RTDs exhibit slow response times. Furthermore, although the cost of RTDs is higher than that of thermocouples, they use copper leads, and thermoelectric effects from terminating junctions do not affect their accuracy. And finally, because their resistance is a function of the absolute temperature, RTDs require no cold-junction compensation.

Caution must be exercised using current excitation because the current through the RTD causes heating. This self-heating changes the temperature of the RTD and appears as a measurement error. Hence, careful attention must be paid to the design of the signal conditioning circuitry so that self-heating is kept below 0.5°C. Manufacturers specify self-heating errors for various RTD values and sizes in still and in moving air. To reduce the error due to self-heating, the minimum current should be used for the required system resolution, and the largest RTD value chosen that results in acceptable response time.

Another effect that can produce measurement error is voltage drop in RTD lead wires. This is especially critical with low-value 2-wire RTDs because the temperature coefficient and the absolute value of the RTD resistance are both small. If the RTD is located a long distance from the signal conditioning circuitry, then the lead resistance can be ohms or tens of ohms, and a small amount of lead resistance

can contribute a significant error to the temperature measurement. To illustrate this point, let us assume that a 100Ω platinum RTD with 30-gauge copper leads is located about 100 feet from a controller's display console. The resistance of 30-gauge copper wire is 0.105Ω/ft, and the two leads of the RTD will contribute a total 21Ω to the network which is shown in Figure 6.14. This additional resistance will produce a 55°C error in the measurement! The leads' temperature coefficient can contribute an additional, and possibly significant, error to the measurement. To eliminate the effect of the lead resistance, a 4-wire technique is used.

A 100Ω Pt RTD WITH 100 FEET OF 30-GAUGE LEAD WIRES



RESISTANCE TC OF COPPER = 0.40%/°C @ 20°C

RESISTANCE TC OF Pt RTD = 0.385%/ °C @ 20°C

Figure 6.14

In Figure 6.15, a 4-wire, or Kelvin, connection is made to the RTD. A constant current is applied though the FORCE leads of the RTD, and the voltage across the RTD itself is measured remotely via the SENSE leads. The measuring device can be a DVM or an instrumentation amplifier, and high accuracy can be achieved provided that the measuring device exhibits high input impedance and/or low input bias current. Since the SENSE leads do not carry appreciable current, this technique is insensitive to lead wire length. Sources of errors are the stability of the constant current source and the input impedance and/or bias currents in the amplifier or DVM.

RTDs are generally configured in a four-resistor bridge circuit. The bridge output is amplified by an instrumentation amplifier for further processing. However, high resolution measurement ADCs such as the AD77XX series allow the RTD output to be digitized directly. In this manner, linearization can be performed digitally, thereby easing the analog circuit requirements.

FOUR-WIRE OR KELVIN CONNECTION TO Pt RTD FOR ACCURATE MEASUREMENTS

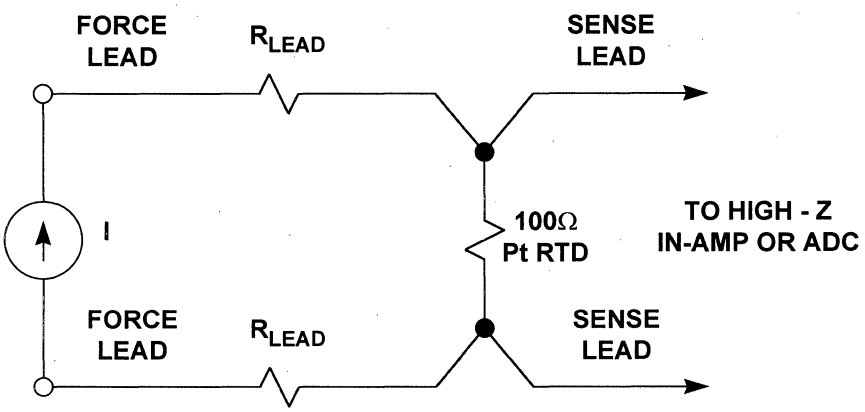


Figure 6.15

Figure 6.16 shows a 100Ω Pt RTD driven with a 400μA excitation current source. The output is digitized by one of the AD77XX series ADCs. Note that the RTD excitation current source also generates the 2.5V reference voltage for the ADC via the 6.25kΩ resistor. Variations in the excitation current do not affect the circuit accuracy, since both the input voltage and the reference voltage vary ratiometrically with the excitation current. However, the 6.25kΩ resistor must have a low temperature coefficient to avoid errors in the measurement. The high resolution of the ADC and the input PGA (gain of 1 to 128) eliminates the need for additional conditioning circuits.

The ADT70 is a complete Pt RTD signal conditioner which provides an output voltage of 5mV/°C when using a 1kΩ RTD (see Figure 6.17). The Pt RTD and the 1kΩ reference resistor are both excited with 1mA matched current sources. This allows temperature measurements to be made over a range of approximately –50°C to +800°C.

The ADT70 contains the two matched current sources, a precision rail-to-rail output instrumentation amplifier, a 2.5V reference, and an uncommitted rail-to-rail output op amp. The ADT71 is the same as the ADT70 except the internal voltage reference is omitted. A shutdown function is included for battery powered equipment that reduces the quiescent current from 3mA to 10μA. The gain or full-scale range for the Pt RTD and ADT70 system is set by a precision external resistor connected to the instrumentation amplifier. The uncommitted op amp may be used for scaling the internal voltage reference, providing a "Pt RTD open" signal or "over temperature" warning, providing a heater switching signal, or other external conditioning determined by the user. The ADT70 is specified for operation from –40°C to +125°C and is available in 20-pin DIP and SOIC packages.

INTERFACING A Pt RTD TO A HIGH RESOLUTION ADC

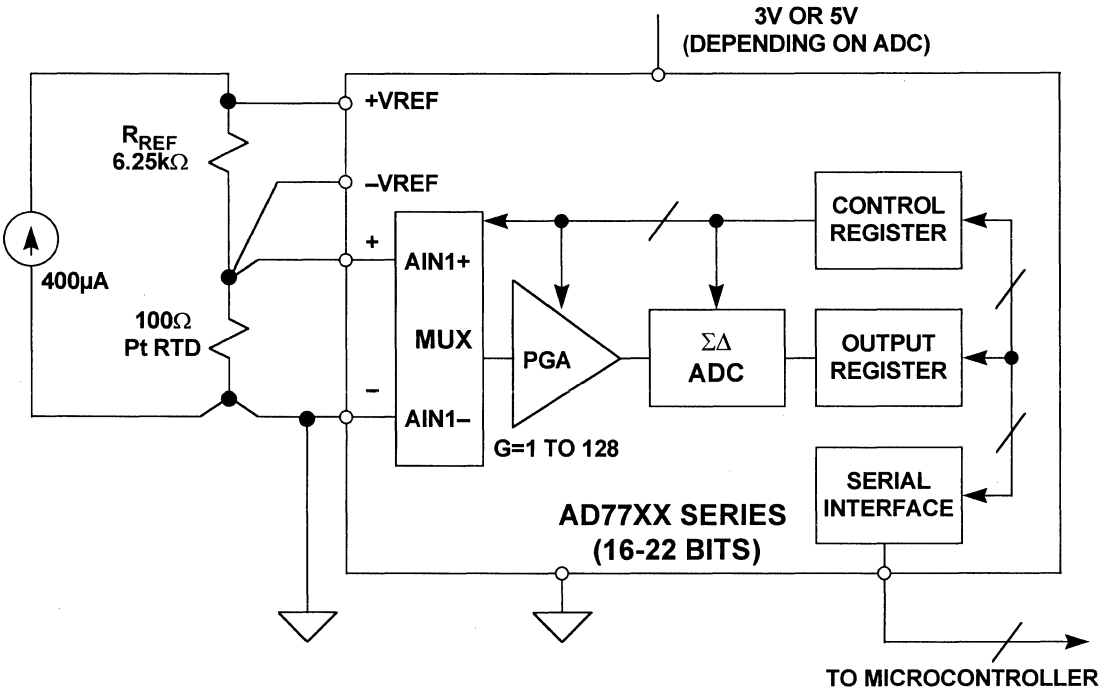


Figure 6.16

CONDITIONING THE PLATINUM RTD USING THE ADT70

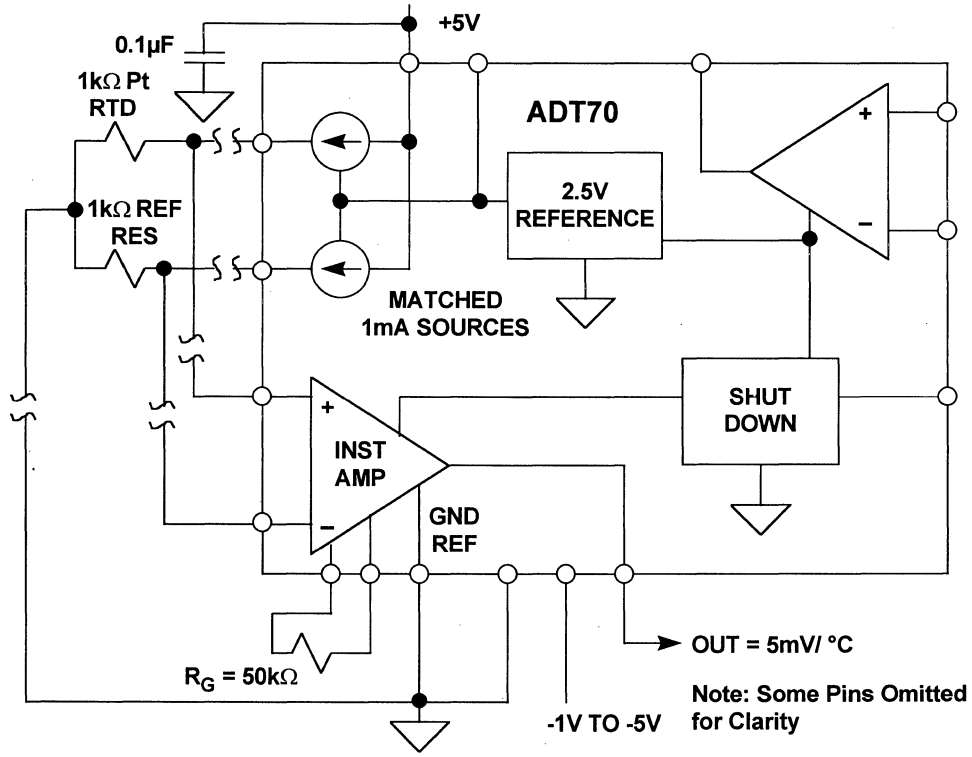


Figure 6.17

THERMISTORS

Similar in function to the RTD, thermistors are low-cost temperature-sensitive resistors and are constructed of solid semiconductor materials which exhibit a positive or negative temperature coefficient. Although positive temperature coefficient devices are available, the most commonly used thermistors are those with a negative temperature coefficient. Figure 6.18 shows the resistance-temperature characteristic of a commonly used NTC (Negative Temperature Coefficient) thermistor. The thermistor is highly non-linear and, of the three temperature sensors discussed, is the most sensitive.

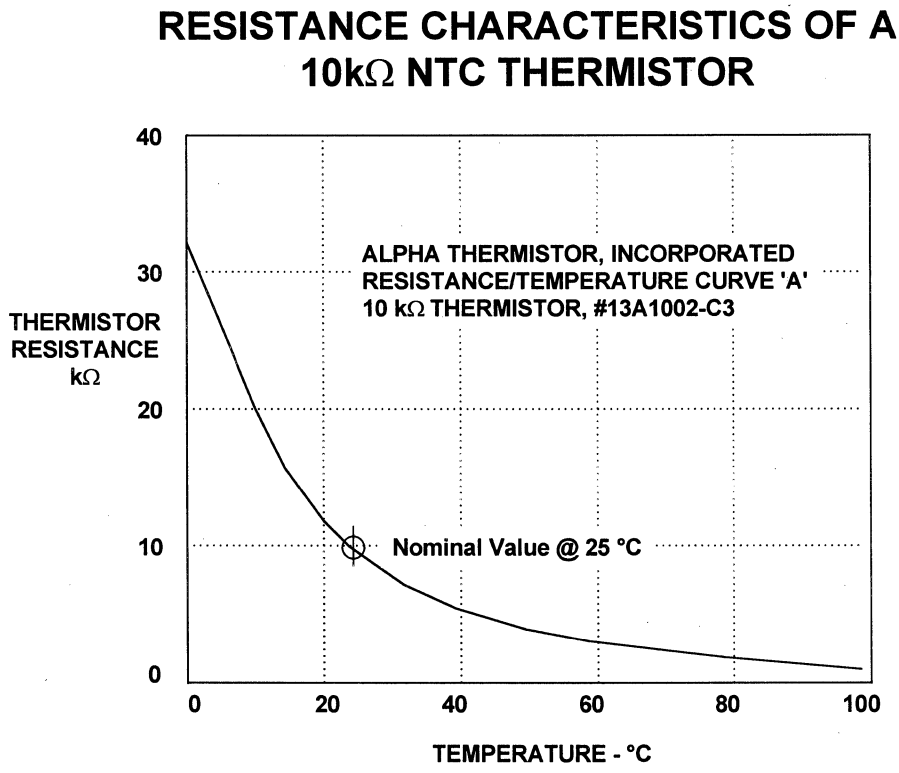


Figure 6.18

The thermistor's high sensitivity (typically, – 44,000ppm/°C at 25°C, as shown in Figure 6.19), allows it to detect minute variations in temperature which could not be observed with an RTD or thermocouple. This high sensitivity is a distinct advantage over the RTD in that 4-wire Kelvin connections to the thermistor are not needed to compensate for lead wire errors. To illustrate this point, suppose a 10kΩ NTC thermistor, with a typical 25°C temperature coefficient of –44,000ppm/°C, were substituted for the 100Ω Pt RTD in the example given earlier, then a total lead wire resistance of 21Ω would generate less than 0.05°C error in the measurement. This is roughly a factor of 500 improvement in error over an RTD.

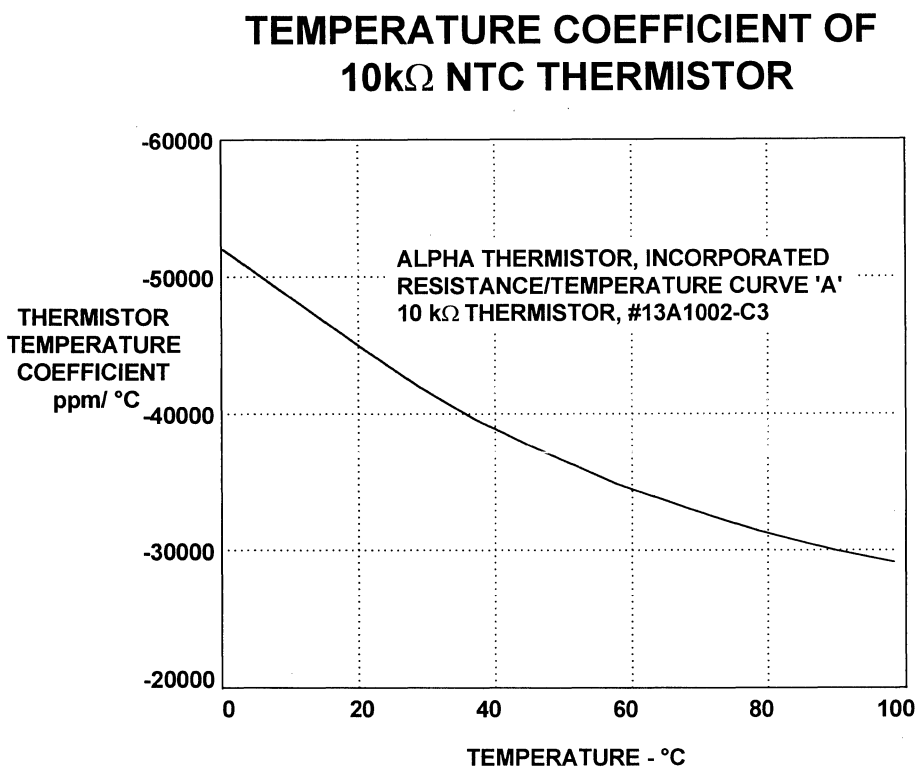


Figure 6.19

However, the thermistor's high sensitivity to temperature does not come without a price. As was shown in Figure 6.18, the temperature coefficient of thermistors does not decrease linearly with increasing temperature as it does with RTDs; therefore, linearization is required for all but the narrowest of temperature ranges. Thermistor applications are limited to a few hundred degrees at best because they are more susceptible to damage at high temperatures. Compared to thermocouples and RTDs, thermistors are fragile in construction and require careful mounting procedures to prevent crushing or bond separation. Although a thermistor's response time is short due to its small size, its small thermal mass makes it very sensitive to self-heating errors.

Thermistors are very inexpensive, highly sensitive temperature sensors. However, we have shown that a thermistor's temperature coefficient varies from –44,000 ppm/°C at 25°C to –29,000ppm/°C at 100°C. Not only is this non-linearity the largest source of error in a temperature measurement, it also limits useful applications to very narrow temperature ranges if linearization techniques are not used.

It is possible to use a thermistor over a wide temperature range only if the system designer can tolerate a lower sensitivity to achieve improved linearity. One approach to linearizing a thermistor is simply shunting it with a fixed resistor. Paralleling the thermistor with a fixed resistor increases the linearity significantly. As shown in Figure 6.20, the parallel combination exhibits a more linear variation with temperature compared to the thermistor itself. Also, the sensitivity of the combination still is high compared to a thermocouple or RTD. The primary

disadvantage to this technique is that linearization can only be achieved within a narrow range.

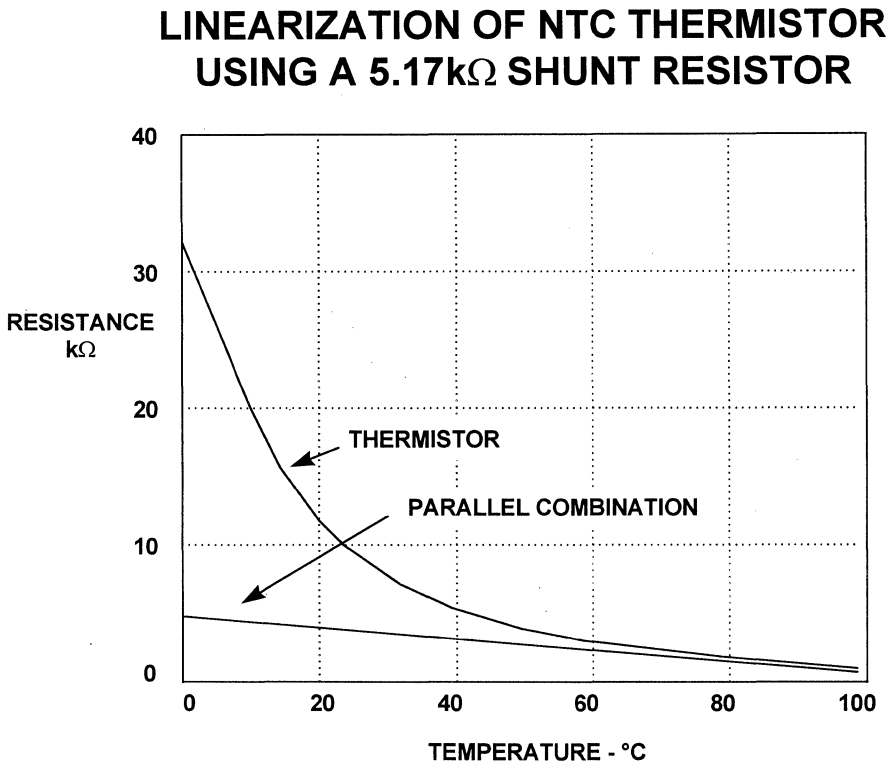


Figure 6.20

The value of the fixed resistor can be calculated from the following equation:

$$R = \frac{RT2 \cdot (RT1 + RT3) - 2 \cdot RT1 \cdot RT3}{RT1 + RT3 - 2 \cdot RT2},$$

where RT1 is the thermistor resistance at T1, the lowest temperature in the measurement range, RT3 is the thermistor resistance at T3, the highest temperature in the range, and RT2 is the thermistor resistance at T2, the midpoint, T2 = (T1 +T3)/2.

For a typical 10kΩ NTC thermistor, RT1 = 32,650Ω at 0°C, RT2 = 6,532Ω at 35°C, and RT3 = 1,752Ω at 70°C. This results in a value of 5.17kΩ for R. The accuracy needed in the signal conditioning circuitry depends on the linearity of the network. For the example given above, the network shows a non-linearity of – 2.3°C/ + 2.0 °C.

The output of the network can be applied to an ADC to perform further linearization as shown in Figure 6.21. Note that the output of the thermistor network has a slope of approximately –10mV/°C, which implies a 12-bit ADC has more than sufficient resolution.

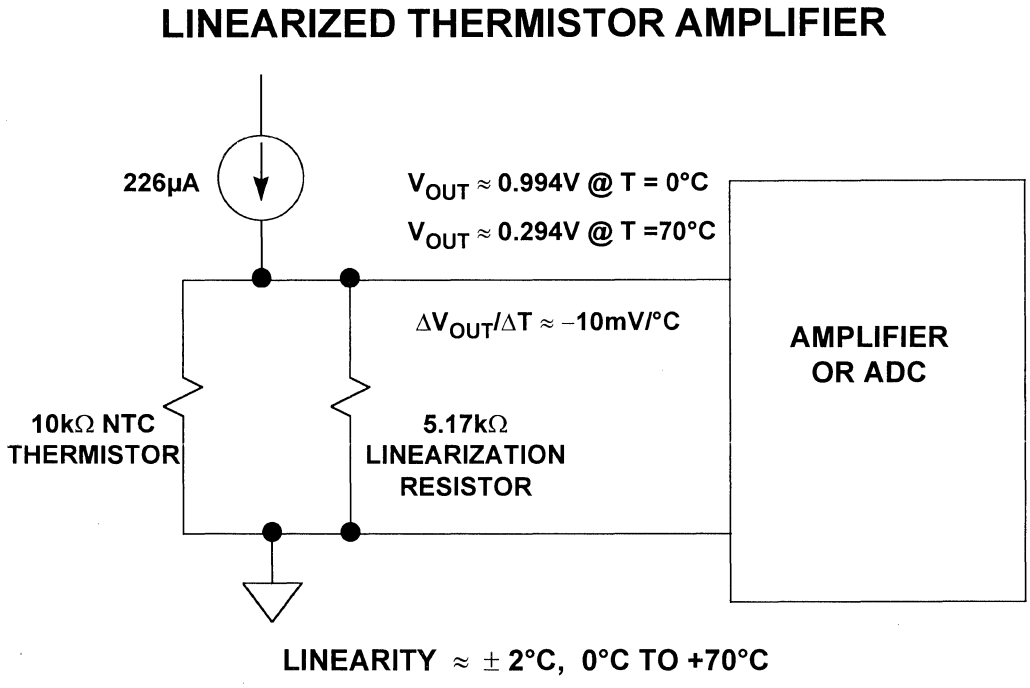


Figure 6.21

SEMICONDUCTOR TEMPERATURE SENSORS

Modern semiconductor temperature sensors offer high accuracy and high linearity over an operating range of about –55°C to +150°C. Internal amplifiers can scale the output to convenient values, such as 10mV/°C. They are also useful in cold-junction-compensation circuits for wide temperature range thermocouples.

All semiconductor temperature sensors make use of the relationship between a bipolar junction transistor's (BJT) base-emitter voltage to its collector current:

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right)$$

where k is Boltzmann's constant, T is the absolute temperature, q is the charge of an electron, and I_S is a current related to the geometry and the temperature of the transistors. (The equation assumes a voltage of at least a few hundred mV on the collector, and ignores Early effects.)

If we take N transistors identical to the first (see Figure 6.22) and allow the total current I_C to be shared equally among them, we find that the new base-emitter voltage is given by the equation

$$V_N = \frac{kT}{q} \ln\left(\frac{I_C}{N \cdot I_S}\right)$$

BASIC RELATIONSHIPS FOR SEMICONDUCTOR TEMPERATURE SENSORS

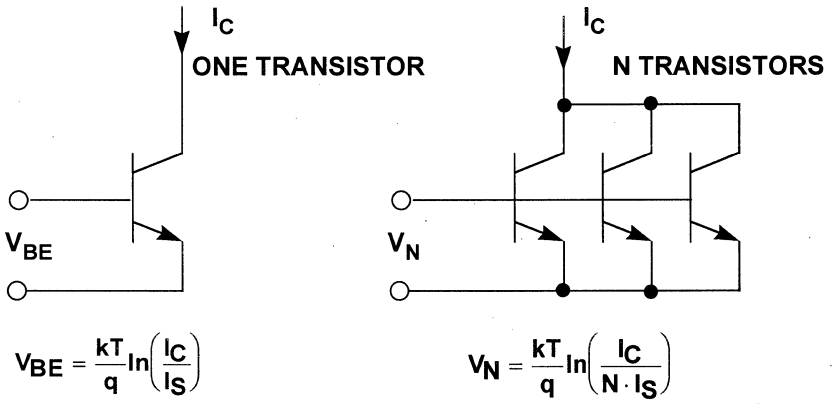


Figure 6.22

Neither of these circuits is of much use by itself because of the strongly temperature dependent current I_S, but if we have equal currents in one BJT and N similar BJTs then the expression for the *difference* between the two base-emitter voltages is proportional to absolute temperature and does not contain I_S.

$$V_{BE} - V_N = \frac{kT}{q} \ln\left(\frac{I_c}{I_S}\right) - \frac{kT}{q} \ln\left(\frac{I_c}{N \cdot I_S}\right)$$

$$V_{BE} - V_N = \frac{kT}{q} \left[\ln\left(\frac{I_c}{I_S}\right) - \ln\left(\frac{I_c}{N \cdot I_S}\right) \right]$$

$$V_{BE} - V_N = \frac{kT}{q} \ln\left[\left(\frac{I_c}{I_S}\right) \Big/ \left(\frac{I_c}{N \cdot I_S}\right) \right] = \frac{kT}{q} \ln(N)$$

The circuit shown in Figure 6.23 implements the above equation and is known as the "Brokaw Cell" (see Reference 10). The voltage $V_{BE} - V_N$ appears across resistor R2. The emitter current in Q2 is therefore $(V_{BE} - V_N)/R2$. The op amp's servo loop and the resistors, R, force the same current to flow through Q1. The Q1 and Q2 currents are equal and are summed and flow into resistor R1. The corresponding voltage developed across R1 is proportional to absolute temperature (PTAT) and given by:

$$V_{PTAT} = \frac{2R1(V_{BE} - V_N)}{R2} = 2\frac{R1}{R2}\frac{kT}{q}\ln(N).$$

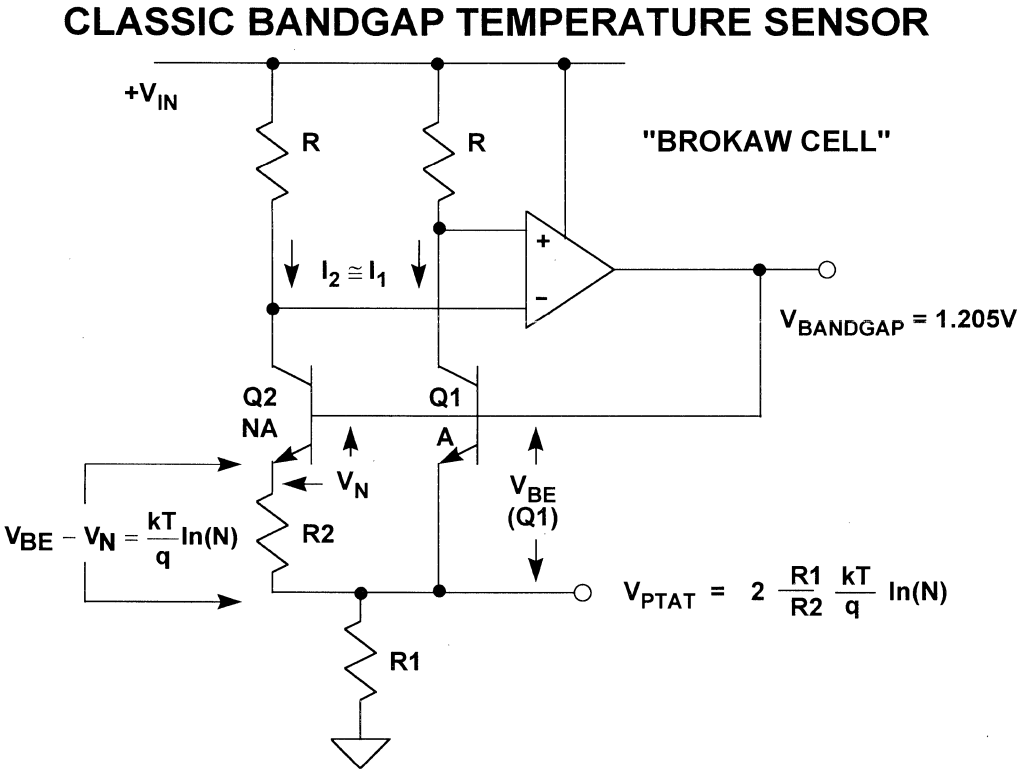


Figure 6.23

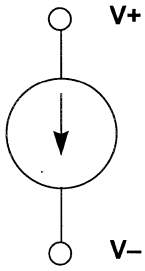
The bandgap cell reference voltage, $V_{BANDGAP}$, appears at the base of Q1 and is the sum of $V_{BE}(Q1)$ and V_{PTAT}. $V_{BE(Q1)}$ is complementary to absolute temperature (CTAT), and summing it with V_{PTAT} causes the bandgap voltage to be constant with respect to temperature (assuming proper choice of R1/R2 ratio and N to make the bandgap voltage equal to1.205V). This circuit is the basic *band-gap* temperature sensor, and is widely used in semiconductor temperature sensors.

6

Current and Voltage Output Temperature Sensors

The concepts used in the bandgap temperature sensor discussion above can be used as the basis for a variety of IC temperature sensors to generate either current or voltage outputs. The AD592 and TMP17 (see Figure 6.24) are current output sensors which have scale factors of 1μA/K. The sensors do not require external calibration and are available in several accuracy grades. The AD592 is available in three accuracy grades. The highest grade version (AD592CN) has a maximum error @ 25°C of ±0.5°C and ±1.0°C error from –25°C to +105°C. Linearity error is ±0.35°C. The TMP17 is available in two accuracy grades. The highest grade version (TMP17F) has a maximum error @ 25°C of ±2.5°C and ±3.5°C error from –40°C to +105°C. Typical linearity error is ±0.5°C. The AD592 is available in a TO-92 package and the TMP17 in an SO-8 package.

CURRENT OUTPUT SENSORS: AD592, TMP17



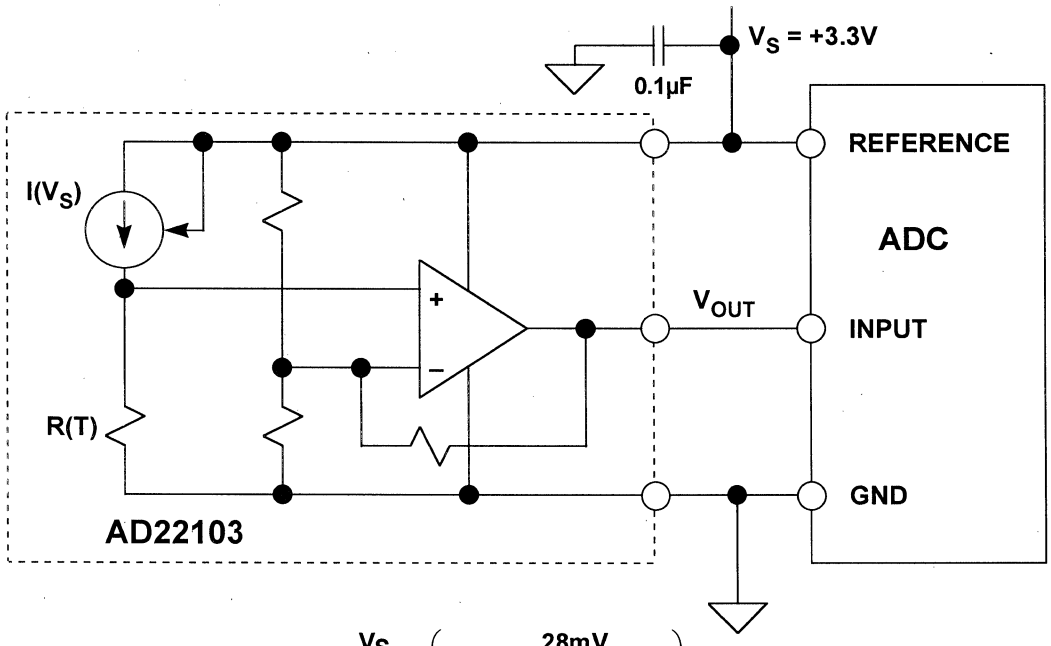
AD592: TO-92 PACKAGE

TMP17: SO-8 PACKAGE

- 1µA/K Scale Factor
- Nominal Output Current @ +25°C: 298.2µA
- Operation from 4V to 30V
- ±0.5°C Max Error @ 25°C, ±1.0°C Error Over Temp, ±0.1°C Typical Nonlinearity (AD592CN)
- ±2.5°C Max Error @ 25°C, ±3.5°C Error Over Temp, ±0.5°C Typical Nonlinearity (TMP17F)
- AD592 Specified from –25°C to +105°C
- TMP17 Specified from –40°C to +105°C

Figure 6.24

RATIOMETRIC VOLTAGE OUTPUT SENSORS



$$V_{OUT} = \frac{V_S}{3.3V} \times \left(0.25V + \frac{28mV}{°C} \times T_A\right)$$

Figure 6.25

In some cases, it is desirable for the output of a temperature sensor to be ratiometric with its supply voltage. The AD22103 (see Figure 6.25) has an output that is ratiometric with its supply voltage (nominally 3.3V) according to the equation:

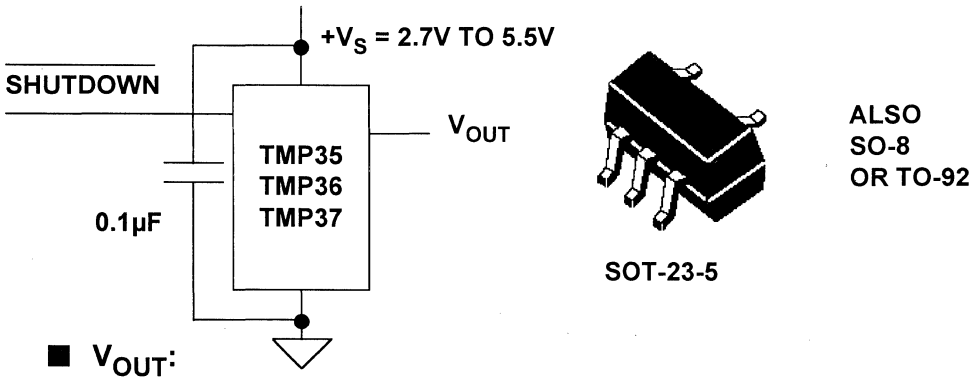
$$V_{OUT} = \frac{V_S}{3.3V} \times \left(0.25V + \frac{28mV}{°C} \times T_A \right).$$

The circuit shown in Figure 6.25 uses the AD22103 power supply as the reference to the ADC, thereby eliminating the need for a precision voltage reference. The AD22103 is specified over a range of 0°C to +100°C and has an accuracy better than ±2.5°C and a linearity better than ±0.5°C.

The TMP35/TMP36/TMP37 are low voltage (2.7V to 5.5V) SOT-23 (5-pin), SO-8, or TO-92 packaged voltage output temperature sensors with a 10mV/°C (TMP35/36) or 20mV/°C (TMP37) scale factor (see Figure 6.26). Supply current is below 50µA, providing very low self-heating (less than 0.1°C in still air). A shutdown feature is provided which reduces the current to 0.5µA.

The TMP35 provides a 250mV output at +25°C and reads temperature from +10°C to +125°C. The TMP36 is specified from –40°C to +125°C. and provides a 750mV output at 25°C. Both the TMP35 and TMP36 have an output scale factor of +10mV/°C. The TMP37 is intended for applications over the range +5°C to +100°C, and provides an output scale factor of 20mV/°C. The TMP37 provides a 500mV output at +25°C.

ABSOLUTE VOLTAGE OUTPUT SENSORS WITH SHUTDOWN

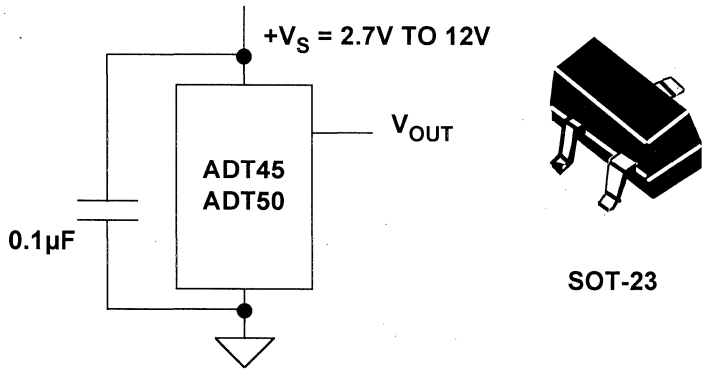


- **V_{OUT}:**
  - **TMP35, 250mV @ 25°C, 10mV/°C (+10°C to +125°C)**
  - **TMP36, 750mV @ 25°C, 10mV/°C (–40°C to +125°C)**
  - **TMP37, 500mV @ 25°C, 20mV/°C (+5°C to +100°C)**
- **±2°C Error Over Temp (Typical), ±0.5°C Non-Linearity (Typical)**
- **Specified –40°C to +125°C**
- **50µA Quiescent Current, 0.5µA in Shutdown Mode**

Figure 6.26

The ADT45/ADT50 are voltage output temperature sensors packaged in a SOT-23-3 package designed for an operating voltage of 2.7V to 12V (see Figure 6.27). The devices are specified over the range of –40°C to +125°C. The output scale factor for both devices is 10mV/°C. Typical accuracies are ±1°C at +25°C and ±2°C over the –40°C to +125°C range. The ADT45 provides a 250mV output at +25°C and is specified for temperature from 0°C to +100°C. The ADT50 provides a 750mV output at +25°C and is specified for temperature from –40°C to +125°C.

ADT45/ADT50 ABSOLUTE VOLTAGE OUTPUT SENSORS



- V_{OUT}:
  - ADT45, 250mV @ 25°C, 10mV/°C Scale Factor
  - ADT50, 750mV @ 25°C, 10mV/°C Scale Factor
- ±2°C Error Over Temp (Typical), ±0.5°C Non-Linearity (Typical)
- Specified –40°C to +125°C
- 60µA Quiescent Current

Figure 6.27

If the ADT45/ADT50 sensors are thermally attached and protected, they can be used in any temperature measurement application where the maximum temperature range of the medium is between –40°C to +125°C. Properly cemented or glued to the surface of the medium, these sensors will be within 0.01°C of the surface temperature. Caution should be exercised, as any wiring to the device can act as heat pipes, introducing errors if the surrounding air-surface interface is not isothermal. Avoiding this condition is easily achieved by dabbing the leads of the sensor and the hookup wires with a bead of thermally conductive epoxy. This will ensure that the ADT45/ADT50 die temperature is not affected by the surrounding air temperature.

In the SOT-23-3 package, the thermal resistance junction-to-case, θ_{JC}, is 180°C/W. The thermal resistance case-to-ambient, θ_{CA}, is the difference between θ_{JA} and θ_{JC}, and is determined by the characteristics of the thermal connection. With no air flow and the device soldered on a PC board, θ_{JA} is 300°C/W. The temperature sensor's power dissipation, P_D, is the product of the total voltage across the device and its total supply current (including any current delivered to the load). The rise in die temperature above the medium's ambient temperature is given by:

$$T_J = P_D \times (\theta_{JC} + \theta_{CA}) + T_A.$$

Thus, the die temperature rise of an unloaded ADT45/ADT50 (SOT-23-3 package) soldered on a board in still air at 25°C and driven from a +5V supply (quiescent current = 60μA, P_D = 300μW) is less than 0.09°C. In order to prevent further temperature rise, it is important to minimize the load current, always keeping it less than 100μA.

The transient response of the ADT45/ADT50 sensors to a step change in temperature is determined by the thermal resistances and the thermal mass of the die and the case. The thermal mass of the case varies with the measurement medium since it includes anything that is in direct contact with the package. In all practical cases, the thermal mass of the case is the limiting factor in the thermal response time of the sensor and can be represented by a single-pole RC time constant. Thermal mass is often considered the thermal equivalent of electrical capacitance.

The thermal time constant of a temperature sensor is defined to be the time required for the sensor to reach 63.2% of the final value for a step change in the temperature. Figure 6.28 shows the thermal time constant of the ADT45/ADT50 series of sensors with the SOT-23-3 package soldered to 0.338" x 0.307" copper PC board as a function of air flow velocity. Note the rapid drop from 32 seconds to 12 seconds as the air velocity increases from 0 (still air) to 100 LFPM. As a point of reference, the thermal time constant of the ADT45/ADT50 series in a stirred oil bath is less than 1 second, which verifies that the major part of the thermal time constant is determined by the case.

The power supply pin of these sensors should be bypassed to ground with a 0.1μF ceramic capacitor having very short leads (preferably surface mount) and located as close to the power supply pin as possible. Since these temperature sensors operate on very little supply current and could be exposed to very hostile electrical environments, it is important to minimize the effects of EMI/RFI on these devices. The effect of RFI on these temperature sensors is manifested as abnormal DC shifts in the output voltage due to rectification of the high frequency noise by the internal IC junctions. In those cases where the devices are operated in the presence of high frequency radiated or conducted noise, a large value tantalum electrolytic capacitor (>2.2μF) placed across the 0.1μF ceramic may offer additional noise immunity.

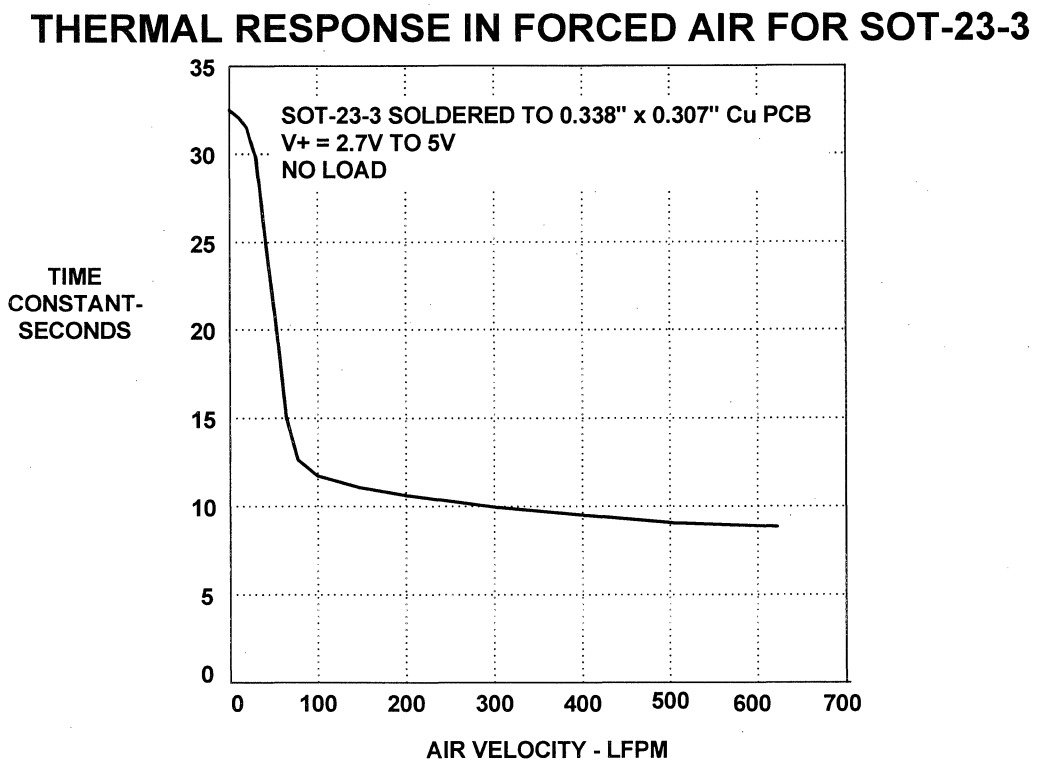


Figure 6.28

Digital Output Temperature Sensors

Temperature sensors which have digital outputs have a number of advantages over those with analog outputs, especially in remote applications. Opto-isolators can also be used to provide galvanic isolation between the remote sensor and the measurement system. A voltage-to-frequency converter driven by a voltage output temperature sensor accomplishes this function, however, more sophisticated ICs are now available which are more efficient and offer several performance advantages.

The TMP03/TMP04 digital output sensor family includes a voltage reference, V_{PTAT} generator, sigma-delta ADC, and a clock source (see Figure 6.29). The sensor output is digitized by a first-order sigma-delta modulator, also known as the "charge balance" type analog-to-digital converter. This converter utilizes time-domain oversampling and a high accuracy comparator to deliver 12 bits of effective accuracy in an extremely compact circuit.

The output of the sigma-delta modulator is encoded using a proprietary technique which results in a serial digital output signal with a mark-space ratio format (see Figure 6.30) that is easily decoded by any microprocessor into either degrees centigrade or degrees Fahrenheit, and readily transmitted over a single wire. Most importantly, this encoding method avoids major error sources common to other modulation techniques, as it is clock-independent. The nominal output frequency is 35Hz at + 25°C, and the device operates with a fixed high-level pulse width (T1) of 10ms.

DIGITAL OUTPUT SENSORS: TMP03/04

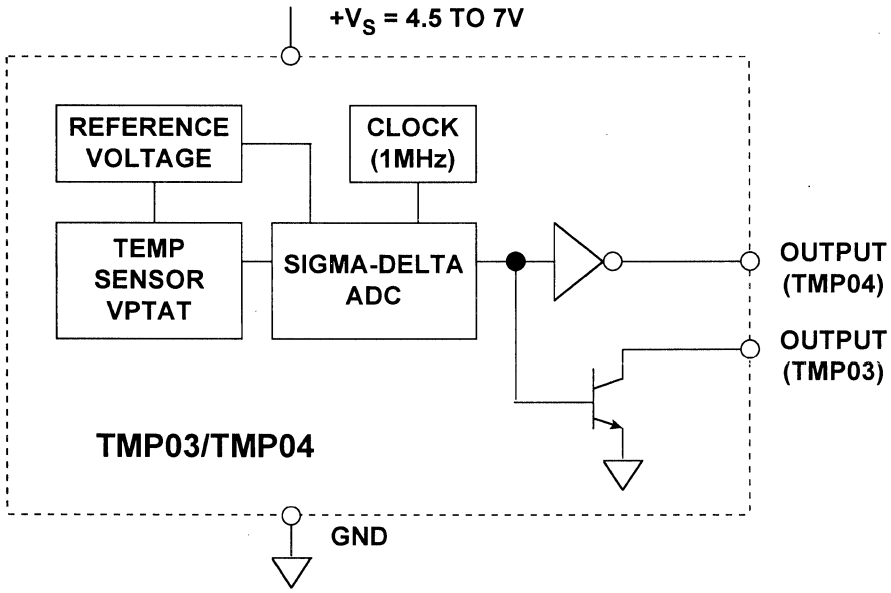
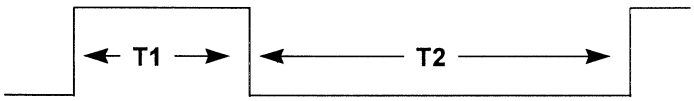


Figure 6.29

TMP03/TMP04 OUTPUT FORMAT



$$\text{TEMPERATURE (°C)} = 235 - \left(\frac{400 \times T1}{T2}\right)$$

$$\text{TEMPERATURE (°F)} = 455 - \left(\frac{720 \times T1}{T2}\right)$$

- T1 Nominal Pulse Width = 10ms
- ±1.5°C Error Over Temp, ±0.5°C Non-Linearity (Typical)
- Specified –40°C to +100°C
- Nominal T1/T2 @ 0°C = 60%
- Nominal Frequency @ +25°C = 35Hz
- 6.5mW Power Consumption @ 5V
- TO-92, SO-8, or TSSOP Packages

Figure 6.30

The TMP03/TMP04 output is a stream of digital pulses, and the temperature information is contained in the mark-space ratio per the equations:

$$\text{Temperature}\,(^\circ\text{C}) = 235 - \left(\frac{400 \times \text{T1}}{\text{T2}}\right)$$

$$\text{Temperature}\,(^\circ\text{F}) = 455 - \left(\frac{720 \times \text{T1}}{\text{T2}}\right).$$

Popular microcontrollers, such as the 80C51 and 68HC11, have on-chip timers which can easily decode the mark-space ratio of the TMP03/TMP04. A typical interface to the 80C51 is shown in Figure 6.31. Two timers, labeled *Timer 0* and *Timer 1* are 16 bits in length. The 80C51's system clock, divided by twelve, provides the source for the timers. The system clock is normally derived from a crystal oscillator, so timing measurements are quite accurate. Since the sensor's output is ratiometric, the actual clock frequency is not important. This feature is important because the microcontroller's clock frequency is often defined by some external timing constraint, such as the serial baud rate.

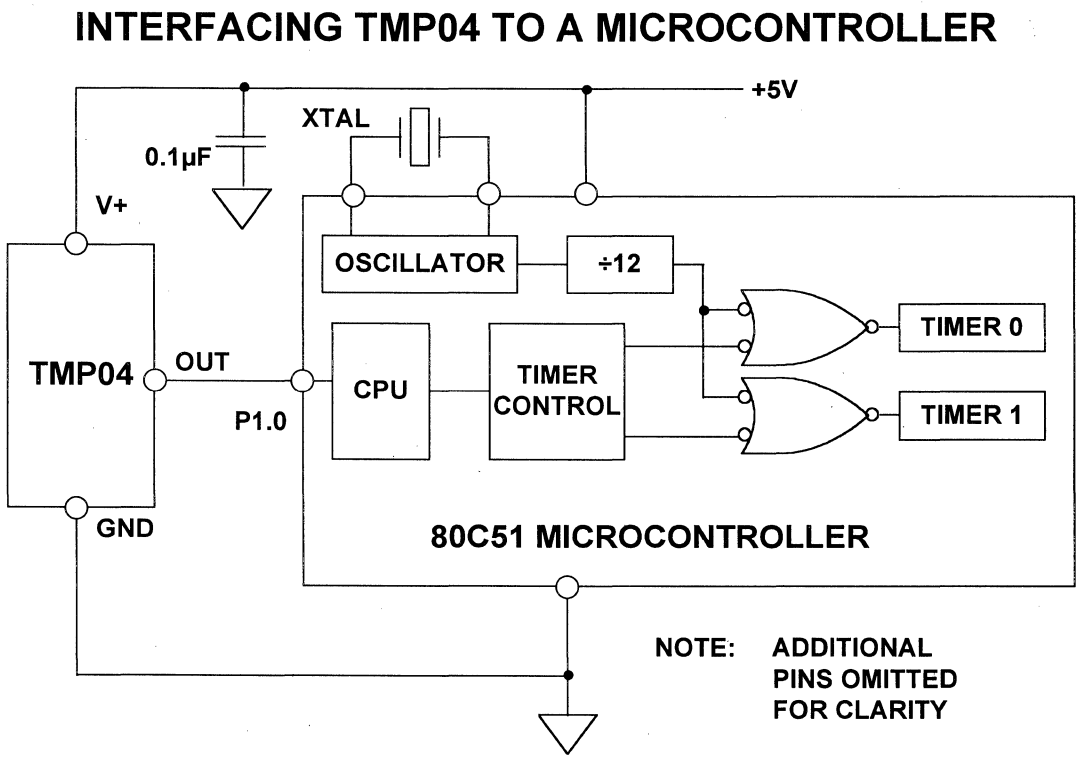


Figure 6.31

Software for the sensor interface is straightforward. The microcontroller simply monitors I/O port P1.0, and starts *Timer 0* on the rising edge of the sensor output. The microcontroller continues to monitor P1.0, stopping *Timer 0* and starting *Timer 1* when the sensor output goes low. When the output returns high, the sensor's T1 and T2 times are contained in registers *Timer 0* and *Timer 1*, respectively. Further software routines can then apply the conversion factor shown in the equations above and calculate the temperature.

The TMP03/TMP04 are ideal for monitoring the thermal environment within electronic equipment. For example, the surface mounted package will accurately reflect the thermal conditions which affect nearby integrated circuits. The TO-92 package, on the other hand, can be mounted above the surface of the board to measure the temperature of the air flowing over the board.

The TMP03 and TMP04 measure and convert the temperature at the surface of their own semiconductor chip. When they are used to measure the temperature of a nearby heat source, the thermal impedance between the heat source and the sensor must be considered. Often, a thermocouple or other temperature sensor is used to measure the temperature of the source, while the TMP03/TMP04 temperature is monitored by measuring T1 and T2. Once the thermal impedance is determined, the temperature of the heat source can be inferred from the TMP03/TMP04 output.

One example of using the TMP04 to monitor a high power dissipation microprocessor or other IC is shown in Figure 6.32. The TMP04, in a surface mount package, is mounted directly beneath the microprocessor's pin grid array (PGA) package. In a typical application, the TMP04's output would be connected to an ASIC where the mark-space ratio would be measured. The TMP04 pulse output provides a significant advantage in this application because it produces a linear temperature output, while needing only one I/O pin and without requiring an ADC.

MONITORING HIGH POWER MICROPROCESSOR OR DSP WITH TMP04

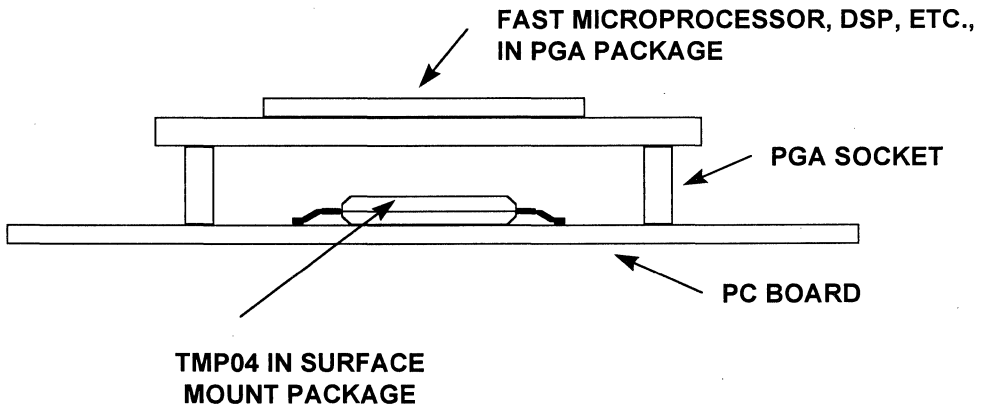


Figure 6.32

Thermostatic Switches and Setpoint Controllers

Temperature sensors used in conjunction with comparators can act as thermostatic switches. ICs such as the ADT05 accomplish this function at low cost and allow a single external resistor to program the setpoint to 2°C accuracy over a range of –40°C to +150°C (see Figure 6.33). The device asserts an open collector output when the ambient temperature exceeds the user-programmed setpoint temperature. The ADT05 has approximately 4°C of hysteresis which prevents rapid thermal on/off cycling. The ADT05 is designed to operate on a single supply voltage from +2.7V to

+7.0V facilitating operation in battery powered applications as well as industrial control systems. Because of low power dissipation (200µW @ 3.3V), self-heating errors are minimized, and battery life is maximized. An optional internal 200kΩ pull-up resistor is included to facilitate driving light loads such as CMOS inputs.

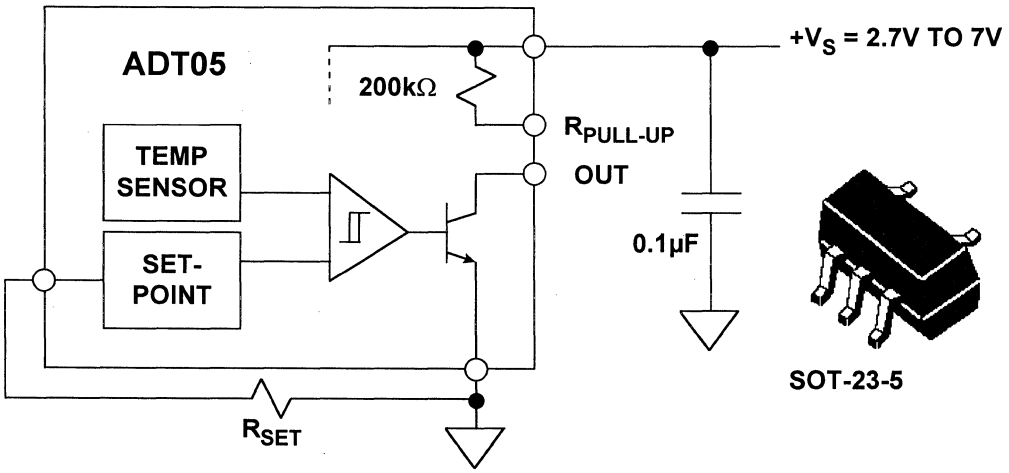
The setpoint resistor is determined by the equation:

$$R_{SET} = \frac{39M\Omega^{\circ}C}{T_{SET}(^{\circ}C) + 281.6^{\circ}C} - 90.3k\Omega.$$

The setpoint resistor should be connected directly between the R_{SET} pin (Pin 4) and the GND pin (Pin 5). If a ground plane is used, the resistor may be connected directly to this plane at the closest available point.

The setpoint resistor can be of nearly any resistor type, but its initial tolerance and thermal drift will affect the accuracy of the programmed switching temperature. For most applications, a 1% metal-film resistor will provide the best tradeoff between cost and accuracy. Once R_{SET} has been calculated, it may be found that the calculated value does not agree with readily available standard resistors of the chosen tolerance. In order to achieve a value as close as possible to the calculated value, a compound resistor can be constructed by connecting two resistors in series or parallel.

ADT05 THERMOSTATIC SWITCH



- ±2°C Setpoint Accuracy
- 4°C Preset Hysteresis
- Specified Operating Range: –40°C to + 150°C
- Power Dissipation: 200µW @ 3.3V

Figure 6.33

The TMP01 is a dual setpoint temperature controller which also generates a PTAT output voltage (see Figure 6.34 and 6.35). It also generates a control signal from one of two outputs when the device is either above or below a specific temperature range. Both the high/low temperature trip points and hysteresis band are determined by user-selected external resistors.

TMP01 PROGRAMMABLE SETPOINT CONTROLLER

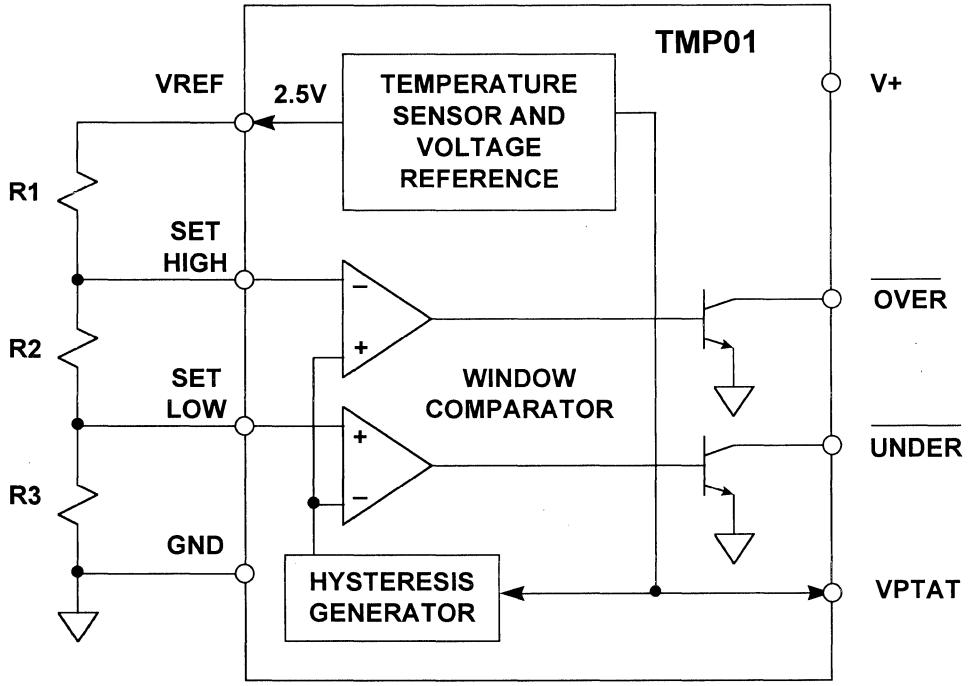


Figure 6.34

The TMP01 consists of a bandgap voltage reference combined with a pair of matched comparators. The reference provides both a constant 2.5V output and a PTAT output voltage which has a precise temperature coefficient of 5mV/K and is 1.49V (nominal) at +25°C. The comparators compare VPTAT with the externally set temperature trip points and generate an open-collector output signal when one of their respective thresholds has been exceeded.

Hysteresis is also programmed by the external resistor chain and is determined by the total current drawn out of the 2.5V reference. This current is mirrored and used to generate a hysteresis offset voltage of the appropriate polarity after a comparator has been tripped. The comparators are connected in parallel, which guarantees that there is no hysteresis overlap and eliminates erratic transitions between adjacent trip zones.

The TMP01 utilizes laser trimmed thin-film resistors to maintain a typical temperature accuracy of ±1°C over the rated temperature range. The open-collector outputs are capable of sinking 20mA, enabling the TMP01 to drive control relays directly. Operating from a +5V supply, quiescent current is only 500μA maximum.

TMP01 SETPOINT CONTROLLER KEY FEATURES

- **V_C: 4.5 to 13.2V**
- **Temperature Output: VPTAT, +5mV/K**
- **Nominal 1.49V Output @ 25°C**
- **±1°C Typical Accuracy Over Temperature**
- **Specified Operating Range: –55°C to + 125°C**
- **Resistor-Programmable Hysteresis**
- **Resistor-Programmable Setpoints**
- **Precision 2.5V ±8mV Reference**
- **400µA Quiescent Current, 1µA in Shutdown**
- **Packages: 8-Pin Dip, 8-Pin SOIC, 8-Pin TO-99**
- **Other Setpoint Controllers:**
  - **Dual Setpoint Controllers: ADT20/21/22 (3V Versions of TMP01 with Internal Hysteresis)**
  - **Quad Setpoint Controller: ADT14**

Figure 6.35

The ADT20/21/22-series are similar to the TMP01 but have internal hysteresis and are designed to operate on a 3V supply. A quad (ADT14) setpoint controller is also available.

An Airflow Monitor Based on the TMP12

For large power dissipation and/or to maintain low T_J's, forced air movement can be used to increase air flow and aid in heat removal. In its most simple form this can consist of a continuously or thermostatically operated fan, directed across high temperature, high wattage dissipation devices such as CPUs, DSP chips, etc.

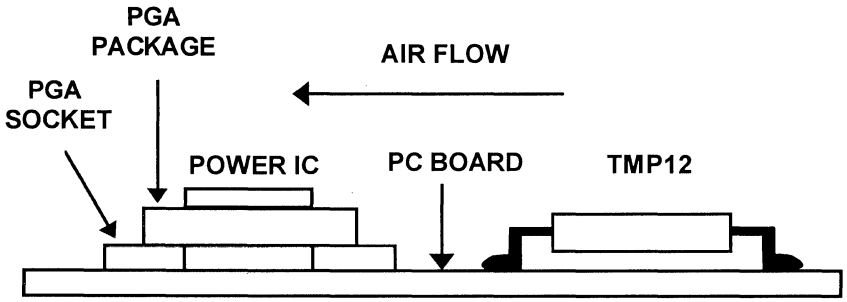
Quite often however, more sophisticated temperature control is necessary. Recent temperature monitoring and control ICs such as the TMP12, an airflow temperature sensor IC, lend themselves to such applications.

The TMP12 includes on chip two comparators, a voltage reference, a temperature sensor and a heater. The heater is used to force a predictable internal temperature rise, to match a power IC such as a microprocessor. The temperature sensing and control portions of the IC can then be programmed to respond to the temperature changes and control an external fan, so as to maintain some range of temperature. Compared to a simple thermostat, this allows infinite resolution of user control for control points and ON/OFF hysteresis.

The device is placed in an air stream near the power IC, such that both see the same stream of air, and will thus have like temperature profiles, assuming proper

control of the stream. This is shown in basic form by the layout diagram of Figure 6.36.

SYSTEM USE OF TMP12 AIRFLOW SENSOR



- TMP12 HAS INTERNAL 250mW HEATER
- TMP12 INTERNAL TEMPERATURE PROPORTIONAL TO AIR FLOW
- TMP12 INTERNAL TEMPERATURE PROPORTIONAL TO POWER IC TEMPERATURE

Figure 6.36

TMP12 TEMPERATURE RELATIONSHIPS

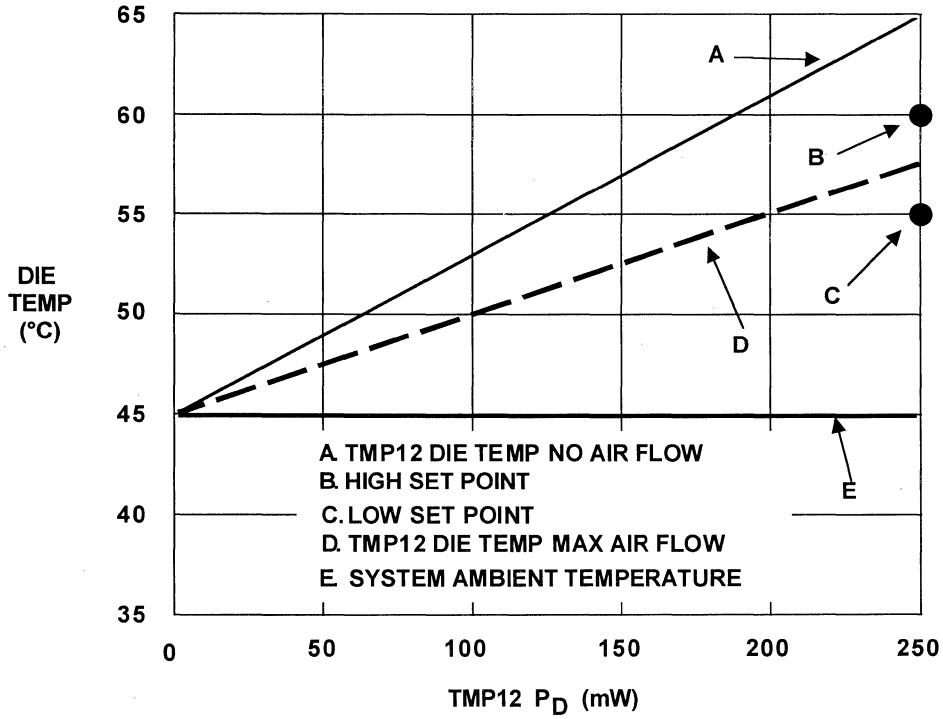


Figure 6.37

With the TMP12's internal 250mW heater ON and no airflow, the TMP12 thermal profile will look like the curve "A" of Figure 6.37, and will show a 20°C rise above T_A. When airflow is provided, this same dissipation results in a lower temperature, "D". In programming the device for airspeed control, the designer can set up to two switch points, shown here symbolically by "B" and "C", which are HIGH and LOW setpoints, respectively. The basic idea is that when the IC substrate reaches point B in temperature, the external fan will be turned on to create the air stream, and lower the temperature. If the overall system setup is reasonable in terms of thermal profiling, this small IC can thus be used to indirectly control another larger and independent power source with regard to its temperature. Note that the dual mode control need not necessarily be used, in all applications. An unused comparator is simply wired high or low.

Figure 6.38 shows a circuit diagram using the TMP12 as a general purpose controller. The device is connected to a 5V supply, which is also used to power a control relay and the TMP12's internal heater at pin 5. Setpoint programming of the TMP12 is accomplished by the resistor string at pins 4 through 1, R1 - R3. These resistors establish a current drain from the internal reference source at pin 4, which sets up a reference current, I_{REF}, which is set as:

$$I_{REF} = (5\mu A/°C \times T_{HYS}) + 7\mu A$$

In this expression, T_{HYS} is the hysteresis temperature swing desired about the setpoint, in °C, and the 7μA is recommended minimum loading of the reference. For a 2°C hysteresis for example, I_{REF} is 17μA; for 5°C, it would be 32μA.

Given a desired setpoint temperature in °C, the setpoint can be converted to a corresponding voltage. Although not available externally, the internal temperature dependent voltage of the TMP12 is scaled at 5mV/°C, and is equal to 1.49V at 25°C.

To convert a setpoint temperature to a voltage $V_{SETPOINT}$,

$$V_{SETPOINT} = 1.49V + [\ 5mV/°C \times (T_{SETPOINT} - T_{25})\ ]$$

where $T_{SETPOINT}$ is the desired setpoint temperature, and T_{25} is 25°C. For a 50°C high setpoint, this works out to be $V_{SETPOINT(HI)} = 1.615V$. For a lower setpoint of 35°C, the voltage $V_{SETPOINT(LO)}$ would be 1.59V.

The divider resistors are then chosen to draw the required current I_{REF} while setting the two tap voltages corresponding to $V_{SETPOINT(HI)}$ and $V_{SETPOINT(LO)}$.

$$R_{TOTAL} = V_{REF} / I_{REF}$$
$$= 2.5V / I_{REF}$$

$$R1 = [\ V_{REF} - V_{SETPOINT(HI)}\ ] / I_{REF}$$
$$= [\ 2.5V - V_{SETPOINT(HI)}\ ] / I_{REF}$$

$$R2 = [\ V_{SETPOINT(HI)} - V_{SETPOINT(LO)}\ ] / I_{REF}$$

$$R3 = V_{SETPOINT(LO)} / I_{REF}$$

In the example of the figure, the resulting standard values for R1 - R3 correspond to the temperature/voltage setpoint examples noted above. Ideal 1% values shown give resistor related errors of only 0.1°C from ideal. Note that this is error is independent of the TMP12 temperature errors, which are ±2°C.

As noted above, both comparators of the device need not always be used, and in this case the lower comparator output is not used. For a single point 50°C controller, the 35°C setpoint is superfluous. One resistor can be eliminated by making R2 + R3 a single value of 95.3kΩ and connecting pin 3 to GND. Pin 6 should be left as a no-connect. If a greater hysteresis is desired, the resistor values will be proportionally lowered.

It is also important to minimize potential parasitic temperature errors associated with the TMP12. Although the open-collector outputs can sink up to 20mA, it is advised that currents be kept low at this node, to limit any additional temperature rise. The Q1 - Q2 transistor buffer shown in the figure raises the current drive to 100mA, allowing a 50Ω/5V coil to be driven. The relay type shown is general purpose, and many other power interfaces are possible with the TMP12. If used as shown, the relay contacts would be used to turn on a fan for airflow when the active low output at pin 7 changes, indicating the upper setpoint threshold.

A basic assumption of the TMP12's operation is that it will "mimic" another device in temperature rise. Therefore, a practical working system must be arranged and tested for proper airflow channeling, minimal disturbances from adjacent devices, etc. Some experimentation should be expected before a final setup will result.

TMP12 50°C SETPOINT CONTROLLER

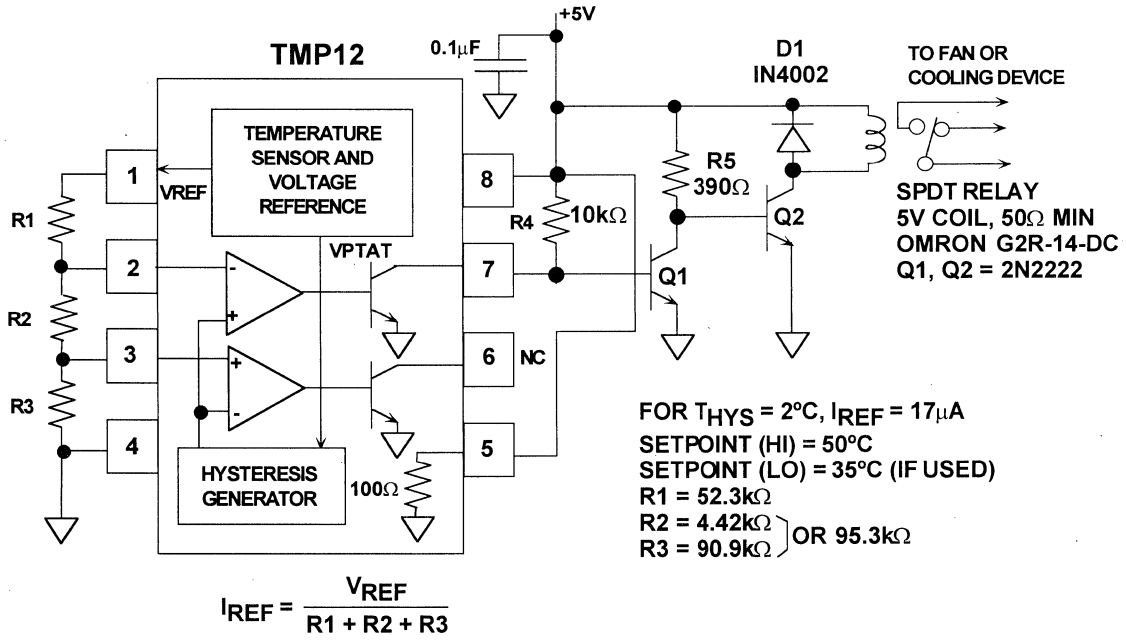


Figure 6.38

ADCs With On-Chip Temperature Sensors

The AD7416/7417/7418-series digital temperature sensors have on-board temperature sensors whose outputs are digitized by a 10-bit ADC. The output interface is I^2C compatible for convenience. The device family offers a variety of input options for further flexibility. The AD7816/7817/7818 are similar but have standard serial interfaces.

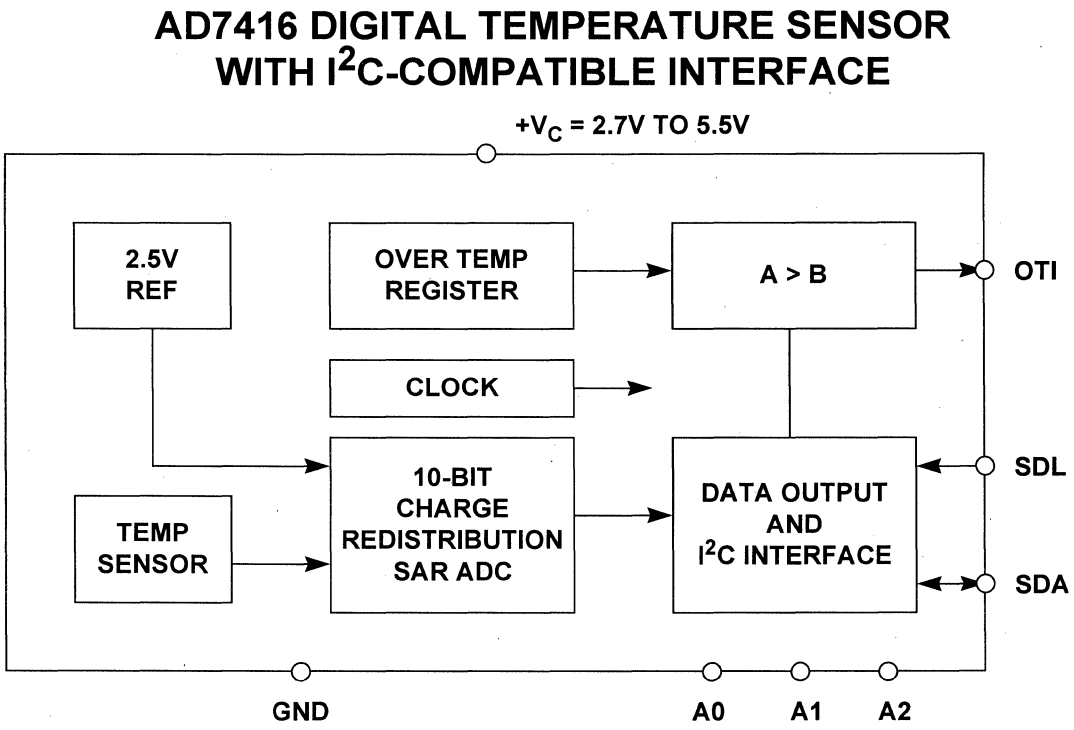


Figure 6.39

AD7416/7417/7418 - SERIES TEMP SENSOR 10-BIT ADCs WITH I^2C-COMPATIBLE INTERFACE

- 10-Bit ADC with 20µs Conversion Time
- I^2C-Compatible Interface
- On-Chip Temperature Sensor: –55°C to + 125°C
- On-Chip Voltage Reference: 2.5V ±0.1%
- +2.7V to +5.5V Power Supply
- 4µW Power Dissipation at 10Hz Sampling Rate
- Auto Power Down after Conversion
- Over-Temp Interrupt Output
- Four Single-Ended Analog Input Channels: AD7417
- One Single-Ended Analog Input Channel: AD7418

- AD7816/7817/7818: Similar, but have Serial Interface

Figure 6.40

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SECTION 7

HARDWARE MONITORING

SECTION 7
HARDWARE MONITORING
Walt Kester

INTRODUCTION

Today's computers require that hardware as well as software operate properly, in spite of the many things that can cause a system crash or lockup. The purpose of hardware monitoring is to monitor the critical items in a computing system and take corrective action should problems occur.

Microprocessor supply voltage and temperature are two critical parameters. If the supply voltage drops below a specified minimum level, further operations should be halted until the voltage returns to acceptable levels. In some cases, it is desirable to reset the microprocessor under "brownout" conditions. It is also common practice to reset the microprocessor on power-up or power-down. Switching to a battery backup may be required if the supply voltage is low.

Under low voltage conditions it is mandatory to inhibit the microprocessor from writing to external CMOS memory by inhibiting the Chip Enable signal to the external memory.

Many microprocessors can be programmed to periodically output a "watchdog" signal. Monitoring this signal gives an indication that the processor and its software are functioning properly and that the processor is not stuck in an endless loop.

The need for hardware monitoring has resulted in a number of ICs, traditionally called "microprocessor supervisory products," which perform some or all of the above functions. These devices range from simple manual reset generators (with debouncing) to complete microcontroller-based monitoring sub-systems with on-chip temperature sensors and ADCs.

The ADM8691-series (see Figures 7.1 and 7.2) are examples of traditional microprocessor supervisory circuits. Comparator accuracy and glitch immunity is key to the circuit's operation. The ADM8691-series provides the following functionality: (1) Power-on reset output during power-up, power-down, and brownout conditions. Circuitry remains operational with V_{CC} as low as 1V. (2) Battery backup switching for CMOS RAM, CMOS microprocessor, or other low power logic. (3) A reset pulse is generated by the optional watchdog timer if the watchdog input has not been toggled within a specified time. (4) A 1.25V threshold detector for power fail warning, low battery detection, or to monitor a supply other than +5V.

An application of the ADM8691 is shown in Figure 7.3. Resistors R1 and R2 divide the regulator input voltage down and provide a Power Fail Indication when the voltage at the POWER FAIL INPUT falls below 1.25V.

The nominal low supply voltage threshold is set internally to 4.65V (ADM8691 and ADM800L) or 4.4V (ADM8693 and ADM800M). If V_{CC} falls below these values, RESET will be asserted.

MICROPROCESSOR SUPERVISORY FUNCTIONS - ADM8691 - SERIES

- **Low Microprocessor Supply Voltage (4.65V or 4.4V)**
- **Battery Backup Steering Switch**
- **Power Failure Monitor (Low Line Voltage at Regulator Input)**
- **Power-On/Power-Down/Brownout Reset**
- **Watchdog Timer**
- **Inhibit Chip Enable to CMOS Memory (Prevents out-of-tolerance Microprocessor Addressing Memory)**

Figure 7.1

ADM8691-SERIES BLOCK DIAGRAM

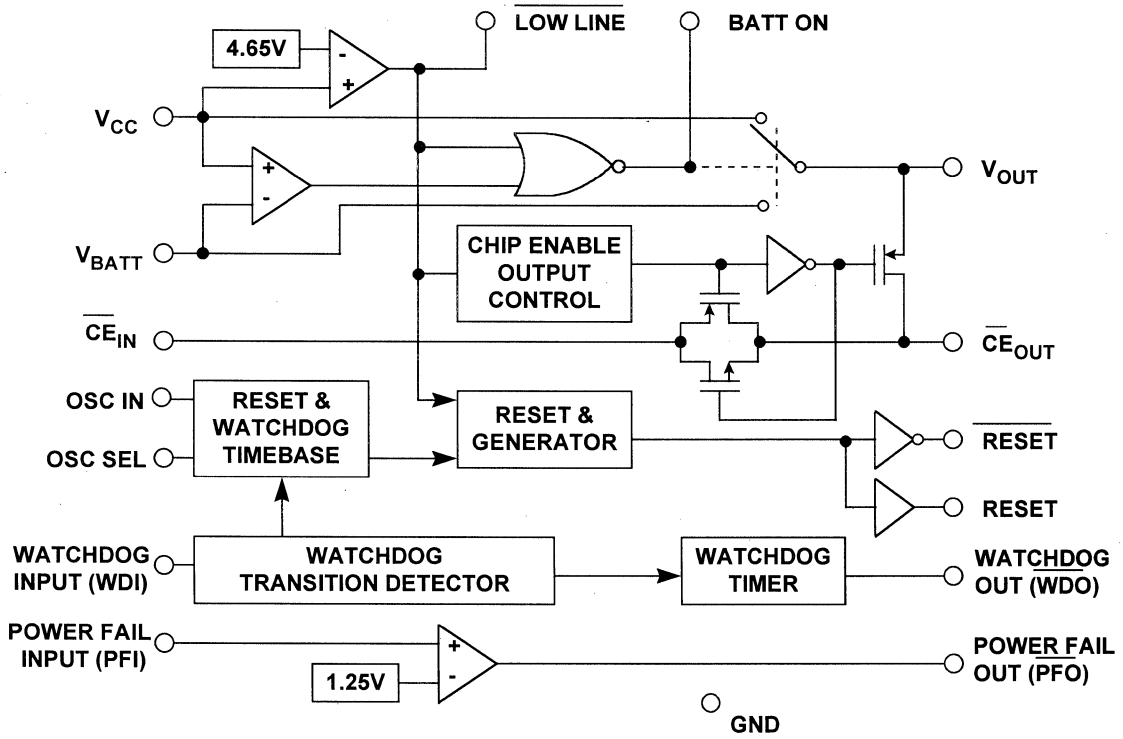

Figure 7.2

APPLICATION OF ADM8691 SERIES

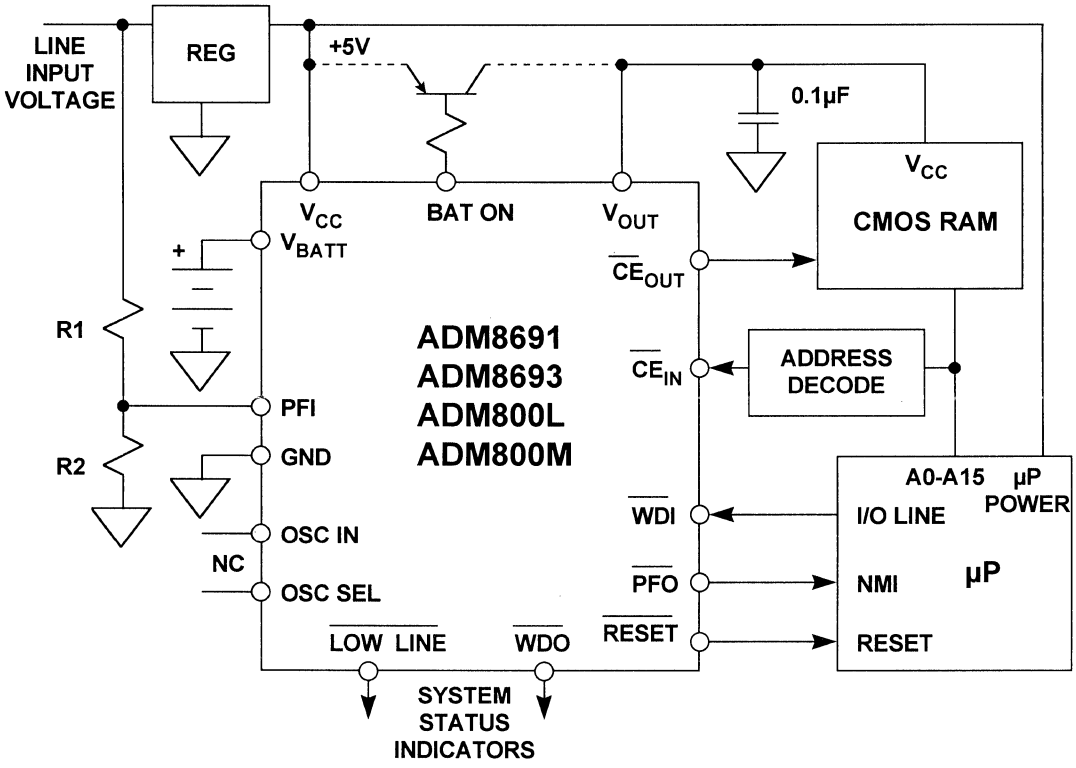

Figure 7.3

Several other actions occur when V_{CC} falls below its threshold value. The battery backup (V_{BATT}) is connected to the CMOS RAM power supply input via the V_{OUT} pin. Under normal operation, V_{CC} is connected to V_{OUT}, and the CMOS RAM receives its power from the V_{CC} input of the chip. The switch resistance from V_{CC} to V_{OUT} is 0.8Ω, and 12Ω from V_{BATT} to V_{OUT}. BATT ON goes high when V_{OUT} is internally switched to the V_{BATT} input. It goes low when V_{OUT} is internally switched to V_{CC}. The BAT ON output may also be used to drive the base (via a resistor) of an external PNP transistor to increase the output current above the 250mA rating of V_{OUT}.

The Chip Enable output ($\overline{CE}_{OUT}$) goes low only when $\overline{CE}_{IN}$ is low and V_{CC} is above the reset threshold. If $\overline{CE}_{IN}$ is low when reset is asserted, $\overline{CE}_{OUT}$ will remain low for 15µs or until $\overline{CE}_{IN}$ goes high, whichever occurs first.

The watchdog input, $\overline{WDI}$, is a three level input. If $\overline{WDI}$ remains either high or low for longer than the watchdog timeout period, $\overline{RESET}$ pulses low, and $\overline{WDO}$ goes low. The internal timer resets with each transition on the $\overline{WDI}$ line. The Watchdog Timer is disabled when $\overline{WDI}$ is left floating or driven to midsupply.

With OSC SEL high or floating, the internal oscillator is enabled and sets the reset delay and the watchdog timeout period. Connecting OSC IN low selects 100ms while leaving it floating selects 1.6sec. With OSC SEL low, OSC IN can be driven by an external clock signal or an external capacitor can be connected between OSC IN and

GND. This capacitor then sets both the reset active pulse timing and the watchdog timeout period.

The ADM8691-series supervisory circuit contains a high degree of functionality. There are many applications, however, where all these features are not required. Figure 7.4 lists some popular supervisory products and the various functions available in each.

TYPICAL SUPERVISORY PRODUCTS

	Batt Switch	CE Gate	Power Fail Monitor	Low Line Monitor	Watch-dog Timer	Vcc Monitor, Reset Gen.	Manual Reset
ADM869x	X	X	X	X	X	X	
ADM1232					X	X	X
ADM707			X		X	X	X
ADM809/810						X	
ADM811/812						X	X

Figure 7.4

The ADM9261 is a triple power supply monitor IC which allows simultaneous monitoring of a 9V and two 3.3V supplies and is designed primarily for pager systems. An error signal is generated if any of the supply voltages falls below an acceptable minimum value. Limits are set at 4V for the 9V supply (SU1 input), 3.0V for the SU2 3.3V input, and 2.8V for the SU3 3.3V input. Power supplies greater than V_{CC} can be monitored because the ADM9261 has on-chip thin film resistor input attenuators. Key features of the design are the comparator hysteresis (3%) and glitch immunity (100mV, 20μs). Glitch immunity minimizes the possibility of spurious triggering by noise spikes on the supplies being monitored. A block diagram of the device is shown in Figure 7.5, key features in Figure 7.6, and a pager application circuit in Figure 7.7.

ADM9261 TRIPLE COMPARATOR AND REFERENCE

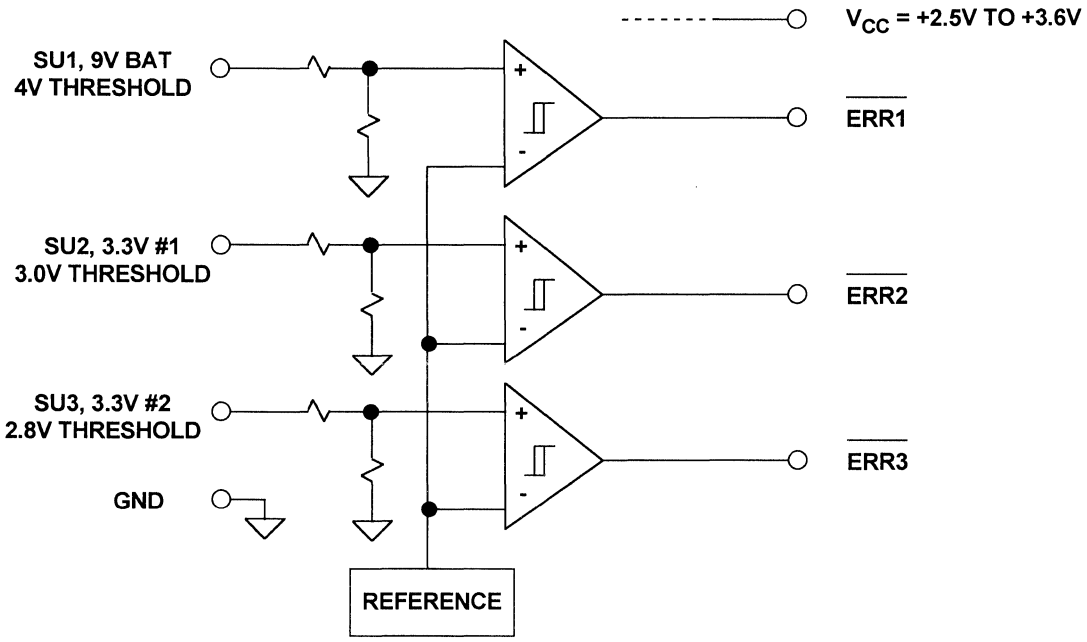

Figure 7.5

ADM9261 KEY SPECIFICATIONS

- Simultaneous Monitoring of 9V, and two 3.3V Supplies
- Limits set at 4V for SU1 9V Input, 3.0V for SU2 3.3V Input, and 2.8V for SU3 3.3V Input
- V_{CC}: 2.5V to 3.6V
- Low Power: 10µA Typical
- Internal Comparator Hysteresis: 3%
- Power Supply Glitch Immunity: 20µs, 100mV on V_{CC} or SU1-SU3
- Guaranteed from –10°C to +60°C
- No External Components Required
- 8-pin Micro SOIC Package

Figure 7.6

ADM9261 PAGER POWER SYSTEM APPLICATION CIRCUIT

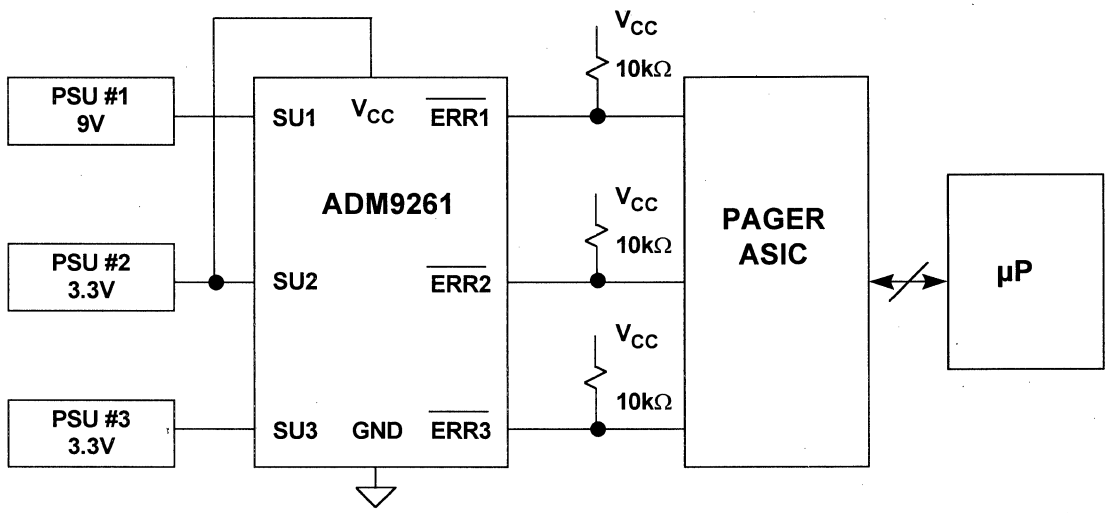

Figure 7.7

The ADM9264 is a quad power supply monitor IC which simultaneously monitors four separate supply voltage and outputs error signals if any of the supply voltages go above or below preset limits. It is designed for desktop PC supply monitoring but can be used in any system where multiple power supplies require monitoring. Each power supply monitor circuit uses a proprietary window comparator design whereby a three resistor network is used in conjunction with two comparators and a single precision reference to check if the supply is within its required operating tolerance. An added feature of this design is that the power supply voltages being monitored can be higher than the power supply voltage to the ADM9264. The allowable tolerance on the monitored voltages are as follows: 12V ± 1V, 5V ±0.5V, 3.3V ± 0.3V, 2.8V ± 0.2V.

The error output signals are available individually and are also gated into a common output, PWROK. Auxiliary inputs ERRX, ERRY are provided which are also gated into the main PWROK signal. Signals other than power supplies can be accomodated as inputs to the ADM9264, such as temperature sensors.

A block diagram of the ADM9264 is shown in Figure 7.8, key specifications in Figure 7.9, and an application circuit in Figure 7.10.

ADM9264 QUAD SUPPLY VOLTAGE MONITOR

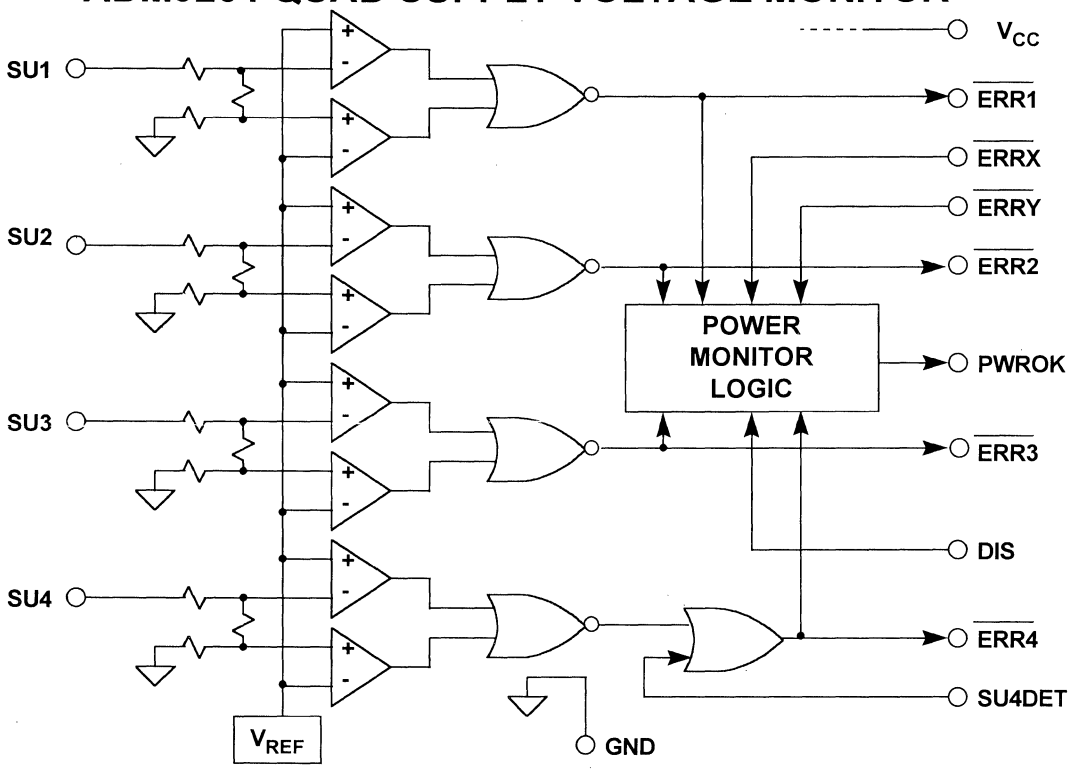

Figure 7.8

ADM9264 KEY SPECIFICATIONS

- Simultaneous Monitoring of 12V, 5V, 3.3V, and 2.8V for Desktop PCs
- Limits Set at 12V ± 1V, 5V ± 0.5V, 3.3V ± 0.3V, and 2.8V ± 0.2V
- Auxiliary Sensor Inputs
- Low Power: 25µA Typical
- Internal Comparator Hysteresis:
  - 320mV for 12V, 130mV for 5V, 90mV for 3.3V, and 80mV for 2.8V
- Power Supply Glitch Immunity: 100mV, 10µs on V_{CC} or SU1- SU4
- V_{CC}: 2.5V to 6V
- Guaranteed: –40°C to +85°C
- No External Components Required
- 16-pin Narrow SOIC Package (150mil wide)

Figure 7.9

ADM9264 APPLICATION CIRCUIT

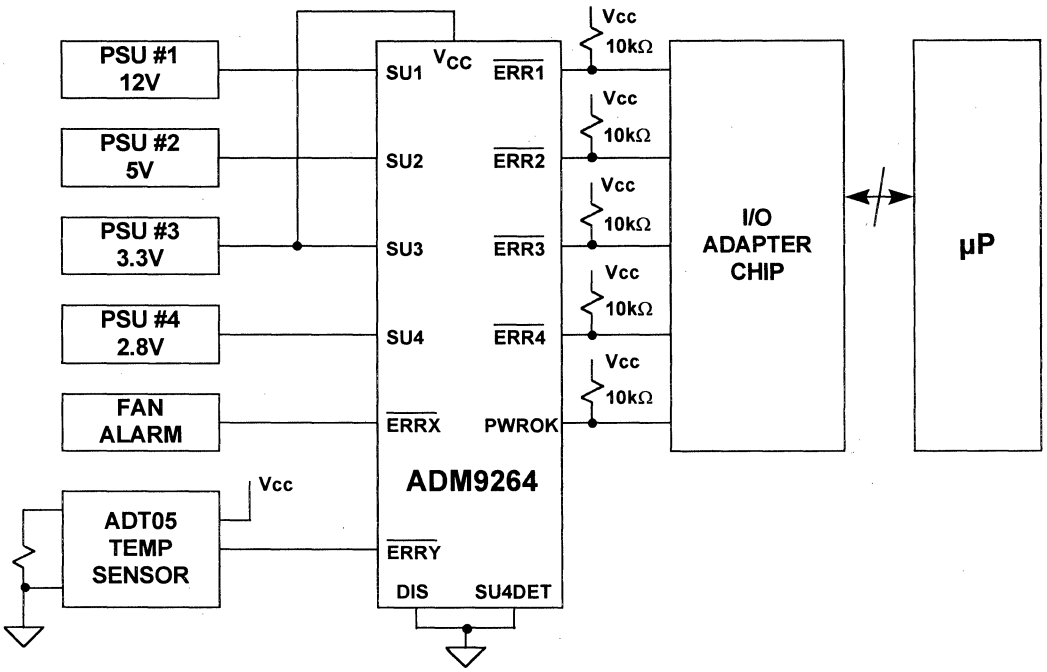

Figure 7.10

The ADM9268 (block diagram not shown) is similar to the ADM9264 but monitors six power supplies in a desktop PC and outputs the status information on an industry standard two-wire I^2C-compatible serial interface. One input of the ADM9268 is designed to monitor the CPU core voltage of a Pentium II processor. The range of CPU voltage options is from 1.3V to 3.5V and is set by a 5-bit VID code which is inputted via the serial I^2C-compatible interface. This makes the ADM9268 compatible with all the CPUs currently available in the marketplace. Key specifications for the ADM9268 are summarized in Figure 7.11.

ADM9268 HEX VOLTAGE MONITOR

- **Monitors All Six Desktop PC Power Supplies Simultaneously with Hex Window Comparators**
- **Monitors 12V (±6%), 5V (±7%), 3.3V (±7%), 2.5V or 3.3V (±7%), 1.5V (±7%), and CPU Core Voltage (±5%)**
- **5-bit VID Code Sets Core Monitor Voltage: 1.3V to 3.5V**
- **Standard two-wire I^2C-Compatible Serial Interface**
- **Operates on V_{CC} from 2.5V to 6V**
- **16-pin Narrow (150mil) SOIC Package**

Figure 7.11

The ADM9240 (see Figure 7.12) is a complete high-level system hardware monitor for microprocessor based systems, providing measurement and limit comparison of up to four power supplies and two processor core voltages, plus temperature, fan speed, and chassis intrusion. Measured values can be read out via an I^2C-compatible serial interface, and values for limit comparisons can be programmed over the same serial bus. The high-speed 10-bit ADC allows frequent sampling of all analog channels to ensure a fast interrupt response to any out-of-limit measurement. Key specifications for the ADM9240 are summarized in Figure 7.13.

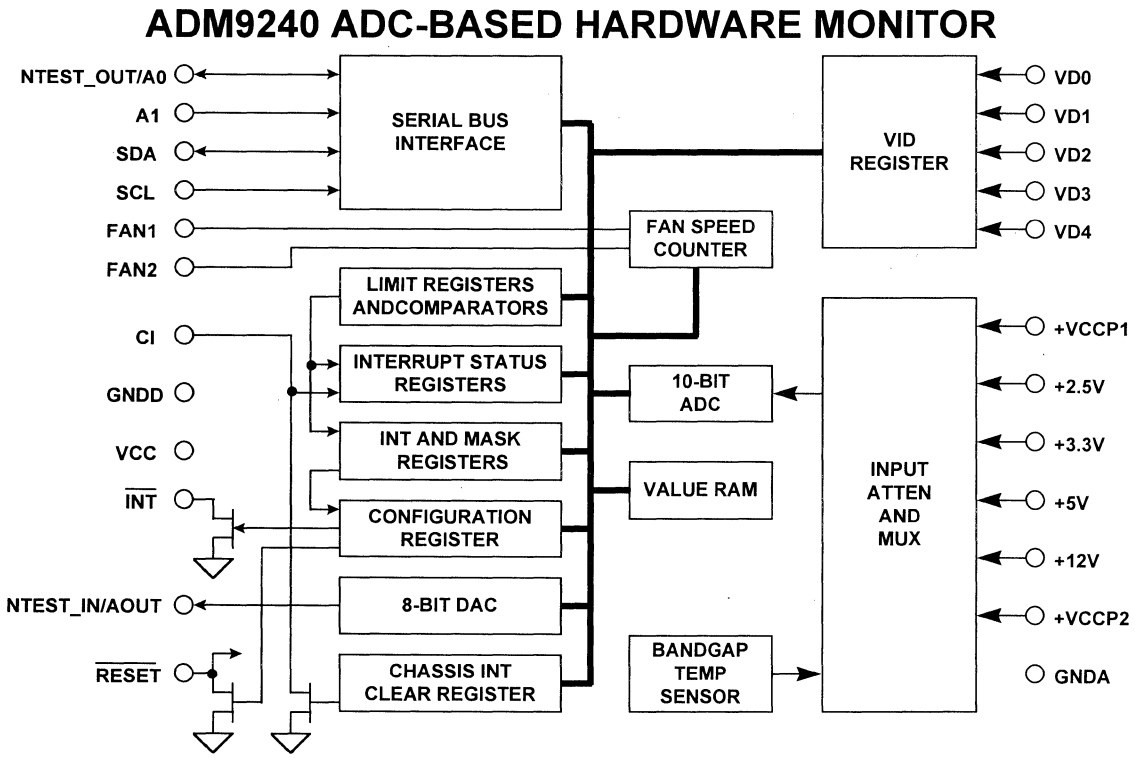

Figure 7.12

ADM9240 KEY SPECIFICATIONS

- **6 Direct Voltage Measurement Inputs (Including 2 Processor Core Voltages) with On-Chip Attenuators**
- **On-Chip 10-bit ADC and 8-bit DAC**
- **5 Digital Voltage Identification (VID) Inputs**
- **2 Fan Speed Monitoring Inputs**
- **I^2C-Compatible System Management Bus**
- **Chassis Intrusion Detect**
- **On-Chip Temperature Sensor**
- **V_{CC}: 2.85V to 5.75V**
- **1.2mA Typical Supply Current, 10µA in Shutdown**
- **24-pin SOIC Package**

Figure 7.13

Figure 7.14 shows a generic application circuit using the AD9240. The analog inputs are connected to the power supplies and processor core voltage. VID inputs are connected to the processor Voltage ID pins. There are two inputs from fans, and the analog output is controlling the speed of a third fan. A chassis intrusion latch with a phototransistor as the sensor is connected to the CI input. In an actual application, every input and output may not be used, in which case unused analog and digital inputs should be tied to analog or digital ground as appropriate.

The chassis intrusion circuit could use a microswitch that opens or closes when the cover is removed, a reed switch operated by a magnet fixed to the cover, a Hall-effect switch operated by a magnet fixed to the cover, or a phototransistor that detects light when the cover is removed. In the circuit shown in Figure 7.14, light falling on the phototransistor when the PC cover is removed will cause it to turn on and pull up the input of N1, thus setting the latch N2/N3. After the cover is replaced, a low reset on the ADM9240 CI output will pull down the input of N3, thus resetting the latch.

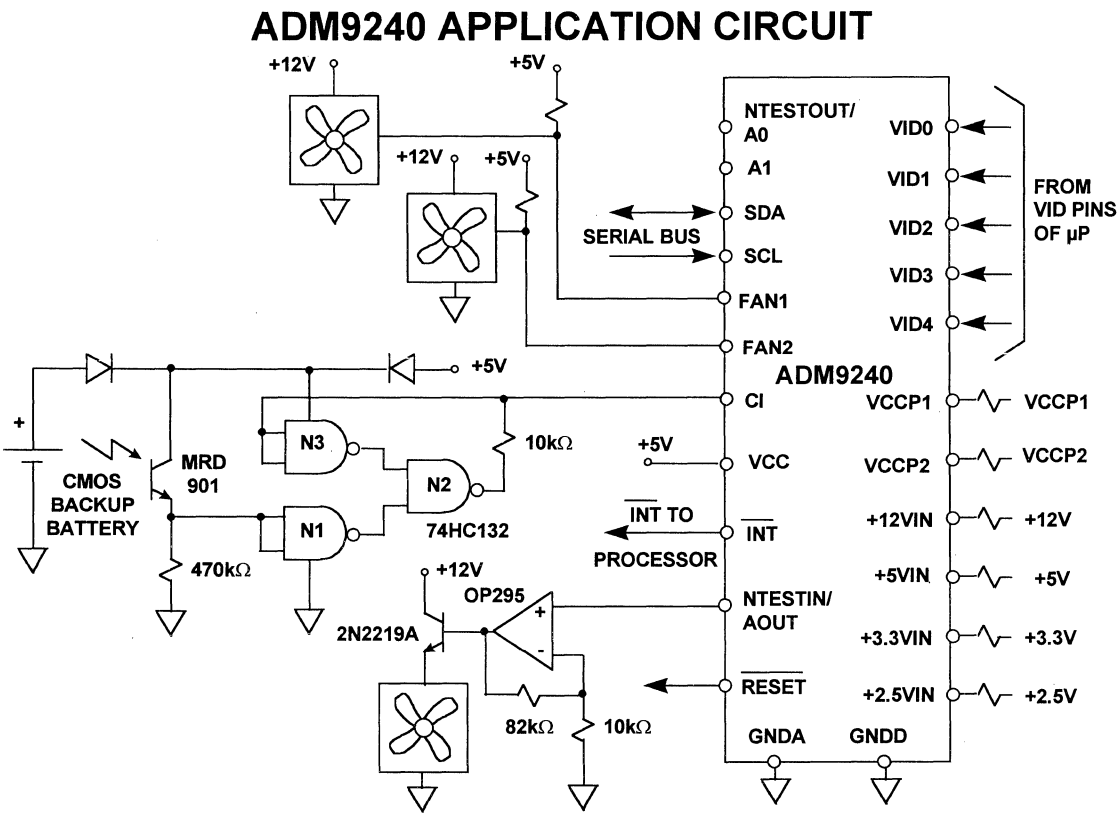

Figure 7.14

In hardware monitoring circuits it is often desirable to use a high-resolution low-cost measurement ADC, for tasks such as monitoring battery voltages during charging. The AD7705 is a 16-bit sigma-delta ADC with a two-channel multiplexed input as shown in Figure 7.15. Key specifications are given in Figure 7.16. The AD7705 has a programmable gain amplifier which can be set for a gain of 1 to 128. The inputs and outputs are handled with a three-wire serial interface. The device has an on-chip digital filter and a programmable output rate from 20Hz to 500Hz.

An application of the AD7705 as a cell monitor in a battery charging circuit is shown in Figure 7.17.

AD7705 16-BIT ADC BATTERY MONITOR

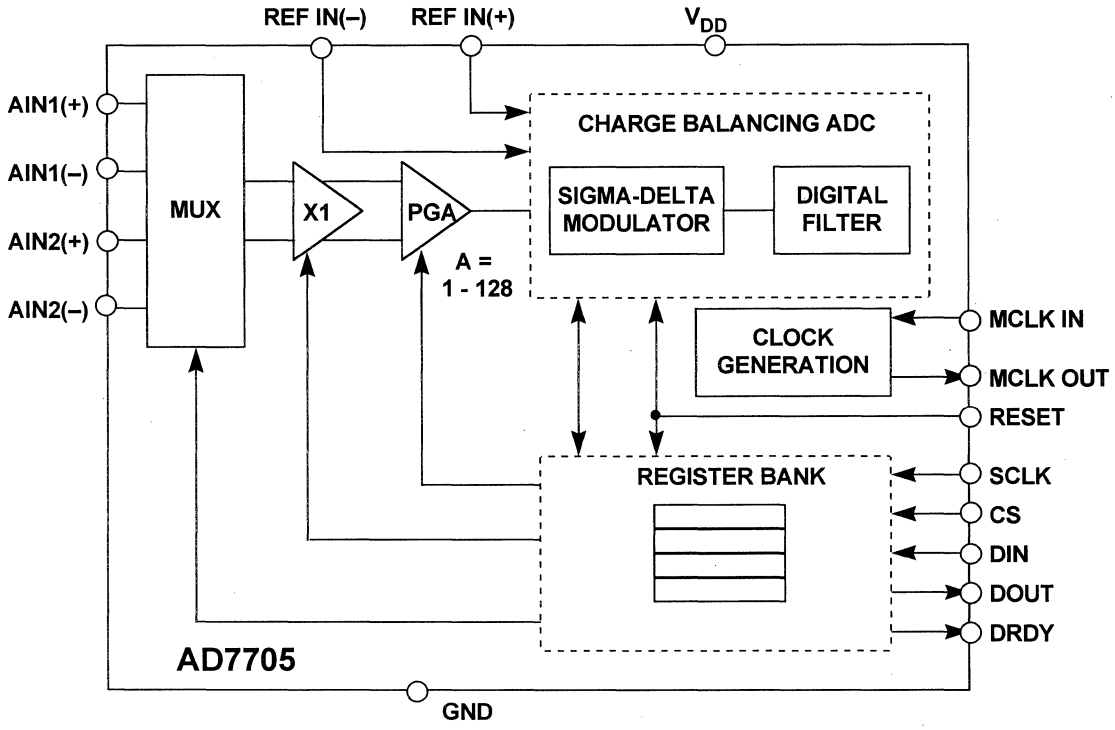

Figure 7.15

AD7705 ADC KEY SPECIFICATIONS

- 2 Channel Charge-Balancing ADC
  - 16-bits, No Missing Codes
  - 0.012% Nonlinearity
- Programmable Front End
  - Binary Gains from 1 to 128
  - Differential Input Capability
- 3 Wire Serial Interface
- Ability to Buffer Analog Input
- 3V or 5V Single Supply Operation
- Low Power: <450µA @ 3V
- Programmable Low-Pass Digital Filter with Programmable Output Rate (20Hz to 500Hz)
- 16-pin DIP, SOIC, and TSSOP

Figure 7.16

AD7705 BATTERY MONITORING APPLICATION

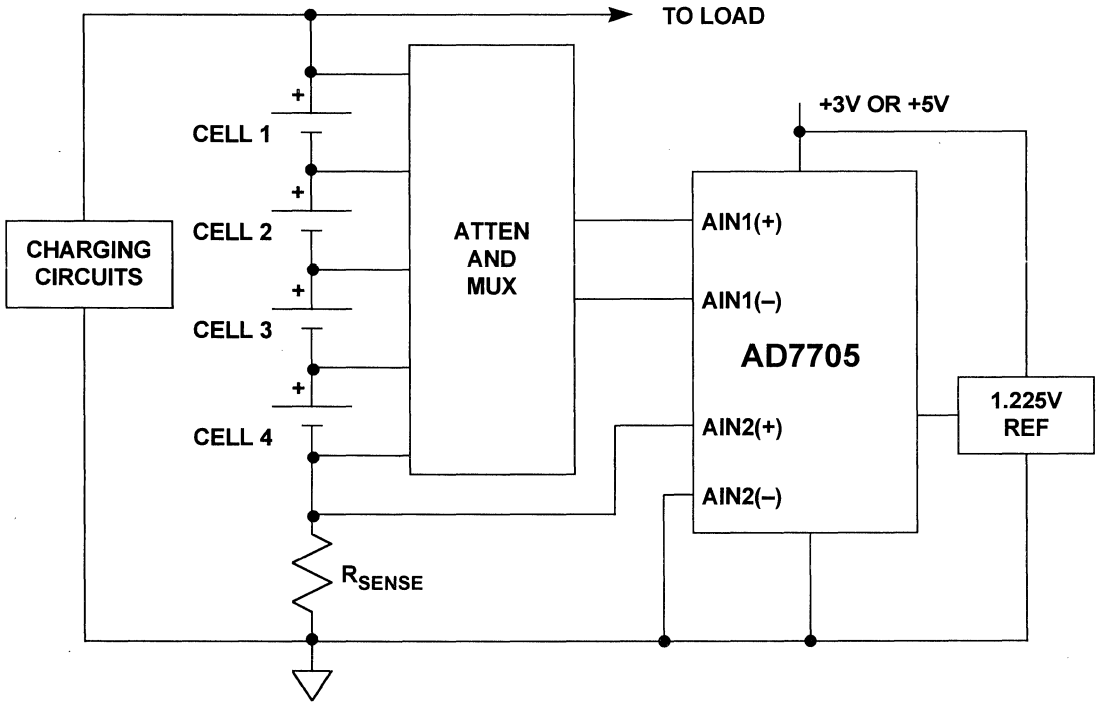

Figure 7.17

Complex hardware monitoring circuits often interface with a microcontroller (such as the 8051) which performs various operations based on the sensor and monitor outputs. The ADu810PC is a MicroConverter™ (combination ADC and microcontroller) based on the standard 8051 core. In addition to the microcontroller core, the device has a 10-bit, 2μs ADC with SHA and a 16-channel analog input multiplexer. The chip also contains a temperature sensor and bandgap voltage reference as well as two 8-bit DACs with voltage output buffers. MicroConverters such as these allow sophisticated monitoring and control functions such as power supply monitoring and watchdog timeout to be performed in a single chip.

ADuC810PC (MicroConverter™)

- Complete Hardware Monitor System with on-chip microcontroller (Standard 8051-based Core)
- Calibrated 10-bit, 2 microsecond ADC with SHA and DMA Mode
- 16 Channel Analog Multiplexer
- On-Chip Temperature Sensor and Bandgap Voltage Reference
- 2 DACs (8-bits) with Voltage Output Buffers
- 3V or 5V Single Supply Operation

- 64 Digital I/O for Address, Data, Interrupts, LEDs, LCDs
- UART and I^2C-Compatible / SPI Serial Interfaces
- 3 x 16-bit Timers / Counters, 2 Muxed for 4-Channel Fans
- Independent Watchdog / Clock and Supply Monitor
- Power Management of Peripherals and I/O

Figure 7.18

ADuC810PC PROCESSOR

- DC TO 16MHz Static Industry-Standard (8051) MCU for up to 1MIP Operation
- 48k Bytes Flash Program Memory
- 2k Bytes Flash/EEPROM Lockable User Data Memory
- 1k Bytes Data RAM
- 64k Bytes External Program and Data Memory Space
- Enhanced Hooks ™ Emulation and Debugging Tools
- Resident Loader and Debugger
- Simplified I/O through Special Function Registers
- Multi-Level, Maskable Interrupts
- 100-pin PQFP 14x14mm Package

Figure 7.19

REFERENCE

Bill Schweber, *Supervisory ICs Establish System Boundaries*, **EDN**, Sept. 28, 1995, p. 71.

SECTION 8

HARDWARE DESIGN TECHNIQUES

- Analog Circuit Simulation
- Prototyping Techniques
- Evaluation Boards
- Grounding Techniques for Regulator Circuits
- Power Supply Noise Reduction and Filtering
- Thermal Management
- EMI/RFI Considerations
- Shielding Concepts

SECTION 8
HARDWARE DESIGN TECHNIQUES
Walt Kester, Walt Jung, James Bryant, Bill Chestnut

ANALOG CIRCUIT SIMULATION

In recent years there has been much pressure placed on system designers to verify their designs with computer simulations before committing to actual printed circuit board layouts and hardware. Simulating complex digital designs is extremely beneficial, and very often, the prototype phase can be eliminated entirely. However, bypassing the prototype phase in high-speed/high-performance analog or mixed-signal circuit designs can be risky for a number of reasons.

For the purposes of this discussion, an *analog* circuit is any circuit which uses ICs such as op amps, instrumentation amps, programmable gain amps (PGAs), voltage controlled amps (VCAs), log amps, mixers, analog multipliers, voltage references, etc. A *mixed-signal* circuit is an A/D converter (ADC), D/A converter (DAC), or combinations of these in conjunction with some amount of digital signal processing which may or may not be on the same IC as the converters. Switching regulators must be classified as high-speed analog circuits because of the frequencies generated by the internal or external switching action.

Consider a typical IC operational amplifier. It may contain some 20-40 transistors, almost as many resistors, and a few capacitors. A complete SPICE (Simulation Program with Integrated Circuit Emphasis, see Reference 1) model will contain all these components, and probably a few of the more important parasitic capacitances and spurious diodes formed by the various junctions in the op-amp chip. For high-speed ICs, the package and wirebond parasitics may also be included. This is the type of model that the IC designer uses to optimize the device during the design phase and is typically run on a CAD workstation. Because it is a detailed model, it will be referred to as a *micromodel.* In simulations, such a model will behave very much like the actual op-amp, but not exactly.

The IC designer uses transistor and other device models based on the actual process upon which the component is fabricated. Semiconductor manufacturers invest considerable time and money developing and refining these device models so that the IC designers can have a high degree of confidence that the first silicon will work and that mask changes (costing additional time and money) required for the final manufactured product are minimized.

However, these *device* models are not published, neither are the IC *micromodels*, as they contain proprietary information which would be of use to other semiconductor companies who might wish to copy or improve on the design. It would also take far too long for a simulation of a system containing several ICs (each represented by its own micromodel) to reach a useful result. SPICE micromodels of analog ICs often fail to converge (especially under transient conditions), and multiple IC circuits make this a greater possibility.

For these reasons, the SPICE models of analog circuits published by manufacturers or software companies are *macromodels* (as opposed to *micromodels*), which simulate the major features of the component, but lack fine detail. Most manufacturers of linear ICs (including Analog Devices) provide these macromodels for components such as operational amplifiers, analog multipliers, references, etc. (Reference 2 and 3). These models represent *approximations* to the actual circuit, and parasitic effects such as package capacitance and inductance and PC board layout are rarely included. The models are designed to work with various versions of SPICE simulation programs such as PSpice® (Reference 4) and run on workstations or personal computers. The models are simple enough so that circuits using multiple ICs can be simulated in a reasonable amount of computation time and with good certainty of convergence. Consequently, SPICE modeling does not always reproduce the exact performance of a circuit and should always be verified experimentally using a carefully built prototype.

Finally, there are mixed-signal ICs such as A/D and D/A converters which have *no* SPICE models, or if they exist, the models do not simulate dynamic performance (Signal-to-noise, effective bits, etc.), and prototypes of circuits using them should always be built. In addition to mixed-signal ICs, switching regulators do not lend themselves to SPICE modelling. The dynamics of either magnetic-based or switched capacitor-based regulators are far too complex for simple macromodels.

ANALOG CIRCUIT SIMULATION CONSIDERATIONS

- **ADSpice Macromodels (Over 500) Exist for the Following:**
  - **Amplifiers**
  - **Analog Multipliers**
  - **Multiplexers and Switches**
  - **Voltage References**
- **No Practical SPICE Macromodels for:**
  - **ADCs, DACs**
  - **Switching Regulators**
- **There is No Substitute for a Good Prototype!!**

Figure 8.1

PROTOTYPING TECHNIQUES
James Bryant, Walt Kester

The basic principle of a breadboard or prototype is that it is a *temporary* structure, designed to test the performance of a circuit or system, and must therefore be easy to modify.

There are many commercial prototyping systems, but almost all of them are designed to facilitate the prototyping of *digital* systems, where noise immunities are hundreds of millivolts or more. Non copper-clad Matrix board, Vectorboard, wire-wrap, and plug-in breadboard systems are, without exception, unsuitable for high performance or high frequency analog prototyping because their resistance, inductance, and capacitance are too high. Even the use of standard IC sockets is inadvisable in many prototyping applications.

An important consideration in selecting a prototyping method is the requirement for a large-area ground plane. This is required for high frequency circuits (including switching power supplies) as well as low speed precision circuits (including references and low dropout linear regulators), especially when prototyping circuits involving ADCs or DACs. The differentiation between *high-speed* and *high-precision* mixed-signal circuits is difficult to make. For example, 16+ bit ADCs (and DACs) may operate on high speed clocks (>10MHz) with rise and fall times of less than a few nanoseconds, while the effective throughput rate of the converters may be less than 100kSPS. Successful prototyping of these circuits requires that equal attention be given to good high-speed and high-precision circuit techniques. Switching regulators also fall into the high-speed catagory. Even though their desired output is a DC voltage, low output ripple voltage is highly dependent upon the use of proper high-speed grounding, layout, and decoupling techniques.

The simplest technique for analog prototyping uses a solid copper-clad board as a ground plane (Reference 5 and 6). The ground pins of the ICs are soldered directly to the plane, and the other components are wired together above it. This allows HF decoupling paths to be very short. All lead lengths should be as short as possible, and signal routing should separate high-level and low-level signals. Connection wires should be located close to the surface of the board to minimize the possibility of stray inductive coupling. In most cases, 18-gauge or larger insulated wire should be used. Parallel runs should not be "bundled" because of possible coupling. Ideally the layout (at least the relative placement of the components on the board) should be similar to the layout to be used on the final PCB. This approach is often referred to as *deadbug prototyping* because the ICs are often mounted upside down with their leads up in the air (with the exception of the ground pins, which are bent over and soldered directly to the ground plane). The upside-down ICs look like deceased insects, hence the name.

Figure 8.2 shows a hand-wired breadboard using two high speed op amps which gives excellent performance in spite of its lack of esthetic appeal. The IC op amps are mounted upside down on the copper board with the leads bent over. The signals are connected with short point-to-point wiring. The characteristic impedance of a wire over a ground plane is about 120Ω, although this may vary as much as ±40% depending on the distance from the plane. The decoupling capacitors are connected directly from the op amp power pins to the copper-clad ground plane. When working at frequencies of several hundred MHz, it is a good idea to use only one side of the board for ground. Many people drill holes in the board and connect both sides together with short pieces of wire soldered to both sides of the board. If care is not taken, however, this may result in unexpected ground loops between the two sides of the board, especially at RF frequencies.

HANDWIRED "DEADBUG" PROTOTYPE

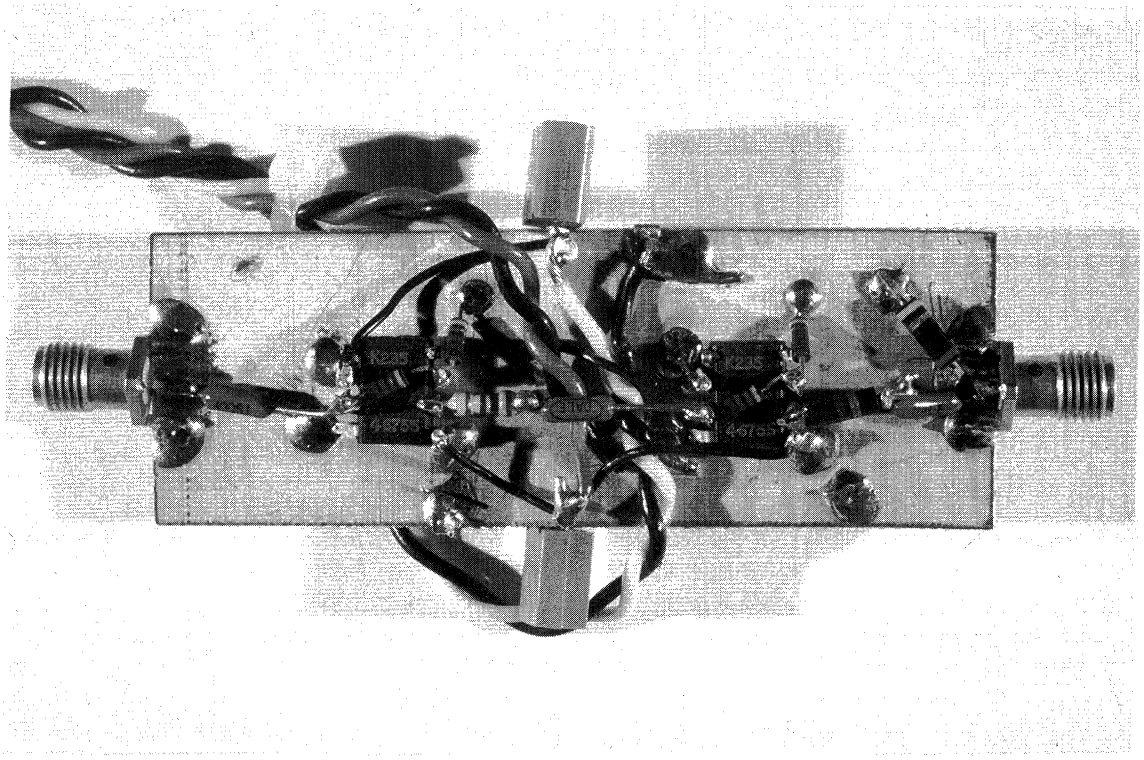

Figure 8.2

Pieces of copper-clad board may be soldered at right angles to the main ground plane to provide screening, or circuitry may be constructed on both sides of the board (with connections through holes) with the board itself providing screening. In this case, the board will need standoffs at the corners to protect the components on the underside from being crushed.

When the components of a breadboard of this type are wired point-to-point in the air (a type of construction strongly advocated by Robert A. Pease of National Semiconductor (Reference 6) and sometimes known as "bird's nest" construction) there is always the risk of the circuitry being crushed and resulting short-circuits. Also, if the circuitry rises high above the ground plane, the screening effect of the ground plane is diminished, and interaction between different parts of the circuit is more likely. Nevertheless, the technique is very practical and widely used because the circuit may easily be modified (assuming the person doing the modifications is adept at using a soldering iron, solder-wick, and a solder-sucker).

Copper-clad boards are available with pre-drilled holes on 0.1" centers (Reference 7). Because of the loss of copper area due to the pre-drilled holes, this technique does not provide as low a ground impedance as a completely covered copper-clad board. However, this type of board is convenient if the ICs in the prototype have the proper pin spacing.

In a variation of this technique, the ICs and other components are mounted on the non-copper-clad side of the board. The holes are used as vias, and the point-to-point wiring is done on the copper-clad side of the board. The copper surrounding each

hole used for a via must be drilled out to prevent shorting. This approach requires that all IC pins be on 0.1" centers. Low profile sockets can be used for low frequency circuits, and the socket pins allow easy point-to-point wiring.

There is a commercial breadboarding system which has most of the advantages of the above techniques (robust ground, screening, ease of circuit alteration, low capacitance and low inductance) and several additional advantages: it is rigid, components are close to the ground plane, and where necessary, node capacitances and line impedances can be calculated easily. This system is made by Wainwright Instruments and is available in Europe as "Mini-Mount" and in the USA (where the trademark "Mini-Mount" is the property of another company) as "Solder-Mount" (Reference 8).

Solder-Mount consists of small pieces of PCB with etched patterns on one side and contact adhesive on the other. These pieces are stuck to the ground plane, and components are soldered to them. They are available in a wide variety of patterns, including ready-made pads for IC packages of all sizes from 3-pin SOT-23 packages to 64-pin DILs, strips with solder pads at intervals (which intervals range from 0.040" to 0.25", the range includes strips with 0.1" pad spacing which may be used to mount DIL devices), strips with conductors of the correct width to form microstrip transmission lines (50Ω, 60Ω, 75Ω or 100Ω) when mounted on the ground plane, and a variety of pads for mounting various other components. Self-adhesive tinned copper strips and rectangles (LO-PADS) are also available as tie-points for connections. They have a relatively high capacitance to ground and therefore serve as low-inductance decoupling capacitors. They come in sheet form and may be cut with a knife or scissors. A few of the many types of Solder-Mount building-block components are shown in Figure 8.3.

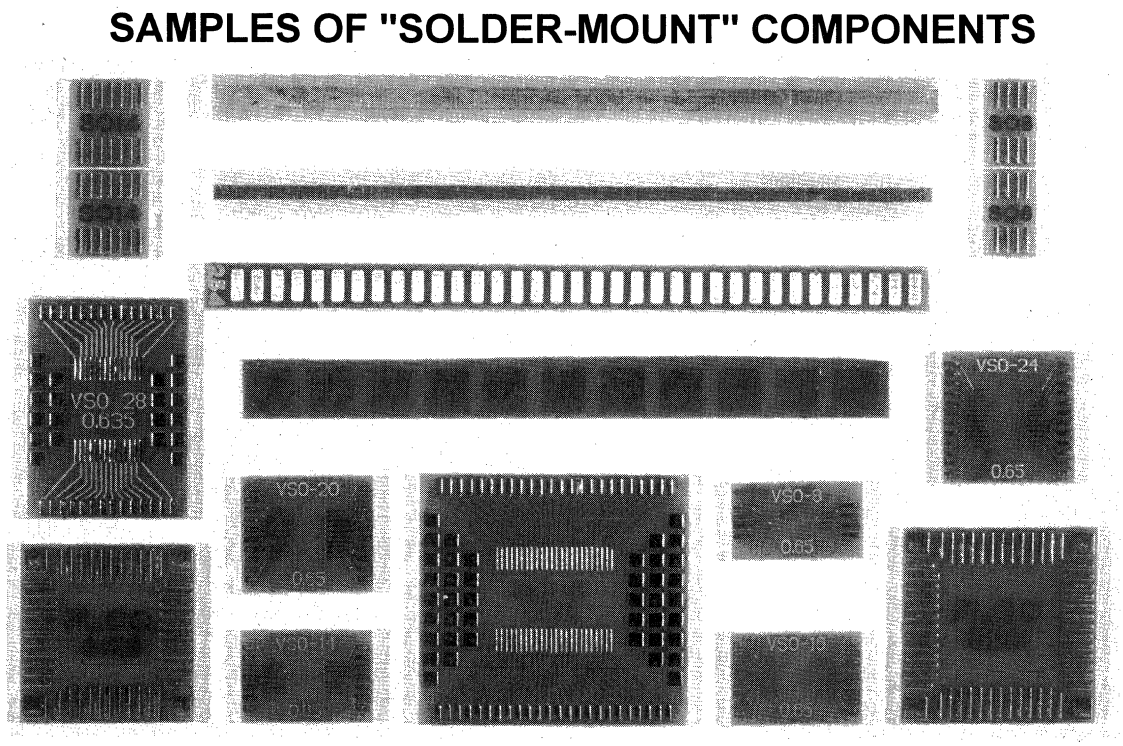

Figure 8.3

The main advantage of Solder-Mount construction over "bird's nest" or "deadbug" is that the resulting circuit is far more rigid, and, if desired, may be made far smaller (the latest Solder-Mounts are for surface-mount devices and allow the construction of breadboards scarcely larger than the final PC board, although it is generally more convenient if the prototype is somewhat larger). Solder-Mount is sufficiently durable that it may be used for small quantity production as well as prototyping.

Both the "deadbug" and the "Solder-Mount" prototyping techniques become somewhat tedious for complex analog or mixed-signal circuits. Larger circuits are often better prototyped using more formal layout techniques.

Another approach to prototyping analog circuits is to actually lay out a single or double-sided board using CAD techniques. PC-based software layout packages offer ease of layout as well as schematic capture to verify connections (Reference 9). Although most layout software has some amount of auto-routing capability, this feature is best left to digital designs. After the components are placed in their desired positions, the interconnections should be routed manually following good analog layout guidelines. After the layout is complete, the software verifies the connections per the schematic diagram net list.

Many design engineers find that they can use CAD techniques to lay out simple boards themselves, or work closely with a layout person who has experience in analog circuit boards. The result is a pattern-generation tape (or Gerber file) which would normally be sent to a PCB manufacturing facility where the final board is made. Rather than use a PC board manufacturer, however, automatic drilling and milling machines are available which accept the PG tape directly (Reference 10). These systems produce single and double-sided circuit boards directly by drilling all holes and use a milling technique to remove copper, and to create insulation paths for the finished board. The result is a board very similar to the final manufactured double-sided PC board, the chief exception being that there is no "plated-through" hole capability, and any "vias" between the two layers of the board must be wired and soldered on both sides. Minimum trace widths of 25 mils (1 mil = 0.001") and 12 mil spacing between traces are standard, although smaller trace widths can be achieved with care. The minimum spacing between lines is dictated by the size of the milling bit, typically 10 to 12 mils.

Figures 8.4 and 8.5 show the top and bottom side of a switching regulator prototype based on the ADP3000. A CAD system was used in the layout, and the board was fabricated using a PC board milling machine (board cutter). The size of the board is approximately 2.5" by 3.5".

The input to the regulator is on the left-hand side of the board (top view), and it is decoupled directly to the ground plane with three 33µF/16V tantalum surface mount capacitors. Note that the connections are directly from the input pad to the ground plane for minimum parasitic series resistance and inductance. The ADP3000 IC is mounted in a low-profile socket on the bottom side of the board near the center. The external energy transfer inductor is located in the upper part of the board slightly to the right of the center of the board. It is mounted in an encapsulated plastic package suitable for surface mounting. The output of the ADP3000 is decoupled

with a 33µF/16V surface mount capacitor and is followed by an LC filter before connecting to the output load.

Notice that all connections are short, especially those to the surface mount capacitors. This isolates the high-speed switching currents to a small area and prevents interference with other circuits which the regulator may be supplying.

HANDWIRED PROTOTYPE (ADP3000) TOP VIEW

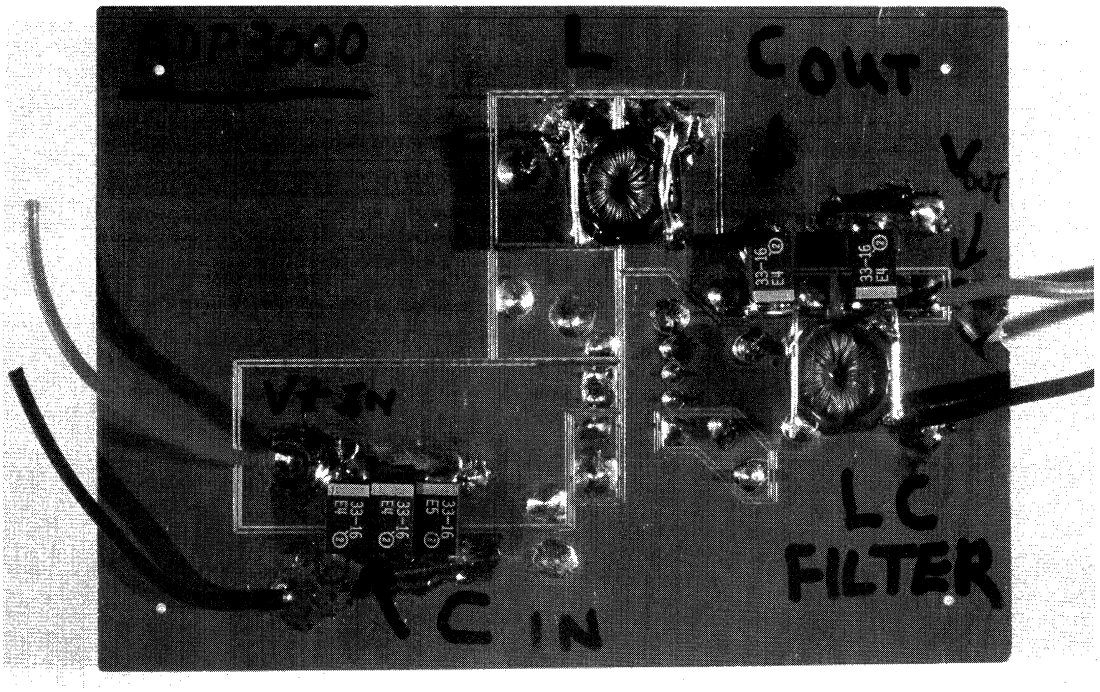

Figure 8.4

In Figure 8.5 (bottom view) note that the ADP3000 is mounted in a low profile IC socket for convenience. The "catch diode" is located directly beneath the ADP3000. The two resistors to the right of the ADP3000 set the output voltage, and the resistor above and to the left of the ADP3000 is the current-limiting resistor. The loop of wire allows the inductor current to be monitored with a current probe. Note that the resistors are in individual pin sockets to allow easy modifications.

HANDWIRED PROTOTYPE (ADP3000) BOTTOM VIEW

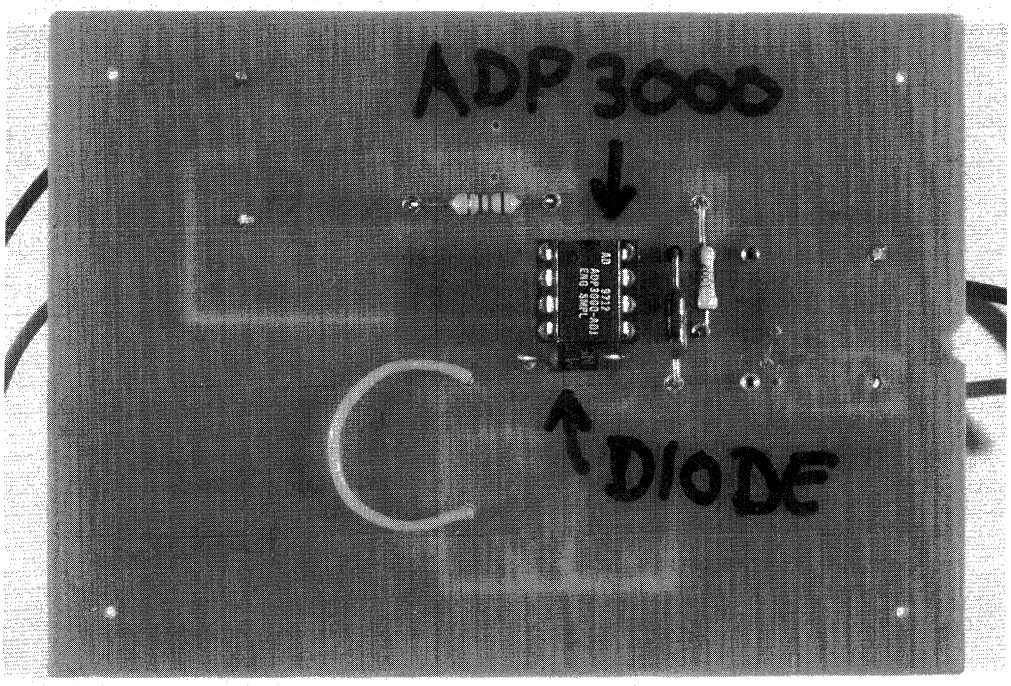

Figure 8.5

IC sockets, however, can degrade the performance of high speed or high precision analog ICs. Although they make prototyping easier, even *low-profile* sockets often introduce enough parasitic capacitance and inductance to degrade the performance of the circuit. If sockets must be used in high speed circuits, an IC socket made of individual *pin sockets* (sometimes called *cage jacks*) mounted in the ground plane board may be acceptable (clear the copper, on both sides of the board, for about 0.5mm around each ungrounded pin socket and solder the grounded ones to ground on both sides of the board). Both capped and uncapped versions of these pin sockets are available (AMP part numbers 5-330808-3, and 5-330808-6, respectively). The pin sockets protrude through the board far enough to allow point-to-point wiring interconnections between them (see Figure 8.6).

The spring-loaded gold-plated contacts within the pin socket makes good electrical and mechanical connection to the IC pins. Multiple insertions, however, may degrade the performance of the pin socket, and pin sockets should never be used in the high-current paths associated with linear or switching regulators. The uncapped versions allow the IC pins to extend out the bottom of the socket. After the prototype is functional and no further changes are to be made, the IC pins can be soldered directly to the bottom of the socket, thereby making a permanent and rugged connection.

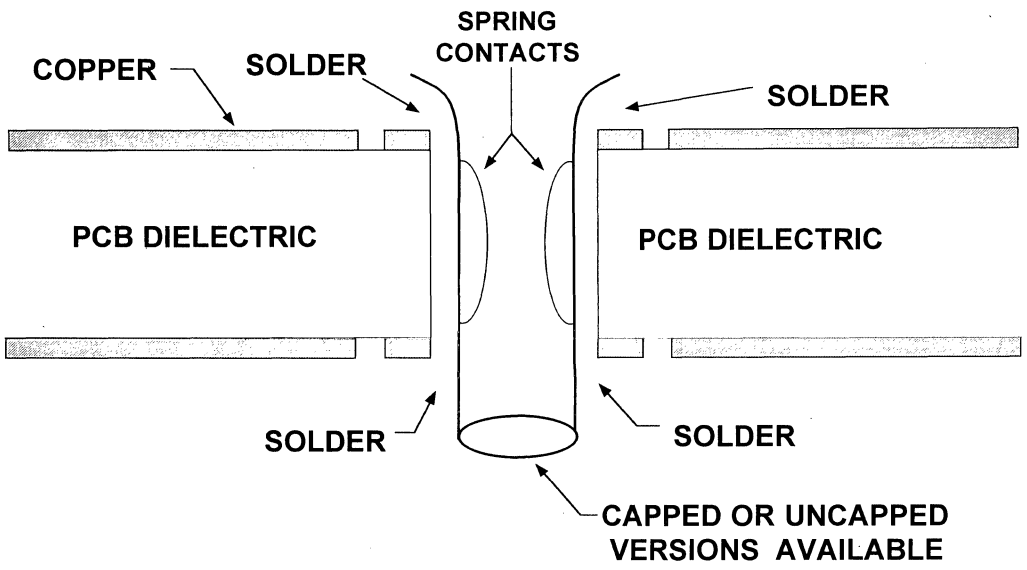

Figure 8.6

The prototyping techniques discussed so far have been limited to single or double-sided PC boards. Multilayer PC boards do not easily lend themselves to standard prototyping techniques. If multilayer board prototyping is required, one side of a double-sided board can be used for ground and the other side for power and signals. Point-to-point wiring can be used for additional runs which would normally be placed on the additional layers provided by a multi-layer board. However, it is difficult to control the impedance of the point-to-point wiring runs, and the high frequency performance of a circuit prototyped in this manner may differ significantly from the final multilayer board.

Other difficulties in prototyping may occur with op amps or other linear devices having bandwidths greater than a few hundred megahertz. Small variations in parasitic capacitance (<1pF) between the prototype and the final board may cause subtle differences in bandwidth and settling time. Oftentimes prototyping is done with DIP packages, when the final production package is an SOIC. This can account for differences between prototype and final PC board performance. However this option may not be available, as many new ICs are only being introduced in surface mount packages.

EVALUATION BOARDS
Walt Kester

Most manufacturers of analog ICs provide evaluation boards (usually at a nominal cost) which allow customers to evaluate products without constructing their own prototypes. Regardless of the product, the manufacturer has taken proper precautions regarding grounding, layout, and decoupling to ensure optimum device performance. The artwork or CAD file is usually made available free of charge,

should the customer wish to copy the layout directly or make modifications to suit the application.

Figure 8.7 shows the very compact evaluation board for the ADP3300 50mA low dropout linear regulator. The ADP3300 is located in the center of the board and is in a SOT-23 6-lead package. The input capacitor (C1) and output capacitor (C2) are both 0.47µF low inductance surface mount devices. The Noise Reduction capacitor (C3) is 10nF. Resistor R1 is a pullup resistor for the open-collector error output pin. The entire active circuit (located within the small square) is approximately 0.6" by 0.6" (15.2mm by 15.2mm).

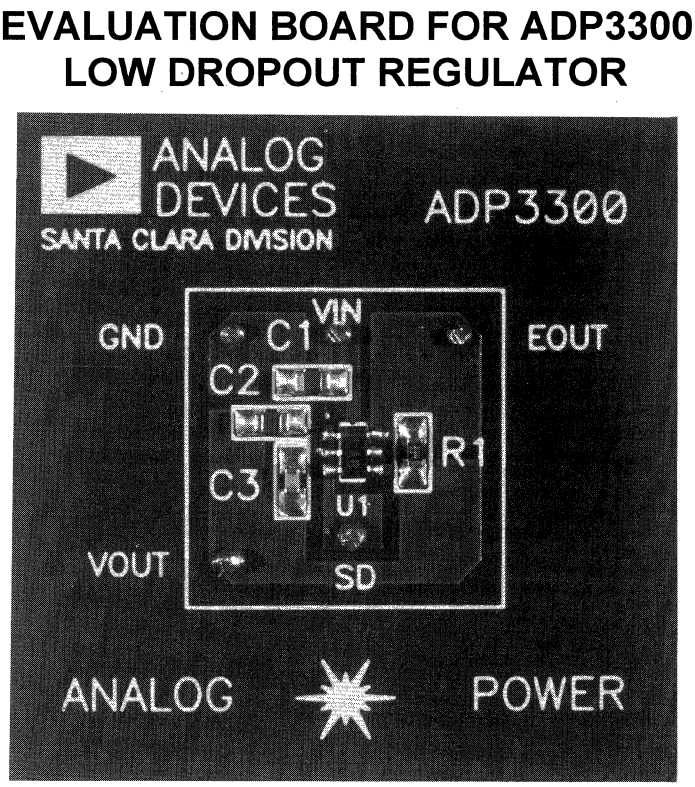

Figure 8.7

Switching regulators, such as the ADP1148, place more exacting demands on layout and decoupling. The evaluation board for the ADP1148 is shown in Figures 8.8 (top view) and 8.9 (bottom view - ground plane). The board size is approximately 2" by 2" (5.1cm by 5.1cm). The input decoupling capacitors (C1 and C1A) are each 220µF/25V general purpose aluminum electrolytic capacitors. Also there is a 1µF tantalum in parallel with C1 and C1A (labeled C2).

The output capacitors (C6 and C6A) are each low ESR OS-CON 220µF/10V. The ADP1148 is located to the right of the center of the board and is in a 14-pin SOIC surface mount package. The energy transfer inductor (L1) is a 68µH surface mount part from Coiltronics. Other readily visible components making up the regulator are two power MOSFETs (Q1 and Q2) and a 0.05Ω current sense resistor (R2).

EVALUATION BOARD FOR ADP1148 SWITCHING REGULATOR - TOP VIEW

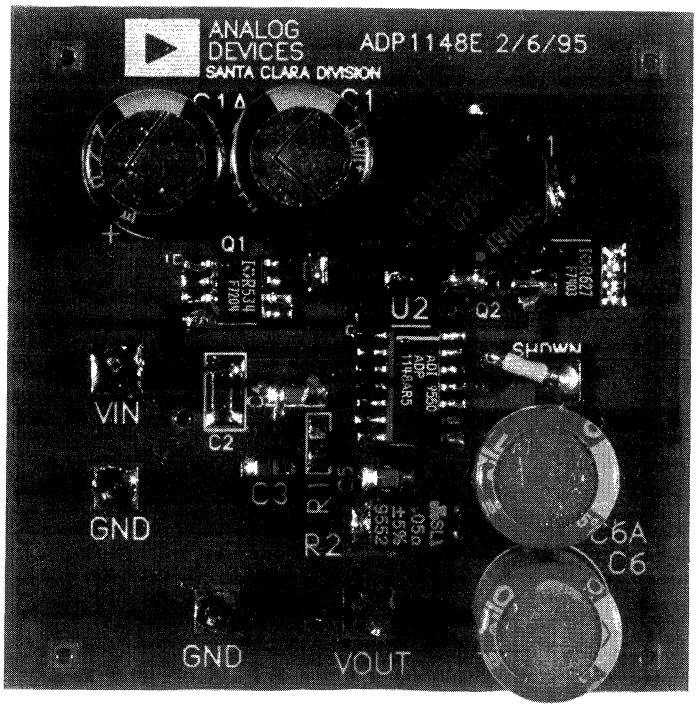

Figure 8.8

EVALUATION BOARD FOR ADP1148 SWITCHING REGULATOR - BOTTOM VIEW (GROUND PLANE)

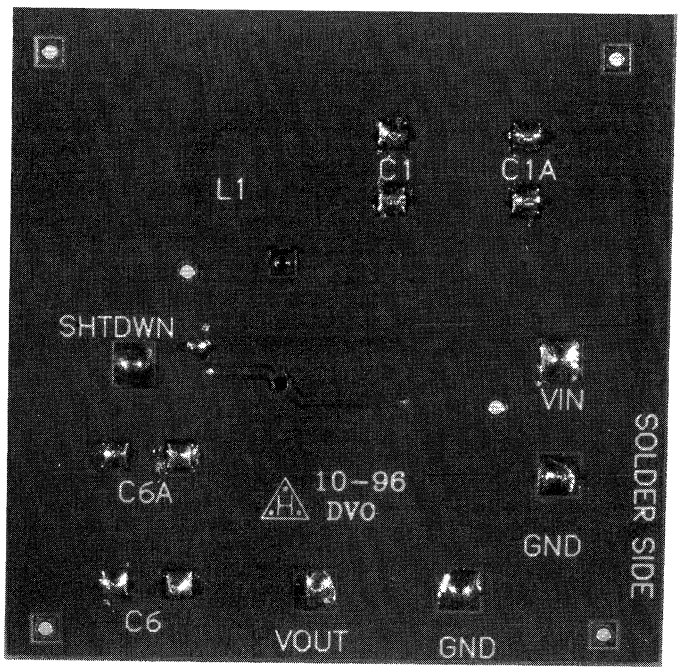

Figure 8.9

The bottom side of the board (ground plane, or "solder side") is shown in Figure 8.9. Note that with the exception of a single crossover and a few vias, the entire layer is ground plane. This in conjunction with the compact layout ensures that high frequency ground currents generated by the switching action of the regulator are localized to prevent EMI/RFI.

Evaluation boards can range from relatively simple ones (linear regulators, for example) to rather complex ones for mixed-signal ICs such as A/D converters. ADC evaluation boards often have on-board memory and DSPs for analyzing the ADC performance. Software is often provided with these more complex evaluation boards so that they can interface with a personal computer to perform complex signal analysis such as histogram and FFT testing.

In summary, good analog designers utilize as many tools as possible to ensure that the final system design performs correctly. The first step is the intelligent use of IC macromodels, where available, to simulate the circuit. The second step is the construction of a prototype board to further verify the design and the simulation. The final PCB layout should be then be based on the prototype layout as much as possible.

Finally, evaluation boards can be extremely useful in evaluating new analog ICs, and allow designers to verify the IC performance with a minimum amount of effort. The layout of the components on the evaluation board can serve as a guide to both the prototype and the final PC board layout. Gerber files are generally available for all evaluation board layouts and may be obtained at no charge.

REFERENCES: SIMULATION, PROTOTYPING, AND EVALUATION BOARDS

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2. **Amplifier Applications Guide**, Section 13, Analog Devices, Inc., Norwood, MA, 1992.

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MicroSim Corporation, 20 Fairbanks, Irvine, CA 92718, 714-770-3022

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7. Vector Electronic Company, 12460 Gladstone Ave., Sylmar, CA 91342, Tel. 818-365-9661, Fax. 818-365-5718.

8. RDI Wainwright, 69 Madison Ave., Telford, PA, 18969-1829, Tel. 215-723-4333, Fax. 215-723-4620.

   Wainwright Instruments GmbH, Widdersberger Strasse 14, DW-8138 Andechs-Frieding, Germany. Tel: +49-8152-3162, Fax: +49-8152-40525.

9. Schematic Capture and Layout Software:
   PADS Software, INC, 165 Forest St., Marlboro, MA, 01752 and ACCEL Technologies, Inc., 6825 Flanders Dr., San Diego, CA, 92121

10. Prototype Board Cutters:

    LPKF CAD/CAM Systems, Inc., 1800 NW 169th Place, Beaverton, OR, 97006 and
    T-Tech, Inc., 5591-B New Peachtree Road, Atlanta, GA, 34341

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GROUNDING TECHNIQUES FOR REGULATOR CIRCUITS
Walt Kester, Walt Jung

The importance of maintaining a low impedance large area ground plane is critical to practically all analog circuits today, especially high current low dropout linear regulators or switching regulators. The ground plane not only acts as a low impedance return path for high frequency switching currents but also minimizes EMI/RFI emissions. In addition, it serves to minimize unwanted voltage drops due to high load currents. Because of the shielding action of the ground plane, the circuit's susceptibility to external EMI/RFI is also reduced. When using multilayer PC boards, it is wise to add a power plane. In this way, low impedances can be maintained on both critical layers.

Figure 8.10 shows a grounding arrangement for a low dropout linear regulator such as the ADP3310. It is important to minimize the total voltage drop between the input voltage and the load, as this drop will subtract from the voltage dropped across the pass transistor and reduce its headroom. For this reason, these runs should be wide, heavy traces and are indicated by the wide interconnection lines on the diagram. The low-current ground (GND) and V_{OUT} (sense) pins of the ADP3310 are connected directly to the load so that the regulator regulates the voltage at the load rather than at its own output. The IS and V_{IN} connections to the R_S current sense resistor should be made directly to the resistor terminals to minimize parasitic resistance, since the current limit resistor is typically a very low value (milliohms). In fact, for very low values it may actually consist of a PC board trace of the proper width, length, and thickness to yield the desired resistance.

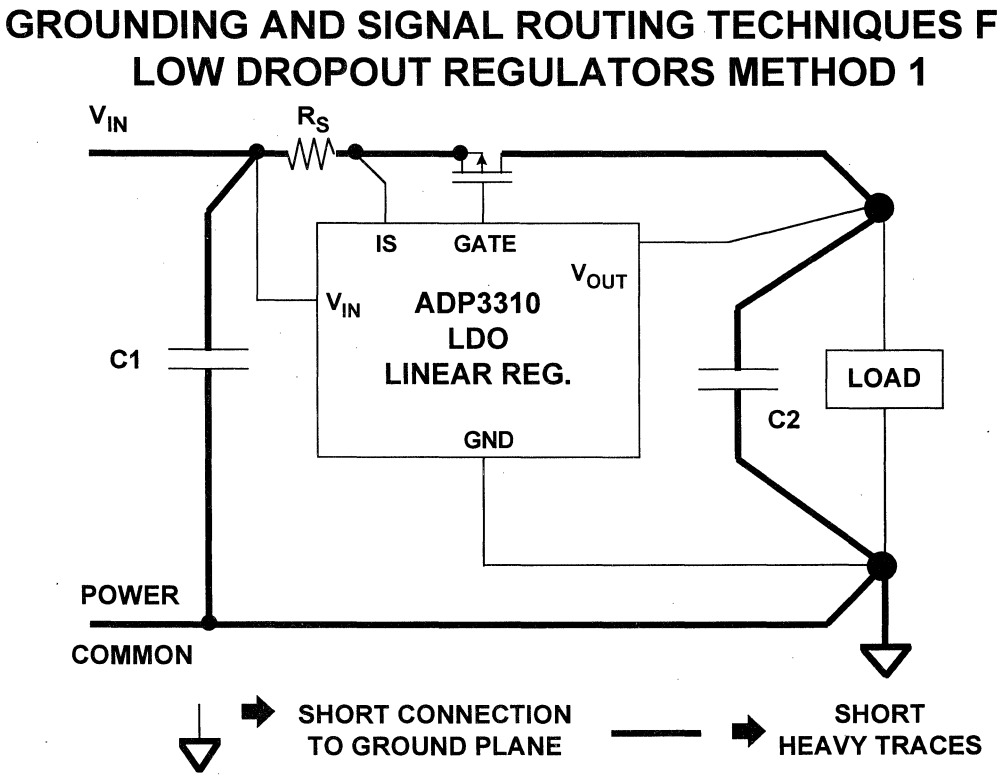

Figure 8.10

The input decoupling capacitor (C1) should be connected with short leads at the regulator input in order to absorb any transients which may couple onto the input voltage line. Similarly, the load capacitor (C2) should have minimum lead length in order to absorb transients at that point and prevent them from coupling back into the regulator. The single-point connection to the low impedance ground plane is made directly at the load.

Figure 8.11 shows a grounding arrangement which is similar to that of Figure 8.10 with the exception that all ground connections are made with direct connections to the ground plane. This method works extremely well when the regulator and the load are on the same PC board, and the load is distributed around the board rather than located at one specific point. If the load is not distributed, the connection from V_{OUT} (sense) should be connected directly to the load as shown by the dotted line in the diagram. This ensures the regulator provides the proper voltage at the load regardless of the drop in the trace connecting the pass transistor output to the load.

GROUNDING AND SIGNAL ROUTING FOR LOW DROPOUT REGULATOR METHOD 2

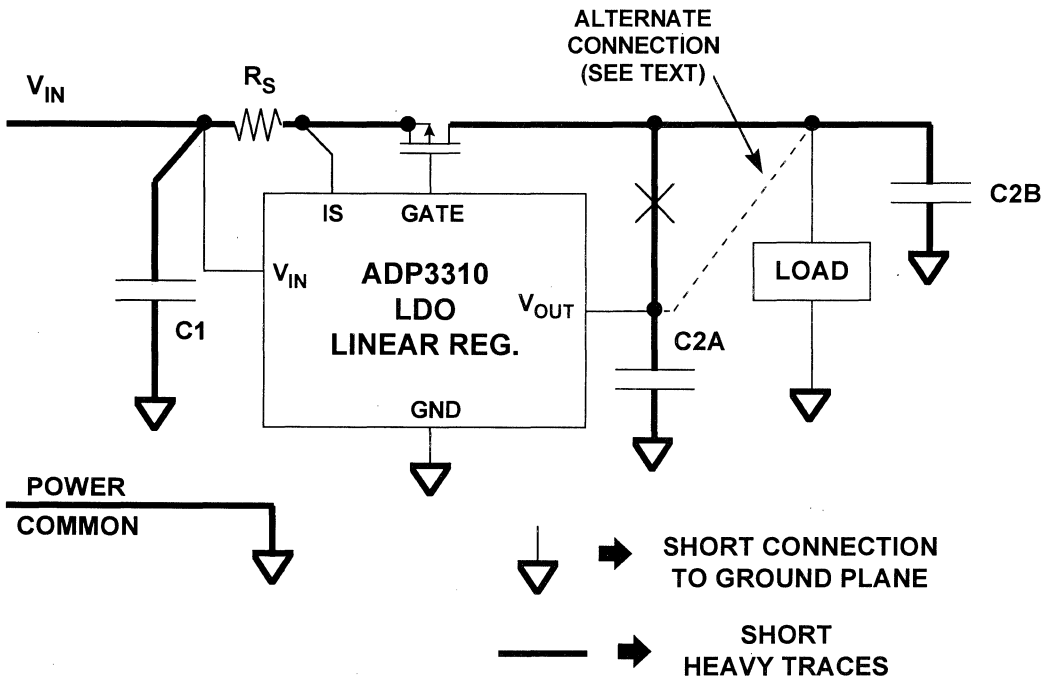

Figure 8.11

Switching regulators present major challenges with respect to layout, grounding, and filtering. The discussion above on linear regulators applies equally to switchers, although the importance of DC voltage drops may not be as great.

There is no way to eliminate high frequency switching currents in a switching regulator, since they are necessary for the proper operation of the regulator. What one must do, however, is to recognize the high switching current paths and take proper measures to ensure that they do not corrupt circuits on other parts of the

board or system. Figure 8.12 shows a generic synchronous switching regulator controller IC and the associated external MOSFET switching transistors. The heavy bold lines indicate the paths where there are large switching currents and/or high DC currents. Notice that all these paths are connected together at a single-point ground which in turn connects to a large area ground plane.

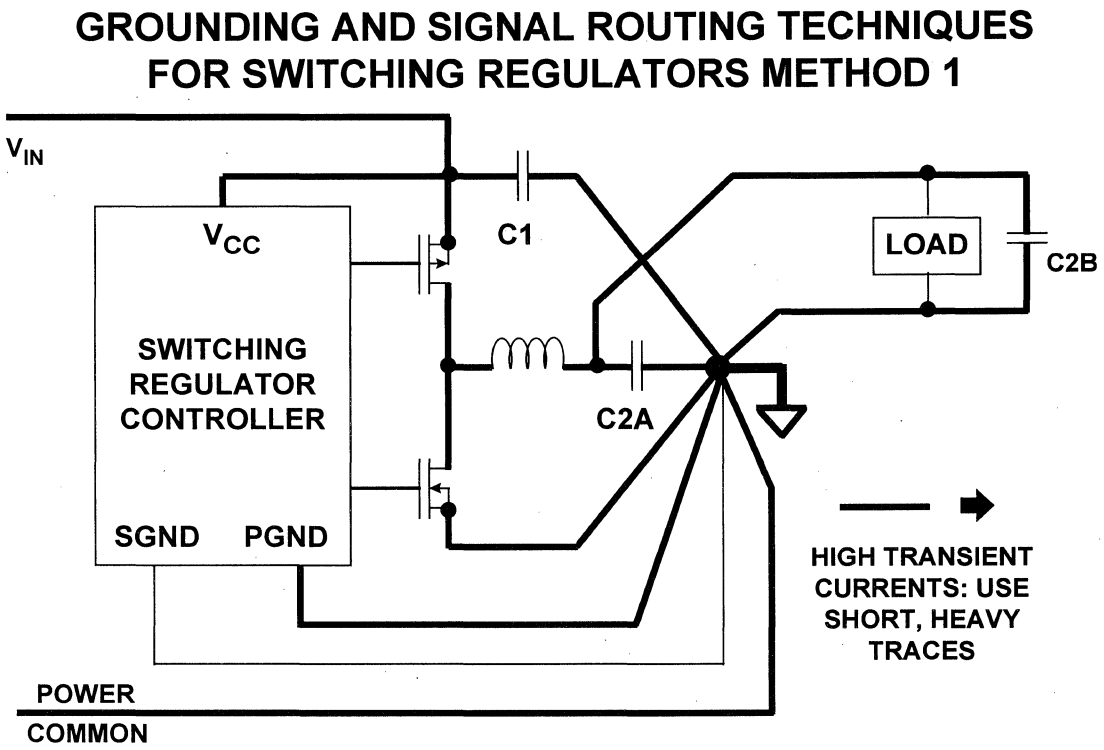

Figure 8.12

In order to minimize stray inductance and resistance, each of the high current paths should be as short as possible. Capacitors C1 and C2A must absorb the bulk or the input and output switching current and shunt it to the single-point ground. Any additional resistance or inductance in series with these capacitors will degrade their effectiveness. Minimizing the area of all the loops containing the switching currents prevents them from significantly affecting other parts of the circuit. In actual practice, however, the single-point concept in Figure 8.12 is difficult to implement without adding additional lead length in series with the various components. The added lead length required to implement the single-point grounding scheme tends to degrade the effects of using the single-point ground in the first place.

A more practical solution is to make multiple connections to the ground plane and make each of them as short as possible. This leads to the arrangement shown in Figure 8.13, where each critical ground connection is made directly to the ground plane with the shortest connection length possible. By physically locating all critical components associated with the regulator close together and making the ground connections short, stray series inductance and resistance are minimized. It is true that several small ground loops may occur using this approach, but they should not cause significant system problems because they are confined to a very small area of the overall ground plane. Refer back to Figure 8.9 (ADP1148 switching regulator

evaluation board - ground plane side) and note that this approach to grounding was used.

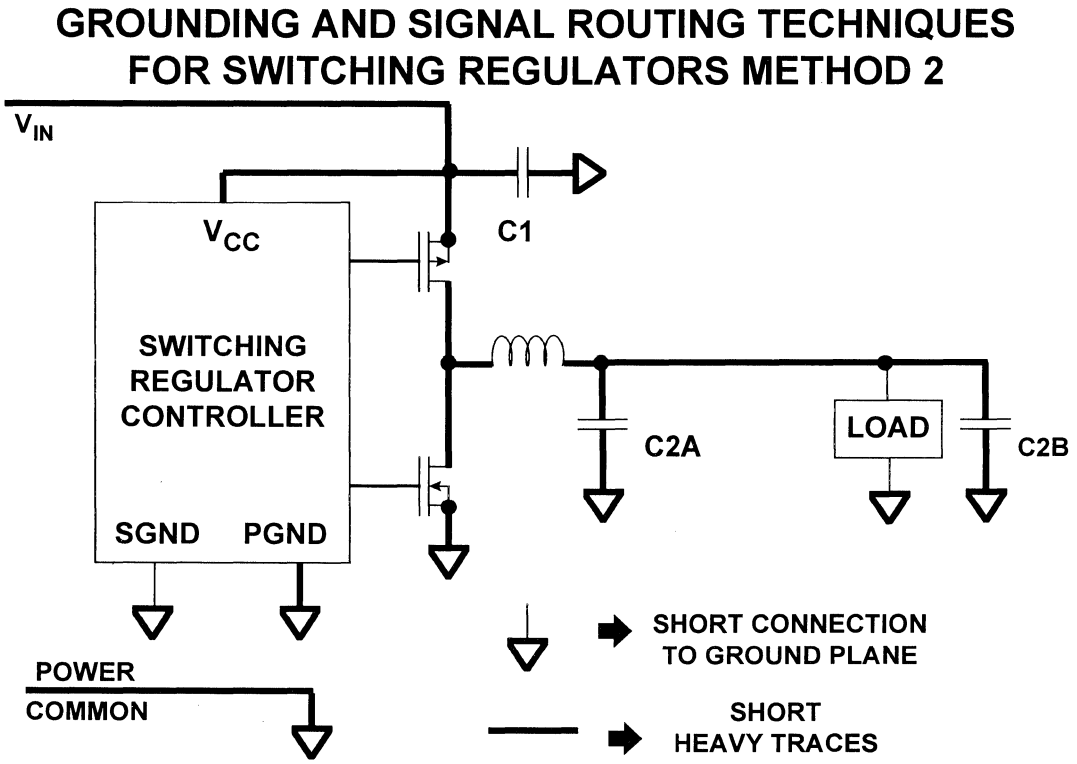

Figure 8.13

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POWER SUPPLY NOISE REDUCTION AND FILTERING

Walt Jung, Walt Kester, Bill Chestnut

Precision analog circuitry has traditionally been powered from well regulated, low noise linear power supplies. During the last decade however, switching power supplies have become much more common in electronic systems. As a consequence, they also are being used for analog supplies. Good reasons for the general popularity include their high efficiency, low temperature rise, small size, and light weight.

In spite of these benefits, switchers *do* have drawbacks, most notably high output noise. This noise generally extends over a broad band of frequencies, resulting in both conducted and radiated noise, as well as unwanted electric and magnetic fields. Voltage output noise of switching supplies are short-duration voltage transients, or spikes. Although the fundamental switching frequency can range from 20kHz to 1MHz, the spikes can contain frequency components extending to 100MHz or more. While specifying switching supplies in terms of RMS noise is common vendor practice, as a user you should also specify the *peak* (or p-p) amplitudes of the switching spikes, with the output loading of your system.

The following section discusses filter techniques for rendering a switching regulator output *analog ready*, that is sufficiently quiet to power precision analog circuitry with relatively small loss of DC terminal voltage. The filter solutions presented are generally applicable to all power supply types incorporating switching element(s) in their energy path. This includes various DC-DC converters as well as popular 5V (PC type) supplies.

An understanding of the EMI process is necessary to understand the effects of supply noise on analog circuits and systems. Every interference problem has a *source*, a *path*, and a *receptor* [Reference 1]. In general, there are three methods for dealing with interference. First, source emissions can be minimized by proper layout, pulse-edge rise time control/reduction, filtering, and proper grounding. Second, radiation and conduction paths should be reduced through shielding and physical separation. Third, receptor immunity to interference can be improved, via supply and signal line filtering, impedance level control, impedance balancing, and utilizing differential techniques to reject undesired common-mode signals. This section focuses on reducing switching power supply noise with external post filters.

Tools useful for combating high frequency switcher noise are shown by Figure 8.14. They differ in electrical characteristics as well as practicality towards noise reduction, and are listed roughly in an order of priorities. Of these tools, L and C are the most powerful filter elements, and are the most cost-effective, as well as small sized.

SWITCHING REGULATOR NOISE REDUCTION TOOLS

- **Capacitors**
- **Inductors**
- **Ferrites**
- **Resistors**
- **Linear Post Regulation**
- **Proper Layout and Grounding Techniques**
- **PHYSICAL SEPARATION FROM SENSITIVE ANALOG CIRCUITS!!**

Figure 8.14

Capacitors are probably the single most important filter component for switchers. There are many different types of capacitors, and an understanding of their individual characteristics is absolutely mandatory to the design of effective practical supply filters. There are generally three classes of capacitors useful in 10kHz-100MHz filters, broadly distinguished as the generic dielectric types; *electrolytic*, *film*, and *ceramic*. These can in turn can be further sub-divided. A thumbnail sketch of capacitor characteristics is shown in the chart of Figure 8.15.

TYPES OF CAPACITORS

	Aluminum Electrolytic (General Purpose)	Aluminum Electrolytic (Switching Type)	Tantalum Electrolytic	OS-CON Electrolytic	Polyester (Stacked Film)	Ceramic (Multilayer)
Size	100 µF	120 µF	120 µF	100 µF	1 µF	0.1 µF
Rated Voltage	25 V	25 V	20 V	20 V	400 V	50 V
ESR	0.6 Ω @ 100 kHz	0.18 Ω @ 100 kHz	0.12 Ω @ 100 kHz	0.02 Ω @ 100 kHz	0.11 Ω @ 1 MHz	0.12 Ω @ 1 MHz
Operating Frequency (*)	≅ 100 kHz	≅ 500 kHz	≅ 1 MHz	≅ 1 MHz	≅ 10 MHz	≅ 1 GHz

(*) Upper frequency strongly size and package dependent

Figure 8.15

With any dielectric, a major potential filter loss element is ESR (equivalent series resistance), the net parasitic resistance of the capacitor. ESR provides an ultimate limit to filter performance, and requires more than casual consideration, because it can vary both with frequency and temperature in some types. Another capacitor loss element is ESL (equivalent series inductance). ESL determines the frequency where the net impedance characteristic switches from capacitive to inductive. This varies from as low as 10kHz in some electrolytics to as high as 100MHz or more in chip ceramic types. Both ESR and ESL are minimized when a leadless package is used. All capacitor types mentioned are available in surface mount packages, preferable for high speed uses.

The *electrolytic* family provides an excellent, cost-effective low-frequency filter component, because of the wide range of values, a high capacitance-to-volume ratio, and a broad range of working voltages. It includes *general purpose aluminum electrolytic* types, available in working voltages from below 10V up to about 500V, and in size from 1 to several thousand μF (with proportional case sizes). All electrolytic capacitors are polarized, and thus cannot withstand more than a volt or so of reverse bias without damage. They also have relatively high leakage currents (up to tens of μA, and strongly dependent upon design specifics).

A subset of the general electrolytic family includes *tantalum* types, generally limited to voltages of 100V or less, with capacitance of 500μF or less[Reference 3]. In a given size, tantalums exhibit a higher capacitance-to-volume ratios than do general purpose electrolytics, and have both a higher frequency range and lower ESR. They are generally more expensive than standard electrolytics, and must be carefully applied with respect to surge and ripple currents.

A subset of aluminum electrolytic capacitors is the *switching* type, designed for handling high pulse currents at frequencies up to several hundred kHz with low losses [Reference 4]. This capacitor type competes directly with tantalums in high frequency filtering applications, with the advantage of a broader range of values.

A more specialized high performance aluminum electrolytic capacitor type uses an organic semiconductor electrolyte [Reference 5]. The *OS-CON* capacitors feature appreciably lower ESR and higher frequency range than do other electrolytic types, with an additional feature of low low-temperature ESR degradation.

Film capacitors are available in very broad value ranges and an array of dielectrics, including polyester, polycarbonate, polypropylene, and polystyrene. Because of the low dielectric constant of these films, their volumetric efficiency is quite low, and a 10μF/50V polyester capacitor (for example) is actually a handful. Metalized (as opposed to foil) electrodes does help to reduce size, but even the highest dielectric constant units among film types (polyester, polycarbonate) are still larger than any electrolytic, even using the thinnest films with the lowest voltage ratings (50V). Where film types excel is in their low dielectric losses, a factor which may not necessarily be a practical advantage for filtering switchers. For example, ESR in film capacitors can be as low as 10mΩ or less, and the behavior of films generally is very high in terms of Q. In fact, this can cause problems of spurious resonance in filters, requiring damping components.

Typically using a wound layer-type construction, film capacitors can be inductive, which can limit their effectiveness for high frequency filtering. Obviously, only non-inductively made film caps are useful for switching regulator filters. One specific style which is non-inductive is the *stacked-film* type, where the capacitor plates are cut as small overlapping linear sheet sections from a much larger wound drum of dielectric/plate material. This technique offers the low inductance attractiveness of a plate sheet style capacitor with conventional leads [see References 4, 5, 6]. Obviously, minimal lead length should be used for best high frequency effectiveness. Very high current polycarbonate film types are also available, specifically designed for switching power supplies, with a variety of low inductance terminations to minimize ESL [Reference 7].

Dependent upon their electrical and physical size, film capacitors can be useful at frequencies to well above 10MHz. At the highest frequencies, only stacked film types should be considered. Some manufacturers are now supplying film types in leadless surface mount packages, which eliminates the lead length inductance.

Ceramic is often the capacitor material of choice above a few MHz, due to its compact size, low loss, and availability up to several μF in the high-K dielectric formulations (X7R and Z5U), at voltage ratings up to 200V [see ceramic families of Reference 3]. NP0 (also called COG) types use a lower dielectric constant formulation, and have nominally zero TC, plus a low voltage coefficient (unlike the less stable high-K types). NP0 types are limited to values of 0.1μF or less, with 0.01μF representing a more practical upper limit.

Multilayer ceramic "chip caps" are very popular for bypassing/ filtering at 10MHz or more, simply because their very low inductance design allows near optimum RF bypassing. For smaller values, ceramic chip caps have an operating frequency range to 1GHz. For high frequency applications, a useful selection can be ensured by selecting a value which has a self-resonant frequency *above* the highest frequency of interest.

All capacitors have some finite ESR. In some cases, the ESR may actually be helpful in reducing resonance peaks in filters, by supplying "free" damping. For example, in most electrolytic types, a nominally flat broad series resonance region can be noted in an impedance vs. frequency plot. This occurs where $|Z|$ falls to a minimum level, nominally equal to the capacitor's ESR at that frequency. This low Q resonance can generally be noted to cover a relatively wide frequency range of several octaves. Contrasted to the very high Q sharp resonances of film and ceramic caps, the low Q behavior of electrolytics can be useful in controlling resonant peaks.

In most electrolytic capacitors, ESR degrades noticeably at low temperature, by as much as a factor of 4-6 times at –55°C vs. the room temperature value. For circuits where ESR is critical to performance, this can lead to problems. Some specific electrolytic types do address this problem, for example within the HFQ switching types, the –10°C ESR at 100kHz is no more than 2× that at room temperature. The OSCON electrolytics have a ESR vs. temperature characteristic which is relatively flat.

As noted, all real capacitors have parasitic elements which limit their performance. The equivalent electrical network representing a real capacitor models both ESR and ESL as well as the basic capacitance, plus some shunt resistance (see Figure 8.16). In such a practical capacitor, at low frequencies the net impedance is almost purely capacitive. At intermediate frequencies, the net impedance is determined by ESR, for example about 0.12Ω to 0.4Ω at 125kHz, for several types. Above about 1MHz these capacitor types become inductive, with impedance dominated by the effect of ESL. All electrolytics will display impedance curves similar in general shape to that of Figure 8.17. The minimum impedance will vary with the ESR, and the inductive region will vary with ESL (which in turn is strongly effected by package style).

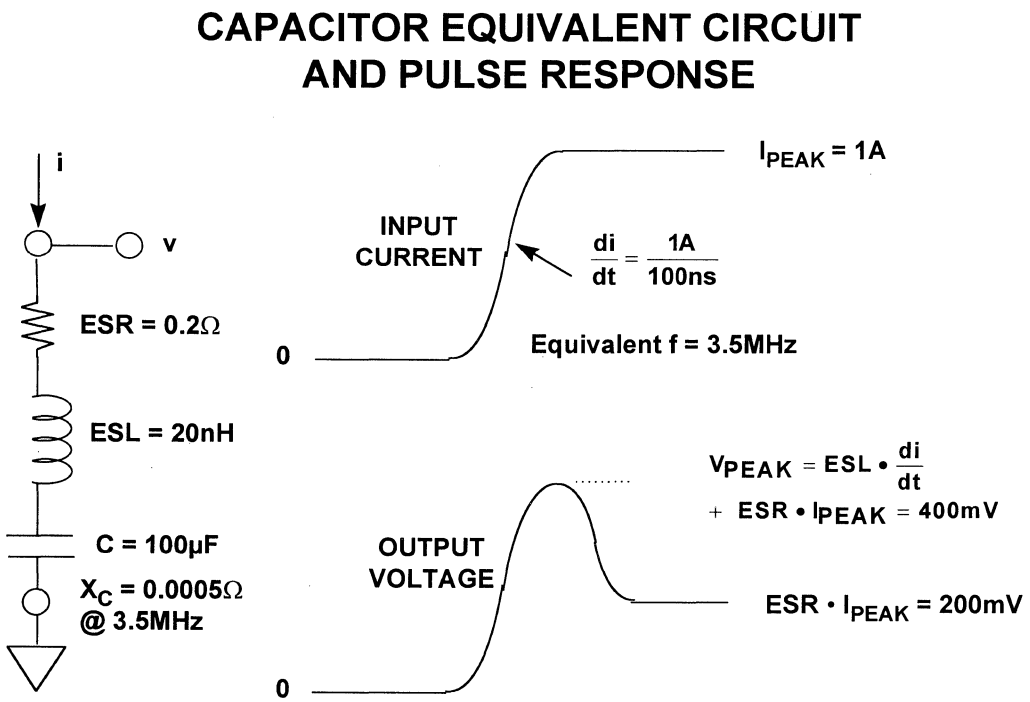


Figure 8.16

Regarding inductors, *Ferrites* (non-conductive ceramics manufactured from the oxides of nickel, zinc, manganese, or other compounds) are extremely useful in power supply filters [Reference 9]. At low frequencies (<100kHz), ferrites are inductive; thus they are useful in low-pass LC filters. Above 100kHz, ferrites become resistive, an important characteristic in high-frequency filter designs. Ferrite impedance is a function of material, operating frequency range, DC bias current, number of turns, size, shape, and temperature. Figure 8.18 summarize a number of ferrite characteristics.

ELECTROLYTIC CAPACITOR IMPEDANCE VERSUS FREQUENCY

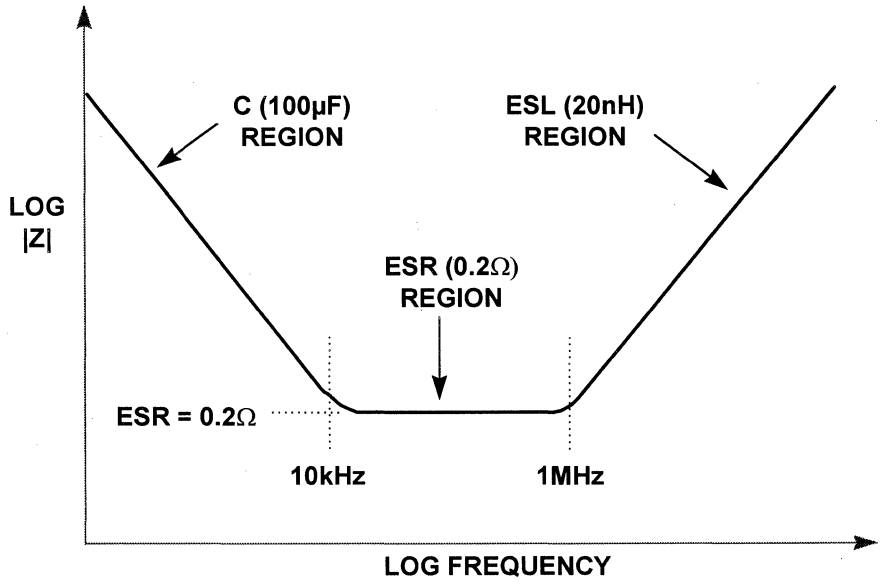


Figure 8.17

FERRITES SUITABLE FOR HIGH FREQUENCY FILTERS

- Ferrites Good for Frequencies Above 25kHz
- Many Sizes and Shapes Available Including Leaded "Resistor Style"
- Ferrite Impedance at High Frequencies Primarily Resistive -- Ideal for HF Filtering
- Low DC Loss: Resistance of Wire Passing Through Ferrite is Very Low
- High Saturation Current Versions Available
- Choice Depends Upon:
  - Source and Frequency of Interference
  - Impedance Required at Interference Frequency
  - Environmental: Temperature, AC and DC Field Strength, Size / Space Available
- Always Test the Design!

Figure 8.18

Several ferrite manufacturers offer a wide selection of ferrite materials from which to choose, as well as a variety of packaging styles for the finished network (see References 10 and 11). A simple form is the *bead* of ferrite material, a cylinder of the ferrite which is simply slipped over the power supply lead to the decoupled stage. Alternately, the *leaded ferrite bead* is the same bead, pre-mounted on a length of wire and used as a component (see Reference 11). More complex beads offer multiple holes through the cylinder for increased decoupling, plus other variations. Surface mount beads are also available.

PSpice ferrite models for Fair-Rite materials are available, and allow ferrite impedance to be estimated [see Reference 12]. These models have been designed to match measured impedances rather than theoretical impedances.

A ferrite's impedance is dependent upon a number of inter-dependent variables, and is difficult to quantify analytically, thus selecting the proper ferrite is not straightforward. However, knowing the following system characteristics will make selection easier. First, determine the frequency range of the noise to be filtered. Second, the expected temperature range of the filter should be known, as ferrite impedance varies with temperature. Third, the DC current flowing through the ferrite must be known, to ensure that the ferrite does not saturate. Although models and other analytical tools may prove useful, the general guidelines given above, coupled with some experimentation with the actual filter connected to the supply output under system load conditions, should lead to a proper ferrite selection.

Using proper component selection, low and high frequency band filters can be designed to smooth a noisy switcher's DC output so as to produce an *analog ready* 5V supply. It is most practical to do this over two (and sometimes more) stages, each stage optimized for a range of frequencies. A basic stage can be used to carry all of the DC load current, and filter noise by 60dB or more up to a 1-10MHz range. This larger filter is used as a *card entry filter* providing broadband filtering for all power entering a PC card. Smaller, more simple local filter stages are also used to provide higher frequency decoupling right at the power pins of individual stages.

SWITCHING REGULATOR EXPERIMENTS

In order to better understand the challenge of filtering switching regulators, a series of experiments were conducted with representative devices (see Figure 8.19).

The first series of experiments were conducted on a low power switching regulator, the ADP3000. The regulator was tested in the boost configuration with a 2V input and a 5V/100mA output. The prototype board shown previously in Figures 8.4 and 8.5 was used for the tests.

The second series of experiments were conducted on the ADP3000 configured in the buck mode with a 9V input and a 5V/100mA output. Again, the prototype board shown previously in Figures 8.4 and 8.5 was used for the tests.

The third series of experiments involved the ADP1148 synchronous buck regulator with a 9V input and a 3.3V/1A output. An evaluation board similar to that shown in Figures 8.8 and 8.9 was used.

The fourth series of experiments were conducted on the ADP1148 synchronous buck regulator driving an ADP3310 low dropout linear regulator. The ADP1148 was configured for a 9V input and a 3.75V/1A output, and the ADP3310 for a 3.3V/1A output.

The fifth series of experiments were made on the ADP3605 +5V to –3V switched capacitor voltage converter. The ADP3605 output load was set for 100mA.

FILTERING SWITCHING REGULATOR OUTPUTS - SUMMARY OF EXPERIMENTS

- **ADP3000, 2V to 5V/100mA Boost Regulator**
- **ADP3000, 9V to 5V/100mA Buck Regulator**
- **ADP1148, 9V to 3.3V/1A Buck Regulator**
- **ADP1148, 9V to 3.75V/1A Buck Regulator with ADP3310, 3.3V/1A Linear LDO Post Regulator**
- **ADP3605, 5V to –3V/100mA Switched Capacitor Voltage Converter**

Figure 8.19

In addition to observing typical input and output waveforms, the objective of these experiments was to reduce the output ripple to less than 10mV peak-to-peak, a value suitable for driving most analog circuits.

Measurements were made using a Tektronix wideband digitizing oscilloscope with the input bandwidth limited to 20MHz so that the ripple generated by the switching

regulators could be more readily observed. In a system, power supply ripple frequencies above 20MHz are best filtered locally at each IC power pin with a low inductance ceramic capacitor and perhaps a series-connected ferrite bead.

Probing techniques are critical for accurate ripple measurements. A standard passive 10X probe was used with a "bayonet" probe tip adapter for making the ground connection as short as possible (see Figure 8.20). Use of the "ground clip lead" is not recommended in making this type of measurement because the lead length in the ground connection forms an unwanted inductive loop which picks up high frequency switching noise, thereby corrupting the signal being measured.

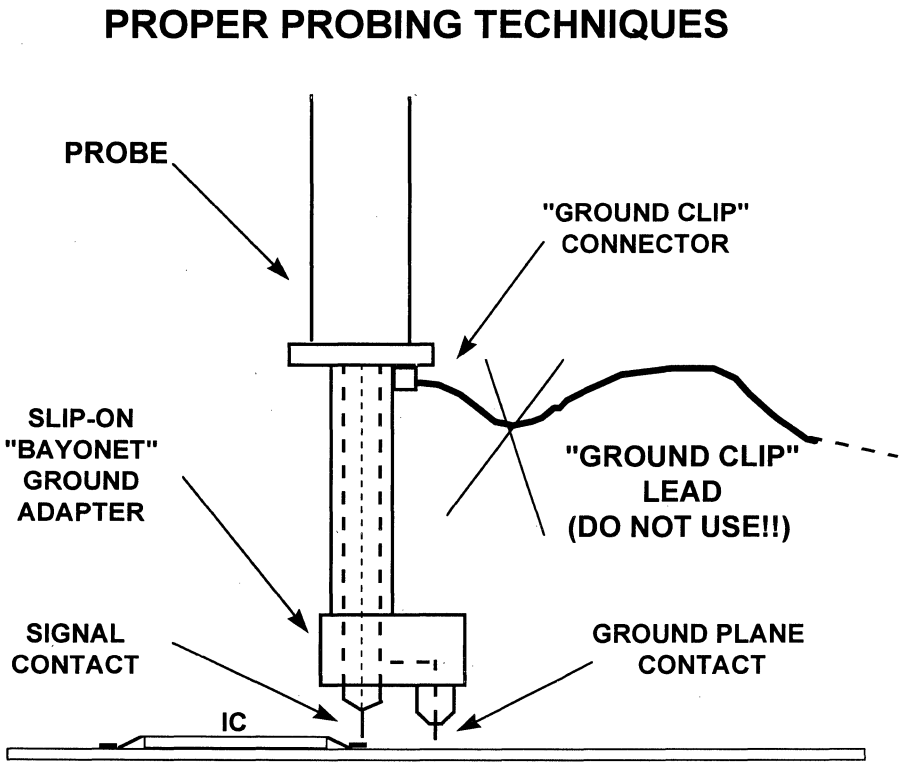


Figure 8.20

Note: Schematic representation of proper physical grounding is almost impossible. In all the following circuit schematics, the connections to ground are made to the ground plane using the shortest possible connecting path, regardless of how they are indicated in the actual circuit schematic diagram.

8

ADP3000 2V TO 5V/100MA BOOST REGULATOR

Figure 8.21 shows the connection diagram for the ADP3000 used as a 2V to 5V/100mA boost regulator. The actual switch is internal to the device. Multiple capacitors are used on both the input and output in order to lower the ESR and ESL.

ADP3000 2V TO 5V BOOST REGULATOR

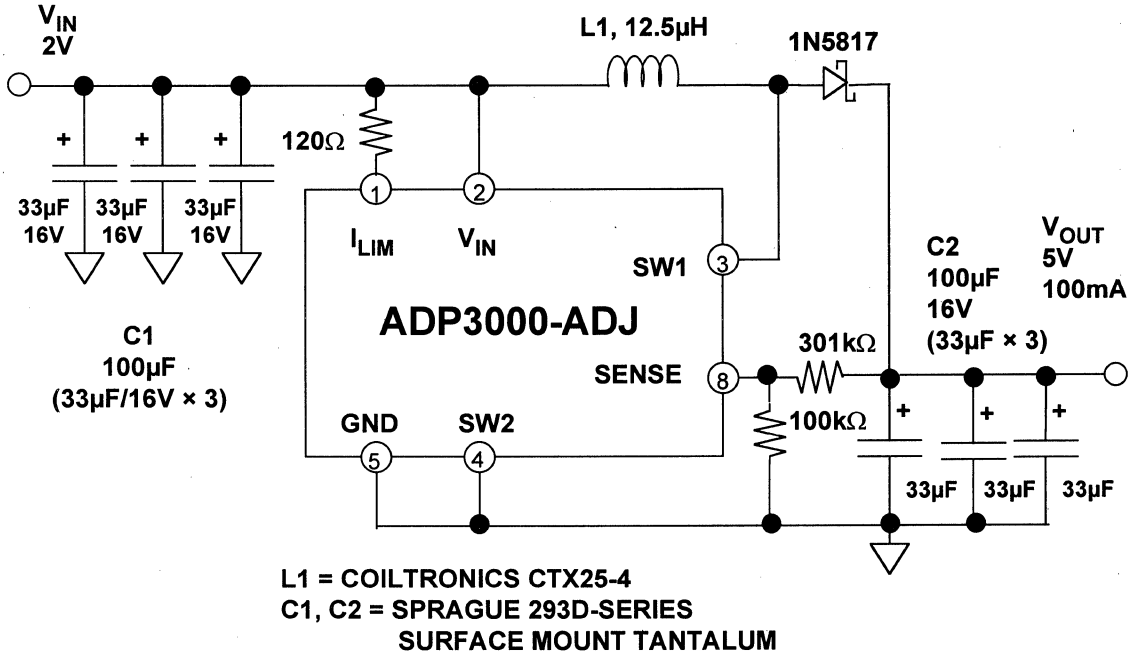
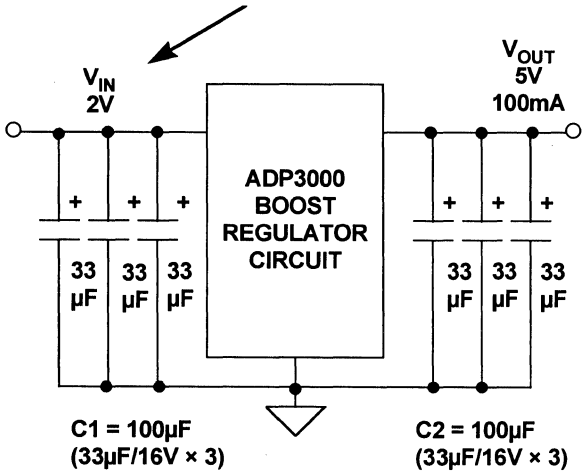


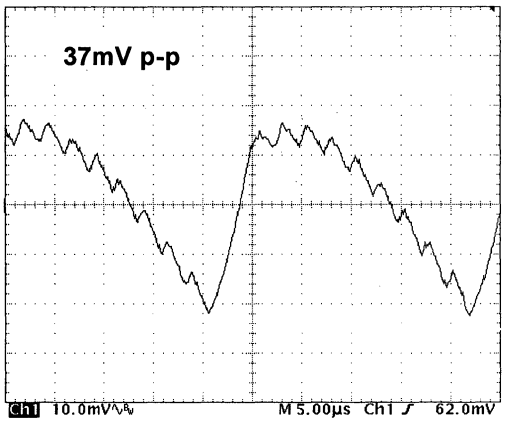
Figure 8.21

The input waveform of the boost regulator is shown in Figure 8.22 and is typical of the gated-oscillator type of regulation used in the ADP3000. It consists of series of gradually decreasing ramp waveforms during the time the inductor is being switched at the 400kHz internal oscillator rate. When the output voltage reaches the proper value, the internal oscillator is turned off, and the input capacitors recharge, as indicated by the positive-going ramp voltage. During this interval, the output voltage gradually decays until the point at which the internal oscillator is gated on again, and the cycle repeats itself.

The output waveform for the circuit is shown in Figure 8.23. This waveform is also characteristic of gated-oscillator boost regulators as indicated by the pulsating waveforms followed by the decaying ramp voltage. It should be noted that the ripple in this waveform is almost entirely determined by the equivalent ESR of the parallel combination of the output capacitors. Adding more capacitors would reduce the ripple, but a more effective method is to add an LC filter on the output as shown in Figure 8.24.

ADP3000 - BOOST INPUT WAVEFORM



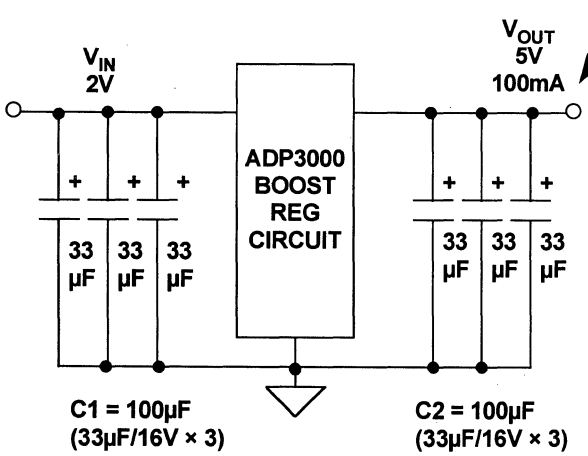


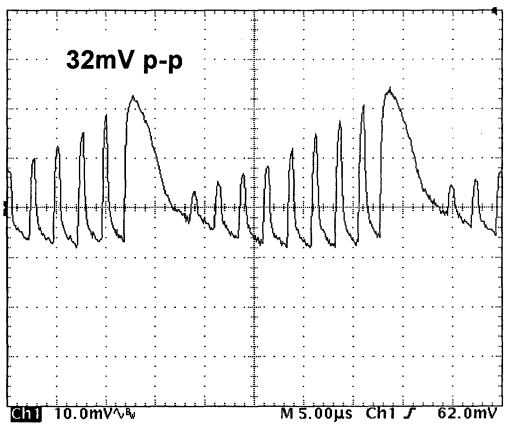
VERTICAL SCALE: 10mV / DIV
HORIZ. SCALE: 5µs / DIV

C1 = C2 = 33uF/16V x 3 , SPRAGUE 293D SURFACE MOUNT TANTALUM

Figure 8.22

ADP3000 BOOST - OUTPUT WAVEFORM





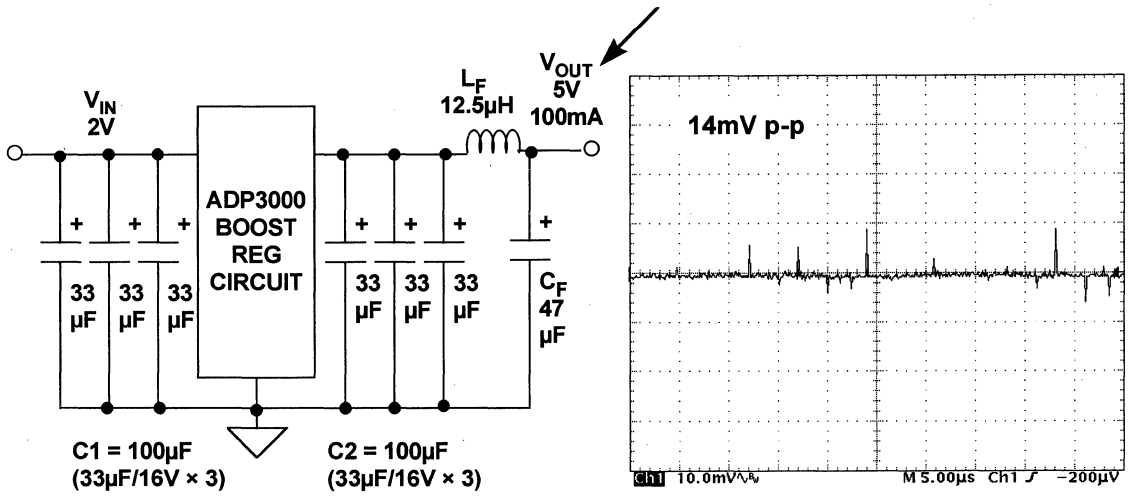
VERTICAL SCALE: 10mV / DIV
HORIZ. SCALE: 5µs / DIV

C1 = C2 = 33µF/16V x 3 , SPRAGUE 293D SURFACE MOUNT TANTALUM

Figure 8.23

8

ADP3000 BOOST FILTERED OUTPUT, CONDITION #1



VERTICAL SCALE: 10mV / DIV
HORIZ. SCALE: 5µs / DIV

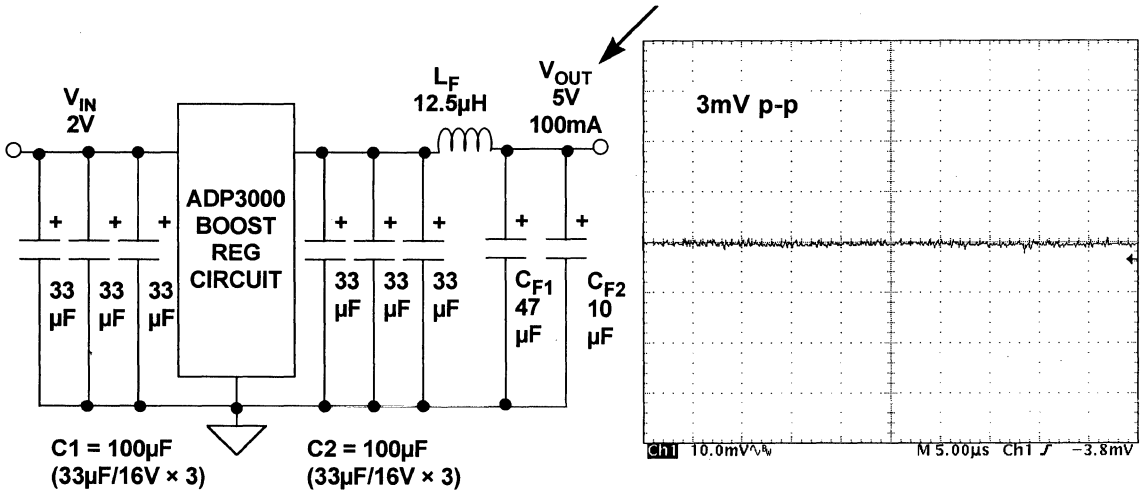
OUTPUT FILTER:
L_F = 12.5µH, COILTRONICS CTX25-4
C_F = 47µF/10V SURFACE MOUNT TANTALUM

Figure 8.24

The inductor selected (L_F = 12.5µH) was the same value and type used as the energy transfer inductor in the regulator circuit, thereby ensuring the inductor has adequate current-carrying capability. The capacitor (C_F = 47µF) was a surface mount tantalum. Peak-to-peak ripple was reduced from 32mV to 14 mV, consisting mostly of high frequency spikes. In order to reduce the high frequency spikes, a second capacitor (C_{F2} = 10µF) was added in parallel with the 47µF. This output filter combination reduced the ripple to approximately 3mV as shown in Figure 8.25. The ESL of the 10µF capacitor was approximately 2.2nH (Kemet T491C-series).

From this experiment, we concluded that the 47µF surface mount tantalum filter capacitor had an ESL/ESR combination which was not sufficiently low to remove the high frequency ripple components. The capacitor was removed and replaced with a 33µF tantalum (Sprague 293D-series). In addition, the regulator output capacitor (C2) was reduced to a single 33µF tantalum (also Sprague 293D-series). The resulting output waveform is shown in Figure 8.26. Note that the high frequency components have been removed, but a small amount of ripple remains at the frequency of the gated oscillator bursts (approximately 40kHz).

ADP3000 BOOST FILTERED OUTPUT, CONDITION #2

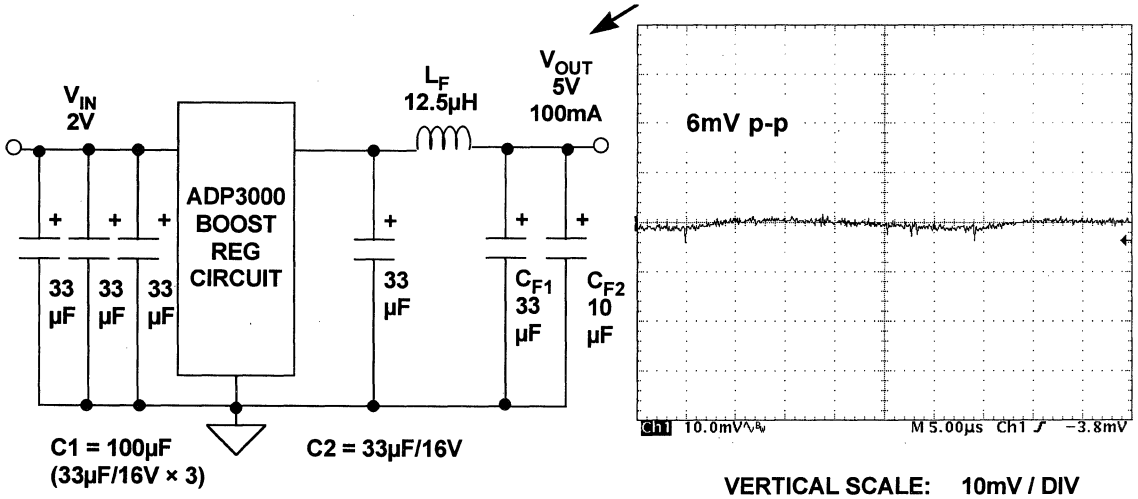


VERTICAL SCALE: 10mV / DIV
HORIZ. SCALE: 5µs / DIV

OUTPUT FILTER: L_F = 12.5µH, COILTRONICS CTX25-4
C_{F1} = 47µF/10V SURFACE MOUNT TANTALUM
C_{F2} = 10µF/16V SURFACE MOUNT TANTALUM, KEMET T491C SERIES

Figure 8.25

ADP3000 BOOST FILTERED OUTPUT, CONDITION #3



VERTICAL SCALE: 10mV / DIV
HORIZ. SCALE: 5µs / DIV

CHANGED C2 TO SINGLE 33µF/16V SURFACE MOUNT TANTALUM

OUTPUT FILTER: (CHANGED C_{F1})
L_F = 12.5µH, COILTRONICS CTX25-4
C_{F1} = 33µF/16V SURFACE MOUNT TANTALUM, SPRAGUE 293D SERIES
C_{F2} = 10µF/16V SURFACE MOUNT TANTALUM, KEMET T491C SERIES

Figure 8.26

ADP3000 9V TO 5V/100MA BUCK REGULATOR

The circuit for the ADP3000 9V to 5V/100mA buck regulator is shown in Figure 8.27. The input waveform is shown in Figure 8.28. Note that the pulsating waveform followed by an increasing ramp voltage is characteristic of the gated-oscillator buck input. The corresponding output waveform is shown in Figure 8.29. The output filter chosen (see Figure 8.30) consisted of a 12.5µH inductor followed by a 33µF capacitor in parallel with a 10µF capacitor (identical to the filter used in the circuit shown in Figure 8.26). The ripple was reduced from 30mV to approximately 6mV peak-to-peak.

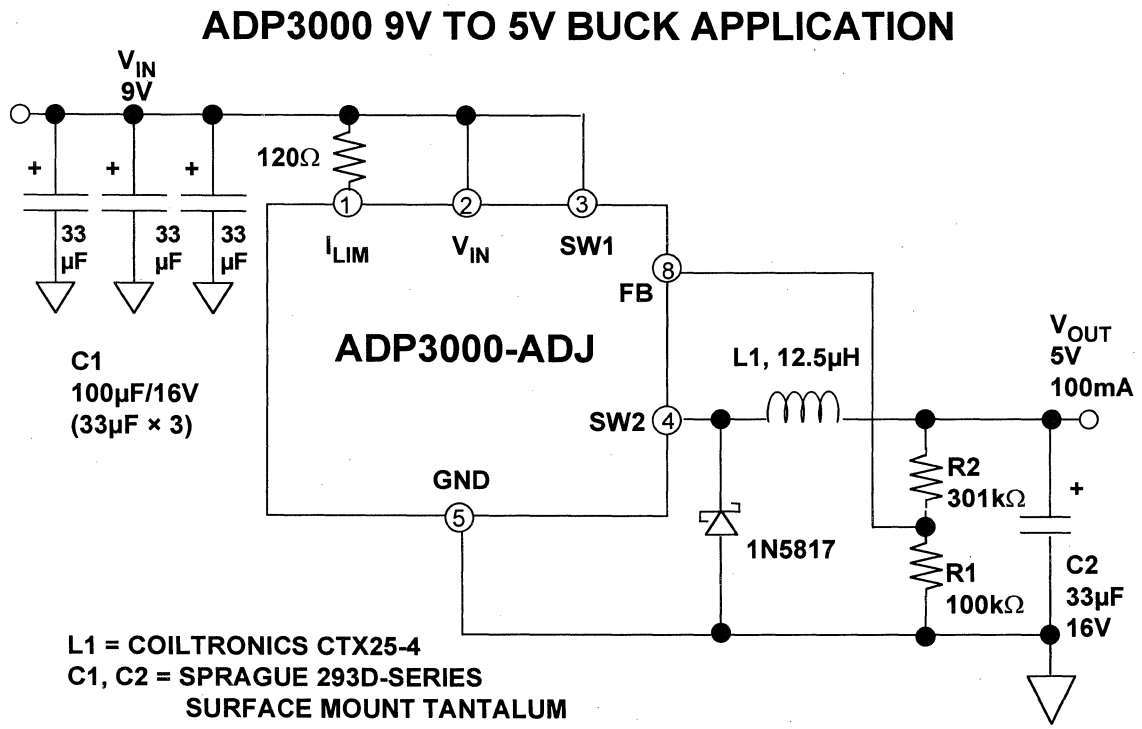
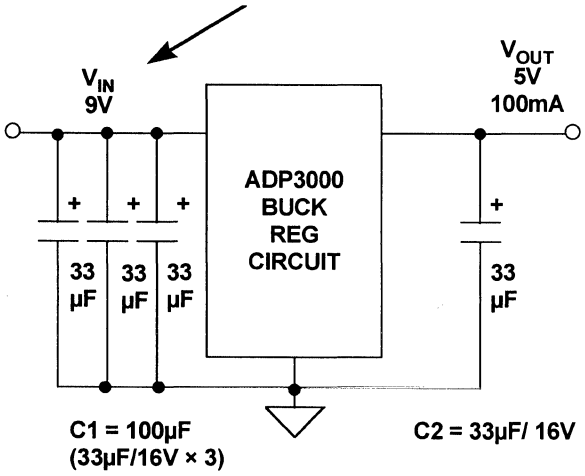
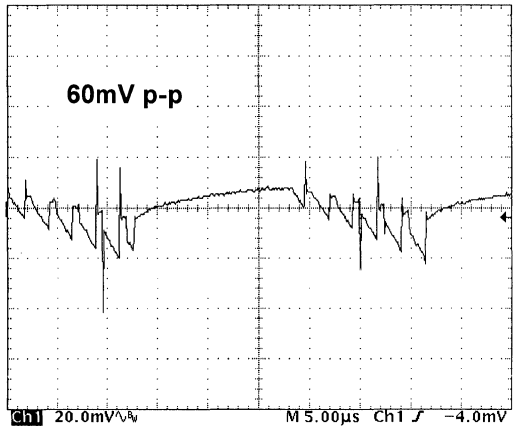


Figure 8.27

ADP3000 BUCK INPUT WAVEFORM



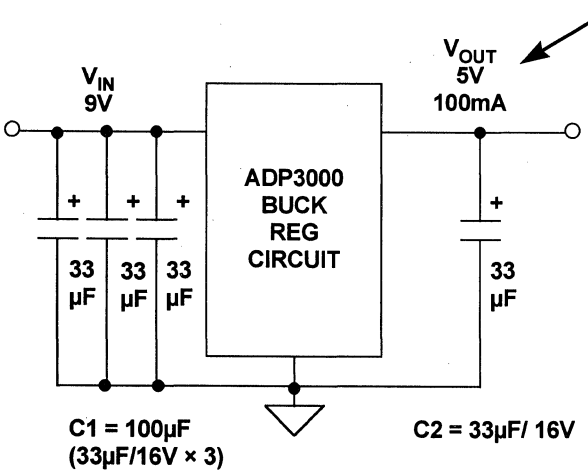


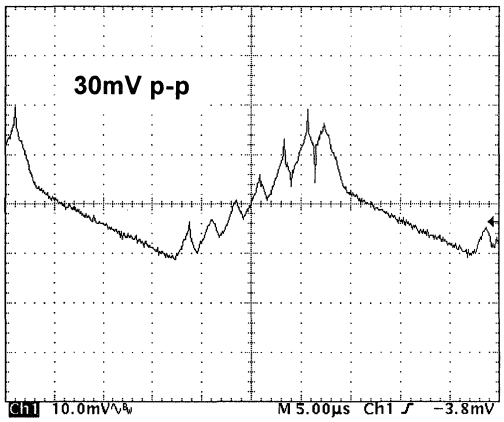
VERTICAL SCALE: 20mV / DIV
HORIZ. SCALE: 5µs / DIV

C1 = 33uF/16V x 3 , SPRAGUE 293D SURFACE MOUNT TANTALUM
C2 = 33µF/16V , SPRAGUE 293D SURFACE MOUNT TANTALUM

Figure 8.28

ADP3000 BUCK OUTPUT WAVEFORM

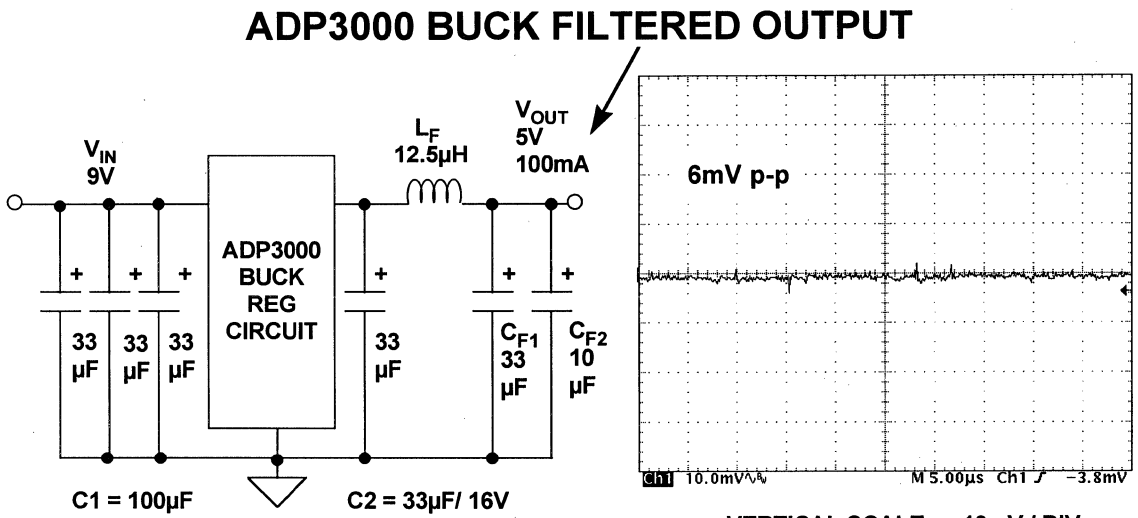




VERTICAL SCALE: 20mV / DIV
HORIZ. SCALE: 5µs / DIV

C1 = 33uF/16V x 3 , SPRAGUE 293D SURFACE MOUNT TANTALUM
C2 = 33µF/16V , SPRAGUE 293D SURFACE MOUNT TANTALUM

Figure 8.29



C1 = 33uF/16V x 3 , SPRAGUE 293D SURFACE MOUNT TANTALUM
C2 = 33µF/16V , SPRAGUE 293D SURFACE MOUNT TANTALUM

OUTPUT FILTER:
L_F = 12.5µH, COILTRONICS CTX25-4
C_{F1} = 33µF/16V SPRAGUE 293D SURFACE MOUNT TANTALUM
C_{F2} = 10µF/16V SURFACE MOUNT TANTALUM, KEMET T491C SERIES

Figure 8.30

ADP1148 9V TO 3.3V/1A BUCK REGULATOR

The circuit for the ADP1148 9V to 3.3V/1A buck regulator is shown in Figure 8.31, and the input waveform in Figure 8.32. The input waveform is characteristic of the PWM buck regulator. The decaying portion of the waveform occurs when the inductor is connected to the input. The flat portion is when the input is disconnected from the inductor. The fundamental switching frequency is approximately 150kHz.

The output waveform of the ADP1148 buck regulator is shown in Figure 8.33. Note that the output filter capacitors consist of two leaded OS-CON types with very low ESR (approximately 0.02Ω each). This results in a low ripple of 6mV peak-to-peak, which is acceptable without further filtering.

ADP1148 BUCK REGULATOR APPLICATION

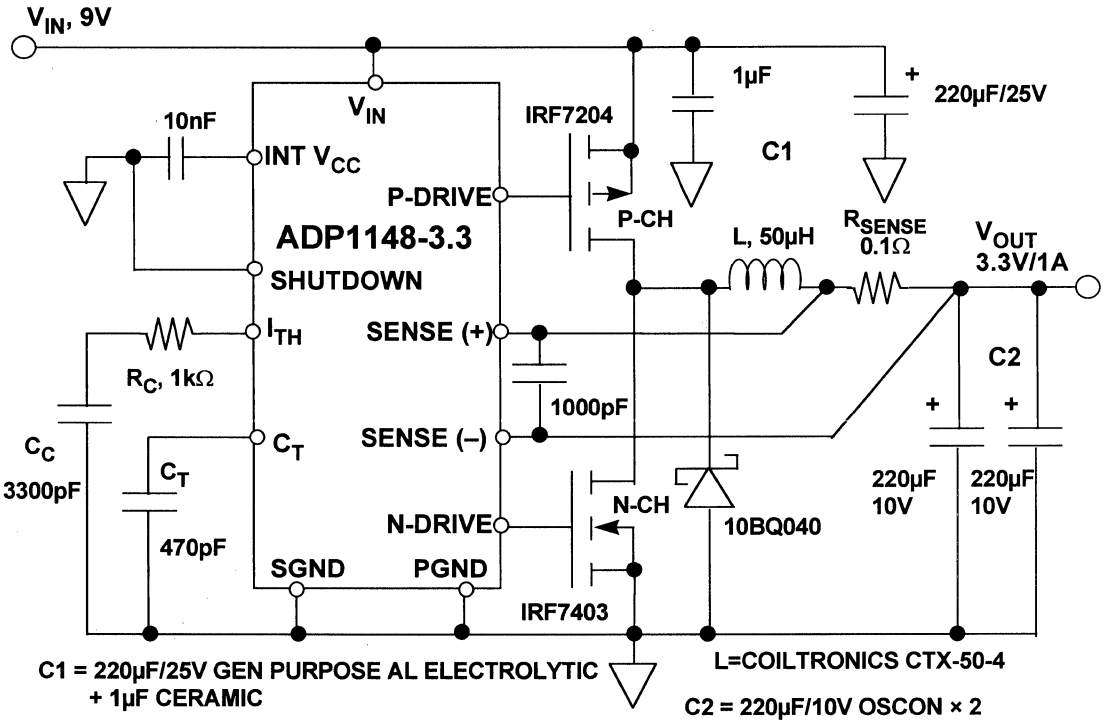
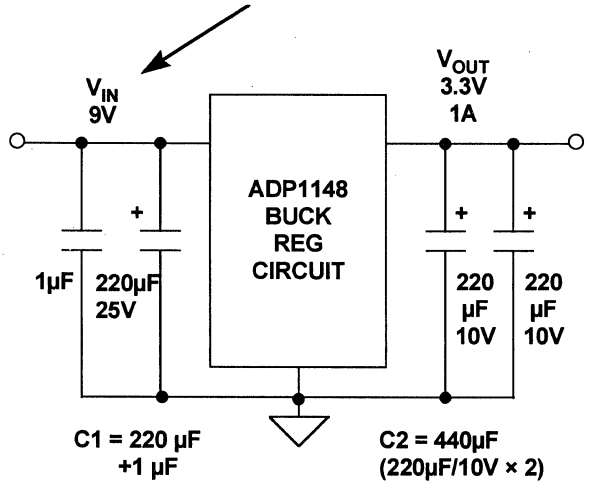
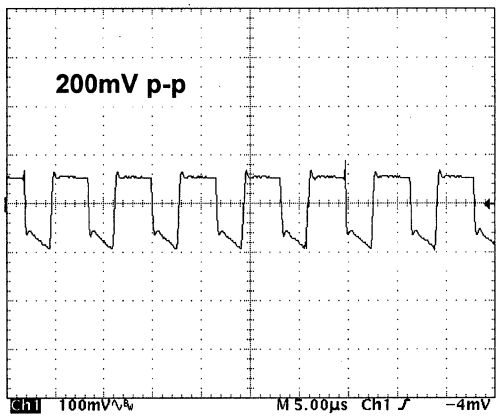


Figure 8.31

ADP1148 BUCK INPUT WAVEFORM - CONDITION 1





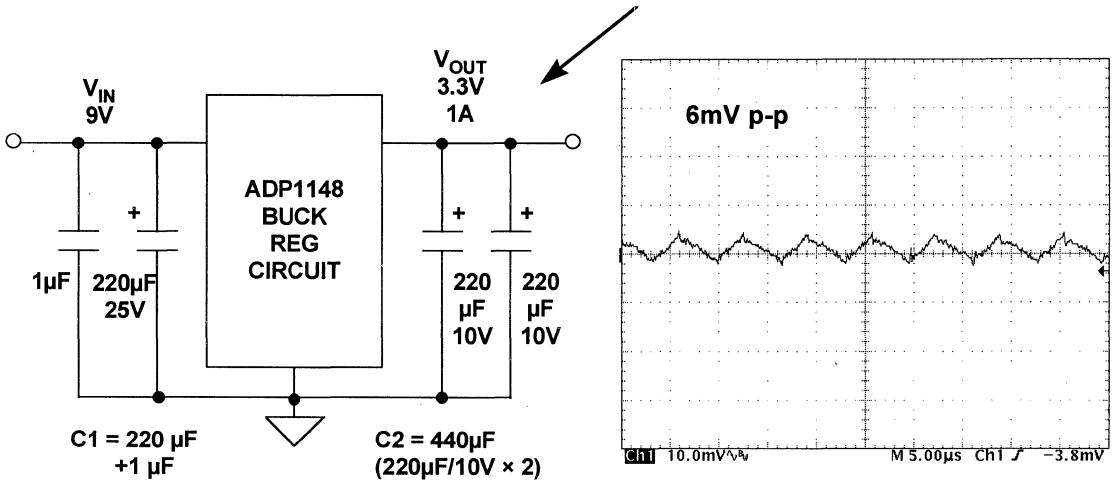
VERTICAL SCALE: 100mV / DIV
HORIZ SCALE: 5µs / DIV

C1 = 1µF CERAMIC + 220µF/25V GENERAL PURPOSE AL ELECTROLYTIC
C2 = 220 µF/10V OSCON × 2

Figure 8.32

In order to evaluate the effects of an output filter, the ripple was increased by replacing the two OS-CON output capacitors with a single 100µF leaded tantalum. The resulting output ripple was increased to 40mV and is shown in Figure 3.34. Now, the effects of a filter could be evaluated. It consisted of a 50µH inductor followed by a 100µF leaded tantalum. Ripple was reduced from 40mV to 3mV as shown in Figure 3.35.

ADP1148 BUCK OUTPUT WAVEFORM - CONDITION 1

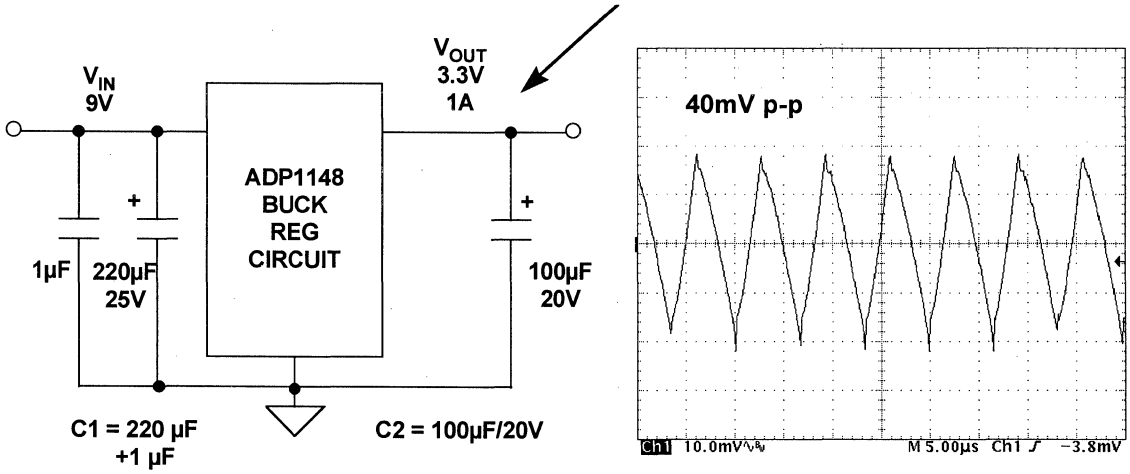


VERTICAL SCALE: 10mV / DIV
HORIZ. SCALE: 5µs / DIV

C1 = 1µF CERAMIC + 220µF/25V GENERAL PURPOSE AL ELECTROLYTIC
C2 = 220 µF/10V OSCON × 2

Figure 8.33

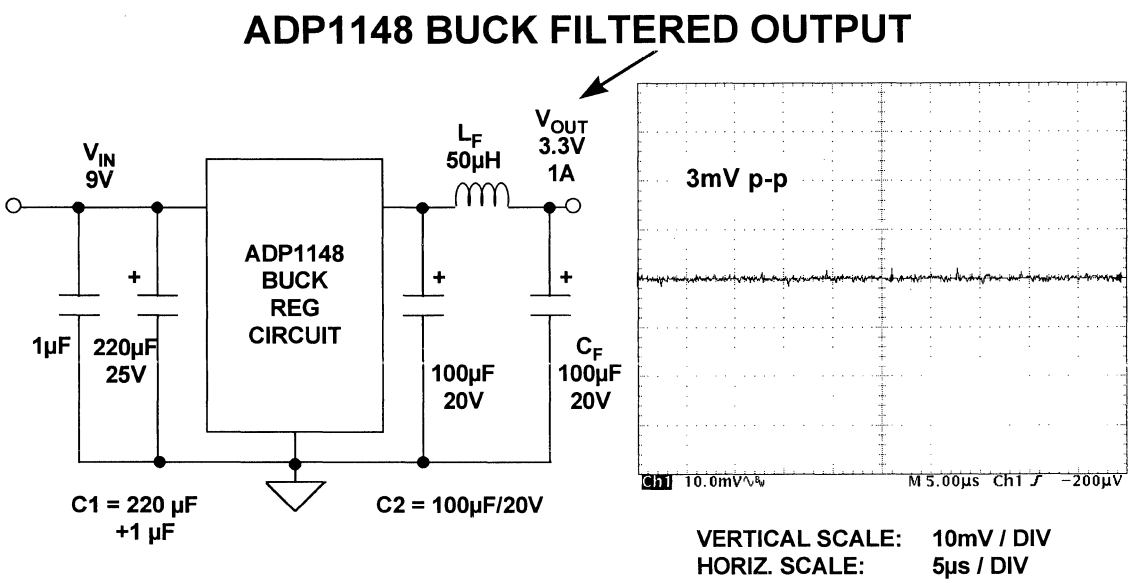
ADP1148 BUCK OUTPUT - CONDITION 2



VERTICAL SCALE: 10mV / DIV
HORIZ. SCALE: 5µs / DIV

C1 = 1µF CERAMIC + 220µF/25V GENERAL PURPOSE AL ELECTROLYTIC
C2 = 100µF/20V LEADED TANTALUM, KEMET T356-SERIES (ESR = 0.6Ω)

Figure 8.34



C1 = 1µF CERAMIC + 220µF/25V GENERAL PURPOSE AL ELECTROLYTIC
C2 = 100µF/20V LEADED TANTALUM, KEMET T356-SERIES (ESR = 0.6Ω)

OUTPUT FILTER
L_F=COILTRONICS CTX-50-4
C_F = 100µF/20V LEADED TANTALUM, KEMET T356-SERIES

Figure 8.35

ADP1148 9V TO 3.75V BUCK REGULATOR FOLLOWED BY ADP3310 3.3V LINEAR LOW DROPOUT POST REGULATOR

Linear regulators are often used following switching regulators for better regulation and lower noise. Low dropout (LDO) regulators such as the ADP3310 are desirable in these applications because they require only a small input-to-output series voltage to maintain regulation. This minimizes power dissipation in the pass device and may eliminate the need for a heat sink. Figure 8.36 shows the ADP1148 buck regulator configured for a 9V input and a 3.75V/1A output. The output drives an ADP3310 linear LDO regulator configured for 3.75V input and 3.3V/1A output. The input and output of the ADP3310 is shown in Figure 8.37. Notice that the regulator reduces the ripple from 25mV to approximately 5mV.

ADP1148 BUCK REGULATOR DRIVING ADP3310 LOW DROPOUT REGULATOR

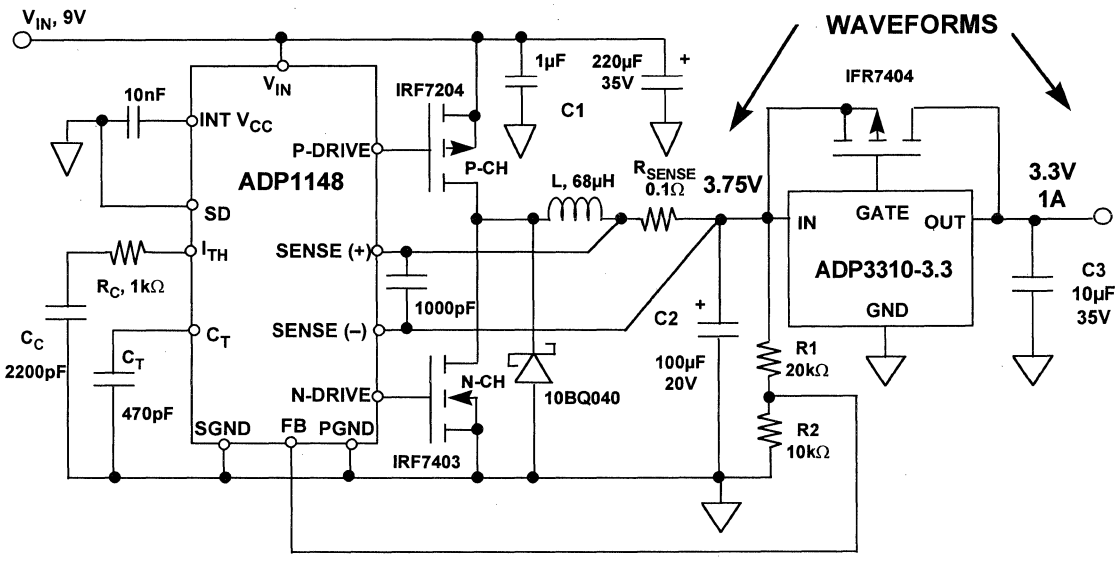
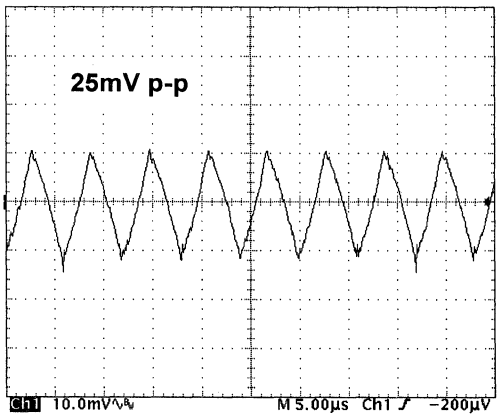


Figure 8.36

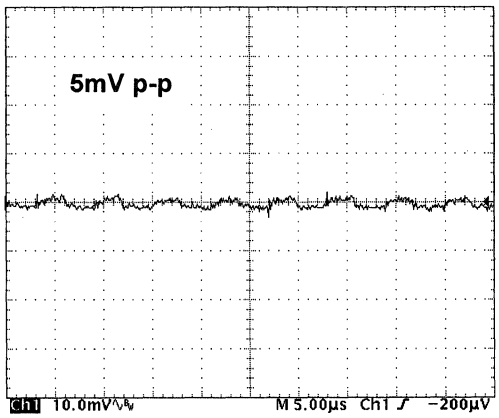
WAVEFORMS FOR ADP1148 BUCK REGULATOR DRIVING ADP3310 LOW DROPOUT REGULATOR

ADP1148 OUTPUT (ADP3310 INPUT)



VERTICAL SCALE: 10mV/DIV
HORIZ. SCALE: 5µs/DIV

ADP3310 OUTPUT



VERTICAL SCALE: 10mV/DIV
HORIZ. SCALE: 5µs/DIV

Figure 8.37

ADP3605 +5V to –3V/100mA Switched Capacitor Voltage Converter

Figure 8.38 shows the application circuit for the ADP3605 switched capacitor voltage converter. All three capacitors (input, output, and pump) are 10µF surface mount tantalum (Kemet T491C-series). Input and output waveforms are shown in Figure 8.39, where the output ripple is approximately 120mV peak-to-peak.

The addition of a 10µH/10µF output filter reduced the ripple to approximately 5mV as shown in Figure 8.40.

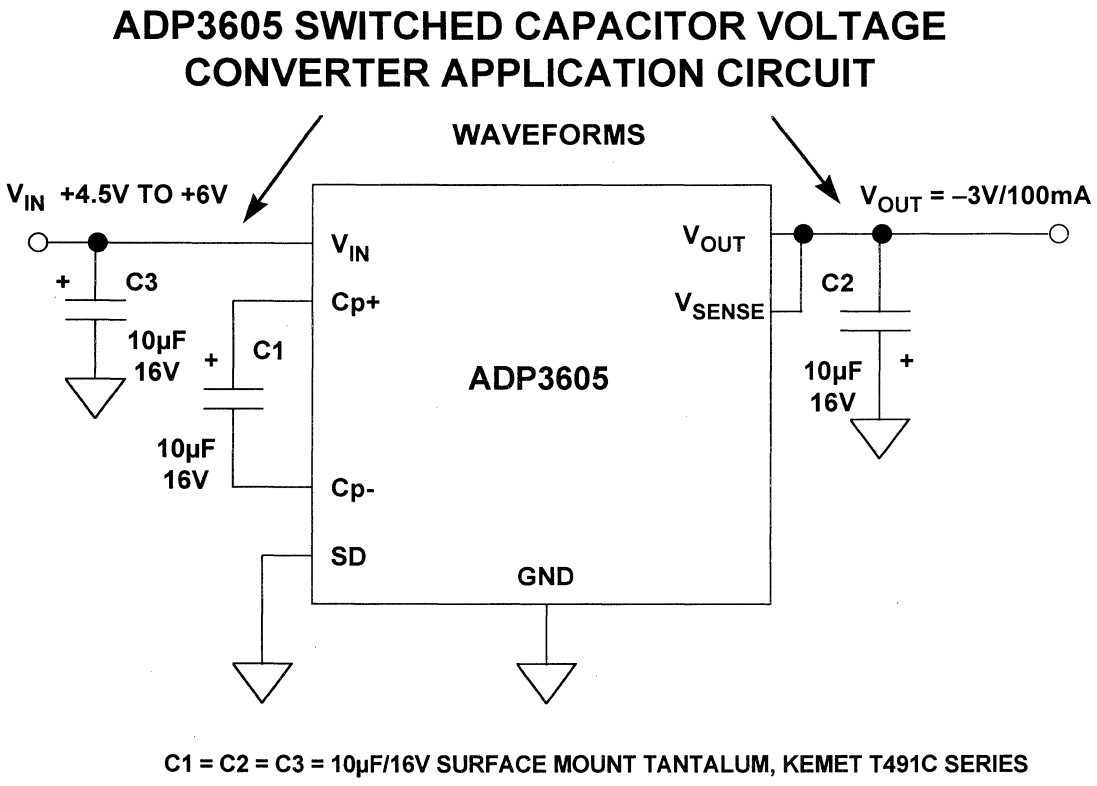
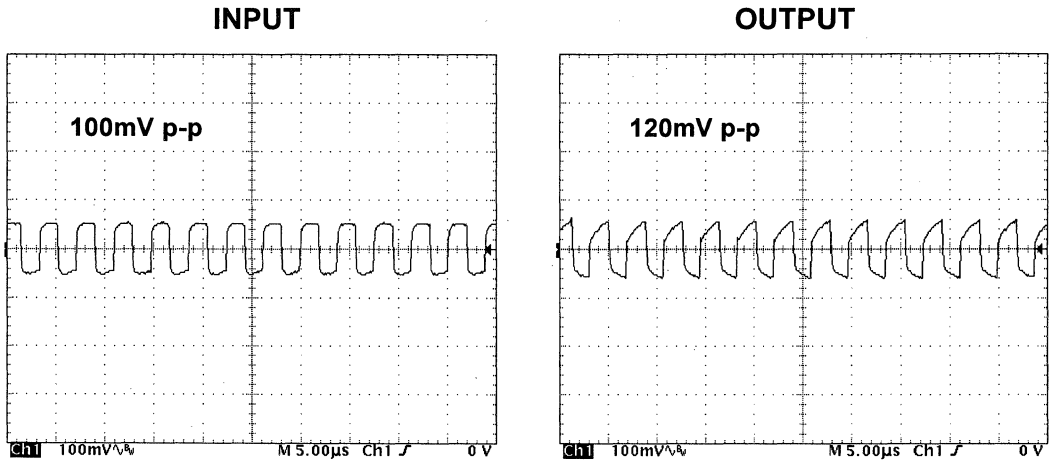


Figure 8.38

ADP3605 INPUT AND OUTPUT WAVEFORMS

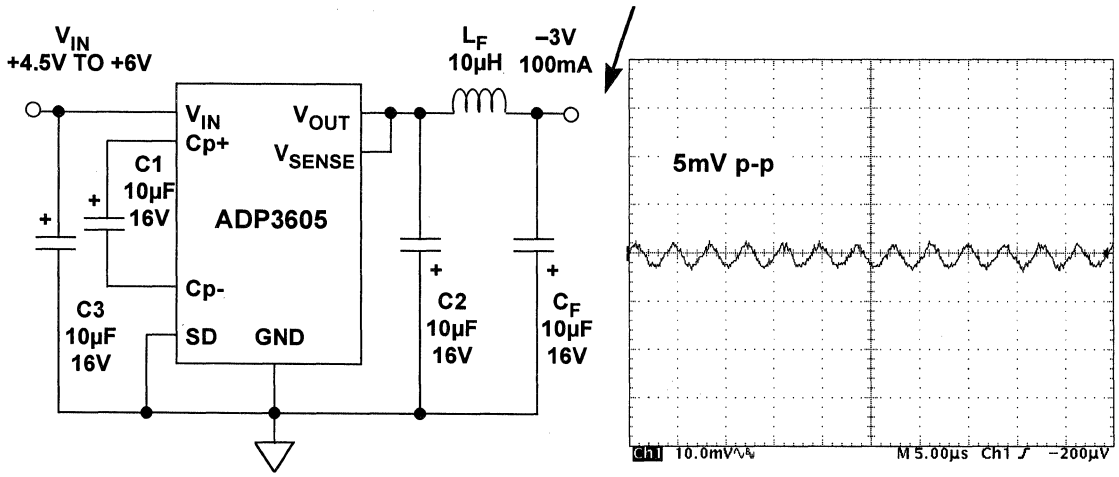


VERTICAL SCALE: 100mV/DIV
HORIZ. SCALE: 5µs/DIV

VERTICAL SCALE: 100mV/DIV
HORIZ. SCALE: 5µs/DIV

Figure 8.39

ADP3605 FILTERED OUTPUT



L_F = 10µH, COILTRONICS CTX10-3
C1 = C2 = C3 = C_F = 10µF/16V, KEMET T491C SERIES

VERTICAL SCALE: 10mV/DIV
HORIZ. SCALE: 5µs/DIV

Figure 8.40

SUMMARY OF RESULTS OF EXPERIMENTS

The preceding experiments serve to illustrate the large number of tradeoffs which can be made when filtering switching regulator outputs. The success of any combination is highly dependent upon a compact layout and the use of a large area

ground plane. As has been stated earlier, all connections to the ground plane should be made as short as possible to minimize parasitic resistance and inductance.

Output ripple can be reduced by the addition of low ESL/ESR capacitors to the output. However, it may be more efficient to use an LC filter to accomplish the ripple reduction. In any case, proper component selection is critical. The inductor should not saturate under the maximum load current, and its DC resistance should be low enough as not to induce significant voltage drop. The capacitors should have low ESL and ESR and be rated to handle the required ripple current.

Low dropout linear post regulators provide both ripple reduction as well as better regulation and can be effective, provided the sacrifice in efficiency is not excessive.

Finally, it is difficult to predict the output ripple current analytically, and there is no substitute for a prototype using the real-world components. Once the filter is proven to provide the desired ripple attenuation (with some added safety margin), care must be taken that parts substitutions or vendor changes are not made in the final production units without first testing them in the circuit for equivalent performance.

SUMMARY OF RESULTS

- **Proper Layout and Grounding (using Ground Plane) Mandatory**
- **Low ESL/ESR Capacitors Give Best Results**
- **External LC Filters Very Effective in Reducing Ripple**
- **Linear Post Regulation Effective for Noise Reduction and Best Regulation**
- **Completely Analytical Approach Difficult, Prototyping is Required for Optimum Results**
- **Once Design is Finalized, Do Not Switch Vendors or Use Parts Substitutions Without First Verifying Their Performance in Circuit**
- **High Frequency Localized Decoupling at IC Power Pins is Still Required**

Figure 8.41

LOCALIZED HIGH FREQUENCY POWER SUPPLY FILTERING

The LC filters described in the previous section are useful in filtering switching regulator outputs. However, it may be desirable to place similar filters on the individual PC boards where the power first enters the board. Of course, if the switching regulator is placed on the PC board, then the LC filter should be an integral part of the regulator design.

Localized high frequency filters may also be required at each IC power pin (see Figure 8.42). This simple filter can be considered an option, one which is exercised dependent upon the high frequency characteristics of the associated IC and the relative attenuation desired. It uses Z1, a leaded ferrite bead such as the Panasonic EXCELSA39, providing a resistance of more than 80Ω at 10MHz, increasing to over 100Ω at 100MHz. The ferrite bead is best used with a local high frequency decoupling cap right at the IC power pins, such as a 0.1μF ceramic unit shown.

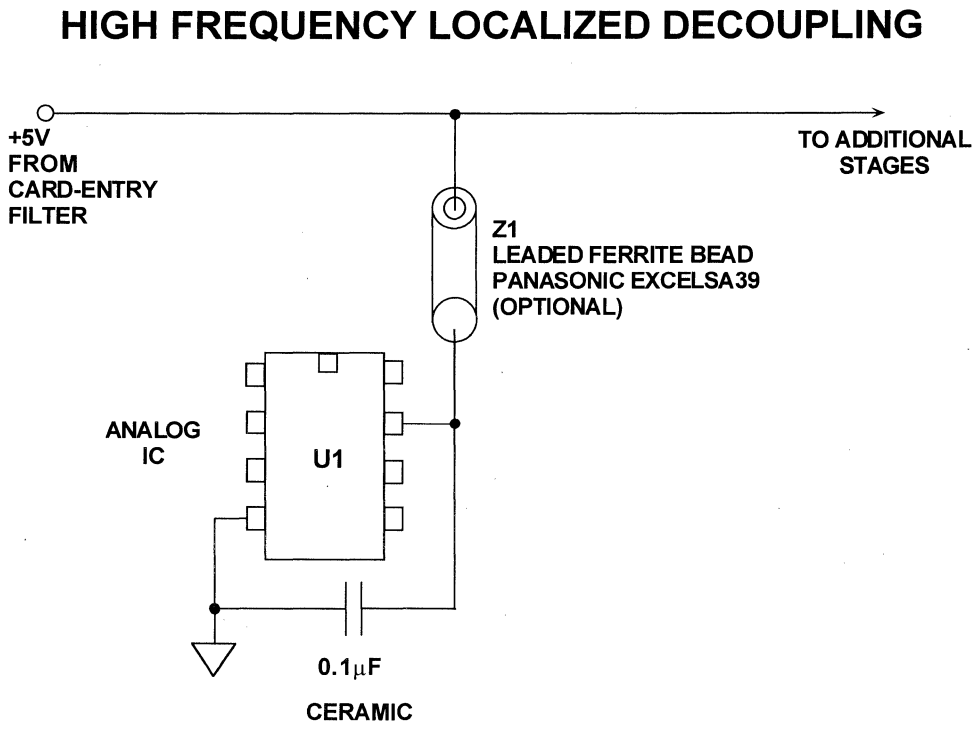


Figure 8.42

The following list summarizes the switching power supply filter layout/construction guidelines which will help ensure that the filter does the best possible job:

(1) *Pick the highest electrical value and voltage rating for filter capacitors which is consistent with budget and space limits. This minimizes ESR, and maximizes filter performance. Pick chokes for low ΔL at the rated DC current, as well as low DCR.*

(2) *Use short and wide PCB tracks to decrease voltage drops and minimize inductance. Make track widths at least 200 mils for every inch of track length for lowest DCR, and use 1 oz or 2 oz copper PCB traces to further reduce IR drops and inductance.*

(3) *Use short leads or better yet,* leadless *components, to minimize lead inductance. This minimizes the tendency to add excessive ESL and/or ESR. Surface mount packages are preferred. Make all connections to the ground plane as short as possible.*

(4) *Use a large-area ground plane for minimum impedance.*

(5) *Know what your components do over frequency, current and temperature variations! Make use of vendor component models for the simulation of prototype designs, and make sure that lab measurements correspond reasonably with the simulation. While simulation is not* absolutely *necessary, it does instill confidence in a design when correlation is achieved*(see Reference 15).

The discussion above assumes that the incoming AC power is relatively clean, an assumption not always valid. The AC power line can also be an EMI entry/exit path! To remove this noise path and reduce emissions caused by the switching power supply or other circuits, a *power line filter* is required.

It is important to remember that AC line power can potentially be lethal! Do not experiment without proper equipment and training! All components used in power line filters should be UL approved, and the best way to provide this is to specify a packaged UL approved filter. It should be installed in such a manner that it is the first thing the AC line sees upon entering the equipment. Standard three wire IEC style line cords are designed to mate with three terminal male connectors integral to many line filters. This is the best way to achieve this function, as it automatically grounds the third wire to the shell of the filter and equipment chassis via a low inductance path.

Commercial power line filters can be quite effective in reducing AC power-line noise. This noise generally has both common-mode and differential-mode components. Common-mode noise is noise that is found on any two of the three power connections (black, white, or green) with the same amplitude and polarity. In contrast, differential-mode noise is noise found only between two lines. By design, most commercially available filters address both noise modes (see Reference 16).

REFERENCES: NOISE REDUCTION AND FILTERING

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6. Ian Clelland, *Metalized Polyester Film Capacitor Fills High Frequency Switcher Needs*, **PCIM**, June 1992.

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12. Steve Hageman, *Use Ferrite Bead Models to Analyze EMI Suppression,* **The Design Center Source,** MicroSim Newsletter**,** January, 1995.

13. Type 5250 and 6000-101K chokes, J. W. Miller, 306 E. Alondra Blvd., Gardena, CA, 90247, (310) 515-1720.

14. DIGI-KEY, PO Box 677, Thief River Falls, MN, 56701-0677, (800) 344-4539.

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16. Eichhoff Electronics, Inc., 205 Hallene Road, Warwick, RI., 02886, (401) 738-1440.

THERMAL MANAGEMENT
Walt Jung, Walt Kester

For reliability reasons, modern semiconductor-based systems are increasingly called upon to observe some form of *thermal management.* All semiconductors have some specified safe upper limit for junction temperature (T_J), usually on the order of 150°C (but sometimes 175°). Like maximum power supply potentials, maximum junction temperature is a worst case limitation which shouldn't be exceeded. In conservative designs, it won't be approached by less than an ample safety margin. This is a critical point, since the lifetime of all semiconductors is inversely related to their operating junction temperature. The cooler semiconductors can be kept during operation, the more closely they will approach maximum useful life.

Thermal basics

The general symbol θ is used for *thermal resistance*, that is:

θ = thermal resistance, in units of °C/watt (or, °C/W).

θ_{JA} and θ_{JC} are two more specific terms used in dealing with semiconductor thermal issues, which are explained below.

In general, a device with a thermal resistance θ equal to 100°C/W will exhibit a temperature differential of 100°C for a power dissipation of 1W, as measured between two reference points. Note that this is a linear relation, so a 500mW dissipation in the same part will produce a 50°C differential, and so forth. For any power P (in watts), calculate the effective temperature differential (ΔT) in °C as:

$$\Delta T = P \times \theta,$$

where θ is the total applicable thermal resistance. Figure 8.43 summarizes these thermal relationships.

As the relationships signify, to maintain a low T_J, either θ or the power dissipated (or both) must be kept low. A low ΔT is the key to extending semiconductor lifetimes, as it leads to low maximum junction temperatures.

In semiconductors, one temperature reference point is always the device junction, taken to mean the hottest spot inside the chip operating within a given package. The other relevant reference point will be either the case of the device, or the *ambient temperature*, T_A, that of the surrounding air. This then leads in turn to the above mentioned individual thermal resistances, θ_{JA} and θ_{JC}.

THERMAL DESIGN BASICS

- θ = Thermal Resistance (°C/W)
- $\Delta T = P \times \theta$
- θ_{JA} = Junction - to - Ambient Thermal Resistance
- θ_{JC} = Junction - to - Case Thermal Resistance
- θ_{CA} = Case - to - Ambient Thermal Resistance
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- $T_J = T_A + (P \times \theta_{JA})$, P = Total Device Power Dissipation
- $T_{J(Max)}$ = 150°C (Sometimes 175°C)

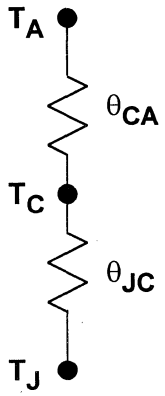


Figure 8.43

Taking the more simple case first, θ_{JA} is the thermal resistance of a given device measured between its *junction* and the *ambient* air. This thermal resistance is most often used with small, relatively low power ICs which do not dissipate serious amounts of power, that is 1W or less. θ_{JA} figures typical of op amps and other small devices are on the order of 90-100°C/W for a plastic 8 pin DIP package. It must be understood that thermal resistances are highly package dependent, as different materials have differing degrees of thermal conductivity. As a general rule of thumb, thermal resistance for the conductors within packaging materials is closely analogous to electrical resistances, that is copper is the best, followed by aluminum, steel, and so on. Thus copper lead frame packages offer the highest performance (lowest θ).

A summary of the thermal resistances of various IC packages is shown in Figures 8.44, 8.45, and 8.46. In general, most of these packages do not lend themselves to easy heat sink attachment (with notable exceptions, such as the older round metal can types or the TO-220 package). Devices which *are* amenable to heat sink attachment will often be noted by a θ_{JC} dramatically lower than the θ_{JA}. See for example the 15 pin SIP package (used by the AD815), the TO-220 package, and the TO-263 package.

STANDARD PACKAGE THERMAL RESISTANCES - 1

Package	ADI Designation	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Comment
3 pin SOT-23	SOT-23-3	300	180	ADT45/ADT50
5 pin SOT-23	SOT-23-5	190		ADT05
6 pin SOT-23	SOT-23-6	165	92	ADP3300
8 pin plastic DIP	N-8	90		AD823
8 pin ceramic DIP	D-8	110	22	AD712
8 pin SOIC	R-8	160	60	
8 pin SOIC	R-8	90	60	ADP3367 Thermal Coastline
8 pin metal can	H-08A (TO-99)	150	45	OP07
10 pin metal can	H-10A (TO-100)	150	25	AD582
12 pin metal can	H-12A (TO-8)	100	30	AD841

Figure 8.44

STANDARD PACKAGE THERMAL RESISTANCES - 2

Package	ADI Designation	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Comment
14 pin plastic DIP	N-14	150		AD713
14 pin ceramic DIP	D-14	110	30	AD585
14 pin SOIC	R-14	120		AD813
15 pin SIP	Y-15	41	2	AD815 Through-Hole
16 pin plastic DIP	N-16	120	40	
16 pin ceramic DIP	D-16	95	22	AD524
16 pin SOIC	R-16	85		AD811
18 pin ceramic DIP	D-18	120	35	AD7575

Figure 8.45

STANDARD PACKAGE THERMAL RESISTANCES - 3

Package	ADI Designation	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Comment
20 pin plastic DIP	N-20	102	31	
20 pin ceramic DIP	D-20	70	10	
20 pin SOIC	R-20	74	24	
24 pin plastic DIP	N-24	105	35	
24 pin ceramic DIP	D-24	120	35	AD7547
28 pin plastic DIP	N-28	74	24	
28 pin ceramic DIP	D-28	51	8	
28 pin SOIC	R-28	71	23	
TO-220		53	3	Through-Hole
TO-263 (D2PAK)		73	3	Surface Mount

Figure 8.46

θ_{JC} is the thermal resistance of a given device as measured between its *junction* and the device *case*. This form is most often used with larger power semiconductors which do dissipate significant amounts of power, that is typically more than 1W. The reason for this is that a *heat sink* generally must be used with such devices, to maintain a sufficiently low internal junction temperature. A heat sink is simply an additional low thermal resistance device attached externally to a semiconductor part to aid in heat removal. It will have some additional thermal resistance of its own, also rated in °C/W.

Rather than just a single number, θ in this case will be composed of more than one component, i.e., θ_1, θ_2, etc. Like series resistors, thermal impedances add, making a net calculation relatively simple. For example, to compute a net θ_{JA} given a relevant θ_{JC}, the thermal resistance of the heat sink, θ_{CA}, or *case* to *ambient* is added to the θ_{JC} as:

$$\theta_{JA} = \theta_{JC} + \theta_{CA},$$

and the result is the θ_{JA} for that specific circumstance.

A real example illustrating these relationships is shown by Figure 8.47. These curves indicate the maximum power dissipation vs. temperature characteristic for a device using standard 8-pin SOIC and a thermal coastline 8-pin SOIC. Expressed in this fashion, the curves are often referred to as *derating* curves. The proprietary Analog Devices' thermal coastline package allows additional power to be dissipated with no increase in package size. For a $T_{J(max)}$ of 150°C, the upper curve shows the allowable power in a thermal coastline package. This corresponds to a θ which can be calculated by dividing the ΔT by P at any point. For example, 1W of power is

allowed at a T_A of 60°C, so the ΔT is 150°C – 60°C = 90°C. Dividing by 1W gives the thermal coastline package's θ of 90°C/W. Similarly, the standard 8-pin SOIC package yields 160°C/W. Given such data as these derating curves, the θ_{JA} for a given device can be readily determined, as above.

MAXIMUM POWER DISSIPATION VS. TEMPERATURE FOR STANDARD AND THERMAL COASTLINE 8-PIN SOICs

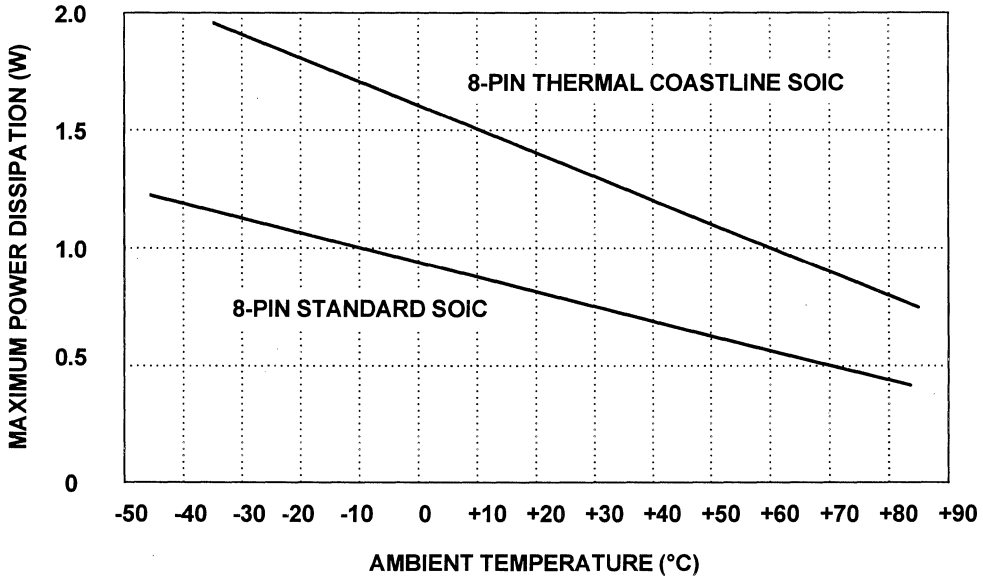


Figure 8.47

A physical comparison of the standard 8-pin SOIC leadframe and the Analog Devices' thermal coastline leadframe is shown in Figure 8.48 and 8.49. Note that the geometry of the thermal coastline leadframe increases the amount of heat transferred to the pins by decreasing the face-to-face distance between the leadframe and the paddle as well as increasing the width of the adjoining faces.

THERMAL COASTLINE PACKAGE

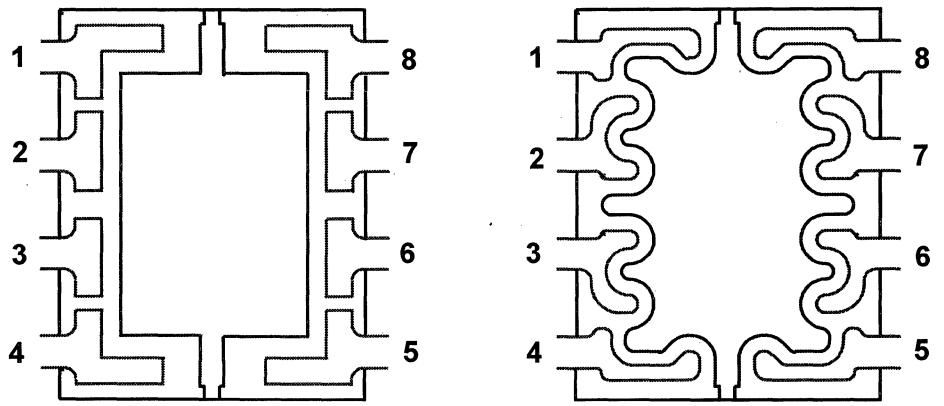


Figure 8.48

DETAILS OF THERMAL COASTLINE PACKAGE

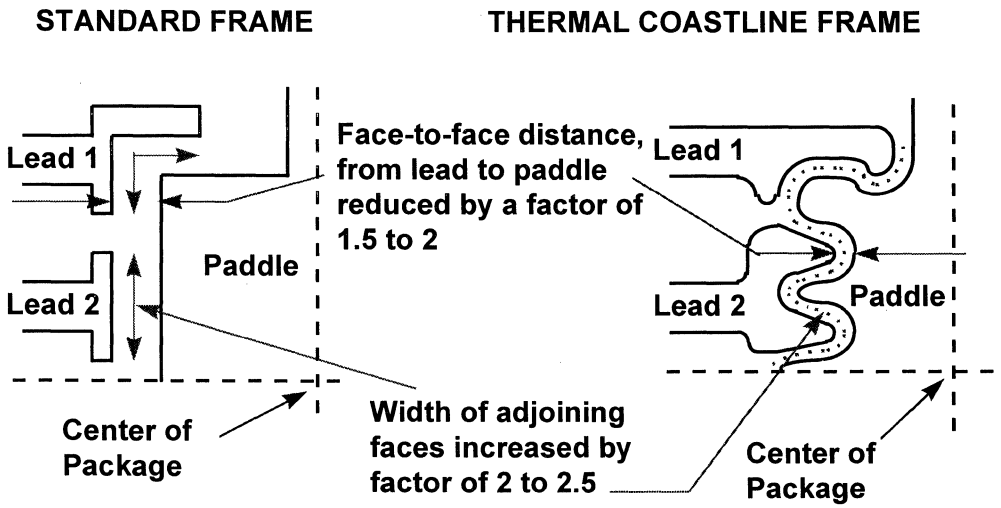


Figure 8.49

Heat Sink and Airflow Considerations

The fundamental purpose of heat sinks and airflow is to allow high power dissipation levels while maintaining safe junction temperatures. There are many tradeoffs which can be made between airflow and heat sink area, and this section examines some of them.

A thermal model of an IC and a heat sink is shown in Figure 8.50. The critical parameter is the junction temperature, T_J, which must be kept below 150°C for most ICs. The model shows the various thermal resistances and temperatures at various parts of the system. T_A is the ambient temperature, T_S is the heat sink temperature, T_C is the IC case temperature, and T_J is the junction temperature. The heat sink is usually attached to the IC in such a manner as to minimize the difference between the IC case temperature and the heat sink temperature. This is accomplished by a variety of means, including thermal grease, machined surface contact area, etc. In any case, the thermal resistance between the heat sink and the IC case can usually be made less than 1°C/W.

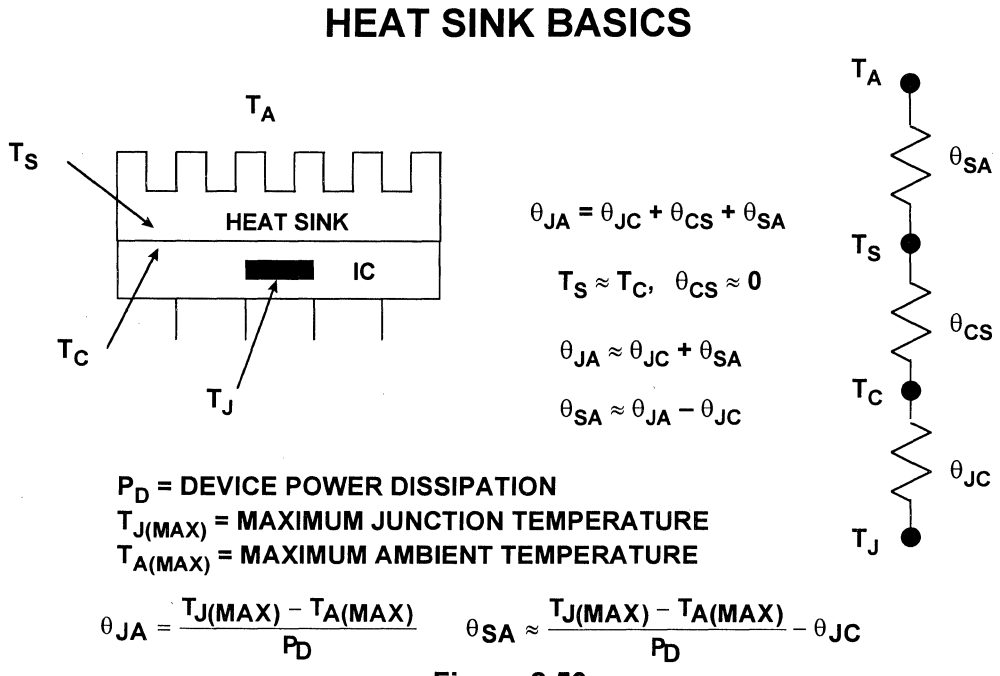


Figure 8.50

The junction-to-ambient thermal resistance, θ_{JA}, is therefore the sum of the three thermal resistance terms:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA},$$

where θ_{JC} is the junction-to-case thermal resistance, θ_{CS} the case-to-heat sink thermal resistance, and θ_{SA} the heat sink-to-ambient thermal resistance. Each term is multiplied by the device power dissipation, P_D, to determine the temperature rise associated with each thermal resistance:

$$T_J = P_D(\theta_{JA}) = P_D\,(\theta_{JC} + \theta_{CS} + \theta_{SA}).$$

In most situations the maximum junction temperature, $T_{J(MAX)}$, maximum ambient temperature, $T_{A(MAX)}$, and P_D are known quantities, and it is desired to calculate the required heat sink thermal resistance, θ_{SA}, which will limit the junction temperature to $T_{J(MAX)}$ under the specified conditions. We know that the junction-to-ambient thermal resistance, θ_{JA}, can be expressed in terms of $T_{J(MAX)}$, $T_{A(MAX)}$, and P_D as follows:

$$\theta_{JA} = \frac{T_{J(MAX)} - T_{A(MAX)}}{P_D}.$$

We also know that θ_{SA} can be expressed in terms of θ_{JA}, θ_{CS}, and θ_{JC}:

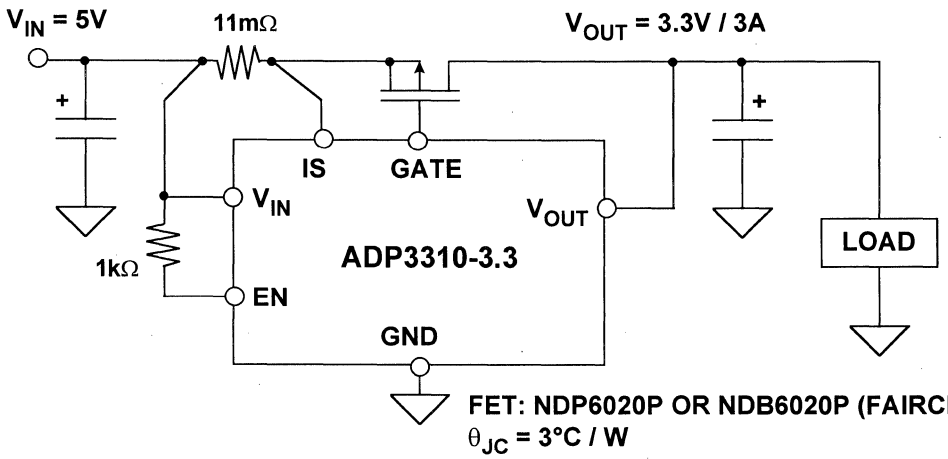
$$\theta_{SA} = \theta_{JA} - \theta_{JC} - \theta_{CS} = \frac{T_{J(MAX)} - T_{A(MAX)}}{P_D} - \theta_{JC} - \theta_{CS}.$$

In most cases, θ_{CS} can be less than 1°C/W with the use of thermal grease, and the expression for the maximum allowable heat sink-to-ambient resistance reduces to:

$$\theta_{SA} \approx \frac{T_{J(MAX)} - T_{A(MAX)}}{P_D} - \theta_{JC}.$$

A design example will help clarify the process and identify the various tradeoffs. Consider the low dropout linear regulator circuit shown in Figure 8.51 based on the ADP3310.

LDO THERMAL DESIGN EXAMPLE



$P_D = (5V - 3.3V)(3A) = 5.1W$

$T_{J(MAX)} = 125°C$, $T_{A(MAX)} = 50°C$

$$\theta_{SA} \approx \frac{T_{J(MAX)} - T_{A(MAX)}}{P_D} - \theta_{JC} = \frac{125 - 50}{5.1} - 3 = 14.7 - 3 = 11.7°C/W$$

Figure 8.51

The power dissipated in the FET pass transistor (Fairchild NDP6020P or NDB6020P) due to the 1.7V drain-to-source voltage drop and the 3A output current is 5.1W. Now assume that we want to hold the maximum transistor junction temperature to $T_{J(MAX)} = 125°C$ at an ambient temperature of $T_{A(MAX)} = 50°C$. The junction-to-case thermal resistance of the FET is specified by the manufacturer to be 3°C/W. We can now calculate the maximum allowable heat sink case-to-ambient thermal resistance (neglecting θ_{CS}, the case-to-heat sink thermal resistance):

$$\theta_{SA} < \frac{T_{J(MAX)} - T_{A(MAX)}}{P_D} - \theta_{JC} = \frac{125 - 50}{5.1} - 3 = 14.7 - 3 = 11.7°C/W.$$

The 6020P Fairchild FET is available in two packages as shown in Figure 8.52. The TO-220 style has a junction-to-ambient thermal resistance of 53°C/W (no airflow) and has a metal tab which is designed to be bolted to a heat sink. The TO-263 style has a junction-to-ambient thermal resistance of 73°C/W (no airflow) and is designed for surface mounting. The metal drain tab of the surface mount package is designed to be soldered directly to the PC board pad which acts as a heat sink.

TO-220 AND TO-263 (D^2PAK) PACKAGES FOR FAIRCHILD NDP6020P/NDB6020P FETs

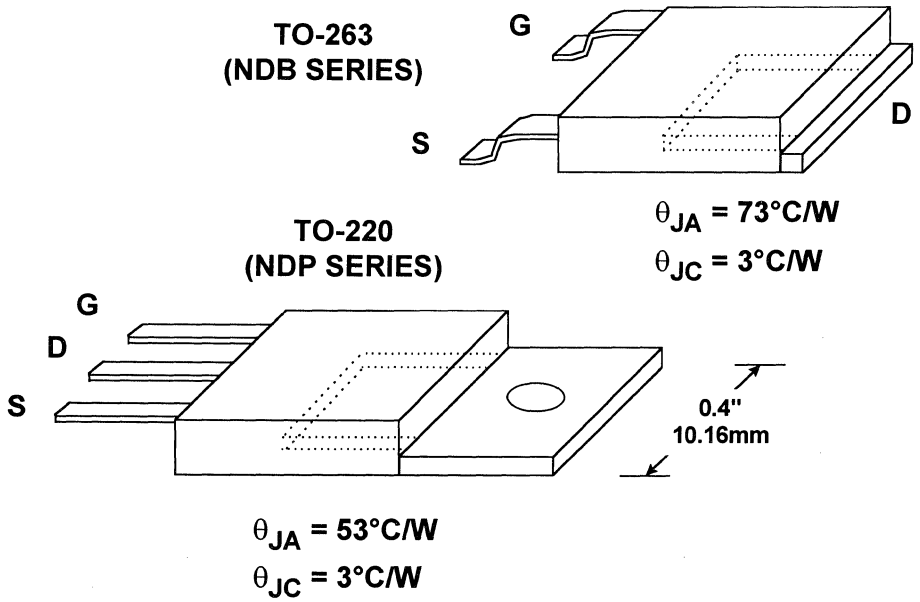


Figure 8.52

We will first select a suitable heat sink for the TO-220 package. Heat sink manufacturers such as AAVID Thermal Technologies have a variety of heat sinks suitable for a wide range of power dissipation levels. Selection tables provide nominal power dissipation, thermal resistance, and physical size for each heat sink available for a given package style.

A heat sink suitable for the TO-220 package is shown in Figure 8.53. It is a finned heat sink manufactured by AAVID Thermal Technologies (AAVID part number 582002B12500). The width of the heat sink is approximately 1.9". The entire assembly is bolted to the PC board, and the through-hole pins of the FET are then soldered to pads on the PC board.

The sink-to-ambient thermal resistance of this heat sink as a function of airflow is shown in Figure 8.54. Notice that even with no airflow, the thermal resistance is approximately 5°C/W, which is much less than the calculated maximum allowable value of 11.7°C/W. This heat sink will therefore provide more than adequate design margin under the specified operating conditions.

AAVID 582002B12500 HEAT SINK FOR TO-220

(Courtesy AAVID Thermal Technologies, Inc.)

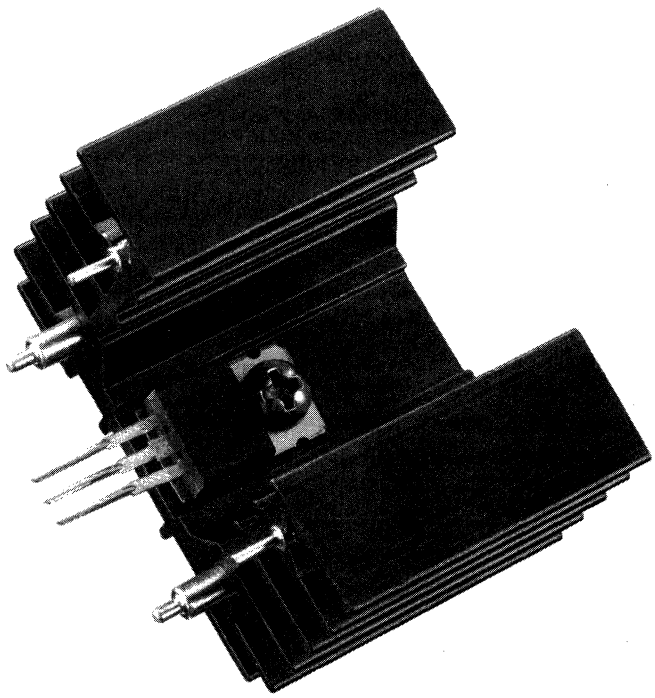


Figure 8.53

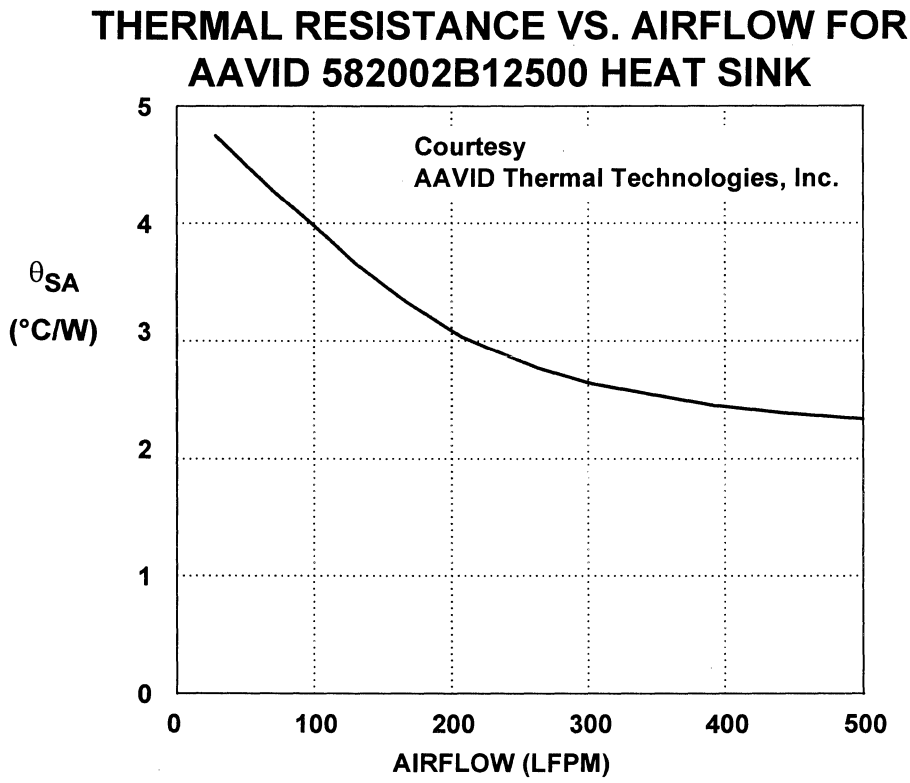


Figure 8.54

Now consider the alternate package, the surface mount TO-263 package. Because the drain pad connection acts as a heat sink, the thermal resistance is a function of the drain pad area on the PC board. Figure 8.55 shows the thermal resistance of the package as a function of PC board drain pad area which is acting as the heat sink. Note that even with 2 square inches of pad area, the thermal resistance is still 30°C/W, which is well above the calculated maximum allowable value of 11.7°C/W.

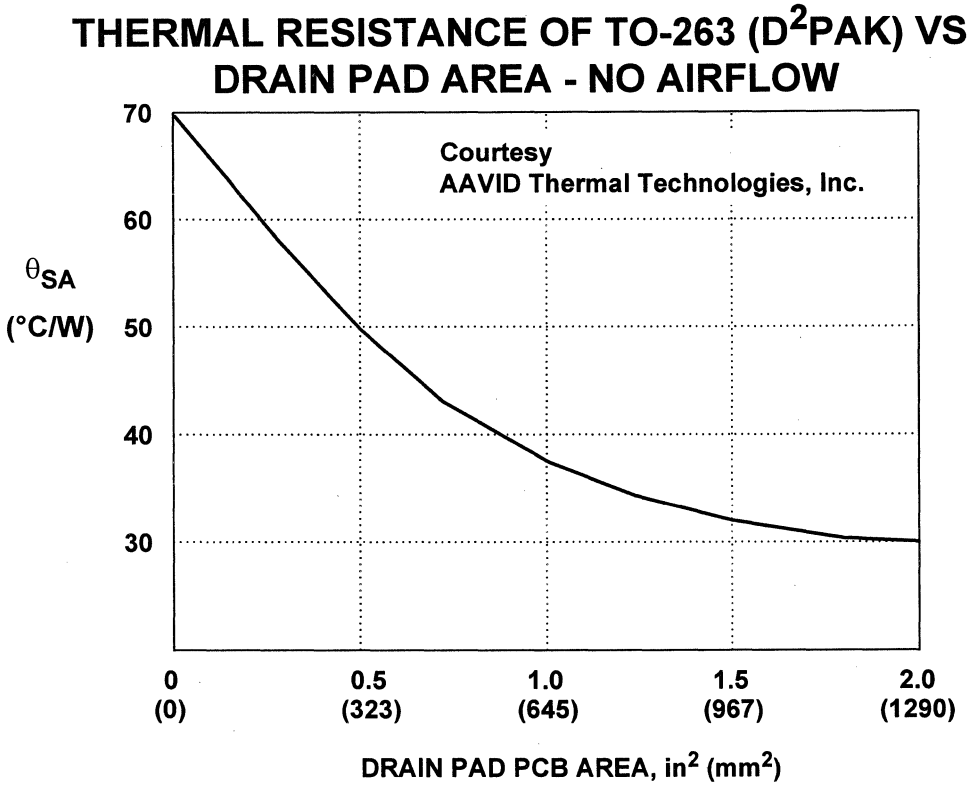


Figure 8.55

The situation can be improved by the addition of a surface-mount heat sink as shown in Figure 8.56 (AAVID part number 573300). This heat sink solders to two pads on the PC board which are extensions of the drain pad connecting area. The thermal resistance of this combination as a function of airflow is shown in Figure 8.57. Note that with the addition of the surface mount heat sink, the thermal resistance of the combination is reduced to approximately 10°C /W with a reasonable amount of airflow (200 linear feet per minute). The curve also shows the thermal resistance with no heat sink as a function of airflow, clearly indicating that a heat sink is required in order to meet the design requirements in a surface mount package.

AAVID 573300 HEAT SINK FOR TO-263 D^{2}PAK

(Courtesy AAVID Thermal Technologies, Inc.)

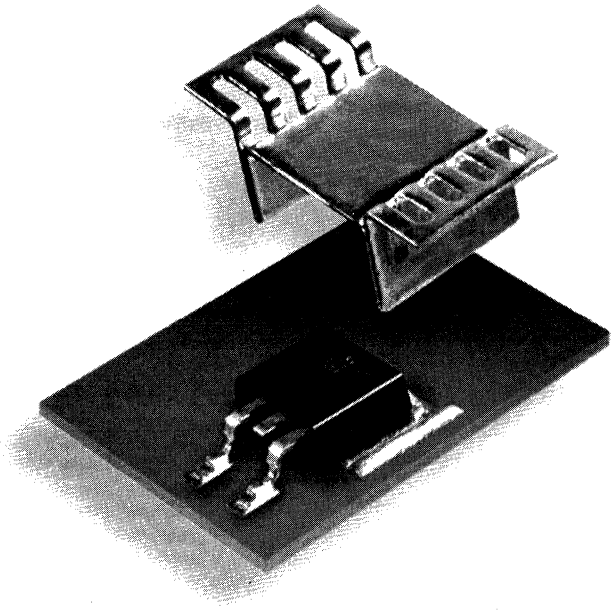


Figure 8.56

THERMAL RESISTANCE OF AAVID 573300 SURFACE MOUNT HEAT SINK VS. AIRFLOW

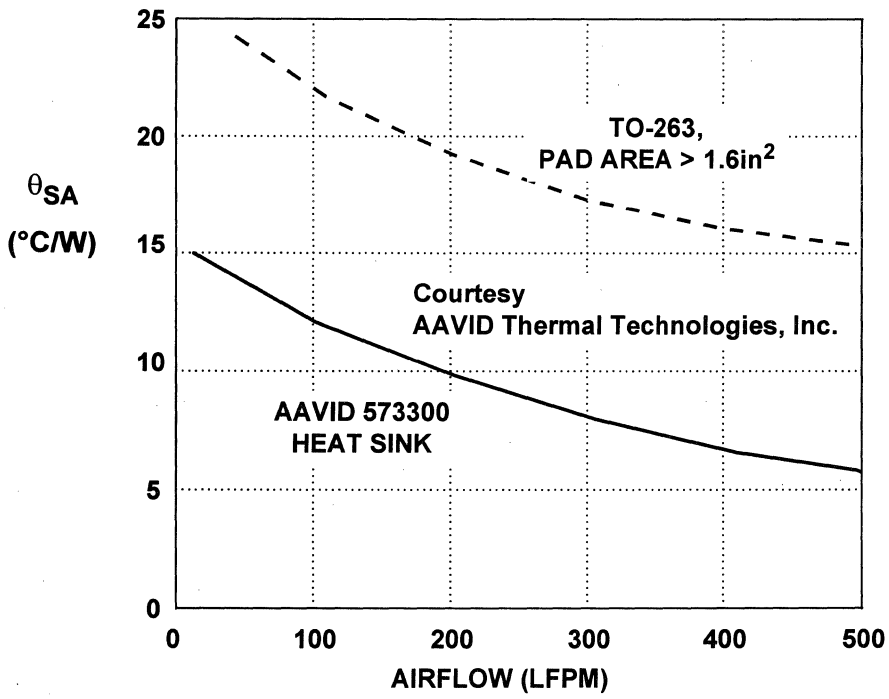


Figure 8.57

These examples illustrate the basic process of thermal design and heat sink selection. Larger heat sinks may lessen or even eliminate the need for airflow. However, when operating heat sinks with no air flow, the heatsink must be oriented such that thermal convection currents can carry the heat away from the heat sink. If additional airflow is required, the air must be allowed to pass freely around the heat sink with no obstruction. Note that small SOIC packages are also useful in conjunction with PCB copper heatsink areas (see References 6 and 7).

Further information on thermal management using heat sinks can be obtained from References 1-7.

REFERENCES: THERMAL MANAGEMENT

1. *Power Consideration* Discussions, **AD815 Data Sheet**, Analog Devices.

2. *Heat Sinks for Multiwatt® Packages,* **AAVID Thermal Technologies, Inc.**, One Kool Path, Laconia, NH, 03246, (603) 528-3400.

3. *General Catalog,* **AAVID Thermal Technologies, Inc.**, One Kool Path, Laconia, NH, 03246, (603) 528-3400.

4. Seri Lee, *How to Select a Heat Sink,* **AAVID Thermal Technologies**, Available on internet site: http://www.aavid.com.

5. Seri Lee, Optimum Design and Selection of Heat Sinks, **11th IEEE SEMI-THERM™ Symposium**, 1995. Also available on internet site: http://www.aavid.com.

6. Alan Li, et all, *Maximum Power Enhancement Techniques for SO-8 Power MOSFETs*, Fairchild Semiconductor application note AN1029, April 1996, http://www.fairchildsemi.com.

7. Rob Blattner, Wharton McDaniel, *Thermal Management in On-Board DC-to-DC Power Conversion,* Temic application note, http://www.temic.com.

EMI/RFI CONSIDERATIONS

Electromagnetic interference (EMI) has become a hot topic in the last few years among circuit designers and systems engineers. Although the subject matter and prior art have been in existence for over the last 50 years or so, the advent of portable and high-frequency industrial and consumer electronics has provided a comfortable standard of living for many EMI testing engineers, consultants, and publishers. With the help of EDN Magazine and Kimmel Gerke Associates, this section will highlight general issues of EMC (electromagnetic compatibility) to familiarize the system/circuit designer with this subject and to illustrate proven techniques for protection against EMI.

A PRIMER ON EMI REGULATIONS

The intent of this section is to summarize the different types of electromagnetic compatibility (EMC) regulations imposed on equipment manufacturers, both voluntary and mandatory. Published EMC regulations apply at this time only to equipment and systems, and not to components. Thus, EMI *hardened* equipment does not necessarily imply that each of the components used (integrated circuits, especially) in the equipment must also be EMI *hardened.*

Commercial Equipment

The two driving forces behind commercial EMI regulations are the FCC (Federal Communications Commission) in the U. S. and the VDE (Verband Deutscher Electrotechniker) in Germany. VDE regulations are more restrictive than the FCC's with regard to emissions and radiation, but the European Community will be adding immunity to RF, electrostatic discharge, and power-line disturbances to the VDE regulations, and now requires mandatory compliance. In Japan, commercial EMC regulations are covered under the VCCI (Voluntary Control Council for Interference) standards and, implied by the name, are much looser than their FCC and VDE counterparts.

All commercial EMI regulations primarily focus on *radiated* emissions, specifically to protect nearby radio and television receivers, although both FCC and VDE standards are less stringent with respect to *conducted* interference (by a factor of 10 over radiated levels). The FCC Part 15 and VDE 0871 regulations group commercial equipment into two classes: Class A, for all products intended for business environments; and Class B, for all products used in residential applications. For example, Figure 8.58 illustrates the electric-field emission limits of commercial computer equipment for both FCC Part 15 and VDE 0871 compliance.

RADIATED EMISSION LIMITS FOR COMMERCIAL COMPUTER EQUIPMENT

Frequency (MHz)	Class A (at 3m)	Class B (at 3m)
30 - 88	300 µV/m	100 µV/m
88 - 216	500 µV/m	150 µV/m
216 - 1000	700 µV/m	200 µV/m

Figure 8.58

In addition to the already stringent VDE emission limits, the European Community EMC standards (IEC and IEEE) now requires mandatory compliance to these additional EMI threats: Immunity to RF fields, electrostatic discharge, and power-line disturbances. All equipment/systems marketed in Europe must exhibit an immunity to RF field strengths of 1-10V/m (IEC standard 801-3), electrostatic discharge (generated by human contact or through material movement) in the range of 10-15kV (IEC standard 801-2), and power-line disturbances of 4kV EFTs (extremely fast transients, IEC standard 801-4) and 6kV lightning surges (IEEE standard C62.41).

Military Equipment

The defining EMC specification for military equipment is MIL-STD-461 which applies to radiated equipment emissions and equipment susceptibility to interference. Radiated emission limits are very typically 10 to 100 times more stringent than the levels shown in Figure 8.58. Required limits on immunity to RF fields are typically 200 times more stringent (RF field strengths of 5-50mV/m) than the limits for commercial equipment.

Medical Equipment

Although not yet mandatory (as of December, 1997), EMC regulations for medical equipment are presently being defined by the FDA (Food and Drug Administration) in the USA and the European Community. The primary focus of these EMC regulations will be on immunity to RF fields, electrostatic discharge, and power-line disturbances, and may very well be more stringent than the limits spelled out in MIL-STD-461. The primary objective of the medical EMC regulations is to guarantee safety to humans.

Industrial- and Process-Control Equipment

Presently, equipment designed and marketed for industrial- and process-control applications are not required to meet pre-existing mandatory EMC regulations. In fact, manufacturers are exempt from complying to any standard in the USA. However, since industrial environments are very much electrically *hostile*, all

equipment manufacturers are required to comply with all European Community EMC regulations as of 1996.

Automotive Equipment

Perhaps the most difficult and hostile environment in which electrical circuits and systems must operate is that found in the automobile. All of the key EMI threats to electrical systems exist here. In addition, operating temperature extremes, moisture, dirt, and toxic chemicals further exacerbate the problem. To complicate matters further, standard techniques (ferrite beads, feed-through capacitors, inductors, resistors, shielded cables, wires, and connectors) used in other systems are not generally used in automotive applications because of the cost of the additional components.

Presently, automotive EMC regulations, defined by the very comprehensive SAE Standards J551 and J1113, are not yet mandatory. They are, however, very rigorous. SAE standard J551 applies to vehicle-level EMC specifications, and standard J1113 (functionally similar to MIL-STD-461) applies to all automotive electronic modules. For example, the J1113 specification requires that electronic modules cannot radiate electric fields greater than 300nV/m at a distance of 3 meters. This is roughly 1000 times more stringent than the FCC Part 15 Class A specification. In many applications, automotive manufacturers are imposing J1113 RF field immunity limits on *each of the active components* used in these modules. Thus, in the very near future, automotive manufacturers will require that IC products comply with existing EMC standards and regulations.

EMC Regulations' Impact on Design

In all these applications and many more, complying with mandatory EMC regulations will require careful design of individual circuits, modules, and systems using established techniques for cable shielding, signal and power-line filtering against both small- and large-scale disturbances, and sound multi-layer PCB layouts. The key to success is to incorporate sound EMC principles early in the design phase to avoid time-consuming and expensive redesign efforts.

A DIAGNOSTIC FRAMEWORK FOR EMI/RFI PROBLEM SOLVING

With any problem, a strategy should be developed before any effort is expended trying to solve it. This approach is similar to the scientific method: initial circuit misbehavior is noted, theories are postulated, experiments designed to test the theories are conducted, and results are again noted. This process continues until all theories have been tested and expected results achieved and recorded. With respect to EMI, a problem solving framework has been developed. As shown in Figure 8.59, the model suggested by Kimmel-Gerke in [Reference 1] illustrates that all three elements (a *source*, a *receptor* or *victim*, and a *path* between the two) must exist in order to be considered an EMI problem. The sources of electromagnetic interference can take on many forms, and the ever-increasing number of portable instrumentation and personal communications/computation equipment only adds the number of possible sources and receptors.

A DIAGNOSTIC FRAMEWORK FOR EMI

ANY INTERFERENCE PROBLEM CAN BE BROKEN DOWN INTO:

- **The SOURCE of interference**
- **The RECEPTOR of interference**
- **The PATH coupling the source to the receptor**

SOURCES	PATHS	RECEPTORS
Microcontroller ◆ Analog ◆ Digital	Radiated ◆ EM Fields ◆ Crosstalk Capacitive Inductive	Microcontroller ◆ Analog ◆ Digital Communications ◆ Receivers
ESD Communications Transmitters Power Disturbances Lightning	Conducted ◆ Signal ◆ Power ◆ Ground	Other Electronic Systems

Figure 8.59

Interfering signals reach the receptor by *conduction* (the circuit or system interconnections) or *radiation* (parasitic mutual inductance and/or parasitic capacitance). In general, if the frequencies of the interference are less than 30MHz, the primary means by which interference is coupled is through the *interconnects*. Between 30MHz and 300MHz, the primary coupling mechanism is *cable radiation and connector leakage*. At frequencies greater than 300MHz, the primary mechanism is *slot and board radiation*. There are many cases where the interference is broadband, and the coupling mechanisms are combinations of the above.

When all three elements exist together, a framework for solving any EMI problem can be drawn from Figure 8.60. There are three types of interference with which the circuit or system designer must contend. The first type of interference is that generated by and emitted from an instrument; this is known as circuit/system *emission* and can be either *conducted* or *radiated*. An example of this would be the personal computer. Portable and desktop computers must pass the stringent FCC Part 15 specifications prior to general use.

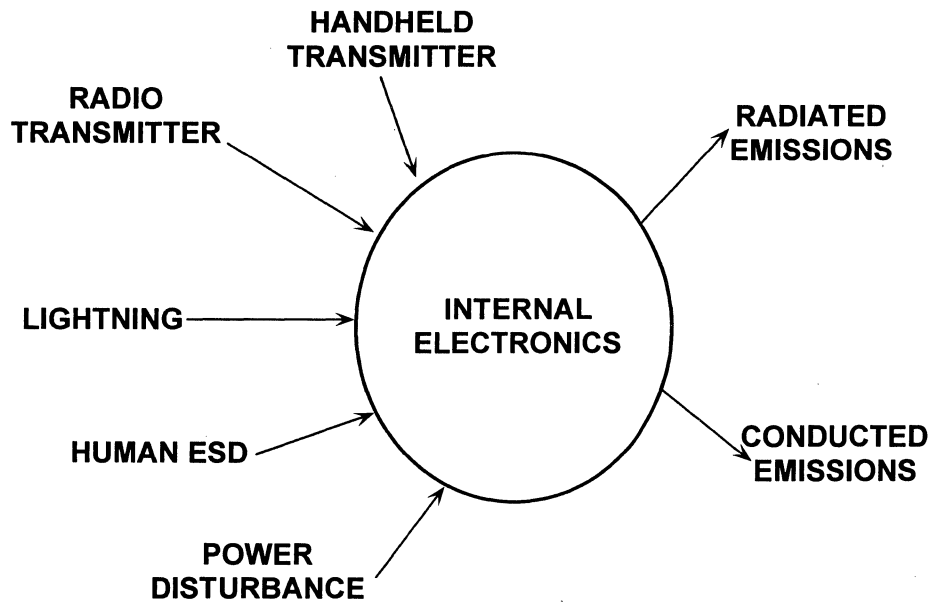


Figure 8.60

The second type of interference is circuit or system *immunity*. This describes the behavior of an instrument when it is exposed to large electromagnetic fields, primarily electric fields with an intensity in the range of 1 to 10V/m at a distance of 3 meters. Another term for immunity is *susceptibility*, and it describes circuit/system behavior against radiated or conducted interference.

The third type of interference is *internal*. Although not directly shown on the figure, internal interference can be high-speed digital circuitry within the equipment which affects sensitive analog (or other digital circuitry), or noisy power supplies which can contaminate both analog and digital circuits. Internal interference often occurs between digital and analog circuits, or between motors or relays and digital circuits. In mixed signal environments, the digital portion of the system often interferes with analog circuitry. In some systems, the internal interference reaches such high levels that even very high-speed digital circuitry can affect other low-speed digital circuitry as well as analog circuits.

In addition to the source-path-receptor model for analyzing EMI-related problems, Kimmel Gerke Associates have also introduced the FAT-ID concept [Reference 1]. FAT-ID is an acronym that describes the five key elements inherent in any EMI problem. These five key parameters are: *frequency*, *amplitude*, *time*, *impedance*, and *distance*.

The *frequency* of the offending signal suggests its path. For example, the path of low-frequency interference is often the circuit conductors. As the interference frequency increases, it will take the path of least impedance, usually stray capacitance. In this case, the coupling mechanism is radiation.

Time and frequency in EMI problems are interchangeable. In fact, the physics of EMI shows that the time response of signals contains all the necessary information to construct the spectral response of the interference. In digital systems, both the signal rise time and pulse repetition rate produce spectral components according to the following relationship:

$$f_{EMI} = \frac{1}{\pi \cdot t_{rise}} \qquad \text{Eq. 8.1}$$

For example, a pulse having a 1ns rise time is equivalent to an EMI frequency of over 300MHz. This time-frequency relationship can also be applied to high-speed analog circuits, where slew rates in excess of 1000V/μs and gain-bandwidth products greater than 500MHz are not uncommon.

When this concept is applied to instruments and systems, EMI emissions are again functions of signal rise time and pulse repetition rates. Spectrum analyzers and high speed oscilloscopes used with voltage and current probes are very useful tools in quantifying the effects of EMI on circuits and systems.

Another important parameter in the analysis of EMI problems is the physical dimensions of cables, wires, and enclosures. Cables can behave as either passive antennas (receptors) or very efficient transmitters (sources) of interference. Their physical length and their shield must be carefully examined where EMI is a concern. As previously mentioned, the behavior of simple conductors is a function of length, cross-sectional area, and frequency. Openings in equipment enclosures can behave as slot antennas, thereby allowing EMI energy to affect the internal electronics.

PASSIVE COMPONENTS: YOUR ARSENAL AGAINST EMI

Minimizing the effects of EMI requires that the circuit/system designer be completely aware of the primary arsenal in the battle against interference: *passive components*. To use successfully these components, the designer must understand their non-ideal behavior. For example, Figure 8.61 illustrates the *real* behavior of the passive components used in circuit design. At very high frequencies, wires become transmission lines, capacitors become inductors, inductors become capacitors, and resistors behave as resonant circuits.

ALL PASSIVE COMPONENTS EXHIBIT "NON-IDEAL" BEHAVIOR

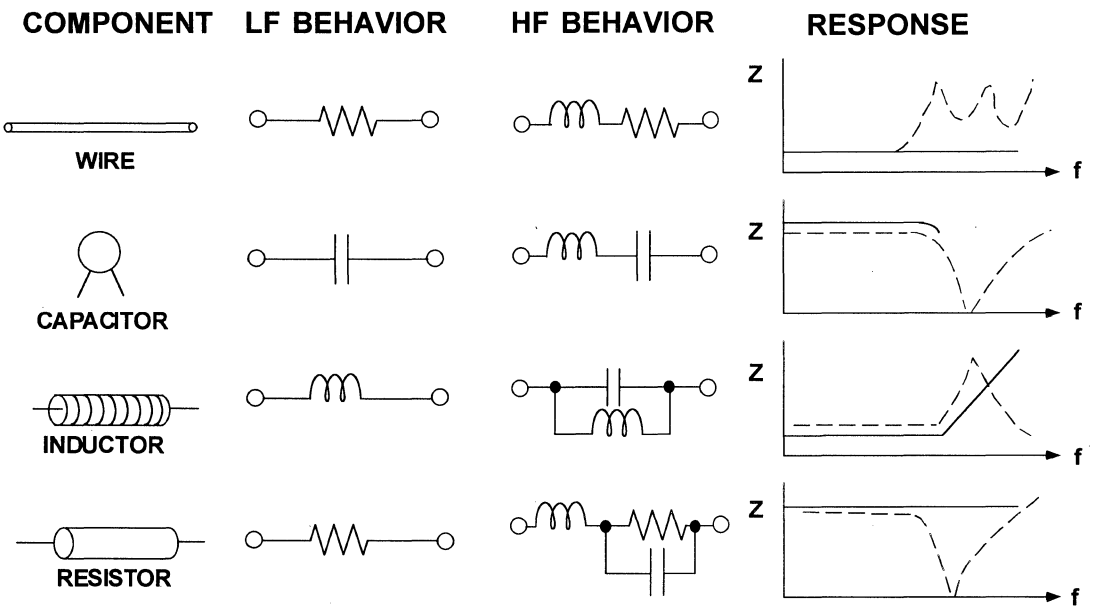


Figure 8.61

A specific case in point is the frequency response of a simple wire compared to that of a ground plane. In many circuits, wires are used as either power or signal returns, and there is no ground plane. A wire will behave as a very low resistance (less than 0.02Ω/ft for 22-gauge wire) at low frequencies, but because of its parasitic inductance of approximately 20nH/inch, it becomes inductive at frequencies above 13kHz. Furthermore, depending on size and routing of the wire and the frequencies involved, it ultimately becomes a transmission line with an uncontrolled impedance. From our knowledge of RF, unterminated transmission lines become antennas with gain. On the other hand, large area ground planes are much more well-behaved, and maintain a low impedance over a wide range of frequencies. With a good understanding of the behavior of *real* components, a strategy can now be developed to find solutions to most EMI problems.

RADIO FREQUENCY INTERFERENCE

The world is rich in radio transmitters: radio and TV stations, mobile radios, computers, electric motors, garage door openers, electric jackhammers, and countless others. All this electrical activity can affect circuit/system performance and, in extreme cases, may render it inoperable. Regardless of the location and magnitude of the interference, circuits/systems must have a minimum level of immunity to radio frequency interference (RFI). The next section will cover two general means by which RFI can disrupt normal instrument operation: the direct effects of RFI sensitive analog circuits, and the effects of RFI on shielded cables.

Two terms are typically used in describing the sensitivity of an electronic system to RF fields. In communications, radio engineers define *immunity* to be an instrument's *susceptibility to the applied RFI power density at the unit.* In more general EMI analysis, the *electric-field intensity* is used to describe RFI stimulus. For comparative purposes, Equation 8.2 can be used to convert electric-field intensity to power density and vice-versa:

$$\vec{E}\left(\frac{V}{m}\right) = 61.4\sqrt{P_T\left(\frac{mW}{cm^2}\right)} \quad \text{Eq. 8.2}$$

where E = Electric Field Strength, in volts per meter, and
P_T = Transmitted power, in milliwatts per cm^2.

From the standpoint of the source-path-receptor model, the *strength of the electric field,* E, surrounding the receptor is a function of *transmitted power, antenna gain,* and *distance* from the source of the disturbance. An approximation for the electric-field intensity (for both near- and far-field sources) in these terms is given by Equation 8.3:

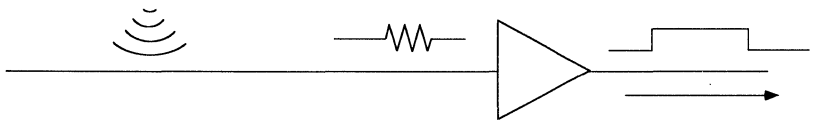
$$\vec{E}\left(\frac{V}{m}\right) = 5.5\left(\frac{\sqrt{P_T \cdot G_A}}{d}\right) \quad \text{Eq. 8.3}$$

where E = Electric field intensity, in V/m;
P_T = Transmitted power, in mW/cm^2;
G_A = Antenna gain (numerical); and
d = distance from source, in meters

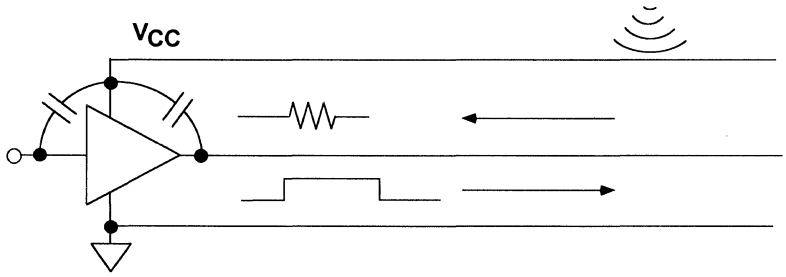
For example, a 1W hand-held radio at a distance of 1 meter can generate an electric-field of 5.5V/m, whereas a 10kW radio transmission station located 1km away generates a field smaller than 0.6V/m.

Analog circuits are generally more sensitive to RF fields than digital circuits because analog circuits, operating at high gains, must be able to resolve signals in the microvolt/millivolt region. Digital circuits, on the other hand, are more immune to RF fields because of their larger signal swings and noise margins. As shown in Figure 8.62, RF fields can use inductive and/or capacitive coupling paths to generate noise currents and voltages which are amplified by high-impedance analog instrumentation. In many cases, out-of-band noise signals are detected and rectified by these circuits. The result of the RFI rectification is usually unexplained offset voltage shifts in the circuit or in the system.

RFI CAN CAUSE RECTIFICATION IN SENSITIVE ANALOG CIRCUITS



- INPUTS PICK UP HIGH FREQUENCY ENERGY ON SIGNAL LINE, WHICH IS DETECTED BY THE AMPLIFIER



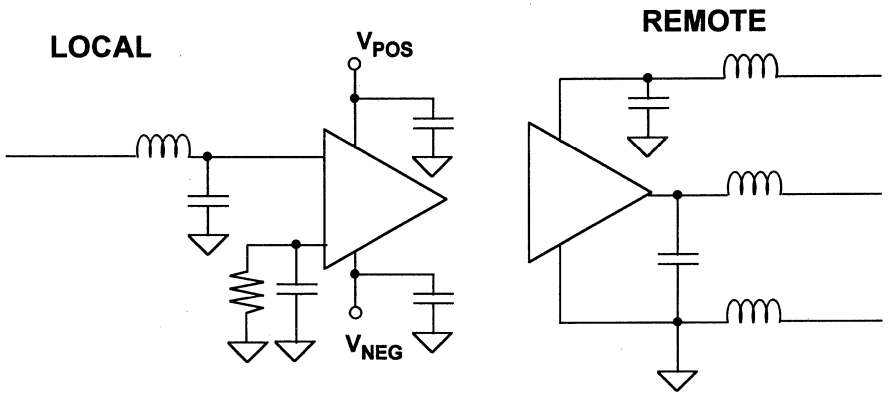
- OUTPUT DRIVERS CAN BE JAMMED, TOO: ENERGY COUPLES BACK TO INPUT VIA V_{CC} OR SIGNAL LINE AND THEN IS DETECTED OR AMPLIFIED

Figure 8.62

There are techniques that can be used to protect analog circuits against interference from RF fields (see Figure 8.63). The three general points of RFI coupling are *signal inputs*, *signal outputs*, and *power supplies*. At a minimum, all power supply pin connections on analog and digital ICs should be decoupled with 0.1μF ceramic capacitors. As was shown in Reference 3, low-pass filters, whose cutoff frequencies are set no higher than 10 to 100 times the signal bandwidth, can be used at the inputs and the outputs of signal conditioning circuitry to filter noise.

Care must be taken to ensure that the low pass filters (LPFs) are effective at the highest RF interference frequency expected. As illustrated in Figure 8.64, real low-pass filters may exhibit *leakage* at high frequencies. Their inductors can lose their effectiveness due to parasitic capacitance, and capacitors can lose their effectiveness due to parasitic inductance. A rule of thumb is that a conventional low-pass filter (made up of a single capacitor and inductor) can begin to *leak* when the applied signal frequency is 100 to 1000 higher than the filter's cutoff frequency. For example, a 10kHz LPF would not be considered very efficient at filtering frequencies above 1MHz.

KEEPING RFI AWAY FROM ANALOG CIRCUITS



- **Decouple all voltage supplies to analog chip with high-frequency capacitors**
- **Use high-frequency filters on all lines that leave the board**
- **Use high-frequency filters on the voltage reference if it is not grounded**

Figure 8.63

A SINGLE LOW PASS FILTER LOSES EFFECTIVENESS AT 100 - 1000 $f3_{dB}$

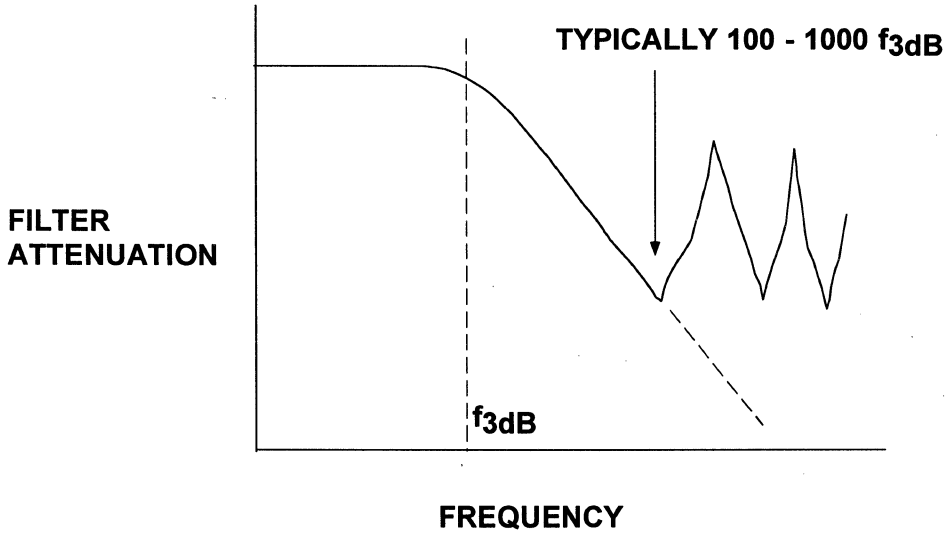
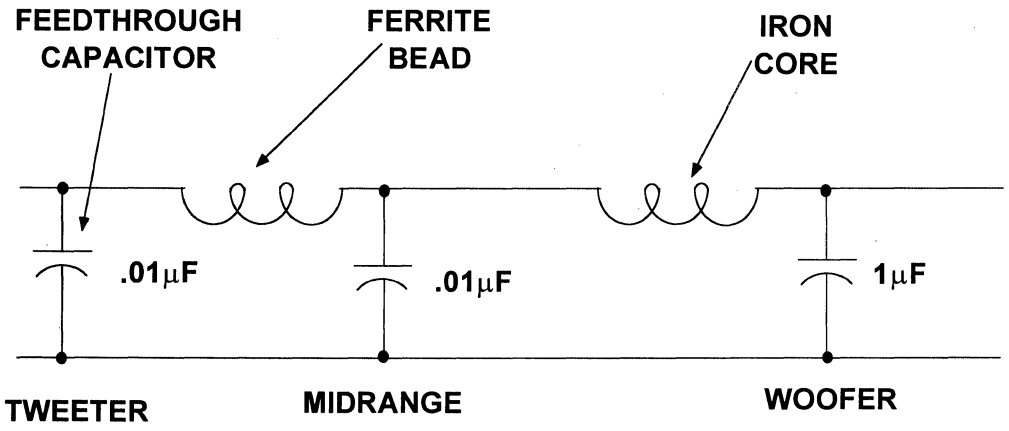


Figure 8.64

Rather than use one LPF stage, it is recommended that the interference frequency bands be separated into *low-band*, *mid-band*, and *high-band*, and then use individual filters for each band. Kimmel Gerke Associates use the stereo speaker analogy of *woofer-midrange-tweeter* for RFI low-pass filter design illustrated in Figure 8.65. In this approach, low frequencies are grouped from 10kHz to 1MHz, mid-band frequencies are grouped from 1MHz to 100MHz, and high frequencies grouped from 100MHz to 1GHz. In the case of a shielded cable input/output, the high frequency section should be located close to the shield to prevent high-frequency leakage at the shield boundary. This is commonly referred to as *feed-through* protection. For applications where shields are not required at the inputs/outputs, then the preferred method is to locate the high frequency filter section as close the analog circuit as possible. This is to prevent the possibility of pickup from other parts of the circuit.

MULTISTAGE FILTERS ARE MORE EFFECTIVE



STEREO SPEAKER ANALOGY

Figure 8.65

Another cause of filter failure is illustrated in Figure 8.66. If there is any impedance in the ground connection (for example, a long wire or narrow trace connected to the ground plane), then the high-frequency noise uses this impedance path to bypass the filter completely. Filter grounds must be broadband and tied to low-impedance points or planes for optimum performance. High frequency capacitor leads should be kept as short as possible, and low-inductance surface-mounted ceramic chip capacitors are preferable.

NON-ZERO (INDUCTIVE AND/OR RESISTIVE) FILTER GROUND REDUCES EFFECTIVENESS

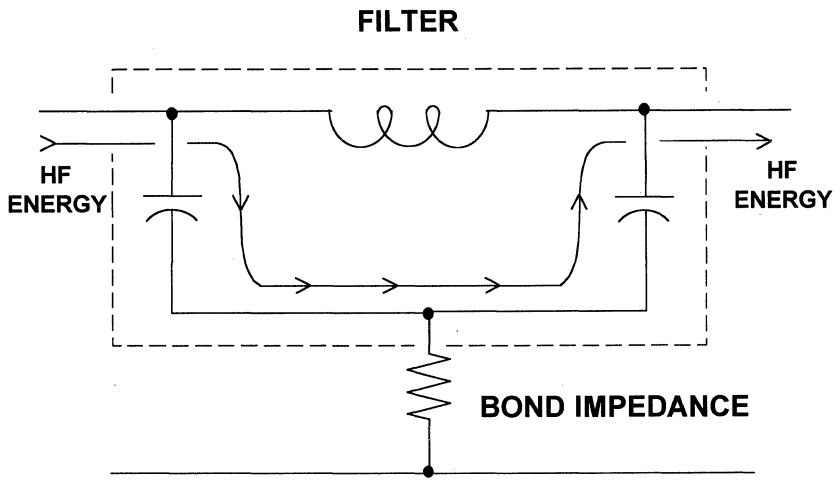


Figure 8.66

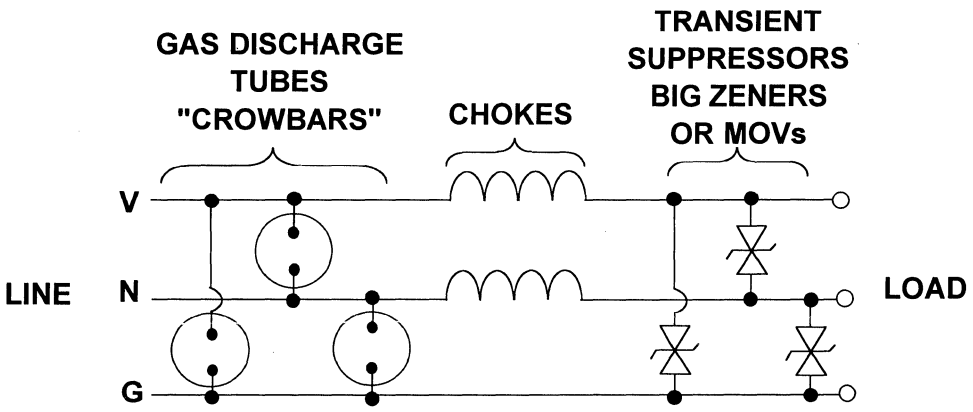
SOLUTIONS FOR POWER-LINE DISTURBANCES

The goal of this next section is not to describe in detail all the circuit/system failure mechanisms which can result from power-line disturbances or faults. Nor is it the intent of this section to describe methods by which power-line disturbances can be prevented. Instead, this section will describe techniques that allow circuits and systems to accommodate *transient* power-line disturbances.

Figure 8.67 is an example of a hybrid power transient protection network commonly used in many applications where lightning transients or other power-line disturbances are prevalent. These networks can be designed to provide protection against transients as high as 10kV and as fast as 10ns. Gas discharge tubes (crowbars) and large geometry zener diodes (clamps) are used to provide both differential and common-mode protection. Metal-oxide varistors (MOVs) can be substituted for the zener diodes in less critical, or in more compact designs. Chokes are used to limit the surge current until the gas discharge tubes fire.

Commercial EMI filters, as illustrated in Figure 8.68, can be used to filter less catastrophic transients or high-frequency interference. These EMI filters provide both common-mode and differential mode filtering. An optional choke in the safety ground can provide additional protection against common-mode noise. The value of this choke cannot be too large, however, because its resistance may affect power-line fault clearing. These filters work in both directions: they are not only protect the equipment from surges on the power line but also prevent transients from the internal switching power supplies from corrupting the power line.

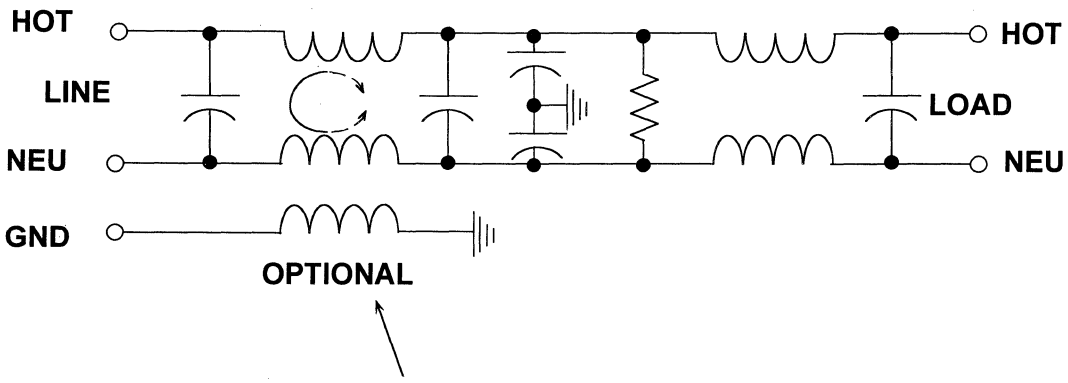
POWER LINE DISTURBANCES CAN GENERATE EMI



■ COMMON-MODE AND DIFFERENTIAL MODE PROTECTION

Figure 8.67

SCHEMATIC FOR A COMMERCIAL POWER LINE FILTER



NOTE: OPTIONAL CHOKE ADDED FOR COMMON-MODE PROTECTION

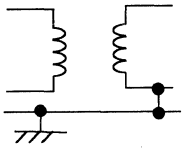
Figure 8.68

Transformers provide the best common-mode power line isolation. They provide good protection at low frequencies (<1MHz), or for transients with rise and fall times greater than 300ns. Most motor noise and lightning transients are in this range, so isolation transformers work well for these types of disturbances. Although the isolation between input and output is galvanic, isolation transformers do not provide sufficient protection against extremely fast transients (<10ns) or those caused by high-amplitude electrostatic discharge (1 to 3ns). As illustrated in Figure 8.69, isolation transformers can be designed for various levels of differential- or

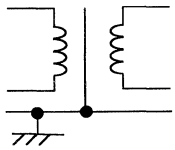
common-mode protection. For differential-mode noise rejection, the Faraday shield is connected to the neutral, and for common-mode noise rejection, the shield is connected to the safety ground.

FARADAY SHIELDS IN ISOLATION TRANSFORMERS PROVIDE INCREASING LEVELS OF PROTECTION

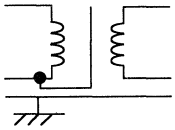
- **STANDARD TRANSFORMER - NO SHIELD**
  - NOTE CONNECTION FROM SECONDARY TO SAFETY GROUND TO ELIMINATE GROUND-TO-NEUTRAL VOLTAGE



- **SINGLE FARADAY SHIELD**
  - CONNECT TO SAFETY GROUND FOR COMMON-MODE PROTECTION



- **SINGLE FARADAY SHIELD**
  - CONNECT TO NOISY-SIDE NEUTRAL WIRE FOR DIFFERENTIAL-MODE PROTECTION



- **TRIPLE FARADAY SHIELD**
  - CONNECT TO SAFETY GROUND FOR COMMON MODE
  - CONNECT TO NEUTRALS FOR DIFFERENTIAL MODE

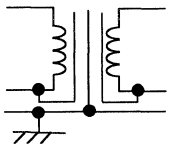


Figure 8.69

PRINTED CIRCUIT BOARD DESIGN FOR EMI PROTECTION

This section will summarize general points regarding the most critical portion of the design phase: the printed circuit board layout. It is at this stage where the performance of the system is most often compromised. This is not only true for signal-path performance, but also for the system's susceptibility to electromagnetic interference and the amount of electromagnetic energy radiated by the system. Failure to implement sound PCB layout techniques will very likely lead to system/instrument EMC failures.

Figure 8.70 is a real-world printed circuit board layout which shows all the paths through which high-frequency noise can couple/radiate into/out of the circuit. Although the diagram shows digital circuitry, the same points are applicable to precision analog, high-speed analog, or mixed analog/digital circuits. Identifying critical circuits and paths helps in designing the PCB layout for both low emissions and susceptibility to radiated and conducted external and internal noise sources.

METHODS BY WHICH HIGH FREQUENCY ENERGY COUPLE AND RADIATE INTO CIRCUITRY VIA PLACEMENT

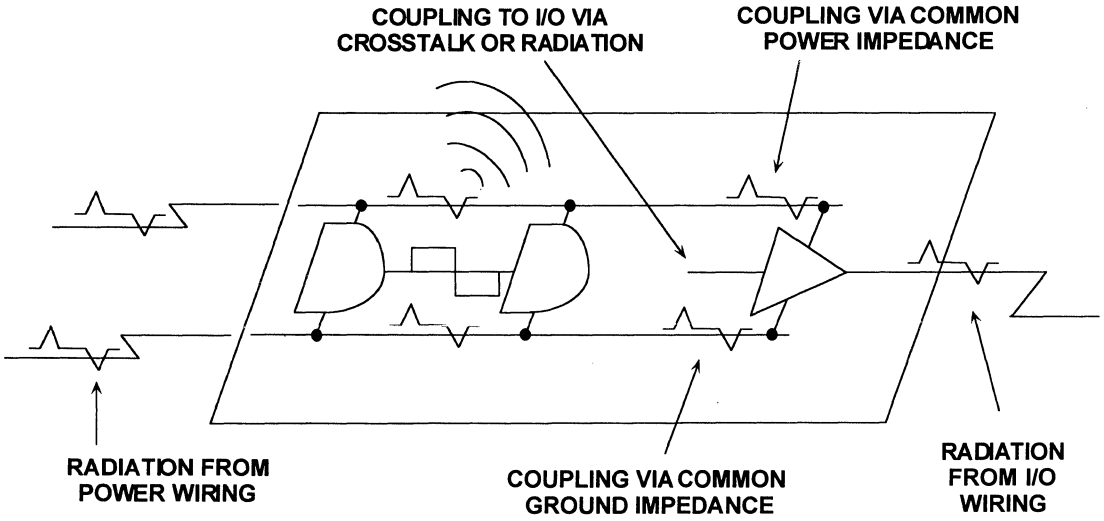


Figure 8.70

A key point in minimizing noise problems in a design is to *choose devices no faster than actually required by the application.* Many designers assume that faster is better: fast logic is better than slow, high bandwidth amplifiers are clearly better than low bandwidth ones, and fast DACs and ADCs are better, even if the speed is not required by the system. Unfortunately, faster is not better, but worse where EMI is concerned.

Many fast DACs and ADCs have digital inputs and outputs with rise and fall times in the nanosecond region. Because of their wide bandwidth, the sampling clock and the digital inputs can respond to any form of high frequency noise, even glitches as narrow as 1 to 3ns. These high speed data converters and amplifiers are easy prey for the high frequency noise of microprocessors, digital signal processors, motors, switching regulators, hand-held radios, electric jackhammers, etc. With some of these high-speed devices, a small amount of input/output filtering may be required to desensitize the circuit from its EMI/RFI environment. Adding a small ferrite bead just before the decoupling capacitor as shown in Figure 8.71 is very effective in filtering high frequency noise on the supply lines. For those circuits that require bipolar supplies, this technique should be applied to both positive and negative supply lines.

To help reduce the emissions generated by extremely fast moving digital signals at DAC inputs or ADC outputs, a small resistor or ferrite bead may be required at each digital input/output.

POWER SUPPLY FILTERING AND SIGNAL LINE SNUBBING GREATLY REDUCES EMI EMISSIONS

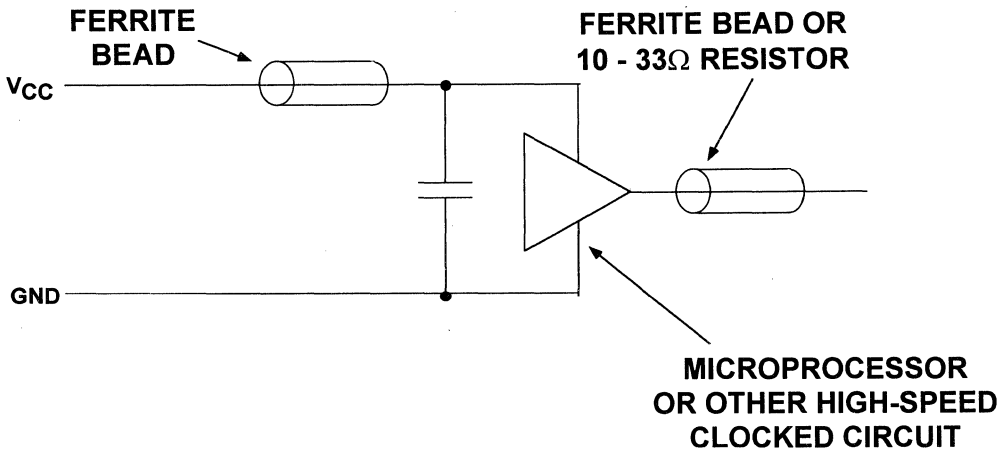


Figure 8.71

Once the system's critical paths and circuits have been identified, the next step in implementing sound PCB layout is to partition the printed circuit board according to circuit function. This involves the appropriate use of power, ground, and signal planes. Good PCB layouts also isolate critical analog paths from sources of high interference (I/O lines and connectors, for example). High frequency circuits (analog and digital) should be separated from low frequency ones. Furthermore, automatic signal routing CAD layout software should be used with extreme caution, and critical paths routed by hand.

Properly designed multilayer printed circuit boards can reduce EMI emissions and increase immunity to RF fields by a factor of 10 or more compared to double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted with signal crossovers, etc. If the system has separate analog and digital ground and power planes, the analog ground plane should be underneath the analog power plane, and similarly, the digital ground plane should be underneath the digital power plane. There should be no overlap between analog and digital ground planes nor analog and digital power planes.

The preferred multi-layer board arrangement is to embed the signal traces between the power and ground planes, as shown in Figure 8.72. These low-impedance planes form very high-frequency *stripline* transmission lines with the signal traces. The return current path for a high frequency signal on a trace is located directly above and below the trace on the ground/power planes. The high frequency signal is thus contained inside the PCB, thereby minimizing emissions. The embedded signal trace approach has an obvious disadvantage: debugging circuit traces that are hidden from plain view is difficult.

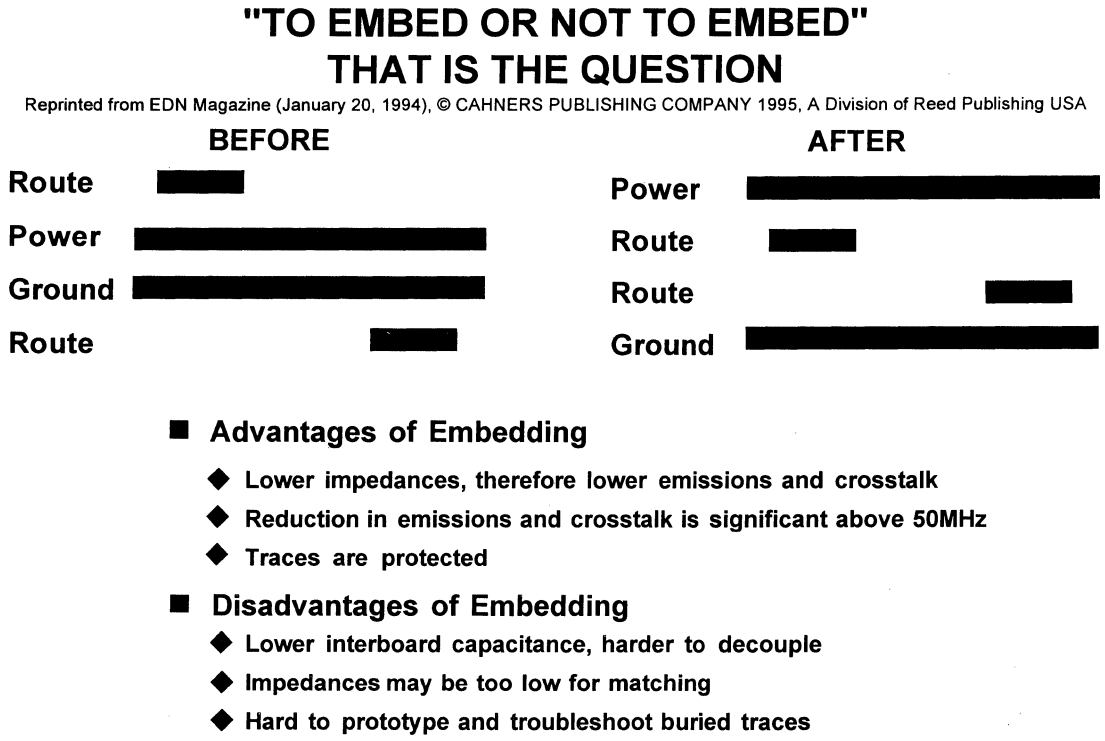


Figure 8.72

Much has been written about terminating printed circuit board traces in their characteristic impedance to avoid reflections. A good rule-of-thumb to determine when this is necessary is as follows: *Terminate the line in its characteristic impedance when the one-way propagation delay of the PCB track is equal to or greater than one-half the applied signal rise/fall time (whichever edge is faster).* A conservative approach is to use a 2 inch (PCB track length)/nanosecond (rise-, fall-time) criterion. For example, PCB tracks for high-speed logic with rise/fall time of 5ns should be terminated in their characteristic impedance if the track length is equal to or greater than 10 inches (including any meanders). The 2 inch/nanosecond track length criterion is summarized in Figure 8.73 for a number of logic families.

This same 2 inch/nanosecond rule of thumb should be used with analog circuits in determining the need for transmission line techniques. For instance, if an amplifier must output a maximum frequency of f_{max}, then the equivalent risetime, t_r, can be calculated using the equation $t_r = 0.35/f_{max}$. The maximum PCB track length is then calculated by multiplying the risetime by 2 inch/nanosecond. For example, a maximum output frequency of 100MHz corresponds to a risetime of 3.5ns, and a track carrying this signal greater than 7 inches should be treated as a transmission line.

LINE TERMINATION SHOULD BE USED WHEN LENGTH OF PCB TRACK EXCEEDS 2 inches/ns

DIGITAL IC FAMILY	t_r, t_s (ns)	PCB TRACK LENGTH (inches)	PCB TRACK LENGTH (cm)
GaAs	0.1	0.2	0.5
ECL	0.75	1.5	3.8
Schottky	3	6	15
FAST	3	6	15
AS	3	6	15
AC	4	8	20
ALS	6	12	30
LS	8	16	40
TTL	10	20	50
HC	18	36	90

t_r = rise time of signal in ns
t_f = fall time of signal in ns
For analog signals @ f_{max}, calculate $t_r = t_f = 0.35 / fmax$

Figure 8.73

Equation 8.4 can be used to determine the characteristic impedance of a PCB track separated from a power/ground plane by the board's dielectric (microstrip transmission line):

$$Z_o(\Omega) = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left[\frac{5.98d}{0.89w + t}\right] \quad \text{Eq. 8.4}$$

where ε_r = dielectric constant of printed circuit board material;
d = thickness of the board between metal layers, in mils;
w = width of metal trace, in mils; and
t = thickness of metal trace, in mils.

The one-way transit time for a single metal trace over a power/ground plane can be determined from Eq. 8.5:

$$t_{pd}(ns/ft) = 1.017\sqrt{0.475\varepsilon_r + 0.67} \quad \text{Eq. 8.5}$$

For example, a standard 4-layer PCB board might use 8-mil wide, 1 ounce (1.4 mils) copper traces separated by 0.021" FR-4 (ε_r=4.7) dielectric material. The characteristic impedance and one-way transit time of such a signal trace would be 88Ω and 1.7ns/ft (7"/ns), respectively.

REFERENCES ON EMI/RFI

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SHIELDING CONCEPTS

The concepts of shielding effectiveness presented next are background material. Interested readers should consult References 1,2, and 6 cited at the end of the section for more detailed information.

Applying the concepts of shielding requires an understanding of the source of the interference, the environment surrounding the source, and the distance between the source and point of observation (the receptor or victim). If the circuit is operating close to the source (in the near-, or induction-field), then the field characteristics are determined by the source. If the circuit is remotely located (in the far-, or radiation-field), then the field characteristics are determined by the transmission medium.

A circuit operates in a near-field if its distance from the source of the interference is less than the wavelength (λ) of the interference divided by 2π, or $\lambda/2\pi$. If the distance between the circuit and the source of the interference is larger than this quantity, then the circuit operates in the far field. For instance, the interference caused by a 1ns pulse edge has an upper bandwidth of approximately 350MHz. The wavelength of a 350MHz signal is approximately 32 inches (the speed of light is approximately 12"/ns). Dividing the wavelength by 2π yields a distance of approximately 5 inches, the boundary between near- and far-field. If a circuit is within 5 inches of a 350MHz interference source, then the circuit operates in the near-field of the interference. If the distance is greater than 5 inches, the circuit operates in the far-field of the interference.

Regardless of the type of interference, there is a characteristic impedance associated with it. The characteristic, or wave impedance of a field is determined by the ratio of its electric (or E-) field to its magnetic (or H-) field. In the far field, the ratio of the electric field to the magnetic field is the characteristic (wave impedance) of free space, given by $Z_0 = 377\Omega$. In the near field, the wave-impedance is determined by the nature of the interference and its distance from the source. If the interference source is high-current and low-voltage (for example, a loop antenna or a power-line transformer), the field is predominately magnetic and exhibits a wave impedance which is less than 377Ω. If the source is low-current and high-voltage (for example, a rod antenna or a high-speed digital switching circuit), then the field is predominately electric and exhibits a wave impedance which is greater than 377Ω.

Conductive enclosures can be used to shield sensitive circuits from the effects of these external fields. These materials present an impedance mismatch to the incident interference because the impedance of the shield is lower than the wave impedance of the incident field. The effectiveness of the conductive shield depends on two things: First is the loss due to the *reflection* of the incident wave off the shielding material. Second is the loss due to the *absorption* of the transmitted wave *within* the shielding material. Both concepts are illustrated in Figure 8.74. The amount of reflection loss depends upon the type of interference and its wave impedance. The amount of absorption loss, however, is independent of the type of interference. It is the same for near- and far-field radiation, as well as for electric or magnetic fields.

REFLECTION AND ABSORPTION ARE THE TWO PRINCIPAL SHIELDING MECHANISMS

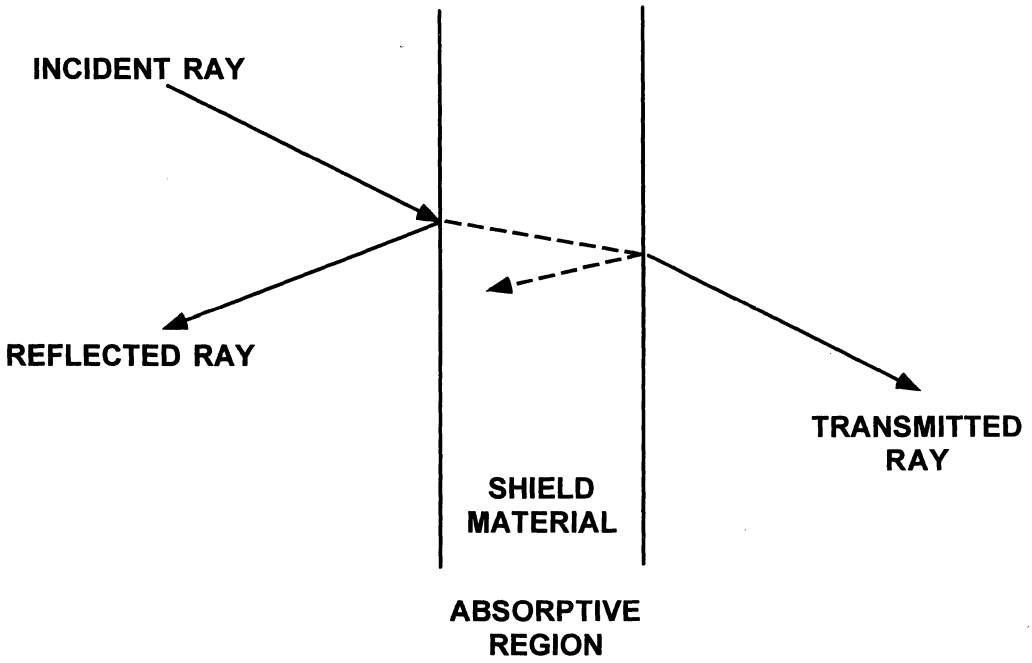


Figure 8.74

Reflection loss at the interface between two media depends on the difference in the characteristic impedances of the two media. For electric fields, reflection loss depends on the frequency of the interference and the shielding material. This loss can be expressed in dB, and is given by:

$$R_e(dB) = 322 + 10\log_{10}\left[\frac{\sigma_r}{\mu_r f^3 r^2}\right] \quad \text{Eq. 8.6}$$

where σ_r = relative conductivity of the shielding material, in Siemens per meter;
μ_r = relative permeability of the shielding material, in Henries per meter;
f = frequency of the interference, and
r = distance from source of the interference, in meters

For magnetic fields, the loss depends also on the shielding material and the frequency of the interference. Reflection loss for magnetic fields is given by:

$$R_m(dB) = 14.6 + 10\log_{10}\left[\frac{fr^2\sigma_r}{\mu_r}\right] \quad \text{Eq. 8.7}$$

and, for plane waves ($r > \lambda/2\pi$), the reflection loss is given by:

$$R_{pw}(dB) = 168 + 10\log_{10}\left[\frac{\sigma_r}{\mu_r f}\right] \qquad \text{Eq. 8.8}$$

Absorption is the second loss mechanism in shielding materials. Wave attenuation due to absorption is given by:

$$A(dB) = 3.34\ t\sqrt{\sigma_r \mu_r f} \qquad \text{Eq. 8.9}$$

where t = thickness of the shield material, in inches. This expression is valid for plane waves, electric and magnetic fields. Since the intensity of a transmitted field decreases exponentially relative to the thickness of the shielding material, the absorption loss in a shield one skin-depth (δ) thick is 9dB. Since absorption loss is proportional to thickness and inversely proportional to skin depth, increasing the thickness of the shielding material improves shielding effectiveness at high frequencies.

Reflection loss for plane waves in the far field decreases with increasing frequency because the shield impedance, Z_S, increases with frequency. Absorption loss, on the other hand, increases with frequency because skin depth decreases. For electric fields and plane waves, the primary shielding mechanism is reflection loss, and at high frequencies, the mechanism is absorption loss. For these types of interference, high conductivity materials, such as copper or aluminum, provide adequate shielding. At low frequencies, both reflection and absorption loss to magnetic fields is low; thus, it is very difficult to shield circuits from low-frequency magnetic fields. In these applications, high-permeability materials that exhibit low-reluctance provide the best protection. These low-reluctance materials provide a magnetic shunt path that diverts the magnetic field away from the protected circuit. Some characteristics of metallic materials commonly used for shielded enclosures are shown in Figure 8.75.

A properly shielded enclosure is very effective at preventing external interference from disrupting its contents as well as confining any internally-generated interference. However, in the real world, openings in the shield are often required to accommodate adjustment knobs, switches, connectors, or to provide ventilation (see Figure 8.76). Unfortunately, these openings may compromise shielding effectiveness by providing paths for high-frequency interference to enter the instrument.

CONDUCTIVITY AND PERMEABILITY FOR VARIOUS SHIELDING MATERIALS

MATERIAL	RELATIVE CONDUCTIVITY	RELATIVE PERMEABILITY
Copper	1	1
Aluminum	1	0.61
Steel	0.1	1,000
Mu-Metal	0.03	20,000

Conductivity: Ability to Conduct Electricity

Permeability: Ability to Absorb Magnetic Energy

Figure 8.75

ANY OPENING IN AN ENCLOSURE CAN ACT AS AN EMI WAVEGUIDE BY COMPROMISING SHIELDING EFFECTIVENESS

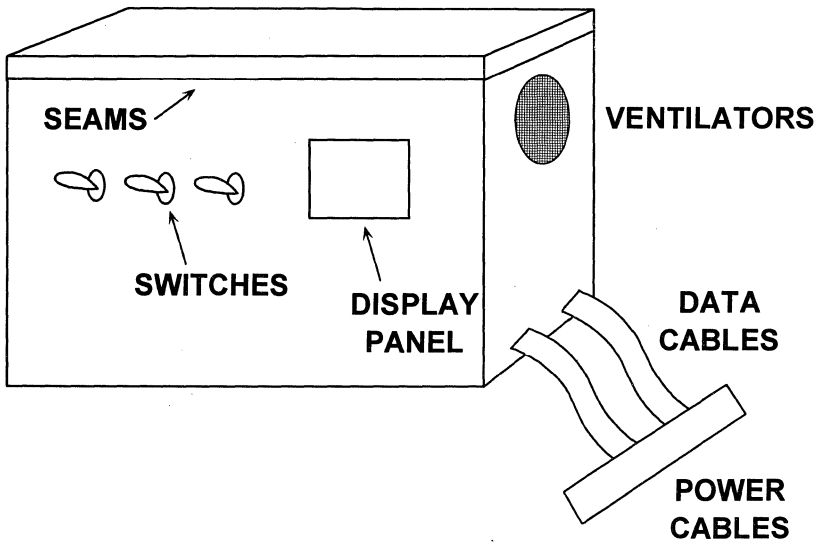


Figure 8.76

The longest dimension (not the total area) of an opening is used to evaluate the ability of external fields to enter the enclosure, because the openings behave as slot antennas. Equation 8.10 can be used to calculate the shielding effectiveness, or the susceptibility to EMI leakage or penetration, of an opening in an enclosure:

$$\text{Shielding Effectiveness (dB)} = 20\log_{10}\left(\frac{\lambda}{2 \cdot L}\right) \qquad \text{Eq. 8.10}$$

where λ = wavelength of the interference and
L = maximum dimension of the opening

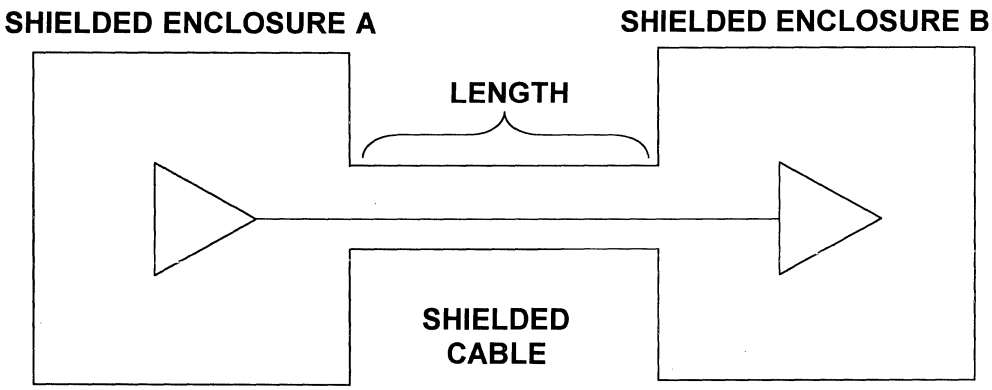
Maximum radiation of EMI through an opening occurs when the longest dimension of the opening is equal to one half-wavelength of the interference frequency (0dB shielding effectiveness). A rule-of-thumb is to keep the longest dimension less than 1/20 wavelength of the interference signal, as this provides 20dB shielding effectiveness. Furthermore, a few small openings on each side of an enclosure is preferred over many openings on one side. This is because the openings on different sides radiate energy in different directions, and as a result, shielding effectiveness is not compromised. If openings and seams cannot be avoided, then conductive gaskets, screens, and paints alone or in combination should be used judiciously to limit the longest dimension of any opening to less than 1/20 wavelength. Any cables, wires, connectors, indicators, or control shafts penetrating the enclosure should have circumferential metallic shields physically bonded to the enclosure at the point of entry. In those applications where unshielded cables/wires are used, then filters are recommended at the point of shield entry.

Sensors and Cable Shielding

The improper use of cables and their shields is a significant contributor to both radiated and conducted interference. As illustrated in Figure 8.77, effective cable and enclosure shielding confines sensitive circuitry and signals within the entire shield without compromising shielding effectiveness.

Depending on the type of interference (pickup/radiated, low/high frequency), proper cable shielding is implemented differently and is very dependent on the length of the cable. The first step is to determine whether the length of the cable is *electrically short* or *electrically long* at the frequency of concern. A cable is considered *electrically short* if the length of the cable is less than 1/20 wavelength of the highest frequency of the interference, otherwise it is *electrically long*. For example, at 50/60Hz, an *electrically short* cable is any cable length less than 150 miles, where the primary coupling mechanism for these low frequency electric fields is capacitive. As such, for any cable length less than 150 miles, the amplitude of the interference will be the same over the entire length of the cable. To protect circuits against low-frequency electric-field pickup, only one end of the shield should be returned to a low-impedance point. A generalized example of this mechanism is illustrated in Figure 8.78.

LENGTH OF SHIELDED CABLES DETERMINES AN "ELECTRICALLY LONG" OR "ELECTRICALLY SHORT" APPLICATION



FULLY SHIELDED ENCLOSURES CONNECTED BY FULLY SHIELDED CABLE KEEP ALL INTERNAL CIRCUITS AND SIGNAL LINES INSIDE THE SHIELD.

- TRANSITION REGION: 1/20 WAVELENGTH

Figure 8.77

CONNECT THE SHIELD AT ONE POINT AT THE LOAD TO PROTECT AGAINST LOW FREQUENCY (50/60Hz)

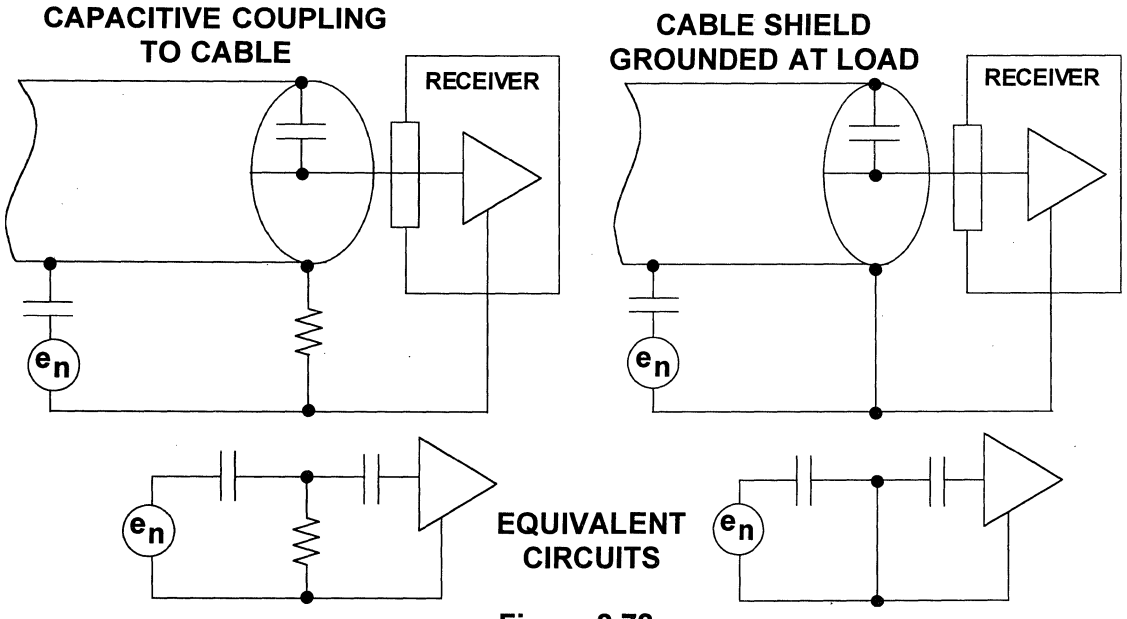


Figure 8.78

In this example, the shield is grounded at the receiver. An exception to this approach (which will be highlighted again later) is the case where line-level (>1Vrms) audio signals are transmitted over long distances using twisted pair, shielded cables. In these applications, the shield again offers protection against low-frequency interference, and an accepted approach is to ground the shield at the driver end (LF and HF ground) and ground it at the receiver with a capacitor (HF ground only).

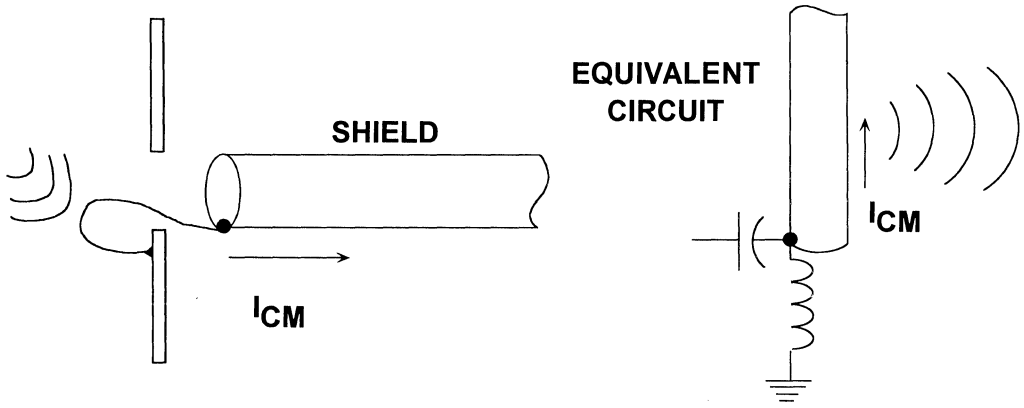
In those applications where the length of the cable is *electrically long*, or protection against high-frequency interference is required, then the preferred method is to connect the cable shield to low-impedance points at both ends (direct connection at the driving end, and capacitive connection at the receiver). Otherwise, unterminated transmission lines effects can cause reflections and standing waves along the cable. At frequencies of 10MHz and above, circumferential (360°) shield bonds and metal connectors are required to main low-impedance connections to ground.

In summary, for protection against low-frequency (<1MHz), electric-field interference, grounding the shield at one end is acceptable. For high-frequency interference (>1MHz), the preferred method is grounding the shield at both ends, using 360° circumferential bonds between the shield and the connector, and maintaining metal-to-metal continuity between the connectors and the enclosure. Low-frequency ground loops can be eliminated by replacing one of the DC shield connections to ground with a low inductance 0.01μF capacitor. This capacitor prevents low frequency ground loops and shunts high frequency interference to ground.

The best shield can be compromised by poor connection techniques. Shields often use "pig-tail" connections to make the connection to ground. A "pig-tail" connection is a single wire connection from shield to either chassis or circuit ground. This type of connection is inexpensive, but at high frequency, it does not provide low impedance. Quality shields do not leave large gaps in the cable/instrument shielding system. Shield gaps provide paths for high frequency EMI to enter the system. The cable shielding system should include the cable end connectors. Ideally, cable shield connectors should make 360° contact with the chassis ground.

As shown in Figure 8.79, pigtail terminations on cables very often cause systems to fail radiated emissions tests because high-frequency noise has coupled into the cable shield, generally through stray capacitance. If the length of the cable is considered *electrically long* at the interference frequency, then it can behave as a very efficient quarter-wave antenna. The cable pigtail forms a matching network, as shown in the s, to radiate the noise which coupled into the shield. In general, pigtails are only recommended for applications below 10kHz, such as 50/60Hz interference protection. For applications where the interference is greater than 10kHz, shielded connectors, electrically and physically connected to the chassis, should be used.

"SHIELDED" CABLE CAN CARRY HIGH FREQUENCY CURRENT AND BEHAVES AS AN ANTENNA



I_{CM} = COMMON-MODE CURRENT

Figure 8.79

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Wainwright Instruments GmbH, Widdersberger Strasse 14, DW-8138 Andechs-Frieding, Germany. Tel: +49-8152-3162, Fax: +49-8152-40525.

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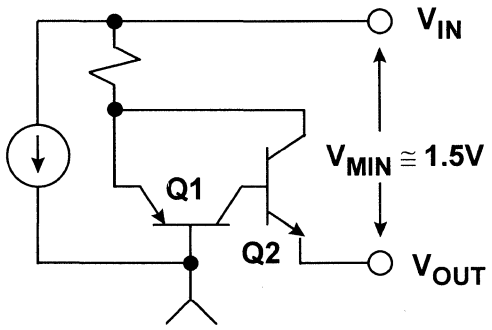
First Printing Errata Sheet (April, 1998)

ANALOG DEVICES

Page 2.8 Figure 2.6: Seventh bullet, Long-term drift should be *100ppm / 1khrs.*

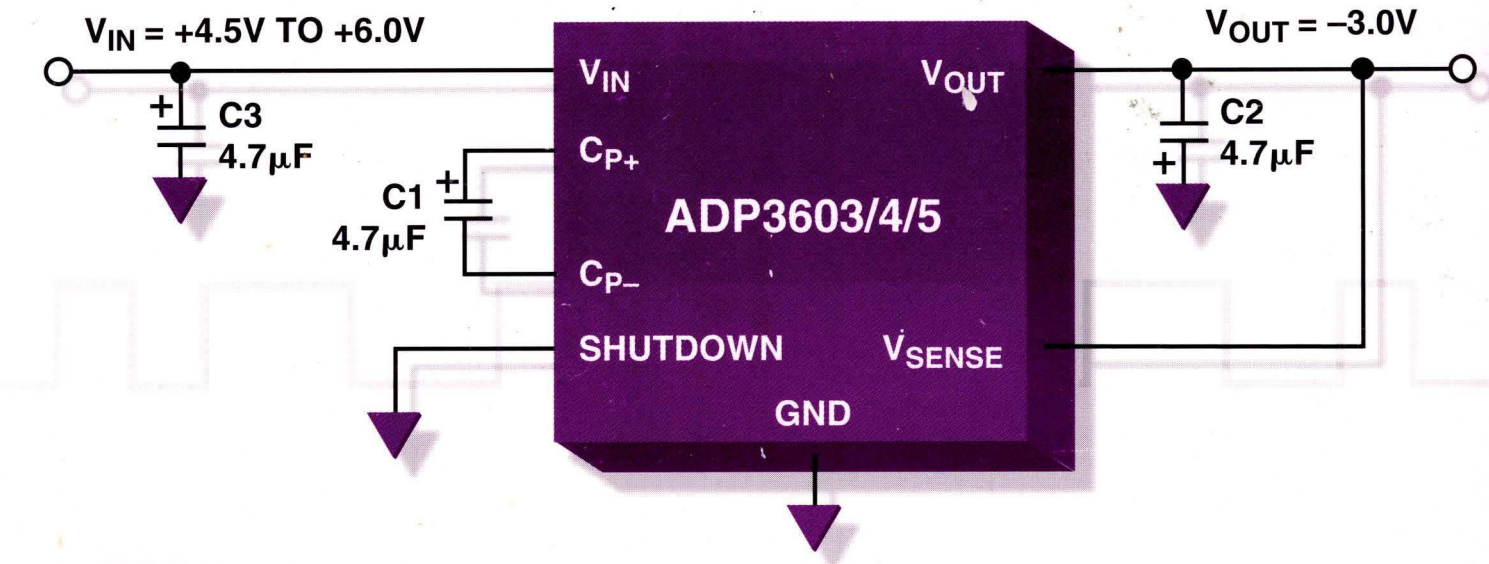
Page 2.16 Figure 2.14: Third bullet, *AD29X* should be *ADR29X.*

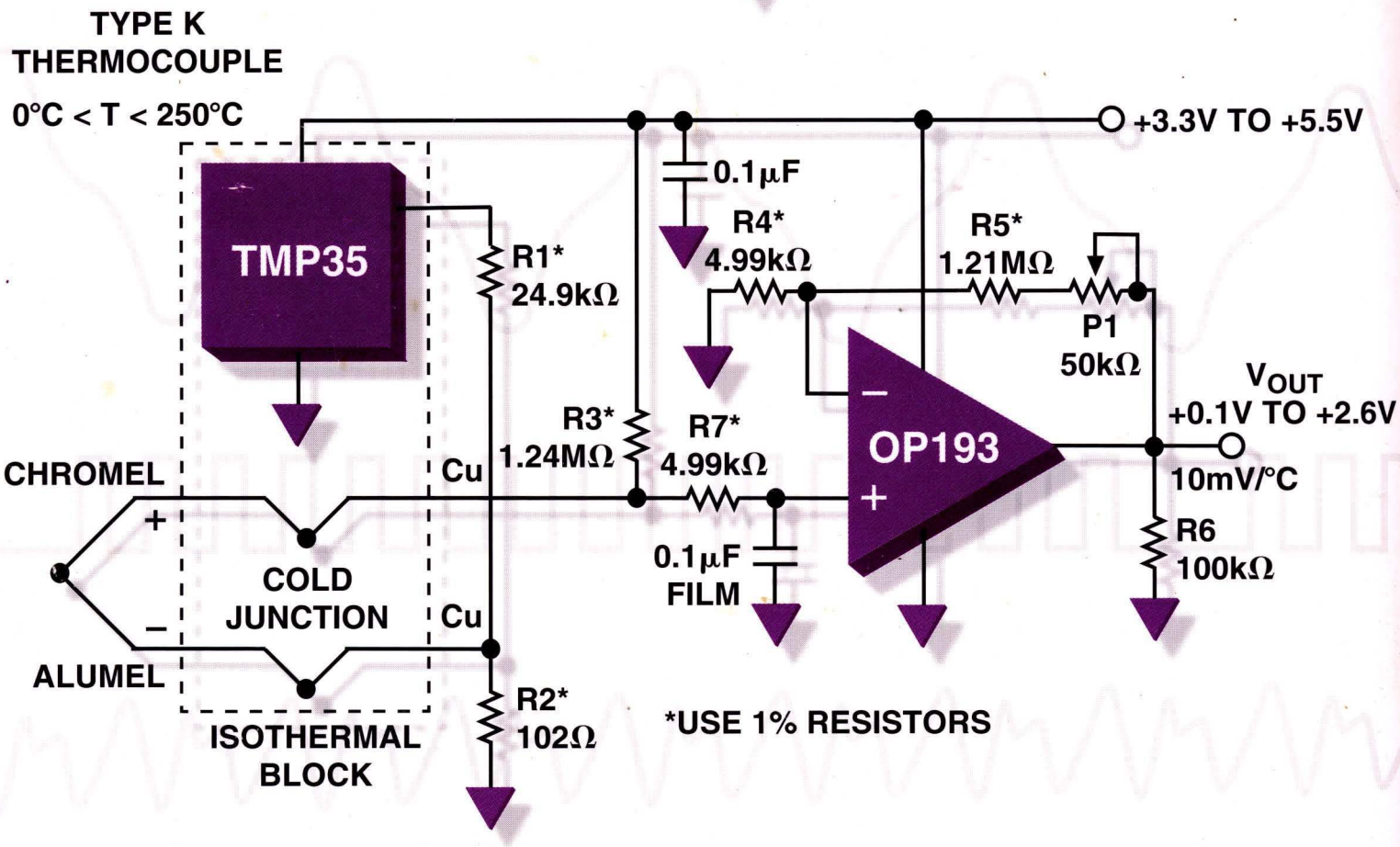
Page 2.30 Figure 2.25: (d) Diagram should be changed to:



(d) PNP/NPN

Page 6.14 Last paragraph: Delete sentence, *The ADT71 is the same as the ADT70 except the internal voltage reference is omitted.*





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