3D RAGE™ LT PRO
Graphics Controller Specifications

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Technical Reference Manual
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Release	Date	Description of Changes
1.00	Nov. 97	First General Release
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Technical Reference Manuals

3D RAGE LT PRO series

- 3D RAGE™ LT PRO Register Reference Guide (RRG-GO3300)
- 3D RAGE™ LT PRO Graphics Controller Specifications (GCS-C03300)

3D RAGE PRO series

- 3D RAGE™ PRO Register Reference Guide (RRG-G03500)
- 3D RAGE™ PRO Graphics Controller Specifications (GCS-C03500)

Table of Contents

Chapter 1: Introduction

Chapter 2: Overview

Chapter 3: Functional Description

Chapter 4: Interfaces

Chapter 5: Controller Configuration

Chapter 6: Pin Descriptions

Chapter 7: Timing Specifications

Chapter 8: Display Modes

Chapter 9: Chip Specifications

Appendix A: Layout Considerations

Index

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Chapter 1
Introduction

1.1 About This Manual

This manual is part of a set of reference documents which provide information necessary to design the *3D RAGE LT PRO* into a graphics subsystem. These documents are listed in the System Publications Index at the beginning of this manual.

The electrical and thermal characteristics described in this document are specific to the *3D RAGE LT PRO* manufactured using UMC's 0.35µm process — which has voltages of 3.3V core, 3.3/5.0V PCI I/O, 3.3V AGP, 3.3V memory interface, and 3.3V panel interface. Please contact ATI to obtain information on how to support all of ATI's graphics controllers, steppings, and foundries in one PCB design.

1.2 Conventions

1.2.1 Mnemonics

Mnemonics are used throughout this manual in place of external strap pin resistor names and signal names. Active-low signal names are identified by the # character.

The following example is the mnemonic for the Interrupt Enable strap signal:

10. ENINT#

The example below refers to the Product Type Code field that occupies bit positions 0 through 15 within the 16-bit vendor ID register in PCI configuration space:

11. SUBSYS_VEN_ID[15:0]

1.2.2 Numeric Representation

Hexadecimal numbers are appended with "h" (Intel assembly-style notation) whenever there is a risk of ambiguity. Other numbers are assumed to be in decimal.

Several signals of identical function are sometimes described by a single expression in which that part of the signal name which differs is shown in parenthesis ( ). For example, the four Select signals - SEL#0, SEL#1, SEL#2, and SEL#3 - are represented by the single expression SEL#(0:3).

1.2.3 Acronyms

Standard acronyms used in the literature are presumed known and will not be explained or listed. For unfamiliar or relatively new acronyms, the reader can refer to the following table for a quick check. Less frequently used and ATI-specific acronyms in general will have the full definition alongside when appearing the first time in the document.

Table 1-1 Acronyms

Acronym	Full Expression
ACPI	Advanced Configuration and Power Interface
AGP	Accelerated Graphics Port
AMC	ATI Multimedia Channel
BGA	Ball Grid Array
CRC	Cyclic Redundancy Check
DSTN	Dual Super-Twisted Nematic - passive matrix
DVS	Digital Video System
EPROM	Erasable Programmable Read Only Memory
FIFO	First In, First Out
I^2C	Bus Protocol (Philips specification)
MDP	MPEG Data Port
MPP	Multimedia Peripheral Port
LCD	Liquid Crystal Display
LOD	Level of Details (refers to texture pixel selection)
LVDS	Low Voltage Differential Signalling
PEROM	Flash Programmable and Erasable Read Only Memory
PQFP	Plastic Quad Flat Pack
STN	Super-Twisted Nematic
TFT	Thin Film Transister - active matrix
UV	Chrominance (also CrCb) (corresponds to the color of an image pixel)
VBI	Vertical Blank Interval
VFC	VGA Feature Connector
VQ	Vector Quantization (refers to texture compression algorithm)

Table 1-1 Acronyms

Acronym	Full Expression
YUV	A method of video signal color encoding which includes luminance (Y, black and white component) and chrominance (UV, color component)
ZV	Zoom Video

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Chapter 2
Overview

2.1 Features Summary

The *3D RAGE LT PRO* is a highly integrated graphics accelerator with superior support for 3D and motion video, making it ideal for notebooks and LCD desktops. It is also the best choice for DVD notebooks and LCD desktops. DVD features include motion compensation, acceleration for soft DVD, integrated TV-out with Macrovision and support for 3rd party MPEG-2 decoders via the ATI Multimedia Channel (AMC).

The *3D RAGE LT PRO* delivers superior 3D acceleration and comprehensive 3D support including a triangle set-up engine, single-pass trilinear filtering, six perspectively correct texturing modes, video texturing, Gouraud and specular shading and a host of 3D special effects. It incorporates comprehensive support for Intel's Accelerated Graphics Port (AGP) including 1X or 2X mode with sidebands

The *3D RAGE LT PRO* supports Tri-View™ in that it can output to LCD, CRT and TV simultaneously. It also includes two output controllers so that any two display devices can have different images and/or refresh rates.

In summary, the *3D RAGE LT PRO* provides OEMs and system designers with the following advantages for high performance and product differentiation:

2.1.1 Unique Features

- First mobile accelerator to use AGP 2X (133 MHz) in AGP Texturing with sideband signals to realize all the benefits of AGP.
- First mobile accelerator to use Tri-View™ architecture for a triple display solution allowing three simultaneous outputs to TV, CRT and LCD with up to two different refresh rates.
- First mobile accelerator to deliver full motion soft DVD using motion compensation circuitry.
- First mobile accelerator with integrated LVDS transmitter.
- Innovative Dynamic Power Management with ACPI compliance.
- Superior 3D performance achieved through a hardware setup engine and a 4KB on-chip texture cache.
- Superior 2D performance with support of 100MHz SGRAM

- TFT and DSTN panel interface support for up to 1280x1024 resolutions.
- Integrated ImpacTV2-quality TV output provides optimal image quality via programmable 6 tap flicker filter, resolution modes scale down from 1024x768 and 16:9 wide mode support. Direct YUV422 mode, Macrovision 7.01 and CGMS support.
- Support for 2, 4, or 8MB frame buffers, and integrated 230MHz DAC.
- High quality ratiometric expansion that fits source images to any panel resolution.
- AGP and PCI versions of the chip available in 2 package options.

2.1.2 General Features

- High integration results in a low cost, small footprint graphics subsystem ideal for motherboard designs.
- PCI version 2.1 with full bus mastering and scatter/gather support.
- Bi-endian support for compliance on a variety of processor platforms.
- Fast response to host commands:
  - 128-level command FIFO
  - 32-bit wide memory-mapped registers
  - Programmable flat or paged memory model with linear frame buffer access
- First triple 8-bit palette DAC with gamma correction for true WYSIWYG color. Pixel rates up to 230 MHz.
- Second triple 8-bit DAC for simultaneous Composite and S-Video, **or** RGB outputs for TV/VCR.
- Supports DRAM, EDO DRAM, SDRAM and SGRAM at up to 100 MHz memory clock providing bandwidths up to 800MB/sec across a 64-bit interface.
- Flexible graphics memory configurations: 2MB up to 8MB EDO/SDRAM/SGRAM.
- Memory upgrade via industry standard SGRAM SO-DIMM, for reduced board area and higher memory speeds.
- DDC1 and DDC2B+ for plug and play monitors.
- Power management for full VESA DPMS and EPA Energy Star compliance.
- Integrated hardware diagnostic tests performed automatically upon initialization.
- High quality components through built-in SCAN, Iddq, CRC and chip diagnostics.
- Single chip solution in 0.35µm, 3.3V CMOS technology, with multiple package options.

- Comprehensive HDKs, SDKs and utilities augmented by full engineering support.
- Complete local language supports (contact ATI for current list).

2.2 Features Detail

This section gives a more detailed description of the features of the *3D RAGE LT PRO* Graphics Controller. Further details are provided in the chapters that follow.

2.2.1 Dual CRT Controller Support

Two independent CRT controllers support two asynchronous simultaneous display paths with the following features:

- dual independent displays (LCD/CRT, LCD/TV, CRT/TV)
- second triple-DAC for TV allows all three displays simultaneously with selectable display path source for each (e.g., CRT+TV/LCD, LCD+TV/CRT, LCD+CRT/TV)
- resolutions, refresh rates and display data can be completely independent.
- supports both independent displays at 1024x768, 24bpp, 75Hz (see mode tables for details)
- primary display path supports VGA and accelerated modes, video overlay, hardware cursor, hardware icon, and palette gamma correction.
- secondary display path supports accelerated modes and YUV422 video data. 24-bit palette is available. Hardware cursor, hardware icon (128x128), video overlay and VGA mode are not supported on the secondary display path.
- video genlocking supported for both CRTCs.
- secondary display path supports YUV422 direct for full-screen direct YUV-to-TV output (ideal for displaying full-screen DVD video on TV).

2.2.2 Integrated LVDS

- integrated dual 65 MHz LVDS interface with up to 10 LVDS channels for power and EMI reduction
- dual pixel SXGA resolution TFT panels and XGA resolution DSTN panels
- 24 bpp TFT (SGA/XGA) using dual pixel LVDS (versus 18 bpp using direct digital interface)
- 455 Mbps/channel with 65 MHz pixel clock rate

- DSTN - 120 Hz XGA (1024x768 60Hz) and 170 Hz SVGA (equivalent to 800x600 85Hz)
- 3 pairs (+1 clock) and 4 pairs (+1 clock) modes for both single and dual pixel LVDS
- FPDI-2 compliant; compatible with receivers from National Semiconductor, Texas Instruments, and THine
- LVDS eye pattern to improve testability of LVDS module

2.2.3 LCD Panel Control

- Flat Panel Power Management
  - Programmable internal timer for automatic power down of the panel.
  - Standby/Suspend pins for hardware Power Management support
  - Standby/Suspend registers for software Power Management support

- Power Up/Down Sequencer

  Power up/down sequencer built in to power up and power down the LCD panel in the correct sequence to avoid damaging of the panel. The delays in the power up/down sequence are programmable.

- Flat Panel support

  Universal panel interface that supports the followings:
  - Color STN/DSTN/CSTN LCD panels up to XGA (1024x768) resolution, up to 160 Hz refresh rate, up to 256k colors on an 8-color panel.
  - Color TFT panel up to 1600x1280 resolution, up to 24-bit per pixel, single/double pixel per clock.
  - 2/4 levels of frame modulation can be done on 9-bit, 12-bit and 18-bit TFT panels.
  - Hardware Z-buffer support with both DSTN and TFT panels.

- Integrated LVDS interface support
- Support for Panel Link Interface

  Support external Panel Link transmitter.

- Panel ID to allow multiple panel support without swapping BIOS

  Five bits allocated for panel ID

- DDC support for LCD monitors

  General purpose I/O pins available to support DDC on LCD monitor applications.

- Ratiometric Expansion in both VGA Graphics Modes and Accelerated Graphics Modes

  Display modes with resolutions lower than the LCD panel resolution can be ratiometrically expanded to fill the whole screen.

  Two tap horizontal and *vertical* filtering to improve both text and graphics image quality.

  Maximum source resolution support with vertical filtering:

  - horizontal: 896 24bpp
  - vertical: no limit

    There is NO limit on source resolution if the vertical filtering is disabled.

- Variable Blink Rate Support

  Different panels have different response time. Variable blink rate support allows the blinking character/cursor to be seen clearly.

- Backlight and Contrast Modulation
  - Pulse Width Modulation for backlight on/off signal to control the brightness of the display.
  - Pulse Width Modulation for bias voltage on/off signal to control the contrast of DSTN panel.

2.2.4 ACPI Power Management

- Advanced Configuration and Power Interface (ACPI) with On, Standby, Suspend and Off
- Mobile AGP 1.0 and mobile PCI 1.0 support
- Pin, Register and Timer modes for hardware and software power management
- Dynamic clock switching
- Panel bias voltage and digital power control
- Self-refresh and F32KHz refresh for Suspend mode

2.2.5 TV-Out

An integrated TV encoder with on-chip triple-DAC allows simultaneous CRT/LCD/TV

output with these outstanding TV-out characteristics:

- **ImpacTV2 proven design** producing scaled, flicker removed, artifact suppressed display on a PAL or NTSC TV with Composite and S-Video, or RGB outputs.
- **Support for Macrovision 7.01 copy protection standard (required by DVD players)** — a fully programmable timing capability, it will accommodate potential changes in the Macrovision algorithm without any hardware changes.
- **YUV Direct/Passthrough mode for video/Mpeg playback and DVD** provides the best quality for movie playback and will allow titles to be displayed on TV with their original high quality and without insertion of any artifact from the TV-out circuit.
- **Secondary Display support** for RGB modes as well as full screen YUV mode specially for video playback and DVD (while potentially displaying scaled video on the CRT).
- **1024x768 24bpp support —** improved from ImpactTV2 to support up to 1024x768 mode. Modes supported include the 800x600 and 16:9 type display modes like 848x480 with user flexibility for moving and sizing the screen.
- **Line 21 Closed Caption and Extended Data Service support** for encoding in Vertical Blanking Interval (VBI) of TV signal.
- **CGMS-A DVD copy management support in VBI** through Line-20 and/or Extended Data Service (Line-21 Field 2).
- **UV filtering** for a higher quality picture and reduced flicker. As in ImpactTV2, a high quality UV filter based on colour averaging is used to help diminish the composite dot crawl effect and also, by being adjustable, help trade off between sharpness and flicker.
- **TV-out power management support**.
- **Proven Y flicker filter with programmable (2, 3, 4, 5, 6) taps** produces high quality output with considerably more stable and crisper pictures.
- **Eliminates "Composite Dot Crawl"** problem for both NTSC and PAL. Composite dot crawl freeze option for PAL and NTSC is actually exclusive to ATI and so far we have not seen any other product that supports this feature.
- **Special sharpness filter and black and white mode to improve text quality.** As in ImpacTV2, we provide more flexibility for TV's that might only have a composite input by adding higher quality sharpness controls. We are also providing a black and white mode which will eliminate any false colour which impacts the quality of the text being displayed. Some of the popular web TV devices are actually doing the same thing on part of their user interfaces that contain a high concentration of text.
- **Brightness and Colour Saturation Control**.
- **Independent Vertical Positioning** of both the TV and CRT images.

- **Independent Horizontal Positioning** of both the TV and CRT images.
- **Independent Horizontal Scaling** of both the TV and CRT images.
- **Vertical Scaling** of the TV and CRT images together.
- **Fully Programmable TV Timing** (facilitates setting a variety of display modes).
- **Programmable filter settings** allow the users to tune the display to their requirements.
- **No overscan limitations** of external ImpactTV2. Overscan can optionally be displayed on the TV.
- **Varied output formats**:
  - NTSC.
  - PAL B, D, G, H, I (PAL B,D,G,H,I are the same for TV-OUT), M (Brazil), N (Uruguay, Paraguay), CN (Argentina).
  - Composite Video (available on the majority of TV's).
  - S-Video (available on Mid to High End TV's, less colour artifacts, better resolution).
  - SCART-RGB connector (direct RGB into the TV - high quality resolution).
  - Output signal is generated at 50+ MSamples/sec to virtually eliminate the need for external analogue filtering.
  - Signal is digitally filtered to insure that it does not exceed bandwidth specifications of TV standards. This insures that it can be recorded, can be broadcast, and will comply with FCC regulations when input into poorly shielded TV sets.
  - Can detect wether TV/VCR is connected or not (Power-down/Power-up over-ride via software).

2.2.6 AGP 1X/2X Mode

Both AGP 1X and AGP 2X are fully supported in the *3D RAGE LT PRO*. The DVD-enabled *3D RAGE LT PRO AGP 2X*, with three times the 3D performance of the previous generation chip, is the first demonstrated AGP accelerator to support the AGP 2X (133MHz) mode. The AGP 2X mode offers a peak bandwidth in excess of 500 MB/s, which is twice the throughput of the AGP 1X (66MHz) mode. In comparison, the PCI graphics devices are limited to a peak bandwidth of 132 MB/s which they must share among themselves. The *3D RAGE LT PRO* also supports AGP's pipelined sideband protocol. This significantly improves the sustained bandwidth leading to an enhanced 3D and video performance.

2.2.7 Floating-Point Set-up Engine

The *3D RAGE LT PRO* integrates a floating-point set-up engine capable of processing up to 1.2 million triangles per second. By off-loading the set-up function from the CPU, allowing it to focus on 3D geometry and lighting transformations, the *3D RAGE LT PRO* dramatically improves the performance of the entire 3D pipeline.

Compared with competing first generation set-up engines which only accept fixed-point parameters, requiring the CPU to perform float-to-fixed conversions that can take up to 100 CPU clocks, ATI's floating point architecture opens the door to the highest level of 3D performance.

2.2.8 100 MHz SGRAM

Frame buffer bandwidth is another important factor to 3D and 2D graphics performance. *3D RAGE LT PRO*'s 64-bit, 100MHz SGRAM interface delivers 800 MB/s of low-latency frame buffer bandwidth, which is the highest bandwidth achieved by any mainstream graphics controller.

It is the ideal complement to the high bandwidth AGP 2X mode interface. By contrast, single-channel, non-concurrent RAMBUS designs used by others are limited to 600 MB/s of high-latency bandwidth.

ATI can provide design assistance, including IBIS models, to allow OEMs to design 100MHz memory upgrades on motherboards using the new industry standard SGRAM SO-DIMMs.

2.2.9 Zoom Video (ZV) Port

- ZV Port (PCMCIA compliant with CCIR601 timing)
- allows transfer of video data directly into frame buffer without loading down PCI bus
- dedicated video port guarantees video frame rates (30 frames per second)
- maximum 40 MHz, 16bpp YUV422 (PCMCIA specs 16 MHz maximum)

2.2.10 DVD and Video Support

DVD and video features include enhanced motion compensation acceleration and a 4-tap horizontal and 2-tap vertical high quality DVD video scaler, providing smooth images without the "jaggies" (jagged edges) common to today's video products. The scaler provides true color video display, independent of the graphics mode used.

3D RAGE LT PRO also features a de-interlacing filter, video on graphics overlay, multi-stream video, color-space conversion, scatter-gather bus-master, planar YUV mode, ATI Multimedia Channel (AMC) video input port, Zoom Video input port (ZV-port), and support for high quality NTSC and PAL TV-out with an integrated TV-out encoder.

By off-loading the motion compensation step from an MMX processor, the *3D RAGE LT PRO* improves software DVD/MPEG-2 frame rate by 20 to 30%. The *3D RAGE LT PRO* provides full motion MPEG-2 playback on Pentium II processors, without the need for DVD hardware.

2.2.11 2D Acceleration

- Hardware acceleration of Bitblt, Line Draw, Polygon / Rectangle Fill, Bit Masking, Monochrome Expansion, Panning/Scrolling, Scissoring, full ROP support and h/w cursor (up to 64x64x2).
- Game acceleration (including support for Microsoft's DirectDraw): Double Buffering, Virtual Sprites, Transparent Blit, Masked Blit and Context Chaining.
- Acceleration in 8/16/24/32 bpp modes. Packed pixel support (24bpp) enables true color in 1MB configurations.

2.2.12 3D Acceleration

- Integrated 1 million triangle/s set-up engine reduces CPU and bus bandwidth requirements and dramatically improves performance of small 3D primitives
- 4K on-chip texture cache dramatically improves large triangle performance.
- Complete 3D primitive support: points, lines, triangles, lists, strips and quadrilaterals and BLTs with Z compare.
- Comprehensive enhanced 3D feature set:
    - Full screen or window double buffering for smooth animation
    - Hidden surface removal using 16-bit Z-buffering
    - Edge anti-aliasing
    - Sub-pixel and sub-texel accuracy
    - Gouraud and specular shaded polygons
    - Perspectively correct mip-mapped texturing with chroma-key support
    - Support for single pass bi- and tri-linear texture filtering, vastly improving bi- and trilinear performance

- Full support of Direct3D texture lighting
- Texture compositing
- Special effects such as complete alpha blending, fog, video textures, texture lighting, reflections, shadows, spotlights, LOD biasing and texture morphing
- Dithering support in 16bpp for near 24bpp quality in less memory
- Texture compression of up to 8:1 using vector quantization

- Extensive 3D mode support:
  - Draw in RGBA32, RGBA16, and RGB16
  - Texture map modes: RGBA32, RGBA16, RGB16, RGB8, ARGB4444, YUV444
  - Compressed texture modes: YUV422, CLUT4 (CI4), CLUT8 (CI8), VQ

2.2.13 Motion Video Acceleration

- Smooth video scaling and enhanced YUV to RGB color space conversion for full-screen / full-speed video playback.
- Front and back end scalers support multi-stream video for video conferencing and other applications.
- Filtered horizontal/vertical, up/down, scaling enhances playback quality.
- Enhanced line buffer allows vertical filtering of native MPEG-2 size (720x480) images.
- DVD / MPEG-2 decode assist provides dramatically improved frame rate without incurring cost of dedicated hardware.
- Special filter circuitry eliminates video artifacts caused by displaying interlaced video on non-interlaced displays.
- Bi-directional bus mastering engine with planar YUV to packed format converter for superior MPEG-2 and video conferencing.
- Hardware mirroring for flipping video images in video conferencing systems.
- Supports graphics and video keying for effective overlay of video and graphics.
- YUV to RGB color space converter with support for both packed and planar YUV:
  - YUV422, YUV410, YUV420
  - RGB32, RGB16/15, RGB8, Mono

2.2.14 AMC Operation

- 16-bit, bi-directional video port allows direct connection to popular video upgrades such as:
  - Video capture / video conferencing
  - Hardware MPEG-2 / DVD player
  - TV Tuner with Intercast support
  - Interface to ATI's ImpacTV chip

For more information, refer to "*AMC Developers Guide*"

2.3 Chip Packaging Options

The *3D RAGE LT PRO* is available in five AGP and PCI variants (packaging options) with different levels of AGP support, giving manufacturers maximum flexibility to differentiate products and upgrade existing designs. The table below indicates the several configurations in which the *3D RAGE LT PRO* is available:

Table 2-1 3D RAGE LT PRO packaging and identification codes

Chip ID	MV	Description
LB	0	312 BGA package, AGP: both 1X and 2X; without Macrovision
	1	312 BGA package, AGP: both 1X and 2X; with Macrovision
LD	0	312 BGA package, AGP: 1X support only; without Macrovision
	1	312 BGA package, AGP: 1X support only; with Macrovision
LI	0	312 BGA package, PCI 33MHz only; without Macrovision
	1	312 BGA package, PCI 33MHz only; with Macrovision
LP	0	256 BGA package, PCI 33MHz; without Macrovision
	1	256 BGA package, PCI 33MHz; with Macrovision
LQ	0	256 BGA package, PCI 33MHz; without Macrovision
	1	256 BGA package, PCI 33MHz; with Macrovision

3D RAGE LT PRO AGP 2X

- Incorporates AGP 2X mode (133MHz) and 230MHz DAC support
- Triple 8-bit palette DAC supporting pixel rates up to 230MHz
- Available in 312-pin BGA for optimal electrical characteristics in the demanding AGP environment.

3D RAGE LT PRO AGP 1X

- Incorporates AGP 1X (66MHz) with pipelined sideband address support.
- Triple 8-bit palette DAC supporting pixel rates up to 200MHz
- Available in 312-pin BGA package. This is a pin-compatible alternative to *3D RAGE LT PRO AGP 2X* for cost-sensitive implementations.

3D RAGE LT PRO PCI

- Incorporates 33MHz PCI revision 2.1 support.
- Available in 312 and 256 pin packages with the following differences:
  - 256 BGA package does not support AGP
  - 256 BGA supports up to 24 bpp, single pixel per clock digital interface; 312 BGA supports up to 24 bpp single pixel per clock and up to 18 bpp double pixel per clock. There is no restriction in LVDS interface, both packages support up to 24 bpp single or dual LVDS channel.
- 256-pin BGA package is pin-compatible with *3D RAGE LT,* **except**:
  - The 36-bit digital LCD interface is no longer supported
  - XGA or SXGA panels with dual pixel interface are supported by the on-chip LVDS interface only.
  - Digital LCD interface support is now limited to 24-bit data. The 12 digital LCD pins, previously removed, are now used for TV encoder pins and other functions;
  - The reset straps are moved from LCD data pins to memory data lines.
- An ideal upgrade to extend the life of existing motherboards, and the most economical solution for non-AGP systems, the PCI version incorporates the same performance enhancements and new features found in the AGP versions.

2.4 Differences between AGP and PCI Variants

2.4.1 Feature Differences

- Motion Compensation in software DVD is supported only in AGP versions.
- AGP 3D texture is supported only in AGP versions.

2.4.2 Performance Differences

The two tables below shows 3D WinBench98 and Reality Large 3D Textures testing results.

Table 2-2 WinBench98 Performance Test

Clock	LT PRO AGP	LT PRO PCI
100/75	501	501
80/80	495	481

Table 2-3 Reality Large 3D Textures Test

Textures size, MB	LT PRO AGP	LT PRO PCI
2.3	39.49	39.59
4.0	38.95	39.14
6.3	38.87	15.2
9.0	36.17	2.56
12.3	33.69	1.02
16.0	30.19	0.79
20.3	29.07	0.63
25.0	27.66	0.51
30.3	23.18	0.43
36.0	25.52	0.36

2.5 Software Support

Table 2-4 Workstation Class / Arcade Level 3D Accelerator

Software Support	DOS	Win 3.x	Win 95	Win NT	Mac OS	OS/2
2D Software Support [1]						
Accelerated driver support	VESA[2]	*	*	*	*	*
AutoCAD / MicroStation						
Video Software Support						
Microsoft DirectDraw			*			
Microsoft ActiveMovie			*			
MPEG-1 software playback	*	*	*			
MPEG-2 software playback			*			
3D Software Support						
Microsoft Direct3D			*			
QuickDraw 3D RAVE			*	*	*	
OpenGL[3]			*	*		

Table 2-4 Workstation Class / Arcade Level 3D Accelerator (Continued)

Software Support	DOS	Win 3.x	Win 95	Win NT	Mac OS	OS/2
Heidi				*		
ATI 3D CIF[4]			*			

1 - Additional 3rd parties (including SCO Unix and UNIXWARE);
2 - Direct BIOS support;
3 - Includes NT 3.51ICD and NT4.0 MCD;
4 - ATI's 3D API for the 3D RAGE family

Chapter 3
Functional Description

The *3D RAGE LT PRO* controller comprises several major subsystems and interfaces as shown in the figure below. This chapter describes them briefly from a functional point of view.

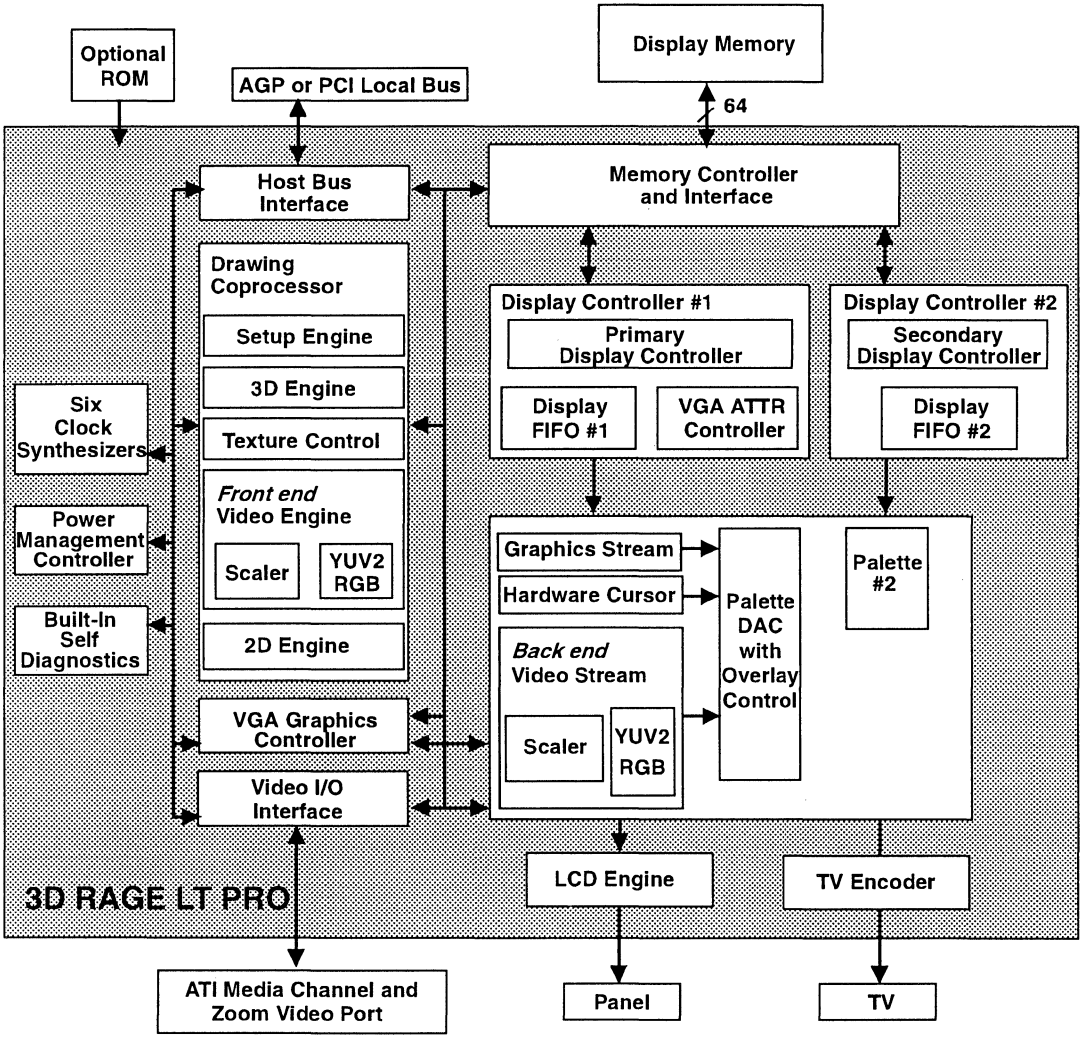

Figure 3-1. 3D RAGE LT PRO Functional Block Diagram

The following diagram shows the primary and secondary display paths, the triple-DAC interfaces, and the LCD interface.

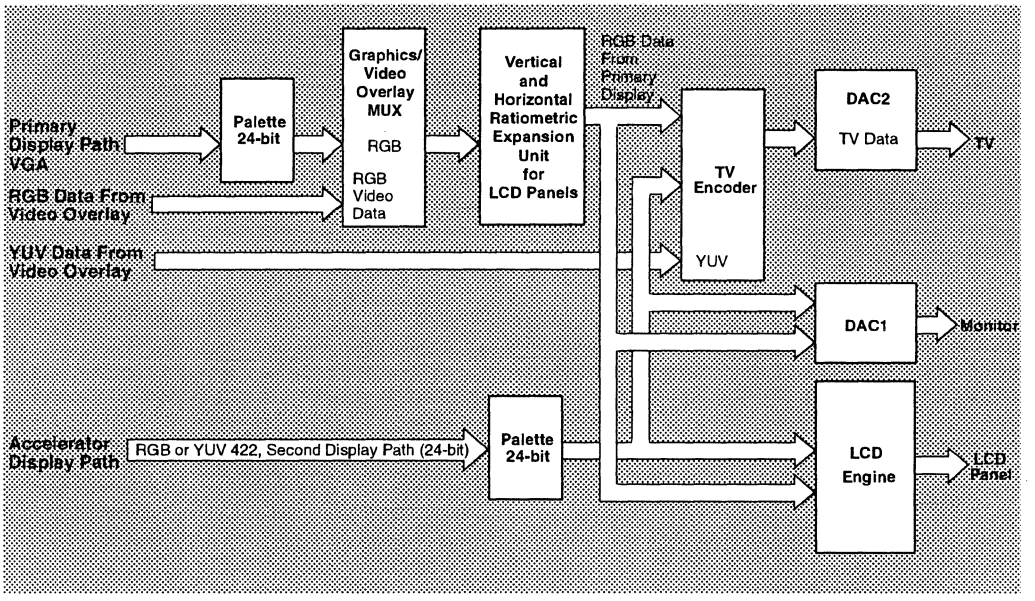

Figure 3-2. 3D RAGE LT PRO Display Pipelines

3.1 3D Graphics Coprocessor

The 3D graphics coprocessor offers a number of orthogonal pixel processing features associated with the rendering of 3D images. These coprocessor functions were chosen to accelerate features of both Microsoft's D3D and Apple's QuickDraw 3D RAVE interfaces. Drivers will be available for all major operating systems and APIs (see *Section 2.5*).

The *3D RAGE LT PRO* graphics processor includes a triangle setup engine, which needs only color, alpha, Z, U and V information at vertices of triangles to successfully draw Gouraud shaded, or perspectively correct texture mapped triangles. The setup engine significantly reduces the CPUs load in 3D graphics applications, giving applications more CPU time to perform non-setup related tasks.

Pixels to be displayed can be further modified by alpha blending with pixels in the destination, by fogging pixels with a fog color, and in the case of texture mapping, by lighting them. Depth buffering is achieved by associating a 16-bit Z value with each pixel. The Z, Alpha, and fog color for each new pixel is supplied from interpolators within the 3D coprocessor. In case of texture mapping, the Alpha factor may even be stored in the texture map on a pixel-by-pixel basis.

Pixels in the 3D coprocessor are always operated on as 24-bit entities (8 bits each of Red, Green, and Blue). Other pixel sizes, i.e., 8-bit and 16-bit, are dithered by the 3D graphics subsystem to output at the desired pixel size.

The 3D coprocessor contains a powerful texture mapping engine. This engine takes a series of precomputed maps (mip maps) and selects texels from these maps in a way that allows them to look perspectively correct. Texels can be filtered in a number of ways, and then lit (lightened or darkened). Once the texel is formed by filtering and lighting, any of the pixel processing modes mentioned previously can be applied to the texel.

A newly added 4K texture cache greatly reduces the memory bandwidth needed to support texture mapping.

With AGP support, texture maps can be stored in system memory and pulled into the local texture cache as needed. This rids the system of the need to add significant amount of local frame buffer memory in order to support multiple detailed texture maps, and allows applications to support a richer and more realistic environment.

3.2 2D Engine

This is a fixed-function subunit that runs concurrently to the host processor. It is dedicated to draw operations which include rectangle fill, line draw, polygon boundary lines, and polygon fill. A sophisticated pixel data path allows monochrome-to-two-color expansion, solid color fill, screen-to-screen bitblts, fixed pattern fill, general pattern fill, general patterns with rotation, and host-to-screen data transfers. Flexible bitblt trajectories allow hyper-efficient off-screen memory management, effectively increasing bitmap and font cache sizes and improving performance.

Other features include GUI engine quick setup which off-loads draw engine setup from the host CPU. A 16-function ALU and a four-function source/destination color comparator allow source and destination to be combined in a multitude of ways, useful for operations such as image overlaying or transparent blits. Bit masking and scissoring can protect memory regions from being written.

All internal draw engine data paths are 64-bit wide. Full drawing features are available in 8, 15, 16, 24, and 32 bits-per-pixel (bpp) modes.

All draw engine registers are 32-bit wide. A 128x32 command FIFO improves throughput over the expansion bus. An additional 64 entries are dedicated to busmastering16x64 source and destination FIFOs improving memory bandwidth throughput.

3.3 Video Coprocessor

The video coprocessor has an optimized data path designed for scaling, filtering, and color space conversion. Dual 768-pixel line buffer has been integrated into this block to provide superior vertical scaling and interpolation. Graphics and video keying capabilities and a window controller allow for overlaying of the graphics and video data streams. This enables simultaneous display of 24bpp video and 8/16/24/32bpp graphics.

3.4 Host Bus Interface

The Host Bus Interface supports both AGP and PCI 2.1 standards. Mobile PCI rev 1.0 and Mobile AGP are supported by the 256 BGA and 312 BGA packages respectively.

Support for AGP includes both sideband and mixed address modes. Texture map data for 3D objects can be obtained directly from system memory. Similarly the AGP can be used to accumulate MPEG-2 playback.

With PCI 2.1, functions such as bus control, data flow control, address/data signal generation, signal timings, and address decoding are supported. Data flow control is enhanced by a 6x64-bit write-through FIFO available in both VGA and direct memory modes.

Bus mastering functions between (1) system memory and frame buffer, (2) system memory and MPP, and (3) system memory and GUI engine, allow all data transfer operations to be off-loaded from the host processor onto the motherboard chip set.

3.5 Memory Controller and Interface

The memory controller subsystem arbitrates requests from the direct memory interface, the VGA graphics controller, the drawing coprocessor, the display controller, the video scaler, and the hardware cursor. Requests are serviced in a manner that ensures display integrity and maximum CPU/coprocessor drawing performance.

A dedicated DRAM frame buffer can be 2MB or 4MB in size using Fast Page or EDO DRAM. A dedicated synchronous DRAM frame buffer can be 2MB, 4MB, or 8MB in size using SDRAM or SGRAM.

Table 3-1 Memory Controller

Memory Type	2MB	4MB	8MB
DRAM, EDO DRAM	-	-	-
	256Kx8	-	-
	256Kx16	256Kx16	-
SDRAM, SGRAM	128Kx16x2	128Kx16x2	-
	128Kx32x2	128Kx32x2	-
	256Kx32x2	256Kx32x2	256Kx32x2

3.6 Extended VGA Graphics Controller

The VGA portion of the graphics controller is fully register compatible with the VGA standard and is BIOS-compatible with VESA super VGA drivers.

3.7 CRT Controller (CRTC)

The CRTC subsystem has additional enhancements such as support for overscan, video memory sizes up to 8MB, and screen resolutions up to 1600x1200 non-interlaced.

3.8 Display Controller #1 (Primary)

The primary display controller subsystem consists of four subunits as follows:

- Display FIFO #1 to manage the memory interface for displayed pixel data.
- Enhanced attribute controller for VGA.
- The primary display controller.

This display controller subsystem supports VGA graphics modes up to 1600x1200 (85Hz), VGA text modes up to 132-column on a PS/2 monitor, and accelerator display modes up to 1600x1200 (85Hz).

3.9 Hardware Cursor/Icon (Primary)

The hardware cursor/icon logic supports a 64x64x2 and 128x128x2 memory-mapped cursor/icon that is also XGA function compatible. The hardware cursor/icon may be used in any display mode supported by this controller. Transparent, complement, and two solid

colors are available.

Note: Hardware cursor/icon is only supported on the primary display.

3.10 Display Controller #2 (Secondary)

The secondary display controller subsystem consists of three subunits as follows:

- Display FIFO #2 to manage the memory interface for displayed pixel data.
- The secondary display controller.
- 24-bit secondary palette.

The secondary display controller supports accelerator display modes up to 1600x1200 with 8, 16, 24 and 32 bpp color depths. It also supports a YUV422 full screen direct YUV mode for TV Output. In this mode, the display controller reads YUV422 from video memory and unpacks to 24-bit YUV pixels for use directly by the TV encoder.

3.11 Palette DAC

The internal palette DAC subsystem consists of a triple 256x8 SRAM palette and a triple 8-bit DAC. It supports the following features:

- Pixel clock rates up to 230MHz for resolutions up to 1600x1200.
- Refresh rates up to 200Hz.
- Built-in DAC reference generation.
- Monitor detection.
- Direct 24-bit color.
- Separate or composite horizontal and vertical Sync signals.
- Optimized slew rate control for the RGB analog output for low EMI emission.

Note: the Palette DAC is used by the display controller which is actively selected for the CRT.

3.12 LCD Engine

The LCD engine processes the RGB (digital) signals from the palette DAC, then sends the output to the LCD panel for display. This block features frame modulation and dithering, on both TFT and STN panels, to generate grey levels. A half frame buffer serves as an interface to the memory controller, and is used mainly for supporting dual scan STN

panels. Besides digital interface to the panel, LVDS interface is also available with built-in transmitter.

3.13 Ratiometric Expansion

The Ratiometric Expansion logic controls the process that scales up the active display area of the current graphics mode by filtering pixels (2-tap filter in the horizontal direction) and lines (2-tap filter in the vertical direction). Whenever the resolution of the current graphics mode is smaller than that of the LCD panel, this block is used to generate the frame that fills the entire LCD panel. Ratiometric expansion uses two algorithms to support the graphics and text modes.

3.14 Chip Power Management

The 3D RAGE LT PRO's sub-micron CMOS integrated circuit is optimized for low power consumption during normal operation. The 3D RAGE LT PRO provides mixed 3.3V and 5V operation through dedicated power pins for internal (core) logic, host bus, memory and display interface. The internal logic always operates at 3.3V to minimize power consumption. A flexible clock synthesizer is used to generate independent memory, 2D/3D and video clocks.

The Advanced Chip Power Management logic supports four device power states — On, Standby, Suspend and Off — defined for the OnNow Architecture. Each power state can be achieved by software control bits, hardware pins or hardware timers. By implementing Power Management Capability registers in PCI configuration space, the chip becomes directly controllable from the system BIOS. Three dedicated pins (CLKRUN#, AGP_BUSY# and STP_AGP#) give the full controllability of the PCI and AGP bus interface to the system chipset.

Clocks to every major functional block (2D, 3D, video, LCD out, TV out, primary display pipe, secondary display pipe) are controlled by a unique dynamic clock switching technique which is completely transparent to the software. By turning off the clock to the block that is idle or not used at that point, the power consumption is significantly reduced during normal operation. If the clock is needed, it can be restored within one clock without affecting overall performance of the chip. For more information, please refer to the Power Management Application Notes.

3.15 Six-Clock Synthesizer

The internal clock synthesizer consists of six independent phase locked loops (PLL) capable of synthesizing any frequency up to 230MHz. All PLLs have been optimized for

low jitter graphics and TV applications.

- The first PLL generates clocks for the CRTC, display controller, and palette DAC. This PLL can be reprogrammed by the BIOS for each display mode.
- The second PLL generates the clock for the drawing coprocessor.
- The third PLL is used to generate the 66 MHz and 133 MHz internal clock synchronous AGP bus operations.
- The fourth PLL generates the clock for the memory controller.
- The fifth PLL generates the clock for the secondary CRTC display controller and palette.
- The sixth PLL generates the clock for the internal TV encoder.

3.16 ATI Multimedia Channel (AMC)

The AMC represents a collection of hardware and software components designed to facilitate the use of ATI products for multimedia applications. It consists of a non-chip audio bus, and three ports into the graphics controller - the DVS port for video input into the graphics controller, the MPP port for video input and output from the graphics controller, and the I^2C port for controlling attached devices.

The Multimedia Peripheral Port (MPP) Mode supported by AMC allows interface with external I/O devices. For example, compressed data can be transferred by means of MPP from the host (CPU) to the MPEG-2 decoder for DVD applications.

The Digital Video Stream (DVS) port accepts industry standard video formats, and allows easy attachment of video decoders and hardware MPEG-2 decoders. The DVS port provides for decoded video data to stream back to the graphics controller.

The I^2C is an industry standard serial bus that allows control and programming of a wide range of peripherals. The *3D RAGE LT PRO* incorporates an I^2C interface to allow programming of peripherals such as video decoders, TV tuners, teletext decoders, and volume control.

3.17 TV Encoder

The TV Output is an integrated and enhanced version of the proven ImpacTV2 high quality NTSC/PAL encoder. This includes 24 bits-per-pixel RGB for graphics and direct YUV for video data. RGB is converted to YUV and a vertical scaler performs programmable Y and UV filtering. Programmable timing generation and modulator produces the TV signal with possible composite and S-Video, or RGB outputs using a triple 8-bit DAC output.

Direct YUV modes for TV include scaled or full screen video using the primary display without ratiometric expansion and full screen YUV422 video on the secondary display. The direct YUV video modes on the primary display include all the YUV modes supported by the video scaler. With ratiometric expansion and TV output enabled on the primary display, both graphics and video data will be in RGB format when passed to the TV encoder. Both primary and secondary display also support TV output using RGB graphics only.

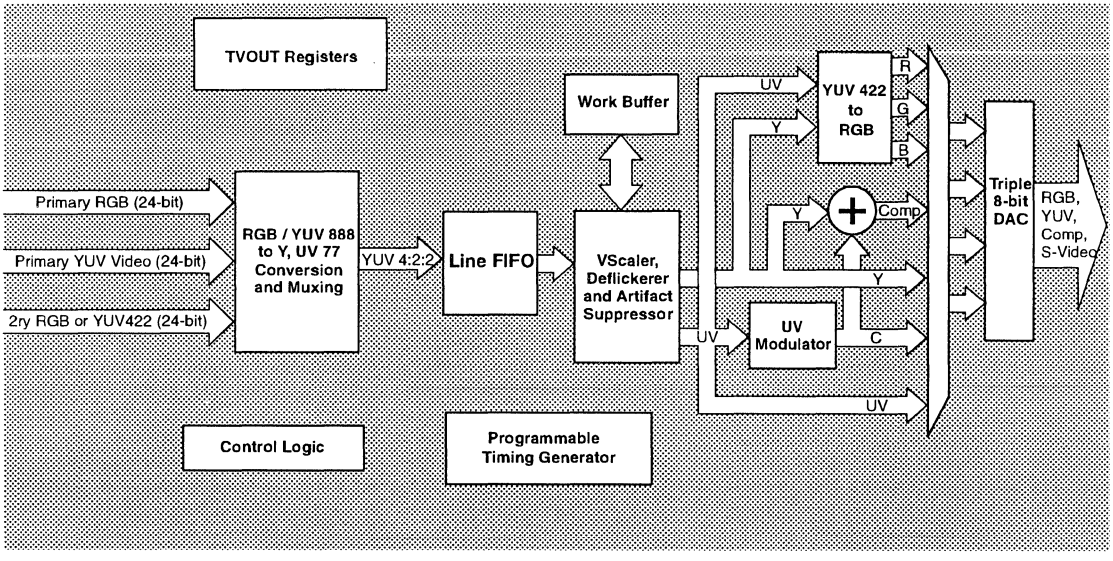

Figure 3-3. TV Out/Encoder

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Chapter 4
Interfaces

The block diagram below depicts the major interfaces required in a typical design based on the *3D RAGE LT PRO*. These interface blocks are further described in later sections of this chapter. Please note that the interface diagrams are generic. You are invited to refer to the reference schematics for this chip for the latest information.

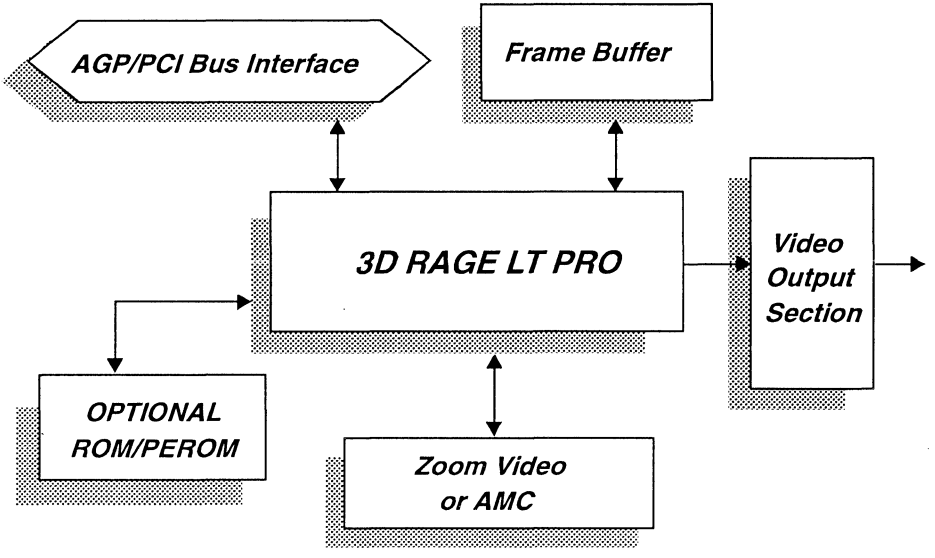


Figure 4-1. Controller Interface

4.1 AGP/PCI Bus Interface

The *3D RAGE LT PRO* controller supports the Accelerated Graphics Port (both AGP 66MHz and 133MHz). Addressing modes include sideband address support. This AGP enabled controller can access large texture maps, stored in system memory, directly. Applications that make use of large numbers of 3D objects can reduce the amount of memory required in the frame buffer.

Together with PCI Version 2.1, the *3D RAGE LT PRO* controller acts as a target device,

supporting 32-bit memory and I/O operations and byte lane swapping. With full 32-bit address decoding available in PCI, it can map the Direct Memory Interface to 4GB of memory space on a 16MB boundary.

The controller achieves zero wait-state memory read/write burst cycles with burst access. It also supports Block I/O decoding and DAC palette snooping.

Bus mastering allows data transfer operations without CPU intervention. In bus master mode, the controller will take control of the PCI bus by driving the address and control signals.

By supporting Mobile AGP and Mobile PCI Version 1.0, the *3D RAGE LT PRO* controller gives the full Power Management controllability to the system where the controller is integrated.

AGP Bus Configuration is shown in *Figure 4-2*.

PCI Bus Configuration is shown in *Figure 4-3*.

4.1.1 AGP Bus Interface

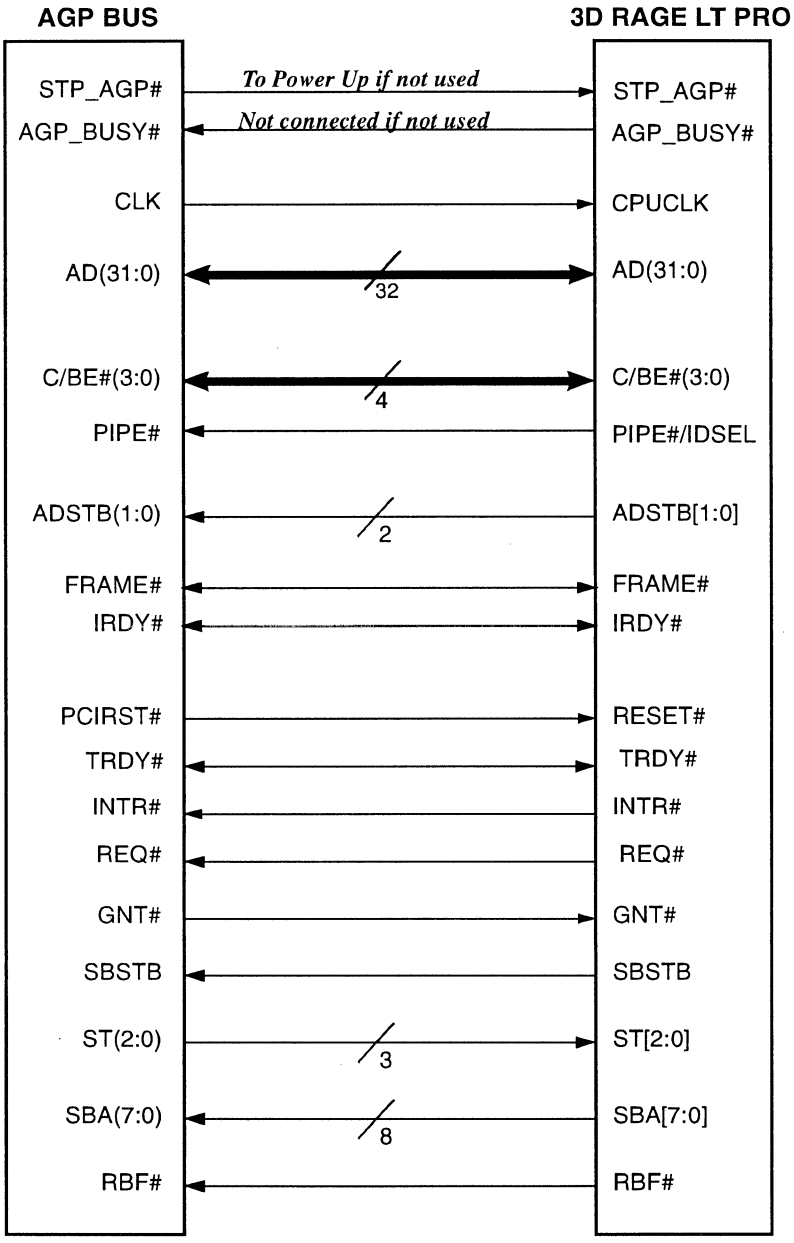


Figure 4-2. AGP Bus Configuration

4.1.2 PCI Bus Interface

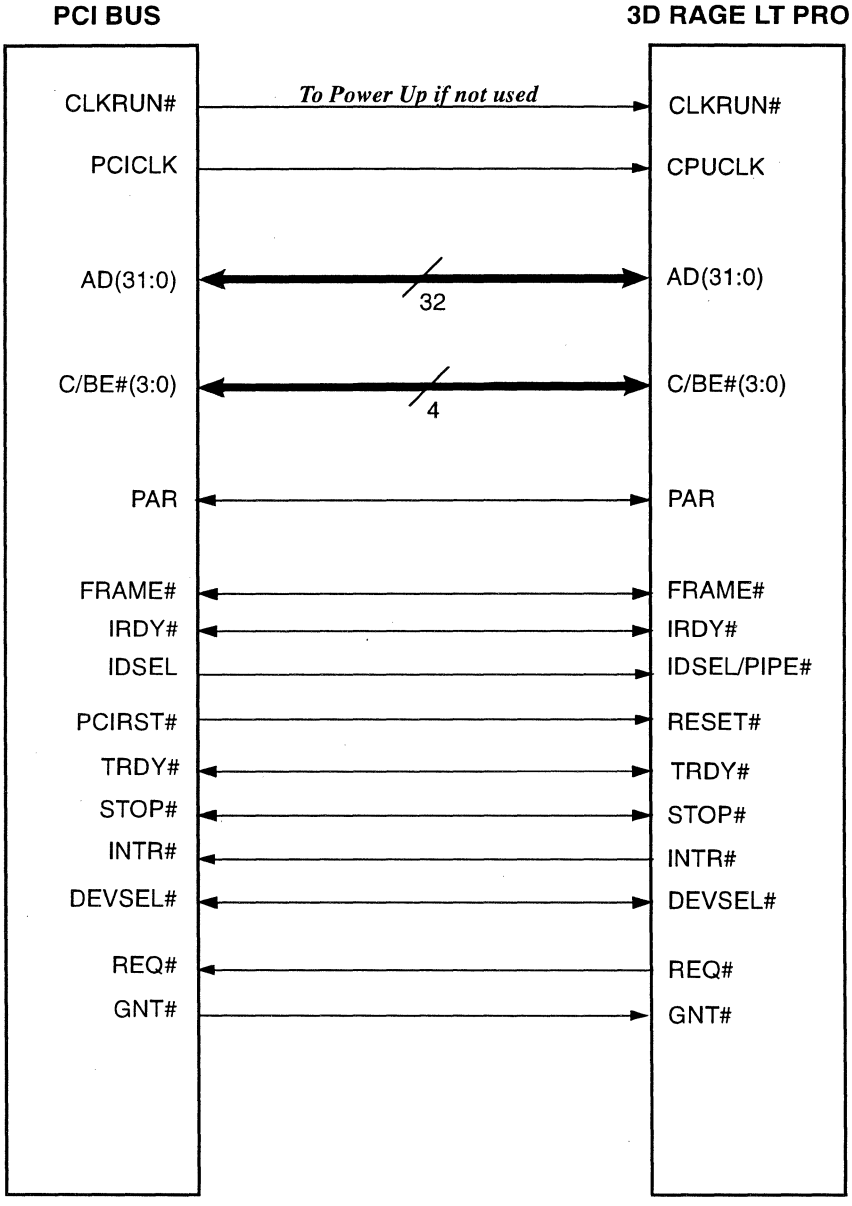


Figure 4-3. PCI Bus Configuration

4.2 Memory Interfaces

The memory interface of this controller supports the following memory devices:

SDRAM and **SGRAM** — 128x16x2, 128x32x2, 256x32x2 and 512x32x2.

DRAM and **EDO DRAM** — 256x4, 256x8, and 256x16.

Memory configurations range from 2MB to 8MB (see table below). This interface supports only a full 64-bit memory path.

This interface supports mixing of memory component sizes — 256x4, 256x8, and 256x16 — within one design. However it does not support mixing of memory types, e.g., the mixing of DRAM and EDO DRAM.

The table below lists the supported memory configurations, and the number of memory parts required:

Memory Size	256x8 (2Mb)	256x16/ 128x16x2 (4Mb)	128x32x2 (8Mb)	256x32x2
2MB	8	4	2	Not supported
4MB	Not recommended	8	4	2
6MB	-	Not recommended	6	-
8MB	-	Not recommended	8	4

Supported memory interface types include "Dual CAS" DRAM, EDO DRAM, SDRAM, and SGRAM devices.

Figure 4-4 shows a 256x16 Dual CAS memory implementation.

An SDRAM memory implementation example using 128x16x2 SDRAM devices is shown in *Figure 4-5*.

An SGRAM memory implementation example using 128x32x2 SGRAM devices is shown in *Figure 4-6*.

An SGRAM example with 256x32x2 is implemented on *Figure 4-7* SGRAM example using 512x32x2 SGRAM devices is shown in *Figure 4-8*.

Figure 4-9 shows an example of SO-DIMM Module Interface implementation.

4.2.1 DRAM Interface

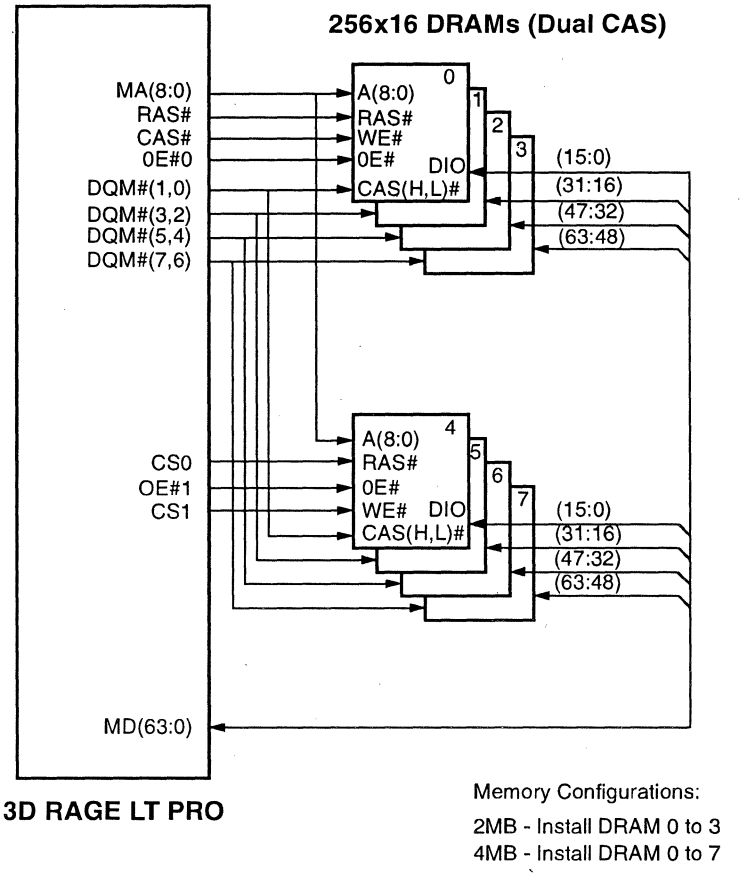


Figure 4-4. DRAM Implementation

4.2.2 SDRAM Interface

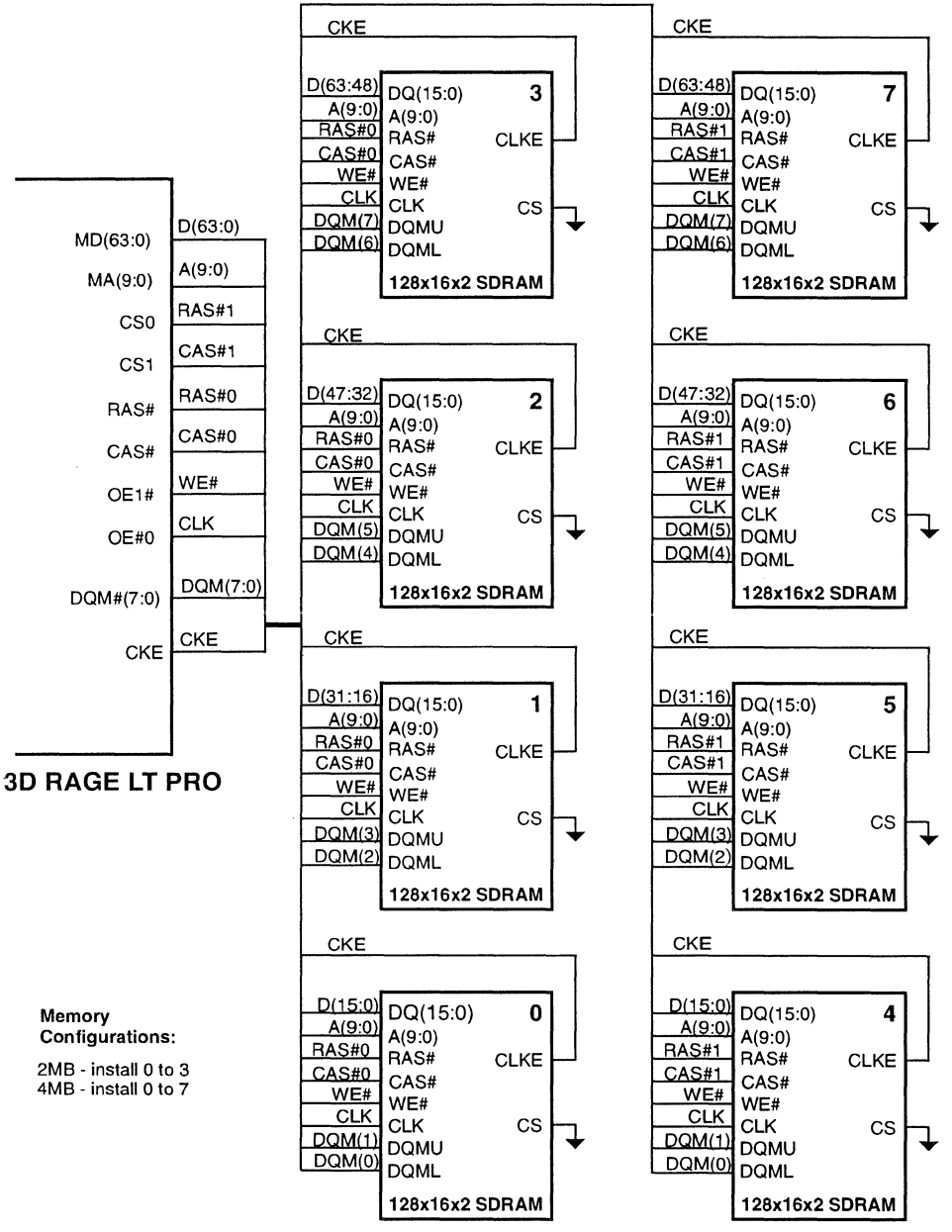


Figure 4-5. SDRAM Implementation

4.2.3 SGRAM Interface with 128x32x2 (8 Mbit) SGRAMs

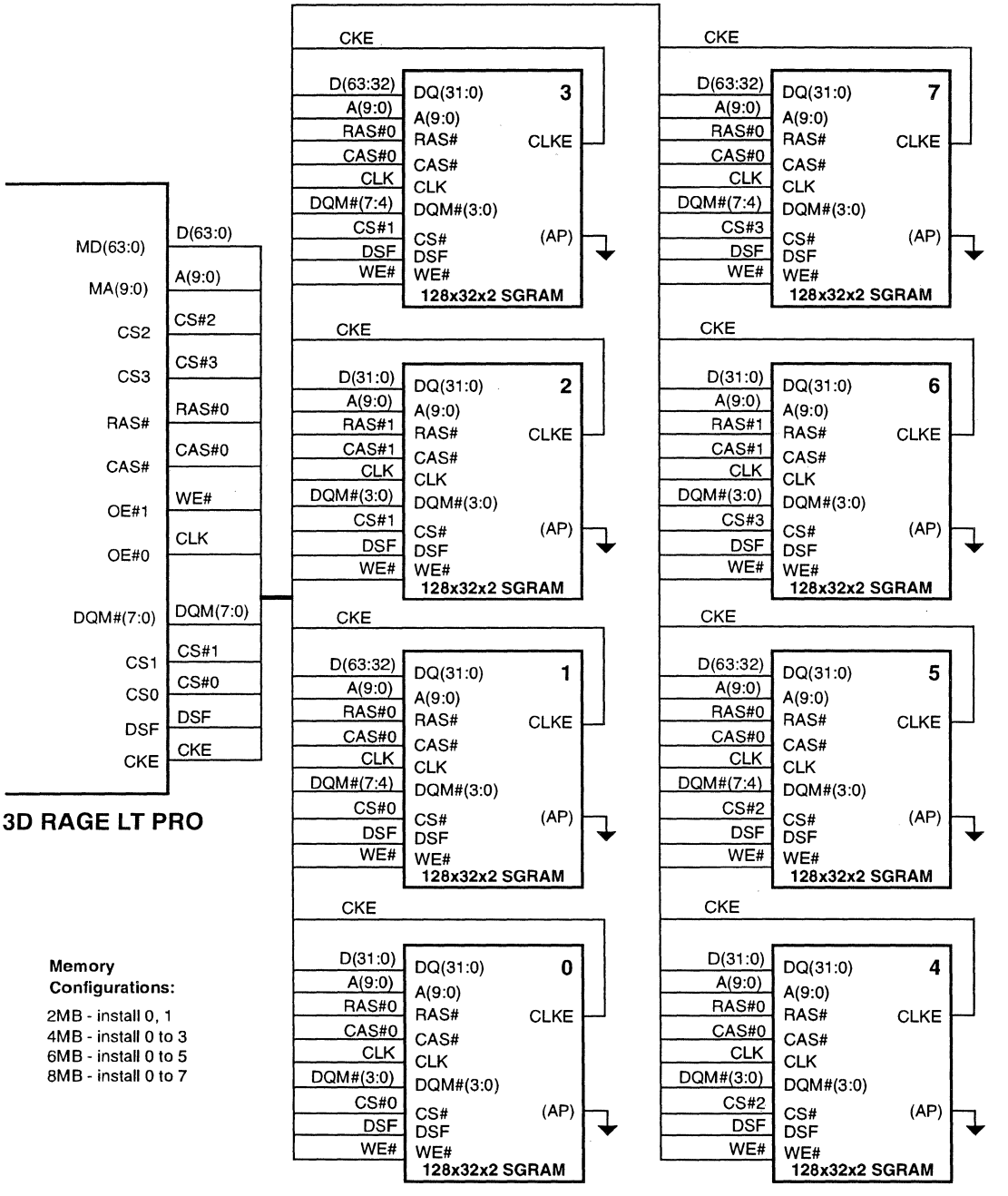


Figure 4-6. SGRAM Implementation (8 Mbit)

4.2.4 SGRAM Interface with 256x32x2 (16 Mbit) SGRAMs

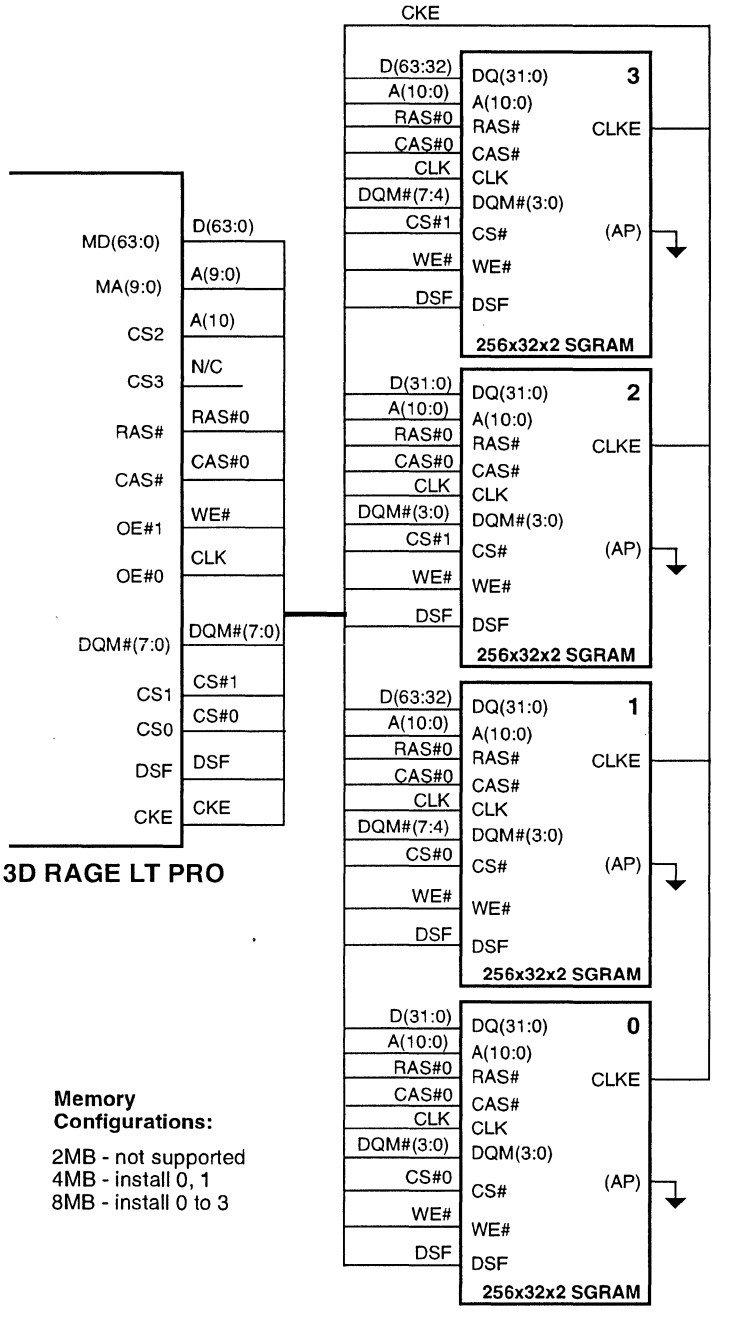


Figure 4-7. SGRAM Implementation (16 Mbit)

4.2.5 SGRAM Interface with 512x32x2 (32 Mbit) SGRAMs

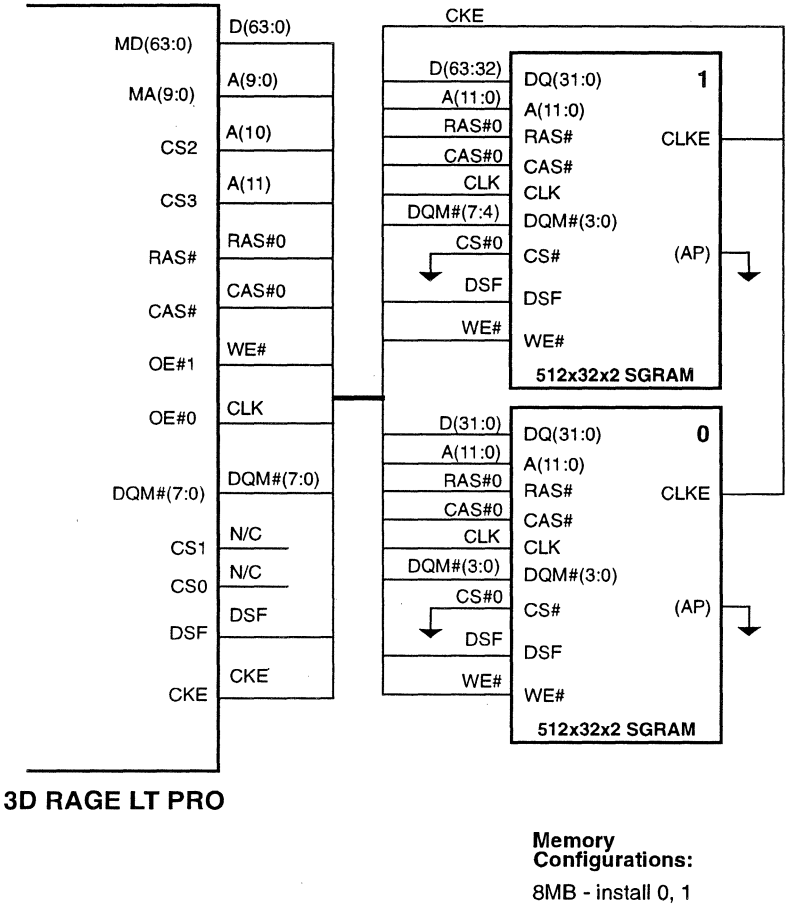


Figure 4-8. SGRAM Implementation (32 Mbit)

4.2.6 SO-DIMM Module Interface

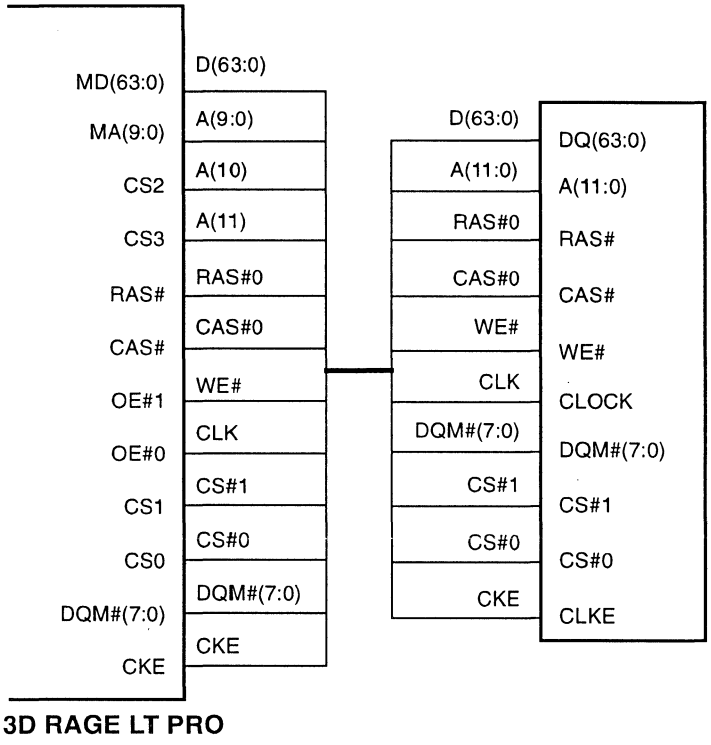


Figure 4-9. SO-DIMM Module Implementation

4.2.7 EPROM Interface

The video BIOS may be stored in either a 32K or a 64K EPROM (27256/27512), or integrated into the system BIOS. ATI offers a BIOS kit which is used for BIOS customization or integration of the video BIOS with the system BIOS (*see Figure 4-10.*). This kit allows certain BIOS options to be created, for example:

- 32K or 36K non-paged (linear) BIOS, or
- 64K BIOS
- 128K BIOS

Please refer to the *mach64 BIOS Kit (BIO-G01000)* manual for additional information on the differences and trade-offs of the various options.

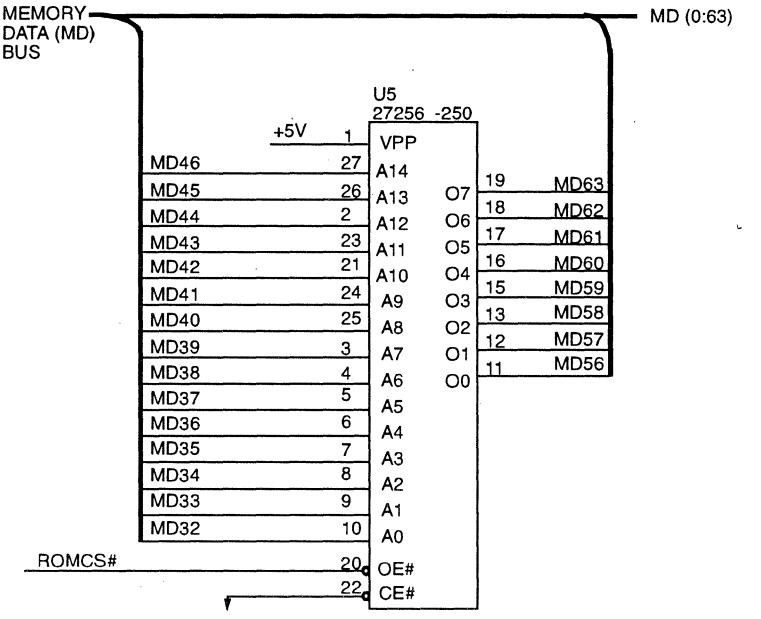


Figure 4-10. EPROM Interface

4.2.8 Flash Memory Interface

Up to 128K of flash memory is supported.

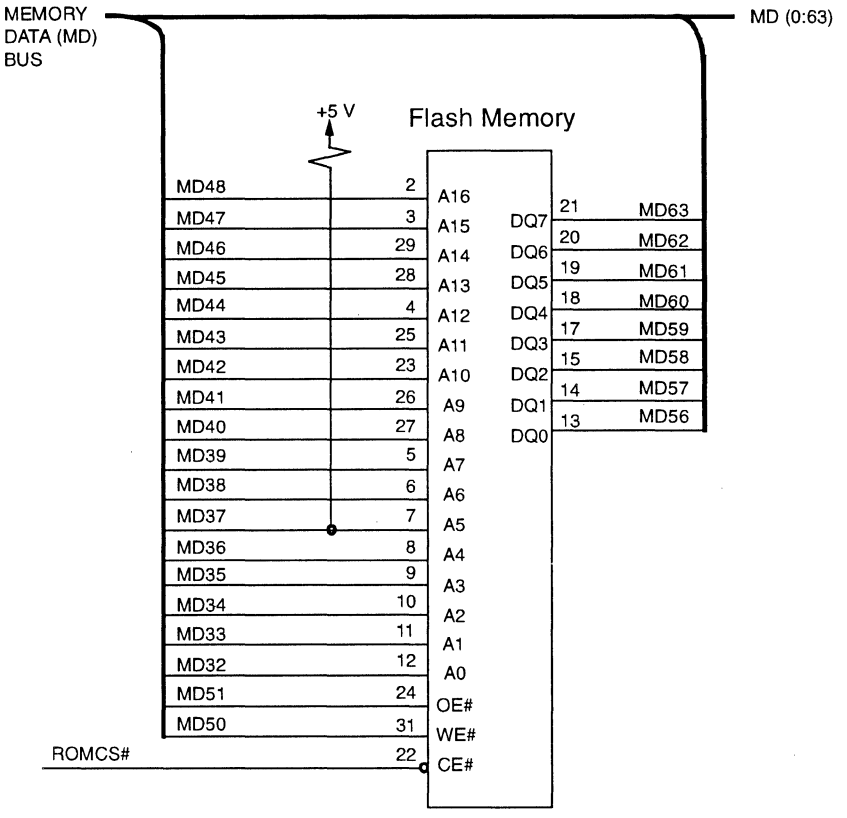


Figure 4-11. Flash Memory Interface

4.3 General Purpose I/O Control

Within the *3D RAGE LT PRO* there are 17 *general purpose* I/O pins and 19 pins for the Zoom Video Port. They are used to support the I^2C bus control, monitor ID and MPP port, ATI Multimedia Channel (AMC) Interface and Zoom Video Port input.

4.4 ATI Multimedia Channel 2.0 Interface (AMC)

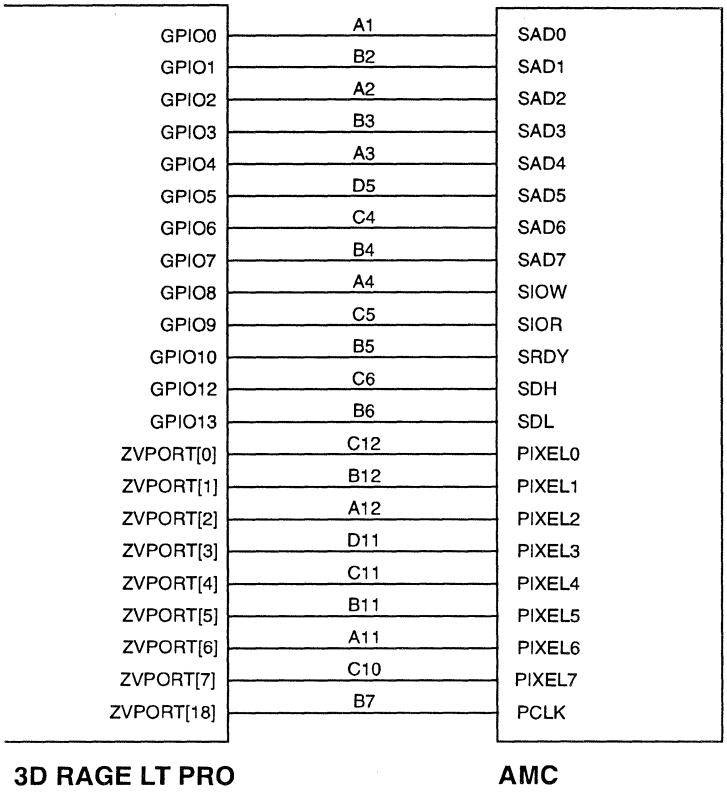


Figure 4-12. ATI Multimedia Channel 2.0 Interface

The AMC is a 40-pin connector that can be added to a design based on the *3D RAGE II*. The AMC can operate in various modes under different conditions. AMC pins have different functions under different modes. They are as follows:

4.4.1 DVS Mode

Digital Video Stream Mode supports a direct connection to a Brooktree Bt829, Bt827, Bt819, Bt817, or Bt815, Philips SAA7112 or SAA7111 and Samsung KSO122 or ITT VPC32xx video decoder. *Figures 4-13* and *4-14* show the 8-bit and 16-bit interface with the *3D RAGE LT PRO* chip.

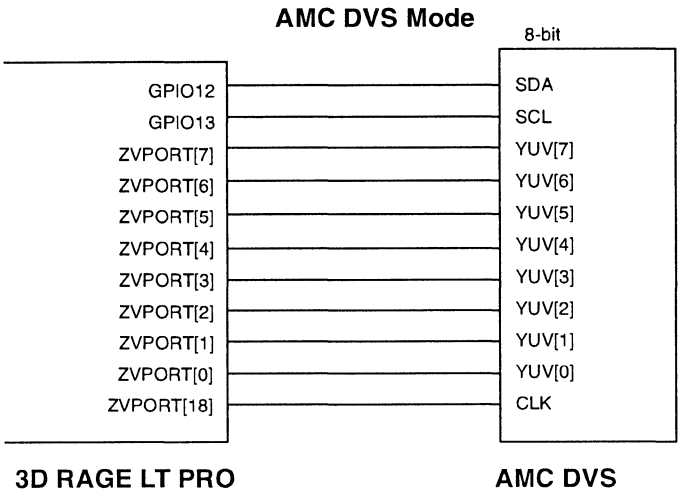


Figure 4-13. AMC DVS Mode (8 bit)

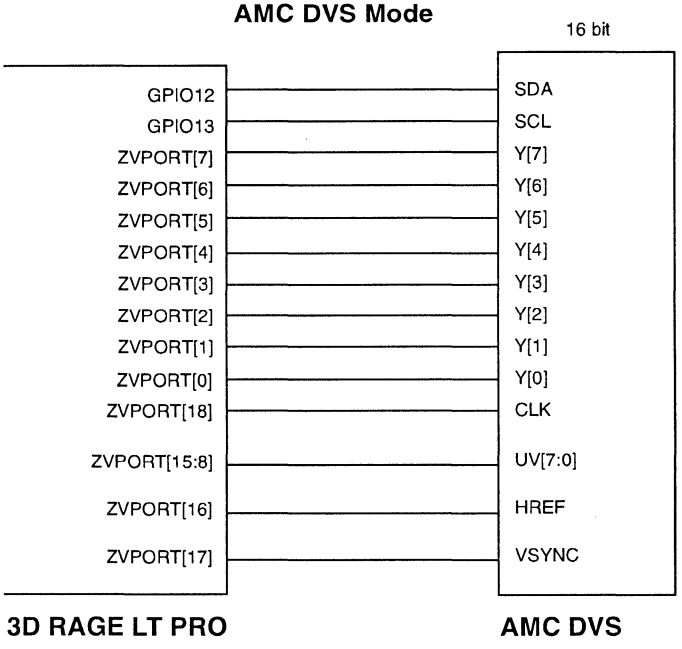


Figure 4-14. AMC DVS Mode (16 bit)

4.4.2 MPP Mode

Multimedia Peripheral Port Mode can stream data from the host memory out of this port. Timing and protocol can be programmed to support peripheral chips. By connecting this port to an external NTSC/PAL encoder, the display screen can be modulated to an NTSC/PAL TV signal. *Figure 4-15* shows the interface between external ImpacTV encoder and *3D RAGE LT PRO* chip.

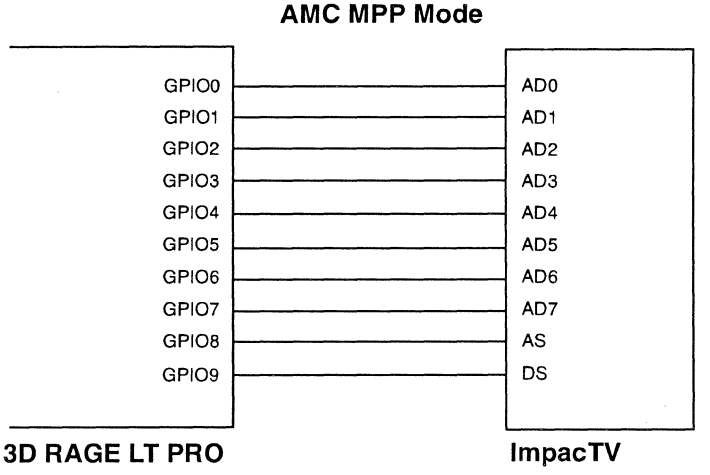


Figure 4-15. AMC MPP Mode

4.5 Zoom Video (ZV) Port Interface

Zoom Video Port (ZV-Port) is also supported with the *3D RAGE LT PRO*. It is a single-source uni-directional video bus between a PC Card socket and a VGA controller. The ZV Port allows video decoders to deliver real-time digital video straight into the VGA frame buffer from a PC Card.

The two following figures show the interface between the *3D RAGE LT PRO* and a ZV Port device, and how the ZV Port Bus can be used with multiple devices.

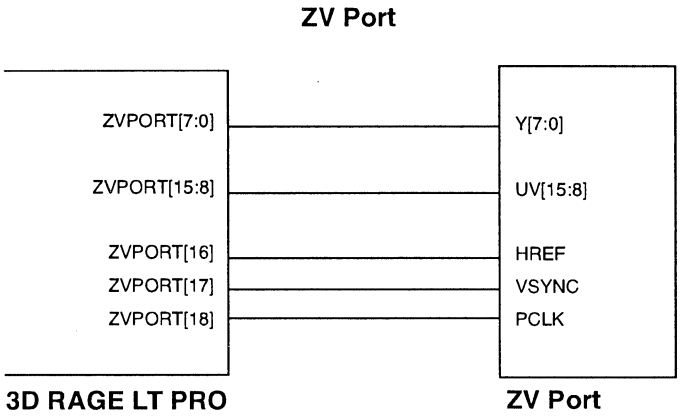


Figure 4-16. Zoom Video Port

For pin descriptions and timing information, please refer to section *7.4*.

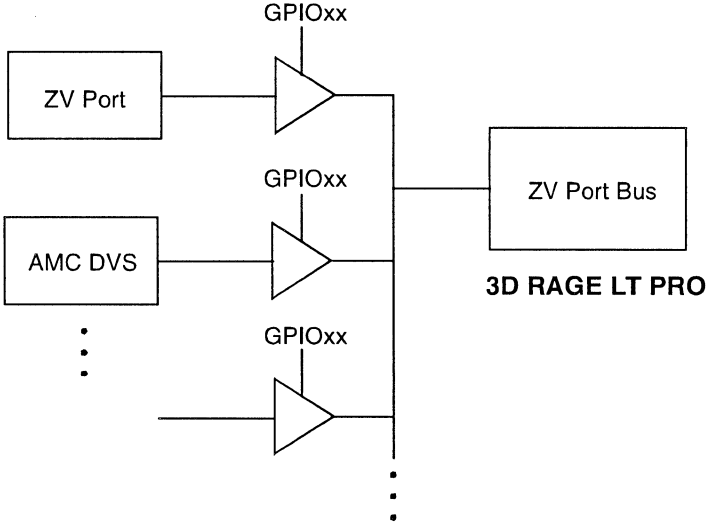


Figure 4-17. Zoom Video Example of Multiple Devices

For more information about ZV Port, please refer to the PCMCIA Standard Document.

4.6 LCD Panel Interface

The *3D RAGE LT PRO* controller has built-in interface to wide range of LCD panels including TFT and STN panels with different color depth and pixel packing format. Besides digital interface, the LVDS transmitter is implemented to reduce EMI and narrow the interface to the panel.

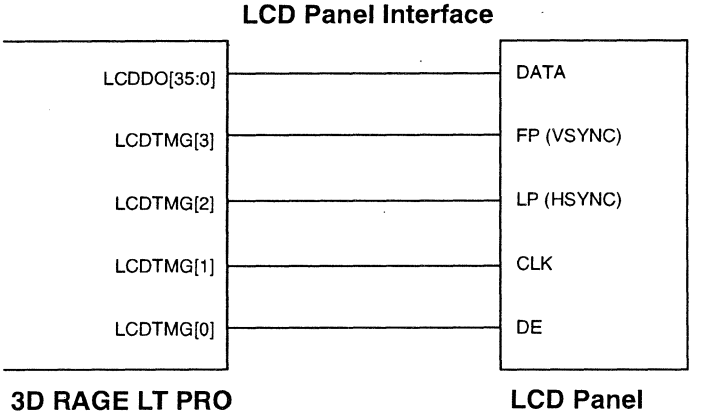


Figure 4-18. LCD Panel Interface

4.6.1 TFT Panel Digital Interface

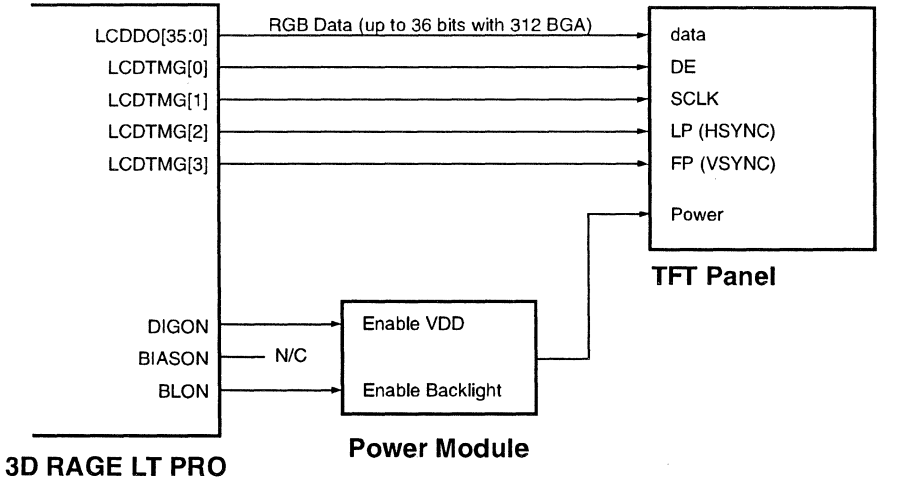


Figure 4-19. TFT Panel (Single/Double Pixel/Clk) Digital Interface

4.6.2 DSTN Panel Digital Interface

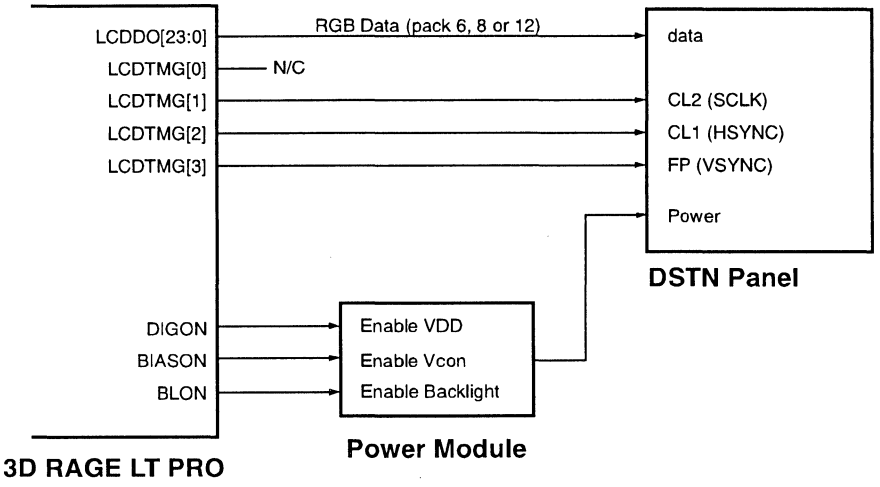


Figure 4-20. DSTN Panel Digital Interface

Note: For data mapping, refer to Chapter 6, Pin Descriptions

4.6.3 TFT Panel or DSTN LVDS Interface

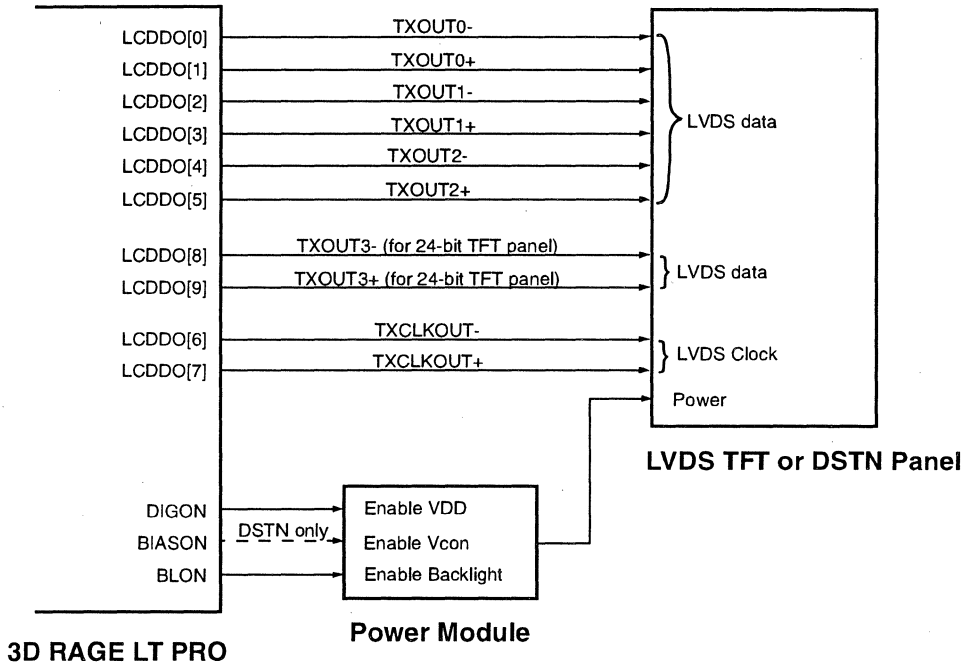
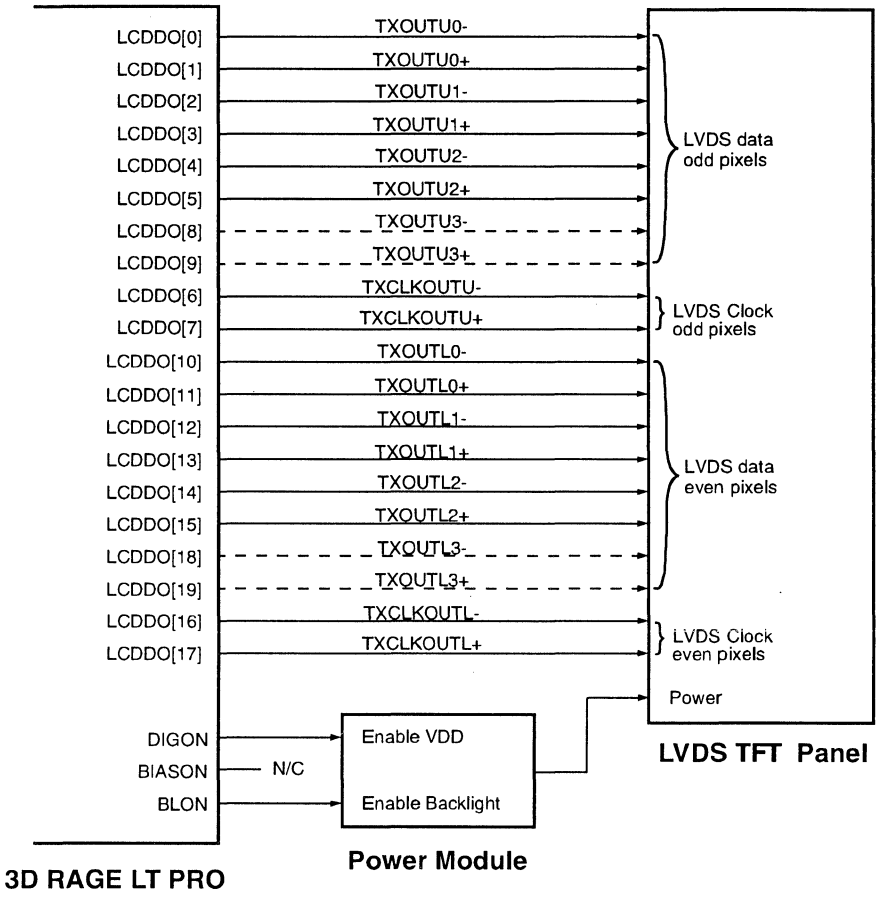


Figure 4-21. TFT Panel (Single Pixel/Clk) or DSTN LVDS Interface

Note: For LVDS data mapping, refer to Chapter 6, Pin Description

4.6.4 TFT Panel LVDS Interface



Note: For LVDS data mapping, refer to Chapter 6, Pin Descriptions.

Figure 4-22. TFT Panel (Double Pixel/Clk) LVDS Interface

4.7 Analog Output Section

Each of the R, G, B lines on the board (see *Figure 4-23*) is to be loaded with a 75Ω resistor. Diodes can be used to protect the controller from any large transient voltages which may enter from the connector when the monitor is connected.

Bypass capacitors can also be placed on all lines in order to filter the output. The RGB lines may also have inductors (ferrites) placed in series. This may be required in order to comply with FCC Class B requirements for radio frequency emissions. The proper value is determined as a trade-off between filtering the signals for FCC requirements and video signal clarity.

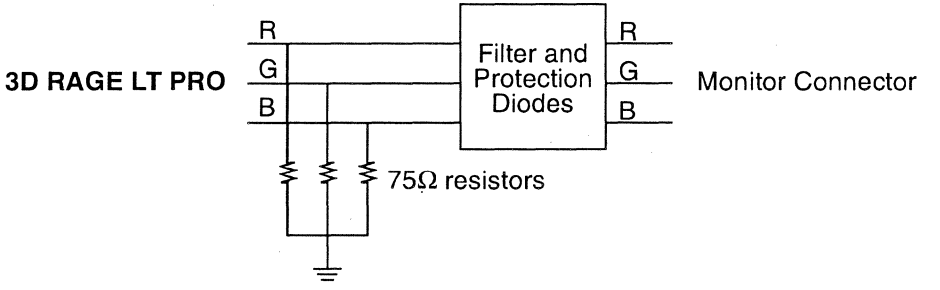


Figure 4-23. Analog Output

4.8 TV-Output Interface

The following implementation is recommended for Y, C, COMP and SYNC (for SCART) TV outputs, as well as R2SET, A2VSS, and A2VDD (for TV-Out DAC). Please refer to *Chapter 6, Pin Descriptions* for detailed pin descriptions.

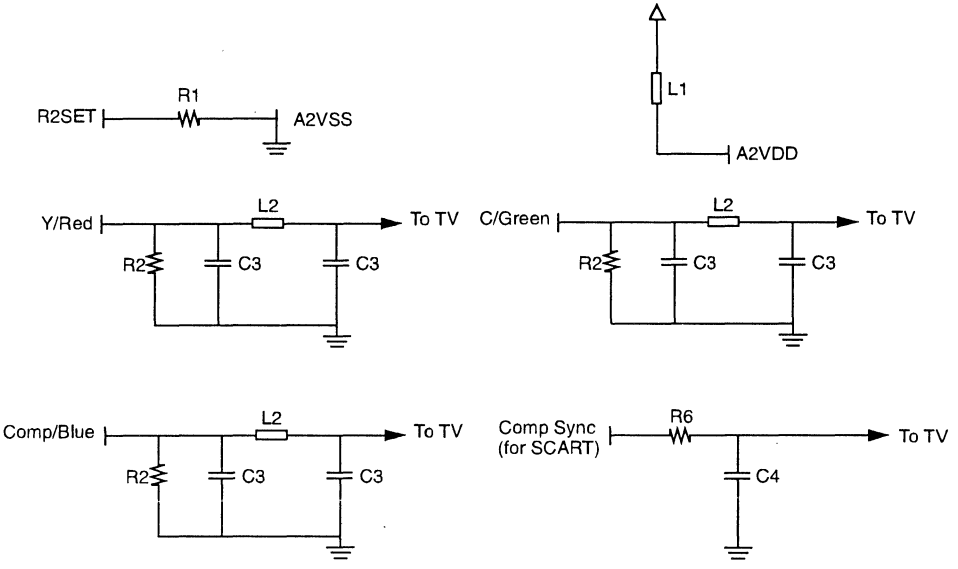


Figure 4-24. TV-Output Interface

Table 4-1 TV-Output Interface Component List

Item#	Qty	Name	Description
1	1	R1	Res. 0.1W 5% SM EIA(0805) T&R 422 R (1%)
2	3	R2	Res. 0.1W 5% SM EIA(0805) T&R 75 R (5% or 1%)
3	1	R6	Res. 0.1W 5% SM EIA(0805) T&R 330 R
4	6	C3	Cap. Ceramic SM 10% EIA(0805) 82pf
5	1	C4	Cap. Ceramic SM 10% EIA(0805) 470pf
6	1	L1	Ferrite Bead SM EIA(1806) T&R MURATA ERIE BLM41A04PT
7	3	L2	Inductor 1.8 µH

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Chapter 5
Controller Configuration

5.1 Strap Resistors Summary

External strap resistors may be used to configure various aspects of the *3D RAGE LT PRO* graphics subsystem. Logic levels at the strap pins are sensed and latched into registers at the first PCI command. The *3D RAGE LT PRO* contains internal pull-down resistors on strap pins to provide a default strap value of logic zero. By pulling the strap pin high via an external pull-up resistor, the strap value can be forced to logic one. In some cases, the registers which hold the strapped values are writable by video BIOS. The table below summarizes the strap pins on the controller. It is followed by a section which provides a detailed explanation of each strapping option.

Table 5-1 3D RAGE LT PRO Strap Resistors

Signal Name	Strap Name	BIOS Configurable	Description
MD63	reserved	n/a	0 = normal operation (default) 1 = reserved
MD62	IDSEL	No	0 = connect IDSEL to AD16 (default) 1 = connect IDSEL to AD17
MD61	ROM_REMAP	No	0 = No ROM Remap (default) 1 = If VGA disabled, accelerator ROM mapped to first 8K
MD60	reserved	n/a	0 = normal operation (default) 1 = reserved
MD59	ENINT#	No	0 = interrupt enable (default) 1 = interrupt disable
MD58	VGA_DISABLE	No	0 = VGA enable (default) 1 = VGA disable
MD57	PCI5VEN	No	Determines PCI signalling level (only when PCI bus is selected) 0 = PCI 3.3V 1 = PCI 5V
MD56	reserved	n/a	0 = normal operation (default) 1 = reserved

Table 5-1 3D RAGE LT PRO Strap Resistors (Continued)

Signal Name	Strap Name	BIOS Configurable	Description
MD55	TESTEN	No	0 = normal operation (default) 1 = test mode enabled
MD54	ID_DISABLE	n/a	0 = normal operation (default) 1 = IDSEL not connected
MD53	PREFETCH_EN	No	0 = disable prefetch (default) 1 = enable prefetch
MD52	reserved	n/a	0 = normal operation (default) 1 = reserved
MD(51:47)	PANEL_ID (4:0)	No	To be determined by the BIOS
MD(46:44)	X1CLK_SKEW (2:0)	No	AGP clock phase adjustment with respect to X2 (000) = 0.0 nsec (default) (001) = 0.5 nsec (010) = 1.0 nsec (011) = 1.5 nsec (100) = 2.0 nsec (101) = 2.5 nsec (110) = 3.0 nsec (111) = 3.5 nsec
MD(43:41)	AGPSKEW (2:0)	No	AGP X1 clock feedback phase adjustment with respect to refclk (cpuclk) (000) = refclk 1 tap earlier than X1 (feedback). Default (001) = refclk 2 taps earlier than X1 (feedback) (010) = refclk 3 taps earlier than X1 (feedback) (011) = agp pll testmode, X2 is used as feedback (100) = feedback (X1) 3 taps earlier than refclk (101) = feedback (X1) 2 taps earlier than refclk (110) = feedback (X1) 1 tap earlier than refclk (111) = feedbacl (X1) and refclk are aligned each tap is worth 0.5 nsec roughly
MD40	BUS_TYPE	No	0 = AGP with 312-BGA, PCI with 256-BGA 1 = PCI with 312-BGA

Table 5-1 3D RAGE LT PRO Strap Resistors (Continued)

Signal Name	Strap Name	BIOS Configurable	Description
MD(39:38)	AGP_VCO_GAIN(1:0)	No	VCO filter gain control (00) = (10) to VCO gain (default), no strap installed (01) = (11) to VCO gain (10) = (00) to VCO gain (11) = (01) to VCO gain
MD(37)	FLASHROM_WR_EN	No	0 = disable write to flash ROM 1 = enable write to flash ROM
MD(36:33)	reserved - not used	n/a	
MD(32:29)	DIMM_TYPE(3:0)	No	SO-DIMM type; see SO-DIMM specification
MD(28:24)	reserved - not used	n/a	
MD(23:8)	SUBSYS_VEN_ID(15:0)	Yes	(xxxxh) = PCI subsystem vendor ID
MD(7:0)	SUBSYS_DEV_ID(7:0)	Yes	(xxh) = LSB of PCI subsystem ID register

Note: Strap resistors do not need to be installed on X1CLKSKEW and AGPSKEW (**MD(46:44)** and **MD(43:41)** respectively).

5.2 Strap Resistor Description

MD62	IDSEL	No	0 = connect IDSEL to AD16 (default) 1 = connect IDSEL to AD17

This strap has only significance for AGP devices since IDSEL is not a signal in the AGP interface. In an AGP implementation, the initialization device select signaling is provided on AD16 as per the AGP specification. The IDSEL strap allows the alternate AD17 signal to be selected. This alternate IDSEL provides a method of initializing a second graphic controller on the AGP bus in some future application. This strap is not used for the PCI variant of *3D RAGE LT PRO* since a dedicated IDSEL signal is provided in the PCI bus interface.

MD61	ROM _REMAP	No	0 = No ROM Remap (default) 1 = If VGA disabled, remap top 8K to bottom

If VGA is disabled, this strap permits the remapping of the top 8K of the ROM to the bottom. This strap is only applicable to add-in cards which use a separate video BIOS ROM.

MD59	ENINT#	No	0 = interrupt enable (default) 1 = interrupt disable

The interrupt strap permits enabling or disabling of interrupts. The *3D RAGE LT PRO* has the capability of generating an interrupt request via the INTA# signal. Strapping MD59 to logic zero places the value 01h in the read-only Interrupt Pin register and enables interrupts. Strapping MD59 to logic one places the value 00h in the interrupt Pin register and disables interrupts. However, disabling the request for an interrupt resource does not prevent the graphics controller form asserting the INTA# signal if it is programmed to do so.

MD58	VGA_DISABLE	No	0 = VGA enable (default) 1 = VGA disable

The VGA disable strap provides a method of disabling the VGA portion of the graphics controller. This feature has possible application in systems containing more than one graphics controller.

MD57	PCI5VEN	No	0 = PCI 3.3V (default) 1 = PCI 5V

This strap signal determines the PCI signaling level of the PCI I/O buffers. If this strap is installed, the I/Os are programmed for 5V PCI signaling.

MD55	TESTEN	No	0 = normal operation (default) 1 = test mode enabled

This strap is used to place the *3D RAGE LT PRO* into test mode. Since test mode is only applicable for out-of-circuit testing, the provision for an external strap resistor is not required.

MD53	PREFETCH_EN	No	0 = disable prefetch (default) 1 = enable prefetch

This strap permits the setting of bit 3 in the memory base address register to mark the range as prefetchable (see the description in the PCI specification in Chapter 6). A device can mark a range as prefetchable if there are no side effects on speculative reads, the device returns all bytes on reads regardless of the byte enables, and a host bridge can merge processor writes into this range without causing errors. The *3D RAGE LT PRO* complies with these requirements.

MD(51:47)	PANEL_ID	No	To be determined by the BIOS

The Panel ID straps are used to identify the panel type that is attached to the graphics controller. It is mainly used by the universal BIOS to determine the configuration sequence for attached panel.

MD40	BUS_TYPE	No	0 = normal bus type (default) 1 = alternated bus type

This strapping has meaning for all *3D RAGE LT PRO* product variants. For devices in a 312 BGA package, the normal bus type is AGP and the alternate bus type is PCI. For devices in a 256 BGA package, the only bus type available is PCI.

MD(39:38)	AGP_VCO_GAIN	No	VCO filter gain control (00) = (10) to VCO gain (default), no strap installed (01) = (11) to VCO gain (10) = (00) to VCO gain (11) = (01) to VCO gain

These strap pins define the gain of the voltage controlled oscillator (VCO) in the PLL subsystem which generates the internal X1 and X2 AGP clock signals. The gain in the VCO circuit does not necessarily increases with increasing binary values of the strap setting. The default gain strapping of (00b) is the target implementation (i.e., no external resistors). However, the foot print for strap resistor on MD39 and MD38 should be provided on all new *3D RAGE LT PRO* designs in order to permit future adjustment of the gain control, if required.

MD37	FLASHROM_WR_EN	No	0 = disable write to Flash ROM (default) 1 = enable write to Flash ROM

This strap pin is used to enable writing to a Flash ROM.

MD(36:32)	reserved - not used	n/a	(xxxxxb) = don't care

These strap pins are not used. They are reserved for possible future use.

MD(32:29)	DIMM_TYPE	No	(xxxb) = determined by SO-DIMM; see SO-DIMM specification

These three bits are mandatory straps on all SO-DIMM modules and indicate the synchronous clock frequency or cycle time of the SO-DIMM. See the SO-DIMM specification for the definition of the strap resistors.

MD(28:24)	reserved - not used	n/a	(xxxxxb) = don't care

These five strap pins are not used. They are reserved for possible future use.

MD(23:8)	SUBSYS_VEN_ID(15:0)	Yes	(xxxxh) = PCI subsystem vendor ID

The subsystem vendor ID is a 16-bit register in PCI configuration space and used to uniquely identify subsystems manufactured by different vendors but with the same PCI or AGP device. The subsystem vendor ID for individual vendors is obtained from the PCI SIG.

The *3D RAGE LT PRO* supports two methods for loading the subsystem vendor ID register. The first involves writing the register with a customizable value stored in the video BIOS. This is the preferred approach and the one which is generally used. The second method involves strapping the MD(28:8) signals to set the desired subsystem vendor ID register value.

MD(7:0)	SUBSYS_DEV_ID(7:0)	Yes	(xxh) = LSB of PCI subsystem ID register

The subsystem ID is a 16-bit register in PCI configuration space and is used to identify a vendor's implementation of a particular subsystem. The subsystem ID is supplied by the vendor. The *3D RAGE LT PRO* supports two methods for loading the register. The first involves writing the register with a customizable value stored in the video BIOS. This is the preferred approach and the one that is generally used. The second method involves strapping the MD(7:0) signals for the desired register value. The strapped values on MD(7:0) are mapped to the lower byte of the subsystem ID register.

PCI33EN	BUS_CLK_SELECT	No	0 = normal bus clock (default) 1 = alternate bus clock

This is not a strap but a special pin on the 312 BGA package used for selecting the bus clock. For AGP versions of *3D RAGE LT PRO*, selecting normal bus clock sets the internal clock to the PLL. Selecting alternate bus clock, sets the internal clock to the external bus clock.

For PCI versions of *3D RAGE LT PRO*, selecting normal sets the internal clock to the PCI bus clock. Selecting alternate sets the internal clock to the PLL generated clock. The normal setting is the default for both AGP and PCI components. Since the alternate bus clock strapping may be useful during system checkout, initial *3D RAGE LT PRO* designs *must* provide the footprint for this pin on the 312 BGA package.

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Chapter 6
Pin Descriptions

6.1 Table Conventions

Controller pins have different operational characteristics. The assigned codes for each of these pin types are listed below. For electrical characteristics please refer to *Chapter 7 "Timing Specifications"*.

Table 6-1 Conventions

Code	Pin Type / Operational Characteristics
I	Input pin
O	Output pin
I/O	Bi-Directional pin
M	Multifunction pin
Pwr	Power pin
Gnd	Ground pin
A	Analog pins

Pin numbers and signal names are sorted by interface and by pin number on the following pages.

All active-low signal names are identified by the succeeding # character throughout this document, e.g. BLANK#.

6.2 Host Bus Interface

Table 6-2 AGP/PCI Bus Interface

Signal Name	Pin Type	Description
RESET#	I	Active Low PCI Reset
CPUCLK	I	Bus Clock
AD[31:0]	I/O	Multiplexed — System Address or Data bits [31:0]
C/BE#[3:0]	I/O	Multiplexed — Bus Command or Byte Enable bits 3:0. (BE# is active low)
IDSEL	I	Initialization Device Select - Used as a Chip Select during configuration read and write transactions. Used as PIPE# in AGP Bus (always "High").

Table 6-2 AGP/PCI Bus Interface (Continued)

Signal Name	Pin Type	Description
FRAME#	I/O	Frame is driven by the current bus master to indicate the beginning and duration of an access
IRDY#	I/O	Initiator Ready — Indicates the bus master is able to complete the current data phase of the transaction
TRDY#	I/O	Target Ready — Indicates the target agent is able to complete the current data phase of the transaction
DEVSEL#	I/O	Device Select — When driven active "Low", it is indication that the controller has decoded its address. Not used by AGP.
STOP#	I/O	Stop — Indicates the current target is requesting the master to stop the current transaction. Not used by AGP
PAR	O	Parity — Even parity used (expand on parity detection)
INTR#	O	Interrupt Request — Level triggered. Active "Low" by default
CLKRUN#	I/O	Power Management signal for PCI bus
REQ#	I/O	Request signal to arbiter — Indicates to the chip set that there is request for bus master cycle
GNT#	I	Grant signal from arbiter — Indicates to the agent that a bus access has been granted
ST(2:0)	O	Status bus for AGP support
SBA(7:0)	I	Sideband Address port for AGP support
RBF#	I	Read buffer full signal for AGP support
ADST#(1:0)	I/O	Address Strobe for AGP-133 support
SBST#	I/O	Sideband Strobe for AGP-133 support
STP_AGP#	I	Power Management signal for AGP bus
AGP_BUSY#	O	Power Management signal for AGP bus
PCI33EN	I	PCI 33MHz enable

The AGP-66 and AGP-133 interfaces are supported only with 312-pin BGA package.

Table 6-3 Host Bus Interface

Signal Name	PCI-33 MHz	AGP-66 MHz	AGP-133 MHz
AD(31:0)	AD(31:0)	AD(31:0)	AD(31:0)
CPUCLK	CPUCLK	CPUCLK	CPUCLK
RESET#	RESET#	RESET#	RESET#
IRDY	IRDY	IRDY	IRDY
FRAME#	FRAME#	FRAME#	FRAME#
IDSEL	IDSEL	PIPE#	PIPE#
TRDY#	TRDY#	TRDY#	TRDY#

Table 6-3 Host Bus Interface

Signal Name	PCI-33 MHz	AGP-66 MHz	AGP-133 MHz
DEVSEL#	DEVSEL#	DEVSEL#	DEVSEL#
STOP#	STOP#	STOP#	STOP#
PAR	PAR	PAR	PAR
CBE#(3)	CBE#(3)	CBE#(3)	CBE#(3)
CBE#(2)	CBE#(2)	CBE#(2)	CBE#(2)
CBE#(1)	CBE#(1)	CBE#(1)	CBE#(1)
CBE#(0)	CBE#(0)	CBE#(0)	CBE#(0)
INTR#	INTR#	INTR#	INTR#
REQ#	REQ#	REQ#	REQ#
GNT#	GNT#	GNT#	GNT#
SBST#			SBST#
ST(2)		ST(2)	ST(2)
ST(1)		ST(1)	ST(1)
ST(0)		ST(0)	ST(0)
SBA(7:0)		SBA(7:0)	SBA(7:0)
RBF#		RBF#	RBF#
ADST#(1:0)			ADST#(1:0)
CLKRUN#	CLKRUN#		
AGP_BUSY#		AGP_BUSY#	AGP_BUSY#
STP_AGP#		STP_AGP#	STP_AGP#
Total	49	62	65

6.3 Memory Interface

Table 6-4 Memory Interface

Signal Name	Pin Type	Description
MD[31:0]	I/O	Memory Data Bus
MD[48:32]	I/O	Memory Data Bus / EPROM Address line A(16:0)
MD[55:49]	I/O	Memory Data Bus
MD[63:56]	I/O	Memory Data Bus / EPROM Data line D(7:0)
MA[9:0]	O	Memory Address Bus
RAS#	O	Row Address Select
CAS#	I/O	Column Address Select

Table 6-4 Memory Interface (Continued)

Signal Name	Pin Type	Description
WE#[7:0]	I/O	This multifunction pin has the following functions: - Write Enable for DRAM - DQM for SDRAM
OE#1	O	This multifunction pin has the following functions: - Output Enable, OE#1, for DRAM - Write Enable, WE#, for SDRAM
OE#0	O	This multifunction pin has the following functions: - Output Enable, OE#0, for DRAM - MCK for SDRAM
CKE	O	Clock enable for SDRAM/SGRAM
CS[3:0]	I/O	Chip Select for SDRAM, 3 down to 0
ROMCS#	I/O	Chip Select for ROM (video BIOS)
DSF	I/O	DSF for SDRAM

Table 6-5 Memory Bus Pins Multiplexing

Pin Name	Memory Type			
	EDO/ Hyperpage DRAM	SDRAM/ SGRAM 128x32x2	SGRAM DIMM 128x32x2	SGRAM & SGRAM DIMM 256x32x2
MD(63:0)	MD(63:0)	MD(63:0)	MD(63:0)	MD(63:0)
MA(9:0)	MA(9:0)	MA(9:0)	MA(9:0)	MA(9:0)
CS(0)	RAS#(1)	RAS(1)	CS0	CS0
RAS#	RAS#(0)	RAS(0)	RAS	RAS
CS(1)	WE#(1)	CAS(1)	CS1	CS1
CAS#	WE#(0)	CAS(0)	CAS	CAS
WE#(7:0)	CAS#(7:0)	DQM(7:0)	DQM(7:0)	DQM(7:0)
OE#(1)	OE#(1)	WE#	WE#	WE#
OE#(0)	OE#(0)	MCK	MCK	MCK
CS(2)		/	CS2	MA(10)
CS(3)		/	CS3	/
CKE		CKE	CKE	CKE
DSF		DSF	DSF	DSF

Notes: The 32-bit memory interface is not supported for any memory type.
UMA memory configuration is no longer supported.

Table 6-6 Possible Memory Configurations

Total Memory Size (MB)	Memory Device		
	EDO	SGRAM 128x32x2	SGRAM 256x32x2
2	Yes	Yes	No
4	Yes	Yes	Yes
6	No	Yes	No
8	No	Yes	Yes

6.4 BIOS (EPROM) Interface

Table 6-7

Memory Data Pins	EPROM Interface		FLASH EPROM Interface	
	64 K	128 K	64 K	128 K
MD(47:32)	A(15:0)	A(15:0)	A(15:0)	A(15:0)
MD(48)	/	A(16)	/	A(16)
MD(63:56)	D(7:0)			
MD(50)	/	/	WE#	WE#
MD(51)	OE#	OE#	OE#	OE#
ROMCS#	CS#	CS#	CS#	CS#

6.5 DAC and Monitor Interface

Table 6-8 DAC1 (CRT) Monitor Interface

Signal Name	Pin Type	Description
R	A-O	Red for Monitor
G	A-O	Green for Monitor
B	A-O	Blue for Monitor
RSET	A-O	Internal Reference
HSYNC	O	Horizontal Sync output
VSYNC	O	Vertical Sync output
AVDD	A-I	DAC1 VDD
AVSS	A-O	DAC1 VSS
AVSS	A-O	DAC1 VSS

6.6 TV-Out Interface

Table 6-9 TV-Out (DAC2) Interface

Signal Name	Pin Type	Description
Y	A-O	DAC Output: outputs either Y (Luminance) for S-Video, or Red for RGB Video (SCART)
C	A-O	DAC Output: outputs either C (Colour/Chrominance) for S-Video, or Green for RGB Video
COMP	A-O	DAC Output: outputs either Composite Video, or Blue for RGB Video
SYNC	O	Composite Sync for SCART PAL TV's that use the EURO AV Connector. It is fed to the "Video In" pin of this connector to provide a signal that the TV can overlay the RGB data onto. This pin may also be used as a general I/O pin for controlling video switch, or for the other Internal timing signals including Hsync, Vsync, etc.
A2VDD	A-I	TV-Out DAC Analog Power, 3.3V
A2VSS	A-O	TV-Out DAC Analog Ground
R2SET	A-O	Current Setting resistor for TV-Out DAC is connected to this pin

6.7 Internal PLL (External Crystal Interface)

Table 6-10 External Crystal Interface

Signal Name	Pin Type	Description
XTALIN	I	PLL Reference Clock or MXCLK source (for oscillator* or crystal)
XTALOUT	O	PLL Reference Clock
PVDD	A-I	Phase Lock Loop Power
PVSS	A-O	Phase Lock Loop Ground
PAVDD	A-I	AGP Phase Lock Loop Power
PAVSS	A-O	AGP Phase Lock Loop Ground

* recommended — 29.498928713 MHz crystal oscillator with 50ppm accuracy (required for TV support)

6.8 Flat Panel Interface

Table 6-11 Flat Panel

Signal Name	Pin Type	Description
LCDDO(35:0)	O	LCD Data Output Pins, 24 pins available in 272 BGA LVDS Support - 20 pins
LCDTMG(3:0)	O	LCD Timing Signals
LTGIO(2:0)	I/O	Genneral purpose I/Os

6.8.1 TFT Panel Mapping

Table 6-12 TFT Panel Pins Multiplexing

LCD DATA Pins	TFT (SGA/XGA) 18-bit, 24-bit LVDS	TFT (XGA) 9-bit	TFT (XGA) 12-bit	TFT (XGA) Config1 18-bit	TFT (XGA) Config2 18-bit	TFT (SGA/ XGA) 24-bit
LCDDO(0)	TxOUTU0-	UR(0)	UR(0)		R(0)	R(0)
LCDDO(1)	TxOUTU0+	UR(1)	UR(1)		R(1)	R(1)
LCDDO(2)	TxOUTU1-	UR(2)	UR(2)	R(0)	R(2)	R(2)
LCDDO(3)	TxOUTU1+	LR(0)	UR(3)	R(1)	R(3)	R(3)
LCDDO(4)	TxOUTU2-	LR(1)	LR(0)	R(2)	R(4)	R(4)
LCDDO(5)	TxOUTU2+	LR(2)	LR(1)	R(3)	R(5)	R(5)
LCDDO(6)	TxCLKOUTU-	UG(0)	LR(2)	R(4)		R(6)
LCDDO(7)	TxCLKOUTU+	UG(1)	LR(3)	R(5)		R(7)
LCDDO(8)	TxOUTU3-	UG(2)	UG(0)		G(0)	G(0)
LCDDO(9)	TxOUTU3+	LG(0)	UG(1)		G(1)	G(1)
LCDDO(10)	TxOUTL0-	LG(1)	UG(2)	G(0)	G(2)	G(2)
LCDDO(11)	TxOUTL0+	LG(2)	UG(3)	G(1)	G(3)	G(3)
LCDDO(12)	TxOUTL1-	UB(0)	LG(0)	G(2)	G(4)	G(4)
LCDDO(13)	TxOUTL1+	UB(1)	LG(1)	G(3)	G(5)	G(5)
LCDDO(14)	TxOUTL2-	UB(2)	LG(2)	G(4)		G(6)
LCDDO(15)	TxOUTL2+	LB(0)	LG(3)	G(5)		G(7)
LCDDO(16)	TxCLKOUTL-	LB(1)	UB(0)		B(0)	B(0)
LCDDO(17)	TxCLKOUTL+	LB(2)	UB(1)		B(1)	B(1)
LCDDO(18)	TxOUTL3-		UB(2)	B(0)	B(2)	B(2)
LCDDO(19)	TxOUTL3+		UB(3)	B(1)	B(3)	B(3)
LCDDO(20)	LTGIO(3)	LTGIO(3)	LB(0)	B(2)	B(4)	B(4)

Table 6-12 TFT Panel Pins Multiplexing (Continued)

LCD DATA Pins	TFT (SGA/XGA) 18-bit, 24-bit LVDS	TFT (XGA) 9-bit	TFT (XGA) 12-bit	TFT (XGA) Config1 18-bit	TFT (XGA) Config2 18-bit	TFT (SGA/ XGA) 24-bit
LCDDO(21)	LTGIO(4)	LTGIO(4)	LB(1)	B(3)	B(5)	B(5)
LCDDO(22)	LTGIO(5)	LTGIO(5)	LB(2)	B(4)		B(6)
LCDDO(23)	LTGIO(6)	LTGIO(6)	LB(3)	B(5)		B(7)
LCDDO(24)						
LCDDO(25)						
LCDDO(26)						
LCDDO(27)						
LCDDO(28)						
LCDDO(29)						
LCDDO(30)						
LCDDO(31)						
LCDDO(32)						
LCDDO(33)	LTGIO(0)	LTGIO(0)	LTGIO(0)	LTGIO(0)	LTGIO(0)	LTGIO(0)
LCDDO(34)	LTGIO(1)	LTGIO(1)	LTGIO(1)	LTGIO(1)	LTGIO(1)	LTGIO(1)
LCDDO(35)	LTGIO(2)	LTGIO(2)	LTGIO(2)	LTGIO(2)	LTGIO(2)	LTGIO(2)

6.8.2 STN Panel Mapping

Table 6-13 STN Panel Pins Multiplexing

LCD DATA Pins	Color STN				
	Single Panel		Split Panel		
	PACK 12	PACK 16	PACK 6	PACK 8	PACK 12
LCDDO(0)	LD0/B(n+3)	LD0	UD0/Bx.1	UD0	UD0
LCDDO(1)	UD0/G(n+3)	UD0	UD1/Gx.1	UD1	UD1
LCDDO(2)	LD1/R(n+3)	LD1	UD2/Rx.1	UD2	UD2
LCDDO(3)	UD1/B(n+2)	UD1	UD3/Bx.0	UD3	UD3
LCDDO(4)	LD2/G(n+2)	LD2	UD4/Gx.0	UD4	UD4
LCDDO(5)	UD2/R(n+2)	UD2	UD5/Rx.0	UD5	UD5
LCDDO(6)	LD3/B(n+1)	LD3		UD6	UD6
LCDDO(7)	UD3/G(n+1)	UD3		UD7	UD7
LCDDO(8)	LD4/R(n+1)	LD4	LD0/Bz.1	LD0	LD0

Table 6-13 STN Panel Pins Multiplexing (Continued)

LCD DATA Pins	Color STN				
	Single Panel		Split Panel		
	PACK 12	PACK 16	PACK 6	PACK 8	PACK 12
LCDDO(9)	UD4/B(n)	UD4	LD1/Gz.1	LD1	LD1
LCDDO(10)	LD5/G(n)	LD5	LD2/Rz.1	LD2	LD2
LCDDO(11)	UD5/R(n)	UD5	LD3/Bz.0	LD3	LD3
LCDDO(12)		LD6	LD4/Gz.0	LD4	LD4
LCDDO(13)		UD6	LD5/Rz.0	LD5	LD5
LCDDO(14)		LD7		LD6	LD6
LCDDO(15)		UD7		LD7	LD7
LCDDO(16)					UD8
LCDDO(17)					UD9
LCDDO(18)					UD10
LCDDO(19)					UD11
LCDDO(20)	LTGIO(3)	LTGIO(3)	LTGIO(3)	LTGIO(3)	LD8
LCDDO(21)	LTGIO(4)	LTGIO(4)	LTGIO(4)	LTGIO(4)	LD9
LCDDO(22)	LTGIO(5)	LTGIO(5)	LTGIO(5)	LTGIO(5)	LD10
LCDDO(23)	LTGIO(6)	LTGIO(6)	LTGIO(6)	LTGIO(6)	LD11
LCDDO(24)					
LCDDO(25)					
LCDDO(26)					
LCDDO(27)					
LCDDO(28)					
LCDDO(29)					
LCDDO(30)					
LCDDO(31)					
LCDDO(32)					
LCDDO(33)	LTGIO(0)	LTGIO(0)	LTGIO(0)	LTGIO(0)	LTGIO(0)
LCDDO(34)	LTGIO(1)	LTGIO(1)	LTGIO(1)	LTGIO(1)	LTGIO(1)
LCDDO(35)	LTGIO(2)	LTGIO(2)	LTGIO(2)	LTGIO(2)	LTGIO(2)

Note: n = number of pixels in a row;
x = row number;
z = x + (panel height 2)

Table 6-14 LCD Control Pins

LCD Control Pins	TFT Panel	STN Panel
LCDTMG(3)	VSYNC	VSYNC/FLM/FP
LCDTMG(2)	HSYNC	HSYNC/CL1/LP
LCDTMG(1)	DCLK	DCLK/CL2
LCDTMG(0)	DTMG	VCLK for external LDVS or Panellink transmitter

Note: In 272 BGA package, digital interface is limited to 24 bits, single pixel per clock.

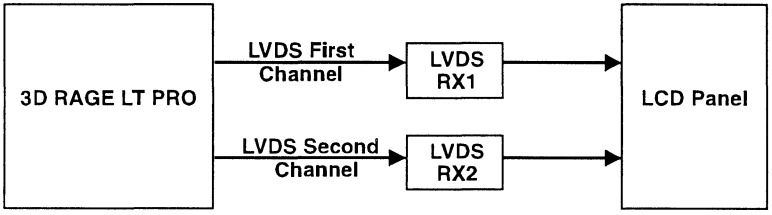
There are additional 3 LTGIO pins - LTGIO(2:0) - that can be used as general purpose I/O pins in any configuration. In case of configuration where LCDDO(23:20) are not used, those pins could be used as the general purpose I/O pins.

Table 6-15 Additional LTGIO Pins

LTGIO Pins	Function
LTGIO(2:0)	General purpose I/O pins

6.9 LVDS Data Arrangement

This section details the data output from the LVDS receiver when connected to the *3D RAGE LT PRO* for single and double pixel TFT and DSTN panels, using Pack 8x2 and Pack 16x2 format. They are the data between LVDS RX1, RX2 and the LCD.

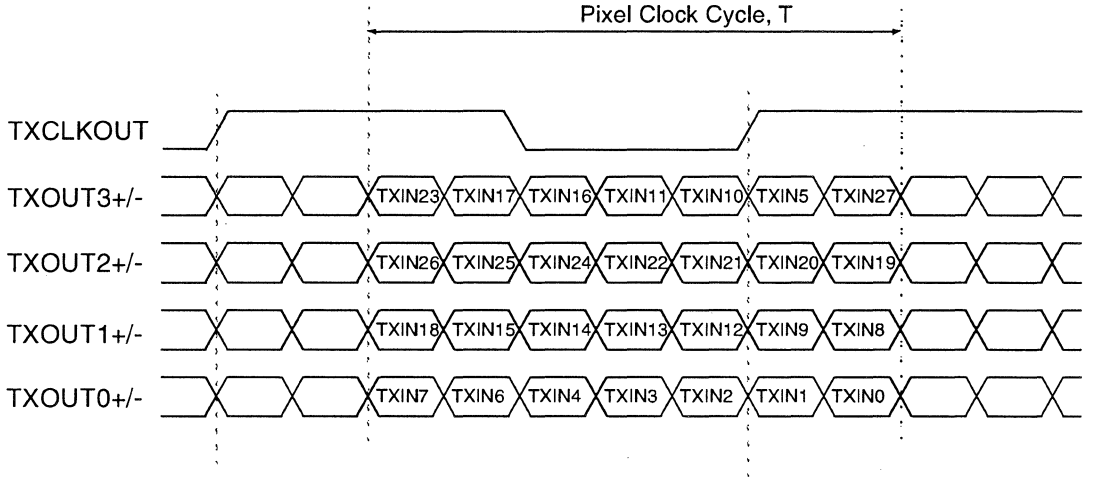


LVDS First Channel includes LT output pins LCDDO0 to LCDDO9
LVDS Second Channel includes LT output pins LCDDO10 to LCDDO19

Figure 6-1. 3D RAGE LT PRO LVDS Interface

6.9.1 LVDS Data/Clock Mapping

The diagram below shows the timing relation between the graphic data and the transmitted clock at the output of LCD CONTROLLER. TxClkOut +/- indicates the LVDS clock, while TxOut0 to TxOut3 indicate the data channels.



Data and clock transitions with labels indicate they belong to the same pixel. Those without lables belong to either the previous or the next pixel.

Figure 6-2. LVDS Data/Clock Mapping

Table 6-16 Signal Definition

Signal	Definition
TxIN	LVDS Transmitter Input (digital)
TxCLK In	LVDS Transmitter Input clock
TxOUT +/-	LVDS positive and negative differential Transmitter Outputs (analogue)
TxCLK Out +/-	LVDS positive and negative differential Transmitter Output clock
RxIN +/-	LVDS positive and negative differential Receiver Inputs (analogue)
RxCLK In +/-	LVDS positive and negative differential Receiver Input clock
RxOUT	LVDS Receiver Output (digital)
RxCLK Out	LVDS Receiver Output clock

Table 6-17 LVDS Pins Multiplexing

3D RAGE LT PRO pin	LVDS signal	Channel
LCDDO0	Txout0-	first
LCDDO1	Txout0+	first
LCDDO2	Txout1-	first
LCDDO3	Txout1+	first
LCDDO4	Txout2-	first
LCDDO5	Txout2+	first
LCDDO6	Txclk-	first
LCDDO7	Txclk+	first
LCDDO8	Txout3-	first
LCDDO9	Txout3+	first
LCDDO10	Txout0-	second
LCDDO11	Txout0+	second
LCDDO12	Txout1-	second
LCDDO13	Txout1+	second
LCDDO14	Txout2-	second
LCDDO15	Txout2+	second
LCDDO16	Txclk-	second
LCDDO17	Txclk+	second
LCDDO18	Txout3-	second
LCDDO19	Txout3+	second

6.9.2 TFT Interface

Table 6-18 18-bit TFT Using Single Pixel per Clock

RX1 output pin	Signal	RX1 output pin	Signal
RxOUT0	R0	RxOUT11	G5
RxOUT1	R1	RxOUT12	B0
RxOUT2	R2	RxOUT13	B1
RxOUT3	R3	RxOUT14	B2
RxOUT4	R4	RxOUT15	B3
RxOUT5	R5	RxOUT16	B4
RxOUT6	G0	RxOUT17	B5
RxOUT7	G1	RxOUT18	HSYNC
RxOUT8	G2	RxOUT19	VSYNC
RxOUT9	G3	RxOUT20	ENABLE
RxOUT10	G4	RxCLK OUT	CLOCK

Note: Output is from RX1 (e.g N.S. DS90C562, TI SN75LVDS86)

Table 6-19 18-bit TFT Using Double Pixel per Clock

RX1 output pin	Signal	RX2 output pin	Signal
RxOUT0	Ro0	RxOUT0	Re0
RxOUT1	Ro1	RxOUT1	Re1
RxOUT2	Ro2	RxOUT2	Re2
RxOUT3	Ro3	RxOUT3	Re3
RxOUT4	Ro4	RxOUT4	Re4
RxOUT5	Ro5	RxOUT5	Re5
RxOUT6	Go0	RxOUT6	Ge0
RxOUT7	Go1	RxOUT7	Ge1
RxOUT8	Go2	RxOUT8	Ge2
RxOUT9	Go3	RxOUT9	Ge3
RxOUT10	Go4	RxOUT10	Ge4
RxOUT11	Go5	RxOUT11	Ge5
RxOUT12	Bo0	RxOUT12	Be0
RxOUT13	Bo1	RxOUT13	Be1
RxOUT14	Bo2	RxOUT14	Be2
RxOUT15	Bo3	RxOUT15	Be3
RxOUT16	Bo4	RxOUT16	Be4

Table 6-19 18-bit TFT Using Double Pixel per Clock (Continued)

RX1 output pin	Signal	RX2 output pin	Signal
RxOUT17	Bo5	RxOUT17	Be5
RxOUT18	HSYNC	RxOUT18	See Note 2
RxOUT19	VSYNC	RxOUT19	See Note 2
RxOUT20	ENABLE	RxOUT20	See Note 2
RxCLK OUT	PCLK	RxCLK OUT	PCLK

Notes:

1) Output is from RX1 and RX2 (e.g N.S. DS90C562, TI SN75LVDS86). RX1 sends out the odd pixel while RX2 sends out the even pixel. In this case, odd pixel refers to the first pixel of the double pixel pair.

2) RxOUT 18/19/20 are LVDS_RESERVED_BIT [1]/[2]/[3] respectively. These bits are reserved to be programmed by the user.

Table 6-20 24 bit TFT Using Single Pixel per Clock

RX1 output pin	Signal	RX1 output pin	Signal
RxOUT0	R0	RxOUT14	G5
RxOUT1	R1	RxOUT15	B0
RxOUT2	R2	RxOUT16	B6
RxOUT3	R3	RxOUT17	B7
RxOUT4	R4	RxOUT18	B1
RxOUT5	R7	RxOUT19	B2
RxOUT6	R5	RxOUT20	B3
RxOUT7	G0	RxOUT21	B4
RxOUT8	G1	RxOUT22	B5
RxOUT9	G2	RxOUT23	NC
RxOUT10	G6	RxOUT24	HSYNC
RxOUT11	G7	RxOUT25	VSYNC
RxOUT12	G3	RxOUT26	ENABLE
RxOUT13	G4	RxOUT27	R6

Note: Output is from RX1 (e.g N.S. DS90C562, TI SN75LVDS86)

Table 6-21 24-bit TFT Using Double Pixel per Clock

RX1 output pin	Signal	RX2 output pin	Signal
RxOUT0	Ro0	RxOUT0	Re0
RxOUT1	Ro1	RxOUT1	Re1
RxOUT2	Ro2	RxOUT2	Re2
RxOUT3	Ro3	RxOUT3	Re3
RxOUT4	Ro4	RxOUT4	Re4
RxOUT5	Ro7	RxOUT5	Re7
RxOUT6	Ro5	RxOUT6	Re5
RxOUT7	Go0	RxOUT7	Ge0
RxOUT8	Go1	RxOUT8	Ge1
RxOUT9	Go2	RxOUT9	Ge2
RxOUT10	Go6	RxOUT10	Ge6
RxOUT11	Go7	RxOUT11	Ge7
RxOUT12	Go3	RxOUT12	Ge3
RxOUT13	Go4	RxOUT13	Ge4
RxOUT14	Go5	RxOUT14	Ge5
RxOUT15	Bo0	RxOUT15	Be0
RxOUT16	Bo6	RxOUT16	Be6
RxOUT17	Bo7	RxOUT17	Be7
RxOUT18	Bo1	RxOUT18	Be1
RxOUT19	Bo2	RxOUT19	Be2
RxOUT20	Bo3	RxOUT20	Be3
RxOUT21	Bo4	RxOUT21	Be4
RxOUT22	Bo5	RxOUT22	Be5
RxOUT23	NC	RxOUT23	NC
RxOUT24	HSYNC	RxOUT24	See Note 2
RxOUT25	VSYNC	RxOUT25	See Note 2
RxOUT26	ENABLE	RxOUT26	See Note 2
RxOUT27	Ro6	RxOUT27	Re6

Notes:

1) Output is from RX1 and RX2 (e.g N.S. DS90C562, TI SN75LVDS86). RX1 sends out the odd pixel while RX2 sends out the even pixel. In this case, odd pixel refers to the first pixel of the double pixel pair.

2) RxOUT 24/25/26 are LVDS_RESERVED_BIT [1]/[2]/[3] respectively. These bits are reserved to be programmed by the user.

6.9.3 DSTN Interface

Table 6-22 DSTN Pack 12 x2 Panel

RX1 output pin	Signal	RX1 output pin	Signal
RxOUT0	DISP.ON	RxOUT14	LD10
RxOUT1	UD0	RxOUT15	LD9
RxOUT2	UD1	RxOUT16	LD8
RxOUT3	UD2	RxOUT17	LD7
RxOUT4	UD3	RxOUT18	LD6
RxOUT5	UD4	RxOUT19	LD5
RxOUT6	UD5	RxOUT20	LD4
RxOUT7	UD6	RxOUT21	LD3
RxOUT8	UD7	RxOUT22	LD2
RxOUT9	UD8	RxOUT23	LD1
RxOUT10	UD9	RxOUT24	LD0
RxOUT11	UD10	RxOUT25	CLOCK
RxOUT12	UD11	RxOUT26	HSYNC
RxOUT13	LD11	RxOUT27	VSYNC

Note: Output is from RX1 (e.g N.S. DS90C582I, TI SN75LVDS82)

Table 6-23 DSTN Pack 8 x2 Panel

RX1 output pin	signal	RX1 output pin	signal
RxOUT0	DISP.ON	RxOUT14	nc
RxOUT1	UD0	RxOUT15	nc
RxOUT2	UD1	RxOUT16	nc
RxOUT3	UD2	RxOUT17	LD7
RxOUT4	UD3	RxOUT18	LD6
RxOUT5	UD4	RxOUT19	LD5
RxOUT6	UD5	RxOUT20	LD4
RxOUT7	UD6	RxOUT21	LD3
RxOUT8	UD7	RxOUT22	LD2
RxOUT9	nc	RxOUT23	LD1
RxOUT10	nc	RxOUT24	LD0
RxOUT11	nc	RxOUT25	CLOCK
RxOUT12	nc	RxOUT26	HSYNC
RxOUT13	nc	RxOUT27	VSYNC

Note: Output is from RX1 (e.g N.S. DS90C582I, TI SN75LVDS82)

6.10 Panel Control Interface

Table 6-24 Panel Control

Signal Name	Pin Type	Description
DIGON	O	Controls Panel Digital Power
BIASON	O	Controls Panel Bias Voltage
BLON	O	Control Backlight On/Off
F32KHz	I	32KHz clock input for memory refresh
STANDBY#	I	It has one of 2 functions: - Pin Mode: Chip goes into standby mode when this pin is active. - Timer mode: Use as activity pin.
SUSPEND#	I	Chip goes into suspend mode when this pin is active

6.11 Zoom Video Port Interface

Table 6-25 ZV Port Interface

Signal Name	Pin Type	Description
ZVPORT(18:0)	I	Zoom Video Port, Video in port, LVDS test mode output

Table 6-26 ZV-Port Pins Multiplexing

Signal Name	ZV, Philips Port		Bt 81975	
	Pin Name	Direction	Pin Name	Direction
ZVPORT(0)	Y0	I	YUV0	I
ZVPORT(1)	Y1	I	YUV1	I
ZVPORT(2)	Y2	I	YUV2	I
ZVPORT(3)	Y3	I	YUV3	I
ZVPORT(4)	Y4	I	YUV4	I
ZVPORT(5)	Y5	I	YUV5	I
ZVPORT(6)	Y6	I	YUV6	I
ZVPORT(7)	Y7	I	YUV7	I
ZVPORT(8)	UV0	I	ZVGPIO(0)	I/O
ZVPORT(9)	UV1	I	ZVGPIO(1)	I/O
ZVPORT(10)	UV2	I	ZVGPIO(2)	I/O
ZVPORT(11)	UV3	I	ZVGPIO(3)	I/O
ZVPORT(12)	UV4	I	ZVGPIO(4)	I/O

Table 6-26 ZV-Port Pins Multiplexing (Continued)

Signal Name	ZV, Philips Port		Bt 81975	
	Pin Name	Direction	Pin Name	Direction
ZVPORT(13)	UV5	I	ZVGPIO(5)	I/O
ZVPORT(14)	UV6	I	ZVGPIO(6)	I/O
ZVPORT(15)	UV7	I	ZVGPIO(7)	I/O
ZVPORT(16)	HREF	I	/	/
ZVPORT(17)	VSYNC	I	/	/
ZVPORT(18)	PCLK	I	PCLK	I

Note: In 8-bit video input mode, ZVPORT(17:8) could be used as general purpose I/Os.

6.12 General Purpose I/O Interface

Table 6-27 General Purpose I/O

Signal Name	Pin Type	Description
GPIO(16:0)	I/O	MPP Port Monitor ID (3 pins) I2C Support (2 pins)

Table 6-28 General Purpose I/O Pins Multiplexing

Pin Name	I2C_SEL(1) = 0	I2C_SEL(1) = 1	Direction
	Function MPP Port	Function MPP Port	
GPIO(0)	SAD0	SAD0	IO
GPIO(1)	SAD1	SAD1	IO
GPIO(2)	SAD2	SAD2	IO
GPIO(3)	SAD3	SAD3	IO
GPIO(4)	SAD4	SAD4	IO
GPIO(5)	SAD5	SAD5	IO
GPIO(6)	SAD6	SAD6	IO
GPIO(7)	SAD7	SAD7	IO
GPIO(8)	SIOR	SIOR	IO
GPIO(9)	SIOW	SIOW	IO
GPIO(10)	SRDY	I2CCLK	IO
GPIO(11)	mon ID3	GPIO	IO
GPIO(12)	I2CSDA	I2CSDA	IO

Table 6-28 General Purpose I/O Pins Multiplexing (Continued)

Pin Name	I2C_SEL(1) = 0	I2C_SEL(1) = 1	Direction
	Function MPP Port	Function MPP Port	
GPIO(13)	I2CCLK	mon ID3	IO
GPIO(14)	mon ID0	mon ID0	IO
GPIO(15)	mon ID1	mon ID1	IO
GPIO(16)	mon ID2	mon ID2	IO

Note: In order to be pin compatible with RAGE LT chip, the position of I2C clock is programmed with I2C_SEL(1) bit.

6.13 Optional ATI Multimedia Channel Interface

Table 6-29 AMC Interface

Signal Name	Pin Type	Descriptions	
		DVS mode	MPP mode
ZVPORT(7:0)		YUV(7:0)	*
ZVPORT(18)	I/O	CLK	Dot (Pixel) Clock
GPIO0	M-I/O	*	SAD0
GPIO1	M-I/O	*	SAD1
GPIO2	M-I/O	*	SAD2
GPIO3	I/O	*	SAD3
GPIO4	I/O	*	SAD4
GPIO5	I/O	*	SAD5
GPIO6	I/O	*	SAD6
GPIO7	I/O	*	SAD7
GPIO8	O	*	SIOR
GPIO9	O	*	SIOW
GPIO10	O	*	SRDY/IRQ
GPIO11	I/O	*	*
GPIO12	I/O	SDA	*
GPIO13	I/O	SCL	*
GPIO14, GPIO15, GPIO16	I/O	*	*

Note: Any extra pins not used (*) in a particular mode can be used as a general purpose I/O pins GPIO.

6.13.1 LCD SYNC Signals Mapping

Table 6-30

LCD Timing	Panel Type	
	TFT	STN
LCDTMG0	Display Enable	Free run clock for external panel link support
LCDTMG1	Data Clock (Shift Clock)	Data Clock
LCDTMG2	Line Pulse (HSync)	Line Pulse
LCDTMG3	Frame Pulse (VSync)	Frame Pulse

6.14 Power and Ground Pins

There are three power rings: core power (VDDC), I/O power (VDDR) and PCI power (VPP). The ground ring (VSS) is common for all of them (VSSC, VSSR and VSSP).

Table 6-31 Power and Ground Pins

Signal Name	Pin Type	Description
VPP (2 pins)	I	PCI Power - 3.3V/5V
VDD (10 pins)	I	Digital Power - 3.3V
VSS (6 + 16 pins)	O	Digital Ground
LPVDD	I	LVDS PLL Power pin
LPVSS	O	LVDS PLL Ground pin

6.15 256-pin BGA Pin Listings

6.15.1 Pinout by Ball Reference

Table 6-32 256 BGA Pinout by Ball Reference

Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name
A1	GPIO0	A2	GPIO2	A3	GPIO4
A4	GPIO8	A5	GPIO11	A6	GPIO14
A7	ZVPORT17	A8	ZVPORT14	A9	ZVPORT13
A10	ZVPORT09	A11	ZVPORT06	A12	ZVPORT02
A13	AD0	A14	AD4	A15	AD7
A16	AD10	A17	AD14	A18	PAR
A19	DEVSEL#	A20	IRDY#	B1	R

Table 6-32 256 BGA Pinout by Ball Reference (Continued)

Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name
B2	GPIO1	B3	GPIO3	B4	GPIO7
B5	GPIO10	B6	GPIO13	B7	ZVPORT18
B8	ZVPORT15	B9	ZVPORT12	B10	ZVPORT08
B11	ZVPORT05	B12	ZVPORT01	B13	AD1
B14	AD5	B15	CBE0#	B16	AD11
B17	AD15	B18	STOP#	B19	TRDY#
B20	FRAME#	C1	RSET	C2	G
C3	AVSS	C4	GPIO6	C5	GPIO9
C6	GPIO12	C7	GPIO16	C8	ZVPORT16
C9	ZVPORT11	C10	ZVPORT07	C11	ZVPORT04
C12	ZVPORT00	C13	AD2	C14	AD6
C15	AD8	C16	AD12	C17	CBE1#
C18	AD17	C19	AD16	C20	CBE2#
D1	PVSS	D2	PVDD	D3	B
D4	AVSS	D5	GPIO5	D6	VDDR
D7	GPIO15	D8	VSS	D9	ZVPORT10
D10	VDDC	D11	ZVPORT03	D12	VSS
D13	AD3	D14	VPP	D15	AD9
D16	AD13	D17	AD21	D18	AD20
D19	AD19	D20	AD18	E1	HSY
E2	VSY	E3	AVDD	E4	VDDR
E17	CBE3#	E18	IDSEL	E19	AD23
E20	AD22	F1	LCDDO0	F2	LPVSSR
F3	XTALOUT	F4	XTALIN	F17	AD27
F18	AD26	F19	AD25	F20	AD24
G1	LCDDO4	G2	LCDDO3	G3	LCDDO2
G4	LCDDO1	G17	AD31	G18	AD30
G19	AD29	G20	AD28	H1	LCDDO8
H2	LCDDO7	H3	LCDDO6	H4	LCDDO5
H17	CLKRUN#	H18	RESET#	H19	GNT#
H20	REQ#	J1	LCDDO9	J2	LPVSS
J3	LPVDD	J4	LPVDDR	J9	VSS
J10	VSS	J11	VSS	J12	VSS
J17	VPP	J18	CPUCLK	J19	MD62
J20	MD61	K1	LCDDO13	K2	LCDDO12

Table 6-32 256 BGA Pinout by Ball Reference (Continued)

Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name
K3	LCDDO11	K4	LCDDO10	K9	VSS
K10	VSS	K11	VSS	K12	VSS
K17	INTR#	K18	MD63	K19	MD60
K20	MD59	L1	LCDDO14	L2	LCDDO15
L3	LCDDO16	L4	VDDC	L9	VSS
L10	VSS	L11	VSS	L12	VSS
L17	VDDC	L18	MD58	L19	MD57
L20	MD56	M1	LCDDO17	M2	LCDDO18
M3	LCDDO19	M4	LPVSSR	M9	VSS
M10	VSS	M11	VSS	M12	VSS
M17	MD52	M18	MD53	M19	MD54
M20	MD55	N1	LCDDO20	N2	LCDDO21
N3	LCDDO22	N4	LCDDO23	N17	MD48
N18	MD49	N19	MD50	N20	MD51
P1	A2VSS	P2	A2VSS	P3	Y
P4	C	P17	MD44	P18	MD45
P19	MD46	P20	MD47	R1	COMP
R2	R2SET	R3	A2VDD	R4	VDDR
R17	MD40	R18	MD41	R19	MD42
R20	MD43	T1	SYNC	T2	LTGIO0
T3	LTGIO1	T4	LTGIO2	T17	MD30
T18	MD37	T19	MD38	T20	MD39
U1	CS3	U2	LCDTMG0	U3	LCDTMG1
U4	VSS	U5	OE#1	U6	DSF
U7	VDDR	U8	MA5	U9	VSS
U10	WE#2	U11	VDDC	U12	MD4
U13	VDDR	U14	MD11	U15	MD15
U16	MD19	U17	MD28	U18	MD31
U19	MD35	U20	MD36	V1	LCDTMG2
V2	LCDTMG3	V3	BIASON	V4	CS1
V5	RAS#0	V6	OE#0	V7	MA2
V8	MA6	V9	MA9	V10	WE#3
V11	MD0	V12	MD3	V13	MD7
V14	MD10	V15	MD14	V16	MD18
V17	MD22	V18	MD29	V19	MD32

Table 6-32 256 BGA Pinout by Ball Reference (Continued)

Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name
V20	MD34	W1	DIGON	W2	F32KHZ
W3	SUSPEND#	W4	CKE	W5	CAS#0
W6	MA0	W7	MA3	W8	MA7
W9	WE#0	W10	WE#4	W11	WE#7
W12	MD2	W13	MD6	W14	MD9
W15	MD13	W16	MD17	W17	MD21
W18	MD24	W19	MD27	W20	MD33
Y1	BLON	Y2	STANDBY#	Y3	CS0
Y4	ROMCS#	Y5	CS2	Y6	MA1
Y7	MA4	Y8	MA8	Y9	WE#1
Y10	WE#5	Y11	WE#6	Y12	MD1
Y13	MD5	Y14	MD8	Y15	MD12
Y16	MD16	Y17	MD20	Y18	MD23
Y19	MD25	Y20	MD26		

6.15.2 Pinout by Signal Name

Table 6-33 256 BGA Pinout by Signal Name

Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.
A2VDD	R3	A2VSS	P1	A2VSS	P2
AD0	A13	AD1	B13	AD2	C13
AD3	D13	AD4	A14	AD5	B14
AD6	C14	AD7	A15	AD8	C15
AD9	D15	AD10	A16	AD11	B16
AD12	C16	AD13	D16	AD14	A17
AD15	B17	AD16	C19	AD17	C18
AD18	D20	AD19	D19	AD20	D18
AD21	D17	AD22	E20	AD23	E19
AD24	F20	AD25	F19	AD26	F18
AD27	F17	AD28	G20	AD29	G19
AD30	G18	AD31	G17	AVDD	E3
AVSS	C3	AVSS	D4	B	D3
BIASON	V3	BLON	Y1	C	P4
CAS#0	W5	CBE0#	B15	CBE1#	C17

Table 6-33 256 BGA Pinout by Signal Name (Continued)

Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.
CBE2#	C20	CBE3#	E17	CKE	W4
CLKRUN#	H17	COMP	R1	CPUCLK	J18
CS0	Y3	CS1	V4	CS2	Y5
CS3	U1	DEVSEL#	A19	DIGON	W1
DSF	U6	F32KHZ	W2	FRAME#	B20
G	C2	GNT#	H19	GPIO0	A1
GPIO1	B2	GPIO2	A2	GPIO3	B3
GPIO4	A3	GPIO5	D5	GPIO6	C4
GPIO7	B4	GPIO8	A4	GPIO9	C5
GPIO10	B5	GPIO11	A5	GPIO12	C6
GPIO13	B6	GPIO14	A6	GPIO15	D7
GPIO16	C7	HSY	E1	IDSEL	E18
INTR#	K17	IRDY#	A20	LCDDO0	F1
LCDDO1	G4	LCDDO2	G3	LCDDO3	G2
LCDDO4	G1	LCDDO5	H4	LCDDO6	H3
LCDDO7	H2	LCDDO8	H1	LCDDO9	J1
LCDDO10	K4	LCDDO11	K3	LCDDO12	K2
LCDDO13	K1	LCDDO14	L1	LCDDO15	L2
LCDDO16	L3	LCDDO17	M1	LCDDO18	M2
LCDDO19	M3	LCDDO20	N1	LCDDO21	N2
LCDDO22	N3	LCDDO23	N4	LCDTMG0	U2
LCDTMG1	U3	LCDTMG2	V1	LCDTMG3	V2
LPVDD	J3	LPVDDR	J4	LPVSS	J2
LPVSSR	F2	LPVSSR	M4	LTGIO0	T2
LTGIO1	T3	LTGIO2	T4	MA0	W6
MA1	Y6	MA2	V7	MA3	W7
MA4	Y7	MA5	U8	MA6	V8
MA7	W8	MA8	Y8	MA9	V9
MD0	V11	MD1	Y12	MD2	W12
MD3	V12	MD4	U12	MD5	Y13
MD6	W13	MD7	V13	MD8	Y14
MD9	W14	MD10	V14	MD11	U14
MD12	Y15	MD13	W15	MD14	V15
MD15	U15	MD16	Y16	MD17	W16
MD18	V16	MD19	U16	MD20	Y17

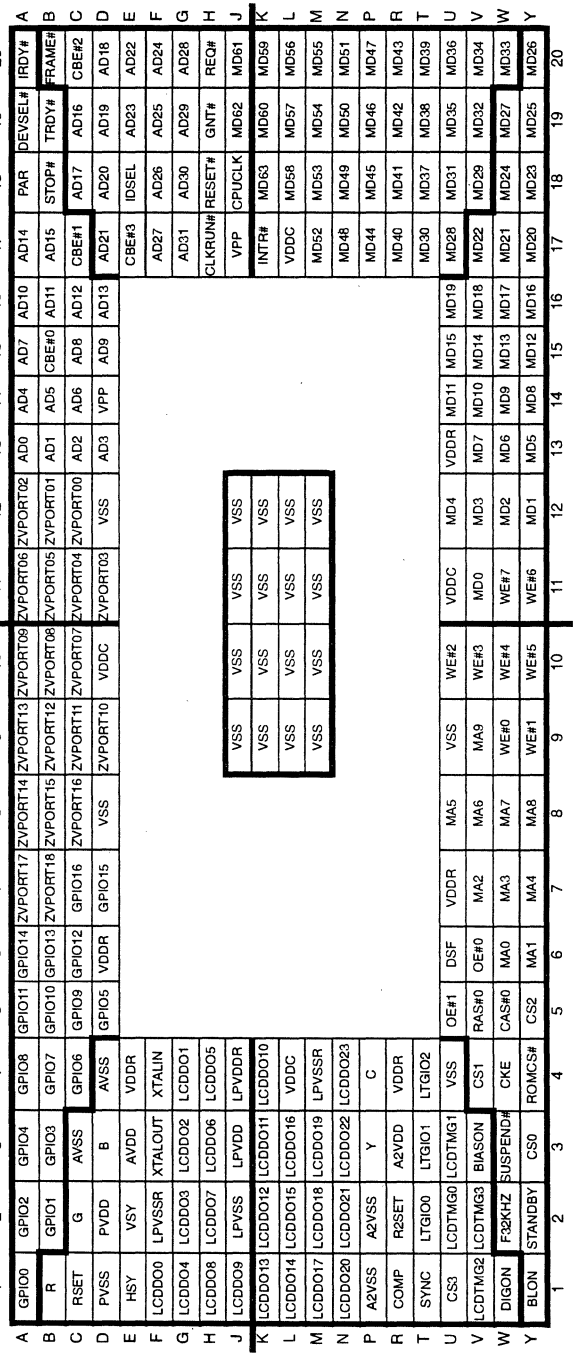
Table 6-33 256 BGA Pinout by Signal Name (Continued)

Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.
MD21	W17	MD22	V17	MD23	Y18
MD24	W18	MD25	Y19	MD26	Y20
MD27	W19	MD28	U17	MD29	V18
MD30	T17	MD31	U18	MD32	V19
MD33	W20	MD34	V20	MD35	U19
MD36	U20	MD37	T18	MD38	T19
MD39	T20	MD40	R17	MD41	R18
MD42	R19	MD43	R20	MD44	P17
MD45	P18	MD46	P19	MD47	P20
MD48	N17	MD49	N18	MD50	N19
MD51	N20	MD52	M17	MD53	M18
MD54	M19	MD55	M20	MD56	L20
MD57	L19	MD58	L18	MD59	K20
MD60	K19	MD61	J20	MD62	J19
MD63	K18	OE#0	V6	OE#1	U5
PAR	A18	PVDD	D2	PVSS	D1
R	B1	R2SET	R2	RAS#0	V5
REQ#	H20	RESET#	H18	ROMCS#	Y4
RSET	C1	STANDBY#	Y2	STOP#	B18
SUSPEND#	W3	SYNC	T1	TRDY#	B19
VDDC	D10	VDDC	L4	VDDC	L17
VDDC	U11	VDDR	D6	VDDR	E4
VDDR	R4	VDDR	U7	VDDR	U13
VPP	D14	VPP	J17	VSS	D8
VSS	D12	VSS	J9	VSS	J10
VSS	J11	VSS	J12	VSS	K9
VSS	K10	VSS	K11	VSS	K12
VSS	L9	VSS	L10	VSS	L11
VSS	L12	VSS	M9	VSS	M10
VSS	M11	VSS	M12	VSS	U4
VSS	U9	VSY	E2	WE#0	W9
WE#1	Y9	WE#2	U10	WE#3	V10
WE#4	W10	WE#5	Y10	WE#6	Y11
WE#7	W11	XTALIN	F4	XTALOUT	F3
Y	P3	ZVPORT00	C12	ZVPORT01	B12

Table 6-33 256 BGA Pinout by Signal Name (Continued)

Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.
ZVPORT02	A12	ZVPORT03	D11	ZVPORT04	C11
ZVPORT05	B11	ZVPORT06	A11	ZVPORT07	C10
ZVPORT08	B10	ZVPORT09	A10	ZVPORT10	D9
ZVPORT11	C9	ZVPORT12	B9	ZVPORT13	A9
ZVPORT14	A8	ZVPORT15	B8	ZVPORT16	C8
ZVPORT17	A7	ZVPORT18	B7		

6.15.3 Ball vs Signal Assignment



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GPIO0	GPIO2	GPIO4	GPIO8	GPIO11	GPIO14	ZVPORT17	ZVPORT14	ZVPORT13	ZVPORT09	ZVPORT06	ZVPORT02	AD0	AD4	AD7	AD10	AD14	PAR	DEVSEL#	IRDY#	A
B	R	GPIO1	GPIO3	GPIO7	GPIO10	GPIO13	ZVPORT18	ZVPORT15	ZVPORT12	ZVPORT08	ZVPORT05	ZVPORT01	AD1	AD5	CBE#0	AD11	AD15	STOP#	TRDY#	FRAME#	B
C	RSET	G	AVSS	GPIO6	GPIO9	GPIO12	GPIO16	ZVPORT16	ZVPORT11	ZVPORT07	ZVPORT04	ZVPORT00	AD2	AD6	AD8	AD12	CBE#1	AD17	AD16	CBE#2	C
D	PVSS	PVDD	B	AVSS	GPIO5	VDDR	GPIO15	VSS	ZVPORT10	VDDC	ZVPORT03	VSS	AD3	VPP	AD9	AD13	AD21	AD20	AD19	AD18	D
E	HSY	VSY	AVDD	VDDR													CBE#3	IDSEL	AD23	AD22	E
F	LCDDO0	LPVSSR	XTALOUT	XTALIN													AD27	AD26	AD25	AD24	F
G	LCDDO4	LCDDO3	LCDDO2	LCDDO1													AD31	AD30	AD29	AD28	G
H	LCDDO8	LCDDO7	LCDDO6	LCDDO5													CLKRUN#	RESET#	GNT#	REQ#	H
J	LCDDO9	LPVSS	LPVDD	LPVDDR													VPP	CPUCLK	MD62	MD61	J
K	LCDDO13	LCDDO12	LCDDO11	LCDDO10					VSS	VSS	VSS	VSS					INTR#	MD63	MD60	MD59	K
L	LCDDO14	LCDDO15	LCDDO16	VDDC					VSS	VSS	VSS	VSS					VDDC	MD58	MD57	MD56	L
M	LCDDO17	LCDDO18	LCDDO19	LPVSSR					VSS	VSS	VSS	VSS					MD52	MD53	MD54	MD55	M
N	LCDDO20	LCDDO21	LCDDO22	LCDDO23													MD48	MD49	MD50	MD51	N
P	A2VSS	A2VSS	Y	C													MD44	MD45	MD46	MD47	P
R	COMP	R2SET	A2VDD	VDDR													MD40	MD41	MD42	MD43	R
T	SYNC	LTGIO0	LTGIO1	LTGIO2													MD30	MD37	MD38	MD39	T
U	CS3	LCDTMG0	LCDTMG1	VSS	OE#1	DSF	VDDR	MA5	VSS	WE#2	VDDC	MD4	VDDR	MD11	MD15	MD19	MD28	MD31	MD35	MD36	U
V	LCDTMG2	LCDTMG2	LCDTMG3	BIASON	CS1	RAS#0	OE#0	MA2	MA6	MA9	WE#3	MD0	MD3	MD7	MD10	MD14	MD18	MD22	MD29	MD32	MD34	V
W	DIGON	F32KHZ	SUSPEND#	CKE	CAS#0	MA0	MA3	MA7	WE#0	WE#4	WE#7	MD2	MD6	MD9	MD13	MD17	MD21	MD24	MD27	MD33	W
Y	BLON	STANDBY	CS0	ROMCS#	CS2	MA1	MA4	MA8	WE#1	WE#5	WE#6	MD1	MD5	MD8	MD12	MD16	MD20	MD23	MD25	MD26	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 6-3. 256 + 16 Ball Plastic Ball Grid Array - Top View

6.16 312-pin BGA Pin Listings

6.16.1 Pinout by Ball Reference

Table 6-34 312 BGA Pinout by Ball Reference

Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name
A1	GPIO0	A2	GPIO1	A3	GPIO3
A4	GPIO5	A5	GPIO8	A6	GPIO13
A7	ZVPORT17	A8	ZVPORT12	A9	ZVPORT08
A10	ZVPORT04	A11	AD1	A12	AD5
A13	AD8	A14	AD12	A15	SBA7
A16	PAR	A17	SBA2	A18	AD13
A19	SBA0	A20	IRDY#	B1	B
B2	GPIO2	B3	GPIO4	B4	GPIO6
B5	GPIO9	B6	GPIO14	B7	ZVPORT16
B8	ZVPORT11	B9	ZVPORT07	B10	ZVPORT03
B11	AD0	B12	AD6	B13	CBE0#
B14	AD15	B15	AGP_BUSY#	B16	SBA5
B17	STOP#	B18	SBA1	B19	TRDY#
B20	AD21	C1	PVDD	C2	G
C3	R	C4	GPIO7	C5	GPIO10
C6	GPIO15	C7	ZVPORT15	C8	ZVPORT10
C9	ZVPORT06	C10	ZVPORT02	C11	AD2
C12	AD4	C13	AD_ST#0	C14	AD10
C15	STP_AGP#	C16	SBA6	C17	SBA3
C18	CBE3#	C19	AD17	C20	SB_STB
D1	XTALOUT	D2	AVDD	D3	RSET
D4	AVSS	D5	GPIO11	D6	GPIO16
D7	ZVPORT14	D8	ZVPORT09	D9	ZVPORT05
D10	ZVPORT01	D11	ZVPORT00	D12	AD3
D13	AD7	D14	AD11	D15	AD14
D16	DEVSEL#	D17	AD27	D18	AD16
D19	FRAME#	D20	AD20	E1	LCDDO3
E2	XTALIN	E3	HSY	E4	AVSS
E5	GPIO12	E6	ZVPORT18	E7	ZVPORT13
E8	VDDR	E9	VSS	E10	VDDC
E11	VPP	E12	VSS	E13	VPP

Table 6-34 312 BGA Pinout by Ball Reference (Continued)

Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name
E14	AD9	E15	CBE1#	E16	SBA4
E17	AD18	E18	AD19	E19	IDSEL
E20	CBE2#	F1	LCDDO4	F2	LCDDO2
F3	LCDDO1	F4	VSY	F5	PVSS
F6	VDDR	F7	VSS	F14	VPP
F15	VSS	F16	AD31	F17	AD_ST#1
F18	AD22	F19	AD23	F20	AD26
G1	LCDDO7	G2	LCDDO6	G3	LCDDO5
G4	LCDDO0	G5	LPVSSR	G6	VSS
G15	VPP	G16	AD29	G17	RESET#
G18	AD24	G19	AD25	G20	AD30
H1	LCDDO8	H2	LCDDO9	H3	LPVDDR
H4	LPVDD	H5	VDDR	H6	VDDC
H16	ST0	H17	ST1	H18	RBF#
H19	CLKRUN#	H20	ST2	J1	LCDDO12
J2	LCDDO11	J3	LCDDO10	J4	LPVSS
J5	VSS	J9	VSS	J10	VSS
J11	VSS	J12	VSS	J16	VPP
J17	REQ#	J18	GNT#	J19	CPUCLK
J20	AD28	K1	LCDDO16	K2	LCDDO15
K3	LCDDO14	K4	LCDDO13	K5	VDDC
K9	VSS	K10	VSS	K11	VSS
K12	VSS	K16	INTR#	K17	PAVDD
K18	PAVSS	K19	MD63	K20	MD62
L1	LCDDO17	L2	LCDDO18	L3	LCDDO19
L4	LCDDO20	L5	LPVSSR	L9	VSS
L10	VSS	L11	VSS	L12	VSS
L16	VDDC	L17	MD61	L18	MD60
L19	MD59	L20	MD58	M1	LCDDO21
M2	LCDDO22	M3	LCDDO23	M4	A2VSS
M5	A2VSS	M9	VSS	M10	VSS
M11	VSS	M12	VSS	M16	NC/R
M17	MD57	M18	MD56	M19	MD55
M20	MD54	N1	Y	N2	C
N3	COMP	N4	R2SET	N5	VDDR

Table 6-34 312 BGA Pinout by Ball Reference (Continued)

Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name
N16	MD49	N17	MD53	N18	MD52
N19	MD51	N20	MD50	P1	A2VDD
P2	SYNC	P3	LCDDO24	P4	LCDDO25
P5	NC/R	P6	VDDR	P15	VDDR
P16	NC/R	P17	MD48	P18	MD47
P19	MD46	P20	MD45	R1	LCDDO26
R2	LCDDO27	R3	LCDDO28	R4	LCDD029
R5	LCDDO30	R6	NC/R	R7	VSS
R15	NC/R	R16	MD40	R17	MD44
R18	MD43	R19	MD42	R20	MD41
T1	LCDDO31	T2	LCDDO32	T3	LCDDO33
T4	LCDDO34	T5	VSS	T6	MA0
T7	VDDR	T8	NC/R	T9	VDDR
T10	VDDC	T11	NC/R	T12	VDDR
T13	NC/R	T14	VDDR	T15	VSS
T16	NC/R	T17	MD39	T18	MD38
T19	MD37	T20	MD36	U1	LCDDO35
U2	CS3	U3	LCDTMG0	U4	LCDTMG1
U5	RAS#	U6	NC/R	U7	MA4
U8	VSS	U9	WE#1	U10	WE#5
U11	VDDC	U12	MD01	U13	VSS
U14	MD08	U15	MD12	U16	MD16
U17	MD35	U18	MD34	U19	MD33
U20	MD32	V1	LCDTMG2	V2	LCDTMG3
V3	DIGON	V4	PCI33EN	V5	DSF
V6	OE#0	V7	MA3	V8	MA7
V9	WE#0	V10	WE#4	V11	WE#6
V12	MD02	V13	MD05	V14	MD09
V15	MD13	V16	MD17	V17	MD20
V18	MD30	V19	MD29	V20	MD31
W1	BIASON	W2	F32KHZ	W3	CS0
W4	OE#1	W5	ROMCS#	W6	CS2
W7	MA2	W8	MA6	W9	MA9
W10	WE#3	W11	WE#7	W12	MD03
W13	MD06	W14	MD10	W15	MD14

Table 6-34 312 BGA Pinout by Ball Reference (Continued)

Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name
W16	MD18	W17	MD21	W18	MD23
W19	MD25	W20	MD28	Y1	BLON
Y2	STANDBY#	Y3	SUSPEND#	Y4	CS1
Y5	CKE	Y6	CAS#	Y7	MA1
Y8	MA5	Y9	MA8	Y10	WE#2
Y11	MD00	Y12	MD04	Y13	MD07
Y14	MD11	Y15	MD15	Y16	MD19
Y17	MD22	Y18	MD24	Y19	MD26
Y20	MD27				

Note: NC/R is "no connect but reserved for future use.

6.16.2 Pinout by Signal Name

Table 6-35 312 BGA Pinout by Signal Name

Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.
A2VDD	P1	A2VSS	M4	A2VSS	M5
AD_ST#0	C13	AD_ST#1	F17	AD0	B11
AD1	A11	AD2	C11	AD3	D12
AD4	C12	AD5	A12	AD6	B12
AD7	D13	AD8	A13	AD9	E14
AD10	C14	AD11	D14	AD12	A14
AD13	A18	AD14	D15	AD15	B14
AD16	D18	AD17	C19	AD18	E17
AD19	E18	AD20	D20	AD21	B20
AD22	F18	AD23	F19	AD24	G18
AD25	G19	AD26	F20	AD27	D17
AD28	J20	AD29	G16	AD30	G20
AD31	F16	AGP_BUSY#	B15	AVDD	D2
AVSS	D4	AVSS	E4	B	B1
BIASON	W1	BLON	Y1	C	N2
CAS#	Y6	CBE0#	B13	CBE1#	E15
CBE2#	E20	CBE3#	C18	CKE	Y5
CLKRUN#	H19	COMP	N3	CPUCLK	J19

Table 6-35 312 BGA Pinout by Signal Name (Continued)

Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.
CS0	W3	CS1	Y4	CS2	W6
CS3	U2	DEVSEL#	D16	DIGON	V3
DSF	V5	F32KHZ	W2	FRAME#	D19
G	C2	GNT#	J18	GPIO0	A1
GPIO1	A2	GPIO2	B2	GPIO3	A3
GPIO4	B3	GPIO5	A4	GPIO6	B4
GPIO7	C4	GPIO8	A5	GPIO9	B5
GPIO10	C5	GPIO11	D5	GPIO12	E5
GPIO13	A6	GPIO14	B6	GPIO15	C6
GPIO16	D6	HSY	E3	IDSEL	E19
INTR#	K16	IRDY#	A20	LCDD029	R4
LCDDO0	G4	LCDDO1	F3	LCDDO2	F2
LCDDO3	E1	LCDDO4	F1	LCDDO5	G3
LCDDO6	G2	LCDDO7	G1	LCDDO8	H1
LCDDO9	H2	LCDDO10	J3	LCDDO11	J2
LCDDO12	J1	LCDDO13	K4	LCDDO14	K3
LCDDO15	K2	LCDDO16	K1	LCDDO17	L1
LCDDO18	L2	LCDDO19	L3	LCDDO20	L4
LCDDO21	M1	LCDDO22	M2	LCDDO23	M3
LCDDO24	P3	LCDDO25	P4	LCDDO26	R1
LCDDO27	R2	LCDDO28	R3	LCDDO30	R5
LCDDO31	T1	LCDDO32	T2	LCDDO33	T3
LCDDO34	T4	LCDDO35	U1	LCDTMG0	U3
LCDTMG1	U4	LCDTMG2	V1	LCDTMG3	V2
LPVDD	H4	LPVDDR	H3	LPVSS	J4
LPVSSR	G5	LPVSSR	L5	MA0	T6
MA1	Y7	MA2	W7	MA3	V7
MA4	U7	MA5	Y8	MA6	W8
MA7	V8	MA8	Y9	MA9	W9
MD00	Y11	MD01	U12	MD02	V12
MD03	W12	MD04	Y12	MD05	V13
MD06	W13	MD07	Y13	MD08	U14
MD09	V14	MD10	W14	MD11	Y14
MD12	U15	MD13	V15	MD14	W15
MD15	Y15	MD16	U16	MD17	V16

Table 6-35 312 BGA Pinout by Signal Name (Continued)

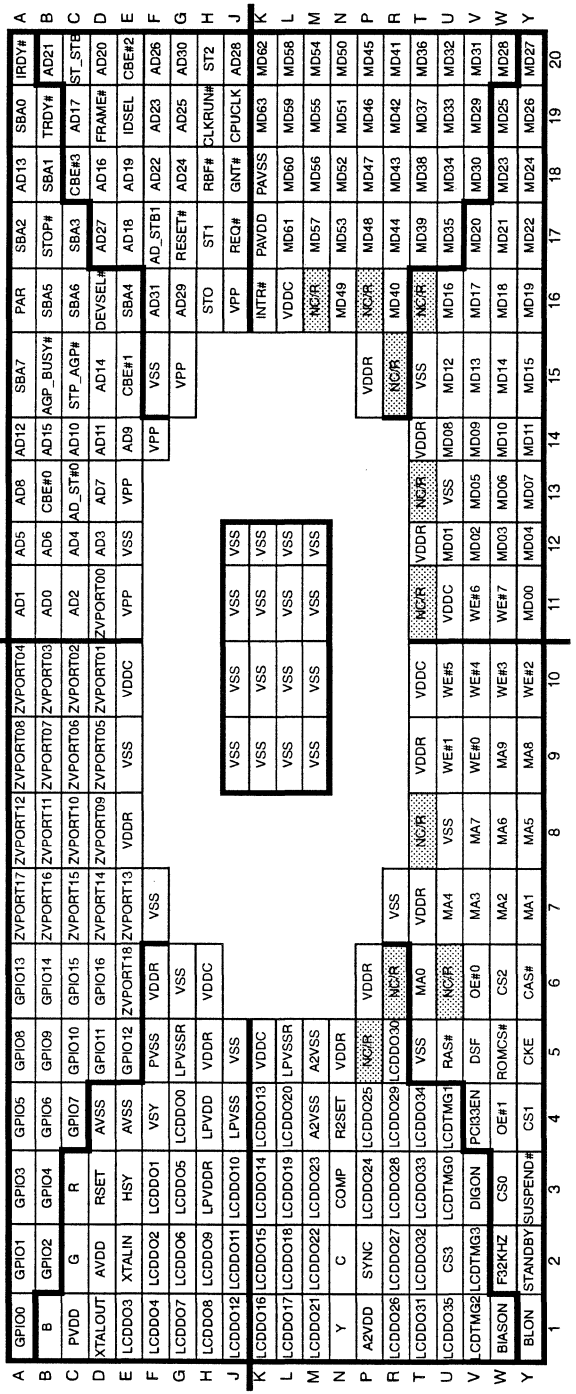
Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.
MD18	W16	MD19	Y16	MD20	V17
MD21	W17	MD22	Y17	MD23	W18
MD24	Y18	MD25	W19	MD26	Y19
MD27	Y20	MD28	W20	MD29	V19
MD30	V18	MD31	V20	MD32	U20
MD33	U19	MD34	U18	MD35	U17
MD36	T20	MD37	T19	MD38	T18
MD39	T17	MD40	R16	MD41	R20
MD42	R19	MD43	R18	MD44	R17
MD45	P20	MD46	P19	MD47	P18
MD48	P17	MD49	N16	MD50	N20
MD51	N19	MD52	N18	MD53	N17
MD54	M20	MD55	M19	MD56	M18
MD57	M17	MD58	L20	MD59	L19
MD60	L18	MD61	L17	MD62	K20
MD63	K19	NC/R	M16	NC/R	P5
NC/R	P16	NC/R	R6	NC/R	R15
NC/R	T8	NC/R	T11	NC/R	T13
NC/R	T16	NC/R	U6	OE#0	V6
OE#1	W4	PAR	A16	PAVDD	K17
PAVSS	K18	PCI33EN	V4	PVDD	C1
PVSS	F5	R	C3	R2SET	N4
RAS#	U5	RBF#	H18	REQ#	J17
RESET#	G17	ROMCS#	W5	RSET	D3
SB_STB	C20	SBA0	A19	SBA1	B18
SBA2	A17	SBA3	C17	SBA4	E16
SBA5	B16	SBA6	C16	SBA7	A15
ST0	H16	ST1	H17	ST2	H20
STANDBY#	Y2	STOP#	B17	STP_AGP#	C15
SUSPEND#	Y3	SYNC	P2	TRDY#	B19
VDDC	E10	VDDC	H6	VDDC	K5
VDDC	L16	VDDC	T10	VDDC	U11
VDDR	E8	VDDR	F6	VDDR	H5
VDDR	N5	VDDR	P6	VDDR	P15
VDDR	T7	VDDR	T9	VDDR	T12

Table 6-35 312 BGA Pinout by Signal Name (Continued)

Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.
VDDR	T14	VPP	E11	VPP	E13
VPP	F14	VPP	G15	VPP	J16
VSS	E9	VSS	E12	VSS	F7
VSS	F15	VSS	G6	VSS	J5
VSS	J9	VSS	J10	VSS	J11
VSS	J12	VSS	K9	VSS	K10
VSS	K11	VSS	K12	VSS	L9
VSS	L10	VSS	L11	VSS	L12
VSS	M9	VSS	M10	VSS	M11
VSS	M12	VSS	R7	VSS	T5
VSS	T15	VSS	U8	VSS	U13
VSY	F4	WE#0	V9	WE#1	U9
WE#2	Y10	WE#3	W10	WE#4	V10
WE#5	U10	WE#6	V11	WE#7	W11
XTALIN	E2	XTALOUT	D1	Y	N1
ZVPORT00	D11	ZVPORT01	D10	ZVPORT02	C10
ZVPORT03	B10	ZVPORT04	A10	ZVPORT05	D9
ZVPORT06	C9	ZVPORT07	B9	ZVPORT08	A9
ZVPORT09	D8	ZVPORT10	C8	ZVPORT11	B8
ZVPORT12	A8	ZVPORT13	E7	ZVPORT14	D7
ZVPORT15	C7	ZVPORT16	B7	ZVPORT17	A7
ZVPORT18	E6				

Note: NC/R is "no connect but reserved for future use".

6.16.3 Ball vs Signal Assignment



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GPIO0	GPIO1	GPIO3	GPIO5	GPIO8	GPIO13	ZVPORT17	ZVPORT12	ZVPORT08	ZVPORT04	AD1	AD5	AD8	AD12	SBA7	PAR	SBA2	AD13	SBA0	IRDY#	A
B	B	GPIO2	GPIO4	GPIO6	GPIO9	GPIO14	ZVPORT16	ZVPORT11	ZVPORT07	ZVPORT03	AD0	AD6	CBE#0	AD15	AGP_BUSY#	SBA5	STOP#	SBA1	TRDY#	AD21	B
C	PVDD	G	R	GPIO7	GPIO10	GPIO15	ZVPORT15	ZVPORT10	ZVPORT06	ZVPORT02	AD2	AD4	AD_ST#0	AD10	STP_AGP#	SBA6	SBA3	CBE#3	AD17	ST_STB	C
D	XTALOUT	AVDD	RSET	AVSS	GPIO11	GPIO16	ZVPORT14	ZVPORT09	ZVPORT05	ZVPORT01	ZVPORT00	AD3	AD7	AD11	AD14	DEVSEL#	AD27	AD16	FRAME#	AD20	D
E	LCDDO3	XTALIN	HSY	AVSS	GPIO12	ZVPORT18	ZVPORT13	VDDR	VSS	VDDC	VPP	VSS	VPP	AD9	CBE#1	SBA4	AD18	AD19	IDSEL	CBE#2	E
F	LCDDO4	LCDDO2	LCDDO1	VSY	PVSS	VDDR	VSS							VPP	VSS	AD31	AD_STB1	AD22	AD23	AD26	F
G	LCDDO7	LCDDO6	LCDDO5	LCDDO0	LPVSSR	VSS									VPP	AD29	RESET#	AD24	AD25	AD30	G
H	LCDDO8	LCDDO9	LPVDDR	LPVDD	VDDR	VDDC										STO	ST1	RBF#	CLKRUN#	ST2	H
J	LCDDO12	LCDDO11	LCDDO10	LPVSS	VSS											VPP	REQ#	GNT#	CPUCLK	AD28	J
K	LCDDO16	LCDDO15	LCDDO14	LCDDO13	VDDC				VSS	VSS	VSS	VSS				INTR#	PAVDD	PAVSS	MD63	MD62	K
L	LCDDO17	LCDDO18	LCDDO19	LCDDO20	LPVSSR				VSS	VSS	VSS	VSS				VDDC	MD61	MD60	MD59	MD58	L
M	LCDDO21	LCDDO22	LCDDO23	A2VSS	A2VSS				VSS	VSS	VSS	VSS				NC/R	MD57	MD56	MD55	MD54	M
N	Y	C	COMP	R2SET	VDDR											MD49	MD53	MD52	MD51	MD50	N
P	A2VDD	SYNC	LCDDO24	LCDDO25	NC/R	VDDR									VDDR	NC/R	MD48	MD47	MD46	MD45	P
R	LCDDO26	LCDDO27	LCDDO28	LCDDO29	LCDDO30	NC/R	VSS								NC/R	MD40	MD44	MD43	MD42	MD41	R
T	LCDDO31	LCDDO32	LCDDO33	LCDDO34	VSS	MA0	VDDR	NC/R	VDDR	VDDC	NC/R	VDDR	NC/R	VDDR	VSS	NC/R	MD39	MD38	MD37	MD36	T
U	LCDDO35	CS3	LCDTMG0	LCDTMG1	RAS#	NC/R	MA4	VSS	WE#1	WE#5	VDDC	MD01	VSS	MD08	MD12	MD16	MD35	MD34	MD33	MD32	U
V	LCDTMG2	LCDTMG3	DIGON	PCI33EN	DSF	OE#0	MA3	MA7	WE#0	WE#4	WE#6	MD02	MD05	MD09	MD13	MD17	MD20	MD30	MD29	MD31	V
W	BIASON	F32KHZ	CS0	OE#1	ROMCS#	CS2	MA2	MA6	MA9	WE#3	WE#7	MD03	MD06	MD10	MD14	MD18	MD21	MD23	MD25	MD28	W
Y	BLON	STANDBY	SUSPEND#	CS1	CKE	CAS#	MA1	MA5	MA8	WE#2	MD00	MD04	MD07	MD11	MD15	MD19	MD22	MD24	MD26	MD27	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Note: *NC/R* = "No Connect but Reserved" for future use.

Figure 6-4. 312 + 16 Ball Plastic Ball Grid Array - Top View

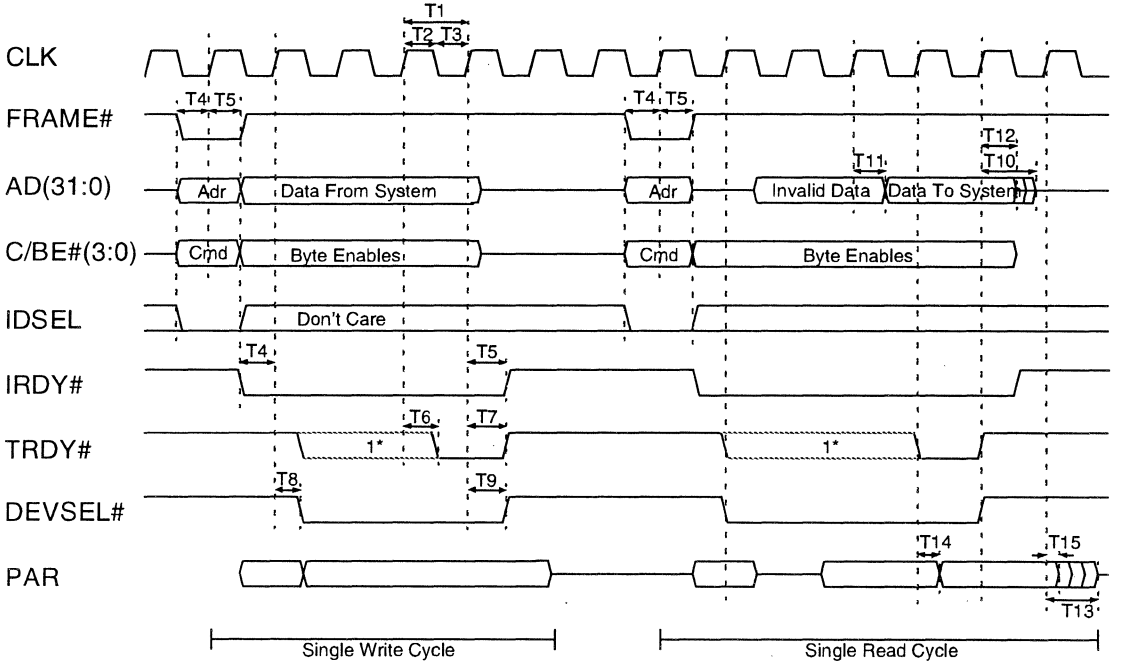
Chapter 7
Timing Specifications

7.1 Bus Timings

Timing specifications for PCI bus operations are given by:

- Single Read/Write Cycle Timing, see *Figure 7-1*.
- Disconnect On Burst Cycle, see *Figure 7-2*.
- Burst Access Timing, see *Figure 7-3*.
- PCI Bus Master Operation, *see Figure 7-4*.
- AGP AC Timing, see *Figure 7-5* and *Figure 7-6*.
- Power Up and Reset Timing, see *Figure 7-10*

7.1.1 Single Read/Write Cycle Timing



1* The minimum number of clocks from FRAME# active to TRDY# active is programmable.

Figure 7-1. Single Read/Write Cycle Timing - PCI Bus

7.1.2 Disconnect On Burst Cycle - PCI Bus

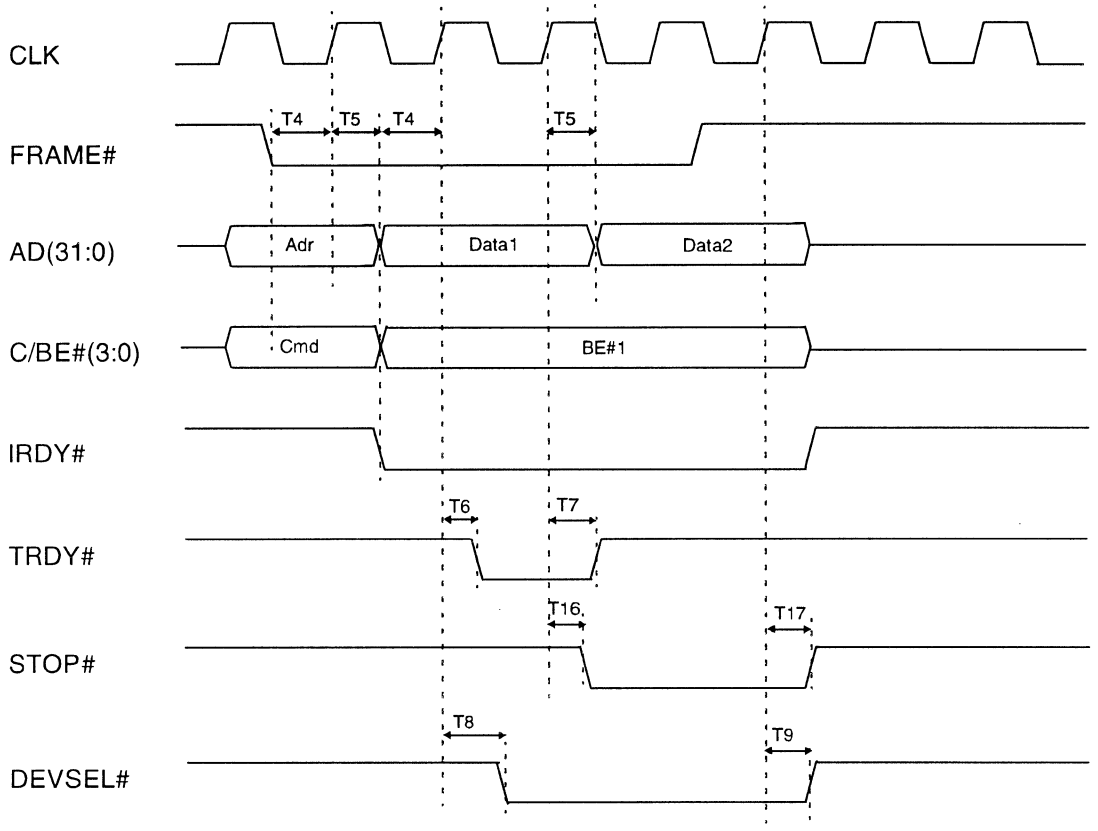


Figure 7-2. Disconnect On Burst Cycle - PCI Bus

7.1.3 Burst Access Timing - PCI

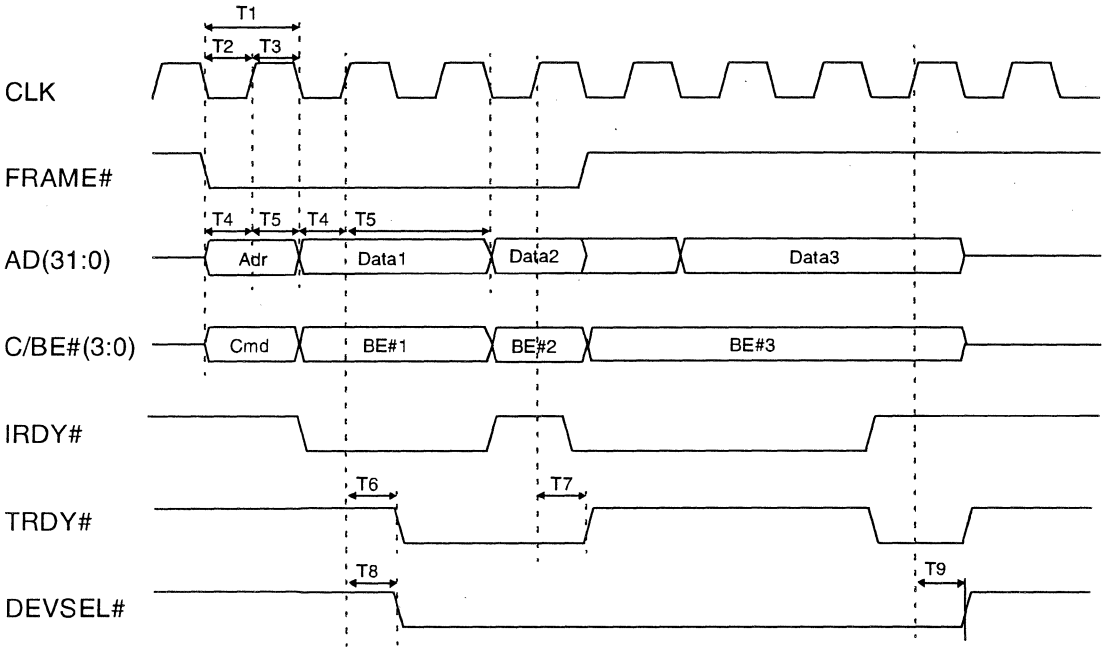


Figure 7-3. Burst Access Timing - PCI Bus

7.1.4 PCI Bus Master Operation

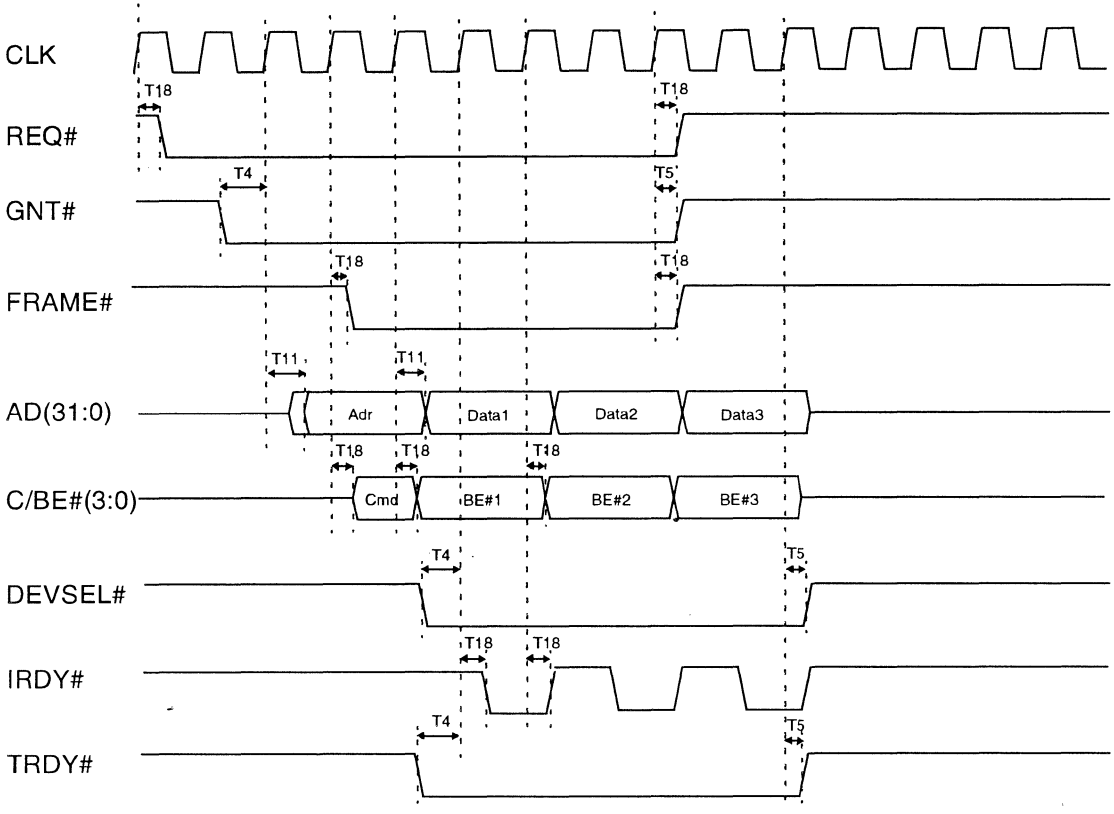


Figure 7-4. PCI Bus Master Operation

Table 7-1 PCI Bus Interface Timing Values

Symbol	Description	Min.(ns)	Max.(ns)
T1	Bus Clock Period	30	-
T2	Bus Clock High Time	12	-
T3	Bus Clock Low Time	12	-
T4	Bus Input Signal Setup to CLK[a]	7	-
T5	Bus Input Signal Hold from CLK[a]	0	-
T6	CLK to TRDY# active	2	11

Table 7-1 PCI Bus Interface Timing Values (Continued)

Symbol	Description	Min.(ns)	Max.(ns)
T7	CLK to TRDY# inactive	2	11
T8	CLK to DEVSEL# active	2	11
T9	CLK to DEVSEL# inactive	2	11
T10	CLK to data output tri-state	2	20
T11	CLK to data output valid delay (data stepping buffer)	2	20
T12	CLK to data output invalid delay	2	-
T13	CLK to PAR tri-state	2	20
T14	CLK to PAR valid delay (data stepping buffer)	2	20
T15	CLK to PAR invalid delay	2	-
T16	CLK to STOP# active delay	2	11
T17	CLK to STOP# inactive delay	2	11
T18	CLK to signal valid delay	2	11

a. Bus input signals include FRAME#, AD(31-0), IDSEL, IRDY#, TRDY#, GNT#, DEVSEL#.

7.1.5 AGP Timing

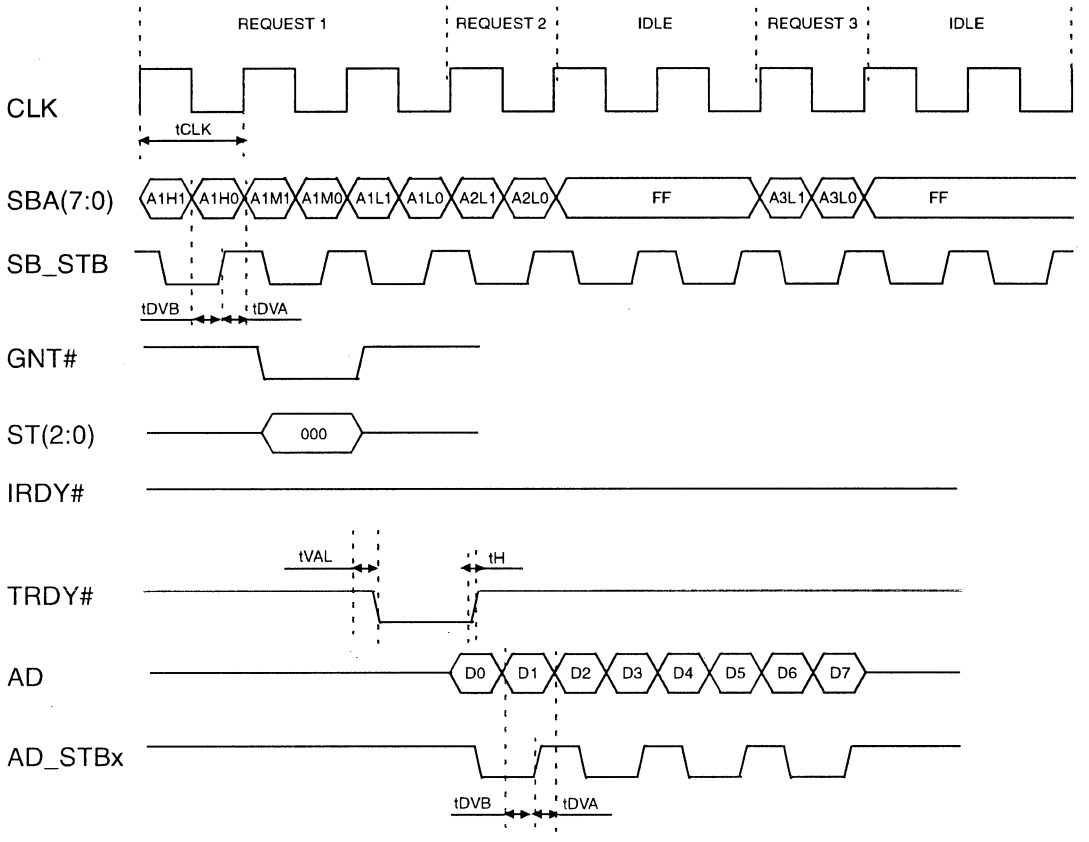


Figure 7-5. AGP 2X Read Request with Return Data (4Qw)

Table 7-2 AGP 2X Timing Parameters

Symbol	Description	Min.(ns)	Max.(ns)
tCLK	Clock	-	15
tDVB	Data valid before	1.7	
tDVA	Data valid after	1.7	-
tVAL	CLK to control signal and Data valid delay	1	5.5
tH	Control signals hold time to CLK	0	-

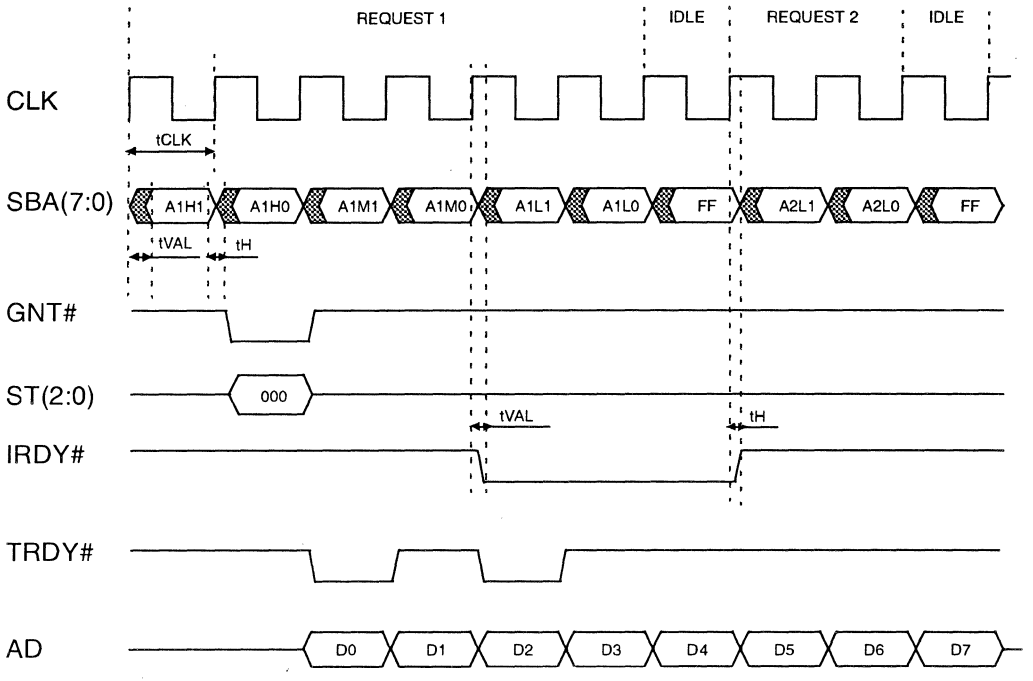


Figure 7-6. AGP 1X Read Request with Return Data (4Qw)

Table 7-3 AGP 1X Timing Parameters

Symbol	Description	Min.(ns)	Max.(ns)
tVAL	CLK to control signal and Data valid delay	1	5.5
tH	Control signals hold time to CLK	0	-

7.1.6 Mobile AGP/PCI Timing

For the mobile environment, three signals are used to maintain the clock and indicate its status. Two signals, **AGP_BUSYB** and **STP_AGPB**, are for the AGP bus, and a third one, **CLKRUNB**, is for the PCI bus.

- **AGP_BUSYB —** generated by the AGP graphic card device and goes to the southbridge. When asserted, it indicates the AGP device is currently busy and the AGP clock should not be stopped; when deasserted, it indicates the AGP device is not running any cycles and the AGP clock can be stopped.
- **STP_AGPB** — an input to the AGP device that indicates the status of the clock. When asserted, the AGP clock is stopped.

- **CLKRUNB** — a sustained tri-state input/output signal with respect to the central resource (clock generation logic), and an open drain output as well as an input with respect to the device. The central resource keeps CLKRUNB asserted when the clock is running normally, whereas, when the clock is stopped or slowed, the central resource monitors CLKRUNB to recognize requests from master and target devices for a change to be made in the state of the PCI clock signal.

  Output drive characteristics are defined by clocking role as follow:

  - **Master/Target** — "open drain" (i.e. low drive capability only), asynchronous.
  - **Central resource** — high and low drive capability, clock synchronous when driven to a high state, along with weak controllable keeper to maintain a high level during clock stop or slowdown.

  There are 3 main states in the clocking protocol:

  - **Clock running** — the clock is running and the bus is operational, with CLKRUNB asserted by the central resource.
  - **About to Stop/Slow** — the central resource deassertes CLKRUNB for one clock to inform the device that the clock is about to stop, then central resource tri-states its CLKRUNB output driver. The clock continues to run unchanged for a minimum of 4 clocks after CLKRUNB is deasserted. During this period of time, a master/target may reassert CLKRUNB for 2 clocks to request continued clock generation. When the central resource samples CLKRUNB reasserted, it will not stop the clock; otherwise, the clock will be stopped and the controllable keeper resistor will maintain the deasserted state of CLKRUNB during the period in which the clock is stopped or slowed.
  - **Clock Stopped/Slowed** — the central resource monitors CLKRUNB while the clock is stopped or slowed. The master may request use of the bus by asserting CLKRUNB for 2 clocks, then it may tri-state its CLKRUNB output driver. The central resource will turn on the clock and assert CLKRUNB.

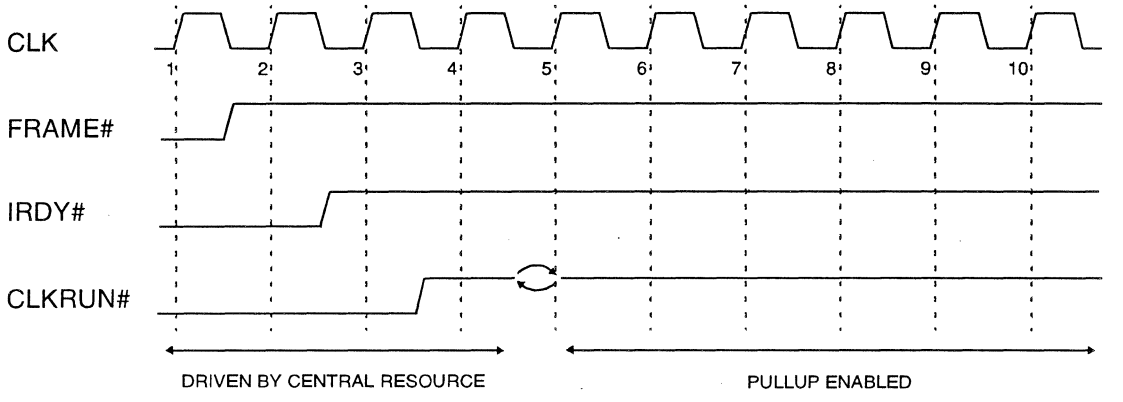


Figure 7-7. Clock Stop or Slow-down

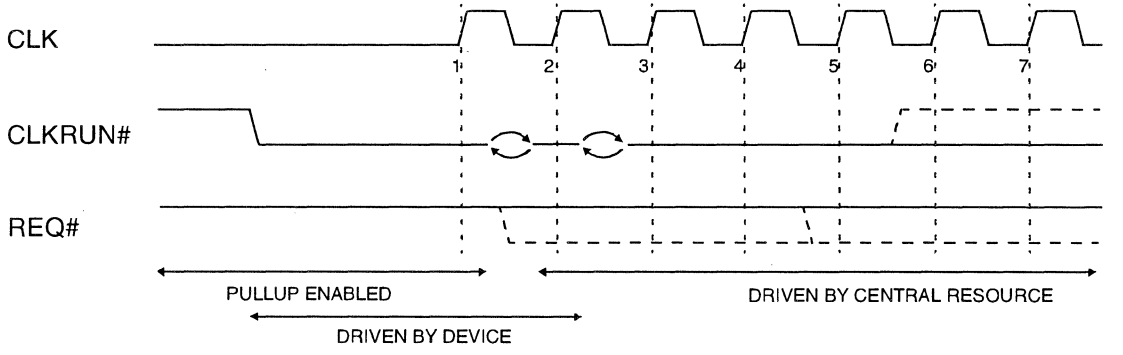


Figure 7-8. Clock Start or Speed-up

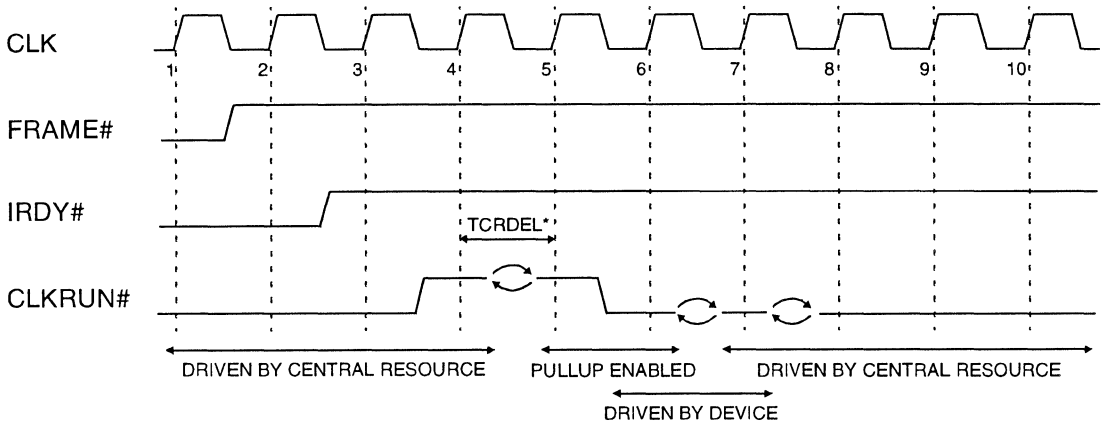


Figure 7-9. Maintaining Clock

*A more detailed description of the mobile environment and the CLKRUNB signal's role can be found in the document entitiled *PCI Mobile Design Guide.*

7.1.7 Power-up and Reset Timing

The assertion and deassertion of the **RST#** signal is asynchronous with respect to clock. After **RST#** is asserted, **PCI** components must asynchronously float their outputs. Meeting both T_rst and T_rst-clk will be considered as proper reset of the internal logic for start-up of the chip.

Table 7-4

Symbol	Parameter	Min	Max	Units
T_rst	Reset Active Time After Power Stable	1		ms
T_cyc	First Cycle after Reset	300		ns
T_rst-clk	Reset Active Time After CLK Stable	100		µs

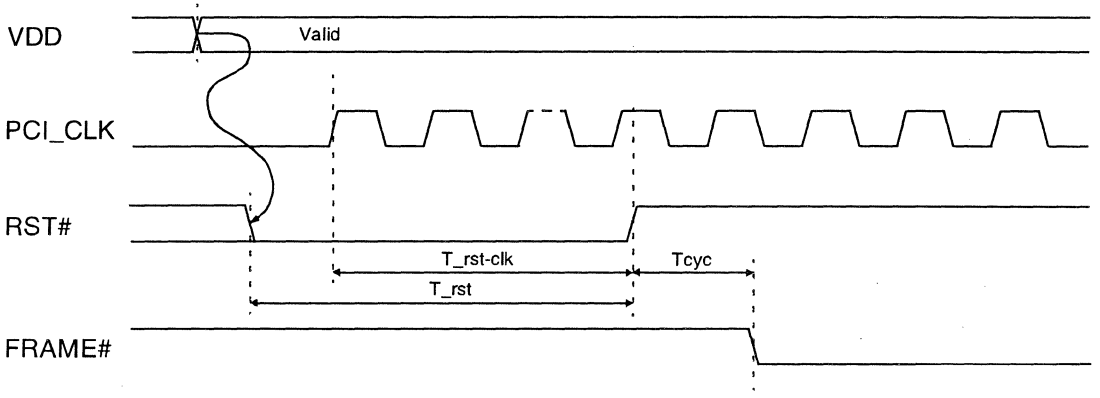


Figure 7-10. Reset Timing

7.2 Memory Timing

Timing specifications for DRAM and SDRAM memory operations are given by:

- DRAM / EDO DRAM Cycle Timing, see *Figure 7-11.*
- Hyperpage EDO DRAM Cycle Timing, see *Figure 7-12*
- Refresh Cycle Timing, see *Figure 7-13.*
- SDRAM/SGRAM Cycle Timing, see *Figure 7-14.*

7.2.1 DRAM / EDO DRAM Cycle Timing

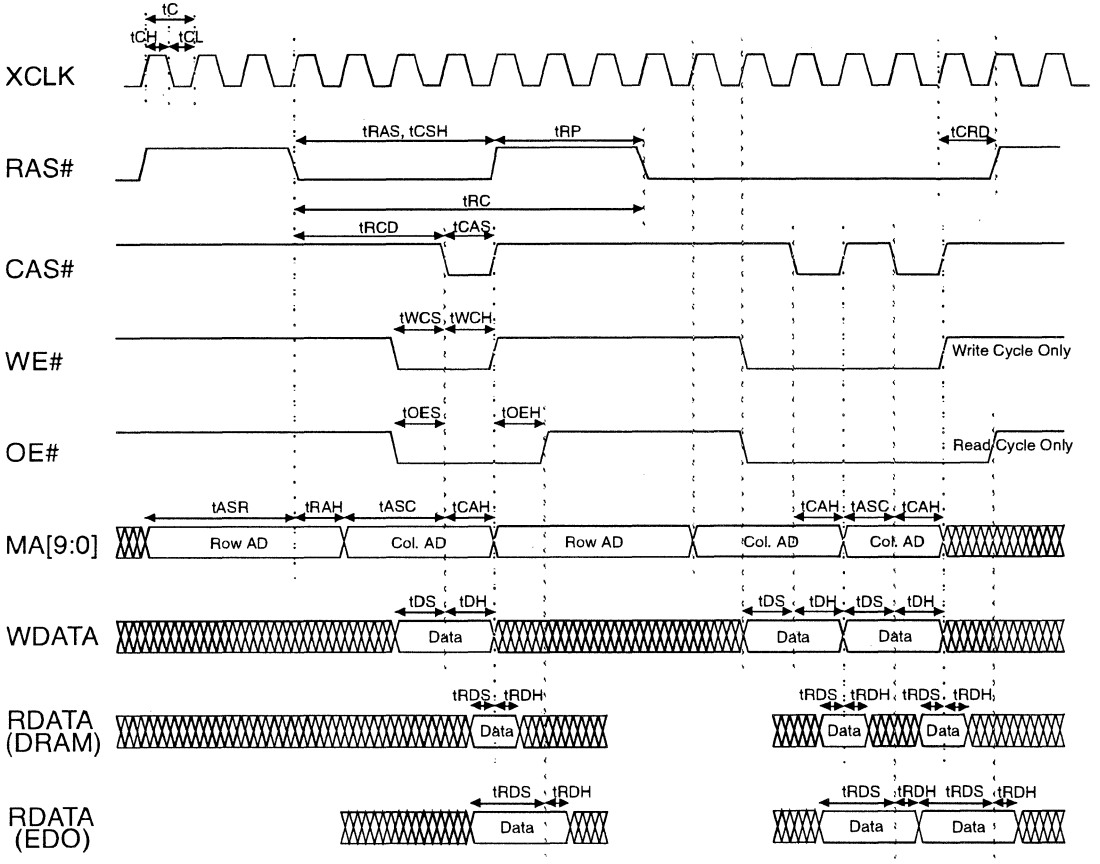


Figure 7-11. DRAM / EDO DRAM Cycle Timing

Table 7-5 DRAM / EDO DRAM Interface Cycle Timing Values

Memory Cycle Length	Symbol	Minimum (ns)	Maximum (ns)
Clock Period	tC	12	20
Clock High	tCH	4	-
Clock Low	tCL	4	-
Read Data Setup	tRDS	1	-
Read Data Hold	tRDH	3	-

DRAM / EDO DRAM Controller Values

Table 7-6 DRAM / EDO DRAM Cycle Timing Values

Memory Cycle Length	DRAM Spec.	Register Field in MEM_CNTL or Calc.	MEM_CNTL Bits	Number of XCLKs
Cycle time	tRC	tRP + tRAS		2 to 12
RAS precharge	tRP	MEM_TRP	[9:8]	1 to 4
RAS pulse	tRAS	MEM_TRAS	[18:16]	1 to 8
RAS to CAS (min.)	tRCD	MEM_TRCD	[11:10]	1 to 4
RAS high - CAS high	tCRD	MEM_TCRD	[12]	0 to 1
RAS - CAS high	tCSH	tRCD + 1		2 to 5
CAS Cycle (page mode)	tPC	-		2
CAS precharge	tCP	-		1
CAS pulse	tCAS	-		1
Row address hold	tRAH	-		1
CAS address hold	tCAH	-		1
Output enable setup	tOES	-		≥1
Output enable hold	tOEH	-		≥1
Write command setup	tWCS	-		≥1
Write command hold	tWCH	-		1
Row address setup	tASR	-		≥1
Column address setup	tASC	-		≥1
Write data setup	tDS	-		1
Write data hold	tDH	-		1

7.2.2 Hyperpage EDO DRAM Cycle Timing

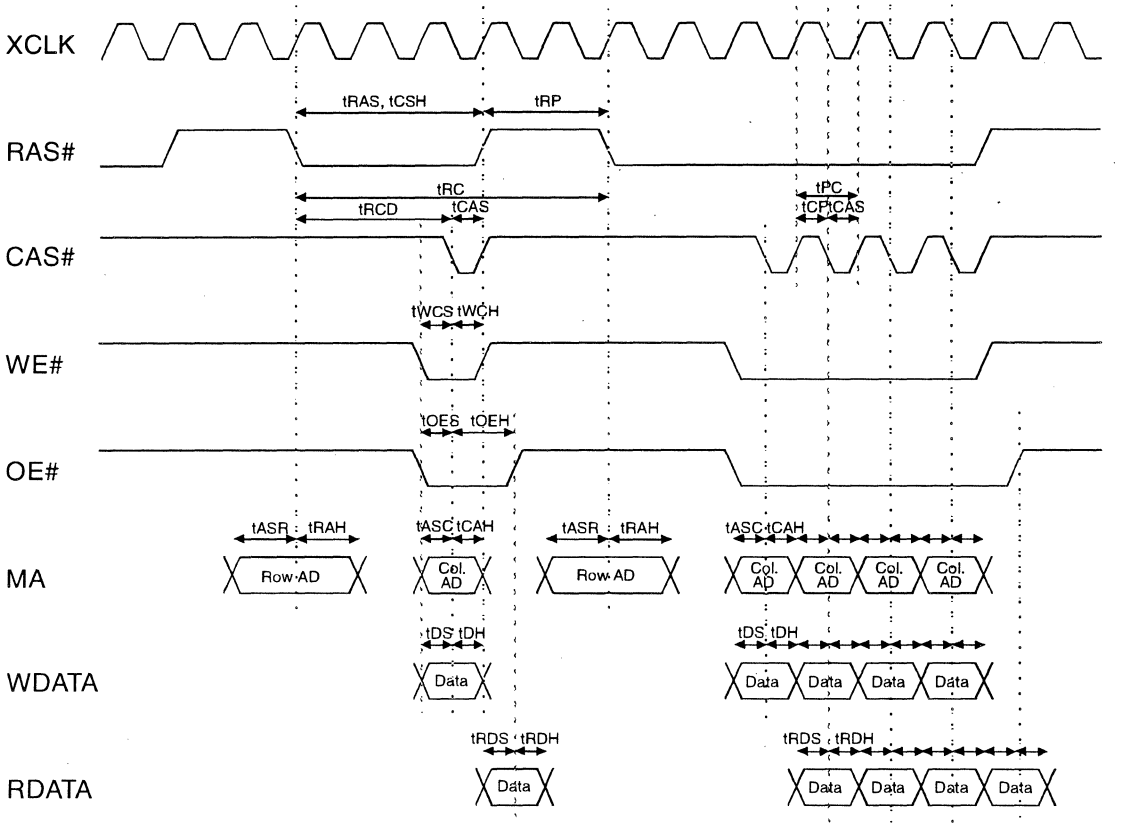


Figure 7-12. Hyperpage EDO DRAM Cycle Timing

Table 7-7 Hyperpage EDO DRAM Timing Values

Memory Cycle Length	DRAM Spec	Min. Time (ns)	Register Field in MEM_CNTL or Calc.	MEM_CNTL Bits
XCLK Period	tC	12		
Cycle time	tRC	2 tC to 12 tC	tRP + tRAS	
RAS precharge	tRP	1 tC to 4 tC	MEM_TRP	9:8
RAS pulse	tRAS	1 tC to 8 tC	MEM_TRAS	18:16
RAS to CAS (min.)	tRCD	1½ tC to 4½ tC	MEM_TRCD + ½	11:10
RAS high - CAS high	tCRD	0 to 1 tC	MEM_TCRD	12
RAS - CAS high	tCSH	2 tC to 5 tC	tRCD + ½	
CAS Cycle	tPC	1 tC	-	

Table 7-7 Hyperpage EDO DRAM Timing Values (Continued)

Memory Cycle Length	DRAM Spec	Min. Time (ns)	Register Field in MEM_CNTL or Calc.	MEM_CNTL Bits
CAS precharge	tCP	½ tC	-	
CAS pulse	tCAS	0.4 tC	-	
Row address hold	tRAH	1 tC	-	
CAS address hold	tCAH	0.4 tC	-	
Output enable setup	tOES	½ tC - 5.0	-	
Output enable hold	tOEH	1 tC	-	
Write command setup	tWCS	½ tC - 5.0	-	
Write command hold	tWCH	0.4 tC	-	
Row address setup	tASR	1 tC	-	
Column address setup	tASC	½ tC - 5.0	-	
Write data setup	tDS	½ tC - 5.0	-	
Write data hold	tDH	0.4 tC	-	

Notes:

- Worst case numbers (max. values) achieved assuming worst case process (setup time): 70 degrees C; 3.0 V; 40 pF on address lines; 28 pF on RAS, WE and OE lines; 14 pF on CAS and data lines.
- Best case numbers (min. values) achieved assuming best case process (hold time): 0 degrees C; 3.6 V; 20 pF on address lines; 28 pF on RAS, WE and OE lines; 7 pF on CAS and data lines.
- Hold and setup time values considered without taking into account transmission line effects of the address, control, and data lines.
- Timing values are provided assuming 1.4V transition level.

7.2.3 DRAM Refresh Cycle Timing

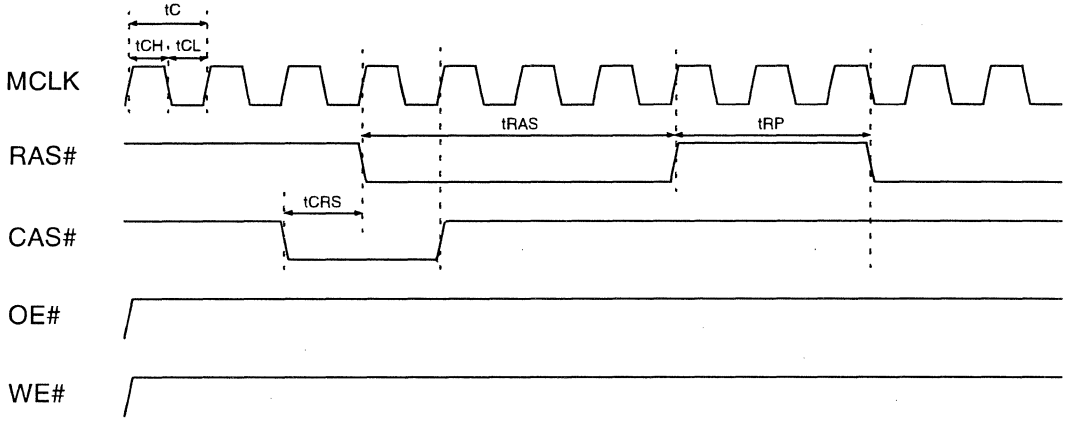


Figure 7-13. Refresh Cycle Timing

Table 7-8 Refresh Cycle Timing Values

Memory Cycle Length	DRAM Spec.	XCLKs (tC)	Register Field in MEM_CNTL or Calc.
Cycle Time	tRC	2 to 12	tRP + tRAS
RAS# precharge time	tRP	1 to 4	MEM_TRP[9:8]
RAS# pulse width	tRAS	1 to 8	MEM_TRAS[18:16]
CAS# to RAS# setup time	tCRS	1	-

7.2.4 SDRAM/SGRAM Cycle Timing

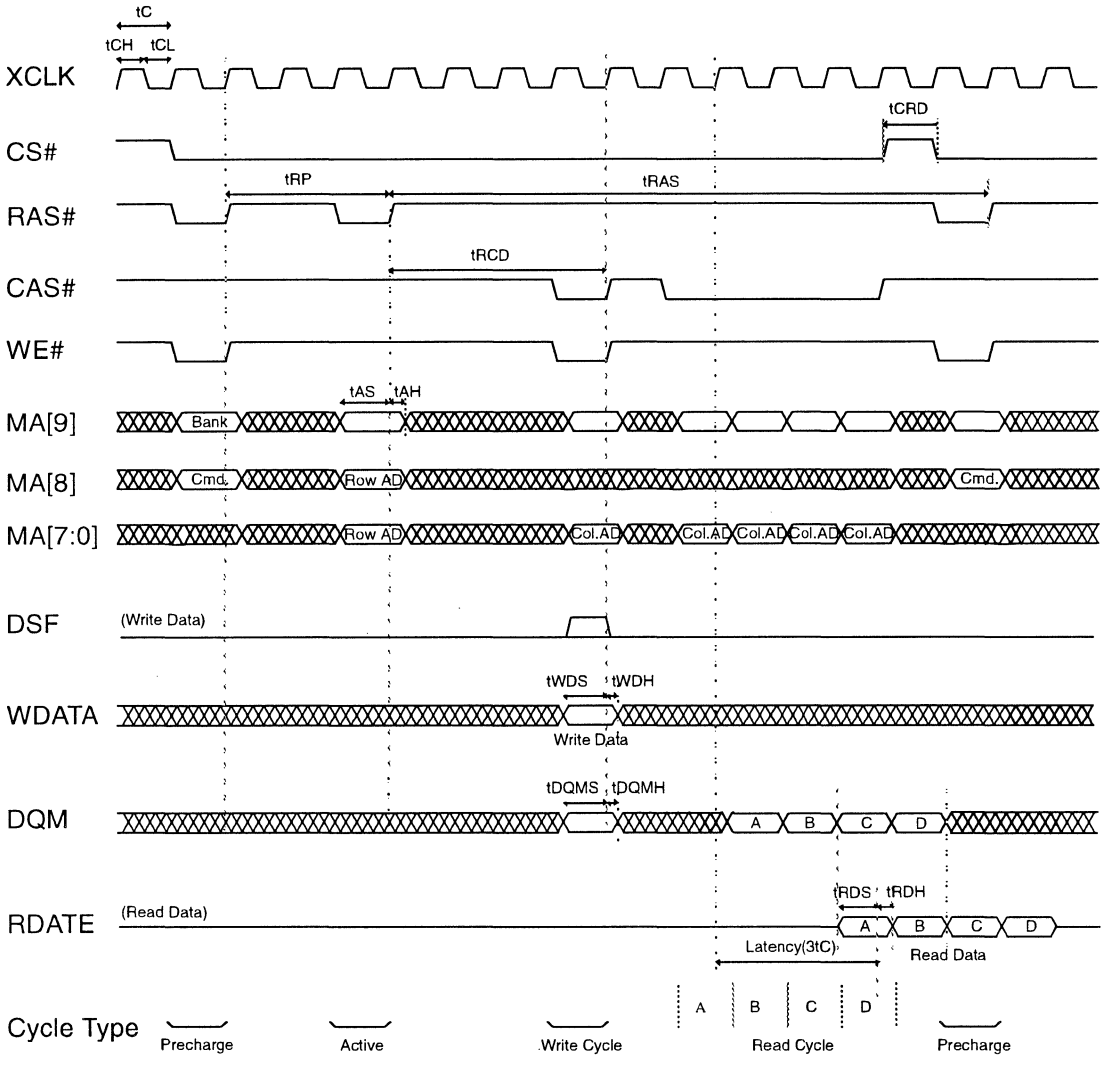


Figure 7-14. SDRAM / SGRAM Cycle Timing

Table 7-9 SDRAM/SGRAM Cycle Timing Values

Parameter	Symbol	Min. (ns)	Max. (ns)	Register in MEM_CNTL
Clock period	tC	10	20	
Clock high time	tCH	4.0	-	
Clock low time	tCL	3.5	-	
Command setup time provided (RAS, CAS, WE, CS, DSF)	tCMS	5.0	-	
Command hold time provided (RAS, CAS, WE, CS, DSF)	tCMH	1.3	-	
DQM setup time provided	tDQMS	5.5	-	
DQM hold time provided	tDQMH	1.2	-	
Address setup time provided	tAS	4.4	-	
Address hold time provided	tAH	1.3	-	
Write data setup time provided	tWDS	3.0	-	
Write data hold time provided	tWDH	2.1	-	
Read data setup time required	tRDS	-0.9	-	
Read data hold time required	tRDH	3.0	-	
Row cycle time	tRC	2 tC	12 tC	MEM_TRP + MEM_TRAS
PRE to ACTV delay	tRP	1 tC	4 tC	MEM_TRP[9:8]
ACTV to PRE min delay	tRAS	1 tC	8 tC	MEM_TRAS[18:16]
ACTV to CMD delay	tRCD	1 tC	4 tC	MEM_TRCD[11:10]
Write recovery time	tWR	1 tC	2 tC	MEM_TCRD[12] + 1
ACTV to ACTV delay	tRRD	2 tC	-	
Block write cycle time	tBWC	2 tC	-	

Notes:

- Worst case numbers (max. values) achieved assuming worst case process (setup time): 70 degrees C, 3.0 V, 45 pF on address and command lines, 30 pF on data and DQM lines.
- Best case number (min. values) achieved assuming best case process (hold time): 0 degrees C, 3.6 V, 5 pF on address and command lines, 3.5 pF on data and DQM lines.
- Hold and setup time values considered without taking into account transmission line effects of the clock, address, command, data and DQM lines.
- Timing values are provided assuming 1.4 V transition level.

7.3 Memory Controller Register Programming Examples

7.3.1 DRAM / EDO DRAM

Table 7-10 DRAM / EDO DRAM - Values for 15ns Clock Period (67 MHz)

Memory Cycle Length	DRAM Specifications	Register Field in MEM_CNTL or Calc.	Number of XCLKs	Time Provided (nS)
Cycle time	tRC = 104 ns min.	tRP + tRAS	8	120
RAS precharge	tRP = 40 ns min.	MEM_TRP=10	3	45
RAS pulse	tRAS = 60 ns min.	MEM_TRAS=100	5	75
RAS to CAS (min.)	tRCD = 14 ns min., tRCD = 45 ns max.	MEM_TRCD = 01	2	30
CAS high - RAS high	tCRD	MEM_TCRD=1	1	15
RAS - CAS high	tCSH = 40 ns min.	tRCD + 1	3	45
CAS Cycle (page mode)	tPC		2	30
CAS precharge	tCP = 10 ns min.		1	15
CAS pulse	tCAS = 10 ns min.		1	15
Row address hold	tRAH = 10 ns min.		1	15
CAS address hold	tCAH = 10 ns min.		1	15
Output enable setup	tOES = 0 ns min.		≥1	15
Output enable hold	tOEH = 0 ns min.		≥1	15
Write command setup	tWCS = 0 ns min.		≥1	15
Write command hold	tWCH = 10 ns min.		1	15
Row address setup	tASR = 0 ns min.		≥1	15
Column address setup	tASC = 0 ns min.		≥1	15
Write data setup	tDS = 0 ns min.		1	15
Write data hold	tDH = 10 ns min.		1	15

Note: All times are shown to the nearest nano-second (ns).

Table 7-11 Additional MEM_CNTL Register Bits to be Programmed

MEM_CNTL Bits	Register Field Name	Value
5:4	MEM_LATENCY	01 (2 clocks)
7:6	MEM_LATCH	10 (positive edge of XCLK)
13	MEM_TR2W	0 (1 clock delay between read and write)
19	MEM_REFRESH_DIS	0 (enabled)

Table 7-11 Additional MEM_CNTL Register Bits to be Programmed (Continued)

MEM_CNTL Bits	Register Field Name	Value
22:20	MEM_REFRESH_RATE	100 (1 every 1031 XCLK or 512 cycles per 7.9 mS for 67MHz operation)

7.3.2 Hyperpage EDO DRAM

Table 7-12 Hyperpage EDO DRAM (Silicon Magic SM81LC256K16A1-35), XCLK Speed = 83 MHz (12 ns period)

Memory Cycle Length	DRAM Specifications	Register Field in MEM_CNTL or Calc.	Min. Time (ns)	Time Provided (nS)
XCLK Period	tC			12
Cycle time	tRC = 48 ns min.	tRP + tRAS	5 tC	60
RAS precharge	tRP = 17 ns min.	MEM_TRP = 01	2 tC	24
RAS pulse	tRAS = 28 ns min.	MEM_TRAS = 010	3 tC	36
RAS to CAS (min.)	tRCD = 10 ns min.	MEM_TRCD = 00	1 ½ tC	18
CAS high - RAS high	tCRD	MEM_TCRD = 1	1 tC	12
RAS - CAS high	tCSH = 22 ns min.	tRCD + ½	2 tC	24
CAS Cycle	tPC = 12 ns min.		1 tC	12
CAS precharge	tCP = 5 ns min.		½ tC	6.0
CAS pulse	tCAS = 5 ns min.		0.4 tC	4.8
Row address hold	tRAH = 6 ns min.		1 tC	12
CAS address hold	tCAH= 5 ns min.		0.4 tC	4.8
Output enable setup	tOES		½ tC - 5.0	1.0
Output enable hold	tOEH=5 min.		1 tC	12
Write command setup	tWCS=0 min.		½ tC - 5.0	12
Write command hold	tWCH=6 min.		0.4 tC	1.0
Row address setup	tASR=0 min.		1 tC	12
Column address setup	tASC=0 min.		½ tC - 5.0	12
Write data setup	tDS=0 min.		½ tC - 5.0	1.0
Write data hold	tDH=6 min.		0.4 tC	4.8

All times are shown to the nearest nano-second (ns).

Table 7-13 Additional MEM_CNTL Register Bits to be Programmed

MEM_CNTL Bits	Register Field Name	Value
5:4	MEM_LATENCY	01 (2 clocks)
7:6	MEM_LATCH	10 (positive edge of XCLK)
13	MEM_TR2W	0 (1 clock delay between read to write)
14	MEM_CAS_PHASE	0 (CAS low when clock low)
19	MEM_REFRESH_DIS	0 (enabled)
22:20	MEM_REFRESH_RATE	110 (1 every 1250 XCLK or 512 cycles per 7.7 mS for 83 MHz operation)

7.3.3 SGRAM

Table 7-14 SGRAM (Hitachi HM5216326-10), XCLK Speed = 100 MHz, CAS Latency = 3

Parameter	SGRAM Specification (ns)	Register Field in MEM_CNTL	Number of XCLKs	Time Provided (ns)
Row cycle time	tRC = 90 min.	tRP + tRAS	9	90
PRE to ACTV delay	tRP = 30 min.	MEM_TRP = 10	3	30
ACTV to PRE mi n. delay	tRAS = 60 min.	MEM_TRAS = 101	6	60
ACTV to CMD delay	tRCD = 30 min.	MEM_TRCD = 10	3	30
Write recovery time	tWR = 20 min.	(MEM_TCRD=1) + 1	2	20

Table 7-15 Additional MEM_CNTL Register Bits to be Programmed

MEM_CNTL Bits	Register Field Name	Value
5:4	MEM_LATENCY	11 (4 clocks, SGRAM CAS latency 3)
7:6	MEM_LATCH	01 (HCLK feedback)
19	MEM_REFRESH_DIS	0 (enabled)
22:20	MEM_REFRESH_RATE	110 (1 every 1250 XCLK or 1024 cycles per 12.8 ms for 100 MHz operation)

Table 7-16 Additional EXT_MEM_CNTL Register Bits to be Programmed

EXT_MEM_CNTL Bits	Register Field Name	Value
0	MEM_CS	1 (allow commands every clock)
9:8	MEM_CLK_SELECT	00 (SD/SGRAM clock from DLL)
11:10	MEM_CAS_LATENCY	11 (SD/SGRAM CAS latency = 3 clocks)
27:24	MEM_GCMRS	0101

7.4 ZV Port Timing

The timing diagram below depicts the relationship amongst the ZV Port signals. The associated video interface timing table (*Table 7-18*) shows the AC parameters associated with the ZV Port signals when the ZV Port custom interface is in use.

Table 7-17 ZV Port Signals

Signal	Description
PCLK	This signal is used to clock valid data and HREF signal into the ZV Port. The maximum rate is 40 Mhz. During display time, rising edge of PCLK is used to clock the 16-bit pixel data into the ZV Port.
VSYNC	This signal supplies the vertical synchronization pulse to the ZV Port that displays the video data
HREF	This signal supplies the horizontal synchronization pulse to the ZV Port that displays the video data.
Y[7:0]	These signals are 8 bits of luminance data that are input to the ZV Port from the PC Card.
UV[7:0]	These signals are 8 bits of chrominance data that are input to the ZV Port from the PC Card.

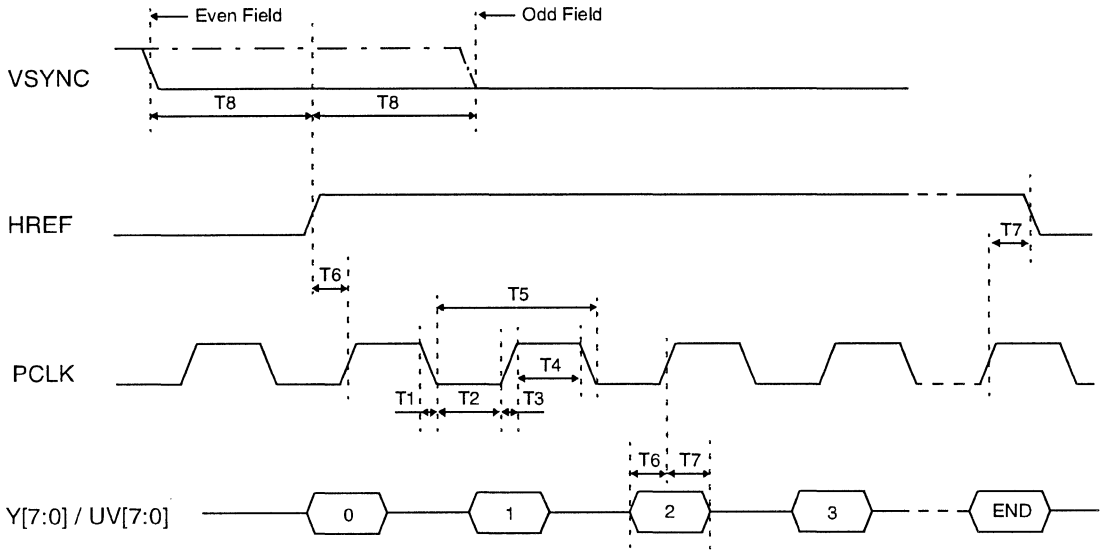


Figure 7-15. Relationships among ZV Port signals

Table 7-18 ZV Port Timing Parameters

Symbol	Parameter	Minimum	Maximum
t1	PCLK fall time	4 ns (TBD)	8 ns (TBD)
t2	PCLK low time	20 ns (TBD).	
t3	PCLK rise time	4 ns (TBD)	8 ns (TBD)
t4	PCLK high time	20 ns (TBD)	
t5	PCLK cycle time	62.5 ns (25 ns)	
t6	Y[7:0] / UV[7:0] / HREF setup time	30 ns (TBD)	
t7	Y[7:0] / UV[7:0] / HREF hold time	10 ns (TBD)	
t8	VSYNC setup / hold time to HREF	100 ns (TBD)	

The ZV port can run with a PCLK period of 25 ns, although the PCMCIA specifies 62.5 ns. The timing at 40 MHz is shown in brackets next to the PCMCIA timing specifications. Please refer to the PCMCIA Zoom Video Port Specification for further details.

7.5 LCD Panel Timing

7.5.1 TFT Panel

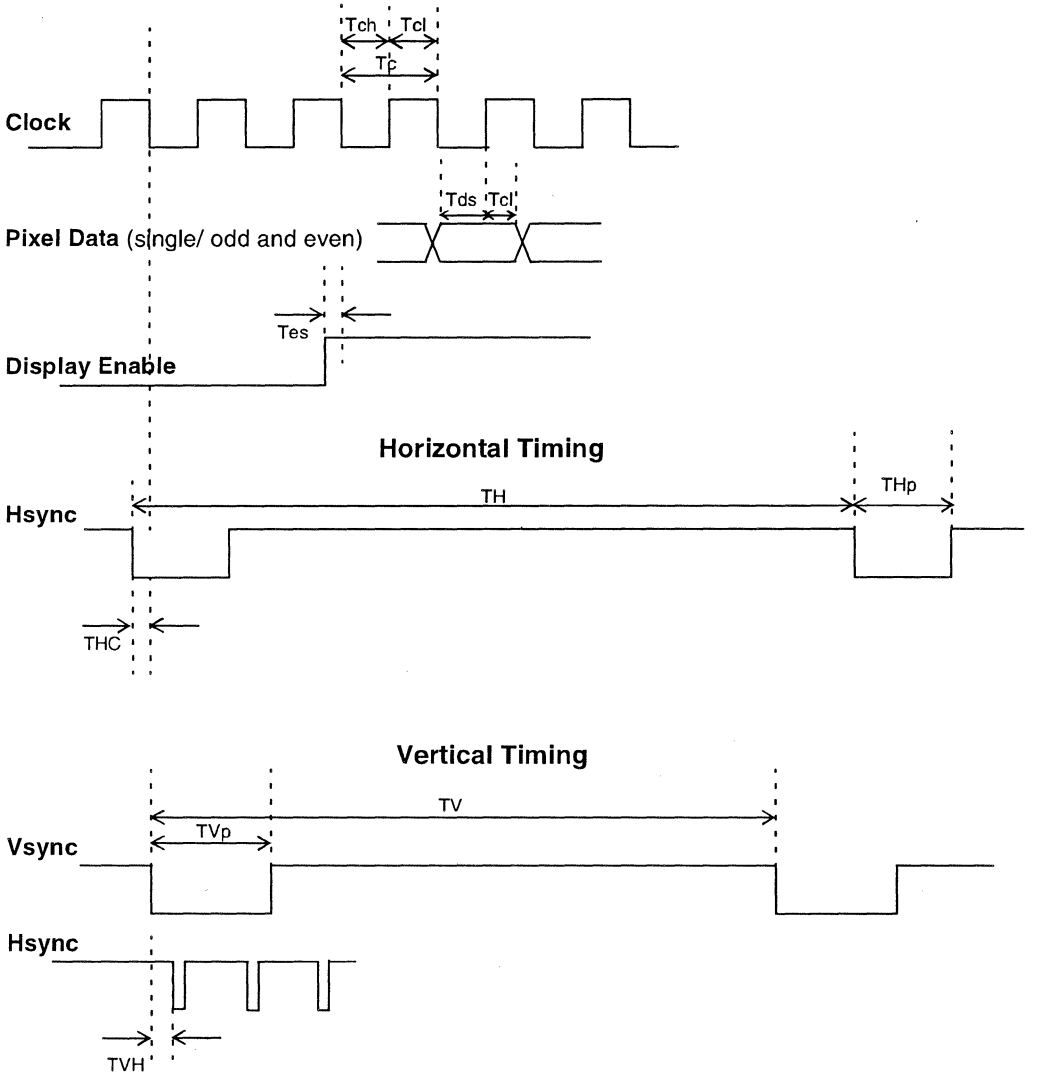


Figure 7-16. TFT Panel Timing.

7.5.2 STN Panel

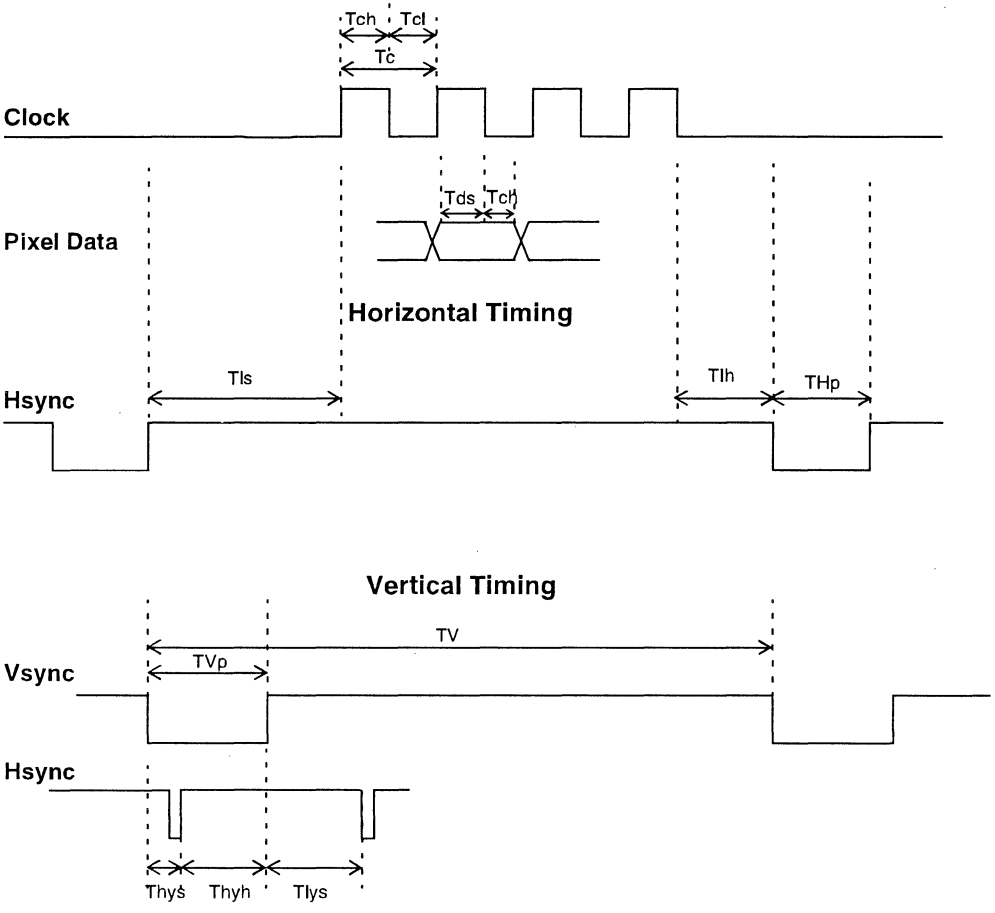


Figure 7-17. STN Panel Timing.

7.5.3 LCD Panel Timing Tables

Table 7-19 TFT Panel (640x480) - Single Pixel per Clock

Symbol	Timings		
	Maximum	Typical	Minimum
I/TV		60Hz	
THp		2.5us	
THC			10ns
TH		32us	
Tch	23ns		20.5ns
Tcl	19.5ns		17ns
Tc		40ns	
Tds			19.4ns
Tdh			16.3ns
Tes			10ns
TVp		64us	
TVH		2us	

Table 7-20 TFT Panel (800x600) - Single Pixel per Clock

Symbol	Timings		
	Maximum	Typical	Minimum
I/TV		60Hz	
THp		1.6us	
THC			10ns
TH		26us	
Tch	15ns		13ns
Tcl	12ns		10ns
Tc		25ns	
Tds			12ns
Tdh			10ns
Tes		12ns	
TVp		52us	
TVH		2us	

Table 7-21 TFT Panel (1024x768) - Odd and Even Pixel per Clock

Symbol	Timings		
	Maximum	Typical	Minimum
I/TV		52Hz	
THp		1.1us	
THC			17ns
TH		24us	
Tch	21.5ns		18ns
Tcl	17ns		13.5ns
Tc		35ns	
Tds			18ns
Tdh			10ns
Tes		10ns	
TVp		34us	
TVH		2us	

Table 7-22 STN Panel (640x480)

Symbol	Timings		
	Maximum	Typical	Minimum
I/TV		60Hz	
THp		2.5us	
TH		32us	
Tch	83.6ns		80ns
Tcl	79.2ns		76.3ns
Tc		160ns	
Tds	80ns		79.5ns
Tdh	77.9ns		74.6ns
Tls		2ns	
Tlh		1us	
TVp		64us	
Thys		200ns	

Table 7-22 STN Panel (640x480)

Symbol	Timings		
	Maximum	Typical	Minimum
Thyh		3us	
Tlys		400ns	

Table 7-23 STN Panel (800x600)

Symbol	Timings		
	Maximum	Typical	Minimum
I/TV		60Hz	
THp		1.65us	
TH		26us	
Tch	53.6ns		50ns
Tcl	46.3ns		49.2ns
Tc		100ns	
Tds	50ns		49.5ns
Tdh	47.9ns		44.6ns
Tls		2ns	
Tlh		1us	
TVp		64us	
Thys		200ns	
Thyh		3us	
Tlys		400ns	

Table 7-24 STN Panel (1024x768)

Symbol	Timings		
	Maximum	Typical	Minimum
I/TV		60Hz	
THp		0.2us	
TH		41us	
Tch		61ns	

Table 7-24 STN Panel (1024x768) (Continued)

Symbol	Timings		
	Maximum	Typical	Minimum
Tcl		61ns	
Tc		123ns	
Tds		61ns	
Tdh		61ns	
Tls		2ns	
Tlh		1us	
TVp		41us	
Thys		200ns	
Thyh		41us	
Tlys		200ns	

7.5.4 LVDS Panel Timing

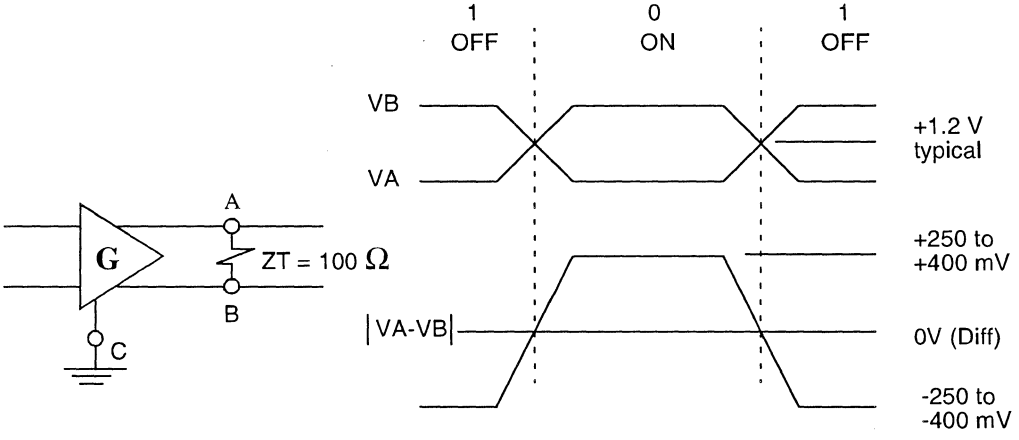


Figure 7-18. LVDS Panel Timing.

Table 7-25

Symbol	Description	Timing
Tccs	Transmitter Channel to Channel Skew defines the skew between clock and data lines with a fixed clock position	100 ps
Tckj	Transmitter Clock Jitter defines the maximum cycle to cycle clock jitter at the transmitter	200 ps

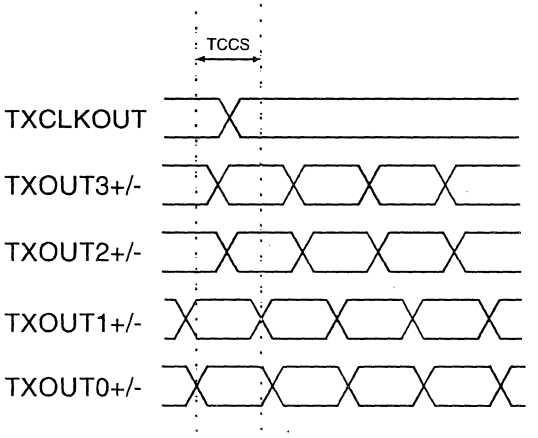
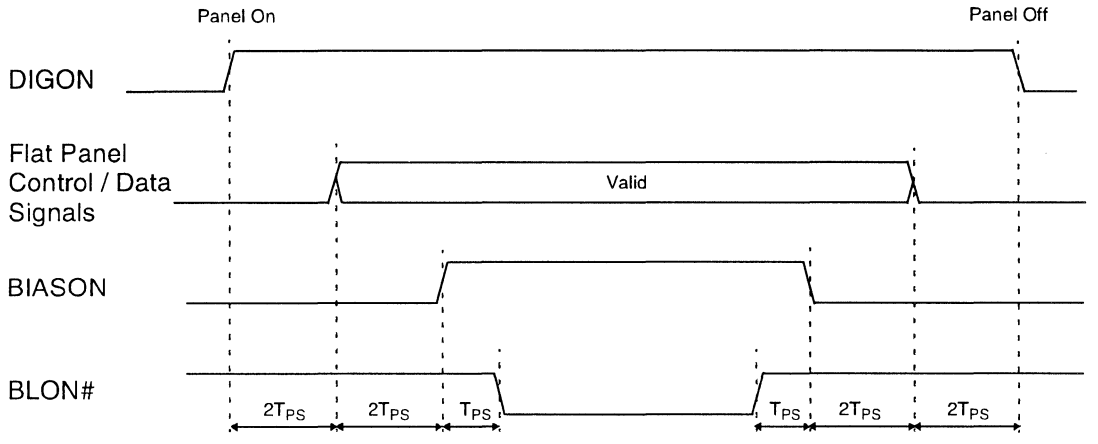


Figure 7-19. Transmitter Channel to Channel Skew

7.5.5 Panel Power Sequencing Timing



T_{PS} = power sequencing delay time

Figure 7-20. Panel Power Sequencing Timing

Note: Tps — power sequencing delay time — is programmable (field PWRSEQ_DELAY, bits 31 to 24 in the ZVGPIO register) from 4 to 1024 ms in increments of 4 ms. At default, Tps = T frame pulse = 16ms for 60Hz refresh rate.

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Chapter 8
Display Modes

The *3D RAGE LT PRO* is capable of a wide variety of modes with various combinations of CRT, LCD and TV-Out outputs. This chapter describes the modes supported and their respective memory requirements for various display combinations (primary and/or secondary CRT Controller), full screen 3D, video/DVD and TV-Out.

NOTE: In all cases, memory configuration is assumed to be 100MHz SGRAM unless otherwise specified.

8.1 Single CRT Controller Modes

The following table represents the modes supported in single CRTC configurations, that is, only one display (either primary or secondary) active. The tables specify the minimum memory requirement for various display sizes and refresh rates. Note that specific display devices (CRT or LCD panels) may not support all modes.

Table 8-1

Single CRT Supported Modes (TFT or DSTN or CRT)						
			Minimum amount of Memory Required			
dsp wid	dsp hgt	ref (HZ)	8 bpp	16 bpp	24 bpp	32 bpp
640	480	60	2 MB	2 MB	2 MB	2 MB
640	480	72	2 MB	2 MB	2 MB	2 MB
640	480	75	2 MB	2 MB	2 MB	2 MB
640	480	90	2 MB	2 MB	2 MB	2 MB
640	480	100	2 MB	2 MB	2 MB	2 MB
800	600	60	2 MB	2 MB	2 MB	4 MB
800	600	70	2 MB	2 MB	2 MB	4 MB
800	600	75	2 MB	2 MB	2 MB	4 MB
800	600	90	2 MB	2 MB	2 MB	4 MB
800	600	100	2 MB	2 MB	2 MB	4 MB
1024	768	60	2 MB	2 MB	4 MB	4 MB
1024	768	72	2 MB	2 MB	4 MB	4 MB
1024	768	75	2 MB	2 MB	4 MB	4 MB
1024	768	90	2 MB	2 MB	4 MB	4 MB
1024	768	100	2 MB	2 MB	4 MB	4 MB
1280	1024	43	2 MB	4 MB	4 MB	6 MB
1280	1024	60	2 MB	4 MB	4 MB	6 MB

Table 8-1 (Continued)

Single CRT Supported Modes (TFT or DSTN or CRT)						
			Minimum amount of Memory Required			
dsp wid	dsp hgt	ref (HZ)	8 bpp	16 bpp	24 bpp	32 bpp
1280	1024	70	2 MB	4 MB	4 MB	6 MB
1280	1024	72	2 MB	4 MB	4 MB	6 MB
1600	1200	60	4 MB	4 MB	6 MB	8 MB
1600	1200	66	4 MB	4 MB	6 MB	8 MB
1600	1200	76	4 MB	4 MB	6 MB	-
1600	1200	85	4 MB	4 MB	6 MB	-
	indicates modes not supported by secondary display					

8.2 Dual CRTC Modes

The following two tables represent the modes supported in dual CRTC configurations, with two independent displays running concurrently. Please note the memory size, type and speed as well as the refresh rates. The tables specify the maximum colour depth (in bits-per-pixel) for the secondary display, given the colour depth and resolution of the primary display and the resolution of the secondary display.

Table 8-2

Dual Display for 4Meg SGRAM 100MHz and 75Hz Refresh for Both Displays							
				Max Secondary Display Resolution			
dsp1 wid	dsp1 hgt	dsp2 wid	dsp2 hgt	dsp1 8bpp	dsp1 16bpp	dsp1 24 bpp	dsp1 32 bpp
640	480	640	480	32 bpp	32 bpp	32 bpp	32 bpp
640	480	800	600	32 bpp	32 bpp	32 bpp	32 bpp
640	480	1024	768	32 bpp	32 bpp	32 bpp	24 bpp
640	480	1280	1024	16 bpp	16 bpp	16 bpp	16 bpp
800	600	640	480	32 bpp	32 bpp	32 bpp	32 bpp
800	600	800	600	32 bpp	32 bpp	32 bpp	32 bpp
800	600	1024	768	32 bpp	32 bpp	24 bpp	16 bpp
800	600	1280	1024	24 bpp	24 bpp	24 bpp	16 bpp
1024	768	640	480	32 bpp	32 bpp	32 bpp	24 bpp
1024	768	800	600	32 bpp	32 bpp	24 bpp	16 bpp
1024	768	1024	768	32 bpp	24 bpp	16 bpp	8 bpp
1024	768	1280	1024	16 bpp	8 bpp	8 bpp	
1280	1024	640	480	32 bpp	32 bpp		
1280	1024	800	600	32 bpp	24 bpp		

Table 8-2 (Continued)

Dual Display for 4Meg SGRAM 100MHz and 75Hz Refresh for Both Displays							
				Max Secondary Display Resolution			
dsp1 wid	dsp1 hgt	dsp2 wid	dsp2 hgt	dsp1 8bpp	dsp1 16bpp	dsp1 24 bpp	dsp1 32 bpp
1280	1024	1024	768	24 bpp	8 bpp		
1280	1024	1280	1024	16 bpp	8 bpp		
1600	1200	640	480	32 bpp	8 bpp		
1600	1200	800	600	32 bpp			
1600	1200	1024	768	16 bpp			
1600	1200	1280	1024	8 bpp			

Table 8-3

Dual Display for 2Meg SGRAM 100MHz and 75Hz Refresh for Both Displays							
				Max Secondary Display Resolution			
dsp1 wid	dsp1 hgt	dsp2 wid	dsp2 hgt	dsp1 8 bpp	dsp1 16 bpp	dsp1 24 bpp	dsp1 32 bpp
640	480	640	480	32 bpp	32 bpp	24 bpp	16 bpp
640	480	800	600	24 bpp	16 bpp	16 bpp	8 bpp
640	480	1024	768	16 bpp	8 bpp	8 bpp	8 bpp
640	480	1280	1024	8 bpp	8 bpp		
800	600	640	480	32 bpp	24 bpp	16 bpp	
800	600	800	600	24 bpp	16 bpp	8 bpp	
800	600	1024	768				
800	600	1280	1024				
1024	768	640	480	32 bpp	8 bpp		
1024	768	800	600	16 bpp			
1024	768	1024	768	8 bpp			
1024	768	1280	1024				
1280	1024	640	480	16 bpp			
1280	1024	800	600	8 bpp			
1280	1024	1024	768				
1280	1024	1280	1024				
1600	1200	640	480				
1600	1200	800	600				
1600	1200	1024	768				
1600	1200	1280	1024				

8.3 Full Screen 3D Modes

The following tables represent the minimum memory requirements for full screen 3D display in various colour depths and resolutions.

Table 8-4

3D in Full Screen Supported Modes (TFT or CRT)										
			Min Req Memory with Z Buffer Enabled				Min Req Memory with Z Buffer Disabled			
dsp wid	dsp hgt	ref (HZ)	8 bpp	16 bpp	24 bpp	32 bpp	8 bpp	16 bpp	24 bpp	32 bpp
640	480	60	2 MB	2 MB	4 MB	4 MB	2 MB	2 MB	2 MB	4 MB
640	480	72	2 MB	2 MB	4 MB	4 MB	2 MB	2 MB	2 MB	4 MB
640	480	75	2 MB	2 MB	4 MB	4 MB	2 MB	2 MB	2 MB	4 MB
640	480	90	2 MB	2 MB	4 MB	4 MB	2 MB	2 MB	2 MB	4 MB
640	480	100	2 MB	2 MB	4 MB	4 MB	2 MB	2 MB	2 MB	4 MB
800	600	60	4 MB	4 MB	4 MB	6 MB	2 MB	2 MB	4 MB	4 MB
800	600	70	4 MB	4 MB	4 MB	6 MB	2 MB	2 MB	4 MB	4 MB
800	600	75	4 MB	4 MB	4 MB	6 MB	2 MB	2 MB	4 MB	4 MB
800	600	90	4 MB	4 MB	4 MB	6 MB	2 MB	2 MB	4 MB	4 MB
800	600	100	4 MB	4 MB	4 MB	6 MB	2 MB	2 MB	4 MB	4 MB
1024	768	60	4 MB	6 MB	8 MB	8 MB	2 MB	4 MB	6 MB	8 MB
1024	768	72	4 MB	6 MB	8 MB	8 MB	2 MB	4 MB	6 MB	8 MB
1024	768	75	4 MB	6 MB	8 MB	8 MB	2 MB	4 MB	6 MB	8 MB
1024	768	90	4 MB	6 MB	8 MB	8 MB	2 MB	4 MB	6 MB	8 MB
1024	768	100	4 MB	6 MB	8 MB	8 MB	2 MB	4 MB	6 MB	8 MB
1280	1024	43	6 MB	8 MB	12 MB	16 MB	4 MB	6 MB	8 MB	12 MB
1280	1024	60	6 MB	8 MB	12 MB	16 MB	4 MB	6 MB	8 MB	12 MB
1280	1024	70	6 MB	8 MB	12 MB	16 MB	4 MB	6 MB	8 MB	12 MB
1280	1024	72	6 MB	8 MB	12 MB	16 MB	4 MB	6 MB	8 MB	12 MB
1600	1200	60	8 MB	12 MB	16 MB	-	4 MB	8 MB	12 MB	16 MB
1600	1200	66	8 MB	12 MB	16 MB	-	4 MB	8 MB	12 MB	16 MB
1600	1200	76	8 MB	12 MB	16 MB	-	4 MB	8 MB	12 MB	-
1600	1200	85	8 MB	12 MB	16 MB	-	4 MB	8 MB	12 MB	-

indicates memory size not supported

8.4 DVD/Video Modes

The following tables represent memory requirements for DVD Video Playback for both software and hardware MPEG decoding in various display modes. Both NTSC and PAL formats are provided in each table. DVD NTSC is a 720x480 YUV mode running at 30 frames per second. DVD PAL is a 720x576 YUV mode running at 25 frames per second. The YUV mode is YUV12 in software MPEG decoding and YUV422 in hardware MPEG decoding.

8.4.1 Software MPEG Decoding

Table 8-5

DVD Video Playback in a Window with Software MPEG Decoding										
			Min Req Memory with DVD NTSC format				Min Req Memory with DVD PAL format			
dsp wid	dsp hgt	ref (HZ)	8 bpp	16 bpp	24 bpp	32 bpp	8 bpp	16 bpp	24 bpp	32 bpp
640	480	60	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
640	480	72	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
640	480	75	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
640	480	90	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
640	480	100	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
800	600	60	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	6 MB
800	600	70	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	6 MB
800	600	75	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	6 MB
800	600	90	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	6 MB
800	600	100	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	6 MB
1024	768	60	4 MB	4 MB	6 MB	6 MB	4 MB	4 MB	6 MB	6 MB
1024	768	72	4 MB	4 MB	6 MB	6 MB	4 MB	4 MB	6 MB	6 MB
1024	768	75	4 MB	4 MB	6 MB	6 MB	4 MB	4 MB	6 MB	6 MB
1024	768	90	4 MB	4 MB	6 MB	6 MB	4 MB	4 MB	6 MB	6 MB
1024	768	100	4 MB	4 MB	6 MB	6 MB	4 MB	4 MB	6 MB	6 MB
1280	1024	43	4 MB	6 MB	6 MB	8 MB	4 MB	6 MB	8 MB	8 MB
1280	1024	60	4 MB	6 MB	6 MB	8 MB	4 MB	6 MB	8 MB	8 MB
1280	1024	70	4 MB	6 MB	6 MB	8 MB	4 MB	6 MB	8 MB	8 MB
1280	1024	74	4 MB	6 MB	6 MB	8 MB	4 MB	6 MB	8 MB	8 MB
1600	1200	60	6 MB	6 MB	8 MB	-	8 MB	8 MB	8 MB	-
1600	1200	66	6 Mb	6 MB	8 MB	-	8 MB	8 MB	8 MB	-
1600	1200	76	6 MB	6 MB	-	-	8 MB	8 MB	-	-
1600	1200	85	6 MB	6 MB	-	-	8 MB	8 MB	-	-

delta between NTSC and PAL formats

8.4.2 Hardware MPEG Decoding

Table 8-6

DVD Video Playback in a Window with Hardware MPEG Decoding										
			Min Req Memory with DVD NTSC format				Min Req Memory with DVD PAL format			
dsp wid	dsp hgt	ref (HZ)	8 bpp	16 bpp	24 bpp	32 bpp	8 bpp	16 bpp	24 bpp	32 bpp
640	480	60	2 MB	2 MB	4 MB	4 MB	2 MB	4 MB	4 MB	4 MB
640	480	72	2 MB	2 MB	4 MB	4 MB	2 MB	4 MB	4 MB	4 MB
640	480	75	2 MB	2 MB	4 MB	4 MB	2 MB	4 MB	4 MB	4 MB
640	480	90	2 MB	2 MB	4 MB	4 MB	2 MB	4 MB	4 MB	4 MB
640	480	100	2 MB	2 MB	4 MB	4 MB	2 MB	4 MB	4 MB	4 MB
800	600	60	2 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
800	600	70	2 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
800	600	75	2 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
800	600	90	2 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
800	600	100	2 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
1024	768	60	4 MB	4 MB	4 MB	6 MB	4 MB	4 MB	6 MB	6 MB
1024	768	72	4 MB	4 MB	4 MB	6 MB	4 MB	4 MB	6 MB	6 MB
1024	768	75	4 MB	4 MB	4 MB	6 MB	4 MB	4 MB	6 MB	6 MB
1024	768	90	4 MB	4 MB	4 MB	6 MB	4 MB	4 MB	6 MB	6 MB
1024	768	100	4 MB	4 MB	4 MB	6 MB	4 MB	4 MB	6 MB	6 MB
1280	1024	43	4 MB	4 MB	6 MB	8 MB	4 MB	6 MB	6 MB	8 MB
1280	1024	60	4 MB	4 MB	6 MB	8 MB	4 MB	6 MB	6 MB	8 MB
1280	1024	70	4 MB	4 MB	6 MB	8 MB	4 MB	6 MB	6 MB	8 MB
1280	1024	74	4 MB	4 MB	6 MB	8 MB	4 MB	6 MB	6 MB	8 MB
1600	1200	60	4 MB	6 MB	8 MB	-	4 MB	6 MB	8 MB	12 MB
1600	1200	66	4 MB	6 MB	8 MB	-	4 MB	6 MB	8 MB	-
1600	1200	76	4 MB	6 MB	-	-	4 MB	6 MB	-	-
1600	1200	85	4 MB	6 MB	-	-	4 MB	6 MB	-	-

delta between NTSC and PAL formats

8.5 TV-Out Modes

The following table lists the modes (VGA and extended) supported by the integrated TV-Out. In general, the TV-Out can directly support any modes up to 1024x768 at 60Hz for NTSC and 50Hz for PAL. The TV-Out is dependent only on scaling limitations and the refresh rate of the TV. There are no memory requirements other than that of supporting the display mode as described in the Single CRTC and Dual CRTC sections above. The TV-Out supports any colour depth supported by the CRTC. By using the dual display and/or independent scaling and timing features of TV-Out, it is possible to support higher resolution modes using panning with a smaller resolution display.

Table 8-7

TV-Out Modes (any colour depth without panning)		
Mode	**NTSC (60Hz)**	**PAL (50Hz)**
320x350	yes	yes
320x400	yes	yes
320x480	yes	yes
360x400	yes	yes
400x600	yes	yes
512x384	yes	yes
640x350	yes	yes
640x400	yes	yes
640x480	yes	yes
720x350	yes	yes
720x400	yes	yes
720x480	yes	yes
704x480	yes	yes
800x600	yes	yes
512x768	yes	yes
640x768	yes	yes
848x480	yes	yes
1024x768	yes	yes
1064x600	as 1024x600	as 1024x600

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The electrical and thermal characteristics described in this document are specific to the *3D RAGE LT PRO*. Please contact ATI to obtain up-to-date information on how to support all of ATI's graphics controllers, steppings, and foundries in one PCB design.

9.1 Electrical Characteristics

9.1.1 Maximum Rating Conditions

Table 9-1 Maximum Rating Conditions

Item	Value
Supply Voltage, VDDC, VDDR	-0.50V to +7.00V
Supply Voltage, VEE	-0.50V to +7.00V
Input or Output Voltage	-0.05V to ($VEE_{MAX.}$ + 0.05V)
DC Forward Bias Current	-12mA (source) + 24mA (sink)
Storage Temperature (Plastic)	-40°C to 125°C

The extreme values determine the maximum rating conditions and are stress related — operation of the controller at these conditions is not recommended. Ratings are referenced to VDD. Operating outside the ranges may cause permanent damage to the device, and operating close to the maximum rating conditions for extended periods may affect device reliability. Use the recommended ranges below.

9.1.2 Recommended DC Operating Conditions

Table 9-2 Recommended DC Operating Conditions

Item	Value
Operating Supply Voltage (VDDC)	3.3V ±5%
Operating Supply Voltage (VDDR)	3.3V ±5%
Operating Supply Voltage (VEE)	5V ±5%
Operating Case Temperature (TC)	TBD

9.1.3 AC Characteristics

Table 9-3 AC Characteristics

Signals	Typical Capacitive Load *
ROMCS#	10pF
AD[31:0], DEVSEL#, TRDY#, STOP#, INTR#, PAR	50pF
ZVPORT[18:0]	25pF
HSYNC, VSYNC	50pF
CAS, MD[63:0], RAS, CS[3:0]	25pF
WE[7:0]	15pF
MA[9:0]	45pF
* 4MB, 256Kx16 DRAMs, through a PCI edge connector.	

9.1.4 DC Characteristics

TTL Interface

Table 9-4 DC Characteristics - TTL Interface

Symbol	Parameter	Condition	Min.	Typical	Max.	Unit
VIL	Low Level Input Voltage	-	-	-	0.8	V
VIH	High Level Input Voltage	-	2.0	-	-	V
VOL	Low Level Output Voltage	IOL=Rated Buffer Current	-	0.2	0.4	V
VOH	High Level Output Voltage	IOH=Rated Buffer Current	2.4	3.3	-	V
VT+	Schmitt Trig. positive threshold	-	-	2.0	2.4	V
VT-	Schmitt Trig negative threshold	-	0.6	0.8	-	V

General

Table 9-5 DC Characteristics - General Interface

Symbol	Parameter	Condition	Min.	Typical	Max.	Unit
IIL	Low level Input Current	VI=VSS	-	-	+1	µA
IIH	High Level Input Current	VI=VCC	-	-	-1	µA
IOZ	Tri-State Output Leakage	VO=0V or VCC	-	-	±10	µA
CIN	Input Capacitance	Freq=1MHz @ 0V	-	4	6	pF
CO	Output Capacitance	Freq=1MHz @ 0V	-	6	-	pF
CIO	Bidirectional I/O Capacitance	Freq=1MHz @ 0V	-	6	10	pF
IKLU	I/O Latch-up Current	V<VSS, V>VCC	500	-	-	mA
VEPO	Electrostatic Protection	C=100pF, R=1.5KΩ	2000	-	-	V

9.1.5 Input/Output Specifications

Table 9-6 Input/Output Electrical Specifications

Pin Name	Type	I_{OL}(min)	I_{OH}(min)	Pull Up/Pull Down	Tri-State	Interface Level
AD[31:0]	I/O	4mA	-4mA	-	-	3.3V/5V
C/BE#[3:0]	I/O	18mA	-18mA	-	-	3.3V/5V
CPUCLK	I	-	-	-	-	3.3V/5V
CLKRUN#	I/O	18mA	-18mA	-	Yes	3.3V/5V
DEVSEL#	I/O	18mA	-18mA	-	Yes	3.3V/5V
FRAME#	I/O	18	-18	-	Yes	3.3V/5V
IDSEL	I	-	-	-	-	3.3V/5V
INTR#	O	18mA	-18mA	-	Yes	3.3V/5V
IRDY#	I/O	18mA	-18mA	-	Yes	3.3V/5V
PAR	I/O	18mA	-18mA	-	Yes	3.3V/5V
RESET#	I	-	-	-	-	3.3V/5V
STOP#	I/O	18mA	-18mA	-	Yes	3.3V/5V
TRDY#	I/O	18mA	-18mA	-	Yes	3.3V/5V
REQ#	I/O	18mA	-18mA	-	Yes	3.3V/5V
GNT#	I	-	-	-	-	3.3V/5V
CAS#	I/O	16mA	-16mA	50K PU	Yes	3.3V, 5V Tol.
MA[9:0]	O	8mA	-8mA	50K PD	Yes	3.3V, 5V Tol.
MD[63:0]	I/O	2mA	-2mA	50K PD	Yes	3.3V, 5V Tol.
OE#[0]	O	16mA	-16mA	-	Yes	3.3V, 5V Tol.
OE#[1]	O	16mA	-16mA	50K PU	Yes	3.3V, 5V Tol.
CKE	O	16mA	-16mA	50K PU	Yes	3.3V, 5V Tol.
ROMCS#	I/O	4mA	-4mA	-	Yes	3.3V, 5V Tol.
DSF	I/O	8mA	-8mA	50K PU	Yes	3.3V, 5V Tol.
RAS#	O	16mA	-16mA	50K PU	Yes	3.3V, 5V Tol.
WE#[7:0]	I/O	16mA	-16mA	50K PU	Yes	3.3V, 5V Tol.
CS[3:0]	I/O	16mA	-16mA	50K PU	Yes	3.3V, 5V Tol.
R, G, B	A	-	-	-	-	-
RSET	A	-	-	-	-	-
HSYNC	O	8mA	-8mA	-	Yes	3.3V, 5V
VSYNC	O	8mA	-8mA	-	Yes	3.3V, 5V
R2SET	A	-	-	-	-	-
Y, C	A	-	-	-	-	-

Table 9-6 Input/Output Electrical Specifications (Continued)

Pin Name	Type	I_{OL}(min)	I_{OH}(min)	Pull Up/Pull Down	Tri-State	Interface Level
COMP	A	-	-	-	-	-
SYNC	O	8mA	-8mA	-	Yes	3.3V, 5V Tol.
XTALIN	I	-	-	-	-	3.3V, 5V Tol.
XTALOUT	O	-	-	-	-	-
GPIO[17:0]	I/O	8mA	-8mA	-	Yes	3.3V, 5V Tol.
LCDDO[23:0] LCDDO[35:0]*	O	8mA	-8mA	50K PD	Yes	3.3V, 5V Tol.
LCDTMG[3:0]	O	8mA	-8mA	50K PD	Yes	3.3V, 5V Tol.
LTGIO[2:0]**	I/O	8mA	-8mA	50K PD	Yes	3.3V, 5V Tol.
DIGON	O	2mA	-2mA	-	Yes	3.3V, 5V Tol.
BIASON	O	2mA	-2mA	-	Yes	3.3V, 5V Tol.
BLON	O	2mA	-2mA	-	Yes	3.3V, 5V Tol.
F32KHz	I	-	-	-	-	3.3V, 5V Tol.
STANDBY#	I	-	-	-	-	3.3V, 5V Tol.
SUSPEND#	I	-	-	-	-	3.3V, 5V Tol.
ZVPORT[18:0]	I/O	2mA	-2mA	50K PD	Yes	3.3V, 5V Tol.
ST[2:0]*	O	8mA	-8mA	-	Yes	3.3V
SBA[7:0]*	I	-	-	-	-	3.3V
RBFB*	I	-	-	-	-	3.3V
ADSTB[1:0]*	I/O	8mA	-8mA	-	Yes	3.3V
SBSTB[1:0]*	I/O	8mA	-8mA	-	Yes	3.3V
STP_AGP#[2:0]*	I	-	-	-	-	3.3V
AGP_BUSY#*	O	8mA	-8mA	-	Yes	3.3V
PCI33EN*	I	-	-	-	-	3.3V, 5V Tol.

*** Applies to 312 BGA package only.**
****Applies to 256 BGA package only.**

9.1.6 TV DAC Characteristics

Table 9-7 TV DAC Characteristics

Parameter	Min	Typ	Max	Notes
Resolution	8 bits	-	-	A
Vo (max) Maximum Output Voltage	1.32143 V (NTSC) 1.3986 V (PAL)	-	-	A
Io (max) Maximum Output Current	35.24 ma (NTSC) 37.3 ma (PAL)	-	-	A
Full Scale error	-10%	-	+10%	B,C
DAC to DAC Correlation	-2%	-	+2%	A,D
Integral Linearity	-1 lsb	-	+1lsb	A,E
Rise Time (10% to 90%)	-	-	3ns	A,F
Full Scale Settling Time	-	<8ns	-	A,G,H
Glitch Energy	-	60 pv-sec	-	A,H
Monotonicity	-	-	-	I

Notes:

A. Tested over the operating temperature range, at nominal supply voltage with an IREF of -3.04mA. (IREF is the level of the current flowing in the RSET resistor).

B. Tested over the operating temperature range, at reduced supply voltage, with a -3.04mA IREF. (IREF is the level of the current flowing in the RSET resistor).

C. Full scale error from the value predicted by the design equations.

D. About the mid point of the distribution of the three DAC's measured at full scale deflection.

E. Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed.

F. Load = 37.5Ω +20pf with IREF = -3.04mA. (IREF is the current flowing in the RSET resistor).

G. From a 2% change in the output voltage until settling to within 2% of the final value.

H. This parameter is sampled, not 100% tested.

I. Monotonicity is guaranteed.

9.1.7 DAC Characteristics

All voltages in the table below are referenced to VSS unless specified otherwise.

The Pixel Clock frequency must be stable for a period of at least 20 seconds. after power up (or after a change in Pixel Clock frequency), before proper device operation characteristics are guaranteed.

Table 9-8 DAC Characteristics*

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
-	Resolution	8	-	-	bits	A
VO(max)	Maximum Output Voltage	1.1	-	-	V	A
IO(max)	Maximum Output Current	-	22.05	-	mA	A
-	Full Scale Error	-10	-	+10	%	B, C
-	DAC to DAC Correlation	-2	-	+2	%	A, D
-	Integral Linearity	-0.5	-	0.5	LSB	A, E
-	Rise Time (10% to 90%)	-	-	3	ns	A, F
-	Full Scale Settling Time	-	8	-	ns	A, G, H
-	Glitch Energy	-	60	-	pV-Sec	A, H
-	Monotonicity	-	-	-	-	I
V_{REFM}	Measured Reference Voltage	-6%	1.235	+6%	V	J

* See Table 9-9 on page 9 for PS/2 DAC characteristics

Notes:

A. Tested over the operating temperature range, at nominal supply voltage with an IREF of -2.93mA. (IREF is the level of the current flowing in the RSET resistor).

B. Tested over the operating temperature range, at reduced supply voltage, with a -2.93mA IREF. (IREF is the level of the current flowing in the RSET resistor).

C. Full scale error from the value predicted by the design equations.

D. About the mid point of the distribution of the three DAC's measured at full scale deflection.

E. Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed.

F. Load = 37.5Ω +20pf with IREF = -2.93mA. (IREF is the current flowing in the RSET resistor).

G. From a 2% change in the output voltage until settling to within 2% of the final value.

H. This parameter is sampled, not 100% tested.

I. Monotonicity is guaranteed.

J. V_{REFM} is the measured value of logged data. It is the idealized V_{REF} shifted by 2.9%.

9.1.8 Calculating RSET Resistance (DAC Interface)

A precision resistor (with 1% of nominal) is placed between RSET (pin 123) and analog ground (AVSS) to set the full-scale DAC current. This resistance is typically 422Ω for PS/2 applications where the effective impedance is 37.5Ω (doubly terminated 75Ω loads, shown in the following figure). 422Ω is an acceptable value for RSET with a slightly reduced white level.

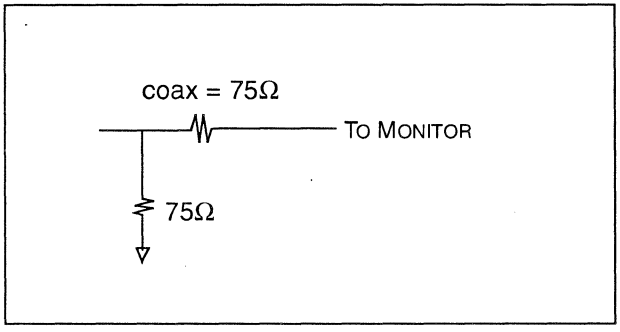


Figure 9-1. PS/2 Example

The required resistor value can be calculated using the formula:

$$\mathbf{RSET}\ (\Omega) = (6.22 \times V_{REF} \times \alpha) / I_{OUT}$$

where: 6.22 is the idealized 8-bit gain constant

V_{REF} is the idealized reference voltage (1.2V)

α is the systematic **composite** skew on idealized V_{REF} and gain constant. It has been empirically determined to be 1.051 from data logging. This amounts to a 5.1 % overall correction. (2.9% attributed to V_{REF} and 2.2% to the gain constant)

I_{OUT} is the required DAC full-scale current given by:
$I_{OUT} = (V_{WHITE} - V_{BLACK}) / Z_{EFF}$

For: $V_{WHITE} = 0.7V$
$V_{BLACK} = 0V$
$Z_{EFF} = 37.5\Omega$

$I_{OUT} = 0.7V - 0V / 37.5\Omega = 0.0186A$

Defining RSET in this fashion allows for a one time compensation for the systematic skew due to shifts on both V_{REF} and the gain constant on the output white level by adjustment of α.

The variation in α has been set to be 10%, of which 6% has been attributed to the bandgap ($V_{REFM} = 1.2 \times 1.029 \pm 6\% = 1.235 \pm 6\%$), and the rest (4%) to the variation of the gain constant. Hence,

I_{OUT} max = 18.6mA x 1.1
I_{OUT} min = 18.6mA x 0.9

PS/2 Example:

$$\mathbf{RSET\ (\Omega) = (6.22 \times V_{REF} \times \alpha) / I_{OUT}}$$
$$\mathbf{= 6.22 \times 1.2 \times 1.051 / 0.0186}$$
$$\mathbf{= 422\Omega}$$

Table 9-9 PS/2 DAC Characteristics*

Parameter	Min.	Typ.	Max.	Unit
V_{WHITE}	630	700	770	mV
I_{OUT}	-10%	18.6	+10%	mA

* Values obtained using 37.5Ω load, 422Ω (± 1%) RSET with 8-bit white level.

9.1.9 Analog Output Specification

Conceptually, each 8-bit DAC can be viewed as two current sources connected in parallel. Each current source is controlled independently as shown below.

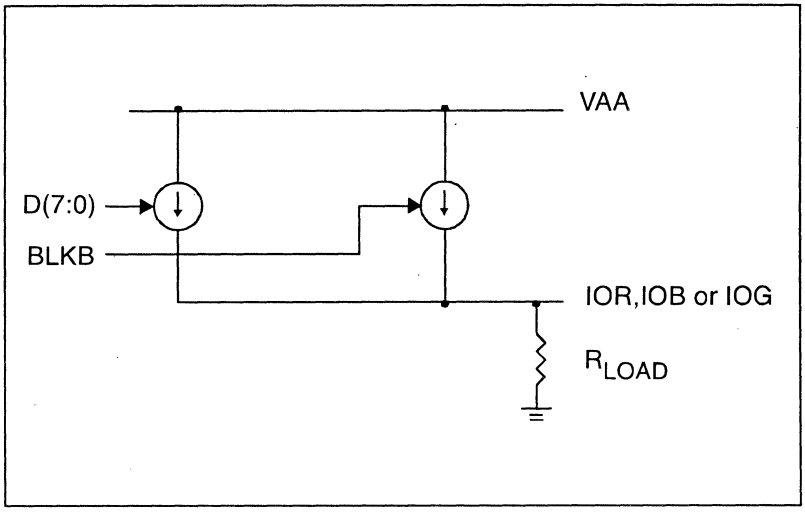


Figure 9-2. Analog Output (DAC)

With a 75Ω doubly-terminated load, VREF=1.2V, and RSET=397Ω PS/2 levels are shown below, with pedestal current set to 7.5 IRE.

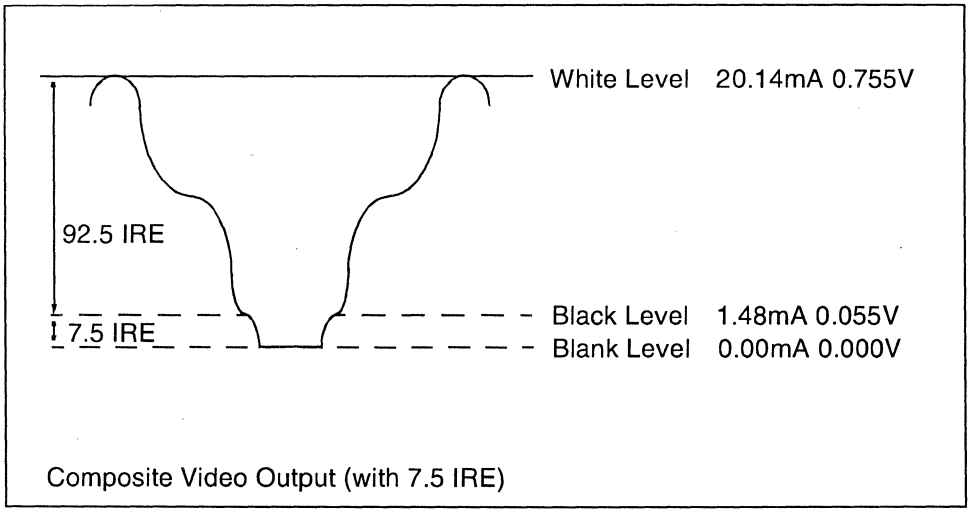


Figure 9-3. Analog Output (Composite)

9.2 Thermal Characteristics

The thermal operation characteristics of the chip depend on the board it is mounted on. The tables below present the values of θCA (case-to-ambient thermal resistance) and TA*max* (maximum ambient temperature) for different airflows over the chip.

Table 9-10 Single-layer Board

Airflow (m/s)	0	0.5	1.0	2.0	3.0
θCA(°C/W)	21.0	15.8	14.5	11.9	11.3
TA*max*(°C)	28	44	49	57	59

Table 9-11 Multi-layer Board with Ground Plane

Airflow (m/s)	0	0.5	1.0	2.0	3.0
θCA(°C/W)	17.6	14	12.5	10.4	10.0
TA*max*(°C)	39	50	55	62	63

9.2.1 Maximum Ambient Temperature

Typical maximum ambient temperatures (TA*max*) can be derived from the following equation:

$$TA_{max} = TC_{max} - P * \theta CA$$

Where TC*max* is maximum case temperature, P is power dissipation, and θCA is case-to-ambient thermal resistance.

Power dissipation varies with different display frequencies but is typically between 1.0W to 2.0W when the chip is operating at nominal VDD. Case temperature (**TC**) may be measured in any environment, and should be taken at the center of the top surface of the device.

9.2.2 Junction Temperature

The junction-to-case thermal resistance (θJC) of this device is approximately 3°C/W. Junction temperature (TJ) may be calculated as follows:

$$TJ = (\theta JC + \theta CA) * P + TA$$

The maximum junction temperature allowed (for worst case condition) is 100 degrees C.

9.3 Power and Case Temperature Measurements

The following table represents the results of *3D RAGE LT PRO* ASIC and memory (4M SGRAM) power consumption and case temperature measurements. Since the power and temperature depend on the activity inside the ASIC, the measurements were done in three categories — 2D demo on, 2D demo off, and 3D demo on — at a room temperature of 23.9 °C

An Intel A2 motherboard was used as a test station, and CRT display (ISR 10011-035) as an output device.

Table 9-12 Power Consumption and Case Temperature

Operation Conditions	ASIC		SGRAM (4M)
	Power	Case Temp.	
Nominal: 640x480x32bpp at 75Hz Both 2D and 3D demo off.	TBD	45 °C	0.5 W
Extreme: 1600x1200x16bpp at 85Hz 3D demo on.	TBD	66 °C	0.8 W

9.4 Physical Dimensions

9.4.1 312-Pin PBGA Package

Package outline PBGA 27x27mm - 312 +16

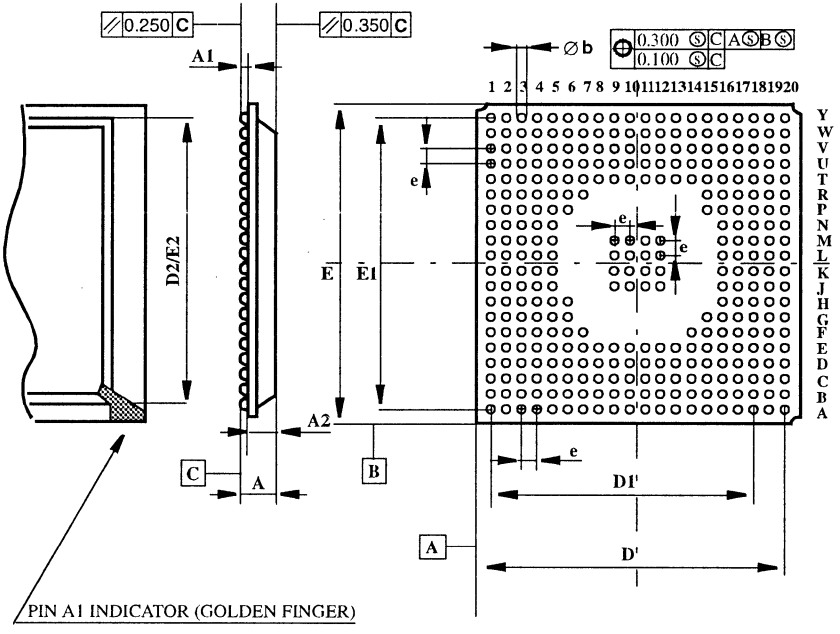


Figure 9-4. 312-pin PBGA Physical Dimensions

Table 9-13 312-Pin PBGA Package Physical Dimensions

Ref.	Millimeters		
	Typical	Min.	Max.
A		2.125	2.595
A1		0.50	0.70
A2		1.625	1.895
b		0.60	0.90
D	27.00	26.82	27.18
D1	24.13 BASIC		
D2		23.90	24.10
e	1.27 BASIC		
E	27.00	26.82	27.18
E1	24.13 BASIC		
E2		23.90	24.10

Notes:

- Drawing BGA 27x27 finished 14090116-004
- Reference document JEDEC M0151

9.4.2 256-Pin PBGA Package

Package outline PBGA 27x27mm - 256 +16

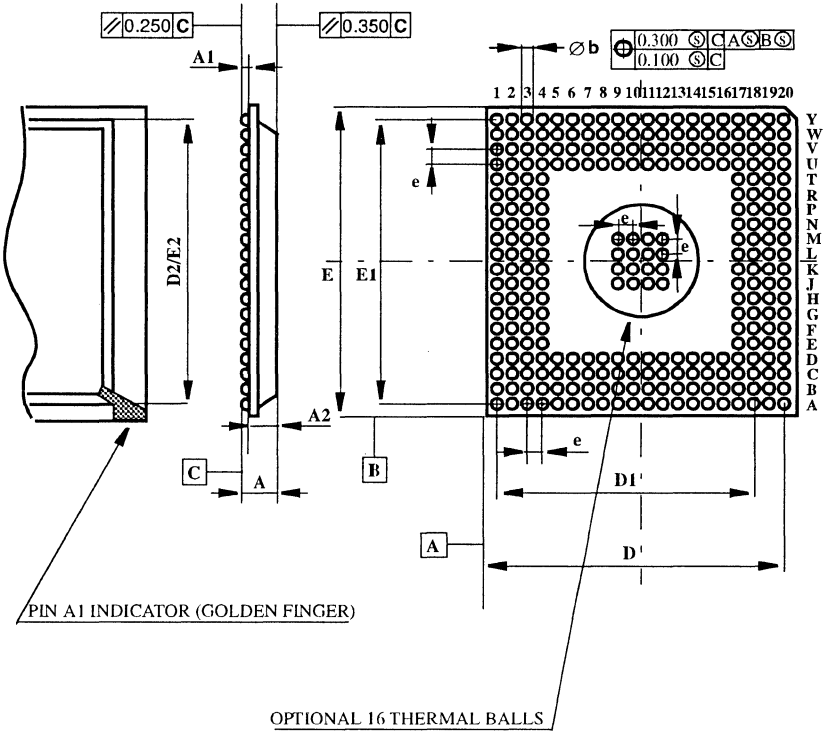


Figure 9-5. 256-pin PBGA Physical Dimensions

Table 9-14 256-Pin PBGA Package Physical Dimensions

Ref.	Millimeters		
	Typical	Min.	Max.
A		2.125	2.595
A1		0.50	0.70
A2		1.625	1.895
b		0.60	0.90
D	27.00	26.82	27.18
D1	24.13 BASIC		
D2		23.90	24.10
e	1.27 BASIC		
E	27.00	26.82	27.18
E1	24.13 BASIC		
E2		23.90	24.10

Notes:

- Drawing BGA 27x27 finished 14090116-004
- Reference document JEDEC M0151

9.5 Environmental Requirements

9.5.1 Ambient Temperature

Operation: TBD

Storage: 32 °F to 162 °F (0 °C to 70 °C)

9.5.2 Relative Humidity

Operation: 5% to 90% non-condensing

Storage: 0% to 95%

Appendix A
Layout Considerations

A.1 AGP Signal Routing

AGP signals must be carefully routed on the graphics card to meet the timing and signal quality requirements set out in the AGP Interface Specification Technical Manual, Rev.1.0. This chapter presents some general guidelines which should be followed. These guidelines are also covered in the Accelerated Graphics Port Platform Design Guide, Rev.1.0. The trace lengths mentioned are the guidelines only, and it is the responsibility of the board designer to simulate the routing in order to verify that the specification is met. All trace lengths are defined for a nominal trace impedance of 65Ω with a variation of +/-15Ω.

A.1.1 Trace Length

Signal Trace length on the AGP board should not be greater than 3.00". This requirement is derived from the flight time budget of 0.7ns for the add-in card.

CPUCLK signal length should be carefully designed to match the 0.6 ns +/-0.1ns flight time requirement in AGP specification. This trace length has to be calculated based on the special implementation requirements: number of layers, thickness of layers, width of trace, etc. A simplified formula can be used to define the propagation delay

$$Tprop\ (ps/in.) = 85\sqrt{(0,475\varepsilon r + 0,67)}$$

where εr is the relative permeability of the substrate.

A.1.2 AGP Signal Grouping and Routing

AD_STB strobe signal is grouped with the address signals AD(15:0) and C/BE[1:0] and should be routed in the middle of the above address group.

AD_STB1 strobe signal is grouped with the address signals AS(31:16) and C/BE[2:3] and should routed in the middle of the above address group.

SB_STB strobe signal is grouped with the side band address signals SBA(7:0) and should routed in the middle of the above address group

Strobe signals should be within +/-0.5" of their respective groups. The pin assignment of the AGP groups on the *3D RAGE PRO* is such that traces can be easily laid out to even tighter requirements.

Example: If strobe signal AD_STB0 = 2.5" then signal group AD(15:0), C/BE[1:0] should be from 2.0" to 3.0" in length.

Some rules will be applied to AD(31:16), SBA(7:0) and their strobes AD_STB1, ST_STB respectively.

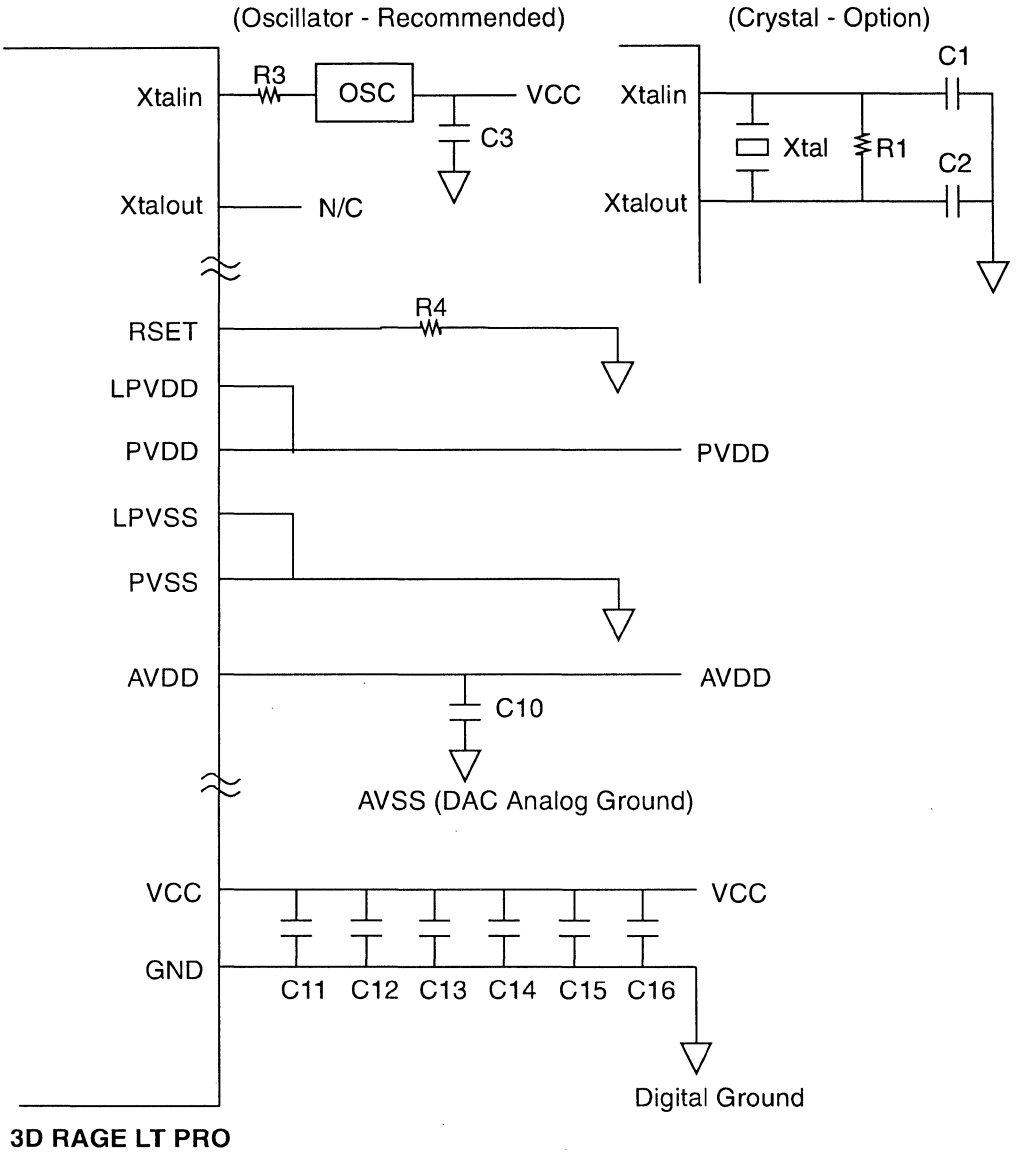
A.1.3 Signal Guarding and Trace Pitch

The following are the time critical signals which have to be guarded in order to minimize crosstalk - AD_STB0, SB_STB and PCI clock. It is intended to have a ratio of 1:4 between signal Trace Width and Trace Pitch dimensions for the guarded signals. All other signals Width to Trace pitch ratios should be minimum 1:2.

A.2 PCB Layout Considerations

Digital circuits can easily generate large ground current spikes that appear as an increase in the circuit's noise floor. You can achieve superior operation of the graphics subsystem when the coupled noise at the PLL and DAC supplies and references are minimized. The following rules of thumb adhere to the guiding premise that ground currents for digital circuits should be adequately bypassed and kept away from sensitive circuit areas and analog supplies.

- Keep digital signals away from analog signals.
- Keep digital components and wires as far away from analog sections as possible. Avoid routing digital signals through analog sections.
- Keep sensitive nets short by placing analog components close to the chip, and short wires over their respective planes. These are RSET, XTALIN, and XTALOUT.
- All power pins need by-pass capacitors placed as close to the pins as possible.
- On 4-layer designs, position the ground plane closest to the component side and the power plane closest to the solder side.
- All ground nets, VSS, AVSS, and PVSS should be joined together at one location as close to the card edge connector as possible.
- Use a low impedance ground, i.e., a continuous ground plane.
- Provide separate filtered power supplies for analog functions.
- Use capacitors and ferrite beads on RGB signals to reduce EMI for FCC requirements.
- Apply PCI specifications to routing traces from the PCI bus.



Note: For specific values, refer to the reference schematic.

Figure A-1. PCB Layout Component Diagram

A.3 Routing and Layer Assignments

A.3.1 Star Grounding

Star grounding minimizes common mode voltages caused by the noise currents traveling through common mode impedances. Common mode impedance is created when long tracks are snaked around a board. A voltage can be developed at the point on the track (away from the common ground or supply point) which a primary current flows into. If this point is then used to provide a common ground point connection for a second macro, the voltage generated by the primary current will be superimposed on the ground of the second macro even if it (second macro) does not sink or source any current.

Star grounding is an idealized grounding topology whereby macros are provided a separate and direct path to a common physical point. This point is tied to a very low impedance path directly to the supply return. In this manner, no common mode impedance can be developed between macros and no noise coupling is possible. When correctly implemented, the Star point should physically appear to have many wires leading away from it to respective macros which rely on the point to provide a potential that is common to them all.

All macros that attach to common analog grounds and supplies should have wide, short, low impedance paths to "star points". Conceptually, this should be a wire to the power supply but practicality restricts it to a point on the circuit board.

On the graphics controller, supplies are logically separated into three pairs:

- AVSS/AVDD
- PVSS/PVDD
- VSS/VCC

As the only one physical ground return exists, AVSS, PVSS, and VSS should be connected together to one point as close to the card edge connector as possible.

A.3.2 Local Bypassing

By bypassing the supply pairs (AVSS/AVDD, PVSS/ PVDD, and VSS/VCC) we minimize residual common mode currents that could couple in noise between macros in the common mode impedances that cannot be eliminated. (e.g., the wire connecting the power supply to the board).

A.3.3 Signal Referencing

Signal referencing on the graphics controller is important since not all the signals are ground referenced. The significance is in the difference between the input node and the node to which it is referenced. For nodes which handle primarily DC and LF (low frequency) information, a high-pass function in the form of either guard ring or guard island can be formed from adjacent tracks and underlying layers, respectively.

A.4 TV Output Layout Considerations

- **Component placement:** The ASIC should be placed as close as possible to the output connectors in order to minimize noise pickup and reflections due to impedance mismatch. Discrete components should be placed as close as possible to the associated ASIC pins, and vias must be avoided as much as possible.
- **Ground plane:** A **common** digital and analog **ground plane** is recommended.
- **Power plane: Separate** digital and analog **power plane** is recommended. These two planes should be connected at a single point through a ferrite bead as illustrated earlier in the implementation diagram.
- **Device Decoupling:** All decoupling capacitors should be placed as close as possible to the ASIC. Surface mount capacitors are recommended for minimum lead inductance. The trace length between groups of power and ground should be as short as possible to minimize inductive ringing.
- **Power supply decoupling:** Pairs of 22 µf and 0.1 µf capacitors are used to perform decoupling on each group of power and ground. These capacitors should be placed as close as possible to the associated ASIC pins and connected with short wide traces. The 22 µf capacitors is for low-frequency power supply ripple and the 0.1 µf capacitors for high-frequency power supply noise rejection.
- **Digital signal interconnect:** The digital inputs to the ASIC should be isolated as much as possible from the analog outputs and other analog circuitry. These input signals should not overlay the analog power plane or analog output signals.
- **Analog signal interconnect:** Digital traces must not be routed under or adjacent to the analog output traces (to avoid crosstalk from digital lines). The video output signals should not overlay the analog power plane (to maximize high frequency power supply rejection). The load resistor should be as close as possible to the ASIC to minimize reflection.

A.5 LVDS Layout Considerations

Low Voltage Differential Signalling (LVDS) will inherantly allow longer traces by cancelling common mode noise. The following layout considerations should be used in the PCB layout:

- Keep differential pairs close to each other and parallel to maximize differential benefit
- Maintain identical physical and electrical length of differential pair
- Use rounded (avoid sharp 90 degree) edges to reduce change in impedance especially for high frequencies
- Separate TTL/CMOS signals from LVDS differential signals to avoid crosstalk; increase distance, run ground trace or use differential plane between TTL/CMOS and LVDS signals
- Use ground plane between differential signal pairs on connector and cable
- Ensure proper impedance matching of PCB trace to avoid reflections
- Place termination resistor as close to the LVDS receiver as possible

Please refer to reference schematics and LVDS Receiver specifications for more details.

Index

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V

Z

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