1989

1.25μ CMOS Cell Library

Standard Cells and Function Blocks

AT&T

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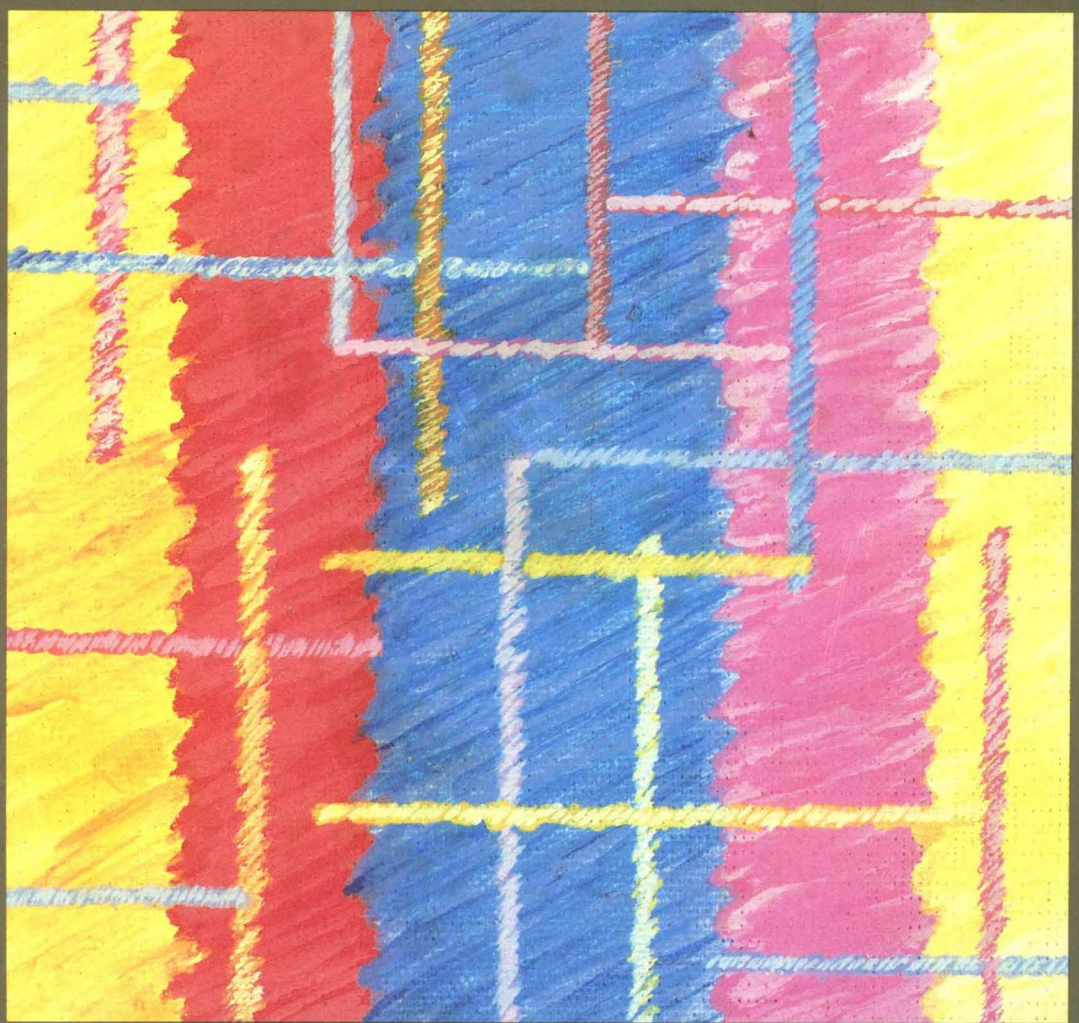

1.25μ CMOS Library

Standard Cells and Building Blocks

Second Edition

January, 1989

AT&T

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Functional Index

Section 1


AT&T

Functional Index 1.25μ CMOS Library

This section provides a quick overview of the functions available in AT&T's 1.25μ CMOS library.

I/O Buffers

Logic Cells

Functional Index

1.25μ CMOS Library

Dynamic Registers

Cell	Grids	Transistors	Clocking	Preset	Clear	Sample	Scan Equivalent	Page
DL2D1A	20	30	MS	--	--	PL	(DR2A1A)	7-12
DR2A1A	7	8	MS	--	--	--	--	7-13
DR2A1AH	8	10	MS	--	--	--	--	7-14
DR2A1B	13	18	MS	PL	--	--	--	7-15
DR2A1D	13	18	MS	--	PL	--	--	7-16
DR2A1E	13	18	MS	--	NL	--	--	7-17
DR2A1F	18	26	MS	PL	NL	--	--	7-18
DR2A1G	13	18	MS	NL	--	--	--	7-19
DR2A1I	10	14	MS	--	SPL	--	--	7-20
DR2A1J	12	12	MS	SPL	--	--	--	7-21
DR2A1M	12	12	MS	--	SNL	--	--	7-22
DR2A1N	18	26	MS	NL	PL	--	--	7-23
DR2B1A	12	18	MS	--	--	PL	--	7-24
DR2B1I	13	20	MS	--	SPL	PL	--	7-25
DR2B1J	13	20	MS	SPL	--	PL	--	7-26
DR2C1A	12	18	MS	--	--	NL	--	7-27
DR2C1I	13	20	MS	--	SPL	NL	--	7-28
DR2D1A	12	18	MS	--	--	PL	DL2D1A	7-29
DR2D1I	13	20	MS	--	SPL	PL	--	7-30
DR2E1A	12	18	MS	--	--	NL	--	7-31
DR2E1I	13	20	MS	--	SPL	NL	--	7-32

MS = Master-Slave, NL = Negative Level, PL = Positive Level, SNL = Synchronous Negative Level, SPL = Synchronous Positive Level

Static Flip-Flops and Latches

Cell	Grids	Transistors	Clocking	Preset	Clear	Sample	Scan Equivalent	Page
FB1S2AX	23	36	NE	--	--	--	--	7-33
FB1S3AX	23	36	PE	--	--	--	--	7-34
FD1N2AX	19	26	NE	--	--	NL	FL1N2AX	7-35
FD1N2JX	21	32	NE	SPL	--	NL	FL1N2JX	7-36
FD1N2MX	21	32	NE	--	SNL	NL	FL1N2MX	7-37
FD1N3AX	19	26	PE	--	--	NL	FL1N3AX	7-38
FD1N3JX	21	32	PE	SPL	--	NL	FL1N3JX	7-39
FD1N3MX	21	32	PE	--	SNL	NL	FL1N3MX	7-40
FD1P2AX	19	26	NE	--	--	PL	FL1P2AX	7-41
FD1P2JX	21	32	NE	SPL	--	PL	FL1P2JX	7-42
FD1P2MX	21	32	NE	--	SNL	PL	FL1P2MX	7-43
FD1P3AX	19	26	PE	--	--	PL	FL1P3AX	7-44
FD1P3JX	21	32	PE	SPL	--	PL	FL1P3JX	7-45
FD1P3MX	21	32	PE	--	SNL	PL	FL1P3MX	7-46
FD1S1A	9	10	PL	--	--	--	--	7-47
FD1S1B	9	12	PL	PL	--	--	--	7-48
FD1S1D	10	14	PL	--	PL	--	--	7-49
FD1S1E	9	12	PL	--	NL	--	--	7-50
FD1S1F	11	14	PL	PL	NL	--	--	7-51
FD1S1G	10	14	PL	NL	--	--	--	7-52

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Cell	Grids	Transistors	Clocking	Preset	Clear	Sample	Scan Equivalent	Page
FD1S2AX	13	18	NE	--	--	--	FL1S2AX	7-53
FD1S2BX	16	22	NE	PL	--	--	FL1S2BX	7-54
FD1S2CX	21	28	NE	PL	PL	--	FL1S2CX	7-55
FD1S2DX	17	24	NE	--	PL	--	FL1S2DX	7-56
FD1S2EX	16	22	NE	--	NL	--	FL1S2EX	7-57
FD1S2FX	19	26	NE	PL	NL	--	FL1S2FX	7-58
FD1S2GX	17	24	NE	NL	--	--	FL1S2GX	7-59
FD1S2IX	18	24	NE	--	SPL	--	FL1S2IX	7-60
FD1S2JX	16	22	NE	SPL	--	--	FL1S2JX	7-61
FD1S2KX	22	30	NE	NL	NL	--	FL1S2KX	7-62
FD1S2LX	18	24	NE	SNL	--	--	FL1S2LX	7-63
FD1S2MX	15	22	NE	--	SNL	--	FL1S2MX	7-64
FD1S2NX	20	28	NE	NL	PL	--	FL1S2NX	7-65
FD1S2OX	19	26	NE	SPL	SPL	--	FL1S2OX	7-66
FD1S3AX	13	18	PE	--	--	--	FL1S3AX	7-67
FD1S3BX	16	22	PE	PL	--	--	FL1S3AX	7-68
FD1S3CX	21	28	PE	PL	PL	--	FL1S3AX	7-69
FD1S3DX	17	24	PE	--	PL	--	FL1S3AX	7-70
FD1S3EX	16	22	PE	--	NL	--	FL1S3AX	7-71
FD1S3FX	19	26	PE	PL	NL	--	FL1S3AX	7-72
FD1S3GX	17	24	PE	NL	--	--	FL1S3AX	7-73
FD1S3IX	18	24	PE	--	SPL	--	FL1S3AX	7-74
FD1S3JX	16	22	PE	SPL	--	--	FL1S3AX	7-75
FD1S3KX	22	30	PE	NL	NL	--	FL1S3AX	7-76
FD1S3LX	18	24	PE	SNL	--	--	FL1S3AX	7-77
FD1S3MX	15	22	PE	--	SNL	--	FL1S3AX	7-78
FD1S3NX	20	28	PE	NL	PL	--	FL1S3AX	7-79
FD1S3OX	19	26	PE	SPL	SPL	--	FL1S3AX	7-80
FD1S5A	9	10	NL	--	--	--	--	7-81
FD1S5B	9	12	NL	PL	--	--	--	7-82
FD1S5D	10	14	NL	--	PL	--	--	7-83
FD1S5E	9	12	NL	--	NL	--	--	7-84
FD1S5F	11	14	NL	PL	NL	--	--	7-85
FD1S5G	10	14	NL	NL	--	--	--	7-86
FD2N1A	20	28	MS	--	--	NL	--	7-87
FD2N1J	23	34	MS	SPL	--	NL	--	7-88
FD2N1M	23	34	MS	--	SNL	NL	--	7-89
FD2P1A	20	28	MS	--	--	PL	--	7-90
FD2P1J	23	34	MS	SPL	--	PL	--	7-91
FD2P1M	23	34	MS	--	SNL	PL	--	7-92
FD2S1A	14	20	MS	--	--	--	FL2S1A	7-93
FD2S1B	17	24	MS	PL	--	--	FL2S1B	7-94
FD2S1CX	20	30	MS	PL	PL	--	FL2S1CX	7-95
FD2S1D	18	26	MS	--	PL	--	FL2S1D	7-96
FD2S1E	17	24	MS	--	NL	--	FL2S1E	7-97
FD2S1FX	19	28	MS	PL	NL	--	FL2S1FX	7-98
FD2S1G	18	26	MS	NL	--	--	FL2S1G	7-99
FD2S1I	17	26	MS	--	SPL	--	FL2S1I	7-100

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Functional Index

1.25μ CMOS Library

Cell	Grids	Transistors	Clocking	Preset	Clear	Sample	Scan Equivalent	Page
FD2S1J	16	24	MS	SPL	--	--	FL2S1J	7-101
FD2S1KX	21	32	MS	NL	NL	--	FL2S1KX	7-102
FD2S1L	17	26	MS	SNL	--	--	FL2S1L	7-103
FD2S1M	16	24	MS	--	SNL	--	FL2S1M	7-104
FD2S1NX	20	30	MS	NL	PL	--	FL2S1NX	7-105
FL1N2AX	26	36	NE	--	--	NL	(FD1N2AX)	7-106
FL1N2JX	27	38	NE	SPL	--	NL	(FD1N2JX)	7-107
FL1N2MX	27	38	NE	--	SNL	NL	(FD1N2MX)	7-108
FL1N3AX	26	36	PE	--	--	NL	(FD1N3AX)	7-109
FL1N3JX	27	38	PE	SPL	--	NL	(FD1N3JX)	7-110
FL1N3MX	27	38	PE	--	SNL	NL	(FD1N3MX)	7-111
FL1P2AX	26	36	NE	--	--	PL	(FD1P2AX)	7-112
FL1P2JX	27	38	NE	SPL	--	PL	(FD1P2JX)	7-113
FL1P2MX	27	38	NE	--	SNL	PL	(FD1P2MX)	7-114
FL1P3AX	26	36	PE	--	--	PL	(FD1P3AX)	7-115
FL1P3JX	27	38	PE	SPL	--	PL	(FD1P3JX)	7-116
FL1P3MX	27	38	PE	--	SNL	PL	(FD1P3MX)	7-117
FL1S2AX	19	30	NE	--	--	--	(FD1S2AX)	7-118
FL1S2BX	22	34	NE	PL	--	--	(FD1S2BX)	7-119
FL1S2CX	28	40	NE	PL	PL	--	(FD1S2CX)	7-120
FL1S2DX	22	32	NE	--	PL	--	(FD1S2DX)	7-121
FL1S2EX	22	34	NE	--	NL	--	(FD1S2EX)	7-122
FL1S2FX	25	38	NE	PL	NL	--	(FD1S2FX)	7-123
FL1S2GX	22	32	NE	NL	--	--	(FD1S2GX)	7-124
FL1S2IX	23	32	NE	--	SPL	--	(FD1S2IX)	7-125
FL1S2JX	21	30	NE	SPL	--	--	(FD1S2JX)	7-126
FL1S2KX	27	38	NE	NL	NL	--	(FD1S2KX)	7-127
FL1S2LX	23	32	NE	SNL	--	--	(FD1S2LX)	7-128
FL1S2MX	20	30	NE	--	SNL	--	(FD1S2MX)	7-129
FL1S2NX	25	36	NE	NL	PL	--	(FD1S2NX)	7-130
FL1S2OX	24	34	NE	SPL	SPL	--	(FD1S2OX)	7-131
FL1S3AX	19	30	PE	--	--	--	(FD1S3AX)	7-132
FL1S3BX	22	34	PE	PL	--	--	(FD1S3BX)	7-133
FL1S3CX	28	40	PE	PL	PL	--	(FD1S3CX)	7-134
FL1S3DX	22	32	PE	--	PL	--	(FD1S3DX)	7-135
FL1S3EX	22	34	PE	--	NL	--	(FD1S3EX)	7-136
FL1S3FX	25	38	PE	PL	NL	--	(FD1S3FX)	7-137
FL1S3GX	22	32	PE	NL	--	--	(FD1S3GX)	7-138
FL1S3IX	23	32	PE	--	SPL	--	(FD1S3IX)	7-139
FL1S3JX	21	30	PE	SPL	--	--	(FD1S3JX)	7-140
FL1S3KX	27	38	PE	NL	NL	--	(FD1S3KX)	7-141
FL1S3LX	23	32	PE	SNL	--	--	(FD1S3LX)	7-142
FL1S3MX	20	30	PE	--	SNL	--	(FD1S3MX)	7-143
FL1S3NX	25	36	PE	NL	PL	--	(FD1S3NX)	7-144
FL1S3OX	24	34	PE	SPL	SPL	--	(FD1S3OX)	7-145
FL2S1A	20	32	MS	--	--	--	(FD2S1A)	7-146
FL2S1B	23	36	MS	PL	--	--	(FD2S1A)	7-147
FL2S1CX	26	42	MS	PL	PL	--	(FD2S1AX)	7-148
FL2S1D	23	34	MS	--	PL	--	(FD2S1A)	7-149
FL2S1E	23	36	MS	--	NL	--	(FD2S1A)	7-150

MS = Master-Slave, NE = Negative Edge Triggered, NL = Negative Level, PE = Positive Edge Triggered, PL = Positive Level, SNL = Synchronous Negative Level, SPL = Synchronous Positive Level

Cell	Grids	Transistors	Clocking	Preset	Clear	Sample	Scan Equivalent	Page
FL2S1FX	25	40	MS	PL	NL	--	(FD2S1AX)	7-151
FL2S1G	23	34	MS	NL	--	--	(FD2S1A)	7-152
FL2S1I	23	34	MS	--	SPL	--	(FD2S1A)	7-153
FL2S1J	21	32	MS	SPL	--	--	(FD2S1A)	7-154
FL2S1KX	26	40	MS	NL	NL	--	(FD2S1AX)	7-155
FL2S1L	23	34	MS	SNL	--	--	(FD2S1A)	7-156
FL2S1M	21	32	MS	--	SNL	--	(FD2S1A)	7-157
FL2S1NX	25	38	MS	NL	PL	--	(FD2S1AX)	7-158
FS0S1A	5	8	--	--	--	--	--	7-159
FS0S1D	6	10	--	--	PL	--	--	7-160
FS0S7A	5	8	--	--	--	--	--	7-161
FS1S1A	7	12	PL	--	--	--	--	7-162
FS1S3A	15	24	PE	--	--	--	--	7-163

MS = Master-Slave, NE = Negative Edge Triggered, NL = Negative Level, PE = Positive Edge Triggered, PL = Positive Level, SNL = Synchronous Negative Level, SPL = Synchronous Positive Level

Parameterized Macrocells

Boundary Scan Cells

Design Considerations

Section 2

AT&T

Contents - Section 2

This book contains the ASIC (Application Specific Integrated Circuit) design information using AT&T's advanced 1.25µ twin-tub CMOS technology. It can be fabricated in single-level or double-level metal technology. The standard cells in this catalog are available in two layout styles. In one style, the cells were made as small as possible. The other style, cells were optimized for performance, and as a result occupy more area than the small cells. The contrast is illustrated below:

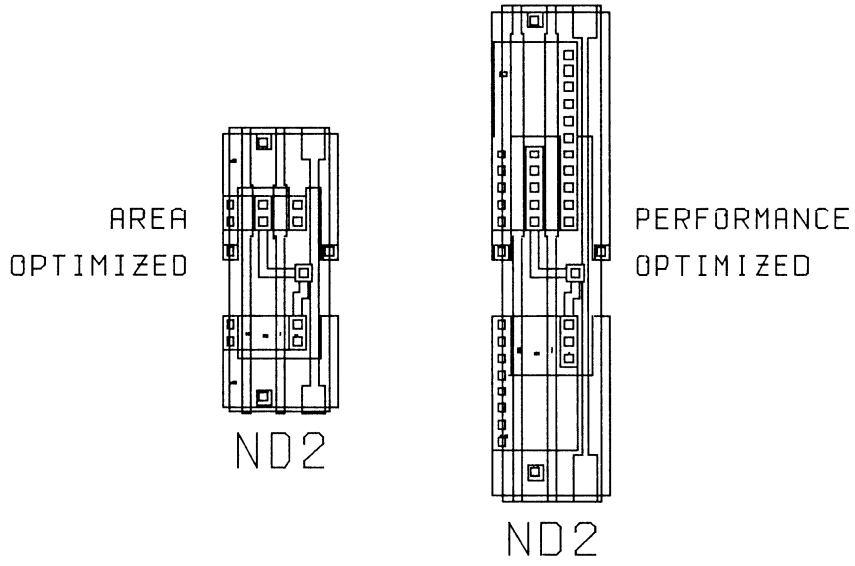

Table 1 - Cell Library Comparison

Item	Area Optimized	Performance Optimized
Cell Height	42.625µ	74.00µ
P-Transistor		
Mask Length	1.75µ	1.75µ
Mask Width	5.00µ	28.00µ
N-Transistor		
Mask Length	1.25µ	1.25µ
Mask Width	5.00µ	20.00µ

The two libraries allow you to make trade-offs between performance and chip size in your design. These trade-offs are discussed in the sections that follow.

Nominal propagation delays are quoted in the 1.25µ Standard Cell Library. To determine exact delays under other conditions, the ADVICE (AT&T's version of SPICE) simulation program should be used with the following conditions:

Table 2

CONDITIONS FOR SIMULATIONS			
CASE	TEMPERATURE	PROCESS FILE	POWER SUPPLY
Worst Case Fast	0°C	APROHC.DAT	5.5 Volts
Nominal	25°C	APRONC.DAT	5.0 Volts
Worst Case Slow	100°C	APROLC.DAT	4.5 Volts

Throughout this catalog, "temperature" always refers to *junction* temperature, and not the ambient. Junction temperature is generally higher than the ambient, due to the fact that the package acts as an insulator, and impedes the dissipation of heat from the silicon to the ambient environment. The difference between the junction and ambient temperatures is dependent on the amount of power the device dissipates, the package type, and the amount of air circulation in the surrounding environment.

The temperature used in worst case simulations is application dependent. The range 0 ° C to 100 ° C is common, however, the minimum and maximum limits are -40 ° C to 125 ° C.

An alternate method to determine worst case propagation delays (although not as accurate as running ADVICE) is to use de-rating factors. A de-rating factor is simply a multiplier of the nominal delay:

$\tau = \tau_{NOMINAL} \times D_{TV} \times D_P$

where

D_{TV} is the de-rating factor for temperature and voltage.

D_P is the de-rating factor for process variation.

These de-rating factors for 1.25µ CMOS can be found in Tables 3 and 4:

Table 3 - Derating for Processing

PROCESS CONDITIONS	DE-RATING FACTOR
Slow	1.31
Nominal	1.0
Fast	0.75

Table 4 - Power Supply and Temperature Derating

		POWER SUPPLY VOLTAGE (VDD)				
		4.50V	4.75V	5.00V	5.25V	5.50V
TEMPERATURE	-40°	0.77	0.73	0.68	0.64	0.61
	0°	1.00	0.93	0.87	0.82	0.78
	25°	1.14	1.07	1.00	0.94	0.90
	85°	1.50	1.40	1.33	1.26	1.20
	100°	1.60	1.49	1.41	1.34	1.28
	125°	1.76	1.65	1.56	1.47	1.41

The recommended maximum operating conditions and absolute maximum ratings for the 1.25µ CMOS library and technology are as follows:

RECOMMENDED MAXIMUM OPERATING CONDITIONS FOR 1.25µ CMOS

Power Supply Voltage	VDD – VSS = 5V
Input Voltages	(VSS – 0.3V) to (VDD + 0.3V)
Junction Temperature	-40°C to 125°C

ABSOLUTE MAXIMUM RATINGS FOR 1.25µ CMOS

Power Supply	VDD – VSS ≤ 7.0V
Input Voltage	VSS to VDD (for 6.1V < VDD – VSS ≤ 7.0V)
Storage Temperature	-40°C to 125°C

The most accurate way to estimate the power a custom CMOS IC will dissipate is to develop an LSL (i.e., netlist) and a complete test vector set, and then let the MOTIS3 circuit simulator do the calculation for you. However, it is often the case that you would like to know well beforehand approximately how much of your board power budget to allocate to your proposed custom device. It is for this reason the following worksheet was developed; *it should only be used as a guideline.*

AC Power

CMOS typically dissipates very little DC power. Most of the power dissipation arises from current required to repeatedly charge up and discharge transistor gates and parasitic capacitances. Accordingly, the expression for the AC power dissipation is:

$$P = C \times V^2 \times F$$

Where:

C = The total capacitance being charged and discharged.

V = The power supply, typically the upper limit for this calculation.

F = The frequency at which the capacitance is being charged and discharged.

Calculating the AC Power for Internal Gates

Estimating the AC power for the chip's internal logic gates is straightforward. The equation for the calculation is:

$$P_{Internal} = PG \times N \times F \times A$$

Where:

PG = Power per gate. This is the approximate power the average primitive logic gate will dissipate at a specified frequency. This factor for the two libraries is:

6μW /gate/MHz for the area-optimized cells, and

10μW /gate/MHz for the performance-optimized cells.

N = The total number of gates. The factors listed above assume that you are going to use equivalent, primitive logic gate count to do this estimate. N represents the total number of those gates.

F = The operating frequency. Here, the frequency refers to the rate at which most of the nodes in the circuit can change, typically the clock frequency.

A = The activity of the circuit. This term is an attempt to acknowledge that not all of the data will in the circuit will be changing at all times. This, of course, is heavily dependent on the application.

As an example, 5,000 gates in a synchronous design being clocked at 8MHz while using the area-optimized cells will dissipate:

$$P_{Internal} = 6\mu W \times 5{,}000 \times 8MHz \times 0.2 = 48mW$$

assuming a 20% activity factor.

Estimating the AC Power for the Output Buffers

Another important component of the total power dissipation can be attributed to the chip's output capacitances. Here, the power would be calculated as:

$$P_{External} = VDD^2 \times C_L \times F \times A$$

Where:

VDD = The upper limit on the allowed value for the power supply, typically 5.5 Volts.

C_L = The sum of all capacitances on all chip outputs.

F = The maximum frequency at which the outputs will change. Normally, one half of the clock frequency.

A = The % activity of the output nodes. This may or may not be the same as the internal activity factor, depending on the application and the circuit.

DC Power

Certain CMOS circuits, by necessity, dissipate DC power. The most common of these are CMOS input buffers that convert TTL levels at the input of the chip to CMOS levels internally. The catalog pages describing these buffers includes power information. It is suggested that you refer to those pages when considering power, as the DC power dissipated by the input buffers may turn out to be significant, depending on your buffer selection and your requirements.

If you are having some special circuitry built for you, it may also need to dissipate some DC power. Again, it may be important to include in the chip power calculation, especially if you have a tight power budget.

Total Chip Power - A Summary

In summary, there are three important contributors to the power dissipation of a CMOS IC that should be included when making an early estimate:

1. The AC power dissipated by the internal gates.
2. The AC power dissipated by the output capacitance.
3. The DC power dissipated by various 'unusual' circuits, most notably the TTL-compatible input buffers.

It is worth repeating that the MOTIS3 circuit simulator will make an accurate calculation of the chip AC power. The techniques presented in this section should only be used for estimation.

The following design practices are suggested for when it is important to obtain the highest possible performance:

1. Use the performance-optimized library.
2. Keep the logic gate depth shallow between latch points.
3. Use low fan-in logic gates. (Fan-in is defined as the number of inputs. For example, an ND2 has a fan-in of 2; an NR4 has a fan-in of 4.) If you are using AT&T's FDS to synthesize combinatorial logic, limit the MAX_FANIN variable to 2 or 3.
4. Plan your chip architecture to do as much parallel processing as possible.
5. Minimize the occurrence of strings of alternating NAND's and NOR's.
6. Avoid the use of high-drive buffers when driving a low fanout.
7. Avoid circuit designs that have highly loaded gates in the critical path. A gate delay will increase as the capacitive load is increased on the output of the gate. The primary sources of load capacitance are routing capacitance and the capacitance of the transistors on the gates being driven.
8. Duplicate logic to reduce fanouts.
9. Use fast adder design techniques - for example, carry look-ahead.
10. Avoid placing heavy loads on flip-flops and latches. On most flip-flops and latches, the Q and QN outputs are unbuffered. Since QN is derived from Q, a high fan-out on QN will slow down Q even if Q is lightly loaded.
11. Some of the cells in the library are available with higher drive capabilities - for example, an ND2H has twice the drive capability of the ND2. An ND2S has 4 times the drive of the ND2. These higher power cells should only be used to drive high fanouts.
12. In general, small macrocells will run faster than large ones. For example, two 1,024 x 8 SRAM's will run faster than one 1,024 x 16 SRAM. In a similar manner, a block of logic implemented with many PLA's will run faster than if it were implemented with one large PLA.

The following design practices are suggested for when it is important to minimize chip area:

1. Use the area-optimized library.
2. Design with repeated, regular subcircuits whenever possible. In layout, each of these subcircuits could be placed and routed very efficiently, and then repeated to form a larger circuit.
3. If you are using AT&T's FDS to synthesize combinatorial logic, experiment with the MAX_FANIN option. By varying MAX_FANIN from its default value of 9, you may be able to synthesize smaller versions of the intended logic.
4. Whenever possible, use both Q and QN signals (which have been made available on each flip-flop and latch) to form inversions.
5. Apply DeMorgan's theorem to minimize the use of inverters.
6. Direct translations from TTL diagrams may be inefficient. Instead, the logic should be designed directly from the cell library.
7. In general, there should be no need to connect any cell input directly to VDD or VSS. Instead, find the cell with the proper number of inputs and function, or have a new cell designed.
8. If you need a flip-flop with a multiplexer on the input, consider using the scan-test version (i.e., the 'FLxSxxX' variety of cells.)
9. Experiment with PLA's and ROM's. In some cases, logic implemented with a PLA or a ROM may offer a significant size advantage over a standard cell implementation.
10. Be aware of the overhead present in macrocells. For example, a single 10K SRAM occupies significantly less area than ten 1K SRAM's, due to the latches, clock drivers and decoders in each SRAM block.
11. A single large block is better than many small blocks doing the equivalent function for another reason - in layout, there is often a 'moat' of inefficient routing around each block. This is due to the fact that the terminal positions on the block cannot be rearranged to make the routing more dense. Therefore, when planning a chip architecture for minimal area usage, try to use a few very large blocks rather than many small blocks.

Presented in this section is a simple technique with which to do an early estimate of the size of a prospective standard cell chip. It is intended for use early in the design to make system architecture-related or partitioning decisions. It is important to understand that the only way to *really* determine a chip size is to lay it out. Using the technique below will only get you to within ±10% per side.

Using Grid Count to Estimate Chip Size

The basic unit used for estimating chip size is the standard cell grid. The width of a standard cell is measured in grids; for example, a 4-input NAND gate is 5 grids wide. An approximate chip size can be easily calculated from the total number of grids in the circuit.

$$S = \sqrt{k_1 \times N^2 + k_2 \times N + 1.2 \times A_{SP}} + H_B$$

Where:

- S = Length of one side of the chip (step and repeat), in thousandths of an inch (mils).
- N = The total number of grids in the LSL.
- k_1, k_2 = Constants that account for routing and overhead in this chip area calculation. These constants are different for the types of cells and layout styles used.

  For the area-optimized cells laid out in single level metal (SLM):

  $$k_1 = 1.2 \times 10^{-5}, k_2 = 1.0$$

  For the performance-optimized cells laid out in single level metal (SLM):

  $$k_1 = 1.0 \times 10^{-5}, k_2 = 1.27$$

  For the area-optimized cells laid out in double level metal (DLM):

  $$k_1 = 1.1 \times 10^{-5}, k_2 = 0.7$$

  For the performance-optimized cells laid out in double level metal (DLM):

  $$k_1 = 1.0 \times 10^{-5}, k_2 = 1.0$$

- A_{SP} = The area of any special blocks, for example RAM or PLA. The area information for these can be obtained from the appropriate datasheets in this catalog.
- H_B = The height of the buffer ring that surrounds the chip, including power bus, saw-grid, and alignment features. The value of H_B depends on whether or not you are pad limited:

  For a pad limited chip:

  $$H_B = 55 \text{ mils.}$$

  For a chip that is not pad limited:

  $$H_B = 35 \text{ mils.}$$

By way of an example, an area estimate for a chip requiring 20,000 grids using the area-optimized standard cells in single level metal technology is determined as follows:

$$S = \sqrt{1.2 \times 10^{-5} \times 20{,}000^2 + 1.0 \times 20{,}000} \quad + 35 = 192 \textit{ mils} \pm 10\ \%$$

A more complete relationship between grids and chip size(non-pad limited) is illustrated in Figure 1.

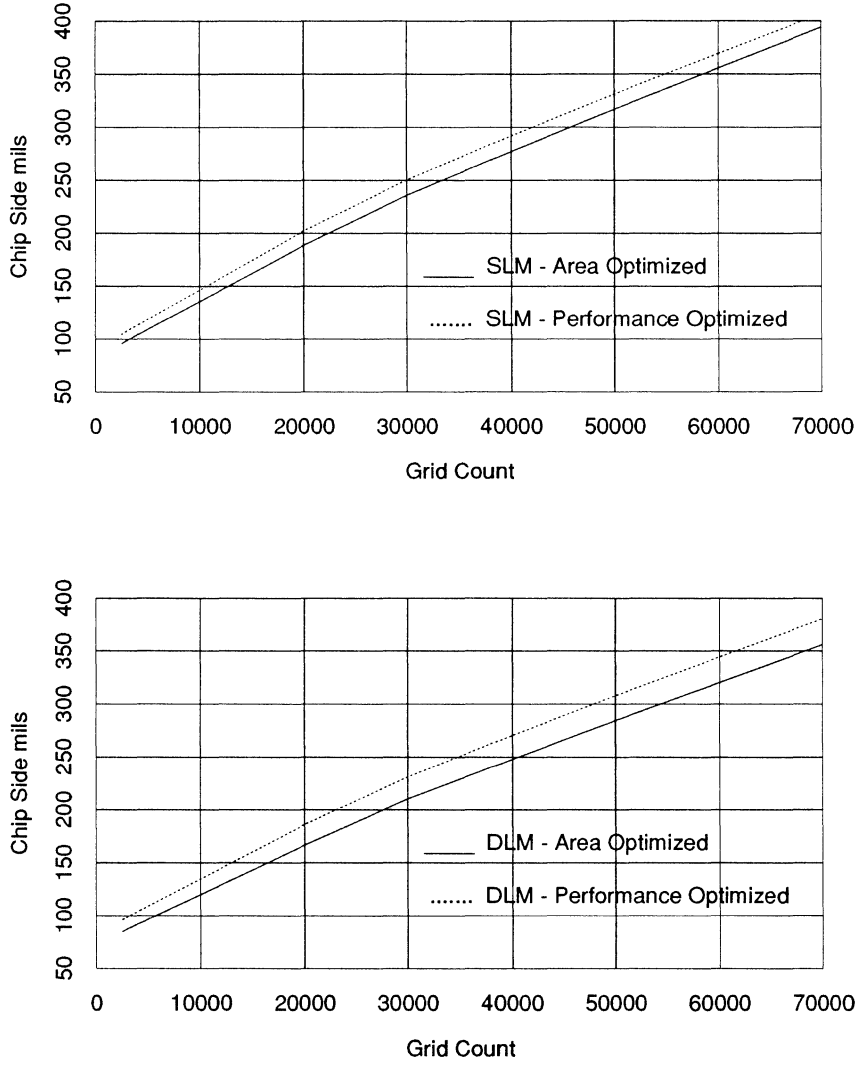

Figure 1. Chip Size as a Function of Grid Count

Estimating the Grid Count before LSL is Available

A grid count is not always available when a chip size estimate is desired. Early in the design, the only indication of the complexity of the chip is often a count of the number of equivalent logic gates. To help you convert from gates to grids, or MOS transistors, the appropriate conversion factors are shown in the following table.

Table 5 - Standard Cell Conversion Factors

	Logic Gates	Grids	Transistors
1 Logic Gate =	1.0	2.6	4.0
1 Grid =	0.38	1.0	1.5
1 Transistor =	0.25	0.67	1.0

Chip Size Limits

There are limits on the range of practical chip sizes. At the lower end of the range, the chip size is limited by the placement of the bond pads on the chip and the allowed length of the wire bonds. The more pins, the larger the minimum chip. At the upper end of the range, limits are imposed by the physical dimensions of the package itself.

The range of minimum and maximum chip sizes for standard packages is summarized on the following page.

Table 6 - Minimum and Maximum Chip Sizes

Package Type	# Pins	Minimum (mils)		Maximum (mils)	
		X	Y	X	Y
Plastic DIP	40	125	125	380	380
	32	110	110	380	380
	28	105	105	330	460
	24	95	95	360	440
	20	90	90	140	300
	18	80	130	130	280
	16	80	80	150	340
Plastic Leaded Chip Carrier	100	230	230	450	450
	84	200	200	405	405
	68	180	180	410	410
	44	130	130	350	350
Plastic SOJ	28	105	105	190	350
	20	90	90	190	350
	16	80	80	190	220
Plastic Quad Flat Package	132	285	285	380	380
	100	230	230	405	405
	84	200	200	340	340

Package Type(1)	# Pins	Minimum (mils)	
		X	Y
Ceramic DIP	48	140	140
	40	125	125
	32	110	110
	28	105	105
	24	95	95
	16	80	80
Ceramic Pin Grid Array	180	370	370
	149	315	315
	133	285	285
	125	270	270
	120	265	265
	100	230	230
	68	175	175
	64	165	165

Note:

1. Due to wide variations in package cavity sizes, chip sizes for ceramic packages other than minimum are available upon request.
2. See Section 3 for more detailed packaging information.

CAD Support Files

A complete set of CAD support files for the 1.25µ CMOS Standard Cell Library is available through the distribution of SysCAD and ADS (AT&T Design System). These files are generated to support the use of several CAD programs for schematic capture, logic and timing simulation, and chip layout. Please contact your AT&T representatives for more information.

Packaging Summary

Section 3

AT&T

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Summary of Package Types: Plastic

Through Hole Mounted Plastic Packages with 100 Mil Pin Spacing

Plastic DIP						
No.	Θ	Chip Size (mils)		Pin Inductance (nH)		Dimension
Pins	(°C/W)	Min	Max	Min	Max	(mils)
16	73	80x80	150x340	4	9	320x810
18	68	80x130	130x280	4	10	320x920
20	64	90x90	140x300	4	12	320x1040
24	57	95x95	360x440	9	15	615x1270
28	52	105x105	330x460	9	16	615x1470
32	49	110x110	380x380	9	18	615x1580
40	42	125x125	380x380	9	20	615x2070

Surface Mounted Plastic Packages with 50 Mil Pin Spacing

SOJ						
No.	Θ	Chip Size (mils)		Pin Inductance (nH)		Dimension
Pins	(°C/W)	Min	Max	Min	Max	(mils)
16	90	80x80	190x220	4	6	355x408
20	85	90x90	190x350	4	7	355x508
28	75	105x105	190x350	4	9	355x708

Plastic Leaded Chip Carrier						
No.	Θ	Chip Size (mils)		Pin Inductance (nH)		Dimension
Pins	(°C/W)	Min	Max	Min	Max	(mils)
44	55	140x140	350x350	7	10	695x695
68	45	180x180	410x410	11	15	995x995
84	43	200x200	405x405	13	19	1190x1190
100	40	230x230	450x450	16	22	1395x1395

Surface Mounted Plastic Packages with 25 Mil Pin Spacing

Plastic Quad Flat Packages						
No.	Θ	Chip Size (mils)		Pin Inductance (nH)		Dimension
Pins	(°C/W)	Min	Max	Min	Max	(mils)
84	68	200x200	340x340	8	12	810x810
100	56	230x230	405x405	10	14	910x910
132	42	285x285	380x380	13	18	1100x1100

Notes:

1) Θ (° C/W) is in still air ambient.
2) Capacitance: Maximum 5pF/pin (not including buffer and pad.)
3) Resistance: Pin to Pad Maximum 0.15 ohm/pin (nominal about 0.09 ohm.)
4) Inductances are estimated worst-case values.
5) The information listed above is meant to be used as a guideline only. For more detailed information regarding your requirements, please consult your AT&T representative.

Summary of Package Types: Ceramic

Through Hole Mounted Ceramic Packages with 100 Mil Pin Spacing

Ceramic DIP						
No.	Θ	Chip Size (mils)		Pin Inductance (nH)		Dimension
Pins	(°C/W)	Min	Max	Min	Max	(mils)
16	64	80x80		4	9	325x815
24	56	95x95		9	15	620x1212
28	51	105x105	See	9	16	620x1412
32	46	110x110	Note	9	18	620x1625
40	35	125x125	(6)	9	20	620x2020
48	31	140x140		11	22	620x2420

Ceramic Pin Grid Array						
No.	Θ	Chip Size (mils)		Pin Inductance (nH)		Dimension
Pins	(°C/W)	Min	Max	Min	Max	(mils)
64	41	165x165		6	16	1000x1000
68	34	175x175		6	17	1100x1100
100	24	230x230		7	20	1320x1320
120	24	265x265	See	7	20	1320x1320
125	24	270x270	Note	7	20	1320x1320
133	24	285x285	(6)	7	20	1320x1320
149	17	315x315		8	23	1560x1560
180	17	370x370		8	23	1560x1560

Summary of Package Types: Ceramic

Surface Mounted Ceramic Packages with 50 Mil Pin Spacing

Ceramic Chip Carrier - Leaded						
No.	Θ	Chip Size (mils)		Pin Inductance (nH)		Dimension
Pins	(°C/W)	Min	Max	Min	Max	(mils)
68	30	180x180	See	11	16	1080x1080
100	20	230x230	Note (6)	13	20	1365x1365

Socket Mounted Ceramic Packages with 50 Mil Pin Spacing

Ceramic Chip Carrier - Leadless						
No.	Θ	Chip Size (mils)		Pin Inductance (nH)		Dimension
Pins	(°C/W)	Min	Max	Min	Max	(mils)
68	30	180x180	See	11	16	996x996
100	20	230x230	Note (6)	13	20	1281x1281

Notes:

1) Θ (°C /W) is in still air ambient.
2) Capacitance: Maximum 5pF/pin (not including buffer and pad.)
3) Resistance: Pin to Pad Maximum 0.15 ohm/pin (nominal about 0.09 ohm.)
4) Inductances are estimated worst-case values.
5) For ceramic packages, minimum chip dimensions are set by bond pad spacing rules and wire bond rules. Maximum chip dimensions are set by ceramic package layout rules, or in the case of very large chips, by reticle technology.
6) Due to wide variation in package cavity sizes, chip size other than minimum are available upon request.
7) The information listed above is meant to be used as a guideline only. For more detailed information regarding your requirements, please consult your AT&T representative.

Reliability & Quality

Section 4

AT&T

Contents - Section 4

In all AT&T products and services, quality is a major thrust. AT&T's policy is to provide products and services that meet the quality expectations of our customers. In addition, AT&T actively pursues ever-improving quality through programs that enable each employee to do the job right the first time. Each employee is a part of the system that allows AT&T to provide high quality products with long term reliability.

AT&T ASIC devices are no exceptions to the rule when quality and reliability are considered. The increasing demands on chip complexity and the constantly shrinking design rules dictate the need for defect-free product. This section describes the procedures adhered to during the design, manufacture, and shipment of AT&T ASIC devices which guarantee the highest quality and assure long term reliability.

It is often the case that quality and reliability are used inter-changeably. At this point, it would be beneficial to define each term and see how each fits into the overall picture. A quality product is one which is designed to be manufactured to perform to a predetermined degree of excellence. In addition to being a quality product, however, a reliable product is one which performs correctly *and* does not produce failures in time which exceed some predetermined limits. It will become apparent to the reader that there is a *quality-by-design* concept evident in not only the AT&T ASIC designs but also in the manufacture of their prototypes. This concept further translates into the reliability program AT&T uses to assure customer product at a reliability level which meets or exceeds customer needs.

From the start of the chip design, quality is built into the process. The use of CAD tools along with a thoroughly precharacterized cell library help to assure a high design success rate. Moreover, each AT&T design engineer presents their final design in a *peer design review* format. During these design reviews, a large team composed of experienced designers review all aspects of the chip design. It is not until each design passes such a review that approval is given to generate masks for manufacture of device models.

Special engineering teams handle all aspects of the models manufacture from the generation of mask sets through the wafer fabrication to the ultimate assembly of packaged devices. Masks are manufactured in the AT&T mask shop which boasts a reputation for delivering the highest quality masks. To maintain the high quality of the masks, special protective layers called pellicles are used. Pellicles are mounted on the front and back surfaces of the masks to prevent any debris from being replicated on the wafers during the photolithography processes. *MASKVIEW*, a CAD tool developed by AT&T, can be used at any time to verify the correctness of the masks against the databases used to generate them. This further enables the job to be done right the first time, thus saving time and money.

The prototype (or "prove-in) lots are fabricated in AT&T cleanrooms; these are the same cleanrooms in which the final proven-in devices will be manufactured. This concept of using manufacturing facilities for prototype fabrication helps to provide for an easier transition into product manufacture. There are no "surprises" that might be encountered moving from one fab line to another. One twenty-five wafer lot is fabricated for each device prove-in. This lot provides wafers for prototype models on a quick turnaround basis. Twenty-four hour engineering coverage helps to assure that these prove-in lots are processed as rapidly as possible and without problems. Parameters identified as important to the manufacture of the product lots are closely monitored for prove-in lots. Special test patterns which assess the electrical and cosmetic quality of the processing for each lot are tested once processing is completed. This information is used to generate databases describing the process quality over an extended period of time. In addition, this information is also used to quickly report process parameters to the fab lines since prove-in lots serve as *health of the line* lots because they are processed more rapidly than production lots.

Any failure mode analysis of the prove-in lots that may be required is done by resident engineers who work closely with both the device prove-in engineers and AT&T product engineers. Models are assembled from prove-in wafers. They are tested and then shipped to the customer for evaluation. The protection of masks, fabrication of prove-in lots in the manufacturing environment, close attention to process parameters, and expert failure mode analysis are some of the aspects that are built into device prove-in to help assure the ultimate high quality of the code in manufacture.

Defect density and electrical resistivity measurements are made on each wafer before it is used for the manufacture of an integrated circuit. Mask alignment, critical dimensions and pattern quality are measured and/or inspected on wafers at the photolithography operations. Final sizes are measured and the quality of patterns transferred after etching are inspected. Polysilicon, dielectric materials, and metallization levels are monitored for defect densities, particle checks, and thickness uniformity. These in-process monitors are reviewed on a lot-by !ot basis. In addition, these process monitors are also used to maintain the fabrication lines at peak operating levels by identifying and correcting any problems as they occur. Electrical parameters are measured on sample wafers from each completed lot. Certain specifications, especially relating to electrical channel lengths, must be met before a lot can be shipped for package assembly.

In package form, a process referred to as burn-in is performed to weed out potentially weak devices. During burn-in, high temperature and high voltage are used to stress the devices and accelerate the failure rate. The circuit may be clocked at either 100kHz or 1MHz to additionally stress the device during burn-in. Burn-in accelerates the initial dropout, or 'infant mortality' rate and helps to ensure that potentially unreliable devices do not find their way into customer product.

AT&T ships devices under a reliability program to meet customer requirements, typically 100 FITS at 40 years. This assurance of reliability, however, can not occur until the integrated circuit family (package type, process technology, etc) has undergone a technology qualification which demonstrates the capability of achieving these high levels of reliability. Such technology qualifications are the responsibility of the appropriate AT&T design organizations. Once a process technology is qualified, changes made to the process require that some re-qualification testing be done.

To begin the qualification procedures, samples are processed, tested, screened, and inspected in the usual manner. This means that no special attention is given to the samples that would distinguish them from ordinary product. Samples used for qualification are composed of approximately equal numbers from three wafer processing lots. When the devices have been stressed and then tested, an electrical failure is defined as a device which does not meet data sheet or end-of-life test specifications. It is imperative that all electrical failures are confirmed for a second time and then analyzed for their causes of failure.

Intermediate Qualification

An intermediate qualification of a new process, demonstrating 300 FITS in 10 years, can be done to allow the shipment of product prior to devices passing a full qualification. Devices are shipped under this intermediate qualification on a limited basis with the requirements that customers are notified of this special status and that intermediate devices are codemarked appropriately. Intermediate devices are shipped for an amount of time limited to six months from the initial shipment of coded devices.

Full Qualification

A new process technology for MOS devices in plastic packages is considered to be fully qualified when all AT&T IC Reliability Standards have been met. The successful completion of all appropriate qualification procedures demonstrates a 100 FIT, 40 year life for product fabricated on a particular wafer process line. Each fab line is separately qualified for each process technology. This assures that the customer receives the identical quality product regardless of its location of manufacture.

Changes made to a qualified process technology must be followed by re-qualification testing. Although it is not necessary that all qualification tests be repeated, a subset of the original tests are done for passivation, metallization, and diffusion changes.

New package qualification, using chips from qualified process technologies, requires additional tests. Since AT&T has package assembly locations throughout the world, each location is fully qualified to assure identical quality of all products to our customers.

Reliability qualification tests and test methods used by AT&T are tabulated on the following page.

Qualification Tests

Test	Test Description	Method Note(1)
1. LT-1 or LT-2	High Temp. Op. Bias, 125°C High Temp. Op. Bias, 150°C	M-1005
2. CL	CLASS Note (2)	L-757214
3. BH	Temp.-Humidity-Bias	A-497337
4. SB	Steam Bomb	PI-12.163
5. TC	Temp. Cycling	M-1010
6. TS	Thermal Shock	M-1011
7. MR	Moisture Resistance	M-1004
8. LK	Gross/Fine Leak	M-1014
9. SA	Salt Atmosphere	M-1009
10. WV	Internal Water Vapor	M-1018
11. RT	Low Temp. Aging	L-757203
13. SE	Soft Error Rate	M-1032
14. PS	Photo Sensitivity	Note (3)
15. FL	Flammability & O_2 index	UL 94 & ASTM 2863-77
16. SR	Solvent Resistance	M-2015
17. IV	Internal Visual	M-2014
18. PD	Physical Dimensions	M-1016
19. SD	Solderability	M-2003
20. MS	Mechanical Shock	M-2002
21. VF	Variable Freq. Vib.	M-2007
22. CA	Const. Acceleration	M-2001
23. SQ	Mechanical Sequence	Note (4)
24. LI	Lead Integrity	M-2004
25. BS	Bond Strength	M-2011
26. DS	Die Shear Strength	M-2019
27. XR	X-ray	M-2012
28. TQ	Lid Torque	M-2024
29. ES	ESD	X-19435
30. LU	Latch-up	L-757185

NOTES:

1) M-XXXX.X denotes test method as specified in MIL-STD-883.
2) CLASS (AT&T-BL L-757214) Component and Lead Assembly Simulation Sequence
3) Applies only to product packaged in white ceramic or white plastic.
4) Mechanical shock, variable frequency vibration, constant acceleration and gross/fine leak tests performed in sequence with the same samples.

After the devices meet the AT&T's qualification requirements, they are committed to production. Their continued long-term reliability is assured to be at the maximum failure rate of 100 FITS after 40 years of life. A comprehensive reliability monitoring program administered by AT&T guarantees that customer product is maintained at this reliability level.

The AT&T reliability testing program provides for two-level testing. Level 1, performed on a six weeks basis, is equivalent to 40 year life. Level 2, performed on a weekly basis, provides on-going reliability data ensuring 300 FIT, 10 year life. This difference does not imply a variation in the reliability levels of shipped customer product. Since all product is manufactured in the same rigid manner, level 1 provides data to evaluate devices against long term goals while level 2 provides early warning should a reliability problem occur.

To ensure that all products are completely covered under this reliability program, products are grouped together by basic design style and function. These groupings, or families, include memories, microprocessors, digital signal processors, codec/analog devices, and ASIC devices. Further division in each family occurs as individual test groups are designated based on those factors likely to be affected by each test performed. Examples of individual test groups are wafer fab lines, package materials, package types, and package assembly lines.

Some testing times are very long as previously noted. In some cases, an entire week's shipment might ordinarily be delayed pending the completion of testing of some reliability samples. To avoid this situation, and to assure the best delivery to customers, early shipment privileges are given to those testing groups which consistently demonstrate good reliability levels. Early shipment qualification is based on a weighted average of the four most recent lots. This level is continually monitored with each new test; early shipment privileges can be lost if the weighted average exceeds a predetermined limit. There will be no compromise in reliability assurance for the sake of early shipment.

Most product is sampled under the 'normal sampling' procedure. This means that a representative device is chosen from the test group to represent all other codes in the same test group. In some cases, however, codes in a test group may be tested on a 'lot by lot' basis because previous samples exceeded the predetermined failure limit. Each device in the test group must individually pass the reliability test.

Devices which do not pass reliability testing undergo failure analysis to determine if they are truly reliability failures. Full characterization of all defectives is done to evaluate failure modes and causes. These characterizations impact on product reliability and future product shipping status.

Data, segregated by families and testing groups, is generated and reviewed on a weekly and quarterly basis for both level 1 and level 2 testing. This data allows all samples to be traced back to wafer fab line and package assembly location.

Summary

AT&T is committed to providing our customers with the highest quality product. ASIC devices are designed and manufactured to the highest quality; their long term reliability is assured to be less than or equal to 100 FITS in 40 years of life. This is accomplished by design, process, and product engineers working together. In addition to these human resources, the finest software, highly innovative procedures, state-of-the-art manufacturing facilities, and good discipline contribute to the high quality product available to our customers.

I/O Buffers

Section 5

AT&T

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The AT&T 1.25μ CMOS Standard Cell Library offers a rich selection of circuits to interface your chip with the outside world. This selection guide should help you quickly see what is in the library, and allow you to select the circuit that best fits your needs.

There are three types of I/O buffers in the library, namely:

1) Input Buffers
2) Output Buffers
3) Bidirectional Buffers

Input Buffers

Each input buffer cell is complete in that it contains a bonding pad, an ESD protection network, power bus and the appropriate circuitry. Table 1 is a summary of the input buffers available in the 1.25μ CMOS library.

Table 1 - 1.25μ CMOS Input Buffers

INPUT BUFFER TYPE	NAME	PROPAGATION DELAY *
Inverting CMOS Level	BIM03	3ns
	BIM05	5ns
	BIM10	10ns
Non-Inverting TTL-Level	BIN06	6ns
	BIN10	10ns
	BIN15	15ns
	BIN20	20ns
	BIN25	25ns
Non-Inverting TTL-Level with Hysteresis (for Slow-Ramping Inputs)	BIH10	10ns
	BIH20	20ns
	BIH40	40ns
	BIH80	80ns
ESD Protection Network Only	BIP02	2ns

* Input buffer delay under the following conditions; slow processing, T=100° C, VDD=4.5V and a load capacitance of 5pF.

Input Buffers With Pull-Ups

Each input buffer can have a P-transistor pull-up attached to the input pad. Four possible minimum value equivalent resistances are available: 20K, 50K, 100K and 200K ohms. Table 2 lists current drawn from an external source by the pull-up under various conditions. The six entries for each pull-up value correspond respectively to: maximum current with AT&T guardband, maximum current under normal operation, maximum current during test, minimum current during test, minimum current under normal operation, and minimum current with AT&T guardband.

Table 2 - Pull-up Resistor Current Limits

Pull-up Value	Conditions				
	VDD	Process	Temp.	V_{INPUT}	I_{PULL}
20K	5.72 V	High Current	-40° C	0 V	280 µA
	5.50 V	High Current	-40° C		259 µA
	5.00 V	High Current	25° C		154 µA
	5.00 V	Low Current	85° C		82.6 µA
	4.50 V	Low Current	125° C		57.4 µA
	4.28 V	Low Current	125° C		50.8 µA
50K	5.72 V	High Current	-40° C	0 V	114 µA
	5.50 V	High Current	-40° C		105 µA
	5.00 V	High Current	25° C		61.3 µA
	5.00 V	Low Current	85° C		34.2 µA
	4.50 V	Low Current	125° C		23.6 µA
	4.28 V	Low Current	125° C		20.8 µA
100K	5.72 V	High Current	-40° C	0 V	57.0 µA
	5.50 V	High Current	-40° C		52.4 µA
	5.00 V	High Current	25° C		30.5 µA
	5.00 V	Low Current	85° C		17.2 µA
	4.50 V	Low Current	125° C		11.8 µA
	4.28 V	Low Current	125° C		10.4 µA
200K	5.72 V	High Current	-40° C	0 V	28.5 µA
	5.50 V	High Current	-40° C		26.2 µA
	5.00 V	High Current	25° C		15.2 µA
	5.00 V	Low Current	85° C		8.63 µA
	4.50 V	Low Current	125° C		5.93 µA
	4.28 V	Low Current	125° C		5.23 µA

Output Buffers

Each output buffer cell contains a bonding pad, power bus, ESD protection and the appropriate circuitry. The selection of output buffers available in the 1.25µ CMOS Library is illustrated in Table 3 below:

Table 3 - 1.25µ CMOS Output Buffers

OUTPUT BUFFER TYPE	NAME	PROPAGATION DELAY *
Non-Inverting	BON08	8ns
	BON10	10ns
	BON15	15ns
	BON20	20ns
	BON30	30ns
	BON40	40ns
	BON80	80ns
Non-Inverting Open-Collector	BOC08	8ns
	BOC10	10ns
	BOC15	15ns
	BOC20	20ns
	BOC30	30ns
	BOC40	40ns
	BOC80	80ns
Non-Inverting Tri-State	BOT08	8ns
	BOT10	10ns
	BOT15	15ns
	BOT20	20ns
	BOT30	30ns
	BOT40	40ns
	BOT80	80ns
Output Driver Only No Inherent Logic	BOX08	> 8ns
	BOX10	> 10ns
	BOX15	> 15ns
	BOX20	> 20ns
	BOX30	> 30ns
	BOX40	> 40ns
	BOX80	> 80ns

* Output buffer delay under the following conditions; slow processing, T=100° C, VDD=4.5V and a load capacitance of 50pF.

Bi-Directional Buffers

A bi-directional buffer (I/O Port) consists of the combination of an input buffer and an output buffer. There are five families of bi-directional I/O buffers, distinguished from each other by having different pairings of input buffers with output buffers, described in Table 4. The five bi-directional I/O families are summarized in Tables 5 and 6. The italicized terms *id* and *od* represent the propagation delays of the input and output stages, respectively.

Table 4 - 1.25µ CMOS Bi-Directional I/O Buffers

I/O Family	Input Buffer	Output Buffer	Reference
BN*id*T*od*	Non-Inverting ("BIN"-type)	Non-Inverting, Tri-State ("BOT"-type)	See Table 5.
BN*id*X*od*	Non-Inverting ("BIN"-type)	Output Driver Only ("BOX"-type)	See Table 5.
BH*id*C*od*	Non-Inverting ("BIH"-type)	Non-Inverting, Open Collector ("BOC"-type)	See Table 6.
BH*id*T*od*	Non-Inverting ("BIH"-type)	Non-Inverting, Tri-State ("BOT"-type)	See Table 6.
BH*id*X*od*	Non-Inverting ("BIH"-type)	Output Driver Only ("BOX"-type)	See Table 6.

Table 5 - BN*id*T*od* and BN*id*X*od* Bi-Directional Buffer Families

Input Buffer Delay (*id*)††	Output Buffer Delay (*od*)† 8ns	10ns	15ns	20ns	30ns	40ns	80ns
6ns	BN06*08						
10ns		BN10*10					
15ns	BN15*08		BN15*15				
20ns		BN20*10		BN20*20	BN20*30		
25ns			BN25*15	BN25*20		BN25*40	BN25*80

† Output buffer delay under the following conditions; slow processing, T=100° C, VDD=4.5V and a load capacitance of 50pF.

†† Input buffer delay under the following conditions; slow processing, T=100° C, VDD=4.5V and a load capacitance of 5pF.

Table 6 - BH*id*C*od*, BH*id*T*od* and BH*id*X*od* Bi-Directional Buffer Families

Input Buffer Delay (*id*)††	Output Buffer Delay (*od*)† 8ns	10ns	15ns	20ns	30ns	40ns	80ns
10ns	BH10*08						
20ns		BH20*10	BH20*15	BH20*20	BH20*30		
40ns	BH40*08	BH40*10	BH40*15	BH40*20		BH40*40	
80ns							BH80*80

† Output buffer delay under the following conditions; slow processing, T=100° C, VDD=4.5V and a load capacitance of 50pF.

†† Input buffer delay under the following conditions; slow processing, T=100° C, VDD=4.5V and a load capacitance of 5pF.

5

Bidirectional I/O Buffers with Pull-Ups

As with input buffers, each bidirectional I/O buffer can have a P-transistor pull-up attached to the pad. Refer to Table 2 for the resistor values available and their current limits.

Once you have made a selection of buffer circuits on the basis of logic function, power and speed, you are still faced with a choice of layout format. Each buffer circuit is available in two layout formats: *-D or -T* format layout. A third layout format, *-P*, is available for all input and output buffer circuits used in weakly pad limited chips. A fourth layout format available only with in double level metal technology, *-H,* is available for buffers with high sinking/sourcing current output drivers. The format is indicated by the cell name suffix (e.g. BON08D, BON08H, BON08P or BON08T). Table 7 summarizes the characteristics of each layout style.

Table 7 - 1.25µ CMOS Buffer Layout Information

LAYOUT FORMAT	KEYWORD	CELL HEIGHT	CELL WIDTH (Cell Dependant)
D	Default	291.750µ 11.49 mils	200.875µ → 354.500µ
H	High Current (Strongly Pad Limited)	540.125µ 21.26 mils	175.000µ → 234.500µ
P	Weakly Pad-Limited	291.750µ 11.49 mils	193.000µ → 293.000µ
T	Tall (Strongly Pad Limited)	540.125µ 21.26 mils	175.000µ → 216.500µ

Before Layout. Will your chip be pad limited? If the answer is a definite "No", then pre-layout simulations may use the -D style buffers. If the answer is "Yes" or "Maybe", then it is suggested that the buffers with the most pessimistic parasitics be used in simulation. If the code is to be designed in the single level metal process, then the -T style should be used in preliminary simulations. If the code is to be designed in double level metal, then use of -H style buffers is indicated.

During Layout. Once chip layout begins, the choice of the right style buffer (-D, -H, -P or -T) becomes very important. The following guidelines will help you choose the correct buffer layout style, so that you may obtain the smallest possible chip with the best protection against latch-up.

Chips that are Not Pad-Limited - This includes chips with a small number of pins, or a very large gate count. The -D layout style is suggested, as it is in the short layout format and the pad is fully guard-banded against latch-up. It affords the most latch-up protection with the smallest chip size as illustrated in Figure 1:

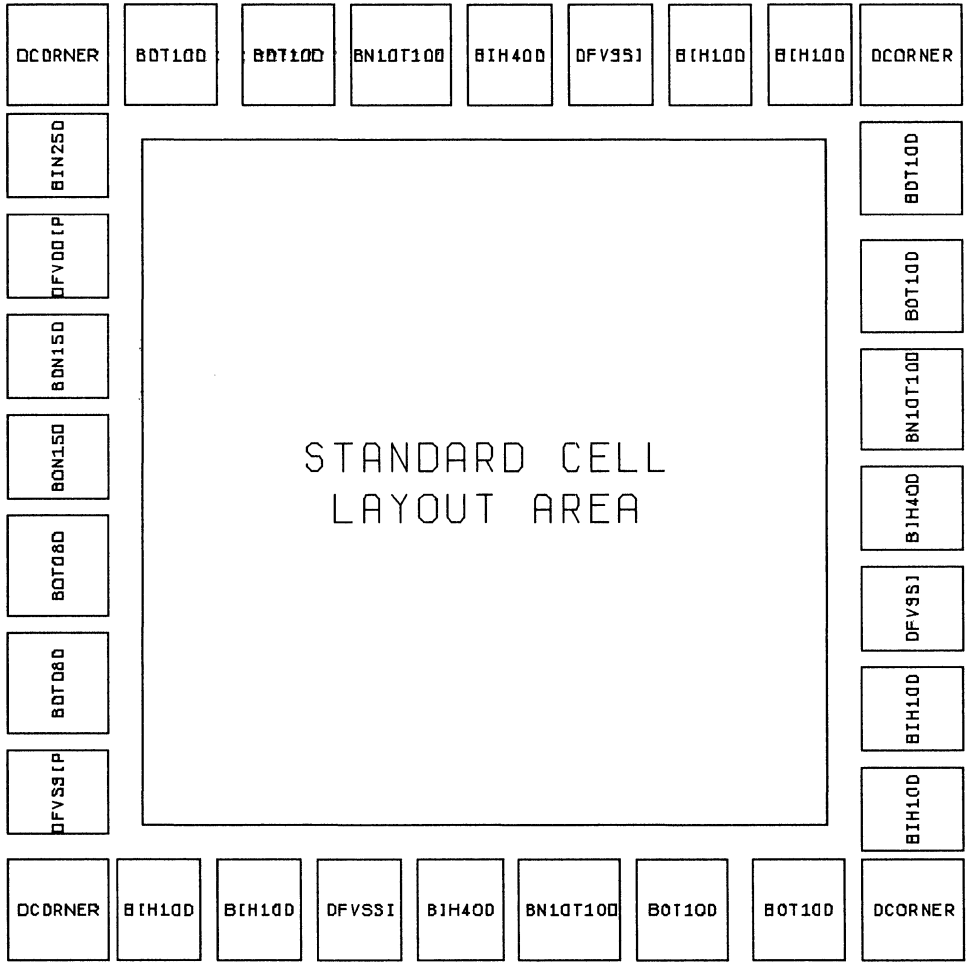


Figure 1 - Buffer Ring for a Chip that is Not Pad-Limited

The only layout precaution required is when a buffer's edge closest to the pad faces another buffer's pad edge; they must separated enough to satisfy wire bond rules, namely pad center to pad center separation greater than or equal to 7 mils (175μ).

Chips that are Weakly Pad-Limited - This includes chips that would otherwise be pad-limited using only the -D style buffers. -P layout buffers may be used on any pin, as long as the cell boundary on the pad side is butted up to it's nearest neighbor buffer. Note that at **NO** time can the pad boundary of a -P buffer be placed next to the pad boundary of its neighbor; this not only can cause wire bonding violations, but also can potentially degrade a chip's latch-up protection.

A -D style buffer **MUST** be placed at the end of a buffer row where the pad would have no neighboring buffer. Also -D styles should be used wherever a -P buffer's pad cannot be abutted next to another buffer; in short, if there is room for a -D, use a -D. Figure 2 illustrates.

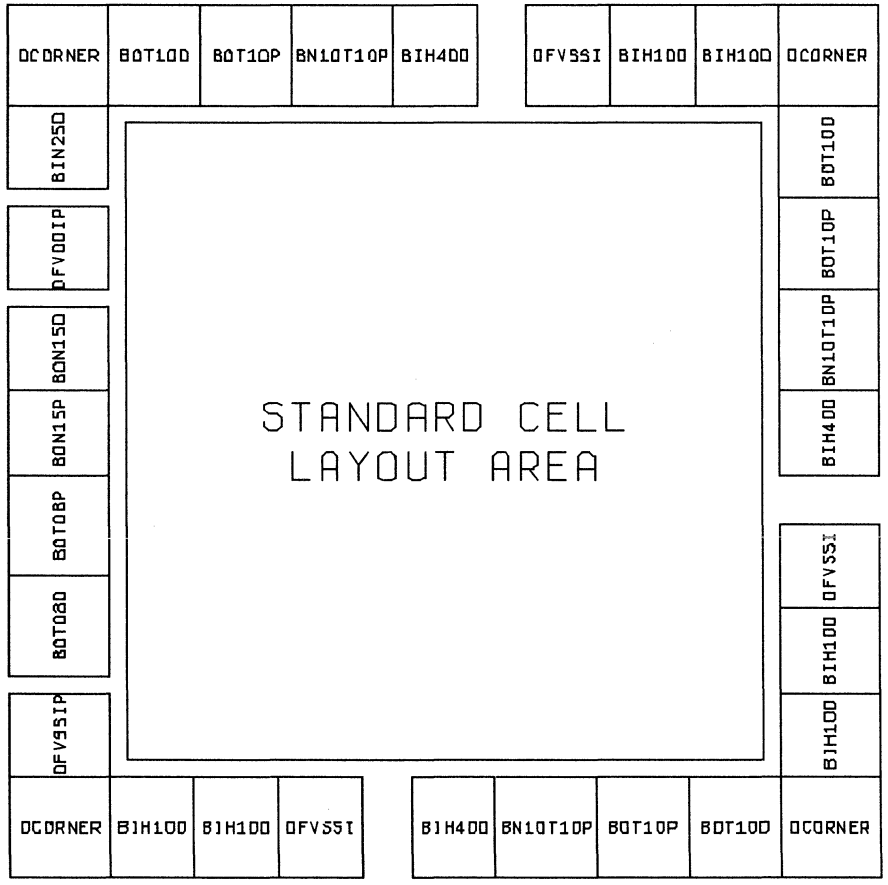


Figure 2 - Buffer Ring for a Chip that is Weakly Pad-Limited

Chips that are Pad-Limited - This includes chips with a large number of pins and/or a small gate count. If the chip layout uses buffers with -D and -P style layouts, these cells may **NOT** be used in the same buffer row as a -H or -T style buffer. The -D and -P cells must also be used in the manner previously described for weakly pad-limited chips. Buffers in -H layout style may be used in buffer rows with -T layout cells only if the chip is made in the double level metal technology (see Figure 3).

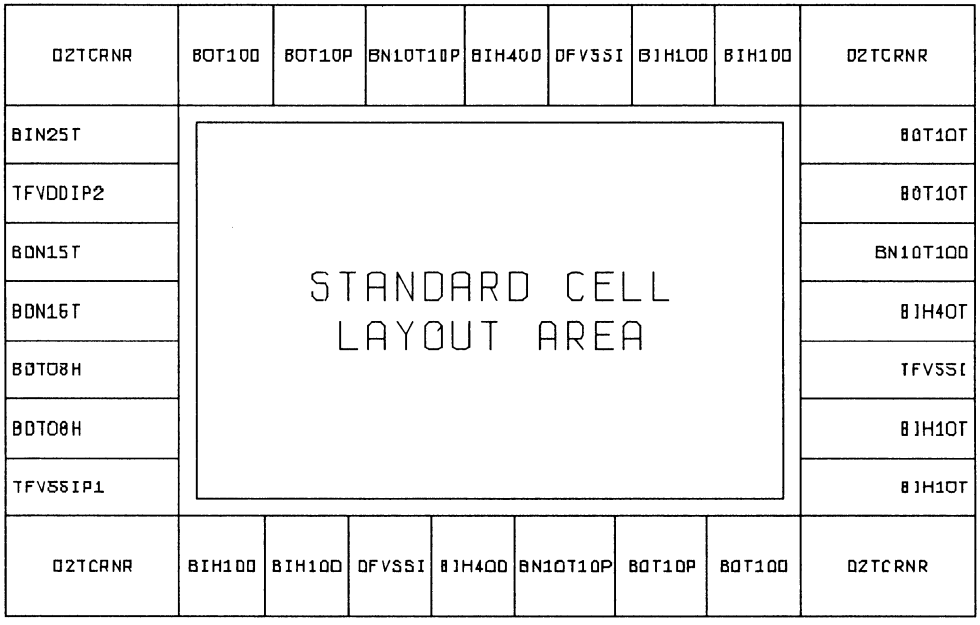


Figure 3 - Buffer Ring Using a Combination of -D, -H, -P and -T Style Buffers

Chips that are Strongly Pad-Limited - If the chip uses -H or -T style buffers exclusively (see Figure 4), no special precautions have to be taken to guard against latch-up. Buffers in -H layout style may be used in buffer rows with -T layout cells only if the chip is made in the double level metal technology.

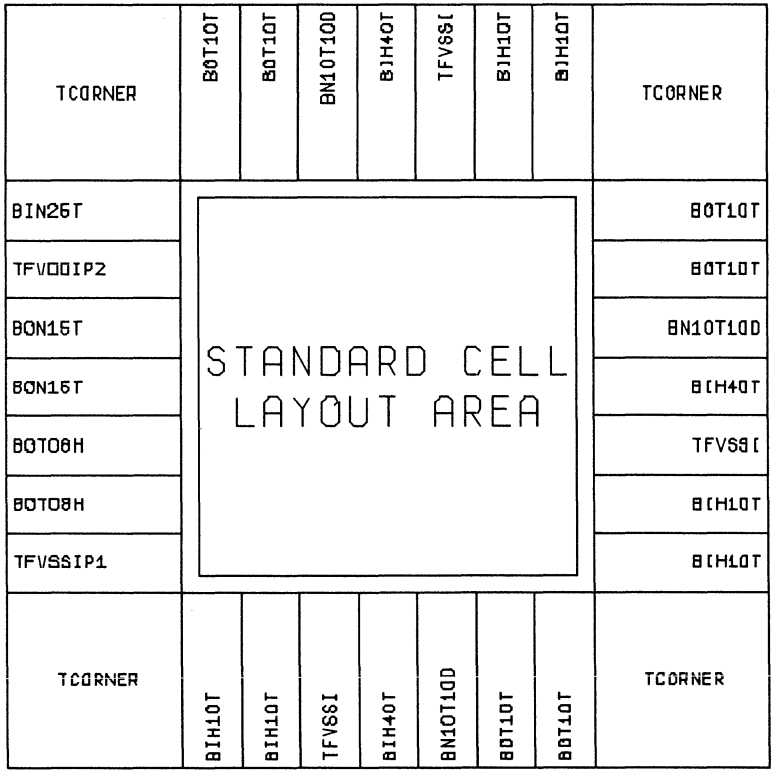


Figure 4 - Buffer Ring for a Chip that is Strongly Pad-Limited

Each buffer circuit includes a circuit network connected to the bonding pad. This network performs two functions: it protects the buffer logic from Electro-Static Discharge (ESD) originating at the chip pins, and prevents latch-up spur currents from entering the internal chip logic. The protection network layout is tailored to each of the *-D, -H, -P* and *-T* buffer formats.

Electro-Static Discharge

Buffers have been characterized for two types of ESD events: the Human-Body Model (HBM), and the Charged Device Model (CDM). The Human Body Model simulates the effect of a charged person contacting the device. The Charged Device Model simulates the electrical discharge caused by the tribo-electrical charging of a packaged device.

Devices are characterized for HBM and CDM using the methodology prescribed by the AT&T spec X-19435, Issue 2. Devices are also characterized for HBM according to the methodology prescribed by MIL-STD 883C Method 3015.6.

The ESD sensitivities of the I/O buffers are summarized in Table 8.

Table 8 - 1.25µ CMOS Buffer ESD Reliability

Test	Failure Voltage	ESD Class
HBM (AT&T)	>1200 V	II
HBM (MIL-STD)	>1200 V	-
CDM (AT&T)	>500 V	II

Latch-Up

Latch-up occurs when parasitic vertical and lateral bi-polar transistors, which form a P-N-P-N structure from VDD to VSS, turn on. One way latch-up can be triggered is by applying external voltages greater than VDD or less than VSS to I/O buffer pads. The current supplied by the external source forward biases one of the ESD protection diodes connected to the pad, and triggers the P-N-P-N SCR. The high current SCR will remain turned on until the device self-destructs, or power is removed.

Table 9 gives DC I-V conditions above which latch-up may occur.

Table 9 - 1.25µ CMOS Latch-Up Immunity*

IO Pad Current	IO Pad Voltage
1.0 A	VSS - 2.3V
1.0 A	VDD + 5.0V

* Note - The latch-up immunity offered by the -P layout style is as good as the -D, -H and -T layout if and only if the -P style buffers are used according to the placement rules described in 'Selecting the Layout Format'.

Ground Bounce

Chips with high speed output buffers driving large capacitive loads generate voltage spikes on the power busses. These voltage spikes are produced when high speed output buffers generate rapidly changing currents through the parasitic inductance in the package and bonding wire. Although inductive noise occurs on both the VDD and VSS busses, ground bounce is more noticeable a problem since most buffers are TTL compatible and therefore have a VSS noise margin much less than their VDD noise margin.

There are several steps the designer can take to reduce the overall chip ground bounce.

Before Layout:

1) Dedicate as many pins as possible to VSS and VDD; with emphasis on VSS.
2) If possible, make separate power pins available to isolate fast buffers from other sensitive circuits.
3) Place the VSS pins where the internal package lead and the wire bond will be shortest.
4) Do not place consecutive VSS pins in groups. Lower overall noise is achieved by interdigitating VSS with either VDD or signal pins.

During Layout:

1) Select output buffers with care. Use the slowest possible output buffer necessary to satisfy through-put delays and sink/source current requirements.
2) If possible, speed up paths with high power standard cells, while using the next slowest output buffer.
3) If an output pin requires high sink/source current, but does not require high speed, then use the "X" driver cells (e.g. BOX08D). The overall circuit speed and noise can then be controlled with a standard cell subcircuit network.

This section describes the various parameters given in the **Circuit Information** and **Layout Information** tables in the **Cell Pages** following. Unless otherwise stated, the parameters were measured in the *ADVICE* simulator, and assumed the double level metal technology.

There is a small set of process and environmental conditions that simulate the worst case performance of all the tests and measurements listed in the circuit page information tables. These conditions are noted as:

WCF - Worst Case Fast

This set of process and environment parameters causes CMOS devices to exhibit the lowest parasitic capacitance and impedance, and the greatest speed and current driving capability. It is characterized in the simulator with the following conditions:

1) Fast Process
2) VDD = 5.5V
3) T = 0° C

NOM - Nominal

This set of process and environment parameters causes CMOS devices to exhibit the typical capacitance and impedance, and the nominal speed and current driving capability. It is characterized in the simulator with the following conditions;

1) Nominal Process
2) VDD = 5.0V
3) T = 25° C

WCS - Worst Case Slow

This set of process and environment parameters causes CMOS devices to exhibit the highest parasitic capacitance and impedance, and the slowest speed and current driving capability. It is characterized in the simulator with the following conditions;

1) Slow Process
2) VDD = 4.5V
3) T = 100° C

General

Capacitance - (WCS) The capacitance associated with the circuit input(s) and output(s) is extracted from data calculated by a layout analysis computer program, *GOALIE2.*

In the case of bonding pad capacitances, it should be noted that this capacitance estimate **DOES NOT** include any wire bond and package capacitance.

Leakage Current - (Fast Process, VDD=5.5V, T=125° C) After manufacture, input pins are tested to pass 0.9µA current leakage and output pins are tested to pass 9µA current leakage with the beginning-of-life (BOL) test. With end-of-life (EOL) test, inputs are tested to pass 1µA current leakage, and outputs are tested to pass 10µA.

Input Buffers

(Including input buffers used in the bidirectional buffers.)

DC Power - (WCF) For TTL compatible Input Buffers, the input gate bias is first held at V_{IL} = 0.8V (a TTL '0'), and at V_{IH} = 2.0V (a TTL '1'). For MOS level Input Buffers, the input gate bias is held at 1.0V and VDD-1.0V.

Under both tests, the current from VDD to VSS is measured. The largest of these two values is multiplied by VDD and recorded as the maximum DC power.

Propagation Delay - (NOM) The propagation delay for input buffers is defined as the time separating two events:

1) The buffer input switching to a valid input logic level.
2) And the buffer output crossing VDD/2.

This measurement is made for both rising and falling input edges over a range of output load capacitances from 1pF to 5pF. The input voltage has rise and fall times of 2ns.

The measurement conditions of propagation delay for TTL-compatible input buffers are illustrated in Figure 5, below. The valid input logic levels are defined to be V_{IL} = 0.8V and V_{IH} = 2.0V.

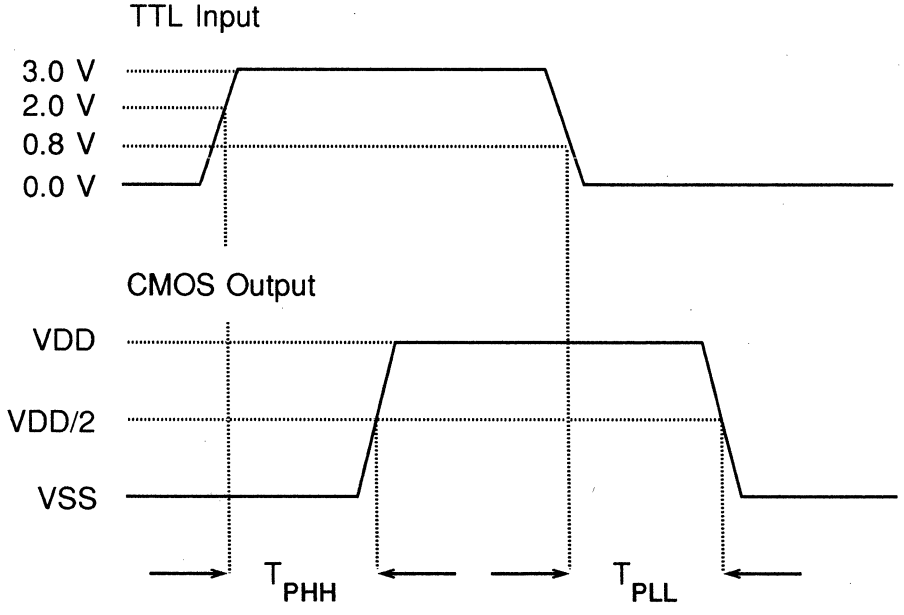


Figure 5 - Measurement Conditions - TTL Level Input Buffer Propagation Delay

For MOS-level input buffers, the delay function is determined by simulations using an input waveform with a rail-to-rail pulse with rise and fall times of 2ns. This is illustrated in Figure 6, below:

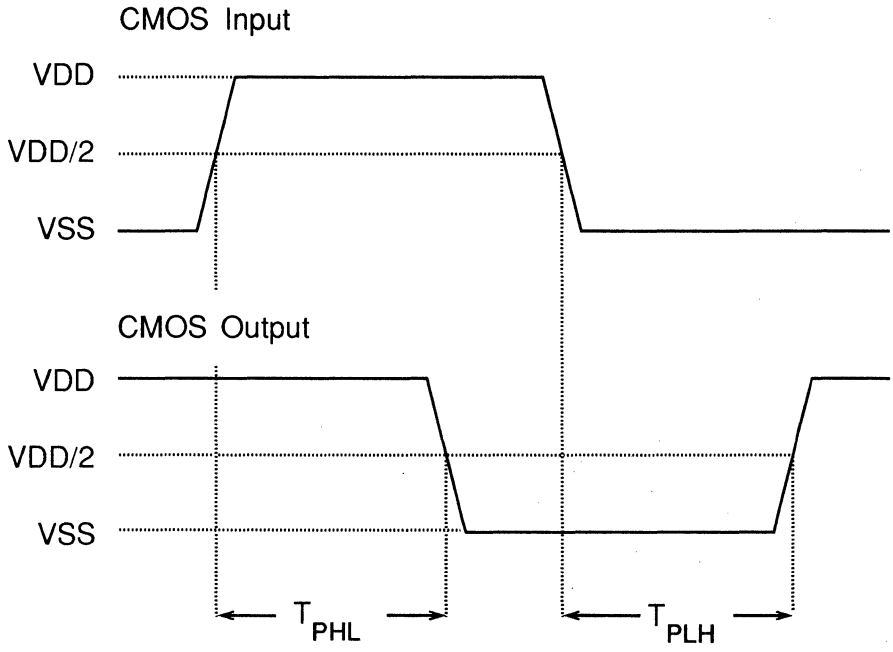


Figure 6 - Measurement Conditions - CMOS Level Input Buffer Propagation Delay

Input Slew - (WCF) The Input Slew Rate of an input buffer is defined as the slowest voltage ramp applied to the input that will not cause the input buffer to oscillate. An input ramp slower than this value may cause the output to bounce rapidly between logic '0' and '1' during switching.

An AC stability analysis is performed over several input biases, thus determining the range of input voltages over which the input buffer is unstable. A set of transient analyses are then performed in which the input ramps through the region of instability. The slowest ramp rate that stimulates a buffer output that can read unambiguously by standard cells is recorded as the Input Slew Rate.

In BIH input buffers and BH bidirectional buffers, the circuit is AC stable, but may still lose data due to sub-threshold leakage effects. For these cells, the minimum input slew rate is calculated using process sub-threshold leakage current limits and the circuit hysteresis (See also Hysteresis below).

Hysteresis - (Slow Process,VDD=4.5, T=0° C) The hysteresis of BIH buffers is not a true hysteresis, although it models one due to the output stage entering a tri-state mode. The range of hysteresis for BIH buffers is therefore defined by the region of input voltage over which the output is in tri-state. See Figure 7 below.

A DC analysis is performed though the switching region, and current drawn by the output stage from an external resistor network is monitored. The region over which no current is drawn or supplied by the output stage is recorded as the minimum hysteresis.

V- - (Fast N Process, Slow P Process, VDD=4.5V, T=100° C) V- denotes the low-going threshold voltage of a circuit with hysteresis. Under these process and environmental variables, V- achieves its lowest value in BIH- type input and bi-directional buffers. See Figure 7 below.

A DC analysis is performed though the switching region, and current drawn by the output stage from an external resistor network is monitored. The lowest voltage at which no current is drawn by the output stage is recorded as V- (see also **Hysteresis**).

V+ - (Slow N Process, Fast P Process, VDD=5.5V, T=0° C) V+ denotes the high-going threshold voltage of a circuit with hysteresis. Under these process and environmental variables, V+ achieves its greatest value in BIH- type input and bi-directional buffers. See Figure 7 below.

A DC analysis is performed though the switching region, and current supplied by the output stage from an external resistor network is monitored. The highest voltage at which no current is supplied by the output stage is recorded as V+ (see also **Hysteresis**).

5

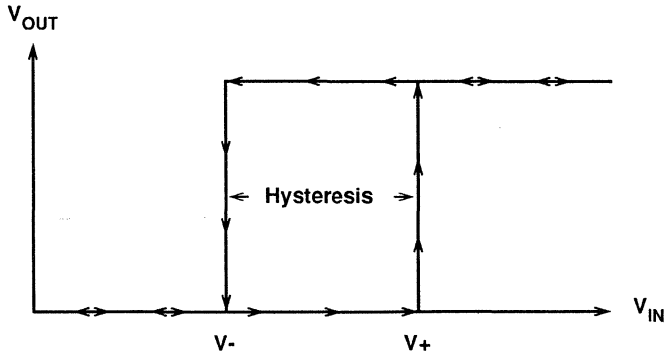


Figure 7 - Measurement Conditions - BIH- type I/O Buffer V-, Hysteresis and V+

V_{LO} - (Fast N Process, Slow P Process, VDD=4.5V, T=100° C) V_{LO} denotes the lowest DC switching voltage (V_{I0}) exhibited by a circuit. A DC analysis is made under these conditions, and the input voltage at which the circuit output crosses VDD/2 is recorded as V_{LO}.

V_{HI} - (Slow N Process, Fast P Process, VDD=5.5V, T=0° C) V_{HI} denotes the highest DC switching voltage (V_{I1}) exhibited by a circuit. A DC analysis is made under these conditions, and the input voltage at which the circuit output crosses VDD/2 is recorded as V_{HI}.

Output Buffers

(Includes output buffers used in bidirectional buffers)

DC Sink/Source Current - (WCS) An output logic '0' is enabled, and a voltage source equal to the a TTL '0' (0.4V) is applied to the output. The current drawn by the output buffer from the external voltage source is recorded as the DC Sink Current. Similarly, an output logic '1' is enabled, and a voltage source equal to TTL '1' (2.4V) is applied to the output, the current supplied by the output buffer to the external voltage source is the DC Source Current. Worst case package and wirebond parasitic resistance values of 0.10Ω and 0.05Ω respectively are included in this evaluation. An estimate of power bus resistance of 0.35Ω (corresponding to 10 sq. of metal) is also included.

Propagation Delay - (NOM) The propagation delay for output buffers is defined as the time separating two events:

1) The buffer input switching to a valid logic level, by crossing VDD/2,
2) And the buffer output achieving a valid TTL level. Logic '1' V_{OH}= 2.4V, and Logic '0' V_{OL}= 0.4V.

The buffer input is loaded with an average routing capacitance and routing resistance, and is driven by an INRB standard cell. The rising and falling edge propagation delays are measured over a range of output load capacitances from 0 pF to 200 pF. The waveforms and levels involved are illustrated in Figure 8, below:

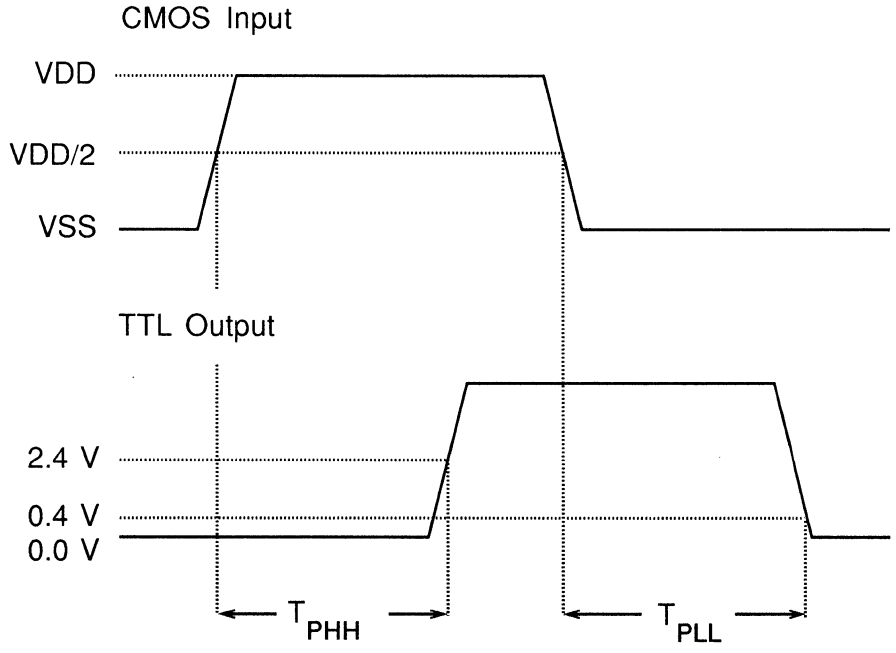


Figure 8 - Measurement Conditions - TTL Level Output Buffer Propagation Delay

Tri-State Delay - (NOM) For tri-state output buffers the Tri-State Delay is defined as the time required for the circuit to go into the tri-state mode, and is defined as the time separating two events:

1) The tri-state control inputs (ST and STN) both switching to the complimentary logic levels that select the tri-state function, by crossing VDD/2.
2) And both transistors of the output driver going into their respective cutoff regions.

The tri-state control inputs are loaded with average routing capacitances and resistances and are driven by INRB standard cells. The driver achieves tri-state when both P and N driver transistors are in cutoff. That is, when:

1) The N-channel driver gate (node I1) voltage is less than V_{TN}, the N-transistor threshold voltage;
2) And the P-channel driver gate (node I2) voltage is greater than (VDD - V_{TP}), a P-transistor threshold voltage below VDD.

The delay coming out of tri-state (if the new logic state does not equal the old logic state) is equal to the propagation delay of the circuit.

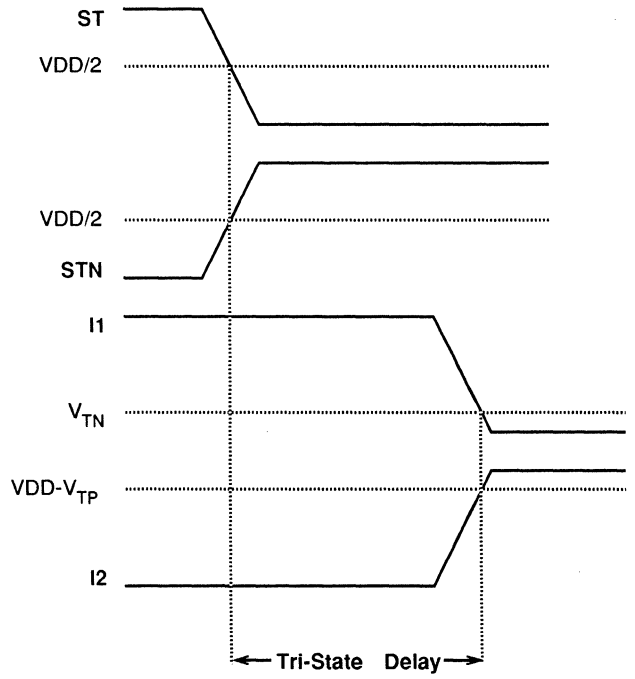


Figure 9 - Measurement Conditions - Output Buffer Tristate Delay

Ancillary features are XY-mask geometries that perform no real logic function on the chip, but are nonetheless necessary to aid in layout completion, chip identification and chip manufacture. The clumps in Table 10 may be used to route power connections from bonding pads to the buffer and standard cell areas. Unless noted, all power pads have ESD protection included in the layout.

Table 10 - Power Routing Ancillary Clumps

Clump Name	Function
D2TCRNR	Chip corner power bus clump, connects D,P to H,T type I/O Buffers
DCORNER	Chip corner power bus clump
DCVDDI	Chip corner power pad, supplies VDD to I/O Buffers only
DCVSSI	Chip corner power pad, supplies VSS to I/O Buffers only
DFVDDI	Chip edge power pad, supplies VDD to I/O Buffers only
DFVDDIP	Chip edge power pad, supplies VDD to I/O Buffers and standard cells
DFVDDM2F	Chip edge power jump module, supplies VDD on Metal-2 to standard cells
DFVDDP0	Chip edge power pad, supplies VDD to standard cells only with no VSS tabs
DFVDDP1	Chip edge power pad, supplies VDD to standard cells only with VSS tab on right side
DFVDDP2	Chip edge power pad, supplies VDD to standard cells only with VSS tabs on both sides
DFVSSI	Chip edge power pad, supplies VSS to I/O Buffers only
DFVSSIP1	Chip edge power pad, supplies VSS to I/O Buffers and standard cells with VDD tab on right side
DFVSSIP2	Chip edge power pad, supplies VSS to I/O Buffers and standard cells with VDD tabs on both sides
DFVSSM2F	Chip edge power jump module, supplies VSS on Metal-2 to standard cells, passes VDD on Metal-1 in I/O Buffer ring
DFVSSP1	Chip edge power pad, supplies VSS to standard cells only with VDD tab on right side
DFVSSP2	Chip edge power pad, supplies VSS to standard cells only with VDD tabs on both sides
TCORNER	Chip corner power bus clump
TCVDDI1	Chip corner power pad, supplies VDD to I/O Buffers only with VSS tabs on right side
TCVDDI2	Chip corner power pad, supplies VDD to I/O Buffers only with VSS tabs on both sides
TCVSSI	Chip corner power pad, supplies VSS to I/O Buffers only

Table 10 (Cont'd.) - Power Routing Ancillary Clumps

Clump Name	Function
TFVDDI1	Chip edge power pad, supplies VDD to I/O Buffers only with VSS tabs on right side
TFVDDI2	Chip edge power pad, supplies VDD to I/O Buffers only with VSS tabs on both sides
TFVDDIP1	Chip edge power pad, supplies VDD to I/O Buffers and standard cells with VSS tabs on right side
TFVDDIP2	Chip edge power pad, supplies VDD to I/O Buffers and standard cells with VSS tabs on both sides
TFVDDM2F	Chip edge jump module, supplies VDD on Metal-2 to standard cells
TFVDDP1	Chip edge power pad, supplies VDD to standard cells only with VSS tabs on right side
TFVDDP2	Chip edge power pad, supplies VDD to standard cells only with VSS tabs on both sides
TFVSSI	Chip edge power pad, supplies VSS to I/O Buffers only
TFVSSIP0	Chip edge power pad, supplies VSS to I/O Buffers and standard cells with no VDD tabs
TFVSSIP1	Chip edge power pad, supplies VSS to I/O Buffers and standard cells with VDD tabs on right side
TFVSSIP2	Chip edge power pad, supplies VSS to I/O Buffers and standard cells with VDD tabs on both sides
TFVSSM2F	Chip edge jump module, supplies VSS on Metal-2 to standard cells, passes VDD on Metal-1 in I/O Buffer ring
TFVSSP0	Chip edge power pad, supplies VSS to standard cells only with no VDD tabs
TFVSSP1	Chip edge power pad, supplies VSS to standard cells only with VDD tabs on right side
TFVSSP2	Chip edge power pad, supplies VSS to standard cells only with VDD tabs on both sides

Bi-Directional Buffer

BH*id*C*od*[D,H,T]

BIH- Input Stage, BOC- Output Stage

FUNCTIONAL DESCRIPTION:

Non-Inverting TTL-Level Input Stage with Hysteresis,
Non-Inverting TTL-Level Open Collector Output Stage

CELL NAME DEFINITIONS:

id = WCS Input Stage Delay in ns @ 5pF load
od = WCS Output Stage Delay in ns @ 50pF load
[D,H,T] = Available Layout Formats

EXAMPLE: BH10C08D

INPUTS: A, PADI
OUTPUTS: Z, PADO

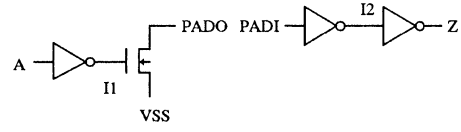
MOTIS Gate Count: 5

5

Truth Table

Inputs		Outputs	
A	PADI	Z	PADO
0	0	0	0
1	0	0	HI-Z
1	1	1	HI-Z

MOTIS Model



Circuit Capacitances

Cell Name	Node			
	A	PAD[D]*	PAD[H]*	PAD[T]*
BH10C08	0.272 pF	4.386 pF	5.072 pF	5.108 pF
BH20C10	0.188 pF	3.853 pF	4.536 pF	4.589 pF
BH20C15	0.100 pF	3.317 pF	4.000 pF	4.068 pF
BH20C20	0.074 pF	3.367 pF	4.053 pF	4.135 pF
BH20C30	0.064 pF	2.765 pF	3.459 pF	3.564 pF
BH40C08	0.272 pF	4.240 pF	4.918 pF	4.952 pF
BH40C10	0.188 pF	3.872 pF	4.550 pF	4.601 pF
BH40C15	0.100 pF	3.334 pF	4.013 pF	4.078 pF
BH40C20	0.074 pF	3.386 pF	4.066 pF	4.144 pF
BH40C40	0.062 pF	2.860 pF	NC	3.659 pF
BH80C80	0.062 pF	2.842 pF	NC	3.606 pF

* Pad capacitance varies with layout format.
NC - Cell not available in this layout format.

Input Stage Circuit Performance

Cell Name	DC Power [1]	Delay [2]				Input Slew [1]
		T_{PHH}		T_{PLL}		
		Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BH10C08	5.87 mW	0.740 ns/pF	0.688 ns	0.623 ns/pF	1.323 ns	>2.4 V/ms
BH20C10	1.93 mW	1.612 ns/pF	1.016 ns	1.384 ns/pF	2.263 ns	>1.4 V/ms
BH20C15	1.93 mW	1.612 ns/pF	1.016 ns	1.384 ns/pF	2.263 ns	>1.4 V/ms
BH20C20	1.93 mW	1.612 ns/pF	1.016 ns	1.384 ns/pF	2.263 ns	>1.4 V/ms
BH20C30	1.93 mW	1.612 ns/pF	1.016 ns	1.384 ns/pF	2.263 ns	>1.4 V/ms
BH40C08	0.83 mW	2.248 ns/pF	1.541 ns	2.785 ns/pF	4.615 ns	>140 V/s
BH40C10	0.83 mW	2.248 ns/pF	1.541 ns	2.785 ns/pF	4.615 ns	>140 V/s
BH40C15	0.83 mW	2.248 ns/pF	1.541 ns	2.785 ns/pF	4.615 ns	>140 V/s
BH40C20	0.83 mW	2.248 ns/pF	1.541 ns	2.785 ns/pF	4.615 ns	>140 V/s
BH40C40	0.83 mW	2.248 ns/pF	1.541 ns	2.785 ns/pF	4.615 ns	>140 V/s
BH80C80	0.32 mW	5.928 ns/pF	3.399 ns	5.327 ns/pF	8.519 ns	>72 V/s

1) Fast Process, VDD=5.5V, T=0° C
2) Nominal Process, VDD=5.0V, T=25° C

Cell Name	V- [3]	Hysteresis [4]	V+ [5]
BH10C08	1.022 V	323 mV	1.789 V
BH20C10	1.012 V	334 mV	1.773 V
BH20C15	1.012 V	334 mV	1.773 V
BH20C20	1.012 V	334 mV	1.773 V
BH20C30	1.012 V	334 mV	1.773 V
BH40C08	0.992 V	331 mV	1.727 V
BH40C10	0.992 V	331 mV	1.727 V
BH40C15	0.992 V	331 mV	1.727 V
BH40C20	0.992 V	331 mV	1.727 V
BH40C40	0.992 V	331 mV	1.727 V
BH80C80	0.985 V	286 mV	1.684 V

3) Fast N Process, Slow P Process, VDD=4.5V, T=100° C
4) Slow Process, VDD=4.5V, T=0° C
5) Slow N Process, Fast P Process, VDD=5.5V, T=0° C

Output Stage Circuit Performance

Cell Name	Delay [1] T_{PLL}		DC Current [2]
	Extrinsic	Intrinsic	Sink
BH10C08D	0.252 ns/10pF	1.226 ns	24.2 mA
BH10C08H	0.252 ns/10pF	1.338 ns	24.2 mA
BH10C08T	0.368 ns/10pF	1.307 ns	13.4 mA
BH20C10D	0.434 ns/10pF	1.209 ns	12.1 mA
BH20C10H	0.437 ns/10pF	1.272 ns	12.1 mA
BH20C10T	0.461 ns/10pF	1.266 ns	11.2 mA
BH20C15D	0.548 ns/10pF	1.774 ns	10.1 mA
BH20C15H	0.552 ns/10pF	1.838 ns	10.1 mA
BH20C15T	0.573 ns/10pF	1.814 ns	9.5 mA
BH20C20D	0.719 ns/10pF	2.229 ns	8.1 mA
BH20C20H	0.724 ns/10pF	2.295 ns	8.1 mA
BH20C20T	0.741 ns/10pF	2.276 ns	7.7 mA
BH20C30D	1.608 ns/10pF	1.839 ns	4.1 mA
BH20C30H	1.609 ns/10pF	2.094 ns	4.1 mA
BH20C30T	1.618 ns/10pF	1.974 ns	4.0 mA
BH40C08D	0.252 ns/10pF	1.303 ns	24.2 mA
BH40C08H	0.252 ns/10pF	1.338 ns	24.2 mA
BH40C08T	0.368 ns/10pF	1.301 ns	13.4 mA
BH40C10D	0.434 ns/10pF	1.232 ns	12.1 mA
BH40C10H	0.437 ns/10pF	1.272 ns	12.1 mA
BH40C10T	0.461 ns/10pF	1.266 ns	11.2 mA
BH40C15D	0.548 ns/10pF	1.774 ns	10.1 mA
BH40C15H	0.552 ns/10pF	1.839 ns	10.1 mA
BH40C15T	0.573 ns/10pF	1.814 ns	9.5 mA
BH40C20D	0.719 ns/10pF	2.231 ns	8.1 mA
BH40C20H	0.724 ns/10pF	2.293 ns	8.1 mA
BH40C20T	0.741 ns/10pF	2.276 ns	7.7 mA
BH40C40D	3.082 ns/10pF	1.969 ns	2.2 mA
BH40C40T	3.105 ns/10pF	2.233 ns	2.1 mA
BH80C80D	6.974 ns/10pF	2.832 ns	1.0 mA
BH80C80T	6.996 ns/10pF	3.416 ns	1.0 mA

1) Nominal Process, VDD=5.0V, T=25° C
2) Slow Process, VDD=4.5V, T=100° C

Layout Information

Cell Name	Transistors	Cell Dimensions	
		X	Y
BH10C08D BH10C08H BH10C08T	24	331.250 µm 211.250 µm 193.250 µm	291.750 µm 540.125 µm 540.125 µm
BH20C10D BH20C10H BH20C10T	18	304.750 µm 184.750 µm 175.000 µm	291.750 µm 540.125 µm 540.125 µm
BH20C15D BH20C15H BH20C15T	16	295.750 µm 175.750 µm 175.000 µm	291.750 µm 540.125 µm 540.125 µm
BH20C20D BH20C20H BH20C20T	14	286.750 µm 175.000 µm 175.000 µm	291.750 µm 540.125 µm 540.125 µm
BH20C30D BH20C30H BH20C30T	12	277.750 µm 175.000 µm 175.000 µm	291.750 µm 540.125 µm 540.125 µm
BH40C08D BH40C08H BH40C08T	24	333.750 µm 213.750 µm 195.750 µm	291.750 µm 540.125 µm 540.125 µm
BH40C10D BH40C10H BH40C10T	18	306.750 µm 186.750 µm 175.000 µm	291.750 µm 540.125 µm 540.125 µm
BH40C15D BH40C15H BH40C15T	16	297.750 µm 177.750 µm 175.000 µm	291.750 µm 540.125 µm 540.125 µm
BH40C20D BH40C20H BH40C20T	14	288.750 µm 175.000 µm 175.000 µm	291.750 µm 540.125 µm 540.125 µm
BH40C40D BH40C40T	10	270.750 µm 175.000 µm	291.750 µm 540.125 µm
BH80C80D BH80C80T	10	276.750 µm 175.000 µm	291.750 µm 540.125 µm

Bi-Directional Buffer

BH*id*T*od*[D,H,T]

BIH- Input Stage, BOT- Output Stage

FUNCTIONAL DESCRIPTION:

Non-Inverting TTL-Level Input Stage with Hysteresis,
Non-Inverting TTL-Level Tri-State Output Stage

CELL NAME DEFINITIONS:

id = WCS Input Stage Delay in ns @ 5pF load
od = WCS Output Stage Delay in ns @ 50pF load
[D,H,T] = Available Layout Formats

EXAMPLE: BH10T08D

INPUTS: A, ST, STN, PADI
OUTPUTS: Z, PADO

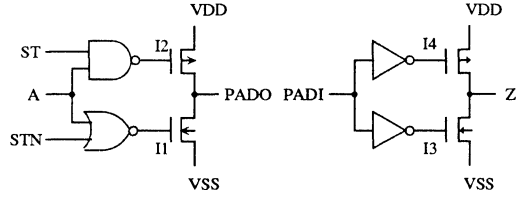
MOTIS Gate Count: 6

5

Truth Table

Inputs				Outputs	
A	ST	STN	PADI	Z	PADO
0	X	0	0	0	0
0	X	1	0	0	HI-Z
0	X	1	1	1	HI-Z
1	0	X	0	0	HI-Z
1	0	X	1	1	HI-Z
1	1	X	1	1	1

MOTIS Model



Circuit Capacitances

Cell Name	Node					
	A	ST	STN	PAD[D]*	PAD[H]*	PAD[T]*
BH10T08	0.742 pF	0.408 pF	0.342 pF	4.391 pF	5.077 pF	5.113 pF
BH20T10	0.400 pF	0.226 pF	0.194 pF	3.858 pF	4.541 pF	4.594 pF
BH20T15	0.183 pF	0.110 pF	0.099 pF	3.316 pF	4.002 pF	4.069 pF
BH20T20	0.120 pF	0.077 pF	0.072 pF	3.371 pF	4.057 pF	4.139 pF
BH20T30	0.098 pF	0.064 pF	0.063 pF	2.766 pF	3.460 pF	3.564 pF
BH40T08	0.742 pF	0.408 pF	0.342 pF	4.245 pF	4.923 pF	4.957 pF
BH40T10	0.400 pF	0.226 pF	0.194 pF	3.877 pF	4.555 pF	4.606 pF
BH40T15	0.183 pF	0.110 pF	0.099 pF	3.335 pF	4.015 pF	4.079 pF
BH40T20	0.120 pF	0.077 pF	0.072 pF	3.390 pF	4.070 pF	4.148 pF
BH40T40	0.112 pF	0.071 pF	0.070 pF	2.859 pF	NC	3.661 pF
BH80T80	0.097 pF	0.064 pF	0.063 pF	2.841 pF	NC	3.608 pF

* Pad capacitance varies with layout format.
NC - Cell not available in this layout format.

Input Stage Circuit Performance

Cell Name	DC Power [1]	Delay [2]				Input Slew [1]
		T_{PHH}		T_{PLL}		
		Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BH10T08	5.87 mW	0.740 ns/pF	0.688 ns	0.623 ns/pF	1.323 ns	>2.4 V/ms
BH20T10	1.93 mW	1.612 ns/pF	1.016 ns	1.384 ns/pF	2.263 ns	>1.4 V/ms
BH20T15	1.93 mW	1.612 ns/pF	1.016 ns	1.384 ns/pF	2.263 ns	>1.4 V/ms
BH20T20	1.93 mW	1.612 ns/pF	1.016 ns	1.384 ns/pF	2.263 ns	>1.4 V/ms
BH20T30	1.93 mW	1.612 ns/pF	1.016 ns	1.384 ns/pF	2.263 ns	>1.4 V/ms
BH40T08	0.83 mW	2.248 ns/pF	1.541 ns	2.785 ns/pF	4.615 ns	>140 V/s
BH40T10	0.83 mW	2.248 ns/pF	1.541 ns	2.785 ns/pF	4.615 ns	>140 V/s
BH40T15	0.83 mW	2.248 ns/pF	1.541 ns	2.785 ns/pF	4.615 ns	>140 V/s
BH40T20	0.83 mW	2.248 ns/pF	1.541 ns	2.785 ns/pF	4.615 ns	>140 V/s
BH40T40	0.83 mW	2.248 ns/pF	1.541 ns	2.785 ns/pF	4.615 ns	>140 V/s
BH80T80	0.32 mW	5.928 ns/pF	3.399 ns	5.327 ns/pF	8.519 ns	>72 V/s

1) Fast Process, VDD=5.5V, T=0° C
2) Nominal Process, VDD=5.0V, T=25° C

Cell Name	V- [3]	Hysteresis [4]	V+ [5]
BH10T08	1.022 V	323 mV	1.789 V
BH20T10	1.012 V	334 mV	1.773 V
BH20T15	1.012 V	334 mV	1.773 V
BH20T20	1.012 V	334 mV	1.773 V
BH20T30	1.012 V	334 mV	1.773 V
BH40T08	0.992 V	331 mV	1.727 V
BH40T10	0.992 V	331 mV	1.727 V
BH40T15	0.992 V	331 mV	1.727 V
BH40T20	0.992 V	331 mV	1.727 V
BH40T40	0.992 V	331 mV	1.727 V
BH80T80	0.985 V	286 mV	1.684 V

3) Fast N Process, Slow P Process, VDD=4.5V, T=100° C
4) Slow Process, VDD=4.5V, T=0° C
5) Slow N Process, Fast P Process, VDD=5.5V, T=0° C

Output Stage Circuit Performance

Cell Name	Delay [1]				
	T_{PHH}		T_{PLL}		Tri-State
	Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BH10T08D	0.283 ns/10pF	2.635 ns	0.271 ns/10pF	2.625 ns	0.630 ns
BH10T08H	0.283 ns/10pF	2.658 ns	0.271 ns/10pF	2.666 ns	
BH10T08T	0.297 ns/10pF	2.686 ns	0.384 ns/10pF	2.612 ns	
BH20T10D	0.461 ns/10pF	2.626 ns	0.455 ns/10pF	2.693 ns	1.016 ns
BH20T10H	0.461 ns/10pF	2.667 ns	0.455 ns/10pF	2.738 ns	
BH20T10T	0.464 ns/10pF	2.672 ns	0.480 ns/10pF	2.721 ns	
BH20T15D	0.594 ns/10pF	4.438 ns	0.588 ns/10pF	4.424 ns	2.042 ns
BH20T15H	0.594 ns/10pF	4.485 ns	0.587 ns/10pF	4.514 ns	
BH20T15T	0.597 ns/10pF	4.493 ns	0.609 ns/10pF	4.458 ns	
BH20T20D	0.779 ns/10pF	5.996 ns	0.771 ns/10pF	6.125 ns	2.995 ns
BH20T20H	0.779 ns/10pF	6.057 ns	0.771 ns/10pF	6.242 ns	
BH20T20T	0.781 ns/10pF	6.069 ns	0.789 ns/10pF	6.192 ns	
BH20T30D	1.847 ns/10pF	4.483 ns	1.617 ns/10pF	5.515 ns	2.157 ns
BH20T30H	1.847 ns/10pF	4.621 ns	1.617 ns/10pF	6.006 ns	
BH20T30T	1.848 ns/10pF	4.643 ns	1.624 ns/10pF	5.703 ns	
BH40T08D	0.283 ns/10pF	2.631 ns	0.271 ns/10pF	2.621 ns	0.630 ns
BH40T08H	0.283 ns/10pF	2.656 ns	0.271 ns/10pF	2.662 ns	
BH40T08T	0.297 ns/10pF	2.681 ns	0.384 ns/10pF	2.606 ns	
BH40T10D	0.461 ns/10pF	2.627 ns	0.455 ns/10pF	2.694 ns	1.016 ns
BH40T10H	0.461 ns/10pF	2.666 ns	0.455 ns/10pF	2.739 ns	
BH40T10T	0.464 ns/10pF	2.672 ns	0.480 ns/10pF	2.722 ns	
BH40T15D	0.594 ns/10pF	4.439 ns	0.588 ns/10pF	4.425 ns	2.042 ns
BH40T15H	0.594 ns/10pF	4.486 ns	0.587 ns/10pF	4.514 ns	
BH40T15T	0.597 ns/10pF	4.494 ns	0.609 ns/10pF	4.458 ns	
BH40T20D	0.779 ns/10pF	5.997 ns	0.771 ns/10pF	6.127 ns	2.995 ns
BH40T20H	0.779 ns/10pF	6.058 ns	0.771 ns/10pF	6.243 ns	
BH40T20T	0.781 ns/10pF	6.070 ns	0.789 ns/10pF	6.193 ns	
BH40T40D	3.113 ns/10pF	2.696 ns	3.083 ns/10pF	3.190 ns	1.211 ns
BH40T40T	3.111 ns/10pF	2.985 ns	3.108 ns/10pF	3.430 ns	
BH80T80D	7.051 ns/10pF	3.450 ns	6.976 ns/10pF	3.884 ns	0.858 ns
BH80T80T	7.052 ns/10pF	4.029 ns	6.996 ns/10pF	4.477 ns	

1) Nominal Process, VDD=5.0V, T=25° C

Circuit Performance

Cell Name	DC Current [1]	
	Sink	Source
BH10T08D	24.2 mA	38.0 mA
BH10T08H	24.2 mA	38.0 mA
BH10T08T	13.4 mA	33.0 mA
BH20T10D	12.1 mA	21.7 mA
BH20T10H	12.1 mA	21.7 mA
BH20T10T	11.2 mA	21.3 mA
BH20T15D	10.1 mA	17.2 mA
BH20T15H	10.1 mA	17.2 mA
BH20T15T	9.5 mA	17.0 mA
BH20T20D	8.1 mA	13.3 mA
BH20T20H	8.1 mA	13.3 mA
BH20T20T	7.7 mA	13.2 mA
BH20T30D	4.1 mA	5.6 mA
BH20T30H	4.1 mA	5.6 mA
BH20T30T	4.0 mA	5.6 mA
BH40T08D	24.2 mA	38.0 mA
BH40T08H	24.2 mA	38.0 mA
BH40T08T	13.4 mA	33.0 mA
BH40T10D	12.1 mA	21.7 mA
BH40T10H	12.1 mA	21.7 mA
BH40T10T	11.2 mA	21.3 mA
BH40T15D	10.1 mA	17.2 mA
BH40T15H	10.1 mA	17.2 mA
BH40T15T	9.5 mA	17.0 mA
BH40T20D	8.1 mA	13.3 mA
BH40T20H	8.1 mA	13.3 mA
BH40T20T	7.7 mA	13.2 mA
BH40T40D	2.2 mA	3.3 mA
BH40T40T	2.1 mA	3.3 mA
BH80T80D	1.0 mA	1.5 mA
BH80T80T	1.0 mA	1.5 mA

1) Slow Process, VDD=4.5V, T=100° C

Layout Information

Cell Name	Transistors	Cell Dimensions	
		X	Y
BH10T08D	30	352.000 µm	291.750 µm
BH10T08H		232.000 µm	540.125 µm
BH10T08T		214.000 µm	540.125 µm
BH20T10D	24	325.500 µm	291.750 µm
BH20T10H		205.500 µm	540.125 µm
BH20T10T		187.500 µm	540.125 µm
BH20T15D	22	316.500 µm	291.750 µm
BH20T15H		196.500 µm	540.125 µm
BH20T15T		178.500 µm	540.125 µm
BH20T20D	20	307.500 µm	291.750 µm
BH20T20H		187.500 µm	540.125 µm
BH20T20T		175.000 µm	540.125 µm
BH20T30D	18	298.500 µm	291.750 µm
BH20T30H		178.500 µm	540.125 µm
BH20T30T		175.000 µm	540.125 µm
BH40T08D	30	354.500 µm	291.750 µm
BH40T08H		234.500 µm	540.125 µm
BH40T08T		216.500 µm	540.125 µm
BH40T10D	24	327.500 µm	291.750 µm
BH40T10H		207.500 µm	540.125 µm
BH40T10T		189.500 µm	540.125 µm
BH40T15D	22	318.500 µm	291.750 µm
BH40T15H		198.500 µm	540.125 µm
BH40T15T		180.500 µm	540.125 µm
BH40T20D	20	309.500 µm	291.750 µm
BH40T20H		189.500 µm	540.125 µm
BH40T20T		175.000 µm	540.125 µm
BH40T40D	16	291.500 µm	291.750 µm
BH40T40T		175.000 µm	540.125 µm
BH80T80D	16	297.500 µm	291.750 µm
BH80T80T		175.000 µm	540.125 µm

Bi-Directional Buffer

BH*idXod[D,H,T]*

BIH- Input Stage, BOX- Output Stage

FUNCTIONAL DESCRIPTION:

Non-Inverting TTL-Level Input Stage with Hysteresis,
Driver Transistors Only (No Inherent Logic) Output Stage

CELL NAME DEFINITIONS:

id = WCS Input Stage Delay in ns @ 5pF load
od = WCS Output Stage Delay in ns @ 50pF load
[D,H,T] = Available Layout Formats

EXAMPLE: BH10X08D

INPUTS: N, P, PADI
OUTPUTS: Z, PADO

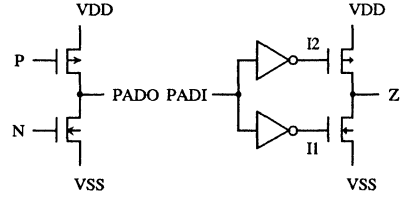
MOTIS Gate Count: 4

5

Truth Table

Inputs			Outputs	
N	P	PADI	Z	PADO
0	0	1	1	1
0	1	0	0	HI-Z
0	1	1	1	HI-Z
1	1	0	0	0

MOTIS Model



Circuit Capacitances

Cell Name	Node				
	N	P	PAD[D]*	PAD[H]*	PAD[T]*
BH10X08	1.718 pF	2.820 pF	4.390 pF	5.076 pF	5.112 pF
BH20X10	1.154 pF	1.680 pF	3.857 pF	4.540 pF	4.593 pF
BH20X15	0.861 pF	1.312 pF	3.317 pF	4.002 pF	4.070 pF
BH20X20	0.631 pF	0.992 pF	3.370 pF	4.056 pF	4.137 pF
BH20X30	0.288 pF	0.420 pF	2.766 pF	3.459 pF	3.565 pF
BH40X08	1.718 pF	2.820 pF	4.244 pF	4.923 pF	4.956 pF
BH40X10	1.154 pF	1.680 pF	3.876 pF	4.554 pF	4.604 pF
BH40X15	0.861 pF	1.312 pF	3.336 pF	4.015 pF	4.080 pF
BH40X20	0.631 pF	0.992 pF	3.389 pF	4.069 pF	4.147 pF
BH40X40	0.165 pF	0.246 pF	2.862 pF	NC	3.661 pF
BH80X80	0.095 pF	0.125 pF	2.844 pF	NC	3.608 pF

* Pad capacitance varies with layout format.
NC - Cell not available in this layout format.

Input Stage Circuit Performance

Cell Name	DC Power [1]	Delay [2]				Input Slew [1]
		T_{PHH}		T_{PLL}		
		Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BH10X08	5.87 mW	0.740 ns/pF	0.688 ns	0.623 ns/pF	1.323 ns	>2.4 V/ms
BH20X10	1.93 mW	1.612 ns/pF	1.016 ns	1.384 ns/pF	2.263 ns	>1.4 V/ms
BH20X15	1.93 mW	1.612 ns/pF	1.016 ns	1.384 ns/pF	2.263 ns	>1.4 V/ms
BH20X20	1.93 mW	1.612 ns/pF	1.016 ns	1.384 ns/pF	2.263 ns	>1.4 V/ms
BH20X30	1.93 mW	1.612 ns/pF	1.016 ns	1.384 ns/pF	2.263 ns	>1.4 V/ms
BH40X08	0.83 mW	2.248 ns/pF	1.541 ns	2.785 ns/pF	4.615 ns	>140 V/s
BH40X10	0.83 mW	2.248 ns/pF	1.541 ns	2.785 ns/pF	4.615 ns	>140 V/s
BH40X15	0.83 mW	2.248 ns/pF	1.541 ns	2.785 ns/pF	4.615 ns	>140 V/s
BH40X20	0.83 mW	2.248 ns/pF	1.541 ns	2.785 ns/pF	4.615 ns	>140 V/s
BH40X40	0.83 mW	2.248 ns/pF	1.541 ns	2.785 ns/pF	4.615 ns	>140 V/s
BH80X80	0.32 mW	5.928 ns/pF	3.399 ns	5.327 ns/pF	8.519 ns	>72 V/s

1) Fast Process, VDD=5.5V, T=0° C
2) Nominal Process, VDD=5.0V, T=25° C

Cell Name	V- [3]	Hysteresis [4]	V+ [5]
BH10X08	1.022 V	323 mV	1.789 V
BH20X10	1.012 V	334 mV	1.773 V
BH20X15	1.012 V	334 mV	1.773 V
BH20X20	1.012 V	334 mV	1.773 V
BH20X30	1.012 V	334 mV	1.773 V
BH40X08	0.992 V	331 mV	1.727 V
BH40X10	0.992 V	331 mV	1.727 V
BH40X15	0.992 V	331 mV	1.727 V
BH40X20	0.992 V	331 mV	1.727 V
BH40X40	0.992 V	331 mV	1.727 V
BH80X80	0.985 V	286 mV	1.684 V

3) Fast N Process, Slow P Process, VDD=4.5V, T=100° C
4) Slow Process, VDD=4.5V, T=0° C
5) Slow N Process, Fast P Process, VDD=5.5V, T=0° C

Output Stage Circuit Performance

Cell Name	Delay [1]				DC Current [2]	
	T_{PHL}		T_{PLH}			
	Extrinsic	Intrinsic	Extrinsic	Intrinsic	Sink	Source
BH10X08D	0.289 ns/10pF	1.765 ns	0.279 ns/10pF	1.968 ns	24.2 mA	38.0 mA
BH10X08H	0.288 ns/10pF	1.798 ns	0.279 ns/10pF	1.992 ns	24.2 mA	38.0 mA
BH10X08T	0.385 ns/10pF	1.789 ns	0.295 ns/10pF	2.041 ns	13.4 mA	33.0 mA
BH20X10D	0.442 ns/10pF	1.453 ns	0.458 ns/10pF	1.256 ns	12.1 mA	21.7 mA
BH20X10H	0.441 ns/10pF	1.498 ns	0.457 ns/10pF	1.292 ns	12.1 mA	21.7 mA
BH20X10T	0.463 ns/10pF	1.496 ns	0.461 ns/10pF	1.298 ns	11.2 mA	21.3 mA
BH20X15D	0.559 ns/10pF	1.302 ns	0.583 ns/10pF	0.991 ns	10.1 mA	17.2 mA
BH20X15H	0.559 ns/10pF	1.351 ns	0.583 ns/10pF	1.035 ns	10.1 mA	17.2 mA
BH20X15T	0.580 ns/10pF	1.350 ns	0.585 ns/10pF	1.045 ns	9.5 mA	17.0 mA
BH20X20D	0.723 ns/10pF	1.227 ns	0.763 ns/10pF	0.848 ns	8.1 mA	13.3 mA
BH20X20H	0.722 ns/10pF	1.290 ns	0.766 ns/10pF	0.892 ns	8.1 mA	13.3 mA
BH20X20T	0.740 ns/10pF	1.304 ns	0.765 ns/10pF	0.920 ns	7.7 mA	13.2 mA
BH20X30D	1.415 ns/10pF	1.950 ns	1.848 ns/10pF	0.862 ns	4.1 mA	5.6 mA
BH20X30H	1.412 ns/10pF	2.106 ns	1.849 ns/10pF	0.996 ns	4.1 mA	5.6 mA
BH20X30T	1.420 ns/10pF	2.121 ns	1.850 ns/10pF	1.015 ns	4.0 mA	5.6 mA
BH40X08D	0.289 ns/10pF	1.761 ns	0.279 ns/10pF	1.965 ns	24.2 mA	38.0 mA
BH40X08H	0.288 ns/10pF	1.794 ns	0.279 ns/10pF	1.989 ns	24.2 mA	38.0 mA
BH40X08T	0.385 ns/10pF	1.783 ns	0.295 ns/10pF	2.036 ns	13.4 mA	33.0 mA
BH40X10D	0.442 ns/10pF	1.454 ns	0.458 ns/10pF	1.257 ns	12.1 mA	21.7 mA
BH40X10H	0.441 ns/10pF	1.499 ns	0.457 ns/10pF	1.292 ns	12.1 mA	21.7 mA
BH40X10T	0.463 ns/10pF	1.496 ns	0.461 ns/10pF	1.298 ns	11.2 mA	21.3 mA
BH40X15D	0.559 ns/10pF	1.303 ns	0.583 ns/10pF	0.991 ns	10.1 mA	17.2 mA
BH40X15H	0.559 ns/10pF	1.352 ns	0.583 ns/10pF	1.036 ns	10.1 mA	17.2 mA
BH40X15T	0.580 ns/10pF	1.350 ns	0.585 ns/10pF	1.045 ns	9.5 mA	17.0 mA
BH40X20D	0.723 ns/10pF	1.228 ns	0.763 ns/10pF	0.849 ns	8.1 mA	13.3 mA
BH40X20H	0.722 ns/10pF	1.291 ns	0.766 ns/10pF	0.893 ns	8.1 mA	13.3 mA
BH40X20T	0.740 ns/10pF	1.305 ns	0.765 ns/10pF	0.920 ns	7.7 mA	13.2 mA
BH40X40D	2.520 ns/10pF	4.122 ns	3.140 ns/10pF	1.196 ns	2.2 mA	3.3 mA
BH40X40T	2.528 ns/10pF	4.478 ns	3.140 ns/10pF	1.479 ns	2.1 mA	3.3 mA
BH80X80D	6.844 ns/10pF	3.075 ns	7.050 ns/10pF	2.360 ns	1.0 mA	1.5 mA
BH80X80T	6.861 ns/10pF	3.674 ns	7.051 ns/10pF	2.941 ns	1.0 mA	1.5 mA

1) Nominal Process, VDD=5.0V, T=25° C
2) Slow Process, VDD=4.5V, T=100° C

Layout Information

Cell Name	Transistors	Cell Dimensions	
		X	Y
BH10X08D BH10X08H BH10X08T	22	326.250 µm 206.250 µm 188.250 µm	291.750 µm 540.125 µm 540.125 µm
BH20X10D BH20X10H BH20X10T	16	299.750 µm 179.750 µm 175.000 µm	291.750 µm 540.125 µm 540.125 µm
BH20X15D BH20X15H BH20X15T	14	290.750 µm 175.000 µm 175.000 µm	291.750 µm 540.125 µm 540.125 µm
BH20X20D BH20X20H BH20X20T	12	281.750 µm 175.000 µm 175.000 µm	291.750 µm 540.125 µm 540.125 µm
BH20X30D BH20X30H BH20X30T	10	272.750 µm 175.000 µm 175.000 µm	291.750 µm 540.125 µm 540.125 µm
BH40X08D BH40X08H BH40X08T	22	328.750 µm 208.750 µm 190.750 µm	291.750 µm 540.125 µm 540.125 µm
BH40X10D BH40X10H BH40X10T	16	301.750 µm 181.750 µm 175.000 µm	291.750 µm 540.125 µm 540.125 µm
BH40X15D BH40X15H BH40X15T	14	292.750 µm 175.000 µm 175.000 µm	291.750 µm 540.125 µm 540.125 µm
BH40X20D BH40X20H BH40X20T	12	283.750 µm 175.000 µm 175.000 µm	291.750 µm 540.125 µm 540.125 µm
BH40X40D BH40X40T	8	265.750 µm 175.000 µm	291.750 µm 540.125 µm
BH80X80D BH80X80T	8	271.750 µm 175.000 µm	291.750 µm 540.125 µm

FUNCTIONAL DESCRIPTION:
Non-Inverting TTL-Level Input Buffer with Hysteresis

CELL NAME DEFINITIONS:
id = WCS Delay in ns @ 5pF load
[D,P,T] = Available Layout Formats

EXAMPLE: BIH10D

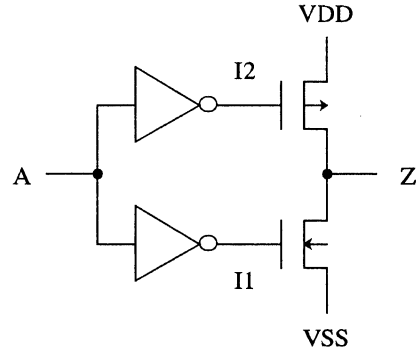
INPUTS: A
OUTPUTS: Z

Transistors: 6
MOTIS Gate Count: 3

Truth Table

Input	Output
A	Z
0	0
1	1

MOTIS Model



Circuit Capacitances

Cell Name	Node		
	A[D]*	A[P]*	A[T]*
BIH10	2.678 pF	2.324 pF	3.270 pF
BIH20	2.514 pF	2.160 pF	3.106 pF
BIH40	2.533 pF	2.179 pF	3.124 pF
BIH80	2.678 pF	2.324 pF	3.267 pF

* Pad capacitance varies with layout format.

Circuit Performance

Cell Name	DC Power [1]	Delay [2]				Input Slew [1]
		T_{PHH}		T_{PLL}		
		Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BIH10	5.87 mW	0.740 ns/pF	0.688 ns	0.623 ns/pF	1.323 ns	>2.4 V/ms
BIH20	1.93 mW	1.612 ns/pF	1.016 ns	1.384 ns/pF	2.263 ns	>1.4 V/ms
BIH40	0.83 mW	2.248 ns/pF	1.541 ns	2.785 ns/pF	4.615 ns	>140 V/s
BIH80	0.32 mW	5.928 ns/pF	3.399 ns	5.327 ns/pF	8.519 ns	>72 V/s

1) Fast Process, VDD=5.5V, T=0° C
2) Nominal Process, VDD=5.0V, T=25° C

Cell Name	V- [3]	Hysteresis [4]	V+ [5]
BIH10	1.022 V	323 mV	1.789 V
BIH20	1.012 V	334 mV	1.773 V
BIH40	0.992 V	331 mV	1.727 V
BIH80	0.985 V	286 mV	1.684 V

3) Fast N Process, Slow P Process, VDD=4.5V, T=100° C
4) Slow Process, VDD=4.5V, T=0° C
5) Slow N Process, Fast P Process, VDD=5.5V, T=0° C

Layout Dimensions

Cell Name	Cell Dimensions	
	X	Y
BIH10D	227.375 µm	291.750 µm
BIH10P	219.500 µm	291.750 µm
BIH10T	175.000 µm	540.125 µm
BIH20D	227.875 µm	291.750 µm
BIH20P	220.000 µm	291.750 µm
BIH20T	175.000 µm	540.125 µm
BIH40D	229.875 µm	291.750 µm
BIH40P	222.000 µm	291.750 µm
BIH40T	175.000 µm	540.125 µm
BIH80D	235.875 µm	291.750 µm
BIH80P	228.000 µm	291.750 µm
BIH80T	175.000 µm	540.125 µm

FUNCTIONAL DESCRIPTION:
Inverting CMOS-Level Input Buffer

CELL NAME DEFINITIONS:
id = WCS Delay in ns @ 5pF load
[D,P,T] = Available Layout Formats

EXAMPLE: BIM03D

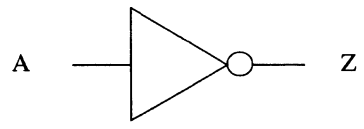
INPUTS: A
OUTPUTS: Z

Transistors: 2
MOTIS Gate Count: 1

Truth Table

Input	Output
A	Z
0	1
1	0

MOTIS Model



Circuit Capacitances

Cell Name	Node		
	A[D]*	A[P]*	A[T]*
BIM03	2.782 pF	2.428 pF	3.382 pF
BIM05	2.622 pF	2.268 pF	3.222 pF
BIM10	2.517 pF	2.163 pF	3.116 pF

* Pad capacitance varies with layout format.

Circuit Performance

Cell Name	DC Power [1]	Delay [2]				Input Slew [1]
		T_{PHL}		T_{PLH}		
		Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BIM03	0.51 µW	0.231 ns/pF	0.393 ns	0.235 ns/pF	0.407 ns	NA
BIM05	0.28 µW	0.416 ns/pF	0.398 ns	0.417 ns/pF	0.417 ns	NA
BIM10	0.14 µW	0.866 ns/pF	0.472 ns	0.867 ns/pF	0.499 ns	NA

1) Fast Process, VDD=5.5V, T=0° C
2) Nominal Process, VDD=5.0V, T=25° C
NA) Not Applicable.

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Cell Name	V_{LO} [3]	V_{HI} [4]
BIM03	1.989 V	2.796 V
BIM05	1.984 V	2.792 V
BIM10	1.972 V	2.785 V

3) Fast N Process, Slow P Process, VDD=4.5V, T=100° C
4) Slow N Process, Fast P Process, VDD=5.5V, T=0° C

Layout Dimensions

Cell Name	Cell Dimensions	
	X	Y
BIM03D	205.875 µm	291.750 µm
BIM03P	198.000 µm	291.750 µm
BIM03T	175.000 µm	540.125 µm
BIM05D	205.875 µm	291.750 µm
BIM05P	198.000 µm	291.750 µm
BIM05T	175.000 µm	540.125 µm
BIM10D	205.875 µm	291.750 µm
BIM10P	198.000 µm	291.750 µm
BIM10T	175.000 µm	540.125 µm

FUNCTIONAL DESCRIPTION:
Non-Inverting TTL-Level Input Buffer

CELL NAME DEFINITIONS:
id = WCS Delay in ns @ 5pF load
[D,P,T] = Available Layout Formats

EXAMPLE: BIN06D

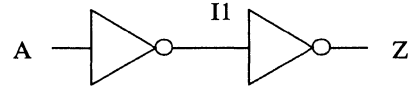
INPUTS: A
OUTPUTS: Z

Transistors: 4
MOTIS Gate Count: 2

Truth Table

Input	Output
A	Z
0	0
1	1

MOTIS Model



Circuit Capacitances

Cell Name	Node		
	A[D]*	A[P]*	A[T]*
BIN06	2.574 pF	2.220 pF	3.169 pF
BIN10	2.481 pF	2.127 pF	3.077 pF
BIN15	2.448 pF	2.094 pF	3.044 pF
BIN20	2.437 pF	2.083 pF	3.033 pF
BIN25	2.434 pF	2.080 pF	3.029 pF

* Pad capacitance varies with layout format.

Circuit Performance

Cell Name	DC Power [1]	Delay [2]				Input Slew [1]
		T_{PHH}		T_{PLL}		
		Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BIN06	7.29 mW	0.451 ns/pF	0.383 ns	0.349 ns/pF	0.893 ns	>2.38 V/µs
BIN10	2.90 mW	0.756 ns/pF	0.540 ns	0.655 ns/pF	1.253 ns	>1.33 V/µs
BIN15	1.35 mW	1.101 ns/pF	0.713 ns	1.004 ns/pF	1.886 ns	>0.63 V/µs
BIN20	0.82 mW	1.596 ns/pF	0.909 ns	1.354 ns/pF	2.548 ns	>0.36 V/µs
BIN25	0.64 mW	2.059 ns/pF	1.045 ns	1.729 ns/pF	3.014 ns	>0.29 V/µs

1) Fast Process, VDD=5.5V, T=0° C
2) Nominal Process, VDD=5.0V, T=25° C

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Cell Name	V_{LO} [3]	V_{HI} [4]
BIN06	1.156 V	1.655 V
BIN10	1.152 V	1.642 V
BIN15	1.147 V	1.618 V
BIN20	1.142 V	1.590 V
BIN25	1.136 V	1.566 V

3) Fast N Process, Slow P Process, VDD=4.5V, T=100° C
4) Slow N Process, Fast P Process, VDD=5.5V, T=0° C

Layout Dimensions

Cell Name	Cell Dimensions	
	X	Y
BIN06D	216.625 µm	291.750 µm
BIN06P	208.750 µm	291.750 µm
BIN06T	175.000 µm	540.125 µm
BIN10D	216.625 µm	291.750 µm
BIN10P	208.750 µm	291.750 µm
BIN10T	175.000 µm	540.125 µm
BIN15D	216.625 µm	291.750 µm
BIN15P	208.750 µm	291.750 µm
BIN15T	175.000 µm	540.125 µm
BIN20D	217.125 µm	291.750 µm
BIN20P	209.250 µm	291.750 µm
BIN20T	175.000 µm	540.125 µm
BIN25D	217.125 µm	291.750 µm
BIN25P	209.250 µm	291.750 µm
BIN25T	175.000 µm	540.125 µm

Input Buffer

BIP02*[D,P,T]*

FUNCTIONAL DESCRIPTION:
ESD Protection Only, No Active Logic

CELL NAME DEFINITIONS:
[D,P,T] = Available Layout Formats

INPUTS: A
OUTPUTS: Z

Transistors: 0
MOTIS Gate Count: 0

5

Truth Table

Input	Output
A	Z
0	0
1	1

MOTIS Model

Circuit Capacitances

Cell Name	Node		
	A[D]*	A[P]*	A[T]*
BIP02	2.448 pF	2.094 pF	3.049 pF

* Pad capacitance varies with layout format.

Circuit Performance

Cell Name	DC Power [1]	Delay [2]				Input Slew [1]
		T_{PHH}		T_{PLL}		
		Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BIP02	Nil	0.125 ns/pF	0.076 ns	0.125 ns/pF	0.077 ns	NA

1) Fast Process, VDD=5.5V, T=0° C
2) Nominal Process, VDD=5.0V, T=25° C
NA) Not Applicable.

Layout Dimensions

Cell Name	Cell Dimensions	
	X	Y
BIP02D	200.875 µm	291.750 µm
BIP02P	193.000 µm	291.750 µm
BIP02T	175.000 µm	540.125 µm

Bi-Directional Buffer

BN*id*T*od*[D,H,T]

BIN- Input Stage, BOT- Output Stage

FUNCTIONAL DESCRIPTION:

Non-Inverting TTL-Level Input Stage,
Non-Inverting TTL-Level Tri-State Output Stage

CELL NAME DEFINITIONS:

id = WCS Input Stage Delay in ns @ 5pF load
od = WCS Output Stage Delay in ns @ 50pF load
[D,H,T] = Available Layout Formats

EXAMPLE: BN06T08D

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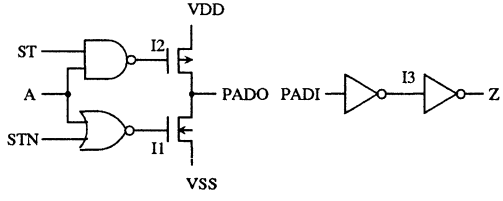
INPUTS: A, ST, STN, PADI
OUTPUTS: Z, PADO

MOTIS Gate Count: 5

Truth Table

Inputs				Outputs	
A	ST	STN	PADI	Z	PADO
0	X	0	0	0	0
0	X	1	0	0	HI-Z
0	X	1	1	1	HI-Z
1	0	X	0	0	HI-Z
1	0	X	1	1	HI-Z
1	1	X	1	1	1

MOTIS Model



Circuit Capacitances

Cell Name	Node					
	A	ST	STN	PAD[D]*	PAD[H]*	PAD[T]*
BN06T08	0.742 pF	0.408 pF	0.342 pF	4.286 pF	5.002 pF	5.051 pF
BN10T10	0.400 pF	0.226 pF	0.194 pF	3.825 pF	4.539 pF	4.602 pF
BN15T08	0.742 pF	0.408 pF	0.342 pF	4.161 pF	4.877 pF	4.925 pF
BN15T15	0.183 pF	0.110 pF	0.099 pF	3.251 pF	3.969 pF	4.049 pF
BN20T10	0.400 pF	0.226 pF	0.194 pF	3.782 pF	4.493 pF	4.557 pF
BN20T20	0.120 pF	0.077 pF	0.072 pF	3.295 pF	4.013 pF	4.108 pF
BN20T30	0.098 pF	0.064 pF	0.063 pF	2.690 pF	3.425 pF	3.552 pF
BN25T15	0.183 pF	0.110 pF	0.099 pF	3.236 pF	3.953 pF	4.033 pF
BN25T20	0.120 pF	0.077 pF	0.072 pF	3.291 pF	4.010 pF	4.104 pF
BN25T40	0.112 pF	0.071 pF	0.070 pF	2.760 pF	NC	3.638 pF
BN25T80	0.097 pF	0.064 pF	0.063 pF	2.597 pF	NC	3.475 pF

* Pad capacitance varies with layout format.
NC - Cell not available in this layout format.

Input Stage Circuit Performance

Cell Name	DC Power [1]	Delay [2]				Input Slew [1]
		T_{PHH}		T_{PLL}		
		Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BN06T08	7.29 mW	0.451 ns/pF	0.383 ns	0.349 ns/pF	0.893 ns	>2.38 V/µs
BN10T10	2.90 mW	0.756 ns/pF	0.540 ns	0.655 ns/pF	1.253 ns	>1.33 V/µs
BN15T08	1.35 mW	1.101 ns/pF	0.713 ns	1.004 ns/pF	1.886 ns	>0.63 V/µs
BN15T15	1.35 mW	1.101 ns/pF	0.713 ns	1.004 ns/pF	1.886 ns	>0.63 V/µs
BN20T10	0.82 mW	1.596 ns/pF	0.909 ns	1.354 ns/pF	2.548 ns	>0.36 V/µs
BN20T20	0.82 mW	1.596 ns/pF	0.909 ns	1.354 ns/pF	2.548 ns	>0.36 V/µs
BN20T30	0.82 mW	1.596 ns/pF	0.909 ns	1.354 ns/pF	2.548 ns	>0.36 V/µs
BN25T15	0.64 mW	2.059 ns/pF	1.045 ns	1.729 ns/pF	3.014 ns	>0.29 V/µs
BN25T20	0.64 mW	2.059 ns/pF	1.045 ns	1.729 ns/pF	3.014 ns	>0.29 V/µs
BN25T40	0.64 mW	2.059 ns/pF	1.045 ns	1.729 ns/pF	3.014 ns	>0.29 V/µs
BN25T80	0.64 mW	2.059 ns/pF	1.045 ns	1.729 ns/pF	3.014 ns	>0.29 V/µs

1) Fast Process, VDD=5.5V, T=0° C
2) Nominal Process, VDD=5.0V, T=25° C

Cell Name	V_{LO} [3]	V_{HI} [4]
BN06T08	1.156 V	1.655 V
BN10T10	1.152 V	1.642 V
BN15T08	1.147 V	1.618 V
BN15T15	1.147 V	1.618 V
BN20T10	1.142 V	1.590 V
BN20T20	1.142 V	1.590 V
BN20T30	1.142 V	1.590 V
BN25T15	1.136 V	1.566 V
BN25T20	1.136 V	1.566 V
BN25T40	1.136 V	1.566 V
BN25T80	1.136 V	1.566 V

3) Fast N Process, Slow P Process, VDD=4.5V, T=100° C
4) Slow N Process, Fast P Process, VDD=5.5V, T=0° C

Output Stage Circuit Performance

Cell Name	Delay [1]				
	T_{PHH}		T_{PLL}		Tri-State
	Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BN06T08D	0.283 ns/10pF	2.632 ns	0.271 ns/10pF	2.622 ns	0.630 ns
BN06T08H	0.283 ns/10pF	2.656 ns	0.271 ns/10pF	2.664 ns	
BN06T08T	0.297 ns/10pF	2.684 ns	0.384 ns/10pF	2.610 ns	
BN10T10D	0.461 ns/10pF	2.625 ns	0.455 ns/10pF	2.692 ns	1.016 ns
BN10T10H	0.461 ns/10pF	2.820 ns	0.455 ns/10pF	2.738 ns	
BN10T10T	0.464 ns/10pF	2.672 ns	0.480 ns/10pF	2.722 ns	
BN15T08D	0.283 ns/10pF	2.629 ns	0.271 ns/10pF	2.619 ns	0.630 ns
BN15T08H	0.283 ns/10pF	2.653 ns	0.271 ns/10pF	2.661 ns	
BN15T08T	0.297 ns/10pF	2.680 ns	0.384 ns/10pF	2.605 ns	
BN15T15D	0.594 ns/10pF	4.434 ns	0.588 ns/10pF	4.420 ns	2.042 ns
BN15T15H	0.594 ns/10pF	4.483 ns	0.587 ns/10pF	4.512 ns	
BN15T15T	0.597 ns/10pF	4.492 ns	0.609 ns/10pF	4.456 ns	
BN20T10D	0.461 ns/10pF	2.622 ns	0.455 ns/10pF	2.690 ns	1.016 ns
BN20T10H	0.461 ns/10pF	2.663 ns	0.455 ns/10pF	2.735 ns	
BN20T10T	0.464 ns/10pF	2.670 ns	0.480 ns/10pF	2.720 ns	
BN20T20D	0.779 ns/10pF	5.990 ns	0.771 ns/10pF	6.119 ns	2.995 ns
BN20T20H	0.779 ns/10pF	6.053 ns	0.771 ns/10pF	6.239 ns	
BN20T20T	0.781 ns/10pF	6.066 ns	0.789 ns/10pF	6.189 ns	
BN20T30D	1.847 ns/10pF	4.468 ns	1.617 ns/10pF	5.503 ns	2.157 ns
BN20T30H	1.847 ns/10pF	4.614 ns	1.617 ns/10pF	6.001 ns	
BN20T30T	1.848 ns/10pF	4.641 ns	1.624 ns/10pF	5.702 ns	
BN25T15D	0.594 ns/10pF	4.433 ns	0.588 ns/10pF	4.419 ns	2.042 ns
BN25T15H	0.594 ns/10pF	4.482 ns	0.587 ns/10pF	4.511 ns	
BN25T15T	0.597 ns/10pF	4.489 ns	0.609 ns/10pF	4.453 ns	
BN25T20D	0.779 ns/10pF	5.990 ns	0.771 ns/10pF	6.119 ns	2.995 ns
BN25T20H	0.779 ns/10pF	6.053 ns	0.771 ns/10pF	6.239 ns	
BN25T20T	0.781 ns/10pF	6.066 ns	0.789 ns/10pF	6.190 ns	
BN25T40D	3.113 ns/10pF	2.665 ns	3.083 ns/10pF	3.160 ns	1.211 ns
BN25T40T	3.111 ns/10pF	2.978 ns	3.108 ns/10pF	3.423 ns	
BN25T80D	7.051 ns/10pF	3.278 ns	6.976 ns/10pF	3.714 ns	0.858 ns
BN25T80T	7.052 ns/10pF	3.936 ns	6.996 ns/10pF	4.386 ns	

1) Nominal Process, VDD=5.0V, T=25° C

Bi-Directional Buffer

BN*id*T*od[D,H,T]*

Circuit Performance

Cell Name	DC Current [1]	
	Sink	Source
BN06T08D	24.2 mA	38.0 mA
BN06T08H	24.2 mA	38.0 mA
BN06T08T	13.4 mA	33.0 mA
BN10T10D	12.1 mA	21.7 mA
BN10T10H	12.1 mA	21.7 mA
BN10T10T	11.2 mA	21.3 mA
BN15T08D	24.2 mA	38.0 mA
BN15T08H	24.2 mA	38.0 mA
BN15T08T	13.4 mA	33.0 mA
BN15T15D	10.1 mA	17.2 mA
BN15T15H	10.1 mA	17.2 mA
BN15T15T	9.5 mA	17.0 mA
BN20T10D	12.1 mA	21.7 mA
BN20T10H	12.1 mA	21.7 mA
BN20T10T	11.2 mA	21.3 mA
BN20T20D	8.1 mA	13.3 mA
BN20T20H	8.1 mA	13.3 mA
BN20T20T	7.7 mA	13.2 mA
BN20T30D	4.1 mA	5.6 mA
BN20T30H	4.1 mA	5.6 mA
BN20T30T	4.0 mA	5.6 mA
BN25T15D	10.1 mA	17.2 mA
BN25T15H	10.1 mA	17.2 mA
BN25T15T	9.5 mA	17.0 mA
BN25T20D	8.1 mA	13.3 mA
BN25T20H	8.1 mA	13.3 mA
BN25T20T	7.7 mA	13.2 mA
BN25T40D	2.2 mA	3.3 mA
BN25T40T	2.1 mA	3.3 mA
BN25T80D	1.0 mA	1.5 mA
BN25T80T	1.0 mA	1.5 mA

1) Slow Process, VDD=4.5V, T=100° C

Layout Information

Cell Name	Transistors	Cell Dimensions	
		X	Y
BN06T08D	28	341.250 µm	291.750 µm
BN06T08H		221.250 µm	540.125 µm
BN06T08T		203.250 µm	540.125 µm
BN10T10D	22	314.250 µm	291.750 µm
BN10T10H		194.250 µm	540.125 µm
BN10T10T		176.250 µm	540.125 µm
BN15T08D	28	341.250 µm	291.750 µm
BN15T08H		221.250 µm	540.125 µm
BN15T08T		203.250 µm	540.125 µm
BN15T15D	20	305.250 µm	291.750 µm
BN15T15H		185.250 µm	540.125 µm
BN15T15T		175.000 µm	540.125 µm
BN20T10D	22	314.750 µm	291.750 µm
BN20T10H		194.750 µm	540.125 µm
BN20T10T		176.750 µm	540.125 µm
BN20T20D	18	296.750 µm	291.750 µm
BN20T20H		176.750 µm	540.125 µm
BN20T20T		175.000 µm	540.125 µm
BN20T30D	16	287.750 µm	291.750 µm
BN20T30H		175.000 µm	540.125 µm
BN20T30T		175.000 µm	540.125 µm
BN25T15D	20	305.750 µm	291.750 µm
BN25T15H		185.750 µm	540.125 µm
BN25T15T		175.000 µm	540.125 µm
BN25T20D	18	296.750 µm	291.750 µm
BN25T20H		176.750 µm	540.125 µm
BN25T20T		175.000 µm	540.125 µm
BN25T40D	14	278.750 µm	291.750 µm
BN25T40T		175.000 µm	540.125 µm
BN25T80D	14	278.750 µm	291.750 µm
BN25T80T		175.000 µm	540.125 µm

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Bi-Directional Buffer

BN*idXod[D,H,T]*

BIN- Input Stage, BOX- Output Stage

FUNCTIONAL DESCRIPTION:

Non-Inverting TTL-Level Input Stage with Hysteresis,
Driver Transistors Only (No Inherent Logic) Output Stage

CELL NAME DEFINITIONS:

id = WCS Input Stage Delay in ns @ 5pF load
od = WCS Output Stage Delay in ns @ 50pF load
[D,H,T] = Available Layout Formats

EXAMPLE: BN06X08D

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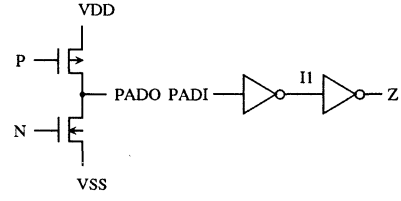
INPUTS: N, P, PADI
OUTPUTS: Z, PADO

MOTIS Gate Count: 3

Truth Table

Inputs			Outputs	
N	P	PADI	Z	PADO
0	0	1	1	1
0	1	0	0	HI-Z
0	1	1	1	HI-Z
1	1	0	0	0

MOTIS Model



Circuit Capacitances

Cell Name	Node				
	N	P	PAD[D]*	PAD[H]*	PAD[T]*
BN06X08	1.718 pF	2.820 pF	4.285 pF	5.001 pF	5.050 pF
BN10X10	1.154 pF	1.680 pF	3.824 pF	4.537 pF	4.600 pF
BN15X08	1.718 pF	2.820 pF	4.160 pF	4.876 pF	4.924 pF
BN15X15	0.861 pF	1.312 pF	3.252 pF	3.970 pF	4.050 pF
BN20X10	1.154 pF	1.680 pF	3.781 pF	4.491 pF	4.555 pF
BN20X20	0.631 pF	0.992 pF	3.294 pF	4.012 pF	4.107 pF
BN20X30	0.288 pF	0.420 pF	2.690 pF	3.425 pF	3.553 pF
BN25X15	0.861 pF	1.312 pF	3.237 pF	3.954 pF	4.033 pF
BN25X20	0.631 pF	0.992 pF	3.290 pF	4.009 pF	4.103 pF
BN25X40	0.165 pF	0.246 pF	2.763 pF	NC	3.638 pF
BN25X80	0.095 pF	0.125 pF	2.600 pF	NC	3.475 pF

* Pad capacitance varies with layout format.
NC - Cell not available in this layout format.

Input Stage Circuit Performance

Cell Name	DC Power [1]	Delay [2]				Input Slew [1]
		T_{PHH}		T_{PLL}		
		Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BN06X08	7.29 mW	0.451 ns/pF	0.383 ns	0.349 ns/pF	0.893 ns	>2.38 V/µs
BN10X10	2.90 mW	0.756 ns/pF	0.540 ns	0.655 ns/pF	1.253 ns	>1.33 V/µs
BN15X08	1.35 mW	1.101 ns/pF	0.713 ns	1.004 ns/pF	1.886 ns	>0.63 V/µs
BN15X15	1.35 mW	1.101 ns/pF	0.713 ns	1.004 ns/pF	1.886 ns	>0.63 V/µs
BN20X10	0.82 mW	1.596 ns/pF	0.909 ns	1.354 ns/pF	2.548 ns	>0.36 V/µs
BN20X20	0.82 mW	1.596 ns/pF	0.909 ns	1.354 ns/pF	2.548 ns	>0.36 V/µs
BN20X30	0.82 mW	1.596 ns/pF	0.909 ns	1.354 ns/pF	2.548 ns	>0.36 V/µs
BN25X15	0.64 mW	2.059 ns/pF	1.045 ns	1.729 ns/pF	3.014 ns	>0.29 V/µs
BN25X20	0.64 mW	2.059 ns/pF	1.045 ns	1.729 ns/pF	3.014 ns	>0.29 V/µs
BN25X40	0.64 mW	2.059 ns/pF	1.045 ns	1.729 ns/pF	3.014 ns	>0.29 V/µs
BN25X80	0.64 mW	2.059 ns/pF	1.045 ns	1.729 ns/pF	3.014 ns	>0.29 V/µs

1) Fast Process, VDD=5.5V, T=0° C
2) Nominal Process, VDD=5.0V, T=25° C

Cell Name	V_{LO} [3]	V_{HI} [4]
BN06X08	1.156 V	1.655 V
BN10X10	1.152 V	1.642 V
BN15X08	1.147 V	1.618 V
BN15X15	1.147 V	1.618 V
BN20X10	1.142 V	1.590 V
BN20X20	1.142 V	1.590 V
BN20X30	1.142 V	1.590 V
BN25X15	1.136 V	1.566 V
BN25X20	1.136 V	1.566 V
BN25X40	1.136 V	1.566 V
BN25X80	1.136 V	1.566 V

3) Fast N Process, Slow P Process, VDD=4.5V, T=100° C
4) Slow N Process, Fast P Process, VDD=5.5V, T=0° C

Output Stage Circuit Performance

Cell Name	Delay [1]				DC Current [2]	
	T_{PHL}		T_{PLH}			
	Extrinsic	Intrinsic	Extrinsic	Intrinsic	Sink	Source
BN06X08D	0.289 ns/10pF	1.762 ns	0.279 ns/10pF	1.966 ns	24.2 mA	38.0 mA
BN06X08H	0.288 ns/10pF	1.796 ns	0.279 ns/10pF	1.990 ns	24.2 mA	38.0 mA
BN06X08T	0.385 ns/10pF	1.786 ns	0.295 ns/10pF	2.039 ns	13.4 mA	33.0 mA
BN10X10D	0.442 ns/10pF	1.452 ns	0.458 ns/10pF	1.255 ns	12.1 mA	21.7 mA
BN10X10H	0.441 ns/10pF	1.498 ns	0.457 ns/10pF	1.292 ns	12.1 mA	21.7 mA
BN10X10T	0.463 ns/10pF	1.496 ns	0.461 ns/10pF	1.298 ns	11.2 mA	21.3 mA
BN15X08D	0.289 ns/10pF	1.759 ns	0.279 ns/10pF	1.962 ns	24.2 mA	38.0 mA
BN15X08H	0.288 ns/10pF	1.793 ns	0.279 ns/10pF	1.987 ns	24.2 mA	38.0 mA
BN15X08T	0.385 ns/10pF	1.781 ns	0.295 ns/10pF	2.035 ns	13.4 mA	33.0 mA
BN15X15D	0.559 ns/10pF	1.299 ns	0.583 ns/10pF	0.987 ns	10.1 mA	17.2 mA
BN15X15H	0.559 ns/10pF	1.349 ns	0.583 ns/10pF	1.033 ns	10.1 mA	17.2 mA
BN15X15T	0.580 ns/10pF	1.348 ns	0.585 ns/10pF	1.044 ns	9.5 mA	17.0 mA
BN20X10D	0.442 ns/10pF	1.450 ns	0.458 ns/10pF	1.253 ns	12.1 mA	21.7 mA
BN20X10H	0.441 ns/10pF	1.496 ns	0.457 ns/10pF	1.290 ns	12.1 mA	21.7 mA
BN20X10T	0.463 ns/10pF	1.494 ns	0.461 ns/10pF	1.296 ns	11.2 mA	21.3 mA
BN20X20D	0.723 ns/10pF	1.221 ns	0.763 ns/10pF	0.842 ns	8.1 mA	13.3 mA
BN20X20H	0.722 ns/10pF	1.293 ns	0.766 ns/10pF	0.896 ns	8.1 mA	13.3 mA
BN20X20T	0.740 ns/10pF	1.302 ns	0.765 ns/10pF	0.917 ns	7.7 mA	13.2 mA
BN20X30D	1.415 ns/10pF	1.939 ns	1.848 ns/10pF	0.848 ns	4.1 mA	5.6 mA
BN20X30H	1.412 ns/10pF	2.101 ns	1.849 ns/10pF	0.990 ns	4.1 mA	5.6 mA
BN20X30T	1.420 ns/10pF	2.119 ns	1.850 ns/10pF	1.013 ns	4.0 mA	5.6 mA
BN25X15D	0.559 ns/10pF	1.298 ns	0.583 ns/10pF	0.986 ns	10.1 mA	17.2 mA
BN25X15H	0.559 ns/10pF	1.348 ns	0.583 ns/10pF	1.032 ns	10.1 mA	17.2 mA
BN25X15T	0.580 ns/10pF	1.347 ns	0.585 ns/10pF	1.042 ns	9.5 mA	17.0 mA
BN25X20D	0.723 ns/10pF	1.265 ns	0.763 ns/10pF	0.888 ns	8.1 mA	13.3 mA
BN25X20H	0.722 ns/10pF	1.287 ns	0.766 ns/10pF	0.888 ns	8.1 mA	13.3 mA
BN25X20T	0.740 ns/10pF	1.302 ns	0.765 ns/10pF	0.917 ns	7.7 mA	13.2 mA
BN25X40D	2.520 ns/10pF	4.097 ns	3.140 ns/10pF	1.165 ns	2.2 mA	3.3 mA
BN25X40T	2.528 ns/10pF	4.473 ns	3.140 ns/10pF	1.472 ns	2.1 mA	3.3 mA
BN25X80D	6.844 ns/10pF	2.908 ns	7.050 ns/10pF	2.188 ns	1.0 mA	1.5 mA
BN25X80T	6.861 ns/10pF	3.582 ns	7.051 ns/10pF	2.848 ns	1.0 mA	1.5 mA

1) Nominal Process, VDD=5.0V, T=25° C
2) Slow Process, VDD=4.5V, T=100° C

Layout Information

Cell Name	Transistors	Cell Dimensions	
		X	Y
BN06X08D	20	315.500 µm	291.750 µm
BN06X08H		195.500 µm	540.125 µm
BN06X08T		177.500 µm	540.125 µm
BN10X10D	14	288.500 µm	291.750 µm
BN10X10H		175.000 µm	540.125 µm
BN10X10T		175.000 µm	540.125 µm
BN15X08D	20	315.500 µm	291.750 µm
BN15X08H		195.500 µm	540.125 µm
BN15X08T		177.500 µm	540.125 µm
BN15X15D	12	279.500 µm	291.750 µm
BN15X15H		175.000 µm	540.125 µm
BN15X15T		175.000 µm	540.125 µm
BN20X10D	14	289.000 µm	291.750 µm
BN20X10H		175.000 µm	540.125 µm
BN20X10T		175.000 µm	540.125 µm
BN20X20D	10	271.000 µm	291.750 µm
BN20X20H		175.000 µm	540.125 µm
BN20X20T		175.000 µm	540.125 µm
BN20X30D	8	262.000 µm	291.750 µm
BN20X30H		175.000 µm	540.125 µm
BN20X30T		175.000 µm	540.125 µm
BN25X15D	12	280.000 µm	291.750 µm
BN25X15H		175.000 µm	540.125 µm
BN25X15T		175.000 µm	540.125 µm
BN25X20D	10	271.000 µm	291.750 µm
BN25X20H		175.000 µm	540.125 µm
BN25X20T		175.000 µm	540.125 µm
BN25X40D	6	253.000 µm	291.750 µm
BN25X40T		175.000 µm	540.125 µm
BN25X80D	6	253.000 µm	291.750 µm
BN25X80T		175.000 µm	540.125 µm

FUNCTIONAL DESCRIPTION:

Non-Inverting TTL-Level Open Collector Output Buffer

CELL NAME DEFINITIONS:

od = WCS Delay in ns @ 50pF load
[D,H,P,T] = Available Layout Formats

EXAMPLE: BOC08D

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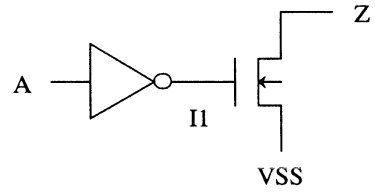
INPUTS: A
OUTPUTS: Z

MOTIS Gate Count: 2

Truth Table

Input	Output
A	Z
0	0
1	HI-Z

MOTIS Model



Circuit Capacitances

Cell Name	Node				
	A	Z[D]*	Z[H]*	Z[P]*	Z[T]*
BOC08	0.272 pF	3.713 pF	4.553 pF	3.359 pF	4.565 pF
BOC10	0.188 pF	3.346 pF	4.107 pF	2.992 pF	4.110 pF
BOC15	0.100 pF	2.807 pF	3.548 pF	2.453 pF	3.551 pF
BOC20	0.074 pF	2.860 pF	3.578 pF	2.506 pF	3.625 pF
BOC30	0.064 pF	2.258 pF	2.987 pF	1.904 pF	3.038 pF
BOC40	0.062 pF	2.333 pF	NC	1.979 pF	3.137 pF
BOC80	0.062 pF	2.170 pF	NC	1.816 pF	2.974 pF

* Pad capacitance varies with layout format.
NC - Cell not available in this layout format.

Circuit Performance

Cell Name	Delay [1] T_{PLL}		DC Current [2]
	Extrinsic	Intrinsic	Sink
BOC08D	0.252 ns/10pF	1.290 ns	24.2 mA
BOC08H	0.252 ns/10pF	1.325 ns	24.2 mA
BOC08P	0.252 ns/10pF	1.280 ns	24.2 mA
BOC08T	0.368 ns/10pF	1.287 ns	13.4 mA
BOC10D	0.434 ns/10pF	1.209 ns	12.1 mA
BOC10H	0.437 ns/10pF	1.253 ns	12.1 mA
BOC10P	0.434 ns/10pF	1.186 ns	12.1 mA
BOC10T	0.461 ns/10pF	1.244 ns	11.2 mA
BOC15D	0.548 ns/10pF	1.746 ns	10.1 mA
BOC15H	0.552 ns/10pF	1.813 ns	10.1 mA
BOC15P	0.549 ns/10pF	1.722 ns	10.1 mA
BOC15T	0.573 ns/10pF	1.784 ns	9.5 mA
BOC20D	0.719 ns/10pF	2.193 ns	8.1 mA
BOC20H	0.724 ns/10pF	2.258 ns	8.1 mA
BOC20P	0.720 ns/10pF	2.160 ns	8.1 mA
BOC20T	0.741 ns/10pF	2.238 ns	7.7 mA
BOC30D	1.608 ns/10pF	1.757 ns	4.1 mA
BOC30H	1.609 ns/10pF	1.972 ns	4.1 mA
BOC30P	1.608 ns/10pF	1.691 ns	4.1 mA
BOC30T	1.618 ns/10pF	1.889 ns	4.0 mA
BOC40D	3.082 ns/10pF	1.807 ns	2.2 mA
BOC40P	3.085 ns/10pF	1.654 ns	2.2 mA
BOC40T	3.105 ns/10pF	2.071 ns	2.1 mA
BOC80D	6.974 ns/10pF	2.363 ns	1.0 mA
BOC80P	6.974 ns/10pF	2.071 ns	1.0 mA
BOC80T	6.996 ns/10pF	2.974 ns	1.0 mA

1) Nominal Process, VDD=5.0V, T=25° C
2) Slow Process, VDD=4.5V, T=100° C

Layout Information

Cell Name	Transistors	Cell Dimensions	
		X	Y
BOC08D	18	280.125 µm	291.750 µm
BOC08H		175.000 µm	540.125 µm
BOC08P		272.250 µm	291.750 µm
BOC08T		175.000 µm	540.125 µm
BOC10D	12	253.125 µm	291.750 µm
BOC10H		175.000 µm	540.125 µm
BOC10P		245.250 µm	291.750 µm
BOC10T		175.000 µm	540.125 µm
BOC15D	10	244.125 µm	291.750 µm
BOC15H		175.000 µm	540.125 µm
BOC15P		236.250 µm	291.750 µm
BOC15T		175.000 µm	540.125 µm
BOC20D	8	235.125 µm	291.750 µm
BOC20H		175.000 µm	540.125 µm
BOC20P		227.250 µm	291.750 µm
BOC20T		175.000 µm	540.125 µm
BOC30D	6	226.125 µm	291.750 µm
BOC30H		175.000 µm	540.125 µm
BOC30P		218.250 µm	291.750 µm
BOC30T		175.000 µm	540.125 µm
BOC40D	4	217.125 µm	291.750 µm
BOC40P		209.250 µm	291.750 µm
BOC40T		175.000 µm	540.125 µm
BOC80D	4	217.125 µm	291.750 µm
BOC80P		209.250 µm	291.750 µm
BOC80T		175.000 µm	540.125 µm

Output Buffer

BON*od[D,H,P,T]*

FUNCTIONAL DESCRIPTION:

Non-Inverting TTL-Level Output Buffer

CELL NAME DEFINITIONS:

od = WCS Delay in ns @ 50pF load
[D,H,P,T] = Available Layout Formats

EXAMPLE: BON08D

INPUTS: A
OUTPUTS: Z

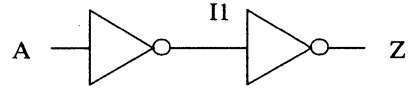
MOTIS Gate Count: 2

5

Truth Table

Input	Output
A	Z
0	0
1	1

MOTIS Model



Circuit Capacitances

Cell Name	Node				
	A	Z[D]*	Z[H]*	Z[P]*	Z[T]*
BON08	0.272 pF	3.718 pF	4.557 pF	3.364 pF	4.569 pF
BON10	0.188 pF	3.349 pF	4.111 pF	2.995 pF	4.114 pF
BON15	0.100 pF	2.809 pF	3.550 pF	2.455 pF	3.553 pF
BON20	0.074 pF	2.862 pF	3.580 pF	2.508 pF	3.627 pF
BON30	0.064 pF	2.259 pF	2.988 pF	1.905 pF	3.039 pF
BON40	0.062 pF	2.335 pF	NC	1.981 pF	3.138 pF
BON80	0.062 pF	2.172 pF	NC	1.818 pF	2.975 pF

* Pad capacitance varies with layout format.
NC - Cell not available in this layout format.

Circuit Performance

Cell Name	Delay [1]				DC Current [2]	
	T_{PHH}		T_{PLL}			
	Extrinsic	Intrinsic	Extrinsic	Intrinsic	Sink	Source
BON08D	0.278 ns/10pF	2.858 ns	0.266 ns/10pF	2.616 ns	24.2 mA	38.0 mA
BON08H	0.277 ns/10pF	2.888 ns	0.266 ns/10pF	2.645 ns	24.2 mA	38.0 mA
BON08P	0.278 ns/10pF	2.844 ns	0.266 ns/10pF	2.600 ns	24.2 mA	38.0 mA
BON08T	0.293 ns/10pF	2.936 ns	0.379 ns/10pF	2.616 ns	13.4 mA	33.0 mA
BON10D	0.458 ns/10pF	2.716 ns	0.449 ns/10pF	2.630 ns	12.1 mA	21.7 mA
BON10H	0.458 ns/10pF	2.748 ns	0.449 ns/10pF	2.669 ns	12.1 mA	21.7 mA
BON10P	0.458 ns/10pF	2.697 ns	0.449 ns/10pF	2.611 ns	12.1 mA	21.7 mA
BON10T	0.461 ns/10pF	2.758 ns	0.474 ns/10pF	2.661 ns	11.2 mA	21.3 mA
BON15D	0.585 ns/10pF	4.420 ns	0.587 ns/10pF	4.358 ns	10.1 mA	17.2 mA
BON15H	0.585 ns/10pF	4.480 ns	0.573 ns/10pF	4.480 ns	10.1 mA	17.2 mA
BON15P	0.585 ns/10pF	4.396 ns	0.574 ns/10pF	4.393 ns	10.1 mA	17.2 mA
BON15T	0.587 ns/10pF	4.477 ns	0.595 ns/10pF	4.462 ns	9.5 mA	17.0 mA
BON20D	0.764 ns/10pF	5.697 ns	0.748 ns/10pF	5.911 ns	8.1 mA	13.3 mA
BON20H	0.764 ns/10pF	5.779 ns	0.748 ns/10pF	5.976 ns	8.1 mA	13.3 mA
BON20P	0.764 ns/10pF	5.663 ns	0.748 ns/10pF	5.876 ns	8.1 mA	13.3 mA
BON20T	0.767 ns/10pF	5.771 ns	0.767 ns/10pF	5.953 ns	7.7 mA	13.2 mA
BON30D	1.845 ns/10pF	3.960 ns	1.608 ns/10pF	4.205 ns	4.1 mA	5.6 mA
BON30H	1.845 ns/10pF	4.189 ns	1.609 ns/10pF	4.412 ns	4.1 mA	5.6 mA
BON30P	1.845 ns/10pF	3.884 ns	1.609 ns/10pF	4.132 ns	4.1 mA	5.6 mA
BON30T	1.846 ns/10pF	4.119 ns	1.619 ns/10pF	4.330 ns	4.0 mA	5.6 mA
BON40D	3.114 ns/10pF	3.044 ns	3.084 ns/10pF	3.486 ns	2.2 mA	3.3 mA
BON40P	3.113 ns/10pF	2.920 ns	3.084 ns/10pF	3.349 ns	2.2 mA	3.3 mA
BON40T	3.114 ns/10pF	3.330 ns	3.106 ns/10pF	3.775 ns	2.1 mA	3.3 mA
BON80D	7.066 ns/10pF	2.570 ns	6.974 ns/10pF	3.181 ns	1.0 mA	1.5 mA
BON80P	7.051 ns/10pF	2.589 ns	6.974 ns/10pF	2.882 ns	1.0 mA	1.5 mA
BON80T	7.051 ns/10pF	3.496 ns	6.996 ns/10pF	3.779 ns	1.0 mA	1.5 mA

1) Nominal Process, VDD=5.0V, T=25° C
2) Slow Process, VDD=4.5V, T=100° C

Layout Information

Cell Name	Transistors	Cell Dimensions	
		X	Y
BON08D	18	280.125 µm	291.750 µm
BON08H		175.000 µm	540.125 µm
BON08P		272.250 µm	291.750 µm
BON08T		175.000 µm	540.125 µm
BON10D	12	253.125 µm	291.750 µm
BON10H		175.000 µm	540.125 µm
BON10P		245.250 µm	291.750 µm
BON10T		175.000 µm	540.125 µm
BON15D	10	244.125 µm	291.750 µm
BON15H		175.000 µm	540.125 µm
BON15P		236.250 µm	291.750 µm
BON15T		175.000 µm	540.125 µm
BON20D	8	235.125 µm	291.750 µm
BON20H		175.000 µm	540.125 µm
BON20P		227.250 µm	291.750 µm
BON20T		175.000 µm	540.125 µm
BON30D	6	226.125 µm	291.750 µm
BON30H		175.000 µm	540.125 µm
BON30P		218.250 µm	291.750 µm
BON30T		175.000 µm	540.125 µm
BON40D	4	217.125 µm	291.750 µm
BON40P		209.250 µm	291.750 µm
BON40T		175.000 µm	540.125 µm
BON80D	4	217.125 µm	291.750 µm
BON80P		209.250 µm	291.750 µm
BON80T		175.000 µm	540.125 µm

FUNCTIONAL DESCRIPTION:

Non-Inverting TTL-Level Tri-State Output Buffer

CELL NAME DEFINITIONS:

od = WCS delay in ns @ 50pF load
[D,H,P,T] = Available Layout Formats

EXAMPLE: BOT08D

5

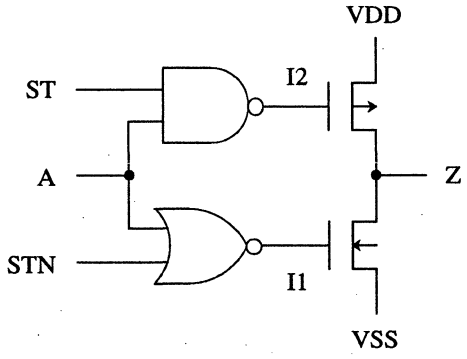
INPUTS: A, ST, STN
OUTPUTS: Z

MOTIS Gate Count: 3

Truth Table

Inputs			Output
A	ST	STN	Z
0	X	0	0
0	X	1	HI-Z
1	0	X	HI-Z
1	1	X	1

MOTIS Model



Circuit Capacitances

Cell Name	Node						
	A	ST	STN	Z[D]*	Z[H]*	Z[P]*	Z[T]*
BOT08	0.728 pF	0.408 pF	0.342 pF	3.719 pF	4.615 pF	3.365 pF	4.651 pF
BOT10	0.394 pF	0.226 pF	0.194 pF	3.351 pF	4.165 pF	2.997 pF	4.188 pF
BOT15	0.180 pF	0.110 pF	0.099 pF	2.809 pF	3.608 pF	2.455 pF	3.633 pF
BOT20	0.119 pF	0.077 pF	0.072 pF	2.864 pF	3.640 pF	2.510 pF	3.665 pF
BOT30	0.097 pF	0.064 pF	0.063 pF	2.258 pF	3.018 pF	1.904 pF	3.029 pF
BOT40	0.112 pF	0.071 pF	0.070 pF	2.333 pF	NC	1.979 pF	3.114 pF
BOT80	0.097 pF	0.064 pF	0.063 pF	2.170 pF	NC	1.816 pF	2.951 pF

* Pad capacitance varies with layout format.
NC - Cell not available in this layout format.

Circuit Performance

Cell Name	Delay [1]				Tri-State
	T_{PHH}		T_{PLL}		
	Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BOT08D	0.283 ns/10pF	2.616 ns	0.271 ns/10pF	2.607 ns	0.630 ns
BOT08H	0.283 ns/10pF	2.645 ns	0.271 ns/10pF	2.654 ns	
BOT08P	0.283 ns/10pF	2.600 ns	0.271 ns/10pF	2.597 ns	
BOT08T	0.297 ns/10pF	2.672 ns	0.384 ns/10pF	2.595 ns	
BOT10D	0.461 ns/10pF	2.603 ns	0.455 ns/10pF	2.670 ns	1.016 ns
BOT10H	0.461 ns/10pF	2.648 ns	0.455 ns/10pF	2.721 ns	
BOT10P	0.461 ns/10pF	2.584 ns	0.456 ns/10pF	2.645 ns	
BOT10T	0.464 ns/10pF	2.653 ns	0.480 ns/10pF	2.702 ns	
BOT15D	0.594 ns/10pF	4.408 ns	0.588 ns/10pF	4.394 ns	2.042 ns
BOT15H	0.594 ns/10pF	4.462 ns	0.587 ns/10pF	4.491 ns	
BOT15P	0.595 ns/10pF	4.378 ns	0.588 ns/10pF	4.364 ns	
BOT15T	0.597 ns/10pF	4.467 ns	0.609 ns/10pF	4.431 ns	
BOT20D	0.779 ns/10pF	5.956 ns	0.771 ns/10pF	6.086 ns	2.995 ns
BOT20H	0.779 ns/10pF	6.024 ns	0.771 ns/10pF	6.210 ns	
BOT20P	0.780 ns/10pF	5.916 ns	0.772 ns/10pF	6.040 ns	
BOT20T	0.781 ns/10pF	6.032 ns	0.789 ns/10pF	6.155 ns	
BOT30D	1.847 ns/10pF	4.389 ns	1.617 ns/10pF	5.433 ns	2.157 ns
BOT30H	1.847 ns/10pF	4.539 ns	1.617 ns/10pF	5.935 ns	
BOT30P	1.848 ns/10pF	4.307 ns	1.617 ns/10pF	5.361 ns	
BOT30T	1.848 ns/10pF	4.544 ns	1.624 ns/10pF	5.617 ns	
BOT40D	3.113 ns/10pF	2.532 ns	3.083 ns/10pF	3.028 ns	1.211 ns
BOT40P	3.112 ns/10pF	2.401 ns	3.082 ns/10pF	2.904 ns	
BOT40T	3.111 ns/10pF	2.815 ns	3.108 ns/10pF	3.260 ns	
BOT80D	7.051 ns/10pF	2.977 ns	6.976 ns/10pF	3.416 ns	0.858 ns
BOT80P	7.048 ns/10pF	2.694 ns	6.976 ns/10pF	3.123 ns	
BOT80T	7.052 ns/10pF	3.566 ns	6.996 ns/10pF	4.017 ns	

1) Nominal Process, VDD=5.0V, T=25° C

5

Circuit Performance

Cell Name	DC Current [1]	
	Sink	Source
BOT08D	24.2 mA	38.0 mA
BOT08H	24.2 mA	38.0 mA
BOT08P	24.2 mA	38.0 mA
BOT08T	13.4 mA	33.0 mA
BOT10D	12.1 mA	21.7 mA
BOT10H	12.1 mA	21.7 mA
BOT10P	12.1 mA	21.7 mA
BOT10T	11.2 mA	21.3 mA
BOT15D	10.1 mA	17.2 mA
BOT15H	10.1 mA	17.2 mA
BOT15P	10.1 mA	17.2 mA
BOT15T	9.5 mA	17.0 mA
BOT20D	8.1 mA	13.3 mA
BOT20H	8.1 mA	13.3 mA
BOT20P	8.1 mA	13.3 mA
BOT20T	7.7 mA	13.2 mA
BOT30D	4.1 mA	5.6 mA
BOT30H	4.1 mA	5.6 mA
BOT30P	4.1 mA	5.6 mA
BOT30T	4.0 mA	5.6 mA
BOT40D	2.2 mA	3.3 mA
BOT40P	2.2 mA	3.3 mA
BOT40T	2.1 mA	3.3 mA
BOT80D	1.0 mA	1.5 mA
BOT80P	1.0 mA	1.5 mA
BOT80T	1.0 mA	1.5 mA

Layout Information

Cell Name	Transistors	Cell Dimensions	
		X	Y
BOT08D	24	300.875 µm	291.750 µm
BOT08H		182.250 µm	540.125 µm
BOT08P		293.000 µm	291.750 µm
BOT08T		175.000 µm	540.125 µm
BOT10D	18	273.875 µm	291.750 µm
BOT10H		175.000 µm	540.125 µm
BOT10P		266.000 µm	291.750 µm
BOT10T		175.000 µm	540.125 µm
BOT15D	16	264.875 µm	291.750 µm
BOT15H		175.000 µm	540.125 µm
BOT15P		257.000 µm	291.750 µm
BOT15T		175.000 µm	540.125 µm
BOT20D	14	255.875 µm	291.750 µm
BOT20H		175.000 µm	540.125 µm
BOT20P		248.000 µm	291.750 µm
BOT20T		175.000 µm	540.125 µm
BOT30D	12	246.875 µm	291.750 µm
BOT30H		175.000 µm	540.125 µm
BOT30P		239.000 µm	291.750 µm
BOT30T		175.000 µm	540.125 µm
BOT40D	10	237.875 µm	291.750 µm
BOT40P		230.000 µm	291.750 µm
BOT40T		175.000 µm	540.125 µm
BOT80D	10	237.875 µm	291.750 µm
BOT80P		230.000 µm	291.750 µm
BOT80T		175.000 µm	540.125 µm

1) Slow Process, VDD=4.5V, T=100° C

Output Buffer

BOX*od[D,H,P,T]*

FUNCTIONAL DESCRIPTION:

Driver Transistors Only (No Inherent Logic) Output Buffer

CELL NAME DEFINITIONS:

od = WCS Delay in ns @ 50pF load

[D,H,P,T] = Available Layout Formats

EXAMPLE: BOX08D

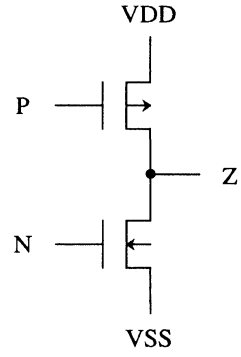
INPUTS: N, P
OUTPUTS: Z

MOTIS Gate Count: 1

Truth Table

Inputs		Outputs
N	P	Z
0	0	1
0	1	HI-Z
1	1	0

MOTIS Model



Circuit Capacitances

Cell Name	Node					
	N	P	Z[D]*	Z[H]*	Z[P]*	Z[T]*
BOX08	1.718 pF	2.820 pF	3.718 pF	4.543 pF	3.364 pF	4.549 pF
BOX10	1.154 pF	1.683 pF	3.349 pF	4.098 pF	2.995 pF	4.096 pF
BOX15	0.861 pF	1.312 pF	2.809 pF	3.536 pF	2.455 pF	3.559 pF
BOX20	0.631 pF	0.996 pF	2.862 pF	3.586 pF	2.508 pF	3.633 pF
BOX30	0.288 pF	0.420 pF	2.259 pF	2.994 pF	1.905 pF	3.045 pF
BOX40	0.165 pF	0.246 pF	2.335 pF	NC	1.981 pF	3.145 pF
BOX80	0.095 pF	0.125 pF	2.172 pF	NC	1.818 pF	2.982 pF

* Pad capacitance varies with layout format.
NC - Cell not available in this layout format.

Circuit Performance

Cell Name	Delay [1]				DC Current [2]	
	T_{PHL}		T_{PLH}			
	Extrinsic	Intrinsic	Extrinsic	Intrinsic	Sink	Source
BOX08D	0.289 ns/10pF	1.746 ns	0.279 ns/10pF	1.950 ns	24.2 mA	38.0 mA
BOX08H	0.288 ns/10pF	1.783 ns	0.279 ns/10pF	1.978 ns	24.2 mA	38.0 mA
BOX08P	0.289 ns/10pF	1.730 ns	0.311 ns/10pF	1.298 ns	24.2 mA	38.0 mA
BOX08T	0.385 ns/10pF	1.767 ns	0.295 ns/10pF	2.024 ns	13.4 mA	33.0 mA
BOX10D	0.442 ns/10pF	1.431 ns	0.458 ns/10pF	1.233 ns	12.1 mA	21.7 mA
BOX10H	0.441 ns/10pF	1.479 ns	0.457 ns/10pF	1.272 ns	12.1 mA	21.7 mA
BOX10P	0.442 ns/10pF	1.404 ns	0.458 ns/10pF	1.213 ns	12.1 mA	21.7 mA
BOX10T	0.463 ns/10pF	1.473 ns	0.461 ns/10pF	1.275 ns	11.2 mA	21.3 mA
BOX15D	0.559 ns/10pF	1.274 ns	0.583 ns/10pF	0.961 ns	10.1 mA	17.2 mA
BOX15H	0.559 ns/10pF	1.325 ns	0.583 ns/10pF	1.008 ns	10.1 mA	17.2 mA
BOX15P	0.559 ns/10pF	1.250 ns	0.583 ns/10pF	0.937 ns	10.1 mA	17.2 mA
BOX15T	0.580 ns/10pF	1.320 ns	0.585 ns/10pF	1.015 ns	9.5 mA	17.0 mA
BOX20D	0.723 ns/10pF	1.190 ns	0.763 ns/10pF	0.809 ns	8.1 mA	13.3 mA
BOX20H	0.722 ns/10pF	1.256 ns	0.766 ns/10pF	0.856 ns	8.1 mA	13.3 mA
BOX20P	0.723 ns/10pF	1.155 ns	0.763 ns/10pF	0.776 ns	8.1 mA	13.3 mA
BOX20T	0.740 ns/10pF	1.267 ns	0.765 ns/10pF	0.881 ns	7.7 mA	13.2 mA
BOX30D	1.415 ns/10pF	1.878 ns	1.848 ns/10pF	0.768 ns	4.1 mA	5.6 mA
BOX30H	1.412 ns/10pF	2.040 ns	1.849 ns/10pF	0.910 ns	4.1 mA	5.6 mA
BOX30P	1.417 ns/10pF	1.797 ns	1.848 ns/10pF	0.692 ns	4.1 mA	5.6 mA
BOX30T	1.420 ns/10pF	2.047 ns	1.850 ns/10pF	0.919 ns	4.0 mA	5.6 mA
BOX40D	2.520 ns/10pF	3.989 ns	3.140 ns/10pF	1.031 ns	2.2 mA	3.3 mA
BOX40P	2.525 ns/10pF	3.839 ns	3.139 ns/10pF	0.906 ns	2.2 mA	3.3 mA
BOX40T	2.528 ns/10pF	4.348 ns	3.140 ns/10pF	1.317 ns	2.1 mA	3.3 mA
BOX80D	6.844 ns/10pF	2.615 ns	7.050 ns/10pF	1.886 ns	1.0 mA	1.5 mA
BOX80P	6.849 ns/10pF	2.293 ns	7.051 ns/10pF	1.587 ns	1.0 mA	1.5 mA
BOX80T	6.861 ns/10pF	3.244 ns	7.051 ns/10pF	2.500 ns	1.0 mA	1.5 mA

1) Nominal Process, VDD=5.0V, T=25° C
2) Slow Process, VDD=4.5V, T=100° C

Layout Information

Cell Name	Transistors	Cell Dimensions	
		X	Y
BOX08D	16	275.125 µm	291.750 µm
BOX08H		175.000 µm	540.125 µm
BOX08P		267.250 µm	291.750 µm
BOX08T		175.000 µm	540.125 µm
BOX10D	10	248.125 µm	291.750 µm
BOX10H		175.000 µm	540.125 µm
BOX10P		240.250 µm	291.750 µm
BOX10T		175.000 µm	540.125 µm
BOX15D	8	239.125 µm	291.750 µm
BOX15H		175.000 µm	540.125 µm
BOX15P		231.250 µm	291.750 µm
BOX15T		175.000 µm	540.125 µm
BOX20D	6	230.125 µm	291.750 µm
BOX20H		175.000 µm	540.125 µm
BOX20P		222.250 µm	291.750 µm
BOX20T		175.000 µm	540.125 µm
BOX30D	4	221.125 µm	291.750 µm
BOX30H		175.000 µm	540.125 µm
BOX30P		213.250 µm	291.750 µm
BOX30T		175.000 µm	540.125 µm
BOX40D	2	212.125 µm	291.750 µm
BOX40P		204.250 µm	291.750 µm
BOX40T		175.000 µm	540.125 µm
BOX80D	2	212.125 µm	291.750 µm
BOX80P		204.250 µm	291.750 µm
BOX80T		175.000 µm	540.125 µm

Logic Cells

Section 6

AT&T

Contents - Section 6

Introduction

Logic Cell Information

This section contains data sheets that provide details about the logic cells in the 1.25µ CMOS Catalog. What follows here is some background information about the logic cell family that should help in guiding you through the wide selection of cells available.

Some of the salient features of the logic cell family are noted as follows:

- There are 197 cells described in this section, broken down by function as follows:

Cell Type	# of Cells	Page Number
AND*n* gates	9	6-10
And-Or-Invert gates (AOI*abcd*)	70	6-11 to 6-14
Built in Self Test Logic (BIST1)	1	6-15
Full Adder (FA)	1	6-16
Inverters (INRB*n*)	5	6-17
Nand gates (ND*n*)	9	6-18
Nor gates (NR*n*)	9	6-19
Or-And-Invert gates (OAI*abcd*)	67	6-20 to 6-23
OR*n* gates	9	6-24
Select Data (SD*abc*)	4	6-25 to 6-28
Tristate bus drivers (TBDI)	2	6-29
Tristate bus drivers (TBUS*i*)	4	6-30 to 6-31
Transmission gates (TG*n*)	3	6-32
XNOR and XOR gates	4	6-33 to 6-34

A complete description of the cell naming convention is provided on the following pages.

- A complete set of And-Or-Invert and Or-And-Invert gates are available. The library has been designed with a complete set of cells to get the maximum efficiency out of logic synthesis tools (see, for example, the description of the FDS functions available in Section 11.) If you are capturing your schematic manually, having a complete set of cells available also means that you will not need to have any cells with unused inputs (that would otherwise require connection to one of the power supplies.) This saves silicon area and improves circuit performance.
- Both area-optimized and performance optimized versions of each cell are available. Thus, if your performance requirements do not tax the limits of the technology, you will be able to save area by using the area-optimized library. (See, for example, guidelines to the calculation of chip area in Section 2.)
- Many of the simpler cells are provided with a number of drive capabilities. For example, in this section you will find a ND2, ND2H, and ND2S. These names refer to 2-input Nand gates with 1X, 2X and 4X drive capability, respectively.

AND*n* The AND cell provides the logical AND of two or more inputs as specified by the parameter ***n***.

Example: AND3 would be a cell whose output is the logical AND of all three of its inputs.

AOI***abcd*** These cells provide the inverted OR of two to four AND groups. The parameters ***a, b, c***, and ***d*** specify how many inputs make up each AND group. These parameters are always specified in descending order and parameters ***c*** and ***d*** are omitted when their values are zero.

Example: AOI422 would be a cell whose output is the inversion of (A1 and A2 and A3 and A4) or (B1 and B2) or (C1 and C2).

BIST1 This cell provides the logic function required for Built in Self Test applications. This function is already present in the BIST Flip-Flops FB1S2AX AND FB1S3AX. The BIST1 cell can be used in conjunction with any other Flip-Flop to create additional BIST compatible Flip-Flops.

FA This cell is a two bit adder with carry in and carry out in addition to the sum output. FA cells can be combined to make arbitrary length adders.

INRB*n* The INRB cells provide the logical inversion of the input signal. This cell can also be used as an inverting buffer and for this purpose many high power varieties exist. The parameter ***n*** will define the power of the cell in multiples of a standard INRB. It is worthwhile to note that the suffix H implies twice the standard INRB while the S suffix implies a fourfold ratio.

Example: INRB12 would be an inverter that is twelve times the power of a standard INRB.

ND*n* The ND cell provides the inversion of the logical AND of two or more inputs as specified by the parameter ***n***.

Example: ND3 would be a cell whose output is the logical NAND of all three of its inputs.

NR*n* The NR cell provides the inversion of the logical OR of two or more inputs as specified by the parameter ***n***.

Example: NR3 would be a cell whose output is the logical NOR of all three of its inputs.

OAI***abcd*** These cells provide the inverted AND of two to four OR groups. The parameters ***a, b, c***, and ***d*** specify how many inputs make up each OR group. These parameters are always specified in descending order and parameters ***c*** and ***d*** are omitted when their values are zero.

Example: OAI422 would be a cell whose output is the inversion of (A1 or A2 or A3 or A4) and (B1 or B2) and (C1 or C2).

ONE The ONE cell is a direct connection to the VDD power supply. The output signal can be used as a logical ONE in other areas of the circuit.

OR*n* The OR cell provides the logical OR of two or more inputs as specified by the parameter ***n***.

Example: OR3 would be a cell whose output is the logical OR of all three of its inputs.

SD*abc* The SD (Select Data) cells have been generated to standardize cells which simply select one of a number of inputs to the output. The inputs themselves may be groups of bits rather than single bits, and in this case, the output would be the selected group of bits. It is also advantageous to allow some of these groups to be inverted when they are selected. The type of cell supplied in the library assigns each group of bits an address, and these inputs are then chosen by applying the address value to the select lines. The naming convention for Select Data cells is as follows:

SD*abc* *a*= Number of addresses.
b= Number of bits per address.
c= Value indicating which addresses are inverted.

Values greater than 9 are not permitted for *a* and *b*.

The value of *c* is calculated by forming a binary number with each bit representing the polarity of an address. The lowest order bit represents the zero address, and a bit value of 1 indicates an inverted address. The choice of 1 to indicate an inversion has the benefit of a zero value for *c* for all non-inverting selectors.

Example: SD212 is the name of a cell which selects one of two data addresses which are one bit wide with address one inverted.

SD212 *a=2* There are two addresses - 0 and 1
b=1 There is one bit per address.
c=2 The decimal value of 10 (address 1 inverted).

TBDI The TBDI cells are tri-statable inverters. These cells are meant for use in internal bus structures.

TBUS*i* The TBUS cells are tri-statable buffers. The presence of the parameter *i* indicates that the cell is an inverting buffer. These cells are meant for use in internal bus structures.

TG*n* The TG cells contain one or more transmission gates whose outputs are connected to form a common bus output. The parameter *n* defines the exact number of transmission gates present in the cell. Transmission gates that are used consist of both an N and a P type transistor.

Example: TG2 contains two transmission gates whose outputs form a common bus.

XNOR The XNOR cell performs the logical EXCLUSIVE NOR function. Additionally, since this function requires two gates to generate an XNOR function the NAND of the two inputs is also provided as an output.

XOR The XOR cell performs the logical EXCLUSIVE OR function. Additionally, since this function requires two gates to generate an XOR function the NOR of the two inputs is also provided as an output.

ZERO The ZERO cell is a direct connection to the VSS power supply. The output signal can be used as a logical ZERO in other areas of the circuit.

Cell Drive Capability

The 1.25µ CMOS Library contains variations of the same function that differ only in drive capability. These higher power versions are commonly denoted by a suffix of H or S. The high power or H version has double the drive of the normal version where S indicates a factor of four. All of the conventions described allow for the possibility of a higher power version.

If you were to turn to page 6-17, which is the data sheet for the INRB family, you would find this table of capacitances:

Capacitances - INRB*n*

	INRB	INRBH	INRBS	INRB8	INRB12
Area	0.034pF	0.067pF	0.133pF	0.265pF	0.397pF
Perf.	0.145pF	0.292pF	0.584pF	1.169pF	1.753pF

These are the input capacitances for the INRB family from both the area optimized and performance optimized libraries. The capacitances have been tabulated in terms of picofarads and since there are two libraries of cells (area-optimized and performance-optimized), a different input capacitance is supplied for each.

The capacitive load, 0.034pF, is the input capacitance of an area-optimized version of the INRB (a 1X inverter gate.) This capacitance is comprised of a 1X P-transistor, a 1X N-transistor and some internal cell routing. Similarly, the capacitive load, which equals 0.145pF, is the input capacitance of a performance-optimized version of the INRB.

Knowing these two values, it becomes easy to compare the input capacitances of different gates to one another. For example, if we look at the capacitance table for the AOI***abcd*** family, we see:

Capacitances - AOI*abcd*

	Normal Power	High Power	Super Power
Area	0.034pF	0.069pF	0.138pF
Perf.	0.145pF	0.294pF	0.588pF

It is now easy to see the input capacitance for all high power AOI***abcd*** gates is approximately twice that of an INRB. The numbers do not, in this case, work out to exact integer ratios because of internal cell routing. Similarly, the input capacitances for super power gates is approximately four times that of a standard INRB

When calculating delays, remember to include estimated routing capacitance. A value of 0.12pF per fanout is the autoroute factor suggested for simulation.

An example of a delay calculation using these input capacitances is provided in the section that follows.

If we turn to the SD210 as an example, it can be seen that the following delay information has been tabulated on page 6-25:

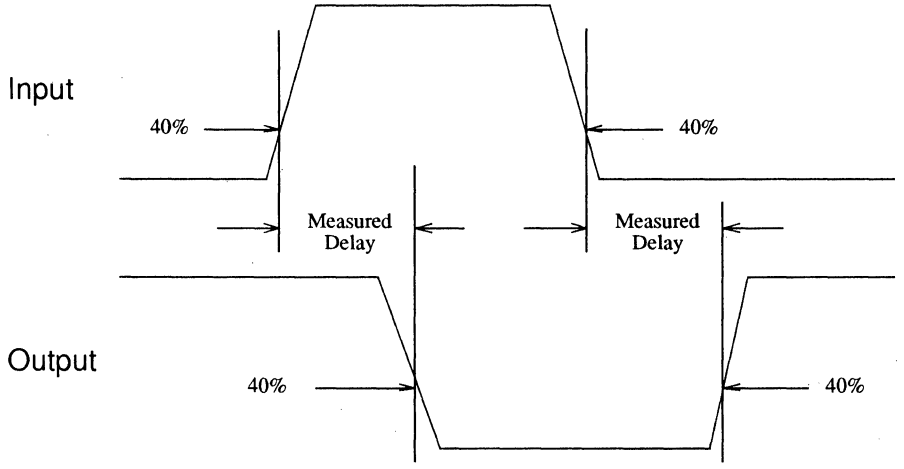
Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	Z ↓	2.10ns/pF	1.42ns	0.50ns/pF	0.80ns
D0 ↑	Z ↑	3.66ns/pF	1.23ns	0.68ns/pF	0.70ns
D1 ↓	Z ↓	2.10ns/pF	1.42ns	0.50ns/pF	0.80ns
D1 ↑	Z ↑	3.66ns/pF	1.23ns	0.68ns/pF	0.70ns
SD ↓	Z ↓	2.10ns/pF	1.42ns	0.50ns/pF	0.80ns
SD ↓	Z ↑	3.66ns/pF	1.09ns	0.70ns/pF	0.73ns
SD ↑	Z ↓	2.10ns/pF	2.09ns	0.50ns/pF	1.09ns
SD ↑	Z ↑	3.66ns/pF	1.23ns	0.68ns/pF	0.70ns

VDD=5V, T=25°C, Nominal Process.

A similar set of delay information is provided for all 197 logic cells in this section. These tables contain linear equations used to approximate the cell delay characteristics.

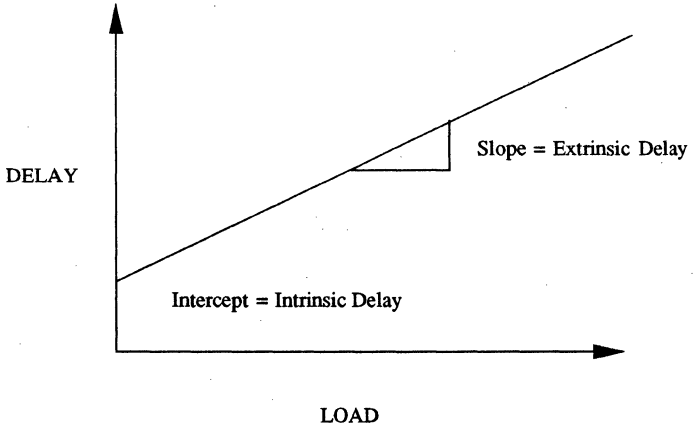
A voltage level of 40% of VDD was used to define where the delays were measured as illustrated in the diagram below.. This value was chosen as it is very close to the INRB unity-gain point (in the nominal process) for both the area-optimized and performance optimized libraries.



The terms and symbols used in the Delay Information tables are defined as follows:

The first two columns indicate the input and output signal names and also indicate rising or falling transitions. The first entry in the SD210 Delay Information table, D0 ↓ to Z ↑, indicates that the propagation delay values approximate the path delay from the D0 input falling to the Z output rising.

An *intrinsic* and *extrinsic* delay value is provided in the Delay Information Table. These two values are terms for a linear equation used to approximate the cell delay characteristics. In graphical terms, they have the following meaning:



Thus, the delay characteristics for the path D0 ↓ to Z ↑ of an area-optimized SD210 can be written as the sum of the intrinsic delay and the extrinsic delay, as follows:

Delay = 1.42ns + (2.10ns/pF) times Total Load in picofarads

In physical terms, the *intrinsic delay* represents the *zero-load* delay of the cell. The *extrinsic delay* is related to the cell's output impedance, and is a measure of how the delay will vary with increasing load. As all of the cells in the library have purely capacitive inputs, DC loading on the outputs is not a concern (some notable exceptions, of course, are output buffers which may interface with TTL.) Thus, given enough time, a CMOS logic gate will always reach a valid logic level regardless of the number of gates being driven. However, that time will increase as the load on the output increases.

It is worthwhile to point out how the delay information was derived. The delay information was obtained by simulating each cell with AT&T's MOTIS3 Multiple-Delay simulator under Worst-Case-Slow conditions (4.5V, 100°C, and Slow Process Conditions). Subsequently, each delay value was derated by a factor of 0.477, which was obtained from the derating tables presented in Section 2, to convert the numbers to Nominal conditions (5.0V, 25°C, and Nominal Process Conditions). This allows Nominal delays to be used in the catalog while providing the most accurate predictions for worst case behavior.

The required derating factor was calculated as follows:

Nominal Delay*1.31 (Slow Process Conditions)*1.60 (4.5V and 100°C) = Worst Case Slow Delay

Therefore,

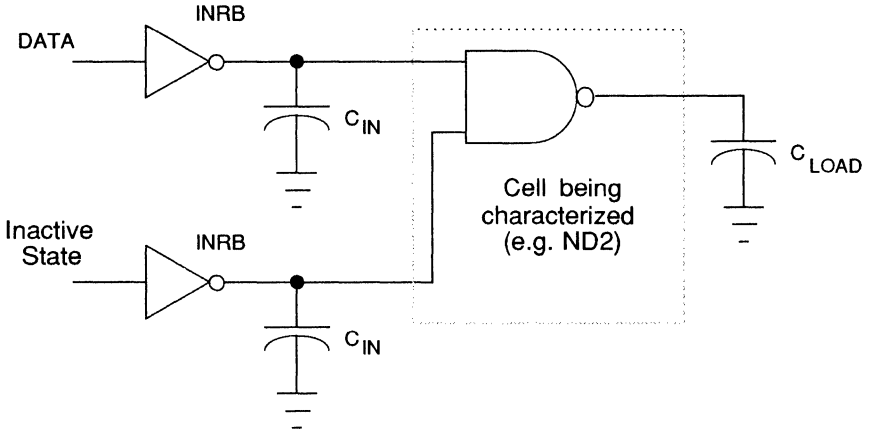
Nominal delay = 0.477 Worst Case Slow Delay

Process Conditions	Derating Factor
Slow	1.31
Nominal	1.0
Fast	0.75

Power Supply and Temperature Derating

		POWER SUPPLY VOLTAGE (VDD)				
		4.50V	4.75V	5.00V	5.25V	5.50V
TEMPERATURE	-40°	0.77	0.73	0.68	0.64	0.61
	0°	1.00	0.93	0.87	0.82	0.78
	25°	1.14	1.07	1.00	0.94	0.90
	85°	1.50	1.40	1.33	1.26	1.20
	100°	1.60	1.49	1.41	1.34	1.28
	125°	1.76	1.65	1.56	1.47	1.41

The following circuit was used for all delay simulations.



6

Notice that in addition to a load being applied to the output of the cell being characterized, a capacitive load equal to a 3 fan-outs was connected to the cell's *input*. A value of 3 fanouts was chosen as this has been found to be quite typical in many designs. Estimated routing capacitance equal to 0.12pF per fanout has been included, both on the outputs and the inputs.

(Of course, one can only use estimated capacitances before layout: early in the circuit design phase, exact layout capacitances are not available. The factor of 0.12pF/autorout is a conservative one - on a typical 1.25µ CMOS design, 90% of all signals will have less than 0.12pF/fanout.)

The inputs of the cells were loaded for delay characterization because it has been found that the slope of the waveform on the input of a gate has a very noticeable effect on its propagation delay. Had this effect been neglected, the delay information provided would have been optimistic by about 10%.

To obtain the cell delay equations, two MOTIS3 simulations were performed for each cell. One simulation was performed with a CLOAD equivalent to a fan-out of 3, and another simulation was performed with CLOAD equivalent to a fan-out of 10. In both cases, the input of the cell was loaded with a capacitance equivalent to a fan-out of three, including estimated routing capacitance. These capacitances work out as follows:

$$C_{LOAD} = 3 \times (0.0335 \text{ pF/gate} + 0.12 \text{ pF/autorout}) = 0.46\text{pF (Fan-out = 3)}$$

$$C_{LOAD} = 10 \times (0.0335 \text{ pF/gate} + 0.12 \text{ pF/autorout}) = 1.53\text{pF (Fan-out = 10)}$$

for the area-optimized library, and:

$$3 \times (0.142 \text{ pF/gate} + 0.12\text{pF/autorout}) = 0.79\text{pF (Fan-out = 3)}$$

$$10 \times (0.142 \text{ pF/gate} + 0.12\text{pF/autorout}) = 2.62\text{pF (Fan-out = 10)}$$

for the performance-optimized library.

The delay values obtained from these simulations were derated by 0.477 (see above) and then used to obtain a line intercept (intrinsic delay) and slope (extrinsic delay.)

By now, it has probably become apparent how the delay information provided in this catalog was obtained, and how it can be used to an advantage. The delay information was calculated with the intent of allowing one to use it to do a circuit design on paper, and then go on with confidence to

MOTIS3 multiple delay simulation knowing that there will be few surprises. Most designers like to avoid surprises as they can often result in design delays.

On the other hand, if you need to squeeze every nanosecond out of the technology, the delay information provided here will only get you started. For the highest degree of simulation accuracy, real layout capacitances should included, and either MOTIS3 gate-level timing simulation or ADVICE device-level simulation should be used (with ADVICE being the most accurate, and CPU hungry.)

Calculating Gate Delays - An Example

A ND2 drives three loads. Consider the following problems:

1) *What are the gate delays under nominal conditions for the performance-optimized version of the cell?*
2) *For the area-optimized version?*
3) *What happens if T=100° C, VDD=4.5V and worst-case slow wafer processing are assumed?*

To solve this problem, we need to look at the Delay Information Table for the ND2:

Delay Information - ND2

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
ND2	3	4	Z↓	4.19ns/pF	1.32ns	0.89ns/pF	0.44ns
			Z↑	3.79ns/pF	0.45ns	0.70ns/pF	0.21ns

VDD = 5V, T = 25° C, Nominal Process.

NOTE: When calculating delays, remember to include estimated routing capacitance. A value of 0.12pF per fanout is the autorout factor suggested for simulation.

Solutions:

As we noted before, it's easiest to take the intrinsic and extrinsic delays, and write the delay characteristics out as an equation. For the performance-optimized ND2, we have

Z↓ delay = 0.44ns + (0.89ns/pF) * Total Load in picofarads

And:

Z↑ delay = 0.21ns + (0.70ns/pF) * Total Load in picofarads

For a fanout of three, the total capacitive load works out to:

3* (0.145pF/INRB gate capacitance) + 3 * (0.12pF/fanout capacitance) = 0.795pF

Putting this back into our equations for Z↓ delay and Z↑ delay:

Z↓ delay = 0.44ns + (0.89ns/pF) * 0.795pF = 1.15ns

And:

Z↑ delay = 0.21ns + (0.70ns/pF) * 0.795pF = 0.77ns

To solve the problem for the area-optimized library, we must re-calculate the capacitive load:

3 * (0.034pF/INRB gate capacitance) + 3 * (0.12pF/fanout capacitance) = 0.462pF

Putting this value into the characteristic delay equations for the area-optimized ND2, we get:

Z↓ delay = 1.32ns + (4.19ns/pF) * 0.462pF = 3.26ns

And:

Z↑ delay = 0.45ns + (3.79ns/pF) * 0.462pF = 2.20ns

3. The next part of the problem is to derate these numbers from nominal conditions to the more severe conditions stated in Part 3 of the problem, namely T=100 ° C, VDD=5V and worst-case slow processing. To do this, we need the derating factors that were presented in Section 2:

Process Conditions	Derating Factor
Slow	1.31
Nominal	1.0
Fast	0.75

Power Supply and Temperature Derating

		POWER SUPPLY VOLTAGE (VDD) 4.50V	4.75V	5.00V	5.25V	5.50V
TEMPERATURE	-40°	0.77	0.73	0.68	0.64	0.61
	0°	1.00	0.93	0.87	0.82	0.78
	25°	1.14	1.07	1.00	0.94	0.90
	85°	1.50	1.40	1.33	1.26	1.20
	100°	1.60	1.49	1.41	1.34	1.28
	125°	1.76	1.65	1.56	1.47	1.41

The derating factor we need can be seen to be:

D = 1.31 (Slow Process) * 1.60 (VDD=4.5V, T=100 ° C) = 2.10

Accordingly, the gate delays for the performance-optimized ND2 become:

Z ↓ delay = 1.15ns * 2.10 = 2.42ns (T=100 ° C, VDD=4.5V, Slow Process)

And:

Z ↑ delay = 0.77ns * 2.10 = 1.62ns (T=100 ° C, VDD=4.5V, Slow Process)

Similarly, for the area-optimized version of the ND2:

Z ↓ delay = 3.26ns * 2.10 = 7.60ns (T=100 ° C, VDD=4.5V, Slow Process)

And:

Z ↑ delay = 2.20ns * 2.10 = 4.62ns (T=100 ° C, VDD=4.5V, Slow Process)

The AND cells provide a logical AND of two to four inputs as specified by the parameter *n*.

High power and super power AND cells are available. A suffix of *H* indicates high power (2x) where an *S* suffix denotes super power (4x).

Example: AND3

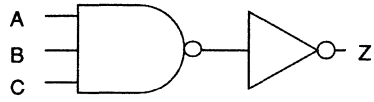
Inputs
A,B,C

Outputs
Z

Logic Equation

Z = (A*B*C)

Motis Model



Capacitances

The input terminal capacitance for all AND cells is provided in the following table and is identical for all AND cells and all higher power versions.

	Terminal Capacitance
Area	0.034pF
Perf.	0.145pF

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
AND2	4	6	Z↓	1.96ns/pF	0.77ns	0.47ns/pF	0.44ns
			Z↑	3.66ns/pF	1.09ns	0.68ns/pF	0.56ns
AND2H	6	8	Z↓	1.07ns/pF	0.94ns	0.23ns/pF	0.63ns
			Z↑	1.83ns/pF	1.40ns	0.36ns/pF	0.76ns
AND2S	8	12	Z↓	0.71ns/pF	1.25ns	0.18ns/pF	0.81ns
			Z↑	0.94ns/pF	1.86ns	0.23ns/pF	1.05ns
AND3	5	8	Z↓	2.05ns/pF	0.82ns	0.50ns/pF	0.47ns
			Z↑	3.66ns/pF	1.42ns	0.68ns/pF	0.85ns
AND3H	7	10	Z↓	1.07ns/pF	1.08ns	0.26ns/pF	0.65ns
			Z↑	1.83ns/pF	1.78ns	0.36ns/pF	1.05ns
AND3S	9	14	Z↓	0.71ns/pF	1.34ns	0.18ns/pF	0.86ns
			Z↑	1.03ns/pF	2.25ns	0.23ns/pF	1.44ns
AND4	6	10	Z↓	1.96ns/pF	0.96ns	0.47ns/pF	0.54ns
			Z↑	3.66ns/pF	1.71ns	0.70ns/pF	0.97ns
AND4H	8	12	Z↓	1.07ns/pF	1.13ns	0.26ns/pF	0.65ns
			Z↑	1.87ns/pF	2.10ns	0.39ns/pF	1.22ns
AND4S	10	16	Z↓	0.67ns/pF	1.41ns	0.18ns/pF	0.86ns
			Z↑	1.03ns/pF	2.68ns	0.26ns/pF	1.70ns

VDD=5V, T=25°C, Nominal Process.

And-Or-Invert — AOI*abcd*

These cells provide the inverted OR of two to four AND groups. The parameters *a, b, c,* and *d* specify how many inputs make up each AND group. These parameters are always specified in descending order and parameters *c* and *d* are omitted when their values are zero.

A small amount of higher power AOI cells are available. A suffix of *H* indicates high power (2x) where an *S* suffix denotes super power (4x).

Example: AOI221

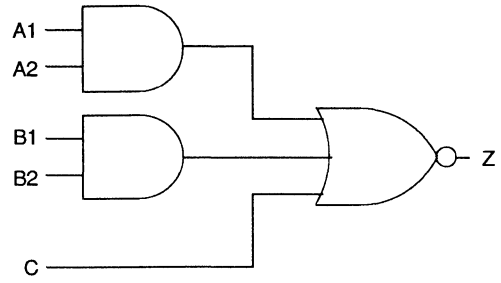
Inputs
A1,A2,B1,B2,C

Outputs
Z

Logic Equation

$$Z = \overline{(A1 \cdot A2)+(B1 \cdot B2)+C}$$

Motis Model



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Capacitances

The input terminal capacitance for all AOI cells is provided in the following table and is a function of the power of the cell.

	Normal Power	High Power	Super Power
Area	0.034pF	0.069pF	0.138pF
Perf.	0.145pF	0.294pF	0.588pF

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
AOI21	4	6	Z↓	4.19ns/pF	1.36ns	0.91ns/pF	0.47ns
			Z↑	6.73ns/pF	0.53ns	1.25ns/pF	0.25ns
AOI21H	7	12	Z↓	2.27ns/pF	1.10ns	0.50ns/pF	0.37ns
			Z↑	3.39ns/pF	0.44ns	0.63ns/pF	0.22ns
AOI211	5	8	Z↓	4.32ns/pF	1.45ns	0.94ns/pF	0.55ns
			Z↑	9.45ns/pF	0.66ns	1.72ns/pF	0.41ns
AOI2111	6	10	Z↓	4.41ns/pF	1.50ns	0.99ns/pF	0.51ns
			Z↑	11.90ns/pF	0.82ns	2.19ns/pF	0.46ns
AOI22	5	8	Z↓	4.19ns/pF	1.41ns	0.91ns/pF	0.47ns
			Z↑	6.73ns/pF	0.58ns	1.25ns/pF	0.25ns
AOI22H	9	16	Z↓	2.32ns/pF	1.13ns	0.47ns/pF	0.44ns
			Z↑	3.39ns/pF	0.54ns	0.63ns/pF	0.27ns

VDD=5V, T=25°C, Nominal Process.

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
AOI22S	17	32	Z ↓	1.29ns/pF	0.98ns	0.26ns/pF	0.37ns
			Z ↑	1.69ns/pF	0.51ns	0.31ns/pF	0.23ns
AOI221	7	10	Z ↓	4.32ns/pF	1.49ns	0.94ns/pF	0.59ns
			Z ↑	9.45ns/pF	0.80ns	1.75ns/pF	0.43ns
AOI2211	7	12	Z ↓	4.41ns/pF	1.60ns	0.99ns/pF	0.55ns
			Z ↑	11.95ns/pF	0.99ns	2.19ns/pF	0.56ns
AOI2211H	15	24	Z ↓	2.36ns/pF	1.35ns	0.52ns/pF	0.49ns
			Z ↑	5.93ns/pF	0.95ns	1.09ns/pF	0.52ns
AOI222	8	12	Z ↓	4.28ns/pF	1.61ns	0.96ns/pF	0.57ns
			Z ↑	9.45ns/pF	0.90ns	1.75ns/pF	0.48ns
AOI2221	9	14	Z ↓	4.41ns/pF	1.64ns	0.96ns/pF	0.67ns
			Z ↑	11.95ns/pF	1.13ns	2.22ns/pF	0.63ns
AOI2222	10	16	Z ↓	4.41ns/pF	1.69ns	0.96ns/pF	0.67ns
			Z ↑	11.90ns/pF	1.25ns	2.19ns/pF	0.70ns
AOI2222H	18	32	Z ↓	2.41ns/pF	1.42ns	0.50ns/pF	0.61ns
			Z ↑	5.93ns/pF	1.18ns	1.09ns/pF	0.66ns
AOI31	5	8	Z ↓	5.84ns/pF	1.42ns	1.30ns/pF	0.50ns
			Z ↑	6.91ns/pF	0.54ns	1.28ns/pF	0.28ns
AOI311	6	10	Z ↓	6.06ns/pF	1.50ns	1.36ns/pF	0.55ns
			Z ↑	9.63ns/pF	0.77ns	1.80ns/pF	0.39ns
AOI3111	7	12	Z ↓	6.20ns/pF	1.59ns	1.38ns/pF	0.63ns
			Z ↑	12.13ns/pF	0.86ns	2.24ns/pF	0.52ns
AOI32	6	10	Z ↓	5.88ns/pF	1.44ns	1.30ns/pF	0.54ns
			Z ↑	6.87ns/pF	0.66ns	1.28ns/pF	0.33ns
AOI321	7	12	Z ↓	6.06ns/pF	1.55ns	1.36ns/pF	0.60ns
			Z ↑	9.63ns/pF	0.87ns	1.80ns/pF	0.44ns
AOI3211	8	14	Z ↓	6.24ns/pF	1.61ns	1.38ns/pF	0.67ns
			Z ↑	12.13ns/pF	1.00ns	2.24ns/pF	0.57ns
AOI322	9	14	Z ↓	6.02ns/pF	1.72ns	1.36ns/pF	0.69ns
			Z ↑	9.67ns/pF	0.99ns	1.77ns/pF	0.60ns
AOI322H	16	28	Z ↓	3.17ns/pF	1.45ns	0.70ns/pF	0.59ns
			Z ↑	4.81ns/pF	0.93ns	0.89ns/pF	0.54ns
AOI3221	10	16	Z ↓	6.24ns/pF	1.80ns	1.38ns/pF	0.82ns
			Z ↑	12.13ns/pF	1.39ns	2.24ns/pF	0.80ns
AOI3222	11	18	Z ↓	6.24ns/pF	1.80ns	1.38ns/pF	0.82ns
			Z ↑	12.13ns/pF	1.39ns	2.24ns/pF	0.80ns
AOI33	7	12	Z ↓	5.88ns/pF	1.54ns	1.30ns/pF	0.59ns
			Z ↑	6.87ns/pF	0.75ns	1.28ns/pF	0.37ns
AOI33H	14	24	Z ↓	3.08ns/pF	1.40ns	0.68ns/pF	0.56ns
			Z ↑	3.43ns/pF	0.76ns	0.63ns/pF	0.41ns
AOI331	8	14	Z ↓	6.06ns/pF	1.65ns	1.38ns/pF	0.63ns
			Z ↑	9.67ns/pF	0.94ns	1.77ns/pF	0.56ns
AOI3311	9	16	Z ↓	6.24ns/pF	1.71ns	1.41ns/pF	0.70ns
			Z ↑	12.13ns/pF	1.15ns	2.24ns/pF	0.66ns
AOI332	9	16	Z ↓	6.02ns/pF	1.76ns	1.36ns/pF	0.69ns
			Z ↑	9.67ns/pF	1.04ns	1.77ns/pF	0.60ns

VDD=5V, T=25°C, Nominal Process.

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
AOI3321	10	18	Z↓	6.24ns/pF	1.76ns	1.38ns/pF	0.77ns
			Z↑	12.13ns/pF	1.29ns	2.27ns/pF	0.69ns
AOI3322	12	20	Z↓	6.20ns/pF	1.92ns	1.38ns/pF	0.86ns
			Z↑	12.13ns/pF	1.53ns	2.27ns/pF	0.83ns
AOI333	10	18	Z↓	6.02ns/pF	1.86ns	1.36ns/pF	0.79ns
			Z↑	9.67ns/pF	1.18ns	1.77ns/pF	0.70ns
AOI333H	22	36	Z↓	3.17ns/pF	1.69ns	0.70ns/pF	0.78ns
			Z↑	4.81ns/pF	1.27ns	0.89ns/pF	0.73ns
AOI3331	11	20	Z↓	6.24ns/pF	1.85ns	1.41ns/pF	0.80ns
			Z↑	12.13ns/pF	1.43ns	2.24ns/pF	0.80ns
AOI3332	12	22	Z↓	6.20ns/pF	1.97ns	1.41ns/pF	0.84ns
			Z↑	12.13ns/pF	1.58ns	2.24ns/pF	0.90ns
AOI3333	13	24	Z↓	6.20ns/pF	2.06ns	1.41ns/pF	0.89ns
			Z↑	12.13ns/pF	1.72ns	2.24ns/pF	1.00ns
AOI41	6	10	Z↓	7.58ns/pF	1.52ns	1.69ns/pF	0.62ns
			Z↑	7.04ns/pF	0.72ns	1.30ns/pF	0.40ns
AOI411	7	12	Z↓	7.80ns/pF	1.71ns	1.77ns/pF	0.70ns
			Z↑	9.85ns/pF	0.95ns	1.85ns/pF	0.49ns
AOI4111	8	14	Z↓	8.07ns/pF	1.73ns	1.82ns/pF	0.75ns
			Z↑	12.35ns/pF	1.14ns	2.29ns/pF	0.67ns
AOI42	7	12	Z↓	7.53ns/pF	1.54ns	1.69ns/pF	0.57ns
			Z↑	7.04ns/pF	0.67ns	1.33ns/pF	0.33ns
AOI421	9	14	Z↓	7.80ns/pF	1.71ns	1.77ns/pF	0.70ns
			Z↑	9.85ns/pF	1.00ns	1.82ns/pF	0.56ns
AOI4211	10	16	Z↓	8.07ns/pF	1.96ns	1.82ns/pF	0.90ns
			Z↑	12.35ns/pF	1.47ns	2.29ns/pF	0.86ns
AOI422	10	16	Z↓	7.80ns/pF	1.80ns	1.75ns/pF	0.81ns
			Z↑	9.85ns/pF	1.10ns	1.85ns/pF	0.59ns
AOI4221	11	18	Z↓	8.07ns/pF	1.96ns	1.82ns/pF	0.90ns
			Z↑	12.35ns/pF	1.47ns	2.29ns/pF	0.86ns
AOI4222	13	20	Z↓	8.07ns/pF	2.11ns	1.80ns/pF	1.06ns
			Z↑	12.35ns/pF	1.67ns	2.29ns/pF	1.00ns
AOI43	8	14	Z↓	7.53ns/pF	1.69ns	1.67ns/pF	0.73ns
			Z↑	7.04ns/pF	0.81ns	1.33ns/pF	0.43ns
AOI431	9	16	Z↓	7.80ns/pF	1.90ns	1.75ns/pF	0.86ns
			Z↑	9.85ns/pF	1.19ns	1.82ns/pF	0.66ns
AOI4311	10	18	Z↓	8.07ns/pF	1.92ns	1.82ns/pF	0.90ns
			Z↑	12.35ns/pF	1.43ns	2.29ns/pF	0.81ns
AOI432	11	18	Z↓	7.80ns/pF	1.90ns	1.77ns/pF	0.84ns
			Z↑	9.85ns/pF	1.19ns	1.85ns/pF	0.64ns
AOI4321	12	20	Z↓	8.07ns/pF	2.01ns	1.82ns/pF	0.94ns
			Z↑	12.35ns/pF	1.52ns	2.29ns/pF	0.91ns
AOI4322	13	22	Z↓	8.07ns/pF	2.11ns	1.82ns/pF	0.99ns
			Z↑	12.35ns/pF	1.67ns	2.32ns/pF	0.93ns
AOI433	11	20	Z↓	7.80ns/pF	1.99ns	1.75ns/pF	0.96ns
			Z↑	9.85ns/pF	1.34ns	1.82ns/pF	0.75ns

VDD=5V, T=25°C, Nominal Process.

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
AOI4331	12	22	Z ↓	8.07ns/pF	2.11ns	1.82ns/pF	0.99ns
			Z ↑	12.39ns/pF	1.64ns	2.32ns/pF	0.93ns
AOI4332	14	24	Z ↓	8.02ns/pF	2.27ns	1.82ns/pF	1.09ns
			Z ↑	12.35ns/pF	1.86ns	2.29ns/pF	1.05ns
AOI4333	14	26	Z ↓	8.07ns/pF	2.25ns	1.82ns/pF	1.09ns
			Z ↑	12.35ns/pF	1.90ns	2.29ns/pF	1.10ns
AOI44	9	16	Z ↓	7.53ns/pF	1.78ns	1.69ns/pF	0.71ns
			Z ↑	7.04ns/pF	0.86ns	1.33ns/pF	0.43ns
AOI441	11	18	Z ↓	7.80ns/pF	1.90ns	1.77ns/pF	0.84ns
			Z ↑	9.85ns/pF	1.19ns	1.82ns/pF	0.71ns
AOI4411	12	20	Z ↓	8.07ns/pF	2.06ns	1.80ns/pF	1.01ns
			Z ↑	12.35ns/pF	1.57ns	2.32ns/pF	0.89ns
AOI442	12	20	Z ↓	7.80ns/pF	1.99ns	1.77ns/pF	0.89ns
			Z ↑	9.90ns/pF	1.27ns	1.82ns/pF	0.75ns
AOI4421	13	22	Z ↓	8.07ns/pF	2.16ns	1.82ns/pF	1.04ns
			Z ↑	12.35ns/pF	1.76ns	2.32ns/pF	0.98ns
AOI4422	15	24	Z ↓	8.07ns/pF	2.30ns	1.82ns/pF	1.13ns
			Z ↑	12.35ns/pF	1.95ns	2.29ns/pF	1.15ns
AOI443	13	22	Z ↓	7.80ns/pF	2.14ns	1.77ns/pF	0.98ns
			Z ↑	9.90ns/pF	1.41ns	1.82ns/pF	0.85ns
AOI4431	14	24	Z ↓	8.07ns/pF	2.30ns	1.82ns/pF	1.13ns
			Z ↑	12.35ns/pF	1.90ns	2.29ns/pF	1.15ns
AOI4432	15	26	Z ↓	8.07ns/pF	2.30ns	1.82ns/pF	1.13ns
			Z ↑	12.35ns/pF	1.95ns	2.29ns/pF	1.15ns
AOI4433	16	28	Z ↓	8.07ns/pF	2.49ns	1.82ns/pF	1.28ns
			Z ↑	12.35ns/pF	2.24ns	2.29ns/pF	1.29ns
AOI444	14	24	Z ↓	7.80ns/pF	2.23ns	1.77ns/pF	1.03ns
			Z ↑	9.85ns/pF	1.57ns	1.82ns/pF	0.90ns
AOI4441	15	26	Z ↓	8.07ns/pF	2.39ns	1.82ns/pF	1.18ns
			Z ↑	12.35ns/pF	2.05ns	2.29ns/pF	1.19ns
AOI4442	17	28	Z ↓	8.02ns/pF	2.61ns	1.82ns/pF	1.33ns
			Z ↑	12.35ns/pF	2.33ns	2.29ns/pF	1.38ns
AOI4443	17	30	Z ↓	8.02ns/pF	2.56ns	1.82ns/pF	1.28ns
			Z ↑	12.39ns/pF	2.22ns	2.32ns/pF	1.27ns
AOI4444	19	32	Z ↓	8.02ns/pF	2.75ns	1.82ns/pF	1.42ns
			Z ↑	12.35ns/pF	2.52ns	2.29ns/pF	1.48ns

VDD=5V, T=25°C, Nominal Process.

Built in Self Test

BIST1

This cell provides the required data select logic to convert any Flip-Flop to a BIST style circuit. The BIST1 cell is used to generate the Flip-Flop data input.

Grids 11, **Transistors** 18

Inputs

D0,D1,B0,B1

Outputs

Z

Capacitances

	D0	D1	B0	B1
Area	0.062pF	0.061pF	0.061pF	0.062pF
Perf	0.223pF	0.222pF	0.222pF	0.223pF

Truth Table

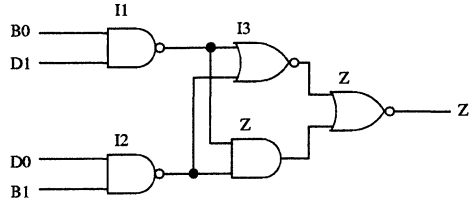
INPUTS				OUTPUT
D0	D1	B0	B1	Z
X	X	0	0	0
1	X	0	1	1
0	X	0	1	0
X	1	1	0	1
X	0	1	0	0
0	0	1	1	0
0	1	1	1	1
1	0	1	1	1
1	1	1	1	0

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
B0 ↓	Z ↓	3.88ns/pF	1.13ns	0.89ns/pF	0.68ns
B0 ↓	Z ↑	6.95ns/pF	1.09ns	1.17ns/pF	0.89ns
B0 ↑	Z ↓	2.18ns/pF	2.19ns	0.47ns/pF	1.35ns
B0 ↑	Z ↑	6.73ns/pF	1.63ns	1.25ns/pF	0.87ns
B1 ↓	Z ↓	3.88ns/pF	1.08ns	0.89ns/pF	0.68ns
B1 ↓	Z ↑	6.95ns/pF	1.05ns	1.17ns/pF	0.89ns
B1 ↑	Z ↓	2.18ns/pF	2.14ns	0.47ns/pF	1.35ns
B1 ↑	Z ↑	6.73ns/pF	1.58ns	1.25ns/pF	0.87ns
D0 ↓	Z ↓	3.88ns/pF	1.08ns	0.89ns/pF	0.68ns
D0 ↓	Z ↑	6.95ns/pF	1.05ns	1.17ns/pF	0.89ns
D0 ↑	Z ↓	2.18ns/pF	2.14ns	0.47ns/pF	1.35ns
D0 ↑	Z ↑	6.73ns/pF	1.58ns	1.25ns/pF	0.87ns
D1 ↓	Z ↓	3.88ns/pF	1.13ns	0.89ns/pF	0.68ns
D1 ↓	Z ↑	6.95ns/pF	1.09ns	1.17ns/pF	0.89ns
D1 ↑	Z ↓	2.18ns/pF	2.19ns	0.47ns/pF	1.35ns
D1 ↑	Z ↑	6.73ns/pF	1.63ns	1.25ns/pF	0.87ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Full Adder

This cell is a two bit full adder which provides inverted sum and carry outputs. FA cells can be combined to make arbitrary length adders.

Grids 15, **Transistors** 24

Inputs

A,B,C

Outputs

ZCN,ZSN

Capacitances

	A	B	C
Area	0.138pF	0.140pF	0.112pF
Perf.	0.589pF	0.591pF	0.450pF

Truth Table

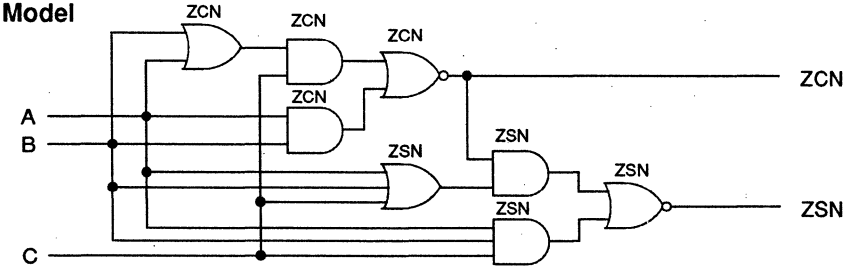
INPUTS			OUTPUTS	
A	B	C	ZSN	ZCN
0	0	0	1	1
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	0

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
A ↓	ZCN ↑	6.78ns/pF	0.94ns	1.25ns/pF	0.54ns
A ↓	ZSN ↓	12.35ns/pF	2.67ns	2.71ns/pF	1.01ns
A ↓	ZSN ↑	6.91ns/pF	0.88ns	1.28ns/pF	0.47ns
A ↑	ZCN ↓	4.24ns/pF	1.72ns	0.94ns/pF	0.69ns
A ↑	ZSN ↓	4.19ns/pF	1.79ns	0.96ns/pF	0.62ns
A ↑	ZSN ↑	10.25ns/pF	2.44ns	2.29ns/pF	0.95ns
B ↓	ZCN ↑	6.78ns/pF	0.94ns	1.25ns/pF	0.54ns
B ↓	ZSN ↓	12.35ns/pF	2.67ns	2.71ns/pF	1.01ns
B ↓	ZSN ↑	6.91ns/pF	0.88ns	1.28ns/pF	0.47ns
B ↑	ZCN ↓	4.24ns/pF	1.72ns	0.94ns/pF	0.69ns
B ↑	ZSN ↓	4.19ns/pF	1.79ns	0.96ns/pF	0.62ns
B ↑	ZSN ↑	10.25ns/pF	2.44ns	2.29ns/pF	0.95ns
C ↓	ZCN ↑	6.78ns/pF	0.94ns	1.25ns/pF	0.54ns
C ↓	ZSN ↓	12.35ns/pF	2.67ns	2.71ns/pF	1.01ns
C ↓	ZSN ↑	6.91ns/pF	0.88ns	1.28ns/pF	0.47ns
C ↑	ZCN ↓	4.50ns/pF	1.32ns	0.99ns/pF	0.55ns
C ↑	ZSN ↓	4.19ns/pF	1.79ns	0.96ns/pF	0.62ns
C ↑	ZSN ↑	10.52ns/pF	2.03ns	2.35ns/pF	0.82ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Inverter

INRB*n*

The INRB cells provide the logical inversion of the input signal. This cell can also be used as an inverting buffer and for this purpose many higher power varieties exist.
The parameter *n* indicates the power of the cell in multiples of a standard INRB. A suffix of H indicates high power (2x) where an S suffix denotes super power (4x). Otherwise the parameter *n* specifies the multiple as a numeric value.

Inputs
A

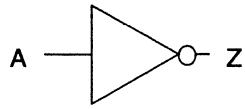
Outputs
Z

Logic Equation

$Z = \overline{A}$

Example: INRB12

Motis Model



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Capacitances

The input terminal capacitance for all INRB cells is provided in the following table.

	INRB	INRBH	INRBS	INRB8	INRB12
Area	0.034pF	0.067pF	0.133pF	0.265pF	0.397pF
Perf.	0.145pF	0.292pF	0.584pF	1.169pF	1.753pF

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
INRB	2	2	Z ↓	2.54ns/pF	1.31ns	0.55ns/pF	0.43ns
			Z ↑	3.70ns/pF	0.44ns	0.68ns/pF	0.23ns
INRBH	3	4	Z ↓	1.47ns/pF	0.99ns	0.31ns/pF	0.28ns
			Z ↑	1.87ns/pF	0.33ns	0.34ns/pF	0.16ns
INRBS	5	8	Z ↓	0.94ns/pF	0.76ns	0.18ns/pF	0.24ns
			Z ↑	0.98ns/pF	0.26ns	0.18ns/pF	0.14ns
INRB8	9	16	Z ↓	0.62ns/pF	0.57ns	0.10ns/pF	0.20ns
			Z ↑	0.53ns/pF	0.23ns	0.10ns/pF	0.11ns
INRB12	13	24	Z ↓	0.49ns/pF	0.49ns	0.08ns/pF	0.18ns
			Z ↑	0.36ns/pF	0.22ns	0.08ns/pF	0.08ns

VDD=5V, T=25°C, Nominal Process.

The ND cells provide a logical NAND of two to four inputs as specified by the parameter *n*.

High power and super power NAND cells are available. A suffix of *H* indicates high power (2x) where an *S* suffix denotes super power (4x).

Example: ND3

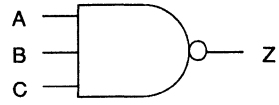
Inputs
A,B,C

Outputs
Z

Logic Equation

$Z = \overline{(A*B*C)}$

Motis Model



Capacitances

The input terminal capacitance for all ND cells is provided in the following table.

	ND2,ND3,ND4	ND2H	ND2S	ND3H	ND3S	ND4H	ND4S
Area	0.034pF	0.069pF	0.137pF	0.067pF	0.133pF	0.034pF	0.133pF
Perf.	0.145pF	0.294pF	0.588pF	0.292pF	0.584pF	0.145pF	0.588pF

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
ND2	3	4	Z ↓	4.19ns/pF	1.32ns	0.89ns/pF	0.44ns
			Z ↑	3.79ns/pF	0.45ns	0.70ns/pF	0.21ns
ND2H	5	8	Z ↓	2.23ns/pF	1.03ns	0.47ns/pF	0.34ns
			Z ↑	1.92ns/pF	0.36ns	0.36ns/pF	0.14ns
ND2S	9	16	Z ↓	1.29ns/pF	0.84ns	0.26ns/pF	0.27ns
			Z ↑	1.03ns/pF	0.29ns	0.18ns/pF	0.14ns
ND3	4	6	Z ↓	5.80ns/pF	1.39ns	1.28ns/pF	0.47ns
			Z ↑	3.83ns/pF	0.57ns	0.73ns/pF	0.23ns
ND3H	8	12	Z ↓	2.94ns/pF	1.17ns	0.65ns/pF	0.39ns
			Z ↑	1.96ns/pF	0.43ns	0.36ns/pF	0.19ns
ND3S	14	24	Z ↓	1.60ns/pF	0.98ns	0.34ns/pF	0.35ns
			Z ↑	1.03ns/pF	0.39ns	0.18ns/pF	0.19ns
ND4	5	8	Z ↓	7.40ns/pF	1.41ns	1.64ns/pF	0.52ns
			Z ↑	3.97ns/pF	0.56ns	0.73ns/pF	0.28ns
ND4H	8	14	Z ↓	1.03ns/pF	2.25ns	0.26ns/pF	1.32ns
			Z ↑	1.83ns/pF	1.07ns	0.34ns/pF	0.73ns
ND4S	18	32	Z ↓	1.92ns/pF	1.17ns	0.42ns/pF	0.43ns
			Z ↑	1.03ns/pF	0.43ns	0.21ns/pF	0.17ns

VDD=5V, T=25°C, Nominal Process.

The NR cells provide a logical NOR of two to four inputs as specified by the parameter *n*.

High power and super power NOR cells are available. A suffix of *H* indicates high power (2x) where an *S* suffix denotes super power (4x).

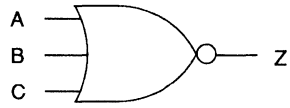
Example: NR3

Inputs
A,B,C

Outputs
Z

Logic Equation

$$Z = \overline{(A+B+C)}$$



Capacitances

The input terminal capacitance for all NR cells is provided in the following table.

	NR2,NR3,NR4	NR2H	NR2S	NR3H	NR3S	NR4H	NR4S
Area	0.034pF	0.069pF	0.138pF	0.071pF	0.141pF	0.069pF	0.137pF
Perf.	0.145pF	0.294pF	0.589pF	0.296pF	0.592pF	0.294pF	0.588pF

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
NR2	3	4	Z↓	2.67ns/pF	1.30ns	0.55ns/pF	0.43ns
			Z↑	6.64ns/pF	0.47ns	1.20ns/pF	0.25ns
NR2H	5	8	Z↓	1.52ns/pF	1.02ns	0.31ns/pF	0.33ns
			Z↑	3.30ns/pF	0.39ns	0.60ns/pF	0.19ns
NR2S	9	16	Z↓	0.98ns/pF	0.74ns	0.18ns/pF	0.29ns
			Z↑	1.65ns/pF	0.39ns	0.29ns/pF	0.20ns
NR3	4	6	Z↓	2.67ns/pF	1.44ns	0.57ns/pF	0.45ns
			Z↑	9.27ns/pF	0.60ns	1.69ns/pF	0.33ns
NR3H	7	12	Z↓	1.52ns/pF	1.12ns	0.31ns/pF	0.37ns
			Z↑	4.59ns/pF	0.51ns	0.83ns/pF	0.25ns
NR3S	13	24	Z↓	0.98ns/pF	0.84ns	0.18ns/pF	0.29ns
			Z↑	2.32ns/pF	0.46ns	0.42ns/pF	0.24ns
NR4	5	8	Z↓	2.76ns/pF	1.45ns	0.57ns/pF	0.50ns
			Z↑	11.72ns/pF	0.71ns	2.11ns/pF	0.43ns
NR4H	10	16	Z↓	1.56ns/pF	1.14ns	0.31ns/pF	0.42ns
			Z↑	5.84ns/pF	0.65ns	1.07ns/pF	0.35ns
NR4S	18	32	Z↓	0.98ns/pF	0.88ns	0.18ns/pF	0.33ns
			Z↑	2.90ns/pF	0.67ns	0.52ns/pF	0.35ns

VDD=5V, T=25°C, Nominal Process.

These cells provide the inverted AND of two to four OR groups. The parameters *a, b, c,* and *d* specify how many inputs make up each OR group. These parameters are always specified in descending order and parameters *c* and *d* are omitted when their values are zero.

A small amount of higher power OAI cells are available. A suffix of *H* indicates high power (2x) where an *S* suffix denotes super power (4x).

Example: OAI221

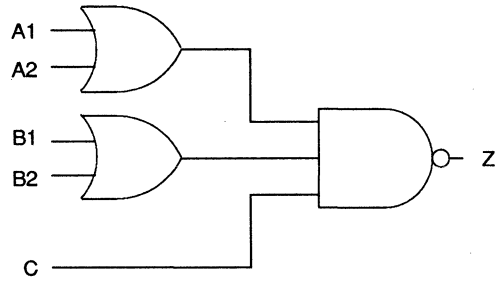
Inputs
A1,A2,B1,B2,C

Outputs
Z

Logic Equation

$$Z = \overline{(A1+A2)*(B1+B2)*C}$$

Motis Model



Capacitances

The input terminal capacitance for all OAI cells is provided in the following table and is a function of the power of the cell.

	Normal Power	High Power	Super Power
Area	0.034pF	0.069pF	0.135pF
Perf.	0.145pF	0.294pF	0.587pF

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
OAI21	4	6	Z ↓	4.19ns/pF	1.41ns	0.91ns/pF	0.47ns
			Z ↑	6.73ns/pF	0.53ns	1.23ns/pF	0.27ns
OAI21H	7	12	Z ↓	2.27ns/pF	1.15ns	0.50ns/pF	0.37ns
			Z ↑	3.39ns/pF	0.44ns	0.63ns/pF	0.22ns
OAI21S	13	24	Z ↓	1.34ns/pF	0.86ns	0.29ns/pF	0.30ns
			Z ↑	1.69ns/pF	0.41ns	0.31ns/pF	0.18ns
OAI211	5	8	Z ↓	5.84ns/pF	1.56ns	1.30ns/pF	0.54ns
			Z ↑	6.91ns/pF	0.59ns	1.28ns/pF	0.33ns
OAI2111	6	10	Z ↓	7.58ns/pF	1.57ns	1.67ns/pF	0.64ns
			Z ↑	7.04ns/pF	0.62ns	1.30ns/pF	0.35ns
OAI22	5	8	Z ↓	4.19ns/pF	1.41ns	0.91ns/pF	0.47ns
			Z ↑	6.73ns/pF	0.58ns	1.25ns/pF	0.25ns

VDD=5V, T=25°C, Nominal Process.

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
OAI22H	9	16	Z↓	1.87ns/pF	1.14ns	0.42ns/pF	0.34ns
			Z↑	3.39ns/pF	0.54ns	0.63ns/pF	0.27ns
OAI221	7	10	Z↓	5.88ns/pF	1.54ns	1.30ns/pF	0.59ns
			Z↑	6.91ns/pF	0.69ns	1.28ns/pF	0.37ns
OAI2211	8	12	Z↓	7.58ns/pF	1.71ns	1.69ns/pF	0.71ns
			Z↑	7.04ns/pF	0.81ns	1.33ns/pF	0.43ns
OAI222	8	12	Z↓	5.88ns/pF	1.59ns	1.30ns/pF	0.64ns
			Z↑	6.87ns/pF	0.80ns	1.28ns/pF	0.42ns
OAI222H	14	24	Z↓	2.10ns/pF	1.42ns	0.63ns/pF	0.36ns
			Z↑	3.39ns/pF	0.73ns	0.63ns/pF	0.36ns
OAI2221	9	14	Z↓	7.53ns/pF	1.78ns	1.67ns/pF	0.78ns
			Z↑	7.04ns/pF	0.86ns	1.33ns/pF	0.43ns
OAI2222	10	16	Z↓	7.53ns/pF	1.83ns	1.69ns/pF	0.76ns
			Z↑	7.04ns/pF	0.91ns	1.33ns/pF	0.48ns
OAI2222H	18	32	Z↓	3.08ns/pF	1.49ns	0.68ns/pF	0.61ns
			Z↑	3.48ns/pF	0.83ns	0.65ns/pF	0.44ns
OAI31	5	8	Z↓	4.32ns/pF	1.45ns	0.96ns/pF	0.48ns
			Z↑	9.45ns/pF	0.57ns	1.75ns/pF	0.29ns
OAI311	6	10	Z↓	6.06ns/pF	1.60ns	1.36ns/pF	0.60ns
			Z↑	9.63ns/pF	0.72ns	1.77ns/pF	0.41ns
OAI3111	7	12	Z↓	7.85ns/pF	1.69ns	1.77ns/pF	0.65ns
			Z↑	9.85ns/pF	0.76ns	1.82ns/pF	0.42ns
OAI32	6	10	Z↓	4.32ns/pF	1.49ns	0.94ns/pF	0.55ns
			Z↑	9.45ns/pF	0.66ns	1.75ns/pF	0.34ns
OAI321	7	12	Z↓	6.06ns/pF	1.65ns	1.36ns/pF	0.65ns
			Z↑	9.67ns/pF	0.80ns	1.80ns/pF	0.44ns
OAI3211	8	14	Z↓	7.80ns/pF	1.80ns	1.77ns/pF	0.70ns
			Z↑	9.85ns/pF	0.86ns	1.85ns/pF	0.45ns
OAI322	9	14	Z↓	6.02ns/pF	1.81ns	1.36ns/pF	0.74ns
			Z↑	9.67ns/pF	0.99ns	1.80ns/pF	0.53ns
OAI3221	10	16	Z↓	7.80ns/pF	1.99ns	1.75ns/pF	0.91ns
			Z↑	9.85ns/pF	1.19ns	1.85ns/pF	0.64ns
OAI3222	11	18	Z↓	7.80ns/pF	1.99ns	1.75ns/pF	0.91ns
			Z↑	9.85ns/pF	1.19ns	1.82ns/pF	0.66ns
OAI33	7	12	Z↓	4.32ns/pF	1.54ns	0.94ns/pF	0.59ns
			Z↑	9.45ns/pF	0.80ns	1.75ns/pF	0.43ns
OAI331	8	14	Z↓	6.06ns/pF	1.69ns	1.36ns/pF	0.69ns
			Z↑	9.63ns/pF	0.96ns	1.77ns/pF	0.56ns
OAI3311	9	16	Z↓	7.80ns/pF	1.85ns	1.77ns/pF	0.75ns
			Z↑	9.85ns/pF	1.00ns	1.82ns/pF	0.56ns
OAI332	9	16	Z↓	6.06ns/pF	1.74ns	1.36ns/pF	0.74ns
			Z↑	9.63ns/pF	1.06ns	1.77ns/pF	0.60ns
OAI3321	10	18	Z↓	7.80ns/pF	1.90ns	1.77ns/pF	0.79ns
			Z↑	9.85ns/pF	1.10ns	1.82ns/pF	0.61ns
OAI3322	12	20	Z↓	7.80ns/pF	2.14ns	1.77ns/pF	0.98ns
			Z↑	9.90ns/pF	1.36ns	1.82ns/pF	0.80ns

VDD=5V, T=25°C, Nominal Process.

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
OAI333	10	18	Z ↓	6.02ns/pF	1.86ns	1.36ns/pF	0.79ns
			Z ↑	9.67ns/pF	1.18ns	1.77ns/pF	0.70ns
OAI3331	11	20	Z ↓	7.80ns/pF	1.99ns	1.75ns/pF	0.91ns
			Z ↑	9.85ns/pF	1.24ns	1.82ns/pF	0.71ns
OAI3332	12	22	Z ↓	7.85ns/pF	2.02ns	1.75ns/pF	0.96ns
			Z ↑	9.85ns/pF	1.34ns	1.82ns/pF	0.75ns
OAI3333	13	24	Z ↓	7.80ns/pF	2.18ns	1.77ns/pF	0.98ns
			Z ↑	9.85ns/pF	1.53ns	1.82ns/pF	0.85ns
OAI41	6	10	Z ↓	4.41ns/pF	1.60ns	0.96ns/pF	0.57ns
			Z ↑	11.90ns/pF	0.87ns	2.19ns/pF	0.46ns
OAI411	7	12	Z ↓	6.20ns/pF	1.82ns	1.41ns/pF	0.70ns
			Z ↑	12.13ns/pF	1.05ns	2.24ns/pF	0.57ns
OAI4111	8	14	Z ↓	8.07ns/pF	1.92ns	1.82ns/pF	0.80ns
			Z ↑	12.35ns/pF	1.09ns	2.29ns/pF	0.62ns
OAI42	7	12	Z ↓	4.41ns/pF	1.60ns	0.96ns/pF	0.57ns
			Z ↑	11.90ns/pF	0.82ns	2.19ns/pF	0.46ns
OAI421	9	14	Z ↓	6.20ns/pF	1.92ns	1.41ns/pF	0.75ns
			Z ↑	12.13ns/pF	1.24ns	2.24ns/pF	0.71ns
OAI4211	10	16	Z ↓	8.07ns/pF	2.16ns	1.82ns/pF	0.94ns
			Z ↑	12.35ns/pF	1.43ns	2.32ns/pF	0.79ns
OAI422	10	16	Z ↓	6.24ns/pF	1.85ns	1.41ns/pF	0.75ns
			Z ↑	12.13ns/pF	1.20ns	2.24ns/pF	0.71ns
OAI4221	11	18	Z ↓	8.07ns/pF	2.16ns	1.82ns/pF	0.94ns
			Z ↑	12.35ns/pF	1.43ns	2.29ns/pF	0.81ns
OAI4222	13	20	Z ↓	8.07ns/pF	2.25ns	1.80ns/pF	1.11ns
			Z ↑	12.35ns/pF	1.62ns	2.29ns/pF	0.95ns
OAI43	8	14	Z ↓	4.41ns/pF	1.64ns	0.96ns/pF	0.62ns
			Z ↑	11.90ns/pF	1.06ns	2.19ns/pF	0.61ns
OAI431	9	16	Z ↓	6.20ns/pF	1.92ns	1.38ns/pF	0.82ns
			Z ↑	12.13ns/pF	1.34ns	2.24ns/pF	0.76ns
OAI4311	10	18	Z ↓	8.07ns/pF	2.06ns	1.82ns/pF	0.90ns
			Z ↑	12.35ns/pF	1.38ns	2.29ns/pF	0.76ns
OAI432	11	18	Z ↓	6.24ns/pF	1.90ns	1.41ns/pF	0.80ns
			Z ↑	12.13ns/pF	1.34ns	2.27ns/pF	0.74ns
OAI4321	12	20	Z ↓	8.07ns/pF	2.16ns	1.80ns/pF	1.01ns
			Z ↑	12.35ns/pF	1.52ns	2.29ns/pF	0.86ns
OAI4322	13	22	Z ↓	8.07ns/pF	2.25ns	1.82ns/pF	1.04ns
			Z ↑	12.35ns/pF	1.62ns	2.29ns/pF	0.95ns
OAI433	11	20	Z ↓	6.20ns/pF	2.01ns	1.41ns/pF	0.84ns
			Z ↑	12.13ns/pF	1.53ns	2.24ns/pF	0.85ns
OAI4331	12	22	Z ↓	8.07ns/pF	2.25ns	1.82ns/pF	1.04ns
			Z ↑	12.35ns/pF	1.67ns	2.29ns/pF	0.95ns
OAI4332	14	24	Z ↓	8.07ns/pF	2.30ns	1.82ns/pF	1.09ns
			Z ↑	12.35ns/pF	1.76ns	2.29ns/pF	1.00ns
OAI4333	14	26	Z ↓	8.07ns/pF	2.35ns	1.80ns/pF	1.15ns
			Z ↑	12.35ns/pF	1.86ns	2.29ns/pF	1.05ns

VDD=5V, T=25°C, Nominal Process.

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
OAI44	9	16	Z↓	4.41ns/pF	1.64ns	0.99ns/pF	0.60ns
			Z↑	11.90ns/pF	1.20ns	2.19ns/pF	0.66ns
OAI441	11	18	Z↓	6.24ns/pF	1.85ns	1.41ns/pF	0.80ns
			Z↑	12.13ns/pF	1.34ns	2.24ns/pF	0.80ns
OAI4411	12	20	Z↓	8.07ns/pF	2.16ns	1.82ns/pF	0.99ns
			Z↑	12.35ns/pF	1.57ns	2.29ns/pF	0.91ns
OAI442	12	20	Z↓	6.24ns/pF	1.99ns	1.38ns/pF	0.91ns
			Z↑	12.13ns/pF	1.62ns	2.24ns/pF	0.90ns
OAI4421	13	22	Z↓	8.07ns/pF	2.25ns	1.82ns/pF	1.04ns
			Z↑	12.39ns/pF	1.69ns	2.32ns/pF	0.93ns
OAI4422	15	24	Z↓	8.07ns/pF	2.39ns	1.82ns/pF	1.18ns
			Z↑	12.35ns/pF	1.90ns	2.29ns/pF	1.15ns
OAI443	13	22	Z↓	6.20ns/pF	2.06ns	1.41ns/pF	0.89ns
			Z↑	12.13ns/pF	1.67ns	2.24ns/pF	0.95ns
OAI4431	14	24	Z↓	8.02ns/pF	2.41ns	1.82ns/pF	1.13ns
			Z↑	12.39ns/pF	1.88ns	2.29ns/pF	1.10ns
OAI4432	15	26	Z↓	8.02ns/pF	2.41ns	1.82ns/pF	1.13ns
			Z↑	12.39ns/pF	1.88ns	2.29ns/pF	1.10ns
OAI4433	16	28	Z↓	8.02ns/pF	2.61ns	1.82ns/pF	1.28ns
			Z↑	12.35ns/pF	2.24ns	2.29ns/pF	1.29ns
OAI444	14	24	Z↓	6.20ns/pF	2.11ns	1.41ns/pF	0.94ns
			Z↑	12.13ns/pF	1.82ns	2.24ns/pF	1.04ns
OAI4441	15	26	Z↓	8.07ns/pF	2.44ns	1.82ns/pF	1.18ns
			Z↑	12.39ns/pF	2.03ns	2.29ns/pF	1.15ns
OAI4442	17	28	Z↓	8.02ns/pF	2.65ns	1.82ns/pF	1.33ns
			Z↑	12.35ns/pF	2.33ns	2.29ns/pF	1.34ns
OAI4443	17	30	Z↓	8.07ns/pF	2.54ns	1.82ns/pF	1.28ns
			Z↑	12.39ns/pF	2.22ns	2.29ns/pF	1.29ns
OAI4444	19	32	Z↓	8.02ns/pF	2.75ns	1.82ns/pF	1.42ns
			Z↑	12.35ns/pF	2.52ns	2.29ns/pF	1.48ns

VDD=5V, T=25°C, Nominal Process.

The OR cells provide a logical OR of two to four inputs as specified by the parameter *n*.

High power and super power OR cells are available. A suffix of *H* indicates high power (2x) where an *S* suffix denotes super power (4x).

Example: OR3

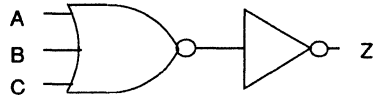
Inputs
A,B,C

Outputs
Z

Logic Equation

Z = (A+B+C)

Motis Model



Capacitances

The input terminal capacitance for all OR cells is provided in the following table and is identical for all OR cells and all higher power versions.

	Terminal Capacitance
Area	0.034pF
Perf.	0.145pF

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
OR2	4	6	Z↓	2.10ns/pF	1.13ns	0.50ns/pF	0.71ns
			Z↑	3.66ns/pF	0.85ns	0.65ns/pF	0.49ns
OR2H	6	8	Z↓	1.20ns/pF	1.45ns	0.31ns/pF	0.90ns
			Z↑	1.78ns/pF	1.14ns	0.34ns/pF	0.64ns
OR2S	8	12	Z↓	0.80ns/pF	2.02ns	0.21ns/pF	1.31ns
			Z↑	0.98ns/pF	1.41ns	0.18ns/pF	0.81ns
OR3	5	8	Z↓	2.23ns/pF	1.84ns	0.55ns/pF	1.05ns
			Z↑	3.66ns/pF	0.94ns	0.68ns/pF	0.51ns
OR3H	7	10	Z↓	1.34ns/pF	2.15ns	0.34ns/pF	1.35ns
			Z↑	1.83ns/pF	1.21ns	0.34ns/pF	0.69ns
OR3S	9	14	Z↓	1.03ns/pF	2.82ns	0.29ns/pF	1.82ns
			Z↑	0.94ns/pF	1.53ns	0.18ns/pF	0.86ns
OR4	6	10	Z↓	2.36ns/pF	2.35ns	0.57ns/pF	1.36ns
			Z↑	3.66ns/pF	0.99ns	0.68ns/pF	0.51ns
OR4H	8	12	Z↓	1.52ns/pF	2.74ns	0.36ns/pF	1.72ns
			Z↑	1.87ns/pF	1.19ns	0.34ns/pF	0.69ns
OR4S	10	16	Z↓	1.11ns/pF	3.64ns	0.31ns/pF	2.38ns
			Z↑	0.94ns/pF	1.57ns	0.18ns/pF	0.91ns

VDD=5V, T=25°C, Nominal Process.

Select Data

SD210

Select either D0 or D1 to the output.

Grids 7, **Transistors** 12

Inputs
D0,D1,SD

Outputs
Z

Truth Table

INPUTS			OUTPUTS
D0	D1	SD	Z
0	X	0	0
1	X	0	1
X	0	1	0
X	1	1	1

Capacitances

	D0	D1	SD
Area	0.037pF	0.034pF	0.066pF
Perf	0.149pF	0.145pF	0.291pF

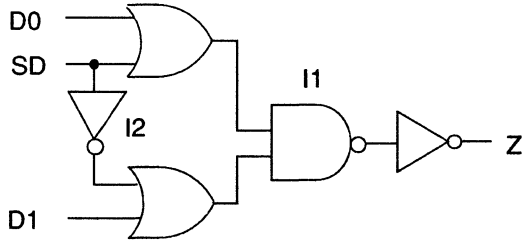
6

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	Z ↓	2.10ns/pF	1.42ns	0.50ns/pF	0.80ns
D0 ↑	Z ↑	3.66ns/pF	1.23ns	0.68ns/pF	0.70ns
D1 ↓	Z ↓	2.10ns/pF	1.42ns	0.50ns/pF	0.80ns
D1 ↑	Z ↑	3.66ns/pF	1.23ns	0.68ns/pF	0.70ns
SD ↓	Z ↓	2.10ns/pF	1.42ns	0.50ns/pF	0.80ns
SD ↓	Z ↑	3.66ns/pF	1.09ns	0.70ns/pF	0.73ns
SD ↑	Z ↓	2.10ns/pF	2.09ns	0.50ns/pF	1.09ns
SD ↑	Z ↑	3.66ns/pF	1.23ns	0.68ns/pF	0.70ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Select Data

SD211

Select either D1 or the inversion of D0 to the output.

Grids 6, **Transistors** 10

Inputs
D0,D1,SD

Outputs
Z

Truth Table

INPUTS			OUTPUTS
D0	D1	SD	Z
0	X	0	1
1	X	0	0
X	0	1	0
X	1	1	1

Capacitances

	D0	D1	SD
Area	0.034pF	0.034pF	0.071pF
Perf	0.145pF	0.145pF	0.296pF

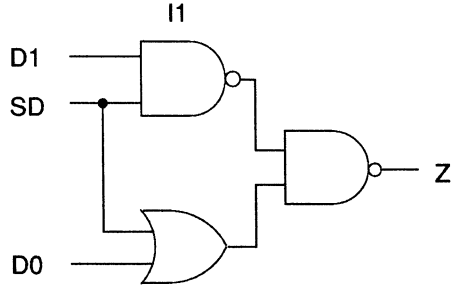
6

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	Z ↑	6.73ns/pF	0.53ns	1.23ns/pF	0.27ns
D0 ↑	Z ↓	4.19ns/pF	1.41ns	0.91ns/pF	0.47ns
D1 ↓	Z ↓	3.97ns/pF	0.66ns	0.89ns/pF	0.44ns
D1 ↑	Z ↑	3.61ns/pF	1.20ns	0.60ns/pF	0.72ns
SD ↓	Z ↓	3.97ns/pF	0.66ns	0.89ns/pF	0.44ns
SD ↓	Z ↑	6.73ns/pF	0.53ns	1.23ns/pF	0.27ns
SD ↑	Z ↓	4.19ns/pF	1.41ns	0.91ns/pF	0.47ns
SD ↑	Z ↑	3.61ns/pF	1.20ns	0.60ns/pF	0.72ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Select Data

SD212

Select either D0 or the inversion of D1 to the output.

Grids 6, **Transistors** 10

Inputs
D0,D1,SD

Outputs
Z

Truth Table

INPUTS			OUTPUTS
D0	D1	SD	Z
0	X	0	0
1	X	0	1
X	0	1	1
X	1	1	0

Capacitances

	D0	D1	SD
Area	0.034pF	0.034pF	0.071pF
Perf	0.145pF	0.145pF	0.296pF

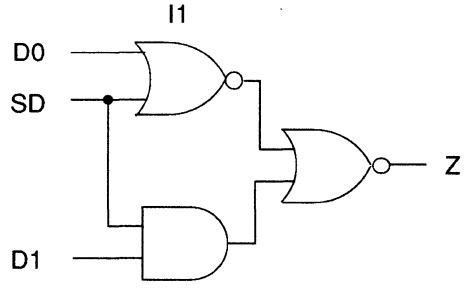
6

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	Z ↓	1.78ns/pF	1.56ns	0.52ns/pF	0.73ns
D0 ↑	Z ↑	6.33ns/pF	1.24ns	1.17ns/pF	0.60ns
D1 ↓	Z ↑	6.78ns/pF	0.51ns	1.25ns/pF	0.25ns
D1 ↑	Z ↓	4.19ns/pF	1.36ns	0.91ns/pF	0.47ns
SD ↓	Z ↓	1.78ns/pF	1.56ns	0.52ns/pF	0.73ns
SD ↓	Z ↑	6.78ns/pF	0.51ns	1.25ns/pF	0.25ns
SD ↑	Z ↓	4.19ns/pF	1.36ns	0.91ns/pF	0.47ns
SD ↑	Z ↑	6.33ns/pF	1.24ns	1.17ns/pF	0.60ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Select Data

SD213

Select either the inversion of D0 or the inversion of D1 to the output.

Grids 6, **Transistors** 10

Inputs
D0,D1,SD

Outputs
Z

Truth Table

INPUTS			OUTPUTS
D0	D1	SD	Z
0	X	0	1
1	X	0	0
X	0	1	1
X	1	1	0

Capacitances

	D0	D1	SD
Area	0.034pF	0.034pF	0.071pF
Perf	0.145pF	0.146pF	0.296pF

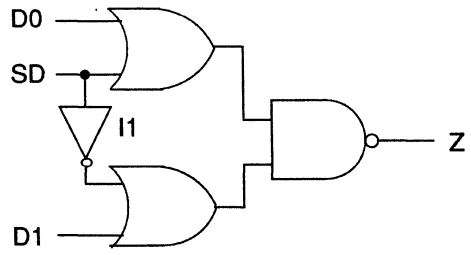
6

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	Z ↑	6.73ns/pF	0.58ns	1.25ns/pF	0.25ns
D0 ↑	Z ↓	4.19ns/pF	1.41ns	0.91ns/pF	0.47ns
D1 ↓	Z ↑	6.73ns/pF	0.58ns	1.25ns/pF	0.25ns
D1 ↑	Z ↓	4.19ns/pF	1.41ns	0.91ns/pF	0.47ns
SD ↓	Z ↓	3.79ns/pF	0.88ns	0.83ns/pF	0.58ns
SD ↓	Z ↑	6.73ns/pF	0.58ns	1.25ns/pF	0.25ns
SD ↑	Z ↓	4.19ns/pF	1.41ns	0.91ns/pF	0.47ns
SD ↑	Z ↑	7.00ns/pF	0.98ns	1.30ns/pF	0.50ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Tri-State Bus Driver — TBDI

The TBDI cells are tri-statable inverters. These cells are intended for internal bus structures.

A high power TBDI cell is available. The suffix of *H* indicates high power (2x).

Inputs
D,CK,CKN

Outputs
QN

Truth Table

INPUTS			OUTPUT
D	CK	CKN	QN
0	1	0	1
1	1	0	0
X	0	1	High Impedance

Capacitances

	TBDI			TBDIH		
	D	CK	CKN	D	CK	CKN
Area	0.034pF	0.018pF	0.018pF	0.067pF	0.039pF	0.039pF
Perf	0.145pF	0.036pF	0.051pF	0.292pF	0.073pF	0.101pF

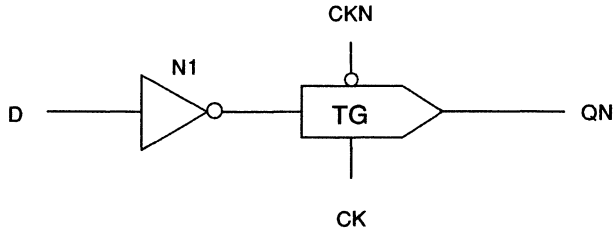
6

Cell Size and Delay Information

					Propagation Delay			
			From	To	Area		Performance	
Cell	Grids	Transistors	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
TBDI	4	4	CK ↑	QN ↓	1.43ns/pF	0.39ns	0.63ns/pF	0.36ns
			CK ↑	QN ↑	2.45ns/pF	0.45ns	0.99ns/pF	0.17ns
			D ↓	QN ↑	8.02ns/pF	0.51ns	1.88ns/pF	0.43ns
			D ↑	QN ↓	4.32ns/pF	1.54ns	1.30ns/pF	0.59ns
TBDIH	7	8	CK ↑	QN ↓	1.47ns/pF	0.47ns	0.68ns/pF	0.32ns
			CK ↑	QN ↑	2.05ns/pF	0.77ns	0.83ns/pF	0.39ns
			D ↓	QN ↑	5.13ns/pF	0.79ns	1.43ns/pF	0.20ns
			D ↑	QN ↓	3.25ns/pF	1.27ns	1.12ns/pF	0.40ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Tri-State Bus Driver — TBUS

The TBUS cells are tri-statable buffers. These cells are intended for internal bus structures.

A high power TBUS cell is available. The suffix of *H* indicates high power (2x).

Inputs
D,CK,CKN

Outputs
Q

Truth Table

INPUTS			OUTPUT
D	CK	CKN	Q
0	X	0	0
1	1	X	1
X	0	1	High Impedance

Capacitances

	TBUS			TBUSH		
	D	CK	CKN	D	CK	CKN
Area	0.071pF	0.035pF	0.036pF	0.071pF	0.035pF	0.036pF
Perf	0.296pF	0.146pF	0.147pF	0.296pF	0.146pF	0.147pF

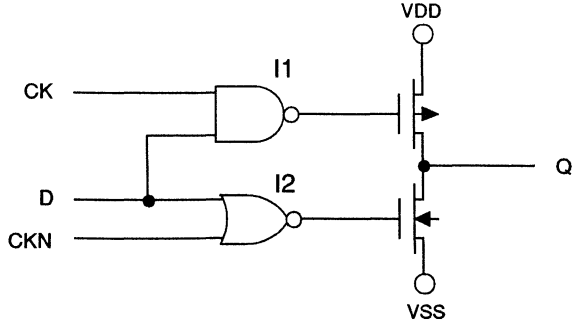
6

Cell Size and Delay Information

Cell	Grids	Transistors	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
TBUS	7	10	CK ↑	Q ↓	1.69ns/pF	0.94ns	0.42ns/pF	0.43ns
			CK ↑	Q ↑	4.50ns/pF	1.84ns	0.76ns/pF	0.74ns
			D ↓	Q ↓	1.69ns/pF	0.94ns	0.42ns/pF	0.43ns
			D ↑	Q ↑	4.50ns/pF	1.03ns	0.76ns/pF	0.55ns
TBUSH	7	12	CK ↑	Q ↓	1.43ns/pF	1.06ns	0.39ns/pF	0.50ns
			CK ↑	Q ↑	3.92ns/pF	1.96ns	0.68ns/pF	0.85ns
			D ↓	Q ↓	1.43ns/pF	1.06ns	0.39ns/pF	0.50ns
			D ↑	Q ↑	3.92ns/pF	1.15ns	0.68ns/pF	0.66ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Tri-State Bus Driver TBUSI

The TBUSI cells are tri-statable inverting buffers and are intended for internal bus structures.

A high power TBUSI cell is available. The suffix of *H* indicates high power (2x).

Inputs
D,CK,CKN

Outputs
Q

Truth Table

INPUTS			OUTPUT
D	CK	CKN	Q
0	1	X	1
1	X	0	0
X	0	1	High Impedance

Capacitances

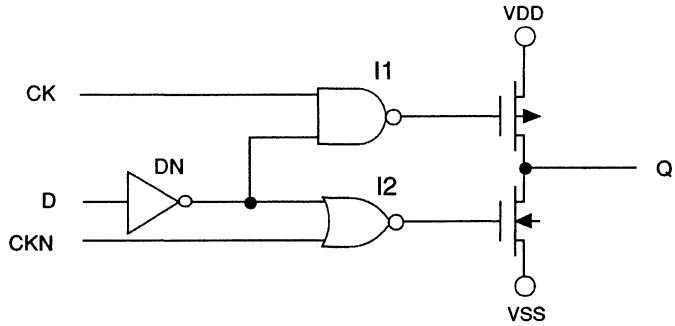
	TBUSI			TBUSIH		
	D	CK	CKN	D	CK	CKN
Area	0.034pF	0.034pF	0.035pF	0.034pF	0.035pF	0.036pF
Perf	0.145pF	0.145pF	0.147pF	0.145pF	0.146pF	0.147pF

Cell Size and Delay Information

Cell	Grids	Transistors	From Input	To Output	Propagation Delay			
					Area		Performance	
					Extrinsic	Intrinsic	Extrinsic	Intrinsic
TBUSI	8	12	CK ↑	Q ↓	1.69ns/pF	0.84ns	0.42ns/pF	0.43ns
			CK ↑	Q ↑	4.46ns/pF	1.86ns	0.78ns/pF	0.67ns
			D ↓	Q ↑	4.50ns/pF	1.12ns	0.78ns/pF	0.72ns
			D ↑	Q ↓	1.69ns/pF	1.70ns	0.42ns/pF	0.91ns
TBUSIH	9	14	CK ↑	Q ↓	1.43ns/pF	1.06ns	0.39ns/pF	0.50ns
			CK ↑	Q ↑	3.92ns/pF	1.96ns	0.68ns/pF	0.85ns
			D ↓	Q ↑	3.92ns/pF	1.25ns	0.68ns/pF	0.90ns
			D ↑	Q ↓	1.43ns/pF	1.87ns	0.39ns/pF	0.93ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Transmission Gate

TG*n*

The TG cells contain one or more transmission gates whose outputs are connected to form a common bus output. The parameter *n* specifies the number of transmission gates and each transmission gate consists of both an N and P type transistor.

Example: TG2

Inputs

D1,D2,CK1,CK1N,CK2,CK2N

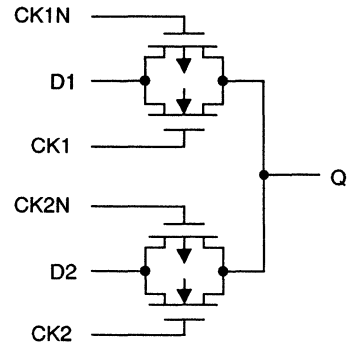
Outputs

Q

Truth Table

INPUTS						OUTPUT
D1	D2	CK1	CK1N	CK2	CK2N	Q
0	X	1	0	0	1	0
1	X	1	0	0	1	1
X	0	0	1	1	0	0
X	1	0	1	1	0	1
X	X	0	1	0	1	High Impedance

Motis Model



Capacitances

The input terminal capacitance for all TG cells is provided in the following table.

	D1,D2,D3	CK1,CK2,CK3	CK1N,CK2N,CK3N
Area	0.026pF	0.018pF	0.018pF
Perf.	0.048pF	0.036pF	0.051pF

Cell Size and Delay Information

Cell	Grids	Transistors	From Input	To Output	Propagation Delay			
					Area		Performance	
					Extrinsic	Intrinsic	Extrinsic	Intrinsic
TG1	4	2	CK ↑	Q ↓	1.52ns/pF	0.35ns	0.76ns/pF	0.17ns
			CK ↑	Q ↑	1.56ns/pF	1.00ns	0.76ns/pF	0.40ns
			D ↓	Q ↓	3.83ns/pF	0.09ns	1.17ns/pF	0.17ns
			D ↑	Q ↑	7.80ns/pF	0.70ns	2.01ns/pF	0.13ns
TG2	6	4	CK ↑	Q ↓	1.47ns/pF	0.47ns	0.76ns/pF	0.26ns
			CK ↑	Q ↑	1.56ns/pF	1.09ns	0.81ns/pF	0.36ns
			D ↓	Q ↓	3.66ns/pF	0.27ns	1.17ns/pF	0.27ns
			D ↑	Q ↑	7.89ns/pF	0.85ns	1.98ns/pF	0.30ns
TG3	9	6	CK ↑	Q ↓	1.52ns/pF	0.45ns	0.76ns/pF	0.26ns
			CK ↑	Q ↑	1.56ns/pF	1.14ns	0.81ns/pF	0.36ns
			D ↓	Q ↓	3.74ns/pF	0.23ns	1.20ns/pF	0.25ns
			D ↑	Q ↑	7.94ns/pF	0.98ns	1.98ns/pF	0.34ns

VDD=5V, T=25°C, Nominal Process.

Exclusive Nor

XNOR

The XNOR and XNORH cells provide the EXCLUSIVE NOR function. Additionally, since two gates are required for the XNOR function the NAND of the inputs is also provided as an output. The suffix of *H* on the XNORH indicates high power (2x).

Inputs
A,B

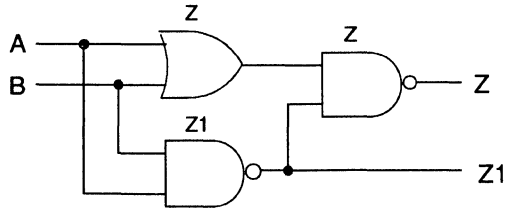
Outputs
Z,Z1

Logic Equations

$$Z = (A * B) + (\overline{A} * \overline{B})$$

$$Z1 = \overline{(A * B)}$$

Motis Model



Capacitances

	XNOR		XNORH	
	A	B	A	B
Area	0.073pF	0.073pF	0.140pF	0.135pF
Perf	0.299pF	0.302pF	0.591pF	0.586pF

Cell Size and Delay Information

Cell	Grids	Transistors	From Input	To Output	Propagation Delay			
					Area		Performance	
					Extrinsic	Intrinsic	Extrinsic	Intrinsic
XNOR	7	10	A ↓	Z ↓	9.27ns/pF	1.12ns	1.54ns/pF	0.84ns
			A ↓	Z ↑	6.73ns/pF	0.53ns	1.23ns/pF	0.27ns
			A ↓	Z1 ↑	3.74ns/pF	0.57ns	0.68ns/pF	0.32ns
			A ↑	Z ↓	4.15ns/pF	1.43ns	1.25ns/pF	0.20ns
			A ↑	Z ↑	8.96ns/pF	1.79ns	1.88ns/pF	0.71ns
			A ↑	Z1 ↓	4.01ns/pF	1.45ns	0.89ns/pF	0.54ns
			B ↓	Z ↓	9.27ns/pF	1.12ns	1.54ns/pF	0.84ns
			B ↓	Z ↑	6.73ns/pF	0.53ns	1.23ns/pF	0.27ns
			B ↓	Z1 ↑	3.74ns/pF	0.57ns	0.68ns/pF	0.32ns
			B ↑	Z ↓	4.15ns/pF	1.43ns	1.25ns/pF	0.20ns
			B ↑	Z ↑	8.96ns/pF	1.79ns	1.88ns/pF	0.71ns
			B ↑	Z1 ↓	4.01ns/pF	1.45ns	0.89ns/pF	0.54ns
XNORH	11	20	A ↓	Z ↓	4.46ns/pF	0.91ns	0.89ns/pF	0.40ns
			A ↓	Z ↑	3.39ns/pF	0.44ns	0.63ns/pF	0.22ns
			A ↓	Z1 ↑	1.92ns/pF	0.50ns	0.34ns/pF	0.30ns
			A ↑	Z ↓	2.27ns/pF	1.15ns	0.50ns/pF	0.37ns
			A ↑	Z ↑	4.77ns/pF	1.38ns	0.96ns/pF	0.67ns
			A ↑	Z1 ↓	2.18ns/pF	1.24ns	0.47ns/pF	0.49ns
			B ↓	Z ↓	4.46ns/pF	0.91ns	0.89ns/pF	0.40ns
			B ↓	Z ↑	3.39ns/pF	0.44ns	0.63ns/pF	0.22ns
			B ↓	Z1 ↑	1.92ns/pF	0.50ns	0.34ns/pF	0.30ns
			B ↑	Z ↓	2.27ns/pF	1.15ns	0.50ns/pF	0.37ns
			B ↑	Z ↑	4.77ns/pF	1.38ns	0.96ns/pF	0.67ns
			B ↑	Z1 ↓	2.18ns/pF	1.24ns	0.47ns/pF	0.49ns

VDD=5V, T=25°C, Nominal Process.

Exclusive Or

XOR

The XOR and XORH cells provide the EXCLUSIVE OR function. Additionally, since two gates are required for the XOR function the NOR of the inputs is also provided as an output. The suffix of *H* on the XORH indicates high power (2x).

Inputs
A,B

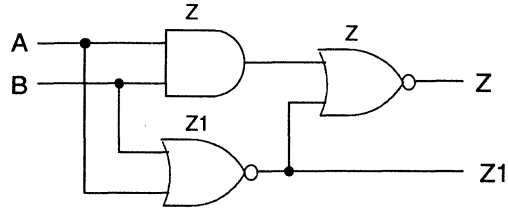
Outputs
Z,Z1

Logic Equations

$Z = (A * \overline{B}) + (\overline{A} * B)$

$Z1 = \overline{(A + B)}$

Motis Model



Capacitances

	XOR		XORH	
	A	B	A	B
Area	0.073pF	0.074pF	0.140pF	0.135pF
Perf	0.302pF	0.300pF	0.591pF	0.586pF

6

Cell Size and Delay Information

Cell	Grids	Transistors	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
XOR	7	10	A ↓	Z ↓	12.53ns/pF	1.77ns	2.61ns/pF	0.66ns
			A ↓	Z ↑	6.95ns/pF	0.43ns	1.30ns/pF	0.21ns
			A ↓	Z1 ↑	6.60ns/pF	0.64ns	1.20ns/pF	0.39ns
			A ↑	Z ↓	3.83ns/pF	1.58ns	0.91ns/pF	0.47ns
			A ↑	Z ↑	9.45ns/pF	1.90ns	1.82ns/pF	0.75ns
			A ↑	Z1 ↓	2.50ns/pF	1.48ns	0.52ns/pF	0.54ns
			B ↓	Z ↓	12.53ns/pF	1.77ns	2.61ns/pF	0.66ns
			B ↓	Z ↑	6.95ns/pF	0.43ns	1.30ns/pF	0.21ns
			B ↓	Z1 ↑	6.60ns/pF	0.64ns	1.20ns/pF	0.39ns
			B ↑	Z ↓	3.83ns/pF	1.58ns	0.91ns/pF	0.47ns
			B ↑	Z ↑	9.45ns/pF	1.90ns	1.82ns/pF	0.75ns
			B ↑	Z1 ↓	2.50ns/pF	1.48ns	0.52ns/pF	0.54ns
XORH	11	20	A ↓	Z ↓	6.78ns/pF	1.18ns	1.36ns/pF	0.50ns
			A ↓	Z ↑	3.39ns/pF	0.44ns	0.63ns/pF	0.22ns
			A ↓	Z1 ↑	3.30ns/pF	0.63ns	0.63ns/pF	0.32ns
			A ↑	Z ↓	2.36ns/pF	1.06ns	0.50ns/pF	0.37ns
			A ↑	Z ↑	4.99ns/pF	1.42ns	0.96ns/pF	0.57ns
			A ↑	Z1 ↓	1.47ns/pF	1.18ns	0.31ns/pF	0.42ns
			B ↓	Z ↓	6.78ns/pF	1.18ns	1.36ns/pF	0.50ns
			B ↓	Z ↑	3.39ns/pF	0.44ns	0.63ns/pF	0.22ns
			B ↓	Z1 ↑	3.30ns/pF	0.63ns	0.63ns/pF	0.32ns
			B ↑	Z ↓	2.36ns/pF	1.06ns	0.50ns/pF	0.37ns
			B ↑	Z ↑	4.99ns/pF	1.42ns	0.96ns/pF	0.57ns
			B ↑	Z1 ↓	1.47ns/pF	1.18ns	0.31ns/pF	0.42ns

VDD=5V, T=25°C, Nominal Process.

Flip-Flops

Section 7

AT&T

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Introduction

Flip-Flop Information

This section contains data sheets that provide detailed information on the Flip-Flops and Latches in the 1.25µ CMOS Library. What follows here is some background about the flip-flop family, and should help with the selection and use of these cells.

- There are 152 flip-flops, latches and registers described in this guide.
- Dynamic and Static storage elements are available. Dynamic registers are smaller, but they require a more complex clock generator and should not be used if static data retention is required.
- If scan-testing is to be used as a test strategy, many of the flip-flops have scan-test replacements available. Flip-flops that have scan-test replacements are indicated in the functional index that follows.
- A complete set of flip-flops have been provided for your use. Included in the 1.25µ CMOS Library are flip-flops and latches with all reasonable combinations of:
  - Presets (both polarities)
  - Clears (both polarities)
  - Sample inputs
  - Clock edge- or level-triggering (both polarities)

  Having a complete set of flip-flops and latches available means that you will always be able to find the cell you need, and will not need to tie off any unused inputs to either VSS or VDD. Synthesis tools (see for example FDS in Section 11) also realize improved efficiency. This saves silicon area and improves circuit performance.
- All static flip-flops and latches have both Q and QN available as outputs. This makes the library easy to use and avoids the need to add inverters to the flip-flops when inverted signals are required.
- Both area-optimized and performance-optimized versions of each cell are available. Thus, if your performance requirements do not tax the limits of the technology, you will be able to save some area by using the area-optimized library.

The convention for naming all of the sequential elements is shown in the following table. Each cell is identified via a seven-character name.

	Name = abcdefg	
a=	F	Static implementation.
	D	Dynamic implementation.
b=	B	These cells contain a BIST select front end for use with the built in self test methodology.
	D	D type Flip-Flop.
	L	These cells contain a scan select front end for use with the scan testable design methodology.
	R	Shift register implementation for D type function.
	S	S-R type Flip-Flop.
c=	value	Number of clocks, not the number of phases.
d=		This parameter identifies the sample capability separately for Static and Dynamic cells.
		Static Cells or *a=F.*
	S	No sample input.
	P	Positive level sample.
	N	Negative level sample.
		Dynamic cells or *a=D.*
	A	No sample input.
	B	Positive level sample.
	C	Negative level sample.
	D	Inverting Data with positive level sample.
	E	Inverting Data with negative level sample.
e=		When the cell has no clock inputs (c=0), this specifies the polarity of the S and R inputs. Otherwise, this refers to the clock inputs.
		Cells with no clock or *c=0.*
	1	Positive level S input and positive level R input.
	2	Negative level S input and negative level R input.
	7	Positive level S input and negative level R input.
	8	Negative level S input and positive level R input.
		Cells with clock inputs.
	1	Positive level sense or Master-Slave clock inputs.
	2	Negative edge triggered.
	3	Positive edge triggered.
	5	Negative level sense.

continued on next page.

(continued from previous page)

	Name = abcdefg	
f=	A	No clear or preset inputs.
	B	Positive level asynchronous preset.
	C	Positive level asynchronous preset and positive level asynchronous clear.
	D	Positive level asynchronous clear.
	E	Negative level asynchronous clear.
	F	Positive level asynchronous preset and negative level asynchronous clear.
	G	Negative level asynchronous preset.
	I	Positive level synchronous clear.
	J	Positive level synchronous preset.
	K	Negative level asynchronous preset and negative level asynchronous clear.
	L	Negative level synchronous preset.
	M	Negative level synchronous clear.
	N	Negative level asynchronous preset and positive level asynchronous clear.
	O	Positive level synchronous preset and positive level synchronous clear.
	P	Positive level synchronous preset and negative level synchronous clear.
	Q	Negative level synchronous preset and negative level synchronous clear.
	R	Negative level synchronous preset and positive level synchronous clear.
g=	X	This cell requires more than one connection for one or more of the inputs. This technique allows circuits designed with one library to be easily converted to any other library.

Example: FD1P3Q is a single clock positive edge triggered Static D type Flip-Flop with a positive level sample, a negative level synchronous preset and a negative level synchronous clear.

FD1P3Q	**a** =	F	Static cell.
	b =	D	D type.
	c =	1	Single clock.
	d =	P	Positive level sample.
	e =	3	Positive edge triggered.
	f =	Q	Synchronous negative level preset and synchronous negative level clear.

Example: DR2B1J is a Dynamic Master-Slave D type register with a positive level sample and a positive level synchronous preset.

DR2B1J	**a** =	D	Dynamic cell.
	b =	R	Shift register implementation for D type function.
	c =	2	Two clocks.
	d =	B	Positive level sample.
	e =	1	Master-Slave clocking.
	f =	J	Positive level synchronous preset.

The following pages tabulate the flip-flops, registers and latches into a functional index.

Dynamic Registers

Cell	Page	Grids	Transistors	Clocking	Preset	Clear	Sample	Scan Equivalent
DL2D1A	7-12	20	30	MS	--	--	PL	(DR2A1A)
DR2A1A	7-13	7	8	MS	--	--	--	--
DR2A1AH	7-14	8	10	MS	--	--	--	--
DR2A1B	7-15	13	18	MS	PL	--	--	--
DR2A1D	7-16	13	18	MS	--	PL	--	--
DR2A1E	7-17	13	18	MS	--	NL	--	--
DR2A1F	7-18	18	26	MS	PL	NL	--	--
DR2A1G	7-19	13	18	MS	NL	--	--	--
DR2A1I	7-20	10	14	MS	--	SPL	--	--
DR2A1J	7-21	12	12	MS	SPL	--	--	--
DR2A1M	7-22	12	12	MS	--	SNL	--	--
DR2A1N	7-23	18	26	MS	NL	PL	--	--
DR2B1A	7-24	12	18	MS	--	--	PL	--
DR2B1I	7-25	13	20	MS	--	SPL	PL	--
DR2B1J	7-26	13	20	MS	SPL	--	PL	--
DR2C1A	7-27	12	18	MS	--	--	NL	--
DR2C1I	7-28	13	20	MS	--	SPL	NL	--
DR2D1A	7-29	12	18	MS	--	--	PL	DL2D1A
DR2D1I	7-30	13	20	MS	--	SPL	PL	--
DR2E1A	7-31	12	18	MS	--	--	NL	--
DR2E1I	7-32	13	20	MS	--	SPL	NL	--

MS = Master-Slave, NL = Negative Level, PL = Positive Level,
SNL = Synchronous Negative Level, SPL = Synchronous Positive Level

Static Flip-Flops and Latches

Cell	Page	Grids	Transistors	Clocking	Preset	Clear	Sample	Scan Equivalent
FB1S2AX	7-33	23	36	NE	--	--	--	--
FB1S3AX	7-34	23	36	PE	--	--	--	--
FD1N2AX	7-35	19	26	NE	--	--	NL	FL1N2AX
FD1N2JX	7-36	21	32	NE	SPL	--	NL	FL1N2JX
FD1N2MX	7-37	21	32	NE	--	SNL	NL	FL1N2MX
FD1N3AX	7-38	19	26	PE	--	--	NL	FL1N3AX
FD1N3JX	7-39	21	32	PE	SPL	--	NL	FL1N3JX
FD1N3MX	7-40	21	32	PE	--	SNL	NL	FL1N3MX
FD1P2AX	7-41	19	26	NE	--	--	PL	FL1P2AX
FD1P2JX	7-42	21	32	NE	SPL	--	PL	FL1P2JX
FD1P2MX	7-43	21	32	NE	--	SNL	PL	FL1P2MX
FD1P3AX	7-44	19	26	PE	--	--	PL	FL1P3AX
FD1P3JX	7-45	21	32	PE	SPL	--	PL	FL1P3JX
FD1P3MX	7-46	21	32	PE	--	SNL	PL	FL1P3MX
FD1S1A	7-47	9	10	PL	--	--	--	--
FD1S1B	7-48	9	12	PL	PL	--	--	--
FD1S1D	7-49	10	14	PL	--	PL	--	--
FD1S1E	7-50	9	12	PL	--	NL	--	--
FD1S1F	7-51	11	14	PL	PL	NL	--	--
FD1S1G	7-52	10	14	PL	NL	--	--	--
FD1S2AX	7-53	13	18	NE	--	--	--	FL1S2AX
FD1S2BX	7-54	16	22	NE	PL	--	--	FL1S2BX
FD1S2CX	7-55	21	28	NE	PL	PL	--	FL1S2CX
FD1S2DX	7-56	17	24	NE	--	PL	--	FL1S2DX
FD1S2EX	7-57	16	22	NE	--	NL	--	FL1S2EX
FD1S2FX	7-58	19	26	NE	PL	NL	--	FL1S2FX
FD1S2GX	7-59	17	24	NE	NL	--	--	FL1S2GX
FD1S2IX	7-60	18	24	NE	--	SPL	--	FL1S2IX
FD1S2JX	7-61	16	22	NE	SPL	--	--	FL1S2JX
FD1S2KX	7-62	22	30	NE	NL	NL	--	FL1S2KX
FD1S2LX	7-63	18	24	NE	SNL	--	--	FL1S2LX
FD1S2MX	7-64	15	22	NE	--	SNL	--	FL1S2MX
FD1S2NX	7-65	20	28	NE	NL	PL	--	FL1S2NX
FD1S2OX	7-66	19	26	NE	SPL	SPL	--	FL1S2OX
FD1S3AX	7-67	13	18	PE	--	--	--	FL1S3AX
FD1S3BX	7-68	16	22	PE	PL	--	--	FL1S3AX
FD1S3CX	7-69	21	28	PE	PL	PL	--	FL1S3AX
FD1S3DX	7-70	17	24	PE	--	PL	--	FL1S3AX
FD1S3EX	7-71	16	22	PE	--	NL	--	FL1S3AX
FD1S3FX	7-72	19	26	PE	PL	NL	--	FL1S3AX
FD1S3GX	7-73	17	24	PE	NL	--	--	FL1S3AX
FD1S3IX	7-74	18	24	PE	--	SPL	--	FL1S3AX
FD1S3JX	7-75	16	22	PE	SPL	--	--	FL1S3AX
FD1S3KX	7-76	22	30	PE	NL	NL	--	FL1S3AX

MS = Master-Slave, NE = Negative Edge Triggered, NL = Negative Level,
PE = Positive Edge Triggered, PL = Positive Level,
SNL = Synchronous Negative Level, SPL = Synchronous Positive Level

Static Flip-Flops and Latches

Cell	Page	Grids	Transistors	Clocking	Preset	Clear	Sample	Scan Equivalent
FD1S3LX	7-77	18	24	PE	SNL	--	--	FL1S3AX
FD1S3MX	7-78	15	22	PE	--	SNL	--	FL1S3AX
FD1S3NX	7-79	20	28	PE	NL	PL	--	FL1S3AX
FD1S3OX	7-80	19	26	PE	SPL	SPL	--	FL1S3AX
FD1S5A	7-81	9	10	NL	--	--	--	--
FD1S5B	7-82	9	12	NL	PL	--	--	--
FD1S5D	7-83	10	14	NL	--	PL	--	--
FD1S5E	7-84	9	12	NL	--	NL	--	--
FD1S5F	7-85	11	14	NL	PL	NL	--	--
FD1S5G	7-86	10	14	NL	NL	--	--	--
FD2N1A	7-87	20	28	MS	--	--	NL	--
FD2N1J	7-88	23	34	MS	SPL	--	NL	--
FD2N1M	7-89	23	34	MS	--	SNL	NL	--
FD2P1A	7-90	20	28	MS	--	--	PL	--
FD2P1J	7-91	23	34	MS	SPL	--	PL	--
FD2P1M	7-92	23	34	MS	--	SNL	PL	--
FD2S1A	7-93	14	20	MS	--	--	--	FL2S1A
FD2S1B	7-94	17	24	MS	PL	--	--	FL2S1B
FD2S1CX	7-95	20	30	MS	PL	PL	--	FL2S1CX
FD2S1D	7-96	18	26	MS	--	PL	--	FL2S1D
FD2S1E	7-97	17	24	MS	--	NL	--	FL2S1E
FD2S1FX	7-98	19	28	MS	PL	NL	--	FL2S1FX
FD2S1G	7-99	18	26	MS	NL	--	--	FL2S1G
FD2S1I	7-100	17	26	MS	--	SPL	--	FL2S1I
FD2S1J	7-101	16	24	MS	SPL	--	--	FL2S1J
FD2S1KX	7-102	21	32	MS	NL	NL	--	FL2S1KX
FD2S1L	7-103	17	26	MS	SNL	--	--	FL2S1L
FD2S1M	7-104	16	24	MS	--	SNL	--	FL2S1M
FD2S1NX	7-105	20	30	MS	NL	PL	--	FL2S1NX
FL1N2AX	7-106	26	36	NE	--	--	NL	(FD1N2AX)
FL1N2JX	7-107	27	38	NE	SPL	--	NL	(FD1N2JX)
FL1N2MX	7-108	27	38	NE	--	SNL	NL	(FD1N2MX)
FL1N3AX	7-109	26	36	PE	--	--	NL	(FD1N3AX)
FL1N3JX	7-110	27	38	PE	SPL	--	NL	(FD1N3JX)
FL1N3MX	7-111	27	38	PE	--	SNL	NL	(FD1N3MX)
FL1P2AX	7-112	26	36	NE	--	--	PL	(FD1P2AX)
FL1P2JX	7-113	27	38	NE	SPL	--	PL	(FD1P2JX)
FL1P2MX	7-114	27	38	NE	--	SNL	PL	(FD1P2MX)
FL1P3AX	7-115	26	36	PE	--	--	PL	(FD1P3AX)
FL1P3JX	7-116	27	38	PE	SPL	--	PL	(FD1P3JX)
FL1P3MX	7-117	27	38	PE	--	SNL	PL	(FD1P3MX)
FL1S2AX	7-118	19	30	NE	--	--	--	(FD1S2AX)
FL1S2BX	7-119	22	34	NE	PL	--	--	(FD1S2BX)
FL1S2CX	7-120	28	40	NE	PL	PL	--	(FD1S2CX)

MS = Master-Slave, NE = Negative Edge Triggered, NL = Negative Level,
PE = Positive Edge Triggered, PL = Positive Level,
SNL = Synchronous Negative Level, SPL = Synchronous Positive Level

Static Flip-Flops and Latches

Cell	Page	Grids	Transistors	Clocking	Preset	Clear	Sample	Scan Equivalent
FL1S2DX	7-121	22	32	NE	--	PL	--	(FD1S2DX)
FL1S2EX	7-122	22	34	NE	--	NL	--	(FD1S2EX)
FL1S2FX	7-123	25	38	NE	PL	NL	--	(FD1S2FX)
FL1S2GX	7-124	22	32	NE	NL	--	--	(FD1S2GX)
FL1S2IX	7-125	23	32	NE	--	SPL	--	(FD1S2IX)
FL1S2JX	7-126	21	30	NE	SPL	--	--	(FD1S2JX)
FL1S2KX	7-127	27	38	NE	NL	NL	--	(FD1S2KX)
FL1S2LX	7-128	23	32	NE	SNL	--	--	(FD1S2LX)
FL1S2MX	7-129	20	30	NE	--	SNL	--	(FD1S2MX)
FL1S2NX	7-130	25	36	NE	NL	PL	--	(FD1S2NX)
FL1S2OX	7-131	24	34	NE	SPL	SPL	--	(FD1S2OX)
FL1S3AX	7-132	19	30	PE	--	--	--	(FD1S3AX)
FL1S3BX	7-133	22	34	PE	PL	--	--	(FD1S3BX)
FL1S3CX	7-134	28	40	PE	PL	PL	--	(FD1S3CX)
FL1S3DX	7-135	22	32	PE	--	PL	--	(FD1S3DX)
FL1S3EX	7-136	22	34	PE	--	NL	--	(FD1S3EX)
FL1S3FX	7-137	25	38	PE	PL	NL	--	(FD1S3FX)
FL1S3GX	7-138	22	32	PE	NL	--	--	(FD1S3GX)
FL1S3IX	7-139	23	32	PE	--	SPL	--	(FD1S3IX)
FL1S3JX	7-140	21	30	PE	SPL	--	--	(FD1S3JX)
FL1S3KX	7-141	27	38	PE	NL	NL	--	(FD1S3KX)
FL1S3LX	7-142	23	32	PE	SNL	--	--	(FD1S3LX)
FL1S3MX	7-143	20	30	PE	--	SNL	--	(FD1S3MX)
FL1S3NX	7-144	25	36	PE	NL	PL	--	(FD1S3NX)
FL1S3OX	7-145	24	34	PE	SPL	SPL	--	(FD1S3OX)
FL2S1A	7-146	20	32	MS	--	--	--	(FD2S1A)
FL2S1B	7-147	23	36	MS	PL	--	--	(FD2S1A)
FL2S1CX	7-148	26	42	MS	PL	PL	--	(FD2S1AX)
FL2S1D	7-149	23	34	MS	--	PL	--	(FD2S1A)
FL2S1E	7-150	23	36	MS	--	NL	--	(FD2S1A)
FL2S1FX	7-151	25	40	MS	PL	NL	--	(FD2S1AX)
FL2S1G	7-152	23	34	MS	NL	--	--	(FD2S1A)
FL2S1I	7-153	23	34	MS	--	SPL	--	(FD2S1A)
FL2S1J	7-154	21	32	MS	SPL	--	--	(FD2S1A)
FL2S1KX	7-155	26	40	MS	NL	NL	--	(FD2S1AX)
FL2S1L	7-156	23	34	MS	SNL	--	--	(FD2S1A)
FL2S1M	7-157	21	32	MS	--	SNL	--	(FD2S1A)
FL2S1NX	7-158	25	38	MS	NL	PL	--	(FD2S1AX)
FS0S1A	7-159	5	8	--	--	--	--	--
FS0S1D	7-160	6	10	--	--	PL	--	--
FS0S7A	7-161	5	8	--	--	--	--	--
FS1S1A	7-162	7	12	PL	--	--	--	--
FS1S3A	7-163	15	24	PE	--	--	--	--

MS = Master-Slave, NE = Negative Edge Triggered, NL = Negative Level,
PE = Positive Edge Triggered, PL = Positive Level,
SNL = Synchronous Negative Level, SPL = Synchronous Positive Level

If we turn to the FD1S2AX as an example, the following setup and propagation delay information has been provided on page 7-53.

Delay Information - FD1S2AX

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	0.67ns	0.57ns	CK ↑	Q ↓	1.96ns/pF	1.20ns	0.47ns/pF	0.82ns
D ↑	1.67ns	0.86ns	CK ↑	Q ↑	3.61ns/pF	1.15ns	0.65ns/pF	0.77ns
			CK ↑	QN ↓	8.92ns/pF	1.34ns	1.67ns/pF	0.88ns
			CK ↑	QN ↑	6.55ns/pF	1.28ns	1.36ns/pF	0.88ns

VDD=5V, T=25°C, Nominal Process.

NOTE:

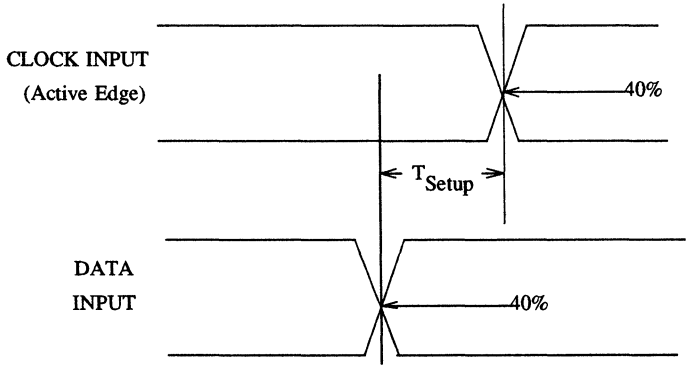
1) *Both Q and QN were equally loaded when this delay information was calculated.*
2) *When calculating estimated delay values, remember to include estimated routing capacitance. A value of 0.12pF per fanout is the autorout suggested for simulation. See section 6 for a detailed description of how the delay information was calculated.*

IMPORTANT NOTE:

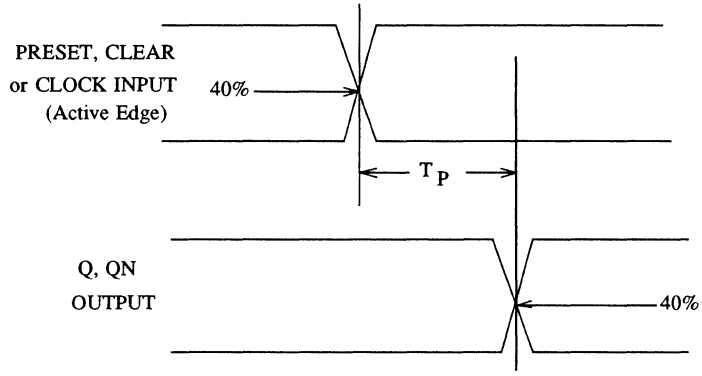
3) ***The signal name CK refers to the common connection of CKA and CKB. The X suffix in any cell name indicates that some input signals require more than one connection to the cell. The Delay and Truth tables always refer to the common connection of these inputs.***

A similar delay table is provided for all 152 flip-flops, registers and latches described in this section.

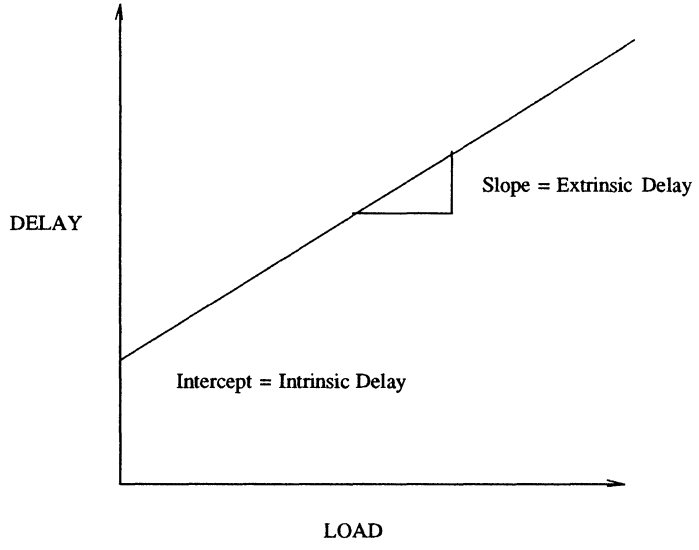
The set-up times in the delay information tables are measured according to the following diagram:



Similarly, the delays from CLOCK, asynchronous PRESET or asynchronous CLEAR to OUTPUT is measured according to the following diagram:



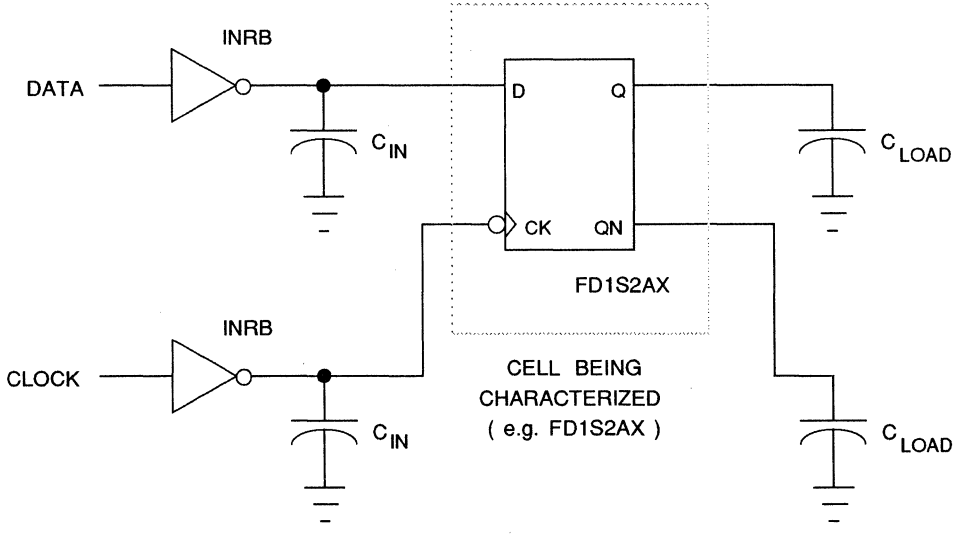
As with the logic cells, both intrinsic and extrinsic delays are specified for the output propagation delays. In graphical terms, they have the following meaning:



In physical terms, the *intrinsic* delay represents the *zero-load* delay of the output stage. The *extrinsic* delay is related to the cell's output impedance, and is a measure of how the delay of the cell will vary under different loading conditions.

As with the logic cells, MOTIS3 was used to characterize the flip-flops and latches to prepare the delay information tables in this catalog. The methodology used was very similar: two sets of simulations for each flip-flop were performed - one with a fan-out of 3, and another with a fan-out of 10. The two delay values were then used to obtain a line intercept (an intrinsic delay) and slope (an extrinsic delay.) (See pages 6-4 to 6-9 for a more detailed description of the cell characterization methodology.)

The circuit used for characterization is illustrated below:



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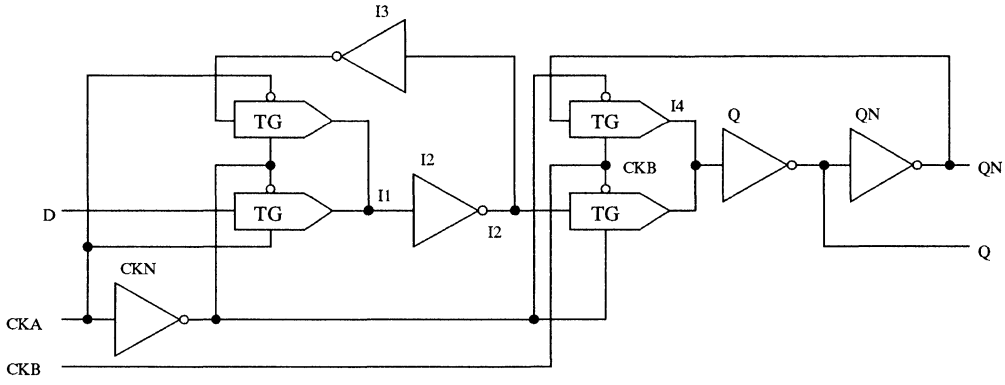
IMPORTANT NOTE:

The signal name CK refers to the common connection of CKA and CKB. The X suffix in any cell name indicates that some input signals require more than one connection to the cell. The Delay and Truth tables always refer to the common connection of these inputs.

Notice that both Q and QN were loaded with CLOAD during the characterization. This is a conservative approach because in most flip-flops, Q and QN are directly related to one another. This can be seen in the schematic of the FD1S2AX, below:



In this case, QN is an inverted version of Q. As the load on Q increases, the CK→QN delay will increase even if there is no load on QN. Thus, characterization of the FD1S2AX with identical loading on both Q and QN makes the CK→QN delay increase much more quickly than if you were to increase the load on either Q or QN alone.

If we return to the delay information table for the FD1S2AX it can be seen that the effect of loading both Q and QN is reflected in both the intrinsic and extrinsic delay values for this cell.

The intrinsic and extrinsic delays for the area-optimized FD1S2AX can be used to write the characteristic CK→Q and CK→QN delay equations:

$T_{CK \rightarrow Q\uparrow}$ = 1.15ns + (3.61ns/pF) times the total load in picofarads

$T_{CK \rightarrow Q\downarrow}$ = 1.20ns + (1.96ns/pF) times the total load in picofarads

$T_{CK \rightarrow QN\uparrow}$ = 1.28ns + (6.55ns/pF) times the total load in picofarads

$T_{CK \rightarrow QN\downarrow}$ = 1.66ns + (8.92ns/pF) times the total load in picofarads

The intrinsic and extrinsic delays for the performance-optimized FD1S2AX can be used in a similar set of equations.

The characteristic equations can be used to estimate the output delay of flip-flops, registers and latches. An example of their use is detailed on Pages 6-4 to 6-9.

Dynamic Shift Register

DL2D1A

Master-Slave clocking, data select front end, inverting data with positive level sample.

Grids 20, **Transistors** 30

Inputs
D0,D1N,SP,MCK,MCKN,SCK,SCKN,SD

Outputs
Q

Truth Table

INPUTS						OUTPUTS	
						OLD	NEW
D0	D1N	SP	MCK	SCK	SD	Q	Q
X	X	0	↓	↑	1	0	0
X	X	0	↓	↑	1	1	1
0	X	X	↓	↑	0	X	0
1	X	X	↓	↑	0	X	1
X	1	1	↓	↑	1	X	0
X	0	1	↓	↑	1	X	1

X = Don't care

Capacitances

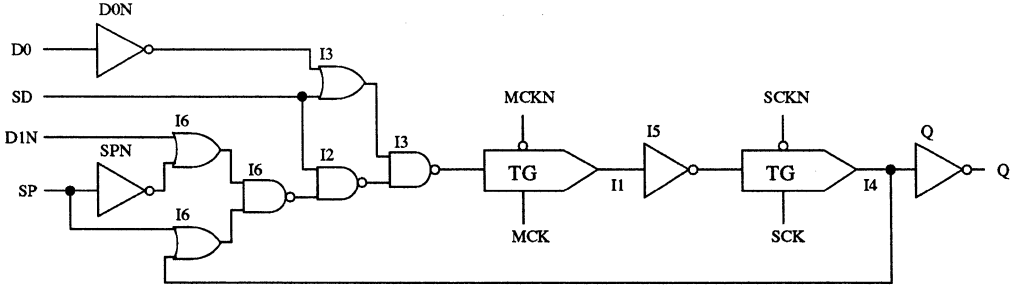
	D0	D1N	SP	MCK	MCKN	SCK	SCKN	SD
Area	0.034pF	0.034pF	0.066pF	0.018pF	0.018pF	0.018pF	0.018pF	0.070pF
Perf	0.145pF	0.145pF	0.291pF	0.036pF	0.051pF	0.036pF	0.051pF	0.295pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	1.24ns	0.81ns	SCKN ↓	Q ↓	2.01ns/pF	0.70ns	0.52ns/pF	0.69ns
D0 ↑	1.91ns	1.14ns	SCKN ↓	Q ↑	3.66ns/pF	0.32ns	0.70ns/pF	0.59ns
D1N ↓	2.29ns	1.43ns						
D1N ↑	2.05ns	1.29ns						
SD ↓	1.29ns	0.81ns						
SD ↑	1.91ns	1.14ns						
SP ↓	2.29ns	1.43ns						
SP ↑	2.86ns	1.76ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Dynamic Shift Register — DR2A1A

Master-Slave clocking.

Grids 7, **Transistors** 8

Inputs
D,MCK,MCKN,SCK,SCKN

Outputs
Q

Truth Table

INPUTS			OUTPUTS	
			OLD	NEW
D	MCK	SCK	Q	Q
0	↓	↑	X	0
1	↓	↑	X	1

X = Don't care

Capacitances

	D	MCK	MCKN	SCK	SCKN
Area	0.026pF	0.018pF	0.018pF	0.018pF	0.018pF
Perf	0.048pF	0.036pF	0.051pF	0.036pF	0.051pF

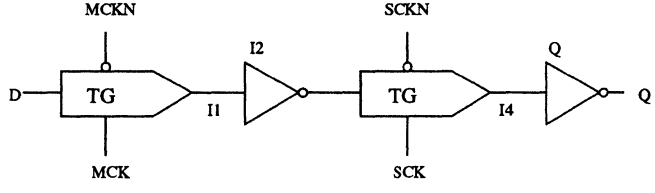
7

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	0.10ns	0.19ns	SCKN ↓	Q ↓	1.96ns/pF	0.43ns	0.50ns/pF	0.42ns
D ↑	1.05ns	0.48ns	SCKN ↓	Q ↑	3.66ns/pF	0.23ns	0.68ns/pF	0.37ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Dynamic Shift Register — DR2A1AH

Master-Slave clocking.

Grids 8, **Transistors** 10

Inputs
D,MCK,MCKN,SCK,SCKN

Outputs
Q

Truth Table

INPUTS			OUTPUTS	
			OLD	NEW
D	MCK	SCK	Q	Q
0	↓	↑	X	0
1	↓	↑	X	1

X = Don't care

Capacitances

	D	MCK	MCKN	SCK	SCKN
Area	0.026pF	0.018pF	0.018pF	0.018pF	0.018pF
Perf	0.048pF	0.036pF	0.051pF	0.036pF	0.051pF

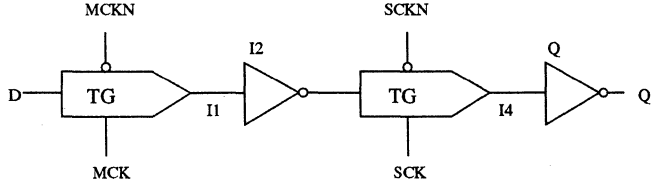
7

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	0.10ns	0.19ns	SCKN ↓	Q ↓	0.98ns/pF	0.65ns	0.29ns/pF	0.58ns
D ↑	1.05ns	0.48ns	SCKN ↓	Q ↑	1.83ns/pF	0.21ns	0.34ns/pF	0.50ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Dynamic Shift Register — DR2A1B

Master-Slave clocking, positive asynchronous preset.

Grids 13, **Transistors** 18

Inputs
D,MCK,MCKN,SCK,SCKN,PD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	MCK	SCK	PD	Q	QN	Q	QN
X	X	X	1	X	X	1	0
0	↓	↑	0	X	X	0	1
1	↓	↑	X	X	X	1	0

X = Don't care

Capacitances

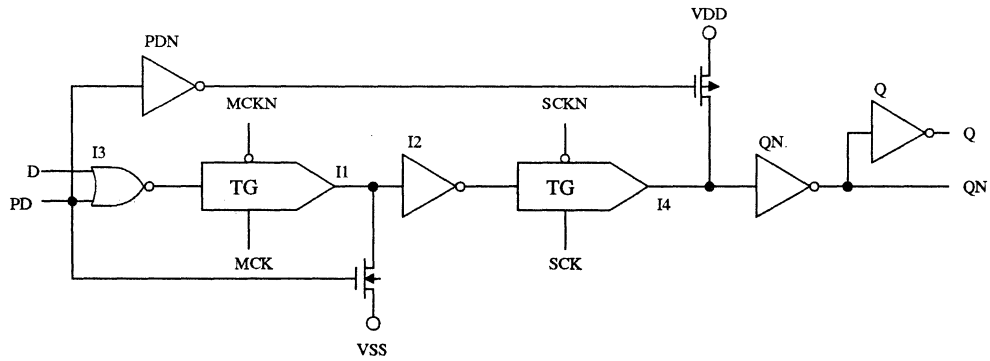
	D	MCK	MCKN	SCK	SCKN	PD
Area	0.034pF	0.018pF	0.018pF	0.018pF	0.018pF	0.091pF
Perf	0.145pF	0.036pF	0.051pF	0.036pF	0.051pF	0.333pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.43ns	0.86ns	PD ↑	Q ↑	6.51ns/pF	1.63ns	1.36ns/pF	1.12ns
D ↑	1.14ns	0.62ns	PD ↑	QN ↓	1.96ns/pF	1.53ns	0.47ns/pF	1.06ns
			SCKN ↓	Q ↓	10.39ns/pF	2.81ns	1.98ns/pF	1.44ns
			SCKN ↓	Q ↑	6.51ns/pF	0.87ns	1.36ns/pF	0.79ns
			SCKN ↓	QN ↓	1.96ns/pF	0.77ns	0.47ns/pF	0.73ns
			SCKN ↓	QN ↑	5.13ns/pF	2.60ns	0.96ns/pF	1.34ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Dynamic Shift Register — DR2A1D

Master-Slave clocking, positive asynchronous clear.

Grids 13, **Transistors** 18

Inputs
D,MCK,MCKN,SCK,SCKN,CD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	MCK	SCK	CD	Q	QN	Q	QN
X	X	X	1	X	X	0	1
0	↓	↑	X	X	X	0	1
1	↓	↑	0	X	X	1	0

X = Don't care

Capacitances

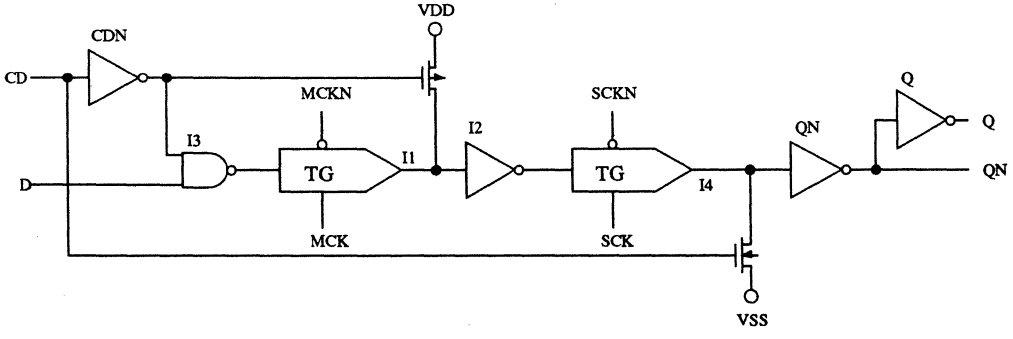
	D	MCK	MCKN	SCK	SCKN	CD
Area	0.034pF	0.018pF	0.018pF	0.018pF	0.018pF	0.056pF
Perf	0.145pF	0.036pF	0.051pF	0.036pF	0.051pF	0.184pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D ↓	0.91ns	0.62ns	CD ↑	Q ↓	8.92ns/pF	4.06ns	1.67ns/pF	1.93ns
D ↑	1.34ns	0.81ns	CD ↑	QN ↑	3.66ns/pF	3.85ns	0.65ns/pF	1.82ns
			SCKN ↓	Q ↓	8.92ns/pF	0.57ns	1.67ns/pF	0.64ns
			SCKN ↓	Q ↑	6.73ns/pF	1.29ns	1.54ns/pF	1.17ns
			SCKN ↓	QN ↓	2.18ns/pF	1.19ns	0.65ns/pF	1.11ns
			SCKN ↓	QN ↑	3.66ns/pF	0.37ns	0.65ns/pF	0.53ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Dynamic Shift Register — DR2A1E

Master-Slave clocking, negative asynchronous clear.

Grids 13, **Transistors** 18

Inputs
D,MCK,MCKN,SCK,SCKN,CDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	MCK	SCK	CDN	Q	QN	Q	QN
X	X	X	0	X	X	0	1
0	↓	↑	X	X	X	0	1
1	↓	↑	1	X	X	1	0

X = Don't care

Capacitances

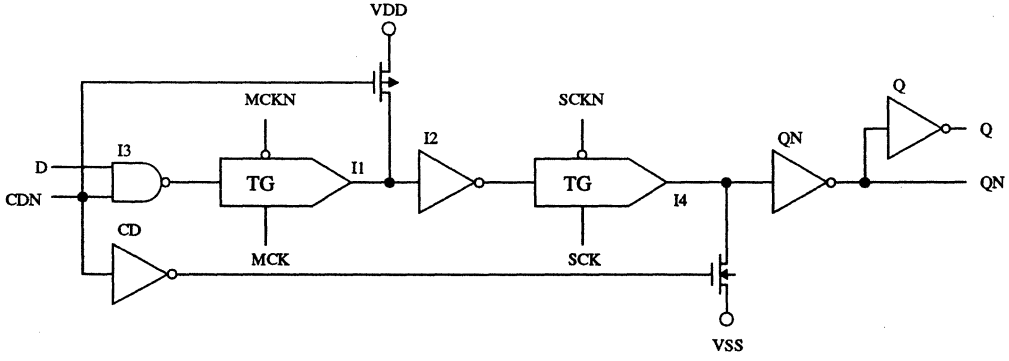
	D	MCK	MCKN	SCK	SCKN	CDN
Area	0.034pF	0.018pF	0.018pF	0.018pF	0.018pF	0.091pF
Perf	0.145pF	0.036pF	0.051pF	0.036pF	0.051pF	0.346pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
D ↓	0.91ns	0.62ns	CDN ↓	Q ↓	8.92ns/pF	1.48ns	1.67ns/pF	1.16ns
D ↑	1.34ns	0.81ns	CDN ↓	QN ↑	3.66ns/pF	1.28ns	0.65ns/pF	1.06ns
			SCKN ↓	Q ↓	8.92ns/pF	0.57ns	1.67ns/pF	0.64ns
			SCKN ↓	Q ↑	6.73ns/pF	1.29ns	1.54ns/pF	1.17ns
			SCKN ↓	QN ↓	2.18ns/pF	1.19ns	0.65ns/pF	1.11ns
			SCKN ↓	QN ↑	3.66ns/pF	0.37ns	0.65ns/pF	0.53ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Dynamic Shift Register

DR2A1F

Master-Slave clocking, negative asynchronous clear, positive asynchronous preset.

Grids 18, **Transistors** 26

Inputs

D,MCK,MCKN,SCK,SCKN,PD,CDN

Outputs

Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D	MCK	SCK	PD	CDN	Q	QN	Q	QN
X	X	X	1	X	X	X	1	0
X	X	X	0	0	X	X	0	1
0	↓	↑	0	X	X	X	0	1
1	↓	↑	X	1	X	X	1	0

X = Don't care

Capacitances

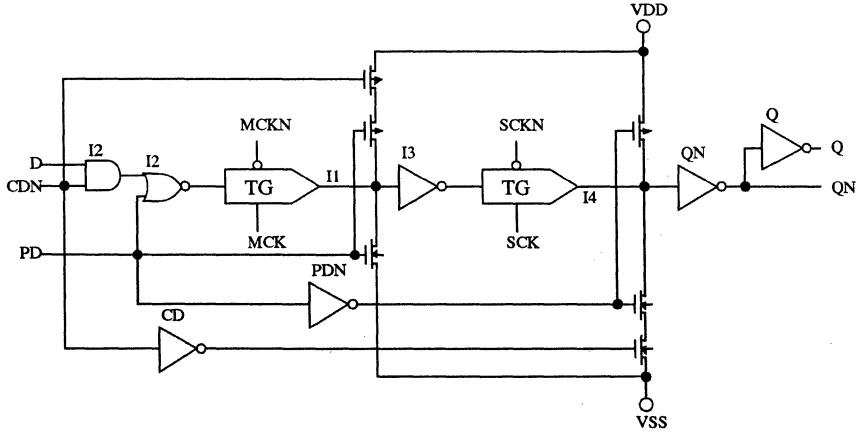
	D	MCK	MCKN	SCK	SCKN	PD	CDN
Area	0.034pF	0.018pF	0.018pF	0.018pF	0.018pF	0.112pF	0.103pF
Perf	0.145pF	0.036pF	0.051pF	0.036pF	0.051pF	0.430pF	0.362pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.62ns	1.14ns	CDN ↓	Q ↓	8.92ns/pF	1.72ns	1.72ns/pF	1.31ns
D ↑	1.48ns	0.91ns	CDN ↓	QN ↑	3.66ns/pF	1.51ns	0.70ns/pF	1.21ns
			PD ↑	Q ↑	6.55ns/pF	1.76ns	1.38ns/pF	1.15ns
			PD ↑	QN ↓	2.01ns/pF	1.65ns	0.50ns/pF	1.09ns
			SCKN ↓	Q ↓	8.92ns/pF	0.67ns	1.72ns/pF	0.69ns
			SCKN ↓	Q ↑	6.55ns/pF	0.90ns	1.38ns/pF	0.86ns
			SCKN ↓	QN ↓	2.01ns/pF	0.79ns	0.50ns/pF	0.80ns
			SCKN ↓	QN ↑	3.66ns/pF	0.46ns	0.70ns/pF	0.59ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Dynamic Shift Register — DR2A1G

Master-Slave clocking, negative asynchronous preset.

Grids 13, **Transistors** 18

Inputs
D,MCK,MCKN,SCK,SCKN,PDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	MCK	SCK	PDN	Q	QN	Q	QN
X	X	X	0	X	X	1	0
0	↓	↑	1	X	X	0	1
1	↓	↑	X	X	X	1	0

X = Don't care

Capacitances

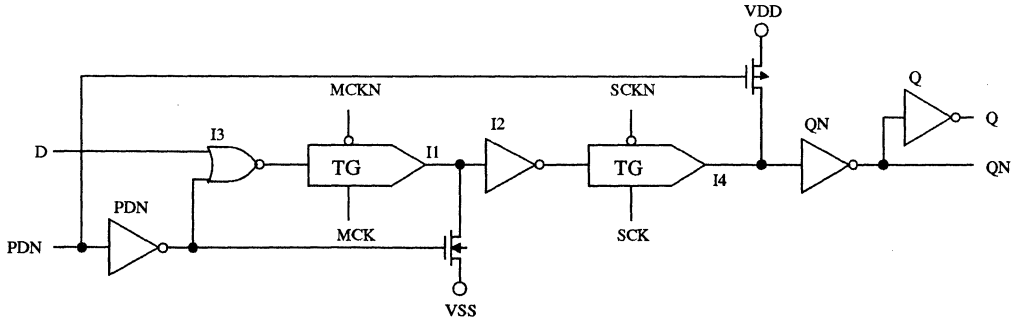
	D	MCK	MCKN	SCK	SCKN	PDN
Area	0.034pF	0.018pF	0.018pF	0.018pF	0.018pF	0.056pF
Perf	0.145pF	0.036pF	0.051pF	0.036pF	0.051pF	0.198pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
D ↓	1.43ns	0.86ns	PDN ↓	Q ↑	6.51ns/pF	1.06ns	1.36ns/pF	0.98ns
D ↑	1.14ns	0.62ns	PDN ↓	QN ↓	1.96ns/pF	0.96ns	0.47ns/pF	0.92ns
			SCKN ↓	Q ↓	10.39ns/pF	2.81ns	1.98ns/pF	1.44ns
			SCKN ↓	Q ↑	6.51ns/pF	0.87ns	1.36ns/pF	0.79ns
			SCKN ↓	QN ↓	1.96ns/pF	0.77ns	0.47ns/pF	0.73ns
			SCKN ↓	QN ↑	5.13ns/pF	2.60ns	0.96ns/pF	1.34ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Dynamic Shift Register

DR2A1I

Master-Slave clocking, positive synchronous clear.

Grids 10, **Transistors** 14

Inputs
D,MCK,MCKN,SCK,SCKN,CD

Outputs
Q

Truth Table

INPUTS				OUTPUTS	
				OLD	NEW
D	MCK	SCK	CD	Q	Q
X	↓	↑	1	X	0
0	↓	↑	X	X	0
1	↓	↑	0	X	1

X = Don't care

Capacitances

	D	MCK	MCKN	SCK	SCKN	CD
Area	0.034pF	0.018pF	0.018pF	0.018pF	0.018pF	0.034pF
Perf	0.145pF	0.036pF	0.051pF	0.036pF	0.051pF	0.145pF

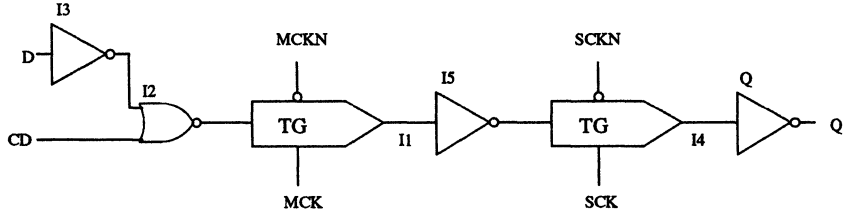
7

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
CD ↓	1.14ns	0.76ns	SCKN ↓	Q ↓	1.96ns/pF	0.43ns	0.47ns/pF	0.49ns
CD ↑	1.05ns	0.57ns	SCKN ↓	Q ↑	3.66ns/pF	0.23ns	0.68ns/pF	0.37ns
D ↓	1.14ns	0.72ns						
D ↑	1.72ns	1.05ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Dynamic Shift Register

DR2A1J

Master-Slave clocking, positive synchronous preset.

Grids 12, **Transistors** 12

Inputs
D,MCK,MCKN,SCK,SCKN,PD

Outputs
Q

Truth Table

INPUTS				OUTPUTS	
				OLD	NEW
D	MCK	SCK	PD	Q	Q
X	↓	↑	1	X	1
0	↓	↑	0	X	0
1	↓	↑	X	X	1

X = Don't care

Capacitances

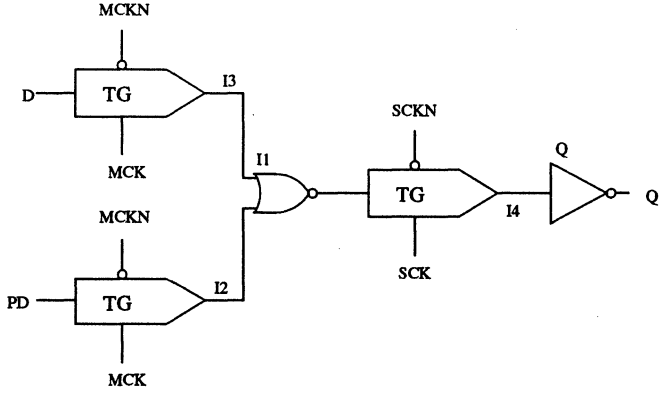
	D	MCK	MCKN	SCK	SCKN	PD
Area	0.026pF	0.039pF	0.039pF	0.018pF	0.018pF	0.025pF
Perf	0.048pF	0.073pF	0.101pF	0.036pF	0.051pF	0.047pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	0.38ns	0.43ns	SCKN ↓	Q ↓	1.96ns/pF	0.48ns	0.47ns/pF	0.49ns
D ↑	1.24ns	0.62ns	SCKN ↓	Q ↑	3.66ns/pF	0.23ns	0.68ns/pF	0.37ns
PD ↓	0.38ns	0.43ns						
PD ↑	1.19ns	0.57ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Dynamic Shift Register

DR2A1M

Master-Slave clocking, negative synchronous clear.

Grids 12, **Transistors** 12

Inputs
D,MCK,MCKN,SCK,SCKN,CDN

Outputs
Q

Truth Table

INPUTS				OUTPUTS	
				OLD	NEW
D	MCK	SCK	CDN	Q	Q
X	↓	↑	0	X	0
0	↓	↑	X	X	0
1	↓	↑	1	X	1

X = Don't care

Capacitances

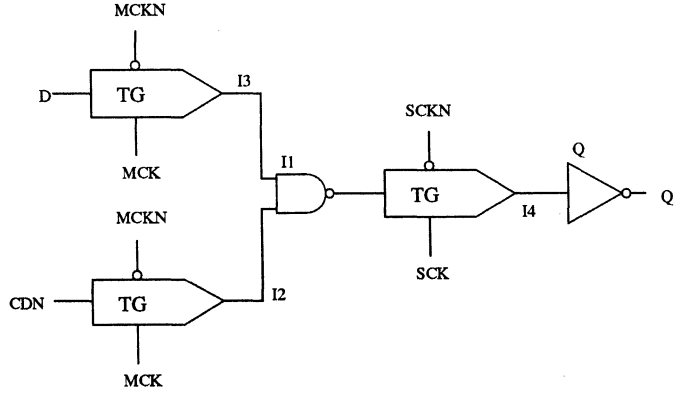
	D	MCK	MCKN	SCK	SCKN	CDN
Area	0.026pF	0.039pF	0.039pF	0.018pF	0.018pF	0.025pF
Perf	0.048pF	0.073pF	0.101pF	0.036pF	0.051pF	0.047pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
CDN ↓	0.33ns	0.38ns	SCKN ↓	Q ↓	1.96ns/pF	0.43ns	0.47ns/pF	0.49ns
CDN ↑	1.29ns	0.67ns	SCKN ↓	Q ↑	3.66ns/pF	0.23ns	0.68ns/pF	0.37ns
D ↓	0.33ns	0.38ns						
D ↑	1.29ns	0.67ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Dynamic Shift Register — DR2A1N

Master-Slave clocking, positive asynchronous clear, negative asynchronous preset.

Grids 18, **Transistors** 26

Inputs
D,MCK,MCKN,SCK,SCKN,PDN,CD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS OLD		OUTPUTS NEW	
D	MCK	SCK	PDN	CD	Q	QN	Q	QN
X	X	X	0	X	X	X	1	0
X	X	X	1	1	X	X	0	1
0	↓	↑	1	X	X	X	0	1
1	↓	↑	X	0	X	X	1	0

X = Don't care

Capacitances

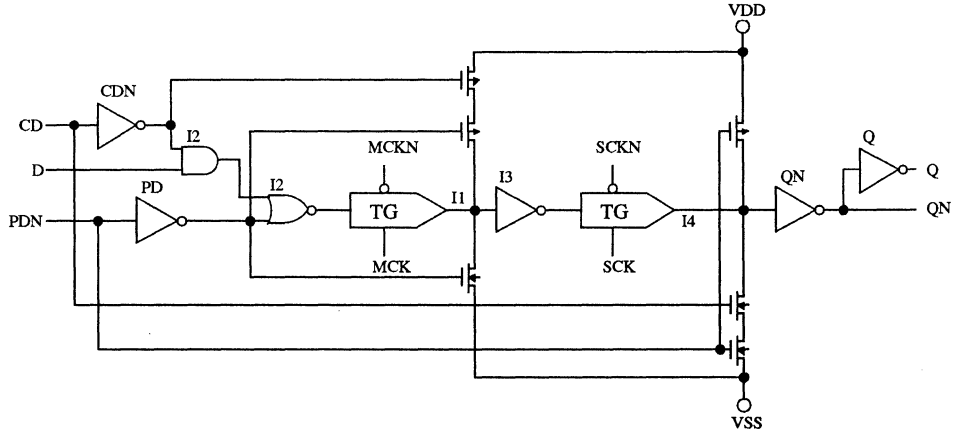
	D	MCK	MCKN	SCK	SCKN	PDN	CD
Area	0.035pF	0.018pF	0.018pF	0.018pF	0.018pF	0.080pF	0.058pF
Perf	0.146pF	0.036pF	0.051pF	0.036pF	0.051pF	0.258pF	0.189pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
D ↓	1.67ns	1.19ns	CD ↑	Q ↓	8.92ns/pF	2.48ns	1.72ns/pF	1.65ns
D ↑	1.48ns	0.95ns	CD ↑	QN ↑	3.66ns/pF	2.28ns	0.70ns/pF	1.54ns
			PDN ↓	Q ↑	6.55ns/pF	0.71ns	1.38ns/pF	0.82ns
			PDN ↓	QN ↓	2.01ns/pF	0.60ns	0.50ns/pF	0.75ns
			SCKN ↓	Q ↓	8.92ns/pF	0.67ns	1.72ns/pF	0.69ns
			SCKN ↓	Q ↑	6.55ns/pF	0.90ns	1.38ns/pF	0.86ns
			SCKN ↓	QN ↓	2.01ns/pF	0.79ns	0.50ns/pF	0.80ns
			SCKN ↓	QN ↑	3.66ns/pF	0.46ns	0.70ns/pF	0.59ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



7

Dynamic Shift Register — DR2B1A

Master-Slave clocking, positive level sample.

Grids 12, **Transistors** 18

Inputs
D,SP,MCK,MCKN,SCK,SCKN

Outputs
Q

Truth Table

INPUTS				OUTPUTS	
				OLD	NEW
D	SP	MCK	SCK	Q	Q
X	0	↓	↑	0	0
X	0	↓	↑	1	1
0	1	↓	↑	X	0
1	1	↓	↑	X	1

X = Don't care

Capacitances

	D	SP	MCK	MCKN	SCK	SCKN
Area	0.034pF	0.068pF	0.018pF	0.018pF	0.018pF	0.018pF
Perf	0.145pF	0.293pF	0.036pF	0.051pF	0.036pF	0.051pF

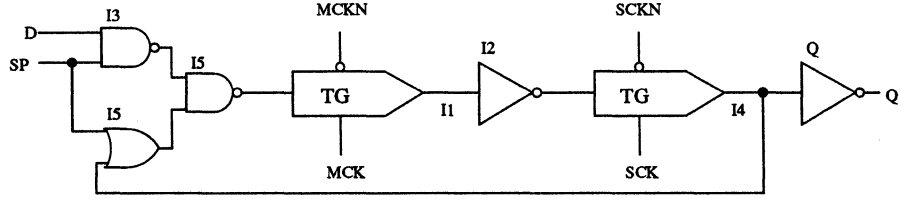
7

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.24ns	0.76ns	SCKN ↓	Q ↓	1.96ns/pF	0.72ns	0.52ns/pF	0.69ns
D ↑	1.91ns	1.14ns	SCKN ↓	Q ↑	3.66ns/pF	0.27ns	0.70ns/pF	0.54ns
SP ↓	1.24ns	0.81ns						
SP ↑	1.91ns	1.14ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Dynamic Shift Register

DR2B1I

Master-Slave clocking, positive level sample, positive synchronous clear.

Grids 13, **Transistors** 20

Inputs
D,SP,MCK,MCKN,SCK,SCKN,CD

Outputs
Q

Truth Table

INPUTS					OUTPUTS	
					OLD	NEW
D	SP	MCK	SCK	CD	Q	Q
X	0	↓	↑	X	0	0
X	0	↓	↑	0	1	1
X	X	↓	↑	1	X	0
0	1	↓	↑	X	X	0
1	1	↓	↑	0	X	1

X = Don't care

Capacitances

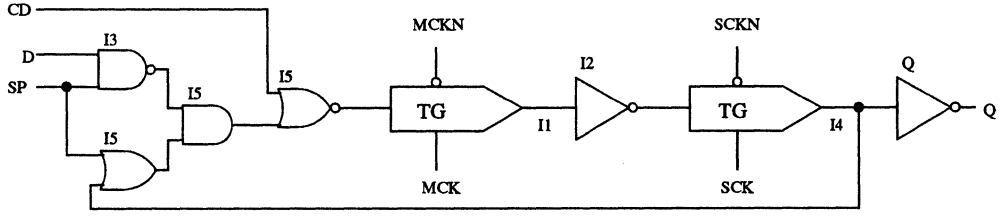
	D	SP	MCK	MCKN	SCK	SCKN	CD
Area	0.034pF	0.068pF	0.018pF	0.018pF	0.018pF	0.018pF	0.034pF
Perf	0.145pF	0.293pF	0.036pF	0.051pF	0.036pF	0.051pF	0.145pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
CD ↓	1.81ns	1.05ns	SCKN ↓	Q ↓	1.96ns/pF	0.72ns	0.52ns/pF	0.69ns
CD ↑	1.19ns	0.62ns	SCKN ↓	Q ↑	3.66ns/pF	0.27ns	0.70ns/pF	0.54ns
D ↓	1.29ns	0.76ns						
D ↑	2.58ns	1.43ns						
SP ↓	1.91ns	1.10ns						
SP ↑	2.58ns	1.43ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Dynamic Shift Register — DR2B1J

Master-Slave clocking, positive level sample, positive synchronous preset.

Grids 13, **Transistors** 20

Inputs
D,SP,MCK,MCKN,SCK,SCKN,PD

Outputs
Q

Truth Table

INPUTS					OUTPUTS	
					OLD	NEW
D	SP	MCK	SCK	PD	Q	Q
X	0	↓	↑	0	0	0
X	0	↓	↑	X	1	1
X	X	↓	↑	1	X	1
0	1	↓	↑	0	X	0
1	1	↓	↑	X	X	1

X = Don't care

Capacitances

	D	SP	MCK	MCKN	SCK	SCKN	PD
Area	0.034pF	0.068pF	0.018pF	0.018pF	0.018pF	0.018pF	0.034pF
Perf	0.145pF	0.293pF	0.036pF	0.051pF	0.036pF	0.051pF	0.145pF

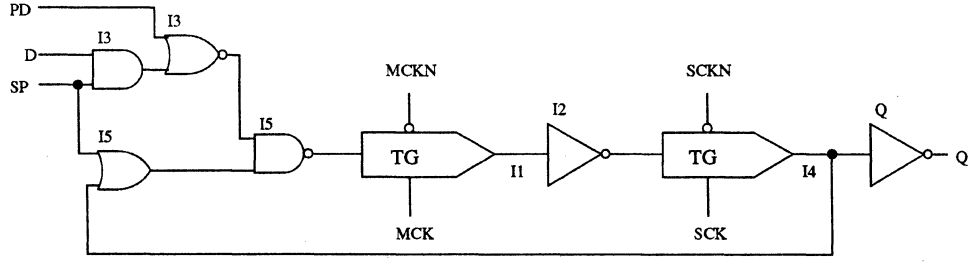
7

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D ↓	1.62ns	0.95ns	SCKN ↓	Q ↓	1.96ns/pF	0.72ns	0.52ns/pF	0.69ns
D ↑	1.96ns	1.19ns	SCKN ↓	Q ↑	3.66ns/pF	0.27ns	0.70ns/pF	0.54ns
PD ↓	1.62ns	0.95ns						
PD ↑	1.86ns	1.10ns						
SP ↓	1.62ns	0.95ns						
SP ↑	1.96ns	1.19ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Dynamic Shift Register

DR2C1A

Master-Slave clocking, negative level sample.

Grids 12, **Transistors** 18

Inputs
D,SPN,MCK,MCKN,SCK,SCKN

Outputs
Q

Truth Table

INPUTS				OUTPUTS	
				OLD	NEW
D	SPN	MCK	SCK	Q	Q
X	1	↓	↑	0	0
X	1	↓	↑	1	1
0	0	↓	↑	X	0
1	0	↓	↑	X	1

X = Don't care

Capacitances

	D	SPN	MCK	MCKN	SCK	SCKN
Area	0.034pF	0.068pF	0.018pF	0.018pF	0.018pF	0.018pF
Perf	0.145pF	0.293pF	0.036pF	0.051pF	0.036pF	0.051pF

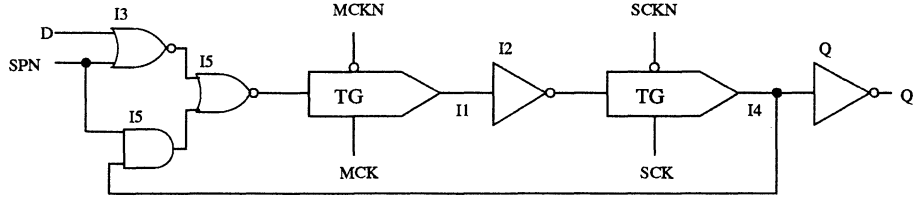
7

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.43ns	0.95ns	SCKN ↓	Q ↓	1.96ns/pF	0.72ns	0.52ns/pF	0.69ns
D ↑	1.81ns	1.14ns	SCKN ↓	Q ↑	3.66ns/pF	0.27ns	0.70ns/pF	0.54ns
SPN ↓	1.43ns	0.95ns						
SPN ↑	1.81ns	1.14ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Dynamic Shift Register

DR2C1I

Master-Slave clocking, negative level sample, positive synchronous clear.

Grids 13, **Transistors** 20

Inputs
D,SPN,MCK,MCKN,SCK,SCKN,CD

Outputs
Q

Truth Table

INPUTS					OUTPUTS	
					OLD	NEW
D	SPN	MCK	SCK	CD	Q	Q
X	1	↓	↑	X	0	0
X	1	↓	↑	0	1	1
X	X	↓	↑	1	X	0
0	0	↓	↑	X	X	0
1	0	↓	↑	0	X	1

X = Don't care

Capacitances

	D	SPN	MCK	MCKN	SCK	SCKN	CD
Area	0.034pF	0.068pF	0.018pF	0.018pF	0.018pF	0.018pF	0.034pF
Perf	0.145pF	0.293pF	0.036pF	0.051pF	0.036pF	0.051pF	0.145pF

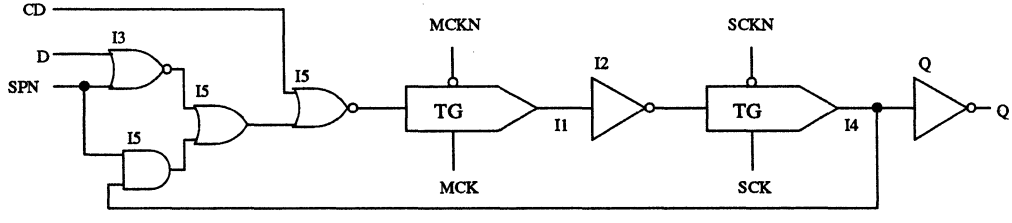
7

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CD ↓	1.86ns	1.10ns	SCKN ↓	Q ↓	1.96ns/pF	0.72ns	0.52ns/pF	0.69ns
CD ↑	1.14ns	0.67ns	SCKN ↓	Q ↑	3.66ns/pF	0.27ns	0.70ns/pF	0.59ns
D ↓	1.48ns	1.00ns						
D ↑	2.43ns	1.43ns						
SPN ↓	1.86ns	1.10ns						
SPN ↑	2.43ns	1.43ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Dynamic Shift Register — DR2D1A

Master-Slave clocking, inverting data with positive level sample.

Grids 12, **Transistors** 18

Inputs
DN,SP,MCK,MCKN,SCK,SCKN

Outputs
Q

Truth Table

INPUTS				OUTPUTS	
				OLD	NEW
DN	SP	MCK	SCK	Q	Q
X	0	↓	↑	0	0
X	0	↓	↑	1	1
1	1	↓	↑	X	0
0	1	↓	↑	X	1

X = Don't care

Capacitances

	DN	SP	MCK	MCKN	SCK	SCKN
Area	0.034pF	0.068pF	0.018pF	0.018pF	0.018pF	0.018pF
Perf	0.145pF	0.293pF	0.036pF	0.051pF	0.036pF	0.051pF

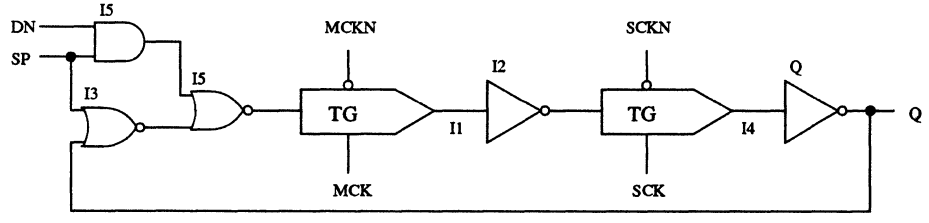
7

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
DN ↓	1.24ns	0.86ns	SCKN ↓	Q ↓	1.92ns/pF	0.55ns	0.47ns/pF	0.54ns
DN ↑	1.19ns	0.72ns	SCKN ↓	Q ↑	3.66ns/pF	0.37ns	0.68ns/pF	0.47ns
SP ↓	1.43ns	1.00ns						
SP ↑	1.76ns	1.10ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Dynamic Shift Register

DR2D1I

Master-Slave clocking, inverting data with positive level sample, positive synchronous clear.

Grids 13, **Transistors** 20

Inputs
DN,SP,MCK,MCKN,SCK,SCKN,CD

Outputs
Q

Truth Table

INPUTS					OUTPUTS	
					OLD	NEW
DN	SP	MCK	SCK	CD	Q	Q
X	0	↓	↑	X	0	0
X	0	↓	↑	0	1	1
X	X	↓	↑	1	X	0
1	1	↓	↑	X	X	0
0	1	↓	↑	0	X	1

X = Don't care

Capacitances

	DN	SP	MCK	MCKN	SCK	SCKN	CD
Area	0.034pF	0.068pF	0.018pF	0.018pF	0.018pF	0.018pF	0.034pF
Perf	0.145pF	0.293pF	0.036pF	0.051pF	0.036pF	0.051pF	0.145pF

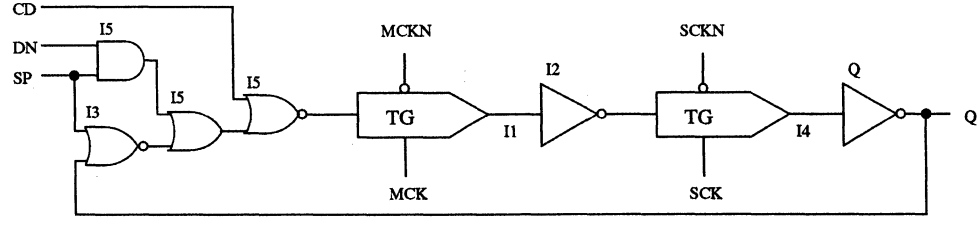
7

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CD ↓	1.86ns	1.10ns	SCKN ↓	Q ↓	1.92ns/pF	0.55ns	0.47ns/pF	0.54ns
CD ↑	1.14ns	0.72ns	SCKN ↓	Q ↑	3.61ns/pF	0.44ns	0.68ns/pF	0.42ns
DN ↓	1.86ns	1.10ns						
DN ↑	1.19ns	0.72ns						
SP ↓	1.86ns	1.10ns						
SP ↑	2.38ns	1.34ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Dynamic Shift Register — DR2E1A

Master-Slave clocking, inverting data with negative level sample.

Grids 12, **Transistors** 18

Inputs
DN,SPN,MCK,MCKN,SCK,SCKN

Outputs
Q

Truth Table

INPUTS				OUTPUTS	
				OLD	NEW
DN	SPN	MCK	SCK	Q	Q
X	1	↓	↑	0	0
X	1	↓	↑	1	1
1	0	↓	↑	X	0
0	0	↓	↑	X	1

X = Don't care

Capacitances

	DN	SPN	MCK	MCKN	SCK	SCKN
Area	0.034pF	0.068pF	0.018pF	0.018pF	0.018pF	0.018pF
Perf	0.145pF	0.293pF	0.036pF	0.051pF	0.036pF	0.051pF

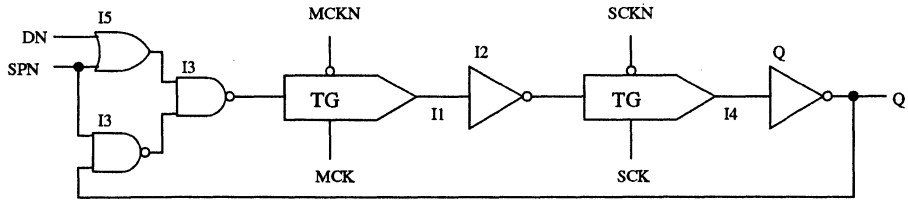
7

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
DN ↓	1.24ns	0.81ns	SCKN ↓	Q ↓	1.92ns/pF	0.55ns	0.47ns/pF	0.54ns
DN ↑	1.24ns	0.72ns	SCKN ↓	Q ↑	3.66ns/pF	0.37ns	0.68ns/pF	0.47ns
SPN ↓	1.24ns	0.81ns						
SPN ↑	1.86ns	1.14ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Dynamic Shift Register — DR2E1I

Master-Slave clocking, inverting data with negative level sample, positive synchronous clear.

Grids 13, **Transistors** 20

Inputs
DN,SPN,MCK,MCKN,SCK,SCKN,CD

Outputs
Q

Truth Table

INPUTS					OUTPUTS	
					OLD	NEW
DN	SPN	MCK	SCK	CD	Q	Q
X	1	↓	↑	X	0	0
X	1	↓	↑	0	1	1
X	X	↓	↑	1	X	0
1	0	↓	↑	X	X	0
0	0	↓	↑	0	X	1

X = Don't care

Capacitances

	DN	SPN	MCK	MCKN	SCK	SCKN	CD
Area	0.034pF	0.070pF	0.018pF	0.018pF	0.018pF	0.018pF	0.034pF
Perf	0.145pF	0.295pF	0.036pF	0.051pF	0.036pF	0.051pF	0.145pF

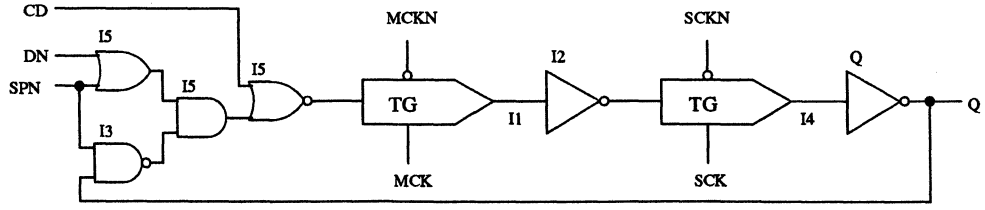
7

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
CD ↓	1.81ns	1.05ns	SCKN ↓	Q ↓	1.92ns/pF	0.55ns	0.47ns/pF	0.54ns
CD ↑	1.19ns	0.62ns	SCKN ↓	Q ↑	3.61ns/pF	0.44ns	0.68ns/pF	0.42ns
DN ↓	1.91ns	1.14ns						
DN ↑	1.34ns	0.72ns						
SPN ↓	1.91ns	1.14ns						
SPN ↑	2.53ns	1.43ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FB1S2AX

Negative edge triggered, BIST select front end.

Grids 23, **Transistors** 36

Inputs
D0,D1,B0,B1,CKA,CKB

Outputs
Q,QN

Capacitances

	D0	D1	B0	B1	CKA	CKB
Area	0.062pF	0.061pF	0.061pF	0.062pF	0.097pF	0.064pF
Perf	0.223pF	0.222pF	0.222pF	0.223pF	0.300pF	0.159pF

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	B0	B1	CK	Q	QN	Q	QN
X	X	0	0	↓	X	X	0	1
0	X	0	X	↓	X	X	0	1
1	X	0	1	↓	X	X	1	0
X	0	X	0	↓	X	X	0	1
X	1	1	0	↓	X	X	1	0
0	0	X	X	↓	X	X	0	1
0	1	1	X	↓	X	X	1	0
1	0	X	1	↓	X	X	1	0
1	1	1	1	↓	X	X	0	1

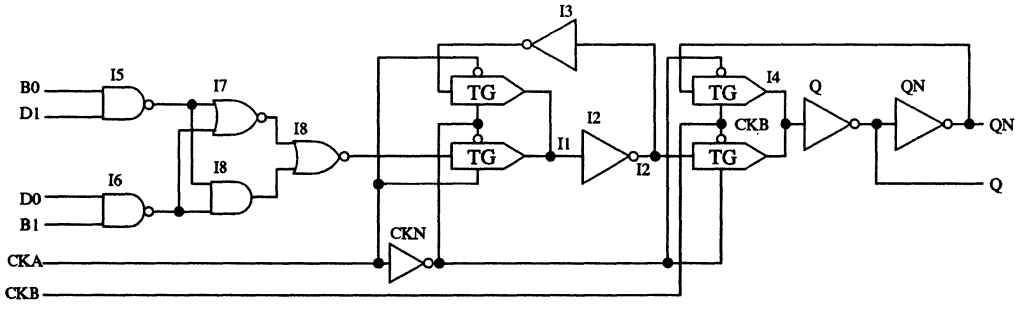
X = Don't care

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
B0 ↓	2.91ns	1.86ns	CK ↑	Q ↓	1.96ns/pF	1.20ns	0.47ns/pF	0.82ns
B0 ↑	3.20ns	1.91ns	CK ↑	Q ↑	3.61ns/pF	1.15ns	0.65ns/pF	0.77ns
B1 ↓	2.86ns	1.86ns	CK ↑	QN ↓	8.92ns/pF	1.34ns	1.67ns/pF	0.88ns
B1 ↑	3.15ns	1.91ns	CK ↑	QN ↑	6.55ns/pF	1.28ns	1.36ns/pF	0.88ns
D0 ↓	2.86ns	1.86ns						
D0 ↑	3.15ns	1.91ns						
D1 ↓	2.91ns	1.86ns						
D1 ↑	3.20ns	1.91ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FB1S3AX

Positive edge triggered, BIST select front end.

Grids 23, **Transistors** 36

Inputs
D0,D1,B0,B1,CKA,CKB

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	B0	B1	CK	Q	QN	Q	QN
X	X	0	0	↑	X	X	0	1
0	X	0	X	↑	X	X	0	1
1	X	0	1	↑	X	X	1	0
X	0	X	0	↑	X	X	0	1
X	1	1	0	↑	X	X	1	0
0	0	X	X	↑	X	X	0	1
0	1	1	X	↑	X	X	1	0
1	0	X	1	↑	X	X	1	0
1	1	1	1	↑	X	X	0	1

X = Don't care

Capacitances

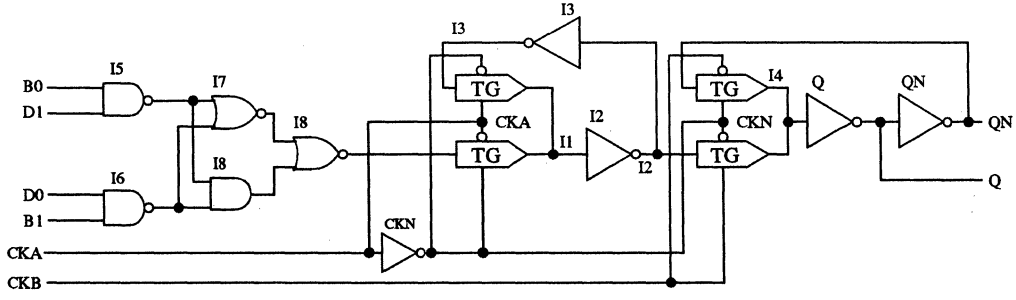
	D0	D1	B0	B1	CKA	CKB
Area	0.062pF	0.061pF	0.061pF	0.062pF	0.097pF	0.063pF
Perf	0.223pF	0.222pF	0.222pF	0.223pF	0.301pF	0.158pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
B0 ↓	2.96ns	1.86ns	CK ↑	Q ↓	1.96ns/pF	2.01ns	0.50ns/pF	1.09ns
B0 ↑	3.24ns	1.91ns	CK ↑	Q ↑	3.61ns/pF	1.96ns	0.68ns/pF	1.04ns
B1 ↓	2.91ns	1.86ns	CK ↑	QN ↓	8.92ns/pF	2.15ns	1.69ns/pF	1.14ns
B1 ↑	3.20ns	1.91ns	CK ↑	QN ↑	6.55ns/pF	2.09ns	1.38ns/pF	1.15ns
D0 ↓	2.91ns	1.86ns						
D0 ↑	3.20ns	1.91ns						
D1 ↓	2.96ns	1.86ns						
D1 ↑	3.24ns	1.91ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1N2AX

Negative edge triggered, negative level sample.

Grids 19, **Transistors** 26

Inputs
D,SPN,CKA,CKB

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	SPN	CK	Q	QN	Q	QN
X	1	↓	1	0	1	0
X	1	↓	0	1	0	1
0	0	↓	X	X	0	1
1	0	↓	X	X	1	0

X = Don't care

Capacitances

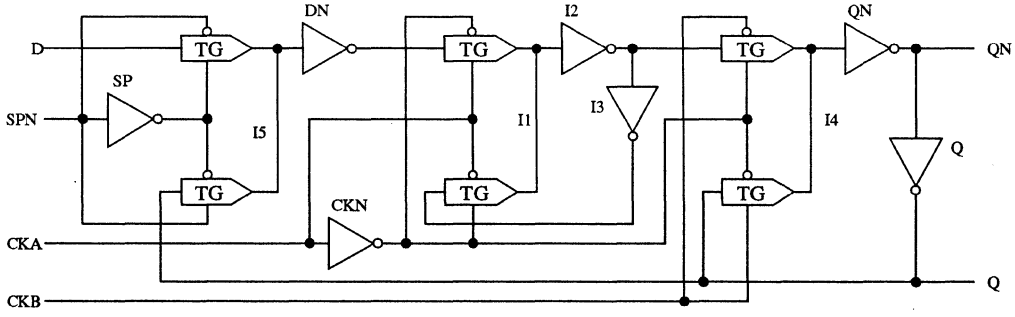
	D	SPN	CKA	CKB
Area	0.026pF	0.070pF	0.076pF	0.037pF
Perf	0.077pF	0.294pF	0.234pF	0.082pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.29ns	1.05ns	CK ↑	Q ↓	8.92ns/pF	1.43ns	1.67ns/pF	0.92ns
D ↑	2.34ns	1.24ns	CK ↑	Q ↑	6.51ns/pF	1.44ns	1.36ns/pF	0.93ns
SPN ↓	1.81ns	1.34ns	CK ↑	QN ↓	1.96ns/pF	1.20ns	0.47ns/pF	0.82ns
SPN ↑	2.53ns	1.57ns	CK ↑	QN ↑	3.61ns/pF	1.15ns	0.65ns/pF	0.77ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1N2JX

Negative edge triggered, negative level sample, positive synchronous preset.

Grids 21, **Transistors** 32

Inputs
D,SPN,CKA,CKB,PD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	SPN	CK	PD	Q	QN	Q	QN
X	1	↓	0	0	1	0	1
X	1	↓	X	1	0	1	0
X	X	↓	1	X	X	1	0
0	0	↓	0	X	X	0	1
1	0	↓	X	X	X	1	0

X = Don't care

Capacitances

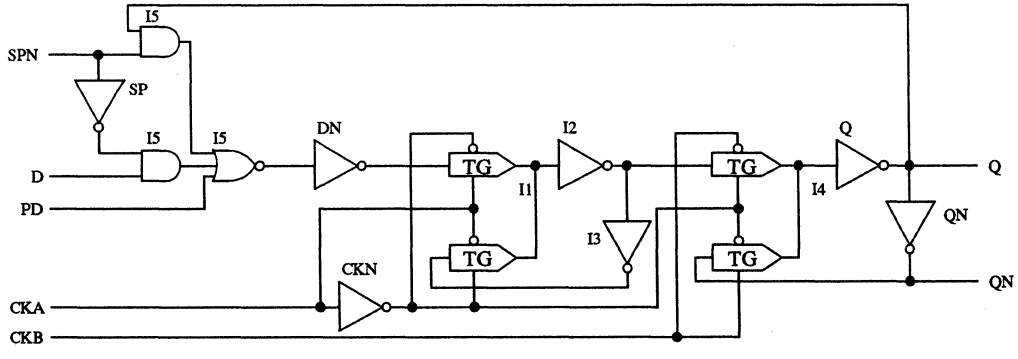
	D	SPN	CKA	CKB	PD
Area	0.036pF	0.073pF	0.070pF	0.037pF	0.034pF
Perf	0.148pF	0.298pF	0.223pF	0.082pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	2.72ns	1.76ns	CK ↑	Q ↓	1.96ns/pF	1.29ns	0.44ns/pF	0.94ns
D ↑	2.29ns	1.53ns	CK ↑	Q ↑	3.61ns/pF	1.34ns	0.65ns/pF	0.87ns
PD ↓	2.72ns	1.76ns	CK ↑	QN ↓	8.92ns/pF	1.62ns	1.67ns/pF	1.02ns
PD ↑	2.19ns	1.53ns	CK ↑	QN ↑	6.51ns/pF	1.44ns	1.33ns/pF	1.05ns
SPN ↓	2.72ns	1.76ns						
SPN ↑	3.29ns	2.10ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1N2MX

Negative edge triggered, negative level sample, negative synchronous clear.

Grids 21, **Transistors** 32

Inputs
D,SPN,CKA,CKB,CDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	SPN	CK	CDN	Q	QN	Q	QN
X	1	↓	X	0	1	0	1
X	1	↓	1	1	0	1	0
X	X	↓	0	X	X	0	1
0	0	↓	X	X	X	0	1
1	0	↓	1	X	X	1	0

X = Don't care

Capacitances

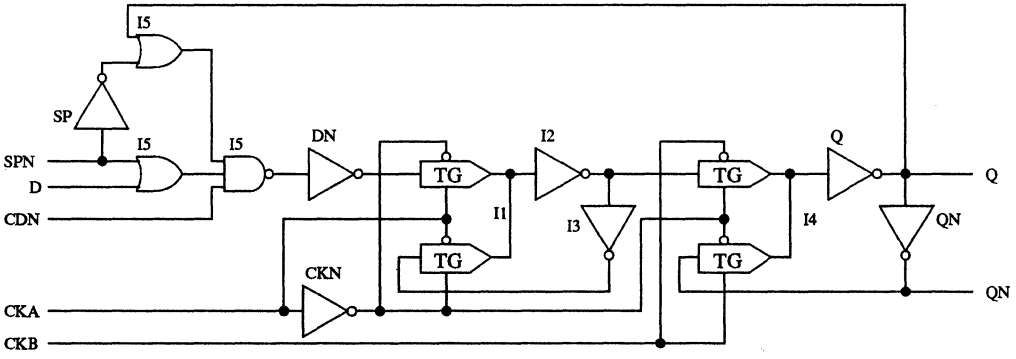
	D	SPN	CKA	CKB	CDN
Area	0.036pF	0.070pF	0.070pF	0.037pF	0.034pF
Perf	0.148pF	0.295pF	0.223pF	0.082pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	1.91ns	1.29ns	CK ↑	Q ↓	1.96ns/pF	1.29ns	0.44ns/pF	0.94ns
CDN ↑	2.58ns	1.62ns	CK ↑	Q ↑	3.61ns/pF	1.34ns	0.65ns/pF	0.87ns
D ↓	2.19ns	1.43ns	CK ↑	QN ↓	8.92ns/pF	1.62ns	1.67ns/pF	1.02ns
D ↑	2.58ns	1.62ns	CK ↑	QN ↑	6.51ns/pF	1.44ns	1.33ns/pF	1.05ns
SPN ↓	2.43ns	1.72ns						
SPN ↑	2.77ns	1.76ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1N3AX

Positive edge triggered, negative level sample.

Grids 19, **Transistors** 26

Inputs
D,SPN,CKA,CKB

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	SPN	CK	Q	QN	Q	QN
X	1	↑	0	1	0	1
X	1	↑	1	0	1	0
0	0	↑	X	X	0	1
1	0	↑	X	X	1	0

X = Don't care

Capacitances

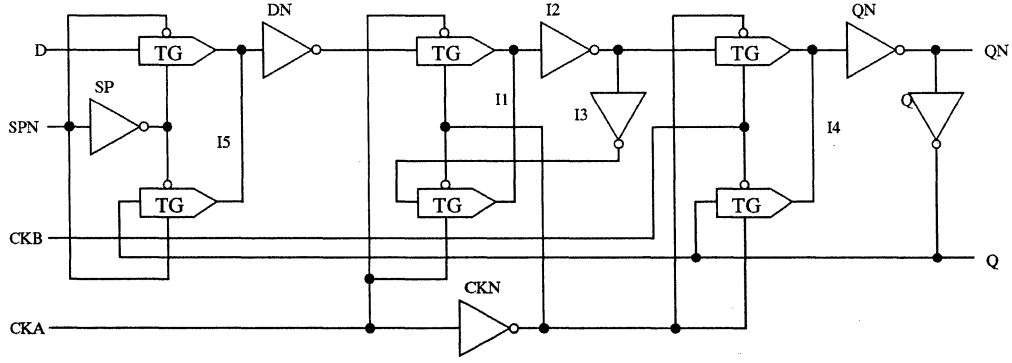
	D	SPN	CKA	CKB
Area	0.026pF	0.070pF	0.076pF	0.037pF
Perf	0.077pF	0.294pF	0.231pF	0.082pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.29ns	1.05ns	CK ↑	Q ↓	8.87ns/pF	2.31ns	1.67ns/pF	1.21ns
D ↑	2.38ns	1.24ns	CK ↑	Q ↑	6.46ns/pF	2.32ns	1.36ns/pF	1.22ns
SPN ↓	1.81ns	1.34ns	CK ↑	QN ↓	1.92ns/pF	2.08ns	0.47ns/pF	1.11ns
SPN ↑	2.53ns	1.57ns	CK ↑	QN ↑	3.57ns/pF	2.03ns	0.65ns/pF	1.06ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1N3JX

Positive edge triggered, negative level sample, positive synchronous preset.

Grids 21, **Transistors** 32

Inputs
D,SPN,CKA,CKB,PD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	SPN	CK	PD	Q	QN	Q	QN
X	1	↑	0	0	1	0	1
X	1	↑	X	1	0	1	0
X	X	↑	1	X	X	1	0
0	0	↑	0	X	X	0	1
1	0	↑	X	X	X	1	0

X = Don't care

Capacitances

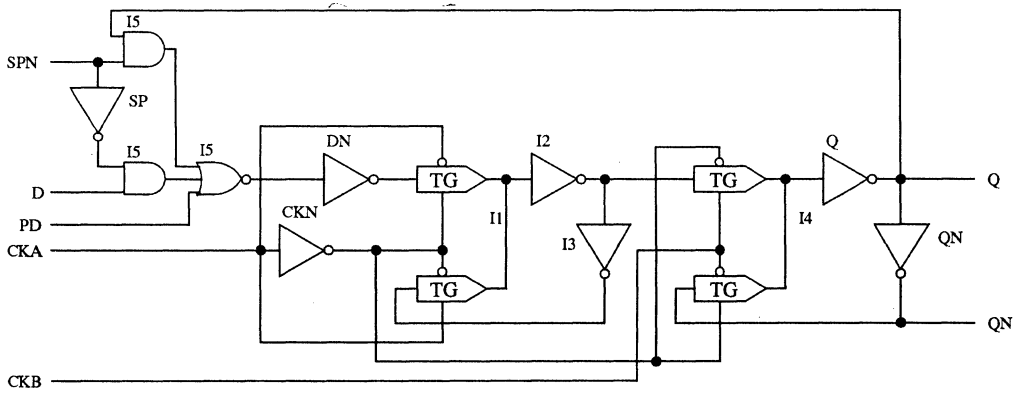
	D	SPN	CKA	CKB	PD
Area	0.036pF	0.073pF	0.070pF	0.037pF	0.034pF
Perf	0.148pF	0.298pF	0.223pF	0.082pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	2.72ns	1.76ns	CK ↑	Q ↓	1.96ns/pF	2.10ns	0.47ns/pF	1.20ns
D ↑	2.34ns	1.57ns	CK ↑	Q ↑	3.61ns/pF	2.15ns	0.68ns/pF	1.13ns
PD ↓	2.72ns	1.76ns	CK ↑	QN ↓	8.92ns/pF	2.43ns	1.69ns/pF	1.29ns
PD ↑	2.24ns	1.57ns	CK ↑	QN ↑	6.51ns/pF	2.25ns	1.36ns/pF	1.31ns
SPN ↓	2.72ns	1.76ns						
SPN ↑	3.29ns	2.10ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1N3MX

Positive edge triggered, negative level sample, negative synchronous clear.

Grids 21, **Transistors** 32

Inputs
D,SPN,CKA,CKB,CDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	SPN	CK	CDN	Q	QN	Q	QN
X	1	↑	X	0	1	0	1
X	1	↑	1	1	0	1	0
X	X	↑	0	X	X	0	1
0	0	↑	X	X	X	0	1
1	0	↑	1	X	X	1	0

X = Don't care

Capacitances

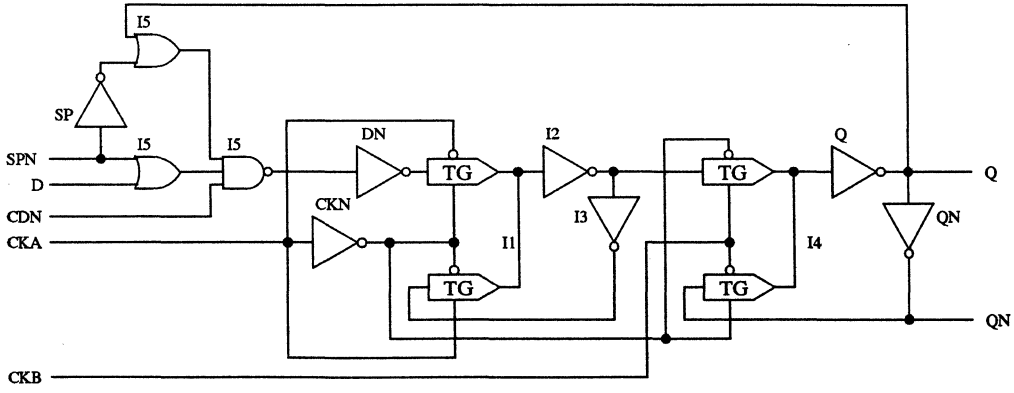
	D	SPN	CKA	CKB	CDN
Area	0.036pF	0.070pF	0.070pF	0.037pF	0.034pF
Perf	0.148pF	0.295pF	0.223pF	0.082pF	0.145pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
CDN ↓	1.96ns	1.29ns	CK ↑	Q ↓	1.96ns/pF	2.10ns	0.44ns/pF	1.22ns
CDN ↑	2.58ns	1.62ns	CK ↑	Q ↑	3.61ns/pF	2.15ns	0.65ns/pF	1.15ns
D ↓	2.24ns	1.43ns	CK ↑	QN ↓	8.92ns/pF	2.43ns	1.67ns/pF	1.31ns
D ↑	2.58ns	1.62ns	CK ↑	QN ↑	6.51ns/pF	2.25ns	1.33ns/pF	1.33ns
SPN ↓	2.43ns	1.72ns						
SPN ↑	2.81ns	1.76ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1P2AX

Negative edge triggered, positive level sample.

Grids 19, **Transistors** 26

Inputs
D,SP,CKA,CKB

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	SP	CK	Q	QN	Q	QN
X	0	↓	0	1	0	1
X	0	↓	1	0	1	0
0	1	↓	X	X	0	1
1	1	↓	X	X	1	0

X = Don't care

Capacitances

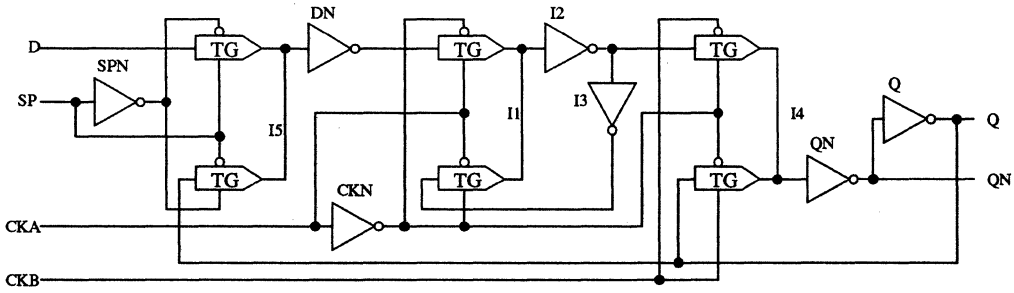
	D	SP	CKA	CKB
Area	0.026pF	0.070pF	0.076pF	0.037pF
Perf	0.077pF	0.294pF	0.234pF	0.082pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.34ns	1.05ns	CK ↑	Q ↓	8.92ns/pF	1.43ns	1.67ns/pF	0.92ns
D ↑	2.34ns	1.19ns	CK ↑	Q ↑	6.51ns/pF	1.44ns	1.36ns/pF	0.93ns
SP ↓	1.81ns	1.29ns	CK ↑	QN ↓	1.96ns/pF	1.20ns	0.47ns/pF	0.82ns
SP ↑	2.67ns	1.57ns	CK ↑	QN ↑	3.61ns/pF	1.15ns	0.65ns/pF	0.77ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1P2JX

Negative edge triggered, positive level sample, positive synchronous preset.

Grids 21, **Transistors** 32

Inputs
D,SP,CKA,CKB,PD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	SP	CK	PD	Q	QN	Q	QN
X	0	↓	0	0	1	0	1
X	0	↓	X	1	0	1	0
X	X	↓	1	X	X	1	0
0	1	↓	0	X	X	0	1
1	1	↓	X	X	X	1	0

X = Don't care

Capacitances

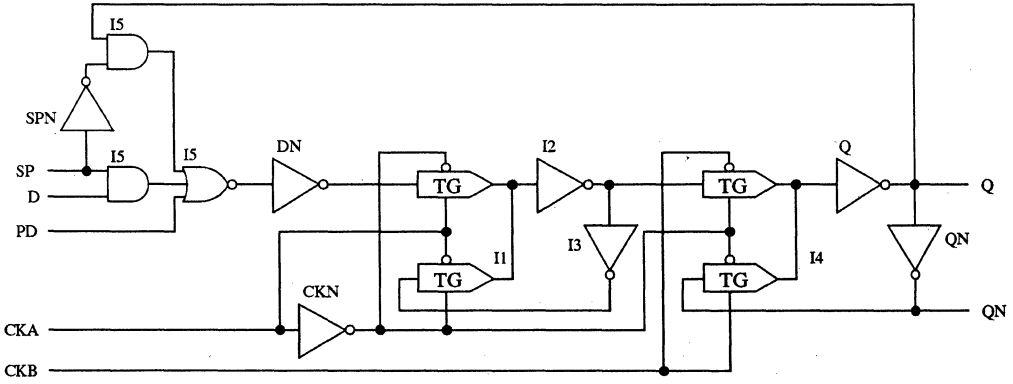
	D	SP	CKA	CKB	PD
Area	0.036pF	0.070pF	0.070pF	0.037pF	0.034pF
Perf	0.148pF	0.295pF	0.223pF	0.082pF	0.145pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D ↓	2.72ns	1.76ns	CK ↑	Q ↓	1.96ns/pF	1.29ns	0.44ns/pF	0.94ns
D ↑	2.29ns	1.53ns	CK ↑	Q ↑	3.61ns/pF	1.34ns	0.65ns/pF	0.87ns
PD ↓	2.72ns	1.76ns	CK ↑	QN ↓	8.92ns/pF	1.62ns	1.67ns/pF	1.02ns
PD ↑	2.19ns	1.53ns	CK ↑	QN ↑	6.51ns/pF	1.44ns	1.33ns/pF	1.05ns
SP ↓	2.72ns	1.76ns						
SP ↑	3.29ns	2.10ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1P2MX

Negative edge triggered, positive level sample, negative synchronous clear.

Grids 21, **Transistors** 32

Inputs
D,SP,CKA,CKB,CDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	SP	CK	CDN	Q	QN	Q	QN
X	0	↓	X	0	1	0	1
X	0	↓	1	1	0	1	0
X	X	↓	0	X	X	0	1
0	1	↓	X	X	X	0	1
1	1	↓	1	X	X	1	0

X = Don't care

Capacitances

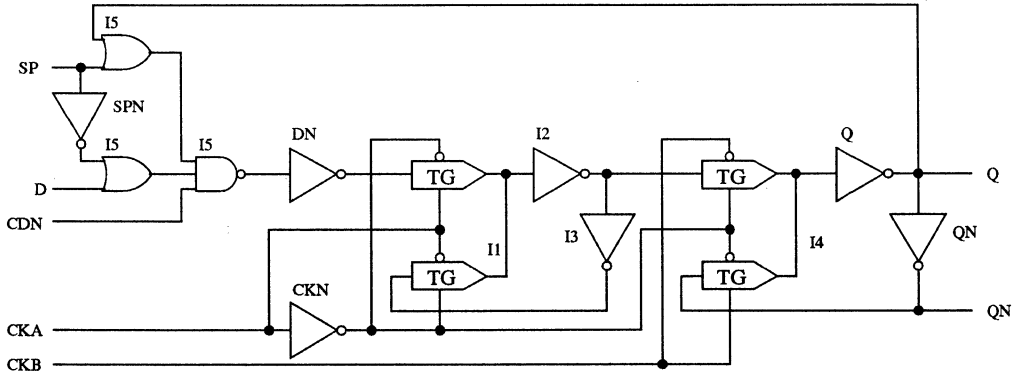
	D	SP	CKA	CKB	CDN
Area	0.036pF	0.073pF	0.070pF	0.037pF	0.034pF
Perf	0.148pF	0.298pF	0.223pF	0.082pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	1.91ns	1.29ns	CK ↑	Q ↓	1.96ns/pF	1.29ns	0.44ns/pF	0.94ns
CDN ↑	2.58ns	1.62ns	CK ↑	Q ↑	3.61ns/pF	1.34ns	0.65ns/pF	0.87ns
D ↓	2.19ns	1.43ns	CK ↑	QN ↓	8.92ns/pF	1.62ns	1.67ns/pF	1.02ns
D ↑	2.58ns	1.62ns	CK ↑	QN ↑	6.51ns/pF	1.44ns	1.33ns/pF	1.05ns
SP ↓	2.38ns	1.72ns						
SP ↑	2.77ns	1.76ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1P3AX

Positive edge triggered, positive level sample.

Grids 19, **Transistors** 26

Inputs
D,SP,CKA,CKB

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	SP	CK	Q	QN	Q	QN
X	0	↑	0	1	0	1
X	0	↑	1	0	1	0
0	1	↑	X	X	0	1
1	1	↑	X	X	1	0

X = Don't care

Capacitances

	D	SP	CKA	CKB
Area	0.026pF	0.070pF	0.076pF	0.037pF
Perf	0.077pF	0.294pF	0.231pF	0.082pF

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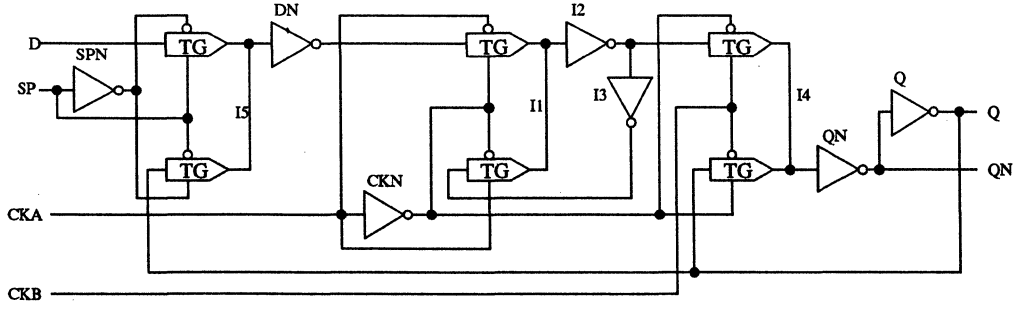
Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.34ns	1.05ns	CK ↑	Q ↓	8.87ns/pF	2.31ns	1.67ns/pF	1.21ns
D ↑	2.38ns	1.19ns	CK ↑	Q ↑	6.46ns/pF	2.32ns	1.36ns/pF	1.22ns
SP ↓	1.81ns	1.29ns	CK ↑	QN ↓	1.92ns/pF	2.08ns	0.47ns/pF	1.11ns
SP ↑	2.67ns	1.57ns	CK ↑	QN ↑	3.57ns/pF	2.03ns	0.65ns/pF	1.06ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1P3JX

Positive edge triggered, positive level sample, positive synchronous preset.

Grids 21, **Transistors** 32

Inputs
D,SP,CKA,CKB,PD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	SP	CK	PD	Q	QN	Q	QN
X	0	↑	0	0	1	0	1
X	0	↑	X	1	0	1	0
X	X	↑	1	X	X	1	0
0	1	↑	0	X	X	0	1
1	1	↑	X	X	X	1	0

X = Don't care

Capacitances

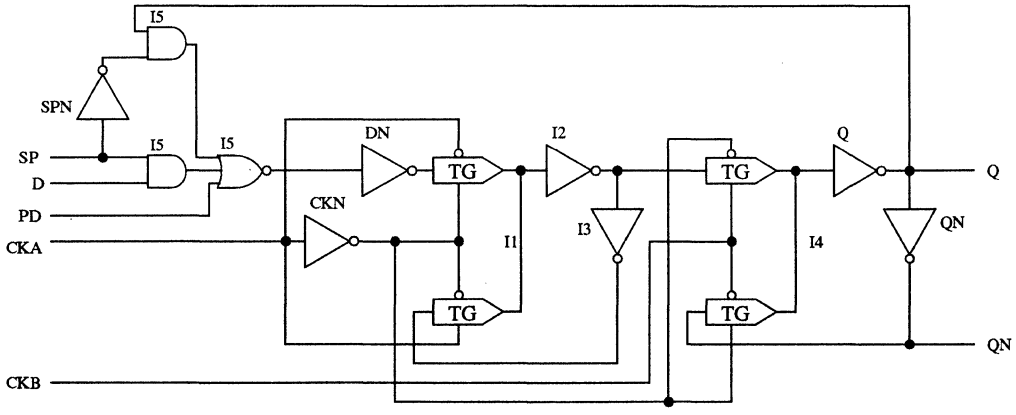
	D	SP	CKA	CKB	PD
Area	0.036pF	0.070pF	0.070pF	0.037pF	0.034pF
Perf	0.148pF	0.295pF	0.223pF	0.082pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	2.72ns	1.76ns	CK ↑	Q ↓	1.96ns/pF	2.10ns	0.47ns/pF	1.20ns
D ↑	2.34ns	1.57ns	CK ↑	Q ↑	3.61ns/pF	2.15ns	0.68ns/pF	1.13ns
PD ↓	2.72ns	1.76ns	CK ↑	QN ↓	8.92ns/pF	2.43ns	1.69ns/pF	1.29ns
PD ↑	2.24ns	1.57ns	CK ↑	QN ↑	6.51ns/pF	2.25ns	1.36ns/pF	1.31ns
SP ↓	2.72ns	1.76ns						
SP ↑	3.29ns	2.10ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1P3MX

Positive edge triggered, positive level sample, negative synchronous clear.

Grids 21, **Transistors** 32

Inputs
D,SP,CKA,CKB,CDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	SP	CK	CDN	Q	QN	Q	QN
X	0	↑	X	0	1	0	1
X	0	↑	1	1	0	1	0
X	X	↑	0	X	X	0	1
0	1	↑	X	X	X	0	1
1	1	↑	1	X	X	1	0

X = Don't care

Capacitances

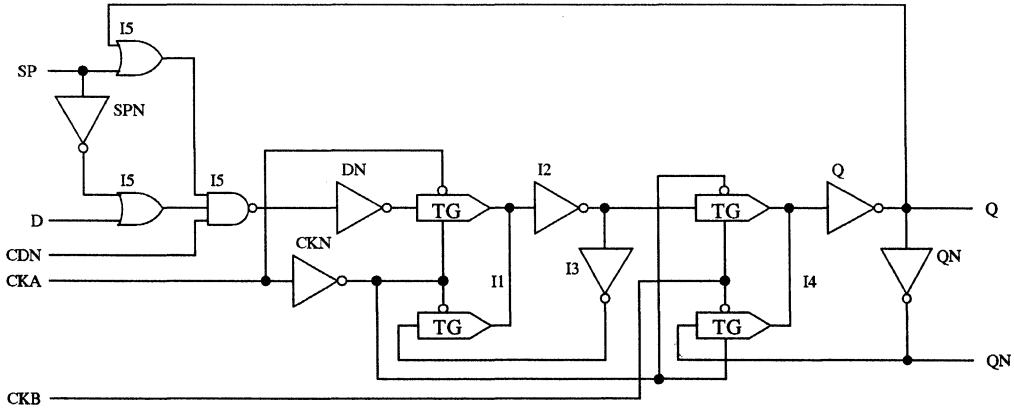
	D	SP	CKA	CKB	CDN
Area	0.036pF	0.073pF	0.070pF	0.037pF	0.034pF
Perf	0.148pF	0.298pF	0.223pF	0.082pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	1.96ns	1.29ns	CK ↑	Q ↓	1.96ns/pF	2.10ns	0.44ns/pF	1.22ns
CDN ↑	2.58ns	1.62ns	CK ↑	Q ↑	3.61ns/pF	2.15ns	0.65ns/pF	1.15ns
D ↓	2.24ns	1.43ns	CK ↑	QN ↓	8.92ns/pF	2.43ns	1.67ns/pF	1.31ns
D ↑	2.58ns	1.62ns	CK ↑	QN ↑	6.51ns/pF	2.25ns	1.33ns/pF	1.33ns
SP ↓	2.38ns	1.72ns						
SP ↑	2.81ns	1.76ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S1A

Positive level sense.

Grids 9, **Transistors** 10

Inputs
D,CK

Outputs
Q,QN

Truth Table

INPUTS		OUTPUTS			
		OLD		NEW	
D	CK	Q	QN	Q	QN
X	0	0	1	0	1
X	0	1	0	1	0
0	1	X	X	0	1
1	1	X	X	1	0

X = Don't care

Capacitances

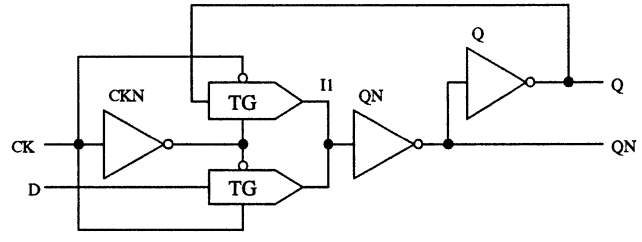
	D	CK
Area	0.026pF	0.071pF
Perf	0.048pF	0.225pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CK ↑	Q ↓	9.05ns/pF	1.75ns	1.69ns/pF	0.95ns
CK ↑	Q ↑	6.55ns/pF	2.04ns	1.38ns/pF	1.10ns
CK ↑	QN ↓	1.96ns/pF	1.91ns	0.50ns/pF	0.99ns
CK ↑	QN ↑	3.74ns/pF	1.52ns	0.70ns/pF	0.78ns
D ↓	Q ↓	8.92ns/pF	0.72ns	1.67ns/pF	0.64ns
D ↓	QN ↑	3.61ns/pF	0.49ns	0.68ns/pF	0.47ns
D ↑	Q ↑	6.55ns/pF	1.80ns	1.38ns/pF	0.91ns
D ↑	QN ↓	1.96ns/pF	1.67ns	0.50ns/pF	0.80ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S1B

Positive level sense, positive asynchronous preset.

Grids 9, **Transistors** 12

Inputs
D,CK,PD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PD	Q	QN	Q	QN
X	0	0	0	1	0	1
X	0	X	1	0	1	0
X	X	1	X	X	1	0
0	1	0	X	X	0	1
1	1	X	X	X	1	0

X = Don't care

Capacitances

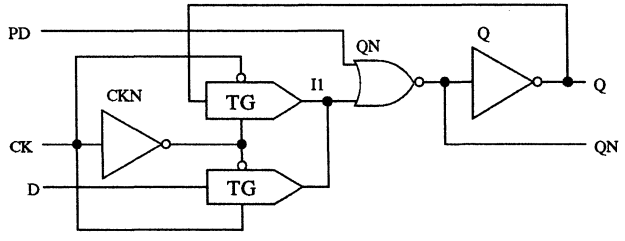
	D	CK	PD
Area	0.026pF	0.070pF	0.034pF
Perf	0.048pF	0.224pF	0.145pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CK ↑	Q ↓	14.62ns/pF	1.67ns	2.68ns/pF	1.03ns
CK ↑	Q ↑	6.64ns/pF	1.86ns	1.33ns/pF	1.10ns
CK ↑	QN ↓	2.18ns/pF	1.71ns	0.47ns/pF	1.01ns
CK ↑	QN ↑	7.00ns/pF	1.41ns	1.28ns/pF	0.80ns
D ↓	Q ↓	14.49ns/pF	0.68ns	2.66ns/pF	0.71ns
D ↓	QN ↑	6.87ns/pF	0.42ns	1.25ns/pF	0.49ns
D ↑	Q ↑	6.64ns/pF	1.62ns	1.33ns/pF	0.91ns
D ↑	QN ↓	2.18ns/pF	1.48ns	0.47ns/pF	0.82ns
PD ↑	Q ↑	6.95ns/pF	1.62ns	1.38ns/pF	0.63ns
PD ↑	QN ↓	2.50ns/pF	1.48ns	0.52ns/pF	0.54ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S1D

Positive level sense, positive asynchronous clear.

Grids 10, **Transistors** 14

Inputs
D,CK,CD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CD	Q	QN	Q	QN
X	0	X	0	1	0	1
X	0	0	1	0	1	0
X	X	1	X	X	0	1
0	1	X	X	X	0	1
1	1	0	X	X	1	0

X = Don't care

Capacitances

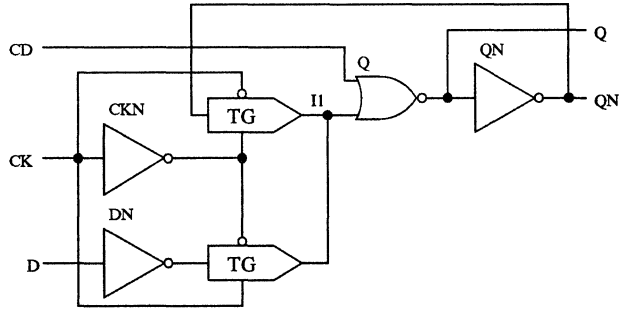
	D	CK	CD
Area	0.034pF	0.075pF	0.034pF
Perf	0.145pF	0.230pF	0.145pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CD ↑	Q ↓	2.50ns/pF	1.48ns	0.52ns/pF	0.54ns
CD ↑	QN ↑	6.95ns/pF	1.62ns	1.38ns/pF	0.63ns
CK ↑	Q ↓	2.18ns/pF	1.71ns	0.47ns/pF	1.01ns
CK ↑	Q ↑	7.00ns/pF	1.41ns	1.28ns/pF	0.80ns
CK ↑	QN ↓	14.62ns/pF	1.67ns	2.68ns/pF	1.03ns
CK ↑	QN ↑	6.64ns/pF	1.86ns	1.33ns/pF	1.10ns
D ↓	Q ↓	2.18ns/pF	1.09ns	0.47ns/pF	0.87ns
D ↓	QN ↑	6.64ns/pF	1.24ns	1.33ns/pF	0.95ns
D ↑	Q ↑	6.87ns/pF	1.33ns	1.25ns/pF	0.87ns
D ↑	QN ↓	14.49ns/pF	1.59ns	2.66ns/pF	1.10ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S1E

Positive level sense, negative asynchronous clear.

Grids 9, **Transistors** 12

Inputs
D,CK,CDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CDN	Q	QN	Q	QN
X	0	X	0	1	0	1
X	0	1	1	0	1	0
X	X	0	X	X	0	1
0	1	X	X	X	0	1
1	1	1	X	X	1	0

X = Don't care

Capacitances

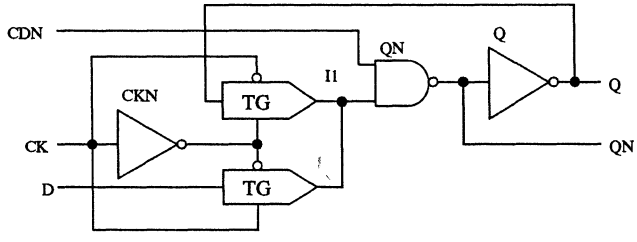
	D	CK	CDN
Area	0.026pF	0.070pF	0.034pF
Perf	0.048pF	0.224pF	0.145pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	Q ↓	8.96ns/pF	0.74ns	1.67ns/pF	0.45ns
CDN ↓	QN ↑	3.74ns/pF	0.57ns	0.68ns/pF	0.32ns
CK ↑	Q ↓	9.01ns/pF	1.63ns	1.64ns/pF	0.99ns
CK ↑	Q ↑	8.87ns/pF	2.17ns	1.98ns/pF	1.06ns
CK ↑	QN ↓	3.61ns/pF	2.06ns	0.94ns/pF	0.93ns
CK ↑	QN ↑	3.79ns/pF	1.45ns	0.65ns/pF	0.87ns
D ↓	Q ↓	8.87ns/pF	0.64ns	1.64ns/pF	0.61ns
D ↓	QN ↑	3.66ns/pF	0.46ns	0.65ns/pF	0.49ns
D ↑	Q ↑	8.87ns/pF	1.93ns	1.98ns/pF	0.87ns
D ↑	QN ↓	3.61ns/pF	1.82ns	0.94ns/pF	0.74ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S1F

Positive level sense, negative asynchronous clear, positive asynchronous preset.

Grids 11, **Transistors** 14

Inputs
D,CK,PD,CDN

Outputs
Q,QN

Capacitances

	D	CK	PD	CDN
Area	0.026pF	0.070pF	0.034pF	0.034pF
Perf	0.048pF	0.224pF	0.145pF	0.145pF

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	CK	PD	CDN	Q	QN	Q	QN
X	0	0	X	0	1	0	1
X	0	X	1	1	0	1	0
X	X	X	0	X	X	0	1
X	X	1	1	X	X	1	0
0	1	0	X	X	X	0	1
1	1	X	1	X	X	1	0

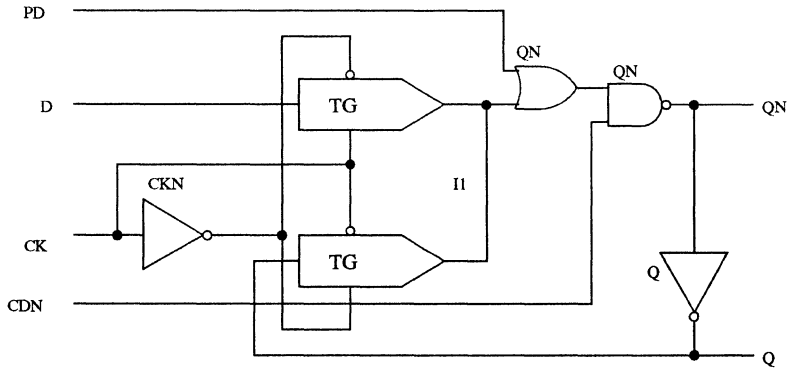
X = Don't care

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	Q ↓	11.28ns/pF	0.77ns	2.14ns/pF	0.36ns
CDN ↓	QN ↑	4.01ns/pF	0.44ns	0.76ns/pF	0.21ns
CK ↑	Q ↓	14.40ns/pF	1.82ns	2.68ns/pF	1.03ns
CK ↑	Q ↑	8.87ns/pF	2.22ns	1.90ns/pF	1.26ns
CK ↑	QN ↓	3.74ns/pF	2.09ns	0.89ns/pF	1.16ns
CK ↑	QN ↑	7.13ns/pF	1.49ns	1.30ns/pF	0.88ns
D ↓	Q ↓	14.27ns/pF	0.83ns	2.68ns/pF	0.65ns
D ↓	QN ↑	7.00ns/pF	0.50ns	1.30ns/pF	0.50ns
D ↑	Q ↑	8.87ns/pF	1.98ns	1.90ns/pF	1.07ns
D ↑	QN ↓	3.74ns/pF	1.85ns	0.89ns/pF	0.97ns
PD ↑	Q ↑	9.27ns/pF	1.70ns	1.93ns/pF	0.72ns
PD ↑	QN ↓	4.15ns/pF	1.57ns	0.91ns/pF	0.61ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S1G

Positive level sense, negative asynchronous preset.

Grids 10, **Transistors** 14

Inputs
D,CK,PDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PDN	Q	QN	Q	QN
X	0	1	0	1	0	1
X	0	X	1	0	1	0
X	X	0	X	X	1	0
0	1	1	X	X	0	1
1	1	X	X	X	1	0

X = Don't care

Capacitances

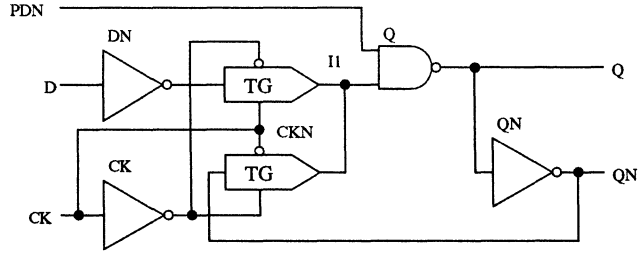
	D	CK	PDN
Area	0.034pF	0.075pF	0.034pF
Perf	0.145pF	0.230pF	0.145pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CK ↑	Q ↓	3.61ns/pF	2.06ns	0.94ns/pF	0.93ns
CK ↑	Q ↑	3.79ns/pF	1.45ns	0.65ns/pF	0.87ns
CK ↑	QN ↓	9.01ns/pF	1.63ns	1.64ns/pF	0.99ns
CK ↑	QN ↑	8.87ns/pF	2.17ns	1.98ns/pF	1.06ns
D ↓	Q ↓	3.61ns/pF	1.44ns	0.96ns/pF	0.72ns
D ↓	QN ↑	8.87ns/pF	1.55ns	2.01ns/pF	0.85ns
D ↑	Q ↑	3.66ns/pF	1.37ns	0.65ns/pF	0.87ns
D ↑	QN ↓	8.87ns/pF	1.55ns	1.64ns/pF	0.99ns
PDN ↓	Q ↑	3.74ns/pF	0.57ns	0.68ns/pF	0.32ns
PDN ↓	QN ↓	8.96ns/pF	0.74ns	1.67ns/pF	0.45ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2AX

Negative edge triggered.

Grids 13, **Transistors** 18

Inputs
D,CKA,CKB

Outputs
Q,QN

Truth Table

INPUTS		OUTPUTS			
		OLD		NEW	
D	CK	Q	QN	Q	QN
0	↓	X	X	0	1
1	↓	X	X	1	0

X = Don't care

Capacitances

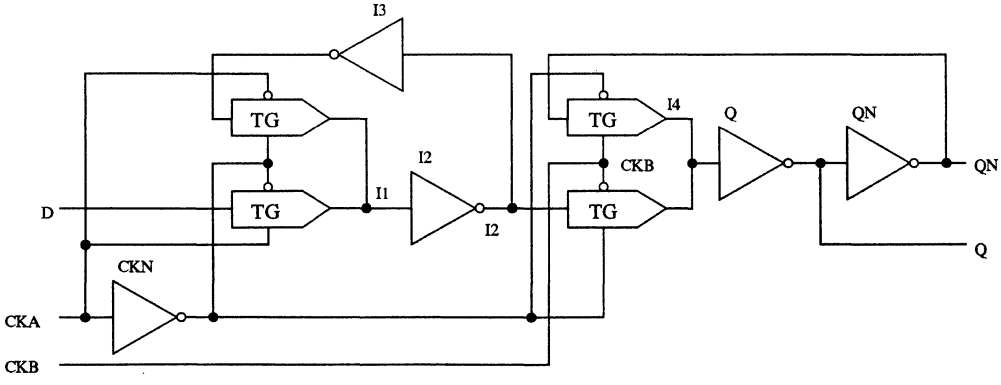
	D	CKA	CKB
Area	0.026pF	0.070pF	0.037pF
Perf	0.048pF	0.223pF	0.082pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	0.67ns	0.57ns	CK ↑	Q ↓	1.96ns/pF	1.20ns	0.47ns/pF	0.82ns
D ↑	1.67ns	0.86ns	CK ↑	Q ↑	3.61ns/pF	1.15ns	0.65ns/pF	0.77ns
			CK ↑	QN ↓	8.92ns/pF	1.34ns	1.67ns/pF	0.88ns
			CK ↑	QN ↑	6.55ns/pF	1.28ns	1.36ns/pF	0.88ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2BX

Negative edge triggered, positive asynchronous preset.

Grids 16, **Transistors** 22

Inputs
D,CKA,CKB,PD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PD	Q	QN	Q	QN
X	X	1	X	X	1	0
0	↓	0	X	X	0	1
1	↓	X	X	X	1	0

X = Don't care

Capacitances

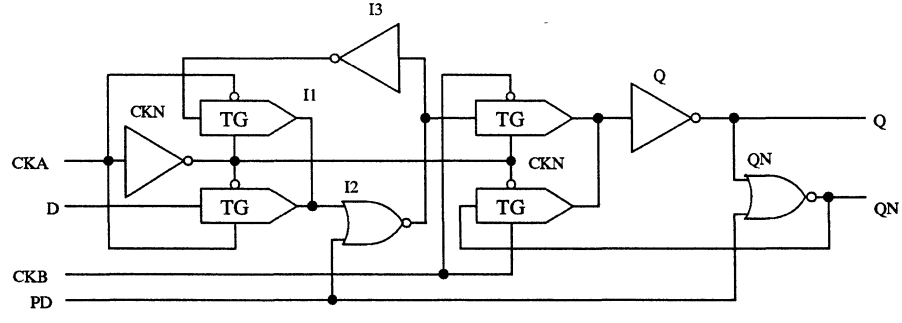
	D	CKA	CKB	PD
Area	0.026pF	0.070pF	0.036pF	0.073pF
Perf	0.048pF	0.224pF	0.081pF	0.298pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.05ns	0.76ns	CK ↑	Q ↓	2.14ns/pF	1.11ns	0.47ns/pF	0.87ns
D ↑	1.67ns	0.91ns	CK ↑	Q ↑	3.88ns/pF	0.98ns	0.68ns/pF	0.80ns
			CK ↑	QN ↓	9.23ns/pF	1.24ns	1.72ns/pF	0.93ns
			CK ↑	QN ↑	9.36ns/pF	1.42ns	1.85ns/pF	1.02ns
			PD ↑	Q ↑	6.55ns/pF	1.66ns	1.20ns/pF	0.91ns
			PD ↑	QN ↓	2.90ns/pF	1.20ns	0.57ns/pF	0.41ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2CX

Negative edge triggered, positive asynchronous clear, positive asynchronous preset.

Grids 21, **Transistors** 28

Inputs
D,CKA,CKB,PDA,PDB,CD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	CK	PD	CD	Q	QN	Q	QN
X	X	X	1	X	X	0	1
X	X	1	0	X	X	1	0
0	↓	0	X	X	X	0	1
1	↓	X	0	X	X	1	0

X = Don't care

Capacitances

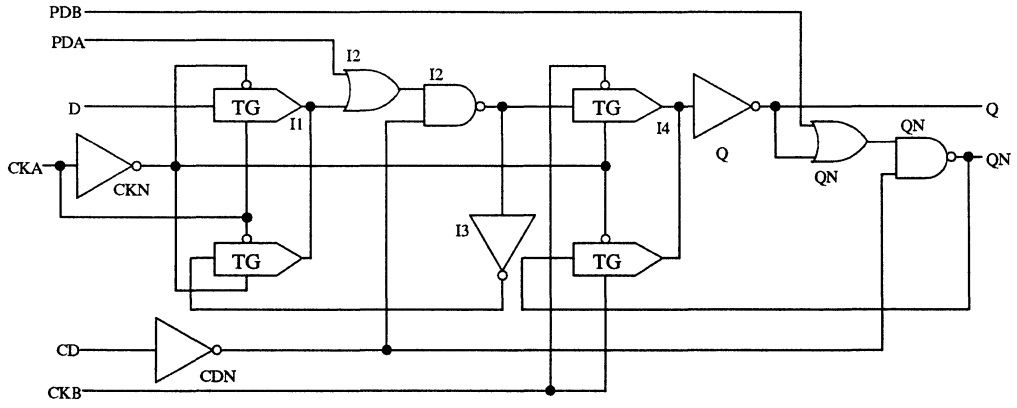
	D	CKA	CKB	PDA	PDB	CD
Area	0.026pF	0.070pF	0.035pF	0.034pF	0.034pF	0.034pF
Perf	0.048pF	0.224pF	0.080pF	0.145pF	0.145pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.10ns	0.86ns	CD ↑	Q ↓	9.09ns/pF	2.69ns	1.67ns/pF	1.45ns
D ↑	1.91ns	1.00ns	CD ↑	QN ↑	3.88ns/pF	1.27ns	0.78ns/pF	0.53ns
			CK ↑	Q ↓	1.96ns/pF	1.39ns	0.44ns/pF	0.89ns
			CK ↑	Q ↑	3.66ns/pF	1.32ns	0.65ns/pF	0.82ns
			CK ↑	QN ↓	10.70ns/pF	1.71ns	2.06ns/pF	1.04ns
			CK ↑	QN ↑	9.27ns/pF	1.89ns	1.82ns/pF	1.13ns
			PD ↑	Q ↑	8.11ns/pF	1.94ns	1.51ns/pF	1.14ns
			PD ↑	QN ↓	4.50ns/pF	1.27ns	0.83ns/pF	0.68ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2DX

Negative edge triggered, positive asynchronous clear.

Grids 17, **Transistors** 24

Inputs
D,CKA,CKB,CD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CD	Q	QN	Q	QN
X	X	1	X	X	0	1
0	↓	X	X	X	0	1
1	↓	0	X	X	1	0

X = Don't care

Capacitances

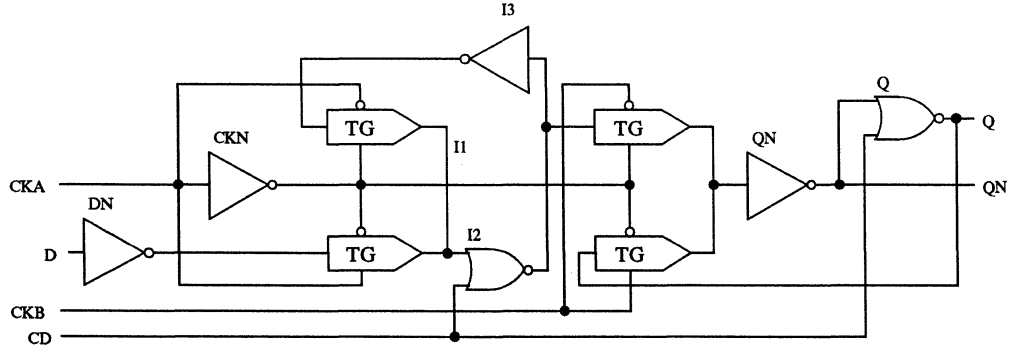
	D	CKA	CKB	CD
Area	0.034pF	0.075pF	0.036pF	0.073pF
Perf	0.145pF	0.230pF	0.081pF	0.298pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D ↓	1.29ns	0.95ns	CD ↑	Q ↓	2.90ns/pF	1.20ns	0.57ns/pF	0.41ns
D ↑	1.96ns	1.14ns	CD ↑	QN ↑	6.55ns/pF	1.66ns	1.20ns/pF	0.91ns
			CK ↑	Q ↓	9.23ns/pF	1.24ns	1.72ns/pF	0.93ns
			CK ↑	Q ↑	9.36ns/pF	1.42ns	1.85ns/pF	1.02ns
			CK ↑	QN ↓	2.14ns/pF	1.11ns	0.47ns/pF	0.87ns
			CK ↑	QN ↑	3.88ns/pF	0.98ns	0.68ns/pF	0.80ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2EX

Negative edge triggered, negative asynchronous clear.

Grids 16, **Transistors** 22

Inputs
D,CKA,CKB,CDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CDN	Q	QN	Q	QN
X	X	0	X	X	0	1
0	↓	X	X	X	0	1
1	↓	1	X	X	1	0

X = Don't care

Capacitances

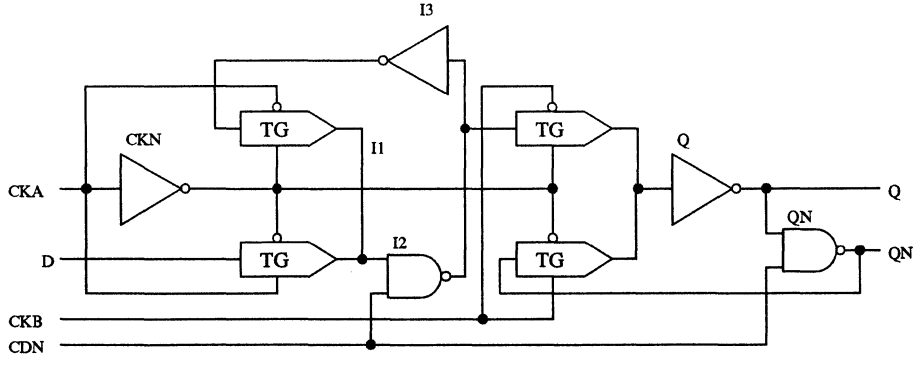
	D	CKA	CKB	CDN
Area	0.026pF	0.070pF	0.035pF	0.071pF
Perf	0.048pF	0.224pF	0.080pF	0.296pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	0.72ns	0.62ns	CDN ↓	Q ↓	7.00ns/pF	1.60ns	1.43ns/pF	0.78ns
D ↑	1.86ns	1.00ns	CDN ↓	QN ↑	3.70ns/pF	0.59ns	0.78ns/pF	0.10ns
			CK ↑	Q ↓	1.87ns/pF	1.24ns	0.47ns/pF	0.82ns
			CK ↑	Q ↑	3.61ns/pF	1.11ns	0.65ns/pF	0.77ns
			CK ↑	QN ↓	10.39ns/pF	1.38ns	2.01ns/pF	0.94ns
			CK ↑	QN ↑	6.51ns/pF	1.39ns	1.38ns/pF	0.91ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2FX

Negative edge triggered, negative asynchronous clear, positive asynchronous preset.

Grids 19, **Transistors** 26

Inputs
D,CKA,CKB,PDA,PDB,CDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	CK	PD	CDN	Q	QN	Q	QN
X	X	X	0	X	X	0	1
X	X	1	1	X	X	1	0
0	↓	0	X	X	X	0	1
1	↓	X	1	X	X	1	0

X = Don't care

Capacitances

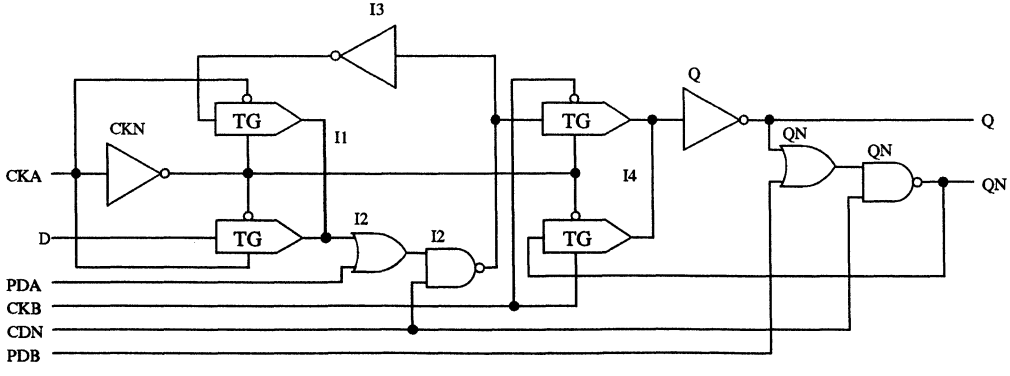
	D	CKA	CKB	PDA	PDB	CDN
Area	0.026pF	0.070pF	0.035pF	0.034pF	0.034pF	0.071pF
Perf	0.048pF	0.224pF	0.080pF	0.145pF	0.145pF	0.296pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.14ns	0.86ns	CDN ↓	Q ↓	8.92ns/pF	2.00ns	1.59ns/pF	1.18ns
D ↑	1.91ns	1.00ns	CDN ↓	QN ↑	3.66ns/pF	0.61ns	0.68ns/pF	0.28ns
			CK ↑	Q ↓	2.01ns/pF	1.37ns	0.44ns/pF	0.89ns
			CK ↑	Q ↑	3.66ns/pF	1.32ns	0.65ns/pF	0.82ns
			CK ↑	QN ↓	10.65ns/pF	1.73ns	2.03ns/pF	1.11ns
			CK ↑	QN ↑	9.32ns/pF	1.87ns	1.82ns/pF	1.18ns
			PD ↑	Q ↑	8.07ns/pF	1.96ns	1.90ns/pF	0.88ns
			PD ↑	QN ↓	4.46ns/pF	1.29ns	1.23ns/pF	0.42ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2GX

Negative edge triggered, negative asynchronous preset.

Grids 17, **Transistors** 24

Inputs
D,CKA,CKB,PDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PDN	Q	QN	Q	QN
X	X	0	X	X	1	0
0	↓	1	X	X	0	1
1	↓	X	X	X	1	0

X = Don't care

Capacitances

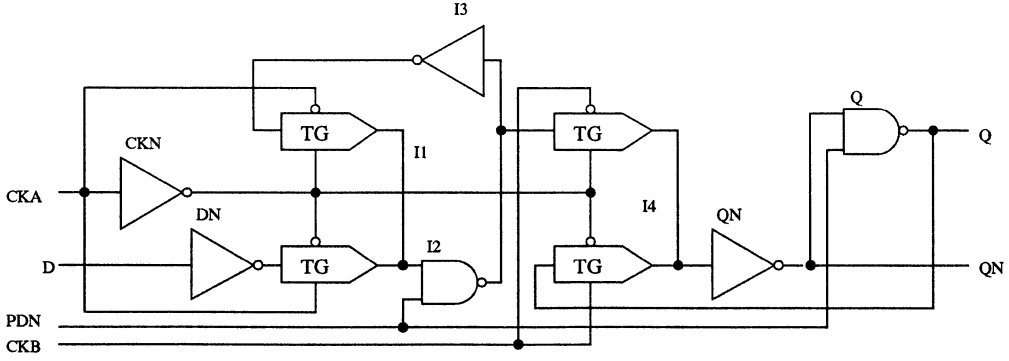
	D	CKA	CKB	PDN
Area	0.034pF	0.076pF	0.035pF	0.071pF
Perf	0.145pF	0.234pF	0.080pF	0.296pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D ↓	1.48ns	1.05ns	CK ↑	Q ↓	10.39ns/pF	1.38ns	2.01ns/pF	0.94ns
D ↑	1.62ns	1.05ns	CK ↑	Q ↑	6.51ns/pF	1.39ns	1.38ns/pF	0.91ns
			CK ↑	QN ↓	1.87ns/pF	1.24ns	0.47ns/pF	0.82ns
			CK ↑	QN ↑	3.61ns/pF	1.11ns	0.65ns/pF	0.77ns
			PDN ↓	Q ↑	3.70ns/pF	0.59ns	0.78ns/pF	0.10ns
			PDN ↓	QN ↓	7.00ns/pF	1.60ns	1.43ns/pF	0.78ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2IX

Negative edge triggered, positive synchronous clear.

Grids 18, **Transistors** 24

Inputs
D,CKA,CKB,CD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CD	Q	QN	Q	QN
X	↓	1	X	X	0	1
0	↓	X	X	X	0	1
1	↓	0	X	X	1	0

X = Don't care

Capacitances

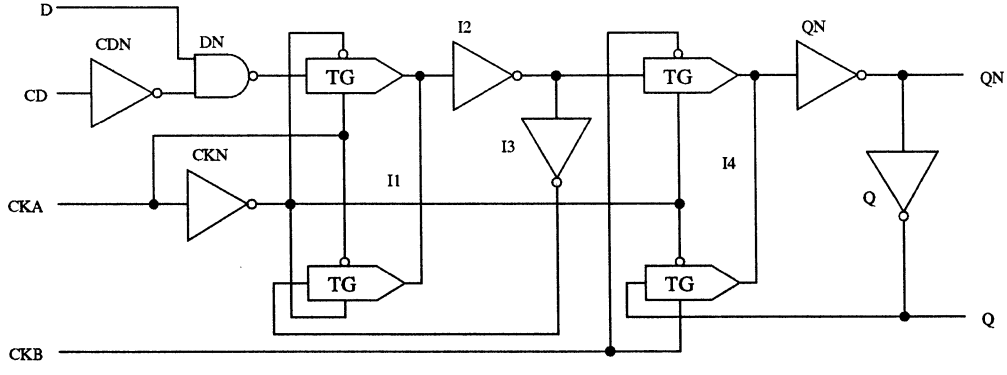
	D	CKA	CKB	CD
Area	0.034pF	0.070pF	0.036pF	0.034pF
Perf	0.145pF	0.223pF	0.081pF	0.145pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
CD ↓	1.91ns	1.19ns	CK ↑	Q ↓	8.92ns/pF	1.34ns	1.67ns/pF	0.88ns
CD ↑	2.05ns	1.24ns	CK ↑	Q ↑	6.55ns/pF	1.28ns	1.33ns/pF	0.91ns
D ↓	1.48ns	0.91ns	CK ↑	QN ↓	1.96ns/pF	1.20ns	0.44ns/pF	0.84ns
D ↑	1.96ns	1.10ns	CK ↑	QN ↑	3.61ns/pF	1.15ns	0.65ns/pF	0.77ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2JX

Negative edge triggered, positive synchronous preset.

Grids 16, **Transistors** 22

Inputs
D,CKA,CKB,PD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PD	Q	QN	Q	QN
X	↓	1	X	X	1	0
0	↓	0	X	X	0	1
1	↓	X	X	X	1	0

X = Don't care

Capacitances

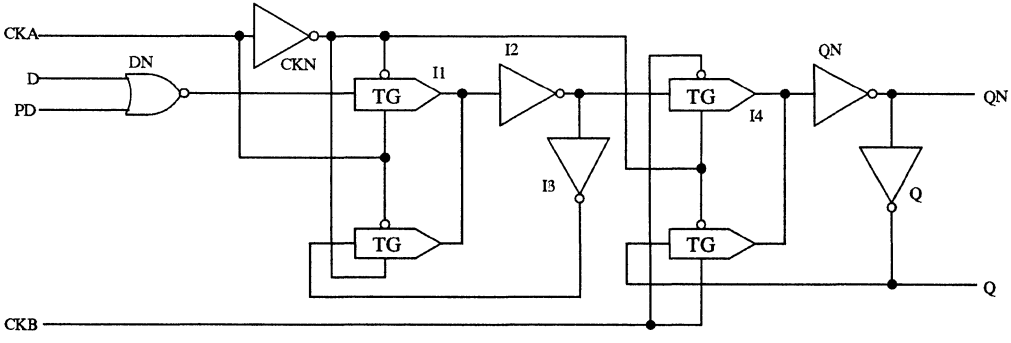
	D	CKA	CKB	PD
Area	0.034pF	0.073pF	0.036pF	0.034pF
Perf	0.145pF	0.226pF	0.081pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.91ns	1.19ns	CK ↑	Q ↓	8.92ns/pF	1.38ns	1.67ns/pF	0.88ns
D ↑	1.72ns	1.00ns	CK ↑	Q ↑	6.55ns/pF	1.33ns	1.33ns/pF	0.91ns
PD ↓	1.91ns	1.19ns	CK ↑	QN ↓	1.96ns/pF	1.24ns	0.44ns/pF	0.84ns
PD ↑	1.72ns	1.00ns	CK ↑	QN ↑	3.61ns/pF	1.20ns	0.65ns/pF	0.77ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2KX

Negative edge triggered, negative asynchronous clear, negative asynchronous preset.

Grids 22, **Transistors** 30

Inputs
D,CKA,CKB,PDNA,PDNB,CDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	CK	PDN	CDN	Q	QN	Q	QN
X	X	X	0	X	X	0	1
X	X	0	1	X	X	1	0
0	↓	1	X	X	X	0	1
1	↓	X	1	X	X	1	0

X = Don't care

Capacitances

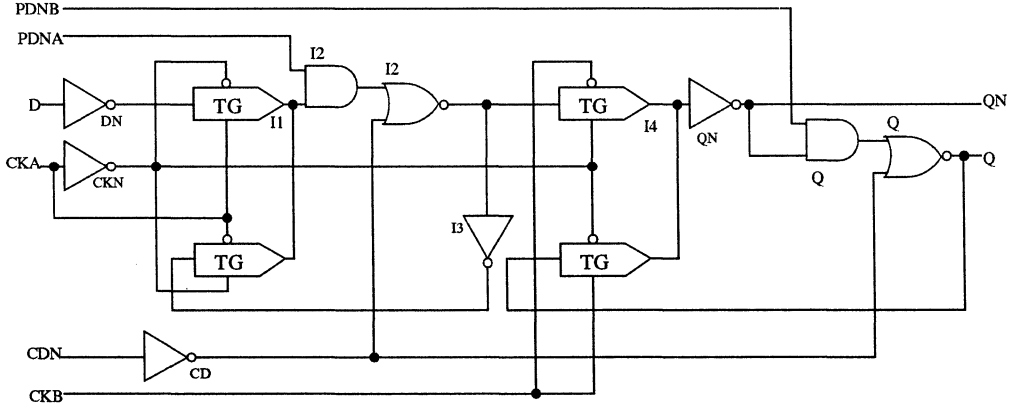
	D	CKA	CKB	PDNA	PDNB	CDN
Area	0.034pF	0.070pF	0.036pF	0.034pF	0.034pF	0.034pF
Perf	0.145pF	0.224pF	0.081pF	0.145pF	0.145pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.53ns	1.05ns	CDN ↓	Q ↓	2.10ns/pF	1.04ns	0.16ns/pF	1.50ns
D ↑	2.10ns	1.24ns	CDN ↓	QN ↑	5.71ns/pF	1.72ns	0.83ns/pF	1.96ns
			CK ↑	Q ↓	10.74ns/pF	1.45ns	2.03ns/pF	1.07ns
			CK ↑	Q ↑	9.45ns/pF	1.66ns	1.85ns/pF	1.11ns
			CK ↑	QN ↓	2.14ns/pF	1.11ns	0.44ns/pF	0.89ns
			CK ↑	QN ↑	3.83ns/pF	1.05ns	0.65ns/pF	0.82ns
			PDN ↓	Q ↑	6.55ns/pF	0.90ns	1.25ns/pF	0.35ns
			PDN ↓	QN ↓	11.95ns/pF	2.37ns	2.19ns/pF	1.23ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2LX

Negative edge triggered, negative synchronous preset.

Grids 18, **Transistors** 24

Inputs
D,CKA,CKB,PDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PDN	Q	QN	Q	QN
X	↓	0	X	X	1	0
0	↓	1	X	X	0	1
1	↓	X	X	X	1	0

X = Don't care

Capacitances

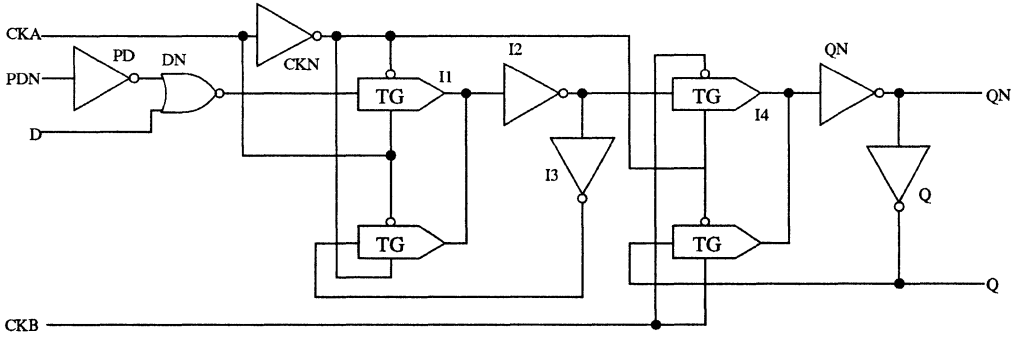
	D	CKA	CKB	PDN
Area	0.034pF	0.070pF	0.036pF	0.034pF
Perf	0.145pF	0.223pF	0.081pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	2.00ns	1.19ns	CK ↑	Q ↓	8.92ns/pF	1.34ns	1.67ns/pF	0.88ns
D ↑	1.76ns	1.00ns	CK ↑	Q ↑	6.55ns/pF	1.28ns	1.33ns/pF	0.91ns
PDN ↓	1.76ns	1.14ns	CK ↑	QN ↓	1.96ns/pF	1.20ns	0.44ns/pF	0.84ns
PDN ↑	2.58ns	1.48ns	CK ↑	QN ↑	3.61ns/pF	1.15ns	0.65ns/pF	0.77ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2MX

Negative edge triggered, negative synchronous clear.

Grids 15, **Transistors** 22

Inputs
D,CKA,CKB,CDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CDN	Q	QN	Q	QN
X	↓	0	X	X	0	1
0	↓	X	X	X	0	1
1	↓	1	X	X	1	0

X = Don't care

Capacitances

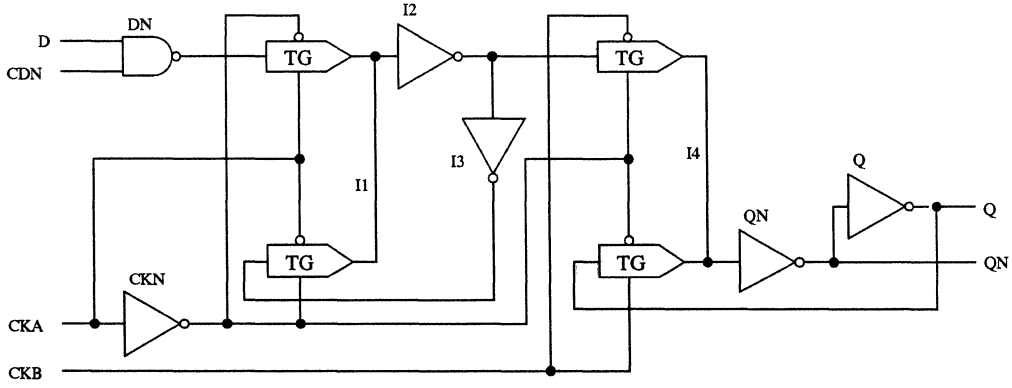
	D	CKA	CKB	CDN
Area	0.034pF	0.073pF	0.036pF	0.034pF
Perf	0.145pF	0.226pF	0.081pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	1.43ns	0.91ns	CK ↑	Q ↓	9.01ns/pF	1.20ns	1.67ns/pF	0.88ns
CDN ↑	1.86ns	1.10ns	CK ↑	Q ↑	6.55ns/pF	1.23ns	1.33ns/pF	0.91ns
D ↓	1.43ns	0.91ns	CK ↑	QN ↓	1.96ns/pF	1.15ns	0.44ns/pF	0.84ns
D ↑	1.86ns	1.10ns	CK ↑	QN ↑	3.70ns/pF	1.02ns	0.65ns/pF	0.77ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2NX

Negative edge triggered, positive asynchronous clear, negative asynchronous preset.

Grids 20, **Transistors** 28

Inputs
D,CKA,CKB,PDNA,PDNB,CD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	CK	PDN	CD	Q	QN	Q	QN
X	X	X	1	X	X	0	1
X	X	0	0	X	X	1	0
0	↓	1	X	X	X	0	1
1	↓	X	0	X	X	1	0

X = Don't care

Capacitances

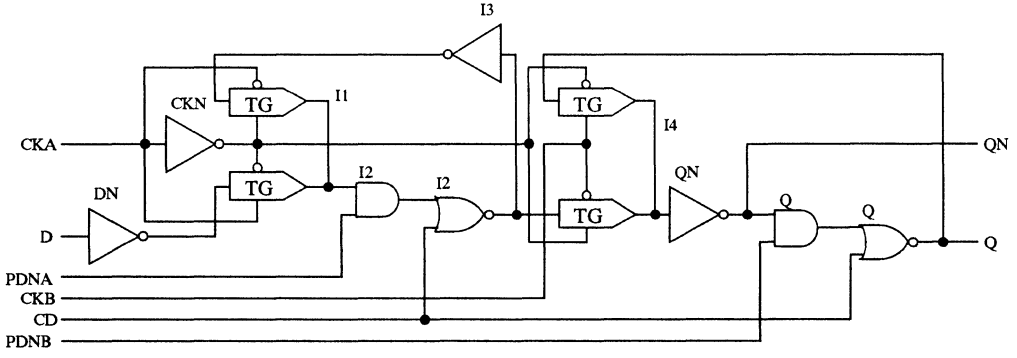
	D	CKA	CKB	PDNA	PDNB	CD
Area	0.034pF	0.072pF	0.036pF	0.034pF	0.034pF	0.071pF
Perf	0.145pF	0.225pF	0.081pF	0.145pF	0.145pF	0.295pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
D ↓	1.53ns	1.05ns	CD ↑	Q ↓	2.32ns/pF	1.56ns	0.26ns/pF	1.08ns
D ↑	2.15ns	1.24ns	CD ↑	QN ↑	5.93ns/pF	2.23ns	0.94ns/pF	1.55ns
			CK ↑	Q ↓	10.57ns/pF	1.72ns	2.06ns/pF	1.04ns
			CK ↑	Q ↑	9.36ns/pF	1.85ns	1.90ns/pF	1.07ns
			CK ↑	QN ↓	2.01ns/pF	1.37ns	0.50ns/pF	0.80ns
			CK ↑	QN ↑	3.66ns/pF	1.32ns	0.70ns/pF	0.73ns
			PDN ↓	Q ↑	6.60ns/pF	0.83ns	1.25ns/pF	0.39ns
			PDN ↓	QN ↓	12.04ns/pF	2.29ns	2.19ns/pF	1.32ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2OX

Negative edge triggered, positive synchronous clear, positive synchronous preset.

Grids 19, **Transistors** 26

Inputs
D,CKA,CKB,PD,CD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	CK	PD	CD	Q	QN	Q	QN
X	↓	X	1	X	X	0	1
X	↓	1	0	X	X	1	0
0	↓	0	X	X	X	0	1
1	↓	X	0	X	X	1	0

X = Don't care

Capacitances

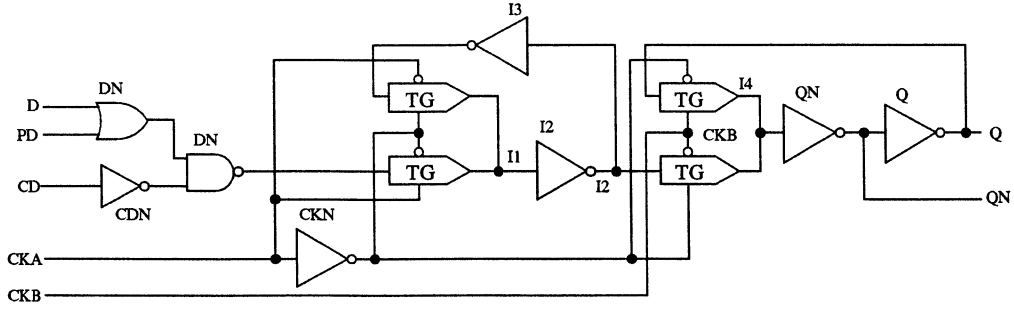
	D	CKA	CKB	PD	CD
Area	0.061pF	0.097pF	0.063pF	0.061pF	0.061pF
Perf	0.222pF	0.300pF	0.158pF	0.222pF	0.222pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CD ↓	1.91ns	1.24ns	CK ↑	Q ↓	8.92ns/pF	1.34ns	1.67ns/pF	0.88ns
CD ↑	2.48ns	1.43ns	CK ↑	Q ↑	6.55ns/pF	1.28ns	1.33ns/pF	0.91ns
D ↓	2.05ns	1.19ns	CK ↑	QN ↓	1.96ns/pF	1.20ns	0.44ns/pF	0.84ns
D ↑	2.00ns	1.14ns	CK ↑	QN ↑	3.61ns/pF	1.15ns	0.65ns/pF	0.77ns
PD ↓	2.05ns	1.19ns						
PD ↑	2.00ns	1.14ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3AX

Positive edge triggered.

Grids 13, **Transistors** 18

Inputs
D,CKA,CKB

Outputs
Q,QN

Truth Table

INPUTS		OUTPUTS			
		OLD		NEW	
D	CK	Q	QN	Q	QN
0	↑	X	X	0	1
1	↑	X	X	1	0

X = Don't care

Capacitances

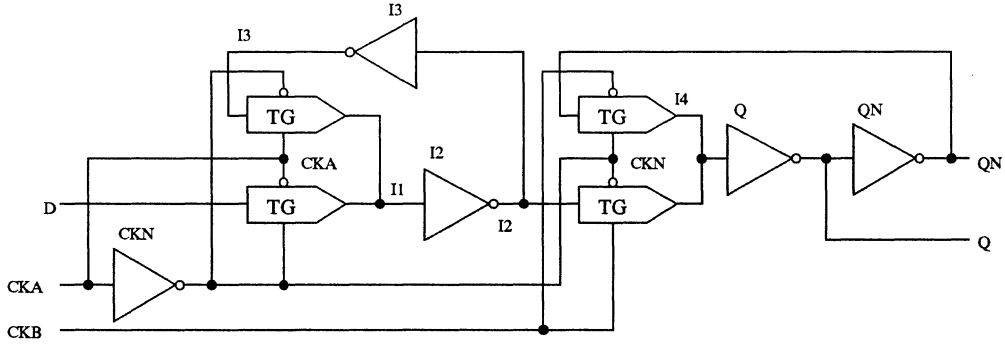
	D	CKA	CKB
Area	0.026pF	0.070pF	0.036pF
Perf	0.048pF	0.223pF	0.081pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	0.62ns	0.57ns	CK ↑	Q ↓	1.96ns/pF	1.91ns	0.47ns/pF	1.06ns
D ↑	1.72ns	0.91ns	CK ↑	Q ↑	3.70ns/pF	1.78ns	0.65ns/pF	1.01ns
			CK ↑	QN ↓	9.01ns/pF	1.96ns	1.67ns/pF	1.11ns
			CK ↑	QN ↑	6.55ns/pF	1.99ns	1.36ns/pF	1.12ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3BX

Positive edge triggered, positive asynchronous preset.

Grids 16, **Transistors** 22

Inputs
D,CKA,CKB,PD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PD	Q	QN	Q	QN
X	X	1	X	X	1	0
0	↑	0	X	X	0	1
1	↑	X	X	X	1	0

X = Don't care

Capacitances

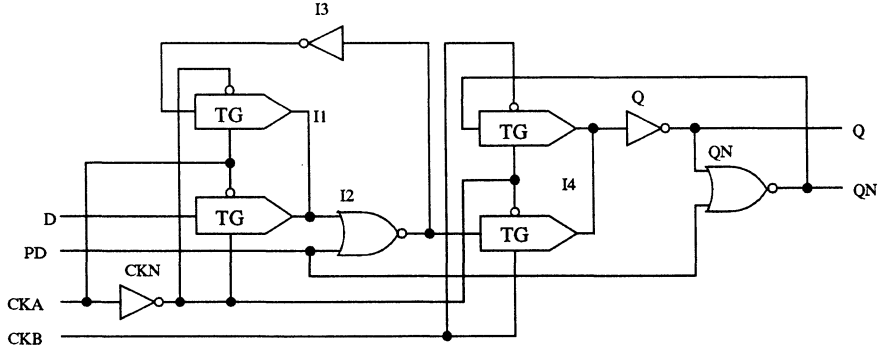
	D	CKA	CKB	PD
Area	0.026pF	0.070pF	0.035pF	0.071pF
Perf	0.048pF	0.224pF	0.080pF	0.296pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D ↓	1.00ns	0.76ns	CK ↑	Q ↓	1.83ns/pF	1.97ns	0.44ns/pF	1.13ns
D ↑	1.67ns	0.95ns	CK ↑	Q ↑	3.57ns/pF	1.84ns	0.65ns/pF	1.06ns
			CK ↑	QN ↓	8.92ns/pF	2.10ns	1.69ns/pF	1.19ns
			CK ↑	QN ↑	9.05ns/pF	2.28ns	1.82ns/pF	1.28ns
			PD ↑	Q ↑	6.55ns/pF	1.66ns	1.20ns/pF	0.91ns
			PD ↑	QN ↓	2.90ns/pF	1.20ns	0.57ns/pF	0.41ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3CX

Positive edge triggered, positive asynchronous clear, positive asynchronous preset.

Grids 21, **Transistors** 28

Inputs
D,CKA,CKB,PDA,PDB,CD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	CK	PD	CD	Q	QN	Q	QN
X	X	X	1	X	X	0	1
X	X	1	0	X	X	1	0
0	↑	0	X	X	X	0	1
1	↑	X	0	X	X	1	0

X = Don't care

Capacitances

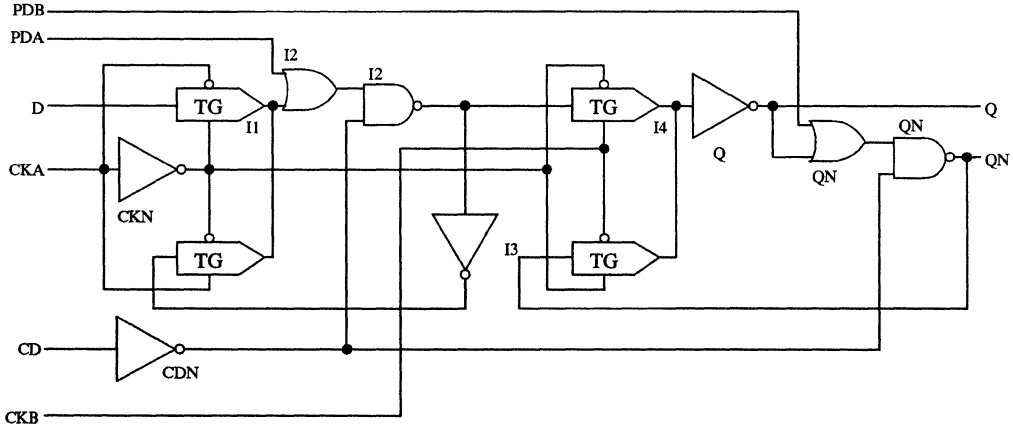
	D	CKA	CKB	PDA	PDB	CD
Area	0.026pF	0.070pF	0.036pF	0.034pF	0.034pF	0.034pF
Perf	0.048pF	0.224pF	0.081pF	0.145pF	0.145pF	0.145pF

Delay Information

Input Signal	Setup Time		From	To	Propagation Delay			
					Area		Performance	
Name	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.05ns	0.86ns	CD ↑	Q ↓	9.09ns/pF	2.69ns	1.67ns/pF	1.45ns
D ↑	1.91ns	1.05ns	CD ↑	QN ↑	3.88ns/pF	1.27ns	0.78ns/pF	0.53ns
			CK ↑	Q ↓	2.18ns/pF	1.81ns	0.47ns/pF	1.06ns
			CK ↑	Q ↑	3.88ns/pF	1.75ns	0.68ns/pF	0.99ns
			CK ↑	QN ↓	10.92ns/pF	2.13ns	2.09ns/pF	1.21ns
			CK ↑	QN ↑	9.50ns/pF	2.31ns	1.85ns/pF	1.30ns
			PD ↑	Q ↑	8.11ns/pF	1.94ns	1.51ns/pF	1.14ns
			PD ↑	QN ↓	4.50ns/pF	1.27ns	0.83ns/pF	0.68ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3DX

Positive edge triggered, positive asynchronous clear.

Grids 17, **Transistors** 24

Inputs
D,CKA,CKB,CD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CD	Q	QN	Q	QN
X	X	1	X	X	0	1
0	↑	X	X	X	0	1
1	↑	0	X	X	1	0

X = Don't care

Capacitances

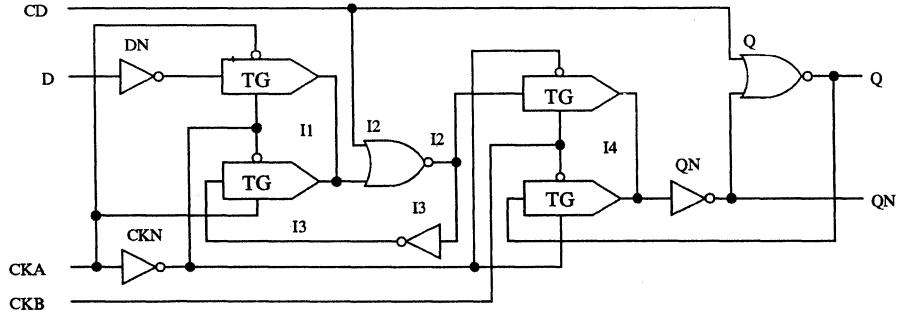
	D	CKA	CKB	CD
Area	0.034pF	0.076pF	0.035pF	0.071pF
Perf	0.145pF	0.231pF	0.080pF	0.296pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.29ns	0.95ns	CD ↑	Q ↓	2.90ns/pF	1.20ns	0.57ns/pF	0.41ns
D ↑	1.96ns	1.14ns	CD ↑	QN ↑	6.55ns/pF	1.66ns	1.20ns/pF	0.91ns
			CK ↑	Q ↓	8.92ns/pF	2.10ns	1.69ns/pF	1.19ns
			CK ↑	Q ↑	9.05ns/pF	2.28ns	1.82ns/pF	1.28ns
			CK ↑	QN ↓	1.83ns/pF	1.97ns	0.44ns/pF	1.13ns
			CK ↑	QN ↑	3.57ns/pF	1.84ns	0.65ns/pF	1.06ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3EX

Positive edge triggered, negative asynchronous clear.

Grids 16, **Transistors** 22

Inputs
D,CKA,CKB,CDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CDN	Q	QN	Q	QN
X	X	0	X	X	0	1
0	↑	X	X	X	0	1
1	↑	1	X	X	1	0

X = Don't care

Capacitances

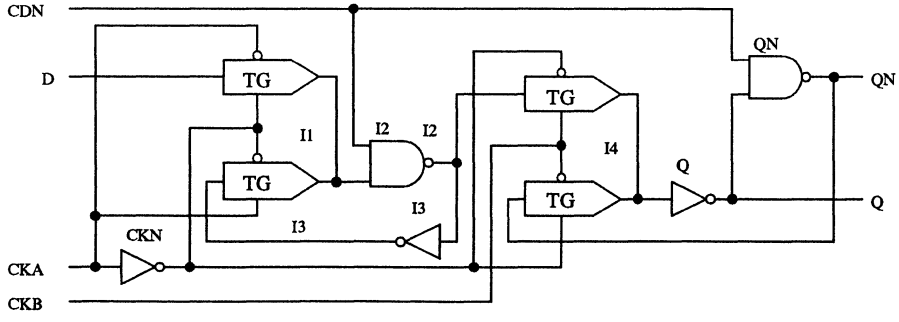
	D	CKA	CKB	CDN
Area	0.026pF	0.070pF	0.036pF	0.073pF
Perf	0.048pF	0.224pF	0.081pF	0.298pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	0.67ns	0.62ns	CDN ↓	Q ↓	7.04ns/pF	1.53ns	1.41ns/pF	0.84ns
D ↑	1.86ns	1.05ns	CDN ↓	QN ↑	3.70ns/pF	0.59ns	0.78ns/pF	0.10ns
			CK ↑	Q ↓	2.10ns/pF	1.90ns	0.44ns/pF	1.13ns
			CK ↑	Q ↑	3.83ns/pF	1.77ns	0.63ns/pF	1.08ns
			CK ↑	QN ↓	10.61ns/pF	2.04ns	1.98ns/pF	1.25ns
			CK ↑	QN ↑	6.73ns/pF	2.06ns	1.36ns/pF	1.22ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3FX

Positive edge triggered, negative asynchronous clear, positive asynchronous preset.

Grids 19, **Transistors** 26

Inputs
D,CKA,CKB,PDA,PDB,CDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	CK	PD	CDN	Q	QN	Q	QN
X	X	X	0	X	X	0	1
X	X	1	1	X	X	1	0
0	↑	0	X	X	X	0	1
1	↑	X	1	X	X	1	0

X = Don't care

Capacitances

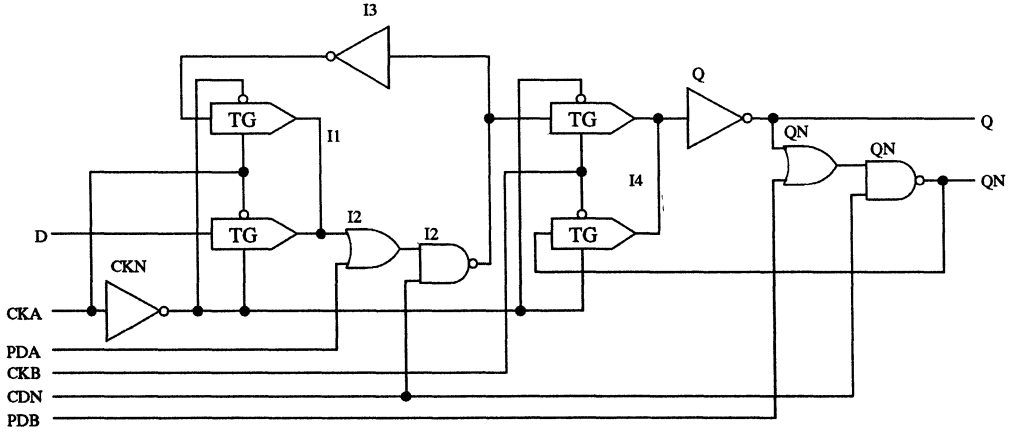
	D	CKA	CKB	PDA	PDB	CDN
Area	0.026pF	0.070pF	0.036pF	0.034pF	0.034pF	0.071pF
Perf	0.048pF	0.224pF	0.081pF	0.145pF	0.145pF	0.296pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D ↓	1.10ns	0.86ns	CDN ↓	Q ↓	8.92ns/pF	2.00ns	1.59ns/pF	1.18ns
D ↑	1.91ns	1.05ns	CDN ↓	QN ↑	3.66ns/pF	0.61ns	0.68ns/pF	0.28ns
			CK ↑	Q ↓	2.23ns/pF	1.79ns	0.47ns/pF	1.06ns
			CK ↑	Q ↑	3.88ns/pF	1.75ns	0.68ns/pF	0.99ns
			CK ↑	QN ↓	10.88ns/pF	2.15ns	2.06ns/pF	1.28ns
			CK ↑	QN ↑	9.54ns/pF	2.29ns	1.85ns/pF	1.35ns
			PD ↑	Q ↑	8.07ns/pF	1.96ns	1.90ns/pF	0.88ns
			PD ↑	QN ↓	4.46ns/pF	1.29ns	1.23ns/pF	0.42ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3GX

Positive edge triggered, negative asynchronous preset.

Grids 17, **Transistors** 24

Inputs
D,CKA,CKB,PDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PDN	Q	QN	Q	QN
X	X	0	X	X	1	0
0	↑	1	X	X	0	1
1	↑	X	X	X	1	0

X = Don't care

Capacitances

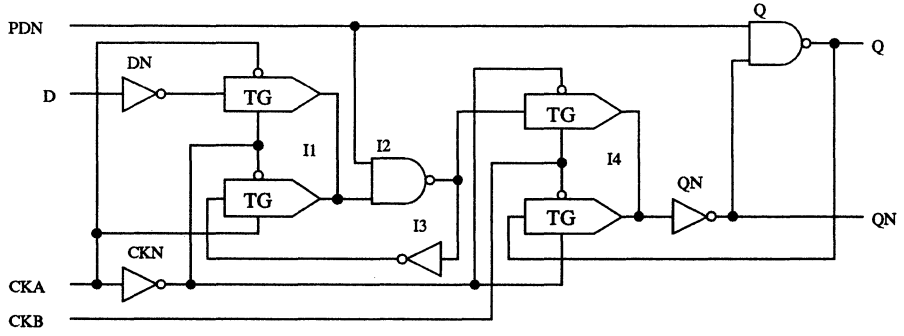
	D	CKA	CKB	PDN
Area	0.034pF	0.075pF	0.036pF	0.073pF
Perf	0.145pF	0.232pF	0.081pF	0.298pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D ↓	1.48ns	1.05ns	CK ↑	Q ↓	10.57ns/pF	2.10ns	1.98ns/pF	1.25ns
D ↑	1.62ns	1.05ns	CK ↑	Q ↑	6.73ns/pF	2.06ns	1.36ns/pF	1.22ns
			CK ↑	QN ↓	2.10ns/pF	1.90ns	0.44ns/pF	1.13ns
			CK ↑	QN ↑	3.79ns/pF	1.83ns	0.63ns/pF	1.08ns
			PDN ↓	Q ↑	3.70ns/pF	0.59ns	0.78ns/pF	0.10ns
			PDN ↓	QN ↓	7.09ns/pF	1.51ns	1.41ns/pF	0.84ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3IX

Positive edge triggered, positive synchronous clear.

Grids 18, **Transistors** 24

Inputs
D,CKA,CKB,CD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CD	Q	QN	Q	QN
X	↑	1	X	X	0	1
0	↑	X	X	X	0	1
1	↑	0	X	X	1	0

X = Don't care

Capacitances

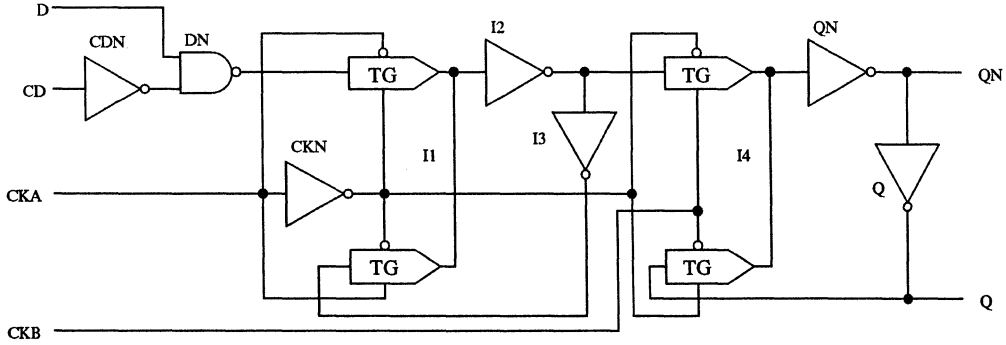
	D	CKA	CKB	CD
Area	0.034pF	0.070pF	0.036pF	0.034pF
Perf	0.145pF	0.223pF	0.081pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CD ↓	1.91ns	1.19ns	CK ↑	Q ↓	8.92ns/pF	2.15ns	1.69ns/pF	1.14ns
CD ↑	2.05ns	1.29ns	CK ↑	Q ↑	6.55ns/pF	2.09ns	1.36ns/pF	1.17ns
D ↓	1.48ns	0.95ns	CK ↑	QN ↓	1.96ns/pF	2.01ns	0.47ns/pF	1.11ns
D ↑	1.96ns	1.10ns	CK ↑	QN ↑	3.61ns/pF	1.96ns	0.68ns/pF	1.04ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3JX

Positive edge triggered, positive synchronous preset.

Grids 16, **Transistors** 22

Inputs
D,CKA,CKB,PD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PD	Q	QN	Q	QN
X	↑	1	X	X	1	0
0	↑	0	X	X	0	1
1	↑	X	X	X	1	0

X = Don't care

Capacitances

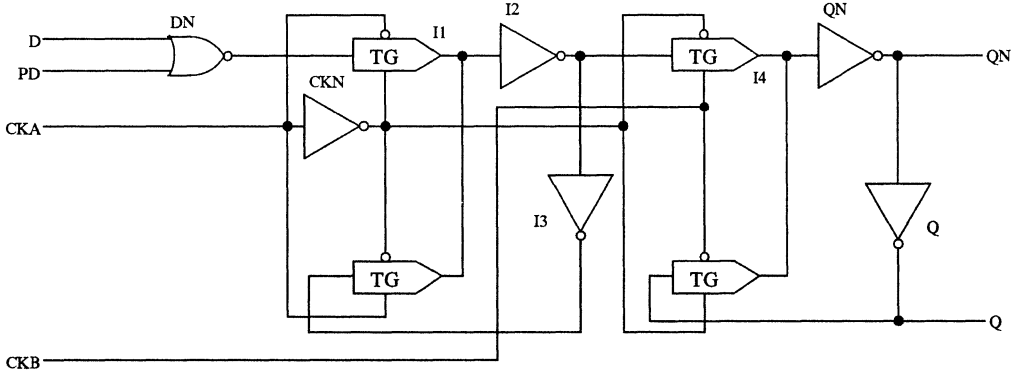
	D	CKA	CKB	PD
Area	0.034pF	0.073pF	0.036pF	0.034pF
Perf	0.145pF	0.226pF	0.081pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.91ns	1.24ns	CK ↑	Q ↓	9.09ns/pF	2.11ns	1.69ns/pF	1.14ns
D ↑	1.72ns	1.00ns	CK ↑	Q ↑	6.73ns/pF	2.06ns	1.36ns/pF	1.17ns
PD ↓	1.91ns	1.24ns	CK ↑	QN ↓	2.14ns/pF	1.97ns	0.47ns/pF	1.11ns
PD ↑	1.72ns	1.00ns	CK ↑	QN ↑	3.79ns/pF	1.93ns	0.68ns/pF	1.04ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3KX

Positive edge triggered, negative asynchronous clear, negative asynchronous preset.

Grids 22, **Transistors** 30

Inputs
D,CKA,CKB,PDNA,PDNB,CDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	CK	PDN	CDN	Q	QN	Q	QN
X	X	X	0	X	X	0	1
X	X	0	1	X	X	1	0
0	↑	1	X	X	X	0	1
1	↑	X	1	X	X	1	0

X = Don't care

Capacitances

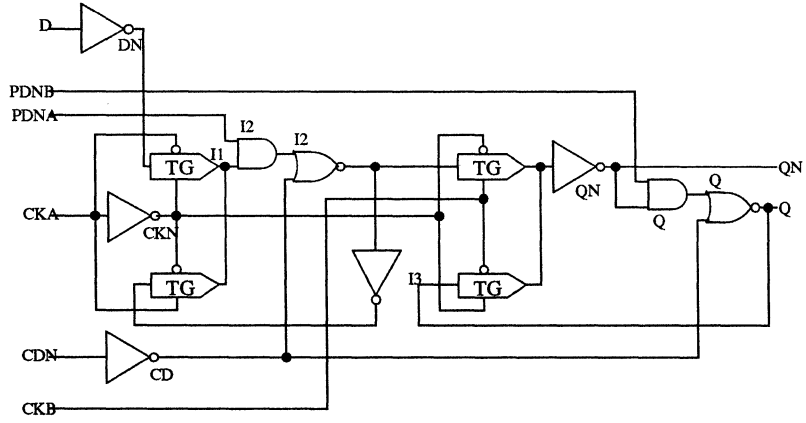
	D	CKA	CKB	PDNA	PDNB	CDN
Area	0.034pF	0.070pF	0.035pF	0.034pF	0.034pF	0.034pF
Perf	0.145pF	0.224pF	0.080pF	0.145pF	0.145pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.57ns	1.05ns	CDN ↓	Q ↓	2.10ns/pF	1.04ns	0.16ns/pF	1.50ns
D ↑	2.10ns	1.24ns	CDN ↓	QN ↑	5.71ns/pF	1.72ns	0.83ns/pF	1.96ns
			CK ↑	Q ↓	10.79ns/pF	2.24ns	2.06ns/pF	1.24ns
			CK ↑	Q ↑	9.50ns/pF	2.45ns	1.88ns/pF	1.28ns
			CK ↑	QN ↓	2.18ns/pF	1.90ns	0.47ns/pF	1.06ns
			CK ↑	QN ↑	3.88ns/pF	1.84ns	0.68ns/pF	0.99ns
			PDN ↓	Q ↑	6.55ns/pF	0.90ns	1.25ns/pF	0.35ns
			PDN ↓	QN ↓	11.95ns/pF	2.37ns	2.19ns/pF	1.23ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3LX

Positive edge triggered, negative synchronous preset.

Grids 18, **Transistors** 24

Inputs
D,CKA,CKB,PDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PDN	Q	QN	Q	QN
X	↑	0	X	X	1	0
0	↑	1	X	X	0	1
1	↑	X	X	X	1	0

X = Don't care

Capacitances

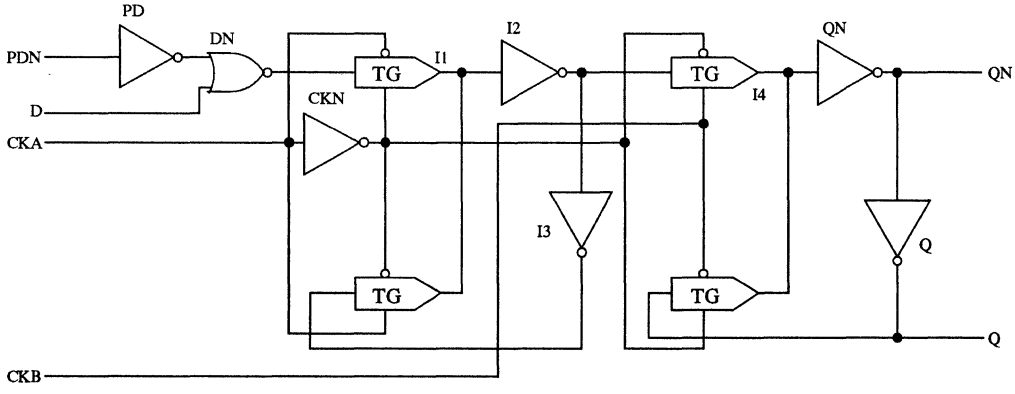
	D	CKA	CKB	PDN
Area	0.034pF	0.070pF	0.036pF	0.034pF
Perf	0.145pF	0.223pF	0.081pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	2.05ns	1.24ns	CK ↑	Q ↓	8.92ns/pF	2.15ns	1.67ns/pF	1.16ns
D ↑	1.76ns	1.00ns	CK ↑	Q ↑	6.55ns/pF	2.09ns	1.33ns/pF	1.19ns
PDN ↓	1.76ns	1.14ns	CK ↑	QN ↓	1.96ns/pF	2.01ns	0.44ns/pF	1.13ns
PDN ↑	2.62ns	1.53ns	CK ↑	QN ↑	3.61ns/pF	1.96ns	0.65ns/pF	1.06ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3MX

Positive edge triggered, negative synchronous clear.

Grids 15, **Transistors** 22

Inputs
D,CKA,CKB,CDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CDN	Q	QN	Q	QN
X	↑	0	X	X	0	1
0	↑	X	X	X	0	1
1	↑	1	X	X	1	0

X = Don't care

Capacitances

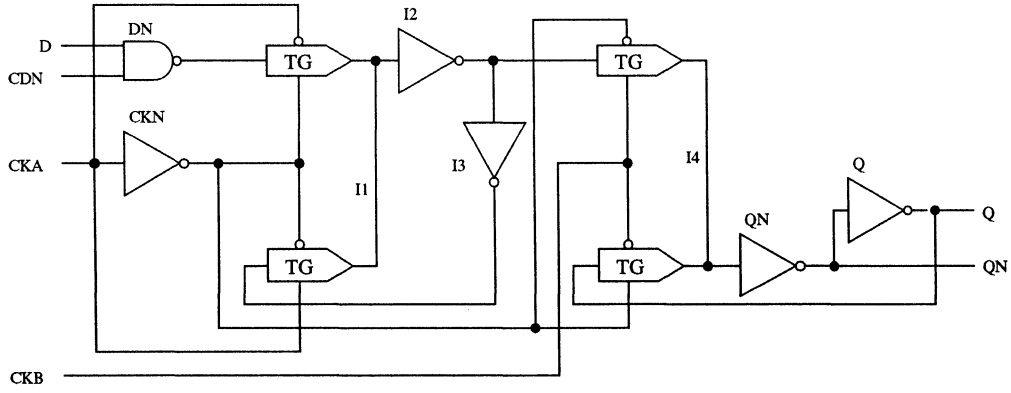
	D	CKA	CKB	CDN
Area	0.034pF	0.073pF	0.036pF	0.034pF
Perf	0.145pF	0.226pF	0.081pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	1.43ns	0.95ns	CK ↑	Q ↓	9.01ns/pF	2.01ns	1.64ns/pF	1.18ns
CDN ↑	1.86ns	1.10ns	CK ↑	Q ↑	6.55ns/pF	2.04ns	1.33ns/pF	1.19ns
D ↓	1.43ns	0.95ns	CK ↑	QN ↓	1.96ns/pF	1.96ns	0.44ns/pF	1.13ns
D ↑	1.86ns	1.10ns	CK ↑	QN ↑	3.70ns/pF	1.83ns	0.63ns/pF	1.08ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3NX

Positive edge triggered, positive asynchronous clear, negative asynchronous preset.

Grids 20, **Transistors** 28

Inputs
D,CKA,CKB,PDNA,PDNB,CD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	CK	PDN	CD	Q	QN	Q	QN
X	X	X	1	X	X	0	1
X	X	0	0	X	X	1	0
0	↑	1	X	X	X	0	1
1	↑	X	0	X	X	1	0

X = Don't care

Capacitances

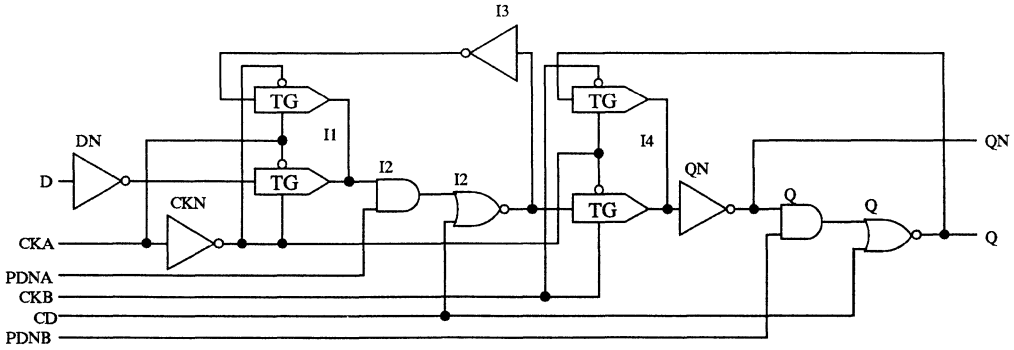
	D	CKA	CKB	PDNA	PDNB	CD
Area	0.034pF	0.075pF	0.035pF	0.034pF	0.034pF	0.070pF
Perf	0.145pF	0.232pF	0.080pF	0.145pF	0.145pF	0.295pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D ↓	1.53ns	1.05ns	CD ↑	Q ↓	2.32ns/pF	1.56ns	0.26ns/pF	1.08ns
D ↑	2.10ns	1.29ns	CD ↑	QN ↑	5.93ns/pF	2.23ns	0.94ns/pF	1.55ns
			CK ↑	Q ↓	10.79ns/pF	2.24ns	2.01ns/pF	1.37ns
			CK ↑	Q ↑	9.58ns/pF	2.36ns	1.85ns/pF	1.40ns
			CK ↑	QN ↓	2.23ns/pF	1.88ns	0.44ns/pF	1.13ns
			CK ↑	QN ↑	3.88ns/pF	1.84ns	0.65ns/pF	1.06ns
			PDN ↓	Q ↑	6.60ns/pF	0.83ns	1.25ns/pF	0.39ns
			PDN ↓	QN ↓	12.04ns/pF	2.29ns	2.19ns/pF	1.32ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3OX

Positive edge triggered, positive synchronous clear, positive synchronous preset.

Grids 19, **Transistors** 26

Inputs
D,CKA,CKB,PD,CD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	CK	PD	CD	Q	QN	Q	QN
X	↑	X	1	X	X	0	1
X	↑	1	0	X	X	1	0
0	↑	0	X	X	X	0	1
1	↑	X	0	X	X	1	0

X = Don't care

Capacitances

	D	CKA	CKB	PD	CD
Area	0.061pF	0.097pF	0.063pF	0.061pF	0.061pF
Perf	0.222pF	0.300pF	0.158pF	0.222pF	0.222pF

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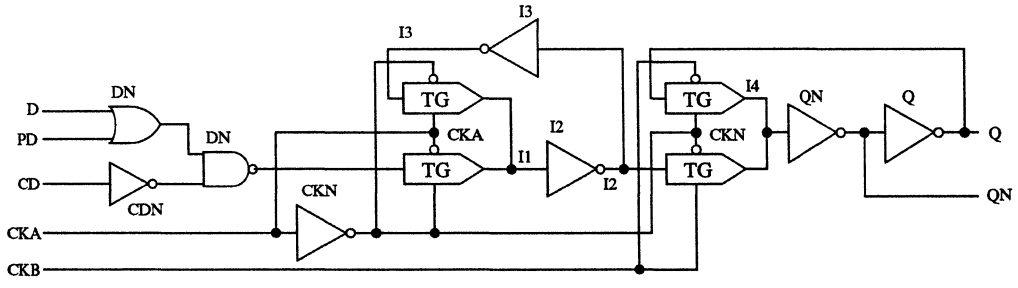
Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
CD ↓	1.91ns	1.24ns	CK ↑	Q ↓	8.92ns/pF	2.15ns	1.67ns/pF	1.16ns
CD ↑	2.53ns	1.48ns	CK ↑	Q ↑	6.55ns/pF	2.09ns	1.33ns/pF	1.19ns
D ↓	2.10ns	1.24ns	CK ↑	QN ↓	1.96ns/pF	2.01ns	0.44ns/pF	1.13ns
D ↑	2.00ns	1.14ns	CK ↑	QN ↑	3.61ns/pF	1.96ns	0.65ns/pF	1.06ns
PD ↓	2.10ns	1.24ns						
PD ↑	2.00ns	1.14ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S5A

Negative level sense.

Grids 9, **Transistors** 10

Inputs
D,CK

Outputs
Q,QN

Truth Table

INPUTS		OUTPUTS			
		OLD		NEW	
D	CK	Q	QN	Q	QN
X	1	0	1	0	1
X	1	1	0	1	0
0	0	X	X	0	1
1	0	X	X	1	0

X = Don't care

Capacitances

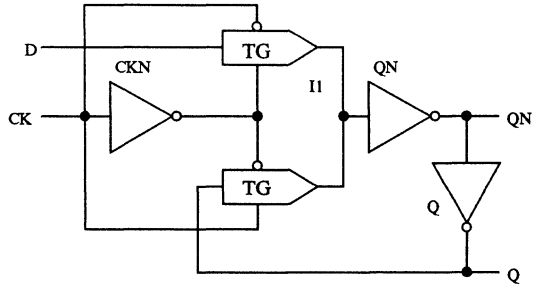
	D	CK
Area	0.026pF	0.070pF
Perf	0.048pF	0.224pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CK ↑	Q ↓	8.92ns/pF	1.19ns	1.67ns/pF	0.78ns
CK ↑	Q ↑	6.55ns/pF	1.14ns	1.38ns/pF	0.77ns
CK ↑	QN ↓	1.96ns/pF	1.01ns	0.50ns/pF	0.66ns
CK ↑	QN ↑	3.61ns/pF	0.96ns	0.68ns/pF	0.61ns
D ↓	Q ↓	8.92ns/pF	0.67ns	1.67ns/pF	0.64ns
D ↓	QN ↑	3.61ns/pF	0.44ns	0.68ns/pF	0.47ns
D ↑	Q ↑	6.55ns/pF	1.76ns	1.38ns/pF	0.96ns
D ↑	QN ↓	1.96ns/pF	1.63ns	0.50ns/pF	0.85ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S5B

Negative level sense, positive asynchronous preset.

Grids 9, **Transistors** 12

Inputs
D,CK,PD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PD	Q	QN	Q	QN
X	1	0	0	1	0	1
X	1	X	1	0	1	0
X	X	1	X	X	1	0
0	0	0	X	X	0	1
1	0	X	X	X	1	0

X = Don't care

Capacitances

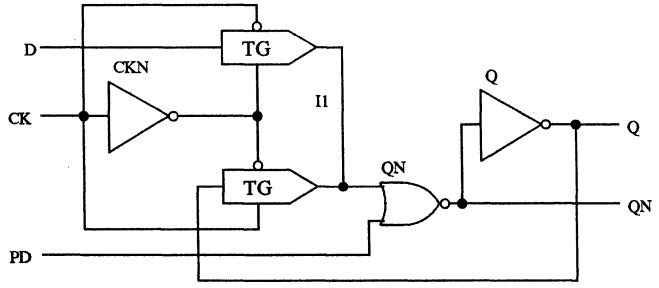
	D	CK	PD
Area	0.026pF	0.070pF	0.034pF
Perf	0.048pF	0.224pF	0.145pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CK ↑	Q ↓	14.49ns/pF	1.16ns	2.66ns/pF	0.86ns
CK ↑	Q ↑	6.64ns/pF	1.00ns	1.33ns/pF	0.76ns
CK ↑	QN ↓	2.18ns/pF	0.86ns	0.47ns/pF	0.68ns
CK ↑	QN ↑	6.87ns/pF	0.90ns	1.25ns/pF	0.63ns
D ↓	Q ↓	14.49ns/pF	0.63ns	2.66ns/pF	0.71ns
D ↓	QN ↑	6.87ns/pF	0.37ns	1.25ns/pF	0.49ns
D ↑	Q ↑	6.64ns/pF	1.62ns	1.33ns/pF	0.95ns
D ↑	QN ↓	2.18ns/pF	1.48ns	0.47ns/pF	0.87ns
PD ↑	Q ↑	6.95ns/pF	1.62ns	1.38ns/pF	0.63ns
PD ↑	QN ↓	2.50ns/pF	1.48ns	0.52ns/pF	0.54ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S5D

Negative level sense, positive asynchronous clear.

Grids 10, **Transistors** 14

Inputs
D,CK,CD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CD	Q	QN	Q	QN
X	1	X	0	1	0	1
X	1	0	1	0	1	0
X	X	1	X	X	0	1
0	0	X	X	X	0	1
1	0	0	X	X	1	0

X = Don't care

Capacitances

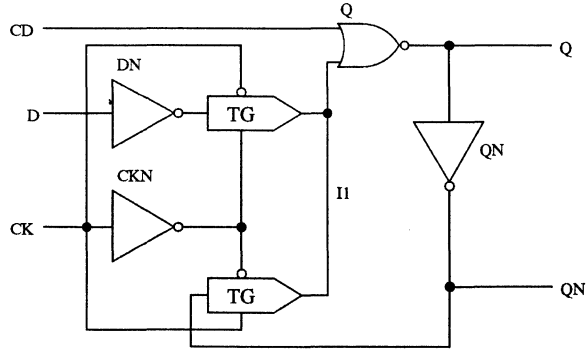
	D	CK	CD
Area	0.034pF	0.075pF	0.034pF
Perf	0.145pF	0.232pF	0.145pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CD ↑	Q ↓	2.50ns/pF	1.48ns	0.52ns/pF	0.54ns
CD ↑	QN ↑	6.95ns/pF	1.62ns	1.38ns/pF	0.63ns
CK ↑	Q ↓	2.18ns/pF	0.86ns	0.47ns/pF	0.68ns
CK ↑	Q ↑	6.87ns/pF	0.90ns	1.25ns/pF	0.63ns
CK ↑	QN ↓	14.49ns/pF	1.16ns	2.66ns/pF	0.86ns
CK ↑	QN ↑	6.64ns/pF	1.00ns	1.33ns/pF	0.76ns
D ↓	Q ↓	2.18ns/pF	1.09ns	0.47ns/pF	0.87ns
D ↓	QN ↑	6.64ns/pF	1.24ns	1.33ns/pF	0.95ns
D ↑	Q ↑	6.87ns/pF	1.37ns	1.25ns/pF	0.92ns
D ↑	QN ↓	14.49ns/pF	1.64ns	2.66ns/pF	1.14ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S5E

Negative level sense, negative asynchronous clear.

Grids 9, **Transistors** 12

Inputs
D,CK,CDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CDN	Q	QN	Q	QN
X	1	X	0	1	0	1
X	1	1	1	0	1	0
X	X	0	X	X	0	1
0	0	X	X	X	0	1
1	0	1	X	X	1	0

X = Don't care

Capacitances

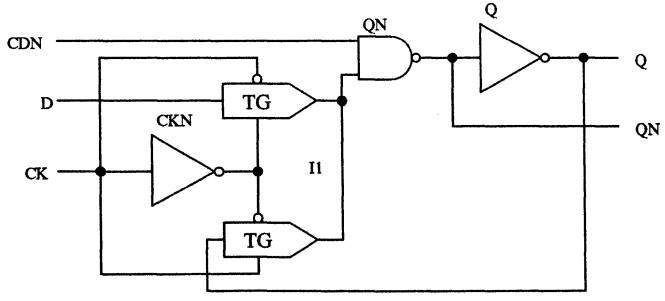
	D	CK	CDN
Area	0.026pF	0.070pF	0.034pF
Perf	0.048pF	0.224pF	0.145pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	Q ↓	8.96ns/pF	0.74ns	1.67ns/pF	0.45ns
CDN ↓	QN ↑	3.74ns/pF	0.57ns	0.68ns/pF	0.32ns
CK ↑	Q ↓	8.87ns/pF	1.12ns	1.67ns/pF	0.73ns
CK ↑	Q ↑	8.87ns/pF	1.31ns	2.01ns/pF	0.70ns
CK ↑	QN ↓	3.61ns/pF	1.20ns	0.96ns/pF	0.57ns
CK ↑	QN ↑	3.66ns/pF	0.94ns	0.68ns/pF	0.61ns
D ↓	Q ↓	8.87ns/pF	0.59ns	1.64ns/pF	0.61ns
D ↓	QN ↑	3.66ns/pF	0.42ns	0.65ns/pF	0.49ns
D ↑	Q ↑	8.87ns/pF	1.93ns	1.98ns/pF	0.92ns
D ↑	QN ↓	3.61ns/pF	1.82ns	0.94ns/pF	0.79ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S5F

Negative level sense, negative asynchronous clear, positive asynchronous preset.

Grids 11, **Transistors** 14

Inputs
D,CK,PD,CDN

Outputs
Q,QN

Capacitances

	D	CK	PD	CDN
Area	0.026pF	0.070pF	0.034pF	0.034pF
Perf	0.048pF	0.224pF	0.145pF	0.145pF

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	CK	PD	CDN	Q	QN	Q	QN
X	1	0	X	0	1	0	1
X	1	X	1	1	0	1	0
X	X	X	0	X	X	0	1
X	X	1	1	X	X	1	0
0	0	0	X	X	X	0	1
1	0	X	1	X	X	1	0

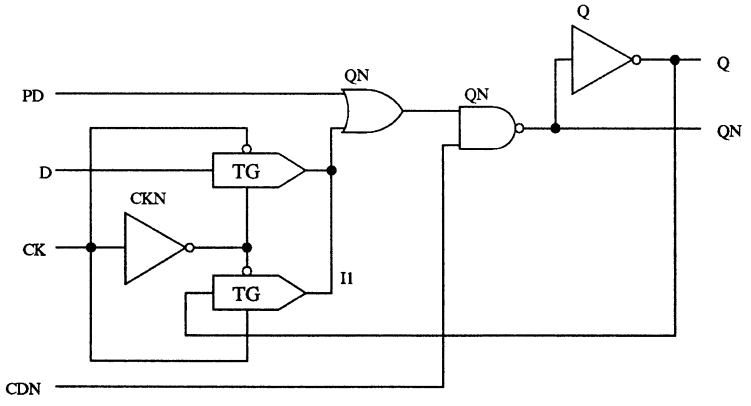
X = Don't care

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	Q ↓	11.28ns/pF	0.77ns	2.14ns/pF	0.36ns
CDN ↓	QN ↑	4.01ns/pF	0.44ns	0.76ns/pF	0.21ns
CK ↑	Q ↓	14.27ns/pF	1.31ns	2.71ns/pF	0.77ns
CK ↑	Q ↑	8.87ns/pF	1.36ns	1.93ns/pF	0.91ns
CK ↑	QN ↓	3.74ns/pF	1.23ns	0.91ns/pF	0.81ns
CK ↑	QN ↑	7.00ns/pF	0.98ns	1.33ns/pF	0.62ns
D ↓	Q ↓	14.27ns/pF	0.83ns	2.68ns/pF	0.65ns
D ↓	QN ↑	7.00ns/pF	0.50ns	1.30ns/pF	0.50ns
D ↑	Q ↑	8.87ns/pF	1.98ns	1.90ns/pF	1.12ns
D ↑	QN ↓	3.74ns/pF	1.85ns	0.89ns/pF	1.02ns
PD ↑	Q ↑	9.27ns/pF	1.70ns	1.93ns/pF	0.72ns
PD ↑	QN ↓	4.15ns/pF	1.57ns	0.91ns/pF	0.61ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



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Static D-Type Flip-Flop

FD1S5G

Negative level sense, negative asynchronous preset.

Grids 10, **Transistors** 14

Inputs
D,CK,PDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PDN	Q	QN	Q	QN
X	1	1	0	1	0	1
X	1	X	1	0	1	0
X	X	0	X	X	1	0
0	0	1	X	X	0	1
1	0	X	X	X	1	0

X = Don't care

Capacitances

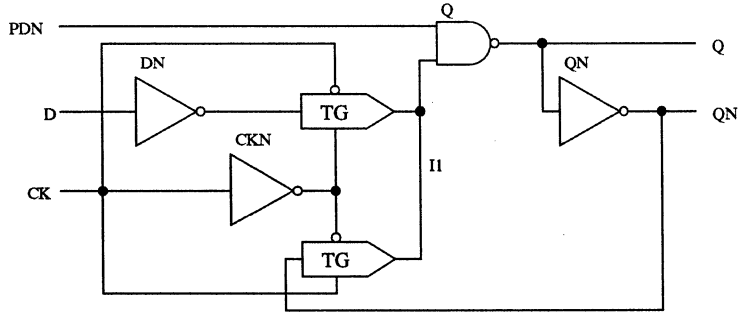
	D	CK	PDN
Area	0.034pF	0.075pF	0.034pF
Perf	0.145pF	0.232pF	0.145pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CK ↑	Q ↓	3.61ns/pF	1.20ns	0.96ns/pF	0.57ns
CK ↑	Q ↑	3.66ns/pF	0.94ns	0.68ns/pF	0.61ns
CK ↑	QN ↓	8.87ns/pF	1.12ns	1.67ns/pF	0.73ns
CK ↑	QN ↑	8.87ns/pF	1.31ns	2.01ns/pF	0.70ns
D ↓	Q ↓	3.61ns/pF	1.44ns	0.94ns/pF	0.79ns
D ↓	QN ↑	8.87ns/pF	1.55ns	1.98ns/pF	0.92ns
D ↑	Q ↑	3.66ns/pF	1.42ns	0.65ns/pF	0.92ns
D ↑	QN ↓	8.87ns/pF	1.60ns	1.64ns/pF	1.04ns
PDN ↓	Q ↑	3.74ns/pF	0.57ns	0.68ns/pF	0.32ns
PDN ↓	QN ↓	8.96ns/pF	0.74ns	1.67ns/pF	0.45ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2N1A

Master-Slave clocking, negative level sample.

Grids 20, **Transistors** 28

Inputs
D,SPN,MCK,SCK

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	SPN	MCK	SCK	Q	QN	Q	QN
X	1	↓	↑	1	0	1	0
X	1	↓	↑	0	1	0	1
0	0	↓	↑	X	X	0	1
1	0	↓	↑	X	X	1	0

X = Don't care

Capacitances

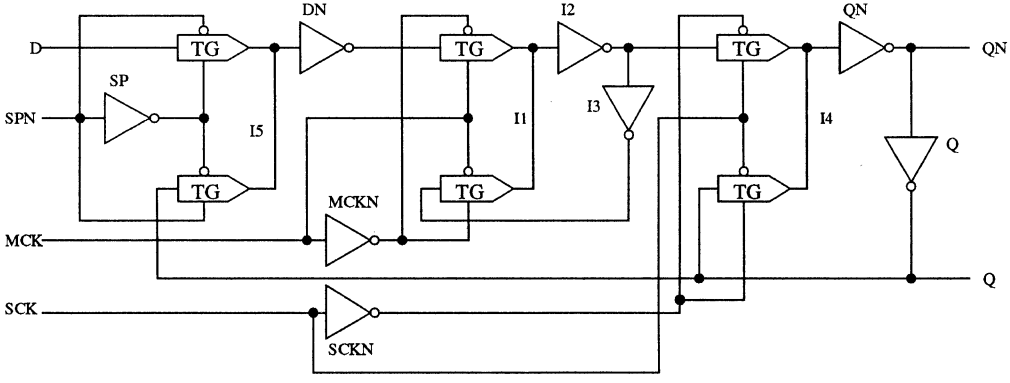
	D	SPN	MCK	SCK
Area	0.026pF	0.070pF	0.072pF	0.070pF
Perf	0.077pF	0.295pF	0.225pF	0.229pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.19ns	1.05ns	SCK ↑	Q ↓	9.01ns/pF	1.68ns	1.67ns/pF	1.02ns
D ↑	2.24ns	1.24ns	SCK ↑	Q ↑	6.46ns/pF	2.04ns	1.33ns/pF	1.14ns
SPN ↓	1.72ns	1.34ns	SCK ↑	QN ↓	1.92ns/pF	1.69ns	0.44ns/pF	0.99ns
SPN ↑	2.48ns	1.57ns	SCK ↑	QN ↑	3.74ns/pF	1.28ns	0.65ns/pF	0.82ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop FD2N1J

Master-Slave clocking, negative level sample, positive synchronous preset.

Grids 23, **Transistors** 34

Inputs
D,SPN,MCK,SCK,PD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D	SPN	MCK	SCK	PD	Q	QN	Q	QN
X	1	↓	↑	0	0	1	0	1
X	1	↓	↑	X	1	0	1	0
X	X	↓	↑	1	X	X	1	0
0	0	↓	↑	0	X	X	0	1
1	0	↓	↑	X	X	X	1	0

X = Don't care

Capacitances

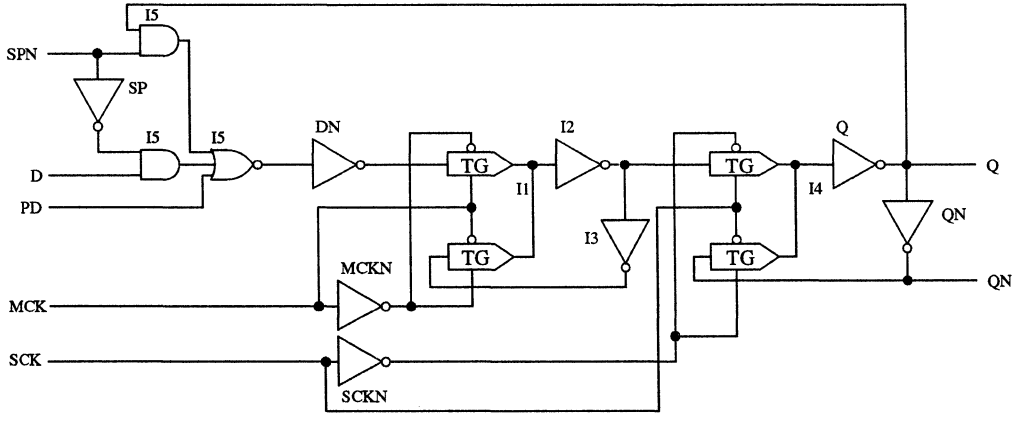
	D	SPN	MCK	SCK	PD
Area	0.038pF	0.071pF	0.070pF	0.071pF	0.034pF
Perf	0.150pF	0.296pF	0.223pF	0.230pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	2.72ns	1.76ns	SCK ↑	Q ↓	1.96ns/pF	1.96ns	0.47ns/pF	1.11ns
D ↑	2.29ns	1.53ns	SCK ↑	Q ↑	3.57ns/pF	1.75ns	0.70ns/pF	0.88ns
PD ↓	2.72ns	1.76ns	SCK ↑	QN ↓	8.83ns/pF	2.14ns	1.72ns/pF	1.07ns
PD ↑	2.19ns	1.53ns	SCK ↑	QN ↑	6.51ns/pF	2.21ns	1.33ns/pF	1.29ns
SPN ↓	2.72ns	1.76ns						
SPN ↑	3.29ns	2.10ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2N1M

Master-Slave clocking, negative level sample, negative synchronous clear.

Grids 23, **Transistors** 34

Inputs
D,SPN,MCK,SCK,CDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D	SPN	MCK	SCK	CDN	Q	QN	Q	QN
X	1	↓	↑	X	0	1	0	1
X	1	↓	↑	1	1	0	1	0
X	X	↓	↑	0	X	X	0	1
0	0	↓	↑	X	X	X	0	1
1	0	↓	↑	1	X	X	1	0

X = Don't care

Capacitances

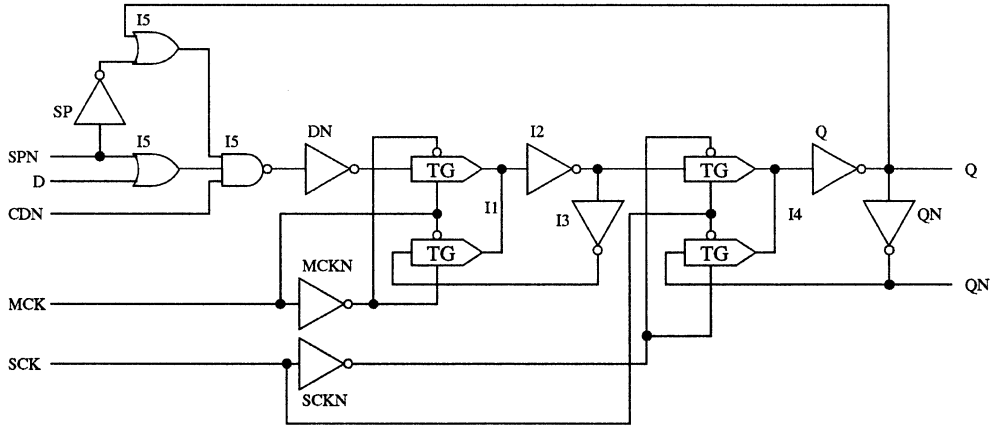
	D	SPN	MCK	SCK	CDN
Area	0.034pF	0.070pF	0.070pF	0.070pF	0.034pF
Perf	0.145pF	0.295pF	0.223pF	0.229pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	1.91ns	1.29ns	SCK ↑	Q ↓	1.96ns/pF	1.96ns	0.47ns/pF	1.11ns
CDN ↑	2.58ns	1.62ns	SCK ↑	Q ↑	3.74ns/pF	1.66ns	0.70ns/pF	0.88ns
D ↓	2.19ns	1.43ns	SCK ↑	QN ↓	9.01ns/pF	2.06ns	1.72ns/pF	1.07ns
D ↑	2.58ns	1.62ns	SCK ↑	QN ↑	6.51ns/pF	2.21ns	1.33ns/pF	1.29ns
SPN ↓	2.38ns	1.72ns						
SPN ↑	2.77ns	1.76ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2P1A

Master-Slave clocking, positive level sample.

Grids 20, **Transistors** 28

Inputs
D,SP,MCK,SCK

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	SP	MCK	SCK	Q	QN	Q	QN
X	0	↓	↑	0	1	0	1
X	0	↓	↑	1	0	1	0
0	1	↓	↑	X	X	0	1
1	1	↓	↑	X	X	1	0

X = Don't care

Capacitances

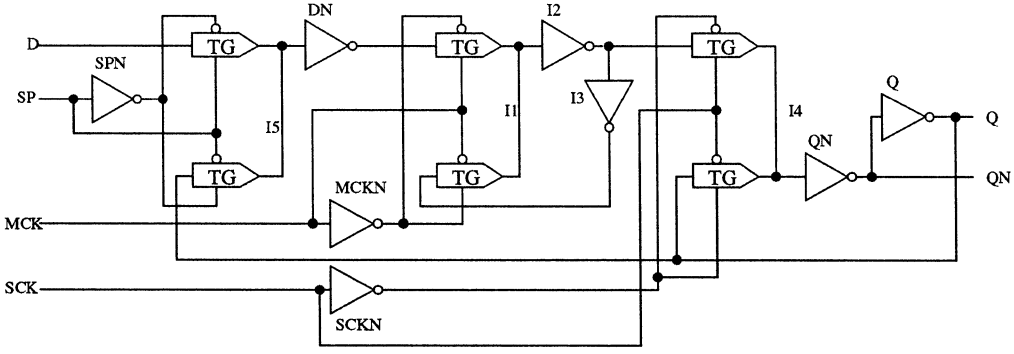
	D	SP	MCK	SCK
Area	0.026pF	0.070pF	0.072pF	0.070pF
Perf	0.077pF	0.295pF	0.225pF	0.229pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.24ns	1.05ns	SCK ↑	Q ↓	9.01ns/pF	1.68ns	1.67ns/pF	1.02ns
D ↑	2.24ns	1.19ns	SCK ↑	Q ↑	6.46ns/pF	2.04ns	1.33ns/pF	1.14ns
SP ↓	1.72ns	1.29ns	SCK ↑	QN ↓	1.92ns/pF	1.69ns	0.44ns/pF	0.99ns
SP ↑	2.58ns	1.57ns	SCK ↑	QN ↑	3.74ns/pF	1.28ns	0.65ns/pF	0.82ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2P1J

Master-Slave clocking, positive level sample, positive synchronous preset.

Grids 23, **Transistors** 34

Inputs
D,SP,MCK,SCK,PD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D	SP	MCK	SCK	PD	Q	QN	Q	QN
X	0	↓	↑	0	0	1	0	1
X	0	↓	↑	X	1	0	1	0
X	X	↓	↑	1	X	X	1	0
0	1	↓	↑	0	X	X	0	1
1	1	↓	↑	X	X	X	1	0

X = Don't care

Capacitances

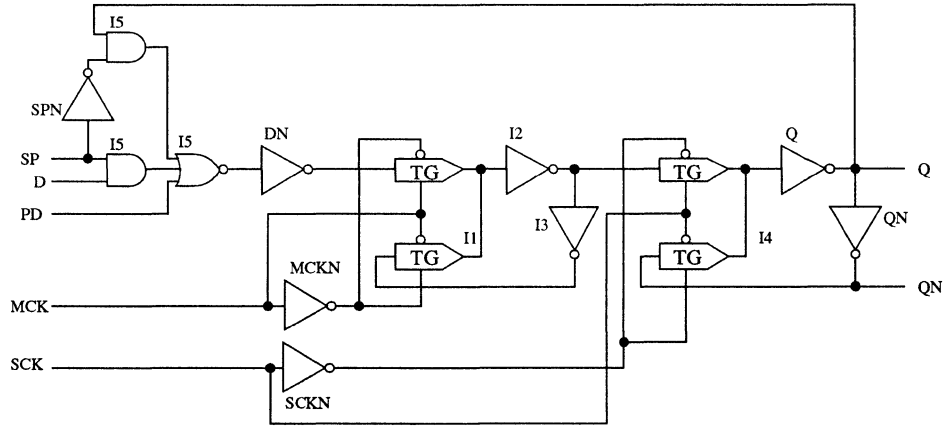
	D	SP	MCK	SCK	PD
Area	0.036pF	0.070pF	0.070pF	0.071pF	0.034pF
Perf	0.148pF	0.295pF	0.223pF	0.230pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	2.72ns	1.76ns	SCK ↑	Q ↓	1.96ns/pF	1.96ns	0.47ns/pF	1.11ns
D ↑	2.29ns	1.53ns	SCK ↑	Q ↑	3.57ns/pF	1.75ns	0.70ns/pF	0.88ns
PD ↓	2.72ns	1.76ns	SCK ↑	QN ↓	8.83ns/pF	2.14ns	1.72ns/pF	1.07ns
PD ↑	2.19ns	1.53ns	SCK ↑	QN ↑	6.51ns/pF	2.21ns	1.33ns/pF	1.29ns
SP ↓	2.72ns	1.76ns						
SP ↑	3.29ns	2.10ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2P1M

Master-Slave clocking, positive level sample, negative synchronous clear.

Grids 23, **Transistors** 34

Inputs
D,SP,MCK,SCK,CDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D	SP	MCK	SCK	CDN	Q	QN	Q	QN
X	0	↓	↑	X	0	1	0	1
X	0	↓	↑	1	1	0	1	0
X	X	↓	↑	0	X	X	0	1
0	1	↓	↑	X	X	X	0	1
1	1	↓	↑	1	X	X	1	0

X = Don't care

Capacitances

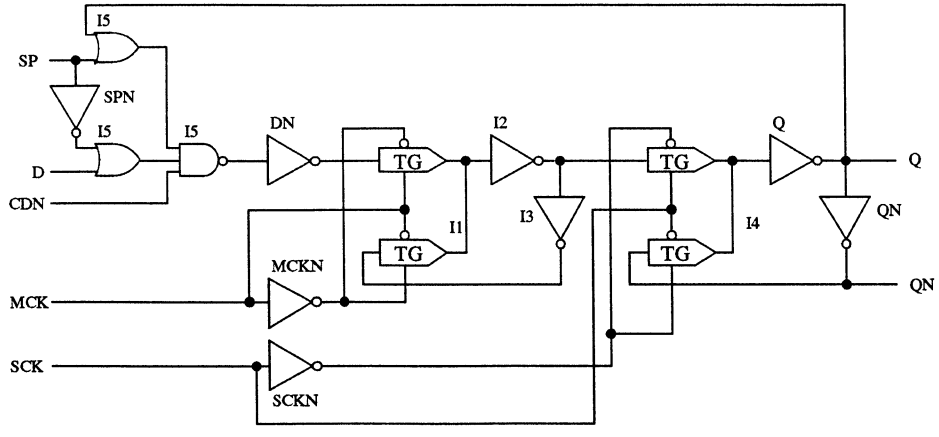
	D	SP	MCK	SCK	CDN
Area	0.034pF	0.070pF	0.070pF	0.070pF	0.034pF
Perf	0.145pF	0.295pF	0.223pF	0.229pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	1.91ns	1.29ns	SCK ↑	Q ↓	1.96ns/pF	1.96ns	0.47ns/pF	1.11ns
CDN ↑	2.58ns	1.62ns	SCK ↑	Q ↑	3.74ns/pF	1.66ns	0.70ns/pF	0.88ns
D ↓	2.19ns	1.43ns	SCK ↑	QN ↓	9.01ns/pF	2.06ns	1.72ns/pF	1.07ns
D ↑	2.58ns	1.62ns	SCK ↑	QN ↑	6.51ns/pF	2.21ns	1.33ns/pF	1.29ns
SP ↓	2.38ns	1.72ns						
SP ↑	2.77ns	1.76ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop FD2S1A

Master-Slave clocking.

Grids 14, **Transistors** 20

Inputs
D,MCK,SCK

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	MCK	SCK	Q	QN	Q	QN
0	↓	↑	X	X	0	1
1	↓	↑	X	X	1	0

X = Don't care

Capacitances

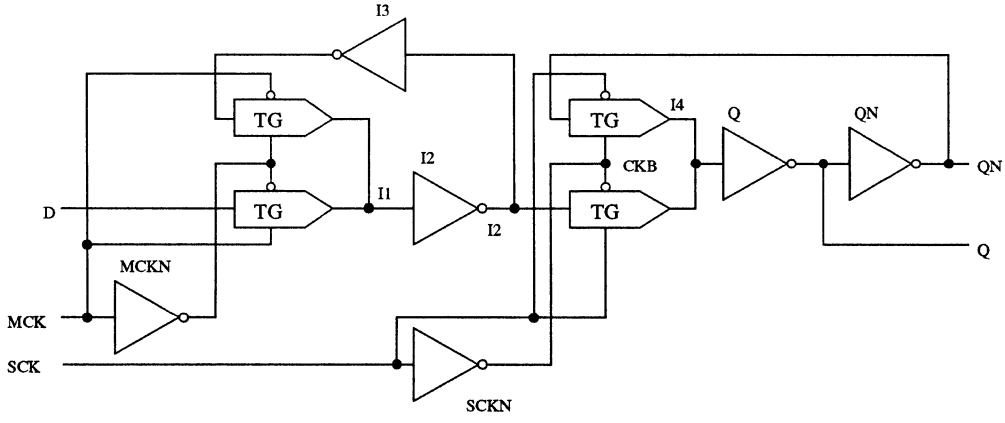
	D	MCK	SCK
Area	0.026pF	0.070pF	0.070pF
Perf	0.048pF	0.223pF	0.228pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	0.62ns	0.57ns	SCK ↑	Q ↓	1.92ns/pF	1.69ns	0.44ns/pF	0.99ns
D ↑	1.62ns	0.86ns	SCK ↑	Q ↑	3.61ns/pF	1.44ns	0.68ns/pF	0.80ns
			SCK ↑	QN ↓	8.87ns/pF	1.74ns	1.69ns/pF	0.95ns
			SCK ↑	QN ↑	6.51ns/pF	1.87ns	1.33ns/pF	1.10ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2S1B

Master-Slave clocking, positive asynchronous preset.

Grids 17, **Transistors** 24

Inputs
D,MCK,SCK,PD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	MCK	SCK	PD	Q	QN	Q	QN
X	X	X	1	X	X	1	0
0	↓	↑	0	X	X	0	1
1	↓	↑	X	X	X	1	0

X = Don't care

Capacitances

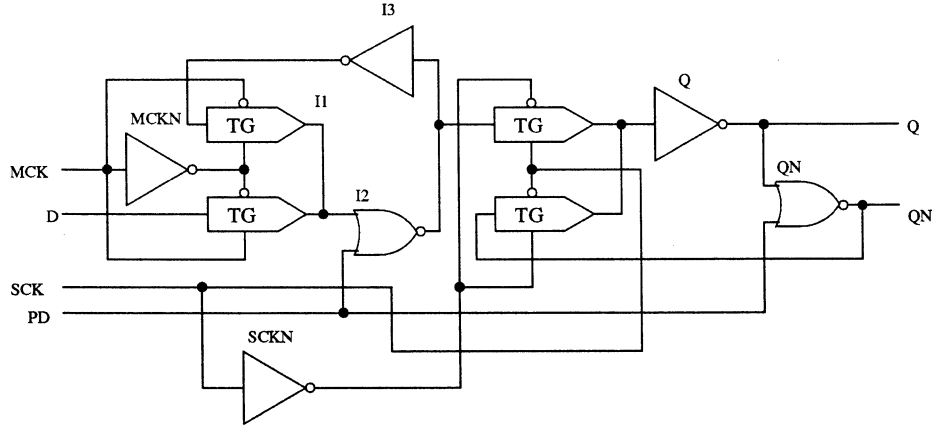
	D	MCK	SCK	PD
Area	0.026pF	0.070pF	0.074pF	0.069pF
Perf	0.048pF	0.223pF	0.228pF	0.294pF

Delay Information

Input Signal	Setup Time		From	To	Propagation Delay			
					Area		Performance	
Name	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.10ns	0.81ns	PD ↑	Q ↑	6.60ns/pF	1.59ns	1.20ns/pF	0.87ns
D ↑	1.72ns	0.95ns	PD ↑	QN ↓	2.90ns/pF	1.20ns	0.57ns/pF	0.41ns
			SCK ↑	Q ↓	1.96ns/pF	1.67ns	0.47ns/pF	0.96ns
			SCK ↑	Q ↑	3.57ns/pF	1.60ns	0.70ns/pF	0.78ns
			SCK ↑	QN ↓	8.92ns/pF	1.86ns	1.75ns/pF	0.91ns
			SCK ↑	QN ↑	9.14ns/pF	2.04ns	1.85ns/pF	1.11ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2S1CX

Master-Slave clocking, positive asynchronous clear, positive asynchronous preset.

Grids 20, **Transistors** 30

Inputs
D,MCK,SCK,PDA,PDB,CD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D	MCK	SCK	PD	CD	Q	QN	Q	QN
X	X	X	X	1	X	X	0	1
X	X	X	1	0	X	X	1	0
0	↓	↑	0	X	X	X	0	1
1	↓	↑	X	0	X	X	1	0

X = Don't care

Capacitances

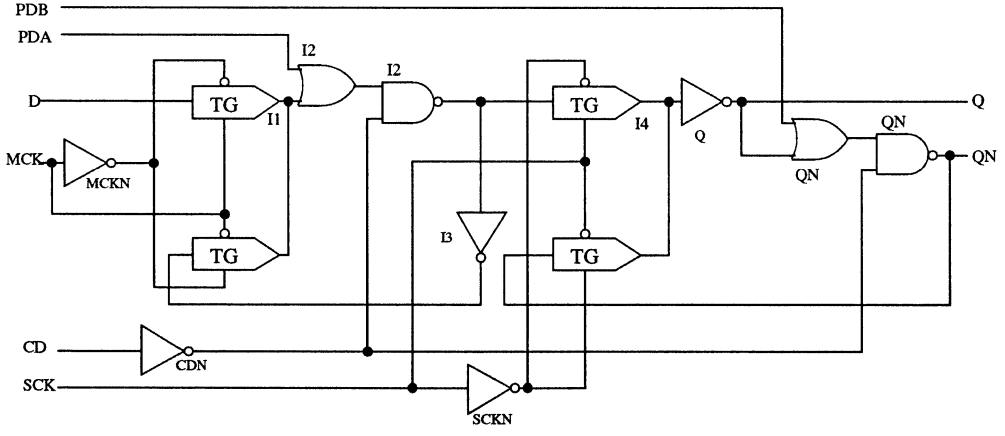
	D	MCK	SCK	PDA	PDB	CD
Area	0.037pF	0.070pF	0.070pF	0.034pF	0.034pF	0.034pF
Perf	0.071pF	0.224pF	0.224pF	0.145pF	0.145pF	0.145pF

Delay Information

Input Signal	Setup Time		From	To	Propagation Delay			
					Area		Performance	
Name	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.19ns	0.76ns	CD ↑	Q ↓	9.05ns/pF	2.47ns	1.64ns/pF	1.42ns
D ↑	1.72ns	0.95ns	CD ↑	QN ↑	3.88ns/pF	1.27ns	0.78ns/pF	0.53ns
			PD ↑	Q ↑	8.07ns/pF	1.87ns	1.49ns/pF	1.12ns
			PD ↑	QN ↓	4.46ns/pF	1.29ns	0.83ns/pF	0.68ns
			SCK ↑	Q ↓	1.92ns/pF	1.65ns	0.44ns/pF	0.99ns
			SCK ↑	Q ↑	3.57ns/pF	1.56ns	0.65ns/pF	0.87ns
			SCK ↑	QN ↓	10.57ns/pF	1.96ns	2.06ns/pF	1.09ns
			SCK ↑	QN ↑	9.18ns/pF	2.17ns	1.82ns/pF	1.23ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2S1D

Master-Slave clocking, positive asynchronous clear.

Grids 18, **Transistors** 26

Inputs
D,MCK,SCK,CD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	MCK	SCK	CD	Q	QN	Q	QN
X	X	X	1	X	X	0	1
0	↓	↑	X	X	X	0	1
1	↓	↑	0	X	X	1	0

X = Don't care

Capacitances

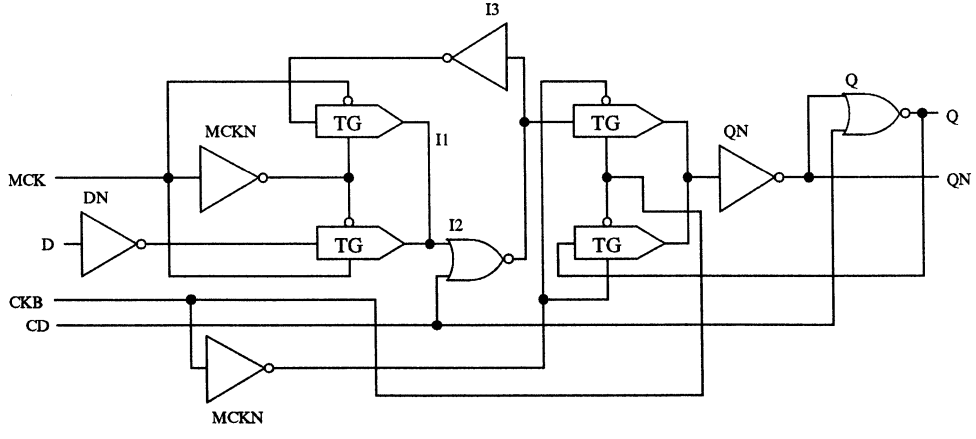
	D	MCK	SCK	CD
Area	0.036pF	0.071pF	0.074pF	0.069pF
Perf	0.148pF	0.224pF	0.228pF	0.294pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D ↓	1.34ns	1.00ns	CD ↑	Q ↓	2.90ns/pF	1.20ns	0.57ns/pF	0.41ns
D ↑	2.05ns	1.19ns	CD ↑	QN ↑	6.60ns/pF	1.59ns	1.20ns/pF	0.87ns
			SCK ↑	Q ↓	8.92ns/pF	1.86ns	1.75ns/pF	0.91ns
			SCK ↑	Q ↑	9.14ns/pF	2.04ns	1.85ns/pF	1.11ns
			SCK ↑	QN ↓	1.96ns/pF	1.67ns	0.47ns/pF	0.96ns
			SCK ↑	QN ↑	3.57ns/pF	1.60ns	0.70ns/pF	0.78ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2S1E

Master-Slave clocking, negative asynchronous clear.

Grids 17, **Transistors** 24

Inputs
D,MCK,SCK,CDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	MCK	SCK	CDN	Q	QN	Q	QN
X	X	X	0	X	X	0	1
0	↓	↑	X	X	X	0	1
1	↓	↑	1	X	X	1	0

X = Don't care

Capacitances

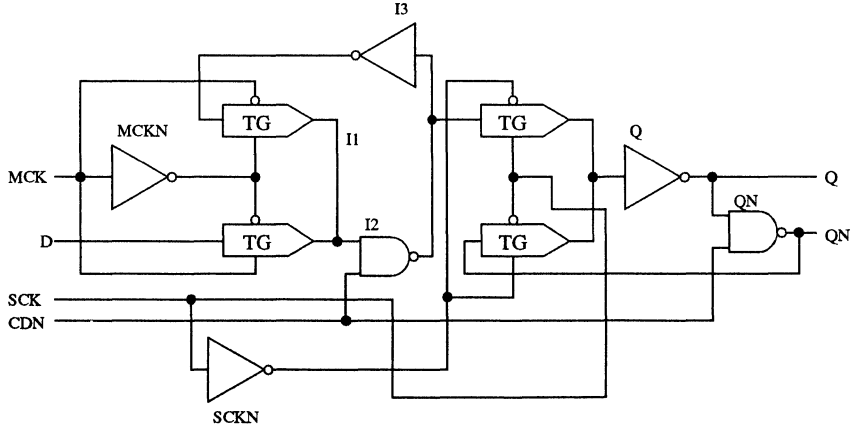
	D	MCK	SCK	CDN
Area	0.026pF	0.070pF	0.074pF	0.069pF
Perf	0.048pF	0.223pF	0.228pF	0.294pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D ↓	0.72ns	0.62ns	CDN ↓	Q ↓	7.09ns/pF	1.46ns	1.43ns/pF	0.78ns
D ↑	1.86ns	1.05ns	CDN ↓	QN ↑	3.66ns/pF	0.66ns	0.78ns/pF	0.10ns
			SCK ↑	Q ↓	1.96ns/pF	1.67ns	0.47ns/pF	0.96ns
			SCK ↑	Q ↑	3.57ns/pF	1.56ns	0.63ns/pF	0.89ns
			SCK ↑	QN ↓	10.34ns/pF	1.83ns	1.98ns/pF	1.06ns
			SCK ↑	QN ↑	6.55ns/pF	1.90ns	1.38ns/pF	1.06ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2S1FX

Master-Slave clocking, negative asynchronous clear, positive asynchronous preset.

Grids 19, **Transistors** 28

Inputs
D,MCK,SCK,PDA,PDB,CDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D	MCK	SCK	PD	CDN	Q	QN	Q	QN
X	X	X	X	0	X	X	0	1
X	X	X	1	1	X	X	1	0
0	↓	↑	0	X	X	X	0	1
1	↓	↑	X	1	X	X	1	0

X = Don't care

Capacitances

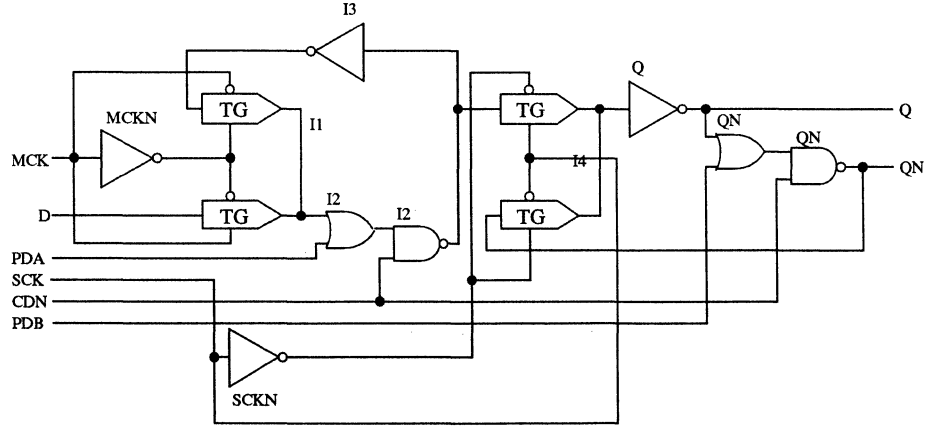
	D	MCK	SCK	PDA	PDB	CDN
Area	0.037pF	0.070pF	0.070pF	0.034pF	0.034pF	0.075pF
Perf	0.071pF	0.224pF	0.224pF	0.145pF	0.145pF	0.300pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.19ns	0.76ns	CDN ↓	Q ↓	8.87ns/pF	1.79ns	1.56ns/pF	1.10ns
D ↑	1.72ns	0.95ns	CDN ↓	QN ↑	3.66ns/pF	0.61ns	0.70ns/pF	0.21ns
			PD ↑	Q ↑	8.11ns/pF	1.85ns	1.49ns/pF	1.12ns
			PD ↑	QN ↓	4.50ns/pF	1.27ns	0.83ns/pF	0.68ns
			SCK ↑	Q ↓	1.92ns/pF	1.65ns	0.44ns/pF	0.99ns
			SCK ↑	Q ↑	3.57ns/pF	1.56ns	0.65ns/pF	0.87ns
			SCK ↑	QN ↓	10.61ns/pF	1.94ns	2.06ns/pF	1.09ns
			SCK ↑	QN ↑	9.23ns/pF	2.15ns	1.82ns/pF	1.23ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2S1G

Master-Slave clocking, negative asynchronous preset.

Grids 18, **Transistors** 26

Inputs
D,MCK,SCK,PDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	MCK	SCK	PDN	Q	QN	Q	QN
X	X	X	0	X	X	1	0
0	↓	↑	1	X	X	0	1
1	↓	↑	X	X	X	1	0

X = Don't care

Capacitances

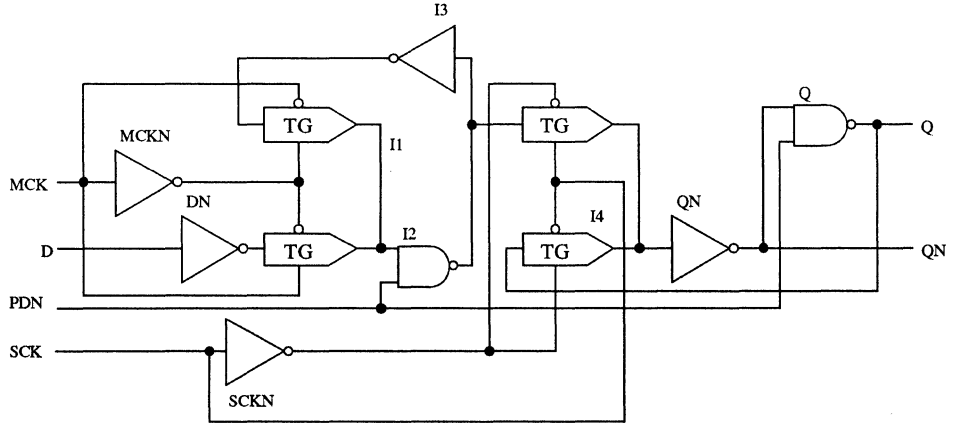
	D	MCK	SCK	PDN
Area	0.036pF	0.071pF	0.074pF	0.069pF
Perf	0.148pF	0.224pF	0.228pF	0.294pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.48ns	1.10ns	PDN ↓	Q ↑	3.66ns/pF	0.66ns	0.78ns/pF	0.10ns
D ↑	1.67ns	1.00ns	PDN ↓	QN ↓	7.09ns/pF	1.46ns	1.43ns/pF	0.78ns
			SCK ↑	Q ↓	10.34ns/pF	1.83ns	1.98ns/pF	1.06ns
			SCK ↑	Q ↑	6.55ns/pF	1.90ns	1.38ns/pF	1.06ns
			SCK ↑	QN ↓	1.96ns/pF	1.67ns	0.47ns/pF	0.96ns
			SCK ↑	QN ↑	3.57ns/pF	1.56ns	0.63ns/pF	0.89ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2S1I

Master-Slave clocking, positive synchronous clear.

Grids 17, **Transistors** 26

Inputs
D,MCK,SCK,CD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	MCK	SCK	CD	Q	QN	Q	QN
X	↓	↑	1	X	X	0	1
0	↓	↑	X	X	X	0	1
1	↓	↑	0	X	X	1	0

X = Don't care

Capacitances

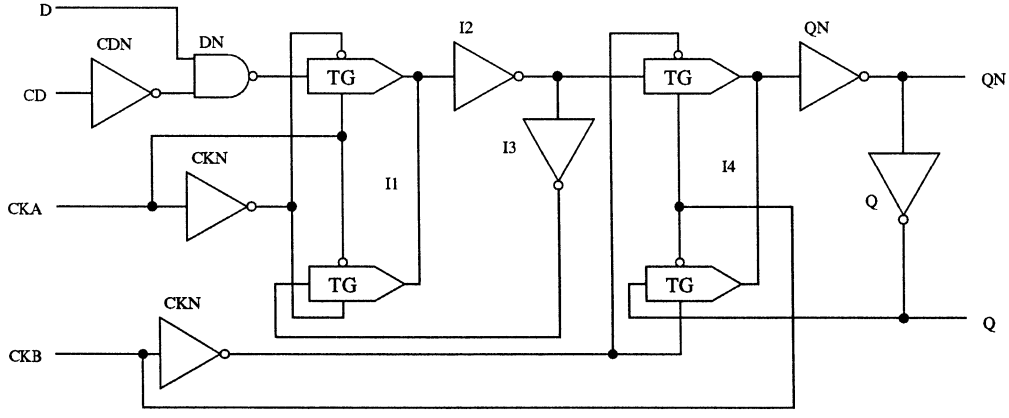
	D	MCK	SCK	CD
Area	0.035pF	0.071pF	0.070pF	0.034pF
Perf	0.147pF	0.224pF	0.228pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CD ↓	1.76ns	1.14ns	SCK ↑	Q ↓	8.87ns/pF	1.74ns	1.69ns/pF	0.95ns
CD ↑	1.91ns	1.19ns	SCK ↑	Q ↑	6.51ns/pF	1.87ns	1.33ns/pF	1.10ns
D ↓	1.29ns	0.86ns	SCK ↑	QN ↓	1.92ns/pF	1.69ns	0.44ns/pF	0.99ns
D ↑	1.72ns	1.05ns	SCK ↑	QN ↑	3.61ns/pF	1.44ns	0.68ns/pF	0.80ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2S1J

Master-Slave clocking, positive synchronous preset.

Grids 16, **Transistors** 24

Inputs
D,MCK,SCK,PD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	MCK	SCK	PD	Q	QN	Q	QN
X	↓	↑	1	X	X	1	0
0	↓	↑	0	X	X	0	1
1	↓	↑	X	X	X	1	0

X = Don't care

Capacitances

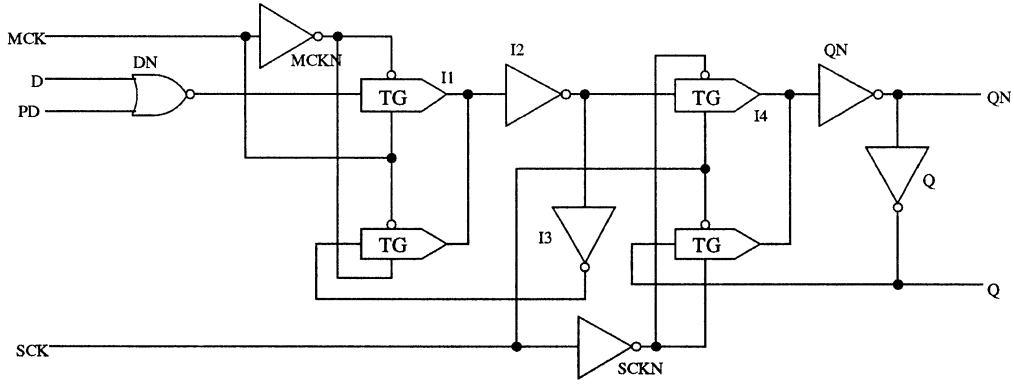
	D	MCK	SCK	PD
Area	0.034pF	0.073pF	0.070pF	0.034pF
Perf	0.145pF	0.226pF	0.228pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.86ns	1.19ns	SCK ↑	Q ↓	8.87ns/pF	1.74ns	1.69ns/pF	0.95ns
D ↑	1.67ns	1.00ns	SCK ↑	Q ↑	6.51ns/pF	1.87ns	1.33ns/pF	1.10ns
PD ↓	1.86ns	1.19ns	SCK ↑	QN ↓	1.92ns/pF	1.69ns	0.44ns/pF	0.99ns
PD ↑	1.67ns	1.00ns	SCK ↑	QN ↑	3.61ns/pF	1.44ns	0.68ns/pF	0.80ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2S1KX

Master-Slave clocking, negative asynchronous clear, negative asynchronous preset.

Grids 21, **Transistors** 32

Inputs
D,MCK,SCK,PDNA,PDNB,CDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D	MCK	SCK	PDN	CDN	Q	QN	Q	QN
X	X	X	X	0	X	X	0	1
X	X	X	0	1	X	X	1	0
0	↓	↑	1	X	X	X	0	1
1	↓	↑	X	1	X	X	1	0

X = Don't care

Capacitances

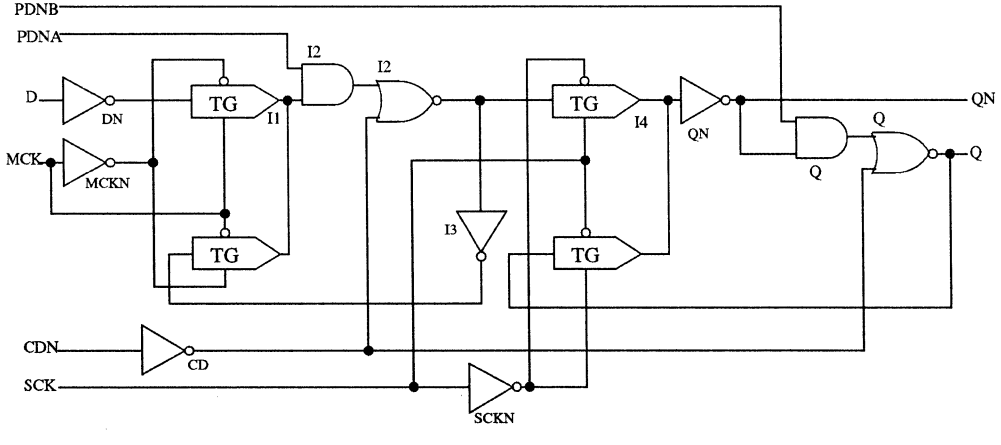
	D	MCK	SCK	PDNA	PDNB	CDN
Area	0.035pF	0.071pF	0.070pF	0.034pF	0.034pF	0.034pF
Perf	0.147pF	0.225pF	0.224pF	0.145pF	0.145pF	0.145pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
D ↓	1.53ns	1.00ns	CDN ↓	Q ↓	2.05ns/pF	1.11ns	0.16ns/pF	1.50ns
D ↑	2.15ns	1.24ns	CDN ↓	QN ↑	5.66ns/pF	1.69ns	0.81ns/pF	1.94ns
			PDN ↓	Q ↑	6.55ns/pF	0.85ns	1.23ns/pF	0.37ns
			PDN ↓	QN ↓	11.95ns/pF	2.09ns	2.14ns/pF	1.27ns
			SCK ↑	Q ↓	10.43ns/pF	2.02ns	2.06ns/pF	1.04ns
			SCK ↑	Q ↑	9.23ns/pF	2.15ns	1.82ns/pF	1.23ns
			SCK ↑	QN ↓	1.92ns/pF	1.65ns	0.44ns/pF	0.99ns
			SCK ↑	QN ↑	3.52ns/pF	1.62ns	0.70ns/pF	0.78ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2S1L

Master-Slave clocking, negative synchronous preset.

Grids 17, **Transistors** 26

Inputs
D,MCK,SCK,PDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	MCK	SCK	PDN	Q	QN	Q	QN
X	↓	↑	0	X	X	1	0
0	↓	↑	1	X	X	0	1
1	↓	↑	X	X	X	1	0

X = Don't care

Capacitances

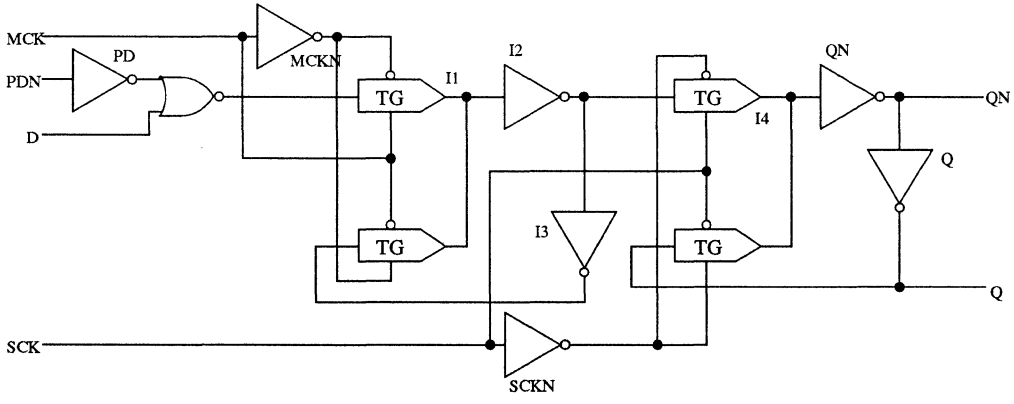
	D	MCK	SCK	PDN
Area	0.035pF	0.071pF	0.070pF	0.034pF
Perf	0.147pF	0.224pF	0.228pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.72ns	1.14ns	SCK ↑	Q ↓	8.87ns/pF	1.74ns	1.69ns/pF	0.95ns
D ↑	1.57ns	0.95ns	SCK ↑	Q ↑	6.51ns/pF	1.87ns	1.33ns/pF	1.10ns
PDN ↓	1.67ns	1.10ns	SCK ↑	QN ↓	1.92ns/pF	1.69ns	0.44ns/pF	0.99ns
PDN ↑	2.29ns	1.43ns	SCK ↑	QN ↑	3.61ns/pF	1.44ns	0.68ns/pF	0.80ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2S1M

Master-Slave clocking, negative synchronous clear.

Grids 16, **Transistors** 24

Inputs
D,MCK,SCK,CDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	MCK	SCK	CDN	Q	QN	Q	QN
X	↓	↑	0	X	X	0	1
0	↓	↑	X	X	X	0	1
1	↓	↑	1	X	X	1	0

X = Don't care

Capacitances

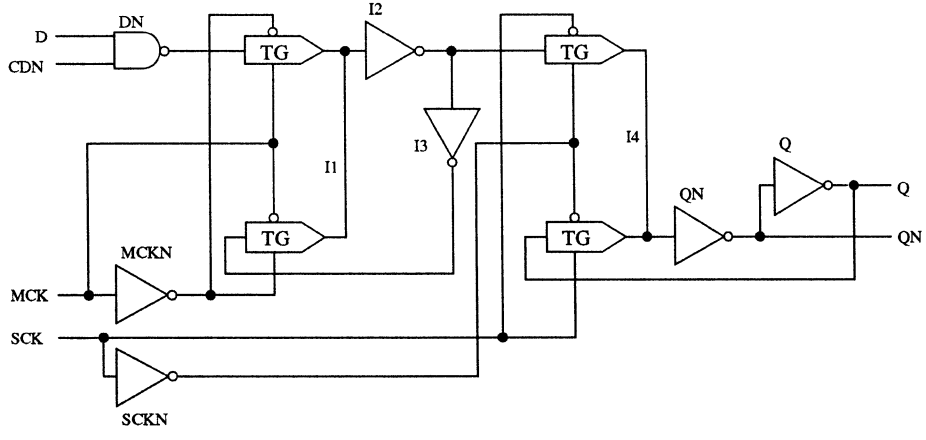
	D	MCK	SCK	CDN
Area	0.034pF	0.073pF	0.070pF	0.034pF
Perf	0.145pF	0.226pF	0.228pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	1.38ns	0.91ns	SCK ↑	Q ↓	8.87ns/pF	1.74ns	1.69ns/pF	0.95ns
CDN ↑	1.86ns	1.10ns	SCK ↑	Q ↑	6.51ns/pF	1.87ns	1.33ns/pF	1.10ns
D ↓	1.38ns	0.91ns	SCK ↑	QN ↓	1.92ns/pF	1.69ns	0.44ns/pF	0.99ns
D ↑	1.86ns	1.10ns	SCK ↑	QN ↑	3.61ns/pF	1.44ns	0.68ns/pF	0.80ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2S1NX

Master-Slave clocking, positive asynchronous clear, negative asynchronous preset.

Grids 20, **Transistors** 30

Inputs
D,MCK,SCK,PDNA,PDNB,CD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS OLD		OUTPUTS NEW	
D	MCK	SCK	PDN	CD	Q	QN	Q	QN
X	X	X	X	1	X	X	0	1
X	X	X	0	0	X	X	1	0
0	↓	↑	1	X	X	X	0	1
1	↓	↑	X	0	X	X	1	0

X = Don't care

Capacitances

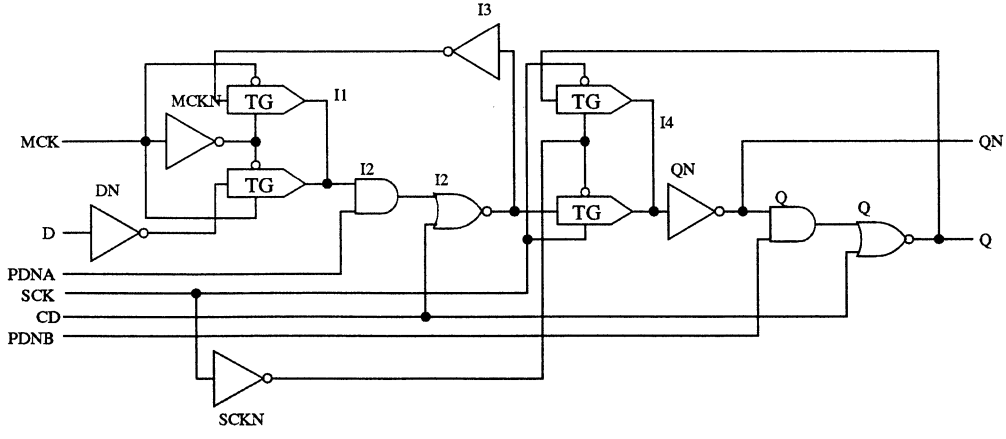
	D	MCK	SCK	PDNA	PDNB	CD
Area	0.035pF	0.071pF	0.070pF	0.034pF	0.034pF	0.075pF
Perf	0.147pF	0.225pF	0.224pF	0.145pF	0.145pF	0.300pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
D ↓	1.53ns	1.00ns	CD ↑	Q ↓	2.32ns/pF	1.56ns	1.15ns/pF	0.33ns
D ↑	2.15ns	1.24ns	CD ↑	QN ↑	5.93ns/pF	2.14ns	1.80ns/pF	0.77ns
			PDN ↓	Q ↑	6.60ns/pF	0.83ns	1.23ns/pF	0.37ns
			PDN ↓	QN ↓	12.04ns/pF	2.00ns	2.14ns/pF	1.27ns
			SCK ↑	Q ↓	10.43ns/pF	2.02ns	2.09ns/pF	1.02ns
			SCK ↑	Q ↑	9.27ns/pF	2.13ns	1.82ns/pF	1.23ns
			SCK ↑	QN ↓	1.92ns/pF	1.65ns	0.44ns/pF	0.99ns
			SCK ↑	QN ↑	3.52ns/pF	1.62ns	0.70ns/pF	0.78ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1N2AX

Negative edge triggered, data select front end, negative level sample.

Grids 26, **Transistors** 36

Inputs
D0,D1,SPN,CKA,CKB,SD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	SPN	CK	SD	Q	QN	Q	QN
0	X	X	↓	0	X	X	0	1
1	X	X	↓	0	X	X	1	0
X	0	0	↓	1	X	X	0	1
X	1	0	↓	1	X	X	1	0
X	X	1	↓	1	0	1	0	1
X	X	1	↓	1	1	0	1	0

X = Don't care

Capacitances

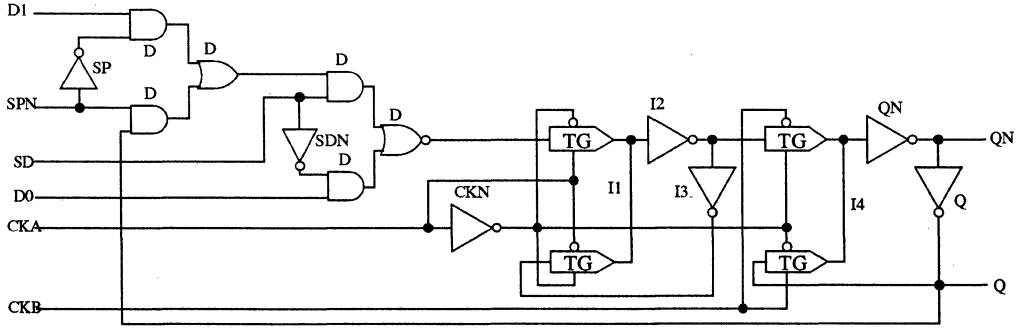
	D0	D1	SPN	CKA	CKB	SD
Area	0.034pF	0.034pF	0.070pF	0.070pF	0.036pF	0.068pF
Perf	0.145pF	0.145pF	0.295pF	0.223pF	0.081pF	0.293pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	3.53ns	1.91ns	CK ↑	Q ↓	8.96ns/pF	1.51ns	1.67ns/pF	1.02ns
D0 ↑	2.77ns	1.48ns	CK ↑	Q ↑	6.51ns/pF	1.59ns	1.36ns/pF	1.03ns
D1 ↓	3.53ns	1.91ns	CK ↑	QN ↓	1.96ns/pF	1.20ns	0.47ns/pF	0.82ns
D1 ↑	2.91ns	1.57ns	CK ↑	QN ↑	3.66ns/pF	1.13ns	0.65ns/pF	0.77ns
SD ↓	3.34ns	1.81ns						
SD ↑	4.20ns	2.24ns						
SPN ↓	3.53ns	1.91ns						
SPN ↑	4.20ns	2.24ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1N2JX

Negative edge triggered, data select front end, negative level sample, positive synchronous preset.

Grids 27, **Transistors** 38

Inputs
D0,D1,SPN,CKA,CKB,SD,PD

Outputs
Q,QN

Capacitances

	D0	D1	SPN	CKA	CKB	SD	PD
Area	0.034pF	0.034pF	0.067pF	0.070pF	0.036pF	0.068pF	0.034pF
Perf	0.145pF	0.145pF	0.292pF	0.223pF	0.081pF	0.293pF	0.145pF

Truth Table

INPUTS						OUTPUTS OLD		OUTPUTS NEW	
D0	D1	SPN	CK	SD	PD	Q	QN	Q	QN
0	X	X	↓	0	X	X	X	0	1
1	X	X	↓	0	X	X	X	1	0
X	X	X	↓	1	1	X	X	1	0
X	0	0	↓	1	0	X	X	0	1
X	1	0	↓	1	X	X	X	1	0
X	X	1	↓	1	0	0	1	0	1
X	X	1	↓	1	X	1	0	1	0

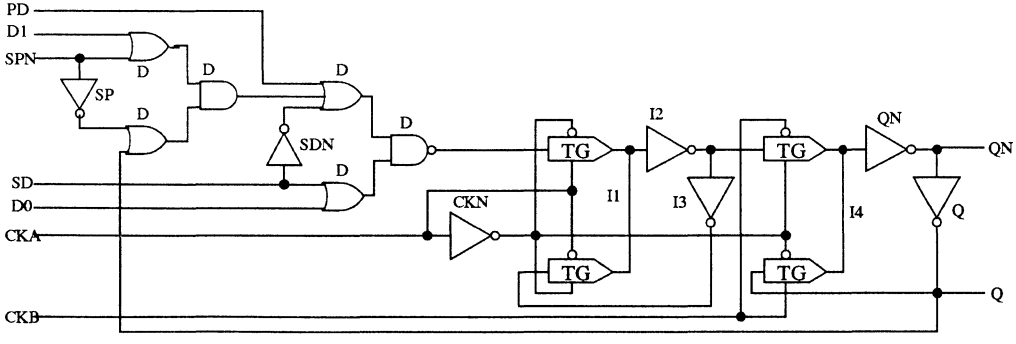
X = Don't care **Note: PD does not function while SD=0**

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	3.96ns	2.10ns	CK ↑	Q ↓	8.96ns/pF	1.51ns	1.67ns/pF	1.02ns
D0 ↑	2.86ns	1.53ns	CK ↑	Q ↑	6.51ns/pF	1.59ns	1.36ns/pF	1.03ns
D1 ↓	4.48ns	2.34ns	CK ↑	QN ↓	1.96ns/pF	1.20ns	0.47ns/pF	0.82ns
D1 ↑	3.01ns	1.57ns	CK ↑	QN ↑	3.66ns/pF	1.13ns	0.65ns/pF	0.77ns
PD ↓	4.48ns	2.29ns						
PD ↑	2.86ns	1.53ns						
SD ↓	3.96ns	2.10ns						
SD ↑	2.86ns	2.67ns						
SPN ↓	4.48ns	2.34ns						
SPN ↑	3.01ns	2.67ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1N2MX

Negative edge triggered, data select front end, negative level sample, negative synchronous clear.

Grids 27, **Transistors** 38

Inputs
D0,D1,SPN,CKA,CKB,SD,CDN

Outputs
Q,QN

Capacitances

Truth Table

INPUTS						OUTPUTS OLD		OUTPUTS NEW	
D0	D1	SPN	CK	SD	CDN	Q	QN	Q	QN
0	X	X	↓	0	X	X	X	0	1
1	X	X	↓	0	X	X	X	1	0
X	X	X	↓	1	0	X	X	0	1
X	0	0	↓	1	X	X	X	0	1
X	1	0	↓	1	1	X	X	1	0
X	X	1	↓	1	X	0	1	0	1
X	X	1	↓	1	1	1	0	1	0

X = Don't care **Note: CDN does not function while SD=0**

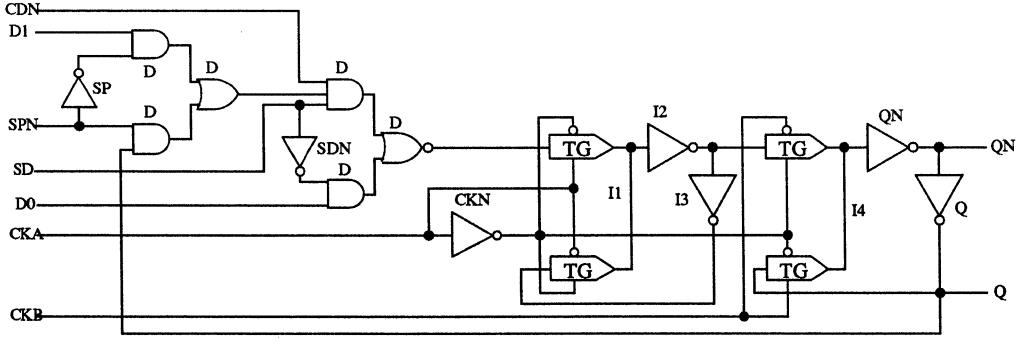
	D0	D1	SPN	CKA	CKB	SD	CDN
Area	0.034pF	0.034pF	0.070pF	0.070pF	0.036pF	0.068pF	0.034pF
Perf	0.145pF	0.145pF	0.295pF	0.223pF	0.081pF	0.293pF	0.145pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
CDN ↓	3.39ns	1.86ns	CK ↑	Q ↓	8.96ns/pF	1.51ns	1.67ns/pF	1.02ns
CDN ↑	3.10ns	1.62ns	CK ↑	Q ↑	6.51ns/pF	1.59ns	1.36ns/pF	1.03ns
D0 ↓	3.29ns	1.86ns	CK ↑	QN ↓	1.96ns/pF	1.20ns	0.47ns/pF	0.82ns
D0 ↑	2.81ns	1.48ns	CK ↑	QN ↑	3.66ns/pF	1.13ns	0.65ns/pF	0.77ns
D1 ↓	3.63ns	2.00ns						
D1 ↑	3.24ns	1.72ns						
SD ↓	3.39ns	1.86ns						
SD ↑	3.91ns	2.15ns						
SPN ↓	3.63ns	2.00ns						
SPN ↑	4.25ns	2.34ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1N3AX

Positive edge triggered, data select front end, negative level sample.

Grids 26, **Transistors** 36

Inputs
D0,D1,SPN,CKA,CKB,SD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	SPN	CK	SD	Q	QN	Q	QN
0	X	X	↑	0	X	X	0	1
1	X	X	↑	0	X	X	1	0
X	0	0	↑	1	X	X	0	1
X	1	0	↑	1	X	X	1	0
X	X	1	↑	1	0	1	0	1
X	X	1	↑	1	1	0	1	0

X = Don't care

Capacitances

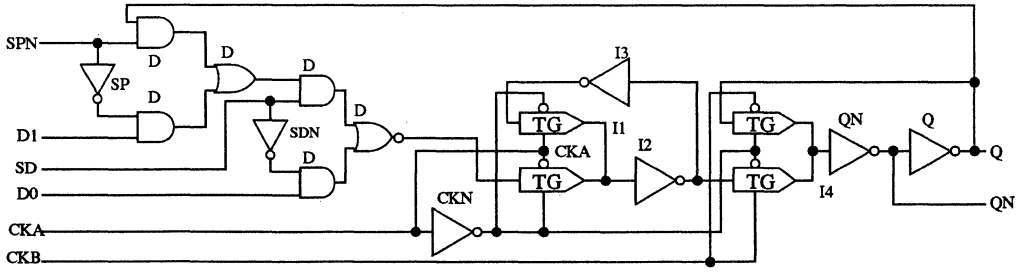
	D0	D1	SPN	CKA	CKB	SD
Area	0.034pF	0.034pF	0.070pF	0.070pF	0.036pF	0.068pF
Perf	0.145pF	0.145pF	0.295pF	0.223pF	0.081pF	0.293pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	3.48ns	1.91ns	CK ↑	Q ↓	9.01ns/pF	2.25ns	1.67ns/pF	1.31ns
D0 ↑	2.77ns	1.48ns	CK ↑	Q ↑	6.55ns/pF	2.33ns	1.36ns/pF	1.31ns
D1 ↓	3.48ns	1.91ns	CK ↑	QN ↓	2.01ns/pF	1.94ns	0.47ns/pF	1.11ns
D1 ↑	2.91ns	1.57ns	CK ↑	QN ↑	3.70ns/pF	1.88ns	0.65ns/pF	1.06ns
SD ↓	3.29ns	1.76ns						
SD ↑	4.15ns	2.19ns						
SPN ↓	3.48ns	1.91ns						
SPN ↑	4.15ns	2.24ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1N3JX

Positive edge triggered, data select front end, negative level sample, positive synchronous preset.

Grids 27, **Transistors** 38

Inputs
D0,D1,SPN,CKA,CKB,SD,PD

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	SPN	CK	SD	PD	Q	QN	Q	QN
0	X	X	↑	0	X	X	X	0	1
1	X	X	↑	0	X	X	X	1	0
X	X	X	↑	1	1	X	X	1	0
X	0	0	↑	1	0	X	X	0	1
X	1	0	↑	1	X	X	X	1	0
X	X	1	↑	1	0	0	1	0	1
X	X	1	↑	1	X	1	0	1	0

X = Don't care Note: PD does not function while SD=0

Capacitances

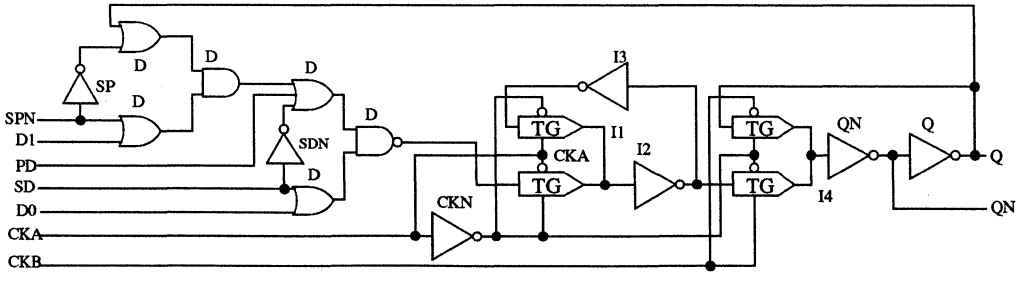
	D0	D1	SPN	CKA	CKB	SD	PD
Area	0.034pF	0.034pF	0.067pF	0.070pF	0.036pF	0.068pF	0.034pF
Perf	0.145pF	0.145pF	0.292pF	0.223pF	0.081pF	0.293pF	0.145pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	3.96ns	2.10ns	CK ↑	Q ↓	9.01ns/pF	2.25ns	1.67ns/pF	1.31ns
D0 ↑	2.86ns	1.53ns	CK ↑	Q ↑	6.55ns/pF	2.33ns	1.36ns/pF	1.31ns
D1 ↓	4.48ns	2.34ns	CK ↑	QN ↓	2.01ns/pF	1.94ns	0.47ns/pF	1.11ns
D1 ↑	3.01ns	1.57ns	CK ↑	QN ↑	3.70ns/pF	1.88ns	0.65ns/pF	1.06ns
PD ↓	4.48ns	2.29ns						
PD ↑	2.86ns	1.53ns						
SD ↓	3.96ns	2.10ns						
SD ↑	2.86ns	2.67ns						
SPN ↓	4.48ns	2.34ns						
SPN ↑	3.01ns	2.67ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1N3MX

Positive edge triggered, data select front end, negative level sample, negative synchronous clear.

Grids 27, **Transistors** 38

Inputs

D0,D1,SPN,CKA,CKB,SD,CDN

Outputs

Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	SPN	CK	SD	CDN	Q	QN	Q	QN
0	X	X	↑	0	X	X	X	0	1
1	X	X	↑	0	X	X	X	1	0
X	X	X	↑	1	0	X	X	0	1
X	0	0	↑	1	X	X	X	0	1
X	1	0	↑	1	1	X	X	1	0
X	X	1	↑	1	X	0	1	0	1
X	X	1	↑	1	1	1	0	1	0

X = Don't care **Note: CDN does not function while SD=0**

Capacitances

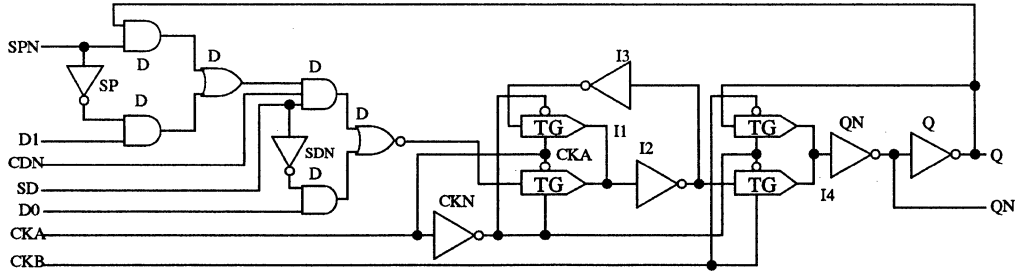
	D0	D1	SPN	CKA	CKB	SD	CDN
Area	0.034pF	0.034pF	0.070pF	0.070pF	0.036pF	0.068pF	0.034pF
Perf	0.145pF	0.145pF	0.295pF	0.223pF	0.081pF	0.293pF	0.145pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
CDN ↓	3.39ns	1.81ns	CK ↑	Q ↓	9.01ns/pF	2.25ns	1.67ns/pF	1.31ns
CDN ↑	3.10ns	1.62ns	CK ↑	Q ↑	6.55ns/pF	2.33ns	1.36ns/pF	1.31ns
D0 ↓	3.29ns	1.81ns	CK ↑	QN ↓	2.01ns/pF	1.94ns	0.47ns/pF	1.11ns
D0 ↑	2.81ns	1.48ns	CK ↑	QN ↑	3.70ns/pF	1.88ns	0.65ns/pF	1.06ns
D1 ↓	3.63ns	2.00ns						
D1 ↑	3.24ns	1.72ns						
SD ↓	3.39ns	1.81ns						
SD ↑	3.91ns	2.15ns						
SPN ↓	3.63ns	2.00ns						
SPN ↑	4.25ns	2.34ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1P2AX

Negative edge triggered, data select front end, positive level sample.

Grids 26, **Transistors** 36

Inputs
D0,D1,SP,CKA,CKB,SD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	SP	CK	SD	Q	QN	Q	QN
0	X	X	↓	0	X	X	0	1
1	X	X	↓	0	X	X	1	0
X	0	1	↓	1	X	X	0	1
X	1	1	↓	1	X	X	1	0
X	X	0	↓	1	0	1	0	1
X	X	0	↓	1	1	0	1	0

X = Don't care

Capacitances

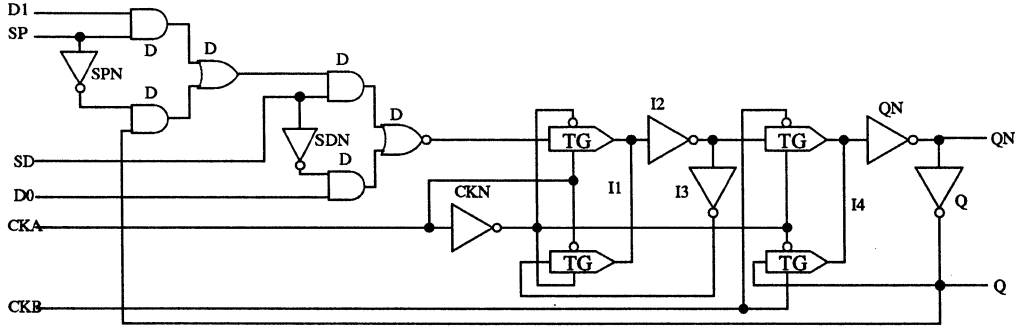
	D0	D1	SP	CKA	CKB	SD
Area	0.034pF	0.034pF	0.068pF	0.070pF	0.036pF	0.068pF
Perf	0.145pF	0.145pF	0.292pF	0.223pF	0.081pF	0.293pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	3.53ns	1.91ns	CK ↑	Q ↓	8.96ns/pF	1.51ns	1.67ns/pF	1.02ns
D0 ↑	2.77ns	1.48ns	CK ↑	Q ↑	6.51ns/pF	1.59ns	1.36ns/pF	1.03ns
D1 ↓	3.53ns	1.91ns	CK ↑	QN ↓	1.96ns/pF	1.20ns	0.47ns/pF	0.82ns
D1 ↑	2.91ns	1.57ns	CK ↑	QN ↑	3.66ns/pF	1.13ns	0.65ns/pF	0.77ns
SD ↓	3.34ns	1.81ns						
SD ↑	4.20ns	2.24ns						
SP ↓	3.53ns	1.91ns						
SP ↑	4.20ns	2.24ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1P2JX

Negative edge triggered, data select front end, positive level sample, positive synchronous preset.

Grids 27, **Transistors** 38

Inputs
D0,D1,SP,CKA,CKB,SD,PD

Outputs
Q,QN

Capacitances

	D0	D1	SP	CKA	CKB	SD	PD
Area	0.034pF	0.034pF	0.070pF	0.070pF	0.036pF	0.068pF	0.034pF
Perf	0.145pF	0.145pF	0.295pF	0.223pF	0.081pF	0.293pF	0.145pF

Truth Table

INPUTS						OUTPUTS OLD		OUTPUTS NEW	
D0	D1	SP	CK	SD	PD	Q	QN	Q	QN
0	X	X	↓	0	X	X	X	0	1
1	X	X	↓	0	X	X	X	1	0
X	X	X	↓	1	1	X	X	1	0
X	0	1	↓	1	0	X	X	0	1
X	1	1	↓	1	X	X	X	1	0
X	X	0	↓	1	0	0	1	0	1
X	X	0	↓	1	X	1	0	1	0

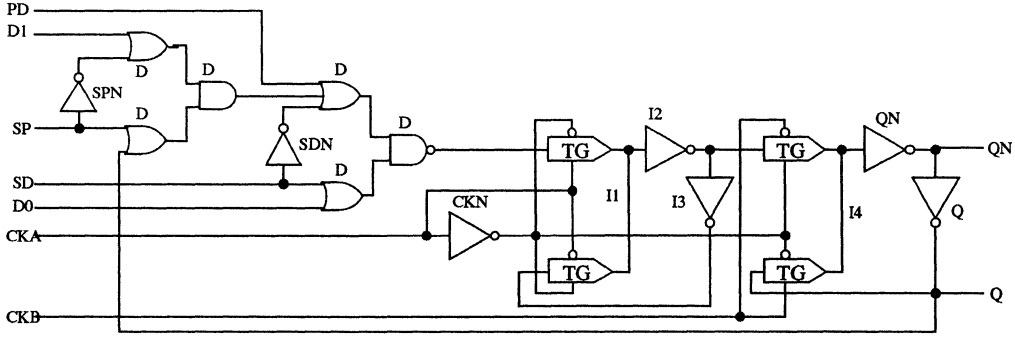
X = Don't care **Note: PD does not function while SD=0**

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	3.96ns	2.10ns	CK ↑	Q ↓	8.96ns/pF	1.51ns	1.67ns/pF	1.02ns
D0 ↑	2.86ns	1.53ns	CK ↑	Q ↑	6.51ns/pF	1.59ns	1.36ns/pF	1.03ns
D1 ↓	4.48ns	2.34ns	CK ↑	QN ↓	1.96ns/pF	1.20ns	0.47ns/pF	0.82ns
D1 ↑	3.01ns	1.57ns	CK ↑	QN ↑	3.66ns/pF	1.13ns	0.65ns/pF	0.77ns
PD ↓	4.48ns	2.29ns						
PD ↑	2.86ns	1.53ns						
SD ↓	3.96ns	2.10ns						
SD ↑	2.86ns	2.67ns						
SP ↓	4.48ns	2.34ns						
SP ↑	3.01ns	2.67ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1P2MX

Negative edge triggered, data select front end, positive level sample, negative synchronous clear.

Grids 27, **Transistors** 38

Inputs
D0,D1,SP,CKA,CKB,SD,CDN

Outputs
Q,QN

Capacitances

	D0	D1	SP	CKA	CKB	SD	CDN
Area	0.034pF	0.034pF	0.067pF	0.070pF	0.036pF	0.068pF	0.034pF
Perf	0.145pF	0.145pF	0.292pF	0.223pF	0.081pF	0.293pF	0.145pF

Truth Table

INPUTS						OUTPUTS OLD		OUTPUTS NEW	
D0	D1	SP	CK	SD	CDN	Q	QN	Q	QN
0	X	X	↓	0	X	X	X	0	1
1	X	X	↓	0	X	X	X	1	0
X	X	X	↓	1	0	X	X	0	1
X	0	1	↓	1	X	X	X	0	1
X	1	1	↓	1	1	X	X	1	0
X	X	0	↓	1	X	0	1	0	1
X	X	0	↓	1	1	1	0	1	0

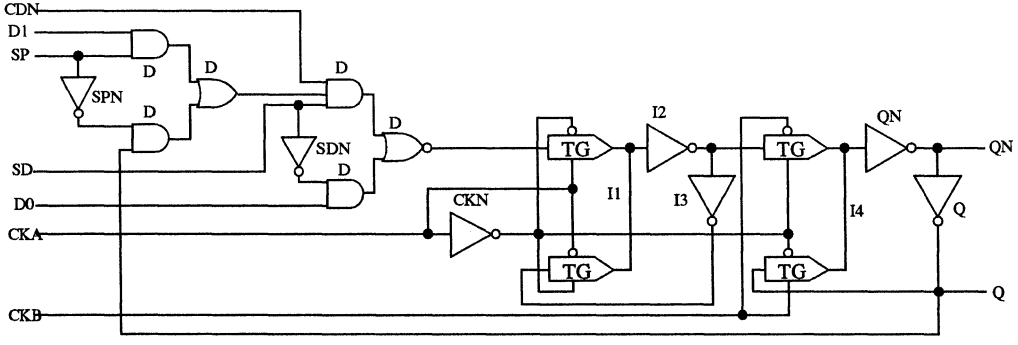
X = Don't care **Note: CDN does not function while SD=0**

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
CDN ↓	3.48ns	1.86ns	CK ↑	Q ↓	8.96ns/pF	1.51ns	1.67ns/pF	1.02ns
CDN ↑	3.15ns	1.62ns	CK ↑	Q ↑	6.51ns/pF	1.59ns	1.36ns/pF	1.03ns
D0 ↓	3.39ns	1.86ns	CK ↑	QN ↓	1.96ns/pF	1.20ns	0.47ns/pF	0.82ns
D0 ↑	2.81ns	1.48ns	CK ↑	QN ↑	3.66ns/pF	1.13ns	0.65ns/pF	0.77ns
D1 ↓	3.72ns	2.00ns						
D1 ↑	3.29ns	1.72ns						
SD ↓	3.48ns	1.86ns						
SD ↑	4.01ns	2.15ns						
SP ↓	3.72ns	2.00ns						
SP ↑	4.34ns	2.34ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1P3AX

Positive edge triggered, data select front end, positive level sample.

Grids 26, **Transistors** 36

Inputs
D0,D1,SP,CKA,CKB,SD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	SP	CK	SD	Q	QN	Q	QN
0	X	X	↑	0	X	X	0	1
1	X	X	↑	0	X	X	1	0
X	0	1	↑	1	X	X	0	1
X	1	1	↑	1	X	X	1	0
X	X	0	↑	1	0	1	0	1
X	X	0	↑	1	1	0	1	0

X = Don't care

Capacitances

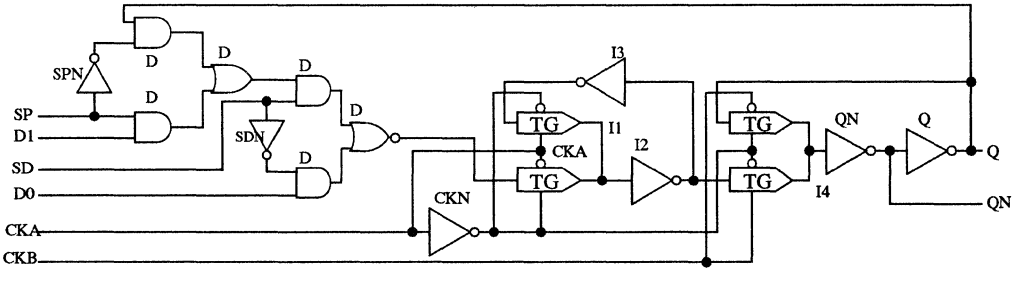
	D0	D1	SP	CKA	CKB	SD
Area	0.034pF	0.034pF	0.068pF	0.070pF	0.036pF	0.068pF
Perf	0.145pF	0.145pF	0.292pF	0.223pF	0.081pF	0.293pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	3.48ns	1.91ns	CK ↑	Q ↓	9.01ns/pF	2.25ns	1.67ns/pF	1.31ns
D0 ↑	2.77ns	1.48ns	CK ↑	Q ↑	6.55ns/pF	2.33ns	1.36ns/pF	1.31ns
D1 ↓	3.48ns	1.91ns	CK ↑	QN ↓	2.01ns/pF	1.94ns	0.47ns/pF	1.11ns
D1 ↑	2.91ns	1.57ns	CK ↑	QN ↑	3.70ns/pF	1.88ns	0.65ns/pF	1.06ns
SD ↓	3.29ns	1.76ns						
SD ↑	4.15ns	2.19ns						
SP ↓	3.48ns	1.91ns						
SP ↑	4.15ns	2.24ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1P3JX

Positive edge triggered, data select front end, positive level sample, positive synchronous preset.

Grids 27, **Transistors** 38

Inputs
D0,D1,SP,CKA,CKB,SD,PD

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	SP	CK	SD	PD	Q	QN	Q	QN
0	X	X	↑	0	X	X	X	0	1
1	X	X	↑	0	X	X	X	1	0
X	X	X	↑	1	1	X	X	1	0
X	0	1	↑	1	0	X	X	0	1
X	1	1	↑	1	X	X	X	1	0
X	X	0	↑	1	0	0	1	0	1
X	X	0	↑	1	X	1	0	1	0

X = Don't care **Note: PD does not function while SD=0**

Capacitances

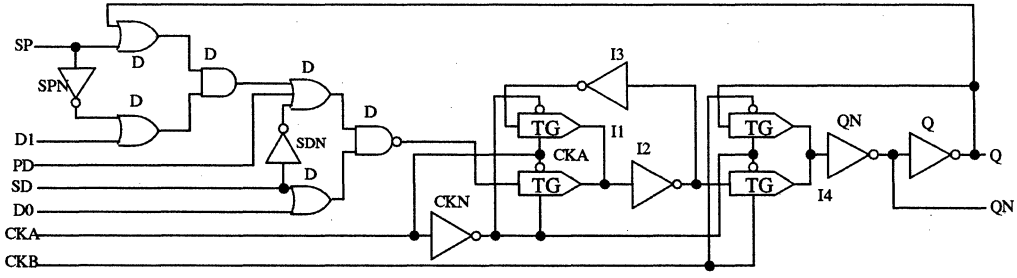
	D0	D1	SP	CKA	CKB	SD	PD
Area	0.034pF	0.034pF	0.070pF	0.070pF	0.036pF	0.068pF	0.034pF
Perf	0.145pF	0.145pF	0.295pF	0.223pF	0.081pF	0.293pF	0.145pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	3.96ns	2.10ns	CK ↑	Q ↓	9.01ns/pF	2.25ns	1.67ns/pF	1.31ns
D0 ↑	2.86ns	1.53ns	CK ↑	Q ↑	6.55ns/pF	2.33ns	1.36ns/pF	1.31ns
D1 ↓	4.48ns	2.34ns	CK ↑	QN ↓	2.01ns/pF	1.94ns	0.47ns/pF	1.11ns
D1 ↑	3.01ns	1.57ns	CK ↑	QN ↑	3.70ns/pF	1.88ns	0.65ns/pF	1.06ns
PD ↓	4.48ns	2.29ns						
PD ↑	2.86ns	1.53ns						
SD ↓	3.96ns	2.10ns						
SD ↑	2.86ns	2.67ns						
SP ↓	4.48ns	2.34ns						
SP ↑	3.01ns	2.67ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1P3MX

Positive edge triggered, data select front end, positive level sample, negative synchronous clear.

Grids 27, **Transistors** 38

Inputs
D0,D1,SP,CKA,CKB,SD,CDN

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	SP	CK	SD	CDN	Q	QN	Q	QN
0	X	X	↑	0	X	X	X	0	1
1	X	X	↑	0	X	X	X	1	0
X	X	X	↑	1	0	X	X	0	1
X	0	1	↑	1	X	X	X	0	1
X	1	1	↑	1	1	X	X	1	0
X	X	0	↑	1	X	0	1	0	1
X	X	0	↑	1	1	1	0	1	0

X = Don't care **Note: CDN does not function while SD=0**

Capacitances

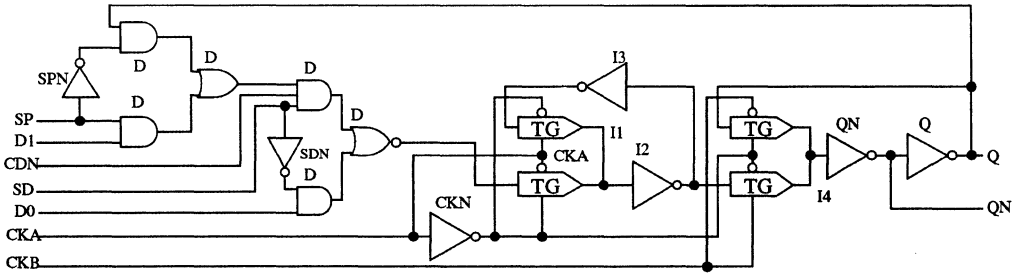
	D0	D1	SP	CKA	CKB	SD	CDN
Area	0.034pF	0.034pF	0.067pF	0.070pF	0.036pF	0.068pF	0.034pF
Perf	0.145pF	0.145pF	0.292pF	0.223pF	0.081pF	0.293pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	3.39ns	1.81ns	CK ↑	Q ↓	9.01ns/pF	2.25ns	1.67ns/pF	1.31ns
CDN ↑	3.10ns	1.62ns	CK ↑	Q ↑	6.55ns/pF	2.33ns	1.36ns/pF	1.31ns
D0 ↓	3.29ns	1.81ns	CK ↑	QN ↓	2.01ns/pF	1.94ns	0.47ns/pF	1.11ns
D0 ↑	2.81ns	1.48ns	CK ↑	QN ↑	3.70ns/pF	1.88ns	0.65ns/pF	1.06ns
D1 ↓	3.63ns	2.00ns						
D1 ↑	3.24ns	1.72ns						
SD ↓	3.39ns	1.81ns						
SD ↑	3.91ns	2.15ns						
SP ↓	3.63ns	2.00ns						
SP ↑	4.25ns	2.34ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2AX

Negative edge triggered, data select front end.

Grids 19, **Transistors** 30

Inputs
D0,D1,CKA,CKB,SD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D0	D1	CK	SD	Q	QN	Q	QN
0	X	↓	0	X	X	0	1
1	X	↓	0	X	X	1	0
X	0	↓	1	X	X	0	1
X	1	↓	1	X	X	1	0

X = Don't care

Capacitances

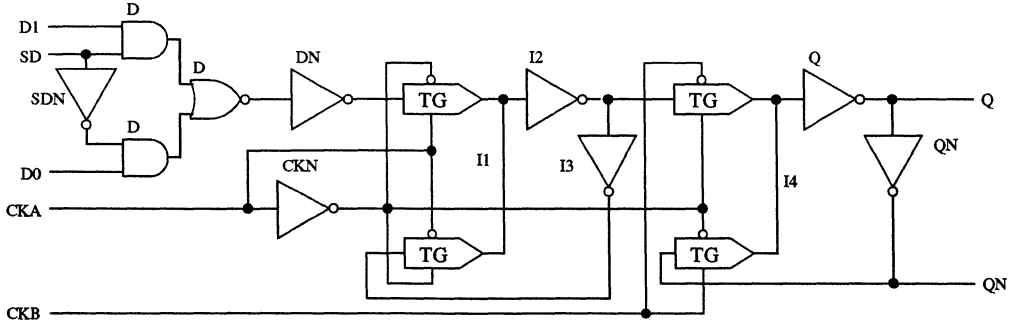
	D0	D1	CKA	CKB	SD
Area	0.034pF	0.037pF	0.070pF	0.036pF	0.066pF
Perf	0.145pF	0.148pF	0.223pF	0.081pF	0.291pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.96ns	1.34ns	CK ↑	Q ↓	1.96ns/pF	1.15ns	0.44ns/pF	0.84ns
D0 ↑	2.19ns	1.38ns	CK ↑	Q ↑	3.70ns/pF	1.02ns	0.65ns/pF	0.77ns
D1 ↓	1.96ns	1.34ns	CK ↑	QN ↓	9.01ns/pF	1.20ns	1.67ns/pF	0.88ns
D1 ↑	2.19ns	1.38ns	CK ↑	QN ↑	6.55ns/pF	1.23ns	1.33ns/pF	0.91ns
SD ↓	2.10ns	1.48ns						
SD ↑	2.62ns	1.62ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2BX

Negative edge triggered, data select front end, positive asynchronous preset.

Grids 22, **Transistors** 34

Inputs
D0,D1,CKA,CKB,SD,PD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS OLD		OUTPUTS NEW	
D0	D1	CK	SD	PD	Q	QN	Q	QN
X	X	X	X	1	X	X	1	0
0	X	↓	0	0	X	X	0	1
1	X	↓	0	X	X	X	1	0
X	0	↓	1	0	X	X	0	1
X	1	↓	1	X	X	X	1	0

X = Don't care

Capacitances

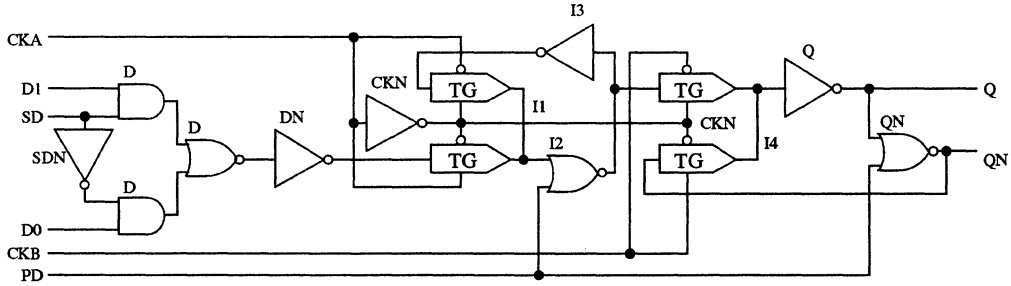
	D0	D1	CKA	CKB	SD	PD
Area	0.034pF	0.037pF	0.070pF	0.036pF	0.066pF	0.073pF
Perf	0.145pF	0.148pF	0.224pF	0.081pF	0.291pF	0.298pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	2.38ns	1.53ns	CK ↑	Q ↓	2.14ns/pF	1.11ns	0.47ns/pF	0.87ns
D0 ↑	2.15ns	1.43ns	CK ↑	Q ↑	3.83ns/pF	1.05ns	0.68ns/pF	0.80ns
D1 ↓	2.38ns	1.53ns	CK ↑	QN ↓	9.18ns/pF	1.31ns	1.72ns/pF	0.93ns
D1 ↑	2.15ns	1.43ns	CK ↑	QN ↑	9.36ns/pF	1.42ns	1.85ns/pF	1.02ns
SD ↓	2.38ns	1.53ns	PD ↑	Q ↑	6.55ns/pF	1.71ns	1.20ns/pF	0.91ns
SD ↑	3.05ns	1.81ns	PD ↑	QN ↓	2.90ns/pF	1.20ns	0.57ns/pF	0.41ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2CX

Negative edge triggered, data select front end, positive asynchronous clear, positive asynchronous preset.

Grids 28, **Transistors** 40

Inputs
D0,D1,CKA,CKB,SD,PDA,PDB,CD

Outputs
Q,QN

Capacitances

	D0	D1	CKA	CKB	SD	PDA	PDB	CD
Area	0.034pF	0.037pF	0.075pF	0.035pF	0.068pF	0.034pF	0.034pF	0.034pF
Perf	0.145pF	0.148pF	0.230pF	0.080pF	0.293pF	0.145pF	0.145pF	0.145pF

Truth Table

INPUTS						OUTPUTS OLD		OUTPUTS NEW	
D0	D1	CK	SD	PD	CD	Q	QN	Q	QN
X	X	X	X	X	1	X	X	0	1
X	X	X	X	1	0	X	X	1	0
0	X	↓	0	0	X	X	X	0	1
1	X	↓	0	X	0	X	X	1	0
X	0	↓	1	0	X	X	X	0	1
X	1	↓	1	X	0	X	X	1	0

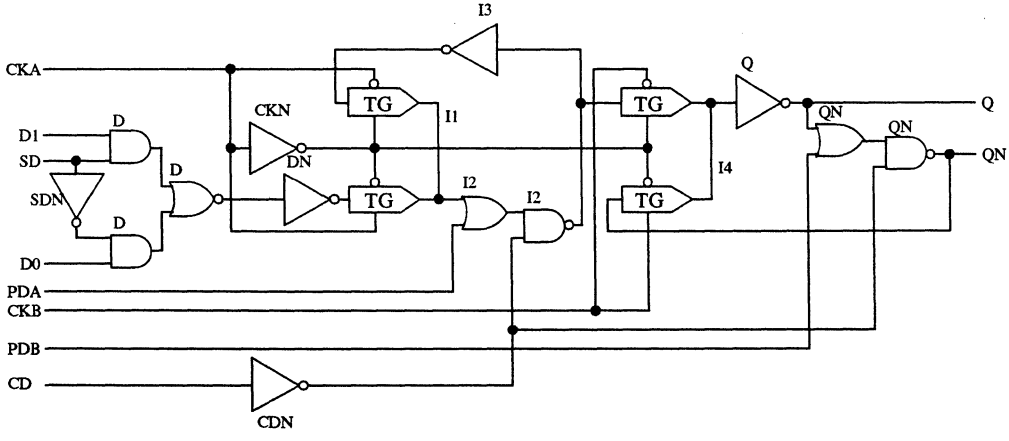
X = Don't care

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	2.43ns	1.62ns	CD ↑	Q ↓	9.09ns/pF	2.69ns	1.67ns/pF	1.45ns
D0 ↑	2.38ns	1.53ns	CD ↑	QN ↑	3.88ns/pF	1.27ns	0.78ns/pF	0.53ns
D1 ↓	2.43ns	1.62ns	CK ↑	Q ↓	1.96ns/pF	1.39ns	0.44ns/pF	0.89ns
D1 ↑	2.38ns	1.53ns	CK ↑	Q ↑	3.66ns/pF	1.32ns	0.65ns/pF	0.82ns
SD ↓	2.43ns	1.62ns	CK ↑	QN ↓	10.70ns/pF	1.71ns	2.06ns/pF	1.04ns
SD ↑	3.05ns	1.91ns	CK ↑	QN ↑	9.27ns/pF	1.89ns	1.82ns/pF	1.13ns
			PD ↑	Q ↑	8.11ns/pF	1.94ns	1.51ns/pF	1.14ns
			PD ↑	QN ↓	4.50ns/pF	1.27ns	0.83ns/pF	0.68ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2DX

Negative edge triggered, data select front end, positive asynchronous clear.

Grids 22, **Transistors** 32

Inputs
D0,D1,CKA,CKB,SD,CD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	CD	Q	QN	Q	QN
X	X	X	X	1	X	X	0	1
0	X	↓	0	X	X	X	0	1
1	X	↓	0	0	X	X	1	0
X	0	↓	1	X	X	X	0	1
X	1	↓	1	0	X	X	1	0

X = Don't care

Capacitances

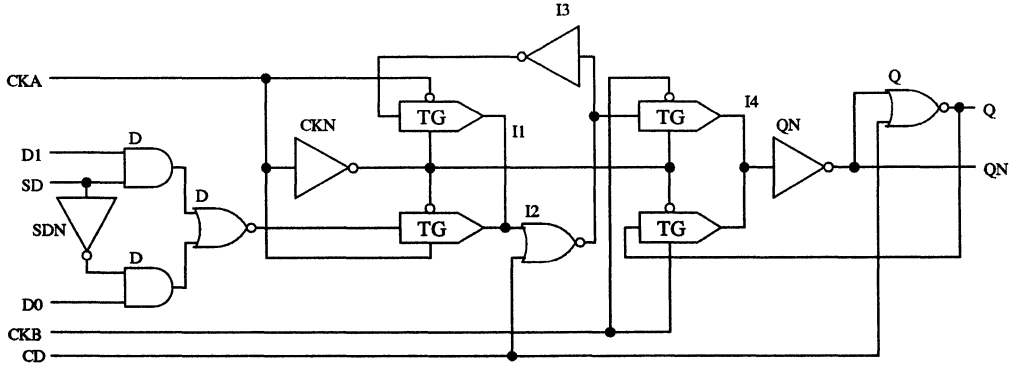
	D0	D1	CKA	CKB	SD	CD
Area	0.034pF	0.036pF	0.070pF	0.036pF	0.068pF	0.073pF
Perf	0.145pF	0.148pF	0.224pF	0.081pF	0.293pF	0.298pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	2.10ns	1.34ns	CD ↑	Q ↓	2.90ns/pF	1.20ns	0.57ns/pF	0.41ns
D0 ↑	2.38ns	1.38ns	CD ↑	QN ↑	6.55ns/pF	1.66ns	1.20ns/pF	0.91ns
D1 ↓	2.10ns	1.34ns	CK ↑	Q ↓	9.23ns/pF	1.19ns	1.72ns/pF	0.93ns
D1 ↑	2.38ns	1.38ns	CK ↑	Q ↑	9.36ns/pF	1.37ns	1.85ns/pF	1.02ns
SD ↓	2.29ns	1.48ns	CK ↑	QN ↓	2.14ns/pF	1.07ns	0.47ns/pF	0.87ns
SD ↑	2.67ns	1.62ns	CK ↑	QN ↑	3.88ns/pF	0.93ns	0.68ns/pF	0.80ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2EX

Negative edge triggered, data select front end, negative asynchronous clear.

Grids 22, **Transistors** 34

Inputs
D0,D1,CKA,CKB,SD,CDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	CDN	Q	QN	Q	QN
X	X	X	X	0	X	X	0	1
0	X	↓	0	X	X	X	0	1
1	X	↓	0	1	X	X	1	0
X	0	↓	1	X	X	X	0	1
X	1	↓	1	1	X	X	1	0

X = Don't care

Capacitances

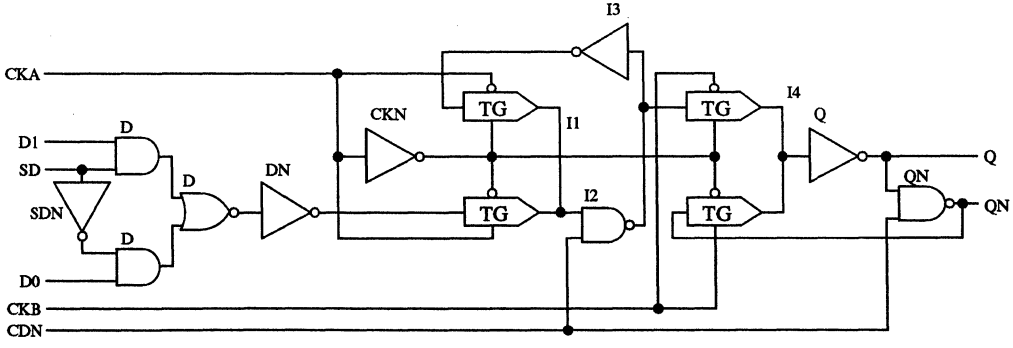
	D0	D1	CKA	CKB	SD	CDN
Area	0.034pF	0.037pF	0.070pF	0.035pF	0.066pF	0.071pF
Perf	0.145pF	0.148pF	0.224pF	0.080pF	0.291pF	0.296pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	2.05ns	1.38ns	CDN ↓	Q ↓	7.04ns/pF	1.58ns	1.43ns/pF	0.78ns
D0 ↑	2.34ns	1.53ns	CDN ↓	QN ↑	3.70ns/pF	0.59ns	0.78ns/pF	0.10ns
D1 ↓	2.05ns	1.38ns	CK ↑	Q ↓	1.87ns/pF	1.29ns	0.47ns/pF	0.82ns
D1 ↑	2.34ns	1.53ns	CK ↑	Q ↑	3.57ns/pF	1.22ns	0.65ns/pF	0.77ns
SD ↓	2.24ns	1.62ns	CK ↑	QN ↓	10.34ns/pF	1.49ns	2.01ns/pF	0.94ns
SD ↑	2.72ns	1.67ns	CK ↑	QN ↑	6.51ns/pF	1.44ns	1.38ns/pF	0.91ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2FX

Negative edge triggered, data select front end, negative asynchronous clear, positive asynchronous preset.

Grids 25, **Transistors** 38

Inputs
D0,D1,CKA,CKB,SD,PDA,PDB,CDN

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	CK	SD	PD	CDN	Q	QN	Q	QN
X	X	X	X	X	0	X	X	0	1
X	X	X	X	1	1	X	X	1	0
0	X	↓	0	0	X	X	X	0	1
1	X	↓	0	X	1	X	X	1	0
X	0	↓	1	0	X	X	X	0	1
X	1	↓	1	X	1	X	X	1	0

X = Don't care

Capacitances

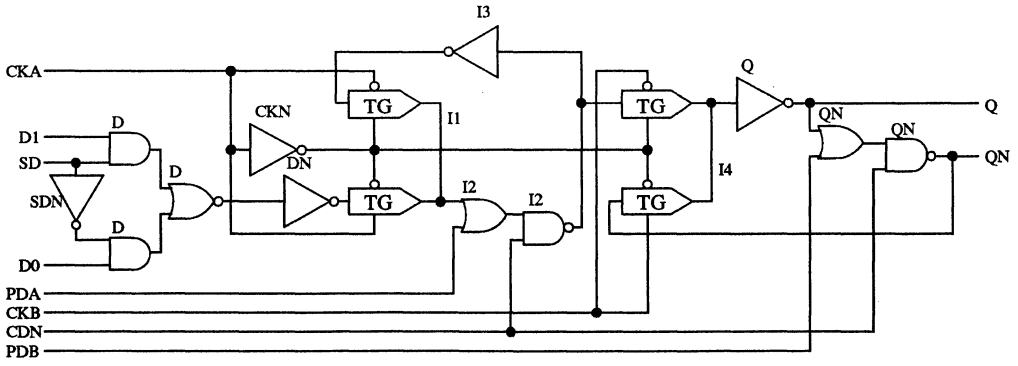
	D0	D1	CKA	CKB	SD	PDA	PDB	CDN
Area	0.034pF	0.037pF	0.070pF	0.035pF	0.069pF	0.034pF	0.034pF	0.071pF
Perf	0.145pF	0.149pF	0.224pF	0.080pF	0.294pF	0.145pF	0.145pF	0.296pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	2.53ns	1.62ns	CDN ↓	Q ↓	8.92ns/pF	2.00ns	1.59ns/pF	1.18ns
D0 ↑	2.43ns	1.53ns	CDN ↓	QN ↑	3.66ns/pF	0.61ns	0.68ns/pF	0.28ns
D1 ↓	2.53ns	1.62ns	CK ↑	Q ↓	2.01ns/pF	1.37ns	0.44ns/pF	0.89ns
D1 ↑	2.43ns	1.53ns	CK ↑	Q ↑	3.66ns/pF	1.32ns	0.65ns/pF	0.82ns
SD ↓	2.53ns	1.62ns	CK ↑	QN ↓	10.65ns/pF	1.73ns	2.03ns/pF	1.11ns
SD ↑	3.10ns	1.91ns	CK ↑	QN ↑	9.32ns/pF	1.87ns	1.82ns/pF	1.18ns
			PD ↑	Q ↑	8.07ns/pF	1.96ns	1.90ns/pF	0.88ns
			PD ↑	QN ↓	4.46ns/pF	1.29ns	1.23ns/pF	0.42ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2GX

Negative edge triggered, data select front end, negative asynchronous preset.

Grids 22, **Transistors** 32

Inputs
D0,D1,CKA,CKB,SD,PDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	PDN	Q	QN	Q	QN
X	X	X	X	0	X	X	1	0
0	X	↓	0	1	X	X	0	1
1	X	↓	0	X	X	X	1	0
X	0	↓	1	1	X	X	0	1
X	1	↓	1	X	X	X	1	0

X = Don't care

Capacitances

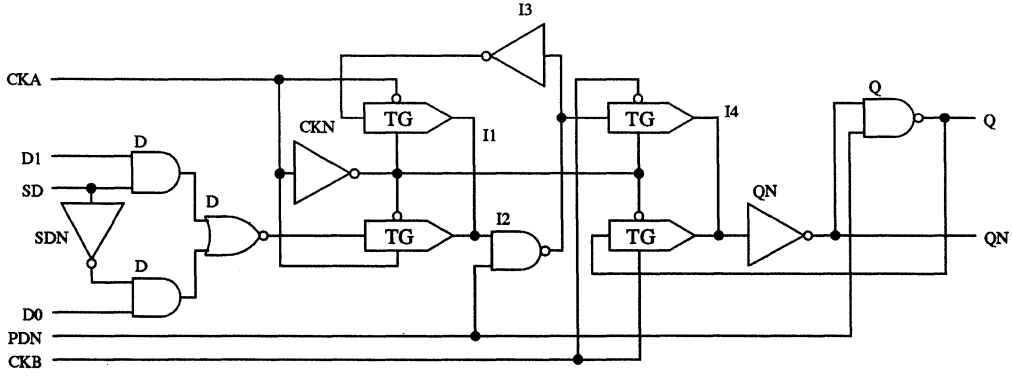
	D0	D1	CKA	CKB	SD	PDN
Area	0.034pF	0.036pF	0.070pF	0.035pF	0.068pF	0.071pF
Perf	0.145pF	0.148pF	0.223pF	0.080pF	0.293pF	0.296pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	2.29ns	1.43ns	CK ↑	Q ↓	10.39ns/pF	1.38ns	2.01ns/pF	0.94ns
D0 ↑	2.05ns	1.24ns	CK ↑	Q ↑	6.51ns/pF	1.39ns	1.38ns/pF	0.91ns
D1 ↓	2.29ns	1.43ns	CK ↑	QN ↓	1.87ns/pF	1.24ns	0.47ns/pF	0.82ns
D1 ↑	2.05ns	1.24ns	CK ↑	QN ↑	3.61ns/pF	1.11ns	0.65ns/pF	0.77ns
SD ↓	2.29ns	1.43ns	PDN ↓	Q ↑	3.70ns/pF	0.59ns	0.78ns/pF	0.10ns
SD ↑	2.86ns	1.72ns	PDN ↓	QN ↓	7.00ns/pF	1.60ns	1.43ns/pF	0.78ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2IX

Negative edge triggered, data select front end, positive synchronous clear.

Grids 23, **Transistors** 32

Inputs
D0,D1,CKA,CKB,SD,CD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	CD	Q	QN	Q	QN
X	X	↓	1	1	X	X	0	1
0	X	↓	0	X	X	X	0	1
1	X	↓	0	X	X	X	1	0
X	0	↓	1	X	X	X	0	1
X	1	↓	1	0	X	X	1	0

X = Don't care **Note: CD does not function while SD=0**

Capacitances

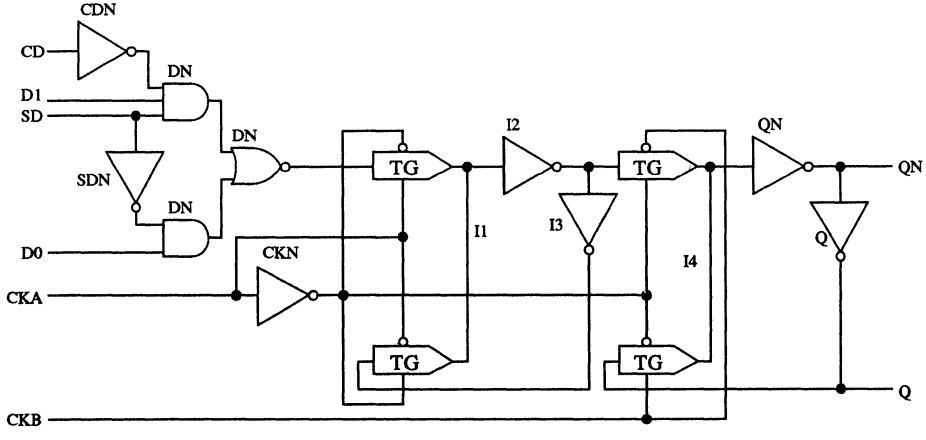
	D0	D1	CKA	CKB	SD	CD
Area	0.034pF	0.034pF	0.070pF	0.036pF	0.071pF	0.034pF
Perf	0.145pF	0.145pF	0.223pF	0.081pF	0.295pF	0.145pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
CD ↓	2.19ns	1.38ns	CK ↑	Q ↓	8.92ns/pF	1.34ns	1.67ns/pF	0.88ns
CD ↑	2.81ns	1.62ns	CK ↑	Q ↑	6.55ns/pF	1.28ns	1.33ns/pF	0.91ns
D0 ↓	2.19ns	1.34ns	CK ↑	QN ↓	1.96ns/pF	1.20ns	0.44ns/pF	0.84ns
D0 ↑	2.19ns	1.19ns	CK ↑	QN ↑	3.61ns/pF	1.15ns	0.65ns/pF	0.77ns
D1 ↓	2.19ns	1.34ns						
D1 ↑	2.29ns	1.29ns						
SD ↓	2.19ns	1.34ns						
SD ↑	2.77ns	1.62ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2JX

Negative edge triggered, data select front end, positive synchronous preset.

Grids 21, **Transistors** 30

Inputs
D0,D1,CKA,CKB,SD,PD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	PD	Q	QN	Q	QN
X	X	↓	1	1	X	X	1	0
0	X	↓	0	X	X	X	0	1
1	X	↓	0	X	X	X	1	0
X	0	↓	1	0	X	X	0	1
X	1	↓	1	X	X	X	1	0

X = Don't care **Note: PD does not function while SD=0**

Capacitances

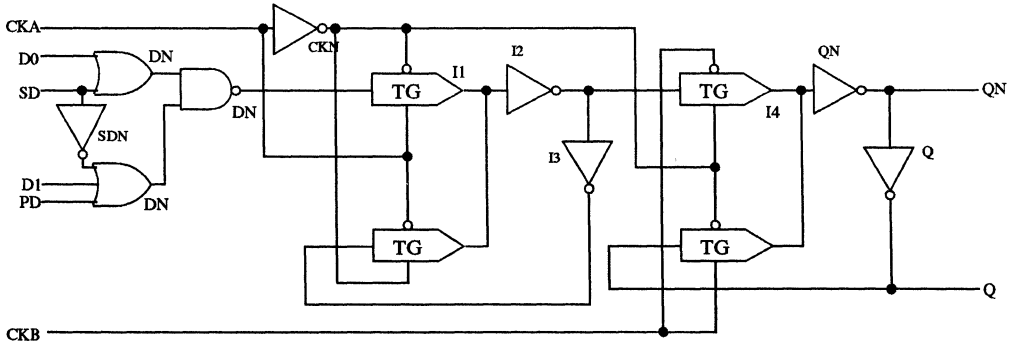
	D0	D1	CKA	CKB	SD	PD
Area	0.034pF	0.034pF	0.070pF	0.036pF	0.068pF	0.034pF
Perf	0.145pF	0.145pF	0.223pF	0.081pF	0.293pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	2.77ns	1.57ns	CK ↑	Q ↓	8.92ns/pF	1.34ns	1.67ns/pF	0.88ns
D0 ↑	2.00ns	1.10ns	CK ↑	Q ↑	6.55ns/pF	1.28ns	1.33ns/pF	0.91ns
D1 ↓	2.96ns	1.67ns	CK ↑	QN ↓	1.96ns/pF	1.20ns	0.44ns/pF	0.84ns
D1 ↑	2.10ns	1.19ns	CK ↑	QN ↑	3.61ns/pF	1.15ns	0.65ns/pF	0.77ns
PD ↓	2.96ns	1.67ns						
PD ↑	2.10ns	1.19ns						
SD ↓	2.77ns	1.57ns						
SD ↑	3.53ns	1.96ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2KX

Negative edge triggered, data select front end, negative asynchronous clear, negative asynchronous preset.

Grids 27, **Transistors** 38

Inputs
D0,D1,CKA,CKB,SD,PDNA,PDNB,CDN

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	CK	SD	PDN	CDN	Q	QN	Q	QN
X	X	X	X	X	0	X	X	0	1
X	X	X	X	0	1	X	X	1	0
0	X	↓	0	1	X	X	X	0	1
1	X	↓	0	X	1	X	X	1	0
X	0	↓	1	1	X	X	X	0	1
X	1	↓	1	X	1	X	X	1	0

X = Don't care

Capacitances

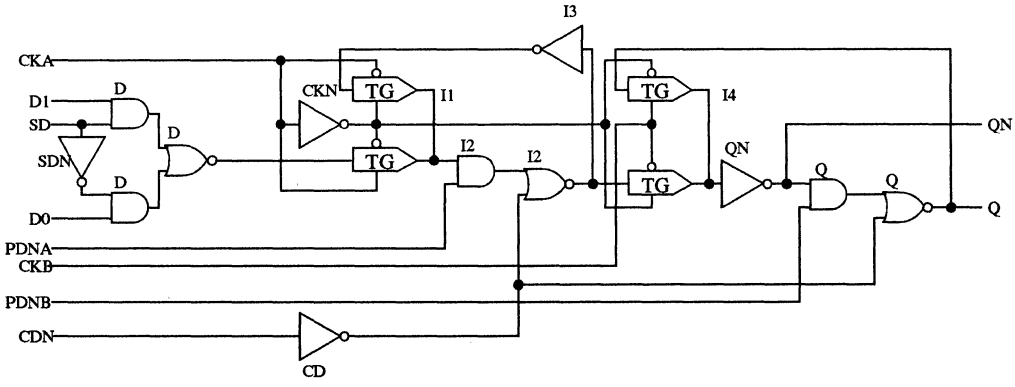
	D0	D1	CKA	CKB	SD	PDNA	PDNB	CDN
Area	0.034pF	0.037pF	0.070pF	0.036pF	0.068pF	0.034pF	0.034pF	0.034pF
Perf	0.145pF	0.148pF	0.223pF	0.081pF	0.293pF	0.145pF	0.145pF	0.145pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	2.29ns	1.43ns	CDN ↓	Q ↓	2.10ns/pF	1.04ns	0.16ns/pF	1.50ns
D0 ↑	2.43ns	1.48ns	CDN ↓	QN ↑	5.71ns/pF	1.72ns	0.83ns/pF	1.96ns
D1 ↓	2.29ns	1.43ns	CK ↑	Q ↓	10.74ns/pF	1.45ns	2.03ns/pF	1.07ns
D1 ↑	2.43ns	1.48ns	CK ↑	Q ↑	9.45ns/pF	1.66ns	1.85ns/pF	1.11ns
SD ↓	2.34ns	1.62ns	CK ↑	QN ↓	2.14ns/pF	1.11ns	0.44ns/pF	0.89ns
SD ↑	2.91ns	1.72ns	CK ↑	QN ↑	3.83ns/pF	1.05ns	0.65ns/pF	0.82ns
			PDN ↓	Q ↑	6.55ns/pF	0.90ns	1.25ns/pF	0.35ns
			PDN ↓	QN ↓	11.95ns/pF	2.37ns	2.19ns/pF	1.23ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2LX

Negative edge triggered, data select front end, negative synchronous preset.

Grids 23, **Transistors** 32

Inputs
D0,D1,CKA,CKB,SD,PDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	PDN	Q	QN	Q	QN
X	X	↓	1	0	X	X	1	0
0	X	↓	0	X	X	X	0	1
1	X	↓	0	X	X	X	1	0
X	0	↓	1	1	X	X	0	1
X	1	↓	1	X	X	X	1	0

X = Don't care **Note: PDN does not function while SD=0**

Capacitances

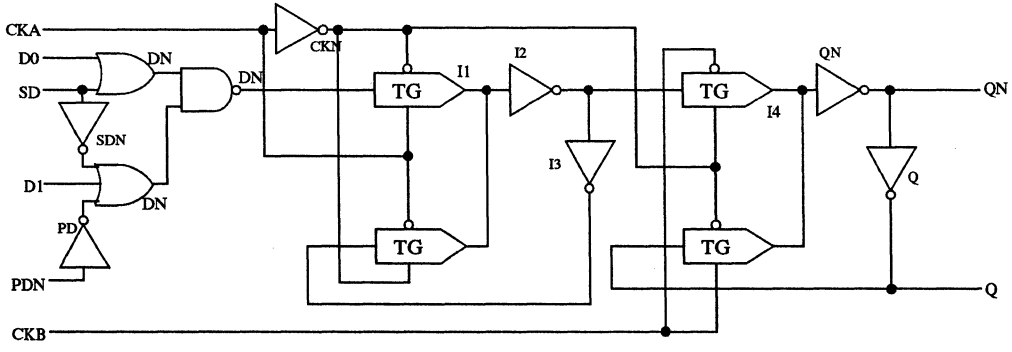
	D0	D1	CKA	CKB	SD	PDN
Area	0.034pF	0.034pF	0.070pF	0.036pF	0.068pF	0.034pF
Perf	0.145pF	0.145pF	0.223pF	0.081pF	0.293pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	2.81ns	1.57ns	CK ↑	Q ↓	8.92ns/pF	1.34ns	1.67ns/pF	0.88ns
D0 ↑	2.00ns	1.10ns	CK ↑	Q ↑	6.55ns/pF	1.28ns	1.33ns/pF	0.91ns
D1 ↓	3.01ns	1.67ns	CK ↑	QN ↓	1.96ns/pF	1.20ns	0.44ns/pF	0.84ns
D1 ↑	2.10ns	1.19ns	CK ↑	QN ↑	3.61ns/pF	1.15ns	0.65ns/pF	0.77ns
PDN ↓	1.96ns	1.34ns						
PDN ↑	3.58ns	1.96ns						
SD ↓	2.81ns	1.57ns						
SD ↑	3.58ns	1.96ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2MX

Negative edge triggered, data select front end, negative synchronous clear.

Grids 20, **Transistors** 30

Inputs
D0,D1,CKA,CKB,SD,CDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	CDN	Q	QN	Q	QN
X	X	↓	1	0	X	X	0	1
0	X	↓	0	X	X	X	0	1
1	X	↓	0	X	X	X	1	0
X	0	↓	1	X	X	X	0	1
X	1	↓	1	1	X	X	1	0

X = Don't care **Note: CDN does not function while SD=0**

Capacitances

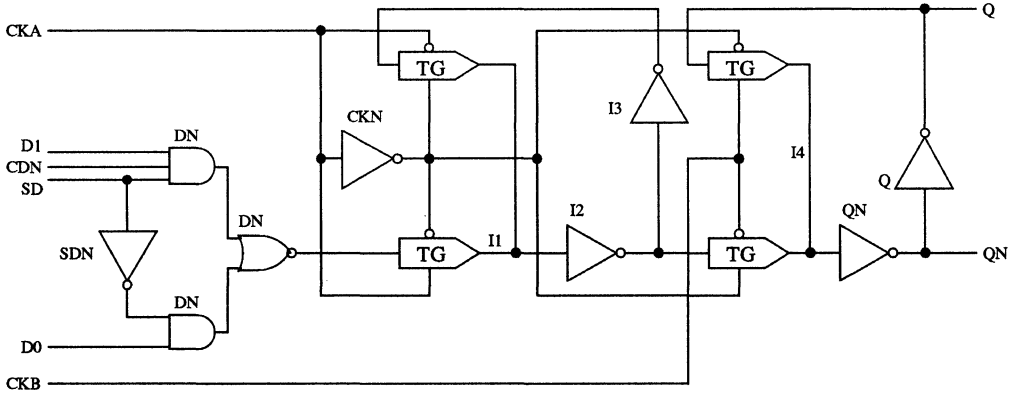
	D0	D1	CKA	CKB	SD	CDN
Area	0.034pF	0.034pF	0.070pF	0.036pF	0.071pF	0.034pF
Perf	0.145pF	0.145pF	0.224pF	0.081pF	0.295pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	2.24ns	1.34ns	CK ↑	Q ↓	9.01ns/pF	1.20ns	1.67ns/pF	0.88ns
CDN ↑	2.24ns	1.29ns	CK ↑	Q ↑	6.55ns/pF	1.23ns	1.33ns/pF	0.91ns
D0 ↓	2.24ns	1.34ns	CK ↑	QN ↓	1.96ns/pF	1.15ns	0.44ns/pF	0.84ns
D0 ↑	2.15ns	1.19ns	CK ↑	QN ↑	3.70ns/pF	1.02ns	0.65ns/pF	0.77ns
D1 ↓	2.24ns	1.34ns						
D1 ↑	2.24ns	1.29ns						
SD ↓	2.24ns	1.34ns						
SD ↑	2.81ns	1.62ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2NX

Negative edge triggered, data select front end, positive asynchronous clear, negative asynchronous preset.

Grids 25, **Transistors** 36

Inputs

D0,D1,CKA,CKB,SD,PDNA,PDNB,CD

Outputs

Q,QN

Truth Table

INPUTS						OUTPUTS OLD		OUTPUTS NEW	
D0	D1	CK	SD	PDN	CD	Q	QN	Q	QN
X	X	X	X	X	1	X	X	0	1
X	X	X	X	0	0	X	X	1	0
0	X	↓	0	1	X	X	X	0	1
1	X	↓	0	X	0	X	X	1	0
X	0	↓	1	1	X	X	X	0	1
X	1	↓	1	X	0	X	X	1	0

X = Don't care

Capacitances

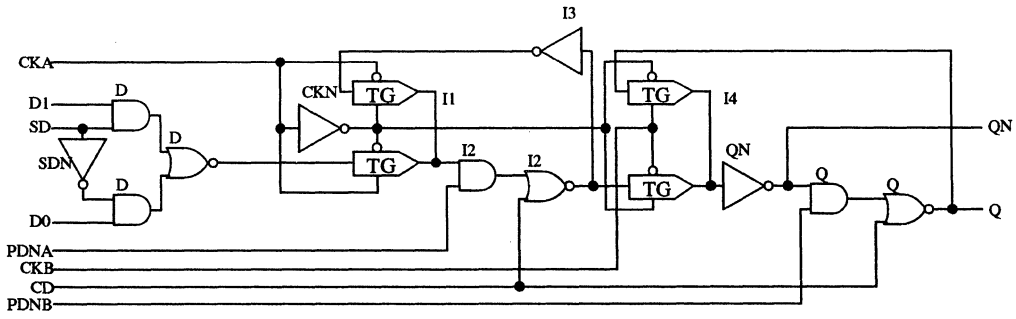
	D0	D1	CKA	CKB	SD	PDNA	PDNB	CD
Area	0.034pF	0.036pF	0.070pF	0.036pF	0.068pF	0.034pF	0.034pF	0.071pF
Perf	0.145pF	0.148pF	0.224pF	0.081pF	0.293pF	0.145pF	0.145pF	0.295pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
D0 ↓	2.29ns	1.43ns	CD ↑	Q ↓	2.32ns/pF	1.56ns	0.26ns/pF	1.08ns
D0 ↑	2.48ns	1.48ns	CD ↑	QN ↑	5.93ns/pF	2.23ns	0.94ns/pF	1.55ns
D1 ↓	2.29ns	1.43ns	CK ↑	Q ↓	10.74ns/pF	1.45ns	2.06ns/pF	1.04ns
D1 ↑	2.48ns	1.48ns	CK ↑	Q ↑	9.54ns/pF	1.57ns	1.90ns/pF	1.07ns
SD ↓	2.38ns	1.57ns	CK ↑	QN ↓	2.18ns/pF	1.09ns	0.50ns/pF	0.80ns
SD ↑	2.86ns	1.72ns	CK ↑	QN ↑	3.83ns/pF	1.05ns	0.70ns/pF	0.73ns
			PDN ↓	Q ↑	6.60ns/pF	0.83ns	1.25ns/pF	0.39ns
			PDN ↓	QN ↓	12.04ns/pF	2.29ns	2.19ns/pF	1.32ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2OX

Negative edge triggered, data select front end, positive synchronous clear, positive synchronous preset.

Grids 24, **Transistors** 34

Inputs
D0,D1,CKA,CKB,SD,PD,CD

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	CK	SD	PD	CD	Q	QN	Q	QN
0	X	↓	0	X	X	X	X	0	1
1	X	↓	0	X	X	X	X	1	0
X	X	↓	1	X	1	X	X	0	1
X	X	↓	1	1	0	X	X	1	0
X	0	↓	1	0	X	X	X	0	1
X	1	↓	1	X	0	X	X	1	0

X = Don't care **Note: PD/CD do not function while SD=0**

Capacitances

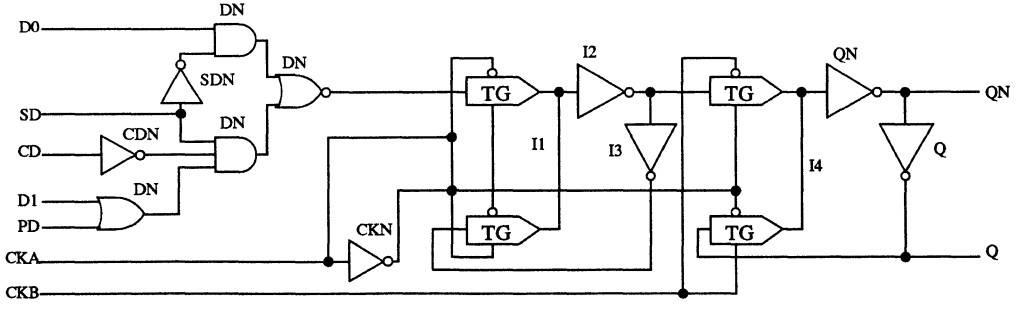
	D0	D1	CKA	CKB	SD	PD	CD
Area	0.061pF	0.061pF	0.097pF	0.063pF	0.098pF	0.061pF	0.061pF
Perf	0.222pF	0.222pF	0.300pF	0.158pF	0.373pF	0.222pF	0.222pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Perf.	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CD ↓	2.24ns	1.43ns	CK ↑	Q ↓	8.92ns/pF	1.34ns	1.67ns/pF	0.88ns
CD ↑	3.58ns	1.91ns	CK ↑	Q ↑	6.55ns/pF	1.28ns	1.33ns/pF	0.91ns
D0 ↓	2.91ns	1.62ns	CK ↑	QN ↓	1.96ns/pF	1.20ns	0.44ns/pF	0.84ns
D0 ↑	2.24ns	1.24ns	CK ↑	QN ↑	3.61ns/pF	1.15ns	0.65ns/pF	0.77ns
D1 ↓	3.15ns	1.72ns						
D1 ↑	2.43ns	1.38ns						
PD ↓	3.15ns	1.72ns						
PD ↑	2.43ns	1.38ns						
SD ↓	2.91ns	1.62ns						
SD ↑	3.48ns	1.91ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3AX

Positive edge triggered, data select front end.

Grids 19, **Transistors** 30

Inputs
D0,D1,CKA,CKB,SD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D0	D1	CK	SD	Q	QN	Q	QN
0	X	↑	0	X	X	0	1
1	X	↑	0	X	X	1	0
X	0	↑	1	X	X	0	1
X	1	↑	1	X	X	1	0

X = Don't care

Capacitances

	D0	D1	CKA	CKB	SD
Area	0.034pF	0.037pF	0.070pF	0.036pF	0.066pF
Perf	0.145pF	0.148pF	0.223pF	0.081pF	0.291pF

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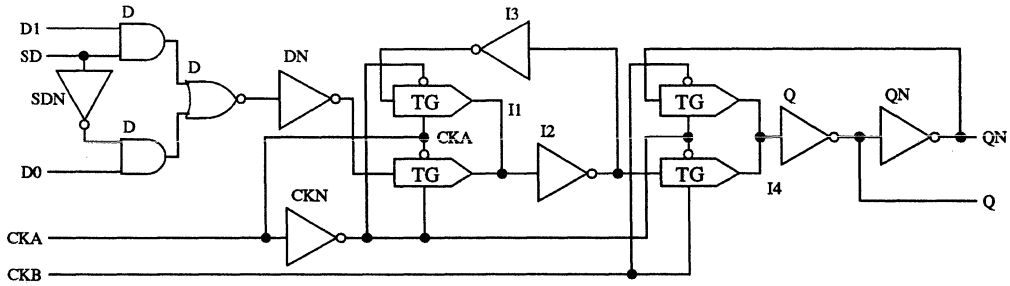
Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.96ns	1.34ns	CK ↑	Q ↓	1.96ns/pF	1.96ns	0.44ns/pF	1.13ns
D0 ↑	2.24ns	1.43ns	CK ↑	Q ↑	3.70ns/pF	1.83ns	0.63ns/pF	1.08ns
D1 ↓	1.96ns	1.34ns	CK ↑	QN ↓	9.01ns/pF	2.01ns	1.64ns/pF	1.18ns
D1 ↑	2.24ns	1.43ns	CK ↑	QN ↑	6.55ns/pF	2.04ns	1.33ns/pF	1.19ns
SD ↓	2.15ns	1.53ns						
SD ↑	2.62ns	1.62ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3BX

Positive edge triggered, data select front end, positive asynchronous preset.

Grids 22, **Transistors** 34

Inputs
D0,D1,CKA,CKB,SD,PD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	PD	Q	QN	Q	QN
X	X	X	X	1	X	X	1	0
0	X	↑	0	0	X	X	0	1
1	X	↑	0	X	X	X	1	0
X	0	↑	1	0	X	X	0	1
X	1	↑	1	X	X	X	1	0

X = Don't care

Capacitances

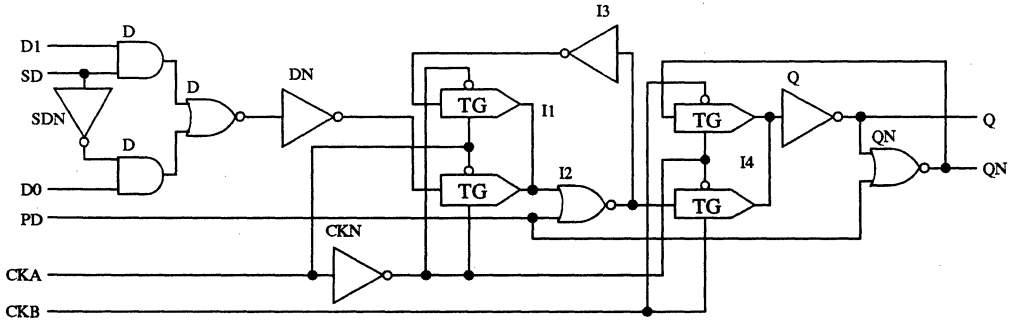
	D0	D1	CKA	CKB	SD	PD
Area	0.034pF	0.037pF	0.070pF	0.035pF	0.066pF	0.073pF
Perf	0.145pF	0.148pF	0.224pF	0.080pF	0.291pF	0.298pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	2.38ns	1.53ns	CK ↑	Q ↓	1.78ns/pF	2.04ns	0.44ns/pF	1.13ns
D0 ↑	2.19ns	1.48ns	CK ↑	Q ↑	3.48ns/pF	1.98ns	0.65ns/pF	1.06ns
D1 ↓	2.38ns	1.53ns	CK ↑	QN ↓	8.83ns/pF	2.24ns	1.69ns/pF	1.19ns
D1 ↑	2.19ns	1.48ns	CK ↑	QN ↑	9.01ns/pF	2.34ns	1.82ns/pF	1.28ns
SD ↓	2.38ns	1.57ns	PD ↑	Q ↑	6.55ns/pF	1.71ns	1.20ns/pF	0.91ns
SD ↑	3.05ns	1.81ns	PD ↑	QN ↓	2.90ns/pF	1.20ns	0.57ns/pF	0.41ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3CX

Positive edge triggered, data select front end, positive asynchronous clear, positive asynchronous preset.

Grids 28, **Transistors** 40

Inputs
D0,D1,CKA,CKB,SD,PDA,PDB,CD

Outputs
Q,QN

Capacitances

	D0	D1	CKA	CKB	SD	PDA	PDB	CD
Area	0.034pF	0.037pF	0.076pF	0.036pF	0.068pF	0.034pF	0.034pF	0.034pF
Perf	0.145pF	0.148pF	0.231pF	0.081pF	0.293pF	0.145pF	0.145pF	0.145pF

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	CK	SD	PD	CD	Q	QN	Q	QN
X	X	X	X	X	1	X	X	0	1
X	X	X	X	1	0	X	X	1	0
0	X	↑	0	0	X	X	X	0	1
1	X	↑	0	X	0	X	X	1	0
X	0	↑	1	0	X	X	X	0	1
X	1	↑	1	X	0	X	X	1	0

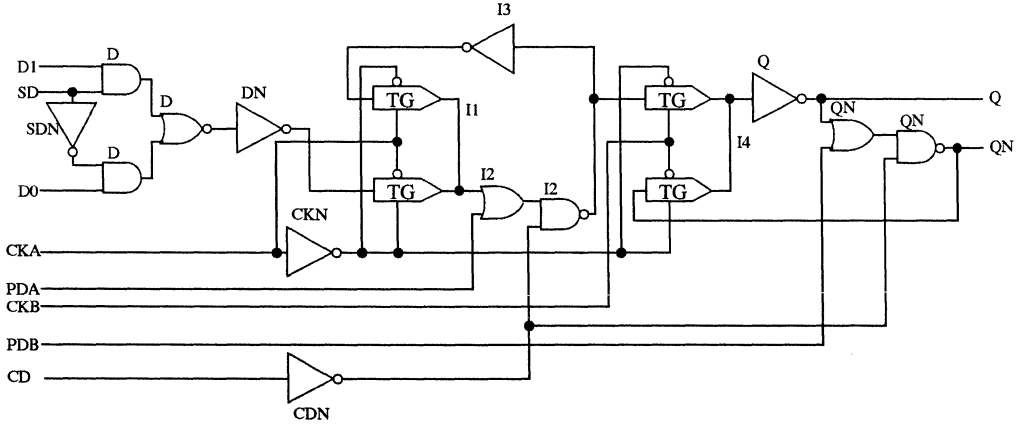
X = Don't care

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	2.43ns	1.62ns	CD ↑	Q ↓	9.09ns/pF	2.69ns	1.67ns/pF	1.45ns
D0 ↑	2.38ns	1.57ns	CD ↑	QN ↑	3.88ns/pF	1.27ns	0.78ns/pF	0.53ns
D1 ↓	2.43ns	1.62ns	CK ↑	Q ↓	2.18ns/pF	1.86ns	0.47ns/pF	1.06ns
D1 ↑	2.38ns	1.57ns	CK ↑	Q ↑	3.88ns/pF	1.79ns	0.68ns/pF	0.99ns
SD ↓	2.43ns	1.67ns	CK ↑	QN ↓	10.92ns/pF	2.18ns	2.09ns/pF	1.21ns
SD ↑	3.05ns	1.91ns	CK ↑	QN ↑	9.50ns/pF	2.36ns	1.85ns/pF	1.30ns
			PD ↑	Q ↑	8.11ns/pF	1.94ns	1.51ns/pF	1.14ns
			PD ↑	QN ↓	4.50ns/pF	1.27ns	0.83ns/pF	0.68ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3DX

Positive edge triggered, data select front end, positive asynchronous clear.

Grids 22, **Transistors** 32

Inputs
D0,D1,CKA,CKB,SD,CD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	CD	Q	QN	Q	QN
X	X	X	X	1	X	X	0	1
0	X	↑	0	X	X	X	0	1
1	X	↑	0	0	X	X	1	0
X	0	↑	1	X	X	X	0	1
X	1	↑	1	0	X	X	1	0

X = Don't care

Capacitances

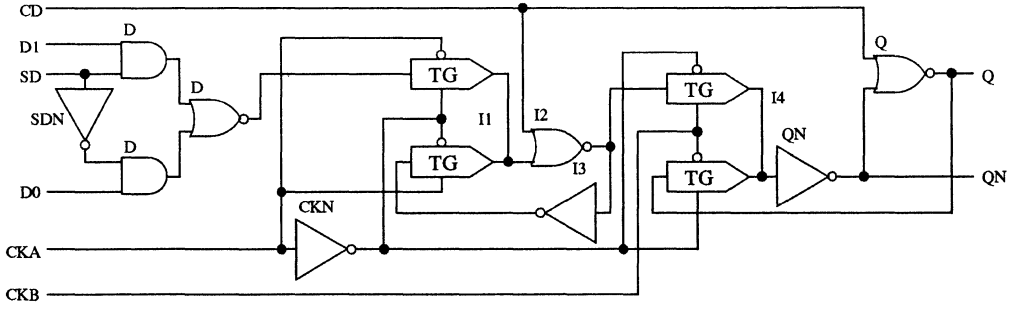
	D0	D1	CKA	CKB	SD	CD
Area	0.034pF	0.036pF	0.070pF	0.035pF	0.068pF	0.071pF
Perf	0.145pF	0.148pF	0.223pF	0.080pF	0.293pF	0.296pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	2.19ns	1.34ns	CD ↑	Q ↓	2.90ns/pF	1.20ns	0.57ns/pF	0.41ns
D0 ↑	2.38ns	1.38ns	CD ↑	QN ↑	6.55ns/pF	1.66ns	1.20ns/pF	0.91ns
D1 ↓	2.19ns	1.34ns	CK ↑	Q ↓	8.92ns/pF	2.10ns	1.69ns/pF	1.19ns
D1 ↑	2.38ns	1.38ns	CK ↑	Q ↑	9.05ns/pF	2.28ns	1.82ns/pF	1.28ns
SD ↓	2.29ns	1.48ns	CK ↑	QN ↓	1.83ns/pF	1.97ns	0.44ns/pF	1.13ns
SD ↑	2.77ns	1.62ns	CK ↑	QN ↑	3.57ns/pF	1.84ns	0.65ns/pF	1.06ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3EX

Positive edge triggered, data select front end, negative asynchronous clear.

Grids 22, **Transistors** 34

Inputs
D0,D1,CKA,CKB,SD,CDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	CDN	Q	QN	Q	QN
X	X	X	X	0	X	X	0	1
0	X	↑	0	X	X	X	0	1
1	X	↑	0	1	X	X	1	0
X	0	↑	1	X	X	X	0	1
X	1	↑	1	1	X	X	1	0

X = Don't care

Capacitances

	D0	D1	CKA	CKB	SD	CDN
Area	0.034pF	0.037pF	0.070pF	0.036pF	0.066pF	0.073pF
Perf	0.145pF	0.148pF	0.224pF	0.081pF	0.291pF	0.298pF

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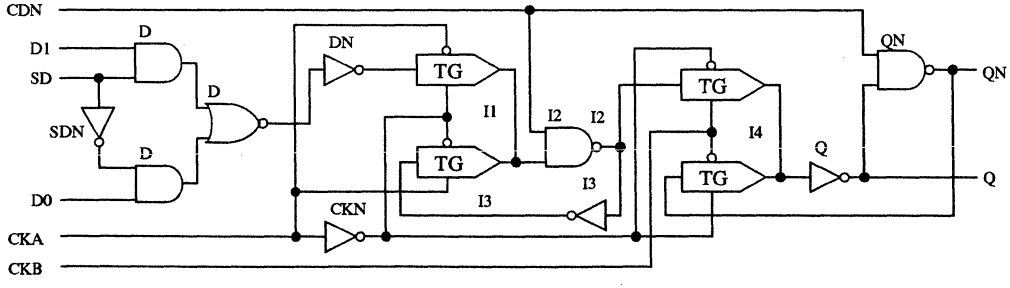
Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	2.05ns	1.38ns	CDN ↓	Q ↓	7.09ns/pF	1.51ns	1.41ns/pF	0.84ns
D0 ↑	2.38ns	1.57ns	CDN ↓	QN ↑	3.70ns/pF	0.59ns	0.78ns/pF	0.10ns
D1 ↓	2.05ns	1.38ns	CK ↑	Q ↓	2.01ns/pF	2.03ns	0.44ns/pF	1.13ns
D1 ↑	2.38ns	1.57ns	CK ↑	Q ↑	3.70ns/pF	1.97ns	0.63ns/pF	1.08ns
SD ↓	2.29ns	1.67ns	CK ↑	QN ↓	10.48ns/pF	2.24ns	1.98ns/pF	1.25ns
SD ↑	2.72ns	1.67ns	CK ↑	QN ↑	6.64ns/pF	2.19ns	1.36ns/pF	1.22ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3FX

Positive edge triggered, data select front end, negative asynchronous clear, positive asynchronous preset.

Grids 25, **Transistors** 38

Inputs
D0,D1,CKA,CKB,SD,PDA,PDB,CDN

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS OLD		OUTPUTS NEW	
D0	D1	CK	SD	PD	CDN	Q	QN	Q	QN
X	X	X	X	X	0	X	X	0	1
X	X	X	X	1	1	X	X	1	0
0	X	↑	0	0	X	X	X	0	1
1	X	↑	0	X	1	X	X	1	0
X	0	↑	1	0	X	X	X	0	1
X	1	↑	1	X	1	X	X	1	0

X = Don't care

Capacitances

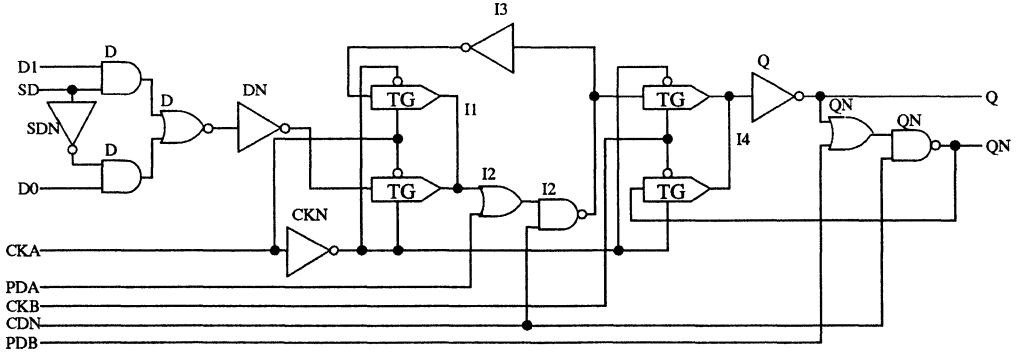
	D0	D1	CKA	CKB	SD	PDA	PDB	CDN
Area	0.034pF	0.037pF	0.070pF	0.036pF	0.069pF	0.034pF	0.034pF	0.071pF
Perf	0.145pF	0.149pF	0.224pF	0.082pF	0.294pF	0.145pF	0.145pF	0.296pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	2.53ns	1.62ns	CDN ↓	Q ↓	8.92ns/pF	2.00ns	1.59ns/pF	1.18ns
D0 ↑	2.48ns	1.57ns	CDN ↓	QN ↑	3.66ns/pF	0.61ns	0.68ns/pF	0.28ns
D1 ↓	2.53ns	1.62ns	CK ↑	Q ↓	2.23ns/pF	1.79ns	0.47ns/pF	1.06ns
D1 ↑	2.48ns	1.57ns	CK ↑	Q ↑	3.88ns/pF	1.75ns	0.68ns/pF	0.99ns
SD ↓	2.53ns	1.62ns	CK ↑	QN ↓	10.88ns/pF	2.15ns	2.06ns/pF	1.28ns
SD ↑	3.10ns	1.91ns	CK ↑	QN ↑	9.54ns/pF	2.29ns	1.85ns/pF	1.35ns
			PD ↑	Q ↑	8.07ns/pF	1.96ns	1.90ns/pF	0.88ns
			PD ↑	QN ↓	4.46ns/pF	1.29ns	1.23ns/pF	0.42ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3GX

Positive edge triggered, data select front end, negative asynchronous preset.

Grids 22, **Transistors** 32

Inputs
D0,D1,CKA,CKB,SD,PDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	PDN	Q	QN	Q	QN
X	X	X	X	0	X	X	1	0
0	X	↑	0	1	X	X	0	1
1	X	↑	0	X	X	X	1	0
X	0	↑	1	1	X	X	0	1
X	1	↑	1	X	X	X	1	0

X = Don't care

Capacitances

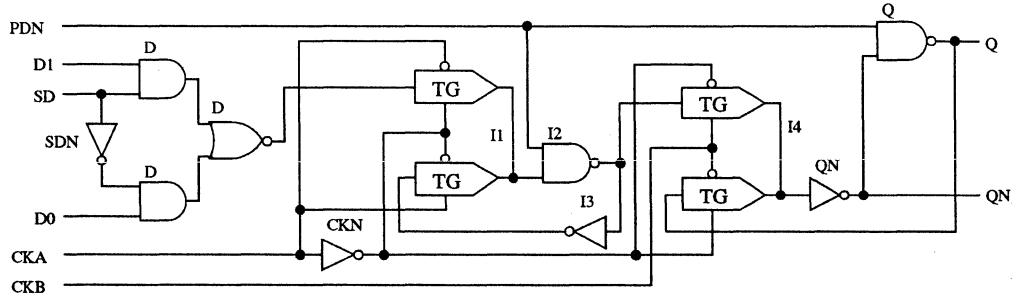
	D0	D1	CKA	CKB	SD	PDN
Area	0.034pF	0.036pF	0.070pF	0.036pF	0.068pF	0.073pF
Perf	0.145pF	0.148pF	0.224pF	0.081pF	0.293pF	0.298pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	2.38ns	1.43ns	CK ↑	Q ↓	10.61ns/pF	2.04ns	2.03ns/pF	1.11ns
D0 ↑	2.05ns	1.24ns	CK ↑	Q ↑	6.73ns/pF	2.06ns	1.41ns/pF	1.08ns
D1 ↓	2.38ns	1.43ns	CK ↑	QN ↓	2.10ns/pF	1.90ns	0.50ns/pF	0.99ns
D1 ↑	2.05ns	1.24ns	CK ↑	QN ↑	3.83ns/pF	1.77ns	0.68ns/pF	0.94ns
SD ↓	2.38ns	1.43ns	PDN ↓	Q ↑	3.70ns/pF	0.59ns	0.78ns/pF	0.10ns
SD ↑	2.96ns	1.72ns	PDN ↓	QN ↓	7.04ns/pF	1.53ns	1.43ns/pF	0.78ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3IX

Positive edge triggered, data select front end, positive synchronous clear.

Grids 23, **Transistors** 32

Inputs
D0,D1,CKA,CKB,SD,CD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	CD	Q	QN	Q	QN
X	X	↑	1	1	X	X	0	1
0	X	↑	0	X	X	X	0	1
1	X	↑	0	X	X	X	1	0
X	0	↑	1	X	X	X	0	1
X	1	↑	1	0	X	X	1	0

X = Don't care **Note: CD does not function while SD=0**

Capacitances

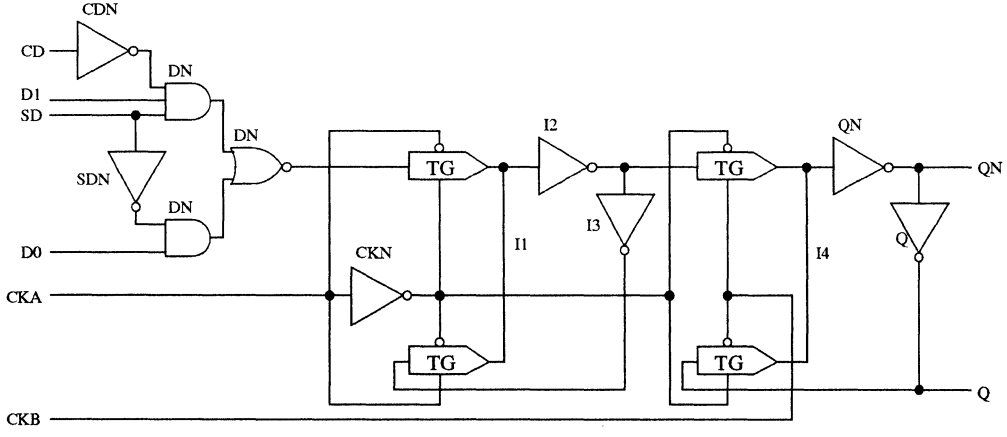
	D0	D1	CKA	CKB	SD	CD
Area	0.034pF	0.034pF	0.070pF	0.036pF	0.071pF	0.034pF
Perf	0.145pF	0.145pF	0.223pF	0.081pF	0.295pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CD ↓	2.19ns	1.38ns	CK ↑	Q ↓	8.92ns/pF	2.15ns	1.69ns/pF	1.14ns
CD ↑	2.91ns	1.62ns	CK ↑	Q ↑	6.55ns/pF	2.09ns	1.36ns/pF	1.17ns
D0 ↓	2.29ns	1.34ns	CK ↑	QN ↓	1.96ns/pF	2.01ns	0.47ns/pF	1.11ns
D0 ↑	2.19ns	1.19ns	CK ↑	QN ↑	3.61ns/pF	1.96ns	0.68ns/pF	1.04ns
D1 ↓	2.29ns	1.34ns						
D1 ↑	2.29ns	1.29ns						
SD ↓	2.29ns	1.34ns						
SD ↑	2.86ns	1.62ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3JX

Positive edge triggered, data select front end, positive synchronous preset.

Grids 21, **Transistors** 30

Inputs
D0,D1,CKA,CKB,SD,PD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	PD	Q	QN	Q	QN
X	X	↑	1	1	X	X	1	0
0	X	↑	0	X	X	X	0	1
1	X	↑	0	X	X	X	1	0
X	0	↑	1	0	X	X	0	1
X	1	↑	1	X	X	X	1	0

X = Don't care **Note: PD does not function while SD=0**

Capacitances

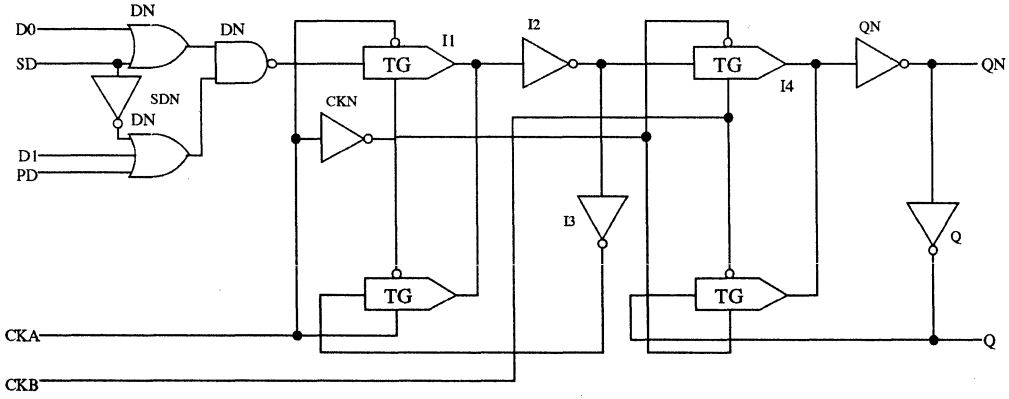
	D0	D1	CKA	CKB	SD	PD
Area	0.034pF	0.034pF	0.070pF	0.036pF	0.068pF	0.034pF
Perf	0.145pF	0.145pF	0.223pF	0.081pF	0.293pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	2.77ns	1.57ns	CK ↑	Q ↓	8.92ns/pF	2.15ns	1.69ns/pF	1.14ns
D0 ↑	2.00ns	1.14ns	CK ↑	Q ↑	6.55ns/pF	2.09ns	1.36ns/pF	1.17ns
D1 ↓	2.96ns	1.67ns	CK ↑	QN ↓	1.96ns/pF	2.01ns	0.47ns/pF	1.11ns
D1 ↑	2.10ns	1.24ns	CK ↑	QN ↑	3.61ns/pF	1.96ns	0.68ns/pF	1.04ns
PD ↓	2.96ns	1.67ns						
PD ↑	2.10ns	1.24ns						
SD ↓	2.77ns	1.57ns						
SD ↑	3.53ns	1.96ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3KX

Positive edge triggered, data select front end, negative asynchronous clear, negative asynchronous preset.

Grids 27, **Transistors** 38

Inputs
D0,D1,CKA,CKB,SD,PDNA,PDNB,CDN

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	CK	SD	PDN	CDN	Q	QN	Q	QN
X	X	X	X	X	0	X	X	0	1
X	X	X	X	0	1	X	X	1	0
0	X	↑	0	1	X	X	X	0	1
1	X	↑	0	X	1	X	X	1	0
X	0	↑	1	1	X	X	X	0	1
X	1	↑	1	X	1	X	X	1	0

X = Don't care

Capacitances

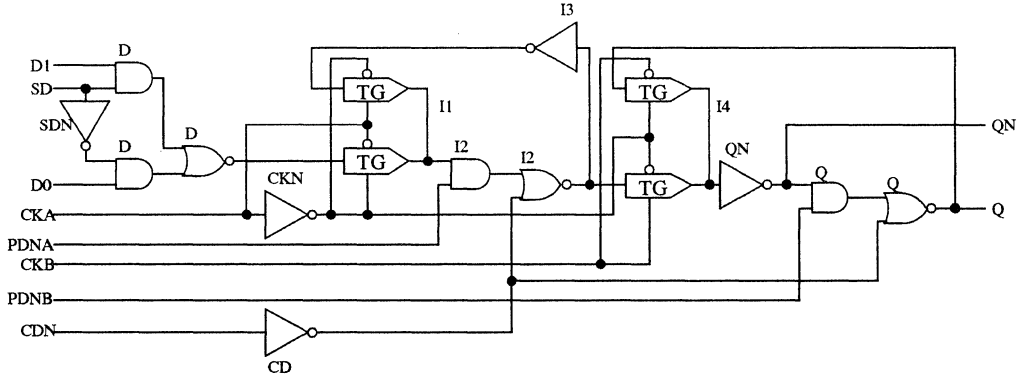
	D0	D1	CKA	CKB	SD	PDNA	PDNB	CDN
Area	0.034pF	0.037pF	0.070pF	0.035pF	0.068pF	0.034pF	0.034pF	0.034pF
Perf	0.145pF	0.148pF	0.223pF	0.080pF	0.293pF	0.145pF	0.145pF	0.145pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
D0 ↓	2.34ns	1.43ns	CDN ↓	Q ↓	2.10ns/pF	1.04ns	0.16ns/pF	1.50ns
D0 ↑	2.43ns	1.48ns	CDN ↓	QN ↑	5.71ns/pF	1.72ns	0.83ns/pF	1.96ns
D1 ↓	2.34ns	1.43ns	CK ↑	Q ↓	10.79ns/pF	2.24ns	2.06ns/pF	1.24ns
D1 ↑	2.43ns	1.48ns	CK ↑	Q ↑	9.50ns/pF	2.45ns	1.88ns/pF	1.28ns
SD ↓	2.34ns	1.62ns	CK ↑	QN ↓	2.18ns/pF	1.90ns	0.47ns/pF	1.06ns
SD ↑	2.96ns	1.72ns	CK ↑	QN ↑	3.88ns/pF	1.84ns	0.68ns/pF	0.99ns
			PDN ↓	Q ↑	6.55ns/pF	0.90ns	1.25ns/pF	0.35ns
			PDN ↓	QN ↓	11.95ns/pF	2.37ns	2.19ns/pF	1.23ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3LX

Positive edge triggered, data select front end, negative synchronous preset.

Grids 23, **Transistors** 32

Inputs
D0,D1,CKA,CKB,SD,PDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	PDN	Q	QN	Q	QN
X	X	↑	1	0	X	X	1	0
0	X	↑	0	X	X	X	0	1
1	X	↑	0	X	X	X	1	0
X	0	↑	1	1	X	X	0	1
X	1	↑	1	X	X	X	1	0

X = Don't care **Note: PDN does not function while SD=0**

Capacitances

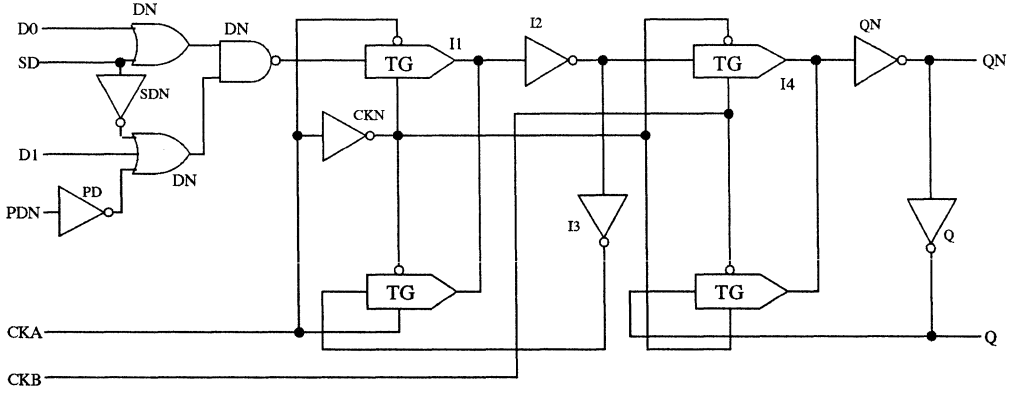
	D0	D1	CKA	CKB	SD	PDN
Area	0.034pF	0.034pF	0.070pF	0.036pF	0.068pF	0.034pF
Perf	0.145pF	0.145pF	0.223pF	0.081pF	0.293pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	2.81ns	1.57ns	CK ↑	Q ↓	8.92ns/pF	2.15ns	1.69ns/pF	1.14ns
D0 ↑	2.00ns	1.10ns	CK ↑	Q ↑	6.55ns/pF	2.09ns	1.36ns/pF	1.17ns
D1 ↓	3.01ns	1.67ns	CK ↑	QN ↓	1.96ns/pF	2.01ns	0.47ns/pF	1.11ns
D1 ↑	2.10ns	1.19ns	CK ↑	QN ↑	3.61ns/pF	1.96ns	0.68ns/pF	1.04ns
PDN ↓	1.96ns	1.34ns						
PDN ↑	3.58ns	1.96ns						
SD ↓	2.81ns	1.57ns						
SD ↑	3.58ns	1.96ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3MX

Positive edge triggered, data select front end, negative synchronous clear.

Grids 20, **Transistors** 30

Inputs
D0,D1,CKA,CKB,SD,CDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	CDN	Q	QN	Q	QN
X	X	↑	1	0	X	X	0	1
0	X	↑	0	X	X	X	0	1
1	X	↑	0	X	X	X	1	0
X	0	↑	1	X	X	X	0	1
X	1	↑	1	1	X	X	1	0

X = Don't care **Note: CDN does not function while SD=0**

Capacitances

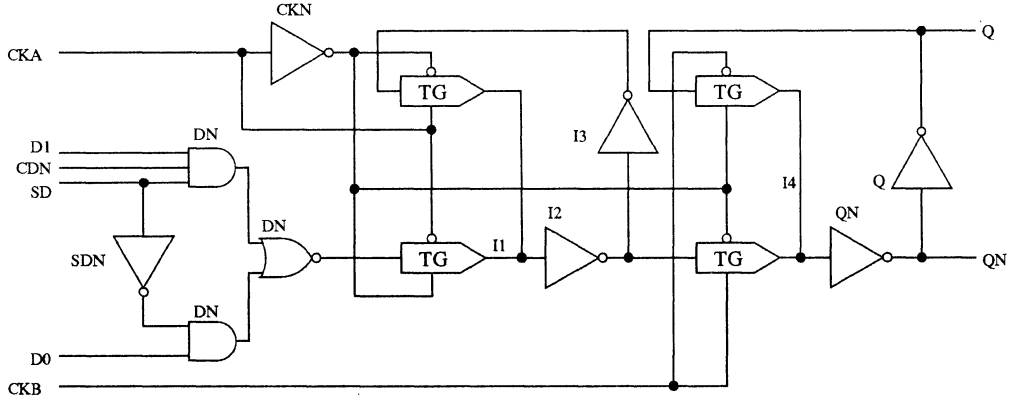
	D0	D1	CKA	CKB	SD	CDN
Area	0.034pF	0.034pF	0.070pF	0.036pF	0.071pF	0.034pF
Perf	0.145pF	0.145pF	0.224pF	0.081pF	0.295pF	0.145pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
CDN ↓	2.34ns	1.34ns	CK ↑	Q ↓	9.01ns/pF	1.96ns	1.67ns/pF	1.11ns
CDN ↑	2.24ns	1.34ns	CK ↑	Q ↑	6.55ns/pF	1.99ns	1.36ns/pF	1.12ns
D0 ↓	2.34ns	1.34ns	CK ↑	QN ↓	1.96ns/pF	1.91ns	0.47ns/pF	1.06ns
D0 ↑	2.15ns	1.24ns	CK ↑	QN ↑	3.70ns/pF	1.78ns	0.65ns/pF	1.01ns
D1 ↓	2.34ns	1.34ns						
D1 ↑	2.24ns	1.34ns						
SD ↓	2.34ns	1.38ns						
SD ↑	2.91ns	1.62ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3NX

Positive edge triggered, data select front end, positive asynchronous clear, negative asynchronous preset.

Grids 25, **Transistors** 36

Inputs
D0,D1,CKA,CKB,SD,PDNA,PDNB,CD

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	CK	SD	PDN	CD	Q	QN	Q	QN
X	X	X	X	X	1	X	X	0	1
X	X	X	X	0	0	X	X	1	0
0	X	↑	0	1	X	X	X	0	1
1	X	↑	0	X	0	X	X	1	0
X	0	↑	1	1	X	X	X	0	1
X	1	↑	1	X	0	X	X	1	0

X = Don't care

Capacitances

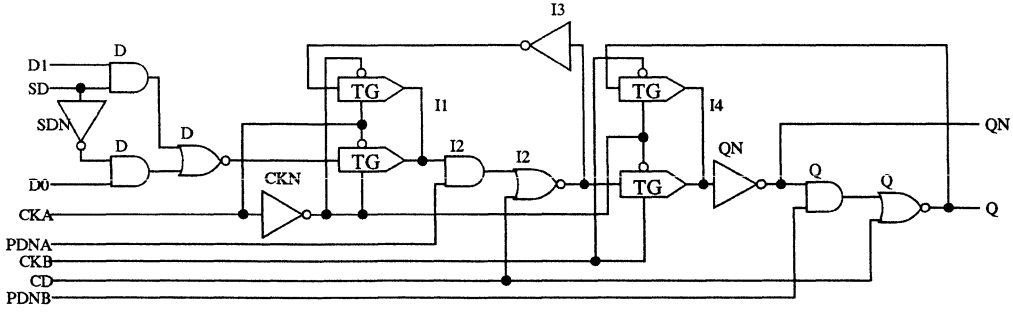
	D0	D1	CKA	CKB	SD	PDNA	PDNB	CD
Area	0.034pF	0.036pF	0.070pF	0.035pF	0.068pF	0.034pF	0.034pF	0.070pF
Perf	0.145pF	0.148pF	0.223pF	0.080pF	0.293pF	0.145pF	0.145pF	0.295pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	2.34ns	1.43ns	CD ↑	Q ↓	2.32ns/pF	1.56ns	0.26ns/pF	1.08ns
D0 ↑	2.43ns	1.48ns	CD ↑	QN ↑	5.93ns/pF	2.23ns	0.94ns/pF	1.55ns
D1 ↓	2.34ns	1.43ns	CK ↑	Q ↓	10.79ns/pF	2.19ns	2.01ns/pF	1.37ns
D1 ↑	2.43ns	1.48ns	CK ↑	Q ↑	9.58ns/pF	2.32ns	1.85ns/pF	1.40ns
SD ↓	2.34ns	1.57ns	CK ↑	QN ↓	2.23ns/pF	1.84ns	0.44ns/pF	1.13ns
SD ↑	2.91ns	1.72ns	CK ↑	QN ↑	3.88ns/pF	1.79ns	0.65ns/pF	1.06ns
			PDN ↓	Q ↑	6.60ns/pF	0.83ns	1.25ns/pF	0.39ns
			PDN ↓	QN ↓	12.04ns/pF	2.29ns	2.19ns/pF	1.32ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3OX

Positive edge triggered, data select front end, positive synchronous clear, positive synchronous preset.

Grids 24, **Transistors** 34

Inputs
D0,D1,CKA,CKB,SD,PD,CD

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS OLD		OUTPUTS NEW	
D0	D1	CK	SD	PD	CD	Q	QN	Q	QN
0	X	↑	0	X	X	X	X	0	1
1	X	↑	0	X	X	X	X	1	0
X	X	↑	1	X	1	X	X	0	1
X	X	↑	1	1	0	X	X	1	0
X	0	↑	1	0	X	X	X	0	1
X	1	↑	1	X	0	X	X	1	0

X = Don't care **Note: PD/CD do not function while SD=0**

Capacitances

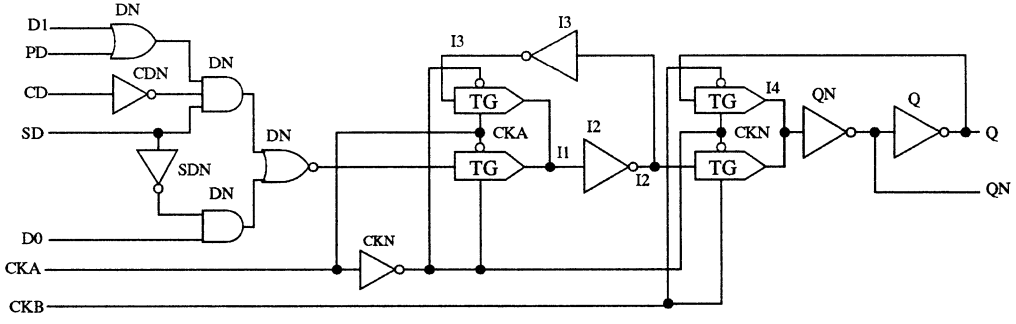
	D0	D1	CKA	CKB	SD	PD	CD
Area	0.061pF	0.061pF	0.097pF	0.063pF	0.098pF	0.061pF	0.061pF
Perf	0.222pF	0.222pF	0.301pF	0.158pF	0.373pF	0.222pF	0.222pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Perf. Extrinsic	Propagation Delay Perf. Intrinsic
CD ↓	2.24ns	1.43ns	CK ↑	Q ↓	8.92ns/pF	2.15ns	1.69ns/pF	1.14ns
CD ↑	3.53ns	1.91ns	CK ↑	Q ↑	6.55ns/pF	2.09ns	1.36ns/pF	1.17ns
D0 ↓	2.86ns	1.62ns	CK ↑	QN ↓	1.96ns/pF	2.01ns	0.47ns/pF	1.11ns
D0 ↑	2.24ns	1.24ns	CK ↑	QN ↑	3.61ns/pF	1.96ns	0.68ns/pF	1.04ns
D1 ↓	3.10ns	1.72ns						
D1 ↑	2.43ns	1.38ns						
PD ↓	3.10ns	1.72ns						
PD ↑	2.43ns	1.38ns						
SD ↓	2.86ns	1.62ns						
SD ↑	3.43ns	1.91ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1A

Master-Slave clocking, data select front end.

Grids 20, **Transistors** 32

Inputs
D0,D1,MCK,SCK,SD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	MCK	SCK	SD	Q	QN	Q	QN
0	X	↓	↑	0	X	X	0	1
1	X	↓	↑	0	X	X	1	0
X	0	↓	↑	1	X	X	0	1
X	1	↓	↑	1	X	X	1	0

X = Don't care

Capacitances

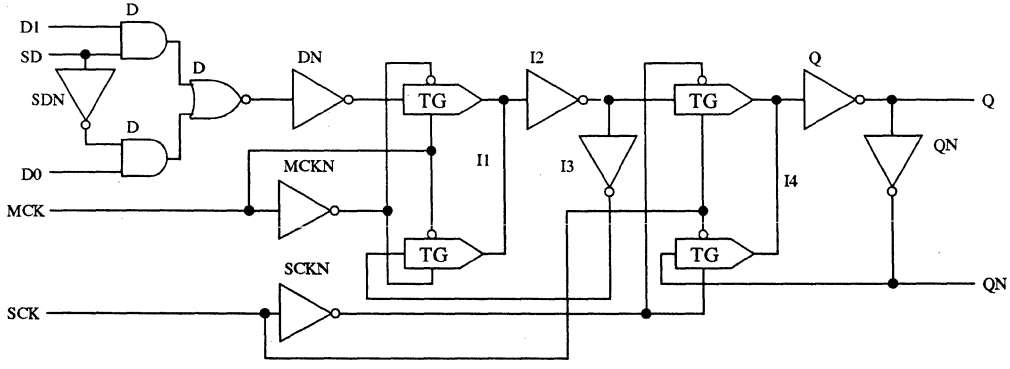
	D0	D1	MCK	SCK	SD
Area	0.034pF	0.037pF	0.075pF	0.070pF	0.066pF
Perf	0.145pF	0.148pF	0.230pF	0.229pF	0.291pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	1.96ns	1.29ns	SCK ↑	Q ↓	1.92ns/pF	1.69ns	0.44ns/pF	0.99ns
D0 ↑	2.10ns	1.38ns	SCK ↑	Q ↑	3.61ns/pF	1.44ns	0.68ns/pF	0.80ns
D1 ↓	1.96ns	1.29ns	SCK ↑	QN ↓	8.87ns/pF	1.74ns	1.69ns/pF	0.95ns
D1 ↑	2.10ns	1.38ns	SCK ↑	QN ↑	6.51ns/pF	1.87ns	1.33ns/pF	1.10ns
SD ↓	1.96ns	1.48ns						
SD ↑	2.62ns	1.57ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1B

Master-Slave clocking, data select front end, positive asynchronous preset.

Grids 23, **Transistors** 36

Inputs
D0,D1,MCK,SCK,SD,PD

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	MCK	SCK	SD	PD	Q	QN	Q	QN
X	X	X	X	X	1	X	X	1	0
0	X	↓	↑	0	0	X	X	0	1
1	X	↓	↑	0	X	X	X	1	0
X	0	↓	↑	1	0	X	X	0	1
X	1	↓	↑	1	X	X	X	1	0

X = Don't care

Capacitances

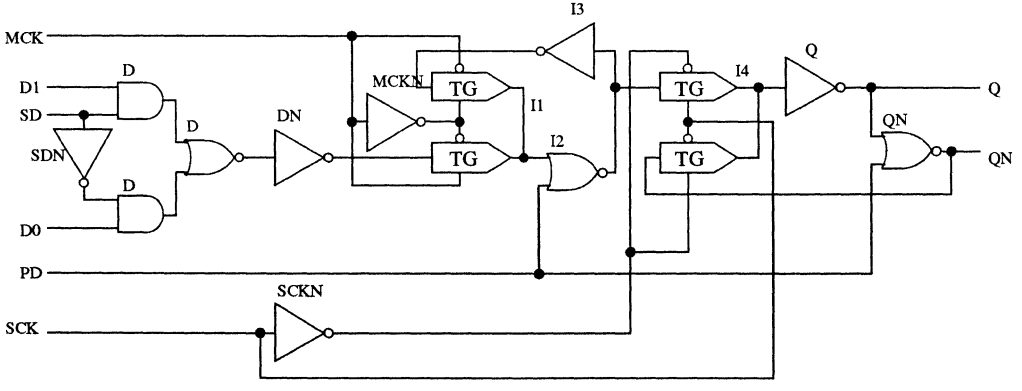
	D0	D1	MCK	SCK	SD	PD
Area	0.034pF	0.036pF	0.070pF	0.074pF	0.066pF	0.069pF
Perf	0.145pF	0.148pF	0.223pF	0.228pF	0.291pF	0.294pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	2.43ns	1.53ns	PD ↑	Q ↑	6.60ns/pF	1.59ns	1.20ns/pF	0.87ns
D0 ↑	2.19ns	1.48ns	PD ↑	QN ↓	2.90ns/pF	1.20ns	0.57ns/pF	0.41ns
D1 ↓	2.43ns	1.53ns	SCK ↑	Q ↓	1.96ns/pF	1.67ns	0.47ns/pF	0.96ns
D1 ↑	2.19ns	1.48ns	SCK ↑	Q ↑	3.57ns/pF	1.60ns	0.70ns/pF	0.78ns
SD ↓	2.43ns	1.57ns	SCK ↑	QN ↓	8.92ns/pF	1.86ns	1.75ns/pF	0.91ns
SD ↑	3.10ns	1.81ns	SCK ↑	QN ↑	9.14ns/pF	2.04ns	1.85ns/pF	1.11ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1CX

Master-Slave clocking, data select front end, positive asynchronous clear, positive asynchronous preset.

Grids 26, **Transistors** 42

Inputs
D0,D1,MCK,SCK,SD,PDA,PDB,CD

Outputs
Q,QN

Capacitances

	D0	D1	MCK	SCK	SD	PDA	PDB	CD
Area	0.034pF	0.037pF	0.070pF	0.070pF	0.069pF	0.034pF	0.034pF	0.034pF
Perf	0.145pF	0.149pF	0.224pF	0.224pF	0.294pF	0.145pF	0.145pF	0.145pF

Truth Table

INPUTS							OUTPUTS OLD		OUTPUTS NEW	
D0	D1	MCK	SCK	SD	PD	CD	Q	QN	Q	QN
X	X	X	X	X	X	1	X	X	0	1
X	X	X	X	X	1	0	X	X	1	0
0	X	↓	↑	0	0	X	X	X	0	1
1	X	↓	↑	0	X	0	X	X	1	0
X	0	↓	↑	1	0	X	X	X	0	1
X	1	↓	↑	1	X	0	X	X	1	0

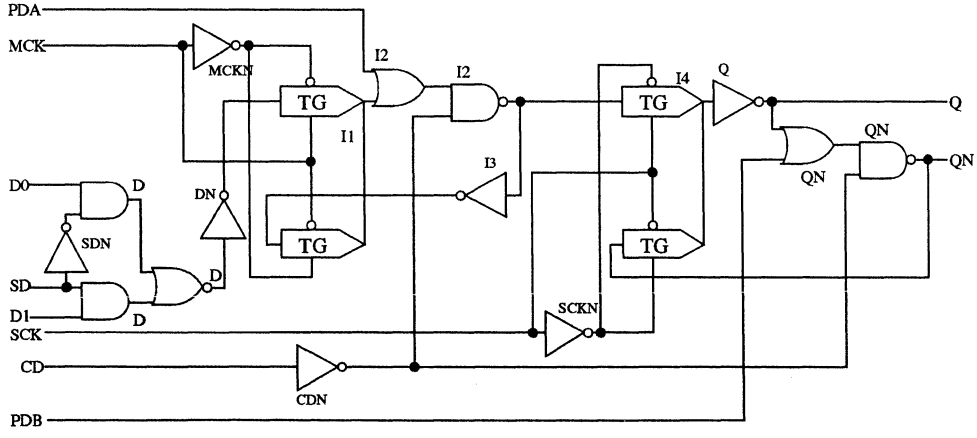
X = Don't care

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
D0 ↓	2.53ns	1.57ns	CD ↑	Q ↓	9.05ns/pF	2.47ns	1.64ns/pF	1.42ns
D0 ↑	2.43ns	1.53ns	CD ↑	QN ↑	3.88ns/pF	1.27ns	0.78ns/pF	0.53ns
D1 ↓	2.53ns	1.57ns	PD ↑	Q ↑	8.07ns/pF	1.87ns	1.49ns/pF	1.12ns
D1 ↑	2.43ns	1.53ns	PD ↑	QN ↓	4.46ns/pF	1.29ns	0.83ns/pF	0.68ns
SD ↓	2.53ns	1.57ns	SCK ↑	Q ↓	1.92ns/pF	1.65ns	0.44ns/pF	0.99ns
SD ↑	3.10ns	1.86ns	SCK ↑	Q ↑	3.57ns/pF	1.56ns	0.65ns/pF	0.87ns
			SCK ↑	QN ↓	10.57ns/pF	1.96ns	2.06ns/pF	1.09ns
			SCK ↑	QN ↑	9.18ns/pF	2.17ns	1.82ns/pF	1.23ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1D

Master-Slave clocking, data select front end, positive asynchronous clear.

Grids 23, **Transistors** 34

Inputs
D0,D1,MCK,SCK,SD,CD

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	MCK	SCK	SD	CD	Q	QN	Q	QN
X	X	X	X	X	1	X	X	0	1
0	X	↓	↑	0	X	X	X	0	1
1	X	↓	↑	0	0	X	X	1	0
X	0	↓	↑	1	X	X	X	0	1
X	1	↓	↑	1	0	X	X	1	0

X = Don't care

Capacitances

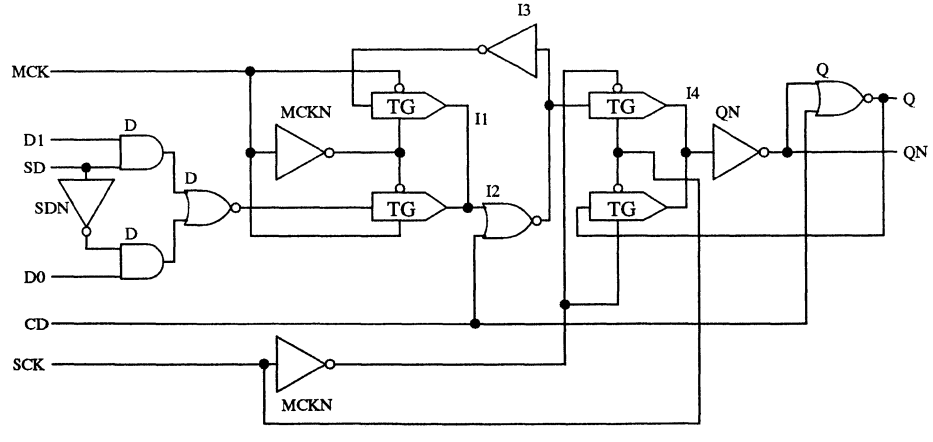
	D0	D1	MCK	SCK	SD	CD
Area	0.034pF	0.036pF	0.070pF	0.074pF	0.066pF	0.069pF
Perf	0.145pF	0.148pF	0.223pF	0.228pF	0.291pF	0.294pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	2.15ns	1.38ns	CD ↑	Q ↓	2.90ns/pF	1.20ns	0.57ns/pF	0.41ns
D0 ↑	2.48ns	1.38ns	CD ↑	QN ↑	6.60ns/pF	1.59ns	1.20ns/pF	0.87ns
D1 ↓	2.15ns	1.38ns	SCK ↑	Q ↓	8.92ns/pF	1.86ns	1.75ns/pF	0.91ns
D1 ↑	2.48ns	1.38ns	SCK ↑	Q ↑	9.14ns/pF	2.04ns	1.85ns/pF	1.11ns
SD ↓	2.43ns	1.53ns	SCK ↑	QN ↓	1.96ns/pF	1.67ns	0.47ns/pF	0.96ns
SD ↑	2.77ns	1.67ns	SCK ↑	QN ↑	3.57ns/pF	1.60ns	0.70ns/pF	0.78ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1E

Master-Slave clocking, data select front end, negative asynchronous clear.

Grids 23, **Transistors** 36

Inputs
D0,D1,MCK,SCK,SD,CDN

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	MCK	SCK	SD	CDN	Q	QN	Q	QN
X	X	X	X	X	0	X	X	0	1
0	X	↓	↑	0	X	X	X	0	1
1	X	↓	↑	0	1	X	X	1	0
X	0	↓	↑	1	X	X	X	0	1
X	1	↓	↑	1	1	X	X	1	0

X = Don't care

Capacitances

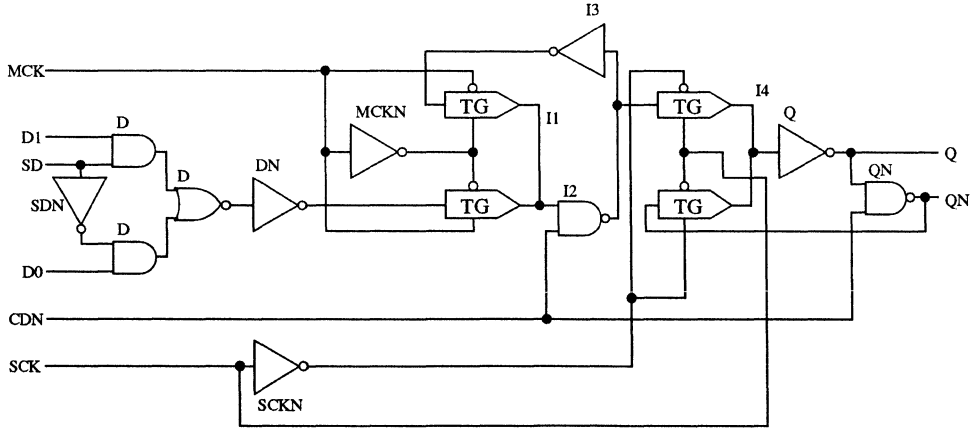
	D0	D1	MCK	SCK	SD	CDN
Area	0.034pF	0.036pF	0.070pF	0.074pF	0.066pF	0.069pF
Perf	0.145pF	0.148pF	0.223pF	0.228pF	0.291pF	0.294pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	2.05ns	1.34ns	CDN ↓	Q ↓	7.09ns/pF	1.46ns	1.43ns/pF	0.78ns
D0 ↑	2.34ns	1.57ns	CDN ↓	QN ↑	3.66ns/pF	0.66ns	0.78ns/pF	0.10ns
D1 ↓	2.05ns	1.34ns	SCK ↑	Q ↓	1.96ns/pF	1.67ns	0.47ns/pF	0.96ns
D1 ↑	2.34ns	1.57ns	SCK ↑	Q ↑	3.57ns/pF	1.56ns	0.63ns/pF	0.89ns
SD ↓	2.24ns	1.67ns	SCK ↑	QN ↓	10.34ns/pF	1.83ns	1.98ns/pF	1.06ns
SD ↑	2.72ns	1.62ns	SCK ↑	QN ↑	6.55ns/pF	1.90ns	1.38ns/pF	1.06ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1FX

Master-Slave clocking, data select front end, negative asynchronous clear, positive asynchronous preset.

Grids 25, **Transistors** 40

Inputs
D0,D1,MCK,SCK,SD,PDA,PDB,CDN

Outputs
Q,QN

Capacitances

	D0	D1	MCK	SCK	SD	PDA	PDB	CDN
Area	0.034pF	0.037pF	0.070pF	0.070pF	0.069pF	0.034pF	0.034pF	0.075pF
Perf	0.145pF	0.149pF	0.224pF	0.224pF	0.294pF	0.145pF	0.145pF	0.300pF

Truth Table

INPUTS							OUTPUTS OLD		OUTPUTS NEW	
D0	D1	MCK	SCK	SD	PD	CDN	Q	QN	Q	QN
X	X	X	X	X	X	0	X	X	0	1
X	X	X	X	X	1	1	X	X	1	0
0	X	↓	↑	0	0	X	X	X	0	1
1	X	↓	↑	0	X	1	X	X	1	0
X	0	↓	↑	1	0	X	X	X	0	1
X	1	↓	↑	1	X	1	X	X	1	0

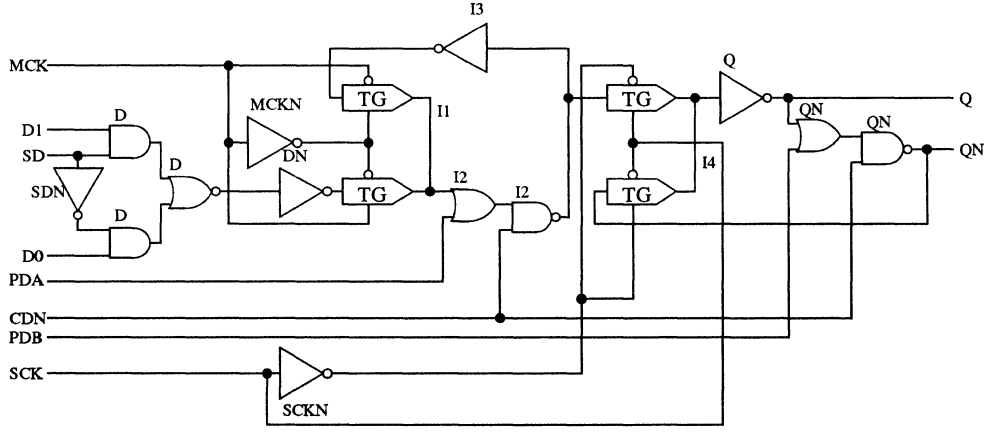
X = Don't care

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	2.53ns	1.57ns	CDN ↓	Q ↓	8.87ns/pF	1.79ns	1.56ns/pF	1.10ns
D0 ↑	2.43ns	1.53ns	CDN ↓	QN ↑	3.66ns/pF	0.61ns	0.70ns/pF	0.21ns
D1 ↓	2.53ns	1.57ns	PD ↑	Q ↑	8.11ns/pF	1.85ns	1.49ns/pF	1.12ns
D1 ↑	2.43ns	1.53ns	PD ↑	QN ↓	4.50ns/pF	1.27ns	0.83ns/pF	0.68ns
SD ↓	2.53ns	1.57ns	SCK ↑	Q ↓	1.92ns/pF	1.65ns	0.44ns/pF	0.99ns
SD ↑	3.10ns	1.86ns	SCK ↑	Q ↑	3.57ns/pF	1.56ns	0.65ns/pF	0.87ns
			SCK ↑	QN ↓	10.61ns/pF	1.94ns	2.06ns/pF	1.09ns
			SCK ↑	QN ↑	9.23ns/pF	2.15ns	1.82ns/pF	1.23ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1G

Master-Slave clocking, data select front end, negative asynchronous preset.

Grids 23, **Transistors** 34

Inputs
D0,D1,MCK,SCK,SD,PDN

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS OLD		OUTPUTS NEW	
D0	D1	MCK	SCK	SD	PDN	Q	QN	Q	QN
X	X	X	X	X	0	X	X	1	0
0	X	↓	↑	0	1	X	X	0	1
1	X	↓	↑	0	X	X	X	1	0
X	0	↓	↑	1	1	X	X	0	1
X	1	↓	↑	1	X	X	X	1	0

X = Don't care

Capacitances

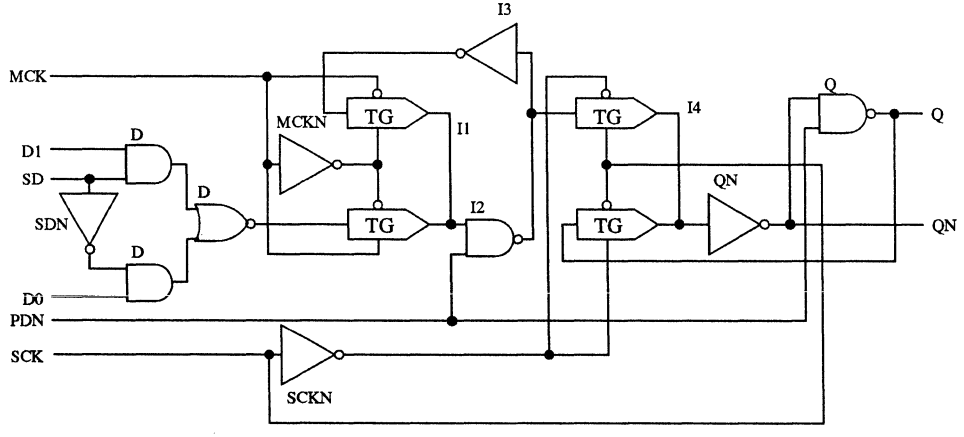
	D0	D1	MCK	SCK	SD	PDN
Area	0.034pF	0.036pF	0.070pF	0.074pF	0.066pF	0.069pF
Perf	0.145pF	0.148pF	0.223pF	0.228pF	0.291pF	0.294pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	2.29ns	1.48ns	PDN ↓	Q ↑	3.66ns/pF	0.66ns	0.78ns/pF	0.10ns
D0 ↑	2.10ns	1.19ns	PDN ↓	QN ↓	7.09ns/pF	1.46ns	1.43ns/pF	0.78ns
D1 ↓	2.29ns	1.48ns	SCK ↑	Q ↓	10.34ns/pF	1.83ns	1.98ns/pF	1.06ns
D1 ↑	2.10ns	1.19ns	SCK ↑	Q ↑	6.55ns/pF	1.90ns	1.38ns/pF	1.06ns
SD ↓	2.29ns	1.48ns	SCK ↑	QN ↓	1.96ns/pF	1.67ns	0.47ns/pF	0.96ns
SD ↑	2.91ns	1.76ns	SCK ↑	QN ↑	3.57ns/pF	1.56ns	0.63ns/pF	0.89ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1I

Master-Slave clocking, data select front end, positive synchronous clear.

Grids 23, **Transistors** 34

Inputs
D0,D1,MCK,SCK,SD,CD

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	MCK	SCK	SD	CD	Q	QN	Q	QN
X	X	↓	↑	1	1	X	X	0	1
0	X	↓	↑	0	X	X	X	0	1
1	X	↓	↑	0	X	X	X	1	0
X	0	↓	↑	1	X	X	X	0	1
X	1	↓	↑	1	0	X	X	1	0

X = Don't care **Note: CD does not function while SD=0**

Capacitances

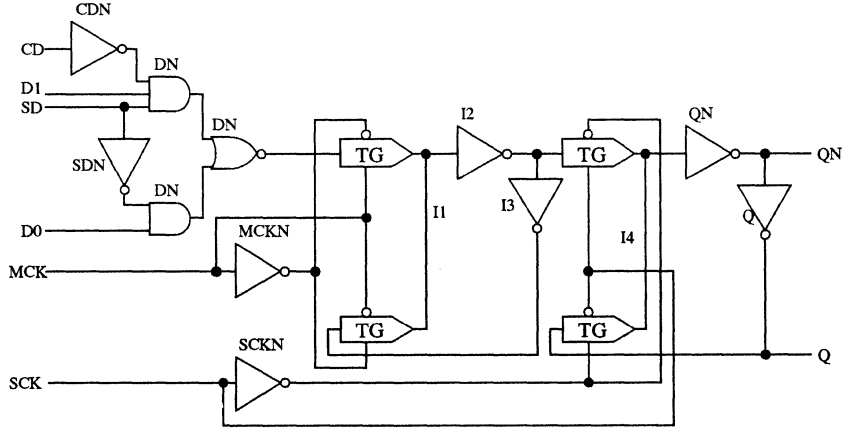
	D0	D1	MCK	SCK	SD	CD
Area	0.034pF	0.034pF	0.070pF	0.070pF	0.071pF	0.034pF
Perf	0.145pF	0.145pF	0.224pF	0.228pF	0.295pF	0.145pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
CD ↓	2.10ns	1.38ns	SCK ↑	Q ↓	8.87ns/pF	1.74ns	1.69ns/pF	0.95ns
CD ↑	2.86ns	1.62ns	SCK ↑	Q ↑	6.51ns/pF	1.87ns	1.33ns/pF	1.10ns
D0 ↓	2.29ns	1.34ns	SCK ↑	QN ↓	1.92ns/pF	1.69ns	0.44ns/pF	0.99ns
D0 ↑	2.10ns	1.19ns	SCK ↑	QN ↑	3.61ns/pF	1.44ns	0.68ns/pF	0.80ns
D1 ↓	2.29ns	1.34ns						
D1 ↑	2.19ns	1.29ns						
SD ↓	2.29ns	1.34ns						
SD ↑	2.81ns	1.62ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1J

Master-Slave clocking, data select front end, positive synchronous preset.

Grids 21, **Transistors** 32

Inputs
D0,D1,MCK,SCK,SD,PD

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	MCK	SCK	SD	PD	Q	QN	Q	QN
X	X	↓	↑	1	1	X	X	1	0
0	X	↓	↑	0	X	X	X	0	1
1	X	↓	↑	0	X	X	X	1	0
X	0	↓	↑	1	0	X	X	0	1
X	1	↓	↑	1	X	X	X	1	0

X = Don't care **Note: PD does not function while SD=0**

Capacitances

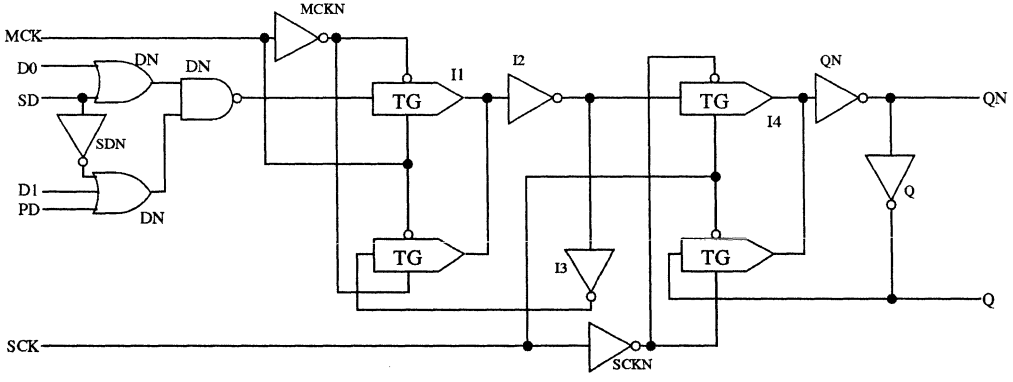
	D0	D1	MCK	SCK	SD	PD
Area	0.034pF	0.034pF	0.070pF	0.070pF	0.068pF	0.034pF
Perf	0.145pF	0.145pF	0.224pF	0.228pF	0.293pF	0.145pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	2.77ns	1.57ns	SCK ↑	Q ↓	8.87ns/pF	1.74ns	1.69ns/pF	0.95ns
D0 ↑	1.96ns	1.10ns	SCK ↑	Q ↑	6.51ns/pF	1.87ns	1.33ns/pF	1.10ns
D1 ↓	2.96ns	1.67ns	SCK ↑	QN ↓	1.92ns/pF	1.69ns	0.44ns/pF	0.99ns
D1 ↑	2.05ns	1.19ns	SCK ↑	QN ↑	3.61ns/pF	1.44ns	0.68ns/pF	0.80ns
PD ↓	2.96ns	1.67ns						
PD ↑	2.05ns	1.19ns						
SD ↓	2.77ns	1.57ns						
SD ↑	3.53ns	1.96ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1KX

Master-Slave clocking, data select front end, negative asynchronous clear, negative asynchronous preset.

Grids 26, **Transistors** 40

Inputs
D0,D1,MCK,SCK,SD,PDNA,PDNB,CDN

Outputs
Q,QN

Capacitances

Truth Table

INPUTS							OUTPUTS OLD		OUTPUTS NEW	
D0	D1	MCK	SCK	SD	PDN	CDN	Q	QN	Q	QN
X	X	X	X	X	X	0	X	X	0	1
X	X	X	X	X	0	1	X	X	1	0
0	X	↓	↑	0	1	X	X	X	0	1
1	X	↓	↑	0	X	1	X	X	1	0
X	0	↓	↑	1	1	X	X	X	0	1
X	1	↓	↑	1	X	1	X	X	1	0

X = Don't care

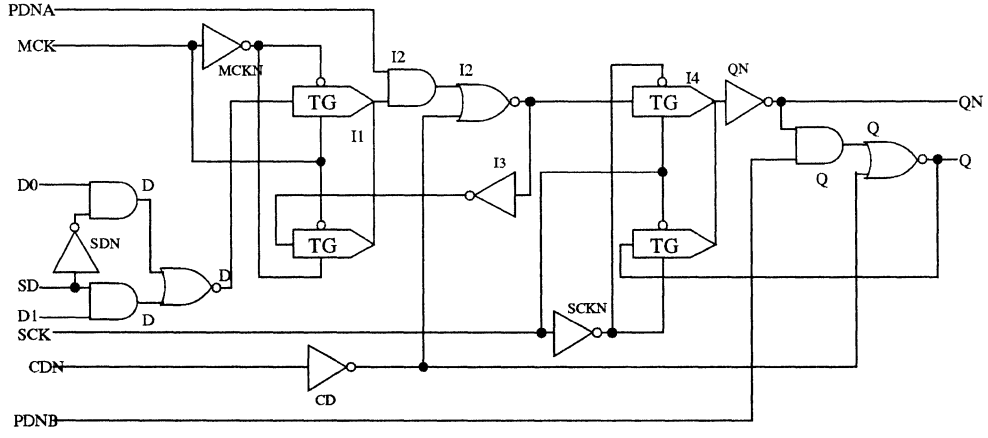
	D0	D1	MCK	SCK	SD	PDNA	PDNB	CDN
Area	0.034pF	0.037pF	0.070pF	0.070pF	0.069pF	0.034pF	0.034pF	0.034pF
Perf	0.145pF	0.149pF	0.224pF	0.224pF	0.294pF	0.145pF	0.145pF	0.145pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	2.24ns	1.34ns	CDN ↓	Q ↓	1.83ns/pF	1.45ns	0.16ns/pF	1.50ns
D0 ↑	2.43ns	1.38ns	CDN ↓	QN ↑	5.44ns/pF	2.03ns	0.81ns/pF	1.94ns
D1 ↓	2.24ns	1.34ns	PDN ↓	Q ↑	6.55ns/pF	0.85ns	1.23ns/pF	0.37ns
D1 ↑	2.43ns	1.38ns	PDN ↓	QN ↓	11.95ns/pF	2.09ns	2.14ns/pF	1.27ns
SD ↓	2.34ns	1.48ns	SCK ↑	Q ↓	10.43ns/pF	2.02ns	2.06ns/pF	1.04ns
SD ↑	2.81ns	1.62ns	SCK ↑	Q ↑	9.23ns/pF	2.15ns	1.82ns/pF	1.23ns
			SCK ↑	QN ↓	1.92ns/pF	1.65ns	0.44ns/pF	0.99ns
			SCK ↑	QN ↑	3.52ns/pF	1.62ns	0.70ns/pF	0.78ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1L

Master-Slave clocking, data select front end, negative synchronous preset.

Grids 23, **Transistors** 34

Inputs
D0,D1,MCK,SCK,SD,PDN

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	MCK	SCK	SD	PDN	Q	QN	Q	QN
X	X	↓	↑	1	0	X	X	1	0
0	X	↓	↑	0	X	X	X	0	1
1	X	↓	↑	0	X	X	X	1	0
X	0	↓	↑	1	1	X	X	0	1
X	1	↓	↑	1	X	X	X	1	0

X = Don't care **Note: PDN does not function while SD=0**

Capacitances

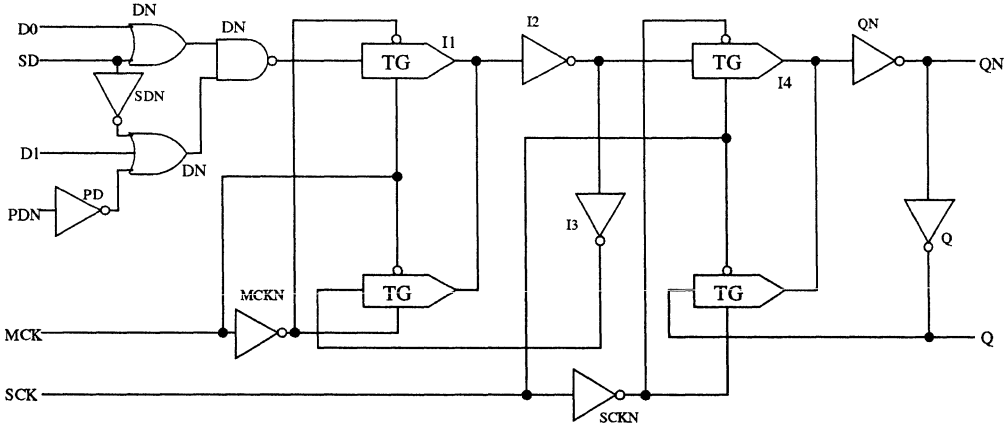
	D0	D1	MCK	SCK	SD	PDN
Area	0.034pF	0.034pF	0.070pF	0.070pF	0.068pF	0.034pF
Perf	0.145pF	0.145pF	0.224pF	0.228pF	0.293pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	2.81ns	1.62ns	SCK ↑	Q ↓	8.87ns/pF	1.74ns	1.69ns/pF	0.95ns
D0 ↑	2.00ns	1.14ns	SCK ↑	Q ↑	6.51ns/pF	1.87ns	1.33ns/pF	1.10ns
D1 ↓	3.01ns	1.72ns	SCK ↑	QN ↓	1.92ns/pF	1.69ns	0.44ns/pF	0.99ns
D1 ↑	2.10ns	1.24ns	SCK ↑	QN ↑	3.61ns/pF	1.44ns	0.68ns/pF	0.80ns
PDN ↓	1.91ns	1.38ns						
PDN ↑	3.63ns	2.00ns						
SD ↓	2.81ns	1.62ns						
SD ↑	3.63ns	2.00ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1M

Master-Slave clocking, data select front end, negative synchronous clear.

Grids 21, **Transistors** 32

Inputs
D0,D1,MCK,SCK,SD,CDN

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	MCK	SCK	SD	CDN	Q	QN	Q	QN
X	X	↓	↑	1	0	X	X	0	1
0	X	↓	↑	0	X	X	X	0	1
1	X	↓	↑	0	X	X	X	1	0
X	0	↓	↑	1	X	X	X	0	1
X	1	↓	↑	1	1	X	X	1	0

X = Don't care **Note: CDN does not function while SD=0**

Capacitances

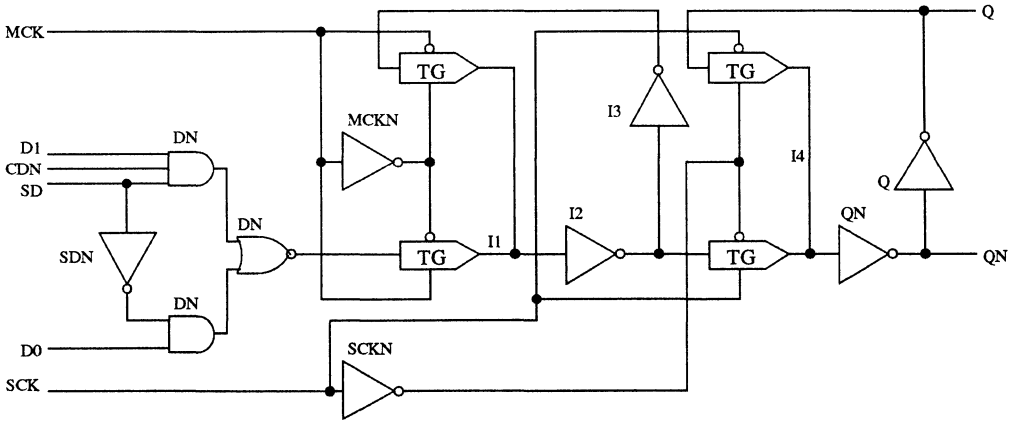
	D0	D1	MCK	SCK	SD	CDN
Area	0.034pF	0.034pF	0.070pF	0.070pF	0.071pF	0.034pF
Perf	0.145pF	0.145pF	0.224pF	0.228pF	0.295pF	0.145pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	2.15ns	1.34ns	SCK ↑	Q ↓	8.87ns/pF	1.74ns	1.69ns/pF	0.95ns
CDN ↑	2.24ns	1.29ns	SCK ↑	Q ↑	6.51ns/pF	1.87ns	1.33ns/pF	1.10ns
D0 ↓	2.15ns	1.34ns	SCK ↑	QN ↓	1.92ns/pF	1.69ns	0.44ns/pF	0.99ns
D0 ↑	2.15ns	1.19ns	SCK ↑	QN ↑	3.61ns/pF	1.44ns	0.68ns/pF	0.80ns
D1 ↓	2.15ns	1.34ns						
D1 ↑	2.24ns	1.29ns						
SD ↓	2.15ns	1.34ns						
SD ↑	2.72ns	1.62ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1NX

Master-Slave clocking, data select front end, positive asynchronous clear, negative asynchronous preset.

Grids 25, **Transistors** 38

Inputs
D0,D1,MCK,SCK,SD,PDNA,PDNB,CD

Outputs
Q,QN

Truth Table

INPUTS							OUTPUTS			
							OLD		NEW	
D0	D1	MCK	SCK	SD	PDN	CD	Q	QN	Q	Q
X	X	X	X	X	X	1	X	X	0	1
X	X	X	X	X	0	0	X	X	1	0
0	X	↓	↑	0	1	X	X	X	0	1
1	X	↓	↑	0	X	0	X	X	1	0
X	0	↓	↑	1	1	X	X	X	0	1
X	1	↓	↑	1	X	0	X	X	1	0

X = Don't care

Capacitances

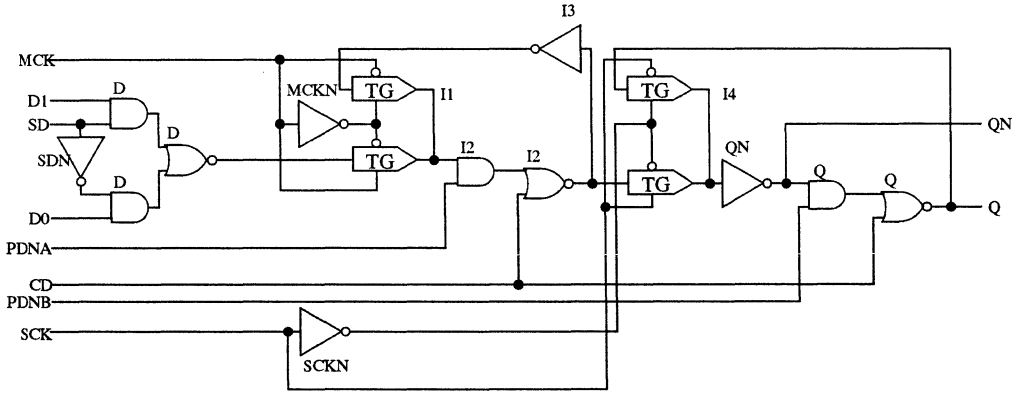
	D0	D1	MCK	SCK	SD	PDNA	PDNB	CD
Area	0.034pF	0.037pF	0.070pF	0.070pF	0.069pF	0.034pF	0.034pF	0.075pF
Perf	0.145pF	0.149pF	0.224pF	0.224pF	0.294pF	0.145pF	0.145pF	0.300pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	2.24ns	1.34ns	CD ↑	Q ↓	2.32ns/pF	1.56ns	1.15ns/pF	0.33ns
D0 ↑	2.43ns	1.38ns	CD ↑	QN ↑	5.93ns/pF	2.14ns	1.80ns/pF	0.77ns
D1 ↓	2.24ns	1.34ns	PDN ↓	Q ↑	6.60ns/pF	0.83ns	1.23ns/pF	0.37ns
D1 ↑	2.43ns	1.38ns	PDN ↓	QN ↓	12.04ns/pF	2.00ns	2.14ns/pF	1.27ns
SD ↓	2.34ns	1.48ns	SCK ↑	Q ↓	10.43ns/pF	2.02ns	2.09ns/pF	1.02ns
SD ↑	2.81ns	1.62ns	SCK ↑	Q ↑	9.27ns/pF	2.13ns	1.82ns/pF	1.23ns
			SCK ↑	QN ↓	1.92ns/pF	1.65ns	0.44ns/pF	0.99ns
			SCK ↑	QN ↑	3.52ns/pF	1.62ns	0.70ns/pF	0.78ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static R-S Flip-Flop

FS0S1A

Positive level S input, positive level R input.

Grids 5, **Transistors** 8

Inputs
S,R

Outputs
Q,QN

Truth Table

INPUTS		OUTPUTS			
		OLD		NEW	
S	R	Q	QN	Q	QN
0	X	0	1	0	1
X	0	1	0	1	0
0	1	X	X	0	1
1	0	X	X	1	0
1	1	X	X	0	0

X = Don't care

Capacitances

	S	R
Area	0.034pF	0.034pF
Perf	0.145pF	0.145pF

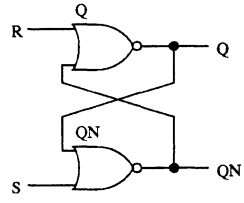
7

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
R ↑	Q ↓	2.63ns/pF	1.37ns	0.47ns/pF	0.58ns
R ↑	QN ↑	9.67ns/pF	1.80ns	1.80ns/pF	0.87ns
S ↑	Q ↑	9.67ns/pF	1.80ns	1.80ns/pF	0.87ns
S ↑	QN ↓	2.63ns/pF	1.37ns	0.47ns/pF	0.58ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static R-S Flip-Flop

FS0S1D

Positive level S input, positive level R input, positive asynchronous clear.

Grids 6, **Transistors** 10

Inputs
S,R,CD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
S	R	CD	Q	QN	Q	QN
0	X	X	0	1	0	1
X	0	0	1	0	1	0
0	X	1	X	X	0	1
0	1	X	X	X	0	1
1	0	0	X	X	1	0
1	X	1	X	X	0	0
1	1	X	X	X	0	0

X = Don't care

Capacitances

	S	R	CD
Area	0.034pF	0.034pF	0.034pF
Perf	0.145pF	0.145pF	0.145pF

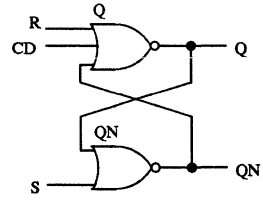
7

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CD ↑	Q ↓	2.54ns/pF	1.45ns	0.50ns/pF	0.56ns
CD ↑	QN ↑	9.50ns/pF	1.93ns	1.80ns/pF	0.87ns
R ↑	Q ↓	2.54ns/pF	1.45ns	0.50ns/pF	0.56ns
R ↑	QN ↑	9.50ns/pF	1.93ns	1.80ns/pF	0.87ns
S ↑	Q ↑	11.72ns/pF	2.38ns	2.32ns/pF	0.98ns
S ↑	QN ↓	2.23ns/pF	1.65ns	0.55ns/pF	0.52ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static R-S Flip-Flop

FS0S7A

Positive level S input, negative level R input.

Grids 5, **Transistors** 8

Inputs
S,RN

Outputs
Q,QN

Truth Table

INPUTS		OUTPUTS			
		OLD		NEW	
S	RN	Q	QN	Q	QN
0	X	0	1	0	1
X	1	1	0	1	0
0	0	X	X	0	1
1	X	X	X	1	0

X = Don't care

Capacitances

	S	RN
Area	0.034pF	0.034pF
Perf	0.145pF	0.145pF

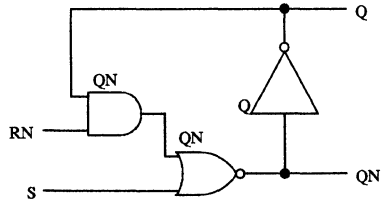
7

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
RN ↓	Q ↓	14.00ns/pF	1.29ns	2.61ns/pF	0.80ns
RN ↓	QN ↑	6.46ns/pF	0.89ns	1.23ns/pF	0.46ns
S ↑	Q ↑	7.40ns/pF	1.75ns	1.46ns/pF	0.75ns
S ↑	QN ↓	2.36ns/pF	1.49ns	0.47ns/pF	0.54ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static R-S Flip-Flop

FS1S1A

Positive level sense.

Grids 7, **Transistors** 12

Inputs
S,R,CK

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
S	R	CK	Q	QN	Q	QN
X	X	0	0	1	0	1
X	X	0	1	0	1	0
0	0	X	0	1	0	1
0	0	X	1	0	1	0
0	1	1	X	X	0	1
1	0	1	X	X	1	0

X = Don't care

Capacitances

	S	R	CK
Area	0.061pF	0.062pF	0.096pF
Perf	0.222pF	0.223pF	0.371pF

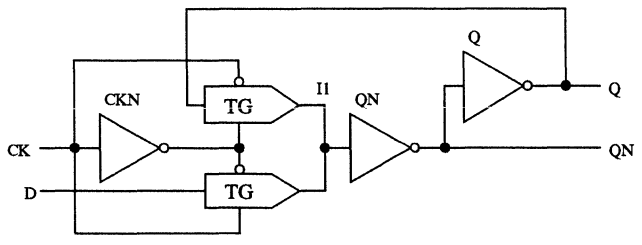
7

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CK ↑	Q ↓	4.15ns/pF	1.81ns	0.86ns/pF	0.66ns
CK ↑	Q ↑	11.32ns/pF	2.52ns	2.29ns/pF	1.00ns
CK ↑	QN ↓	4.15ns/pF	1.81ns	0.86ns/pF	0.66ns
CK ↑	QN ↑	11.32ns/pF	2.52ns	2.29ns/pF	1.00ns
R ↑	Q ↓	4.15ns/pF	1.81ns	0.86ns/pF	0.66ns
R ↑	QN ↑	11.32ns/pF	2.52ns	2.29ns/pF	1.00ns
S ↑	Q ↑	11.32ns/pF	2.52ns	2.29ns/pF	1.00ns
S ↑	QN ↓	4.15ns/pF	1.81ns	0.86ns/pF	0.66ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static R-S Flip-Flop

FS1S3A

Positive edge triggered.

Grids 15, **Transistors** 24

Inputs
SN,RN,CK

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
SN	RN	CK	Q	QN	Q	QN
1	1	↑	0	1	0	1
1	1	↑	1	0	1	0
1	0	↑	X	X	0	1
0	1	↑	X	X	1	0

X = Don't care

Capacitances

	SN	RN	CK
Area	0.035pF	0.034pF	0.139pF
Perf	0.146pF	0.145pF	0.590pF

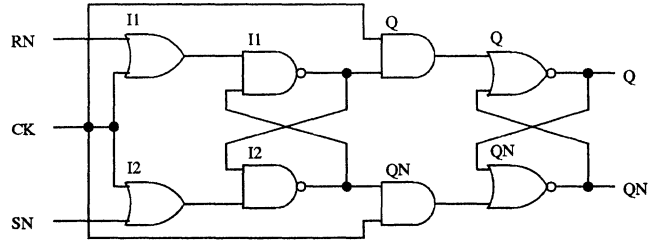
7

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
RN ↓	2.00ns	1.34ns	CK ↑	Q ↓	4.15ns/pF	1.77ns	0.86ns/pF	0.66ns
SN ↓	2.00ns	1.29ns	CK ↑	Q ↑	11.32ns/pF	2.42ns	2.29ns/pF	1.00ns
			CK ↑	QN ↓	4.15ns/pF	1.77ns	0.86ns/pF	0.66ns
			CK ↑	QN ↑	11.32ns/pF	2.42ns	2.29ns/pF	1.00ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Parameterized Macrocells

Section 8

AT&T

Contents - Section 8

Parameterized Macrocells Introduction

This section describes the selection of parameterized macrocells available in the 1.25µ CMOS Standard Cell Library. These are functions that are customized into complete, functional building blocks to satisfy the requirements of the circuit at hand. Depending on the function, the final building block will be implemented as a densely-packed, pitch-matched array either stand alone or in conjunction with a standard cell circuit layout. Using a complex function block layout generator, many functions can be realized in a much more efficient manner than is possible with a standard cell approach. Some examples of such functions are:

- FIFO
- Register File
- SRAM
- ROM
- PLA
- Shift Register
- Multiplier

Accessing Macrocells Through *MACLOG*

These complex functions can be customized through *MACLOG*. *MACLOG* is a menu driven program that allows you to configure a macrocell through specific variables. *MACLOG* provides general information about any of the macrocells and specific information about the characteristics and timing of your particular configuration. This will allow you to select and customize any of these macrocells to meet the specific circuit requirements.

When the variables have been fully specified, you may automatically synthesize any or all of the following items:

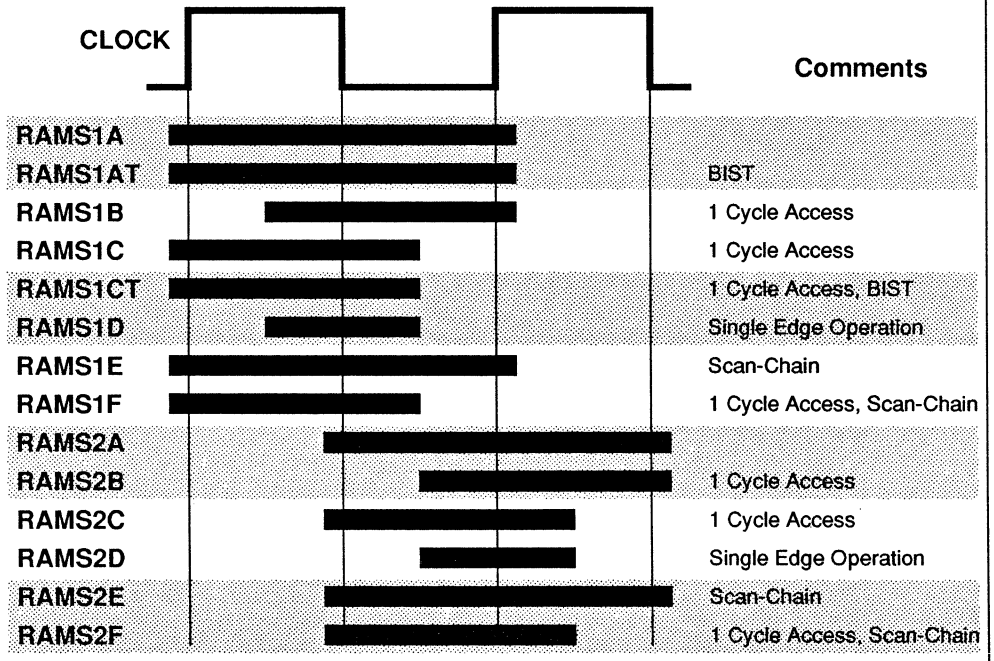
1) A customized symbol for the macrocell, suitable for placement into the overall schematic diagram.
2) A customized circuit model that will accurately simulate the behavior of the macrocell.
3) A customized fault simulation model.
4) A customized model for circuit hazard analysis.
5) A symbolic description of the block, suitable for use in circuit layout for automatic placement and routing.
6) The mask artwork for the macrocell, to be included in the final chip layout.

For more detailed information regarding the generation and use of these cells, contact your AT&T representative.

MACROCELL SELECTION GUIDE

NAME	DESCRIPTION
FIFO	First-in-First-out Memory
MULTP	Multiplier
PLAC2B	Programmable Logic Array
RAMs	Random Access Memories - See Below
REGFILE	Register file, Sync. write, Async read port
ROMS1A	Positive Edge-Triggered Read Only Memory
ROMS2A	Negative Edge-Triggered Read Only Memory
SRGEN	Dynamic Shift Register

RAM SELECTION GUIDE



The left end of the dark bar represents the relative time in a clock cycle where inputs must be valid. The right end represents output being valid. This is not intended to represent actual delay. Delay Information may be found in the individual data sheets.

CHARACTERISTICS AND TIMING

The macrocells in this section have been characterized using worst case slow processing model files and 4.5 volts supply(VDD) at 125° C. The values as reported in the tables in this section, including coefficients to equations, have been converted to nominal processing and 5.0 volts supply at 25° C using the derating factors provided in section 2. Using these derating factors will yield accurate results when converting to any of the worst case conditions previously mentioned.

The switching characteristics for the macrocells reported in the tables were measured from 40% of the high input voltage to 40% of the high output voltage with a 1 nanosecond rise or fall time slope on the input signal as indicated in Figure 1. The timing requirements reported in the tables were also taken from 40% voltage levels with 1 nanosecond rise and fall times for input signals as indicated in Figure 2

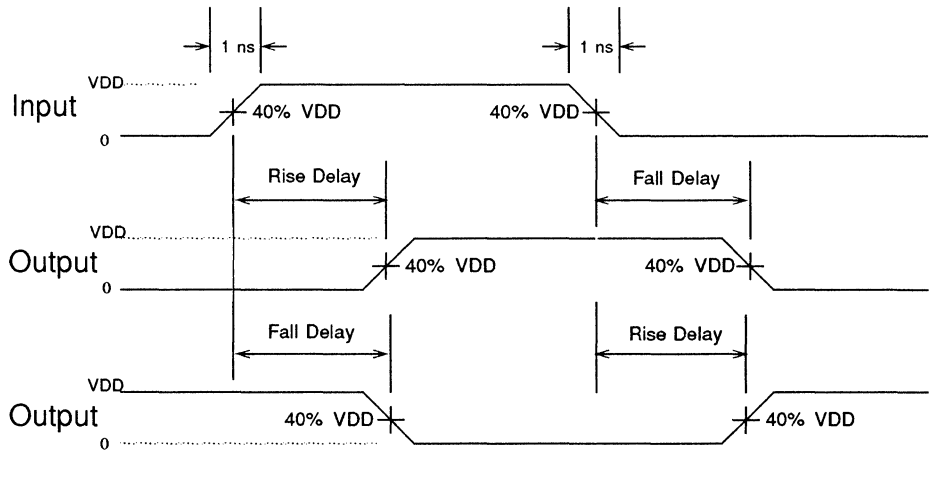


Figure1. Switching Characteristics

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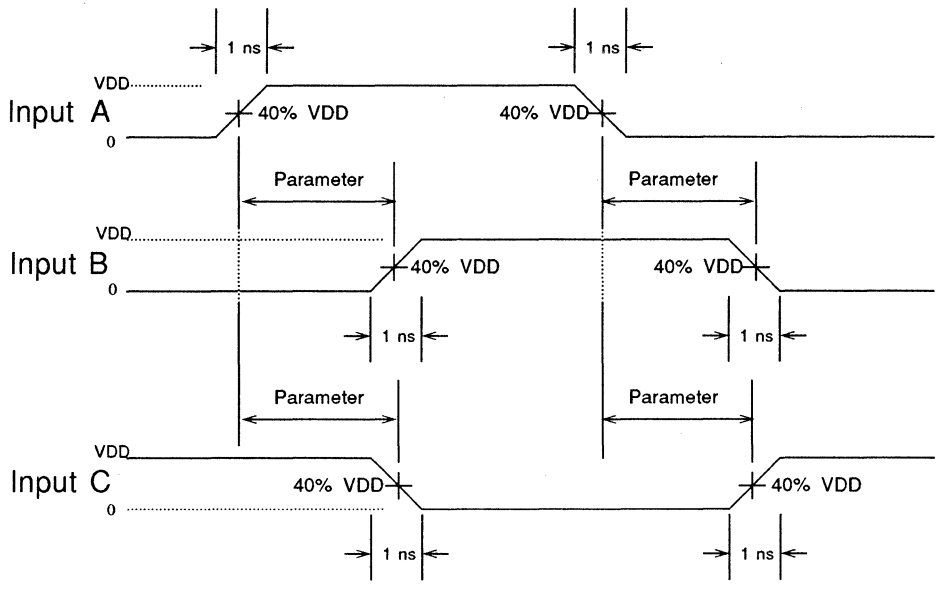


Figure 2. Timing Requirements

8

Parameterized Macrocell Data Sheets

8

FUNCTIONAL DESCRIPTION AND FEATURES

FIFO is a parameterized First-in First-out memory function supported by automatic layout generation software. The synthesis of the FIFO is accomplished in two sections. The FIFO memory array is implemented as a custom, pitch-matched array of cells that is very area-efficient. The FIFO control and status logic is implemented as a standard cell layout using performance optimized cells.

FIFO has been designed specifically for use on standard cell chips and has the following features:

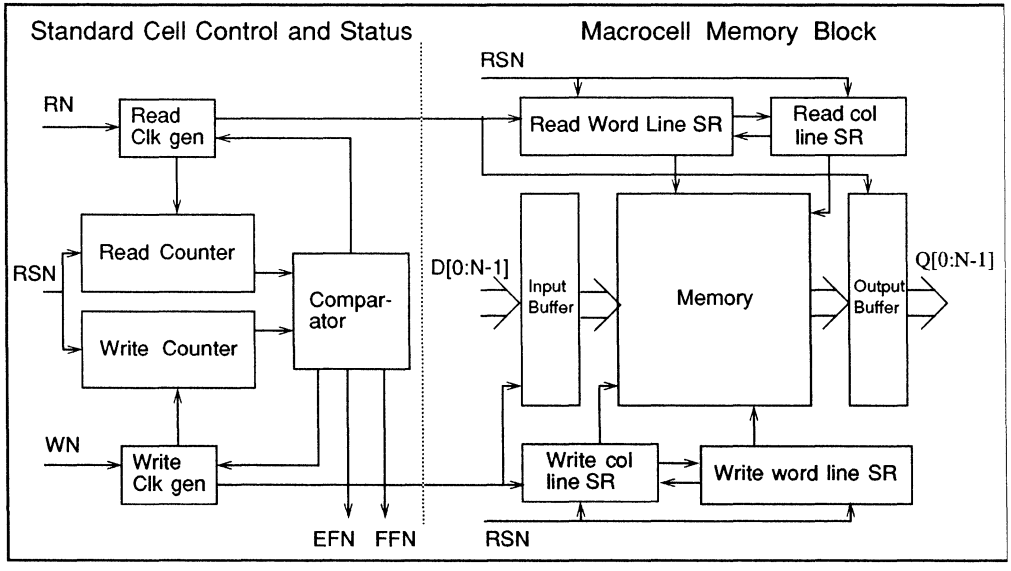
- First-in first-out buffer memory.
- Independent asynchronous inputs and outputs.
- 3-State Outputs.
- Organized as W words of N bits.
- Dual port RAM architecture.
- Empty and Full Status Flags.

The FIFO can be customized with the following parameters:

Parameter	Description	Limit		
		Increment	Min	Max
N	Bits/Word	1	1	21
W	Words	8	16	512

8

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: RN, WN, D[0:N-1], RSN;

OUTPUTS: FFN, Q[0:N-1], EFN;

Functional Descriptions

Inputs

RN	Read FIFO Not, Initiates a Read
WN	Write FIFO Not, Initiates a Write
D[0:N-1]	Data Inputs
RSN	Reset FIFO Not

Outputs

FN	FIFO Full Flag Not
Q[0:N-1]	Data Outputs
EFN	FIFO Empty Flag Not

CHARACTERISTICS

The parameters N and W can be used to estimate the characteristics for a FIFO that is W words X N bits per word.

Parameter	Value	Unit
Number of Transistors:		
Macrocell Memory Block	20.25W +99N + 420	
Polycell Control Section	$131\sqrt{W}$ - 2.6W + 1210	
Height of Memory Block	5.0625W + 440	µ
Width of Memory Block	141.6N + 475	µ
Polycell Grids - Control and Status*	$88.75\sqrt{W}$ - 1.8W + 837	
Power		
Write Cycle	$(1100N+3.6NW+24W+5900/W+3100)10^{-6}$ VDD^2 f_w**	mW
Read Cycle	$(1200N+5.5NW+24W+5900/W+3100)10^{-6}$ VDD^2 f_r**	mW
Input Capacitance:		
D[0:N-1]	0.054	pF
RN	0.500	pF
WN	0.500	pF
RSN	0.120	pF
Output Capacitance:		
Q[0:N-1]	0.054	pF
FFN	0.090	pF
EFN	0.090	pF

* The total area required for the control and status section of the FIFO depends on the efficiency of the particular layout. The size of this area can be estimated from the grid count.

** VDD =the power supply voltage, f_r =the read clock frequency in MHz, and f_w =the write clock frequency in MHz.

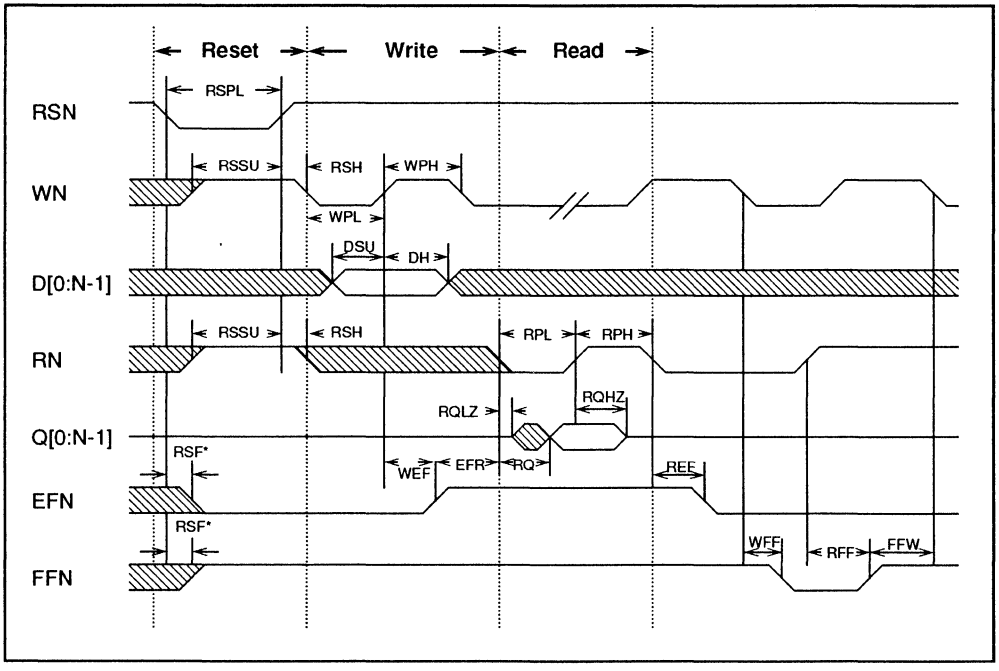
SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, NOM Processing				
Symbol	From INPUT	To OUTPUT	Intrinsic (ns)	Extrinsic (ns/pF)
RQLZ	RN↓	Q[0:N-1](Low Z)	2.1	0.3
RQ	RN↓	Q[0:N-1]	0.1N + 11.9	0.78
RQHZ	RN↑	Q[0:N-1](High Z)	2.7	0.37
WEF	WN↑	EFN↑	8.2	0.42
REF	RN↓	EFN↓	9.8	0.42
WFF	WN↓	FFN↓	10.0	0.42
RFF	RN↑	FFN↑	7.6	0.42
RSF*	RSN↓ RSN↓	FFN↑ EFN↓	9.4 9.4	0.42 0.42
RSF*	WN↑RN↑ WN↑RN↑	FFN↑ EFN↓	10.1 10.1	0.42 0.42

*** Use the greater value. This depends on which edge occurs last.**

8

Timing Requirements VDD=5.0V, T=25°C, NOM Processing			
Symbol	Description	Value	Unit
RSPL	Minimum Reset Pulse Low	0.004W + 6.3	
RSSU	Minimum RN and WN High before RSN ↑	RSPL + 0.02N + 1.1	
RSH	Minimum RN and WN High after RSN ↑	2.4	
WPL	Minimum Write Pulse Low	0.1N + 10.3	
WPH	Minimum Write Pulse High	0.01W + 11.1	
DSU	Minimum Data Setup before WN↑	1.0	ns
DH	Minimum Data Hold after WN↑	1.7	
RPL	Minimum Read Pulse Low	0.1N + 13.6	
RPH	Minimum Read Pulse High	0.01W + 10.4	
EFR	Minimum EFN↑ before RN↓	0.02W	
FFW	Minimum FFN↑ before WN↓	0.02W	

TIMING DIAGRAM



FUNCTIONAL OPERATION

Write Mode

A write cycle is initiated on the falling edge of the WN input, provided that the FFN status flag is not asserted, as shown in the timing diagram. The input data must meet the requirements of setup and hold time with respect to the rising edge of the WN pulse.

The FFN status flag will be asserted after the last valid write. Once the FFN flag is set, any further write cycles will be inhibited. The FFN flag can only be reset after the occurrence of at least one valid read cycle. The write operation can resume after a specified time from the reset of the FFN flag.

Read Mode

A read cycle is initiated on the falling edge of the RN input, provided that the EFN status flag is not asserted, as shown in the timing diagram. The output data will be available after a specified time from the falling edge of the RN pulse. When the read operation is inactive, the output will be tristated.

The EFN flag will be asserted after the last valid read. Once the EFN flag is set, any further read cycles will be inhibited. The EFN flag can only be reset after the occurrence of at least one valid write cycle. The read operation can resume after a specified time from the reset of the EFN flag.

Reset Mode

Reset initiates when RSN is low, but will execute properly only when both WN and RN are high for a specified time before and after RSN returns high, as illustrated in the timing diagram. The EFN and FFN flags will be reset

USER NOTES

1) The FIFO must be reset before any read or write function can be performed.
2) The READ signal and the WRITE signal each generate a pair of non-overlapping clock pulses to the memory array block. A feedback loop for each clock must be provided during layout to guarantee that the phases do not overlap.
3) Outputs remain tristate when the FIFO is empty (empty flag active), even if the READ input(RN) is activated. This applies as well to the period immediately after reset when the empty flag is active.
4) The FIFO was designed to use only performance optimized polycells for the control and status section.

FUNCTIONAL DESCRIPTION AND FEATURES

MULTP is a parameterized two's complement parallel multiplier function supported by automatic layout generation software. The layout of the MULTP is implemented as a custom, pitch-matched array of cells that is very area-efficient.

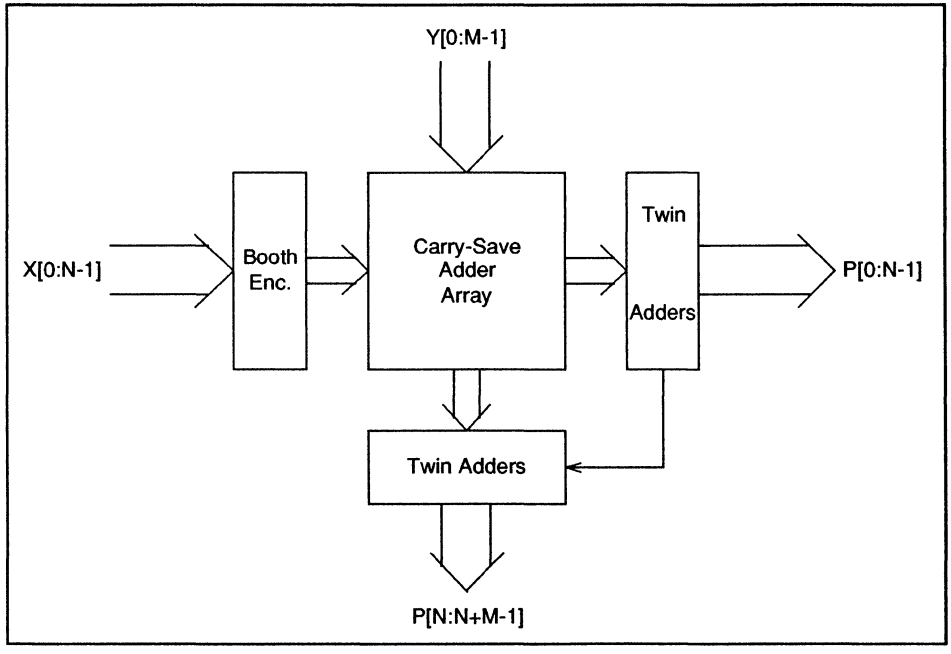
MULTP has been designed specifically for use on standard cell chips and has the following features:

- Asynchronous operation.
- Organized as N multiplier bits by M multiplicand bits.
- Two's complement data format.
- Three-bit Booth encoding of multiplier bits halves the number of shift-adds needed.
- Carry-save adder array generates partial products in parallel.
- Fast twin adders using two-bit look ahead technique are used for carry-propagate and final product generation.

The MULTP can be customized with the following parameters:

Parameter	Description	Limit		
		Increment	Min	Max
N	# Multiplier Bits	2	6	32
M	# Multiplicand Bits	2	2	32

BLOCK DIAGRAM



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TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: X[0:N-1],Y[0:M-1];

OUTPUTS: P[0:N+M-1];

Functional Descriptions

INPUTS

X[0:N-1]	Multiplier Bits (X0=LSB)
Y[0:M-1]	Multiplicand Bits (Y0=LSB)

OUTPUTS

P[0:N+M-1]	Product Bits (P0=LSB)

CHARACTERISTICS

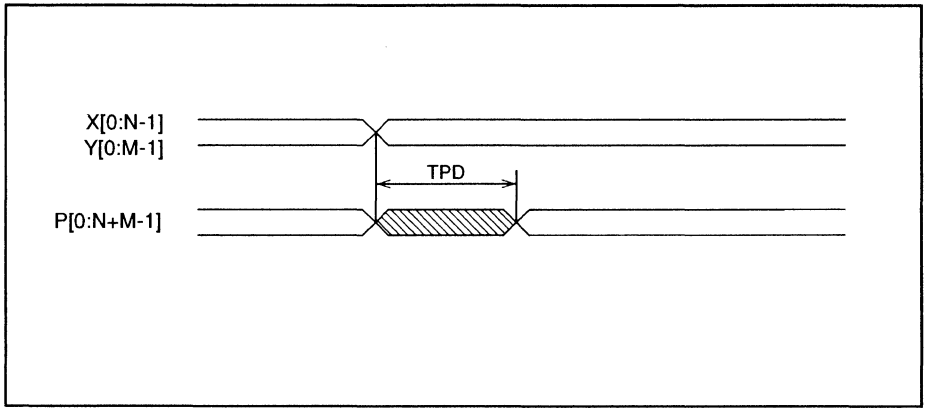
The parameters **N** and **M** can be used to estimate the characteristics for an **N** X **M** multiplier generated by MULTP

Parameter	Value	Unit
Number of Transistors	24.5NM + 104.5N + 7.5M - 28	
Height	91.2N + 224	μ
Width	81.25M + 494.6	μ
Worst Case Power	$VDD^2(1.4NM + 7.1N + 3.0M - 2.3)f^*$	μW
Input Capacitance:		
X[0:N-1]	1.331	pF
Y[0:M-1]	0.151	pF
Output Capacitance:		
P[0:N+M-1]	0.082	pF

* **VDD** =the power supply voltage, **f** =the frequency in MHz of change of X- and Y-bits.

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, NOM Processing				
Symbol	From INPUT	To OUTPUT	Intrinsic (ns)	Extrinsic (ns/pF)
TPD	X[0:N-1],Y[0:M-1]	P[0:N+M-1]	0.74N + 0.47M + 7.1	1.75

TIMING DIAGRAM



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USER NOTES

1) X_0, Y_0 and P_0 are the least-significant bits (LSB's) of the multiplier, the multiplicand and the product. X_{N-1}, Y_{M-1} and P_{N+M-1} are the MSB's (the sign-bits) of the corresponding numbers.
2) The MULTP design does not include embedded input or output registers which could restrict its usefulness as a general function block. The product outputs can be sampled after an interval of TPD is elapsed from the time inputs X and Y have stabilized.
3) When the two numbers being multiplied are not the same size, higher multiplication speed would be achieved if the wider number can be applied to the multiplicand (the Y inputs) and the narrower one to the multiplier (the X inputs). Circumstances permitting, the guideline to follow here for higher speed is:

$$N \leq M.$$

4) Since N and M can only accept even values, if odd-size numbers are to be multiplied a multiplier with even-size inputs should be generated and the sign-bit properly extended to the extra bit.

FUNCTIONAL DESCRIPTION AND FEATURES

PLAC2B is a parameterized clocked PLA function supported by automatic mask layout generation software. The layout of the PLAC2B is implemented as a custom, pitch-matched array of cells that is very area-efficient.

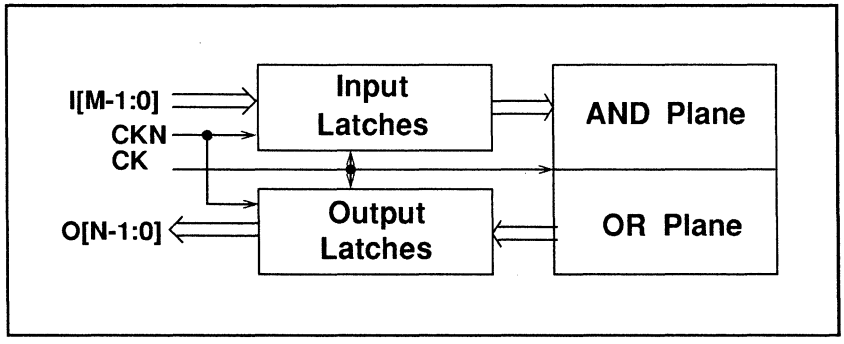
The PLAC2B has been designed specifically for use on standard cell chips, and has overhead circuitry already built-in including negative edge-triggered output latches and negative level-sense input latches. The PLAC2B can be used to implement sequential state machines.

The PLAC2B can be customized with the following parameters:

Parameter	Description	Limit		
		Increment	Min	Max
N	Data Inputs	1	1	N + M < 100
M	Data Outputs	1	1	N + M < 100
P	Product Terms	1	1	P < 200

8

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: I[N:1], CK, CKN;

OUTPUTS: O[M:1];

Functional Descriptions

INPUTS

I[N:1]	Data Inputs
CK	Clock
CKN	Inverted Clock

OUTPUTS

O[M:1]	Data Outputs

CHARACTERISTICS

The parameters **N**, **M**, and **P** can be used to estimate the characteristics for a particular version of the PLAC2B.

Parameter	Value	Unit
Number of Transistors:	N(13 + P) + M(15 + 2P) + 2P + 4 - 2(# desired output 0s' in truth table)	
Height	7.125P + 265	µ
Width	11.25N + 11.25M + 65	
Worst Case Power	$VDD^2f(0.032M)$*	mW/MHz
Input Capacitance:		
I[N:1]	0.025	pF
CK	0.086N + 0.053M + 0.015P + 0.167	
CKN	0.088N + 0.068M + 0.115	
Output Capacitance:		
O[M:1]	0.049	pF

* **VDD** = the power supply voltage, **f** = the clock frequency in MHz.

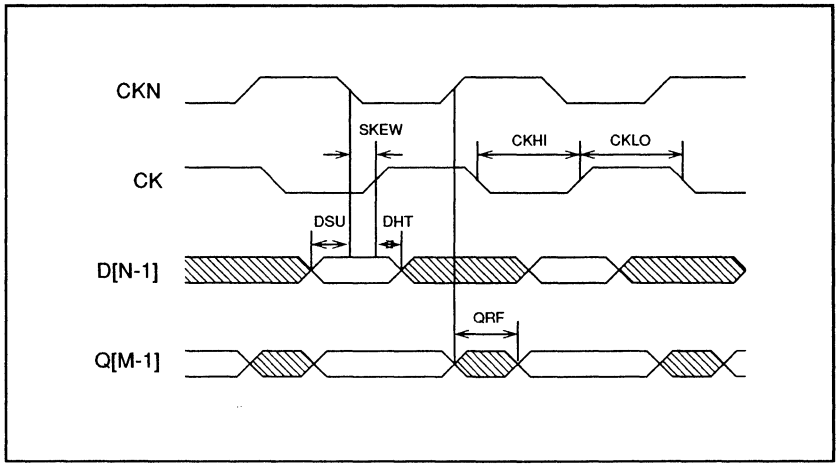
SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, NOM Processing				
Symbol	From INPUT	To OUTPUT	Intrinsic (ns)	Extrinsic (ns/pF)
QRF	CK↑	O[M:1] ↑	0.94+SKEW	0.81
	CK↑	O[M:1] ↓	0.94+SKEW	0.92

Timing Requirements VDD=5.0V, T=25°C, NOM Processing			
Symbol	Description	Value	Unit
CKHI	Minimum Clock High	0.055N - 0.163M + 0.03P + 0.061L + 5.2 + SKEW	ns
CKLO	Minimum Clock Low	2.6 + SKEW	
DSU	Minimum Data Set-Up Time	0.9	
DHT	Minimum Data Hold Time	0	
SKEW	Typical Clock Skew	0	

8

* L=max. # of product terms included in any single output.

TIMING DIAGRAM



USER NOTES

1) The transistor count, maximum power dissipation, and minimum clock high time are all truth table dependent. The corresponding formulas above are meant to determine upper boundaries.
2) CK should be generated from CKN and in such a way as to minimize skewing. Any skewing between the clocks will detract from the performance of the PLAC2B.
3) Because of the dynamic nature in which PLAC2B decodes the data inputs, CK should not be high and CKN should not be low for longer than 1μs.
4) The actual functional behavior of the PLAC2B must be specified by a truth table.

8

FUNCTIONAL DESCRIPTION AND FEATURES

RAMS1A is a parameterized static RAM function supported by automatic layout generation software. The layout of the RAMS1A is implemented as a custom, pitch-matched array of cells that is very area-efficient.

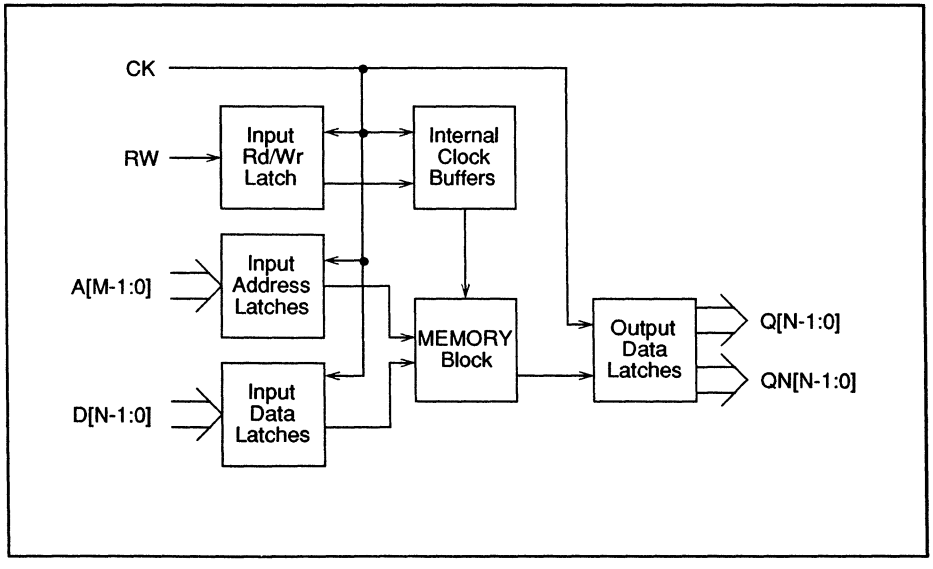
The RAMS1A has been designed specifically for use on standard cell chips and has overhead circuitry already built-in including:

- Positive Edge-Triggered Input Data Latches with Minimum Set-up Times
- Positive Edge-Triggered Address Latches with Minimum Set-up Times
- Positive Edge-Triggered Read/ Write Latch with Minimum Set-up Times
- Positive Edge-Triggered Output Data Latches with Minimum Set-up Times
- Column and Row Decoding
- A Clock Generator that derives all necessary internal clocks from a single clock input.

RAMS1A can be customized with the following parameters:

Parameter	Description	Limits		
		Increment	Min	Max
N	Bits/Word	1	2	32
M	Address Bits	1	3	10
W	Words	8	8	1,024

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A[M-1:0], D[N-1:0], RW, CK;

OUTPUTS: Q[N-1:0], QN[N-1:0];

Functional Descriptions

Inputs

A[M-1:0]	Address In (A0 = LSB)
D[N-1:0]	Data In
RW	Read/Write - (Read = '1')
CK	Clock

Outputs

Q[N-1:0]	Data Out
QN[N-1:0]	Complement Data Out

CHARACTERISTICS

The parameters **N**, **M** and **W** can be used to estimate the characteristics for a RAMS1A that is **W** words X **N** bits per word with **M** address bits.

Parameter	Value	Unit
Number of Transistors	240 + 56M + 170N + (34 + M)W/8 + 6NW	
Height	735 + 5W	µ
Width	322 + 75.75N	µ
Worst Case Power	$(26.0+2.4M+0.11W+3.9N+0.0088NW+0.0044MW)VDD^2F/1{,}000$*	mW
Input Capacitance:		
A[M-1:0]	0.16	pF
D[N-1:0]	0.16	pF
RW	0.16	pF
CK	0.23 + 0.23N + 0.08M	pF
Output Capacitance:		
Q[N-1:0]	0.30	pF
QN[N-1:0]	0.29	pF

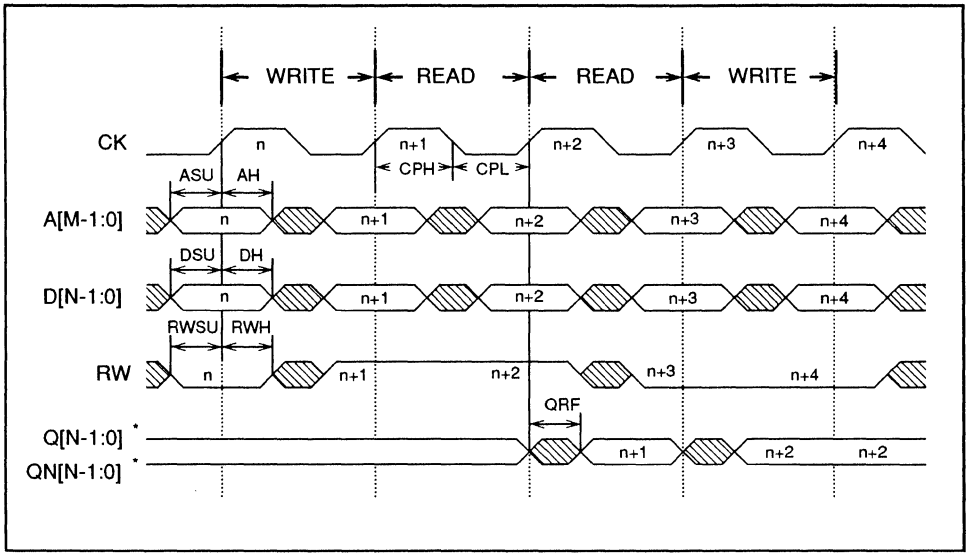
* VDD = the power supply voltage in Volts and F = the clock frequency in MHz.

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing				
Symbol	From INPUT	To OUTPUT	Intrinsic (ns)	Extrinsic (ns/pF)
QRF	CK↑	Q[N-1:0]↑	2.0*	0.6
	CK↑	Q[N-1:0]↓	2.0*	0.3
	CK↑	QN[N-1:0]↑	2.0*	0.6
	CK↑	QN[N-1:0]↓	2.0*	0.3

* In situations where the actual clock pulse width low (PWL) is less than (CPL+11)ns, then add (CPL+11-PWL)ns. CPL is the minimum clock pulse low as given in the Timing Requirements table.

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing		
Symbol	Description	Value (ns)
CPH	Minimum Clock Pulse High	10+N/8+(2+N/8)(W-256)/768
CPL	Minimum Clock Pulse Low	10+N/8+(2+N/8)(W-256)/768
ASU	Minimum Address Setup before CK↑	3.0
AH	Minimum Address Hold after CK↑	0.0
DSU	Minimum Data Setup before CK↑	3.0
DH	Minimum Data Hold after CK↑	0.0
RWSU	Minimum Read/Write Setup before CK↑	3.0
RWH	Minimum Read/Write Hold after CK↑	0.0

TIMING DIAGRAM



n=nth cycle number.

*Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ output is continuously available during subsequent WRITE operations.

8

USER NOTES

1) Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ outputs are continuously available during subsequent WRITE operations.
2) No glitches are allowed on the clock input CK. If the minimum clock pulse widths (high or low) are violated, any of the internal memory contents can be corrupted.
3) If the setup and hold time specs on the address inputs are violated, any of the internal memory contents can be corrupted.

FUNCTIONAL DESCRIPTION AND FEATURES

RAMS1AT is a parameterized static RAM function supported by automatic layout generation software. The layout of the RAMS1AT is implemented as a custom, pitch-matched array of cells that is very area-efficient.

The RAMS1AT has been designed specifically for use on standard cell chips and has overhead circuitry already built-in including:

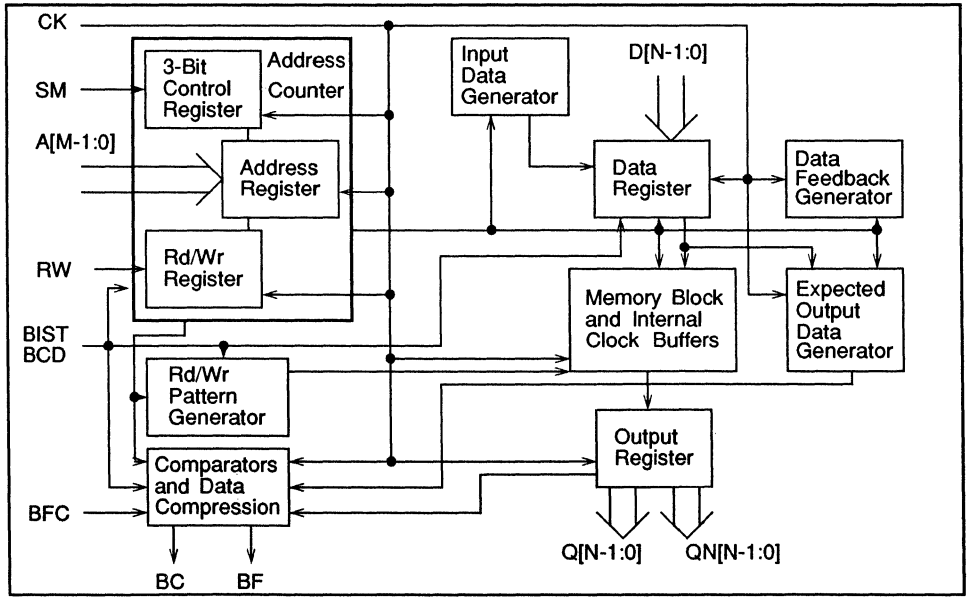
- Positive Edge-Triggered Input Data Latches with Minimum Set-Up Times
- Positive Edge-Triggered Address Latches with Minimum Set-Up Times
- Positive Edge-Triggered Read/ Write Latch with Minimum Set-Up Time
- Positive Edge-Triggered Output Data Latches with Minimum Propagation Delays
- Column and Row Decoding
- A Clock Generator that derives all necessary internal clocks from a single clock input.
- Select macrocell capability that allows the RAMS1AT to power down while it's not being used.
- Built-In Self-Test circuitry that tests itself as well as the memory.

RAMS1AT can be customized with the following parameters:

Parameter	Description	Limits		
		Increment	Min	Max
N	Bits/Word	1	4	32
M	Address Bits	1	3	10
W	Words	8	8	1,024

8

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A[M-1:0], D[N-1:0], RW, SM, CK, BCD, BFC, BIST;

OUTPUTS: Q[N-1:0], QN[N-1:0], BF, BC;

Functional Descriptions

Inputs

A[M-1:0]	Address In (A0 = LSB)
D[N-1:0]	Data In
RW	Read/Write - (Read = '1')
SM	Select Macrocell - (Active High)
CK	Clock
BCD	BIST Clear - (Active High)
BFC	BIST Flag Check - (Active High)
BIST	BIST test mode - (Active High)

Outputs

Q[N-1:0]	Data Out
QN[N-1:0]	Complement Data Out
BF	BIST Flag - (Good device: See Built-In Self-Test Mode timing diagram)
BC	BIST Complete - (BIST test completed = '1')

CHARACTERISTICS

The parameters **N**, **M** and **W** can be used to estimate the characteristics for a RAMS1AT that is **W** words X **N** bits per word with **M** address bits.

Parameter	Value	Unit
Number of Transistors	907 + 90**M** + 232**N** + (34 + **M**)**W**/8 + 6**NW***	
Height	968 + 5**W**	μ
Width	325.25 + 75.75**N**	μ
Worst Case Power	1.2(26.0+2.4**M**+0.11**W**+3.9**N**+0.0088**NW**+0.0044**MW**)**VDD**^{2}**F**/1,000**	mW
Input Capacitance:		
A[M-1:0]	0.08	pF
D[N-1:0]	0.10	pF
RW	0.08	pF
SM	0.09	pF
CK	1.46 + 0.25**N** + 0.08**M**	pF
BCD	0.44 + 0.08**N** + 0.08**M**	pF
BFC	0.08	pF
BIST	0.66 + 0.15**N** + 0.16**M**	pF
Output Capacitance:		
Q[N-1:0]	0.46	pF
QN[N-1:0]	0.30	pF
BF	0.15	pF
BC	0.32	pF

* For **N** equal to 4 and 5, add 36 and 18 transistors, respectively.

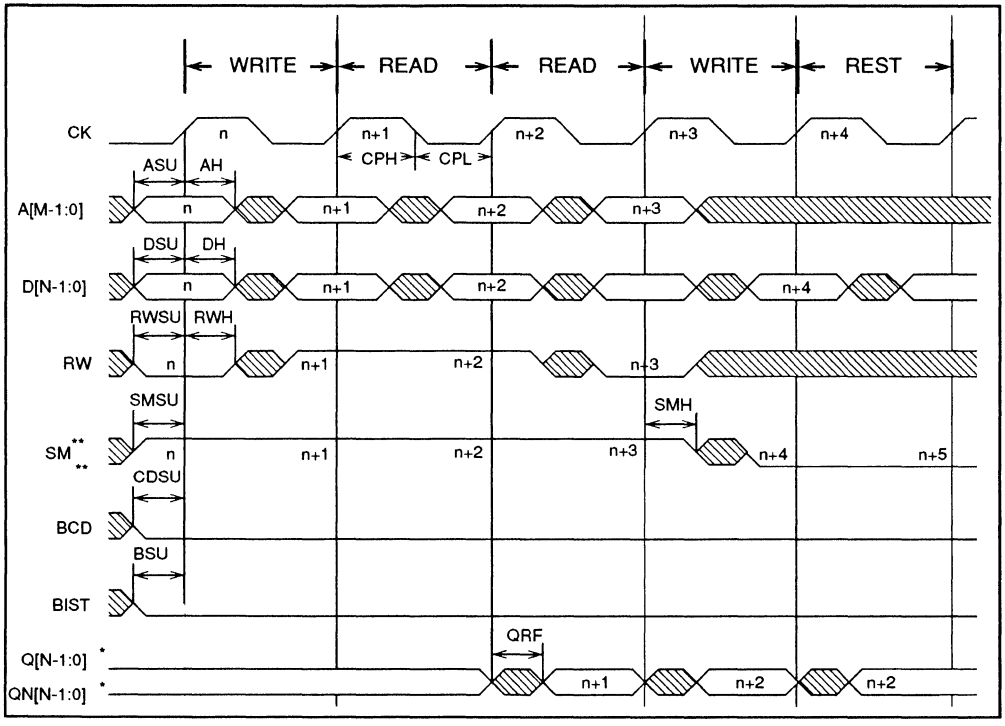
** **VDD** = the power supply voltage in Volts and **F** = the clock frequency in MHz.

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing				
Symbol	From INPUT	To OUTPUT	Intrinsic (ns)	Extrinsic (ns/pF)
QRF	CK↑	Q[N-1:0]↑	2.1*	0.6
	CK↑	Q[N-1:0]↓	2.1*	0.3
	CK↑	QN[N-1:0]↑	2.1*	0.6
	CK↑	QN[N-1:0]↓	2.1*	0.3
BFRF	CK↑	BF↑	3.9	2.0
	CK↑	BF↓	2.9	1.2
BCRF	CK↑	BC↑	2.3	2.1
	CK↑	BC↓	3.2	1.4

* In situations where the actual clock pulse width low (call it PWL) is less than (CPL+11)ns, then add (CPL+11-PWL)ns. CPL is the minimum clock pulse low as given in the Timing Requirements table.

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing		
Symbol	Description	Value (ns)
CPH	Minimum Clock Pulse High	10+N/8+(2+N/8)(W-256)/ 768
CPL	Minimum Clock Pulse Low	10+N/8+(2+N/8)(W-256)/ 768
ASU	Minimum Address Setup before CK↑	3.6
AH	Minimum Address Hold after CK↑	0.0
DSU	Minimum Data Setup before CK↑	4.1
DH	Minimum Data Hold after CK↑	0.0
RWSU	Minimum Read/Write Setup before CK↑	3.7
RWH	Minimum Read/Write Hold after CK↑	0.0
SMSU	Minimum Select Macrocell Setup before CK↑	3.5
SMH	Minimum Select Macrocell Hold after CK↑	0.0
CDSU	Minimum BIST Clear Setup before CK↑	2.6 + 0.088N
CDH	Minimum BIST Clear Hold after CK↑	0.0
FCSU	Minimum BIST Flag Check Setup before CK↑	4.4
FCH	Minimum BIST Flag Check Hold after CK↑	0.0
BSU	Minimum BIST Test Mode Setup before CK↑	4.1 + 0.16N
BH	Minimum BIST Test Mode Hold after CK↑	0.0

FUNCTIONAL MODE TIMING DIAGRAM



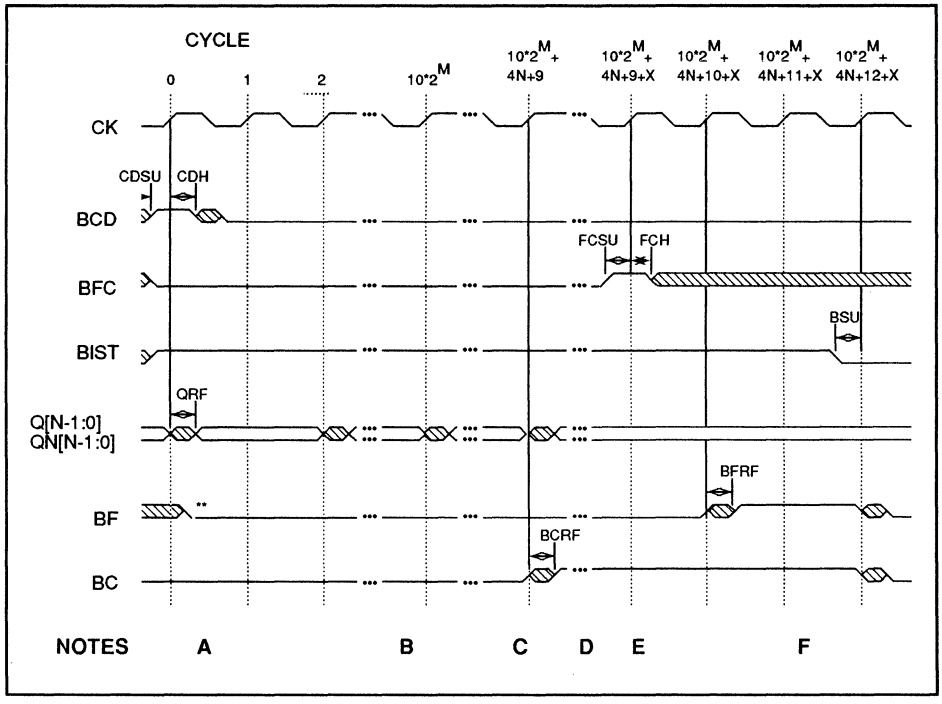
n=nth cycle number.

*Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ output is continuously available during subsequent WRITE operations.

**Setting SM low disables the inputs and freezes the internal contents and outputs of the RAMS1AT. The RAMS1AT is powered down during rest (deselected) cycles.

8

Built-In Self-Test Mode



8

* See User note 9.

** See User note 10.

A) RAM is initialized for BIST. The input BCD can be held high for any number of clock cycles. The 0'th clock cycle is defined as the last clock cycle in which the BCD input is clocked in as a '1'.

B) Internal memory test is completed. BIST overhead test is automatically initiated. As soon as a fault is detected, BF will go high and remain there until BIST goes low.

C) BIST overhead test is completed. This event is signaled to the user by driving BC high.

D) BF should be checked after BC goes high. If BF is high, the RAM is bad. If BF is low, a stuck-at-0 fault for BF must now be checked. The RAM contents and output are frozen until the user signals the last fault to be tested. This feature allows the user to check BF whenever he is ready (the waveform diagram indicates a variable wait time of X clock cycles). It also allows the user to run BIST in parallel for several RAMs having different organizations.

E) BFC is set high to start the test for the last fault.

F) One cycle after BFC is latched in, BF should go high to indicate that the RAM is good. The RAM should be considered bad otherwise.

USER NOTES

1) Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ outputs are continuously available during subsequent WRITE operations.
2) No glitches are allowed on the clock input CK. If the minimum clock pulse widths (high or low) are violated, any of the internal memory contents can be corrupted.

3) If the setup and hold time specs on the address inputs are violated, any of the internal memory contents can be corrupted.
4) If the clock cycles can be accurately counted while monitoring BF during the built-in self-test mode, then the output BC can be directly connected to the input BFC to save on the number of user-supplied I/O signals.
5) Outputs BF and BC will default to a low and input BFC is ignored while the RAMS1AT is not in the built-in self-test mode (BIST = '0').
6) Inputs A[M-1:0], D[N-1:0], RW, and SM are completely ignored while the RAMS1AT is in the built-in self-test mode.
7) Outputs Q[N-1:0] and QN[N-1:0] will change in response to each READ operation that is exercised in the built-in self-test mode.
8) Up to 90 % of the power can be saved when the RAMS1AT is deselected (SM = '0').
9) When the BIST input is low, the BF and BC outputs are held low. If the initial highs on the BIST and the BCD inputs are latched in at the same time, BF and BC will remain low. If the BIST input goes high one or more cycles before the BCD input goes high, the BF output may go high until it is cleared after the high on the BCD input is latched into the RAMS1AT. It can be avoided by placing the RAMS1AT in the WRITE mode during the clock cycle just before a high on the BIST input is latched into the RAMS1AT. A high on the BCD input should then be latched no more than one clock cycle after a high on the BIST input is latched into the RAMS1AT.
10) Some failure modes may exist within the RAMS1AT that force the BF output to go high early while freezing the BC output low. This should be checked with external logic, software, or test vectors.

FUNCTIONAL DESCRIPTION AND FEATURES

RAMS1B is a parameterized static RAM function supported by automatic layout generation software. The layout of the RAMS1B is implemented as a custom, pitch-matched array of cells that is very area-efficient.

The RAMS1B has been designed specifically for use on standard cell chips and has overhead circuitry already built-in including:

- Negative Edge-Triggered Input Data Latches with Relaxed Set-Up Times
- Negative Edge-Triggered Address Latches with Relaxed Set-Up Times
- Negative Edge-Triggered Read/ Write Latch with Relaxed Set-Up Times
- Positive Edge-Triggered Output Data Latches with Minimum Propagation Delays
- Column and Row Decoding
- A Clock Generator that derives all necessary internal clocks from a single clock input.

RAMS1B can be customized with the following parameters:

Parameter	Description	Limits		
		Increment	Min	Max
N	Bits/Word	1	2	32
M	Address Bits	1	3	10
W	Words	8	8	1,024

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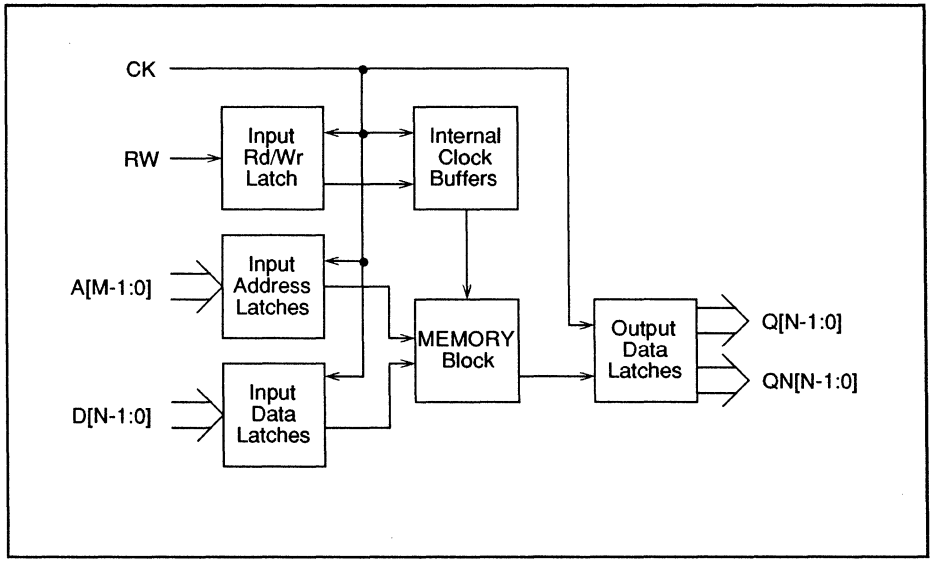
BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A[M-1:0], D[N-1:0], RW, CK;

OUTPUTS: Q[N-1:0], QN[N-1:0];

Functional Descriptions

Inputs

A[M-1:0]	Address In (A0 = LSB)
D[N-1:0]	Data In
RW	Read/Write - (Read = '1')
CK	Clock

Outputs

Q[N-1:0]	Data Out
QN[N-1:0]	Complement Data Out

CHARACTERISTICS

The parameters **N**, **M** and **W** can be used to estimate the characteristics for a RAMS1B that is **W** words X **N** bits per word with **M** address bits.

Parameter	Value	Unit
Number of Transistors	232 + 48M + 162N + (34 + M)W/8 + 6NW	
Height	705 + 5W	µ
Width	322 + 75.75N	µ
Worst Case Power	$(25.5+2.1M+0.11W+3.7N+0.0088NW+0.0044MW)VDD^2F/1{,}000$*	mW
Input Capacitance:		
A[M-1:0]	0.16	pF
D[N-1:0]	0.16	pF
RW	0.16	pF
CK	0.23 + 0.23N + 0.08M	pF
Output Capacitance:		
Q[N-1:0]	0.30	pF
QN[N-1:0]	0.29	pF

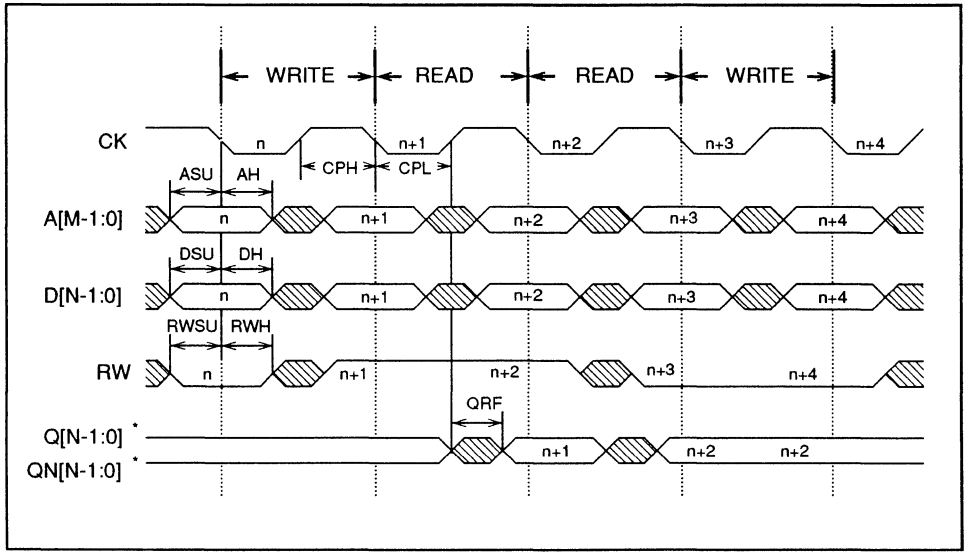
* **VDD** = the power supply voltage in Volts and **F** = the clock frequency in MHz.

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing				
Symbol	From INPUT	To OUTPUT	Intrinsic (ns)	Extrinsic (ns/pF)
QRF	CK↑	Q[N-1:0]↑	2.0*	0.6
	CK↑	Q[N-1:0]↓	2.0*	0.3
	CK↑	QN[N-1:0]↑	2.0*	0.6
	CK↑	QN[N-1:0]↓	2.0*	0.3

* In situations where the actual clock pulse width low (call it PWL) is less than (CPL+11)ns, then add (CPL+11-PWL)ns. CPL is the minimum clock pulse low as given in the Timing Requirements table.

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing		
Symbol	Description	Value (ns)
CPH	Minimum Clock Pulse High	10+N/8+(2+N/8)(W-256)/768
CPL	Minimum Clock Pulse Low	10+N/8+(2+N/8)(W-256)/768
ASU	Minimum Address Setup before CK↓	10.0
AH	Minimum Address Hold after CK↓	0.0
DSU	Minimum Data Setup before CK↓	10.0
DH	Minimum Data Hold after CK↓	0.0
RWSU	Minimum Read/Write Setup before CK↓	10.0
RWH	Minimum Read/Write Hold after CK↓	0.0

TIMING DIAGRAM



n=nth cycle number.

*Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ output is continuously available during subsequent WRITE operations.

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USER NOTES

1) Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ outputs are continuously available during subsequent WRITE operations.
2) No glitches are allowed on the clock input CK. If the minimum clock pulse widths (high or low) are violated, any of the internal memory contents can be corrupted.
3) If the setup and hold time specs on the address inputs are violated, any of the internal memory contents can be corrupted.

FUNCTIONAL DESCRIPTION AND FEATURES

RAMS1C is a parameterized static RAM function supported by automatic layout generation software. The layout of the RAMS1C is implemented as a custom, pitch-matched array of cells that is very area-efficient.

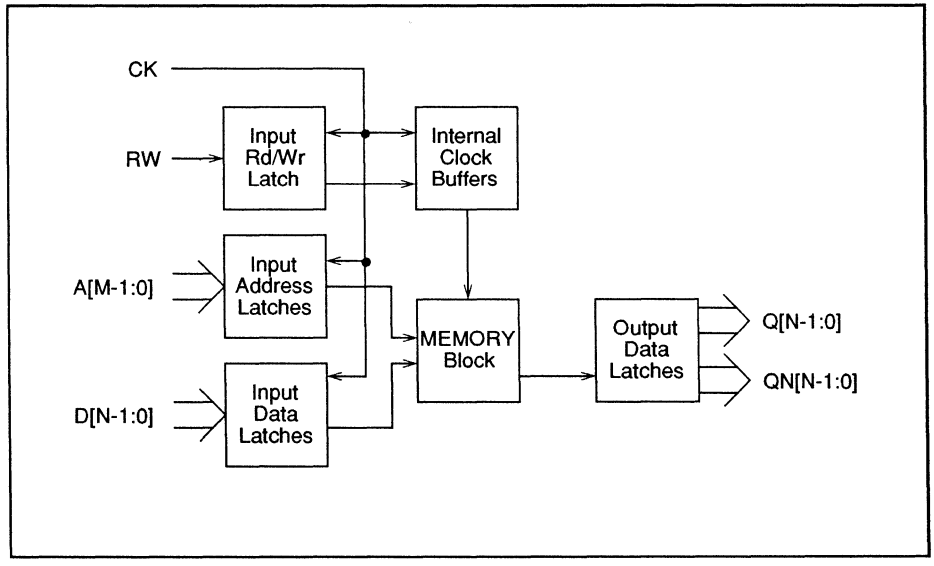
The RAMS1C has been designed specifically for use on standard cell chips and has overhead circuitry already built-in including:

- Positive Edge-Triggered Input Data Latches with Minimum Set-Up Times
- Positive Edge-Triggered Address Latches with Minimum Set-Up Times
- Positive Edge-Triggered Read/ Write Latch with Minimum Set-Up Time
- Negative Edge-Triggered Output Data Latches with Relaxed Propagation Delays
- Column and Row Decoding
- A Clock Generator that derives all necessary internal clocks from a single clock input.

RAMS1C can be customized with the following parameters:

Parameter	Description	Limits		
		Increment	Min	Max
N	Bits/Word	1	2	32
M	Address Bits	1	3	10
W	Words	8	8	1,024

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A[M-1:0], D[N-1:0], RW, CK;

OUTPUTS: Q[N-1:0], QN[N-1:0];

Functional Descriptions

Inputs

A[M-1:0]	Address In (A0 = LSB)
D[N-1:0]	Data In
RW	Read/Write - (Read = '1')
CK	Clock

Outputs

Q[N-1:0]	Data Out
QN[N-1:0]	Complement Data Out

CHARACTERISTICS

The parameters **N**, **M** and **W** can be used to estimate the characteristics for a RAMS1C that is **W** words X **N** bits per word with **M** address bits.

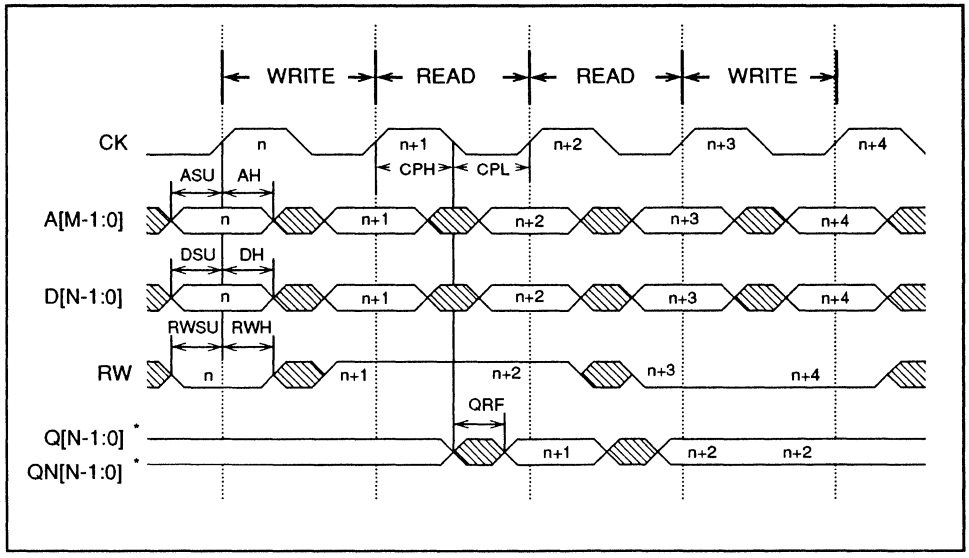
Parameter	Value	Unit
Number of Transistors	240 + 56**M** + 168**N** + (34 + **M**)**W**/8 + 6**NW**	
Height	730 + 5**W**	µ
Width	322 + 75.75**N**	µ
Worst Case Power	(26.0+2.4**M**+0.11**W**+3.8**N**+0.0088**NW**+0.0044**MW**)**VDD**^{2}**F**/1,000*	mW
Input Capacitance:		
A[M-1:0]	0.16	pF
D[N-1:0]	0.16	pF
RW	0.16	pF
CK	0.23 + 0.08**N** + 0.08**M**	pF
Output Capacitance:		
Q[N-1:0]	0.27	pF
QN[N-1:0]	0.27	pF

* **VDD** = the power supply voltage in Volts and **F** = the clock frequency in MHz.

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing				
Symbol	**From INPUT**	**To OUTPUT**	**Intrinsic (ns)**	**Extrinsic (ns/pF)**
QRF	CK↓	Q[N-1:0]↑	21+N/8+(2+N/8)(W-256)/ 768	0.6
	CK↓	Q[N-1:0]↓	21+N/8+(2+N/8)(W-256)/ 768	0.3
	CK↓	QN[N-1:0]↑	21+N/8+(2+N/8)(W-256)/ 768	0.6
	CK↓	QN[N-1:0]↓	21+N/8+(2+N/8)(W-256)/ 768	0.3

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing		
Symbol	**Description**	**Value (ns)**
CPH	Minimum Clock Pulse High	10+N/8+(2+N/8)(W-256)/ 768
CPL	Minimum Clock Pulse Low	10+N/8+(2+N/8)(W-256)/ 768
ASU	Minimum Address Setup before CK↑	3.0
AH	Minimum Address Hold after CK↑	0.0
DSU	Minimum Data Setup before CK↑	3.0
DH	Minimum Data Hold after CK↑	0.0
RWSU	Minimum Read/Write Setup before CK↑	3.0
RWH	Minimum Read/Write Hold after CK↑	0.0

TIMING DIAGRAM



n=nth cycle number.

*Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ output is continuously available during subsequent WRITE operations.

USER NOTES

1) Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ outputs are continuously available during subsequent WRITE operations.
2) No glitches are allowed on the clock input CK. If the minimum clock pulse widths (high or low) are violated, any of the internal memory contents can be corrupted.
3) If the setup and hold time specs on the address inputs are violated, any of the internal memory contents can be corrupted.

FUNCTIONAL DESCRIPTION AND FEATURES

RAMS1CT is a parameterized static RAM function supported by automatic layout generation software. The layout of the RAMS1CT is implemented as a custom, pitch-matched array of cells that is very area-efficient.

The RAMS1CT has been designed specifically for use on standard cell chips and has overhead circuitry already built-in including:

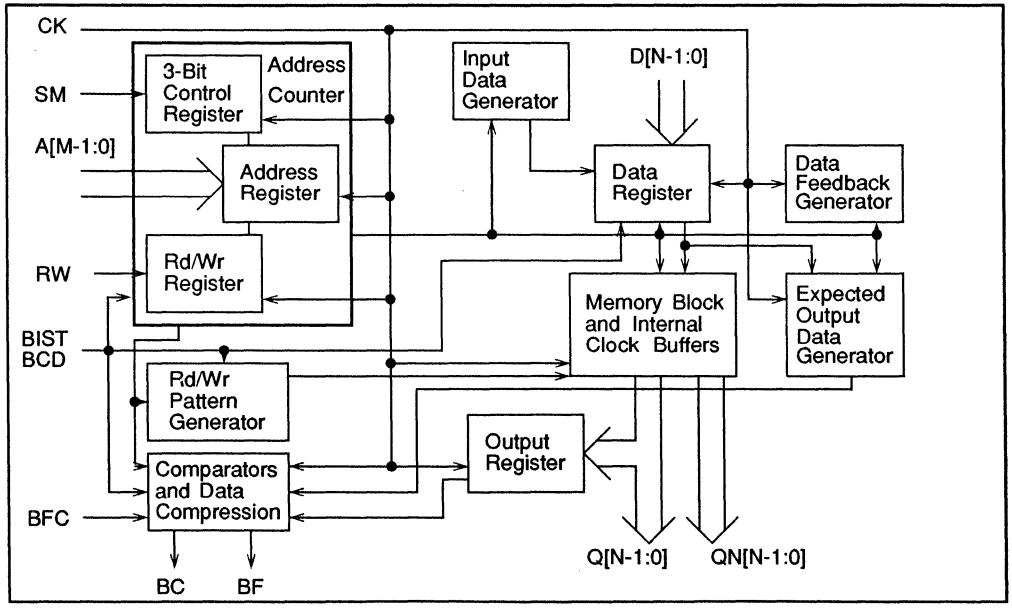
- Positive Edge-Triggered Input Data Latches with Minimum Set-Up Times
- Positive Edge-Triggered Address Latches with Minimum Set-Up Times
- Positive Edge-Triggered Read/ Write Latch with Minimum Set-Up Time
- Negative Edge-Triggered Output Data Latches with Relaxed Propagation Delays
- Column and Row Decoding
- A Clock Generator that derives all necessary internal clocks from a single clock input.
- Select macrocell capability that allows the RAMS1CT to power down while it's not being used.
- Built-In Self-Test circuitry that tests itself as well as the memory.

RAMS1CT can be customized with the following parameters:

Parameter	Description	Limits		
		Increment	Min	Max
N	Bits/Word	1	4	32
M	Address Bits	1	3	10
W	Words	8	8	1,024

8

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A[M-1:0], D[N-1:0], RW, SM, CK, BCD, BFC, BIST;
OUTPUTS: Q[N-1:0], QN[N-1:0], BF, BC;

Functional Descriptions

Inputs

A[M-1:0]	Address In (A0 = LSB)
D[N-1:0]	Data In
RW	Read/Write - (Read = '1')
SM	Select Macrocell - (Active High)
CK	Clock
BCD	BIST Clear - (Active High)
BFC	BIST Flag Check - (Active High)
BIST	BIST test mode - (Active High)

Outputs

Q[N-1:0]	Data Out
QN[N-1:0]	Complement Data Out
BF	BIST Flag - (Good device: See Built-In Self-Test Mode timing diagram)
BC	BIST Complete - (BIST test completed = '1')

CHARACTERISTICS

The parameters N, M and W can be used to estimate the characteristics for a RAMS1CT that is W words X N bits per word with M address bits.

Parameter	Value	Unit
Number of Transistors	907 + 90M + 236N + (34 + M)W/8 + 6NW*	
Height	977.5 + 5W	µ
Width	325.25 + 75.75N	µ
Worst Case Power	$1.2(26.0+2.4M+0.11W+3.9N+0.0088NW+0.0044MW)VDD^2F/1{,}000$**	mW
Input Capacitance:		
A[M-1:0]	0.08	pF
D[N-1:0]	0.10	pF
RW	0.08	pF
SM	0.09	pF
CK	1.46 + 0.25N + 0.08M	pF
BCD	0.44 + 0.08N + 0.08M	pF
BFC	0.08	pF
BIST	0.66 + 0.15N + 0.16M	pF
Output Capacitance:		
Q[N-1:0]	0.31	pF
QN[N-1:0]	0.31	pF
BF	0.15	pF
BC	0.32	pF

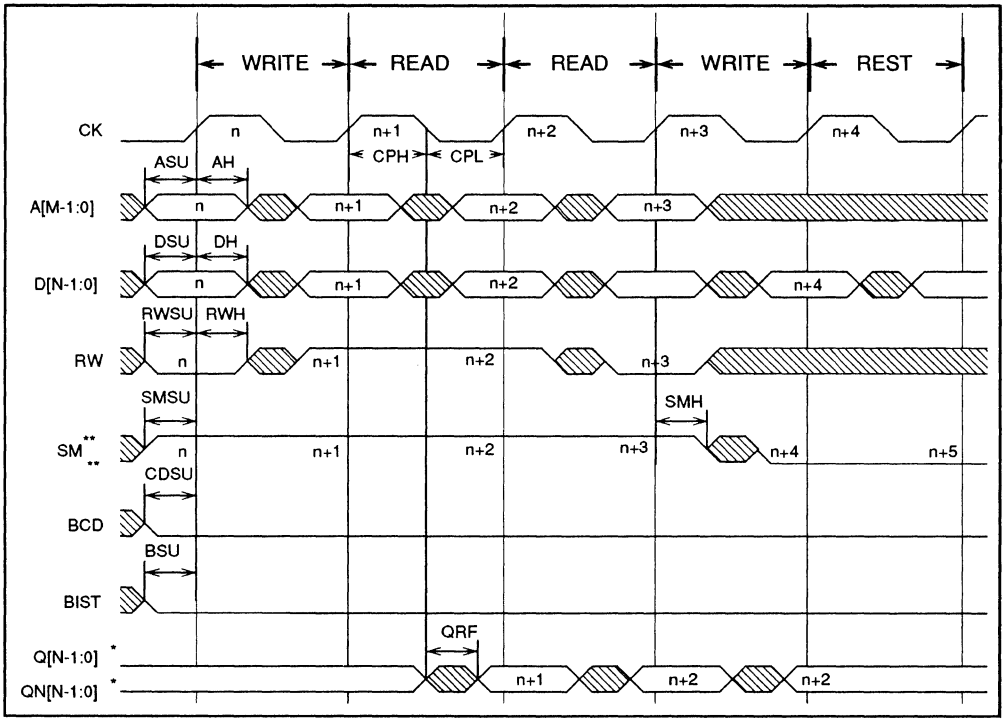
* For N equal to 4 and 5, add 36 and 18 transistors, respectively.

** VDD = the power supply voltage in Volts and F = the clock frequency in MHz.

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing				
Symbol	From INPUT	To OUTPUT	Intrinsic (ns)	Extrinsic (ns/pF)
QRF	CK↓	Q[N-1:0]↑	21+N/8+(2+N/8)(W-256)/ 768	0.6
	CK↓	Q[N-1:0]↓	21+N/8+(2+N/8)(W-256)/ 768	0.3
	CK↓	QN[N-1:0]↑	21+N/8+(2+N/8)(W-256)/ 768	0.6
	CK↓	QN[N-1:0]↓	21+N/8+(2+N/8)(W-256)/ 768	0.3
BFRF	CK↑	BF↑	3.9	2.0
	CK↑	BF↓	2.9	1.2
BCRF	CK↑	BC↑	2.3	2.1
	CK↑	BC↓	3.2	1.4

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing		
Symbol	Description	Value (ns)
CPH	Minimum Clock Pulse High	10+N/8+(2+N/8)(W-256)/ 768
CPL	Minimum Clock Pulse Low	10+N/8+(2+N/8)(W-256)/ 768
ASU	Minimum Address Setup before CK↑	3.6
AH	Minimum Address Hold after CK↑	0.0
DSU	Minimum Data Setup before CK↑	4.1
DH	Minimum Data Hold after CK↑	0.0
RWSU	Minimum Read/Write Setup before CK↑	3.7
RWH	Minimum Read/Write Hold after CK↑	0.0
SMSU	Minimum Select Macrocell Setup before CK↑	3.5
SMH	Minimum Select Macrocell Hold after CK↑	0.0
CDSU	Minimum BIST Clear Setup before CK↑	2.6 + 0.088N
CDH	Minimum BIST Clear Hold after CK↑	0.0
FCSU	Minimum BIST Flag Check Setup before CK↑	4.4
FCH	Minimum BIST Flag Check Hold after CK↑	0.0
BSU	Minimum BIST Test Mode Setup before CK↑	4.1 + 0.16N
BH	Minimum BIST Test Mode Hold after CK↑	0.0

FUNCTIONAL MODE TIMING DIAGRAM



n=nth cycle number.

*Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ output is continuously available during subsequent WRITE operations.

**Setting SM low disables the inputs and freezes the internal contents and outputs of the RAMS1CT. The RAMS1CT is powered down during rest (deselected) cycles.

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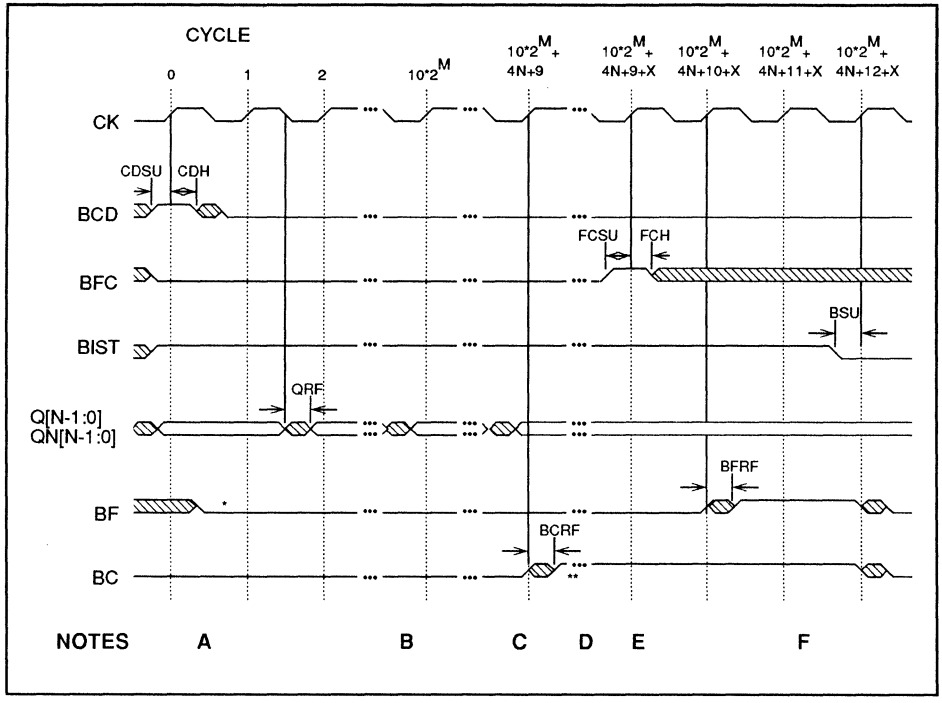
BUILT-IN SELF-TEST TIMING DIAGRAM



* See User Note 9.

** See User Note 10.

A) RAM is initialized for BIST. The input BCD can be held high for any number of clock cycles. The 0'th clock cycle is defined as the last clock cycle in which the BCD input is clocked in as a '1'.

B) Internal memory test is completed. BIST overhead test is automatically initiated. As soon as a fault is detected, BF will go high and remain there until BIST goes low.

C) BIST overhead test is completed. This event is signaled to the user by driving BC high.

D) BF should be checked after BC goes high. If BF is high, the RAM is bad. If BF is low, a stuck-at-0 fault for BF must now be checked. The RAM contents and output are frozen until the user signals the last fault to be tested. This feature allows the user to check BF whenever he is ready (the waveform diagram indicates a variable wait time of X clock cycles). It also allows the user to run BIST in parallel for several RAMs having different organizations.

E) BFC is set high to start the test for the last fault.

F) One cycle after BFC is latched in, BF should go high to indicate that the RAM is good. The RAM should be considered bad otherwise.

USER NOTES:

1) Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ outputs are continuously available during subsequent WRITE operations.
2) No glitches are allowed on the clock input CK. If the minimum clock pulse widths (high or low) are violated, any of the internal memory contents can be corrupted.

3) If the setup and hold time specs on the address inputs are violated, any of the internal memory contents can be corrupted.
4) If the clock cycles can be accurately counted while monitoring BF during the built-in self-test mode, then the output BC can be directly connected to the input BFC to save on the number of user-supplied I/O signals.
5) Outputs BF and BC will default to a low and input BFC is ignored while the RAMS1CT is not in the built-in self-test mode (BIST = '0').
6) Inputs A[M-1:0], D[N-1:0], RW, and SM are completely ignored while the RAMS1CT is in the built-in self-test mode.
7) Outputs Q[N-1:0] and QN[N-1:0] will change in response to each READ operation that is exercised in the built-in self-test mode.
8) Up to 90 % of the power can be saved when the RAMS1CT is deselected (SM = '0'). When the BIST input is low, the BF and BC outputs are held low. If the initial highs on the BIST and the BCD inputs are latched in at the same time, BF and BC will remain low.
9) If the BIST input goes high one or more cycles before the BCD input goes high, the BF output may go high until it is cleared after the high on the BCD input is latched into the RAMS1CT. It can be avoided by placing the RAMS1CT in the WRITE mode during the clock cycle just before a high on the BIST input is latched into the RAMS1AT. A high on the BCD input should then be latched no more than one clock cycle after a high on the BIST input is latched into the RAMS1CT.
10) Some failure modes may exist within the RAMS1CT that force the BF output to go high early while freezing the BC output low. This should be checked with external logic, software, or test vectors.

FUNCTIONAL DESCRIPTION AND FEATURES

RAMS1D is a parameterized static RAM function supported by automatic layout generation software. The layout of the RAMS1D is implemented as a custom, pitch-matched array of cells that is very area-efficient.

The RAMS1D has been designed specifically for use on standard cell chips and has overhead circuitry already built-in including:

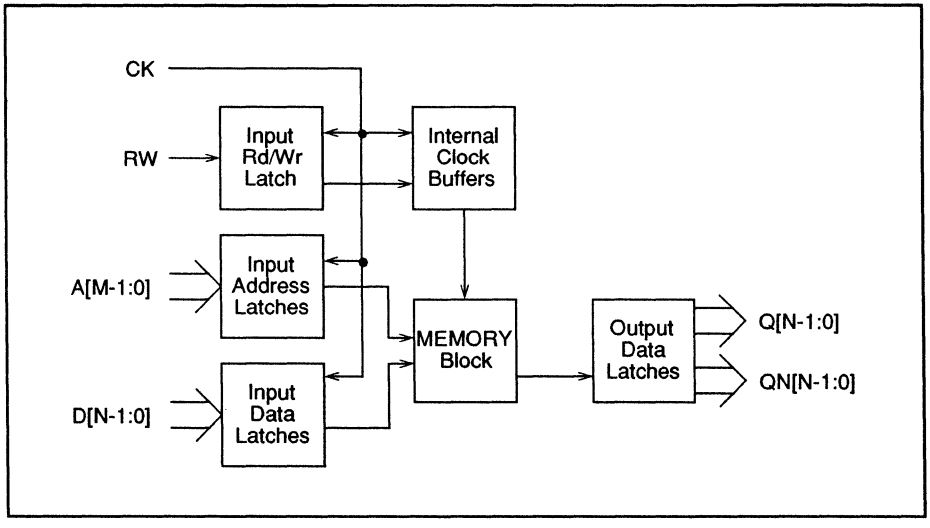
- Negative Edge-Triggered Input Data Latches with Relaxed Set-Up Times
- Negative Edge-Triggered Address Latches with Relaxed Set-Up Times
- Negative Edge-Triggered Read/ Write Latch with Relaxed Set-Up Time
- Negative Edge-Triggered Output Data Latches with Relaxed Propagation Delays
- Column and Row Decoding
- A Clock Generator that derives all necessary internal clocks from a single clock input.

RAMS1D can be customized with the following parameters:

Parameter	Description	Limits		
		Increment	Min	Max
N	Bits/Word	1	2	32
M	Address Bits	1	3	10
W	Words	8	8	1,024

8

BLOCK DIAGRAM:



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A[M-1:0], D[N-1:0], RW, CK;

OUTPUTS: Q[N-1:0], QN[N-1:0];

Functional Descriptions

Inputs

A[M-1:0]	Address In (A0 = LSB)
D[N-1:0]	Data In
RW	Read/Write - (Read = '1')
CK	Clock

Outputs

Q[N-1:0]	Data Out
QN[N-1:0]	Complement Data Out

CHARACTERISTICS:

The parameters N, M and W can be used to estimate the characteristics for a RAMS1D that is W words X N bits per word with M address bits.

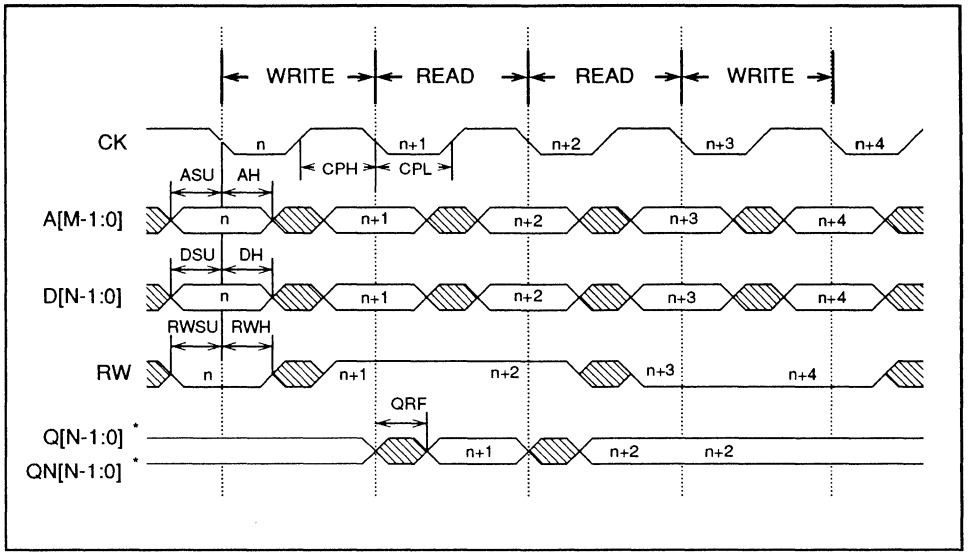
Parameter	Value	Unit
Number of Transistors	260 + 48M + 160N + (34 + M)W/8 + 6NW	
Height	700 + 5W	µ
Width	322 + 75.75N	µ
Worst Case Power	$(25.5+2.1M+0.11W+3.6N+0.0088NW+0.0044MW)VDD^2F/1,000$*	mW
Input Capacitance:		
A[M-1:0]	0.16	pF
D[N-1:0]	0.16	pF
RW	0.16	pF
CK	0.23 + 0.08N + 0.08M	pF
Output Capacitance:		
Q[N-1:0]	0.27	pF
QN[N-1:0]	0.27	pF

* VDD = the power supply voltage in Volts and F = the clock frequency in MHz.

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing				
Symbol	From INPUT	To OUTPUT	Intrinsic (ns)	Extrinsic (ns/pF)
QRF	CK↓	Q[N-1:0]↑	21+N/8+(2+N/8)(W-256)/ 768	0.6
	CK↓	Q[N-1:0]↓	21+N/8+(2+N/8)(W-256)/ 768	0.3
	CK↓	QN[N-1:0]↑	21+N/8+(2+N/8)(W-256)/ 768	0.6
	CK↓	QN[N-1:0]↓	21+N/8+(2+N/8)(W-256)/ 768	0.3

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing		
Symbol	Description	Value (ns)
CPH	Minimum Clock Pulse High	10+N/8+(2+N/8)(W-256)/ 768
CPL	Minimum Clock Pulse Low	10+N/8+(2+N/8)(W-256)/ 768
ASU	Minimum Address Setup before CK↓	10.0
AH	Minimum Address Hold after CK↓	0.0
DSU	Minimum Data Setup before CK↓	10.0
DH	Minimum Data Hold after CK↓	0.0
RWSU	Minimum Read/Write Setup before CK↓	10.0
RWH	Minimum Read/Write Hold after CK↓	0.0

TIMING DIAGRAM



n=nth cycle number.

*Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ output is continuously available during subsequent WRITE operations.

8

USER NOTES

1) Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ outputs are continuously available during subsequent WRITE operations.
2) No glitches are allowed on the clock input CK. If the minimum clock pulse widths (high or low) are violated, any of the internal memory contents can be corrupted.
3) If the setup and hold time specs on the address inputs are violated, any of the internal memory contents can be corrupted.

FUNCTIONAL DESCRIPTION AND FEATURES

RAMS1E is a parameterized static RAM function supported by automatic layout generation software. The layout of the RAMS1E is implemented as a custom, pitch-matched array of cells that is very area-efficient.

The RAMS1E has been designed specifically for use on standard cell chips that use a scan-testing strategy and has overhead circuitry already built-in including:

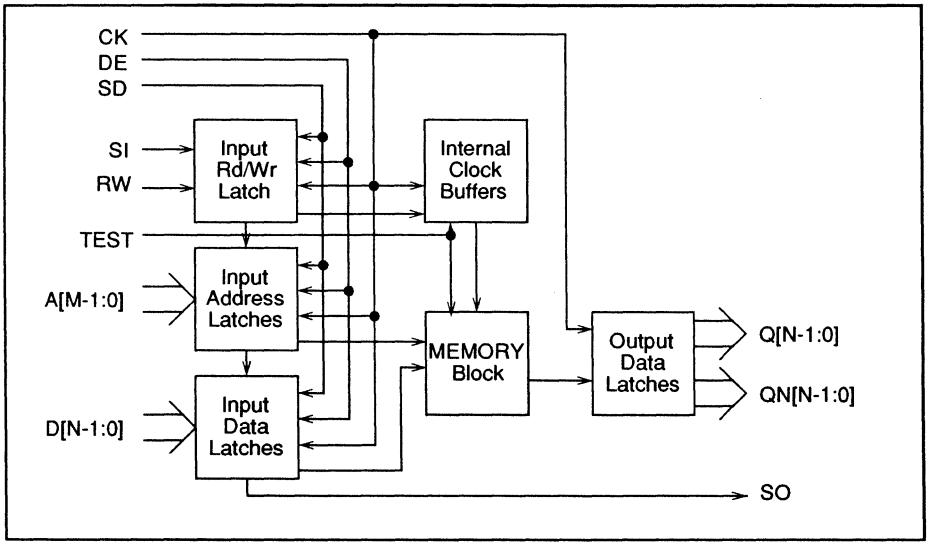
- Positive Edge-Triggered Input Data Latches with Minimum Set-Up Times
- Positive Edge-Triggered Address Latches with Minimum Set-Up Times
- Positive Edge-Triggered Read/ Write Latch with Minimum Set-Up Time
- Positive Edge-Triggered Output Data Latches with Minimum Propagation Delays
- Column and Row Decoding
- A Clock Generator that derives all necessary internal clocks from a single clock input.
- A scan-chain that internally connects all of the input latches.

RAMS1E can be customized with the following parameters:

Parameter	Description	Limits		
		Increment	Min	Max
N	Bits/Word	1	2	32
M	Address Bits	1	3	10
W	Words	8	8	1,024

8

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A[M-1:0], D[N-1:0], RW, CK, SI, DE, SD, TEST;

OUTPUTS: Q[N-1:0], QN[N-1:0], SO;

Functional Descriptions

Inputs

A[M-1:0]	Address In (A0 = LSB)
D[N-1:0]	Data In
RW	Read/Write - (Read = '1')
CK	Clock
SI	Scan-In Data
DE	Data Enable - (Active High)
SD	Select Data - (Active High)
TEST	Test Mode - (Active Low)

Outputs

Q[N-1:0]	Data Out
QN[N-1:0]	Complement Data Out
SO	Scan-Out Data

CHARACTERISTICS

The parameters N, M and W can be used to estimate the characteristics for a RAMS1E that is W words X N bits per word with M address bits.

Parameter	Value	Unit
Number of Transistors	288 + 72M + 200N + (34 + M)W/8 + 6NW	
Height	850 + 5W	µ
Width	322 + 75.75N	µ
Worst Case Power	$(26.3+3.1M+0.11W+4.3N+0.0088NW+0.0044MW)VDD^2F/1,000$*	mW
Input Capacitance:		
A[M-1:0]	0.09	pF
D[N-1:0]	0.09	pF
RW	0.09	pF
CK	0.23 + 0.23N + 0.08M	pF
SI	0.10	pF
DE	0.26 + 0.18N	pF
SD	0.43 + 0.16N + 0.16M	pF
TEST	0.22 + 0.14N	pF
Output Capacitance:		
Q[N-1:0]	0.29	pF
QN[N-1:0]	0.30	pF
SO	0.34	pF

* VDD = the power supply voltage in Volts and F = the clock frequency in MHz.

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing				
Symbol	From INPUT	To OUTPUT	Intrinsic (ns)	Extrinsic (ns/pF)
QRF	CK↑	Q[N-1:0]↑	2.0* 40.0**	0.6 0.6
	CK↑	Q[N-1:0]↓	2.0* 40.0**	0.3 0.3
	CK↑	QN[N-1:0]↑	2.0* 40.0**	0.6 0.6
	CK↑	QN[N-1:0]↓	2.0* 40.0**	0.3 0.3
SORF	CK↑	SO↑	5.0	2.0
	CK↑	SO↓	7.0	2.0

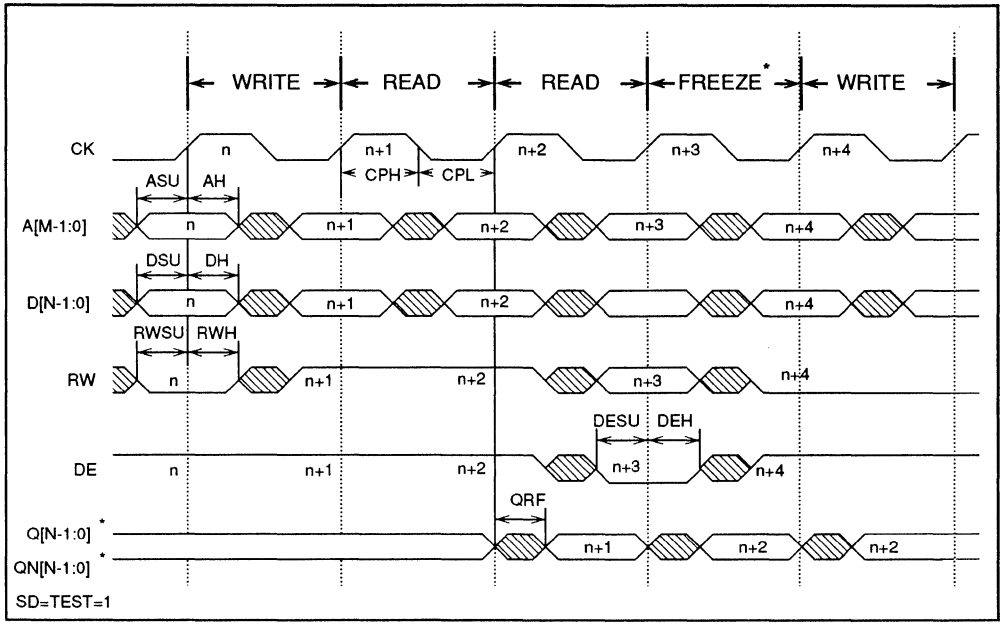
* While not in the Scan-Test mode. Additionally, in situations where the actual clock pulse width low (call it PWL) is less than (CPL+11)ns, then add (CPL+11-PWL)ns. CPL is the minimum clock pulse low as given in the Timing Requirements table.

** During Scan-Testing Only

8

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing		
Symbol	Description	Value(ns)
CPH	Minimum Clock Pulse High	10+N/8+(2+N/8)(W-256)/ 768
CPL	Minimum Clock Pulse Low	10+N/8+(2+N/8)(W-256)/ 768
ASU	Minimum Address Setup before CK↑	0.0
AH	Minimum Address Hold after CK↑	0.0
DSU	Minimum Data Setup before CK↑	3.0
DH	Minimum Data Hold after CK↑	0.0
RWSU	Minimum Read/Write Setup before CK↑	3.0
RWH	Minimum Read/Write Hold after CK↑	0.0
SISU	Minimum Scan-In Data Setup before CK↑	3.0
SIH	Minimum Scan-In Data Hold after CK↑	0.0
DESU	Minimum Data Enable Setup before CK↑	3.0
DEH	Minimum Data Enable Hold after CK↑	0.0
SDSU	Minimum Select Data Setup before CK↑	5.0 + 0.5N
SDH	Minimum Select Data Hold after CK↑	0.0

FUNCTIONAL MODE TIMING DIAGRAM



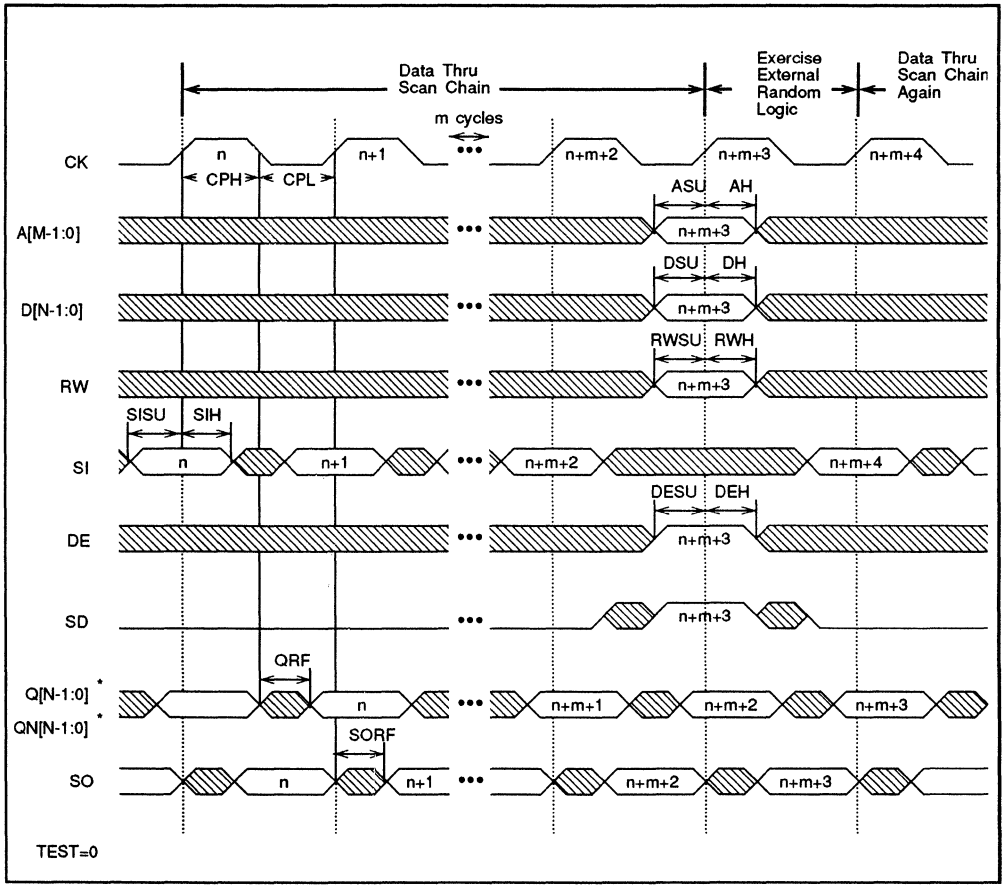
n=nth cycle number.

*A freeze cycle is executed when DE is low and SD is high. This cycle is provided as a convenience for freezing the RAMS1E. It can be applied anywhere or not at all. During this cycle information at inputs A[M-1:0], D[N-1:0], and RW is ignored. Instead, the information that was clocked in by CK in the previous cycle is reclocked and reused.

**Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ output is continuously available during subsequent WRITE operations.

8

SCAN TEST MODE TIMING DIAGRAM



n=nth cycle number.

*For the scan-testing mode, TEST is set low to place RAMS1E in a pseudo-transparent mode where the word addressed is simultaneously written and read. Thus, the input data, clocked in on the rising edge of CK, passes to the outputs Q and QN after CK goes low. With RAMS1E being pseudo-transparent in this mode, the random logic to RAMS1E can be more easily controlled and observed.

**For the scan-testing mode, CK should be run at one-tenth of the normal functional mode frequency.

FUNCTIONAL OPERATION

Scan Chain

During LSSD the faults in the external random logic around the RAMS1E are tested. Only the input latches are connected together to form a scan chain; the output latches are by-passed to allow quick access to the external random logic connected at the outputs. In terms of the primary inputs for the input latches, the following specifies the ordering of the scan chain:

A[0:M-1], D[0:P-1], RW, D[P:N-1]

where P (= N/2) is rounded up to the nearest integer.

Mode Control

Functional/Scan-Testing Mode Control					
DE	SD	TEST	Allowed*	Mode	State
1	1	1	Yes	Functional	Normal
0	1	1	Yes	Functional	Freeze
1	0	1	No	Functional	Data Scanning with RW confusion
0	0	1	No	Functional	Data Scanning with RW confusion
1	1	0	Yes	Scan Test	Random Logic Clock
0	1	0	No	Scan Test	Freeze
1	0	0	Yes	Scan Test	Data Scanning
0	0	0	Yes	Scan Test	Data Scanning

*The disallowed states can be simulated, but they serve no useful purpose and should be avoided.

USER NOTES:

1) Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ outputs are continuously available during subsequent WRITE operations.
2) No glitches are allowed on the clock input CK. If the minimum clock pulse widths (high or low) are violated, any of the internal memory contents can be corrupted.
3) If the setup and hold time specs on the address inputs are violated, any of the internal memory contents can be corrupted.
4) The scan-test circuitry is present in the RAMS1E to support the scan-testing of the surrounding logic, and not the RAMS1E itself. In fact, the RAMS1E is constructed so that it effectively disappears from the chip during scan-testing.
5) The scan output SO is basically the output from the last latch in the scan chain, which is the latch for the D[N-1:N-1] input. Thus, in the functional mode, SO will follow the D[N-1:N-1] input.

FUNCTIONAL DESCRIPTION AND FEATURES

RAMS1F is a parameterized static RAM function supported by automatic layout generation software. The layout of the RAMS1F is implemented as a custom, pitch-matched array of cells that is very area-efficient.

The RAMS1F has been designed specifically for use on standard cell chips that use a scan-testing strategy and has overhead circuitry already built-in including:

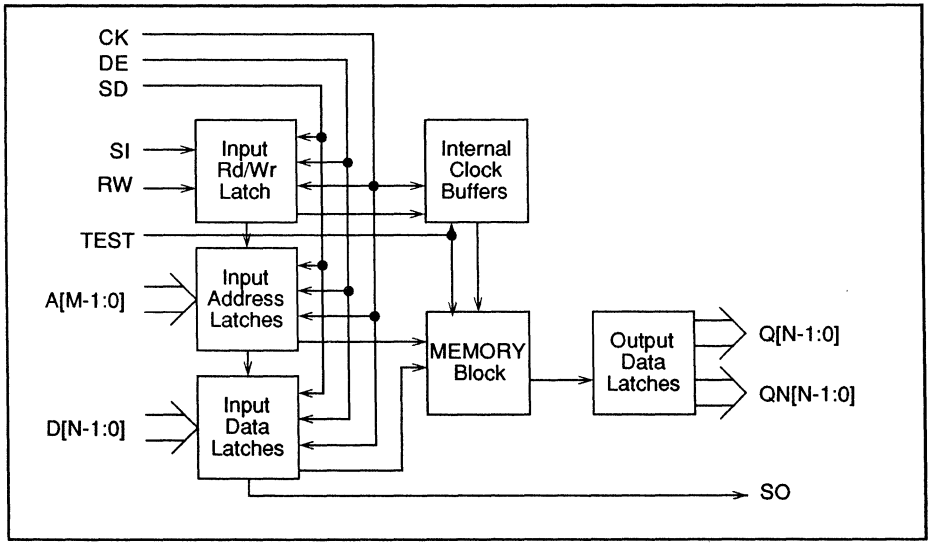
- Positive Edge-Triggered Input Data Latches with Minimum Set-Up Times
- Positive Edge-Triggered Address Latches with Minimum Set-Up Times
- Positive Edge-Triggered Read/ Write Latch with Minimum Set-Up Time
- Negative Edge-Triggered Output Data Latches with Relaxed Propagation Delays
- Column and Row Decoding
- A Clock Generator that derives all necessary internal clocks from a single clock input.
- A scan-chain that internally connects all of the input latches.

RAMS1F can be customized with the following parameters:

Parameter	Description	Limits		
		Increment	Min	Max
N	Bits/Word	1	2	32
M	Address Bits	1	3	10
W	Words	8	8	1,024

8

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A[M-1:0], D[N-1:0], RW, CK, SI, DE, SD, TEST;

OUTPUTS: Q[N-1:0], QN[N-1:0], SO;

Functional Descriptions

Inputs

A[M-1:0]	Address In (A0 = LSB)
D[N-1:0]	Data In
RW	Read/Write - (Read = '1')
CK	Clock
SI	Scan-In Data
DE	Data Enable - (Active High)
SD	Select Data - (Active High)
TEST	Test Mode - (Active Low)

Outputs

Q[N-1:0]	Data Out
QN[N-1:0]	Complement Data Out
SO	Scan-Out Data

CHARACTERISTICS

The parameters **N**, **M** and **W** can be used to estimate the characteristics for a RAMS1F that is **W** words X **N** bits per word with **M** address bits.

Parameter	Value	Unit
Number of Transistors	288 + 72M + 184N + (34 + M)W/8 + 6NW	
Height	820 + 5W	μ
Width	322 + 75.75N	μ
Worst Case Power	$(26.3+3.1M+0.11W+3.9N+0.0088NW+0.0044MW)VDD^2F/1{,}000$*	mW
Input Capacitance:		
A[M-1:0]	0.09	pF
D[N-1:0]	0.09	pF
RW	0.09	pF
CK	0.23 + 0.08N + 0.08M	pF
SI	0.10	pF
DE	0.26 + 0.18N	pF
SD	0.43 + 0.16N + 0.16M	pF
TEST	0.18	pF
Output Capacitance:		
Q[N-1:0]	0.27	pF
QN[N-1:0]	0.27	pF
SO	0.34	pF

* **VDD** = the power supply voltage in Volts and **F** = the clock frequency in MHz.

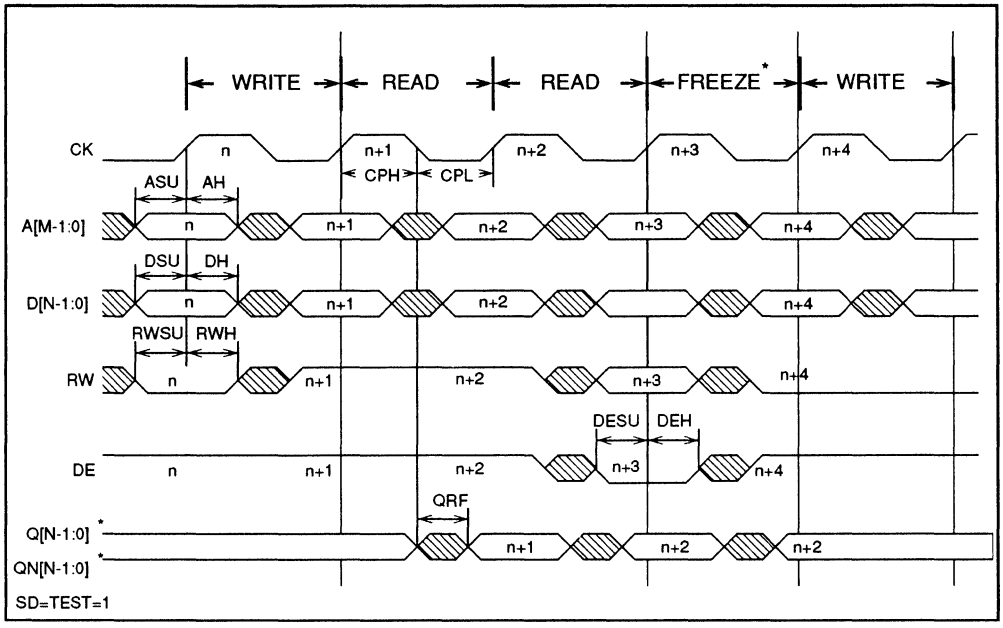
SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing				
Symbol	From INPUT	To OUTPUT	Intrinsic (ns)	Extrinsic (ns/pF)
QRF	CK↑	Q[N-1:0]↑	21+N/8+(2+N/8)(W-256)/ 768* 40.0**	0.6
	CK↑	Q[N-1:0]↓	21+N/8+(2+N/8)(W-256)/ 768* 40.0**	0.3
	CK↑	QN[N-1:0]↑	21+N/8+(2+N/8)(W-256)/ 768* 40.0**	0.6
	CK↑	QN[N-1:0]↓	21+N/8+(2+N/8)(W-256)/ 768* 40.0**	0.3
SORF	CK↑	SO↑	5.0	2.0
	CK↑	SO↓	7.0	2.0

* While not in the Scan-Test mode.

** During Scan-Testing Only.

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing		
Symbol	Description	Value (ns)
CPH	Minimum Clock Pulse High	10+N/8+(2+N/8)(W-256)/ 768
CPL	Minimum Clock Pulse Low	10+N/8+(2+N/8)(W-256)/ 768
ASU	Minimum Address Setup before CK↑	3.0
AH	Minimum Address Hold after CK↑	0.0
DSU	Minimum Data Setup before CK↑	3.0
DH	Minimum Data Hold after CK↑	0.0
RWSU	Minimum Read/Write Setup before CK↑	3.0
RWH	Minimum Read/Write Hold after CK↑	0.0
SISU	Minimum Scan-In Data Setup before CK↑	3.0
SIH	Minimum Scan-In Data Hold after CK↑	0.0
DESU	Minimum Data Enable Setup before CK↑	3.0
DEH	Minimum Data Enable Hold after CK↑	0.0
SDSU	Minimum Select Data Setup before CK↑	5.0 + 0.5N
SDH	Minimum Select Data Hold after CK↑	0.0

FUNCTIONAL MODE TIMING DIAGRAM



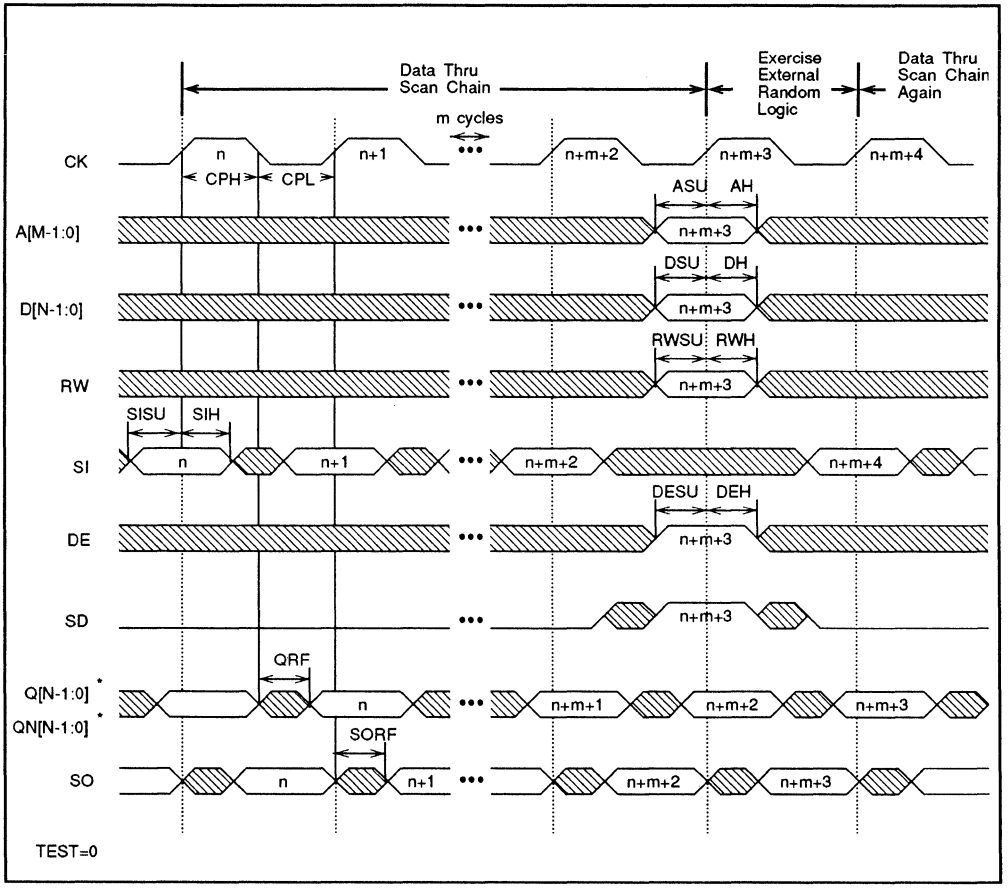
n=nth cycle number.

*A freeze cycle is executed when DE is low and SD is high. This cycle is provided as a convenience for freezing the RAMS1F. It can be applied anywhere or not at all. During this cycle information at inputs A[M-1:0], D[N-1:0], and RW is ignored. Instead, the information that was clocked in by CK in the previous cycle is reclocked and reused.

**Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ output is continuously available during subsequent WRITE operations.

8

SCAN TEST MODE TIMING DIAGRAM



n=nth cycle number.

*For the scan-testing mode, TEST is set low to place RAMS1F in a pseudo-transparent mode where the word addressed is simultaneously written and read. Thus, the input data, clocked in on the rising edge of CK, passes to the outputs Q and QN after CK goes low. With RAMS1F being pseudo-transparent in this mode, the random logic to RAMS1F can be more easily controlled and observed.

**For the scan-testing mode, CK should be run at one-tenth of the normal functional mode frequency.

FUNCTIONAL OPERATION

Scan Chain

During LSSD the faults in the external random logic around the RAMS1F are tested. Only the input latches are connected together to form a scan chain; the output latches are by-passed to allow quick access to the external random logic connected at the outputs. In terms of the primary inputs for the input latches, the following specifies the ordering of the scan chain:

A[0:M-1], D[0:P-1], RW, D[P:N-1]

where P (= N/2) is rounded up to the nearest integer.

RAMS1F Mode Control

Functional/Scan-Testing Mode Control					
DE	SD	TEST	Allowed*	Mode	State
1	1	1	Yes	Functional	Normal
0	1	1	Yes	Functional	Freeze
1	0	1	No	Functional	Data Scanning with RW confusion
0	0	1	No	Functional	Data Scanning with RW confusion
1	1	0	Yes	Scan Test	Random Logic Clock
0	1	0	No	Scan Test	Freeze
1	0	0	Yes	Scan Test	Data Scanning
0	0	0	Yes	Scan Test	Data Scanning

*The disallowed states can be simulated, but they serve no useful purpose and should be avoided.

USER NOTES

1) Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ outputs are continuously available during subsequent WRITE operations.
2) No glitches are allowed on the clock input CK. If the minimum clock pulse widths (high or low) are violated, any of the internal memory contents can be corrupted.
3) If the setup and hold time specs on the address inputs are violated, any of the internal memory contents can be corrupted.
4) The scan-test circuitry is present in the RAMS1F to support the scan-testing of the surrounding logic, and not the RAMS1F itself. In fact, the RAMS1F is constructed so that it effectively disappears from the chip during scan-testing.

FUNCTIONAL DESCRIPTION AND FEATURES

RAMS2A is a parameterized static RAM function supported by automatic layout generation software. The layout of the RAMS2A is implemented as a custom, pitch-matched array of cells that is very area-efficient.

The RAMS2A has been designed specifically for use on standard cell chips and has overhead circuitry already built-in including:

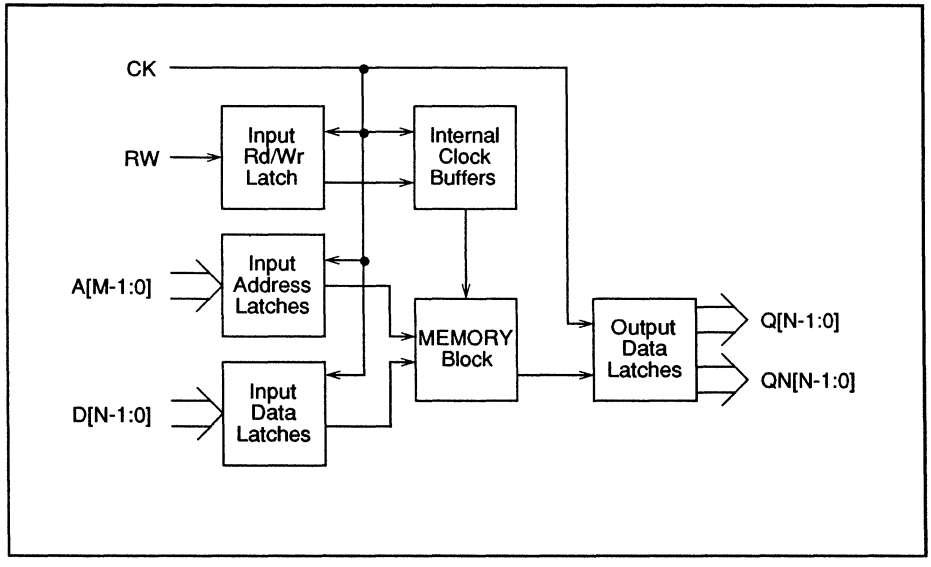
- Negative Edge-Triggered Input Data Latches with Minimum Set-Up Times
- Negative Edge-Triggered Address Latches with Minimum Set-Up Times
- Negative Edge-Triggered Read/ Write Latch with Minimum Set-Up Times
- Negative Edge-Triggered Output Latches with Minimum Propagation Delays
- Column and Row Decoding
- A Clock Generator that derives all necessary internal clocks from a single clock input.

RAMS2A can be customized with the following parameters:

Parameter	Description	Limits		
		Increment	Min	Max
N	Bits/Word	1	2	32
M	Address Bits	1	3	10
W	Words	8	8	1,024

8

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A[M-1:0], D[N-1:0], RW, CK;
OUTPUTS: Q[N-1:0], QN[N-1:0];

Functional Descriptions

Inputs

A[M-1:0]	Address In (A0 = LSB)
D[N-1:0]	Data In
RW	Read/Write - (Read = '1')
CK	Clock

Outputs

Q[N-1:0]	Data Out
QN[N-1:0]	Complement Data Out

CHARACTERISTICS

The parameters **N**, **M** and **W** can be used to estimate the characteristics for a RAMS2A that is **W** words X **N** bits per word with **M** address bits.

Parameter	Value	Unit
Number of Transistors	238 + 56M + 170N + (34 + M)W/8 + 6NW	
Height	735 + 5W	µ
Width	322 + 75.75N	µ
Worst Case Power	$(26.0+2.4M+0.11W+3.9N+0.0088NW+0.0044MW)VDD^2F/1{,}000$*	mW
Input Capacitance:		
A[M-1:0]	0.16	pF
D[N-1:0]	0.16	pF
RW	0.16	pF
CK	0.40 + 0.24N + 0.08M	pF
Output Capacitance:		
Q[N-1:0]	0.30	pF
QN[N-1:0]	0.29	pF

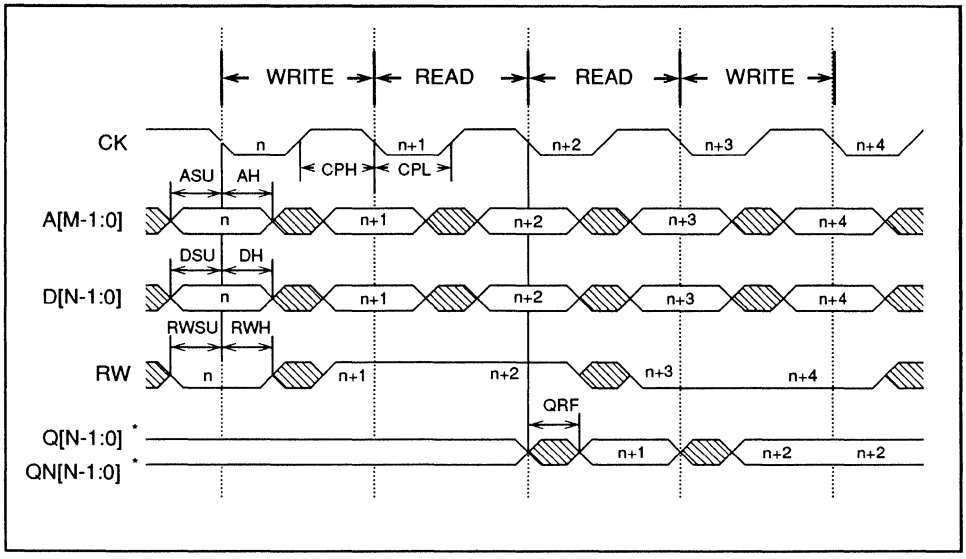
* VDD = the power supply voltage in Volts and F = the clock frequency in MHz.

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing				
Symbol	From INPUT	To OUTPUT	Intrinsic (ns)	Extrinsic (ns/pF)
QRF	CK↓	Q[N-1:0]↑	2.0*	0.6
	CK↓	Q[N-1:0]↓	2.0*	0.3
	CK↓	QN[N-1:0]↑	2.0*	0.6
	CK↓	QN[N-1:0]↓	2.0*	0.3

* In situations where the actual clock pulse width high (call it PWH) is less than (CPH+11)ns, then add (CPH+11-PWH)ns. CPH is the minimum clock pulse high as given in the Timing Requirements table.

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing		
Symbol	Description	Value (ns)
CPH	Minimum Clock Pulse High	10+N/8+(2+N/8)(W-256)/768
CPL	Minimum Clock Pulse Low	10+N/8+(2+N/8)(W-256)/768
ASU	Minimum Address Setup before CK↓	3.0
AH	Minimum Address Hold after CK↓	0.0
DSU	Minimum Data Setup before CK↓	3.0
DH	Minimum Data Hold after CK↓	0.0
RWSU	Minimum Read/Write Setup before CK↓	3.0
RWH	Minimum Read/Write Hold after CK↓	0.0

TIMING DIAGRAM



n=nth cycle number.

*Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ output is continuously available during subsequent WRITE operations.

8

USER NOTES

1) Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ outputs are continuously available during subsequent WRITE operations.
2) No glitches are allowed on the clock input CK. If the minimum clock pulse widths (high or low) are violated, any of the internal memory contents can be corrupted.
3) If the setup and hold time specs on the address inputs are violated, any of the internal memory contents can be corrupted.

FUNCTIONAL DESCRIPTION AND FEATURES

RAMS2B is a parameterized static RAM function supported by automatic layout generation software. The layout of the RAMS2B is implemented as a custom, pitch-matched array of cells that is very area-efficient.

The RAMS2B has been designed specifically for use on standard cell chips and has overhead circuitry already built-in including:

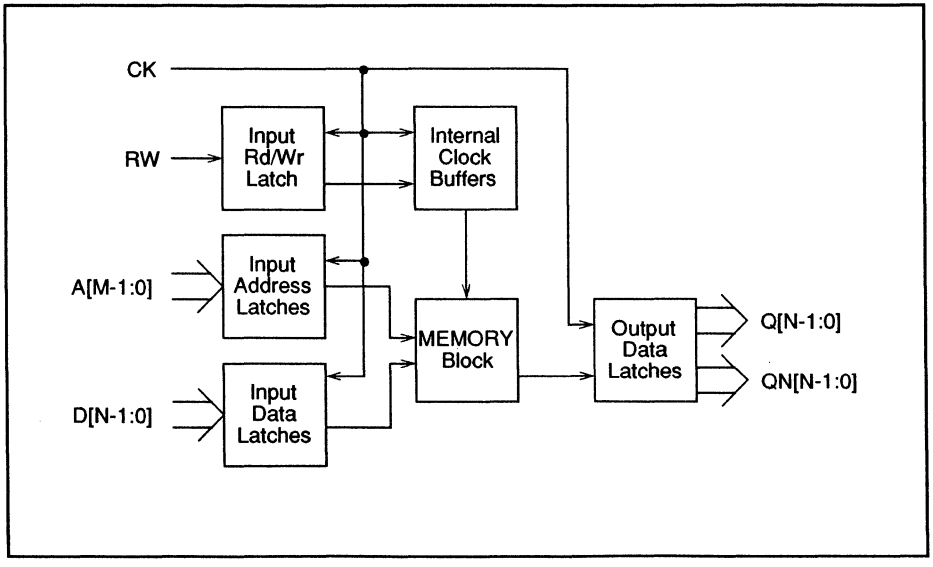
- Positive Edge-Triggered Input Data Latches with Relaxed Set-Up Times
- Positive Edge-Triggered Address Latches with Relaxed Set-Up Times
- Positive Edge-Triggered Read/ Write Latch with Relaxed Set-Up Time
- Negative Edge-Triggered Output Data Latches with Minimum Propagation Delays
- Column and Row Decoding
- A Clock Generator that derives all necessary internal clocks from a single clock input.

RAMS2B can be customized with the following parameters:

Parameter	Description	Limits		
		Increment	Min	Max
N	Bits/Word	1	2	32
M	Address Bits	1	3	10
W	Words	8	8	1,024

8

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A[M-1:0], D[N-1:0], RW, CK;
OUTPUTS: Q[N-1:0], QN[N-1:0];

Functional Descriptions

Inputs

A[M-1:0]	Address In (A0 = LSB)
D[N-1:0]	Data In
RW	Read/Write - (Read = '1')
CK	Clock

Outputs

Q[N-1:0]	Data Out
QN[N-1:0]	Complement Data Out

CHARACTERISTICS

The parameters **N**, **M** and **W** can be used to estimate the characteristics for a RAMS2B that is W words X N bits per word with M address bits.

Parameter	Value	Unit
Number of Transistors	230 + 48**M** + 162**N** + (34 + **M**)**W**/8 + 6**NW**	
Height	705 + 5**W**	µ
Width	322 + 75.75**N**	µ
Worst Case Power	(25.5+2.1**M**+0.11**W**+3.7**N**+0.0088**NW**+0.0044**MW**)**VDD**^{2}**F**/1,000*	mW
Input Capacitance:		
A[M-1:0]	0.16	pF
D[N-1:0]	0.16	pF
RW	0.16	pF
CK	0.40 + 0.24**N** + 0.08**M**	pF
Output Capacitance:		
Q[N-1:0]	0.30	pF
QN[N-1:0]	0.29	pF

* **VDD** = the power supply voltage in Volts and **F** = the clock frequency in MHz.

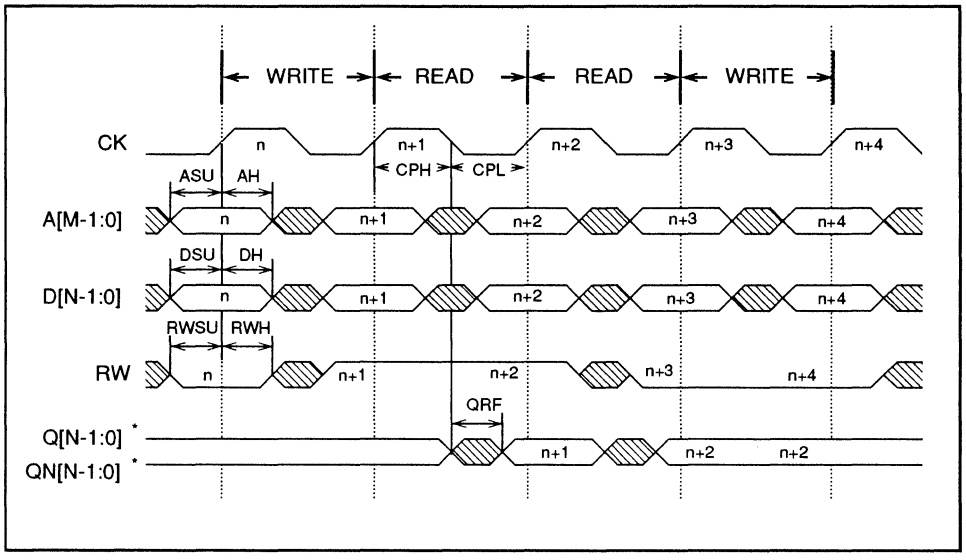
SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing				
Symbol	From INPUT	To OUTPUT	Intrinsic (ns)	Extrinsic (ns/pF)
QRF	CK↓	Q[N-1:0]↑	2.0*	0.6
	CK↓	Q[N-1:0]↓	2.0*	0.3
	CK↓	QN[N-1:0]↑	2.0*	0.6
	CK↓	QN[N-1:0]↓	2.0*	0.3

* In situations where the actual clock pulse width high (call it PWH) is less than (CPH+11)ns, then add (CPH+11-PWH)ns. CPH is the minimum clock pulse high as given in the Timing Requirements table.

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing		
Symbol	Description	Value (ns)
CPH	Minimum Clock Pulse High	10+N/8+(2+N/8)(W-256)/768
CPL	Minimum Clock Pulse Low	10+N/8+(2+N/8)(W-256)/768
ASU	Minimum Address Setup before CK↑	10.0
AH	Minimum Address Hold after CK↑	0.0
DSU	Minimum Data Setup before CK↑	10.0
DH	Minimum Data Hold after CK↑	0.0
RWSU	Minimum Read/Write Setup before CK↑	10.0
RWH	Minimum Read/Write Hold after CK↑	0.0

8

TIMING DIAGRAM



n=nth cycle number.

*Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ output is continuously available during subsequent WRITE operations.

USER NOTES

1) Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ outputs are continuously available during subsequent WRITE operations.
2) No glitches are allowed on the clock input CK. If the minimum clock pulse widths (high or low) are violated, any of the internal memory contents can be corrupted.
3) If the setup and hold time specs on the address inputs are violated, any of the internal memory contents can be corrupted.

8

FUNCTIONAL DESCRIPTION AND FEATURES

RAMS2C is a parameterized static RAM function supported by automatic layout generation software. The layout of the RAMS2C is implemented as a custom, pitch-matched array of cells that is very area-efficient.

The RAMS2C has been designed specifically for use on standard cell chips and has overhead circuitry already built-in including:

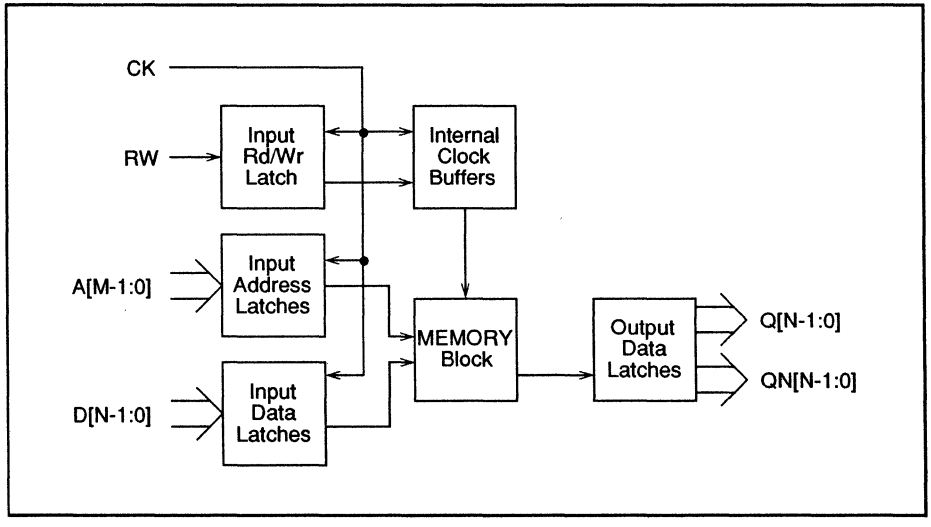
- Negative Edge-Triggered Input Data Latches with Minimum Set-Up Times
- Negative Edge-Triggered Address Latches with Minimum Set-Up Times
- Negative Edge-Triggered Read/ Write Latch with Minimum Set-Up Time
- Positive Edge-Triggered Output Data Latches with Relaxed Propagation Delays
- Column and Row Decoding
- A Clock Generator that derives all necessary internal clocks from a single clock input.

RAMS2C can be customized with the following parameters:

Parameter	Description	Limits		
		Increment	Min	Max
N	Bits/Word	1	2	32
M	Address Bits	1	3	10
W	Words	8	8	1,024

8

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A[M-1:0], D[N-1:0], RW, CK;
OUTPUTS: Q[N-1:0], QN[N-1:0];

Functional Descriptions

Inputs

A[M-1:0]	Address In (A0 = LSB)
D[N-1:0]	Data In
RW	Read/Write - (Read = '1')
CK	Clock

Outputs

Q[N-1:0]	Data Out
QN[N-1:0]	Complement Data Out

CHARACTERISTICS

The parameters **N**, **M** and **W** can be used to estimate the characteristics for a RAMS2C that is **W** words X **N** bits per word with **M** address bits.

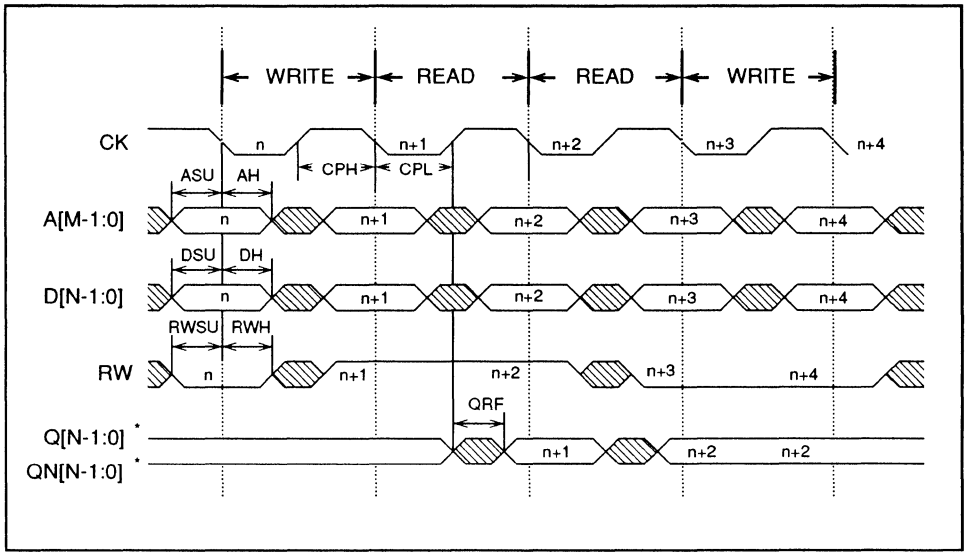
Parameter	Value	Unit
Number of Transistors	238 + 56M + 168N + (34 + M)W/8 + 6NW	
Height	730 + 5W	µ
Width	322 + 75.75N	µ
Worst Case Power	$(26.0+2.4M+0.11W+3.8N+0.0088NW+0.0044MW)VDD^2F/1{,}000$*	mW
Input Capacitance:		
A[M-1:0]	0.16	pF
D[N-1:0]	0.16	pF
RW	0.16	pF
CK	0.40 + 0.08N + 0.08M	pF
Output Capacitance:		
Q[N-1:0]	0.27	pF
QN[N-1:0]	0.27	pF

* VDD = the power supply voltage in Volts and F = the clock frequency in MHz.

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing				
Symbol	From INPUT	To OUTPUT	Intrinsic (ns)	Extrinsic (ns/pF)
QRF	CK↑	Q[N-1:0]↑	21+N/8+(2+N/8)(W-256)/ 768	0.6
	CK↑	Q[N-1:0]↓	21+N/8+(2+N/8)(W-256)/ 768	0.3
	CK↑	QN[N-1:0]↑	21+N/8+(2+N/8)(W-256)/ 768	0.6
	CK↑	QN[N-1:0]↓	21+N/8+(2+N/8)(W-256)/ 768	0.3

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing		
Symbol	Description	Value (ns)
CPH	Minimum Clock Pulse High	10+N/8+(2+N/8)(W-256)/ 768
CPL	Minimum Clock Pulse Low	10+N/8+(2+N/8)(W-256)/ 768
ASU	Minimum Address Setup before CK↓	3.0
AH	Minimum Address Hold after CK↓	0.0
DSU	Minimum Data Setup before CK↓	3.0
DH	Minimum Data Hold after CK↓	0.0
RWSU	Minimum Read/Write Setup before CK↓	3.0
RWH	Minimum Read/Write Hold after CK↓	0.0

TIMING DIAGRAM



n=nth cycle number.

*Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ output is continuously available during subsequent WRITE operations.

8

USER NOTES

1) Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ outputs are continuously available during subsequent WRITE operations.
2) No glitches are allowed on the clock input CK. If the minimum clock pulse widths (high or low) are violated, any of the internal memory contents can be corrupted.
3) If the setup and hold time specs on the address inputs are violated, any of the internal memory contents can be corrupted.

FUNCTIONAL DESCRIPTION AND FEATURES

RAMS2D is a parameterized static RAM function supported by automatic layout generation software. The layout of the RAMS2D is implemented as a custom, pitch-matched array of cells that is very area-efficient.

The RAMS2D has been designed specifically for use on standard cell chips and has overhead circuitry already built-in including:

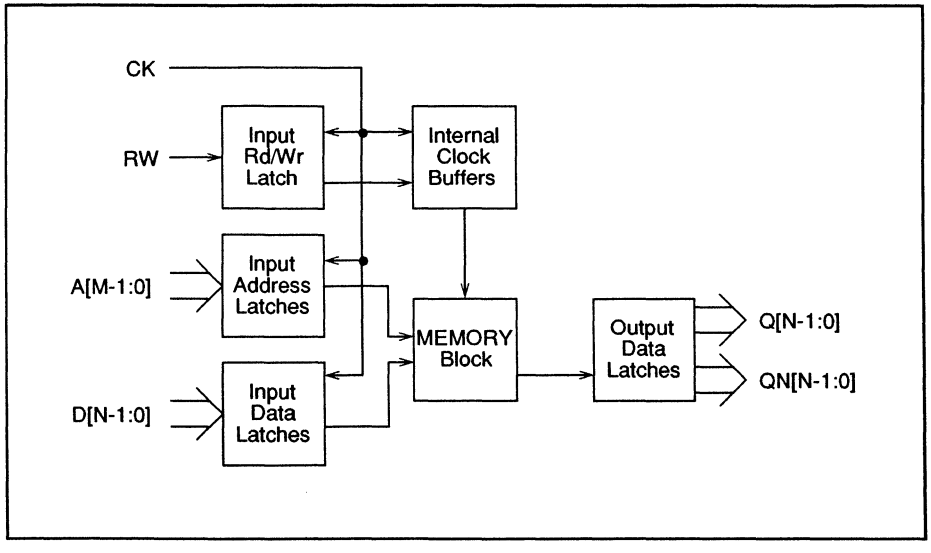
- Positive Edge-Triggered Input Data Latches with Relaxed Set-Up Times
- Positive Edge-Triggered Address Latches with Relaxed Set-Up Times
- Positive Edge-Triggered Read/ Write Latch with Relaxed Set-Up Time
- Positive Edge-Triggered Output Data Latches with Relaxed Propagation Delays
- Column and Row Decoding
- A Clock Generator that derives all necessary internal clocks from a single clock input.

RAMS2D can be customized with the following parameters:

Parameter	Description	Limits		
		Increment	Min	Max
N	Bits/Word	1	2	32
M	Address Bits	1	3	10
W	Words	8	8	1,024

8

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A[M-1:0], D[N-1:0], RW, CK;

OUTPUTS: Q[N-1:0], QN[N-1:0];

Functional Descriptions

Inputs

A[M-1:0]	Address In (A0 = LSB)
D[N-1:0]	Data In
RW	Read/Write - (Read = '1')
CK	Clock

Outputs

Q[N-1:0]	Data Out
QN[N-1:0]	Complement Data Out

CHARACTERISTICS

The parameters N, M and W can be used to estimate the characteristics for a RAMS2D that is W words X N bits per word with M address bits.

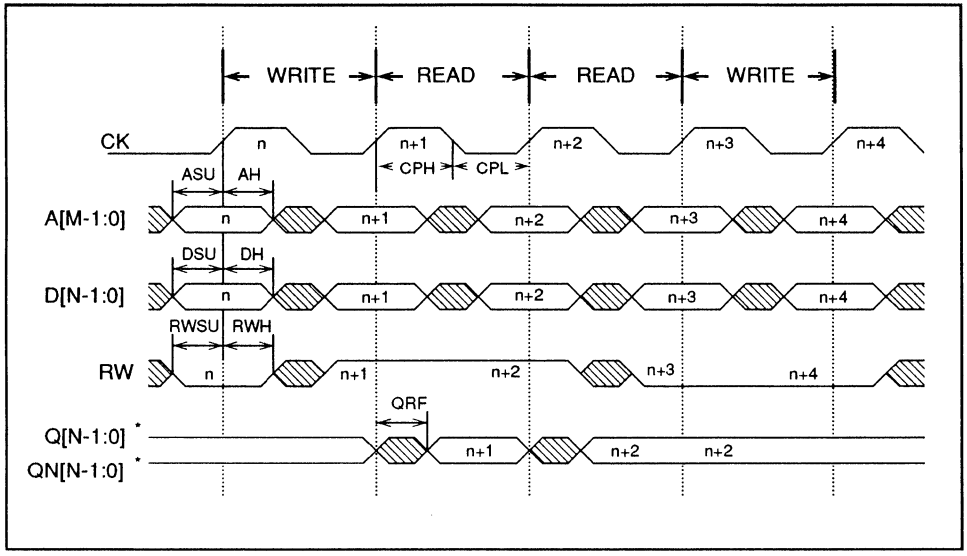
Parameter	Value	Unit
Number of Transistors	258 + 48M + 160N + (34 + M)W/8 + 6NW	
Height	700 + 5W	µ
Width	322 + 75.75N	µ
Worst Case Power	$(25.5+2.1M+0.11W+3.6N+0.0088NW+0.0044MW)VDD^2F/1,000$*	mW
Input Capacitance:		
A[M-1:0]	0.16	pF
D[N-1:0]	0.16	pF
RW	0.16	pF
CK	0.40 + 0.08N + 0.08M	pF
Output Capacitance:		
Q[N-1:0]	0.27	pF
QN[N-1:0]	0.27	pF

* VDD = the power supply voltage in Volts and F = the clock frequency in MHz.

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing				
Symbol	From INPUT	To OUTPUT	Intrinsic (ns)	Extrinsic (ns/pF)
QRF	CK↑	Q[N-1:0]↑	21+N/8+(2+N/8)(W-256)/ 768	0.6
	CK↑	Q[N-1:0]↓	21+N/8+(2+N/8)(W-256)/ 768	0.3
	CK↑	QN[N-1:0]↑	21+N/8+(2+N/8)(W-256)/ 768	0.6
	CK↑	QN[N-1:0]↓	21+N/8+(2+N/8)(W-256)/ 768	0.3

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing		
Symbol	Description	Value (ns)
CPH	Minimum Clock Pulse High	10+N/8+(2+N/8)(W-256)/ 768
CPL	Minimum Clock Pulse Low	10+N/8+(2+N/8)(W-256)/ 768
ASU	Minimum Address Setup before CK↑	10.0
AH	Minimum Address Hold after CK↑	0.0
DSU	Minimum Data Setup before CK↑	10.0
DH	Minimum Data Hold after CK↑	0.0
RWSU	Minimum Read/Write Setup before CK↑	10.0
RWH	Minimum Read/Write Hold after CK↑	0.0

TIMING DIAGRAM



n=nth cycle number.

*Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ output is continuously available during subsequent WRITE operations.

8

USER NOTES

1) Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ outputs are continuously available during subsequent WRITE operations.
2) No glitches are allowed on the clock input CK. If the minimum clock pulse widths (high or low) are violated, any of the internal memory contents can be corrupted.
3) If the setup and hold time specs on the address inputs are violated, any of the internal memory contents can be corrupted.

FUNCTIONAL DESCRIPTION AND FEATURES:

RAMS2E is a parameterized static RAM function supported by automatic layout generation software. The layout of the RAMS2E is implemented as a custom, pitch-matched array of cells that is very area-efficient.

The RAMS2E has been designed specifically for use on standard cell chips that use a scan-testing strategy and has overhead circuitry already built-in including:

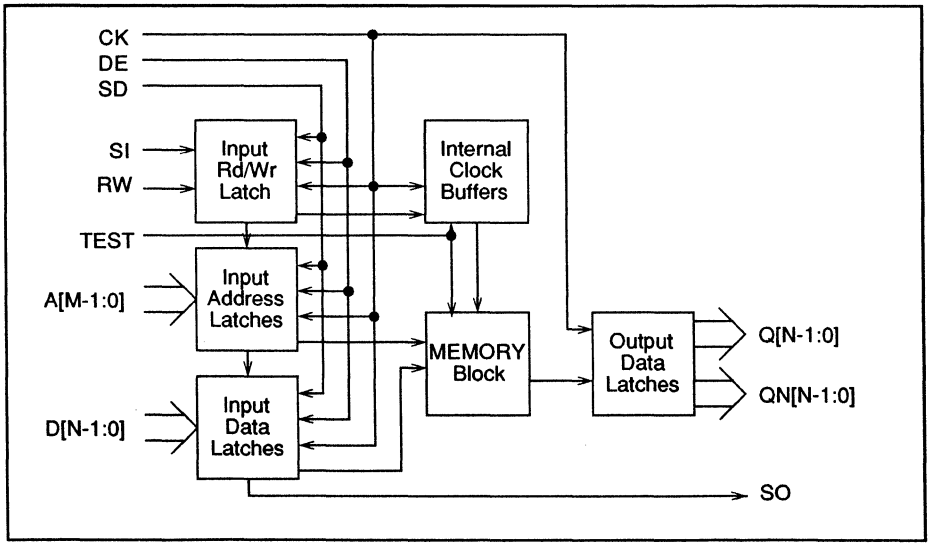
- Negative Edge-Triggered Input Data Latches with Minimum Set-Up Times
- Negative Edge-Triggered Address Latches with Minimum Set-Up Times
- Negative Edge-Triggered Read/ Write Latch with Minimum Set-Up Time
- Negative Edge-Triggered Output Data Latches with Minimum Propagation Delays
- Column and Row Decoding
- A Clock Generator that derives all necessary internal clocks from a single clock input.
- A scan-chain that internally connects all of the input latches.

RAMS2E can be customized with the following parameters:

Parameter	Description	Limits		
		Increment	Min	Max
N	Bits/Word	1	2	32
M	Address Bits	1	3	10
W	Words	8	8	1,024

8

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A[M-1:0], D[N-1:0], RW, CK, SI, DE, SD, TEST;

OUTPUTS: Q[N-1:0], QN[N-1:0], SO;

Functional Descriptions

Inputs

A[M-1:0]	Address In (A0 = LSB)
D[N-1:0]	Data In
RW	Read/Write - (Read = '1')
CK	Clock
SI	Scan-In Data
DE	Data Enable - (Active High)
SD	Select Data - (Active High)
TEST	Test Mode - (Active Low)

Outputs

Q[N-1:0]	Data Out
QN[N-1:0]	Complement Data Out
SO	Scan-Out Data

CHARACTERISTICS

The parameters **N**, **M** and **W** can be used to estimate the characteristics for a RAMS2E that is W words X N bits per word with M address bits.

Parameter	Value	Unit
Number of Transistors	286 + 72M + 200N + (34 + M)W/8 + 6NW	
Height	850 + 5W	µ
Width	322 + 75.75N	µ
Worst Case Power	$(26.3+3.1M+0.11W+4.3N+0.0088NW+0.0044MW)VDD^2F/1{,}000$*	mW
Input Capacitance:		
A[M-1:0]	0.09	pF
D[N-1:0]	0.09	pF
RW	0.09	pF
CK	0.23 + 0.23N + 0.08M	pF
SI	0.10	pF
DE	0.26 + 0.18N	pF
SD	0.43 + 0.16N + 0.16M	pF
TEST	0.22 + 0.14N	pF
Output Capacitance:		
Q[N-1:0]	0.29	pF
QN[N-1:0]	0.30	pF
SO	0.34	pF

* VDD = the power supply voltage in Volts and F = the clock frequency in MHz.

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing				
Symbol	From INPUT	To OUTPUT	Intrinsic (ns)	Extrinsic (ns/pF)
QRF	CK↓	Q[N-1:0]↑	2.0* 40.0**	0.6
	CK↓	Q[N-1:0]↓	2.0* 40.0**	0.3
	CK↓	QN[N-1:0]↑	2.0* 40.0**	0.6
	CK↓	QN[N-1:0]↓	2.0* 40.0**	0.3
SORF	CK↓	SO↑	5.0	2.0
	CK↓	SO↓	7.0	2.0

* While not in the Scan-Test mode. Additionally, in situations where the actual clock pulse width high (call it PWH) is less than (CPH+11)ns, then add (CPL+11-PWH)ns. CPH is the minimum clock pulse high as given in the Timing Requirements table.

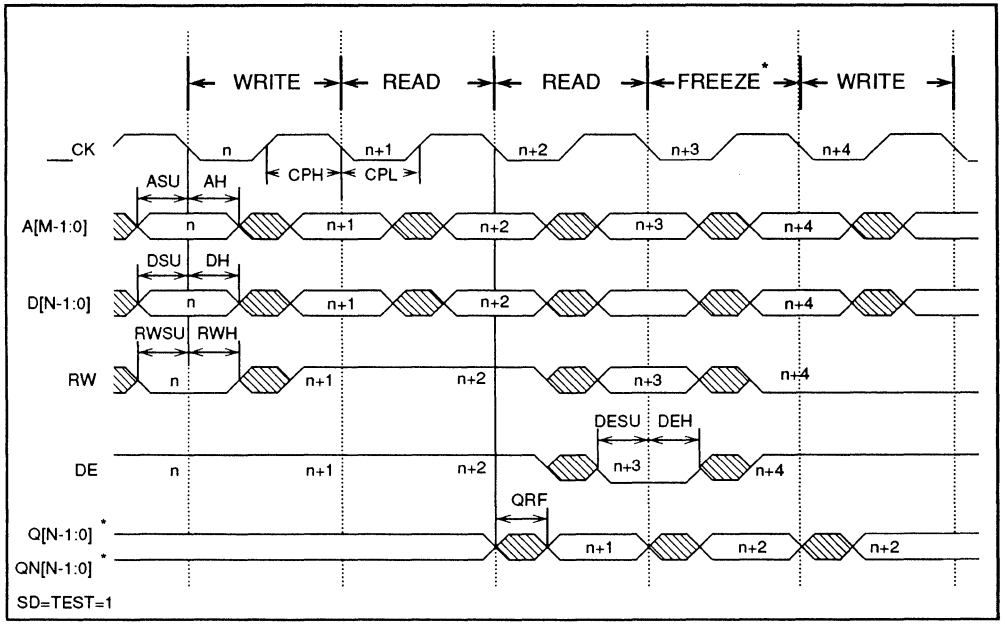
** During Scan-Testing Only.

8

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing		
Symbol	Description	Value(ns)
CPH	Minimum Clock Pulse High	10+N/8+(2+N/8)(W-256)/ 768
CPL	Minimum Clock Pulse Low	10+N/8+(2+N/8)(W-256)/ 768
ASU	Minimum Address Setup before CK↓	3.0
AH	Minimum Address Hold after CK↓	0.0
DSU	Minimum Data Setup before CK↓	3.0
DH	Minimum Data Hold after CK↓	0.0
RWSU	Minimum Read/Write Setup before CK↓	3.0
RWH	Minimum Read/Write Hold after CK↓	0.0
SISU	Minimum Scan-In Data Setup before CK↓	3.0
SIH	Minimum Scan-In Data Hold after CK↓	0.0
DESU	Minimum Data Enable Setup before CK↓	3.0
DEH	Minimum Data Enable Hold after CK↓	0.0
SDSU	Minimum Select Data Setup before CK↓	5.0 + 0.5N
SDH	Minimum Select Data Hold after CK↓	0.0

TIMING DIAGRAM:

Functional Mode



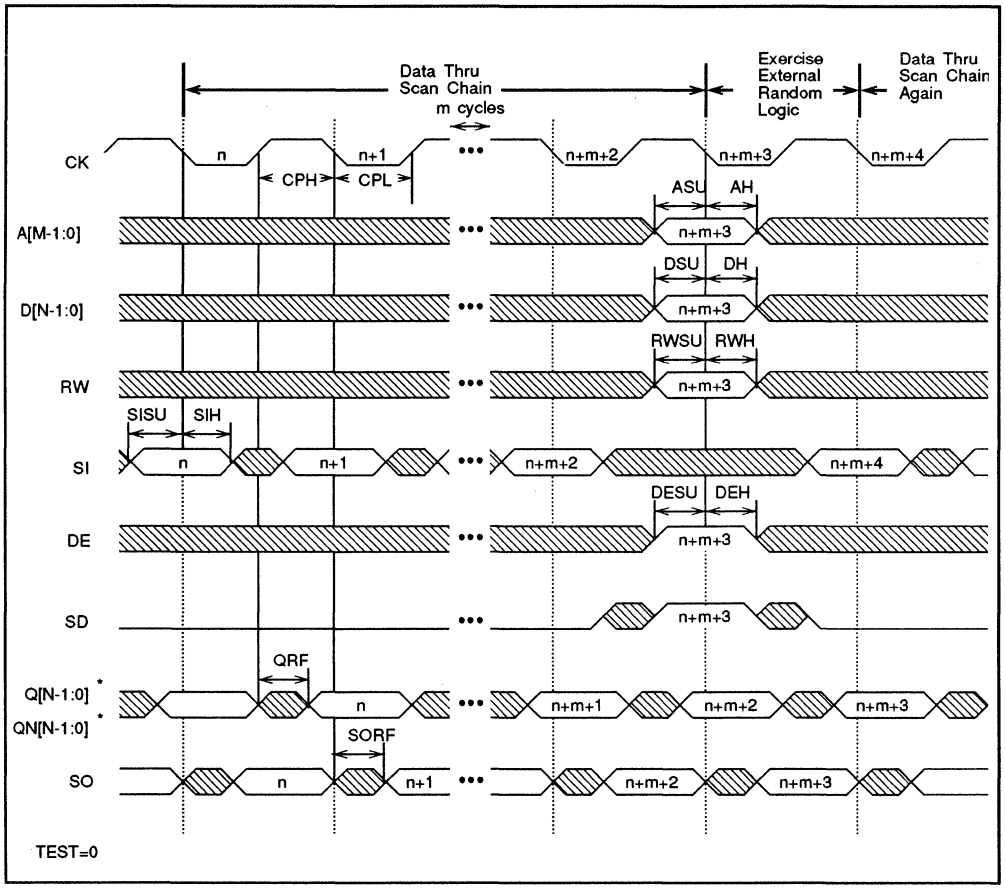
n=nth cycle number.

*A freeze cycle is executed when DE is low and SD is high. This cycle is provided as a convenience for freezing the RAMS2E. It can be applied anywhere or not at all. During this cycle information at inputs A[M-1:0], D[N-1:0], and RW is ignored. Instead, the information that was clocked in by CK in the previous cycle is reclocked and reused.

**Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ output is continuously available during subsequent WRITE operations.

8

SCAN TEST MODE TIMING DIAGRAM



n=nth cycle number.

*For the scan-testing mode, TEST is set low to place RAMS2E in a pseudo-transparent mode where the word addressed is simultaneously written and read. Thus, the input data, clocked in on the falling edge of CK, passes to the outputs Q and QN after CK goes high. With RAMS2E being pseudo-transparent in this mode, the random logic to RAMS2E can be more easily controlled and observed.

**For the scan-testing mode, CK should be run at one-tenth of the normal functional mode frequency.

FUNCTIONAL OPERATION

SCAN CHAIN

During LSSD the faults in the external random logic around the RAMS2E are tested. Only the input latches are connected together to form a scan chain; the output latches are by-passed to allow quick access to the external random logic connected at the outputs. In terms of the primary inputs for the input latches, the following specifies the ordering of the scan chain:

A[0:M-1], D[0:P-1], RW, D[P:N-1]

where P (= N/2) is rounded up to the nearest integer.

RAMS2E Mode Control

Functional/Scan-Testing Mode Control					
DE	SD	TEST	Allowed*	Mode	State
1	1	1	Yes	Functional	Normal
0	1	1	Yes	Functional	Freeze
1	0	1	No	Functional	Data Scanning with RW confusion
0	0	1	No	Functional	Data Scanning with RW confusion
1	1	0	Yes	Scan Test	Random Logic Clock
0	1	0	No	Scan Test	Freeze
1	0	0	Yes	Scan Test	Data Scanning
0	0	0	Yes	Scan Test	Data Scanning

*The disallowed states can be simulated, but they serve no useful purpose and should be avoided.

USER NOTES

1) Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ outputs are continuously available during subsequent WRITE operations.
2) No glitches are allowed on the clock input CK. If the minimum clock pulse widths (high or low) are violated, any of the internal memory contents can be corrupted.
3) If the setup and hold time specs on the address inputs are violated, any of the internal memory contents can be corrupted.
4) The scan-test circuitry is present in the RAMS2E to support the scan-testing of the surrounding logic, and not the RAMS2E itself. In fact, the RAMS2E is constructed so that it effectively disappears from the chip during scan-testing.

FUNCTIONAL DESCRIPTION AND FEATURES:

RAMS2F is a parameterized static RAM function supported by automatic layout generation software. The layout of the RAMS2F is implemented as a custom, pitch-matched array of cells that is very area-efficient.

The RAMS2F has been designed specifically for use on standard cell chips that use a scan-testing strategy and has overhead circuitry already built-in including:

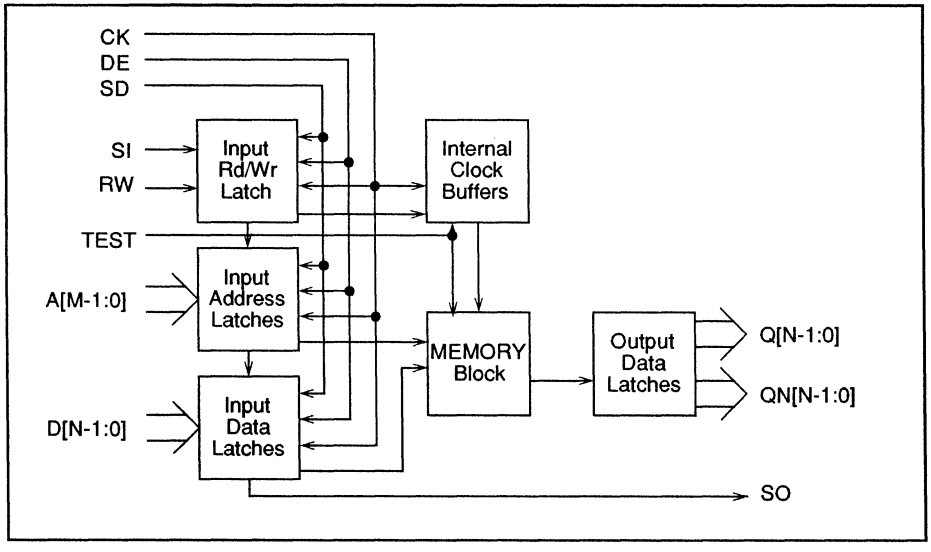
- Negative Edge-Triggered Input Data Latches with Minimum Set-Up Times
- Negative Edge-Triggered Address Latches with Minimum Set-Up Times
- Negative Edge-Triggered Read/ Write Latch with Minimum Set-Up Time
- Positive Edge-Triggered Output Data Latches with Relaxed Propagation Delays
- Column and Row Decoding
- A Clock Generator that derives all necessary internal clocks from a single clock input.
- A scan-chain that internally connects all of the input latches.

RAMS2F can be customized with the following parameters:

Parameter	Description	Limits		
		Increment	Min	Max
N	Bits/Word	1	2	32
M	Address Bits	1	3	10
W	Words	8	8	1,024

8

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A[M-1:0], D[N-1:0], RW, CK, SI, DE, SD, TEST;

OUTPUTS: Q[N-1:0], QN[N-1:0], SO;

Functional Descriptions

Inputs

A[M-1:0]	Address In (A0 = LSB)
D[N-1:0]	Data In
RW	Read/Write - (Read = '1')
CK	Clock
SI	Scan-In Data
DE	Data Enable - (Active High)
SD	Select Data - (Active High)
TEST	Test Mode - (Active Low)

Outputs

Q[N-1:0]	Data Out
QN[N-1:0]	Complement Data Out
SO	Scan-Out Data

CHARACTERISTICS:

The parameters **N**, **M** and **W** can be used to estimate the characteristics for a RAMS2F that is **W** words X **N** bits per word with **M** address bits.

Parameter	Value	Unit
Number of Transistors	286 + 72M + 184N + (34 + M)W/8 + 6NW	
Height	820 + 5W	µ
Width	322 + 75.75N	µ
Worst Case Power	$(26.3+3.1M+0.11W+3.9N+0.0088NW+0.0044MW)VDD^2F/1{,}000$*	mW
Input Capacitance:		
A[M-1:0]	0.09	pF
D[N-1:0]	0.09	pF
RW	0.09	pF
CK	0.23 + 0.08N + 0.08M	pF
SI	0.10	pF
DE	0.26 + 0.18N	pF
SD	0.43 + 0.16N + 0.16M	pF
TEST	0.18	pF
Output Capacitance:		
Q[N-1:0]	0.27	pF
QN[N-1:0]	0.27	pF
SO	0.34	pF

* VDD = the power supply voltage in Volts and F = the clock frequency in MHz.

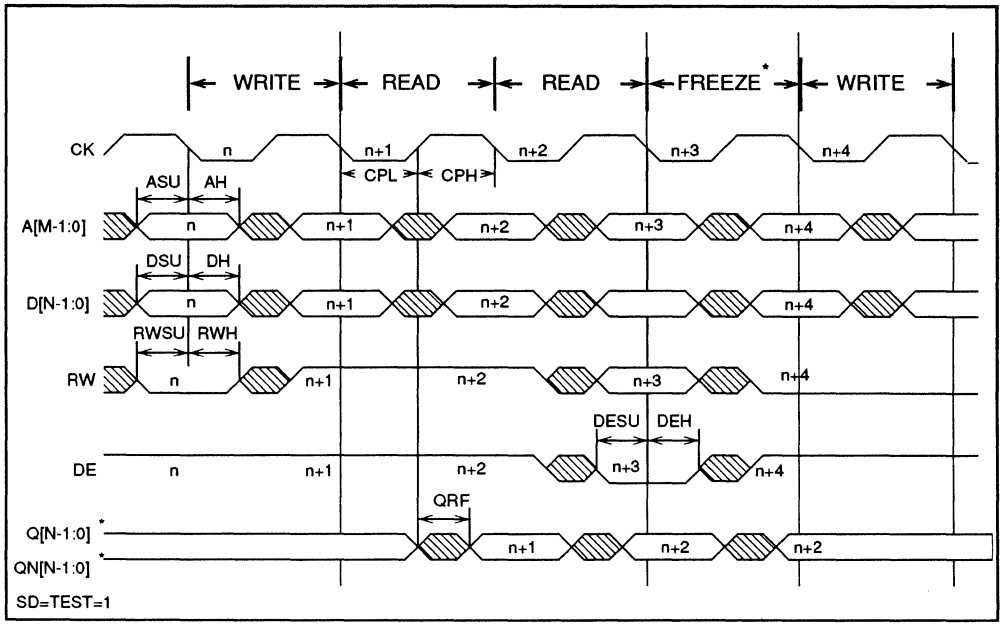
SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing				
Symbol	From INPUT	To OUTPUT	Intrinsic (ns)	Extrinsic (ns/pF)
QRF	CK↑	Q[N-1:0]↑	21+N/8+(2+N/8)(W-256)/ 768* 40.0**	0.6
	CK↑	Q[N-1:0]↓	21+N/8+(2+N/8)(W-256)/ 768* 40.0**	0.3
	CK↑	QN[N-1:0]↑	21+N/8+(2+N/8)(W-256)/ 768* 40.0**	0.6
	CK↑	QN[N-1:0]↓	21+N/8+(2+N/8)(W-256)/ 768* 40.0**	0.3
SORF	CK↓	SO↑	5.0	2.0
	CK↓	SO↓	7.0	2.0

* While not in the Scan-Test mode.

** During Scan-Testing Only.

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing		
Symbol	Description	Value (ns)
CPH	Minimum Clock Pulse High	10+N/8+(2+N/8)(W-256)/ 768
CPL	Minimum Clock Pulse Low	10+N/8+(2+N/8)(W-256)/ 768
ASU	Minimum Address Setup before CK↓	3.0
AH	Minimum Address Hold after CK↓	0.0
DSU	Minimum Data Setup before CK↓	3.0
DH	Minimum Data Hold after CK↓	0.0
RWSU	Minimum Read/Write Setup before CK↓	3.0
RWH	Minimum Read/Write Hold after CK↓	0.0
SISU	Minimum Scan-In Data Setup before CK↓	3.0
SIH	Minimum Scan-In Data Hold after CK↓	0.0
DESU	Minimum Data Enable Setup before CK↓	3.0
DEH	Minimum Data Enable Hold after CK↓	0.0
SDSU	Minimum Select Data Setup before CK↓	5.0 + 0.5N
SDH	Minimum Select Data Hold after CK↓	0.0

FUNCTIONAL MODE TIMING DIAGRAM



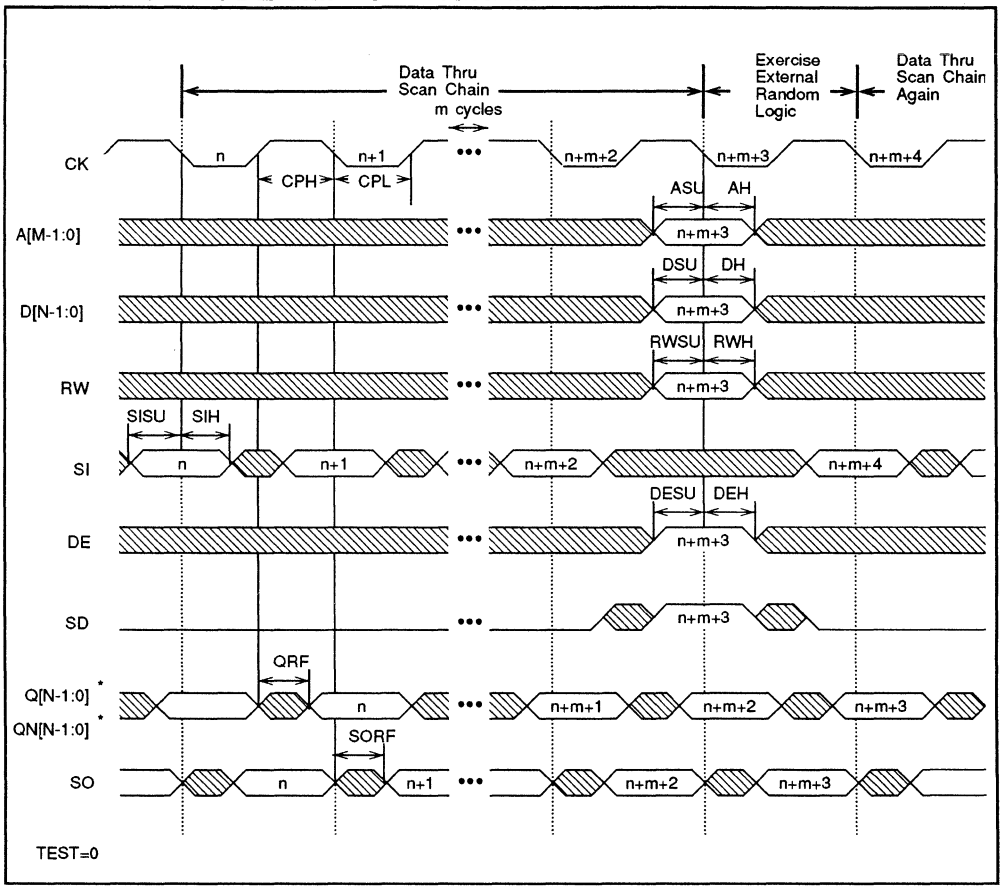
n=nth cycle number.

*A freeze cycle is executed when DE is low and SD is high. This cycle is provided as a convenience for freezing the RAMS2F. It can be applied anywhere or not at all. During this cycle information at inputs A[M-1:0], D[N-1:0], and RW is ignored. Instead, the information that was clocked in by CK in the previous cycle is reclocked and reused.

**Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ output is continuously available during subsequent WRITE operations.

8

SCAN TEST MODE TIMING DIAGRAM



n=nth cycle number.

*For the scan-testing mode, TEST is set low to place RAMS2F in a pseudo-transparent mode where the word addressed is simultaneously written and read. Thus, the input data, clocked in on the falling edge of CK, passes to the outputs Q and QN after CK goes high. With RAMS2F being pseudo-transparent in this mode, the random logic to RAMS2F can be more easily controlled and observed.

**For the scan-testing mode, CK should be run at one-tenth of the normal functional mode frequency.

FUNCTIONAL OPERATION

SCAN CHAIN

During LSSD the faults in the external random logic around the RAMS2F are tested. Only the input latches are connected together to form a scan chain; the output latches are by-passed to allow quick access to the external random logic connected at the outputs. In terms of the primary inputs for the input latches, the following specifies the ordering of the scan chain:

A[0:M-1], D[0:P-1], RW, D[P:N-1]

where P (= N/2) is rounded up to the nearest integer.

RAMS2F Mode Control

Functional/Scan-Testing Mode Control					
DE	SD	TEST	Allowed*	Mode	State
1	1	1	Yes	Functional	Normal
0	1	1	Yes	Functional	Freeze
1	0	1	No	Functional	Data Scanning with RW confusion
0	0	1	No	Functional	Data Scanning with RW confusion
1	1	0	Yes	Scan Test	Random Logic Clock
0	1	0	No	Scan Test	Freeze
1	0	0	Yes	Scan Test	Data Scanning
0	0	0	Yes	Scan Test	Data Scanning

*The disallowed states can be simulated, but they serve no useful purpose and should be avoided.

USER NOTES

1) Outputs Q[N-1:0] and QN[N-1:0] are latched at each READ operation. Therefore, the last READ outputs are continuously available during subsequent WRITE operations.
2) No glitches are allowed on the clock input CK. If the minimum clock pulse widths (high or low) are violated, any of the internal memory contents can be corrupted.
3) If the setup and hold time specs on the address inputs are violated, any of the internal memory contents can be corrupted.
4) The scan-test circuitry is present in the RAMS2F to support the scan-testing of the surrounding logic, and not the RAMS2F itself. In fact, the RAMS2F is constructed so that it effectively disappears from the chip during scan-testing.

FUNCTIONAL DESCRIPTION AND FEATURES

REGFILE is a parameterized register file function supported by automatic layout generation software. The layout of the REGFILE is implemented as a custom, pitch-matched array of cells designed to be area-efficient.

REGFILE has been designed specifically for use on standard cell chips and has the following features:

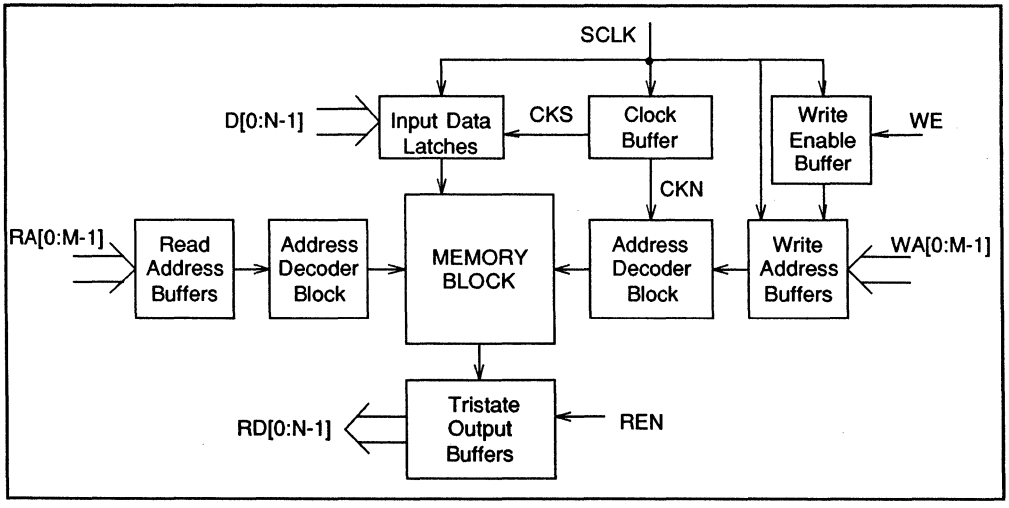
- Separate Read/Write Addressing permits simultaneous reading and writing.
- Asynchronous read operation.
- Tristate Outputs.
- Synchronous write operation requiring a single clock.
- Organized as W words of N bits.
- Negative edge triggered address, write enable and input data registers.

REGFILE can be customized with parameters N and W of the following table:

Parameter	Description	Limit		
		Increment	Min	Max
N	Bits/Word	1	2	32
M	Address Bits	2	4	8
W	Words	2	2	128

8

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: RA[0:M-1], D[0:N-1], RESET, WE, IWA[0:M-1], SCLK, RDEN;

OUTPUTS: RD[0:N-1];

Functional Descriptions

Inputs

RA[0:M-1]	Read Address Bits, RA0 is the LSB
D[0:N-1]	Data Inputs
RESET	Write all registers (No longer supported, RESET must be low)
WE	Write Enable (WE=1 Write)
IWA[0:M-1]	Write Address Bits (IWA0 is the LSB)
SCLK	Write Clock
RDEN	Output Enable Not

Outputs

RD[0:N-1]	Data Out Functional Mode

CHARACTERISTICS

The parameters **N**, **M** and **W** can be used to estimate the characteristics for a REGFILE that is **W** words X **N** bits per word.

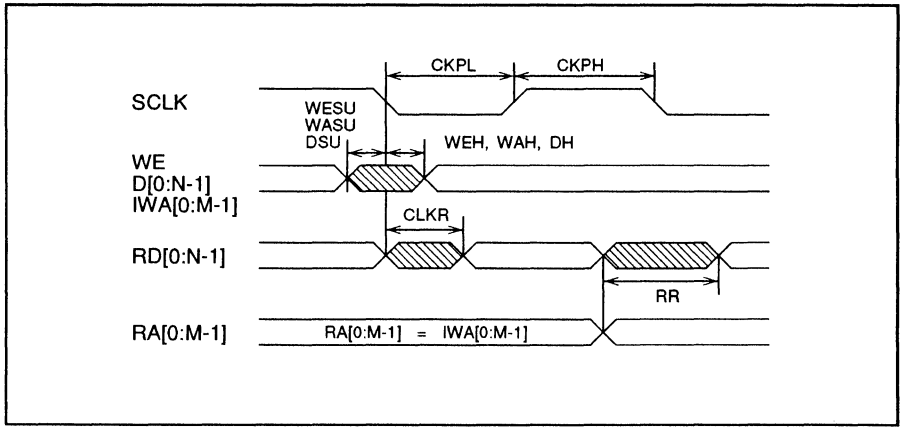
Parameter	Value	Unit
Height	280.875 + 19.625W	µ
Width	128.625 + 34.375N + 40.25M	µ
Worst Case Power	(24N + f (1.02 + 0.43M + 0.54N + (0.045 + 0.013N + 0.026M) W)) $VDD^2/1000$*	mW
Transistors	64 + 12W + 49N + 46M + 8WN + 4WM	
Input Capacitance:		
RA[0:M-1]	0.075	pF
D[0:N-1]	0.023	pF
RESET	0.029	pF
WE	0.058	pF
IWA[0:M-1]	0.029	pF
SCLK	0.256 + 0.055N + 0.063M	pF
RDEN	0.079N	pF
Output Capacitance:		
RD[0:N-1]	0.100	pF

* **VDD** = power supply potential (Volt), **f** = write clock frequency / frequency of read access (MHz).

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing				
Symbol	From INPUT	To OUTPUT	Intrinsic (ns)	Extrinsic (ns/pF)
RR	RA[0:M-1]	RD[0:N-1]	15.7 + 0.082W + 0.061N	0.7
CLKR	SCLK↓	RD[0:N-1]	5.51+ 0.061W + 0.066N	0.7

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing			
Symbol	Description	Value	Unit
WESU	WE Setup before SCLK↓	1.1	ns
WEH	WE Hold after SCLK↓	0.0	
WASU	Write Address Setup before SCLK↓	1.2	
WAH	Write Address Hold after SCLK↓	0.0	
DSU	D[0:N-1] Setup before SCLK↓	0.9	
DH	D[0:N-1] Setup after SCLK↓	0.0	
CKPL	Minimum SCLK Pulse Low	1.9 + 0.022W + 0.09N	
CKPH	Minimum SCLK Pulse High	1.2	

TIMING DIAGRAM



USER NOTES

1) Extra Address Bit: The architecture of REGFILE requires M, the number of address bits, to be an even integer. Many possible configuration of REGFILE, therefore, will have an extra address bit. The extra bit is the most significant bit and should be tied low.
2) Reset: The reset option is no longer supported. The reset signal should be tied low.
3) Zero Hold Times: Hold times, as specified, is defined as the time needed after the active edge of the clock to shut off the input latch. A hold time of 0.3ns guarantees proper operation even if the clock falls at a very slow rate.

FUNCTIONAL DESCRIPTION AND FEATURES

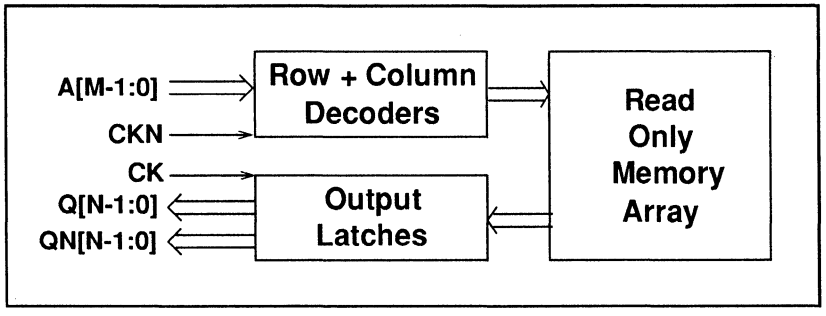
ROMS1A is a parameterized static fully decoded ROM function supported by automatic layout generation software. The layout of the ROMS1A is implemented as a custom, pitch-matched array of cells that is very area-efficient.

The ROMS1A has been designed specifically for use on standard cell chips, and as such, has overhead circuitry already built-in including positive edge-triggered output latches and full column and row decoding. Input latches are NOT included with the ROMS1A. Addresses should be latched with standard cell flip-flops.

The ROMS1A can be customized with the following parameters:

Parameter	Description	Limit		
		Increment	Min	Max
N	Bits/Word	1	2	32
M	Address bits	1	6	11
W	Words	2^M	64	2048

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A[M-1:0], CK, CKN;
OUTPUTS: Q[N-1:0], QN[N-1:0];

Functional Descriptions

Inputs

A[M-1:0]	Address Inputs
CK	Output Data Latch Clock
CKN	Inverted Precharge Clock

Outputs

Q[N-1:0]	Data Outputs
QN[N-1:0]	Complement Data Outputs

CHARACTERISTICS

The parameters N, M, and W can be used to estimate the characteristics for a particular version of the ROMS1A.

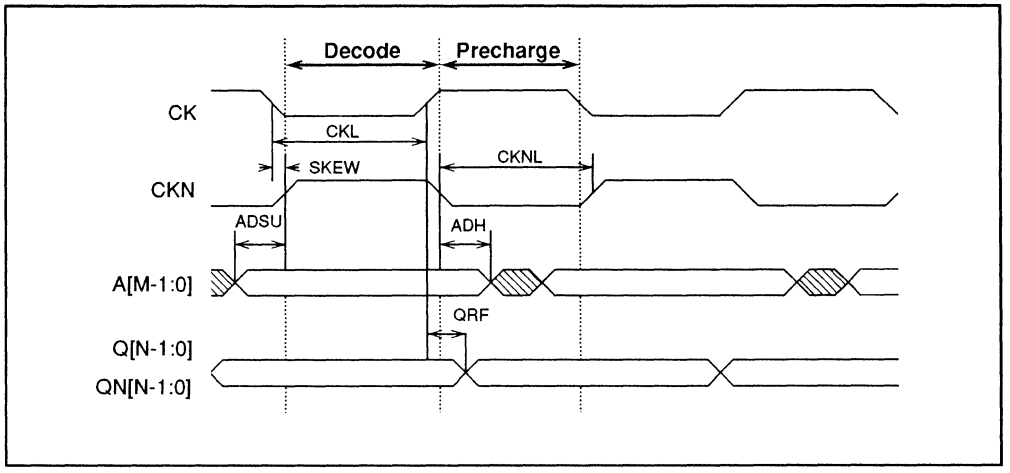
Parameter	Value	Unit
Number of Transistors:	$0.133(W/64)^2 + 77.34(W/64) + 212.52 + 54N + (\#\text{ of logical 0's})$	
Height	$0.625W + 252.125$	µ
Width	$47.25N + 10M + 283.125$	µ
Worst Case Power	$0.22VDD^2fNW^*$	µW
Input Capacitance:		
A[M-1:0]	$0.148 + (1.13 \times 10^{-4})W$	pF
CK	$0.0965N + (1.23 \times 10^{-4})W + 0.135$	pF
CKN	$0.56N + (5.55 \times 10^{-3})W + 1.050$	pF
Output Capacitance:		
Q[N-1:0]	0.148	pF
QN[N-1:0]	0.146	pF

* VDD = the power supply voltage, f = the clock frequency in MHz.

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing				
Symbol	From INPUT	To OUTPUT	Intrinsic (ns)	Extrinsic (ns/pF)
QRF	CK↑	Q[N-1:0]↑	1.4	1.9
	CK↑	Q[N-1:0]↓	0.8	1.2

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Symbol	Description	Value	Unit
CKNL	Minimum Precharge Clock Low	0.012(NW/256) + 1.51(N/4) + 0.28(W/64) + 4.74 + SKEW	ns
CKL	Minimum Clock Low	0.014(NW/256) + 0.37(N/4) + 0.23(W/64) + 3.54	
ADSU	Minimum Address Set-Up Time	$0.02(N/4)^2$ + 0.9(N/4) + 1.16	
ADH	Minimum Address Hold Time	0	
SKEW	Clock Skew	>0	

TIMING DIAGRAM



USER NOTES

1) The ROMS1A can only be generated fully decoded. When a word count is desired that does not lend itself to full decoding, choose the next largest size. The remaining words will be set to logical 1's.
2) CKN must be generated from CK.
3) Input latches are NOT included with the ROMS1A. Any changes in the Address during the decode will result in corrupt output data.
4) The Rise/Fall times for CK and CKN should be less than 25ns.

8

FUNCTIONAL DESCRIPTION AND FEATURES

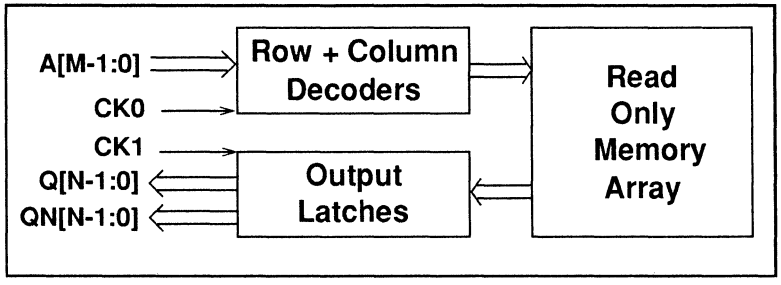
ROMS2A is a parameterized static fully decoded ROM function supported by automatic layout generation software. The layout of the ROMS2A is implemented as a custom, pitch-matched array of cells that is very area-efficient.

The ROMS2A has been designed specifically for use on standard cell chips, and as such, has overhead circuitry already built-in including negative edge-triggered output latches and full column and row decoding. Input latches are NOT included with the ROMS2A. Addresses should be latched with standard cell flip-flops.

The ROMS2A can be customized with the following parameters:

Parameter	Description	Limit		
		Increment	Min	Max
N	Bits/Word	1	2	32
M	Address bits	1	6	11
W	Words	2^M	64	2048

BLOCK DIAGRAM



8

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A[M-1:0], CK0, CKN1;

OUTPUTS: Q[N-1:0], QN[N-1:0];

Functional Descriptions

Inputs

A[M-1:0]	Address Inputs
CK0	Precharge Clock
CK1	Output Data Latch Clock

Outputs

Q[N-1:0]	Data Outputs
QN[N-1:0]	Complementary Data Outputs

CHARACTERISTICS

The parameters N, M, and W can be used to estimate the characteristics for a particular version of the ROMS2A.

Parameter	Value	Unit
Number of Transistors:	$0.133(W/64)^2 + 77.34(W/64) + 212.52 + 54N + (\#\ of\ logical\ 0s)'$	
Height	$0.625W + 252.125$	µ
Width	$47.25N + 10\ M + 283.125$	
Worst Case Power	$0.22VDD^2fNW$*	µW
Input Capacitance:		
A[M-1:0]	$0.148 + (1.13X10^{-4})W$	pF
CK1	$0.0965N + (1.23X10^{-4})W + 0.135$	
CK0	$0.56N + (5.55X10^{-3})W + 1.050$	
Output Capacitance:		
Q[N-1:0]	0.148	pF
QN[N-1:0]	0.146	

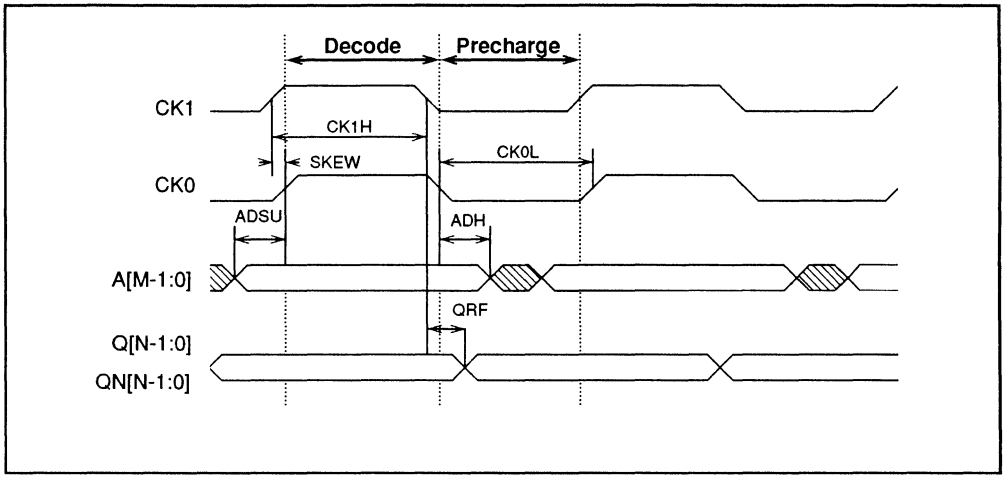
* VDD = the power supply voltage, f = the clock frequency in MHz.

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, NOM Processing				
Symbol	From INPUT	To OUTPUT	Intrinsic (ns)	Extrinsic (ns/pF)
QRF	CK1↑	Q[N-1:0]↑	1.4	1.9
	CK1↑	Q[N-1:0]↓	0.8	1.2

Timing Requirements VDD=5.0V, T=25°C, NOM Processing			
Symbol	Description	Value	Unit
CK1H	Minimum Clock High	0.014(NW/256) + 0.37(N/4) + 0.23(W/64) + 3.54	ns
CK0L	Minimum Precharge Clock Low	0.012(NW/256) + 1.51(N/4) + 0.28(W/64) + 4.74 + SKEW	
ADSU	Minimum Address Set-Up Time	$0.02(N/4)^2$ + 0.9(N/4) + 1.16	
ADH	Minimum Address Hold Time	0	
SKEW	Clock Skew	0	

8

TIMING DIAGRAM



USER NOTES

1) The ROMS2A can only be generated fully decoded. When a word count is desired that does not lend itself to full decoding, choose the next largest size. The remaining words will be set to logical 1's.
2) CK0 should be applied in such a way as to minimize skewing with respect to CK1. Any skewing between the clocks will detract from the performance of the ROMS2A.
3) Input latches are NOT included with the ROMS2A. Addresses should be latched with standard cell flip-flops.
4) The Rise/Fall times for CK0 and CK1 should be less than 25ns.
5) If the Rise/Fall times for CK1 and CK0 are greater than 25ns, CK0 must be delayed from CK1 to insure the proper latching of the data outputs.

FUNCTIONAL DESCRIPTION AND FEATURES:

SRGEN is a parameterized Shift Register function supported by automatic layout generation software. The layout of SRGEN is implemented as a custom, pitch-matched array of cells that is very area efficient.

SRGEN has been designed specifically for use on standard cell chips and has the following features:

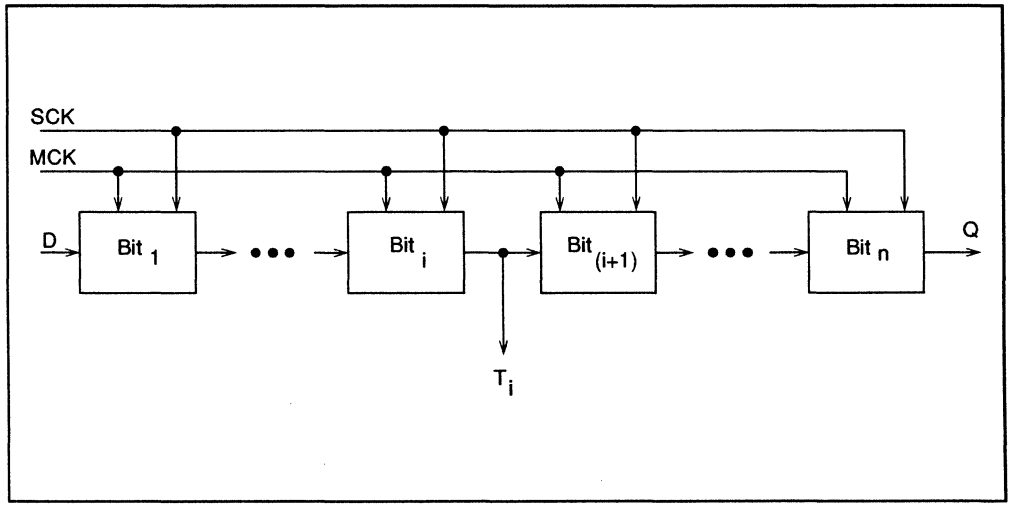
- Requires non-overlapping Master and Slave clocks.
- Can be implemented with multiple tap bits.
- Tap Bits can be automatically placed along the shift register.
- Outputs, including tap bits, are properly buffered to interface with standard cell circuitry.
- The aspect ratio of the shift register can be easily modified to suit the needs of the chip layout.

The Shift Register can be customized with the following parameters:

Parameter	Description	Limit		
		Increment	Min	Max
N	Bits in Depth	1	1	65,000
$T_i,...,T_n$	Tapped Locations	1	0	65,000
M	Rows to Fold the Array	1	1	N/205

8

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: MCK, SCK, D;

OUTPUTS: T_i,...,T_n, Q;

Functional Descriptions

Inputs

MCK	Master Clock
SCK	Slave Clock
D	Data Input

Outputs

T_i,...,T_n	Tapped Data Out (Subscript corresponds to the register position tapped)
Q	Data Out (Tap of last register)

CHARACTERISTICS

The parameters N, T and M can be used to estimate the characteristics for a Shift Register that is N bits deep, has T tapped locations and is folded into M rows.

Parameter	Value	Unit
Number of Transistors	8N + 4T + 4	
Height	33.125M + 4T +3.75(N/244)* + 17	µ
Width	24.75[(N+2T+1)/M]* + 0.004N + 40	µ
Worst Case Power	$VDD^2f(0.0556N + 2.268T)$**	µW
Input Capacitance:		
D	0.010	pF
MCK	[2.9H + 1.63W(N/244)* + 1.96(HN/M + 28.129N + 15)***]10^{-4}	pF
SCK	[2.9H + 1.63W(N/244)* + 1.96(HN/M + 28.129N + 15)***]10^{-4}	pF
Output Capacitance:		
Q	0.000163W/2**** + 0.091	pF
T_i,...,T_n	0.000163W/2**** + 0.091	pF

* Round to the next higher integer.

** VDD = the power supply voltage, f = the clock frequency in MHz.

*** H and W represent the height and the width(in microns) of the shift register respectively.

**** The term given here represents an average value. To get a more accurate value replace W/2 by the actual distance from the tapped(or last cell) to the edge of the shift register where the corresponding output terminal is located.

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing				
Symbol	From INPUT	To OUTPUT	Intrinsic (ns)	Extrinsic (ns/pF)
SQ	SCK↑	Q↑	3.1	0.9
	SCK↑	Q↓	2.6	0.6
	SCK↑	T_i...,T_n↑	3.1	0.9
	SCK↑	T_i...,T_n↓	2.6	0.6

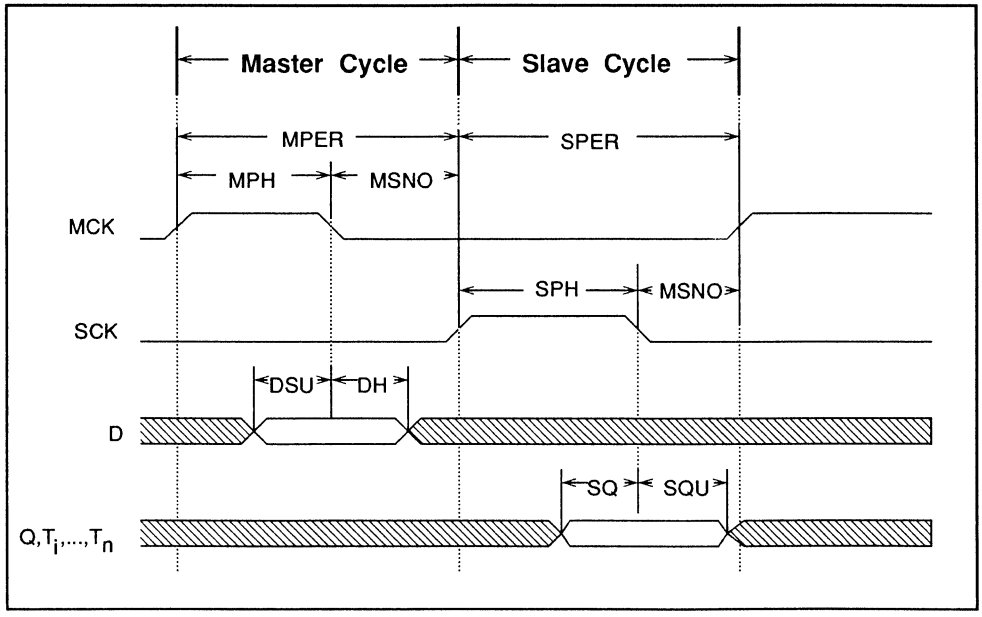
Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Symbol	Description	Value	Unit
MPH	Minimum Master Clock Pulse High	1.5	ns
MPER	Minimum Master Clock Cycle	3.4	ns
	Maximum Master Clock Cycle	41.7 ***	µs
SPH	Minimum Slave Clock Pulse High	1.8	ns
SPER	Minimum Slave Clock Cycle	2.9 + 2.5C_{max}*	ns
	Maximum Slave Clock Cycle	41.7 ***	µs
MSNO	Minimum Time Between Master and Slave Pulses	0.3**	ns
	Maximum Time Between Master and Slave Pulses	41.7 ***	µs
DSU	Minimum Data In Setup Time	0.4	ns
DH	Minimum Data In Hold Time	0	
SQU	Maximum Hold Time for Data Out	41.7 ***	µs

* C_{max} = the largest capacitive load(in pF) on any single output.

** The time shown is for rise and fall times of 1 ns. For different rise and fall times, a zero overlap of master and slave pulses at V_{thn} must be assured.

*** These values are actually the worst case hold time for the dynamic nodes.

TIMING DIAGRAM



USER NOTES

1) In order to reduce leakage current from the dynamic nodes, every effort should be made to reduce noise on the clocks and insure that they are indeed non-overlapping.
2) The propagation delay shown in the tables is worst case for the cell furthest from the slave clock input terminal. There is some skew, due to routing parasitics, in the clock delay to different tapped locations.
3) The dynamic shift register is inherently subject to alpha induced soft errors. This macrocell should not be used to store critical data.

Linear Cells

Section 9

AT&T

Contents - Section 9

Introduction

This section describes the Linear CMOS cells that are available for use with the 1.25µ Standard Cell Library. The reason for the introduction of linear cells into an otherwise digital world is to add versatility to the digital chips by providing functions that can not be done with strictly digital circuits.

The linear cells are designed to be as similar to the digital standard cells and buffers as possible. The digital CMOS process, with only a single level of polysilicon, is standard. The software for circuit simulation, netlist capture, and layout is identical to that used on digital cells. The linear cells are also designed to be testable in a digital environment. It is intended that the linear cells form a small part of the entire chip, typically less than 10% of the area.

Since most linear CMOS cells in this library are I/O intensive, they are configured to be placed in the buffer area on the periphery of the chip. Many of them will fit into the standard I/O buffer ring and connect to the buffer power supplies. Some linear cells, however, are too noise sensitive to use these digital power supplies, and they require their own power and ground connections.

Many VLSI CMOS chips are designed to be retrofits of existing SSI boards. The linear chips on these boards are mostly bipolar. Bipolar linear circuits usually have some performance characteristics not obtainable with linear CMOS. It may not be possible for a linear CMOS cell to meet the specs of a (bipolar) part that is currently in use. Therefore, consult with your AT&T representative about what specs are realistic.

CAD Support Files

The CAD Support files for Linear CMOS are modeled as closely as possible after those used for digital circuits.

ADVICE

The standard process files used for ADVICE simulations of digital circuits (***apronc.dat***, ***aprolc.dat***, and ***aprohc.dat***) are also used with the Linear Cells. In addition to these process files, a special device file ***advldev.dat***, from the linear library, must be used in order to run ADVICE.

The easiest way to do this is to include the line ***.USE advldev.dat*** in your ADVICE file.

All of the linear cells have been characterized using ADVICE, and the resulting characteristics are presented in the following pages. Unless otherwise specified, the worst-case simulations were all done assuming VDD=5 volts ±10%, a temperature range of 0°C to 100°C, standard (digital) fast and slow process files, and a ±30% variation from nominal resistor values. Any circuit parameters that are not specified cannot be guaranteed.

Since P+ resistors are used in many Linear Cells, the model parameter ***SCAL*** of the PPLUS resistor model is used to globally adjust the scale factor of these resistors. It is initialized at unity in ***advldev.dat***. The variation of resistors due to process drift is ±30%. Thus for low resistors use ***.MODEL PPLUS SCAL=0.7*** and for high resistors use ***.MODEL PPLUS SCAL=1.3***. In addition to this global scaling ability, the resistor model has built-in temperature and voltage coefficients.

MOTIS3

Simulations with MOTIS3 models are ***not*** intended to replace ADVICE simulations. The true analog nature of these circuits cannot be simulated in the current MOTIS3 environment. The real reason to use the MOTIS3 models is that they allow the designer to use a single netlist throughout the design process. However, ADVICE is still required to simulate the detailed analog behavior and timing, using the circuit descriptions found in the file ***advlc.dat*** from the linear library.

Schmitt Trigger Input Buffer

BICSI09[*D,T*]

Inverting CMOS Level

FUNCTIONAL DESCRIPTION

These are inverting Schmitt trigger CMOS level input buffers, designed for use with slowly varying and/or noisy signals which cause ordinary input buffers to oscillate.

NETLIST ORDER

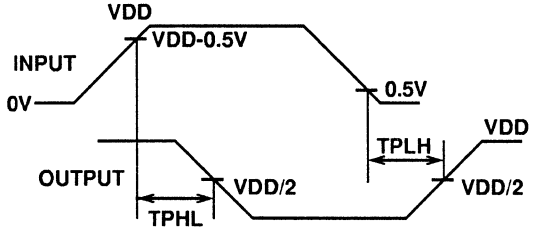
INPUTS: IN;

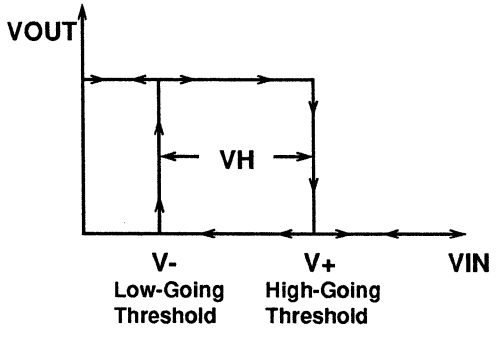
OUTPUTS: OUT;

CIRCUIT INFORMATION

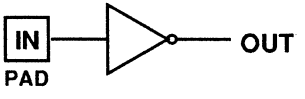
PARAMETER	BICSI09
MAX POWER	NIL
MAX DELAY *	5.8ns + 0.60ns/pF
MIN DELAY*	2.1ns + 0.22ns/pF
MAX INPUT CAPACITANCE	3.4pF
DC CHARACTERISTICS	
(Refer to the figure below)	
MIN V-	0.5V
MAX V+	VDD - 0.5V
MIN VH (HYSTERESIS)	1.8V
CELL SIZE	
BICSI09D	337µ x 291.75µ
BICSI09T	175µ x 540.125µ

*With waveforms as shown below





SCHEMA SYMBOL



Schmitt Trigger Input Buffer

BICSN09[*D,T*]

Non-inverting CMOS Level

FUNCTIONAL DESCRIPTION

These are non-inverting Schmitt trigger CMOS level input buffers, designed for use with slowly varying and/or noisy signals which cause ordinary input buffers to oscillate.

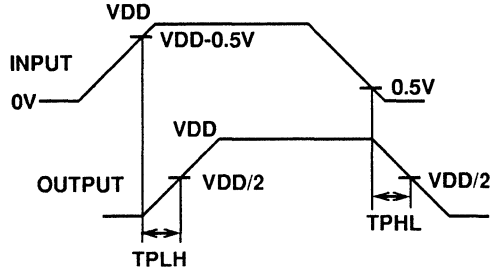
NETLIST ORDER

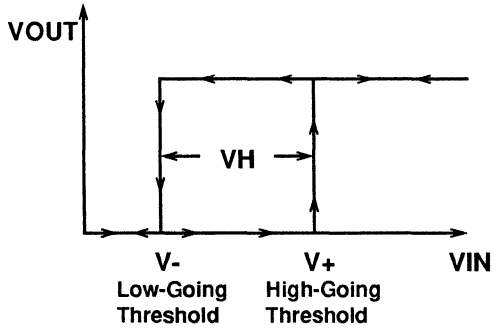
INPUTS: IN;
OUTPUTS: OUT;

CIRCUIT INFORMATION

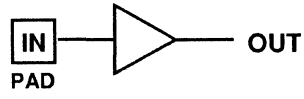
PARAMETER	BICSN09
MAX POWER	NIL
MAX DELAY *	6.1ns + 0.60ns/pF
MIN DELAY*	2.1ns + 0.22ns/pF
MAX INPUT CAPACITANCE	3.4pF
DC CHARACTERISTICS (Refer to the figure below)	
MIN V-	0.5V
MAX V+	VDD - 0.5V
MIN VH (HYSTERESIS)	1.8V
CELL SIZE	
BICSI09D	349µ x 291.75µ
BICSI09T	175µ x 540.125µ

* With waveforms as shown below





SCHEMA SYMBOL



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Schmitt Trigger Input Buffer

BITSI[*08,12*][*D,T*]

Inverting TTL Level

FUNCTIONAL DESCRIPTION

These are inverting Schmitt trigger TTL level input buffers, designed for use with slowly varying and/or noisy signals which cause ordinary input buffers to oscillate.

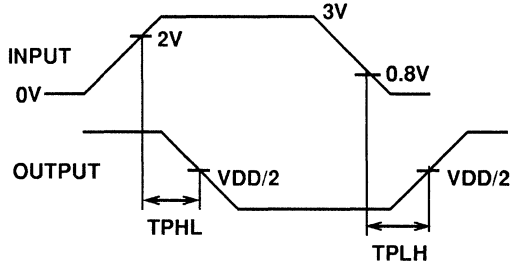
NETLIST ORDER

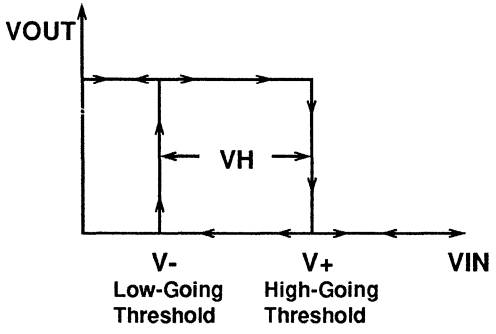
INPUTS: IN;
OUTPUTS: OUT;

CIRCUIT INFORMATION

PARAMETER	BITSI08x	BITSI12x
MAX POWER at VIN=2V	12mW	4mW
MAX DELAY *	4.5ns + 0.70ns/pF	9.0ns + 0.70ns/pF
MIN DELAY*	1.4ns + 0.22ns/pF	3.5ns + 0.22ns/pF
MAX INPUT CAPACITANCE	3.8pF	3.8pF
DC CHARACTERISTICS (Refer to the figure below)		
MIN V-	0.8V	0.8V
MAX V+	2.0V	2.0V
MIN VH (HYSTERESIS)	0.3V	0.3V
CELL SIZE		
BITSI[08,12]D	271µ x 291.75µ	349µ x 291.75µ
BITSI[08,12]T	175µ x 540.125µ	175µ x 540.125µ

* With waveforms as shown below





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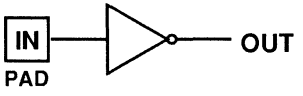


Schmitt Trigger Input Buffer

BITSN[*08,12*][*D,T*]

Non-inverting TTL Level

FUNCTIONAL DESCRIPTION

These are non-inverting Schmitt trigger TTL level input buffers, designed for use with slowly varying and/or noisy signals which cause ordinary input buffers to oscillate.

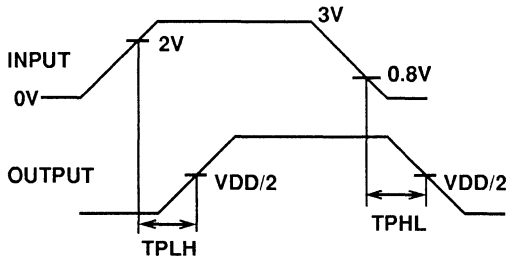
NETLIST ORDER

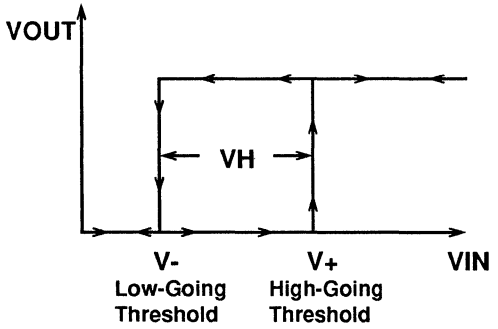
INPUTS: IN;
OUTPUTS: OUT;

CIRCUIT INFORMATION

PARAMETER	BITSN08x	BITSN12x
MAX POWER at VIN=2V	12mW	4mW
MAX DELAY *	5.0ns + 0.60ns/pF	9.2ns + 0.60ns/pF
MIN DELAY*	1.6ns + 0.22ns/pF	3.5ns + 0.22ns/pF
MAX INPUT CAPACITANCE	3.8pF	3.8pF
DC CHARACTERISTICS (Refer to the figure below)		
MIN V-	0.8V	0.8V
MAX V+	2.0V	2.0V
MIN VH (HYSTERESIS)	0.3V	0.3V
CELL SIZE		
BITSN[08,12]D	275µ x 291.75µ	363µ x 291.75µ
BITSN[08,12]T	175µ x 540.125µ	175µ x 540.125µ

* With waveforms as shown below





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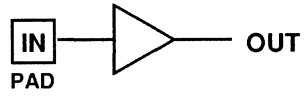

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FUNCTIONAL DESCRIPTION

The function of the LOT15U is to detect the loss of a signal which, under proper operating conditions, regularly changes its state. This would most often be used with a clock, but can be used with any signal.

This cell detects either a stuck-high or stuck-low condition. It will work with any signal in the frequency range of 250KHz to 100MHz, whose duty cycle is between 20% and 80%.

In order to use ADVICE with the LOT15U, the cells BISN2A, SINRB, and SNR2, from the linear CMOS library, must be appended to the main circuit.

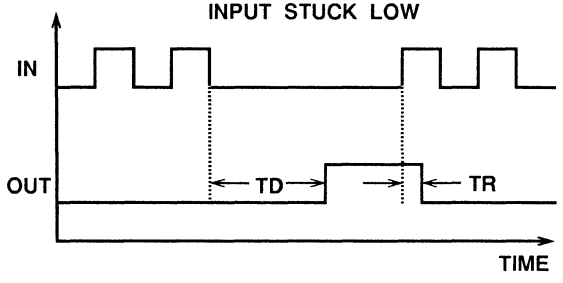
The cell height is the same as digital D and P style buffers. This cell does not contain a bonding pad.

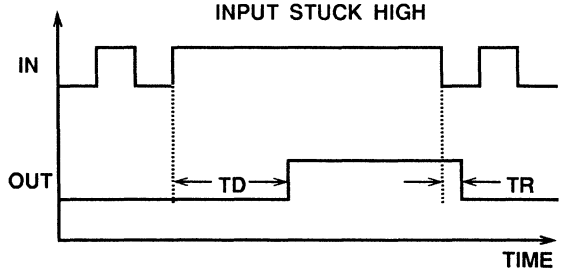
NETLIST ORDER

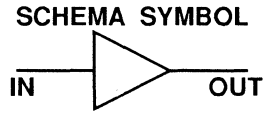
INPUTS: IN;
OUTPUTS: OUT;

CIRCUIT INFORMATION

PARAMETER	LOT15U
MAX POWER	1mW
DETECT TIME TD	
MINIMUM	7 µs
NOMINAL	15µs
MAXIMUM	31µs
RECOVERY TIME TR	
MAXIMUM	0.2µs
CELL SIZE	372µ x 291.75µ







Low Voltage Detector

LVD[*60,600*]

60mV or 600mV hysteresis

FUNCTIONAL DESCRIPTION

These circuits provide a high output whenever VDD exceeds a threshold voltage. The nominal threshold is 3.79 volts, with a 60mV (nominal) hysteresis for LVD60, and with a 600mV (nominal) hysteresis for LVD600. The actual threshold depends on processing and temperature.

The subcircuit CP09E, for LVD60, and subcircuit CP09D, for LVD600, must be used in order to run ADVICE. The subcircuits are located in the linear CMOS library.

The cell heights are the same as digital D and P style buffers. These cells do not contain bonding pads.

NETLIST ORDER

OUTPUTS: OUT;

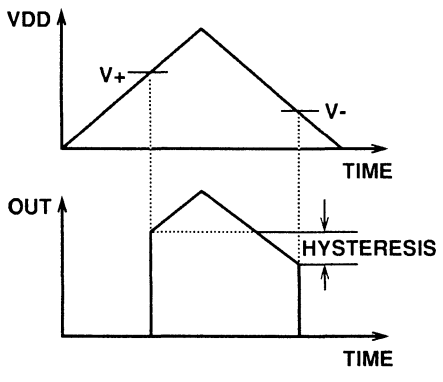
CIRCUIT INFORMATION

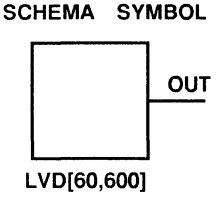
PARAMETER	LVD60			LVD600		
	V+ (volts)	V- (volts)	HYSTERESIS (mV)	V+ (volts)	V- (volts)	HYSTERESIS (mV)
MAXIMUM*	4.36	4.28	80	4.34	3.64	700
MAX TEST**	4.28	4.20	80	4.24	3.49	750
NOMINAL	3.79	3.73	60	3.79	3.19	600
MINIMUM***	3.14	3.10	40	3.13	2.63	500
MAX POWER	2mW			1mW		
CELL SIZE	493.5µ x 291.75µ			493.5µ x 291.75µ		

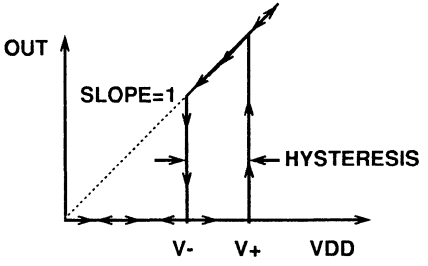
* Maximum conditions: Slow process, resistors low, T=0°C

** Maximum test conditions: Slow process, resistors low, T=85°C

*** Minimum conditions: Fast process, resistors high, T=100°C







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Power-up Reset

PURA[*3M,300U,30U*]

3ms, 300µs, 30µs Nominal Pulse Width with Test Mode

FUNCTIONAL DESCRIPTION

These circuits are designed to provide a clear pulse immediately upon chip power-up. After a time TP, the clear pulse goes low, and stays low as long as VDD stays high and the test input TST is low.

The cell heights are the same as digital D and P style buffers. These cells do not contain bonding pads.

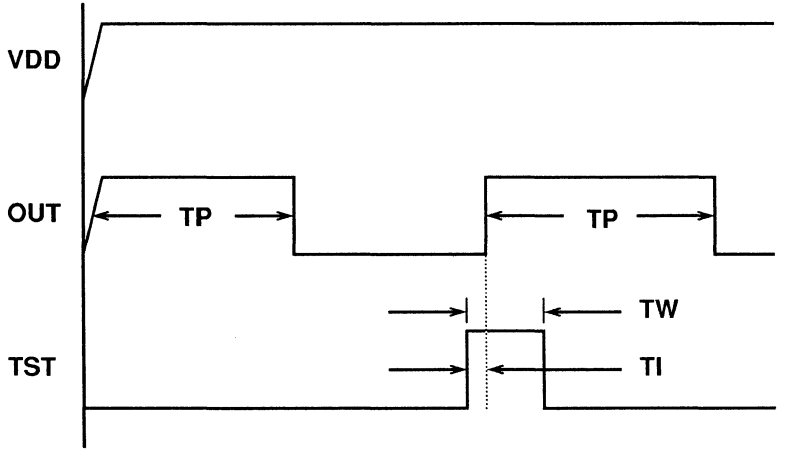
NETLIST ORDER

INPUTS: TST;
OUTPUTS: OUT;

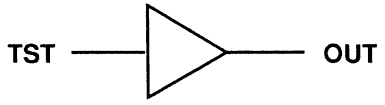
CIRCUIT INFORMATION

PARAMETER	PURA3M			PURA300U			PURA30U		
	TW	TP	TI	TW	TP	TI	TW	TP	TI
MAXIMUM	N/A	7ms*	200ns	N/A	700µs**	70ns	N/A	70µs***	70ns
NOMINAL	N/A	3ms	90ns	N/A	300µs	30ns	N/A	30µs	30ns
MINIMUM	300ns	1.5ms	45ns	100ns	150µs	15ns	100ns	15µs	15ns
MAX POWER	0.5mW			0.5mW			0.5mW		
CELL SIZE	534µ x 291.75µ			369µ x 291.75µ			369µ x 291.75µ		

*As long as VDD≥4 volts within 1ms of start-up
**As long as VDD≥4 volts within 100µs of start-up
*** As long as VDD≥4 volts within 20µs of start-up



SCHEMA SYMBOL



Test Function Enhancement Circuit — TBAD

FUNCTIONAL DESCRIPTION

This circuit is a two-bit A/D converter which is designed to operate in a noisy digital environment. It will provide four undecoded states from a single input pad as an aid in selecting different test paths during wafer or package testing. The circuit should not be used as a general purpose A/D. To save on power, connect IN to VSS when not actually using the circuit.

The subcircuits CP01TBD, CP02TBD, and CS2TBD from the linear CMOS library must be used with TBAD in order to run ADVICE.

The cell height is the same as digital D and P style buffers.

NETLIST ORDER

INPUTS: IN;
OUTPUTS: A0,A1,A2;

CIRCUIT INFORMATION

PARAMETER				STATE		
VDD	4.5	5.0	5.5	A2	A1	A0
Vin*	VSS	VSS	VSS	0	0	0
	1.687	1.875	2.062	0	0	1
	2.812	3.125	3.437	0	1	1
	VDD	VDD	VDD	1	1	1

*The values shown are the recommended input voltages that will maximize noise immunity.

PARAMETER	TBAD
MAX POWER	5mW
MAX DELAY	110ns
CELL SIZE	644.25µ x 291.75µ

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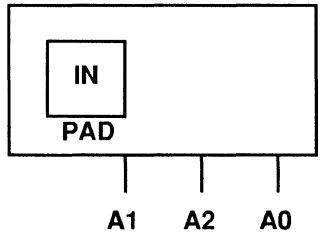
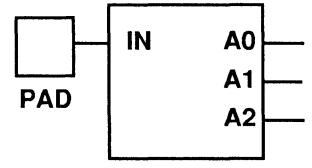
CELL LAYOUT



SCHEMA SYMBOL



Introduction

The crystal oscillators available in the AT&T 1.25µ CMOS Standard Cell library are all of the Pierce type. An inverter is used as the amplifying element, the crystal is connected between input and output terminals, and capacitors are connected from input to ground and from output to ground, respectively. The generic circuit topology is shown in Figure 1. This circuit configuration operates the crystal in a parallel resonant condition, which means that the operating frequency will be several hundred ppm (parts per million) above the crystal's series resonant frequency, and will be dependent on the capacitances present in the circuit.

Several different oscillator cells are available. Their distinguishing characteristics are frequency range, presence or absence of on-chip capacitors, and level compatibility (TTL or CMOS) for input buffer applications. Refer to the individual data sheets for specific information about these characteristics.

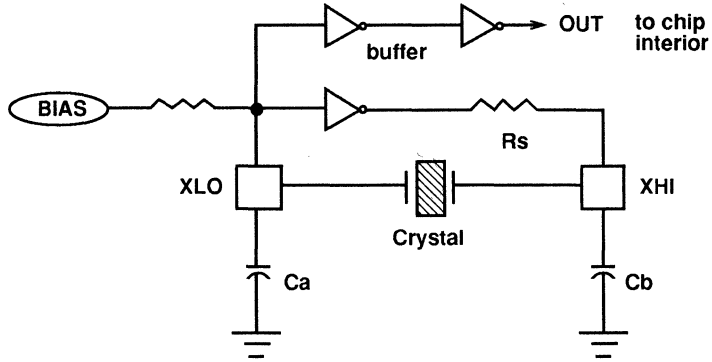


Figure 1. Pierce Crystal Oscillator Based on CMOS Inverter

As shown in Figure 1, the crystal terminals are XLO and XHI. XLO is the input side of the amplifier and XHI is the output side. Because these terminals are pads for external connections, the usual protection circuitry is in place (adding approximately 2 picofarads of shunt capacitance and 200Ω of series resistance to each pad). Capacitors ***Ca*** and ***Cb*** may be on or off-chip. Resistor ***Rs*** is on-chip, and has a nominal value of 1000Ω. The signal from the oscillator is taken from the XLO terminal, and buffered by two inverter stages before passing into the chip interior.

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Crystal Considerations

The operation of the oscillator is influenced to a great extent by the characteristics of the particular crystal being used. For a specific application, the crystal and the oscillator circuit must be considered (and possibly simulated) together to verify acceptability of performance.

The crystal chosen for operation with any of these oscillators must be a *fundamental mode* unit. The frequency should be specified under parallel resonance conditions, with a load capacitance which is approximately 2pF more than the series combination of capacitors ***Ca*** and ***Cb***. (***Ca*** and ***Cb*** include any stray capacitances present on their respective nodes). The frequency tolerance and stability should be specified according to the needs of the application; ±100 ppm is commonly available at reasonable cost, with tighter specs available at higher cost.

A ceramic resonator behaves like a low-Q crystal, and may be used as a less expensive alternative to the quartz crystal with any of these oscillators. Generally, this substitution trades off some degree of frequency stability for lower component cost and faster oscillator startup.

The Negative Resistance Plot

It is convenient to characterize an oscillator circuit in terms of its negative resistance. The impedance seen looking into the oscillator terminals (with the crystal removed) consists of a negative imaginary part (indicating net capacitance) and a negative real part (see Figure 2). The negative real part is indi-

cative of the circuit's potential for oscillation. A parallel resonant crystal appears as an equivalent resistance-inductance series combination. If the magnitude of negative resistance (at the crystal frequency) is greater than the crystal resistance, the net resistance will be negative, and the circuit will oscillate at the frequency where the crystal's inductance cancels the circuit's capacitance.

Each oscillator cell datasheet displays its negative resistance versus frequency. To produce a more useful graph, we have included the shunt capacitance of the crystal (*C0*) and the capacitors *Ca* and *Cb* with the oscillator in plotting the negative resistance characteristics shown in the oscillator data sheets. This way, the series resistance (*R1*) of the crystal may be directly compared to the negative resistance plot. Not shown, but also included in the simulation which produced the negative resistance plots, are typical stray capacitances of 5pF from each crystal terminal (XLO, XHI) to ground, and 2pF between the crystal terminals.

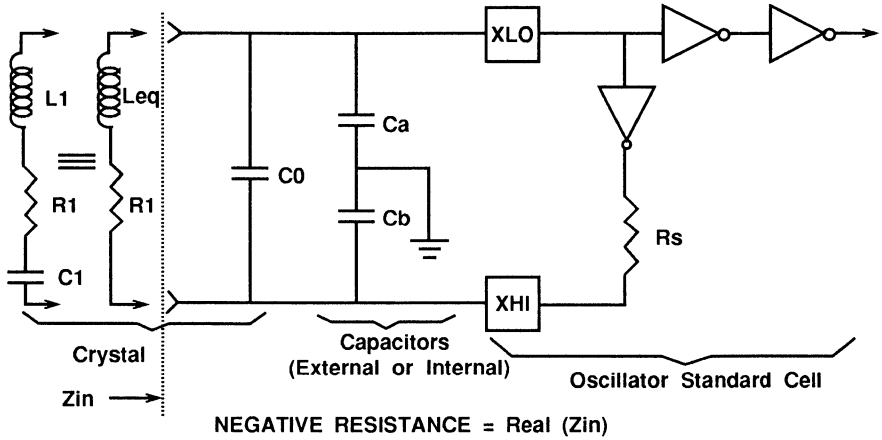


Figure 2. Comparison of Crystal Series Branch Impedance with Oscillator Impedance

Oscillator Operation

To determine whether oscillation is possible with a given crystal and oscillator, obtain the negative resistance at the crystal frequency from the plot in the data sheet. Compare the magnitude of negative resistance with the maximum resistance (*R1*) specified on the crystal data sheet. The crystal resistance should be smaller by at least a factor of two for reasonable loop gain margin (reliable oscillation under a variety of conditions).

A capacitor (*Ca*,*Cb*) must be connected from each pad to circuit ground for proper operation. External capacitors may be used, or the optional on-chip capacitors may be selected by choosing the proper oscillator. In the latter case, the only required external component is the crystal. For *XC*-prefix oscillators, the two external capacitors should be the same value. For *XT*-prefix oscillators, the value of *Ca* should be 2 to 3 times larger than the value of *Cb*.

The oscillator frequency stability is primarily governed by the crystal, but can be affected by any perturbation in the capacitances of the circuit. Generally, larger capacitances (at *Ca* and *Cb*) produce better frequency stability, because unknown (e.g. stray) capacitances can be kept to a smaller fraction of the total.

A crystal behaves like a tuned circuit with a very high Q (quality factor). Because of this, many thousands of cycles are required for the amplitude of the oscillation to grow to its steady-state level after power is applied. Up to 20 milliseconds should be allowed for oscillations to reach steady state at lower (< 10 MHz) frequencies. Start-up time generally increases with increasing crystal Q, increasing capacitive load, and decreasing frequency.

Input Buffer Operation

If an external clock signal is available, the oscillator cell may be used as a noninverting input buffer. *XC*-prefix cells are CMOS-compatible; *XT*-prefix cells are TTL-compatible. During input buffer operation, the input signal must be applied at the XLO pad, and the XHI pad must be left unconnected. External components (crystal, capacitors) should not be used during operation as an input buffer.

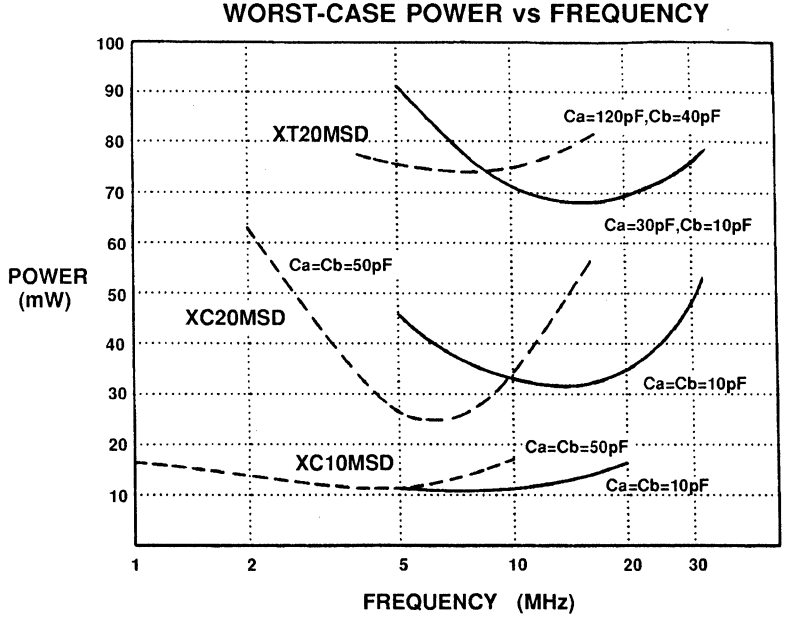
Standard Characterization Conditions

Worst-case characterization of the crystal oscillator cells has been performed under those conditions which minimize negative resistance, and, separately, under those conditions which maximize power consumption:

1) For negative resistance: maximum capacitance at XLO (*Ca*) and at XHI (*Cb*), worst-case slow processing, high (100°C) temperature and low (4.5 volts) VDD.
2) For power consumption: maximum capacitance at XLO (*Ca*) and at XHI (*Cb*), worst-case fast processing, low (0°C) temperature and high (5.5 volts) VDD.

Power Consumption

The curves below display the worst-case simulated power consumption of the oscillator cells as a function of frequency, for selected capacitor values at XLO and XHI. Note that for each set of capacitor values, there is an optimum frequency for power consumption. Above this frequency, power increases with capacitance and frequency, as is usual for CMOS. However, at lower frequencies, power again increases, due to increasing attenuation in the feedback network. A smaller signal level is available at the input of the CMOS inverter. This causes the P- and N-channel devices to remain simultaneously on during more of the waveform cycle, consuming higher d.c. power. Often, the power at low frequencies can be reduced by increasing capacitors *Ca* and *Cb*. This increases the amplitude of the waveform at the inverter input, and operates the stage in more of a switching mode, reducing the power consumption.



Crystal Oscillator

XC10MS[*D,1D,2D*]

1MHz-15MHz

FUNCTIONAL DESCRIPTION

The XC10MSD family of oscillators will provide stable rail-to-rail output waveforms suitable for clocking on-chip digital circuitry. The allowable frequency range, with proper capacitor selection, is from 1MHz to 15MHz. XC10MSD requires off-chip capacitors connected from each pad (XLO and XHI) to ground. XC10MS1D has on-chip 10pF capacitors connected from each pad to ground. XC10MS2D has on-chip 20pF capacitors connected from each pad to ground.

A fundamental mode quartz crystal of the desired frequency must be connected between pads XLO and XHI. The crystal is operated in parallel resonance.

XC10MS[D,1D,2D] may also be used as a non-inverting input buffer by applying an external CMOS-level clock to XLO. XHI must remain unconnected.

The frequency of oscillation of this cell depends on the crystal used and the total capacitance appearing at the crystal terminals. This capacitance includes wiring and package parasitics, as well as capacitors Ca and Cb (whether external or internal).

The oscillator cell heights are compatible with digital D and P style buffers.

NETLIST ORDER

INPUTS: XLO;
OUTPUTS: XHI,OUT;

FUNCTIONAL DESCRIPTION OF INPUTS AND OUTPUTS

XLO: Oscillator input: connection of one crystal terminal and capacitor if used as an oscillator; CMOS level input if used as an input buffer

XHI: Oscillator output: connection of one crystal terminal and capacitor if used as an oscillator; remains open if used as an input buffer

OUT: Output to clock on-chip circuitry

CIRCUIT INFORMATION

PARAMETER	XC10MS[D,1D,2D]		
FREQUENCY RANGE	1MHz† to 15MHz††		
OSCILLATOR POWER	SEE GENERAL INFORMATION, Page 9-12		
DUTY CYCLE	40% to 60%		
FREQ STABILITY vs VDD*	8ppm/V		
DELAY (RISING)**	0.88ns + 0.14ns/pF		
DELAY (FALLING)**	0.92ns + 0.15ns/pF		
CELL SIZE	592.25µ × 291.75µ		
ON-CHIP CAPACITANCE	**XC10MSD**	**XC10MS1D**	**XC10MS2D**
NODE XLO	1.9pF	12.0pF	22.0pF
NODE XHI	1.8pF	11.8pF	21.9pF

† Ca=Cb=50pF This minimum frequency assumes a maximum effective series crystal resistance of 500Ω. Crystal resistance rises rapidly at frequencies below 1MHz. Lower operating frequencies may be possible with larger Ca and Cb, but crystal resistance must be considered at frequencies below 1MHz. Also see the Negative Resistance graph for crystal resistances that will guarantee sufficient loop gain to oscillate.

†† Ca=Cb=10pF

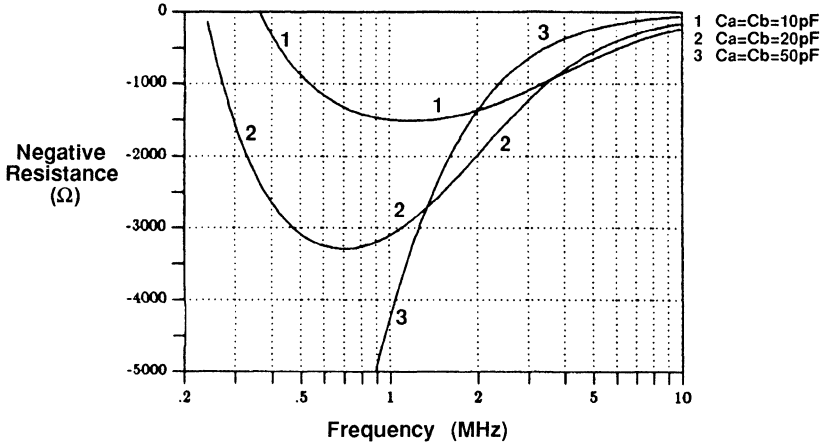
* Simulated with a typical 10MHz crystal having C1=0.02pF, C0=4pF, over a voltage range of 4.5 to 5.5 volts at 25°C, nominal process, and Ca=Cb=10pF. Actual stability depends on the crystal and values of Ca and Cb.

** From XLO to OUT, when used as an input buffer, with VDD=5V, T=25°C, nominal process.

Negative Resistance

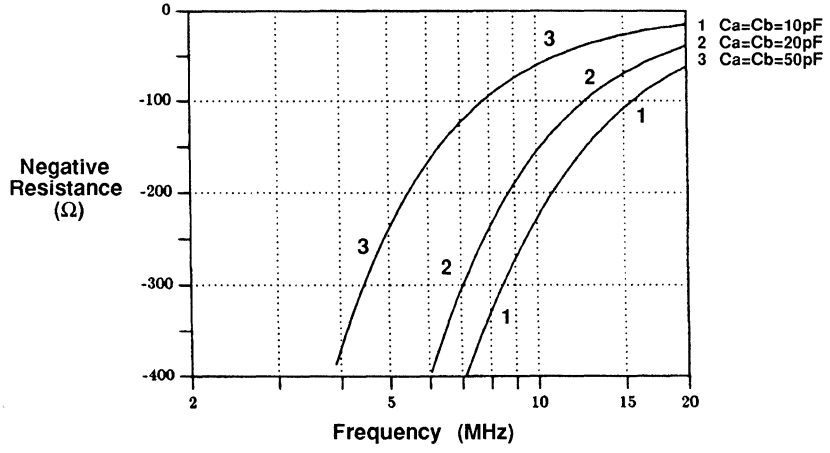
The real part of oscillator input impedance (including crystal shunt capacitance C0=7pF, oscillator capacitors Ca and Cb, and stray capacitances) is displayed as a function of frequency.

WORST-CASE* NEGATIVE RESISTANCE vs FREQUENCY



Negative Resistance (Expanded)

WORST-CASE* NEGATIVE RESISTANCE vs FREQUENCY



* Slow processing, VDD=4.5V, T=100°C

Crystal Oscillator

XC20MS[*D,1D,2D*]

5MHz-32MHz

FUNCTIONAL DESCRIPTION

The XC20MSD family of oscillators will provide stable rail-to-rail output waveforms suitable for clocking on-chip digital circuitry. The allowable frequency range, with proper capacitor selection, is from 5MHz to 32MHz. XC20MSD requires off-chip capacitors connected from each pad (XLO and XHI) to ground. XC20MS1D has on-chip 10pF capacitors connected from each pad to ground. XC20MS2D has on-chip 20pF capacitors connected from each pad to ground.

A fundamental mode quartz crystal of the desired frequency must be connected between pads XLO and XHI. The crystal is operated in parallel resonance.

XC20MS[D,1D,D2] may also be used as a non-inverting input buffer by applying an external CMOS-level clock to XLO. XHI must remain unconnected.

The frequency of oscillation of this cell depends on the crystal used and the total capacitance appearing at the crystal terminals. This capacitance includes wiring and package parasitics, as well as capacitors Ca and Cb (whether external or internal).

The oscillator cell heights are compatible with digital D and P style buffers.

NETLIST ORDER

INPUTS: XLO;
OUTPUTS: XHI,OUT;

FUNCTIONAL DESCRIPTION OF INPUTS AND OUTPUTS

XLO: Oscillator input: connection of one crystal terminal and capacitor if used as an oscillator; CMOS level input if used as an input buffer

XHI: Oscillator output: connection of one crystal terminal and capacitor if used as an oscillator; remains open if used as an input buffer

OUT: Output to clock on-chip circuitry

CIRCUIT INFORMATION

PARAMETER	XC20MS[D,1D,2D]		
FREQUENCY RANGE	5MHz† to 32MHz††		
OSCILLATOR POWER	SEE GENERAL INFORMATION, Page 9-12		
DUTY CYCLE	40% to 60%		
FREQ STABILITY vs VDD*	5ppm/V		
DELAY (RISING)**	0.66ns + 0.14ns/pF		
DELAY (FALLING)**	0.72ns + 0.15ns/pF		
CELL SIZE	592.25µ x 291.75µ		
ON-CHIP CAPACITANCE	**XC20MSD**	**XC20MS1D**	**XC20MS2D**
NODE XLO	2.0pF	12.1pF	22.1pF
NODE XHI	1.8pF	11.8pF	21.9pF

† Ca=Cb=50pF (Lower operating frequencies can be obtained with larger Ca and Cb).

†† Ca=Cb=10pF

* Simulated with a typical 20MHz crystal having C1=0.02pF, C0=4pF, over a voltage range of 4.5 to 5.5 volts at 25°C, nominal process, and Ca=Cb=10pF. Actual stability depends on the crystal and values of Ca and Cb.

** From XLO to OUT, when used as an input buffer, with VDD=5V, T=25°C, nominal process.

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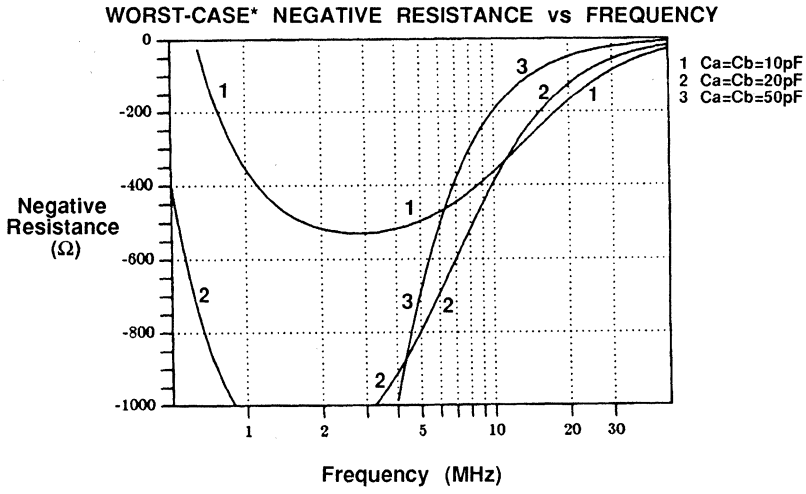
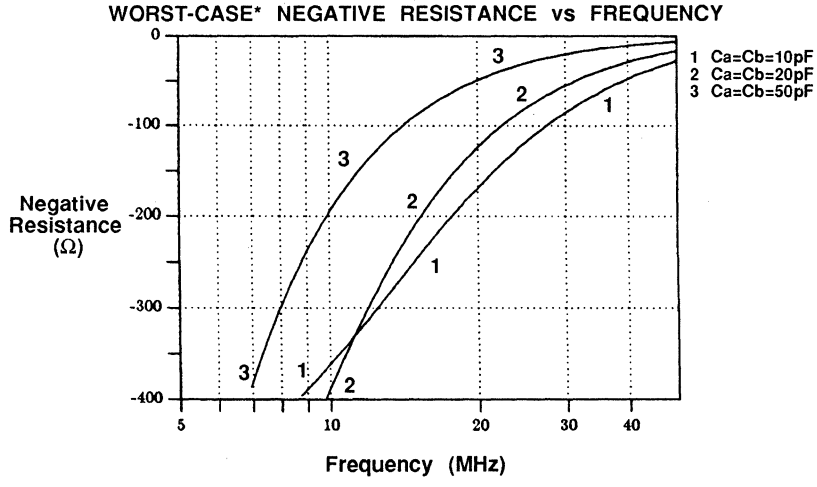
5MHz-32MHz

Negative Resistance

The real part of oscillator input impedance (including crystal shunt capacitance C0=7pF, oscillator capacitors Ca and Cb, and stray capacitances) is displayed as a function of frequency.



Negative Resistance (Expanded)



* Slow processing, VDD=4.5V, T=100°C

Crystal Oscillator

XT20MS[*D,3D*]

4MHz-32MHz

FUNCTIONAL DESCRIPTION

The XT20MSD family of oscillators will provide stable rail-to-rail output waveforms suitable for clocking on-chip digital circuitry. The allowable frequency range, with proper capacitor selection, is from 4MHz to 32MHz. XT20MSD requires off-chip capacitors connected from each pad (XLO and XHI) to ground. XT20MS3D has an on-chip 30pF capacitor connected from XLO to ground, and a 10pF on-chip capacitor connected from XHI to ground.

A fundamental mode quartz crystal of the desired frequency must be connected between pads XLO and XHI. The crystal is operated in parallel resonance.

XT20MS[D,3D] may also be used as a non-inverting input buffer by applying an external TTL-level clock to XLO. XHI must remain unconnected.

The frequency of oscillation of this cell depends on the crystal used and the total capacitance appearing at the crystal terminals. This capacitance includes wiring and package parasitics, as well as capacitors Ca and Cb (whether external or internal).

The oscillator cell heights are compatible with digital D and P style buffers.

NETLIST ORDER

INPUTS: XLO;
OUTPUTS: XHI,OUT;

FUNCTIONAL DESCRIPTION OF INPUTS AND OUTPUTS

XLO: Oscillator input: connection of one crystal terminal and capacitor if used as an oscillator; TTL level input if used as an input buffer

XHI: Oscillator output: connection of one crystal terminal and external capacitor if used as an oscillator; remains open if used as an input buffer

OUT: Output to clock on-chip circuitry

CIRCUIT INFORMATION

PARAMETER	XT20MS[D,3D]	
FREQUENCY RANGE	4MHz† to 32MHz††	
OSCILLATOR POWER	SEE GENERAL INFORMATION, Page 9-12	
BUFFER DC POWER†††	97.5mW	
DUTY CYCLE	40% to 60%	
FREQ STABILITY vs VDD*	8ppm/V	
DELAY (RISING)**	0.55ns + 0.17ns/pF	
DELAY (FALLING)**	0.84ns + 0.22ns/pF	
CELL SIZE	668.75µ × 291.75µ	
ON CHIP CAPACITANCE	**XT20MSD**	**XT20MS3D**
NODE XLO	2.4pF	32.4pF
NODE XHI	2.0pF	12.1pF

† Ca=120pF, Cb=40pF (Lower operating frequencies can be obtained with larger Ca and Cb).

†† Ca=30pF, Cb=10pF

††† With XLO held at 2.0V, VDD=5.5V, T=0°C, fast process.

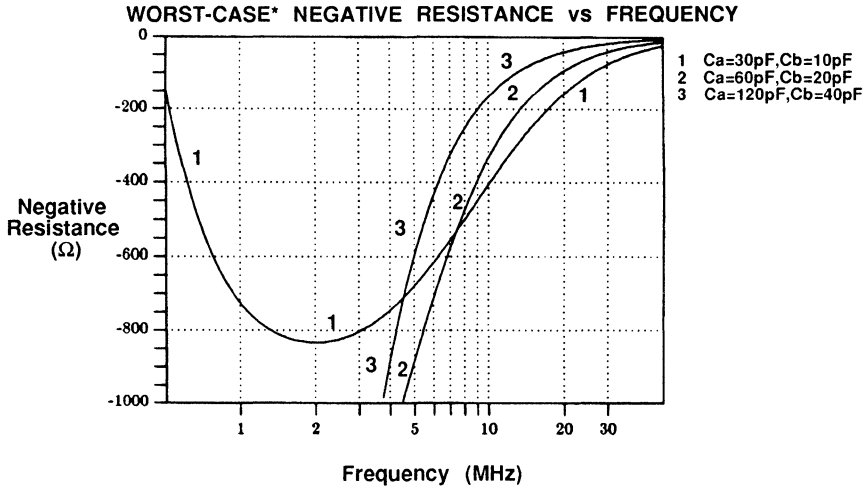
* Simulated with a typical 20MHz crystal having C1=0.02pF, C0=4pF, over a voltage range of 4.5 to 5.5 volts at 25°C, nominal process, and Ca=30pF, Cb=10pF. Actual stability depends on the crystal and values of Ca and Cb.

** From XLO to OUT, when used as an input buffer, with VDD=5V, T=25°C, nominal process.

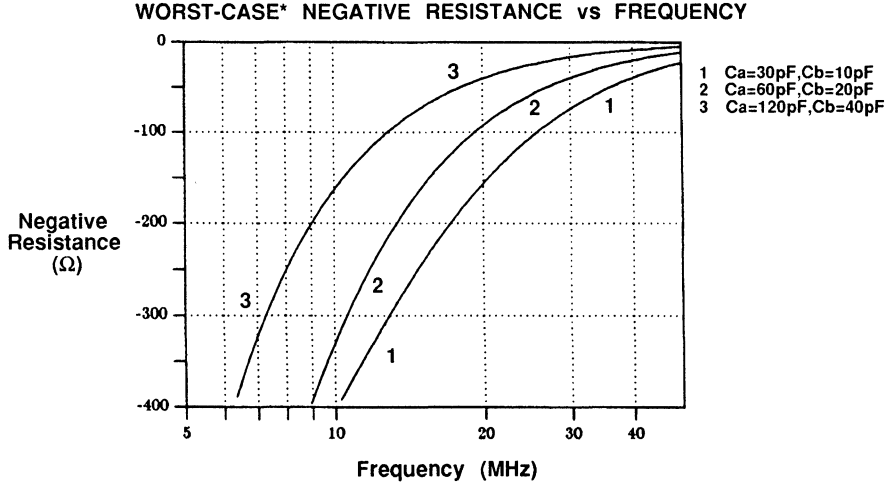
4MHz-32MHz

Negative Resistance

The real part of oscillator input impedance (including crystal shunt capacitance C0=7pF, oscillator capacitors Ca and Cb, and stray capacitances) is displayed as a function of frequency.



Negative Resistance (Expanded)



* Slow processing, VDD=4.5V, T=100°C

Capacitors

CAP[*3A,5A,10A,3P,5P,10P*]

For Area and Performance-Optimized Standard Cells

FUNCTIONAL DESCRIPTION

Unlike most Linear Standard Cells, these capacitors are meant to be used in standard cell rows rather than in the I/O buffer region. *The rows occupied by these cells must be separated by at least four routing tracks (≥ 10μm) from other rows, or any special cells.*

The normal process-induced variation is ±5%.

The capacitors are modeled in ADVICE as p-channel transistors with L=20μm. The transistor width selected is such that the gate area gives the desired value of capacitance. Process variation of the capacitance is caused by gate oxide variation. The gate oxide, TOX, is defined in the process files, thus using the worst-case fast and slow transistor files, aprohc.dat and aprolc.dat, will automatically give the proper capacitance variation due to processing.

The bottom plate of the capacitor is tied to VSS. Thus physically, capacitors have only one terminal. A second terminal has been appended, though, in order to make the capacitors more amenable to digital CAD tools.

NETLIST ORDER

INPUTS: A;
OUTPUTS: Z;

CELL INFORMATION

CELL NAME	CAP VALUE	NUMBER OF GRIDS
AREA OPTIMIZED		
CAP3A	3pF	20
CAP5A	5pF	28
CAP10A	10pF	48
PERFORMANCE OPTIMIZED		
CAP3P	3pF	14
CAP5P	5pF	18
CAP10P	10pF	28

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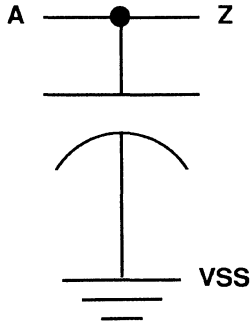
SCHEMA SYMBOL



RC Delay Lines

RC[*1-10*][*A,P*]

For Area and Performance-Optimized Standard Cells

FUNCTIONAL DESCRIPTION

The integrated RC Delay Lines have nominal time constants ranging from 1ns for RC[1A,1P] to 10ns for RC[10A,10P]. The basic element in each cell is a 500 ohm N+ resistor and a 2pF gate oxide capacitor. For these relatively small RC delay times, the integrated delay lines occupy less than half the space that would be needed by separate resistor and capacitor cells in the Linear Library. *The rows occupied by these cells must be separated by at least four routing tracks (≥ 10μm) from other rows, or any special cells.*

The actual delay through an RC line is not simply equal to the RC product. It is necessary to make an ADVICE run, which must include all logic elements and stray capacitances connected to the RC line, to find the actual delay.

Normal process-induced resistor variation is ±20%. The best way to do worst-case fast and slow ADVICE runs with resistors is to change the resistor model parameter ***SCAL***. The resistor model, NPLUS, is defined so that all resistors can be globally scaled with the single command:

.MODEL NPLUS SCAL=1.2 ("slow resistors")

or

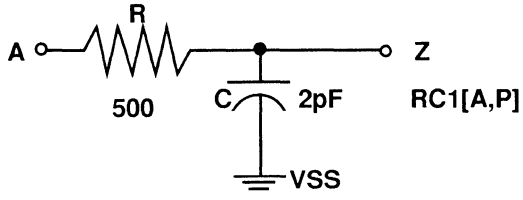
.MODEL NPLUS SCAL=0.8 ("fast resistors")

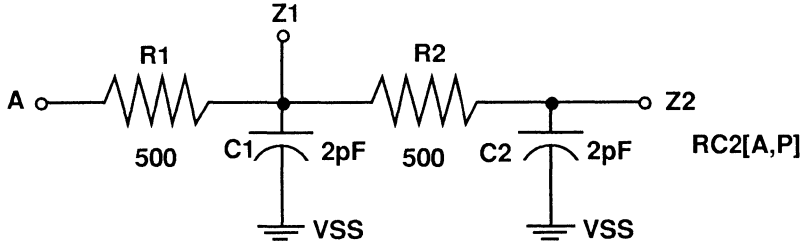
Unfortunately, the process-induced resistor variation does not correlate with transistor speed. This means that while using aprolc.dat and .MODEL NPLUS SCAL=1.2 will give maximum delay, and aprohc.dat and .MODEL NPLUS SCAL=0.8 will give a minimum delay, the other two combinations of process and resistor speeds may have to be investigated for paths where critical races are possible.

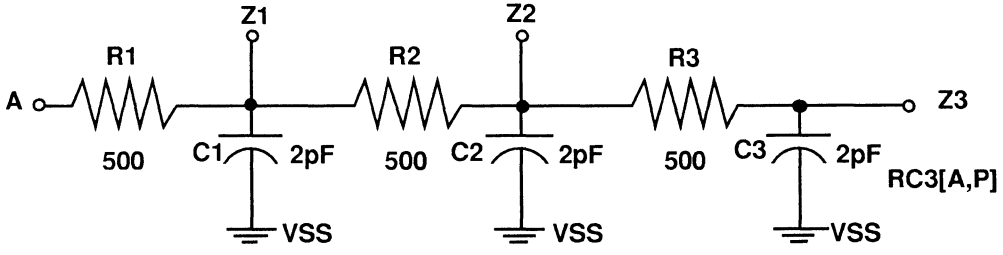
CELL INFORMATION

CELL NAME	NOMINAL RC PRODUCT	NUMBER OF GRIDS	INPUT	OUTPUTS
AREA OPTIMIZED				
RC1A	1ns	21	A	Z
RC2A	2ns	36	A	Z1,Z2
RC3A	3ns	51	A	Z1,Z2,Z3
RC4A	4ns	66	A	Z1,Z2,Z3,Z4
RC5A	5ns	81	A	Z1,Z2,Z3,Z4,Z5
RC6A	6ns	96	A	Z1,Z2,.....,Z6
RC7A	7ns	111	A	Z1,Z2,.....,Z7
RC8A	8ns	126	A	Z1,Z2,.....,Z8
RC9A	9ns	141	A	Z1,Z2,.....,Z9
RC10A	10ns	156	A	Z1,Z2,.....,Z10
PERFORMANCE OPTIMIZED				
RC1P	1ns	21	A	Z
RC2P	2ns	36	A	Z1,Z2
RC3P	3ns	51	A	Z1,Z2,Z3
RC4P	4ns	66	A	Z1,Z2,Z3,Z4
RC5P	5ns	81	A	Z1,Z2,Z3,Z4,Z5
RC6P	6ns	96	A	Z1,Z2,.....,Z6
RC7P	7ns	111	A	Z1,Z2,.....,Z7
RC8P	8ns	126	A	Z1,Z2,.....,Z8
RC9P	9ns	141	A	Z1,Z2,.....,Z9
RC10P	10ns	156	A	Z1,Z2,.....,Z10

SCHEMA Symbols of RC[1-3][A,P]







Although they are not pictured, similar symbols exist for RC[4-10][A,P].

9

Resistors

For Area and Performance-Optimized Standard Cells

RES[*1A,2A,5A,10A,20A, 1P,2P,5P,10P,20P*]

FUNCTIONAL DESCRIPTION

Unlike most Linear Standard Cells, these resistors are meant to be used in standard cell rows rather than in the I/O buffer region.

The normal process-induced variation is ±30%. The best way to do worst-case fast and slow ADVICE runs with resistors is to change the resistor model parameter ***SCAL***. The resistor model, PPLUS, is defined so that all resistors can be globally scaled with a single command:

.MODEL PPLUS SCAL=1.3 ("slow resistors")

or

.MODEL PPLUS SCAL=0.7 ("fast resistors")

The value of ***SCAL*** is initialized as 1.0 in the file advldev.dat. When changing the resistor scale be sure that the temperature is first set to 25°C, then change the resistor scale to the desired value, and then reset the temperature to its operating value. Failure to follow this sequence will result in ADVICE doing strange things to the resistor values. Unfortunately, the process-induced resistor variation does not correlate with the transistor speed. This means that while the use of aprolc.dat and .MODEL PPLUS SCAL=1.3 will give the maximum delay, and aprohc.dat and .MODEL PPLUS SCAL=0.7 will give the minimum delay, the other two combinations of transistor and resistor speeds may have to be investigated for paths where critical races are possible. Temperature and voltage variations are included in the PPLUS model.

NETLIST ORDER

INPUTS: A;

OUTPUTS: Z;

CELL INFORMATION

CELL NAME	NOMINAL RES VALUE	NUMBER OF GRIDS
AREA OPTIMIZED		
RES1A	1K	10
RES2A	2K	11
RES5A	5K	16
RES10A	10K	24
RES20A	20K	40
PERFORMANCE OPTIMIZED		
RES1P	1K	8
RES2P	2K	9
RES5P	5K	12
RES10P	10K	18
RES20P	20K	30

SCHEMA SYMBOL

Differential Line Receiver

With Fixed Input Threshold

DRECV1A

FUNCTIONAL DESCRIPTION

This circuit meets the CCITT input specifications for ISDN T or S interfaces. It is designed to work with a transformer whose turns ratio is between 1:1 and 1:5. The threshold of the circuit, V_{th}, is mask programmable, and should be directly proportional to this turns ratio. The default value of V_{th} for a turns ratio of 1:2.5 and VDD=5V, is 0.155V.

The subcircuit CP07 from the linear CMOS library must be used with DRECV1A in order to run ADVICE.

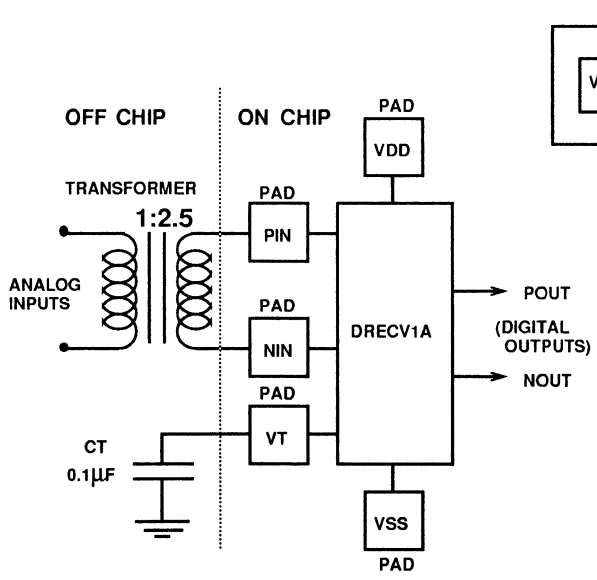
NETLIST ORDER

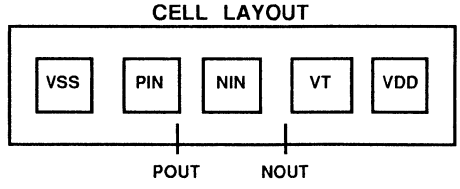
INPUTS: PIN,NIN,VT;
OUTPUTS: POUT,NOUT;

CIRCUIT INFORMATION

PARAMETER	DRECV1A
MAX POWER	2.4mW
MAX DELAY	0.20µs (with 1pF load)
MIN INPUT IMPEDANCE	100K
MAX INPUT CAPACITANCE	10pF
POWER SUPPLY	5V ± 5%
CELL SIZE	1600µ × 300.25µ

INPUT SIGNALS	POUT	NOUT
$-V_{th}<(PIN-NIN)<V_{th}$	0	0
$(PIN-NIN)< -V_{th}$	0	1
$(PIN-NIN)>V_{th}$	1	0





9

Transmitter

DXMIT2C

Tri-state, Voltage Limited Current Source Transmitter for ISDN S or T Interfaces

FUNCTIONAL DESCRIPTION

This circuit meets CCITT output specifications for ISDN S or T interfaces. It must be used with a transformer whose turns ratio is 2.5:1, and external resistors.

The subcircuits OPO3, SNR2, SINRB, and SXNOR from the linear CMOS library must be used with DXMIT2C in order to run ADVICE.

NETLIST ORDER

INPUTS: PIN,NIN,VT;
OUTPUTS: POUT,NOUT;

CIRCUIT INFORMATION

PARAMETER	DRECV1A
MAX DELAY	150µs (with 200pF load)
MAX OUTPUT CAPACITANCE	10pF
POWER SUPPLY	5V ±5%
CELL SIZE	1350µ × 553.25µ

INPUTS		OUTPUT VOLTAGES		OUTPUT
PIN	NIN	POUT	NOUT	LOGIC
0	0	Z*	Z*	1
0	1	NOUT-1.875V**	NOUT	0
1	0	NOUT+1.875V**	NOUT	0
1	1	Z*	Z*	1

* Z=TRI-STATE

** This reflects to 0.75V on the line side of the transformer.

WORST-CASE POWER †	1.875V OUTPUT	OUTPUT=Z	
		LP=HIGH	LP=LOW
ELECTRICAL	39mW	3.4mW	1.3mW
THERMAL	25mW	3.4mW	1.3mW

† The difference between electrical and thermal power on the chip is due to the power consumed in the external components.

APPLICATION NOTES (Refer to the figure on the following page)

LP is a low power option. It must be held high during logic "0". During logic "1" it can remain high, or be set low to conserve power. If it is set low in this state, it must be set high at least 500ns before logic "0" can be sent, and must remain high for at least 100ns after logic "0" is removed.

R_B and R_C are 5% external resistors whose value depends on the maximum specified temperature.

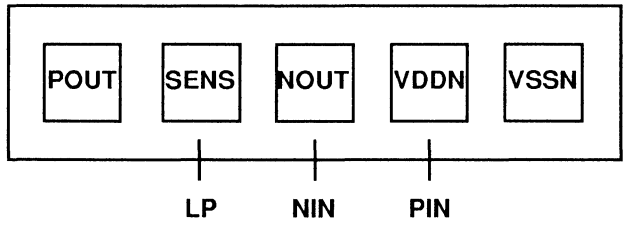
For circuits with a junction temperature not exceeding 80°C, $R_B=R_C \leq 30\ \Omega$.

For circuits with a junction temperature not exceeding 100°C, $R_B=R_C \leq 25\ \Omega$.

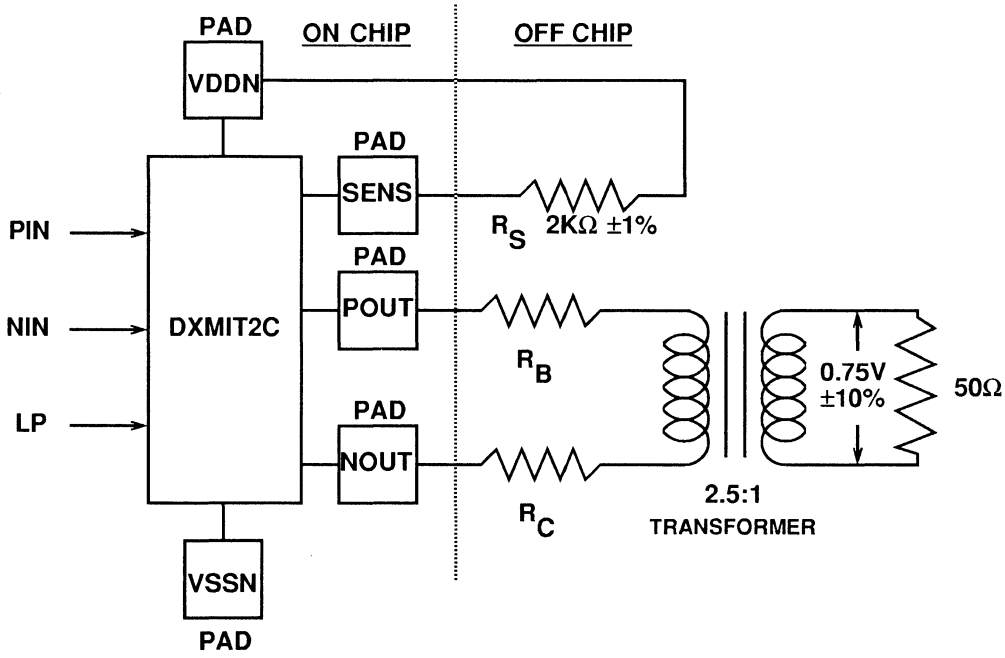
Transmitter

Tri-state, Voltage Limited Current Source Transmitter for ISDN S or T Interface

CELL LAYOUT



CIRCUIT DIAGRAM



9

BiCMOS Cells

Section 10

AT&T

Contents - Section 10

I. Introduction

AT&T now offers a BiCMOS technology option. The BiCMOS cells currently available are a series of ECL buffers. ECL (Emitter Coupled Logic) is a well known bipolar circuit technique which is extensively used in high speed systems. Its main attractions are low noise, good capacitive drive capability, and very high speed. ECL is also capable of driving low impedance lines with either single-ended or balanced (differential) signals. Its main drawback is its very high power consumption. Some systems, which do not need the high speed performance available with ECL, would like to move away from the high power, relatively low density ECL standard cells to low power, high density CMOS. The problem with this retrofit, which has been extensively done with TTL level chips, is the difficulty that CMOS circuits have in driving ECL levels, and thus in allowing direct interface with existing ECL systems.

The main problem interfacing TTL and ECL levels is that TTL levels are positive and ECL levels are negative, as illustrated in figure 1. Thus CMOS chips need a translator chip to communicate with ECL systems, as shown in figure 2. Our "10 volt" TTL compatible BiCMOS ECL buffers enable a chip to communicate with both TTL and ECL levels at the same time. They are called 10 volt buffers because they require the use of two power supplies: +5 volts and -5 volts.

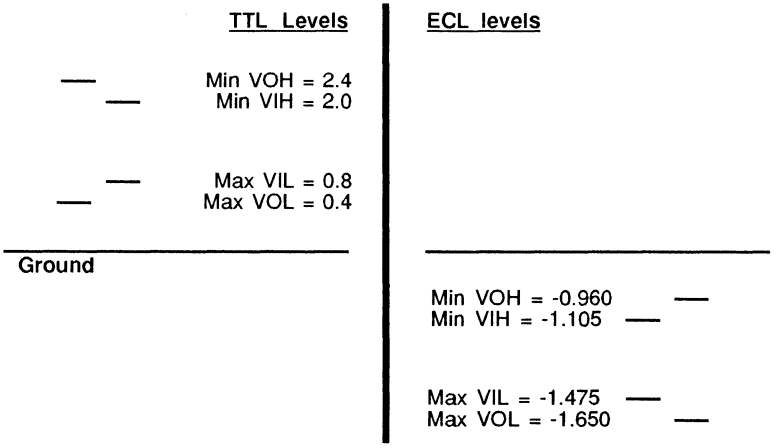


Figure 1. Comparison of ECL and TTL levels.

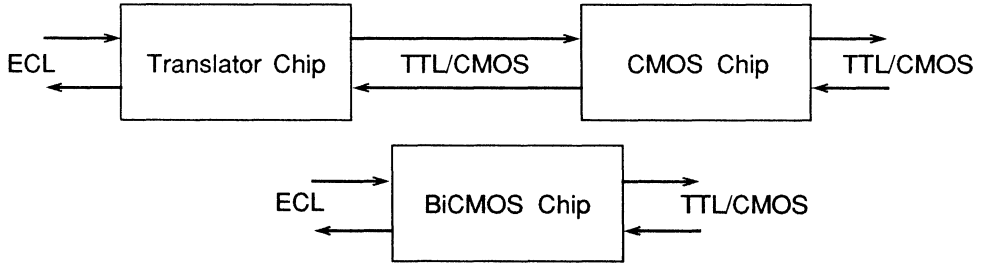


Figure 2. ECL level signals to CMOS and BiCMOS chips.

If it is not necessary to communicate with both real TTL and ECL levels, another option is the "5 volt" ECL buffers. These operate off a single power supply, either +5 volts or -5 volts, depending on the system. In the former case the chip can communicate with true TTL levels and with "pseudo" ECL levels. When a -5 volt supply is used, the chip can communicate with real ECL levels and with "pseudo" TTL levels, as shown in figure 3.

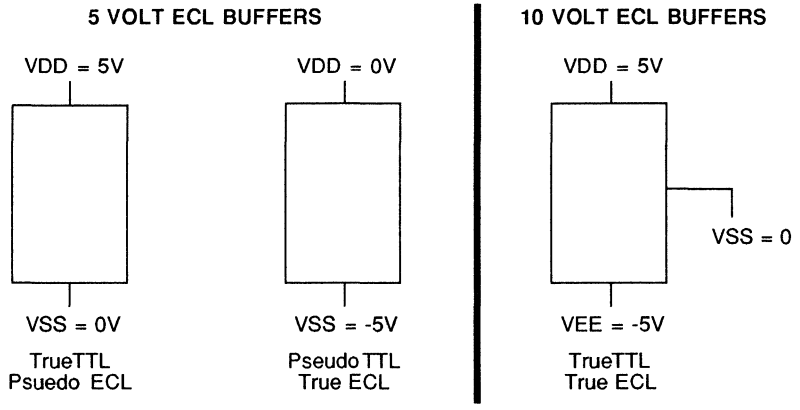


Figure 3. Possible BiCMOS ECL chip configurations.

All ECL Buffers are compatible with the 10K and 10KH level specifications. All of the ECL buffers except the BIET07T, are also compatible with 100K level specifications. This buffer, however, can be modified to meet the 100K specifications.

II. BiCMOS Process and Transistor Structure

The 1.25µ BiCMOS process used in these circuits adds only a single mask step (base implant) to the standard CMOS process. The npn transistor has a measured ft of 3.8GHz and a typical current gain of 100.

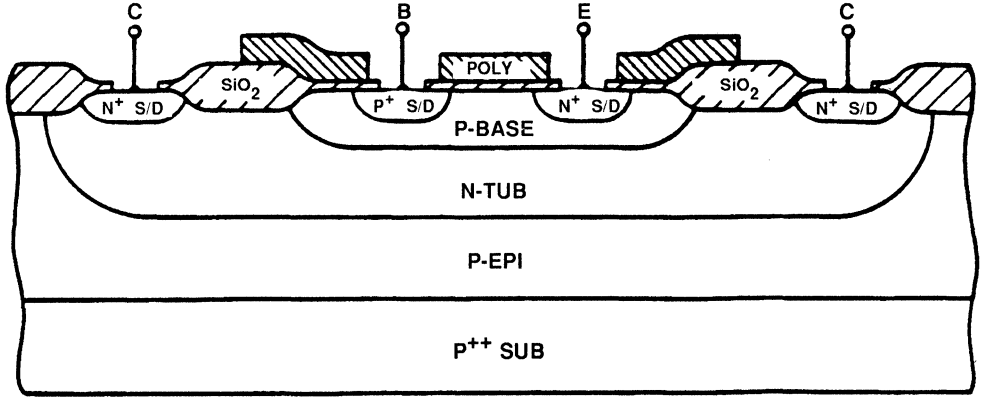


Figure 4. Simplified npn cross-section.

A cross section of the npn transistor is shown in figure 4. The collector of the npn is formed by the N-tub of the CMOS P-channel. *This collector has a nominal sheet resistance of 625 ohms/sq, which results in relatively high collector resistance.* The base is made using a special implant that is not used anywhere else in the CMOS process. This allows the base implant to be optimized for the bipolar transistor without any adverse effect on the MOS transistor properties. The base contact is the P^+ Source/Drain implant, and the emitter is the N^+ Source/Drain implant.

III. Physical Size and Placement of ECL Buffers.

A listing of the ECL buffers that are available is shown in Tables I through IV. Note that these buffers are made in a tall configuration. This is necessary because of the large number of busses that are needed. It should also be noted that input and output buffers are of different height. This serves as a forceful reminder that output and input buffers must be placed in separate physical locations from each other and from any TTL buffers, since the bus structures are mutually incompatible. This results in a certain loss of flexibility compared to TTL buffers, in which input and outputs can be placed on a "mix-and-match" basis (subject to noise considerations!).

Name	Type	Prop Delay *			DC Power	
		WC Slow**	Nom.	WC Fast***	WC Fast***	Nom.
BIEF09T	Input	7.5 ns	5.0 ns	3.2ns	24 mW	14 mW
BIEF14T	Input	12.0 ns	7.5 ns	4.7ns	12 mW	7 mW
BIEF16T	Input	13.0 ns	8.0 ns	5.3ns	8 mW	4 mW
BIEBF09T	Balanced Input	7.4 ns	5.0 ns	3.1ns	24 mW	14 mW
BOEF05T	Output	3.5 ns	2.0 ns	1.6ns	22 mW	13 mW
BOEBF05T	Balanced Output	3.9 ns	2.0 ns	1.8ns	44 mW	26 mW
BE16F05V	Bidirectional	+	+	+	+	+

Table I. 5 Volt ECL Buffers; prop delay and power, at 50% duty cycle.

* Prop Delay with CL=5pF for Input Buffers, 50pF for Output Buffers

** WC Slow: Slow process, VDD=4.5 volts, T=100°C.

*** WC Fast: Fast process, VDD=5.5 volts, T=0°C.

+ Use BIEF16T and BOEF05T specs

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Name	Type	Size (μ)	Pad Cap.
BIEF09T	Input	175 x 527.25	4 pF
BIEF14T	Input	175 x 527.25	4 pF
BIEF16T	Input	175 x 527.25	4 pF
BIEBF09T	Balanced Input	350 x 527.25	4.4 pF
BOEF05T	Output	200 x 571.875	6.8 pF
BOEBF05T	Balanced Output	400 x 571.875	6.8 pF
BE16F05V	Bidirectional	202 x 885	7 pF

Table II. 5 Volt ECL Buffers; size and pad capacitance.

Name	Type	Prop. Delay*			DC Power	
		WC Slow**	Nom.	WC Fast***	WC Fast***	Nom.
BIET07T	Input	7.6 ns	4.8 ns	3.2 ns	23 mW	12 mW
BIEBT07T	Balanced Input	7.4 ns	4.8 ns	3.2 ns	23 mW	12 mW
BOET05T	Output	5.5 ns	3.9 ns	2.4 ns	35 mW	24 mW
BOEBT05T	Balanced Output	6.2 ns	4.0 ns	2.7 ns	70 mW	48 mW

Table III. 10 Volt ECL Buffers; prop. delay and power, at 50% duty cycle.

* Prop. Delay with CL=5 pF for Input Buffers, 50 pF for Output Buffers

** WC Slow: Slow process, VDD=4.5 volts, VEE=-4.5 volts, T=100 ° C.

***WC Fast: Fast process, VDD=5.5 volts, VEE=-5.5 volts, T=0 ° C.

Name	Type	Size (μ)	Pad Cap.
BIET07T	Input	175 x 527	4.2 pF
BIEBT07T	Balanced Input	350 x 527	4.2 pF
BOET05T	Output	253.75 x 591	6.8 pF
BOEBT05T	Balanced Output	483.5 x 591	6.8 pF

Table IV. 10 Volt ECL Buffers; size and pad capacitance.

The most widespread use of ECL buffers is in I/O intensive chips. The large number of busses needed for ECL, combined with the large currents that the circuits must handle, make it necessary to use two-level metal in laying out these buffers.

As an aid in connecting the many different power/ground busses, a number of ancillary "Pad Cells" have been built. These are listed in Tables V and VI, along with the requirements on the maximum number of buffers that these pads can support. These limits are due to either the maximum DC voltage drops allowable or the maximum current density allowed to ensure good reliability.

Buffer type	Bus name	Cell name	Max. # buffers/Pad Cell
Input	VSQIF	VSQIFPAD	12 *
Input	VDQIF	VDQIFPAD	12 *
Input	VSS	VSSIFPAD +	20 *
Input	VDD	VDDIFPAD++	no limits
Input	-	CORIF	corner bus routing
Output	VDQOF	VDQOFPAD	12
Output	VDNOF	VDNOFPAD	8 **
Output	VSS	VSSOFPAD +	12
Output	VDD	VDDOFPAD ++	no limits
Output	-	COROF	corner bus routing
Bidirectional	VSQBF	VSQBFPAD	18
Bidirectional	VDQBF	VDQBFPAD	18
Bidirectional	VDNBF	VDNBFPAD	8 **
Bidirectional	VSS	VSSBFPAD +	12
Bidirectional	VDD	VDDBFPAD ++	no limits
Bidirectional	-	CORBF	corner bus routing

Table V. 5 volt ECL Ancillary Cells for Power/Ground Pads and Chip Corner Routing.

* These numbers are for BIEF09T. For each BIEF09T one can substitute 2 BIEF14T or 3 BIEF16T buffers.

** This depends on package resistance. These numbers assume a dedicated ground plane in the package and/or a total lead resistance less than 0.15 ohm.

+ This pad may also be used to route VSS to the standard cell area.

++ This pad may also be used to route VDD to the standard cell area.

Buffer type	Bus name	Cell name	Max. # buffers/Pad Cell
Input	VSQIT	VSQITPAD	20
Input	VEEI	VEEIPAD	20
Input	VSS	VSSITPAD*	20
Input	VDD	VDDITPAD**	20
Input	-	CORIT	corner bus routing
Output	VSQOT	VSQOTPAD	20
Output	VSNOT	VSNOTPAD	8 ***
Output	VEEO	VEEOPAD	20
Output	VDD	VDDOTPAD**	20
Output	-	COROT	corner bus routing

Table VI. 10 volt ECL Ancillary Cells for Power/Ground Pads and Chip Corner Routing.

* This pad may also be used to route VSS to the standard cell area.

** This pad may also be used to route VDD to the standard cell area.

*** This depends on package resistance. These numbers assume a dedicated ground plane in the package and/or a total lead resistance less than 0.15 ohm.

The "5 volt" ECL circuits require the use of the Reference Voltage Generator CS4T. This cell fits physically into the ECL Input buffer row, and provides all of the necessary reference voltage levels to run the 5 volt input, output, and bidirectional buffers. The "10 volt" ECL buffers do not need this circuit, as all reference voltages are provided by resistor dividers built into each buffer.

IV. CAD tools available for ECL Buffers.

These ECL buffers are compatible with all of the standard CAD tools; ADVICE, LARC, SCHEMA, MOTIS3, LTX2, and testing on the Takeda with TPG2. All ADVICE simulations were done using HCAP generated files.

Anyone wishing to run ADVICE simulations on 5 volt ECL buffers MUST use the support files BEF.LO (for WC slow conditions) or BEF.HI (for BC fast conditions). For the 10 volt ECL buffers the corresponding files BET.LO or BET.HI must be used. In addition, the bipolar transistor process files BIMOD.LO (slow) or BIMOD.HI (fast) must be used with all ECL circuits.

BiCMOS Input Buffer

BIEBF09T

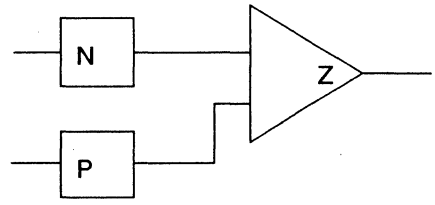
Balanced, 5 volt

CELL SIZE: X = 350 μ
Y = 527.25 μ

NETLIST ORDER

INPUTS: N,P;
OUTPUTS: Z;

SCHEMA SYMBOL



TRUTH TABLE

P	N	Z
0	1	0
1	0	1

CAPACITANCES

NODE	CAPACITANCE
N,P	4.4 pF

CIRCUIT INFORMATION

PARAMETER	VALUE
WC DC Power*	24 mW
WC Slow Intrinsic Delay**	5.0 ns
WC Fast Intrinsic Delay*	2.16 ns
WC Slow Extrinsic Delay**	0.46 ns/pF
WC Fast Extrinsic Delay*	0.18 ns/pF

*VDD= 5.5V, T= 0°C,Fast Process
**VDD= 4.5V, T= 100°C, Slow Process

POWER SUPPLY INFORMATION

VDD = 5 volts ± 10%
VSS = 0 volts

This allows the chip to communicate with true TTL/CMOS levels, but only with "pseudo" ECL levels. See Introduction for more details.

OR

VDD = 0
VSS = -5 volts ± 10%

This allows the chip to communicate with true ECL levels but only with "pseudo" TTL or CMOS levels. See Introduction for more details.

Note: The Reference Voltage Generator CS4T must be used with this cell.

10

BiCMOS Input Buffer

BIEBT07T

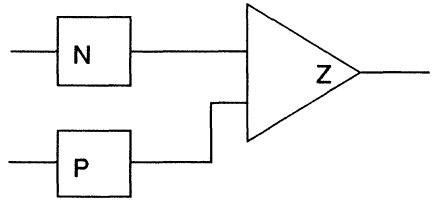
Balanced, 10 volt

CELL SIZE: X = 350 μ
Y = 527 μ

NETLIST ORDER

INPUTS: N,P;
OUTPUTS: Z;

SCHEMA SYMBOL



TRUTH TABLE

P	N	Z
0	1	0
1	0	1

CAPACITANCES

NODE	CAPACITANCE
N,P	4.2 pF

CIRCUIT INFORMATION

PARAMETER	VALUE
WC DC Power*	23 mW
WC Slow Intrinsic Delay**	5.8 ns
WC Fast Intrinsic Delay*	2.5 ns
WC Slow Extrinsic Delay**	0.32 ns/pF
WC Fast Extrinsic Delay*	0.13 ns/pF

*VDD= 5.5V, VEE= -5.5V, T= 0°C,Fast Process
**VDD= 4.5V, VEE= -4.5V, T= 100°C, Slow Process

10

POWER SUPPLY INFORMATION

VDD = 5 volts ± 10%
VSS = 0 volts
VEE = -5 volts ± 10%

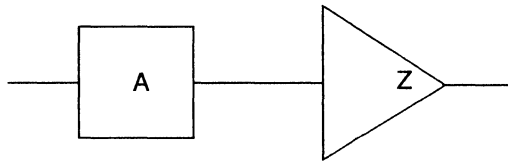
BiCMOS Input Buffer

BIEF[*09T,14T,16T*]

Non-inverting, 5 volt

CELL SIZE: X = 175 μ
Y = 527.25 μ

SCHEMA SYMBOL



NETLIST ORDER

INPUTS: A;
OUTPUTS: Z;

TRUTH TABLE

A	Z
0	0
1	1

CAPACITANCES

NODE	CAPACITANCE
A	4 pF

CIRCUIT INFORMATION

PARAMETER	BIEF09T	BIEF14T	BIEF16T
WC DC Power*	24 mW	12 mW	8 mW
WC Slow Intrinsic Delay**	5.20 ns	7.75 ns	8.75 ns
WC Fast Intrinsic Delay*	2.24 ns	2.98 ns	3.56 ns
WC Slow Extrinsic Delay**	0.46 ns/pF	0.85 ns/pF	0.85 ns/pF
WC Fast Extrinsic Delay*	0.18 ns/pF	0.33 ns/pF	0.33 ns/pF

*VDD= 5.5V, T= 0°C,Fast Process
**VDD= 4.5V, T= 100°C, Slow Process

POWER SUPPLY INFORMATION

VDD = 5 volts ± 10%
VSS = 0 volts

This allows the chip to communicate with true TTL/CMOS levels, but only with "pseudo" ECL levels. See Introduction for more details.

OR

VDD = 0
VSS = -5 volts ± 10%

This allows the chip to communicate with true ECL levels but only with "pseudo" TTL or CMOS levels. See Introduction for more details.

Note: The Reference Voltage Generator CS4T must be used with this cell.

BiCMOS Input Buffer

BIET07T

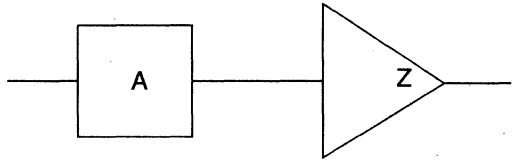
Non-inverting, 10 volt

CELL SIZE: X = 175 μ
Y = 527 μ

NETLIST ORDER

INPUTS: A;
OUTPUTS: Z;

SCHEMA SYMBOL



TRUTH TABLE

A	Z
0	0
1	1

CAPACITANCES

NODE	CAPACITANCE
A	4.2 pF

CIRCUIT INFORMATION

PARAMETER	VALUE
WC DC Power*	23 mW
WC Slow Intrinsic Delay**	6.0 ns
WC Fast Intrinsic Delay*	2.6 ns
WC Slow Extrinsic Delay**	0.33 ns/pF
WC Fast Extrinsic Delay*	0.13 ns/pF

*VDD= 5.5V, VEE= -5.5V, T= 0°C,Fast Process
**VDD= 4.5V, VEE= -4.5V, T= 100°C, Slow Process

10

POWER SUPPLY INFORMATION

VDD = 5 volts ± 10%
VSS = 0 volts
VEE = -5 volts ± 10%

BiCMOS Output Buffer

BOEBF05T

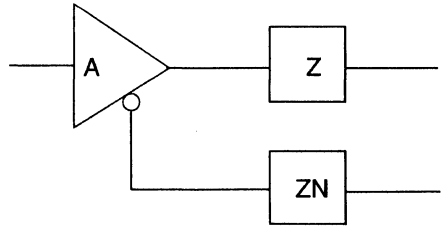
Balanced, 5 volt

CELL SIZE: X = 400 μ
Y = 571.875 μ

NETLIST ORDER

INPUTS: A;
OUTPUTS: Z,ZN;

SCHEMA SYMBOL



TRUTH TABLE

A	Z	ZN
0	0	1
1	1	0

CAPACITANCES

NODE	CAPACITANCE
A	0.22 pF
Z,ZN	6.8 pF

CIRCUIT INFORMATION

PARAMETER	VALUE
WC DC Power*	44 mW
WC Slow Intrinsic Delay**	2.91 ns
WC Fast Intrinsic Delay*	1.05 ns
WC Slow Extrinsic Delay**	0.019 ns/pF
WC Fast Extrinsic Delay*	0.014 ns/pF

*VDD= 5.5V, T= 0°C,Fast Process
**VDD= 4.5V, T= 100°C, Slow Process

POWER SUPPLY AND EXTERNAL COMPONENT INFORMATION

VDD = 5 volts ± 10%
VSS = 0 volts

The output pads are connected to 3 volts through external 50 ohm resistors. This allows the chip to communicate with true TTL/CMOS levels, but only with "pseudo" ECL levels. See Introduction for more details.

OR

VDD = 0
VSS = -5 volts ± 10%

The output pads are connected to -2 volts through external 50 ohm resistors. This allows the chip to communicate with true ECL levels but only with "pseudo" TTL or CMOS levels. See Introduction for more details.

Note: The Reference Voltage Generator CS4T must be used with this cell.

BiCMOS Output Buffer

BOEBT05T

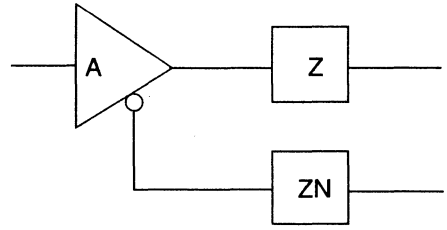
Balanced, 10 volt

CELL SIZE: X = 483.5 μ
Y = 591 μ

NETLIST ORDER

INPUTS: A;
OUTPUTS: Z,ZN;

SCHEMA SYMBOL



TRUTH TABLE

A	Z	ZN
0	0	1
1	1	0

CAPACITANCES

NODE	CAPACITANCE
A	0.588 pF
Z,ZN	6.8 pF

CIRCUIT INFORMATION

PARAMETER	VALUE
WC DC Power*	70 mW
WC Slow Intrinsic Delay**	5.36 ns
WC Fast Intrinsic Delay*	2.2 ns
WC Slow Extrinsic Delay**	0.02 ns/pF
WC Fast Extrinsic Delay*	0.012 ns/pF

*VDD= 5.5V, VEE= -5.5V, T= 0°C,Fast Process
**VDD= 4.5V, VEE= -4.5V, T= 100°C, Slow Process

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POWER SUPPLY AND EXTERNAL COMPONENT INFORMATION

VDD = 5 volts ± 10%
VSS = 0 volts
VEE = -5 volts ± 10%

The output pads are connected to -2 volts through external 50 ohm resistors.

BiCMOS Output Buffer

BOEF05T

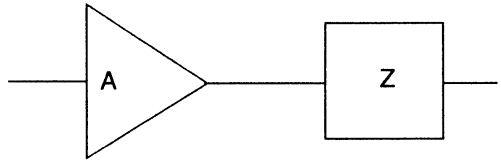
Non-inverting, 5 volt

CELL SIZE: X = 200 μ
Y = 571.875 μ

NETLIST ORDER

INPUTS: A;
OUTPUTS: Z;

SCHEMA SYMBOL



TRUTH TABLE

A	Z
0	0
1	1

CAPACITANCES

NODE	CAPACITANCE
A	0.34 pF
Z	6.8 pF

CIRCUIT INFORMATION

PARAMETER	VALUE
WC DC Power*	22 mW
WC Slow Intrinsic Delay**	2.55 ns
WC Fast Intrinsic Delay*	0.87 ns
WC Slow Extrinsic Delay**	0.019 ns/pF
WC Fast Extrinsic Delay*	0.014 ns/pF

*VDD= 5.5V, T= 0°C,Fast Process
**VDD= 4.5V, T= 100°C, Slow Process

POWER SUPPLY AND EXTERNAL COMPONENT INFORMATION

VDD = 5 volts ± 10%
VSS = 0 volts

The output pad is connected to 3 volts through an external 50 ohm resistor. This allows the chip to communicate with true TTL/CMOS levels, but only with "pseudo" ECL levels. See Introduction for more details.

OR

VDD = 0
VSS = -5 volts ± 10%

The output pad is connected to -2 volts through an external 50 ohm resistor. This allows the chip to communicate with true ECL levels but only with "pseudo" TTL or CMOS levels. See Introduction for more details.

Note: The Reference Voltage Generator CS4T must be used with this cell.

BiCMOS Output Buffer

BOET05T

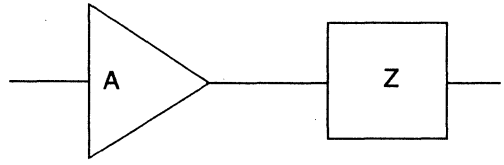
Non-inverting, 10 volt

CELL SIZE: **X = 253.75 μ**
Y = 591 μ

NETLIST ORDER

INPUTS: A;
OUTPUTS: Z;

SCHEMA SYMBOL



TRUTH TABLE

A	Z
0	0
1	1

CAPACITANCES

NODE	CAPACITANCE
A	0.12 pF
Z	6.8 pF

CIRCUIT INFORMATION

PARAMETER	VALUE
WC DC Power*	35 mW
WC Slow Intrinsic Delay**	4.63 ns
WC Fast Intrinsic Delay*	1.84 ns
WC Slow Extrinsic Delay**	0.02 ns/pF
WC Fast Extrinsic Delay*	0.012 ns/pF

*VDD= 5.5V, VEE= -5.5V, T= 0°C,Fast Process
**VDD= 4.5V, VEE= -4.5V, T= 100°C, Slow Process

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POWER SUPPLY AND EXTERNAL COMPONENT INFORMATION

VDD = 5 volts ± 10%
VSS = 0 volts
VEE = -5 volts ± 10%

The output pad is connected to -2 volts through an external 50 ohm resistor.

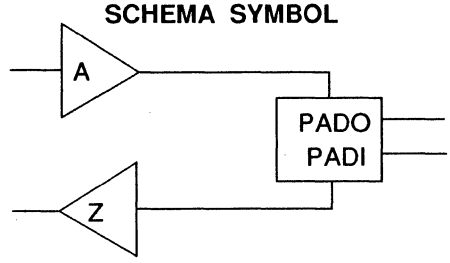
BiCMOS Bidirectional Buffer

BE16F05V

Non-inverting input stage,
Non-inverting output stage, 5 volt

CELL SIZE: X = 202 μ
Y = 885 μ

SCHEMA SYMBOL



NETLIST ORDER
INPUTS: A, PADI;
OUTPUTS: Z, PADO;

TRUTH TABLE

A	PADO	PADI	Z
0	0	0	0
0	1	1	1
1	1	X	1

CAPACITANCES

NODE	CAPACITANCE
PAD	7.0 pF
A	0.60 pF

CIRCUIT INFORMATION

INPUT STAGE	VALUE
WC DC Power*	8 mW
WC Slow Intrinsic Delay**	8.75 ns
WC Fast Intrinsic Delay*	3.56 ns
WC Slow Extrinsic Delay**	0.85 ns/pF
WC Fast Extrinsic Delay*	0.33 ns/pF
OUTPUT STAGE	**VALUE**
WC DC Power*	22 mW
WC Slow Intrinsic Delay**	2.55 ns
WC Fast Intrinsic Delay*	0.87 ns
WC Slow Extrinsic Delay**	0.019 ns/pF
WC Fast Extrinsic Delay*	0.014 ns/pF

*VDD= 5.5V, T= 0°C,Fast Process
**VDD= 4.5V, T= 100°C, Slow Process

POWER SUPPLY AND EXTERNAL COMPONENT INFORMATION

VDD = 5 volts ± 10%
VSS = 0 volts

The output pad is connected to 3 volts through an external 50 ohm resistor. This allows the chip to communicate with true TTL/CMOS levels, but only with "pseudo" ECL levels. See Introduction for more details.

OR

VDD = 0
VSS = -5 volts ± 10%

The output pad is connected to -2 volts through an external 50 ohm resistor. This allows the chip to communicate with true ECL levels but only with "pseudo" TTL or CMOS levels. See Introduction for more details.

Note: The Reference Voltage Generator CS4T must be used with this cell.

FDS Synthesized Macrocells

Section 11

AT&T

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Functional Design System — Introduction

FDS is a logic synthesis system that automatically generates the netlist implementation in standard cells of several parameterizable functional primitives. For each primitive, a wide range of user definable features are available.
The following primitives are supported in FDS:

- adders
- combinational blocks
- comparators
- counters
- decoders
- finite state machines
- multiplexers
- parity generators
- registers

FDS also features a friendly interface for capturing the design parameters and the external view of desired primitives. In addition, schematics corresponding to the netlist of the primitive may be generated. It consists of standard cells from either the performance or area optimized library. All of the FDS functional primitives' features are user selectable, creating a large variety of possible configurations. For more information on how to generate these cells, consult the FDS manual.

Specifically, the following functions are available:

Capture Symbol	Prompts the user to define the external view and specify applicable options of a functional primitive and creates it
Simulation Model	Produces a simulation model for MOTIS3
Synthesize	Implements the captured functional primitive
Draw Schematic	Displays the internal schematic of the synthesized standard cell functional primitive

A functional primitive in FDS may be added to a schematic diagram in SCHEMA, which may then be used to generate a connectivity list incorporating the primitive as part of an integrated circuit design. The connectivity list is available in two formats: the LSL format, which may be used for simulation in MOTIS3, and the ADVICE format, used as input to ADVICE program. Hard copies of the final schematics can be produced on an off-line plotter.

FUNCTIONAL DESCRIPTION AND FEATURES:

The FDS adder is a netlist that can be parameterized with many options.

The ADDER has the following features:

- Bus or Non Bus pin notation
- Optional Carry-Input
- Optional Carry-Output
- Inverted/noninverted inputs and outputs
- Optional Ripple carry
- Optional Carry-look-ahead
- Optional Mixture of Ripple-Carry and Carry-Look-Ahead
- Fully combinatorial

ADDER can be customized with the parameter N as shown in the following table:

Parameter	Description	Limit		
		Increment	Min	Max
N	Bits	1	2	128

TERMINAL DESCRIPTIONS:

Netlist Order :

option dependent, consult the FDS manual

Functional Descriptions

INPUTS:

A[N-1:0]	First Input to add
B[N-1:0]	Second Input to add
CI	Optional Carry-In

OUTPUTS:

S[N-1:0]	Sum of A[N-1:0] and B[N-1:0]
CO	Optional Carry-Out

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CHARACTERIZATION:

Due to the large number of possible configurations, no attempt was made to characterize the ADDER cell. It is advisable to run CRITIC after generating any FDS block to verify that the performance matches your requirements.

FUNCTIONAL DESCRIPTION AND FEATURES:

The FDS **combinational block** allows the user to specify multiple output combinational circuits. The output functions are defined with either truth table or boolean equation format.

The CMB has the following features:

- Various logic minimization techniques
- Use of complements as candidates for synthesis
- Optional user-specified input and output names
- Optional user-specified maximum fan-in for gates (a value less than 9 fan-ins, the default)

CMB can be customized with the parameters M, N as shown in the following table:

Parameter	Description	Limit		
		Increment	Min	Max
M	Input Pins	1	1	128-N
N	Output Pins	1	1	128-M

TERMINAL DESCRIPTIONS:

Netlist Order :

option dependent, consult the FDS manual

Functional Descriptions

INPUTS:

IN_NAME_1, IN_NAME_2,..... IN_NAME_M
User defined, no default name

OUTPUTS:

OUT_NAME_1, OUT_NAME_2,..... OUT_NAME_N
User defined, no default name

CHARACTERIZATION:

Due to the large number of possible configurations, no attempt was made to characterize the CMB cell. It is advisable to run CRITIC after generating any FDS block to verify that the performance matches your requirements.

FUNCTIONAL DESCRIPTION AND FEATURES:

The FDS **comparator** compares two binary or decimal numbers for logical conditions selected by the user. Logical conditions include magnitude (greater-than, less-than), equality (inequality), and combinations of magnitude and equality.

The COMP has the following features:

- Optional decimal or binary comparator structure
- BCD, EXCESS-3, or EXCESS-3-GRAY codes are available for the decimal decoder
- Bus or Non Bus pin notation
- One or more comparison criteria can be chosen
- Optional low-active or high-active output signals
- Optional inverted inputs

COMP can be customized with the parameter N as shown in the following table:

Parameter	Description	Limit		
		Increment	Min	Max
N	Binary Bits	1	2	256
N	Decimal Bits	4	4	256

TERMINAL DESCRIPTIONS:

Netlist Order :

option dependent, consult the FDS manual

Functional Descriptions

INPUTS:

A[N-1:0]	Operand A
B[N-1:0]	Operand B

OUTPUTS:

LT	A < B
EQ	A = B
GT	A > B
LE	A <= B
GE	A >= B
NE	A != B

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CHARACTERIZATION:

Due to the large number of possible configurations, no attempt was made to characterize the COMP cell. It is advisable to run CRITIC after generating any FDS block to verify that the performance matches your requirements.

FUNCTIONAL DESCRIPTION AND FEATURES:

The FDS **counter** is a binary up or down counter. The size of counter may vary from 2 to 128 bits. Counters with more than 16 bits use ripple carry.

The COUNTER has the following features:

- Optional parallel load
- Bus or Non Bus pin notation
- Optional bits tapped as Q (QN) outputs
- Optional up, down, or updown counting scheme
- Optional decode binary counter
- Optional fast or ripple carry scheme
- Optional PRESET, PRECLEAR, or INITIALIZATION control signal
- Optional asynchronous or synchronous control timing
- Optional inhibit signal
- Optional dynamic or static clocking scheme
- Optional rising or falling edge triggered static clock

COUNTER can be customized with the parameter N as shown in the following table:

Optional Condition	Parameter	Description	Limit		
			Increment	Min	Max
Ripple Carry	N	Bits	1	2	128
Fast Carry	N	Bits	1	2	16
Initial Signal	N	Bits	1	2	30
Decade Counter	N	Bits	_	4	4

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TERMINAL DESCRIPTIONS:

Netlist Order :

option dependent, consult the FDS manual

Functional Descriptions

INPUTS:

PI[N-1:0]	Parallel loaded input signals
CTLD	Count/Load control
CUCD	Counter up/down control
CI	Carry-In
INH	Control input clock inhibit signal
PS	Preset assigns each bit in the counter to 1
PC	Preclear assigns each bit in the counter to 0
INIT	Initialization sets the counter to a bit pattern specified by the user
CK	Static clocking is triggered by the rising-edge or the falling edge of the clock
MCK,SCK,MCKN,SCKN	Four clocks for dynamic clocking

OUTPUTS:

Q[N-1:0]	Output signals of the counter
QN[N-1:0]	Complementary output signals of the counter
CO	Carry-Out

CHARACTERIZATION:

Due to the large number of possible configurations, no attempt was made to characterize the COUNTER cell. It is advisable to run CRITIC after generating any FDS block to verify that the performance matches your requirements.

FUNCTIONAL DESCRIPTION AND FEATURES:

The FDS **decoder** is a select-line to output-line decoder. Select lines (inputs) jointly represent a binary or decimal encoded number.

The DECODER has the following features:

- Optional decimal and binary decoder structure
- BCD, EXCESS-3 or EXCESS-3-GRAY codes are available for decimal decoders
- Bus or Non Bus pin notation
- User-specified number of select and output lines, using guidelines given below
- Optional inverted select lines
- Optional low-active or high-active output signal
- Optional enable signal

DECODER can be customized with the parameters M, N as shown in the following table:

Decoder	Parameter	Description	Limit		
			Increment	Min	Max
Binary	M	Select Lines	1	1	10
	N	Output Lines	1	$2^{M-1}+1$	2^{M}

Decoder	Output Lines	Select Lines	Limit		
			Increment	Min	Max
Decimal*	N	M=4	1	2	10
	N	M=8	1	11	100

*For decimal decoder, the select lines must equal 4 or 8; the number of output lines for each configuration is specified above.

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TERMINAL DESCRIPTIONS:

Netlist Order :

option dependent, consult the FDS manual

Functional Descriptions

INPUTS:

S[M-1:0]	Select lines
EN	Enable signal

OUTPUTS:

Y[N-1:0]	It sets the output line that has the same numeric value as the encoded number to its active voltage level

CHARACTERIZATION:

Due to the large number of possible configurations, no attempt was made to characterize the DECODER cell. It is advisable to run CRITIC after generating any FDS block to verify that the performance matches your requirements.

FDS Finite State Machine FSM

FUNCTIONAL DESCRIPTION AND FEATURES:

The FDS **finite state machine** synthesizer models circuit behavior in terms of a number of states, state transitions, and output functions. The FSM Synthesizer produces implementation in polycells, and input files for MOTIS3 functional simulation.

The FSM has the following features:

- Support vector format for inputs and outputs
- User-specified inputs and outputs
- Specification of state transitions and output functions via state transition diagram
- User-specified INITIALIZATION signal
- Optional asynchronous or synchronous control scheme
- Optional dynamic or static clocking scheme
- Optional rising-edge or falling-edge of static clock
- Create a simulation model for input to MOTIS3
- State based simulation

FSM has the following constrain:

Inputs + Outputs + Present State Signals + Next State Signals ≤ 128

TERMINAL DESCRIPTIONS:

Netlist Order :

option dependent, consult the FDS manual

Functional Descriptions

INPUTS:

User-defined

CK	Static clocking is triggered by the rising-edge or the falling edge of the clock
MCK,SCK,MCKN,SCKN	Four clocks for dynamic clocking
INIT	Initial signal

OUTPUTS:

User-defined

CHARACTERIZATION:

Due to the large number of possible configurations, no attempt was made to characterize the FSM. It is advisable to run CRITIC after generating any FDS block to verify that the performance matches your requirements.

FDS Multiplexer

FUNCTIONAL DESCRIPTION AND FEATURES:

The FDS **multiplexer** is a multi-word-to-one-word or multi-line-to-one-line multiplexer.

The MUX has the following features:

- Bus or Non Bus pin notation
- Optional encoded select lines
- User-specified number of words and number of bits per word
- Optional inverted select lines
- Optional enable signal
- Optional forced outputs to high, low or tri-state, when enable signal is inactive
- Optional complementary outputs
- Optional use of large cells (e.g. AOI3333)

MUX(N,M) can be customized with the parameters K, M, N as shown in the following table:

Parameter	Description	Limit		
		Increment	Min	Max
N	Words	1	2	M*N ≤ 512
M	Bits/word	1	2	16

Parameter	Description	Value
K	Select lines (nonencoded)	N
K	Select lines (encoded)	$\log_2 N$

TERMINAL DESCRIPTIONS:

Netlist Order :

option dependent, consult the FDS manual

Functional Descriptions

INPUTS:

D[N-1:0, M-1:0]	The root name for the input signals
S[K-1:0]	Select lines
EN	Optional enable line

OUTPUTS:

Y[N-1:0]	Normal output
YN[N-1:0]	Complementary output

CHARACTERIZATION:

Due to the large number of possible configurations, no attempt was made to characterize the MUX cell. It is advisable to run CRITIC after generating any FDS block to verify that the performance matches your requirements.

FUNCTIONAL DESCRIPTION AND FEATURES:

The FDS **parity generator** can generate odd, even, or odd and even parity via the implementation of a tree of XOR cells.

PAR has the following features:

- Bus or Non Bus pin notation
- User specified number of bits
- Optional inverted inputs
- Optional parity generated of ODD, EVEN, or BOTH
- Optional low-active or high-active output signals

PAR can be customized with the parameter N as shown in the following table:

Parameter	Description	Limit		
		Increment	Min	Max
N	Bits	1	2	512

TERMINAL DESCRIPTIONS:

Netlist Order :

option dependent, consult the FDS manual

Functional Descriptions

INPUTS:

D[N-1:0]	N bits inputs

OUTPUTS:

ODD	When ODD or BOTH parity is selected
EVEN	When EVEN or BOTH parity is selected

CHARACTERIZATION:

Due to the large number of possible configurations, no attempt was made to characterize the PAR cell. It is advisable to run CRITIC after generating any FDS block to verify that the performance matches your requirements.

FUNCTIONAL DESCRIPTION AND FEATURES:

The FDS universal register can be an ordinary latch (parallel-in parallel-out) or a shift (serial-in parallel-out) register. It also accommodates combined parallel and serial input to parallel output.

The UNREG has the following features:

- Shift can be right-to-left, left-to-right, or bidirectional
- Optional parallel, serial or both of data input mode
- Bus or Non Bus pin notation
- Optional bits tapped as Q (QN) outputs, also allows the user to enter the specified bit-pattern for tapping Q (QN) output signals
- PRESET, PRECLEAR, and INITIALIZATION are available with asynchronous or synchronous control
- Optional inhibit signal INH
- Optional dynamic or static clocking scheme
- Optional rising or falling edge of static clock

UNREG can be customized with the parameter N as shown in the following table:

Condition	Parameter	Description	Limit		
			Increment	Min	Max
Normal	N	Bits	1	2	128
With Initial Signal	N	Bits	1	2	30

TERMINAL DESCRIPTIONS:

Netlist Order :

option dependent, consult the FDS manual

Functional Descriptions

INPUTS:

PI[N-1:0]	The root name of input signal
LE	Left entry (right shift)
RE	Right entry (left shift)
RL	Bidirectional shift
SHLD	Shift/Load
INH	Inhibit signal
PS	Preset
PC	Preclear
INIT	Initialization signal
CK	Static clocking is triggered by the rising-edge or the falling-edge of the clock
MCK,SCK,MCKN,SCKN	Four clocks for dynamic clocking

OUTPUTS:

Q[N-1:0]	Normal outputs
QN[N-1:0]	Complementary outputs

CHARACTERIZATION:

Due to the large number of possible configurations, no attempt was made to characterize the UNREG1 cell. It is advisable to run CRITIC after generating any FDS block to verify that the performance matches your requirements.

MSI/LSI Functions

Section 12

AT&T

Contents - Section 12

Introduction

This section describes a variety of digital functions that are available in the 1.25µ CMOS Library. Many of the functions are provided as standard cell netlists, and can either be used 'as-is', or can be modified to suit your particular needs. Using one of these netlists as a starting point could save you some time compared to starting from scratch.

The *CM*-series of cells in this section are very similar to some 74XX-series functions. For example, the CM42 is functionally equivalent to the 7442 4-Line-to-10-Line BCD-to-Decimal Decoder.

The functionality for these cells are described either in detailed schematics (for simple functions) or in the block diagrams (for more complex functions).

Timing characteristics provided in this section are obtained with AT&T's static timing analyzer, CRITIC. They are estimated with an average routing capacitance of 0.12 pF per fanout. The more accurate circuit simulator, GSIM, should be used to verify the proper timing for your final designs.

For more detailed information regarding the use of these functions, please contact your AT&T representative.

2-Bit Arithmetic Logic Unit — ALU2

146 grids, 214 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The ALU2 performs arithmetic and logic operations on two 2-bit words. These operations are selected by four function select lines (S0, S1, S2, S3). The operation mode is controlled by the LAN input. It is implemented with standard cells.

- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Plus other arithmetic operations
- Logic function modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus other logic operations

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A0, A1, B0, B1, S0, S1, S2, S3, CN0, LAN;

OUTPUTS: F0, F1, XN, YN, CNP2, AEB;

Functional Descriptions

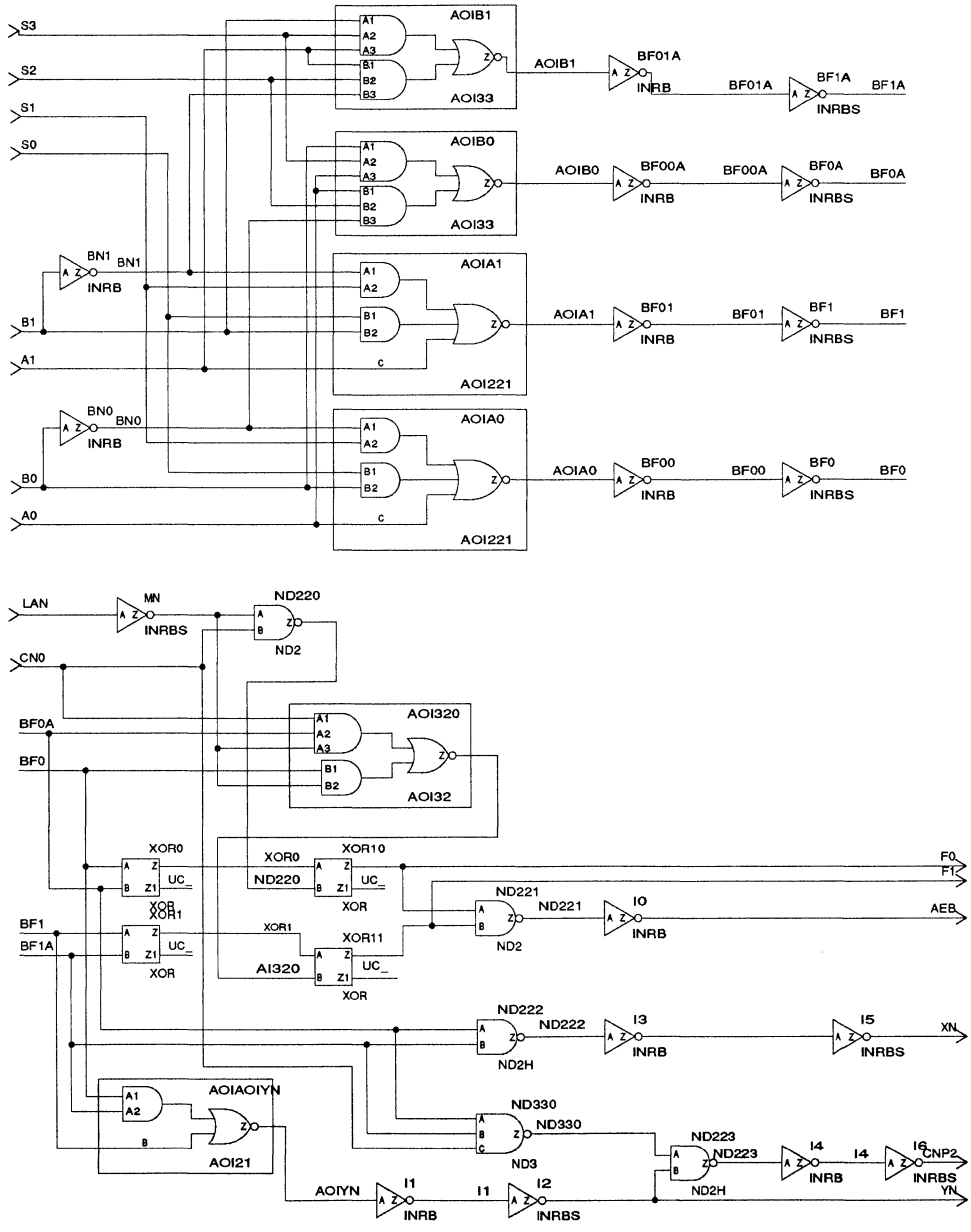
Inputs:

A[0:1]	Word A inputs
B[0:1]	Word B inputs
S[0:3]	Function select inputs
CN0	Inverted Carry input
LAN	Mode control input

Outputs:

F[0:1]	Function outputs
XN	Carry PROPAGATE output
YN	Carry GENERATE output
CNP2	Inverted Carry output
AEB	Comparator output

DETAILED SCHEMATIC



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CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
A[0:1],B[0:1],S[0:3]	AEB↑	12.05	3.70	5.19	0.68
A[0:1],B[0:1],S[0:3]	AEB↓	11.10	2.54	4.71	0.55
A[0:1],B[0:1],S[0:3]	CNP2↑	10.62	0.98	4.71	0.18
A[0:1],B[0:1],S[0:3]	CNP2↓	11.52	0.94	5.00	0.18
A[0:1],B[0:1],S[0:3]	F[0:1]↑	10.14	9.45	4.43	1.82
A[0:1],B[0:1],S[0:3]	F[0:1]↓	9.81	12.53	4.24	2.61
A[0:1],B[0:1],S[0:3]	XN↑	7.57	0.98	3.29	0.18
A[0:1],B[0:1],S[0:3]	XN↓	7.33	0.94	3.33	0.18
A[0:1],B[0:1],S[0:3]	YN↑	9.52	0.98	4.05	0.18
A[0:1],B[0:1],S[0:3]	YN↓	9.10	0.94	4.00	0.18
CN0	AEB↑	5.76	3.70	2.43	0.68
CN0	AEB↓	4.86	2.54	2.05	0.55
CN0	CNP2↑	3.10	0.98	1.57	0.18
CN0	CNP2↓	3.19	0.94	1.48	0.18
CN0	F[0:1]↑	3.86	9.45	1.67	1.82
CN0	F[0:1]↓	3.57	12.53	1.57	2.61
LAN	AEB↑	6.00	3.70	2.52	0.68
LAN	AEB↓	5.10	2.54	2.10	0.55
LAN	F[0:1]↑	4.10	9.45	1.76	1.82
LAN	F[0:1]↓	3.81	12.58	1.62	2.61

FUNCTIONAL MODES

SELECTION				ACTIVE HIGH DATA		
				LAN=H	LAN=L ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	CN0=H (no carry)	CN0=L (with carry)
L	L	L	L	$F=\overline{A}$	F=A	F=A plus 1
L	L	L	H	$F=\overline{A+B}$	F=A+B	F=(A+B) plus 1
L	L	H	L	$F=\overline{A}B$	$F=A+\overline{B}$	$F=(A+\overline{B})$ plus 1
L	L	H	H	F=0	F=minus 1(2's Compl)	F=zero
L	H	L	L	$F=\overline{AB}$	$F=A$ plus $A\overline{B}$	F=A plus $A\overline{B}$ plus 1
L	H	L	H	$F=\overline{B}$	F=(A+B) plus $A\overline{B}$	F=(A+B) plus $A\overline{B}$ plus 1
L	H	H	L	F=A⊕B	F=A minus B minus 1	F=A minus B
L	H	H	H	$F=A\overline{B}$	F=$A\overline{B}$ minus 1	F=$A\overline{B}$
H	L	L	L	$F=\overline{A}+B$	F=A plus AB	F=A plus AB plus 1
H	L	L	H	$F=\overline{A\oplus B}$	F=A plus B	F=A plus B plus 1
H	L	H	L	F=B	$F=(A+\overline{B})$ plus AB	$F=(A+\overline{B})$ plus AB plus 1
H	L	H	H	F=AB	F=AB minus 1	F=AB
H	H	L	L	F=1	F=A plus A*	F=A plus A plus 1
H	H	L	H	$F=A+\overline{B}$	F=(A+B) plus A	F=(A+B) plus A plus 1
H	H	H	L	F=A+B	$F+(A+\overline{B})$ plus A	$F=(A+\overline{B})$ plus A plus 1
H	H	H	H	F=A	F=A minus 1	F=A

Note: * means LEFT SHIFT operation on A

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4-Bit Arithmetic Logic Unit — ALU4

316 grids, 462 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The ALU4 is functionally equivalent to the 74181 Arithmetic Logic Unit/Functional Generator within the standard 74XX Series logic families of devices. The ALU4 performs arithmetic and logic operations on two 4-bit words. These operations are selected by four function select lines (S0, S1, S2, S3). The operation mode is controlled by the LAN input. It is implemented with standard cells.

- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Plus other arithmetic operations
- Logic function modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus other logic operations

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A0, A1, A2, A3, B0, B1, B2, B3, S0, S1, S2, S3, CN0, LAN;

OUTPUTS: F0, F1, F2, F3, XN, YN, CNP4, AEB;

Functional Descriptions

Inputs:

A[0:3]	Word A inputs
B[0:3]	Word B inputs
S[0:3]	Function select inputs
CN0	Inverted Carry input
LAN	Mode control input

Outputs:

F[0:3]	Function outputs
XN	Carry PROPAGATE output
YN	Carry GENERATE output
CNP4	Inverted Carry output
AEB	Comparator output

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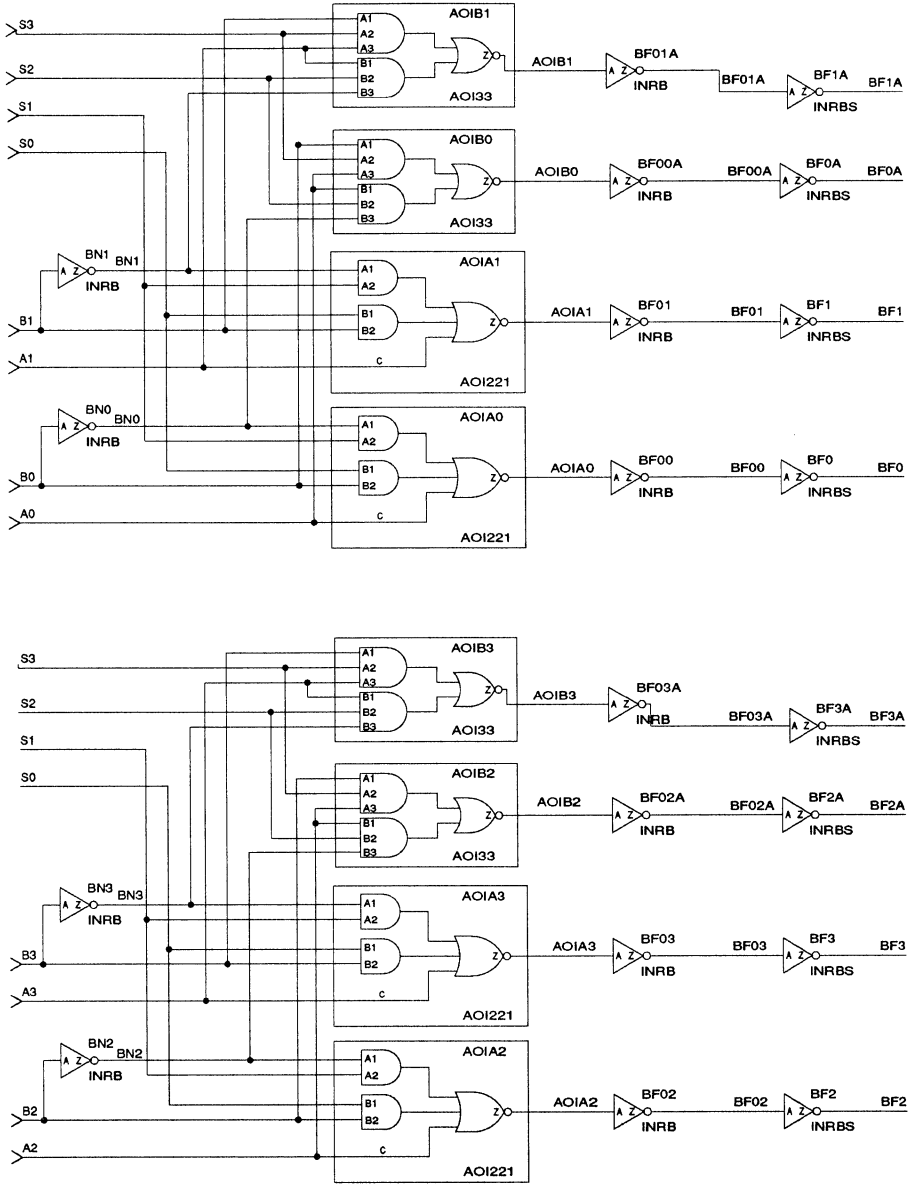
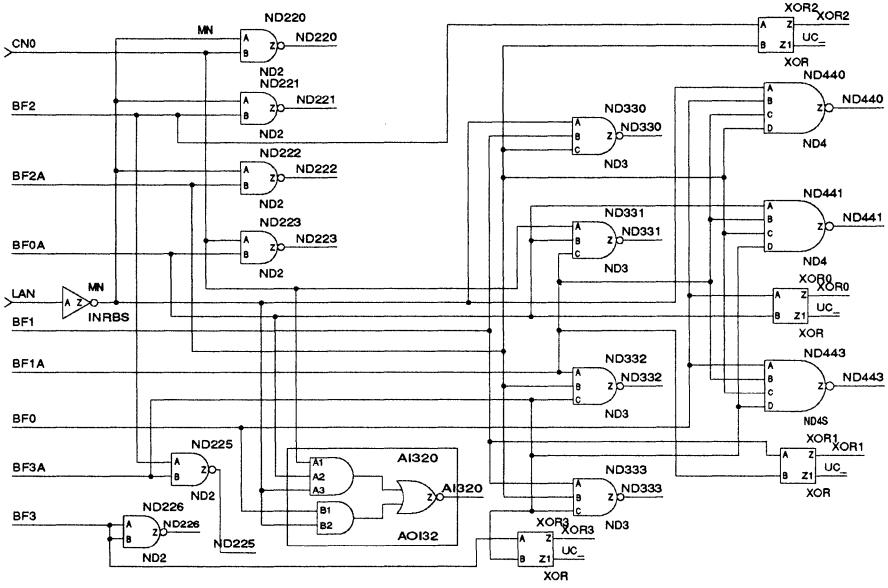
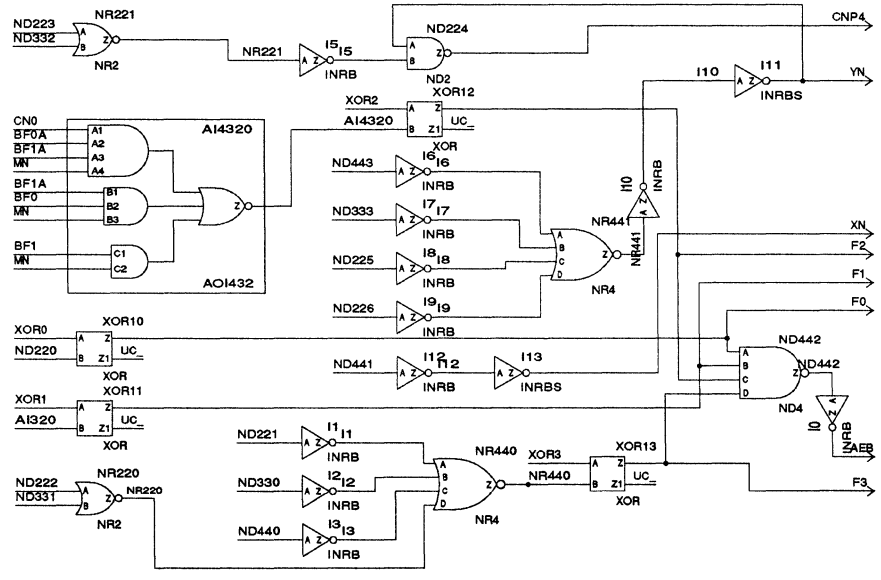
DETAILED SCHEMATIC



12

DETAILED SCHEMATIC (continued)





CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
A[0:3],B[0:3],S[0:3]	AEB↑	17.05	9.45	7.19	1.82
A[0:3],B[0:3],S[0:3]	AEB↓	15.67	12.53	6.52	2.61
A[0:3],B[0:3],S[0:3]	CNP4↑	11.57	3.79	4.95	0.70
A[0:3],B[0:3],S[0:3]	CNP4↓	14.29	4.19	5.86	0.89
A[0:3],B[0:3],S[0:3]	F[0:3]↑	14.29	9.45	6.05	1.82
A[0:3],B[0:3],S[0:3]	F[0:3]↓	14.33	12.53	5.95	2.61
A[0:3],B[0:3],S[0:3]	XN↑	8.90	0.98	3.90	0.18
A[0:3],B[0:3],S[0:3]	XN↓	9.81	0.94	4.38	0.18
A[0:3],B[0:3],S[0:3]	YN↑	14.05	0.98	5.76	0.18
A[0:3],B[0:3],S[0:3]	YN↓	11.48	0.94	4.90	0.18
CN0	AEB↑	10.24	9.45	4.29	1.82
CN0	AEB↓	8.86	12.53	3.62	2.61
CN0	CNP4↑	3.71	3.79	1.38	0.70
CN0	CNP4↓	2.95	4.19	1.10	0.89
CN0	F[0:3]↑	7.48	9.45	3.14	1.82
CN0	F[0:3]↓	7.52	12.53	3.05	2.61
LAN	AEB↑	11.33	9.45	4.71	1.82
LAN	AEB↓	9.95	12.53	4.05	2.61
LAN	F[0:3]↑	8.57	9.45	3.57	1.82
LAN	F[0:3]↓	8.62	12.53	3.48	2.61

FUNCTIONAL MODES

SELECTION				ACTIVE HIGH DATA		
				LAN=H	LAN=L ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	CN0=H (no carry)	CN0=L (with carry)
L	L	L	L	F=$\overline{A}$	F=A	F=A plus 1
L	L	L	H	F=$\overline{A+B}$	F=A+B	F=(A+B) plus 1
L	L	H	L	F=$\overline{A}$B	F=A+$\overline{B}$	F=(A+$\overline{B}$) plus 1
L	L	H	H	F=0	F=minus 1(2's Compl)	F=zero
L	H	L	L	F=$\overline{AB}$	F=A plus A$\overline{B}$	F=A plus A$\overline{B}$ plus 1
L	H	L	H	F=$\overline{B}$	F=(A+B) plus A$\overline{B}$	F=(A+B) plus A$\overline{B}$ plus 1
L	H	H	L	F=A⊕B	F=A minus B minus 1	F=A minus B
L	H	H	H	F=A$\overline{B}$	F=A$\overline{B}$ minus 1	F=A$\overline{B}$
H	L	L	L	F=$\overline{A}$+B	F=A plus AB	F=A plus AB plus 1
H	L	L	H	F=$\overline{A⊕B}$	F=A plus B	F=A plus B plus 1
H	L	H	L	F=B	F=(A+$\overline{B}$) plus AB	F=(A+$\overline{B}$) plus AB plus 1
H	L	H	H	F=AB	F=AB minus 1	F=AB
H	H	L	L	F=1	F=A plus A*	F=A plus A plus 1
H	H	L	H	F=A+$\overline{B}$	F=(A+B) plus A	F=(A+B) plus A plus 1
H	H	H	L	F=A+B	F+(A+$\overline{B}$) plus A	F=(A+$\overline{B}$) plus A plus 1
H	H	H	H	F=A	F=A minus 1	F=A

Note: * means LEFT SHIFT operation on A

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UART

ARTI

7736 grids, 11268 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The ARTI is an asynchronous receiver/transmitter interface. The device is used as a single-channel, half-duplex or full-duplex interface with data communication equipment (DCE) and data terminal equipment (DTE). The ARTI is compatible with the bus protocol and timing specifications of the Intel 8051 Microcontroller and the Intel 8088 Microprocessor, and may be used in a polled or interrupt-driven system.

To reduce the interrupt overhead and potential for overruns, the transmitter has four data buffers and the receiver has six.

This netlist is a circuit that can also be obtained as a stand-alone IC. Two package styles are available; a 24-pin plastic DIP and a 28-pin SOJ. Contact your AT&T Representative for more information.

- Programmable data format:
  - Seven data bits plus parity
  - Odd, even, no parity
  - One or two stop bits
- Six receive and four transmit data buffers
- Receive break detection and transmit break generation.
- Intel 8088 and 8051 Microprocessor interface without wait states.
- Clear-to-send/request-to-send selectable signals for DTE or DCE modes and EIA flow control.
- Programmable interrupt system:
  - Fill level interrupt of receive FIFOs (first-in, first-out).
  - Receive break detection and error interrupt.
  - Empty level of transmit FIFO.
- Transmit/receive FIFO status bits indicate FIFO levels.
- Flexible polling capabilities.
- On chip programmable baud rate generator.
- Speed matching (autobaud) capability.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: ADI0, ADI1, ADI2, ADI3, ADI4, ADI5, ADI6, ADI7, RDN, WRN, ALE, CSN, HWRESET, CLK1, SERDATIN, RTS, DTR;

OUTPUTS: DFC0, DFC1, DFC2, DFC3, DFC4, DFC5, DFC6, DFC7, SERDAT, CTS, DSR, RXI, TXI;

Functional Descriptions

Inputs:

RDN	Read enable (Microprocessor Interface)
WRN	Write enable (Microprocessor Interface)
ALE	Address latch enable (Microprocessor Interface)
CSN	Chip select (Microprocessor Interface)
HWRESET	Power up reset
CLK1	Clock
SERDATIN	Serial receive data
RTS	Request to send
DTR	Data terminal ready

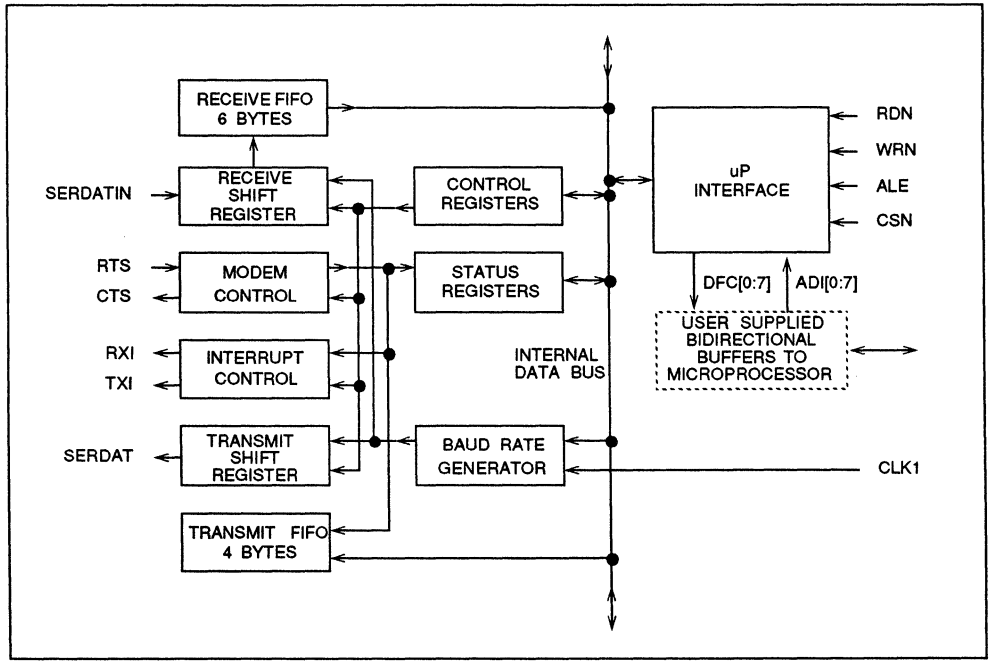
Outputs:

SERDAT	Serial transmit data
CTS	Clear to send
DSR	Data set ready
RXI	Receive interrupt
TXI	Transmit interrupt
REGREAD(N)	Tristate control signals for user supplied bidirectional buffers

Bidirectionals:

ADI[0:7],DFC[0:7]	Address and data bus (Microprocessor Interface)

BLOCK DIAGRAM



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CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
ALE	DFC[0:7]↑	25.76	3.79	11.33	0.70
ALE	DFC[0:7]↓	15.57	4.19	7.76	0.89
CLK1	DFC[0:7]↑	45.38	3.79	19.05	0.70
CLK1	DFC[0:7]↓	38.29	4.19	16.86	0.89
CSN	DFC[0:7]↑	42.00	3.79	18.52	0.70
CSN	DFC[0:7]↓	41.24	4.19	17.81	0.89
RDN	DFC[0:7]↑	28.52	3.79	11.14	0.70
RDN	DFC[0:7]↓	18.67	4.19	7.48	0.89

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum ADI[0:7] Setup before ALE	0.67	0.67
Minimum ADI[0:7] Setup before CSN	0.67	0.67
Minimum CLK1 Setup before CSN	8.95	3.71

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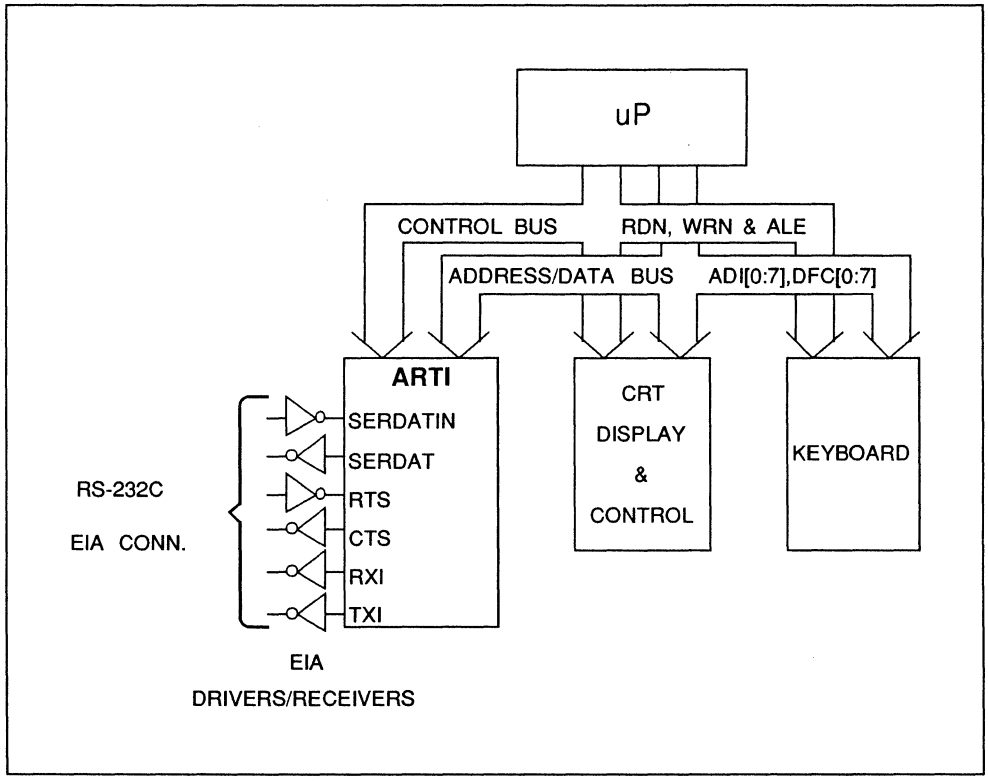
APPLICATION NOTES



2593 grids, 3230 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The BL29C01 is the functional equivalent of AMD's 2901 four-bit microprocessor slice. AMD describes the 2901 as follows: "The 2901 is a high speed, cascadable ALU intended for use in CPUs, peripheral controllers, and programmable microprocessors. The microinstruction flexibility of the 2901 permits efficient emulation of almost any digital computing machine."

The device, as shown in the block diagram, consists of a 16-word by 4-bit-per-word dual port RAM, an eight function ALU, and associated shifting, decoding and multiplexing circuitry. The nine bit microinstruction word is organized into three groups of three bits each that select the ALU source operands, the ALU function, and the ALU destination register. The 2901 is cascadable with full look ahead or with ripple carry, has tristate outputs, and provides various status flag outputs from the ALU.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: I8, I7, I6, I5, I4, I3, I2, I1, I0, A3, A2, A1, A0, B3, B2, B1, B0, D3, D2, D1, D0, RAM0I, RAM3I, Q0I, Q3I, CN, CP, OEN;

OUTPUTS: Y3, Y2, Y1, Y0, GN, PN, OVR, FEQ0, F3, CN4, RAM0O, RAM3O, Q0O, Q3O;

Functional Descriptions

Inputs:

I[8:0]	The nine instruction control lines. Used to determine what data sources will be applied to the ALU (I[0:2]), what function the ALU will perform (I[3:5]), and what data is to be deposited in the Q-register or the register stack (I[6:8]).
A[3:0]	The four address inputs to the register stack used to select one register whose contents are displayed through the A port.
B[3:0]	The four address inputs to the register stack used to select one register whose contents are displayed through the B port and into which new data can be written when the clock goes LOW.
D[3:0]	Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the device.
CN	The carry-in to the internal ALU.
CP	The clock input.
OEN	Output enable, active low

Outputs:

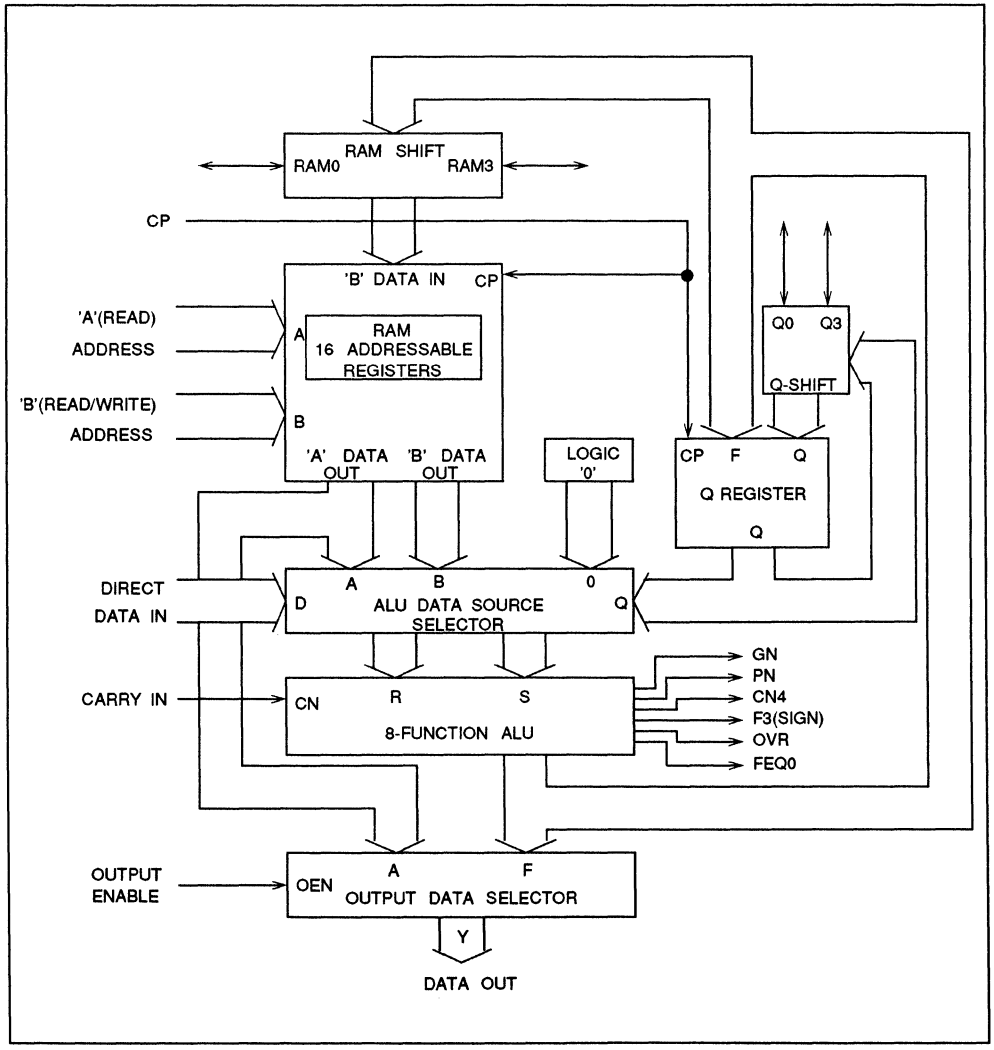
Y[3:0]	The four data outputs. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack.
GN	The carry generate output of the internal ALU.
PN	The carry propagate output of the internal ALU.
OVR	Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU.
FEQ0	Indicates the result of an ALU operation is zero.
F3	The most significant ALU bit.
CN4	The carry-out of the internal ALU.

Functional Descriptions (continued)

Bidirectionals:

RAM0	A shift line at the LSB of the register stack.
RAM3	A shift line at the MSB of the register stack.
Q0	A shift line at the LSB of the Q register.
Q3	A shift line at the MSB of the Q register.

BLOCK DIAGRAM



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CHARACTERISTICS

AREA OPTIMIZED SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing								
	Intrinsic Delay To Output (ns)							
From Input	Y[0:3]	F3	CN4	GN,PN	FEQ0	OVR	RAM[0,3]O	Q[0,3]O
CN	33.62	28.71	10.33	-	30.95	17.48	31.38	-
CP↑	55.14	50.24	33.19	32.90	52.48	39.00	52.90	1.24
D[0:3]	51.24	46.33	29.38	29.10	48.59	35.10	49.00	-
I[0:2]	58.90	54.00	37.05	36.76	56.24	42.76	56.67	-
I[3:5]	60.24	55.33	38.38	38.10	57.57	44.10	58.00	-
I[6:8]	14.14	-	-	-	-	-	14.33	14.33
Extrinsic (ns/pf)	3.70	7.40	7.40	7.40	11.72	7.40	3.70	3.57

PERFORMANCE OPTIMIZED SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing								
	Intrinsic Delay To Output (ns)							
From Input	Y[0:3]	F3	CN4	GN,PN	FEQ0	OVR	RAM[0,3]O	Q[0,3]O
CN	12.67	10.76	3.57	-	11.95	6.48	11.86	-
CP↑	22.33	20.43	13.81	13.76	21.62	16.14	21.52	1.00
D[0:3]	19.43	17.52	10.95	10.90	18.71	13.24	18.62	-
I[0:2]	22.05	20.14	13.57	13.52	21.33	15.86	21.24	-
I[3:5]	22.52	20.62	14.05	14.00	21.89	16.33	21.71	-
I[6:8]	5.00	-	-	-	-	-	4.33	4.33
Extrinsic (ns/pf)	0.68	1.64	1.64	1.64	2.11	1.64	0.68	0.65

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum A[0:3],B[0:3] Setup before CP	29.86	10.62
Minimum CN Setup before CP↑	35.86	13.67
Minimum D[0:3] Setup before CP↑	53.48	20.43
Minimum I[0:2] Setup before CP↑	61.14	23.05
Minimum I[3:5] Setup before CP↑	62.48	23.52
Minimum I[6:8] Setup before CP↓	17.05	5.76
Minimum Q[0,3]I Setup before CP↑	3.71	1.86
Minimum RAM[0,3]I Setup before CP↑	5.67	2.24

12

733 grids, 1016 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The BL29C09 is the functional equivalent of AMD's 2909 microprogram sequencer. The 2909 is a four-bit wide address controller intended for sequencing through a series of microinstructions contained in a ROM. Two or more 2909's can be connected to form eight-bit or larger addresses.

The device can be used to select an address from any of four sources. They are:

- A set of external inputs(D)
- External data from the R inputs, stored in an internal register
- A four word deep push/pop stack
- A program counter register which usually contains the last address plus one.

The push/pop stack includes control lines that enable it to efficiently execute nested subroutine linkages. Each of the four outputs can be OR'ed with an external input for conditional skip or branch instructions, and a separate line forces all of the outputs to zero. The outputs are tristatable.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: CK, R0, R1, R2, R3, REB, D0, D1, D2, D3, S0, S1, OR0, OR1, OR2, OR3, ZEROB, OEB, CN, FEB, PUP;

OUTPUTS: Y0, Y1, Y2, Y3, CN4;

Functional Descriptions

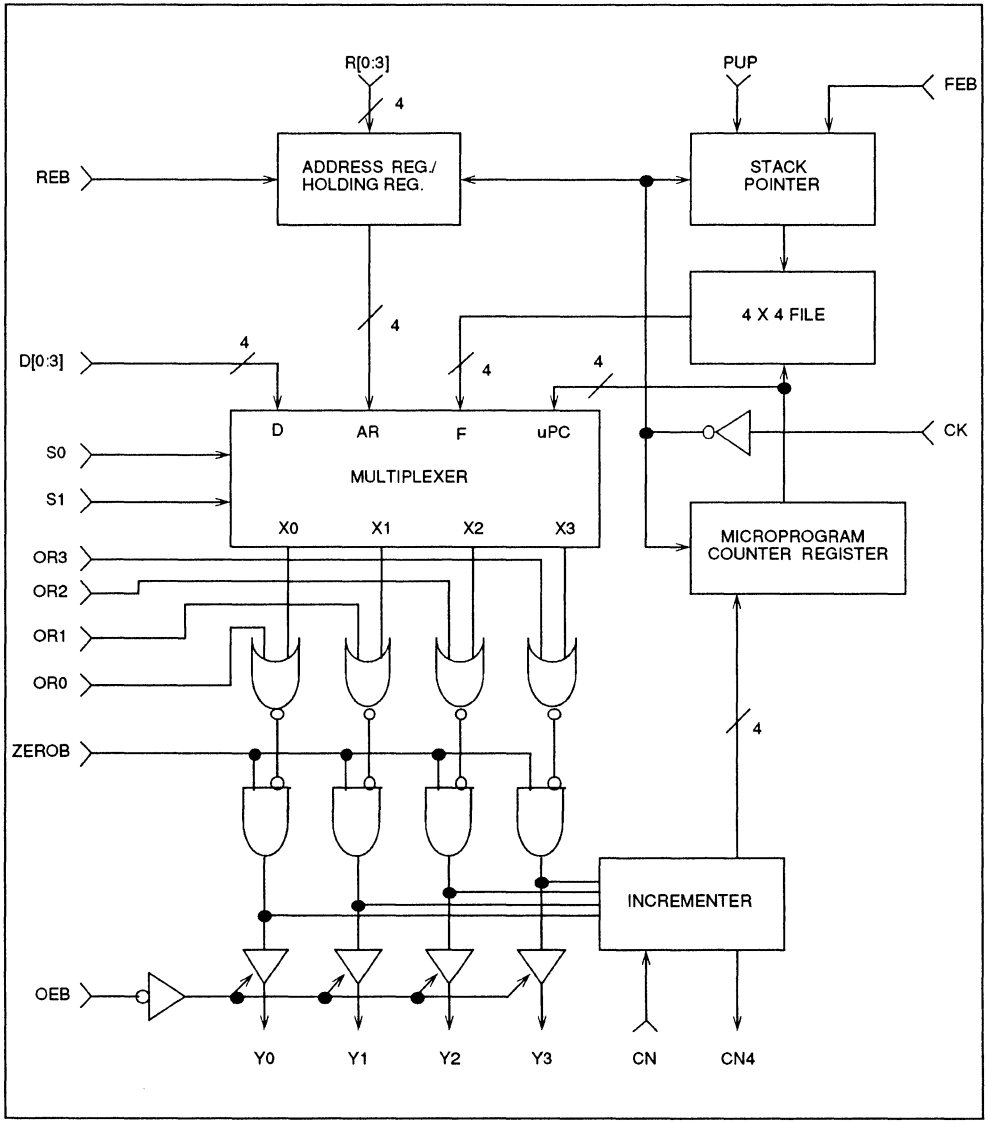
Inputs:

CK	Clock
R[0:3]	Inputs to the internal address register
REB	Enable line for internal address register, active low
D[0:3]	Direct inputs to the multiplexer
S[0:1]	Control lines for address source selection
OR[0:3]	Logic OR inputs on each address output line
ZEROB	Logic AND input on the output lines, active low
OEB	Output enable, active low
CN	Carry-in to the incrementer
FEB	Control line for the push/pop stack, active low
PUP	Control line for the push/pop stack

Outputs:

Y[0:3]	Address outputs
CN4	Carry out from the incrementer

BLOCK DIAGRAM



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CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
CK↑	CN4↑	19.67	3.70	8.05	0.68
CK↑	CN4↓	14.71	2.54	6.29	0.55
CK↑	Y[0:3]↑	15.81	3.70	6.62	0.68
CK↑	Y[0:3]↓	12.00	2.54	5.29	0.55
D[0:3]	CN4↑	15.67	3.70	5.52	0.68
D[0:3]	CN4↓	11.90	2.54	4.43	0.55
D[0:3]	Y[0:3]↑	11.81	3.70	4.10	0.68
D[0:3]	Y[0:3]↓	9.19	2.54	3.43	0.55
OEB	Y[0:3]↑	3.29	3.70	0.95	0.68
OEB	Y[0:3]↓	3.10	2.54	0.86	0.55
OR[0:3]	CN4↑	13.24	3.70	4.62	0.68
OR[0:3]	CN4↓	8.86	2.54	3.24	0.55
OR[0:3]	Y[0:3]↑	9.38	3.70	3.19	0.68
OR[0:3]	Y[0:3]↓	6.14	3.70	2.24	0.55
S[0:1]	CN4↑	22.90	3.70	8.10	0.68
S[0:1]	CN4↓	16.19	2.54	5.95	0.55
S[0:1]	Y[0:3]↑	19.05	3.70	6.67	0.68
S[0:1]	Y[0:3]↓	13.48	2.54	4.95	0.55
ZEROB	CN4↑	13.48	3.70	4.71	0.68
ZEROB	CN4↓	8.52	2.54	3.10	0.55
ZEROB	Y[0:3]↑	9.62	3.70	3.29	0.68
ZEROB	Y[0:3]↓	5.81	2.54	2.10	0.55

CHARACTERISTICS (continued)

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CN Setup before CK↑	4.19	2.48
Minimum D[0:3] Setup before CK↑	15.14	6.33
Minimum FEB Setup before CK↑	4.24	2.19
Minimum OR[0:3] Setup before CK↑	12.71	5.43
Minimum PUP Setup before CK↑	9.05	3.62
Minimum R[0:3] Setup before CK↑	1.48	1.10
Minimum REB Setup before CK↑	2.90	1.67
Minimum S[0:1] Setup before CK↑	22.38	8.90
Minimum ZEROB Setup before CK↑	12.95	5.52

4-Phase Clock Generator — CKGEN

128 grids, 218 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The CKGEN is a 4-phase non-overlapping clock generator. It is designed for logic verification and not meant to drive large capacitive loads.

- NAND NOR implementation
- Minimum built-in non-overlap

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: CKI;

OUTPUTS: MCK, SCK, MCKN, SCKN;

Functional Descriptions

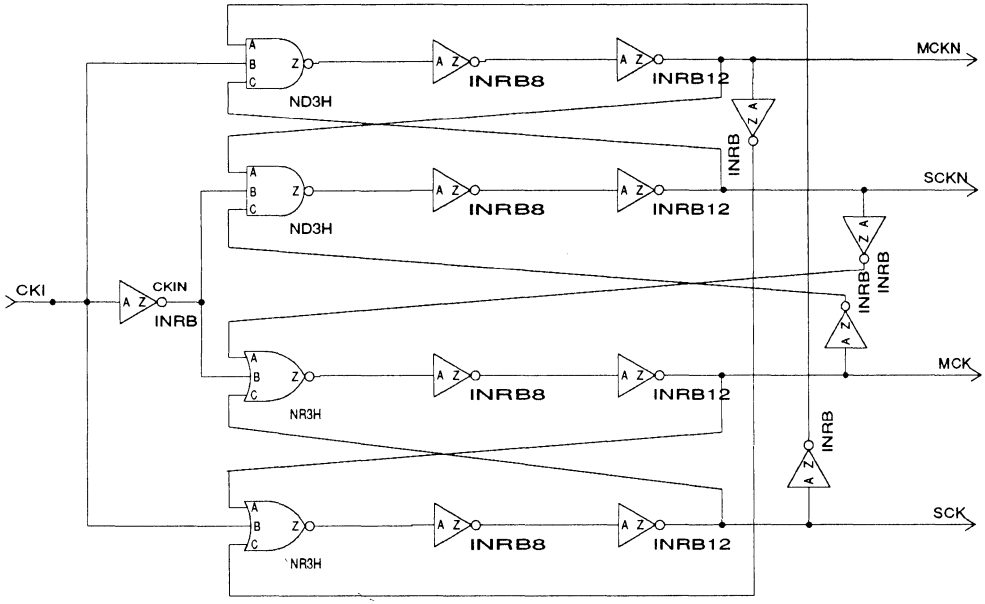
Inputs:

CKI	Input clock

Outputs:

MCK	Master clock
SCK	Slave clock
MCKN	Complement of MCK
SCKN	Complement of SCK

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS
VDD=5.0V, T=25°C, Nominal Processing

From Input	To Output	Area		Performance	
		Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
CKI↑	MCK↑	4.67	0.36	3.67	0.08
CKI↓	MCK↓	1.90	0.49	1.48	0.08
CKI↓	SCK↑	4.62	0.36	3.48	0.08
CKI↑	SCK↓	0.76	0.49	0.57	0.08
CKI↓	MCKN↑	1.14	0.36	0.90	0.08
CKI↑	MCKN↓	3.19	0.49	2.71	0.08
CKI↑	SCKN↑	1.57	0.36	1.33	0.08
CKI↓	SCKN↓	4.00	0.49	3.29	0.08

12

BCD-to-Decimal Decoder CM42

58 grids, 80 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The CM42 is functionally equivalent to the 7442 4-Line-TO-10-Line BCD-to-Decimal Decoder within the standard 74XX Series logic families of devices.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A, B, C, D;

OUTPUTS: Z0, Z1, Z2, Z3, Z4, Z5, Z6, Z7, Z8, Z9;

Functional Descriptions

Inputs:

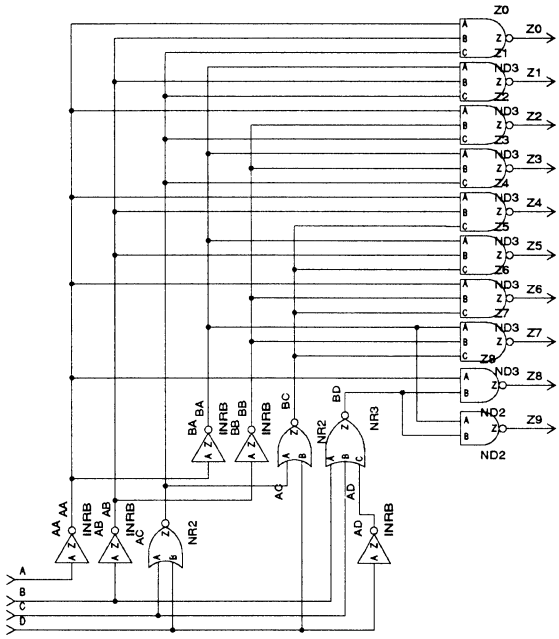
A, B, C, D	BCD inputs

Outputs:

Z[0:9]	Decimal output

12

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
A,B,C,D	Z[0:9]↑	10.85	3.79	3.67	0.70
A,B,C,D	Z[0:9]↓	7.95	4.19	2.86	0.89

12

2-Bit Binary Full Adder — CM82

48 grids, 68 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The CM82 is functionally equivalent to the 7482 2-Bit Binary FULL ADDER within the standard 74XX Series logic families of devices.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: C0, A0, B0, A1, B1;

OUTPUTS: S0, S1, C2;

Functional Descriptions

Inputs:

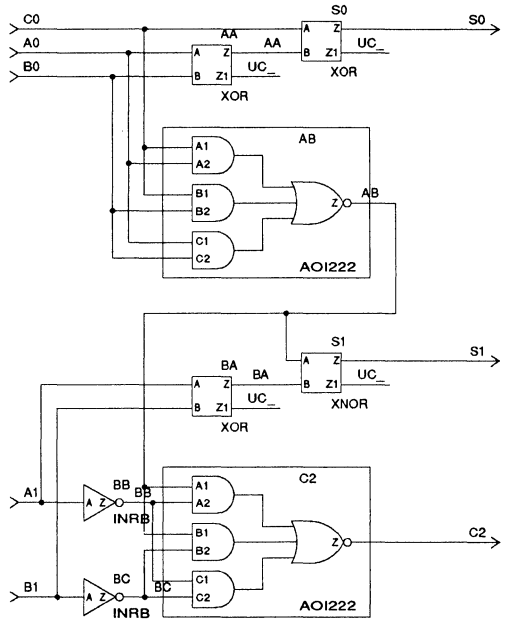
C0	Carry input
A[0:1], B[0:1]	Data input

Outputs:

S[0:1]	Sum output
C2	Carry output

12

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
A0,B0	C2↑	3.38	9.45	1.71	1.75
A0,B0	C2↓	7.67	4.28	3.09	0.96
A0,B0	S[0:1]↑	8.09	9.45	3.33	1.82
A0,B0	S[0:1]↓	7.43	12.53	2.90	2.61
A1,B1	C2↑	1.48	9.45	0.76	1.75
A1,B1	C2↓	2.05	4.28	0.81	0.96
A1,B1	S1↑	2.86	0.37	1.38	0.35
A1,B1	S1↓	2.57	0.42	1.19	0.37
C0	C2↑	3.38	9.45	1.71	1.75
C0	C2↓	7.67	4.28	3.09	0.96
C0	S[0:1]↑	8.09	9.45	3.33	1.82
C0	S[0:1]↓	7.43	12.53	2.90	2.61

12

4-Bit Magnitude Comparator — CM85

104 grids, 144 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The CM85 is functionally equivalent to the 7485 4-Bit Magnitude Comparator within the standard 74XX Series logic families of devices.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: ALBI, AEBI, AGBI, A3, B3, A2, B2, A1, B1, A0, B0;

OUTPUTS: ALBO, AEBO, AGBO;

Functional Descriptions

Inputs:

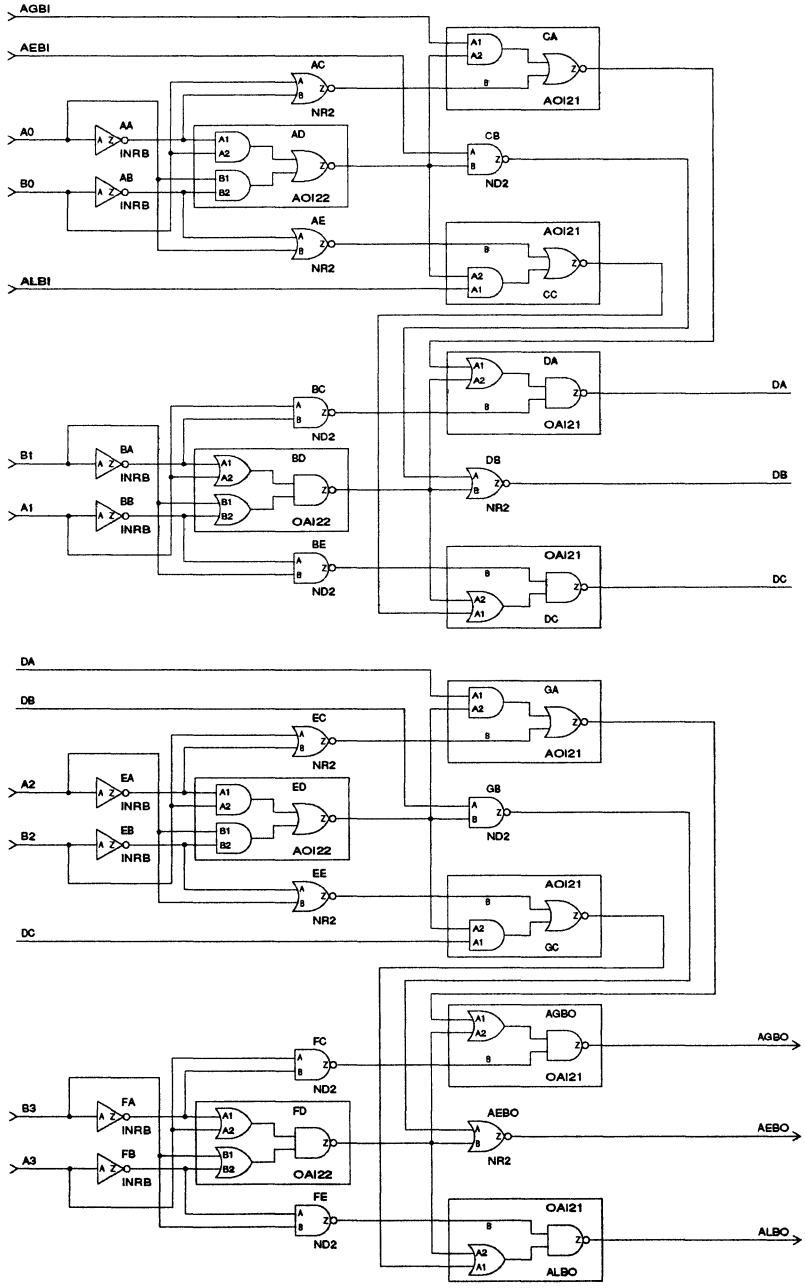
A[L,E,G]BI	Cascading inputs
A[3:0], B[3:0]	Data inputs

Outputs:

ALBO	A less than B output
AEBO	A equal to B output
AGBO	A greater than B output

12

DETAILED SCHEMATIC



12

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
A[0:3],B[0:3]	AEBO↑	10.24	6.73	3.62	1.23
A[0:3],B[0:3]	AEBO↓	7.52	4.19	2.71	0.91
A[0:3],B[0:3]	ALBO,AGBO↑	10.29	6.73	3.81	1.23
A[0:3],B[0:3]	ALBO,AGBO↓	10.00	4.19	3.71	0.91
AEBI	AEBO↑	4.14	6.73	1.48	1.23
AEBI	AEBO↓	2.76	4.19	0.95	0.91
AGBI	AGBO↑	4.19	6.73	1.71	1.23
AGBI	AGBO↓	5.33	4.19	2.00	0.91
ALBI	ALBO↑	4.19	6.73	1.71	1.23
ALBI	ALBO↓	5.33	4.19	2.00	0.91

3-to-8-Line Decoder/Demultiplexer CM138

56 grids, 82 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The CM138 is functionally equivalent to the 74138 3-TO-8-Line Decoder/Demultiplexer within the standard 74XX Series logic families of devices.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A, B, C, G1, G2A, G2B;

OUTPUTS: Z0, Z1, Z2, Z3, Z4, Z5, Z6, Z7;

Functional Descriptions

Inputs:

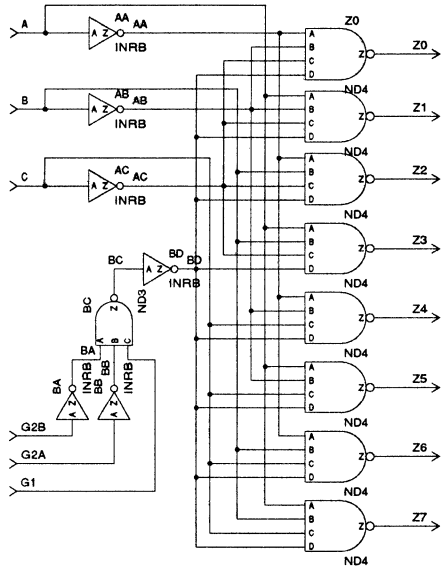
A, B, C,	Select inputs
G1, G2[A,B]	Enable inputs

Outputs:

Z[0:7]	Data outputs

12

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
A,B,C	Z[0:7]↑	1.57	3.97	0.67	0.73
A,B,C	Z[0:7]↓	3.48	7.40	1.29	1.64
G1,G2A,G2B	Z[0:7]↑	5.19	3.97	2.00	0.73
G1,G2A,G2B	Z[0:7]↓	9.05	7.40	3.33	1.64

12

1-of-16 Gated Data Select/Multiplexer CM150

88 grids, 134 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The CM150 is functionally equivalent to the 74150 1-OF-16 Gated Data Select/Multiplexer within the standard 74XX Series logic families of devices.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, A, B, C, D, SN;

OUTPUTS: Z;

Functional Descriptions

Inputs:

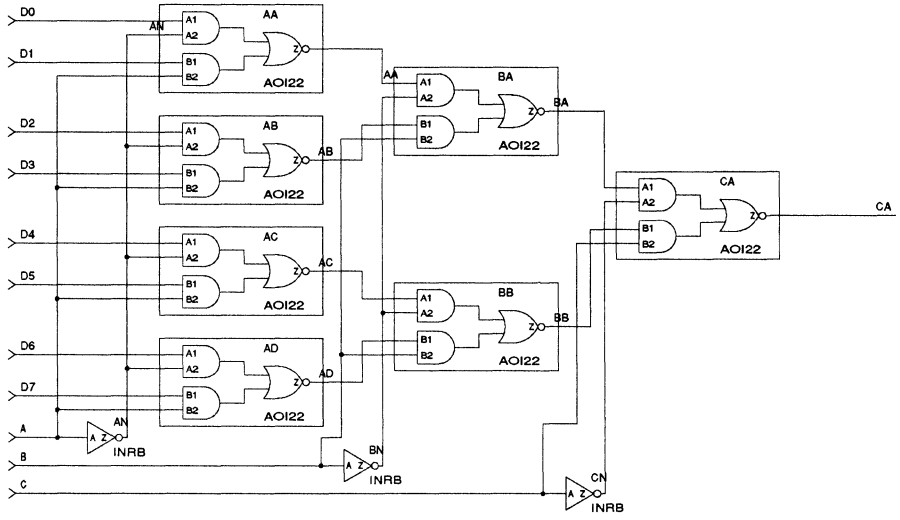
D[0:15]	Data inputs
A, B, C, D	Data select inputs
SN	Strobe input, active low

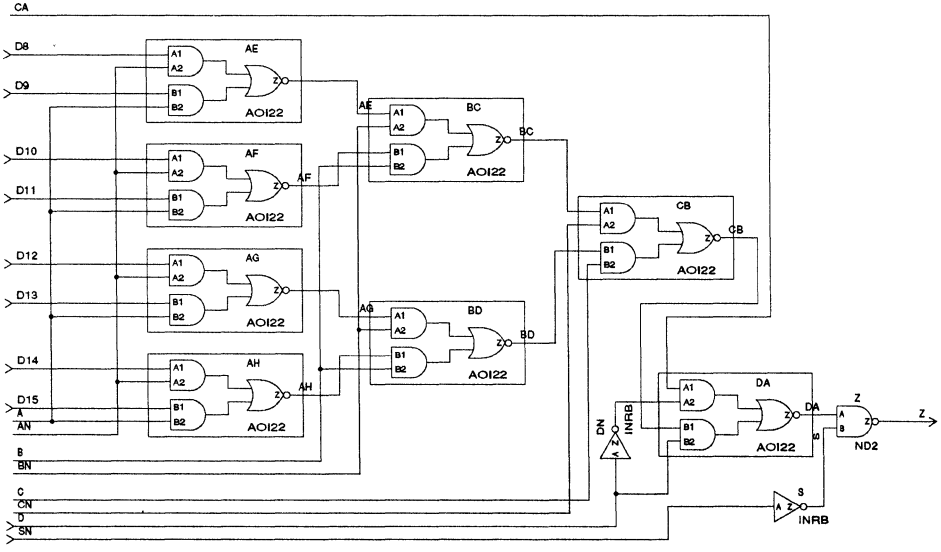
Outputs:

Z	Inverted data output

12

DETAILED SCHEMATIC





CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
A,B,C,D	Z↑	9.81	3.79	3.81	0.70
A,B,C,D	Z↓	12.95	4.19	4.57	0.89
D[0:15]	Z↑	6.90	3.79	2.57	0.70
D[0:15]	Z↓	6.33	4.19	2.48	0.89
SN	Z↑	0.52	3.79	0.24	0.70
SN	Z↓	1.05	4.19	0.43	0.89

1-of-8 Gated Data Select/Multiplexer CM151

46 grids, 68 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The CM151 is functionally equivalent to the 74151 1-OF-8 Gated Data Select/Multiplexer within the standard 74XX Series logic families of devices.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: D0, D1, D2, D3, D4, D5, D6, D7, A, B, C, SN;

OUTPUTS: Y, W;

Functional Descriptions

Inputs:

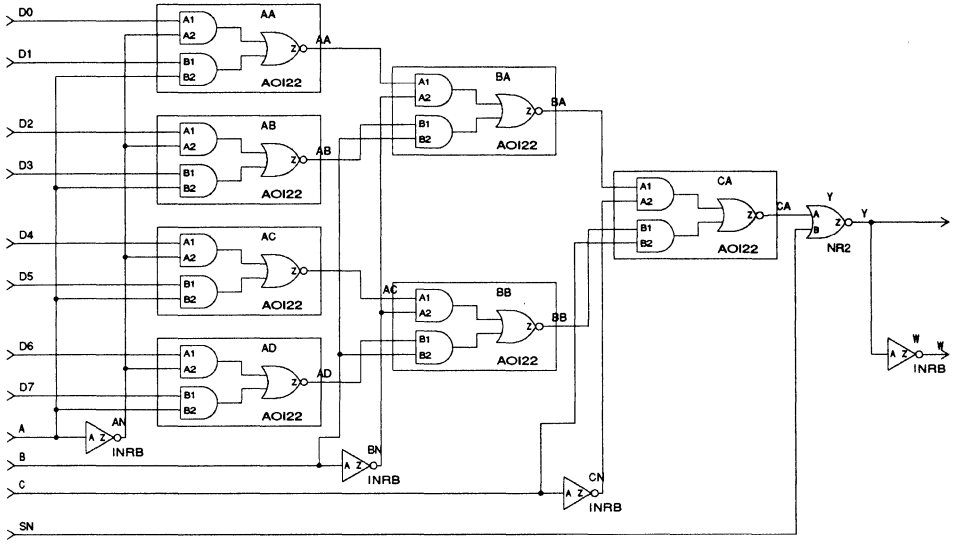
D[0:7]	Data inputs
A, B, C	Data select inputs
SN	Strobe input, active low

Outputs:

W	Inverted output
Y	Output

12

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS
VDD=5.0V, T=25°C, Nominal Processing

From Input	To Output	Area		Performance	
		Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
A,B,C	Y↑	9.33	6.64	3.33	1.20
A,B,C	Y↓	7.81	2.67	2.90	0.55
A,B,C	W↑	8.00	3.70	3.00	0.68
A,B,C	W↓	9.90	2.54	3.57	0.55
D[0:7]	Y↑	5.66	6.64	2.14	1.20
D[0:7]	Y↓	6.19	2.67	2.29	0.55
D[0:7]	W↑	6.38	3.70	2.38	0.68
D[0:7]	W↓	6.24	2.54	2.38	0.55
SN	Y↑	1.24	6.64	0.38	1.20
SN	Y↓	0.33	2.67	0.14	0.55
SN	W↑	0.52	3.70	0.24	0.68
SN	W↓	1.81	2.54	0.62	0.55

1-of-8 Data Select/Multiplexer CM152

41 grids, 62 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The CM152 is functionally equivalent to the 74152 1-OF-8 Data Select/Multiplexer within the standard 74XX Series logic families of devices.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: D0, D1, D2, D3, D4, D5, D6, D7, A, B, C;

OUTPUTS: Z;

Functional Descriptions

Inputs:

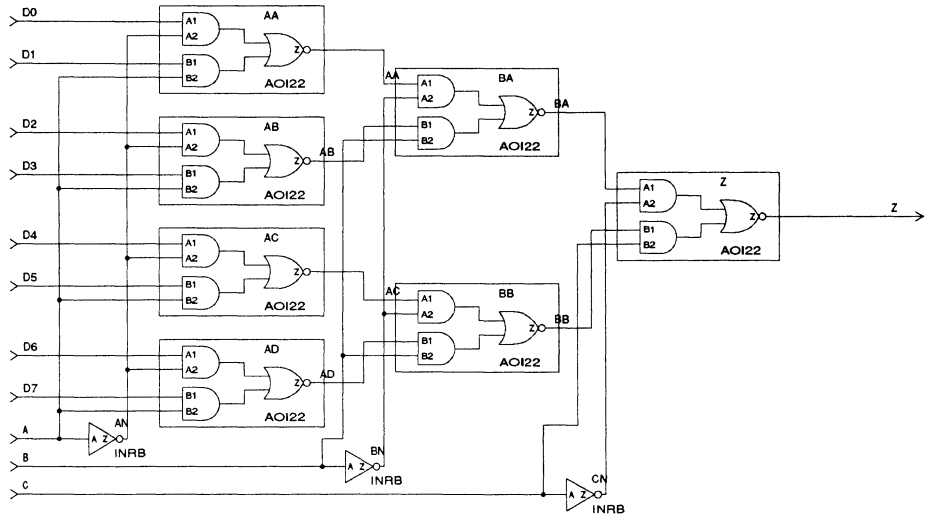
D[0:7]	Data inputs
A, B, C	Select inputs

Outputs:

Z	Inverted output

12

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
A,B,C	Z↑	5.29	6.73	2.10	1.25
A,B,C	Z↓	6.90	4.19	2.48	0.91
D[0:7]	Z↑	3.67	6.73	1.48	1.25
D[0:7]	Z↓	3.24	4.19	1.28	0.91

12

4-Line-to-1 Data Select/Multiplexer CM153X

24 grids, 34 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The CM153X is functionally equivalent to one-half of the 74153 DUAL 4-Line-TO-1-Line Data Select/Multiplexer within the standard 74XX Series logic families of devices.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: 1GN, 1D0, 1D1, 1D2, 1D3, A, B;

OUTPUTS: 1Z;

Functional Descriptions

Inputs:

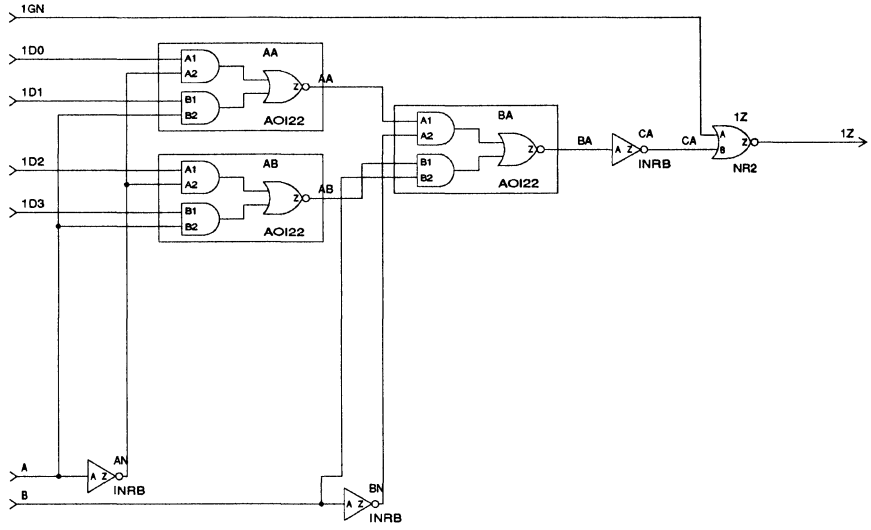
1GN	Strobe input, active low
1D[0:3]	Data inputs
A, B	Select inputs

Outputs:

1Z	Data output

12

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
1D[0:3]	1Z↑	4.05	6.64	1.57	1.20
1D[0:3]	1Z↓	4.52	2.67	1.62	0.55
1GN	1Z↑	0.47	6.64	0.25	1.20
1GN	1Z↓	1.30	2.67	0.43	0.55
A,B	1Z↑	6.19	6.64	2.24	1.20
A,B	1Z↓	5.29	2.67	2.00	0.55

12

2-Line-1-Line Data Select/Multiplexer CM157X

10 grids, 14 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The CM157X is functionally equivalent to one-fourth of the 74157 Quadruple 2-Line-TO-1-Line Data Select/Multiplexer within the standard 74XX Series logic families of devices.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A1, B1, S, GN;

OUTPUTS: Z1;

Functional Descriptions

Inputs:

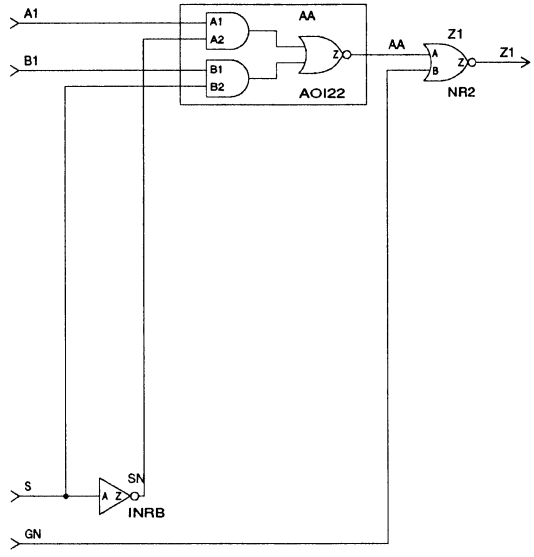
A1, B1	Data inputs
S	Select input
GN	Strobe input, active low

Outputs:

Z1	Data output

12

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
A1,B1	Z1↑	1.09	6.64	0.52	1.20
A1,B1	Z1↓	1.86	2.67	0.71	0.55
GN	Z1↑	0.47	6.64	0.25	1.20
GN	Z1↓	1.30	2.67	0.43	0.55
S	Z1↑	2.33	6.64	0.95	1.20
S	Z1↓	2.33	2.67	0.90	0.55

12

2-Line-1-Line Data Select/Multiplexer CM158X

13 grids, 18 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The CM158X is functionally equivalent to one-fourth of the 74158 Quadruple 2-Line-TO-1-Line Inverting Data Select/Multiplexer within the standard 74XX Series logic families of devices.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A1, B1, GN, S;

OUTPUTS: Z1;

Functional Descriptions

Inputs:

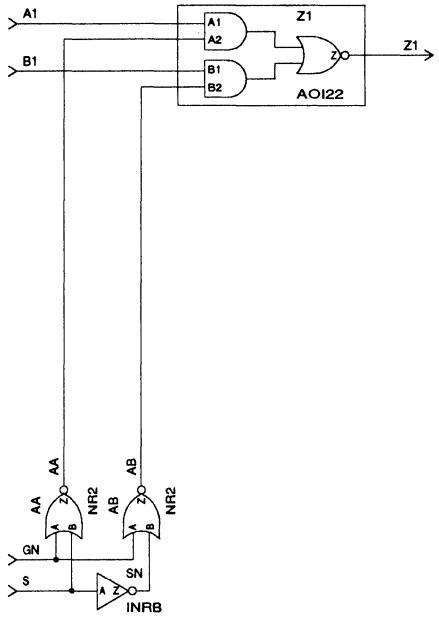
A1, B1	Data inputs
GN	Strobe input, active low
S	Select input

Outputs:

Z1	Inverted data output

12

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
A1,B1	Z1↑	0.33	6.73	0.14	1.25
A1,B1	Z1↓	0.33	4.19	0.09	0.91
GN	Z1↑	0.81	6.73	0.33	1.25
GN	Z1↓	2.05	4.19	0.76	0.91
S	Z1↑	2.05	6.73	0.76	1.25
S	Z1↓	2.48	4.19	0.95	0.91

12

Synchronous 4-Bit Decade Counter CM160

150 grids, 216 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The CM160 is functionally equivalent to the 74160 Synchronous 4-Bit Decade Counter with Asynchronous CLEAR within the standard 74XX Series logic families of devices.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A, B, P, L, T, CK, CD, C, D;

OUTPUTS: QA, QAN, QB, QBN, QC, QCN, QD, QDN, CO;

Functional Descriptions

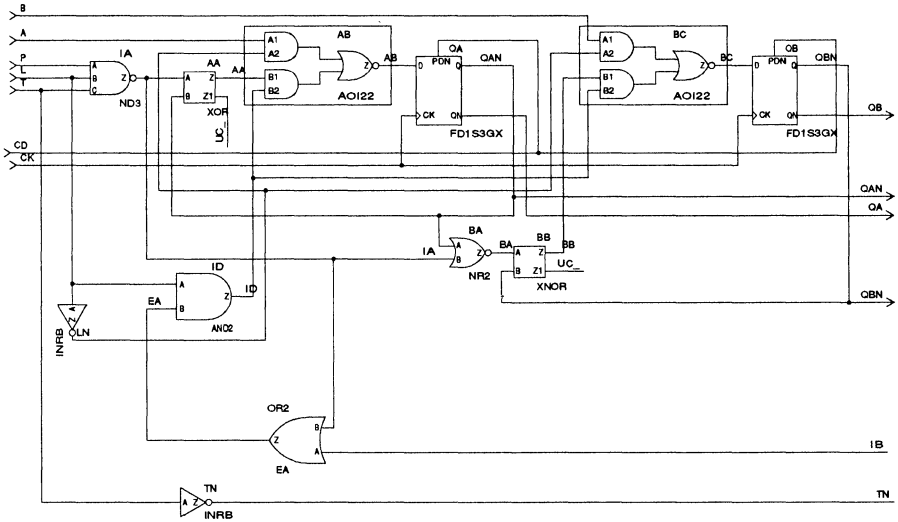
Inputs:

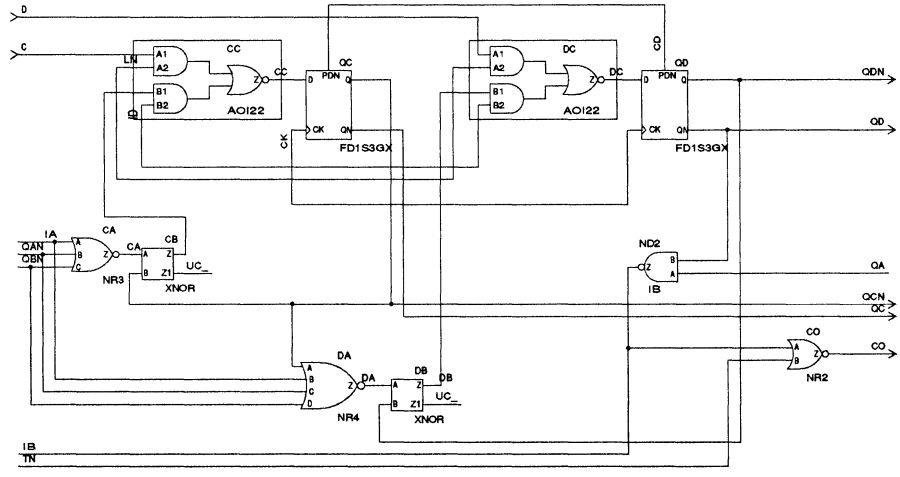
A, B, C, D	Data inputs
P, T	Enable inputs
L	Load input, active low
CK	Clock input
CD	Asynchronous clear input, active low

Outputs:

Q[A,B,C,D]	Data outputs
Q[A,B,C,D]N	Complimentary data outputs
CO	Carry output

DETAILED SCHEMATIC





CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From Input	To Output	Area		Performance	
		Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
CD↓	ANY Q↓	3.17	3.70	1.14	0.78
CD↓	ANY QN↑	2.96	7.09	1.49	1.41
CK↑	ANY Q↑	4.95	6.73	2.52	1.36
CK↑	ANY Q↓	5.76	10.57	3.10	1.98
CK↑	CO↑	3.14	6.64	2.10	1.20
CK↑	CO↓	2.38	2.67	1.38	0.55
T	CO↑	0.62	6.64	0.29	1.20
T	CO↓	1.00	2.67	0.38	0.55

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum A,B,C,D Setup before CK↑	2.67	1.52
Minimum L Setup before CK↑	14.57	6.81
Minimum P Setup before CK↑	14.57	6.81
Minimum T Setup before CK↑	14.57	6.81

12

Synchronous 4-Bit Binary Counter CM161

143 grids, 206 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The CM161 is functionally equivalent to the 74161 Synchronous 4-Bit Binary Counter with Asynchronous CLEAR within the standard 74XX Series logic families of devices.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A, B, P, T, CK, CD, L, C, D;

OUTPUTS: QA, QAN, QB, QBN, QC, QCN, QD, QDN, CO;

Functional Descriptions

Inputs:

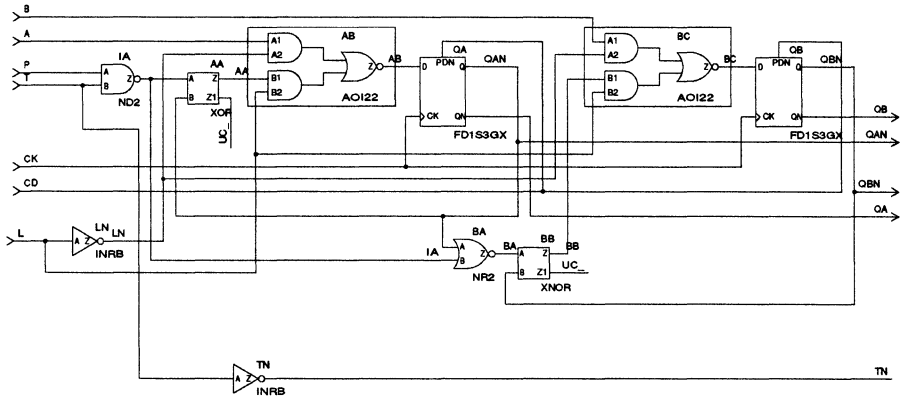
A, B, C, D	Data inputs
P, T	Enable inputs
CK	Clock input
CD	Asynchronous clear input, active low
L	Load input, active low

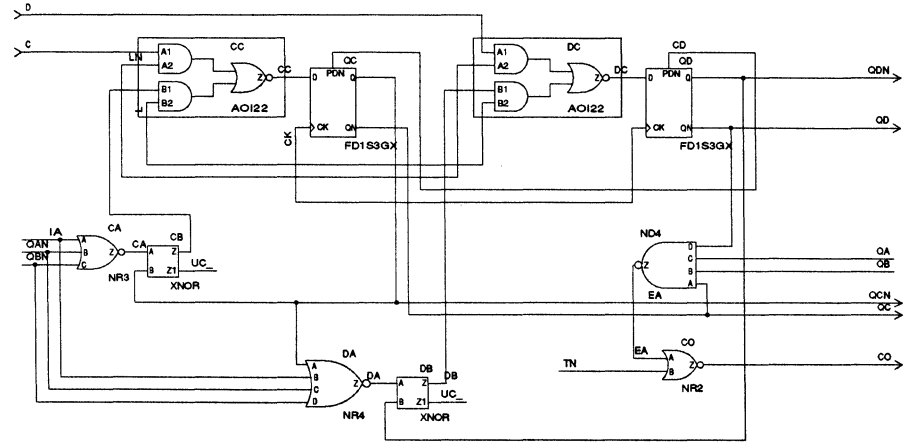
Outputs:

Q[A,B,C,D]	Data outputs
Q[A,B,C,D]N	Complimentary data outputs
CO	Carry output

12

DETAILED SCHEMATIC





12

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
CD↓	ANY Q↓	3.17	3.70	1.14	0.78
CD↓	ANY QN↑	2.96	7.09	1.49	1.41
CK↑	ANY Q↑	4.95	6.73	2.52	1.36
CK↑	ANY Q↓	5.76	10.57	3.10	1.98
CK↑	CO↑	3.14	6.64	2.10	1.20
CK↑	CO↓	1.76	2.67	1.14	0.55
T	CO↑	0.62	6.64	0.29	1.20
T	CO↓	1.00	2.67	0.38	0.55

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum A,B,C,D Setup before CK↑	2.67	1.52
Minimum L Setup before CK↑	5.81	2.57
Minimum P Setup before CK↑	11.86	5.48
Minimum T Setup before CK↑	11.86	5.48

12

Synchronous 4-Bit Decade Counter CM162

141 grids, 200 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The CM162 is functionally equivalent to the 74162 Synchronous 4-Bit Decade Counter with Synchronous CLEAR within the standard 74XX Series logic families of devices.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A, B, P, L, T, CK, CL, C, D;

OUTPUTS: QA, QAN, QB, QBN, QC, QCN, QD, QDN, CO;

Functional Descriptions

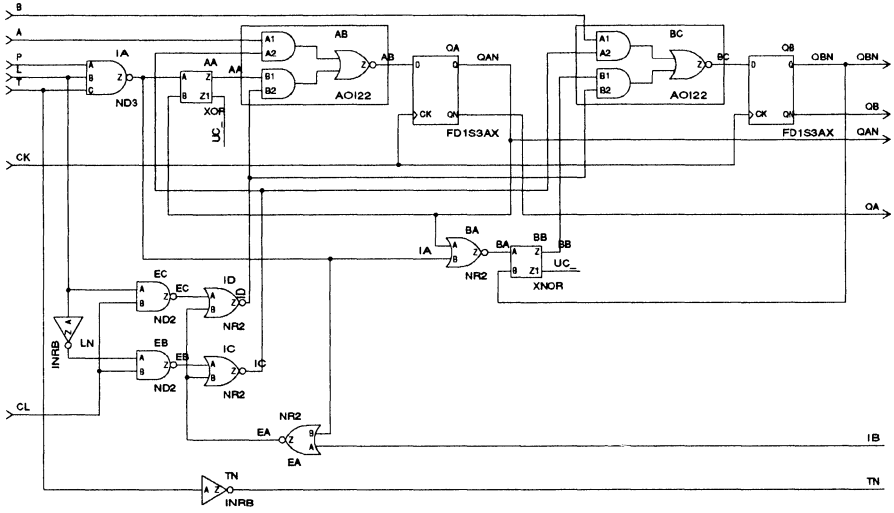
Inputs:

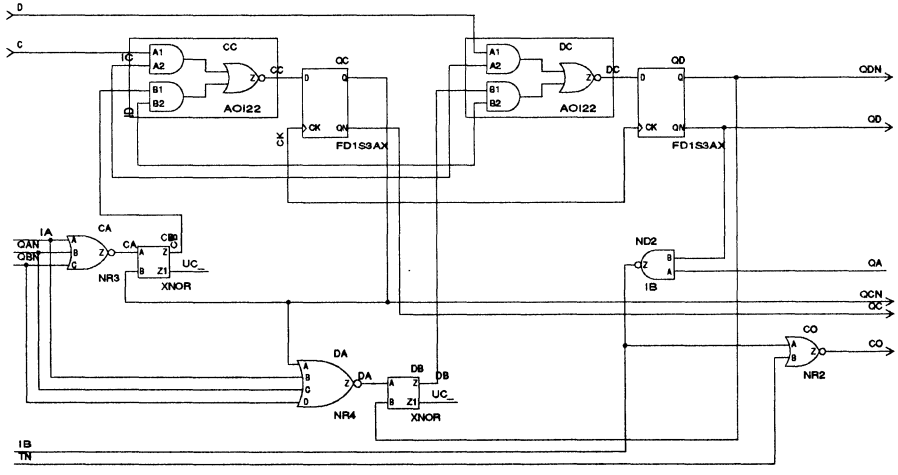
A, B, C, D	Data inputs
P, T	Enable inputs
L	Load input, active low
CK	Clock input
CL	Synchronous clear input, active low

Outputs:

Q[A,B,C,D]	Data outputs
Q[A,B,C,D]N	Complimentary data outputs
CO	Carry output

DETAILED SCHEMATIC





12

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
CK↑	ANY Q↑	3.71	3.70	2.14	0.65
CK↑	ANY Q↓	4.67	9.01	2.24	1.67
CK↑	CO↑	6.14	6.64	3.14	1.20
CK↑	CO↓	6.57	2.67	3.67	0.55
T	CO↑	0.62	6.64	0.29	1.20
T	CO↓	1.00	2.67	0.38	0.55

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum A,B,C,D Setup before CK↑	1.95	1.05
Minimum CL Setup before CK↑	8.71	3.38
Minimum L Setup before CK↑	14.14	6.33
Minimum P Setup before CK↑	14.14	6.33
Minimum T Setup before CK↑	14.14	6.33

12

Synchronous 4-Bit Binary Counter CM163

135 grids, 194 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The CM163 is functionally equivalent to the 74163 Synchronous 4-Bit Decade Counter with Synchronous CLEAR within the standard 74XX Series logic families of devices.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A, B, P, T, CK, L, CL, C, D;

OUTPUTS: QA, QAN, QB, QBN, QC, QCN, QD, QDN, CO;

Functional Descriptions

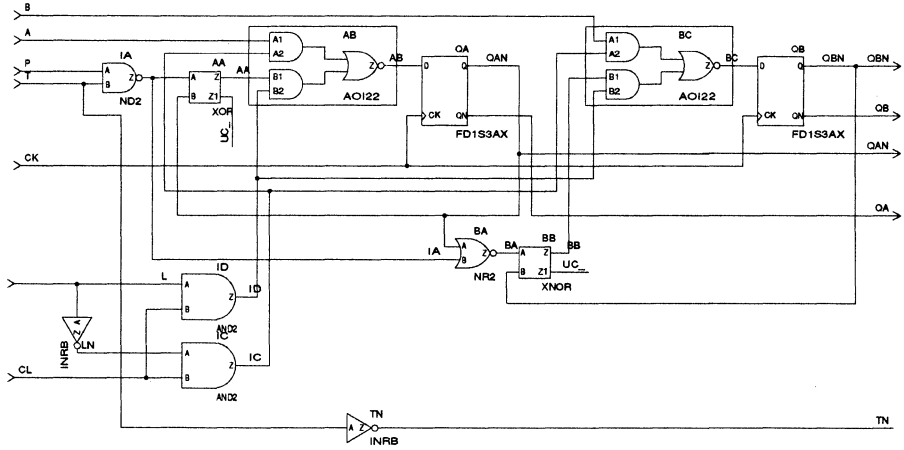
Inputs:

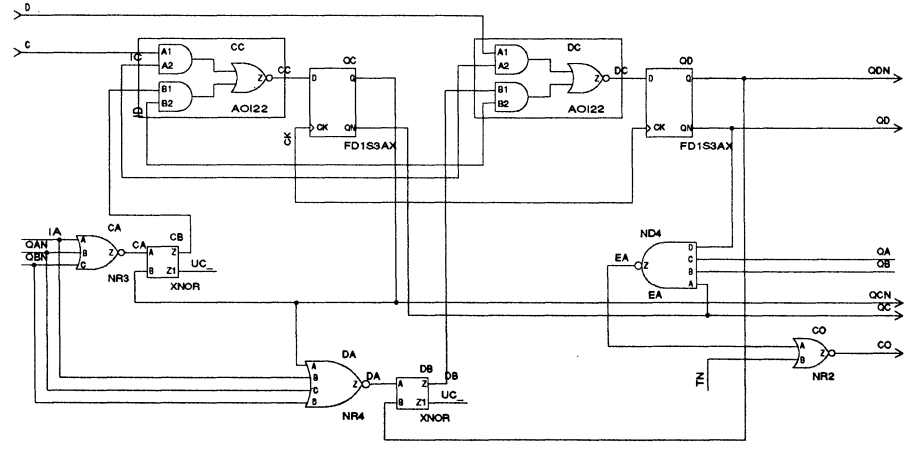
A, B, C, D	Data inputs
P, T	Enable inputs
CK	Clock input
L	Load input, active low
CL	Synchronous clear input, active low

Outputs:

Q[A,B,C,D]	Data outputs
Q[A,B,C,D]N	Complimentary data outputs
CO	Carry output

DETAILED SCHEMATIC





CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
CK↑	ANY Q↑	3.71	3.70	2.14	0.65
CK↑	ANY Q↓	4.67	9.01	2.24	1.67
CK↑	CO↑	6.19	6.64	3.67	1.20
CK↑	CO↓	5.95	2.67	2.90	0.55
T	CO↑	0.62	6.64	0.29	1.20
T	CO↓	1.00	2.67	0.38	0.55

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum A,B,C,D Setup before CK↑	1.90	1.00
Minimum CL Setup before CK↑	5.28	2.33
Minimum L Setup before CK↑	6.38	2.71
Minimum P Setup before CK↑	11.09	5.05
Minimum T Setup before CK↑	11.09	5.05

12

Synchronous 4-Bit Up/Down Counter CM169

161 grids, 228 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The CM169 is functionally equivalent to the 74169 Synchronous 4-Bit Up/Down Counter within the standard 74XX Series logic families of devices.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A, B, PN, TN, CK, UP, L, C, D;

OUTPUTS: QA, QB, QC, QD, CON;

Functional Descriptions

Inputs:

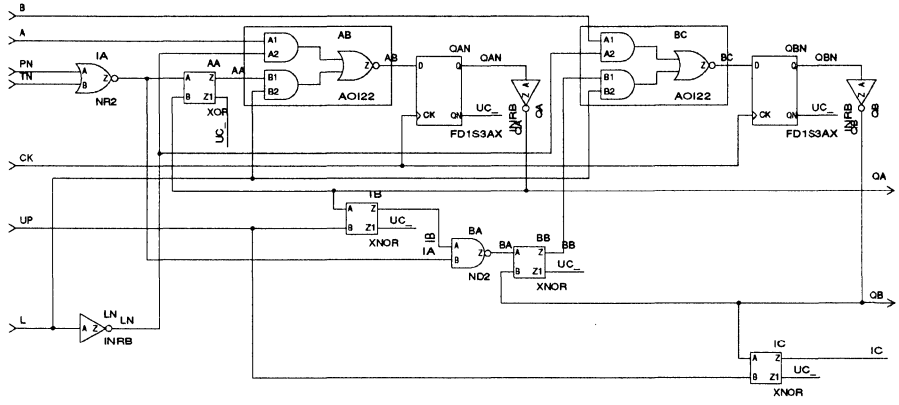
A, B, C, D	Data inputs
PN, TN	Count enable inputs, active low
CK	Clock input
UP	Up/Down select input
L	Load input, active low

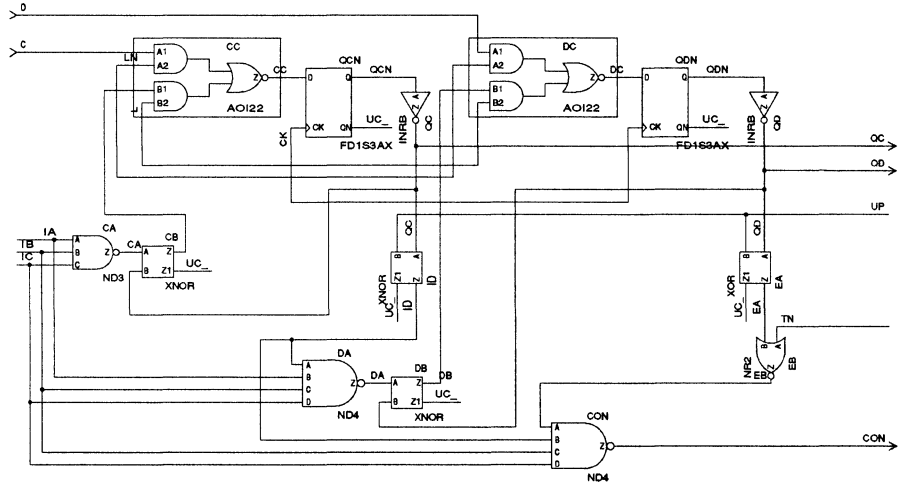
Outputs:

Q[A,B,C,D]	Data outputs
CON	Inverted Carry output

12

DETAILED SCHEMATIC





12

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
CK↑	ANY Q↑	2.14	3.70	1.48	0.68
CK↑	ANY Q↓	2.29	2.54	2.05	0.55
CK↑	CON↑	6.57	3.97	3.67	0.73
CK↑	CON↓	8.71	7.40	4.38	1.64
TN	CON↑	0.62	3.97	0.29	0.73
TN	CON↓	2.28	7.40	0.81	1.64
UP	CON↑	3.29	3.97	1.48	0.73
UP	CON↓	6.10	7.40	2.19	1.64

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum A,B,C,D Setup before CK↑	1.90	1.00
Minimum L Setup before CK↑	5.05	2.05
Minimum PN Setup before CK↑	13.19	5.33
Minimum TN Setup before CK↑	13.19	5.33
Minimum UP Setup before CK↑	12.62	5.05

12

Cyclic Redundancy Checker — CRC

1620 grids, 2434 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

This subcircuit is used to check or generate the CCITT Cyclic Redundancy Check when connected to parallel bus (8 or 16 bit wide). The design operates with INTEL 8051, 80186 (8MHz) and MC68010 (10MHz) microprocessors. The subcircuit receives asynchronous signals from the microprocessor and synchronizes them to internal chip clock of the semi-custom circuit.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: CLK, READ, OVRDCSN, CSN, AD1, AD0, WORDN, QUAL, BLDATI0, BLDATI1, BLDATI2, BLDATI3, BLDATI4, BLDATI5, BLDATI6, BLDATI7, BHDATI0, BHDATI1, BHDATI2, BHDATI3, BHDATI4, BHDATI5, BHDATI6, BHDATI7;

OUTPUTS: LMCRC0, LMCRC1, LMCRC2, LMCRC3, LMCRC4, LMCRC5, LMCRC6, LMCRC7, HMCRC0, HMCRC1, HMCRC2, HMCRC3, HMCRC4, HMCRC5, HMCRC6, HMCRC7, CRCCKN;

Functional Descriptions

Inputs:

CLK	Clock
READ	Read/$\overline{\text{Write}}$
OVRDCSN	Override chip select (active low)
CSN	Chip select (active low)
AD[1:0]	Address leads
WORDN	Byte/$\overline{\text{Word}}$ Mode
QUAL	Qualifier
BLDATI[0:7]	Lower order data bus
BHDATI[0:7]	Higher order data bus

Outputs:

LMCRC[0:7]	Lower order data bus
HMCRC[0:7]	Higher order data bus
CRCCKN	CRC check (active low)

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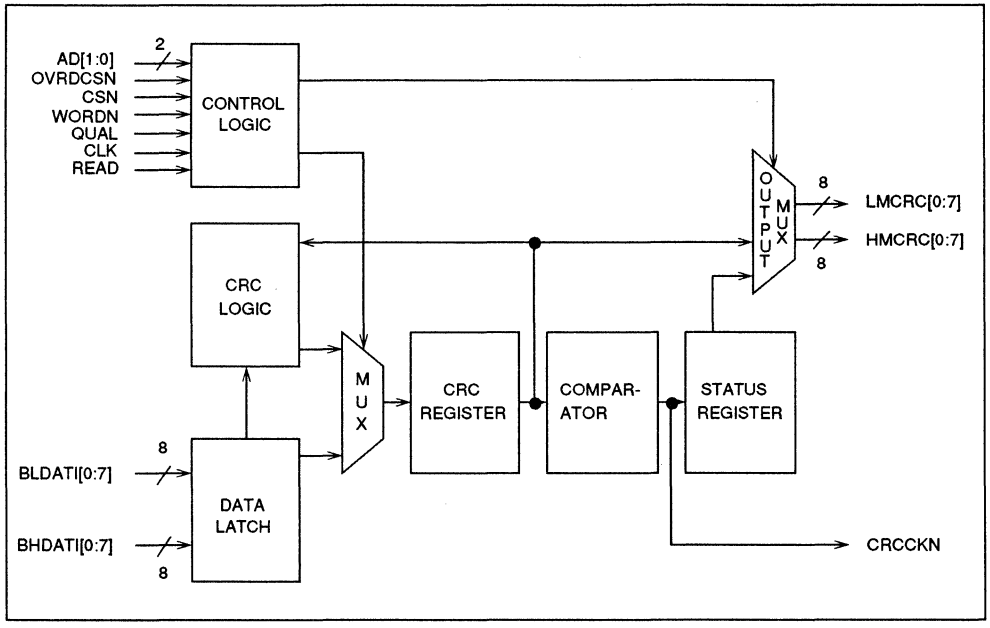
BLOCK DIAGRAM



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From Input	To Output	Area		Performance	
		Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
AD[0:1]	LMCRC[0:7]↑	13.33	3.79	4.90	0.70
AD[0:1]	LMCRC[0:7]↓	11.90	4.19	4.62	0.89
AD[0:1]	HMCRC[0:7]↑	7.00	3.70	2.86	0.68
AD[0:1]	HMCRC[0:7]↓	8.57	2.54	3.19	0.55
CLK	CRCCKN↑	13.05	1.03	7.00	0.18
CLK	CRCCKN↓	15.19	1.29	8.05	0.26
CLK	LMCRC[0:7]↑	14.29	3.79	7.52	0.70
CLK	LMCRC[0:7]↓	17.24	4.19	8.86	0.89
CLK	HMCRC[0:7]↑	11.48	3.70	6.29	0.68
CLK	HMCRC[0:7]↓	12.05	2.54	5.71	0.55
WORDN	LMCRC[0:7]↑	10.86	3.79	4.33	0.70
WORDN	LMCRC[0:7]↓	10.86	4.19	4.24	0.89

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum AD[0:1] Setup before CLK	0.67	0.67
Minimum BLDATI[0:7] Setup before CLK	0.67	0.67
Minimum BHDATI[0:7] Setup before CLK	0.67	0.67
Minimum CSN Setup before CLK	0.67	0.67
Minimum OVRDCSN Setup before CLK	0.67	0.67
Minimum READ Setup before CLK	0.67	0.67

Divide-by-4 Counter DIV4

43 grids, 58 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

DIV4 is a twisted ring divide-by-4 counter with data select front end. For frequency division the SC input should be high.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: DI, SC, CK, CD;

OUTPUTS: Q1;

Functional Descriptions

Inputs:

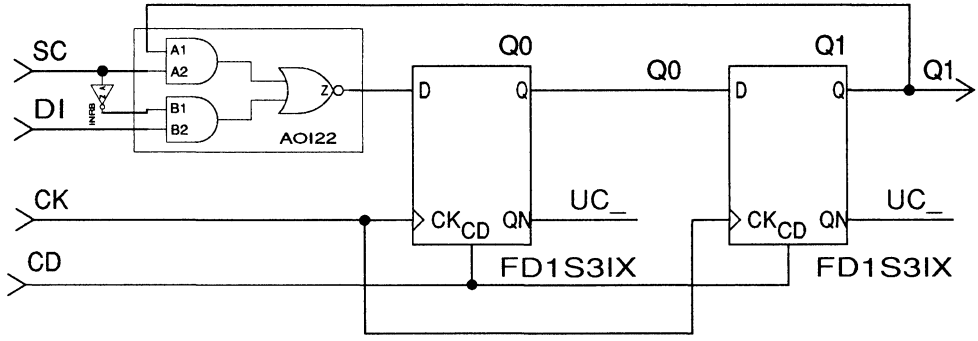
DI	Test data input
SC	Mode select
CK	Clock input
CD	Synchronous clear input

Outputs:

Q1	Divide by 4 output

12

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
CK↑	Q1↑	1.00	8.92	0.76	1.69
CK↑	Q1↓	1.05	6.55	0.71	1.36

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.33
Minimum DI Setup before CK↑	2.05	1.81
Minimum SC Setup before CK↑	3.71	2.05

12

Divide-by-6 Counter DIV6

61 grids, 82 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

DIV6 is a twisted ring divide-by-6 counter with data select front end. For frequency division the SC input should be high.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: DI, SC, CK, CD;

OUTPUTS: Q2;

Functional Descriptions

Inputs:

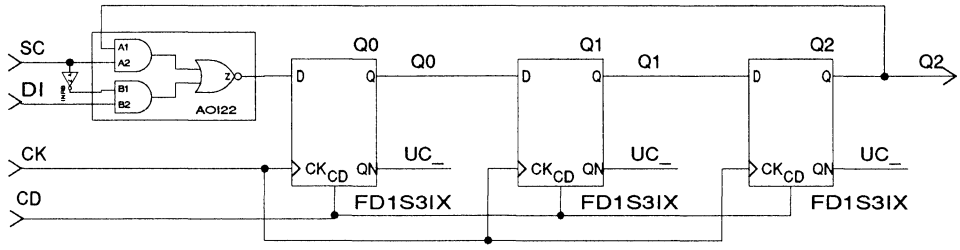
DI	Test data input
SC	Mode select
CK	Clock input
CD	Synchronous clear input

Outputs:

Q2	Divide by 6 output

12

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
CK↑	Q2↑	1.00	8.92	0.76	1.69
CK↑	Q2↓	1.05	6.55	0.71	1.36

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.33
Minimum DI Setup before CK↑	2.05	1.81
Minimum SC Setup before CK↑	3.71	2.05

12

Divide-by-8 Counter DIV8

79 grids, 106 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

DIV8 is a twisted ring divide-by-8 counter with data select front end. For frequency division the SC input should be high.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: DI, SC, CK, CD;

OUTPUTS: Q3;

Functional Descriptions

Inputs:

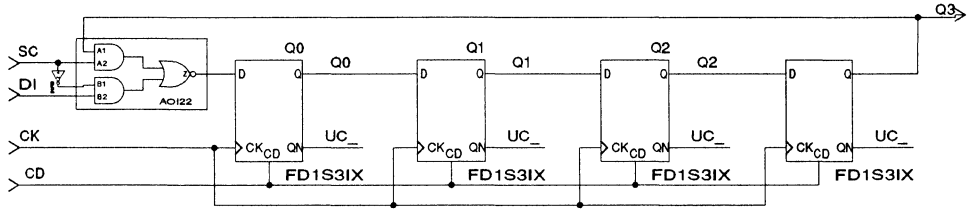
DI	Test data input
SC	Mode select
CK	Clock input
CD	Synchronous clear input

Outputs:

Q3	Divide by 8 output

12

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
CK↑	Q3↑	1.00	8.92	0.76	1.69
CK↑	Q3↓	1.05	6.55	0.71	1.36

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.33
Minimum DI Setup before CK↑	2.05	1.81
Minimum SC Setup before CK↑	3.71	2.05

12

4-Bit Fast Adder

FA4

143 grids, 212 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The FA4 is functionally equivalent to the 7483 4-Bit Binary Full Adder With Fast Carry within the standard 74XX Series logic families of devices. This full adder circuit provides binary addition of two 4-bit binary numbers, with internal carry look ahead across all four bits for fast operation. The corresponding outputs for each bit are: SUM1, SUM2, SUM3 and SUM4. The carry out is C4.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: A1, A2, A3, A4, B1, B2, B3, B4, C0;

OUTPUTS: SUM1, SUM2, SUM3, SUM4, C4;

Functional Descriptions

Inputs:

A[1:4]	Word 'A' inputs
B[1:4]	Word 'B' inputs
C0	Carry in

Outputs:

SUM[1:4]	Sum outputs
C4	Carry out

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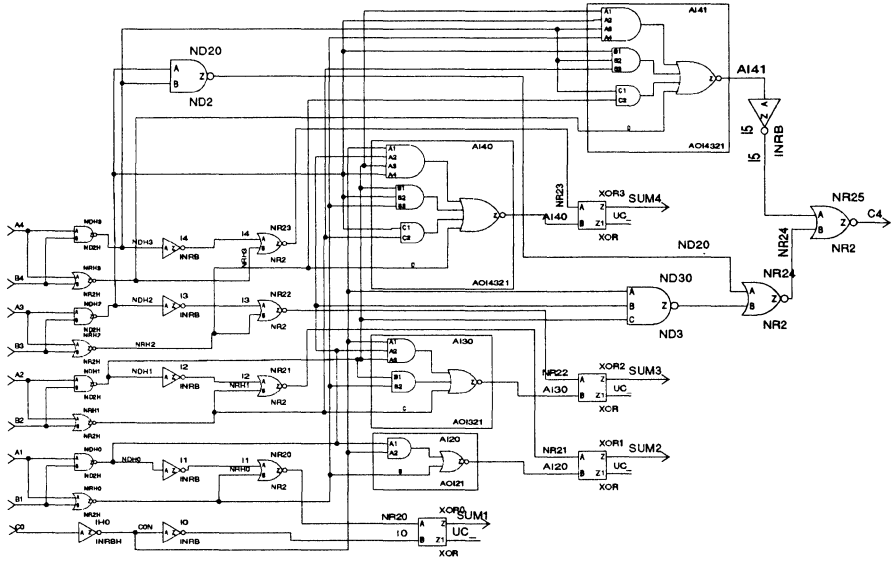
DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
A[1:4],B[1:4]	C4↑	8.81	6.64	3.57	1.20
A[1:4],B[1:4]	C4↓	7.81	2.67	3.10	0.55
A[1:4],B[1:4]	SUM[1:4]↑	8.33	9.45	3.81	1.82
A[1:4],B[1:4]	SUM[1:4]↓	7.90	12.53	3.53	2.61
C0	C4↑	3.05	6.64	1.19	1.20
C0	C4↓	5.57	2.67	2.05	0.55
C0	SUM[1:4]↑	6.71	9.45	3.14	1.82
C0	SUM[1:4]↓	6.29	12.53	2.86	2.61

12

High-Level Data Link Controller — HDLC

4550 grids, 11200 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

This circuit has been designed to perform formatting functions to data when connected to an 8-bit bus. These functions are summarized below. This function conforms with the HDLC specifications described in the International Standard document Ref. No. ISO 3309-1976 (E) entitled *Data Communication - High Level Data Link Control Procedures - Frame Structure.* The HDLC has a transmit section, a receive section, and two Dual-Port RAMS. A block diagram of the HDLC controller is illustrated after the summary of the features.

- CRC (CCITT-16 polynomial cyclic redundancy check) generation and check
- Zero bit stuffing and destuffing.
- Parallel to serial and serial to parallel data conversion.
- Flag generation and detection/deletion.
- Sixteen bytes of queue for both receive and transmit sections.
- Multiple frames can be entered in the receive and transmit queues.
- The CRC is never entered in the receive queue.
- Binary encoding is utilized for all queue levels.
- Number of available bytes to first end of frame in receive queue is included in queue status.
- An end of frame byte in the receive queue includes status information on bad CRC, abort, overrun, and bad byte count.
- Receive queue global status register indicates end of frame, idle and overrun.
- Receive/transmit queue interrupts with 16 programmable fill/empty levels.
- The CRC generated by the transmitter can be externally corrupted for testing purposes.
- Separate programmable data inverts for receiver and transmitter.
- Automatic request to send/clear to send handshaking in the transmitter.

NOTE: This circuit contains a custom block which will be provided in XYMASK form.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: C6M, TCLK, MCTSN, D7, D6, D5, D4, D3, D2, D1, D0, W2, W3, R2N, R3N, R5N, R10D, R10LN, R14N, IRDN, TINV, TRES, ENT, TEL3N, TEL2N, TEL1N, TEL0N, TCRCB, RCLK, SDI, SHIFTIN, RINV, RFL3, RFL2, RFL1, RFL0, RRES, RINTN, TXIDLE, TINIT;

OUTPUTS: DOUT, RTSN, WWQS4, WWQS3, WWQS2, WWQS1, WWQS0, TDONE, TE, UNDABT, TCYCLE, TKBYTE, FRMEND, FF7, FF6, FF5, FF4, FF3, FF2, FF1, FF0, RF, RQS4, RQS3, RQS2, RQS1, RQS0, IDLE, NOEOFN, OVERRUN, REOF;

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Functional Descriptions

Inputs:

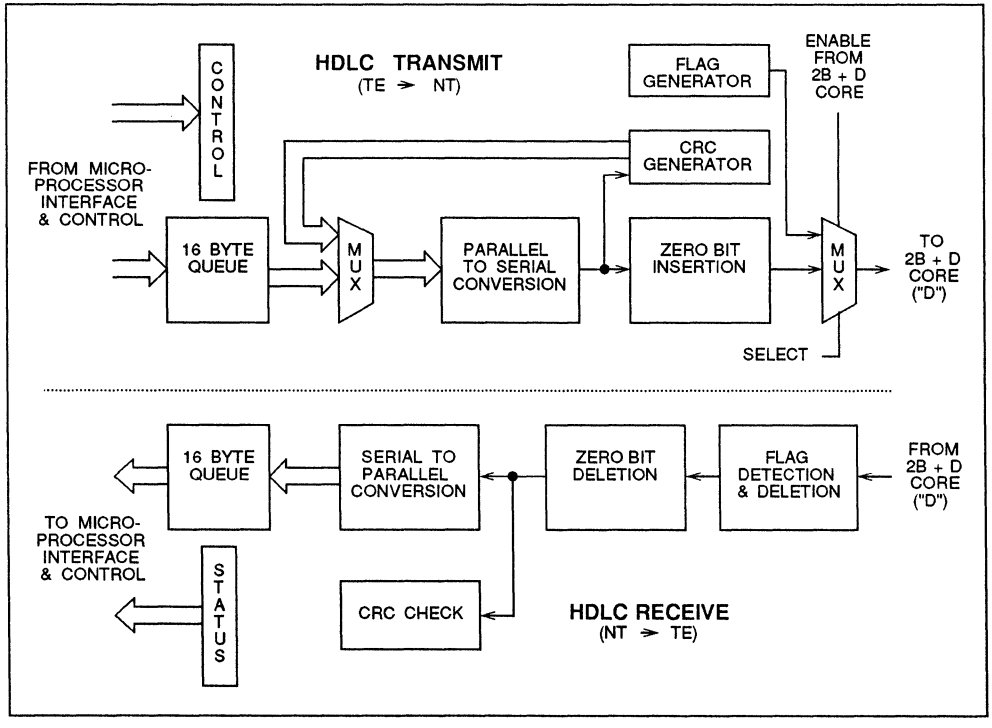
C6M	6.144 Mhz System Clock. C6M can be any frequency provided it is greater than ten times TCLK, RCLK.
TCLK	Transmitter Clock. XMIT input and output data are latched on falling edge of TCLK.
MCTSN	Multiplexed Clear to Send signal into transmitter. Active low signal.
D[7:0]	Input Data Byte to XMIT queue from the microprocessor interface. D7 is the Most Significant Bit.
W2	Control signal, which when R2N is asserted, enables and End of Frame byte or a soft abort to be written in the XMIT queue.
W3	Control signal which allows D[7:0] to be written in the 16 byte XMIT queue.
R2N	See W2 (active low signal).
R3N	Control signal which enables reading a RCV queue data byte when IRDN is asserted (active low signal).
R5N	Control signal which enables reading the RCV queue status when IRDN is asserted (active low signal).
R10D	Control signal which enables the XMIT and RCV read interrupts and which also clears them.
R10LN	Control signal which prevents performing a read interrupt in the middle of another read interrupt in either the XMIT or RCV sections. Active low signal.
R14N	Control signal which reads and clears the XMIT queue status when IRDN is asserted (active low signal).
IRDN	See R3N, R5N and R14N (active low signal).
TINV	Inverts XMIT Data Out (DOUT) when enabled.
TRES	Transmitter Reset signal.
ENT	Transmitter Enable signal.
TEL[3:0]N	Used to set the XMIT Queue Empty Interrupt signal (TE) when queue reaches programmed level of emptiness (active low). Binary encoding is utilized.
TCRCB	This input can corrupt the CRC for testing purposes.
RCLK	Input and output data to RCV block are latched on rising edge of RCLK.
SDI	Stuffed Serial Data into the RCV block. It includes flags and CRC.
SHIFTIN	Signal which qualifies the serial data stream in the RCVR. SDI is sampled only when SHIFTIN is high.
RINV	Controls the Inversion of the RCV Input Data.
RFL[3:0]	Inputs which program the Receive Fill Interrupt Trigger level.
RRES	Receive Reset
RINTN	Active low RCV Reset.
TXIDLE	This input is used to determine the interframe time fill. If set to "0", ITF is flags (01111110), and if set to "1" ITF is idle (ie "1"'s).
TINIT	Transmitter Reset Signal

Functional Descriptions (continued)

Outputs:

DOUT	Stuffed XMIT Serial Data which includes opening/closing flags and 16 bit CRC.
RTSN	Request to Send from the transmitter (active low signal).
WWQS[4:0]	Number of Empty Bytes Available in XMIT queue encoded in binary.
TDONE	Transmitter Done Interrupt signal.
TE	Transmit Empty Interrupt signal.
UNDABT	XMIT Underrun Abort signal.
TCYCLE	Transmit Data Cycle in the XMIT section.
TKBYTE	XMIT Take Byte, a pulse showing when D[7:0] is being sampled.
FRMEND	A pulse showing when the last "0" of a closing flag is in DOUT.
FF[7:0]	Destuffed RCV Queue Data Byte which includes end of frame information.
RF	RCV Fill Interrupt Trigger level.
RQS[4:0]	Number of Bytes to First EOF in RCV queue. If no EOF is in queue, then number of bytes in queue is given. Binary encoding is utilized.
IDLE	RCV Idle signal. Active when fifteen or more "1"'s occur after a closing flag is detected.
NOEOFN	No End of Frame in the receiver (active low signal).
OVERRUN	Active when an Overrun condition occurs in the RCV queue.
REOF	RCV End of Frame Interrupt signal.

BLOCK DIAGRAM



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
C6M	RQS[0:4]↑	0.95	1.96	0.62	0.47
C6M	RQS[0:4]↓	0.81	3.70	0.48	0.65
C6M	RTSN↑	8.00	3.83	3.86	0.73
C6M	RTSN↓	6.95	5.80	4.33	1.28
C6M	UNDABT↑	7.81	9.50	4.29	1.80
C6M	UNDABT↓	7.14	2.23	4.14	0.55
C6M	WWQS[0:4]↑	0.10	1.96	0.14	0.47
C6M	WWQS[0:4]↓	0.10	3.70	0.14	0.65
TCLK	DOUT↑	28.38	6.60	12.10	1.20
TCLK	DOUT↓	28.90	2.50	12.48	0.52
TCLK	FRMEND↑	21.86	6.64	10.10	1.20
TCLK	FRMEND↓	23.33	2.67	10.81	0.55
TCLK	RTSN↑	11.33	3.83	6.10	0.73
TCLK	RTSN↓	10.52	5.80	6.71	1.28
TCLK	TCYCLE↑	0.71	3.66	0.57	0.65
TCLK	TCYCLE↓	6.57	2.01	0.57	0.44
TCLK	TKBYTE↑	25.05	1.87	11.52	0.34
TCLK	TKBYTE↓	25.71	1.47	11.90	0.31
TCLK	UNDABT↑	9.90	9.50	6.10	1.80
TCLK	UNDABT↓	8.00	2.23	6.19	0.55
RCLK	IDLE↑	22.81	3.70	10.48	0.68
RCLK	IDLE↓	13.62	2.54	6.67	0.55

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum D[2:3] Setup before C6M	4.95	2.52
Minimum W[2:3] Setup before C6M	5.38	2.95
Minimum R[3,5,14]N Setup before C6M	135.95	50.67
Minimum IRDN Setup before C6M	135.95	50.67
Minimum TRES Setup before C6M	5.29	2.81
Minimum TEL[0:3]N Setup before C6M	15.76	7.48
Minimum RFL[0:3]N Setup before C6M	17.38	8.00

4-Bit Look Ahead Carry Generator — LACG4

98 grids, 152 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The LACG4 is functionally equivalent to the 74182 Look-Ahead Carry Generator within the standard 74XX Series logic families of devices. LACG4 provides carry, generate carry function and propagate carry function with fast carry look ahead.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: X0, X1, X2, X3, Y0, Y1, Y2, Y3, CN0;

OUTPUTS: XA, YA, CNPX, CNPY, CNPZ;

Functional Descriptions

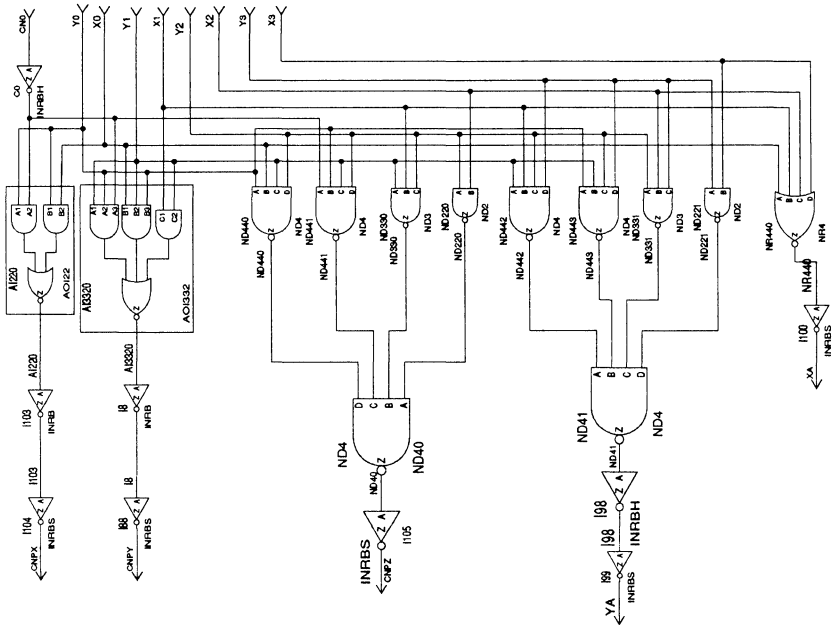
Inputs:

X[0:3]	Carry propagate inputs, active low
Y[0:3]	Carry generate inputs, active low
CN0	Carry input

Outputs:

XA	Carry propagate output, active low
YA	Carry generate output, active low
CNP[X,Y,Z]	Carry outputs

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
CN0	CNP[X,Y,Z]↑	5.62	0.98	2.43	0.18
CN0	CNP[X,Y,Z]↓	4.90	0.94	2.10	0.18
X[0:3],Y[0:3]	CNP[X,Y,Z]↑	5.14	0.98	2.24	0.18
X[0:3],Y[0:3]	CNP[X,Y,Z]↓	3.42	0.94	1.67	0.18
X[0:3]	XA↑	0.67	0.98	0.48	0.18
X[0:3]	XA↓	4.81	0.94	2.43	0.18
X[1:3],Y[0:3]	YA↑	3.90	0.98	1.81	0.18
X[1:3],Y[0:3]	YA↓	4.19	0.94	2.00	0.18

12

16 X 16 Multiplier

MUL16X16

5443 grids, 8100 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

The MUL16X16 is a high-speed, 16 X 16 multiplier in 2's complement arithmetic implemented as a standard cell netlist. It has been designed with static combinatorial logic without pipelining. True high-performance and ease of use is achieved by eliminating complicated timing requirements and latency associated with pipe-lined structures. The design is suitable for a wide range of computation-intensive applications, for example digital signal processing.

The partial products to be summed are generated from the M-inputs by the Booth Selector, which is controlled by the outputs of the Booth Encoder that operates on the N-inputs. The partial products are summed by carry-save adders arranged in a Wallace Tree structure. The final carry-propagate is performed by an optimally partitioned carry-select adder stage.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: M0, M1, M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, M12, M13, M14, M15, N0, N1, N2, N3, N4, N5, N6, N7, N8, N9, N10, N11, N12, N13, N14, N15;

OUTPUTS: P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, P17, P18, P19, P20, P21, P22, P23, P24, P25, P26, P27, P28, P29, P30, P31;

Functional Descriptions

Inputs:

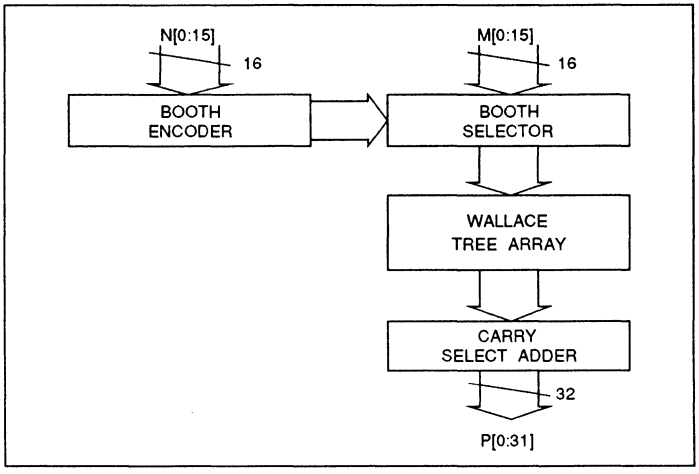
M[0:15], N[0:15]	Inputs

Outputs:

P[0:31]	Outputs

12

BLOCK DIAGRAM



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
M[0:15],N[0:15]	P[0:31]	57.0	3.70	27.0	0.68

12

3-Bit Majority Vote

MV3

13 grids, 18 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

MV3 is a 3-bit majority vote circuit. The output is high when a majority is present at the inputs.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: V1, V2, V3;

OUTPUTS: MVI;

Functional Descriptions

Inputs:

V[1:3]	Data inputs

Outputs:

MVI	Majority indicator

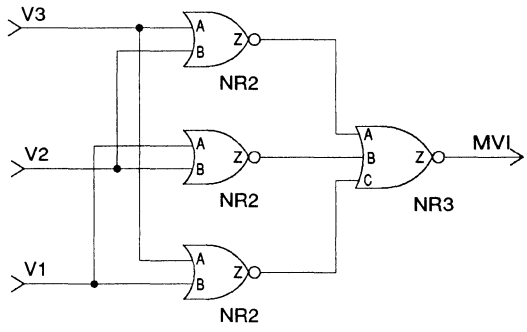
TRUTH TABLE

V1	V2	V3	MVI
0	0	X	0
0	X	0	0
X	0	0	0
1	1	X	1
1	X	1	1
X	1	1	1

X = Don't Care

12

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
V[1:3]	MVI↑	0.86	9.27	0.43	1.69
V[1:3]	MVI↓	1.90	2.67	0.71	0.57

12

5-Bit Majority Vote

MV5

41 grids, 62 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

MV5 is a 5-bit majority vote circuit. The output is high when a majority is present at the inputs.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: V1, V2, V3, V4, V5;

OUTPUTS: MVI;

Functional Descriptions

Inputs:

V[1:5]	Data inputs

Outputs:

MVI	Majority indicator

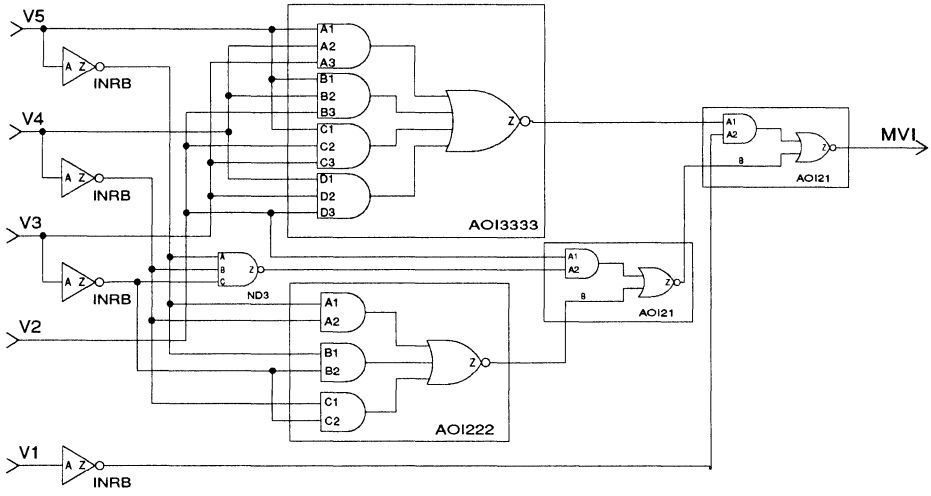
TRUTH TABLE

V1	V2	V3	V4	V5	MVI
0	0	0	X	X	0
0	0	X	X	0	0
0	X	X	0	0	0
X	X	0	0	0	0
X	0	0	0	X	0
1	1	1	X	X	1
1	1	X	X	1	1
1	X	X	1	1	1
X	X	1	1	1	1
X	1	1	1	X	1

X = Don't Care

12

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
V1	MVI↑	0.67	6.73	0.29	1.25
V1	MVI↓	1.14	4.19	0.43	0.91
V2	MVI↑	2.19	6.73	1.19	1.25
V2	MVI↓	5.10	4.19	2.19	0.91
V[3:5]	MVI↑	6.05	6.73	2.33	1.25
V[3:5]	MVI↓	6.24	4.19	2.29	0.91

12

3-Bit Programmable Counter/Timer PCLE3

96 grids, 140 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

PCLE3 is a programmable counter/timer with positive load, enable and synchronous clear. The counter has linear feedback and counts in a pseudo-random sequence. The timer generates a positive-going pulse when the last state is reached. The enable input should be kept high for counting or loading a starting value. The counter can be set to any non-zero starting value by applying a 3-bit binary code to inputs D[0:2] and keeping the load input high. The value is loaded after the next clock cycle. The counter will count from the loaded value until it reaches a value of (001). If a new value is not loaded and the counter is not disabled, it will recycle and generate a positive-going pulse after seven (7) counts.

- Programmable
- Positive load and count enable
- Synchronous clear

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: D0, D1, D2, LD, EN, CK, CD;

OUTPUTS: Z;

Functional Descriptions

Inputs:

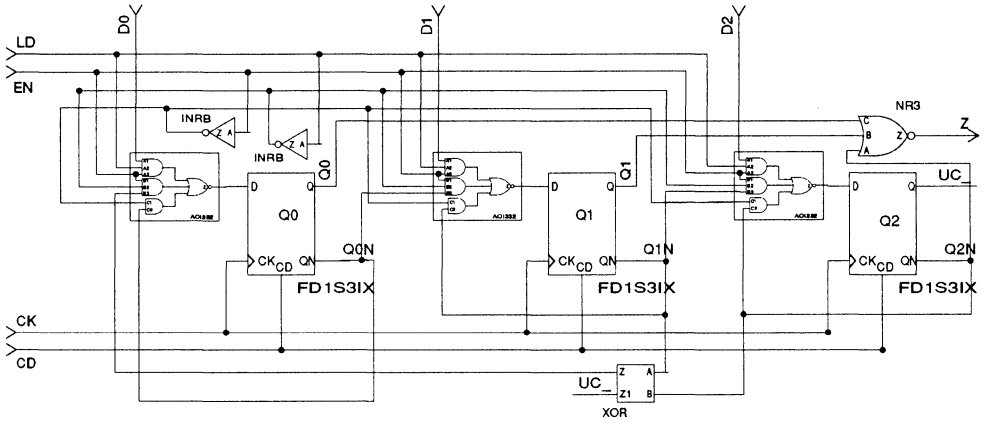
D[0:2]	Parallel data inputs
LD	Load input, active high
EN	Count enable, active high
CK	Clock input
CD	Clear input, active high

Outputs:

Z	Output

12

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
CK↑	Z↑	4.43	9.27	2.43	1.69
CK↑	Z↓	4.05	2.67	2.57	0.57

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.33
Minimum D[0:2] Setup before CK↑	4.10	2.38
Minimum EN Setup before CK↑	5.67	2.81
Minimum LD Setup before CK↑	6.10	2.95

12

4-Bit Programmable Counter/Timer PCLE4

124 grids, 182 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

PCLE4 is a programmable counter/timer with positive load, enable and synchronous clear. The counter has linear feedback and counts in a pseudo-random sequence. The timer generates a positive-going pulse when the last state is reached. The enable input should be kept high for counting or loading a starting value. The counter can be set to any non-zero starting value by applying a 4-bit binary code to inputs D[0:3] and keeping the load input high. The value is loaded after the next clock cycle. The counter will count from the loaded value until it reaches a value of (0001). If a new value is not loaded and the counter is not disabled, it will recycle and generate a positive-going pulse after fifteen (15) counts.

- Programmable
- Positive load and count enable
- Synchronous clear

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: D0, D1, D2, D3, LD, EN, CK, CD;

OUTPUTS: Z;

Functional Descriptions

Inputs:

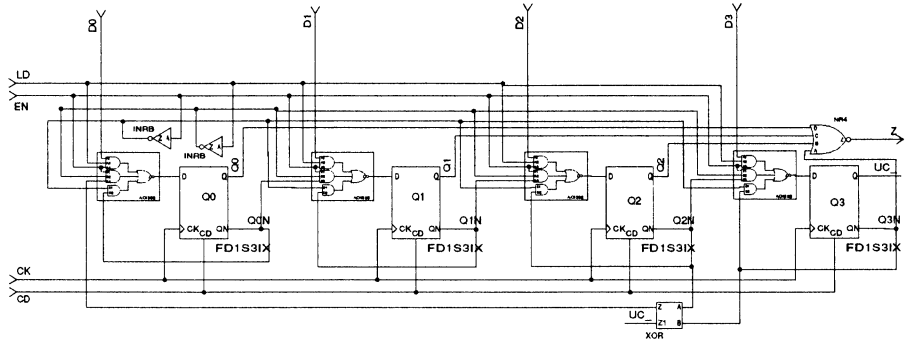
D[0:3]	Parallel data inputs
LD	Load input, active high
EN	Count enable, active high
CK	Clock input
CD	Clear input, active high

Outputs:

Z	Output

12

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
CK↑	Z↑	4.52	11.72	2.48	2.11
CK↑	Z↓	4.14	2.76	2.67	0.57

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.33
Minimum D[0:3] Setup before CK↑	4.14	2.38
Minimum EN Setup before CK↑	6.48	3.05
Minimum LD Setup before CK↑	6.76	3.24

12

5-Bit Programmable Counter/Timer PCLE5

156 grids, 228 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

PCLE5 is a programmable counter/timer with positive load, enable and synchronous clear. The counter has linear feedback and counts in a pseudo-random sequence. The timer generates a positive-going pulse when the last state is reached. The enable input should be kept high for counting or loading a starting value. The counter can be set to any non-zero starting value by applying a 5-bit binary code to inputs D[0:4] and keeping the load input high. The value is loaded after the next clock cycle. The counter will count from the loaded value until it reaches a value of (00001). If a new value is not loaded and the counter is not disabled, it will recycle and generate a positive-going pulse after thirty-one (31) counts.

- Programmable
- Positive load and count enable
- Synchronous clear

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: D0, D1, D2, D3, D4, LD, EN, CK, CD;

OUTPUTS: Z;

Functional Descriptions

Inputs:

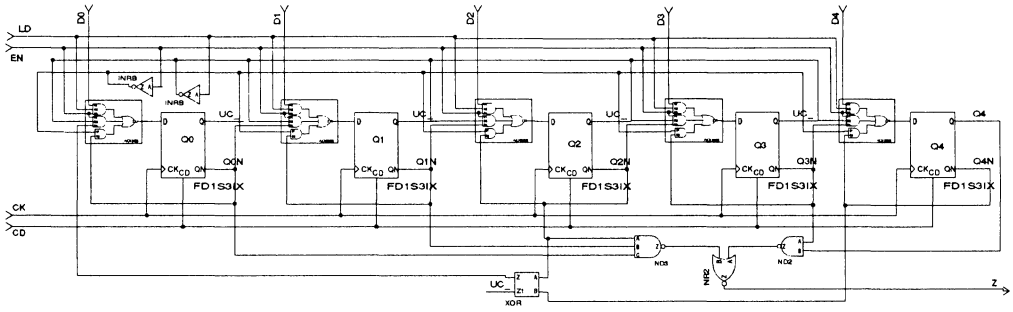
D[0:4]	Parallel data inputs
LD	Load input, active high
EN	Count enable, active high
CK	Clock input
CD	Clear input, active high

Outputs:

Z	Output

12

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
CK↑	Z↑	6.67	6.64	3.81	1.20
CK↑	Z↓	4.43	2.67	2.62	0.55

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.33
Minimum D[0:4] Setup before CK↑	4.05	2.33
Minimum EN Setup before CK↑	7.24	3.29
Minimum LD Setup before CK↑	7.57	3.48

12

6-Bit Programmable Counter/Timer PCLE6

184 grids, 270 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

PCLE6 is a programmable counter/timer with positive load, enable and synchronous clear. The counter has linear feedback and counts in a pseudo-random sequence. The timer generates a positive-going pulse when the last state is reached. The enable input should be kept high for counting or loading a starting value. The counter can be set to any non-zero starting value by applying a 6-bit binary code to inputs D[0:5] and keeping the load input high. The value is loaded after the next clock cycle. The counter will count from the loaded value until it reaches a value of (000001). If a new value is not loaded and the counter is not disabled, it will recycle and generate a positive-going pulse after sixty-three (63) counts.

- Programmable
- Positive load and count enable
- Synchronous clear

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: D0, D1, D2, D3, D4, D5, LD, EN, CK, CD;

OUTPUTS: Z;

Functional Descriptions

Inputs:

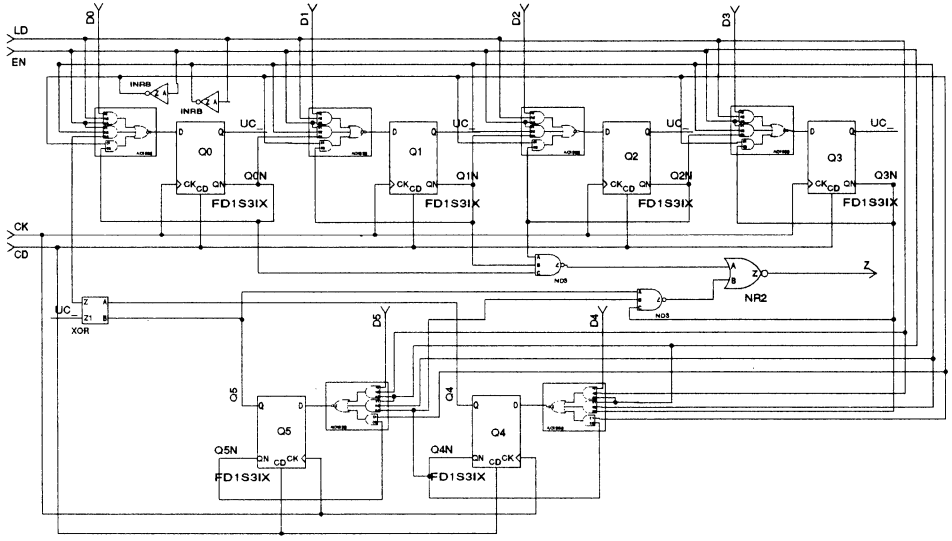
D[0:5]	Parallel data inputs
LD	Load input, active high
EN	Count enable, active high
CK	Clock input
CD	Clear input, active high

Outputs:

Z	Output

12

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
CK↑	Z↑	5.57	6.64	3.86	1.20
CK↑	Z↓	3.86	2.67	2.76	0.55

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.33
Minimum D[0:5] Setup before CK↑	4.10	2.33
Minimum EN Setup before CK↑	7.95	3.48
Minimum LD Setup before CK↑	8.19	3.71

12

8-Bit Programmable Counter/Timer PCLE8

240 grids, 354 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

PCLE8 is a programmable counter/timer with positive load, enable and synchronous clear. The counter has linear feedback and counts in a pseudo-random sequence. The timer generates a positive-going pulse when the last state is reached. The enable input should be kept high for counting or loading a starting value. The counter can be set to any non-zero starting value by applying a 8-bit binary code to inputs D[0:7] and keeping the load input high. The value is loaded after the next clock cycle. The counter will count from the loaded value until it reaches a value of (00000001). If a new value is not loaded and the counter is not disabled, it will recycle and generate a positive-going pulse after two-hundred-seventeen (217) counts.

- Programmable
- Positive load and count enable
- Synchronous clear

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: D0, D1, D2, D3, D4, D5, D6, D7, LD, EN, CK, CD;

OUTPUTS: Z;

Functional Descriptions

Inputs:

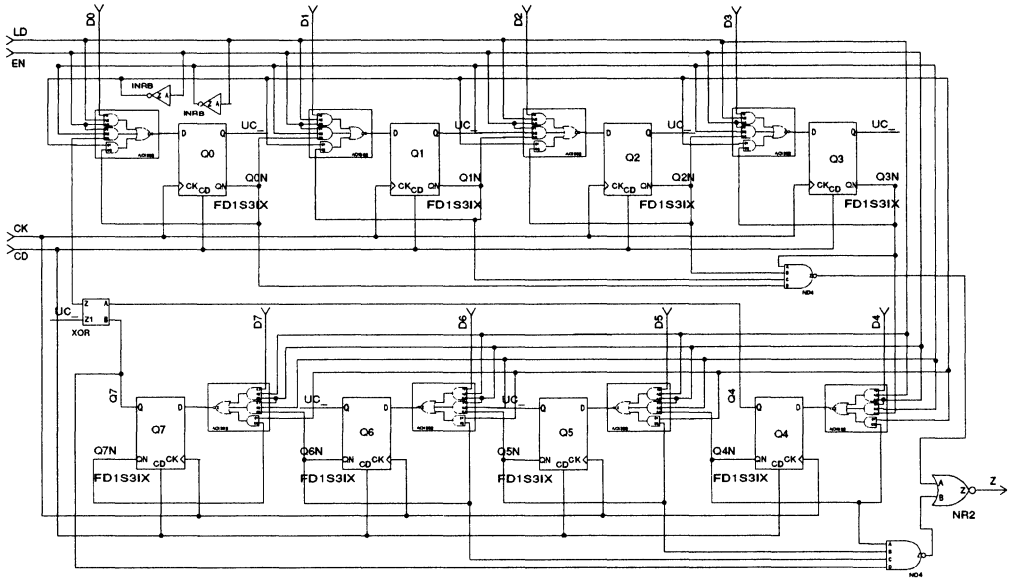
D[0:7]	Parallel data inputs
LD	Load input, active high
EN	Count enable, active high
CK	Clock input
CD	Clear input, active high

Outputs:

Z	Output

12

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From Input	To Output	Area		Performance	
		Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
CK↑	Z↑	5.95	6.64	4.00	1.20
CK↑	Z↓	3.90	2.67	2.76	0.55

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.33
Minimum D[0:7] Setup before CK↑	4.19	2.33
Minimum EN Setup before CK↑	9.29	4.00
Minimum LD Setup before CK↑	9.52	4.14

12

3-Bit Programmable Counter/Timer PCLER3

99 grids, 144 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

PCLER3 is a programmable counter/timer with positive load, enable and synchronous clear. The counter has linear feedback and counts in a pseudo-random sequence. The timer generates a positive-going pulse when the last state is reached. The enable input should be kept high for counting or loading a starting value. The counter can be set to any non-zero starting value by applying a 3-bit binary code to inputs D[0:2] and keeping the load input high. The value is loaded after the next clock cycle. The counter will count from the loaded value until it reaches a value of (001). If a new value is not loaded and the counter is not disabled, it will reload the value at it's D[0:2] inputs. The maximum count is 7.

- Programmable
- Positive load and count enable
- Synchronous clear
- Recycle from last loaded value

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: D0, D1, D2, LD, EN, CK, CD;

OUTPUTS: Z;

Functional Descriptions

Inputs:

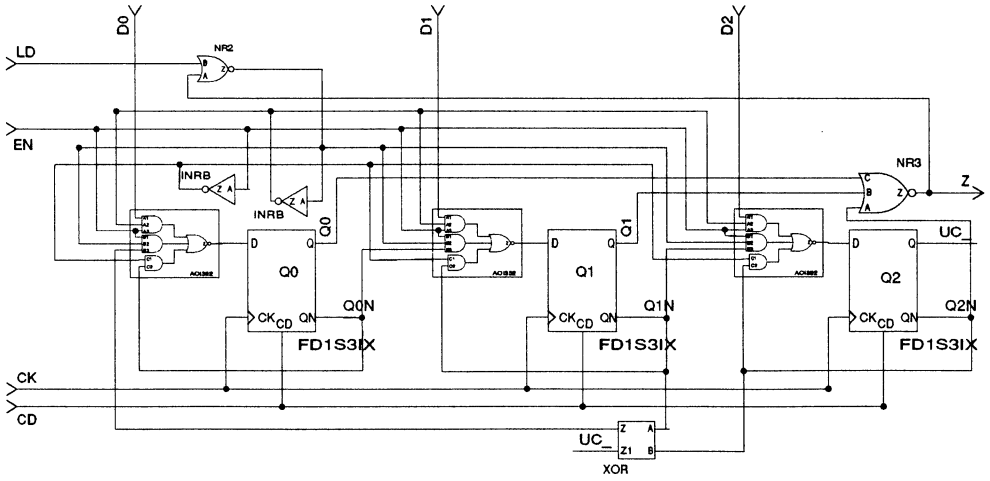
D[0:2]	Parallel data inputs
LD	Load input, active high
EN	Count enable, active high
CK	Clock input
CD	Clear input, active high

Outputs:

Z	Output

12

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From Input	To Output	Area		Performance	
		Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
CK↑	Z↑	5.86	9.27	2.81	1.69
CK↑	Z↓	5.14	2.67	3.33	0.57

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.33
Minimum D[0:2] Setup before CK↑	4.10	2.38
Minimum EN Setup before CK↑	5.62	2.81
Minimum LD Setup before CK↑	12.81	5.19

12

4-Bit Programmable Counter/Timer PCLER4

127 grids, 186 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

PCLER4 is a programmable counter/timer with positive load, enable and synchronous clear. The counter has linear feedback and counts in a pseudo-random sequence. The timer generates a positive-going pulse when the last state is reached. The enable input should be kept high for counting or loading a starting value. The counter can be set to any non-zero starting value by applying a 4-bit binary code to inputs D[0:3] and keeping the load input high. The value is loaded after the next clock cycle. The counter will count from the loaded value until it reaches a value of (0001). If a new value is not loaded and the counter is not disabled, it will reload the value at it's D[0:3] inputs. The maximum count is 15.

- Programmable
- Positive load and count enable
- Synchronous clear
- Recycle from last loaded value

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: D0, D1, D2, D3, LD, EN, CK, CD;

OUTPUTS: Z;

Functional Descriptions

Inputs:

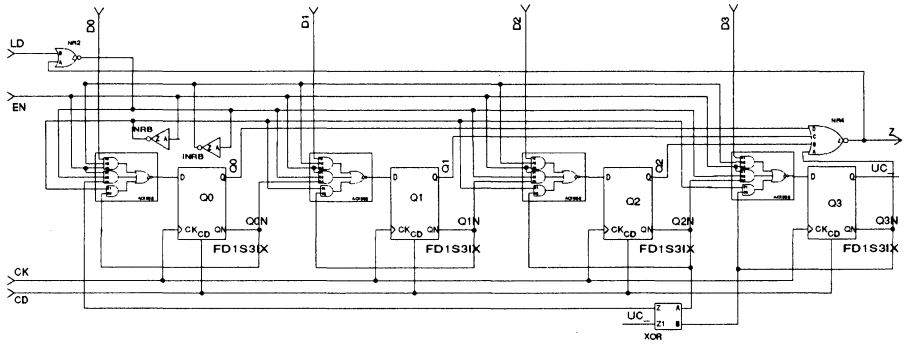
D[0:3]	Parallel data inputs
LD	Load input, active high
EN	Count enable, active high
CK	Clock input
CD	Clear input, active high

Outputs:

Z	Output

12

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
CK↑	Z↑	6.29	11.72	3.05	2.11
CK↑	Z↓	5.29	2.76	3.52	0.57

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.33
Minimum D[0:3] Setup before CK↑	4.14	2.38
Minimum EN Setup before CK↑	6.33	3.05
Minimum LD Setup before CK↑	14.90	6.00

12

5-Bit Programmable Counter/Timer PCLER5

159 grids, 232 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

PCLER5 is a programmable counter/timer with positive load, enable and synchronous clear. The counter has linear feedback and counts in a pseudo-random sequence. The timer generates a positive-going pulse when the last state is reached. The enable input should be kept high for counting or loading a starting value. The counter can be set to any non-zero starting value by applying a 5-bit binary code to inputs D[0:4] and keeping the load input high. The value is loaded after the next clock cycle. The counter will count from the loaded value until it reaches a value of (00001). If a new value is not loaded and the counter is not disabled, it will reload the value at it's D[0:4] inputs. The maximum count is 31.

- Programmable
- Positive load and count enable
- Synchronous clear
- Recycle from last loaded value

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: D0, D1, D2, D3, D4, LD, EN, CK, CD;

OUTPUTS: Z;

Functional Descriptions

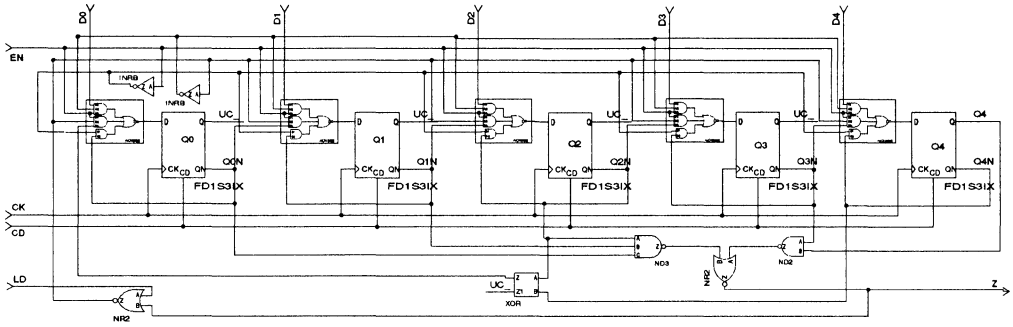
Inputs:

D[0:4]	Parallel data inputs
LD	Load input, active high
EN	Count enable, active high
CK	Clock input
CD	Clear input, active high

Outputs:

Z	Output

DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
CK↑	Z↑	7.76	6.64	4.19	1.20
CK↑	Z↓	5.10	2.67	2.86	0.55

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.33
Minimum D[0:4] Setup before CK↑	4.05	2.33
Minimum EN Setup before CK↑	7.29	3.29
Minimum LD Setup before CK↑	17.05	6.67

12

6-Bit Programmable Counter/Timer PCLER6

187 grids, 274 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

PCLER6 is a programmable counter/timer with positive load, enable and synchronous clear. The counter has linear feedback and counts in a pseudo-random sequence. The timer generates a positive-going pulse when the last state is reached. The enable input should be kept high for counting or loading a starting value. The counter can be set to any non-zero starting value by applying a 6-bit binary code to inputs D[0:5] and keeping the load input high. The value is loaded after the next clock cycle. The counter will count from the loaded value until it reaches a value of (000001). If a new value is not loaded and the counter is not disabled, it will reload the value at it's D[0:5] inputs. The maximum count is 63.

- Programmable
- Positive load and count enable
- Synchronous clear
- Recycle from last loaded value

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: D0, D1, D2, D3, D4, D5, LD, EN, CK, CD;

OUTPUTS: Z;

Functional Descriptions

Inputs:

D[0:5]	Parallel data inputs
LD	Load input, active high
EN	Count enable, active high
CK	Clock input
CD	Clear input, active high

Outputs:

Z	Output

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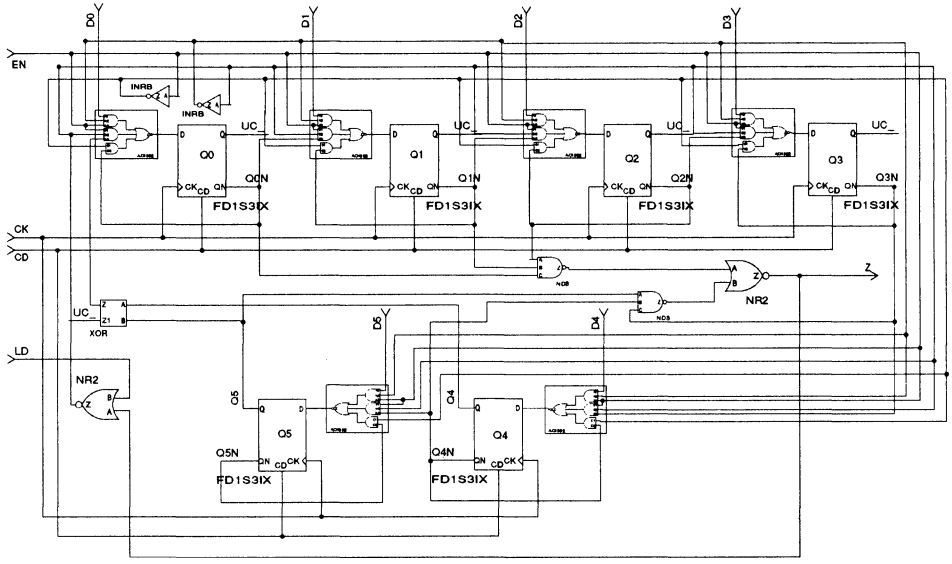
DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From Input	To Output	Area		Performance	
		Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
CK↑	Z↑	6.67	6.64	4.24	1.20
CK↑	Z↓	4.52	2.67	3.00	0.55

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.33
Minimum D[0:5] Setup before CK↑	4.10	2.33
Minimum EN Setup before CK↑	7.90	3.48
Minimum LD Setup before CK↑	19.05	7.33

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8-Bit Programmable Counter/Timer PCLER8

243 grids, 358 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

PCLER8 is a programmable counter/timer with positive load, enable and synchronous clear. The counter has linear feedback and counts in a pseudo-random sequence. The timer generates a positive-going pulse when the last state is reached. The enable input should be kept high for counting or loading a starting value. The counter can be set to any non-zero starting value by applying a 8-bit binary code to inputs D[0:7] and keeping the load input high. The value is loaded after the next clock cycle. The counter will count from the loaded value until it reaches a value of (00000001). If a new value is not loaded and the counter is not disabled, it will reload the value at it's D[0:7] inputs. The maximum count is 217.

- Programmable
- Positive load and count enable
- Synchronous clear
- Recycle from last loaded value

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: D0, D1, D2, D3, D4, D5, D6, D7, LD, EN, CK, CD;

OUTPUTS: Z;

Functional Descriptions

Inputs:

D[0:7]	Parallel data inputs
LD	Load input, active high
EN	Count enable, active high
CK	Clock input
CD	Clear input, active high

Outputs:

Z	Output

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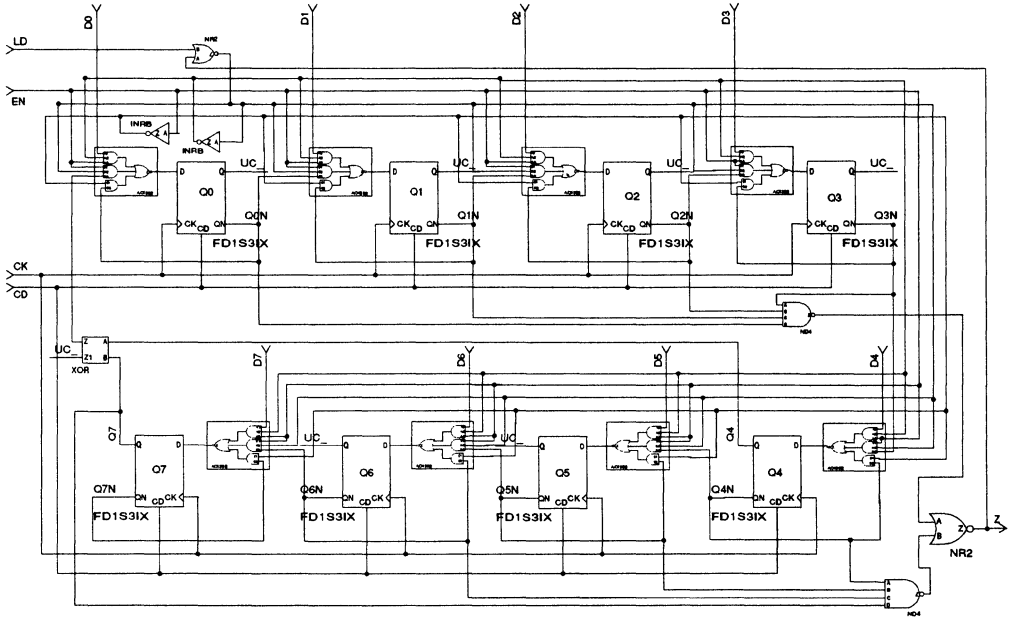
DETAILED SCHEMATIC



CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From Input	To Output	Area		Performance	
		Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
CK↑	Z↑	7.10	6.64	4.38	1.20
CK↑	Z↓	4.57	2.67	3.00	0.55

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.33
Minimum D[0:7] Setup before CK↑	4.19	2.33
Minimum EN Setup before CK↑	9.24	4.00
Minimum LD Setup before CK↑	22.95	8.76

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Phase Locked Loop — PLLPAIR

5398 grids, 7596 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

PLLPAIR consists of two Phase Locked Loops, NRDPLL and NTDPLL, which run synchronously on a 9.216 Mhz clock. They phase lock to asynchronous data signals ranging from 700 Hz to 70 Khz. Output jitter is less than 5% of the data's period assuming input jitter is less than 18% of the period. The maximum search time is approximately 300 ms. They are provided as standard cell netlists.

Designed to modulate and demodulate PWM data, either circuit locks to the rising edge of each period. NRDPLL produces a 50-50 duty cycle reproduction (RFO) of the input frequency and data strobed (RDO) from the midpoint of the estimated period. NTDPLL produces two pulses (TPO1, TPO2) representing the first 33% and the second 33% of the input signal. These pulses can be combined with data to create the modulated PWM signal.

Because of the highly sequential nature of this circuit, significant logic has been included to permit test vector design for both high functional and high fault coverage.

- Wide data rate frequency locking range: 700 Hz - 70 Khz with 9 Mhz CLK
- Fast-locking algorithm locks in less than 300 ms., aids testing.
- Implemented as a standard cell netlist.
- Standard cell models are easily modified.
  - Change frequency locking range.
  - Change jitter characteristics.
  - Change frequency multiplication.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: RFI, RTC1, RTC2, RTC3, RTC4, RTC5, RTC6, RTC7, RTC8, RTC9, RTC10, RTC11, RTC12, RTC13, RTC14, RTC15, RTC16, RTC17, RTC18, RTC19, RTC20, RTC21, RTC22, 9MCLK, TFI, TTC1, TTC2, TTC3, TTC4, TTC5, TTC6, TTC7, TTC8, TTC9, TTC10, TTC11, TTC12, TTC13, TTC14, TTC15, TTC16, TTC17, TTC18, TTC19, TTC20, TTC21, TTC22;

OUTPUTS: RDO, RFO, RTO1, RTO2, RTO3, RTO4, RTO5, TP01, TTO1, TTO2, TTO3, TTO4, TTO5, TP02;

Functional Descriptions (NRDPLL)

Inputs:

9MCLK	Remote system clock (9MHZ)
RFI	Pulse Width Modulated data from transmission network
RTC[1:22]	IC test control

Outputs:

RDO	Received demodulated data
RFO	Received clock
RTO[1:5]	Test out

Functional Descriptions (NTDPLL)

Inputs:

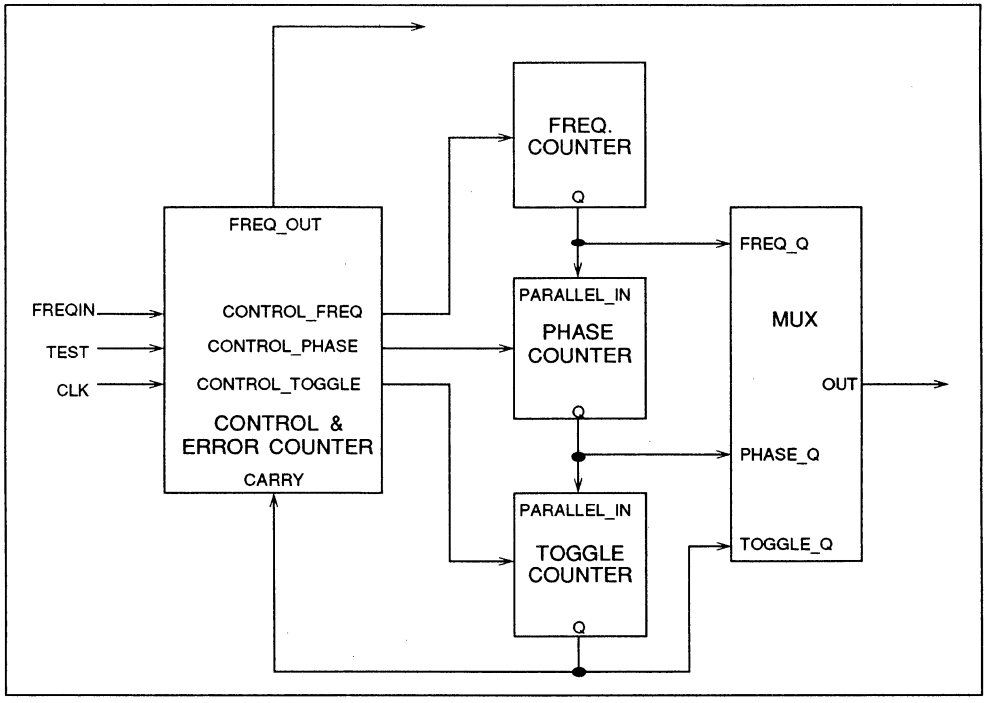
9MCLK	Local system clock (9MHZ)
TFI	Local data clock (700 HZ - 70 KHZ)
TTC[1:22]	IC test control

Outputs:

TP01	Phase 1 to Custom Logic
TP02	Phase 2 to Custom Logic
TTO[1:5]	Test out

BLOCK DIAGRAM

The diagram below shows a simplified block diagram of either PLL circuit. The schematics also reflect this architecture.



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CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
9MCLK	RDO↑	1.05	8.92	0.81	1.67
9MCLK	RDO↓	1.24	6.55	0.86	1.36
9MCLK	RFO↑	4.14	1.96	1.71	0.47
9MCLK	RFO↓	2.86	3.61	1.57	0.65
9MCLK	TP01↑	3.52	1.96	1.57	0.47
9MCLK	TP01↓	2.52	3.61	1.48	0.65
9MCLK	TP02↑	4.14	1.96	1.71	0.47
9MCLK	TP02↓	2.86	3.61	1.57	0.65

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum RFI Setup before 9MCLK	1.95	1.00
Minimum TFI Setup before 9MCLK	0.67	0.67

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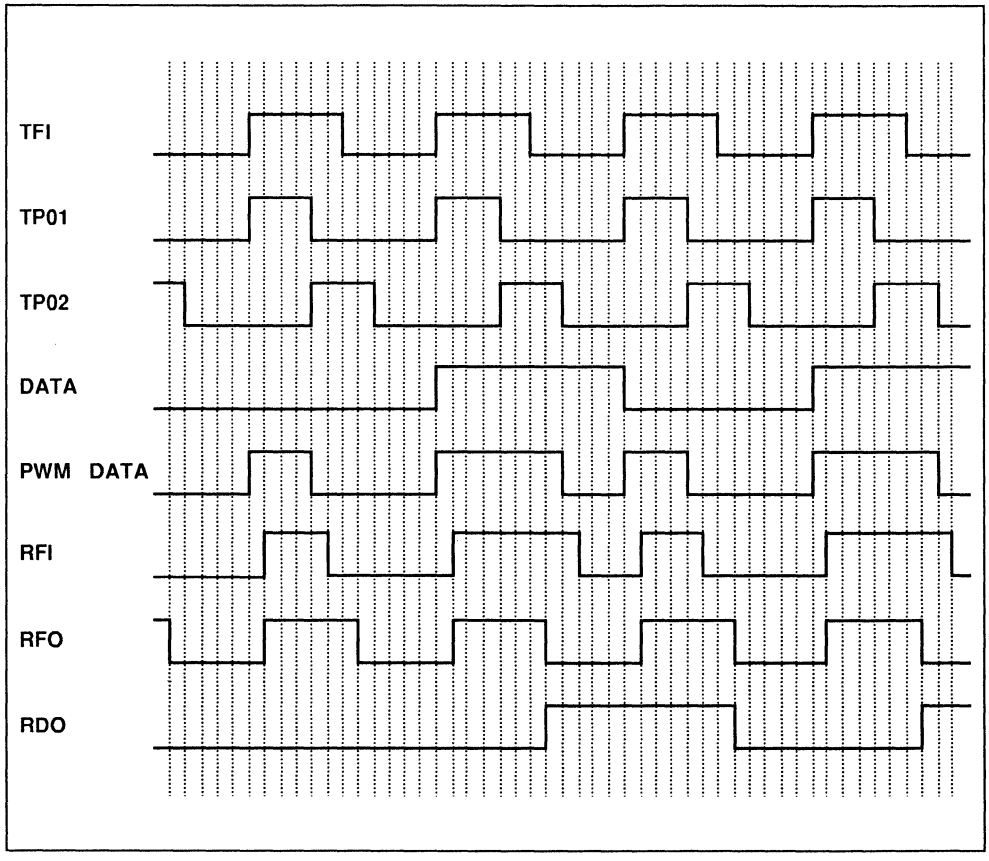
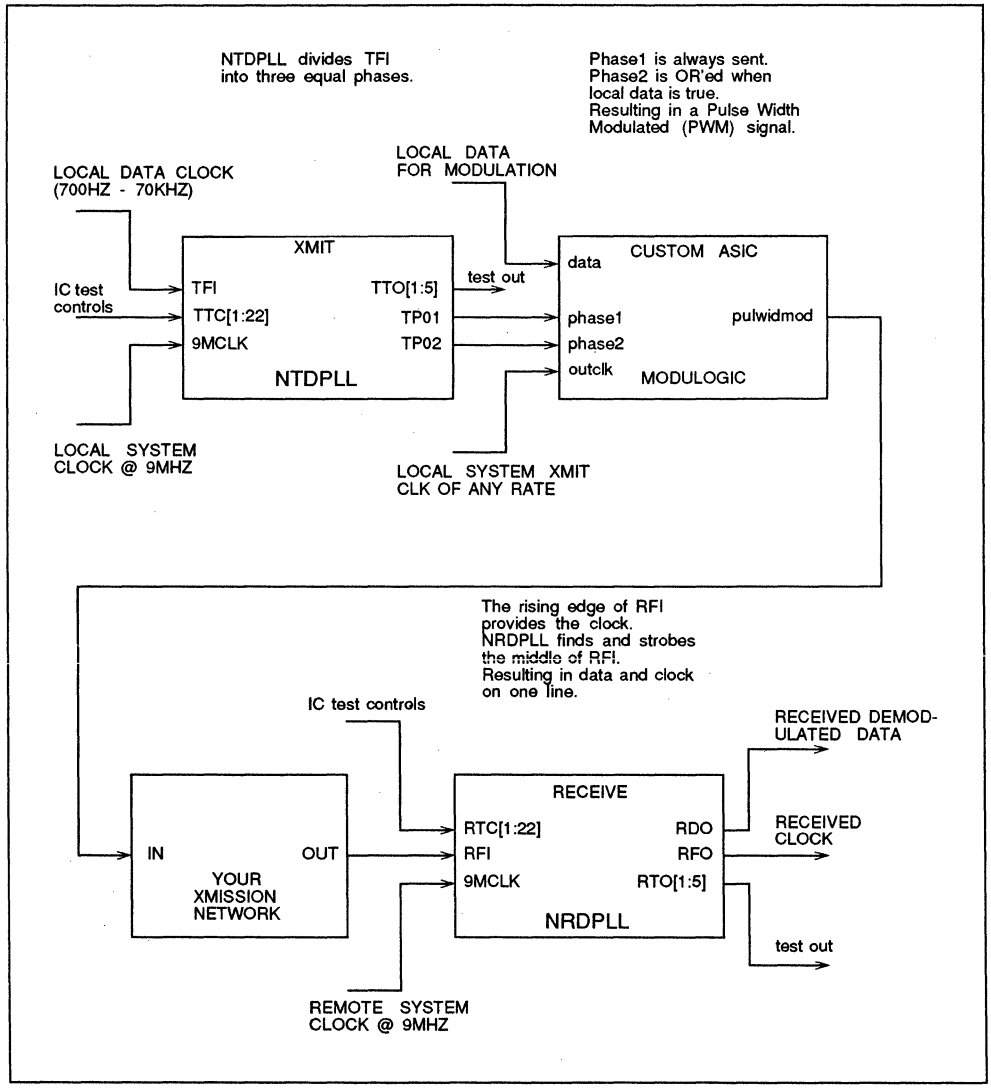
TIMING RELATIONS

The diagram below reiterates the locked on phase behavior of NRDPLL and NTDPLL. As shown NRDPLL estimates the midpoint of RFI and NTDPLL estimates the one third and two thirds points in the TFI period.



APPLICATION NOTES

The diagram below suggests a scheme for transmitting PWM data using the two PLL circuits: NTD-PLL and NRDPLL. As indicated the transmission details are left to the particular design application.



Z80 Counter Timer Circuit

Z80_CTC

5610 grids, 7534 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

Designed to sit on an 8-bit bus, the Z80_CTC is a general purpose, programmable counter timer circuit. Programming is performed by first writing an 8-bit control word and then an 8-bit time constant to each channel. Optionally an interrupt vector can be programmed to be read when time-out occurs and interrupts are enabled. The interrupt protocol is similar to the ZILOG Z80 CTC.

Three exceptions to the ZILOG Z80 CTC function are implemented. First the ZC_TO[0:2] signals pulse high for exactly 1 clock period, rather than 1.5 clocks as on the ZILOG circuit. This change is consistent with a synchronous design philosophy.

Similarly during reads the D[0:7] signals are NOT presented for 1.5 CLK periods as on the ZILOG circuit. Instead the Z80_CTC drives D[0:7] as long as IORQN and RDN are held low.

Finally the Z80 microprocessor RETI (return from interrupt) instruction is not decoded by the Z80_CTC since it's unlikely to be used. This may complicate true "Daisy-Chained" interrupt handling, but can be added if needed.

- Virtually functionally equivalent to the ZILOG Z8430. (Z80 CTC)
- Four independent counter/timer channels.
- Each channel stores an 8-bit control word and an 8-bit time constant.
- Each channel counts or times down to zero, pulses ZC_TO, reloads the constant and continues.
- Times based on 16 or 256 times the CLK period (and time constant).
- Counts on either positive or negative clock edges.
- Channels are cascadable for longer times.
- Latest counts can be read from the D[0:7] bus.
- Fast High Level models for simulation.
- Provided as a netlist of standard cells.
- Easily expanded or modified.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: CLK, M1N, CEN, CS0, CS1, RESETN, IORQN, RDN, CLK_TRG0, CLK_TRG1, CLK_TRG2, CLK_TRG3;

OUTPUTS: ZC_T00, ZC_T01, ZC_T02;

IOPUTS: D0, D1, D2, D3, D4, D5, D6, D7;

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Functional Descriptions

Inputs:

CLK	System clock
M1N	Machine cycle one signal from CPU (active low)
CEN	Chip enable (active low)
CS[0:1]	Channel select
RESETN	Reset (active low)
IORQN	Input / Output request from CPU (active low)
RDN	Read cycle status from the CPU (active low)
CLK_TRG[0:3]	External clock / timer trigger

Outputs:

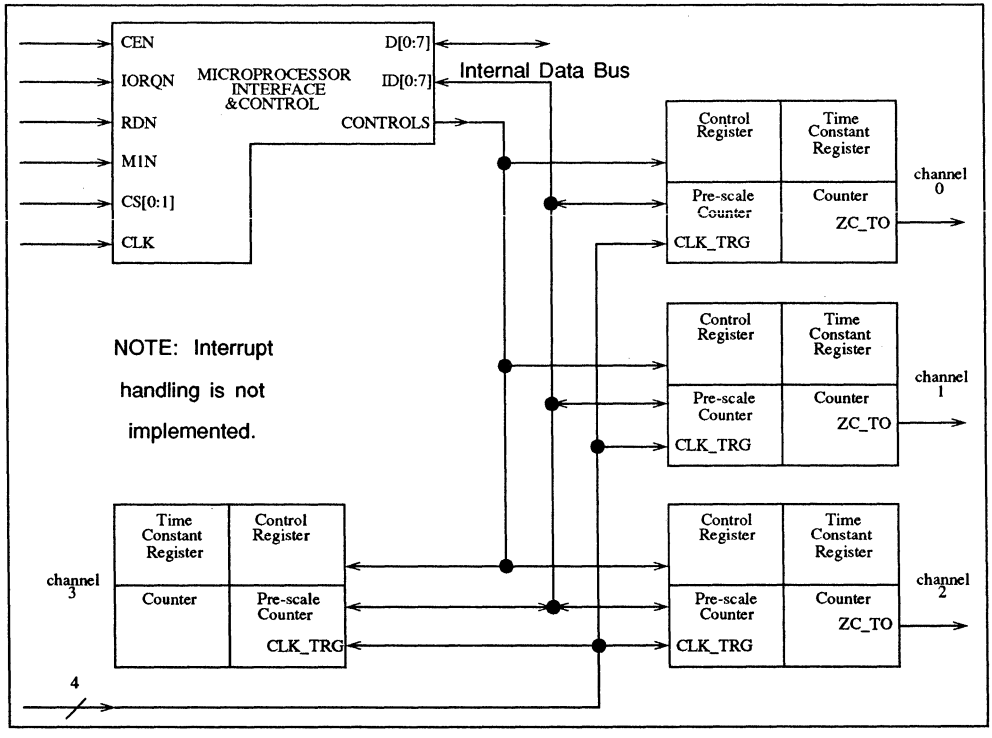
ZC_T0[0:2]	Zero count / timeout

Ioputs:

D[0:7]	Z80 CPU data bus

BLOCK DIAGRAM

The diagram below shows a simplified block diagram of the Z80_CTC. The schematics also reflect this architecture.



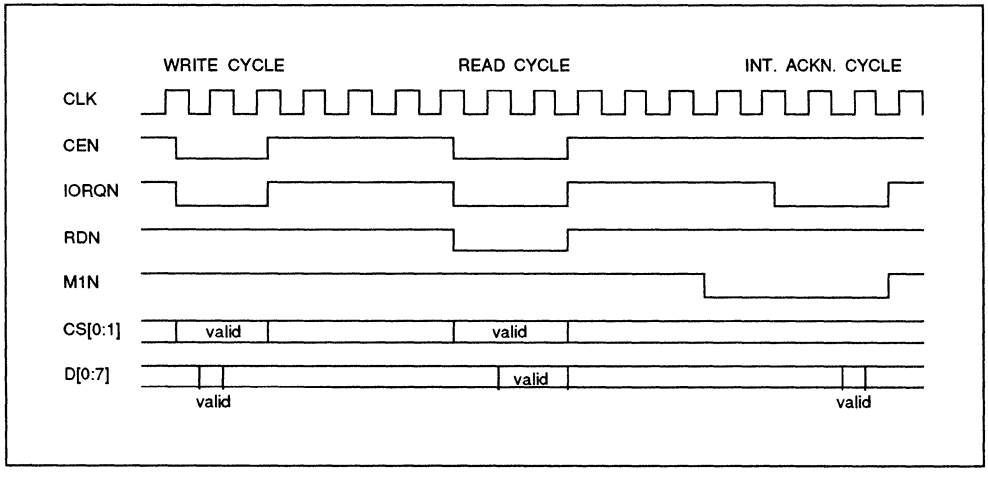
CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
CLK	ZC_T0[0:2]↑	18.38	3.70	9.90	0.68
CLK	ZC_T0[0:2]↓	15.48	2.54	7.24	0.55

TIMING RELATIONS

The diagram below describes the basic IO relations for Z80_CTC writes, reads and interrupt acknowledge. The most important aspect to remember is that two rising edges are required for either reading or writing.

Not shown is ZC_T0 timing. ZC_T0 goes active on the rising CLK which causes the count to reach zero. ZC_T0 remains active until the next rising CLK.



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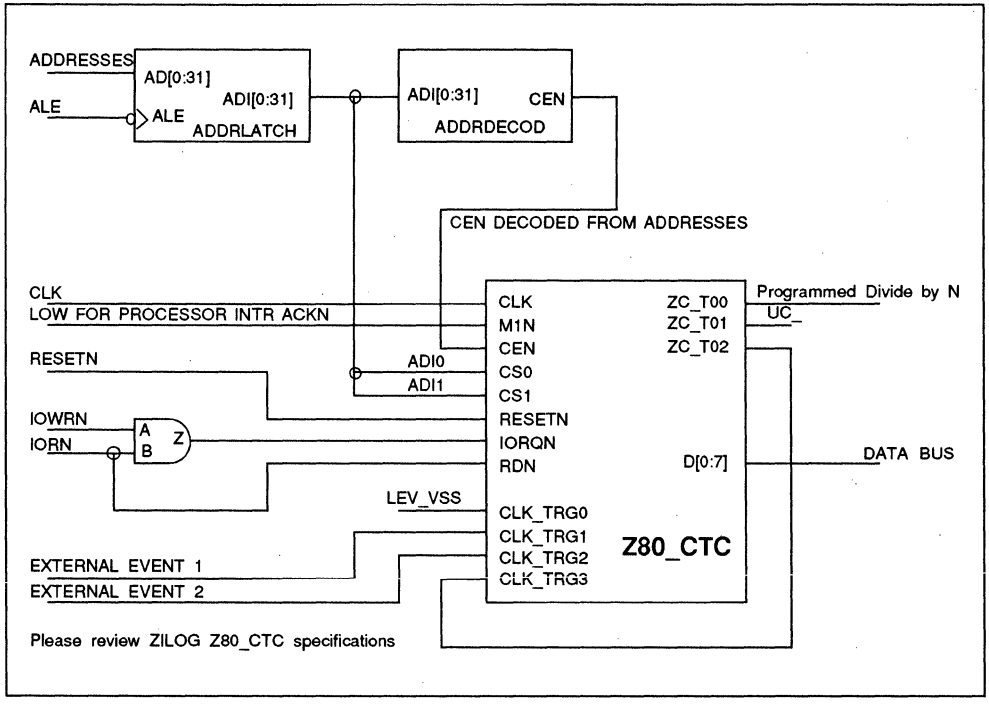
APPLICATION NOTES

The diagram below shows a simple application of the Z80_CTC. In the diagram the Z80_CTC is addressed by latched and decoded addresses controlling CEN. IORQN and RDN are computed from more common IORN and IOWRN signals. Two channels are cascaded to permit longer times. One channel counts external events.



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Boundary Scan Cells

Section 13

AT&T

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Boundary-Scan Introduction

Due to the increasing complexity of Integrated circuits, surface-mount interconnection technology has created significant new problems in the development and application of tests for printed circuit boards. To cope with this problem, a proposal has been prepared by an *ad hoc* international standards body, the Joint Test Action Group (JTAG), to standardize board interconnect test using Boundary-Scan (B-S). This proposal has been subsequently adopted by the IEEE P1149 Testability Bus Standards Committee as the P1149.1 standard. The adoption of JTAG's standard will accomplish two major goals: 1) to simplify testing of high-density circuit boards through B-S, and 2) to provide a common access to the various chip-level BIST resources for test and diagnosis at all levels of assembly.

JTAG is an international group representing companies in Europe and North America seeking solutions for the test problems in hybrid and PCB products created by the combination of complex integrated circuits and surface-mount technology.

A schematic overview of BIST & Boundary-Scan on a board is showing on the next page.

The B-S cells for the pins of a chip are interconnected so as to perform a shift register chain around the border of the device. This path is provided with serial input and output connections and appropriate clock and control signals. The serial path can be used for three purposes:
(1) External B-S Test
allows the interconnections between the various chips to be tested. Test data can be shifted into all BSOUT[1-3] cells associated with chip outputs pins and loaded in parallel through the chip interconnections into those BSIN[1-5] cells associated with input pins.
(2) Internal B-S Test
allows chips on a board to be tested. The B-S register can be used as a means of isolating system logic from stimuli received from surrounding chips while an internal self-test is performed.
(3) Sample Test
by parallel loading the BSIN[1-5] cells at inputs and the BSOUT[1-3] cells at outputs of a chip, and shifting out the results, the B-S register provides a means of , 'sampling' the data flowing through a chip without interfering with its normal function. This sample B-S test is valuable for design debugging and fault diagnosis.

BOUNDARY-SCAN TEST MODE DEFINITION

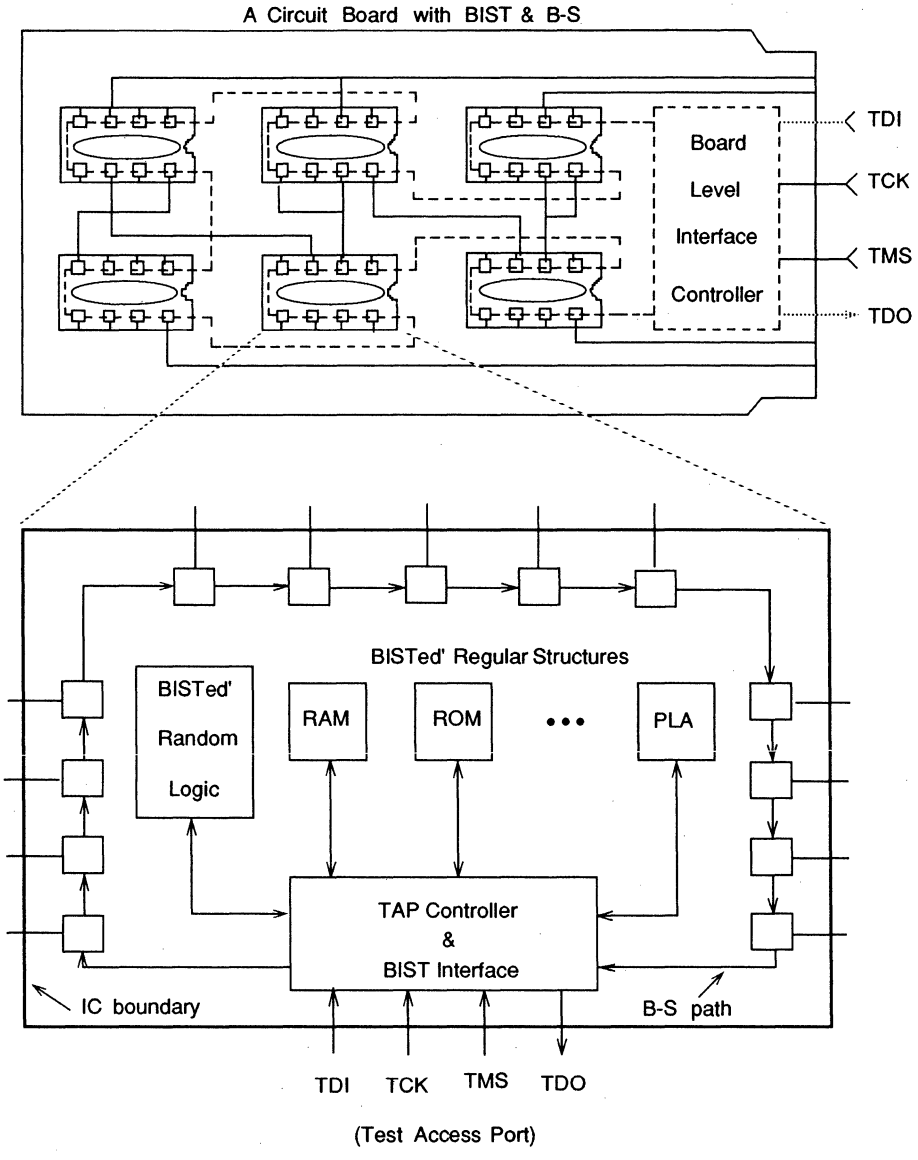
Test Mode	Logic Value of B-S Cells' MODE Line	
	Input (or MODI)	Output (or MODO)
Sample/Normal	0	0
External Only	0	1
Internal Only	1	0
External & Internal*	1	1

* used with BSIN5 and BSOUT3 cells only; non-test logic is protected during testing.

All BSIN[1-5] and BSOUT[1-3] cells support the three modes except BSIN3 supports "External and Normal Mode" only.

The performance, or maximum clock frequency, of B-S circuitry is dictated by that of the TAP controller (BSTAP).

BIST & BOUNDARY SCAN OVERVIEW



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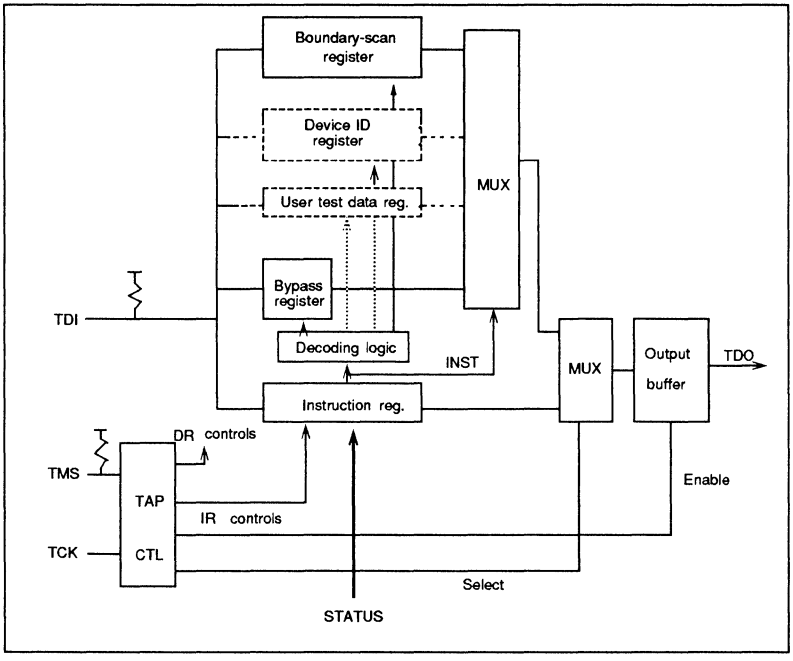
BLOCK DIAGRAM



B-S Identification Register BSATT

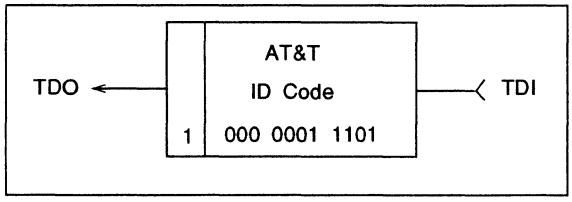
228 grids, 360 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSATT is the 12 most significant bits of the manufacturer's ID register for AT&T. It is compatible to JTAG 2.0 standard.

- When the SHIFTN pin is high, this register is loaded with/initialized to "1000 0001 1101" (or hex 81D) which is the official JTAG code assigned to AT&T. The code can be shifted out towards TDO when the SHIFTN pin is low.

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: TDI,TCK,SHIFTN;
OUTPUT: TDO;

Functional Descriptions

Inputs:

TDI	Serial test data input
TCK	Boundary Scan test clock
SHIFTN	Derived from SHIFTDR signal generated by BSTAP controller; active low

Output:

TDO	Serial test data output

CHARACTERISTICS

SWITCHING CHARACTERISTICS
VDD=5.0V, T=25°C, Nominal Processing

From Input	To Output	Area		Performance	
		Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
TCK↑	TDO↓	0.25	2.39	0.41	0.63
TCK↑	TDO↑	0.31	4.48	0.36	0.92

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Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area value	Perf. value	Unit
Minimum TDI Setup before TCK↑ Minimum SHIFTN Setup before TCK↑	3.4 3.4	2.4 2.4	ns

B-S Bidirectional Cell BSBD

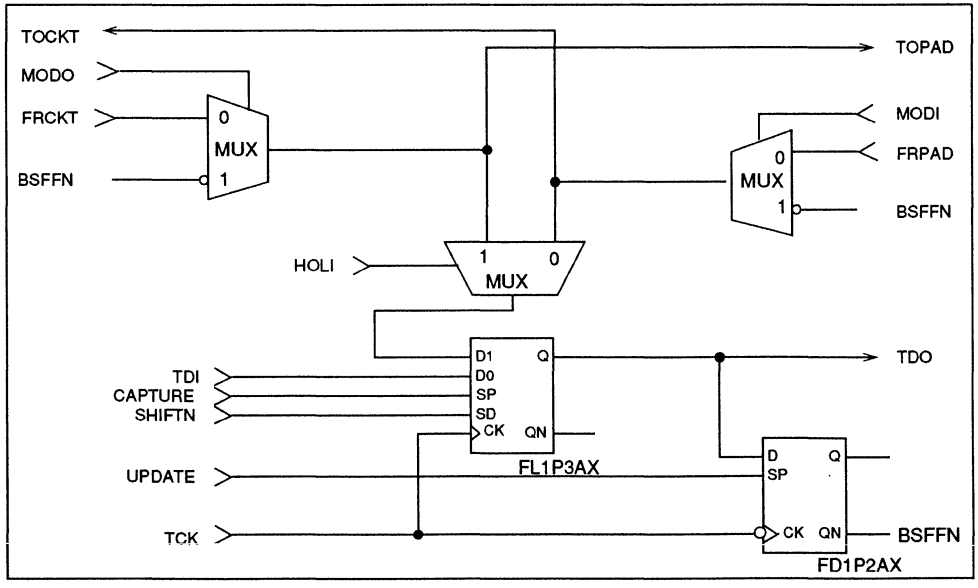
64 grids, 94 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSBD is a JTAG compatible boundary scan bidirectional cell.

- Used along with bidirectional I/O buffer
- Directional control line (HOLI) is controlled by BSOE
- Acts as an BSIN1 when HOLI = 0
- Acts as an BSOUT1 when HOLI = 1

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: FRCKT,TDI,TCK,HOLI,MODI,MODO,CAPTURE,SHIFTN,UPDATE,FRPAD;

OUTPUTS: TOCKT,TOPAD,TDO;

Functional Descriptions

Inputs:

FRCKT	Input from chip internal circuitry (to output pad)
TDI	Serial test data input (from previous boundary scan cell)
TCK	Boundary scan test clock
HOLI	Direction control signal (Hi:Output, Lo:Input)
MODI	Input mode control (asserted in "Internal Mode" only)
MODO	Output mode control (asserted in "External Mode" only)
CAPTURE	Capture/load scan register; from BSTAP controller
SHIFTN	Shift scan register (active low); from BSTAP controller
UPDATE	Update parallel output register (after SHIFT); from BSTAP controller
FRPAD	Input from chip input pad (to internal circuit)

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Outputs:

TOCKT	Output to chip internal circuit (from input pad)
TOPAD	Output to chip output pad (from internal circuit)
TDO	Serial test data output (to next boundary scan cell)

CHARACTERISTICS

SWITCHING CHARACTERISTICS
VDD=5.0V, T=25°C, Nominal Processing

From Input	To Output	Area		Performance	
		Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
TCK↓	TOCKT↓	2.95	5.37	3.00	1.20
TCK↓	TOCKT↑	2.39	9.25	2.29	1.69
TCK↓	TOPAD↓	2.95	5.37	3.00	1.20
TCK↓	TOPAD↑	2.39	9.25	2.29	1.69
TCK↑	TDO↓	1.83	6.54	1.22	1.01
TCK↑	TDO↑	2.19	2.00	1.17	0.87
FRCKT	TOPAD↓	1.42	5.37	0.76	1.20
FRCKT	TOPAD↑	1.48	9.25	0.61	1.69
MODI	TOCKT↓	1.42	5.37	0.76	1.20
MODI	TOCKT↑	1.48	9.25	0.61	1.69
MODO	TOPAD↓	1.42	5.37	0.76	1.20
MODO	TOPAD↑	1.48	9.25	0.61	1.69
FRPAD	TOCKT↓	1.42	5.37	0.76	1.20
FRPAD	TOCKT↑	1.48	9.25	0.61	1.69

Timing Requirements
VDD=5.0V, T=25°C, Nominal Processing

Description	Area value	Perf. value	Unit
Minimum FRCKT Setup before TCK↑	7.3	4.1	ns
Minimum TDI Setup before TCK↑	4.0	2.5	
Minimum HOLI Setup before TCK↑	5.6	3.4	
Minimum MODI Setup before TCK↑	7.3	4.1	
Minimum MODO Setup before TCK↑	7.3	4.1	
Minimum CAPTURE Setup before TCK↑	4.0	2.5	
Minimum SHIFTN Setup before TCK↑	4.0	2.5	
Minimum UPDATE Setup before TCK↓	1.6	1.2	
Minimum FRPAD Setup before TCK↑	7.3	4.1	

B-S By-Pass Cell

BSBP

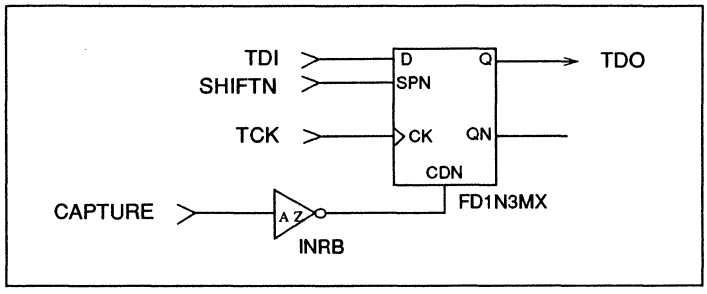
23 grids, 34 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSBP is a JTAG compatible boundary scan by-pass cell.

- Provides a short-circuit route for test data in scanning cycle especially during board diagnosis

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: TDI,TCK,CAPTURE,SHIFTN;
OUTPUT: TDO;

Functional Descriptions

Inputs:

TDI	Serial test data input (from TDI input pad)
TCK	Boundary scan test clock
CAPTURE	Capture/ load (logic 0) into by-pass register; derived from BSTAP controller
SHIFTN	Shift DR signal (active low); derived from BSTAP controller

Output:

TDO	Serial test data output (to the DR MUX)

CHARACTERISTICS

SWITCHING CHARACTERISTICS
VDD=5.0V, T=25°C, Nominal Processing

From Input	To Output	Area		Performance	
		Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
TCK↑	TDO↓	0.25	2.69	0.41	0.63
TCK↑	TDO↑	0.31	4.48	0.36	0.85

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Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area value	Perf. value	Unit
Minimum TDI Setup before TCK↑	2.7	1.9	ns
Minimum CAPTURE Setup before TCK↑	3.3	2.2	
Minimum SHIFTN Setup before TCK↑	2.7	1.9	

BIST RAM Interface Controller

BSBRIC

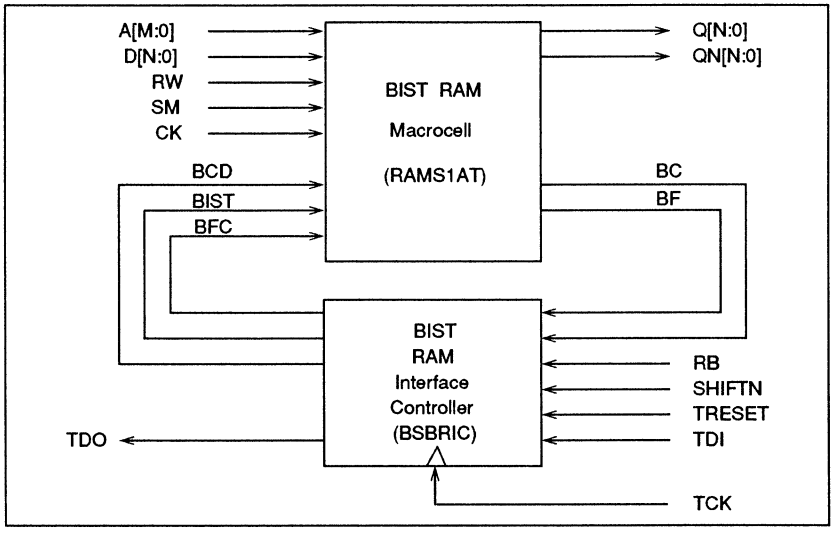
86 grids, 132 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

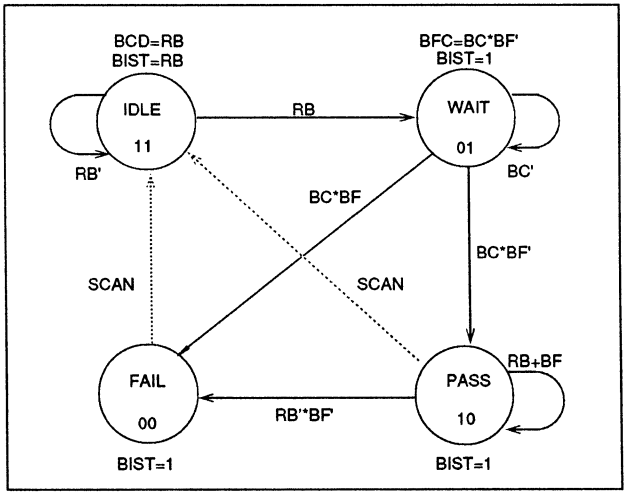
BSBRIC is a JTAG compatible circuit.

- Utilizes the JTAG boundary scan protocol to actuate the built-in self-test features of the AT&T RAMS1AT and then to shift out the results over the boundary scan output pin
- BSBRIC forces a 2-bit user test data register which is connected in parallel with the B-S register and bypass register

BLOCK DIAGRAM



STATE DIAGRAM



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TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: TDI,TCK,SHIFTN,RB,BC,BF,TRESET;
OUTPUTS: BCD,BFC,BIST,TDO;

Functional Descriptions

Inputs:

TDI	Serial test data input
TCK	Boundary scan test clock also used for RAMS1AT
SHIFTN	Shift out results (active low) from BSTAP controller
RB	Start BIST command input
BC	BIST complete from RAMS1AT
BF	BIST flag from RAMS1AT indicating PASS/FAIL (see RAMS1AT)
TRESET	Asynchronous reset command from BSTAP

Outputs:

BCD	BIST clear to RAMS1AT
BFC	BIST flag check to RAMS1AT, high checks for BF stuck at 0
BIST	BIST test mode to RAMS1AT
TDO	Serial test data output (to next boundary scan cell)

CHARACTERISTICS

SWITCHING CHARACTERISTICS
VDD=5.0V, T=25°C, Nominal Processing

From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
TCK↑	BCD↓	4.73	2.39	2.95	0.70
TCK↑	BCD↑	6.46	4.48	3.87	0.77
TCK↑	BFC↓	3.41	2.39	2.95	0.63
TCK↑	BFC↑	6.82	4.48	5.19	0.77
TCK↑	BIST↓	3.87	2.69	3.61	0.70
TCK↑	BIST↑	6.67	4.48	5.19	0.77
TCK↑	TDO↓	1.02	2.69	1.32	0.70
TCK↑	TDO↑	1.02	4.48	1.17	0.85

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area value	Perf. value	Unit
Minimum TDI Setup before TCK↑	2.9	2.1	ns
Minimum SHIFTN Setup before TCK↑	2.9	2.1	
Minimum RB Setup before TCK↑	6.4	3.6	
Minimum BC Setup before TCK↑	6.6	3.6	
Minimum BF Setup before TCK↑	6.6	3.5	
Minimum TRESET Setup before TCK↑	2.9	2.1	

System/Test Clock Multiplexer BSCKMUX

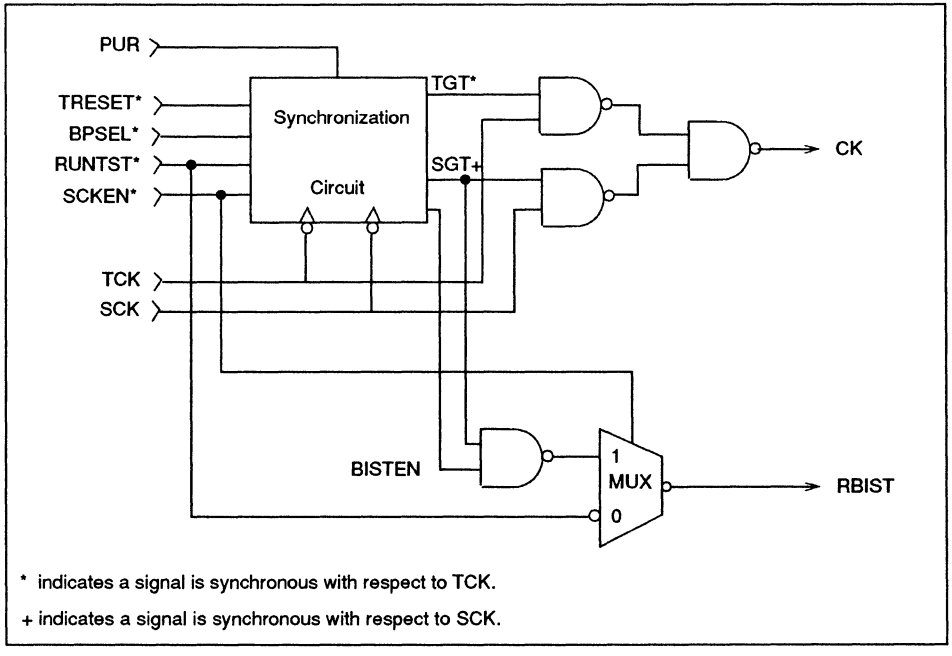
118 grids, 168 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSCKMUX is a system/test clock multiplexer for chip designs with boundary scan. It features:

- Two synchronizing D-type FF's are used for each input clock gating signal (SGT or TGT) to insure metastable free multiplexing.
- A Run BIST (RBIST) signal which assures synchronous activation of built-in self-test (e.g. BILBO; circular BIST) by the BSTAP. Note that when BIST runs on TCK (SCK), RBIST is simply driven by the RUNTST (SGT) signal, assuring its synchronization with respect to BSCKMUX output clock (CK).
- Input clock waveform duty-cycle is maintained by using multiplexing NAND gates which provide equivalent delay paths for both the rising and falling edges.

BLOCK DIAGRAM



* indicates a signal is synchronous with respect to TCK.

\+ indicates a signal is synchronous with respect to SCK.

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System/Test Clock Switching Conditions

CK Outputs	Conditions
SCK	1. TAP is in Test-Logic-Reset state (TRESET = 1) or 2. Bypass path is selected by an instruction in IR (BPSEL = 1) or 3. TAP is in Run-Test/Idle state AND system clock is enabled by an instruction in IR (RUNTST = SCKEN = 1) [NOTE: RBIST, synchronous with respect to SCK, is asserted if RUNTST = 1]
TCK	1. TRESET = BPSEL = RUNTST = 0 or 2. TRESET = BPSEL = SCKEN = 0 [NOTE: RBIST, synchronous with respect to TCK, is asserted if RUNTST = 1]

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: SCK,TCK,TRESET,RUNTST,SCKEN,BPSEL,PUR;
OUTPUTS: CK,RBIST;

FUNCTIONAL DESCRIPTIONS

Inputs:

SCK	System clock to be multiplexed
TCK	Test clock to be multiplexed
TRESET	Test logic reset signal from BSTAP
RUNTST	Run test signal from BSTAP
SCKEN	Enable system clock (during BIST), decoded from B-S IR
BPSEL	By-pass path select signal, decoded from b-s IR
[NOTE: SCK is always selected in by-pass mode according to JTAG spec.]	
PUR	Power Up Reset (e.g. from PUR40U), preset TRESET high

Outputs:

CK	Hazard-free clock signal (driven by SCK or TCK)
RBIST	Synchronized control signal for activating BIST; issued on falling edge of CK

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
TCK,SCK↓	CK↓	2.39	5.07	2.29	1.27
TCK,SCK↓	CK↑	3.31	4.48	2.95	0.77
SCK↓	RBIST↓	4.07	1.19	3.31	0.28
SCK↓	RBIST↑	5.19	1.19	4.02	0.21
TCK↑	RBIST↓	5.19	1.19	3.61	0.28
TCK↑	RBIST↑	7.23	1.19	5.34	0.21
RUNTST	RBIST↓	3.56	1.19	1.68	0.28
RUNTST	RBIST↑	2.70	1.19	1.42	0.21
SCKEN	RBIST↓	3.77	1.19	1.83	0.28
SCKEN	RBIST↑	4.02	1.19	1.98	0.21
PUR↓	CK↓	5.50	5.07	3.10	1.27
PUR↓	CK↑	9.41	4.48	4.89	0.77

Since BSCKMUX operates asynchronously, specification of set up times is meaningless here.

B-S Input 1 BSIN1

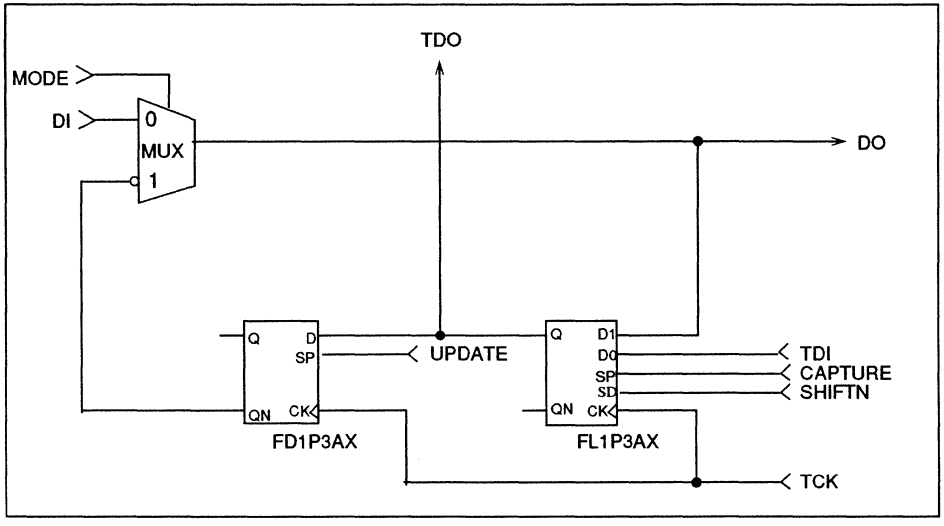
51 grids, 72 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSIN1 is a JTAG compatible standard boundary scan input cell.

- Includes shift register and parallel output register (update register)
- Totally synchronous operation

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: DI,TDI,TCK,MODE,CAPTURE,SHIFTN,UPDATE;

OUTPUTS: DO,TDO;

Functional Descriptions

Inputs:

DI	Normal input from chip input pad
TDI	Serial test data input (from previous boundary scan cell)
TCK	Boundary scan test clock
MODE	Input mode control (asserted in "Internal Mode" only)
CAPTURE	Capture/load scan register; from BSTAP controller
SHIFTN	Shift scan register (active low); from BSTAP controller
UPDATE	Update parallel output register (after SHIFT); from BSTAP controller

Outputs:

DO	Output from boundary scan input cell; drives normal input to chip internal circuitry
TDO	Serial test data output (to next boundary scan cell)

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
DI	DO↓	1.37	5.37	0.71	1.20
DI	DO↑	1.58	9.25	0.61	1.69
TCK↑	DO↓	2.14	5.37	1.73	1.20
TCK↑	DO↑	2.04	9.25	1.27	1.69
TCK↑	TDO↓	1.83	6.54	1.22	1.01
TCK↑	TDO↑	2.19	2.00	1.17	0.87
MODE	DO↓	1.37	5.37	0.71	1.20
MODE	DO↑	1.58	9.25	0.61	1.69

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area value	Perf. value	Unit
Minimum DI Setup before TCK↑	5.6	3.3	ns
Minimum TDI Setup before TCK↑	4.0	2.5	
Minimum MODE Setup before TCK↑	5.6	3.3	
Minimum CAPTURE Setup before TCK↑	4.0	2.5	
Minimum SHIFTN Setup before TCK↑	4.0	2.5	
Minimum UPDATE Setup before TCK↑	1.6	1.2	

B-S Input 2 BSIN2

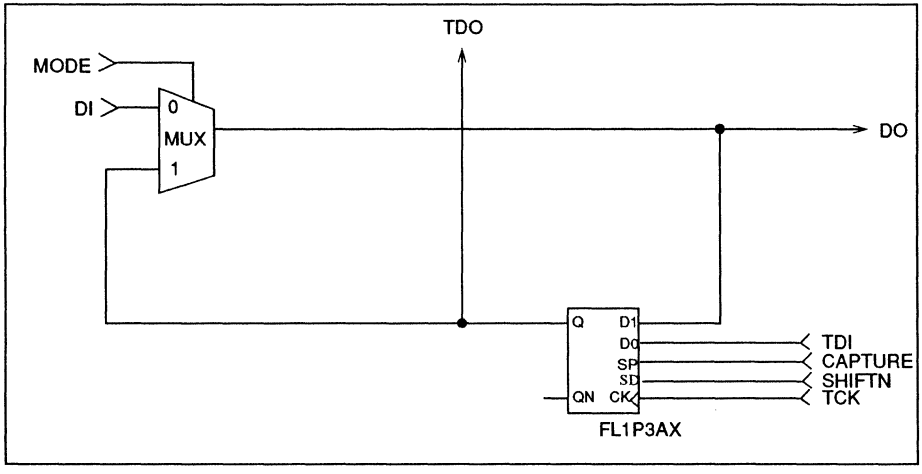
32 grids, 46 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSIN2 is a JTAG compatible boundary scan input cell.

- Boundary scan input cell without "update" register
- Totally synchronous operation

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: DI,TDI,TCK,MODE,CAPTURE,SHIFTN;

OUTPUTS: DO,TDO;

Functional Descriptions

Inputs:

DI	Normal input from chip input pad
TDI	Serial test data input (from previous boundary scan cell)
TCK	Boundary scan test clock
MODE	Input mode control (asserted in "Internal Mode" only)
CAPTURE	Capture/load scan register; from BSTAP controller
SHIFTN	Shift scan register (active low); from BSTAP controller

Outputs:

DO	Output from boundary scan input cell; drives normal input to chip internal circuitry
TDO	Serial test data output (to next boundary scan cell)

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B-S Input 2

BSIN2

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
DI	DO↓	1.37	5.37	0.71	1.20
DI	DO↑	1.58	9.25	0.61	1.69
TCK↑	DO↓	2.14	9.00	1.83	0.43
TCK↑	DO↑	1.93	3.70	1.32	0.63
TCK↑	TDO↓	1.88	6.54	1.27	1.01
TCK↑	TDO↑	2.04	2.00	1.22	0.87
MODE	DO↓	1.37	5.37	0.71	1.20
MODE	DO↑	1.58	9.25	0.61	1.69

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area value	Perf. value	Unit
Minimum DI Setup before TCK↑	5.6	3.3	ns
Minimum TDI Setup before TCK↑	4.0	2.5	
Minimum MODE Setup before TCK↑	5.6	3.3	
Minimum CAPTURE Setup before TCK↑	4.0	2.5	
Minimum SHIFTN Setup before TCK↑	4.0	2.5	

B-S Input 3

BSIN3

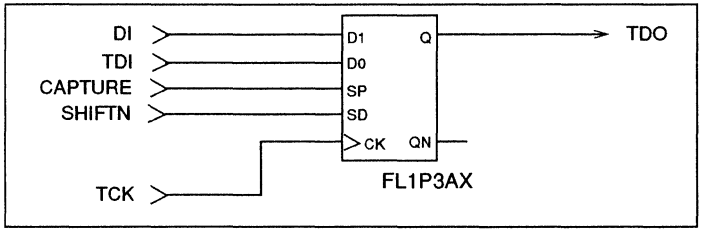
26 grids, 36 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSIN3 is a JTAG compatible boundary scan input cell.

- Boundary scan input cell without "update" output buffer; JTAG "External and Sample" mode are supported
- Totally synchronous operation

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: DI,TDI,TCK,CAPTURE,SHIFTN;

OUTPUT: TDO;

Functional Descriptions

Inputs:

DI	Normal input from chip input pad
TDI	Serial test data input (from previous boundary scan cell)
TCK	Boundary scan test clock
CAPTURE	Capture/ load scan register; from BSTAP controller
SHIFTN	Shift scan register (active low); from BSTAP controller

Output:

TDO	Serial test data output (to next boundary scan cell)

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
TCK↑	TDO↓	1.48	6.54	0.97	1.01
TCK↑	TDO↑	1.73	2.00	0.92	0.87

B-S Input 3

BSIN3

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area value	Perf. value	Unit
Minimum DI Setup before TCK↑	3.97	2.54	ns
Minimum TDI Setup before TCK↑	3.97	2.54	
Minimum CAPTURE Setup before TCK↑	3.97	2.54	
Minimum SHIFTN Setup before TCK↑	3.97	2.54	

B-S Input 4 BSIN4

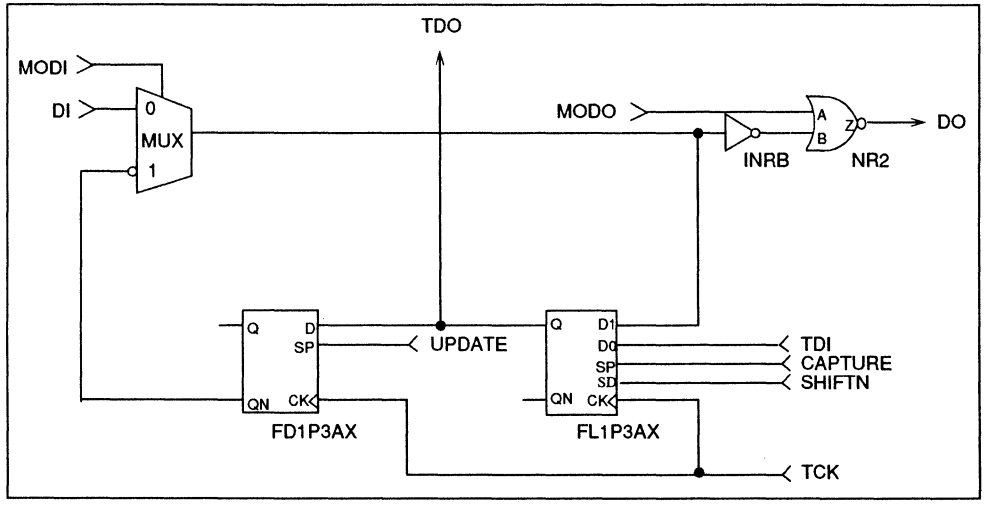
56 grids, 78 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSIN4 is a JTAG compatible boundary scan input cell.

- Standard boundary scan input cell with active high input pin signal which is inactivated or held low during boundary scan external test (e.g. used with active high RESET pin)
- Totally synchronous operation

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: DI,TDI,TCK,MODI,MODO,CAPTURE,SHIFTN,UPDATE;

OUTPUTS: DO,TDO;

Functional Descriptions

Inputs:

DI	Normal input from chip input pad
TDI	Serial test data input (from previous boundary scan cell)
TCK	Boundary scan test clock
MODI	Input mode control (asserted in "Internal Mode" only)
MODO	Output mode control (asserted in "External Mode" only)
CAPTURE	Capture/load scan register; from BSTAP controller
SHIFTN	Shift scan register (active low); from BSTAP controller
UPDATE	Update parallel output register (after SHIFT); from BSTAP controller

Outputs:

DO	Output from boundary scan input cell; drives normal input to chip internal circuitry
TDO	Serial test data output (to next boundary scan cell)

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From Input	To Output	Area		Performance	
		Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
DI	DO↓	3.26	2.99	1.53	0.70
DI	DO↑	4.78	8.66	1.73	1.48
TCK↑	DO↓	4.27	2.99	2.67	0.70
TCK↑	DO↑	5.34	8.66	2.44	1.48
TCK↑	TDO↓	1.83	6.54	1.22	1.01
TCK↑	TDO↑	2.19	2.00	1.17	0.87
MODI	DO↓	3.26	2.99	1.53	0.70
MODI	DO↑	4.78	8.66	1.73	1.48
MODO	DO↓	0.05	2.99	0.00	0.70
MODO	DO↑	0.20	8.66	0.10	1.48

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area value	Perf. value	Unit
Minimum DI Setup before TCK↑	6.5	3.5	ns
Minimum TDI Setup before TCK↑	4.0	2.5	
Minimum MODI Setup before TCK↑	6.5	3.5	
Minimum CAPTURE Setup before TCK↑	4.0	2.5	
Minimum SHIFTN Setup before TCK↑	4.0	2.5	
Minimum UPDATE Setup before TCK↑	1.6	1.2	

B-S Input 4N BSIN4N

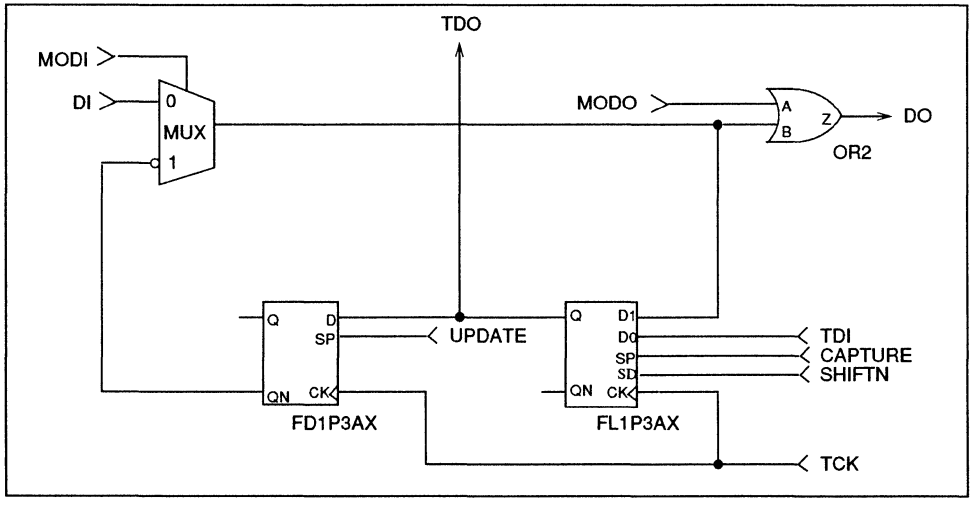
55 grids, 78 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSIN4N is a JTAG compatible boundary scan input cell.

- Standard boundary scan input cell with active low input pin signal inactivated or held high during boundary scan external test (e.g. used with active low RESET pin)
- Totally synchronous operation

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: DI,TDI,TCK,MODI,MODO,CAPTURE,SHIFTN,UPDATE;

OUTPUTS: DO,TDO;

Functional Descriptions

Inputs:

DI	Normal input from chip input pad
TDI	Serial test data input (from previous boundary scan cell)
TCK	Boundary scan test clock
MODI	Input mode control (asserted in "Internal Mode" only)
MODO	Output mode control (asserted in "External Mode" only)
CAPTURE	Capture/load scan register; from BSTAP controller
SHIFTN	Shift scan register (active low); from BSTAP controller
UPDATE	Update parallel output register (after SHIFT); from BSTAP controller

Outputs:

DO	Output from boundary scan input cell; drives normal input to chip internal circuitry
TDO	Serial test data output (to next boundary scan cell) .

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From Input	To Output	Area		Performance	
		Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
DI	DO↓	2.80	2.39	1.58	0.63
DI	DO↑	3.72	4.18	1.53	0.77
TCK↑	DO↓	3.81	2.39	2.75	0.63
TCK↑	DO↑	4.27	4.18	2.24	0.77
TCK↑	TDO↓	1.83	6.54	1.22	1.01
TCK↑	TDO↑	2.19	2.00	1.17	0.87
MODI	DO↓	2.80	2.39	1.58	0.63
MODI	DO↑	3.72	4.18	1.53	0.77
MODO	DO↓	0.66	2.39	0.46	0.63
MODO	DO↑	0.25	4.18	0.15	0.77

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area value	Perf. value	Unit
Minimum DI Setup before TCK↑	6.5	3.5	ns
Minimum TDI Setup before TCK↑	4.0	2.5	
Minimum MODI Setup before TCK↑	6.5	3.5	
Minimum CAPTURE Setup before TCK↑	4.0	2.5	
Minimum SHIFTN Setup before TCK↑	4.0	2.5	
Minimum UPDATE Setup before TCK↑	1.6	1.2	

B-S Input 5 BSIN5

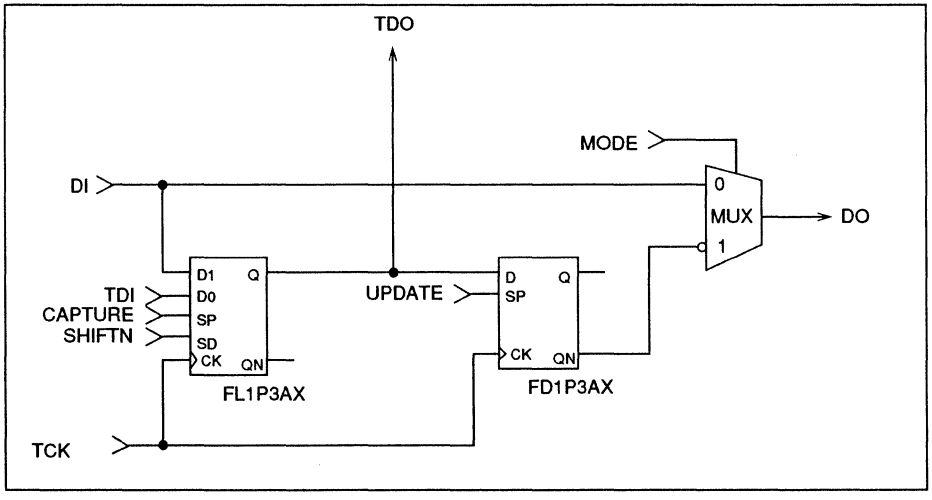
51 grids, 72 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSIN5 is a JTAG compatible boundary scan input cell.

- Standard boundary scan input cell with input pin signal controllable by the update register
- Shield chip logic from disturbances during boundary scan External Test (by setting MODE=1)
- Totally synchronous operation

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: DI,TDI,TCK,MODE,CAPTURE,SHIFTN,UPDATE;

OUTPUTS: DO,TDO;

Functional Descriptions

Inputs:

DI	Normal input from chip input pad
TDI	Serial test data input (from previous boundary scan cell)
TCK	Boundary scan test clock
MODE	Input mode control (asserted in "Internal Mode" only)
CAPTURE	Capture/ load scan register; from BSTAP controller
SHIFTN	Shift scan register (active low); from BSTAP controller
UPDATE	Update parallel output register (after SHIFT); from BSTAP controller

Outputs:

DO	Output from boundary scan input cell; drives normal input to chip internal circuitry
TDO	Serial test data output (to next boundary scan cell)

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
DI	DO↓	0.87	5.37	0.56	1.20
DI	DO↑	0.46	9.25	0.25	1.69
TCK↑	DO↓	1.17	5.37	1.22	1.20
TCK↑	DO↑	0.92	9.25	0.92	1.69
TCK↑	TDO↓	1.83	6.54	1.22	1.01
TCK↑	TDO↑	2.19	2.00	1.17	0.87
MODE	DO↓	0.87	5.37	0.56	1.20
MODE	DO↑	0.46	9.25	0.25	1.69

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area value	Perf. value	Unit
Minimum DI Setup before TCK↑	4.0	2.5	ns
Minimum TDI Setup before TCK↑	4.0	2.5	
Minimum CAPTURE Setup before TCK↑	4.0	2.5	
Minimum SHIFTN Setup before TCK↑	4.0	2.5	
Minimum UPDATE Setup before TCK↑	1.6	1.2	

B-S Instruction Register 1 BSIR1

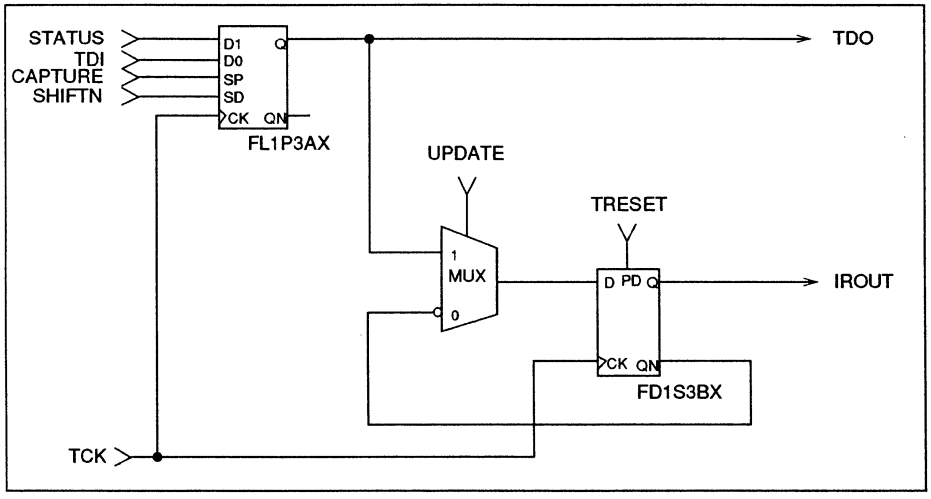
48 grids, 68 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSIR1 is a JTAG compatible boundary scan instruction register.

- Allows an instruction to be shifted into the device
- Fault isolation of the board-level serial test data path is supported. A constant '10' pattern must be loaded into the 2 most significant bits of the instruction register at the start of the instruction scan cycle.
- Includes shift register and parallel output register
- Instruction register with status input during capture

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: STATUS,TDI,TCK,TRESET,CAPTURE,SHIFTN,UPDATE;
OUTPUTS: IROUT,TDO;

Functional Descriptions

Inputs:

STATUS	Status data to be loaded with IR capture (BSIR1 only)
TDI	Serial test data input (from previous boundary scan IR cell)
TCK	Boundary scan test clock
TRESET	Test logic reset signal from BSTAP controller
CAPTURE	Capture/load scan register; from BSTAP controller
SHIFTN	Shift scan register (active low); from BSTAP controller
UPDATE	Update parallel output register (after SHIFT); from BSTAP controller

Outputs:

IROUT	Output from instruction register
TDO	Serial test data output (to next boundary scan IR cell)

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From Input	To Output	Area		Performance	
		Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
TCK↑	IROUT↓	0.10	2.69	0.20	0.70
TCK↑	IROUT↑	0.10	4.48	0.15	0.85
TCK↑	TDO↓	1.88	6.54	1.98	1.01
TCK↑	TDO↑	2.19	2.00	1.98	0.87

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area value	Perf. value	Unit
Minimum STATUS Setup before TCK↑	4.0	2.5	ns
Minimum TDI Setup before TCK↑	4.0	2.5	
Minimum TRESET Setup before TCK↑	1.2	1.0	
Minimum CAPTURE Setup before TCK↑	4.0	2.5	
Minimum SHIFTN Setup before TCK↑	4.0	2.5	
Minimum UPDATE Setup before TCK↑	2.5	1.4	

B-S Instruction Register 2 BSIR2

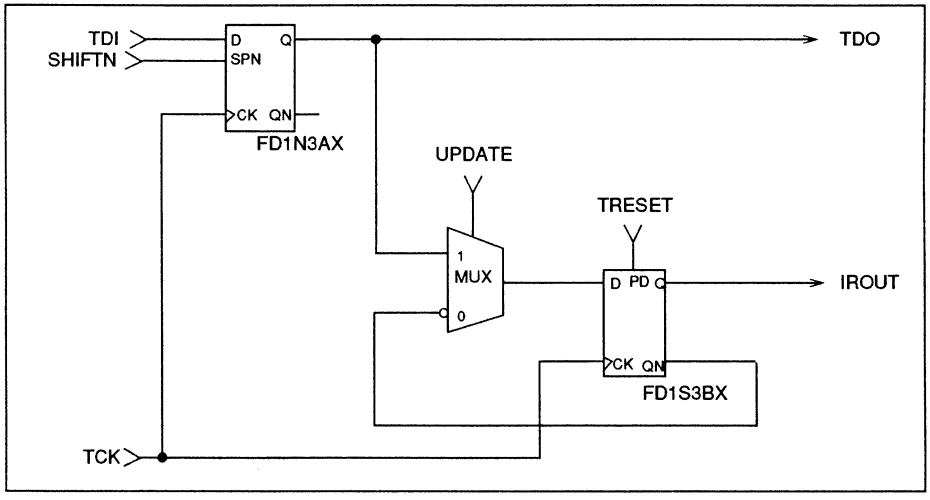
41 grids, 58 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSIR2 is a JTAG compatible boundary scan instruction register.

- Allows an instruction to be shifted into the device
- Fault isolation of the board-level serial test data path is supported. A constant '10' pattern must be loaded into the 2 most significant bits of the instruction register at the start of the instruction scan cycle.
- Includes shift register and parallel output register
- BSIR1 cell without status capture

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: TDI,TCK,TRESET,SHIFTN,UPDATE;
OUTPUTS: IROUT,TDO;

Functional Descriptions

Inputs:

TDI	Serial test data input (from previous boundary scan IR cell)
TCK	Boundary scan test clock
TRESET	Test logic reset signal from BSTAP controller
SHIFTN	Shift scan register (active low); from BSTAP controller
UPDATE	Update parallel output register (after SHIFT); from BSTAP controller

Outputs:

IROUT	Output from instruction register
TDO	Serial test data output (to next boundary scan IR cell)

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
TCK↑	IROUT↓	0.10	2.69	0.20	0.70
TCK↑	IROUT↑	0.10	4.48	0.15	0.85
TCK↑	TDO↓	1.48	10.8	0.92	2.04
TCK↑	TDO↑	1.32	7.76	0.97	1.69

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area value	Perf. value	Unit
Minimum TDI Setup before TCK↑	1.6	1.2	ns
Minimum TRESET Setup before TCK↑	1.2	1.0	
Minimum SHIFTN Setup before TCK↑	1.6	1.2	
Minimum UPDATE Setup before TCK↑	2.5	1.5	

B-S Output Enable Control BSOE

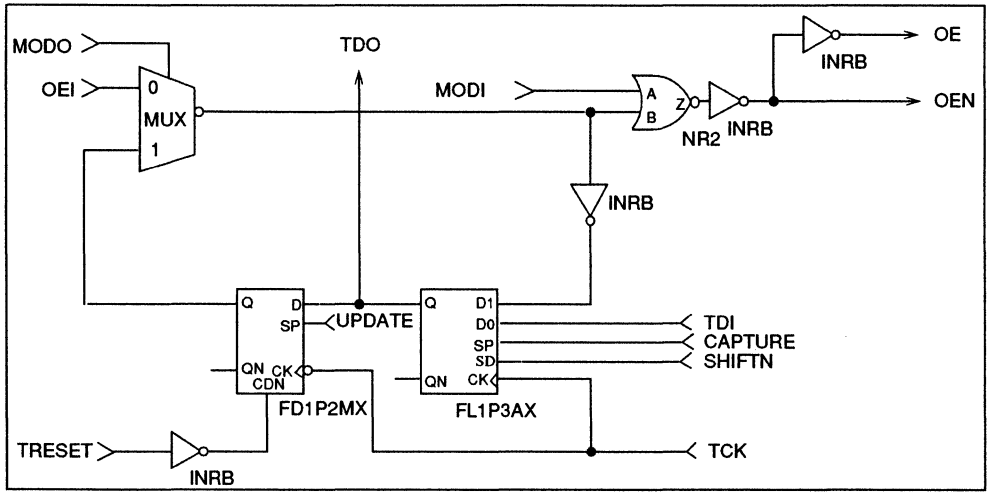
64 grids, 90 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSOE is a JTAG compatible boundary scan output enable control cell

- Shift register with capture for controlling the tri-state output pin or bidirectional pin

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: OEI,TDI,TCK,TRESET,MODI,MODO,CAPTURE,SHIFTN,UPDATE;
OUTPUTS: OE,OEN,TDO;

Functional Descriptions

Inputs:

OEI	Output enable input signal (deployed in normal/system mode)
TDI	Serial test data input (from previous boundary scan cell)
TCK	Boundary scan test clock
TRESET	Test logic reset signal from BSTAP controller
MODI	Input mode control (asserted in "Internal Mode" only)
MODO	Output mode control (asserted in "External Mode" only)
CAPTURE	Capture/ load scan register; from BSTAP controller
SHIFTN	Shift scan register (active low); from BSTAP controller
UPDATE	Update parallel output register (after SHIFT); from BSTAP controller

Outputs:

OE	Output enable signal to tri-state buffer
OEN	Negated output enable to tri-state buffer
TDO	Serial test data output (to next boundary scan cell)

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
OEI	OE↓	5.50	2.99	1.98	0.70
OEI	OE↑	4.53	4.48	1.83	0.77
OEI	OEN↓	4.30	2.99	1.73	0.70
OEI	OEN↑	5.14	4.48	1.83	0.77
TCK↑	TDO↓	1.88	6.54	1.98	1.01
TCK↑	TDO↑	2.19	2.00	1.98	0.87
TCK↓	OE↓	6.36	2.99	3.66	0.70
TCK↓	OE↑	6.62	4.48	4.53	0.77
TCK↓	OEN↓	6.41	2.99	4.43	0.70
TCK↓	OEN↑	6.01	4.48	3.51	0.77
MODI	OE↓	1.53	2.99	0.61	0.70
MODI	OE↑	2.85	4.48	1.02	0.77
MODI	OEN↓	2.65	2.99	0.92	0.70
MODI	OEN↑	1.17	4.48	0.46	0.77
MODO	OE↓	5.60	2.99	2.09	0.70
MODO	OE↑	5.09	4.48	2.41	0.77
MODO	OEN↓	4.89	2.99	2.04	0.70
MODO	OEN↑	5.24	4.48	1.93	0.77

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area value	Perf. value	Unit
Minimum OEI Setup before TCK↑	8.3	4.1	ns
Minimum TDI Setup before TCK↑	4.0	2.5	
Minimum TRESET Setup before TCK↓	3.3	2.2	
Minimum MODO Setup before TCK↑	8.4	4.2	
Minimum CAPTURE Setup before TCK↑	4.0	2.5	
Minimum SHIFTN Setup before TCK↑	4.0	2.5	
Minimum UPDATE Setup before TCK↓	2.7	1.9	

B-S Output 1 BSOUT1

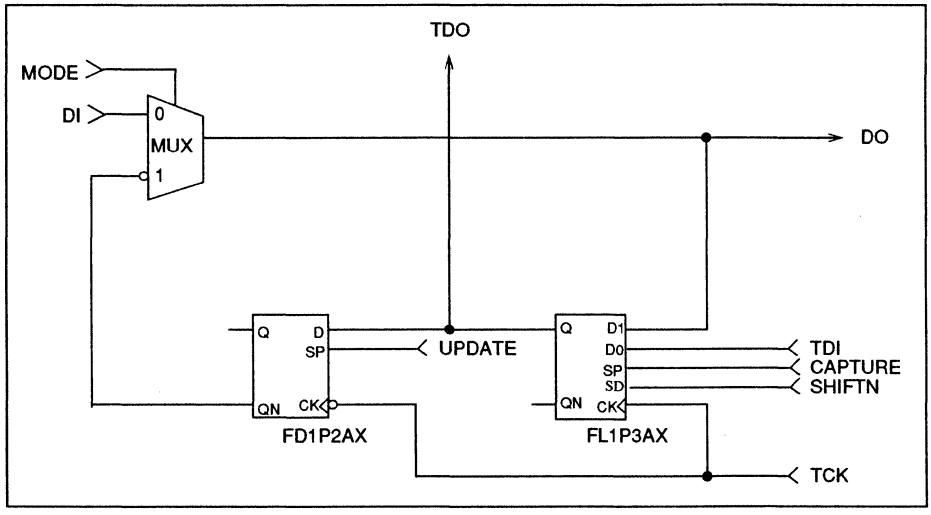
51 grids, 72 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSOUT1 is a JTAG compatible boundary scan output cell.

- Includes both shift register and parallel output register
- Device's normal output is captured in the shift register

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: DI,TDI,TCK,MODE,CAPTURE,SHIFTN,UPDATE;
OUTPUTS: DO,TDO;

Functional Descriptions

Inputs:

DI	Input from chip internal circuitry
TDI	Serial test data input (from previous boundary scan cell)
TCK	Boundary scan test clock
MODE	Output mode control (asserted in "External Mode" only)
CAPTURE	Capture/load scan register; from BSTAP controller
SHIFTN	Shift scan register (active low); from BSTAP controller
UPDATE	Update parallel output register (after SHIFT); from BSTAP controller

Outputs:

DO	Output to normal chip output pad
TDO	Serial test data output (to next boundary scan cell)

B-S Output 1 BSOUT1

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
DI	DO↓	1.37	5.37	0.71	1.20
DI	DO↑	1.53	9.25	0.61	1.69
TCK↓	DO↓	1.98	10.8	1.83	2.11
TCK↓	DO↑	1.88	7.76	1.32	1.69
TCK↑	TDO↓	1.83	6.54	1.22	1.01
TCK↑	TDO↑	2.19	2.00	1.17	0.87
MODE	DO↓	1.37	5.37	0.71	1.20
MODE	DO↑	1.53	9.25	0.61	1.69

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area value	Perf. value	Unit
Minimum DI Setup before TCK↑	5.5	3.3	ns
Minimum TDI Setup before TCK↑	4.0	2.5	
Minimum MODE Setup before TCK↑	5.5	3.3	
Minimum CAPTURE Setup before TCK↑	4.0	2.5	
Minimum SHIFTN Setup before TCK↑	4.0	2.5	
Minimum UPDATE Setup before TCK↓	1.6	1.2	

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B-S Output 2 BSOUT2

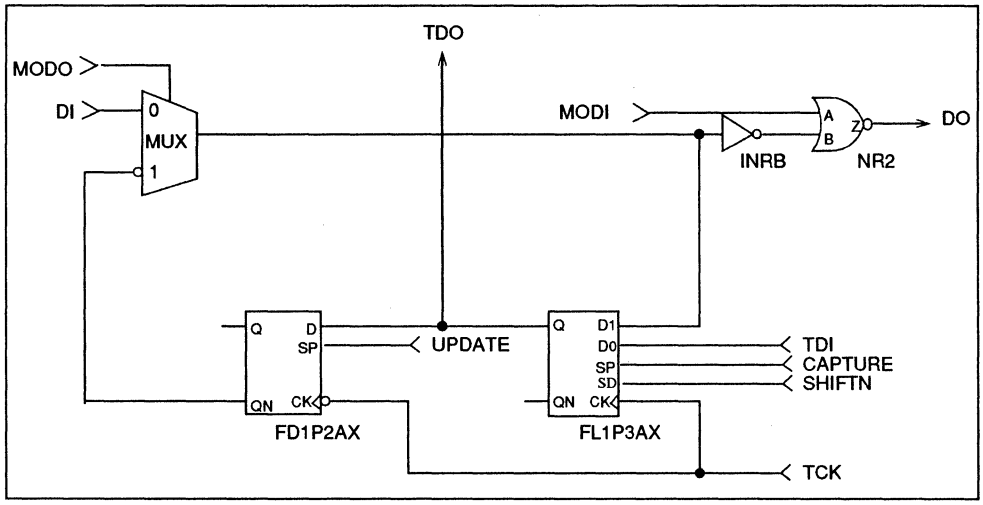
56 grids, 78 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSOUT2 is a JTAG compatible boundary scan output cell.

- Standard boundary scan output cell with (active high) output pin inactivated or held low during internal test (e.g. used with active high interrupt pin)

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: DI,TDI,TCK,MODI,MODO,CAPTURE,SHIFTN,UPDATE;
OUTPUTS: DO,TDO;

Functional Descriptions

Inputs:

DI	Input from chip internal circuitry
TDI	Serial test data input (from previous boundary scan cell)
TCK	Boundary scan test clock
MODI	Input mode control (asserted in "Internal Mode" only)
MODO	Output mode control (asserted in "External Mode" only)
CAPTURE	Capture/load scan register; from BSTAP controller
SHIFTN	Shift scan register (active low); from BSTAP controller
UPDATE	Update parallel output register (after SHIFT); from BSTAP controller

Outputs:

DO	Output to normal chip output pad
TDO	Serial test data output (to next boundary scan cell)

B-S Output 2 BSOUT2

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
DI	DO↓	3.31	2.99	1.53	0.70
DI	DO↑	4.73	8.66	1.73	1.48
TCK↓	DO↓	4.12	2.99	2.99	0.70
TCK↓	DO↑	5.19	8.66	8.66	1.48
TCK↑	TDO↓	1.83	6.54	2.99	1.01
TCK↑	TDO↑	2.19	2.00	8.66	0.87
MODI	DO↓	0.05	2.99	0.00	0.70
MODI	DO↑	0.20	8.66	0.10	1.48
MODO	DO↓	3.31	2.99	1.53	0.70
MODO	DO↑	4.73	8.66	1.73	1.48

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area value	Perf. value	Unit
Minimum DI Setup before TCK↑	6.5	3.5	ns
Minimum TDI Setup before TCK↑	4.0	2.5	
Minimum MODO Setup before TCK↑	6.4	3.5	
Minimum CAPTURE Setup before TCK↑	4.0	2.5	
Minimum SHIFTN Setup before TCK↑	4.0	2.5	
Minimum UPDATE Setup before TCK↓	1.6	1.2	

B-S Output 2N BSOUT2N

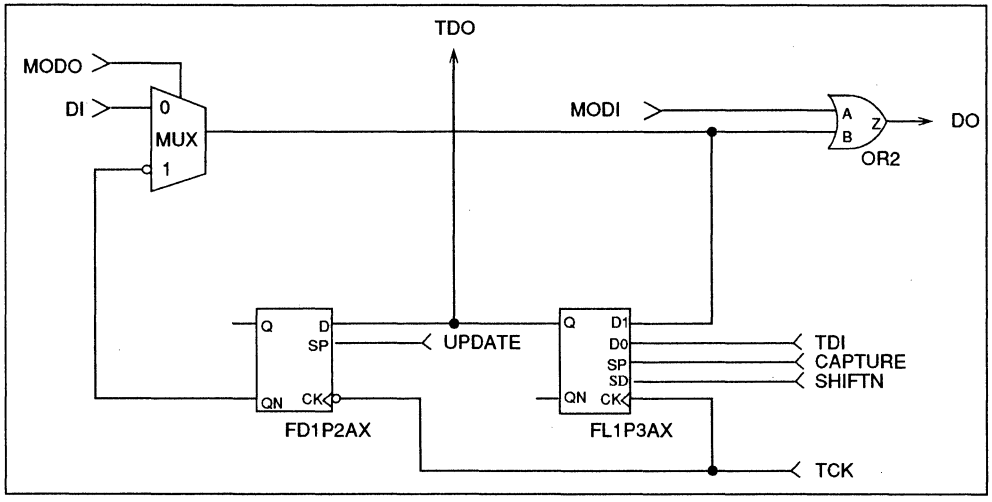
55 grids, 78 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSOUT2N is a JTAG compatible boundary scan output cell.

- Standard boundary scan output cell with (active low) output pin inactivated or held high during internal test (e.g. used with active low interrupt pin)

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: DI,TDI,TCK,MODI,MODO,CAPTURE,SHIFTN,UPDATE;
OUTPUTS: DO,TDO;

Functional Descriptions

Inputs:

DI	Input from chip internal circuitry
TDI	Serial test data input (from previous boundary scan cell)
TCK	Boundary scan test clock
MODI	Input mode control (asserted in "Internal Mode" only)
MODO	Output mode control (asserted in "External Mode" only)
CAPTURE	Capture/load scan register; from BSTAP controller
SHIFTN	Shift scan register (active low); from BSTAP controller
UPDATE	Update parallel output register (after SHIFT); from BSTAP

Outputs:

DO	Output to normal chip output pad
TDO	Serial test data output (to next boundary scan cell)

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
DI	DO↓	2.85	2.39	1.58	0.63
DI	DO↑	3.66	4.18	1.53	0.77
TCK↓	DO↓	1.37	2.39	2.85	0.63
TCK↓	DO↑	4.12	4.18	2.29	0.77
TCK↑	TDO↓	1.83	6.54	1.22	1.01
TCK↑	TDO↑	2.19	2.00	1.17	0.87
MODI	DO↓	0.66	2.39	0.46	0.63
MODI	DO↑	0.25	4.18	0.15	0.77
MODO	DO↓	2.85	2.39	1.58	0.63
MODO	DO↑	3.66	4.18	1.52	0.77

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area value	Perf. value	Unit
Minimum DI Setup before TCK↑	6.5	3.5	ns
Minimum TDI Setup before TCK↑	4.0	2.5	
Minimum MODO Setup before TCK↑	6.5	3.5	
Minimum CAPTURE Setup before TCK↑	4.0	2.5	
Minimum SHIFTN Setup before TCK↑	4.0	2.5	
Minimum UPDATE Setup before TCK↓	1.6	1.2	

B-S Output 3 BSOUT3

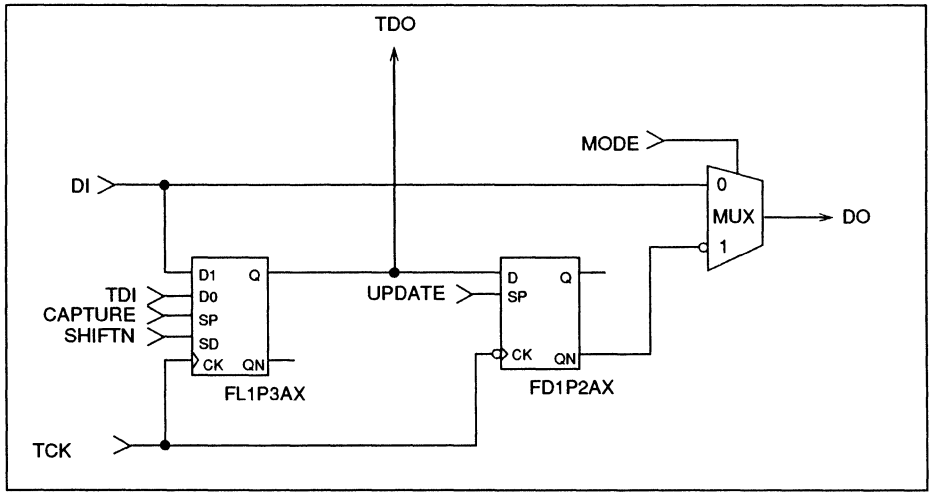
51 grids, 72 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSOUT3 is a JTAG compatible boundary scan output cell.

- Standard boundary scan output cell with output pin controllable by update register
- Shield outside circuitry from disturbances during boundary scan Internal Test (by setting MODE=1).

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: DI,TDI,TCK,MODE,CAPTURE,SHIFTN,UPDATE;
OUTPUTS: DO,TDO;

Functional Descriptions

Inputs:

DI	Input from chip internal circuitry
TDI	Serial test data input (from previous boundary scan cell)
TCK	Boundary scan test clock
MODE	Output mode control (asserted in "External Mode" only)
CAPTURE	Capture/load scan register; from BSTAP controller
SHIFTN	Shift scan register (active low); from BSTAP controller
UPDATE	Update parallel output register (after SHIFT); from BSTAP

Outputs:

DO	Output to normal chip output pad
TDO	Serial test data output (to next boundary scan cell)

B-S Output 3 BSOUT3

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
DI	DO↓	0.87	5.37	0.56	1.20
DI	DO↑	0.43	9.25	0.25	1.69
TCK↓	DO↓	1.12	5.37	1.22	1.20
TCK↓	DO↑	0.81	9.25	0.92	1.69
TCK↑	TDO↓	1.83	6.54	1.22	1.01
TCK↑	TDO↑	2.19	2.00	1.17	0.87
MODE	DO↓	0.87	5.37	0.56	1.20
MODE	DO↑	0.46	9.25	0.25	1.69

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area value	Perf. value	Unit
Minimum DI Setup before TCK↑	4.0	2.5	ns
Minimum TDI Setup before TCK↑	4.0	2.5	
Minimum MODE Setup before TCK↑	4.0	2.5	
Minimum CAPTURE Setup before TCK↑	4.0	2.5	
Minimum SHIFTN Setup before TCK↑	4.0	2.5	
Minimum UPDATE Setup before TCK↓	1.6	1.2	

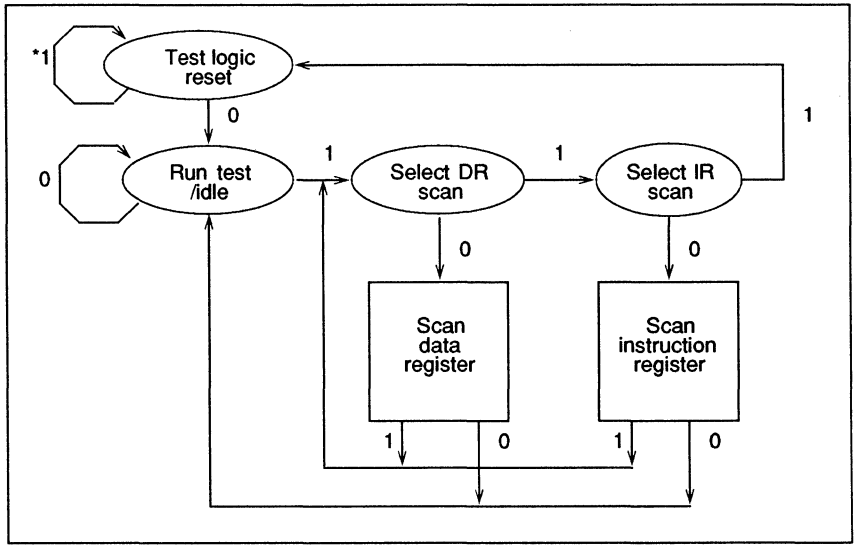
223 grids, 336 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSTAP is a JTAG compatible Test Access Port (BSTAP) controller. State assignments used are from JTAG 2.0/P1149.1 specifications. All control signals are issued on the rising edge of TCK, except ENABLE which changes on the falling edge. This is to conform to the JTAG requirement that TDO should be updated on the falling edge of TCK. SELECT signal is asserted in RESET and RUNTEST states to reduce the associated logic. The following features of BSTAP contribute to the viability of JTAG/P1149.1 as an international standard:

- A fixed set of pins: Test Data Input (TDI), Test Data Output (TDO), Test Mode Select (TMS), Test Clock (TCK), and an optional asynchronous reset pin for initializing test logic up on power up.
- A well-defined protocol ensuring inter-operability among all B-S equipped devices from different vendors.
- A set of internal control signals, which separate a single serial bit stream (applied on TDI) into test data and test instructions. This provides great design flexibility to the chip designer.
- A unified scan mechanism for controlling and accessing on-chip BIST structures.

MAIN STATE DIAGRAM



* The logic value adjacent to a state transition arc corresponds the value of TMS.

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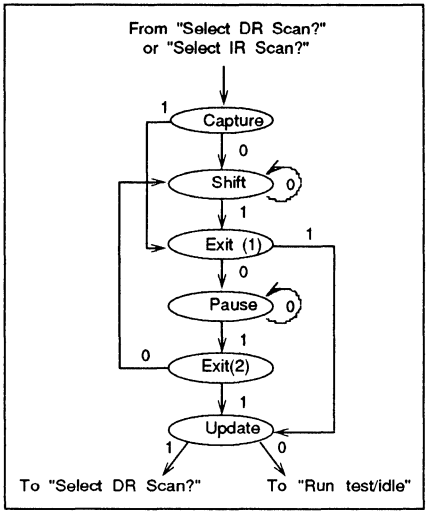
SCAN STATE DIAGRAM



Function Table

STATE	State Assignment (HEX)	Control Signals Asserted
RESET	(F)	TRESET, SELECT
RUNTEST	(C)	RUNTST, SELECT
SCAN DR	(7)	--
CAPTURE DR	(6)	CAPTUREDR, ENABLE
SHIFT DR	(2)	SHIFTDR, ENABLE
EXIT1 DR	(1)	ENABLE
UPDATE DR	(5)	UPDATEDR
EXIT2 DR	(0)	ENABLE
PAUSE DR	(3)	ENABLE
SCAN IR	(4)	--
CAPTURE IR	(E)	CAPTUREIR, ENABLE, SELECT
SHIFT IR	(A)	SHIFTIR, ENABLE, SELECT
EXIT1 IR	(9)	ENABLE, SELECT
UPDATE IR	(D)	UPDATEIR, SELECT
EXIT2 IR	(8)	ENABLE, SELECT
PAUSE IR	(B)	ENABLE, SELECT

TERMINAL DESCRIPTION

Netlist Order

Inputs: TMS, TCK, PUR;
Outputs: TRESET, RUNTST, SELECT, ENABLE, CAPTUREDR, CAPTUREIR, SHIFTDR,SHIFTIR, UPDATEDR, UPDATEIR;

FUNCTIONAL DESCRIPTIONS

Inputs:

TMS	Test Mode Select
TCK	Test Clock
PUR	Power Up Reset (e.g. from PUR40U), forces TRESET high

Outputs:

TRESET	Test logic reset
RUNTST	Run test (start internal BIST tests)
SELECT	HI: select IR; LO: select DR
ENABLE	Test data output pin (TDO) enable; issued on falling TCK
CAPTUREDR	Capture/parallel load DR
CAPTUREIR	Capture/parallel load IR
SHIFTDR	Shift DR
SHIFTIR	Shift IR
UPDATEDR	Update/parallel load DR output buffer FFs
UPDATEIR	Update/parallel load IR output buffer FFs

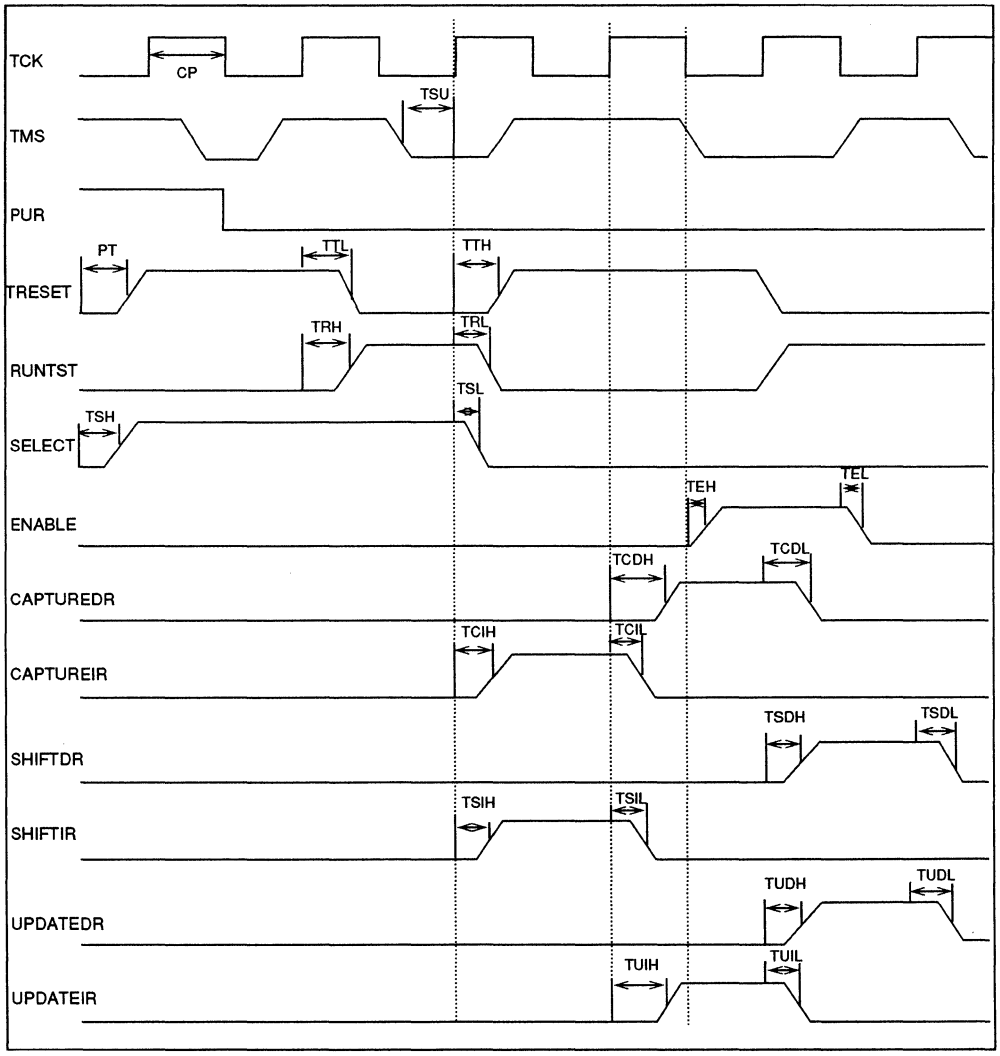
CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing						
Symbol	From Input	To Output	Area		Performance	
			Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
TTL	TCK↑	TRESET↓	3.61	2.69	2.95	0.70
TTH	TCK↑	TRESET↑	4.02	17.0	3.92	2.89
TRL	TCK↑	RUNTST↓	5.24	2.69	4.12	0.70
TRH	TCK↑	RUNTST↑	5.29	17.0	3.92	2.89
TSL	TCK↑	SELECT↓	3.51	2.99	2.85	0.70
TSH	TCK↑	SELECT↑	3.46	4.48	3.66	0.77
TEL	TCK↓	ENABLE↓	0.10	2.69	0.20	0.63
TEH	TCK↓	ENABLE↑	0.15	4.48	0.20	0.85
TCDL	TCK↑	CAPTUREDR↓	5.04	2.69	4.12	0.70
TCDH	TCK↑	CAPTUREDR↑	5.19	17.0	3.92	2.89
TCIL	TCK↑	CAPTUREIR↓	5.04	2.69	4.12	0.70
TCIH	TCK↑	CAPTUREIR↑	5.19	17.0	3.92	2.89
TSDL	TCK↑	SHIFTDR↓	5.34	2.69	4.33	0.70
TSDH	TCK↑	SHIFTDR↑	5.65	17.0	3.72	2.89
TSIL	TCK↑	SHIFTIR↓	5.34	2.69	4.33	0.70
TSIH	TCK↑	SHIFTIR↑	5.65	17.0	3.92	2.89
TUDL	TCK↑	UPDATEDR↓	5.24	2.69	4.12	0.70
TUDH	TCK↑	UPDATEDR↑	5.29	17.0	3.92	2.89
TUIL	TCK↑	UPDATEIR↓	5.24	2.69	4.12	0.70
TUIH	TCK↑	UPDATEIR↑	5.29	17.0	3.92	2.89
PT	PUR↑	TRESET↑	4.02	17.0	3.92	2.89

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing				
Symbol	Description	Area value	Perf. value	Unit
TSU	Minimum TMS Setup before TCK↑	6.2	2.9	ns
CP	Minimum Clock Pulse High *	6.9	5.2	

* = (50% duty cycle required by JTAG)

TIMING DIAGRAM



B-S Serial Output Cell — BSTDO

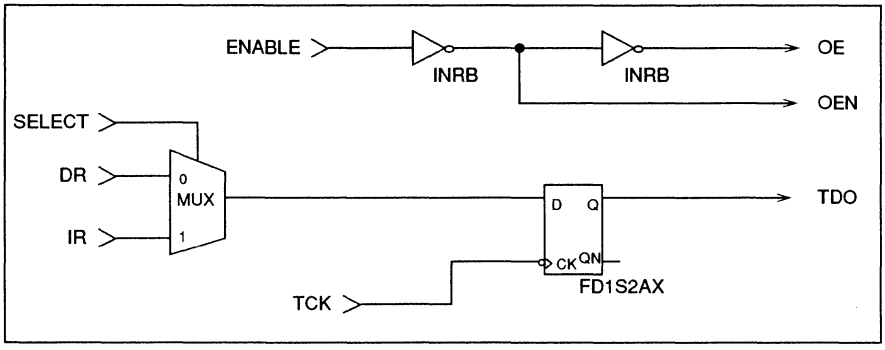
24 grids, 34 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSTDO is a JTAG compatible TDO output buffer cell.

- Generates TDO signal on the falling edge of TCK according to JTAG spec
- Contains an input MUX for selecting the MSB of either Data register or Instruction register as serial output
- Generates the tri-state buffer control signal for TDO
- Used with standard tri-state output buffer

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: DR,IR,TCK,SELECT,ENABLE;
OUTPUTS: OE,OEN,TDO;

Functional Descriptions

Inputs:

DR	MSB of a data register
IR	MSB of the instruction register
TCK	Boundary Scan test clock
SELECT	Select (IR) signal; from BSTAP controller
ENABLE	Enable (TDO) signal; from BSTAP controller

Outputs:

OE	Output enable signal (to TDO tri-state buffer)
OEN	Negated output enable signal (to TDO tri-state buffer)
TDO	Serial test data output (to TDO output pad)

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pf)	Intrinsic (ns)	Extrinsic (ns/pf)
TCK↓	TDO↓	0.10	2.69	0.20	0.63
TCK↓	TDO↑	0.15	4.48	0.20	0.85
ENABLE	OE↓	1.02	2.99	0.41	0.70
ENABLE	OE↑	0.56	4.48	0.25	0.77
ENABLE	OEN↓	0.36	2.99	0.15	0.70
ENABLE	OEN↑	0.66	4.48	0.25	0.77

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area value	Perf. value	Unit
Minimum DR Setup before TCK↓	2.1	1.4	ns
Minimum IR Setup before TCK↑	2.1	1.4	
Minimum SELECT Setup before TCK↑	2.2	1.5	

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Section 14

AT&T


AT&T

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