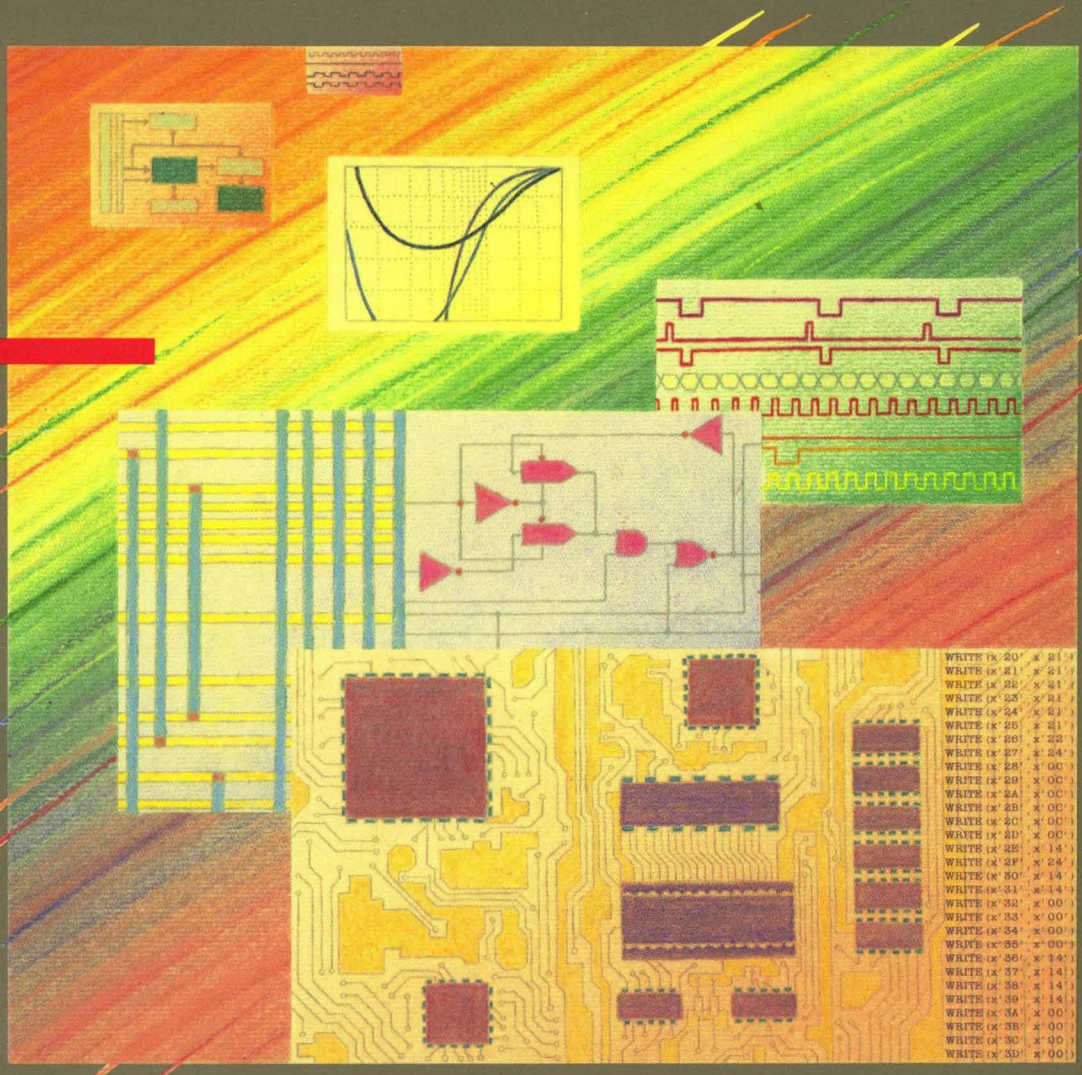
0.9 μm CMOS Cell Library

AT&T

Standard Cells and Function Blocks



1990

0.9 μm CMOS Cell Library

Standard Cells and Function Blocks

AT&T

ASIC Standard-Cell Library

0.9μm CMOS Technology

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January, 1990

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This section provides a quick overview of the functions available in AT&T's 0.9µm CMOS library.

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FD1N3JX	21	32	PE	SPL	--	NL	FL1N3JX	7-17
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FD1P2AX	19	26	NE	--	--	PL	FL1P2AX	7-19
FD1P2JX	21	32	NE	SPL	--	PL	FL1P2JX	7-20
FD1P2MX	21	32	NE	--	SNL	PL	FL1P2MX	7-21
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MS = Master-Slave, NE = Negative Edge-Triggered, NL = Negative Level,
PE = Positive Edge-Triggered, PL = Positive Level,
SNL = Synchronous Negative Level, SPL = Synchronous Positive Level

Static Flip-Flops and Latches

Cell	Grids	Transistors	Clocking	Preset	Clear	Sample	Scan Equivalent	Page
FD1S3IX	18	24	PE	--	SPL	--	FL1S3IX	7-52
FD1S3JX	16	22	PE	SPL	--	--	FL1S3JX	7-53
FD1S3KX	22	30	PE	NL	NL	--	FL1S3KX	7-54
FD1S3LX	18	24	PE	SNL	--	--	FL1S3LX	7-55
FD1S3MX	15	22	PE	--	SNL	--	FL1S3MX	7-56
FD1S3NX	20	28	PE	NL	PL	--	FL1S3NX	7-57
FD1S3OX	19	26	PE	SPL	SPL	--	FL1S3OX	7-58
FD1S5A	9	10	NL	--	--	--	--	7-59
FD1S5B	9	12	NL	PL	--	--	--	7-60
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FD2N1A	20	28	MS	--	--	NL	--	7-65
FD2N1J	23	34	MS	SPL	--	NL	--	7-66
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FD2S1I	17	26	MS	--	SPL	--	FL2S1I	7-78
FD2S1J	16	24	MS	SPL	--	--	FL2S1J	7-79
FD2S1KX	21	32	MS	NL	NL	--	FL2S1KX	7-80
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FD2S1M	16	24	MS	--	SNL	--	FL2S1M	7-82
FD2S1NX	20	30	MS	NL	PL	--	FL2S1NX	7-83
FL1N2AX	26	36	NE	--	--	NL	(FD1N2AX)	7-84
FL1N2JX	27	38	NE	SPL	--	NL	(FD1N2JX)	7-85
FL1N2MX	27	38	NE	--	SNL	NL	(FD1N2MX)	7-86
FL1N3AX	26	36	PE	--	--	NL	(FD1N3AX)	7-87
FL1N3JX	27	38	PE	SPL	--	NL	(FD1N3JX)	7-88
FL1N3MX	27	38	PE	--	SNL	NL	(FD1N3MX)	7-89
FL1P2AX	26	36	NE	--	--	PL	(FD1P2AX)	7-90
FL1P2JX	27	38	NE	SPL	--	PL	(FD1P2JX)	7-91
FL1P2MX	27	38	NE	--	SNL	PL	(FD1P2MX)	7-92
FL1P3AX	26	36	PE	--	--	PL	(FD1P3AX)	7-93
FL1P3JX	27	38	PE	SPL	--	PL	(FD1P3JX)	7-94
FL1P3MX	27	38	PE	--	SNL	PL	(FD1P3MX)	7-95

MS = Master-Slave, NE = Negative Edge-Triggered, NL = Negative Level,
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Static Flip-Flops and Latches

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Parameterized Macrocells

Linear Cells Designed to Fit into the I/O Buffer Ring

Linear Cells Designed to Fit into Standard-Cell Rows

(Suffix A for area-optimized cells, suffix P for performance-optimized cells)

FDS Synthesized Macrocells

MSI/LSI Functions

Boundary Scan Cells

Introduction

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Section 1

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1

Introduction

0.9μm CMOS Library

This book contains the ASIC (Application Specific Integrated Circuit) design information using AT&T's state-of-the-art, 0.9μm, twin-tub CMOS technology. To exploit the VLSI capabilities of custom circuits, AT&T has developed a comprehensive computer-based and cell-based custom design that offers the benefits of full-custom circuits at significantly reduced development time and cost. This system has enabled us to achieve exceptionally high first-model success rates.

If you are a system or IC design-house representative, consider the complete range of services from AT&T:

- State-of-the-art CMOS technology
- Extensive cell libraries
- Industry-leading CAD tools that carry your design ideas from schematic capture to layout
- Support of leading workstation platforms by schedule shown on the next page
- Regional design centers, staffed with experienced AT&T engineers and equipped with the latest hardware
- Complete photomask and wafer production capabilities in our own manufacturing plants (both in the United States and Europe)
- Fast turnaround of fully assembled and tested chips in both model and production quantities. Normally, chips are tested to full specifications.

From concept to final review, our design cycle offers a variety of entry points. The typical transfer of responsibility to AT&T is the pre-layout review. But the choice of where we take over the job is up to you.

To help ensure the manufacturability of all of your designs, we process your initial prototypes on the same fabrication line that will supply your production.

CAD System

AT&T's integrated CAD system is comprehensive. There are CAD tools, which are among the most powerful in the industry, available to assist the designer in each phase of IC development. The output from any CAD tool is in the form required for input to the next tool in the design cycle. This results in a fully integrated CAD environment and frees the designer from time-consuming and error-prone data conversions.

The schematic-capture tool is flexible and easy to use and offers the powerful features needed for complex VLSI circuits. One of the most important and useful features of the CAD system is the Design Audit tool. The Design Audit tool allows early detection and correction of design problems, checks for gated and asynchronous loops, lists all flip-flop preset and clear signals, and identifies potential testing difficulties. The simulator provides the ability to more quickly and accurately verify both the logic and timing requirements. Another important feature is the design-for-testability tools that alleviate the usually laborious task of generating high fault-coverage vectors. Automatic placement and routing help assure that even the most complex circuits are properly interconnected and optimally laid out.

The AT&T CAD system has demonstrated a very high first-time success rate on custom cell-based designs. The tools facilitate the design of circuits that push the limit of technology, both in gate-count and performance.

You can use AT&T's powerful CAD system and do the entire design at an AT&T Design Center. Or if you prefer to work at your own site, AT&T can help. Our cell library is supported on commercially available CAD systems. You can also use AT&T CAD tools through a licensing agreement or through a dial-up link to an AT&T Design Center.

The following is a list of AT&T's CAD tools:

CAD Tools

- SCHEMA – allows schematic entry and automated netlist generation
- VIEW*logic* WORKVIEW 5150 – a commercial schematic-capture tool used as an alternative to SCHEMA (only used with AT&T's cell library)
- FDS – synthesizes complex functions (see section 10 for more detail)
- MOTIS – provides logic, timing, and fault analysis for complete chip design
- MISL – generates test vectors from high-level language
- ALERT – detects design flaws, such as races, glitches, asynchronous loops, etc.
- TESTPILOT – designs for testability system using scan path method
- CRITIC – analyzes performance of individual circuit paths
- ADVICE (SPICE-like circuit simulator) – provides transistor-level simulations
- LTX2 – produces optimum chip layout with respect to chip size and performance
- GOALIE – extracts layout connectivity and device parasitics
- GRED – allows interactive layout editing
- LARC – provides layout design rule checking
- VAUDIT – detects potential hazards in test vectors
- TPG2 – program for automatic test program generation
- IKOS – a commercial hardware accelerator used as an alternative to MOTIS
- AGSIM – accelerated MOTIS simulator using AT&T's hardware accelerator board
- HASTEN – AT&T interface to the ZYCAD hardware accelerator used as an alternative to MOTIS

Workstation Support

In addition to supporting AT&T's CAD tools on the SUN workstation, AT&T continues to enhance the support of leading workstation platforms. The schedule is shown as follows.

• SUN workstation with VIEW*logic* schematic capture	Use with AT&T's cell library only	now
• Daisy Workstation	Schematic capture and logic simulation	now
	Timing simulation with backannotation	end of 4th quarter, 1989
• Valid Workstation	Schematic capture and logic simulation	end of 4th quarter, 1989
	Timing simulation with backannotation	end of 1st quarter, 1990
• Mentor Workstation	Schematic capture and logic simulation	now
	Timing simulation with backannotation	end of 2nd quarter, 1990

Design Methodology

All AT&T's cell-based designs follow the structured design methodology illustrated in Figure 1. Extensive reviews are held at various points during the design cycle to help ensure the quality of the designs. Adherence to the milestone verifications, simulations, reviews and tests has yielded a very high first-time success rate.

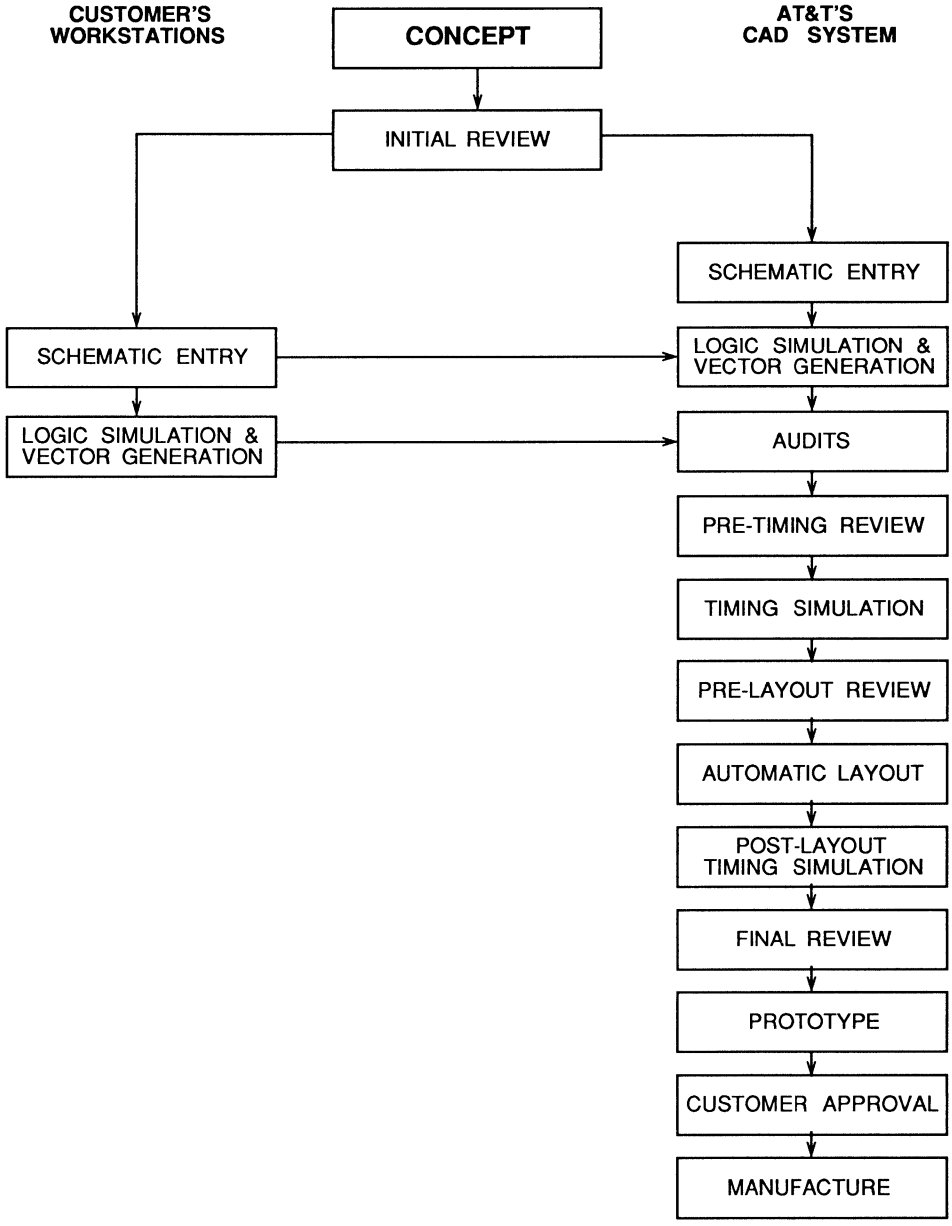

Figure 1. Design Cycle

Design Considerations

Section 2

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The standard cells in this catalog are available in two layout styles. In one style, the cells are made as small as possible. In the other style, cells are optimized for performance and as a result occupy more area than the small cells. The contrast is illustrated below:

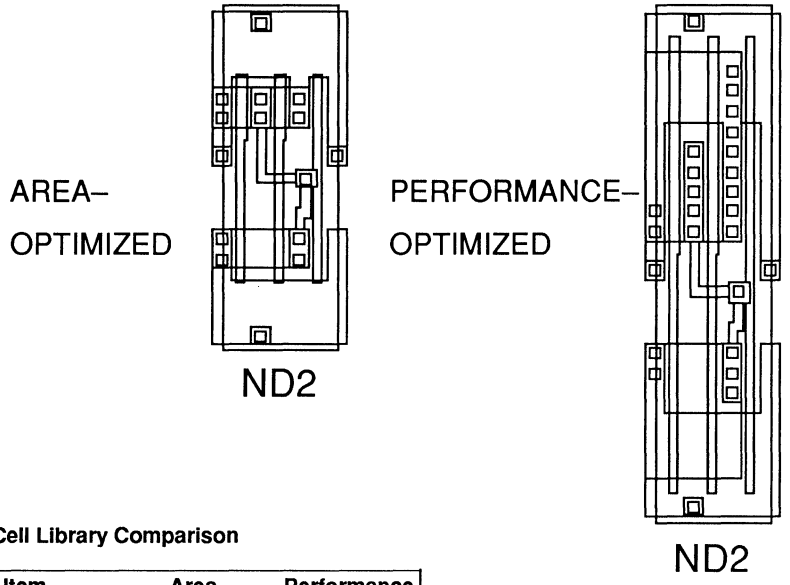

Table 1 - Cell Library Comparison

Item	Area-Optimized	Performance-Optimized
Cell Height	32.6 µm	48.9 µm
Grid Pitch (Unit for Cell Width)	3.6 µm	3.6 µm
P-Transistor:		
Mask Length	1.0 µm	1.0 µm
Mask Width	3.7 µm	18.1 µm
N-Transistor:		
Mask Length	0.9 µm	0.9 µm
Mask Width	3.7 µm	12.8 µm

The two libraries allow you to make trade-offs between performance and chip size in your design. These trade-offs are discussed in the sections that follow.

Nominal propagation delays are quoted in the 0.9µm Standard-Cell Library. To determine exact delays under other conditions, the ADVICE (AT&T's version of SPICE) simulation program should be used with the following conditions:

Table 2. Conditions for Simulations

CONDITIONS FOR SIMULATIONS			
CASE	TEMPERATURE	PROCESS FILE	POWER SUPPLY
Worst-Case Fast	0 °C	APROHC.DAT	5.5 V
Nominal	25 °C	APRONC.DAT	5.0 V
Worst-Case Slow	100 °C	APROLC.DAT	4.5 V

Throughout this catalog, "temperature" always refers to *junction* temperature and not the ambient. Junction temperature is generally higher than the ambient because the package acts as an insulator and impedes the dissipation of heat from the silicon to the ambient environment. The difference between the junction and ambient temperatures is dependent on the amount of power the device dissipates, the package type, and the amount of air circulation in the surrounding environment.

The temperature used in worst-case simulations is application-dependent. The range 0 ° C to 100 ° C is common; however, the minimum and maximum limits are -40 ° C to 125 ° C.

An alternate method to determine worst-case propagation delays (although not as accurate as running ADVICE) is to use de-rating factors. A de-rating factor is simply a multiplier of the nominal delay:

$$\tau = \tau_{NOMINAL} \times D_{TV} \times D_P$$

where

D_{TV} is the derating factor for temperature and voltage.

D_P is the derating factor for process variation.

These derating factors for 0.9µm CMOS are found in Tables 3 and 4:

Table 3. Derating for Processing

PROCESS CONDITIONS	DERATING FACTOR
Slow	1.26
Nominal	1.0
Fast	0.83

Table 4. Power Supply and Temperature Derating

TEMPERATURE °C	POWER SUPPLY VOLTAGE (V_{DD}) 4.50 V	4.75 V	5.00 V	5.25 V	5.50 V
-40	0.81	0.77	0.74	0.72	0.70
0	0.98	0.94	0.90	0.87	0.85
25	1.09	1.04	1.00	0.96	0.94
85	1.33	1.28	1.23	1.18	1.14
100	1.39	1.33	1.28	1.23	1.18
125	1.48	1.41	1.35	1.31	1.26

The recommended maximum operating conditions and absolute maximum ratings for the 0.9µm CMOS library and technology are as follows:

RECOMMENDED MAXIMUM OPERATING CONDITIONS FOR 0.9µm CMOS

Power Supply Voltage	$V_{DD} - V_{SS} = 5$ V
Input Voltages	($V_{SS} - 0.3$ V) to ($V_{DD} + 0.3$ V)
Junction Temperature	-40 °C to 125 °C

ABSOLUTE MAXIMUM RATINGS FOR 0.9 µm CMOS

Power Supply	$V_{DD} - V_{SS} \leq 7.0$ V
Input Voltage	V_{SS} to V_{DD} (for 6.1 V < $V_{DD} - V_{SS} \leq 7.0$ V)
Storage Temperature	-40 °C to 125 °C

The most accurate way to estimate the power dissipation of a custom CMOS IC is to develop an LSL (i.e., netlist) and a complete test vector set, and then let the MOTIS3 circuit simulator do the calculation for you. However, often you would like to know well beforehand how much of your board power budget to allocate to your proposed custom device. It is for this reason the following worksheet was developed; ***it should only be used as a guideline.***

AC Power

CMOS typically dissipates very little DC power. Most of the power dissipation arises from current required to repeatedly charge up and discharge transistor gates and parasitic capacitances. Accordingly, the expression for the AC power dissipation is:

$$P = C \times V^2 \times F$$

where

C = The total capacitance being charged and discharged.

V = The power supply, typically the upper limit for this calculation.

F = The frequency at which the capacitance is being charged and discharged.

Calculating the AC Power for Internal Gates

Estimating the AC power for the chip's internal logic gates is straightforward. The equation for the calculation is:

$$P_{Internal} = PG \times N \times F \times A$$

where

PG = Power per gate. This is the approximate power the average primitive logic gate (with fan-out of 3) dissipates at a specified clock frequency. This factor for the two libraries is:

5μW /gate/MHz for the area-optimized cells and

8μW /gate/MHz for the performance-optimized cells.

N = The total number of gates. The factors listed above assume that you are going to use equivalent, primitive logic gate count to do this estimate. N represents the total number of those gates.

F = The operating clock frequency.

A = The activity of the circuit. This term is an attempt to acknowledge that not all of the data in the circuit is changing at all times. This, of course, is heavily dependent on the application.

As an example, 5,000 gates in a synchronous design being clocked at 8MHz while using the area-optimized cells dissipate:

$$P_{Internal} = 5\,\mu W \times 5{,}000 \times 8\ MHz \times 0.2 = 40\ mW$$

assuming a 20% activity factor.

Estimating the AC Power for the Output Buffers

Another important component of the total power dissipation can be attributed to the chip's output capacitances. Here, the power is calculated as:

$$P_{External} = V_{DD}^2 \times C_L \times F \times A$$

where

V_{DD} = The upper limit on the allowed value for the power supply, typically 5.5 V

C_L = The sum of all capacitances on all chip outputs

F = The maximum frequency at which the outputs change. Normally, one half of the clock frequency.

A = The % activity of the output nodes. This may or may not be the same as the internal activity factor, depending on the application and the circuit.

DC Power

Certain CMOS circuits, by necessity, dissipate DC power. The most common of these are CMOS input buffers that convert TTL levels at the input of the chip to CMOS levels internally. The catalog pages describing these buffers include power information. It is suggested that you refer to those pages when considering power, because the DC power dissipated by the input buffers can turn out to be significant, depending on your buffer selection and your requirements.

If you are having some special circuitry built for you, it may also need to dissipate some DC power. Again, this dissipation can be important to include in the chip power calculation, especially if you have a tight power budget.

Total Chip Power - A Summary

In summary, there are three important contributors to the power dissipation of a CMOS IC that should be included when making an early estimate:

- The AC power dissipated by the internal gates
- The AC power dissipated by the output capacitance
- The DC power dissipated by various 'unusual' circuits, most notably the TTL compatible input buffers.

It is worth repeating that the MOTIS3 circuit simulator makes an accurate calculation of the chip AC power. The techniques presented in this section should only be used for estimation.

The following design practices are suggested to obtain the highest possible performance:

- Use the performance-optimized library.
- Keep the logic-gate depth shallow between latch points.
- Use low fan-in logic gates. (Fan-in is defined as the number of inputs. For example, an ND2 has a fan-in of 2; an NR4 has a fan-in of 4.) If you are using AT&T's FDS to synthesize combinatorial logic, limit the MAX_FANIN variable to 2 or 3.
- Plan your chip architecture to do as much parallel processing as possible.
- Minimize the occurrence of strings of alternating NANDs and NORs.
- Avoid the use of high-drive buffers when driving a low fanout.
- Avoid circuit designs that have highly loaded gates in the critical path. A gate delay increases as the capacitive load is increased on the output of the gate. The primary sources of load capacitance are routing capacitance and the capacitance of the transistors on the gates being driven.
- Duplicate logic to reduce fanouts.
- Use fast adder design techniques - for example, carry look-ahead.
- Avoid placing heavy loads on flip-flops and latches. On most flip-flops and latches, the Q and QN outputs are unbuffered. Since QN is derived from Q, a high fan-out on QN slows down Q even if Q is lightly loaded.
- Some of the cells in the library are available with higher drive capabilities - for example, an ND2H has twice the drive capability of the ND2. An ND2S has four times the drive of the ND2. These higher-power cells should only be used to drive high fanouts.
- In general, small macrocells run faster than large ones. For example, two $1,024 \times 8$ SRAMs run faster than one $1,024 \times 16$ SRAM. In a similar manner, a block of logic implemented with many PLAs runs faster than if it were implemented with one large PLA.

The following design practices are suggested to minimize chip area:

- Use the area-optimized library.
- Design with repeated, regular subcircuits whenever possible. In layout, each of these subcircuits can be placed and routed very efficiently and then repeated to form a larger circuit.
- If you are using AT&T's FDS to synthesize combinatorial logic, experiment with the MAX_FANIN option. By varying MAX_FANIN from its default value of 9, you may be able to synthesize smaller versions of the intended logic.
- Whenever possible, use both Q and QN signals (which have been made available on each flip-flop and latch) to form inversions.
- Apply DeMorgan's theorem to minimize the use of inverters.
- Direct translations from TTL diagrams can be inefficient. Instead, design the logic directly from the cell library.
- In general, do not connect any cell input directly to VDD or VSS. Instead, find the cell with the proper number of inputs and function, or have a new cell designed.
- If you need a flip-flop with a multiplexer on the input, consider using the scan-test version (i.e., the 'FLxSxxX' variety of cells.)
- Experiment with PLAs and ROMs. In some cases, logic implemented with a PLA or a ROM can offer a significant size advantage over a standard-cell implementation.
- Be aware of the overhead present in macrocells. For example, a single 10K SRAM occupies significantly less area than ten 1K SRAMs, because of the latches, clock drivers and decoders in each SRAM block.
- A single large block is better than many small blocks doing the equivalent function for another reason: in layout, there is often a 'moat' of inefficient routing around each block. This is because the terminal positions on the block cannot be rearranged to make the routing more dense. Therefore, when planning a chip architecture for minimal area usage, use a few very large blocks rather than many small blocks.

Presented in this section is a simple technique to do an early estimate of the size of a prospective standard-cell chip. It is intended for use early in the design to make system architecture-related or partitioning decisions. The only way to ***really*** determine a chip size is to lay it out. Using the technique below gets you only to within ± 10% per side.

Using Grid Count to Estimate Chip Size

The basic unit used for estimating chip size is the standard-cell grid. The width of a standard cell is measured in grids; for example, a 4-input NAND gate is 5 grids wide. An approximate chip size can be easily calculated from the total number of grids in the circuit.

$$S = \sqrt{k_1 \times N^2 + k_2 \times N + 1.2 \times A_{SP}} + H_B$$

where

S = Length of one side of the chip (step and repeat) in thousandths of an inch (mils).

N = The total number of grids in the LSL.

k_1, k_2 = Constants that account for routing and overhead in this chip area calculation. These constants are different for the types of cells and layout styles used.

For the area-optimized cells:

$$k_1 = 5.0 \times 10^{-6}, k_2 = 0.4$$

For the performance-optimized cells:

$$k_1 = 5.0 \times 10^{-6}, k_2 = 0.5$$

A_{SP} = The area of any special blocks, for example RAM or PLA. The area information for these can be obtained from the appropriate data sheets in this catalog.

H_B = The height of the buffer ring that surrounds the chip, including power bus, saw-grid, and alignment features. The value of H_B depends on whether or not you are pad-limited:

For a pad-limited chip:

$$H_B = 50 \text{ mils.}$$

For a chip that is not pad-limited:

$$H_B = 31 \text{ mils.}$$

For example, an area estimate for a chip requiring 20,000 grids using the area-optimized standard cells is determined as follows:

$$S = \sqrt{5.0 \times 10^{-6} \times 20{,}000^2 + 0.4 \times 20{,}000} + 31 = 131 \textit{ mils} \pm 10\ \%$$

A more complete relationship between grids and chip size (non-pad-limited) is illustrated in Figure 1.

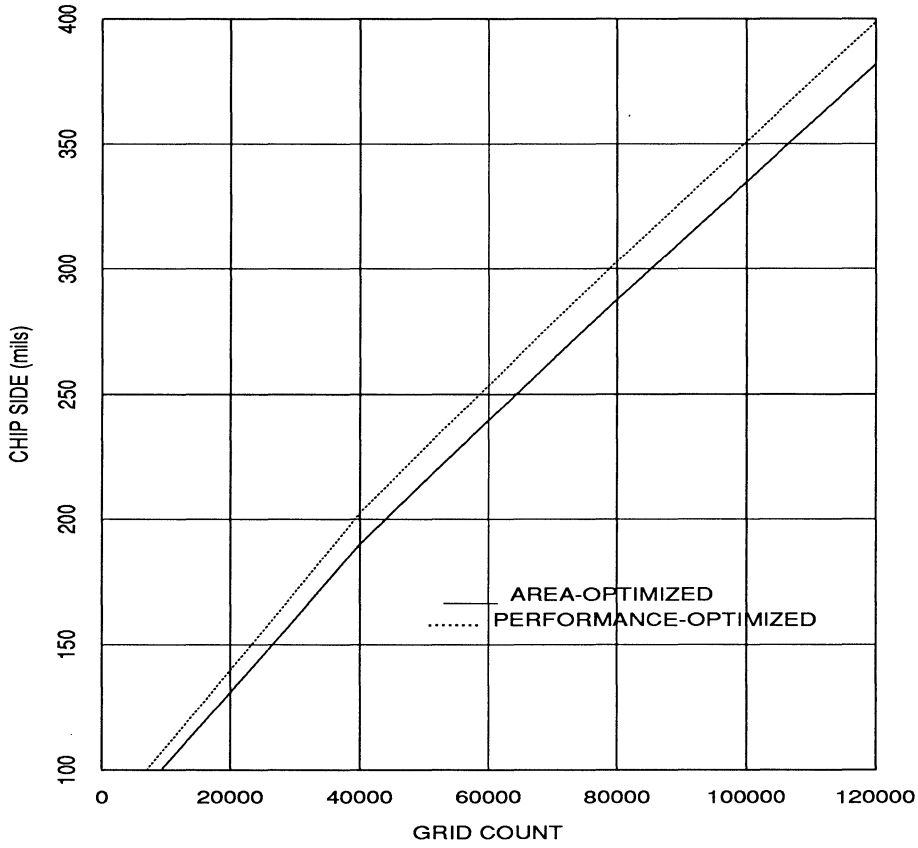

Figure 1. Chip Size as a Function of Grid Count

Estimating the Grid Count Before LSL is Available

A grid count is not always available when a chip-size estimate is desired. Early in the design, the only indication of the complexity of the chip is often a count of the number of equivalent logic gates. To help you convert from gates to grids or MOS transistors, the appropriate conversion factors are shown in the following table.

Table 5. Standard-Cell Conversion Factors

	Logic Gates	Grids	Transistors
1 Logic Gate =	1.0	2.6	4.0
1 Grid =	0.38	1.0	1.5
1 Transistor =	0.25	0.67	1.0

Chip Size Limits

There are limits on the range of practical chip sizes. At the lower end of the range, the chip size is limited by the placement of the bond pads on the chip and the allowed length of the wire bonds. The more pins, the larger the minimum chip. At the upper end of the range, limits are imposed by the physical dimensions of the package itself.

The range of minimum and maximum chip sizes for standard packages is summarized on the following page.

Table 6. Minimum and Maximum Chip Sizes

Package Type	# Pins	Minimum (mils)		Maximum (mils)	
		X	Y	X	Y
Plastic DIP	40	125	125	380	380
	32	110	110	380	380
	28	105	105	330	460
	24	95	95	360	440
	20	90	90	140	300
	18	80	130	130	280
	16	80	80	150	340
Plastic, Leaded Chip Carrier	100	230	230	450	450
	84	200	200	405	405
	68	180	180	410	410
	44	130	130	350	350
Plastic SOJ	28	105	105	190	350
	20	90	90	190	350
	16	80	80	190	220
Plastic, Quad, Flat Package	164	380	380	460	460
	132	285	285	380	380
	100	240	240	405	405
	84	200	200	340	340

Package Type(1)	# Pins	Minimum (mils)	
		X	Y
Ceramic DIP	48	140	140
	40	125	125
	32	110	110
	28	105	105
	24	95	95
	16	80	80
Ceramic Pin-Grid Array	224	450	450
	180	370	370
	149	315	315
	133	285	285
	125	270	270
	120	265	265
	100	230	230
	68	175	175
	64	165	165

Notes:

1. Because of wide variations in package cavity sizes, chip sizes for ceramic packages other than minimum are available upon request.
2. See Section 3 for more detailed packaging information.

CAD Support Files

A complete set of CAD support files for the 0.9µm CMOS Standard-Cell Library is available through the distribution of SysCAD and ADS (AT&T Design System). These files support the use of several CAD programs for schematic-capture, logic and timing simulation, and chip layout. Please contact your AT&T representatives for more information.

Packaging Summary

Section 3

Contents - Section 3

AT&T recognizes that packaging has a dramatic effect on device and system performance. With today's accelerated development of smaller, more powerful devices, packaging technology has been compelled to react swiftly. Higher power ranges and tighter packaging densities are forcing engineers to re-evaluate the effectiveness of older, more traditional packaging technologies and styles.

Through the research efforts of AT&T Bell Laboratories, we are spearheading the development and acceptance of new packaging options in order to meet future demands for state-of-the-art devices and system applications. Because of our ongoing development efforts, we suggest that frequent inquiries be made regarding availability of new packaging options. Some of our development plans include: high-pin-count, JEDEC, plastic, quad, flat packs (PQFP); EIAJ, plastic, quad, flat packs (PQFP); high-pin-count, fine-pitch, ceramic, leaded chip carriers (CLCC); and ceramic, quad, flat packs (CQFP). In addition, AT&T offers assistance in resolving your special packaging needs.

Packages such as chip carriers, pin-grid arrays, and small-outline configurations bridge the gap of advancements in chip technology and the developments in automated circuit-board assembly processes to lower circuit-board costs and enhance system performance. Currently, we offer a choice of packages in both through-hole and surface-mount technologies. These packages accommodate high packaging densities with proven reliability.

As a member of JEDEC and its committees, AT&T has been instrumental in setting the standards for new packaging technologies. Our ongoing participation in JEDEC is your assurance that many of our packages not only meet industry standards, but in some cases actually help establish those standards. Our devices are protected by our conformance with the United States Semiconductor Chip Protection Act of 1984.

All of our packaging support services, including sophisticated CAM systems and state-of-the-art assembly and testing procedures, enable us to provide "***total IC service***" to our customers. These qualities are what make AT&T a leader in integrated circuit technology and performance.

Following is the summary of package types currently available.

Through-Hole-Mount, Plastic Packages with 100-Mil Pin Spacing

Plastic DIP						
No.	Θ	Chip Size (mils)		Pin Inductance (nH)		Dimension
Pins	(°C/W)	Min	Max	Min	Max	(mils)
16	73	80×80	150×340	4	11	320×810
18	68	80×130	130×280	4	11	320×920
20	64	90×90	140×300	4	12	320×1040
24	57	95×95	360×440	5	14	615×1270
28	52	105×105	330×460	5	16	615×1470
32	49	110×110	380×380	5	18	615×1580
40	42	125×125	380×380	5	23	615×2070

Surface-Mount, Plastic Packages with 50-Mil Pin Spacing

SOJ						
No.	Θ	Chip Size (mils)		Pin Inductance (nH)		Dimension
Pins	(°C/W)	Min	Max	Min	Max	(mils)
16	90	80×80	190×220	4	9	355×408
20	85	90×90	190×350	4	9	355×508
28	75	105×105	190×350	4	11	355×708

Plastic, Leaded Chip Carrier						
No.	Θ	Chip Size (mils)		Pin Inductance (nH)		Dimension
Pins	(°C/W)	Min	Max	Min	Max	(mils)
44	55	130×130	350×350	4	10	695×695
68	45	180×180	410×410	7	13	995×995
84	43	200×200	405×405	9	17	1190×1190
100	40	230×230	450×450	9	18	1395×1395

Surface-Mount, Plastic Packages with 25-Mil Pin Spacing

Plastic, Quad, Flat Package						
No.	Θ	Chip Size(mils)		Pin Inductance(nH)		Dimension
Pins	(°C/W)	Min	Max	Min	Max	(mils)
84	68	200×200	340×340	5	8	810×810
100	56	240×240	405×405	6	10	910×910
132	42	285×285	380×380	8	13	1100×1100
164	40	380×380	460×460	10	17	1300×1300

Notes:

1. Θ (° C/W) is in still-air-ambient.
2. Capacitance: maximum 5 pF/pin (not including buffer and pad).
3. Resistance: pin-to-pad maximum 0.15 Ω/pin (nominal about 0.09 Ω).
4. Inductances are estimated worst-case values.
5. The information listed above is meant to be used as a guideline only. For more detailed information regarding your requirements, please consult your AT&T representative.

Summary of Package Types: Ceramic

Through-Hole-Mount, Ceramic Packages with 100-Mil Pin Spacing

Ceramic DIP						
No.	θ	Chip Size (mils)		Pin Inductance (nH)		Dimension
Pins	(°C/W)	Min	Max	Min	Max	(mils)
16	64	80x80		4	11	325x815
24	56	95x95		9	15	620x1212
28	51	105x105	See	5	14	620x1412
32	46	110x110	Note	5	18	620x1625
40	35	125x125	(6)	5	23	620x2020
48	31	140x140		6	25	620x2420

Ceramic Pin-Grid Array						
No.	θ	Chip Size(mils)		Pin Inductance(nH)		Dimension
Pins	(°C/W)	Min	Max	Min	Max	(mils)
64	41	165x165		6	16	1000x1000
68	34	175x175		6	17	1100x1100
100	24	230x230		7	20	1320x1320
120	24	265x265	See	7	20	1320x1320
125	24	270x270	Note	7	20	1320x1320
133	24	285x285	(6)	7	20	1320x1320
149	17	315x315		8	23	1560x1560
180	17	370x370		8	23	1560x1560
224	17	450x450		8	23	1560x1560

Surface-Mount, Ceramic Packages with 50-Mil Pin Spacing

Ceramic Chip Carrier - Leaded						
No. Pins	θ (°C/W)	Chip Size (mils) Min	Chip Size (mils) Max	Pin Inductance (nH) Min	Pin Inductance (nH) Max	Dimension (mils)
68	30	180×180	See	7	13	1080×1080
100	20	230×230	Note (6)	9	18	1365×1365

Socket-Mount, Ceramic Packages with 50-Mil Pin Spacing

Ceramic Chip Carrier - Leadless						
No. Pins	θ (°C/W)	Chip Size (mils) Min	Chip Size (mils) Max	Pin Inductance (nH) Min	Pin Inductance (nH) Max	Dimension (mils)
68	30	180×180	See	6	12	996×996
100	20	230×230	Note (6)	8	17	1281×1281

Notes:

1. θ (°C /W) is in still-air-ambient.
2. Capacitance: maximum 5 pF/pin (not including buffer and pad).
3. Resistance: pin-to-pad maximum 0.15 Ω/pin (nominal about 0.09 Ω).
4. Inductances are estimated worst-case values.
5. For ceramic packages, minimum chip dimensions are set by bond-pad spacing rules and wire-bond rules. Maximum chip dimensions are set by ceramic-package-layout rules, or in the case of very large chips, by reticle technology.
6. Because of wide variation in package cavity sizes, chip sizes other than minimum are available upon request.
7. The information listed above is a guideline only. For more detailed information regarding your requirements, please consult your AT&T representative.

Reliability & Quality

Section 4

Contents - Section 4

Introduction

In all AT&T products and services, quality is a major thrust. AT&T's policy is to provide products and services that meet the quality expectations of our customers. In addition, AT&T actively pursues ever-improving quality through programs that enable each employee to do the job right the first time. Each employee is a part of the system that allows AT&T to provide high-quality products with long-term reliability.

AT&T ASIC devices are no exceptions to the rule when quality and reliability are considered. The increasing demands on chip complexity and the constantly shrinking design rules dictate the need for defect-free product. This section describes the procedures adhered to during the design, manufacture, and shipment of AT&T ASIC devices which help to guarantee the highest quality and assure long term reliability.

It is often the case that quality and reliability are used interchangeably, but there is a subtle difference. A quality product is one which is designed to be manufactured to perform to a predetermined degree of excellence. In addition to being a quality product, however, a reliable product is one which performs correctly *and* does not produce failures in time which exceed some predetermined limits. It will become apparent to the reader that there is a *quality-by-design* concept evident in not only the AT&T ASIC designs but also in the manufacture of their prototypes. This concept further translates into the reliability program AT&T uses to help assure customer product meets or exceeds customer needs.

Circuit Design, Prototype Fabrication & Product Manufacture

From the start of the chip design, quality is built into the process. The use of CAD tools along with a thoroughly precharacterized cell library helps to assure a high rate of design sucess. Moreover, each AT&T design engineer presents his or her final design in a *peer-design-review* format. During these design reviews, a large team composed of experienced designers review all aspects of the chip design. It is not until each design passes such a review that approval is given to generate masks for manufacture of device models.

Special engineering teams handle all aspects of the models' manufacture, from the generation of mask sets, through the wafer fabrication, to the ultimate assembly of packaged devices. Masks are manufactured in the AT&T mask shop, which boasts a reputation for delivering the highest quality masks. To maintain the high quality of the masks, special protective layers called pellicles are used. Pellicles are mounted on the front and back surfaces of the masks to prevent any debris from being replicated on the wafers during the photolithography processes. *MASKVIEW*, a CAD tool developed by AT&T, can be used at any time to verify the correctness of the masks against the databases used to generate them. This further helps the job to be done right the first time, thus saving time and money.

The prototype (or "prove-in") lots are fabricated in AT&T cleanrooms; these are the same cleanrooms in which the final proven-in devices will be manufactured. This concept of using manufacturing facilities for prototype fabrication helps to provide for an easier transition into product manufacture. There are no 'surprises' that might be encountered moving from one fab line to another. One twenty-five-wafer lot is fabricated for each device prove-in. This lot provides wafers for prototype models on a quick turnaround basis. Twenty-four-hour engineering coverage helps to assure that these prove-in lots are processed as rapidly as possible and without problems. Parameters identified as important to the manufacture of the product lots are closely monitored for prove-in lots. Special test patterns which assess the electrical and cosmetic quality of the processing for each lot are tested once processing is completed. This information is used to generate databases describing the process quality over an extended period of time. In addition, this information is also used to quickly report process parameters to the fab lines since prove-in lots serve as *health-of-the-line* lots because they are processed more rapidly than production lots.

Any required failure-mode analysis of the prove-in lots is done by resident engineers who work closely with both the device prove-in engineers and AT&T product engineers. Models are assembled from prove-in wafers. They are tested and then shipped to the customer for evaluation. The protection of masks, fabrication of prove-in lots in the manufacturing environment, close attention to process parameters, and expert failure-mode analysis are some of the aspects that are built into device prove-in to help assure the ultimate high-quality of the code in manufacture.

Defect density and electrical resistivity measurements are made on each wafer before it is used for the manufacture of an integrated circuit. Mask alignment, critical dimensions and pattern quality are measured and/or inspected on wafers at the photolithography operations. Final sizes are measured and the quality of patterns transferred after etching is inspected. Polysilicon, dielectric materials, and metallization levels are monitored for defect densities, particle checks, and thickness uniformity. These in-process monitors are reviewed on a lot-by-lot basis. In addition, these process monitors are also used to maintain the fabrication lines at peak operating levels by identifying and correcting any problems as they occur. Electrical parameters are measured on sample wafers from each completed lot. Certain specifications, especially relating to electrical channel lengths, must be met before a lot can be shipped for package assembly.

In package form, a process referred to as burn-in is performed to weed out potentially weak devices. During burn-in, high temperature and high voltage are used to stress the devices and accelerate the failure rate. The circuit can be clocked at either 100 kHz or 1 MHz to additionally stress the device during burn-in. Burn-in accelerates the initial dropout ('infant mortality' rate) and helps to ensure that potentially unreliable devices do not find their way into customer product.

AT&T ships devices under a reliability program to meet customer requirements, typically 100 FITS at 40 years. This assurance of reliability, however, cannot occur until the integrated circuit family (package type, process technology, etc.) has undergone a technology qualification which achieves these high levels of reliability. Such technology qualifications are the responsibility of the appropriate AT&T design organizations. Once a process technology is qualified, changes made to the process require that some re-qualification testing be done.

To begin the qualification procedures, samples are processed, tested, screened, and inspected in the usual manner. This means that no special attention is given to the samples that would distinguish them from ordinary product. Samples used for qualification are composed of approximately equal numbers from three wafer-processing lots. When the devices have been stressed and then tested, an electrical failure is defined as a device which does not meet data sheet or end-of-life test specifications. It is imperative that all electrical failures are confirmed for a second time and then analyzed for their causes of failure.

Intermediate Qualification

An intermediate qualification of a new process, demonstrating 300 FITS in 10 years, can be done to allow the shipment of product prior to devices passing a full qualification. Devices are shipped under this intermediate qualification on a limited basis with the requirements that customers are notified of this special status and that intermediate devices are codemarked appropriately. Intermediate devices are shipped for an amount of time limited to six months from the initial shipment of coded devices.

Full Qualification

A new process technology for MOS devices in plastic packages is considered to be fully qualified when all AT&T IC Reliability Standards have been met. The successful completion of all appropriate qualification procedures demonstrates a 100 FIT, 40-year life for product fabricated on a particular wafer process line. Each fab line is separately qualified for each process technology. This helps assure that the customer receives the identical quality product regardless of its location of manufacture.

Changes made to a qualified process technology must be followed by re-qualification testing. Although it is not necessary that all qualification tests be repeated, a subset of the original tests is done for passivation, metallization, and diffusion changes.

New package qualification, using chips from qualified process technologies, requires additional tests. Since AT&T has package assembly locations throughout the world, each location is fully qualified to help assure identical quality of all products to our customers.

Reliability qualification tests and test methods used by AT&T are tabulated on the following page.

Qualification Tests

Test	Test Description	Method Note(1)
1. LT-1 or LT-2	High Temp. Op. Bias, 125 °C High Temp. Op. Bias, 150 °C	M-1005
2. CL	CLASS Note (2)	L-757214
3. BH	Temp.-Humidity-Bias	A-497337
4. SB	Steam Bomb	PI-12.163
5. TC	Temp. Cycling	M-1010
6. TS	Thermal Shock	M-1011
7. MR	Moisture Resistance	M-1004
8. LK	Gross/Fine Leak	M-1014
9. SA	Salt Atmosphere	M-1009
10. WV	Internal Water Vapor	M-1018
11. RT	Low Temp. Aging	L-757203
13. SE	Soft Error Rate	M-1032
14. PS	Photo Sensitivity	Note (3)
15. FL	Flammability & O_2 index	UL 94 & ASTM 2863-77
16. SR	Solvent Resistance	M-2015
17. IV	Internal Visual	M-2014
18. PD	Physical Dimensions	M-1016
19. SD	Solderability	M-2003
20. MS	Mechanical Shock	M-2002
21. VF	Variable Freq. Vib.	M-2007
22. CA	Const. Acceleration	M-2001
23. SQ	Mechanical Sequence	Note (4)
24. LI	Lead Integrity	M-2004
25. BS	Bond Strength	M-2011
26. DS	Die Shear Strength	M-2019
27. XR	X-ray	M-2012
28. TQ	Lid Torque	M-2024
29. ES	ESD	X-19435
30. LU	Latch-up	L-757185

NOTES:

1. M-XXXX.X denotes test method as specified in MIL-STD-883.
2. CLASS (AT&T-BL L-757214) Component and Lead Assembly Simulation Sequence
3. Applies only to product packaged in white ceramic or white plastic.
4. Mechanical shock, variable frequency vibration, constant acceleration and gross/fine leak tests performed in sequence with the same samples.

After the devices meet the AT&T's qualification requirements, they are committed to production. Their continued long-term reliability is assured to be at the maximum failure rate of 100 FITS after 40 years of life. A comprehensive reliability monitoring program administered by AT&T guarantees that customer product is maintained at this reliability level.

The AT&T reliability testing program provides for two-level testing. Level 1, performed on a six-weeks basis, is equivalent to 40 years of life. Level 2, performed on a weekly basis, provides on-going reliability data ensuring 300 FIT, 10 year life. This difference does not imply a variation in the reliability levels of shipped customer product. Since all product is manufactured in the same rigid manner, level 1 provides data to evaluate devices against long-term goals, while level 2 provides early warning should a reliability problem occur.

To help ensure that all products are completely covered under this reliability program, products are grouped together by basic design style and function. These groupings, or families, include memories, microprocessors, digital signal processors, codec/analog devices, and ASIC devices. Further division in each family occurs as individual test groups are designated based on those factors likely to be affected by each test performed. Examples of individual test groups are wafer-fab lines, package materials, package types, and package-assembly lines.

Some testing times are very long, as previously noted. In some cases, an entire week's shipment might ordinarily be delayed pending the completion of testing of some reliability samples. To avoid this situation and to help assure the best delivery to customers, early shipment privileges are given to those testing groups which consistently demonstrate good reliability levels. Early shipment qualification is based on a weighted average of the four most recent lots. This level is continually monitored with each new test; early shipment privileges can be lost if the weighted average exceeds a predetermined limit. There will be no compromise in reliability assurance for the sake of early shipment.

Most product is sampled under the 'normal sampling' procedure. This means that a representative device is chosen from the test group to represent all other codes in the same test group. In some cases, however, codes in a test group may be tested on a lot-by-lot basis because previous samples exceeded the predetermined failure limit. Each device in the test group must individually pass the reliability test.

Devices which do not pass reliability testing undergo failure analysis to determine if they are truly reliability failures. Full characterization of all defectives is done to evaluate failure modes and causes. These characterizations impact on product reliability and future product shipping status.

Data, segregated by families and testing groups, is generated and reviewed on a weekly and quarterly basis for both level 1 and level 2 testing. This data allows all samples to be traced back to wafer-fab-line and package-assembly location.

Summary

AT&T is committed to providing our customers with the highest quality product. ASIC devices are designed and manufactured to the highest quality; their long-term reliability is assured to be less than or equal to 100 FITS in 40 years of life. This is accomplished by design, process, and product engineers working together. In addition to these human resources, the finest software, highly innovative procedures, state-of-the-art manufacturing facilities, and good discipline contribute to the high-quality product available to our customers.

I/O Buffers

Section 5

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I/O Buffer Selection Guide

The AT&T 0.9 μm CMOS Standard-Cell Library offers a rich selection of circuits to interface your chip with the outside world. This selection guide helps you to quickly see what is in the library, and allows you to select the circuit that best fits your needs.

There are three types of I/O buffers in the library, namely:

- Input Buffers
- Output Buffers
- Bi-directional Buffers

Input Buffers

Each input buffer cell contains a bonding pad, power and ground busses, an ESD protection network, and the appropriate circuitry. Table 1 is a summary of the input buffers available in the 0.9 μm CMOS library.

Table 1. 0.9 μm CMOS Input Buffers

INPUT BUFFER TYPE	NAME	PROPAGATION DELAY *
Non-Inverting TTL-Level with Hysteresis	BIH05 BIH10 BIH20	5 ns 10 ns 20 ns
Inverting CMOS-Level	BIM02 BIM03 BIM05 BIM10	2 ns 3 ns 5 ns 10 ns
Non-Inverting TTL-Level	BIN04 BIN06 BIN10 BIN15 BIN20 BIN25	4 ns 6 ns 10 ns 15 ns 20 ns 25 ns
ESD Protection Network Only	BIP02	2 ns
Inverting CMOS-Level Schmitt Trigger	BIS07	7 ns
Inverting TTL-Level Schmitt Trigger	BIT06 BIT11	6 ns 11 ns

* Input buffer delay under the following conditions; slow processing, T = 125 ° C, V_{DD} = 4.5 V and a load capacitance of 5 pF.

Input Buffers With Pull-Ups

Each input buffer can have a P-transistor pull-up attached to the input pad. Four possible minimum-value equivalent resistances are available: 20, 50, 100, and 200 KΩ. Table 2 lists current drawn from an external source by the pull-up under various conditions. The six entries for each pull-up value correspond respectively to: maximum current with AT&T guard-band, maximum current under normal operation, maximum current during test, minimum current during test, minimum current under normal operation, and minimum current with AT&T guard-band.

Table 2. Pull-Up Resistor Current Limits

Pull-up Value	Conditions				
	V_{DD}	Process	Temp.	V_{INPUT}	I_{PULL}
20K	5.72 V	High Current	0° C	0 V	269 µA
	5.50 V	High Current	0° C		250 µA
	5.00 V	High Current	25° C		185 µA
	5.00 V	Low Current	85° C		103 µA
	4.50 V	Low Current	125° C		72.4 µA
	4.28 V	Low Current	125° C		64.6 µA
50K	5.72 V	High Current	0° C	0 V	117 µA
	5.50 V	High Current	0° C		109 µA
	5.00 V	High Current	25° C		79.8 µA
	5.00 V	Low Current	85° C		45.2 µA
	4.50 V	Low Current	125° C		31.6 µA
	4.28 V	Low Current	125° C		28.1 µA
100K	5.72 V	High Current	0° C	0 V	60.4 µA
	5.50 V	High Current	0° C		55.9 µA
	5.00 V	High Current	25° C		41.0 µA
	5.00 V	Low Current	85° C		23.3 µA
	4.50 V	Low Current	125° C		16.3 µA
	4.28 V	Low Current	125° C		14.5 µA
200K	5.72 V	High Current	0° C	0 V	30.7 µA
	5.50 V	High Current	0° C		28.4 µA
	5.00 V	High Current	25° C		20.8 µA
	5.00 V	Low Current	85° C		11.9 µA
	4.50 V	Low Current	125° C		8.26 µA
	4.28 V	Low Current	125° C		7.34 µA

Output Buffers

Each output buffer cell contains a bonding pad, power and ground buses, an ESD protection network, and the appropriate circuitry. The selection of output buffers available in the 0.9 µm CMOS Library is illustrated in Table 3 below:

Table 3. 0.9 µm CMOS Output Buffers

OUTPUT BUFFER TYPE	NAME	PROPAGATION DELAY *
Non-Inverting TTL-Level Open-Collector	BOC06	6 ns
	BOC08	8 ns
	BOC10	10 ns
	BOC15	15 ns
	BOC20	20 ns
	BOC30	30 ns
	BOC40	40 ns
	BOC80	80 ns
Non-Inverting CMOS-Level 3-state	BOM05	5 ns
	BOM10	10 ns
	BOM15	15 ns
Non-Inverting TTL-Level	BON06	6 ns
	BON08	8 ns
	BON10	10 ns
	BON15	15 ns
	BON20	20 ns
	BON30	30 ns
	BON40	40 ns
	BON80	80 ns
Non-Inverting TTL-Level 3-state	BOT06	6 ns
	BOT08	8 ns
	BOT10	10 ns
	BOT15	15 ns
	BOT20	20 ns
	BOT30	30 ns
	BOT40	40 ns
	BOT80	80 ns
Output Driver Only TTL-Level No Inherent Logic	BOX06	> 6 ns
	BOX08	> 8 ns
	BOX10	> 10 ns
	BOX15	> 15 ns
	BOX20	> 20 ns
	BOX30	> 30 ns
	BOX40	> 40 ns
	BOX80	> 80 ns

* Output buffer delay under the following conditions; slow processing, T = 125 ° C, V_{DD} = 4.5 V and a load capacitance of 50 pF.

Bi-Directional Buffers

A bi-directional buffer (I/O Port) consists of the combination of an input buffer and an output buffer. There are five families of bi-directional I/O buffers, distinguished from each other by having different pairings of input buffers with output buffers, as described in Table 4. The five bi-directional I/O families are summarized in Tables 5 and 6. The italicized terms *id* and *od* represent the propagation delays of the input and output stages, respectively.

Table 4. 0.9 µm CMOS Bi-Directional I/O Buffers

I/O Family	Input Buffer	Output Buffer	Reference
BH*id*C*od*	Non-Inverting ("BIH"-type)	Non-Inverting, Open Collector ("BOC"-type)	See Table 5.
BH*id*T*od*	Non-Inverting ("BIH"-type)	Non-Inverting, 3-State ("BOT"-type)	See Table 5.
BH*id*X*od*	Non-Inverting ("BIH"-type)	Output Driver Only ("BOX"-type)	See Table 5.
BM*id*M*od*	Inverting ("BIM"-type)	Non-Inverting, 3-State ("BOM"-type)	See Table 6.
BN*id*T*od*	Non-Inverting ("BIN"-type)	Non-Inverting, 3-State ("BOT"-type)	See Table 7.
BN*id*X*od*	Non-Inverting ("BIN"-type)	Output Driver Only ("BOX"-type)	See Table 7.

Table 5. BH*id*C*od*, BHidT*od* and BH*id*X*od* Bi-Directional Buffer Families

Input Buffer Delay (*id*)††	Output Buffer Delay (*od*)†					
	6 ns	8 ns	10 ns	15 ns	20 ns	30 ns
5 ns	BH05*06		BH05*10			
10 ns		BH10*08		BH10*15		
20 ns	BH20*06		BH20*10		BH20*20	BH20*30

† Output buffer delay under the following conditions: slow processing, T = 125° C, V_{DD} = 4.5 V and a load capacitance of 50 pF.

†† Input buffer delay under the following conditions: slow processing, T = 125° C, V_{DD} = 4.5 V and a load capacitance of 5 pF.

Table 6. BM*id*M*od* Bi-Directional Buffer Family

Input Buffer Delay (*id*)††	Output Buffer Delay (*od*)† 5 ns	10 ns	15 ns
2 ns	BM02M05		
3 ns	BM03M05	BM03M10	
5 ns	BM05M05	BM05M10	BM05M15
10 ns	BM10M05	BM10M10	BM10M15

† Output buffer delay under the following conditions: slow processing, T = 125° C, V_{DD} = 4.5 V and a load capacitance of 50 pF.

†† Input buffer delay under the following conditions: slow processing, T = 125° C, V_{DD} = 4.5 V and a load capacitance of 5 pF.

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Table 7. BN*id*T*od* and BN*id*X*od* Bi-Directional Buffer Families

Input Buffer Delay (*id*)††	Output Buffer Delay (*od*)† 8 ns	10 ns	15 ns	20 ns	30 ns	40 ns	80 ns
6 ns	BN06*08						
10 ns		BN10*10					
15 ns	BN15*08		BN15*15				
20 ns		BN20*10		BN20*20	BN20*30		
25 ns			BN25*15	BN25*20		BN25*40	BN25*80

† Output buffer delay under the following conditions: slow processing, T = 125° C, V_{DD} = 4.5 V and a load capacitance of 50 pF.

†† Input buffer delay under the following conditions: slow processing, T = 125° C, V_{DD} = 4.5 V and a load capacitance of 5 pF.

Bidirectional I/O Buffers with Pull-Ups

As with input buffers, each bidirectional I/O buffer can have a P-transistor pull-up attached to the pad. Refer to Table 2 for the resistor values available and their current limits.

Once buffer circuits have been selected on the basis of logic function, power, and speed, you are still faced with a choice of layout format. Each buffer circuit is available in two layout formats: *-D or -T* format layout. The format is indicated by the cell name suffix (e.g., BOM05D or BOM05T). Table 8 summarizes the characteristics of each layout style.

Table 8. 0.9 μm CMOS Buffer Layout Information

LAYOUT FORMAT	KEYWORD	CELL HEIGHT	CELL WIDTH (Cell Dependent)
D	Default	283.50 μm 11.16 mils	192.95 μm → 310.40 μm
T	Tall (Pad Limited)	522.90 μm 20.59 mils	175.00 μm

Before Layout. If it is known a chip design will not be pad-limited, pre-layout timing simulations may use the -D style buffers. If it is known a chip design will be pad-limited, pre-layout timing simulations may use the -T style buffers. If it is unknown whether a chip will be pad-limited or not, it is suggested that the -T style buffers be used anyway, as they have larger parasitic capacitances.

During Layout. Once chip layout begins, the choice of the right style of buffer (-D or -T) becomes very important. The following guidelines will help choose the correct buffer layout style, so that the smallest possible chip area may be obtained.

Non-Pad-Limited Chips - This includes chips with a small number of pins, or a very large gate count. The -D (or short) layout style is suggested, as it yields the smallest chip size (see Figure 1).

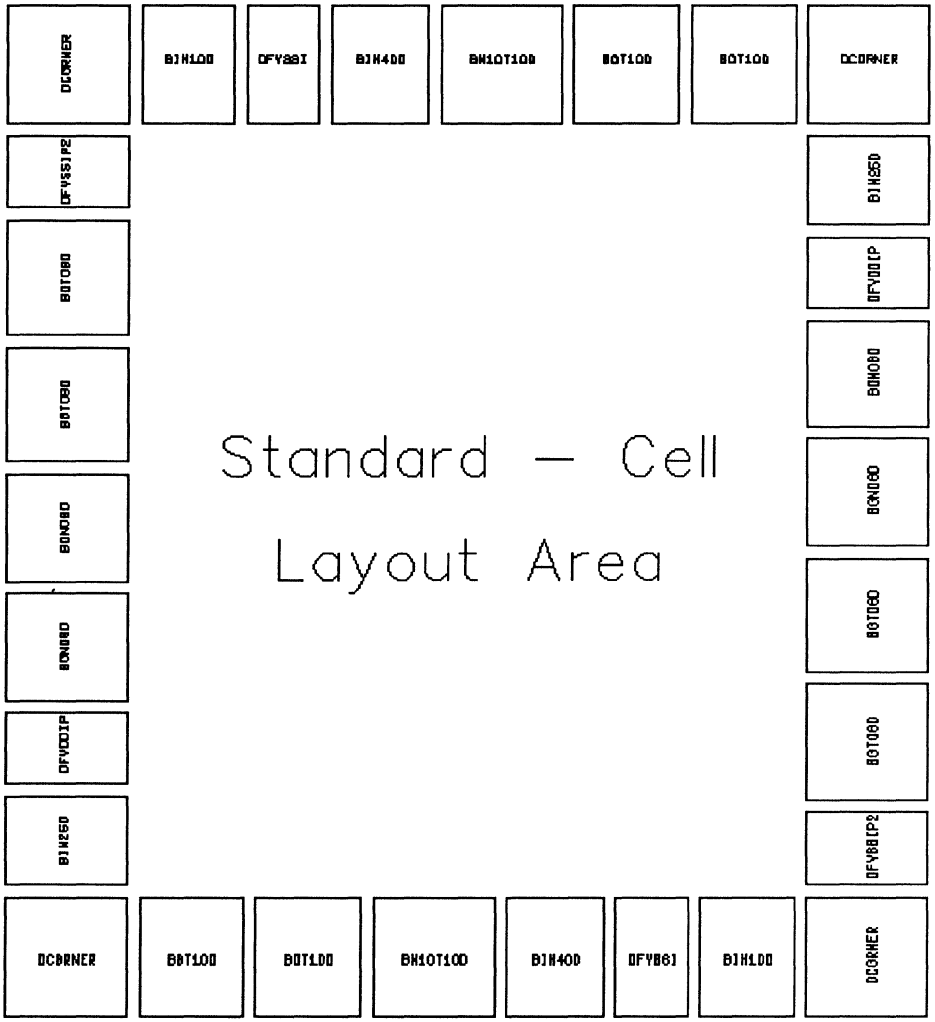

Figure 1. Buffer Ring for a Chip that is Not Pad-Limited

The only layout precaution required is when a buffer's edge closest to its pad faces another buffer's pad edge; they must be separated enough to satisfy wire-bond rules, namely pad-center-to-pad-center separation greater than or equal to 7 mils (175 µm). They may otherwise be abutted freely.

Pad-Limited Chips - This includes chips with a large number of pins and/or a small gate count. If the chip layout uses buffers with -D style layouts, these cells may **NOT** be used in the same buffer row as a -T style buffer. The -D cells must also be used in the manner previously described for non-pad-limited chips (see Figure 2).

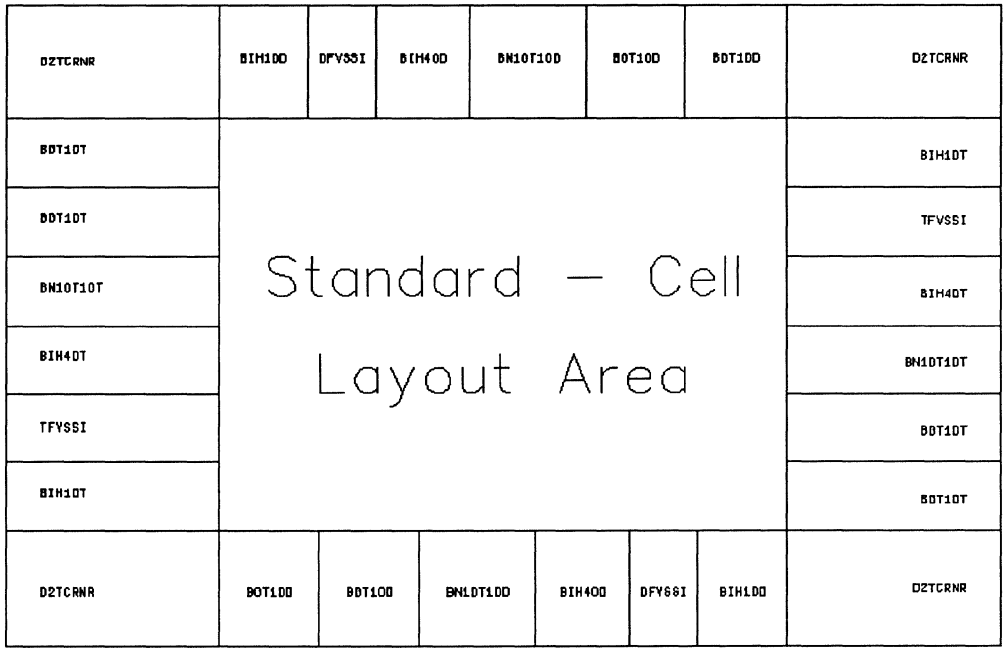

Figure 2. Buffer Ring Using a Combination of -D and -T Style Buffers

Chips that are Strongly Pad-Limited - If the chip uses -T style buffers exclusively (see Figure 3), no special precautions have to be taken with regard to buffer placement.

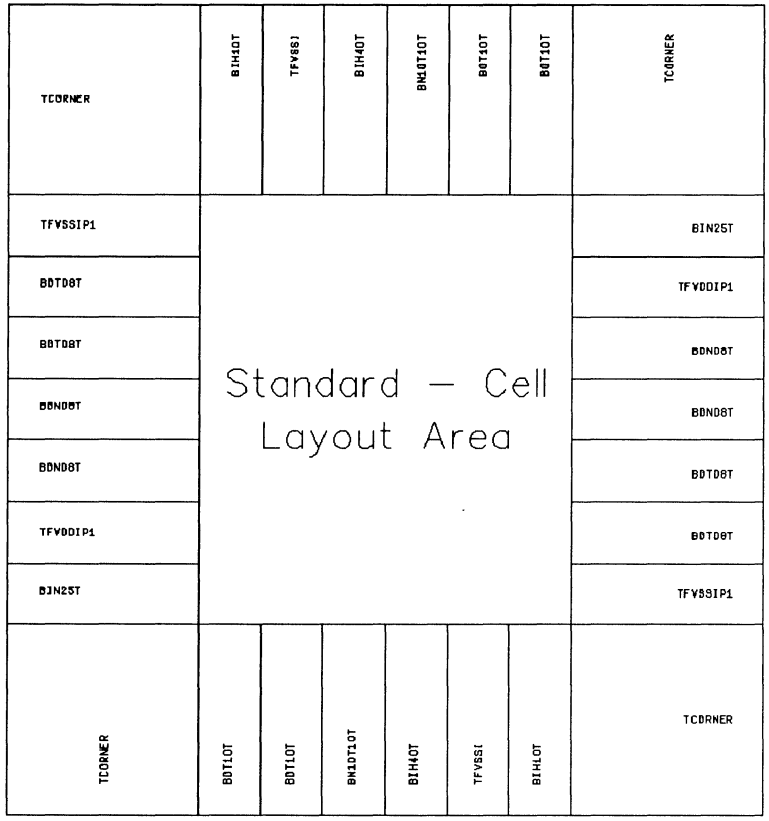

Figure 3. Buffer Ring for a Chip that Is Strongly Pad-Limited

Each buffer circuit includes a circuit network connected to the bonding pad. This network performs two functions: it protects the buffer logic from Electro-Static Discharge (ESD) originating at the chip pins and prevents latch-up spur currents from entering the internal chip logic. The protection network layout is tailored to each of the *-D* and *-T* buffer formats.

Electro-Static Discharge

Buffers have been characterized for two types of ESD events: the Human-Body Model (HBM), and the Charged-Device Model (CDM). The Human-Body Model simulates the effect of a charged person contacting the device. The Charged-Device Model simulates the electrical discharge caused by the tribo-electrical charging of a packaged device.

Devices are characterized for HBM and CDM by using the methodology prescribed by the AT&T spec X-19435, Issue 2. Devices are also characterized for HBM according to the methodology prescribed by MIL-STD 883C Method 3015.6.

Latch-Up

Latch-up occurs when parasitic vertical and lateral bi-polar transistors, which form a P-N-P-N structure from V_{DD} to V_{SS}, turn on. One way latch-up can be triggered is by applying external voltages greater than V_{DD} or less than V_{SS} to I/O buffer pads. The current supplied by the external source forward-biases one of the ESD protection diodes connected to the pad and triggers the P-N-P-N SCR. The high-current SCR will remain turned on until the device self-destructs, or power is removed.

Table 9 gives I-V conditions above which latch-up may occur.

Table 9. - 0.9 µm CMOS Latch-Up Reliability

I/O Pad Current	I/O Pad Voltage
1.0 A	V_{SS} - 1.6V
1.0 A	V_{DD} + 2.5V

Ground-Bounce

Chips with high-speed output buffers driving large capacitive loads generate voltage spikes on the power busses. These voltage spikes are produced when high-speed output buffers generate rapidly changing currents through the parasitic inductance in the package and bonding wire. Although inductive noise occurs on both the V_{DD} and V_{SS} buses, ground-bounce is more noticeable a problem since most buffers are TTL compatible and therefore have a V_{SS} noise margin much less than their V_{DD} noise margin.

There are several steps the designer can take to reduce the overall chip ground-bounce.

System Design:

- Consider CMOS-level compatible I/O over TTL-level compatible I/O.

Package Selection:

- Dedicate as many pins as possible to V_{SS} and V_{DD} with emphasis on V_{SS}.
- If possible, make separate power pins available to isolate fast buffers from other sensitive circuits.
- Place the V_{SS} pins where the internal package lead and the wire bond will be shortest.
- Do not place consecutive V_{SS} pins in groups. Lower overall noise is achieved by interdigitating V_{SS} with either V_{DD} or signal pins.

Layout:

- Select output buffers with care. Use the slowest possible output buffer necessary to satisfy through-put delays and sink/source current requirements.
- If possible, speed up paths with high-power standard-cells, while using the next slowest output buffer.
- If an output pin requires high sink/source current but does not require high speed, use the "X" driver cells (e.g. BOX08D). The output driver speed and noise can then be controlled with a standard-cell subcircuit network.

This section describes the various parameters given in the **Circuit Information** and **Layout Information** tables in the **Cell Pages** following. Unless otherwise stated, the parameters were measured in the *ADVICE* simulator.

There is a small set of process and environmental conditions that simulate the worst-case performance of all the tests and measurements listed in the circuit information tables. These conditions are noted as:

WCF - Worst-Case Fast

This set of process and environment parameters causes CMOS devices to exhibit the lowest parasitic capacitance and impedance and the greatest speed and current-driving capability. It is characterized in the simulator with the following conditions:

- Fast process
- V_{DD} = 5.5 V
- T = 0 ° C

NOM - Nominal

This set of process and environment parameters causes CMOS devices to exhibit the typical capacitance and impedance and the nominal speed and current-driving capability. It is characterized in the simulator with the following conditions:

- Nominal process
- V_{DD} = 5.0 V
- T = 25 ° C

WCS - Worst-Case Slow

This set of process and environment parameters causes CMOS devices to exhibit the highest parasitic capacitance and impedance and the slowest speed and current-driving capability. It is characterized in the simulator with the following conditions:

- Slow process
- V_{DD} = 4.5 V
- T = 125 ° C

General

Capacitance (WCS). The capacitance associated with the circuit input(s) and output(s) is extracted from data calculated by a layout analysis computer program, *GOALIE2.*

In the case of bonding pad nodes, the extracted capacitance value **DOES NOT include any wire-bond or package capacitances.**

Leakage Current (Fast process, V_{DD} = 5.5 V, T = 125 ° C). After manufacture, input pins are tested to pass 0.9 µA current leakage and output pins are tested to pass 9 µA current leakage with the beginning-of-life (BOL) test. With end-of-life (EOL) test, inputs are tested to pass 1 µA current leakage, and outputs are tested to pass 10 µA.

Input Buffers

(includes input buffers used in the bidirectional buffers)

DC Power (WCF). For TTL compatible input buffers, the input gate bias is first held at V_{IL} = 0.8 V (a TTL 0), and at V_{IH} = 2.0 V (a TTL 1). For MOS-level input buffers, the input gate bias is held at 1.0 V and at V_{DD} - 1.0 V.

Under both tests, the current from V_{DD} to V_{SS} is measured. The largest of these two values is multiplied by V_{DD} and recorded as the maximum DC power.

Propagation Delay (NOM). The propagation delay for input buffers is defined as the time separating two events:

- The buffer input switching to a valid input logic level.
- And the buffer output crossing $V_{DD}/2$.

This measurement is made for both rising and falling input edges over a range of output load capacitances from 1 pF to 5 pF. The input voltage has rise and fall times of 2 ns.

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The measurement conditions of propagation delay for TTL-compatible input buffers are illustrated in Figure 4 below. The valid input logic levels are defined to be V_{IL} = 0.8 V and V_{IH} = 2.0 V.

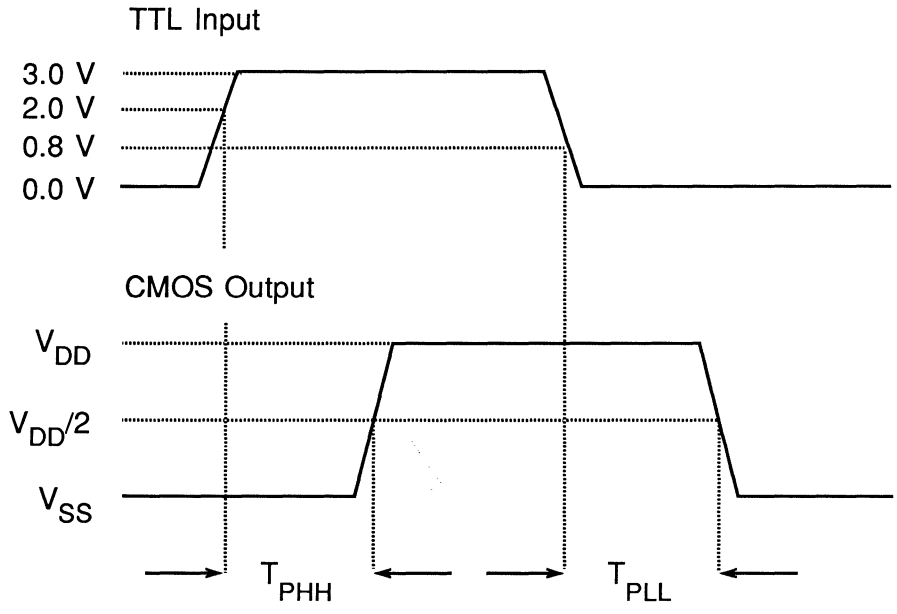


Figure 4. Measurement Conditions - TTL Level Input Buffer Propagation Delay

V- (Fast N process, slow P process, V_{DD} = 4.5 V, T = 125 °C). V- denotes the lowest low-going threshold voltage of a circuit with hysteresis. See Figure 6 below. Under these process and environmental variables, V- achieves its lowest value in BIH- type input and bi-directional buffers. The BIS- and BIT- Schmitt Trigger buffers may exhibit their lowest V- at different conditions than these, however.

A DC analysis is performed though the switching region, and the input voltage at which the circuit output crosses $V_{DD}/2$ is recorded as V- (see also **Hysteresis**).

V+ (Slow N process, fast P process, V_{DD} = 5.5 V, T = 0 °C). V+ denotes the greatest high-going threshold voltage of a circuit with hysteresis. See Figure 6 below. Under these process and environmental variables, V+ achieves its greatest value in BIH-, BIS- and BIT- type input and bi-directional buffers.

A DC analysis is performed though the switching region, and the input voltage at which the circuit output crosses $V_{DD}/2$ is recorded as V+ (see also **Hysteresis**).

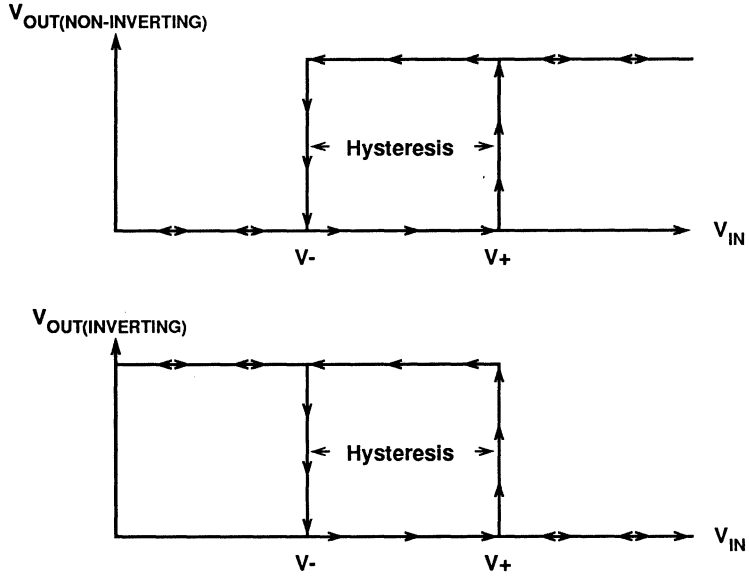


Figure 6. Measurement Conditions - Input Buffer V-, Hysteresis and V+

V_{LO} (Fast N process, slow P process, V_{DD} = 4.5 V, T = 125 °C). V_{LO} denotes the lowest DC switching voltage (V_{I0}) exhibited by a circuit. A DC analysis is made under these conditions, and the input voltage at which the circuit output crosses $V_{DD}/2$ is recorded as V_{LO}.

V_{HI} (Slow N process, fast P process, V_{DD} = 5.5 V, T = 0 °C). V_{HI} denotes the highest DC switching voltage (V_{I1}) exhibited by a circuit. A DC analysis is made under these conditions, and the input voltage at which the circuit output crosses VDD/2 is recorded as V_{HI}.

For MOS-level input buffers, the delay function is determined by simulations using an input waveform with a rail-to-rail pulse with rise and fall times of 2 ns. This is illustrated in Figure 5 below.

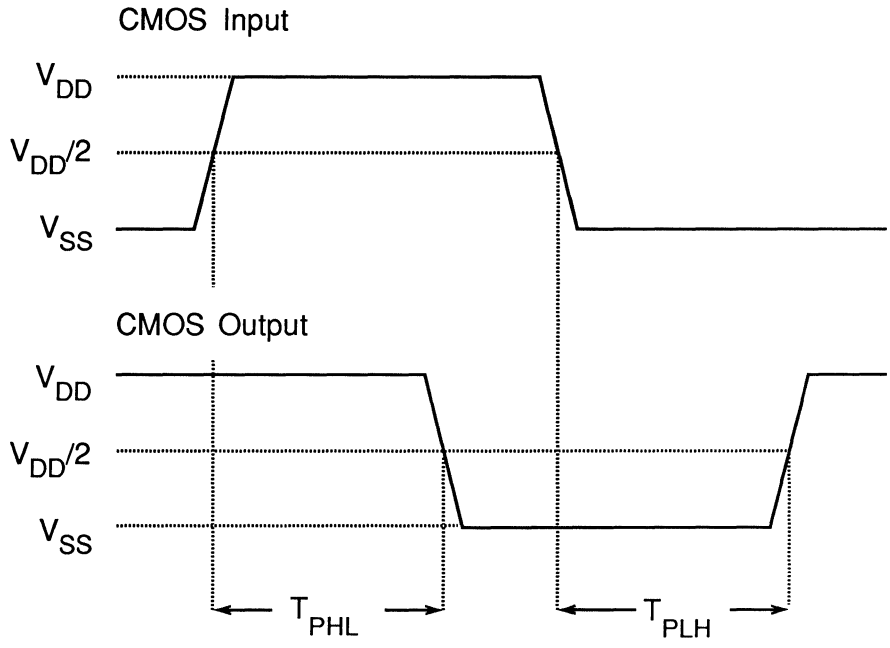


Figure 5. Measurement Conditions - CMOS Level Input Buffer Propagation Delay

Minimum Input Slew (WCF). The Minimum Input Slew Rate of an input buffer is defined as the slowest voltage ramp applied to the input that does not cause the input buffer to oscillate between logic 0 and 1 during switching.

An AC-stability analysis is performed over several input biases, determining the range of input voltages over which the input buffer is unstable. A set of transient analyses is then performed in which the input ramps through the region of instability. The slowest ramp rate that stimulates a buffer output that can read unambiguously by standard-cells is recorded as the Input Slew Rate.

In BIH input buffers and BH bidirectional buffers, the circuit is AC-stable but may still lose data because of sub-threshold leakage effects. For these cells, the minimum input slew rate is calculated by using process sub-threshold leakage current limits and the circuit hysteresis (see also **Hysteresis**).

Hysteresis (Slow process, V_{DD} = 4.5, T = 0 °C). The hysteresis of BIH buffers is not a true hysteresis, although it models one because of the output stage entering a 3-state mode. The range of hysteresis for BIH buffers is therefore defined by the region of input voltage over which the output is in 3-state. See Figure 6 below.

A DC analysis is performed though the switching region, and current drawn by the output stage from an external resistor network is monitored. The region over which no current is drawn or supplied by the output stage is recorded as the minimum hysteresis.

Output Buffers (MOS-Level)

(includes MOS-level output buffers used in bidirectional buffers)

DC Sink/Source Current (WCS). An output logic 0 is enabled, and a voltage source of 0.5 V is applied to the output. The current drawn by the output buffer from the external voltage source is recorded as the DC Sink Current. Similarly, an output logic 1 is enabled, and a voltage source equal to V_{DD} - 0.5 V is applied to the output. The current supplied by the output buffer to the external voltage source is the DC Source Current. Worst-case package and wire-bond parasitic resistance values of 0.10 Ω and 0.05 Ω, respectively, are included in this evaluation. An estimate of power-bus resistance of 0.35 Ω (corresponding to 10 sq. of metal) is also included.

Propagation Delay (NOM). The propagation delay for output buffers is defined as the time separating two events:

- The buffer input switching to a valid logic level, by crossing $V_{DD}/2$,
- And the buffer output crossing $V_{DD}/2$.

The buffer input is loaded with an average routing capacitance and routing resistance and is driven by a performance-optimized INRB standard cell. The rising and falling edge propagation delays are measured over a range of output load capacitances from 0 pF to 200 pF. The waveforms and levels involved are illustrated in Figure 8 below:

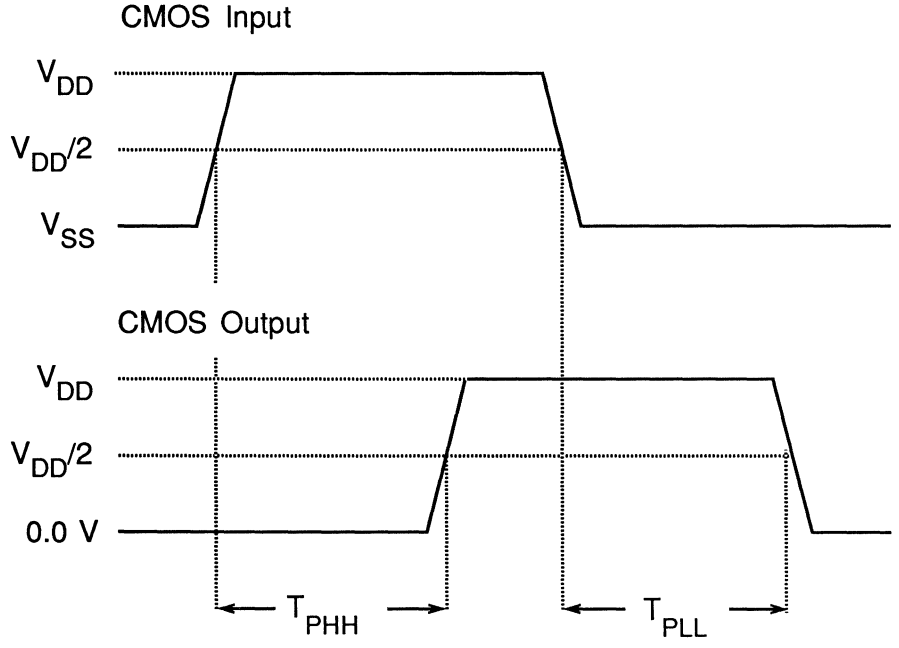


Figure 8. Measurement Conditions - MOS-Level Output Buffer Propagation Delay

Output Buffers (TTL-Level)

(includes TTL-level output buffers used in bidirectional buffers)

DC Sink/Source Current (WCS). An output logic 0 is enabled, and a voltage source equal to a TTL 0 (0.4 V) is applied to the output. The current drawn by the output buffer from the external voltage source is recorded as the DC sink current. Similarly, an output logic 1 is enabled, and a voltage source equal to TTL 1 (2.4 V) is applied to the output. The current supplied by the output buffer to the external voltage source is the DC source current. Worst-case package and wirebond parasitic resistance values of 0.10 Ω and 0.05 Ω, respectively, are included in this evaluation. An estimate of power bus resistance of 0.35 Ω (corresponding to 10 sq. of metal) is also included.

Propagation Delay (NOM). The propagation delay for output buffers is defined as the time separating two events:

1) The buffer input switching to a valid logic level, by crossing $V_{DD}/2$,
2) And the buffer output achieving a valid TTL level, where Logic 1 V_{OH} = 2.4 V, and Logic 0 V_{OL} = 0.4 V.

The buffer input is loaded with an average routing capacitance and routing resistance and is driven by a performance-optimized INRB standard cell. The rising- and falling-edge propagation delays are measured over a range of output load capacitances from 0 pF to 200 pF. The waveforms and levels involved are illustrated in Figure 7 below.

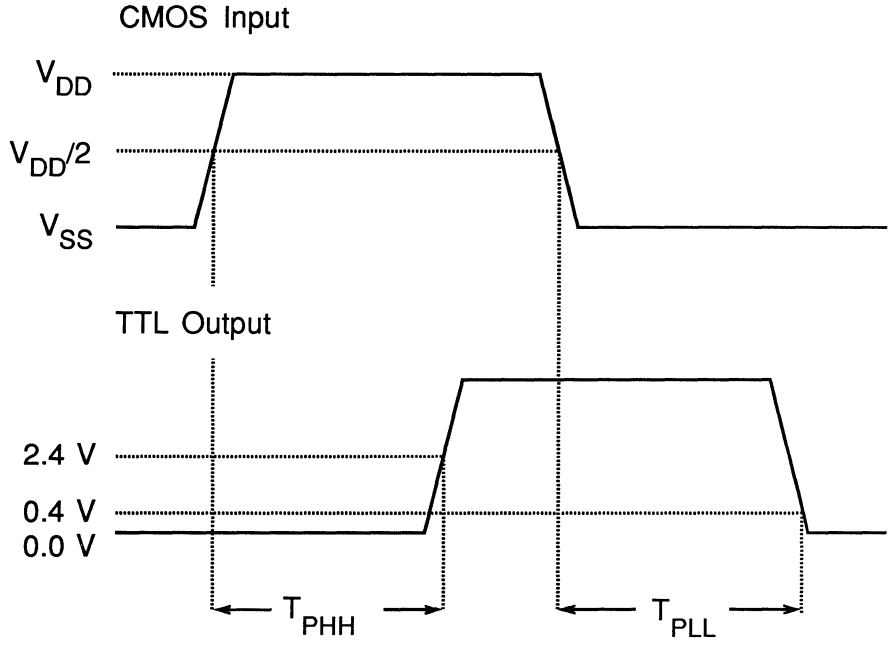


Figure 7. Measurement Conditions - TTL-Level Output Buffer Propagation Delay

3-State Delay - (NOM) For 3-state output buffers the 3-state delay is defined as the time required for the circuit to go into the 3-state mode and is defined as the time separating the following events, as shown in Figure 9 below:

- The 3-state control inputs (ST and STN) both switching to the complimentary logic levels that select the 3-state function, by crossing $V_{DD}/2$.
- And both transistors of the output driver going into their respective cutoff regions.

The 3-state control inputs are loaded with average routing capacitances and resistances and are driven by performance-optimized INRB standard cells. The driver achieves 3-state when both P and N driver transistors are in cutoff. That is, when:

- The N-channel driver gate (node I1) voltage is less than V_{TN}, the N-transistor threshold voltage.
- And the P-channel driver gate (node I2) voltage is greater than (V_{DD} - V_{TP}), a P-transistor threshold voltage below V_{DD}.

The delay coming out of 3-state (if the new logic state does not equal the old logic state) is equal to the propagation delay of the circuit.

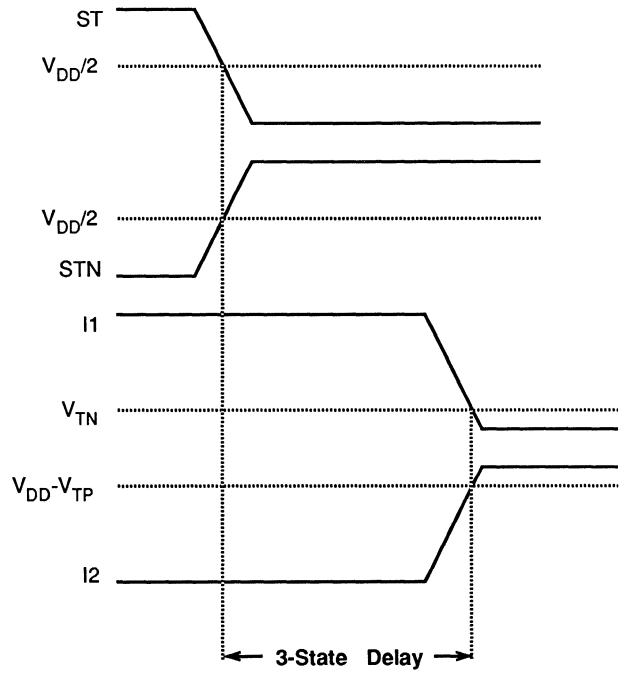


Figure 9. Measurement Conditions - Output Buffer 3-state Delay

Ancillary features are XY-mask geometries that perform no real logic function on the chip but are nonetheless necessary to aid in layout completion, chip identification and chip manufacture. The clumps in Table 10 may be used to route power connections from bonding pads to the buffer and standard-cell areas. All power pads have ESD protection between V_{DD} and V_{SS} included in the layout.

Table 10. Power Routing Ancillary Clumps

Clump Name	Function
D2TCRNR	Chip-corner power bus, connects D to T type I/O buffers
DCORNER	Chip-corner power bus
DCVDDI	Chip-corner power pad, supplies V_{DD} to I/O buffers only
DCVSSI	Chip-corner power pad, supplies V_{SS} to I/O buffers only
DFVDDI	Chip-edge power pad, supplies V_{DD} to I/O buffers only
DFVDDIP	Chip-edge power pad, supplies V_{DD} to I/O buffers and standard cells
DFVDDM2F	Chip-edge power jump-module, supplies V_{DD} to standard cells
DFVDDP0	Chip-edge power pad, supplies V_{DD} to standard cells only with no V_{SS} tabs
DFVDDP1	Chip-edge power pad, supplies V_{DD} to standard cells only with V_{SS} tab on right side
DFVDDP2	Chip-edge power pad, supplies V_{DD} to standard cells only with V_{SS} tabs on both sides
DFVSSI	Chip-edge power pad, supplies V_{SS} to I/O buffers only
DFVSSIP1	Chip-edge power pad, supplies V_{SS} to I/O buffers and standard cells with V_{DD} tab on right side
DFVSSIP2	Chip-edge power pad, supplies V_{SS} to I/O buffers and standard cells with V_{DD} tabs on both sides
DFVSSM2F	Chip-edge power jump-module, supplies V_{SS} to standard cells, passes V_{DD} unbroken
DFVSSP1	Chip-edge power pad, supplies V_{SS} to standard cells only with V_{DD} tab on right side
DFVSSP2	Chip-edge power pad, supplies V_{SS} to standard cells only with V_{DD} tabs on both sides
TCORNER	Chip-corner power bus
TCVDDI1	Chip-corner power pad, supplies V_{DD} to I/O buffers only with V_{SS} tabs on right side
TCVDDI2	Chip-corner power pad, supplies V_{DD} to I/O buffers only with V_{SS} tabs on both sides
TCVSSI	Chip-corner power pad, supplies V_{SS} to I/O buffers only

Table 10 (Cont'd). Power Routing Ancillary Clumps

Clump Name	Function
TFVDDI1	Chip-edge power pad, supplies V_{DD} to I/O buffers only with V_{SS} tabs on right side
TFVDDI2	Chip-edge power pad, supplies V_{DD} to I/O buffers only with V_{SS} tabs on both sides
TFVDDIP1	Chip-edge power pad, supplies V_{DD} to I/O buffers and standard cells with V_{SS} tabs on right side
TFVDDIP2	Chip-edge power pad, supplies V_{DD} to I/O buffers and standard cells with V_{SS} tabs on both sides
TFVDDM2F	Chip-edge jump-module, supplies V_{DD} to standard cells
TFVDDP1	Chip-edge power pad, supplies V_{DD} to standard cells only with V_{SS} tabs on right side
TFVDDP2	Chip-edge power pad, supplies V_{DD} to standard cells only with V_{SS} tabs on both sides
TFVDM2P	Chip-edge power pad, supplies V_{DD} to standard cells only, passes V_{SS} through unbroken
TFVSM2IP	Chip-edge power pad, supplies V_{SS} to I/O buffers and standard cells, passes V_{DD} through unbroken
TFVSM2P	Chip-edge power pad, supplies V_{SS} to standard cells only, passes V_{DD} through unbroken
TFVSSI	Chip-edge power pad, supplies V_{SS} to I/O buffers only
TFVSSIP0	Chip-edge power pad, supplies V_{SS} to I/O buffers and standard cells with no V_{DD} tabs
TFVSSIP1	Chip-edge power pad, supplies V_{SS} to I/O buffers and standard cells with V_{DD} tabs on right side
TFVSSIP2	Chip-edge power pad, supplies V_{SS} to I/O buffers and standard cells with V_{DD} tabs on both sides
TFVSSM2F	Chip-edge jump-module, supplies V_{SS} to standard cells, passes V_{DD} through unbroken
TFVSSP0	Chip-edge power pad, supplies V_{SS} to standard cells only with no V_{DD} tabs
TFVSSP1	Chip-edge power pad, supplies V_{SS} to standard cells only with V_{DD} tabs on right side
TFVSSP2	Chip-edge power pad, supplies V_{SS} to standard cells only with V_{DD} tabs on both sides

Bi-Directional Buffer

BH*id*C*od*[D,T]

BIH- Input Stage, BOC- Output Stage

FUNCTIONAL DESCRIPTION:

Non-Inverting, TTL-Level, Input Stage with Hysteresis,
Non-Inverting, TTL-Level, Open-Collector, Output Stage

CELL NAME DEFINITIONS:

id = WCS input-stage delay in ns @ 5 pF load
od = WCS output-stage delay in ns @ 50 pF load
[D,T] = available layout formats

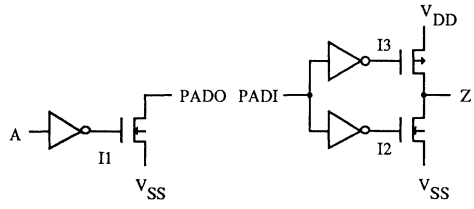
EXAMPLE: BH05C06D

INPUTS: A, PADI
OUTPUTS: Z, PADO
MOTIS Gate Count: 5

Truth Table

Inputs		Outputs	
A	PADI	Z	PADO
0	0	0	0
1	0	0	HI-Z
1	1	1	HI-Z

MOTIS Model



Circuit Capacitances

Cell Name	Node		
	A	PAD[D]*	PAD[T]*
BH05C06	0.409 pF	4.375 pF	5.576 pF
BH05C10	0.119 pF	3.776 pF	5.001 pF
BH10C08	0.170 pF	3.748 pF	4.969 pF
BH10C15	0.077 pF	3.336 pF	4.524 pF
BH20C06	0.409 pF	4.791 pF	5.940 pF
BH20C10	0.119 pF	4.192 pF	5.362 pF
BH20C20	0.078 pF	3.727 pF	4.918 pF
BH20C30	0.067 pF	3.582 pF	4.848 pF

* Pad capacitance varies with layout format.

Input-Stage Circuit Performance

Cell Name	DC Power [1]	Propagation Delay [2]				Input Slew [1]
		T_{PHH}		T_{PLL}		
		Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BH05C06D BH05C06T	6.63 mW	0.267 ns/pF 0.267 ns/pF	1.013 ns 1.003 ns	0.226 ns/pF 0.226 ns/pF	1.411 ns 1.404 ns	>3.1 V/ms
BH05C10D BH05C10T	6.63 mW	0.267 ns/pF 0.267 ns/pF	1.013 ns 1.003 ns	0.226 ns/pF 0.226 ns/pF	1.411 ns 1.404 ns	>3.1 V/ms
BH10C08D BH10C08T	3.17 mW	0.860 ns/pF 0.860 ns/pF	1.158 ns 1.157 ns	0.758 ns/pF 0.758 ns/pF	1.564 ns 1.568 ns	>0.95 V/ms
BH10C15D BH10C15T	3.17 mW	0.860 ns/pF 0.860 ns/pF	1.158 ns 1.157 ns	0.758 ns/pF 0.758 ns/pF	1.564 ns 1.568 ns	>0.95 V/ms
BH20C06D BH20C06T	1.34 mW	1.549 ns/pF 1.549 ns/pF	2.240 ns 2.237 ns	1.329 ns/pF 1.329 ns/pF	4.161 ns 4.168 ns	>0.61 V/ms
BH20C10D BH20C10T	1.34 mW	1.549 ns/pF 1.549 ns/pF	2.240 ns 2.237 ns	1.329 ns/pF 1.329 ns/pF	4.161 ns 4.168 ns	>0.61 V/ms
BH20C20D BH20C20T	1.34 mW	1.549 ns/pF 1.549 ns/pF	2.240 ns 2.237 ns	1.329 ns/pF 1.329 ns/pF	4.161 ns 4.168 ns	>0.61 V/ms
BH20C30D BH20C30T	1.34 mW	1.549 ns/pF 1.549 ns/pF	2.240 ns 2.237 ns	1.329 ns/pF 1.329 ns/pF	4.161 ns 4.168 ns	>0.61 V/ms

1) Fast process, V_{DD} = 5.5 V, T = 0 ° C.
2) Nominal process, V_{DD} = 5.0 V, T = 25 ° C.

V- [3]	Hysteresis [4]	V+ [5]
1.0 V	260 mV	1.8 V

3) Fast N process, slow P process, V_{DD} = 4.5 V, T = 125 ° C
4) Slow process, V_{DD} = 4.5 V, T = 0 ° C
5) Slow N process, fast P process, V_{DD} = 5.5 V, T = 0 ° C

Output-Stage Circuit Performance

Cell Name	Propagation Delay [1] T_{PLL}		DC Current [2]
	Extrinsic	Intrinsic	Sink
BH05C06D BH05C06T	0.272 ns/10pF 0.272 ns/10pF	0.955 ns 1.009 ns	24.0 mA
BH05C10D BH05C10T	0.606 ns/10pF 0.608 ns/10pF	1.358 ns 1.441 ns	10.0 mA
BH10C08D BH10C08T	0.487 ns/10pF 0.488 ns/10pF	1.144 ns 1.211 ns	12.0 mA
BH10C15D BH10C15T	0.798 ns/10pF 0.799 ns/10pF	1.871 ns 1.965 ns	8.0 mA
BH20C06D BH20C06T	0.272 ns/10pF 0.272 ns/10pF	0.966 ns 1.019 ns	24.0 mA
BH20C10D BH20C10T	0.606 ns/10pF 0.608 ns/10pF	1.383 ns 1.463 ns	10.0 mA
BH20C20D BH20C20T	1.708 ns/10pF 1.711 ns/10pF	1.342 ns 1.534 ns	4.0 mA
BH20C30D BH20C30T	2.389 ns/10pF 2.392 ns/10pF	1.815 ns 2.088 ns	3.0 mA

1) Nominal process, V_{DD} = 5.0 V, T = 25 ° C.
2) Slow process, V_{DD} = 4.5 V, T = 125 ° C.

Layout Information

Cell Name	Transistors	Cell Dimensions	
		X	Y
BH05C06D BH05C06T	20	288.00 µm 175.00 µm	283.50 µm 522.90 µm
BH05C10D BH05C10T	14	266.60 µm 175.00 µm	283.50 µm 522.90 µm
BH10C08D BH10C08T	16	273.60 µm 175.00 µm	283.50 µm 522.90 µm
BH10C15D BH10C15T	12	258.20 µm 175.00 µm	283.50 µm 522.90 µm
BH20C06D BH20C06T	20	295.20 µm 175.00 µm	283.50 µm 522.90 µm
BH20C10D BH20C10T	14	273.80 µm 175.00 µm	283.50 µm 522.90 µm
BH20C20D BH20C20T	10	258.40 µm 175.00 µm	283.50 µm 522.90 µm
BH20C30D BH20C30T	10	258.40 µm 175.00 µm	283.50 µm 522.90 µm

Bi-Directional Buffer

BH*id*T*od[D,T]*

BIH- Input Stage, BOT- Output Stage

FUNCTIONAL DESCRIPTION:

Non-Inverting, TTL-Level, Input Stage with Hysteresis,
Non-Inverting, TTL-Level, 3-State, Output Stage

CELL NAME DEFINITIONS:

id = WCS input-stage delay in ns @ 5 pF load
od = WCS output-stage delay in ns @ 50 pF load
[D,T] = available layout formats

EXAMPLE: BH05T06D

INPUTS: A, ST, STN, PADI
OUTPUTS: Z, PADO
MOTIS Gate Count: 6

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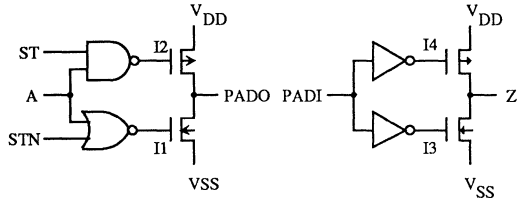
Truth Table

Inputs				Outputs	
A	ST	STN	PADI	Z	PADO
0	X	0	0	0	0
0	X	1	0	0	HI-Z
0	X	1	1	1	HI-Z
1	0	X	0	0	HI-Z
1	0	X	1	1	HI-Z
1	1	X	1	1	1

MOTIS Model



Circuit Capacitances

Cell Name	Node				
	A	ST	STN	PAD[D]*	PAD[T]*
BH05T06	0.884 pF	0.461 pF	0.426 pF	4.374 pF	5.575 pF
BH05T10	0.307 pF	0.166 pF	0.143 pF	3.775 pF	5.000 pF
BH10T08	0.488 pF	0.267 pF	0.233 pF	3.748 pF	4.968 pF
BH10T15	0.191 pF	0.103 pF	0.091 pF	3.336 pF	4.524 pF
BH20T06	0.884 pF	0.461 pF	0.426 pF	4.790 pF	5.940 pF
BH20T10	0.307 pF	0.166 pF	0.143 pF	4.191 pF	5.362 pF
BH20T20	0.193 pF	0.104 pF	0.091 pF	3.727 pF	4.918 pF
BH20T30	0.154 pF	0.084 pF	0.082 pF	3.582 pF	4.848 pF

* Pad capacitance varies with layout format.

Input-Stage Circuit Performance

Cell Name	DC Power [1]	Propagation Delay [2]				Input Slew [1]
		T_{PHH}		T_{PLL}		
		Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BH05T06D	6.63 mW	0.267 ns/pF	1.013 ns	0.226 ns/pF	1.411 ns	>3.1 V/ms
BH05T06T		0.267 ns/pF	1.003 ns	0.226 ns/pF	1.404 ns	
BH05T10D	6.63 mW	0.267 ns/pF	1.013 ns	0.226 ns/pF	1.411 ns	>3.1 V/ms
BH05T10T		0.267 ns/pF	1.003 ns	0.226 ns/pF	1.404 ns	
BH10T08D	3.17 mW	0.860 ns/pF	1.158 ns	0.758 ns/pF	1.564 ns	>0.95 V/ms
BH10T08T		0.860 ns/pF	1.157 ns	0.758 ns/pF	1.568 ns	
BH10T15D	3.17 mW	0.860 ns/pF	1.158 ns	0.758 ns/pF	1.564 ns	>0.95 V/ms
BH10T15T		0.860 ns/pF	1.157 ns	0.758 ns/pF	1.568 ns	
BH20T06D	1.34 mW	1.549 ns/pF	2.240 ns	1.329 ns/pF	4.161 ns	>0.61 V/ms
BH20T06T		1.549 ns/pF	2.237 ns	1.329 ns/pF	4.168 ns	
BH20T10D	1.34 mW	1.549 ns/pF	2.240 ns	1.329 ns/pF	4.161 ns	>0.61 V/ms
BH20T10T		1.549 ns/pF	2.237 ns	1.329 ns/pF	4.168 ns	
BH20T20D	1.34 mW	1.549 ns/pF	2.240 ns	1.329 ns/pF	4.161 ns	>0.61 V/ms
BH20T20T		1.549 ns/pF	2.237 ns	1.329 ns/pF	4.168 ns	
BH20T30D	1.34 mW	1.549 ns/pF	2.240 ns	1.329 ns/pF	4.161 ns	>0.61 V/ms
BH20T30T		1.549 ns/pF	2.237 ns	1.329 ns/pF	4.168 ns	

1) Fast process, V_{DD} = 5.5 V, T = 0 ° C.
2) Nominal process, V_{DD} = 5.0 V, T = 25 ° C.

V- [3]	Hysteresis [4]	V+ [5]
1.0 V	260 mV	1.8 V

3) Fast N process, slow P process, V_{DD} = 4.5 V, T = 125 ° C
4) Slow process, V_{DD} = 4.5 V, T = 0 ° C
5) Slow N process, fast P process, V_{DD} = 5.5 V, T = 0 ° C

Output-Stage Circuit Performance

Cell Name	Propagation Delay [1]				3-State	DC Current [2]
	T_{PHH}		T_{PLL}			
	Extrinsic	Intrinsic	Extrinsic	Intrinsic		Sink/Source
BH05T06D BH05T06T	0.319 ns/10pF 0.319 ns/10pF	1.432 ns 1.480 ns	0.282 ns/10pF 0.281 ns/10pF	1.903 ns 1.949 ns	0.480 ns 0.480 ns	24.0 mA
BH05T10D BH05T10T	0.751 ns/10pF 0.751 ns/10pF	1.715 ns 1.812 ns	0.615 ns/10pF 0.615 ns/10pF	2.328 ns 2.413 ns	0.743 ns 0.744 ns	10.0 mA
BH10T08D BH10T08T	0.582 ns/10pF 0.582 ns/10pF	1.407 ns 1.441 ns	0.495 ns/10pF 0.495 ns/10pF	1.886 ns 1.942 ns	0.576 ns 0.577 ns	12.0 mA
BH10T15D BH10T15T	0.986 ns/10pF 0.986 ns/10pF	2.444 ns 2.555 ns	0.808 ns/10pF 0.808 ns/10pF	3.111 ns 3.206 ns	1.050 ns 1.050 ns	8.0 mA
BH20T06D BH20T06T	0.319 ns/10pF 0.319 ns/10pF	1.445 ns 1.492 ns	0.282 ns/10pF 0.281 ns/10pF	1.915 ns 1.959 ns	0.480 ns 0.480 ns	24.0 mA
BH20T10D BH20T10T	0.751 ns/10pF 0.751 ns/10pF	1.746 ns 1.839 ns	0.615 ns/10pF 0.615 ns/10pF	2.354 ns 2.436 ns	0.743 ns 0.744 ns	10.0 mA
BH20T20D BH20T20T	2.016 ns/10pF 2.016 ns/10pF	1.834 ns 2.057 ns	1.716 ns/10pF 1.716 ns/10pF	2.112 ns 2.310 ns	0.609 ns 0.610 ns	4.0 mA
BH20T30D BH20T30T	2.866 ns/10pF 2.866 ns/10pF	1.691 ns 2.017 ns	2.399 ns/10pF 2.399 ns/10pF	2.732 ns 3.012 ns	0.739 ns 0.740 ns	3.0 mA

1) Nominal process, V_{DD} = 5.0 V, T = 25 ° C.
2) Slow process, V_{DD} = 4.5 V, T = 125 ° C.

Layout Information

Cell Name	Transistors	Cell Dimensions	
		X	Y
BH05T06D BH05T06T	26	303.20 µm 175.00 µm	283.50 µm 522.90 µm
BH05T10D BH05T10T	20	281.80 µm 175.00 µm	283.50 µm 522.90 µm
BH10T08D BH10T08T	22	288.80 µm 175.00 µm	283.50 µm 522.90 µm
BH10T15D BH10T15T	18	273.40 µm 175.00 µm	283.50 µm 522.90 µm
BH20T06D BH20T06T	26	310.40 µm 175.00 µm	283.50 µm 522.90 µm
BH20T10D BH20T10T	20	289.00 µm 175.00 µm	283.50 µm 522.90 µm
BH20T20D BH20T20T	16	273.60 µm 175.00 µm	283.50 µm 522.90 µm
BH20T30D BH20T30T	16	273.60 µm 175.00 µm	283.50 µm 522.90 µm

Bi-Directional Buffer

BH*id*X*od*[D,T]

BIH- Input Stage, BOX- Output Stage

FUNCTIONAL DESCRIPTION:

Non-Inverting, TTL-Level, Input Stage with Hysteresis,
Driver-Transistors-Only, (No Inherent Logic) Output Stage

CELL NAME DEFINITIONS:

id = WCS input-stage delay in ns @ 5 pF load
od = WCS output-stage delay in ns @ 50 pF load
[D,T] = available layout formats

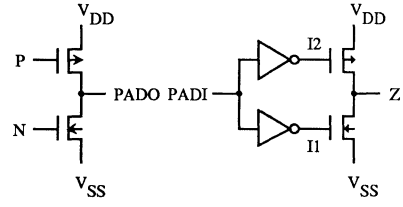
EXAMPLE: BH05X06D

INPUTS: N, P, PADI
OUTPUTS: Z, PADO
MOTIS Gate Count: 4

Truth Table

Inputs			Outputs	
N	P	PADI	Z	PADO
0	0	1	1	1
0	1	0	0	HI-Z
0	1	1	1	HI-Z
1	1	0	0	0

MOTIS Model



Circuit Capacitances

Cell Name	Node			
	N	P	PAD[D]*	PAD[T]*
BH05X06	1.663 pF	1.914 pF	4.374 pF	5.575 pF
BH05X10	0.821 pF	0.820 pF	3.784 pF	5.009 pF
BH10X08	1.073 pF	1.072 pF	3.748 pF	4.968 pF
BH10X15	0.601 pF	0.615 pF	3.336 pF	4.524 pF
BH20X06	1.663 pF	1.914 pF	4.790 pF	5.940 pF
BH20X10	0.821 pF	0.820 pF	4.200 pF	5.370 pF
BH20X20	0.282 pF	0.302 pF	3.727 pF	4.918 pF
BH20X30	0.211 pF	0.223 pF	3.582 pF	4.848 pF

* Pad capacitance varies with layout format.

Input-Stage Circuit Performance

Cell Name	DC Power [1]	Propagation Delay [2]				Input Slew [1]
		T_{PHH}		T_{PLL}		
		Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BH05X06D BH05X06T	6.63 mW	0.267 ns/pF 0.267 ns/pF	1.013 ns 1.003 ns	0.226 ns/pF 0.226 ns/pF	1.411 ns 1.404 ns	>3.1 V/ms
BH05X10D BH05X10T	6.63 mW	0.267 ns/pF 0.267 ns/pF	1.013 ns 1.003 ns	0.226 ns/pF 0.226 ns/pF	1.411 ns 1.404 ns	>3.1 V/ms
BH10X08D BH10X08T	3.17 mW	0.860 ns/pF 0.860 ns/pF	1.158 ns 1.157 ns	0.758 ns/pF 0.758 ns/pF	1.564 ns 1.568 ns	>0.95 V/ms
BH10X15D BH10X15T	3.17 mW	0.860 ns/pF 0.860 ns/pF	1.158 ns 1.157 ns	0.758 ns/pF 0.758 ns/pF	1.564 ns 1.568 ns	>0.95 V/ms
BH20X06D BH20X06T	1.34 mW	1.549 ns/pF 1.549 ns/pF	2.240 ns 2.237 ns	1.329 ns/pF 1.329 ns/pF	4.161 ns 4.168 ns	>0.61 V/ms
BH20X10D BH20X10T	1.34 mW	1.549 ns/pF 1.549 ns/pF	2.240 ns 2.237 ns	1.329 ns/pF 1.329 ns/pF	4.161 ns 4.168 ns	>0.61 V/ms
BH20X20D BH20X20T	1.34 mW	1.549 ns/pF 1.549 ns/pF	2.240 ns 2.237 ns	1.329 ns/pF 1.329 ns/pF	4.161 ns 4.168 ns	>0.61 V/ms
BH20X30D BH20X30T	1.34 mW	1.549 ns/pF 1.549 ns/pF	2.240 ns 2.237 ns	1.329 ns/pF 1.329 ns/pF	4.161 ns 4.168 ns	>0.61 V/ms

1) Fast process, V_{DD} = 5.5 V, T = 0 ° C.
2) Nominal Process, V_{DD} = 5.0 V, T = 25 ° C.

V- [3]	Hysteresis [4]	V+ [5]
1.0 V	260 mV	1.8 V

3) Fast N process, slow P process, V_{DD} = 4.5 V, T = 125 ° C
4) Slow process, V_{DD} = 4.5 V, T = 0 ° C
5) Slow N process, fast P process, V_{DD} = 5.5 V, T = 0 ° C

Output-Stage Circuit Performance

Cell Name	Propagation Delay [1]				DC Current [2]
	T_{PHL}		T_{PLH}		
	Extrinsic	Intrinsic	Extrinsic	Intrinsic	Sink/Source
BH05X06D BH05X06T	0.317 ns/10pF 0.317 ns/10pF	1.584 ns 1.633 ns	0.303 ns/10pF 0.302 ns/10pF	1.557 ns 1.613 ns	24.0 mA
BH05X10D BH05X10T	0.748 ns/10pF 0.748 ns/10pF	0.825 ns 0.923 ns	0.611 ns/10pF 0.611 ns/10pF	1.066 ns 1.147 ns	10.0 mA
BH10X08D BH10X08T	0.582 ns/10pF 0.581 ns/10pF	0.970 ns 1.048 ns	0.500 ns/10pF 0.499 ns/10pF	1.148 ns 1.230 ns	12.0 mA
BH10X15D BH10X15T	0.984 ns/10pF 0.984 ns/10pF	0.662 ns 0.769 ns	0.800 ns/10pF 0.799 ns/10pF	0.900 ns 0.994 ns	8.0 mA
BH20X06D BH20X06T	0.317 ns/10pF 0.317 ns/10pF	1.597 ns 1.645 ns	0.303 ns/10pF 0.302 ns/10pF	1.570 ns 1.624 ns	24.0 mA
BH20X10D BH20X10T	0.748 ns/10pF 0.748 ns/10pF	0.856 ns 0.950 ns	0.611 ns/10pF 0.611 ns/10pF	1.091 ns 1.169 ns	10.0 mA
BH20X20D BH20X20T	2.016 ns/10pF 2.016 ns/10pF	0.818 ns 1.035 ns	1.710 ns/10pF 1.710 ns/10pF	0.925 ns 1.108 ns	4.0 mA
BH20X30D BH20X30T	2.866 ns/10pF 2.866 ns/10pF	0.987 ns 1.304 ns	2.339 ns/10pF 2.338 ns/10pF	1.273 ns 1.558 ns	3.0 mA

1) Nominal process, V_{DD} = 5.0 V, T = 25 ° C.
2) Slow process, V_{DD} = 4.5 V, T = 125 ° C.

Layout Information

Cell Name	Transistors	Cell Dimensions	
		X	Y
BH05X06D BH05X06T	18	284.40 µm 175.00 µm	283.50 µm 522.90 µm
BH05X10D BH05X10T	12	263.00 µm 175.00 µm	283.50 µm 522.90 µm
BH10X08D BH10X08T	14	270.00 µm 175.00 µm	283.50 µm 522.90 µm
BH10X15D BH10X15T	10	254.60 µm 175.00 µm	283.50 µm 522.90 µm
BH20X06D BH20X06T	18	291.60 µm 175.00 µm	283.50 µm 522.90 µm
BH20X10D BH20X10T	12	270.20 µm 175.00 µm	283.50 µm 522.90 µm
BH20X20D BH20X20T	8	254.80 µm 175.00 µm	283.50 µm 522.90 µm
BH20X30D BH20X30T	8	254.80 µm 175.00 µm	283.50 µm 522.90 µm

Input Buffer

BIH*id[D,T]*

FUNCTIONAL DESCRIPTION:

Non-Inverting, TTL-Level, Input Buffer with Hysteresis

CELL NAME DEFINITIONS:

id = WCS delay in ns @ 5pF load

[D,T] = available layout formats

EXAMPLE: BIH05D

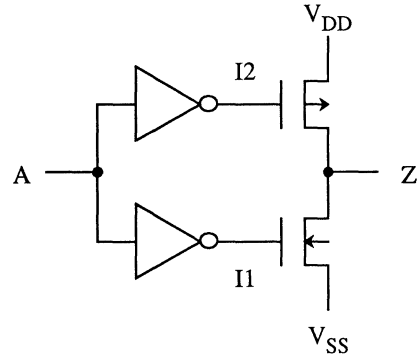
INPUTS: A
OUTPUTS: Z
MOTIS Gate Count: 3 **Transistors:** 6

5

Truth Table

Input	Output
A	Z
0	0
1	1

MOTIS Model



Circuit Capacitances

Cell Name	Node	
	A[D]*	A[T]*
BIH05	2.832 pF	3.647 pF
BIH10	2.835 pF	3.650 pF
BIH20	3.248 pF	4.060 pF

* Pad capacitance varies with layout format.

Circuit Performance

Cell Name	DC Power [1]	Propagation Delay [2]				Input Slew [1]
		T_{PHH}		T_{PLL}		
		Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BIH05D	6.63 mW	0.267 ns/pF	1.013 ns	0.226 ns/pF	1.411 ns	>3.1 V/ms
BIH05T		0.267 ns/pF	1.003 ns	0.226 ns/pF	1.404 ns	
BIH10D	3.17 mW	0.860 ns/pF	1.158 ns	0.758 ns/pF	1.564 ns	>0.95 V/ms
BIH10T		0.860 ns/pF	1.157 ns	0.758 ns/pF	1.568 ns	
BIH20D	1.34 mW	1.549 ns/pF	2.240 ns	1.329 ns/pF	4.161 ns	>0.61 V/ms
BIH20T		1.549 ns/pF	2.237 ns	1.329 ns/pF	4.168 ns	

1) Fast process, V_{DD} = 5.5 V, T = 0 ° C.
2) Nominal process, V_{DD} = 5.0 V, T = 25 ° C.

V- [3]	Hysteresis [4]	V+ [5]
1.0 V	260 mV	1.8 V

3) Fast N process, slow P process, V_{DD} = 4.5 V, T = 125 ° C
4) Slow process, V_{DD} = 4.5 V, T = 0 ° C
5) Slow N process, fast P process, V_{DD} = 5.5 V, T = 0 ° C

Layout Dimensions

Cell Name	Cell Dimensions	
	X	Y
BIH05D	213.85 µm	283.50 µm
BIH05T	175.00 µm	522.90 µm
BIH10D	214.85 µm	283.50 µm
BIH10T	175.00 µm	522.90 µm
BIH20D	221.05 µm	283.50 µm
BIH20T	175.00 µm	522.90 µm

Input Buffer

BIM*id[D,T]*

FUNCTIONAL DESCRIPTION:

Inverting, CMOS-Level Input Buffer

CELL NAME DEFINITIONS:

id = WCS delay in ns @ 5pF load
[D,T] = available layout formats

EXAMPLE: BIM02D

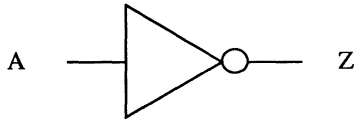
INPUTS: A
OUTPUTS: Z
MOTIS Gate Count: 1 **Transistors:** 2

5

Truth Table

Input	Output
A	Z
0	1
1	0

MOTIS Model



Circuit Capacitances

Cell Name	Node	
	A[D]*	A[T]*
BIM02	3.279 pF	4.101 pF
BIM03	3.071 pF	3.895 pF
BIM05	2.835 pF	3.658 pF
BIM10	2.707 pF	3.531 pF

* Pad capacitance varies with layout format.

Circuit Performance

Cell Name	DC Power [1]	Propagation Delay [2]				Input Slew [1]
		T_{PHL}		T_{PLH}		
		Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BIM02D	0.31 µW	0.133 ns/pF	0.640 ns	0.138 ns/pF	0.669 ns	NA
BIM02T		0.132 ns/pF	0.636 ns	0.137 ns/pF	0.663 ns	
BIM03D	0.16 µW	0.237 ns/pF	0.664 ns	0.256 ns/pF	0.684 ns	NA
BIM03T		0.236 ns/pF	0.659 ns	0.255 ns/pF	0.677 ns	
BIM05D	0.09 µW	0.409 ns/pF	0.626 ns	0.489 ns/pF	0.685 ns	NA
BIM05T		0.409 ns/pF	0.621 ns	0.488 ns/pF	0.679 ns	
BIM10D	0.04 µW	0.964 ns/pF	0.699 ns	1.044 ns/pF	0.745 ns	NA
BIM10T		0.964 ns/pF	0.699 ns	1.044 ns/pF	0.745 ns	

1) Fast process, V_{DD} = 5.5 V, T = 0 ° C.
2) Nominal process, V_{DD} = 5.0 V, T = 25 ° C.
NA) Not Applicable.

V_{LO} [3]	V_{HI} [4]
1.9 V	2.9 V

3) Fast N process, slow P process, V_{DD} = 4.5 V, T = 0 ° C
4) Slow N process, fast P process, V_{DD} = 5.5 V, T = 125 ° C

Layout Dimensions

Cell Name	Cell Dimensions	
	X	Y
BIM02D	200.15 µm	283.50 µm
BIM02T	175.00 µm	522.90 µm
BIM03D	196.85 µm	283.50 µm
BIM03T	175.00 µm	522.90 µm
BIM05D	196.85 µm	283.50 µm
BIM05T	175.00 µm	522.90 µm
BIM10D	196.85 µm	283.50 µm
BIM10T	175.00 µm	522.90 µm

FUNCTIONAL DESCRIPTION:

Non-Inverting, TTL-Level Input Buffer

CELL NAME DEFINITIONS:

id = WCS delay in ns @ 5pF load
[D,T] = available layout formats

EXAMPLE: BIN04D

INPUTS: A
OUTPUTS: Z
MOTIS Gate Count: 2 **Transistors:** 4

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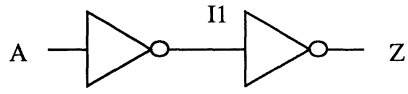
Truth Table

Input	Output
A	Z
0	0
1	1

MOTIS Model



Circuit Capacitances

Cell Name	Node	
	A[D]*	A[T]*
BIN04	2.839 pF	3.658 pF
BIN06	2.725 pF	3.544 pF
BIN10	2.706 pF	3.526 pF
BIN15	2.737 pF	3.556 pF
BIN20	2.853 pF	3.671 pF
BIN25	2.862 pF	3.680 pF

* Pad capacitance varies with layout format.

Circuit Performance

Cell Name	DC Power [1]	Propagation Delay [2]				Input Slew [1]
		T_{PHH}		T_{PLL}		
		Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BIN04D BIN04T	6.70 mW	0.251 ns/pF 0.249 ns/pF	0.801 ns 0.796 ns	0.168 ns/pF 0.168 ns/pF	1.393 ns 1.385 ns	>3.0 V/ms
BIN06D BIN06T	3.35 mW	0.365 ns/pF 0.364 ns/pF	0.788 ns 0.783 ns	0.319 ns/pF 0.318 ns/pF	1.691 ns 1.684 ns	>2.4 V/ms
BIN10D BIN10T	1.53 mW	0.822 ns/pF 0.821 ns/pF	0.912 ns 0.912 ns	0.676 ns/pF 0.675 ns/pF	2.077 ns 2.078 ns	>1.3 V/ms
BIN15D BIN15T	0.82 mW	1.312 ns/pF 1.312 ns/pF	1.185 ns 1.189 ns	1.040 ns/pF 1.041 ns/pF	2.972 ns 2.976 ns	>0.63 V/ms
BIN20D BIN20T	0.53 mW	1.813 ns/pF 1.811 ns/pF	1.656 ns 1.671 ns	1.329 ns/pF 1.329 ns/pF	4.401 ns 4.396 ns	>0.36 V/ms
BIN25D BIN25T	0.37 mW	2.215 ns/pF 2.213 ns/pF	1.992 ns 2.013 ns	1.657 ns/pF 1.659 ns/pF	5.384 ns 5.381 ns	>0.29 V/ms

1) Fast process, V_{DD} = 5.5 V, T = 0 ° C.
2) Nominal process, V_{DD} = 5.0 V, T = 25 ° C.

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V_{LO} [3]	V_{HI} [4]
1.1 V	1.7 V

3) Fast N process, slow P process, V_{DD} = 4.5 V, T = 125 ° C
4) Slow N process, fast P process, V_{DD} = 5.5 V, T = 0 °C

Layout Dimensions

Cell Name	Cell Dimensions	
	X	Y
BIN04D BIN04T	205.35 µm 175.00 µm	283.50 µm 522.90 µm
BIN06D BIN06T	205.35 µm 175.00 µm	283.50 µm 522.90 µm
BIN10D BIN10T	205.85 µm 175.00 µm	283.50 µm 522.90 µm
BIN15D BIN15T	206.85 µm 175.00 µm	283.50 µm 522.90 µm
BIN20D BIN20T	208.85 µm 175.00 µm	283.50 µm 522.90 µm
BIN25D BIN25T	209.85 µm 175.00 µm	283.50 µm 522.90 µm

FUNCTIONAL DESCRIPTION:
ESD Protection Only, No Active Logic

CELL NAME DEFINITIONS:
id = WCS delay in ns @ 5pF load
[D,T] = available layout formats

INPUTS: A
OUTPUTS: Z
MOTIS Gate Count: 0 **Transistors:** 0

Truth Table

Input	Output
A	Z
0	0
1	1

MOTIS Model

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Circuit Capacitances

Cell Name	Node	
	A[D]*	A[T]*
BIP02	2.672 pF	3.510 pF

* Pad capacitance varies with layout format.

Circuit Performance

Cell Name	DC Power [1]	Propagation Delay [2]				Input Slew [1]
		T_{PHH}		T_{PLL}		
		Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BIP02D	Nil	0.366 ns/pF	0.249 ns	0.369 ns/pF	0.255 ns	NA
BIP02T		0.366 ns/pF	0.247 ns	0.368 ns/pF	0.253 ns	

1) Fast process, V_{DD} = 5.5 V, T = 0 ° C.
2) Nominal process, V_{DD} = 5.0 V, T = 25 ° C.
NA) Not Applicable.

Layout Dimensions

Cell Name	Cell Dimensions	
	X	Y
BIP02D	192.95 µm	283.50 µm
BIP02T	175.00 µm	522.90 µm

FUNCTIONAL DESCRIPTION:

Inverting, CMOS-Level, Schmitt Trigger Input Buffer

CELL NAME DEFINITIONS:

id = WCS delay in ns @ 5pF load
[D,T] = available layout formats

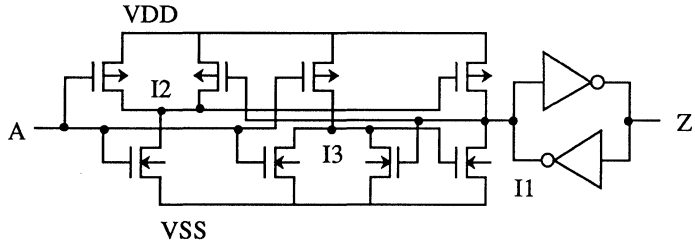
EXAMPLE: BIS07D

INPUTS: A
OUTPUTS: Z
MOTIS Gate Count: 5 **Transistors:** 12

Truth Table

Input	Output
A	Z
0	1
1	0

MOTIS Model



Circuit Capacitances

Cell Name	Node	
	A[D]*	A[T]*
BIS07	2.937 pF	3.740 pF

* Pad capacitance varies with layout format.

Circuit Performance

Cell Name	DC Power [1]	Propagation Delay [2]				Input Slew [1]
		T_{PHH}		T_{PLL}		
		Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BIS07D	0.12 µW	0.253 ns/pF	3.147 ns	0.272 ns/pF	3.218 ns	NA
BIS07T		0.252 ns/pF	3.137 ns	0.270 ns/pF	3.200 ns	

1) Fast process, V_{DD} = 5.5 V, T = 0 ° C.
2) Nominal process, V_{DD} = 5.0 V, T = 25 ° C.
NA) Not Applicable.

V- [3]	Hysteresis [4]	V+ [5]
0.5 V	1.8 V	VDD - 0.5 V

3) fast N process, slow P process, V_{DD} = 4.5 V, T = 0 ° C
4) Fast process, V_{DD}=4.5 V, T=125° C
5) Slow N process, fast P process, V_{DD} = 4.5 V, T = 0 ° C

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Layout Dimensions

Cell Name	Cell Dimensions	
	X	Y
BIS07D	238.85 µm	283.50 µm
BIS07T	175.00 µm	522.90 µm

FUNCTIONAL DESCRIPTION:

Inverting, TTL-Level, Schmitt Trigger Input Buffer

CELL NAME DEFINITIONS:

id = WCS delay in ns @ 5pF load
[D,T] = available layout formats

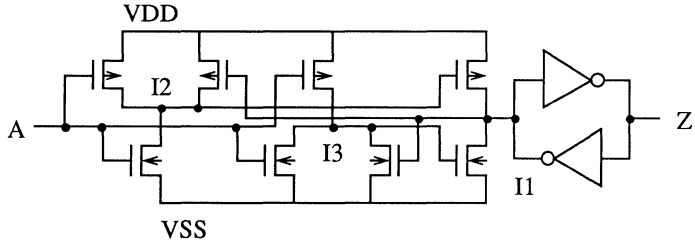
EXAMPLE: BIT06D

INPUTS: A
OUTPUTS: Z
MOTIS Gate Count: 5 **Transistors:** 12

Truth Table

Input	Output
A	Z
0	1
1	0

MOTIS Model



Circuit Capacitances

Cell Name	Node	
	A[D]*	A[T]*
BIT06	3.070 pF	3.876 pF
BIT11	3.639 pF	4.495 pF

* Pad capacitance varies with layout format.

Circuit Performance

Cell Name	DC Power [1]	Propagation Delay [2]				Input Slew [1]
		T_{PHH}		T_{PLL}		
		Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BIT06D	11.5 mW	0.289 ns/pF	2.005 ns	0.283 ns/pF	2.503 ns	NA
BIT06T		0.289 ns/pF	1.995 ns	0.283 ns/pF	2.493 ns	
BIT11D	4.4 mW	0.339 ns/pF	4.447 ns	0.307 ns/pF	6.176 ns	NA
BIT11T		0.338 ns/pF	4.445 ns	0.306 ns/pF	6.172 NS	

1) Fast process, V_{DD} = 5.5 V, T = 0 ° C.
2) Nominal process, V_{DD} = 5.0 V, T = 25 ° C.
NA) Not Applicable.

V- [3]	Hysteresis [4]	V+ [5]
0.9 V	300 mV	1.9 V

3) Fast N process, slow P process, V_{DD} = 4.5 V, T = 0 °C
4) Fast process, V_{DD} = 4.5 V, T = 125 ° C
5) Slow N process, fast P process, V_{DD} = 5.5 V, T = 0 ° C

Layout Dimensions

Cell Name	Cell Dimensions	
	X	Y
BIT06D	243.25 µm	283.50 µm
BIT06T	175.00 µm	522.90 µm
BIT11D	253.85 µm	283.50 µm
BIT11T	175.00 µm	522.90 µm

Bi-Directional Buffer

BM*id*M*od[D,T]*

FUNCTIONAL DESCRIPTION:

Inverting, MOS-Level, Input Stage,
Non-Inverting, MOS-Level, 3-State, Output Stage

CELL NAME DEFINITIONS:

id = WCS input-stage delay in ns @ 5pF load
od = WCS output-stage delay in ns @ 50pF load
[D,T] = available layout formats

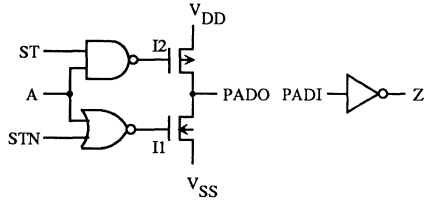
EXAMPLE: BM02M05D

INPUTS: A, ST, STN, PADI
OUTPUTS: Z, PADO
MOTIS Gate Count: 4

Truth Table

Inputs				Outputs	
A	ST	STN	PADI	Z	PADO
0	X	0	0	1	0
0	X	1	0	1	HI-Z
0	X	1	1	0	HI-Z
1	0	X	0	1	HI-Z
1	0	X	1	0	HI-Z
1	1	X	1	0	1

MOTIS Model



Circuit Capacitances

Cell Name	Node				
	A	ST	STN	PAD[D]*	PAD[T]*
BM02M05	0.754 pF	0.368 pF	0.389 pF	4.669 pF	6.011 pF
BM03M05	0.754 pF	0.368 pF	0.389 pF	4.461 pF	5.830 pF
BM03M10	0.457 pF	0.229 pF	0.231 pF	3.370 pF	4.932 pF
BM05M05	0.754 pF	0.368 pF	0.389 pF	4.225 pF	5.594 pF
BM05M10	0.457 pF	0.229 pF	0.231 pF	3.134 pF	4.696 pF
BM05M15	0.284 pF	0.150 pF	0.137 pF	3.212 pF	4.778 pF
BM10M05	0.754 pF	0.368 pF	0.389 pF	4.098 pF	5.467 pF
BM10M10	0.457 pF	0.229 pF	0.231 pF	3.007 pF	4.569 pF
BM10M15	0.284 pF	0.150 pF	0.137 pF	3.085 pF	4.651 pF

* Pad capacitance varies with layout format.

Input-Stage Circuit Performance

Cell Name	DC Power [1]	Propagation Delay [2]				Input Slew [1]
		T_{PHH}		T_{PLL}		
		Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BM02M05D BM02M05T	0.31 µW	0.133 ns/pF 0.132 ns/pF	0.640 ns 0.636 ns	0.138 ns/pF 0.137 ns/pF	0.669 ns 0.663 ns	NA
BM03M05D BM03M05T	0.16 µW	0.237 ns/pF 0.236 ns/pF	0.664 ns 0.659 ns	0.256 ns/pF 0.255 ns/pF	0.684 ns 0.677 ns	NA
BM03M10D BM03M10T	0.16 µW	0.237 ns/pF 0.236 ns/pF	0.664 ns 0.659 ns	0.256 ns/pF 0.255 ns/pF	0.684 ns 0.677 ns	NA
BM05M05D BM05M05T	0.09 µW	0.409 ns/pF 0.409 ns/pF	0.626 ns 0.621 ns	0.489 ns/pF 0.488 ns/pF	0.685 ns 0.679 ns	NA
BM05M10D BM05M10T	0.09 µW	0.409 ns/pF 0.409 ns/pF	0.626 ns 0.621 ns	0.489 ns/pF 0.488 ns/pF	0.685 ns 0.679 ns	NA
BM05M15D BM05M15T	0.09 µW	0.409 ns/pF 0.409 ns/pF	0.626 ns 0.621 ns	0.489 ns/pF 0.488 ns/pF	0.685 ns 0.679 ns	NA
BM10M05D BM10M05T	0.04 µW	0.964 ns/pF 0.964 ns/pF	0.699 ns 0.699 ns	1.044 ns/pF 1.044 ns/pF	0.745 ns 0.745 ns	NA
BM10M10D BM10M10T	0.04 µW	0.964 ns/pF 0.964 ns/pF	0.699 ns 0.699 ns	1.044 ns/pF 1.044 ns/pF	0.745 ns 0.745 ns	NA
BM10M15D BM10M15T	0.04 µW	0.964 ns/pF 0.964 ns/pF	0.699 ns 0.699 ns	1.044 ns/pF 1.044 ns/pF	0.745 ns 0.745 ns	NA

1) Fast process, V_{DD} = 5.5 V, T = 0 ° C.
2) Nominal process, V_{DD} = 5.0 V, T = 25 ° C.
NA) Not Applicable.

V_{LO} [3]	V_{HI} [4]
1.9 V	2.9 V

3) Fast N process, slow P process, V_{DD} = 4.5 V, T = 0 ° C
4) Slow N process, fast P process, V_{DD} = 5.5 V, T = 125 ° C

Output-Stage Circuit Performance

Cell Name	Propagation Delay [1]				3-State	DC Current [2]
	T_{PHH}		T_{PLL}			
	Extrinsic	Intrinsic	Extrinsic	Intrinsic		Sink/Source
BM02M05D BM02M05T	0.266 ns/10pF 0.266 ns/10pF	1.455 ns 1.503 ns	0.226 ns/10pF 0.226 ns/10pF	1.839 ns 1.889 ns	0.685 ns 0.686 ns	11.0 mA
BM03M05D BM03M05T	0.266 ns/10pF 0.266 ns/10pF	1.449 ns 1.498 ns	0.226 ns/10pF 0.226 ns/10pF	1.835 ns 1.885 ns	0.685 ns 0.686 ns	11.0 mA
BM03M10D BM03M10T	0.959 ns/10pF 0.959 ns/10pF	0.871 ns 1.015 ns	0.894 ns/10pF 0.894 ns/10pF	1.289 ns 1.433 ns	0.551 ns 0.551 ns	3.0 mA
BM05M05D BM05M05T	0.266 ns/10pF 0.266 ns/10pF	1.443 ns 1.492 ns	0.226 ns/10pF 0.226 ns/10pF	1.829 ns 1.879 ns	0.685 ns 0.686 ns	11.0 mA
BM05M10D BM05M10T	0.959 ns/10pF 0.959 ns/10pF	0.848 ns 0.993 ns	0.894 ns/10pF 0.894 ns/10pF	1.268 ns 1.412 ns	0.551 ns 0.551 ns	3.0 mA
BM05M15D BM05M15T	1.459 ns/10pF 1.456 ns/10pF	1.820 ns 2.166 ns	1.446 ns/10pF 1.446 ns/10pF	1.260 ns 1.592 ns	0.507 ns 0.507 ns	2.0 mA
BM10M05D BM10M05T	0.266 ns/10pF 0.266 ns/10pF	1.439 ns 1.489 ns	0.226 ns/10pF 0.226 ns/10pF	1.826 ns 1.876 ns	0.685 ns 0.686 ns	11.0 mA
BM10M10D BM10M10T	0.959 ns/10pF 0.959 ns/10pF	0.836 ns 0.981 ns	0.894 ns/10pF 0.894 ns/10pF	1.257 ns 1.400 ns	0.551 ns 0.551 ns	3.0 mA
BM10M15D BM10M15T	1.459 ns/10pF 1.456 ns/10pF	1.764 ns 2.012 ns	1.446 ns/10pF 1.446 ns/10pF	1.205 ns 1.439 ns	0.507 ns 0.507 ns	2.0 mA

1) Nominal process, V_{DD} = 5.0 V, T = 25 ° C.
2) Slow process, V_{DD} = 4.5 V, T = 125 °C.

Layout Information

Cell Name	Transistors	Cell Dimensions	
		X	Y
BM02M05D BM02M05T	26	298.90 µm 175.00 µm	283.50 µm 522.90 µm
BM03M05D BM03M05T	24	295.60 µm 175.00 µm	283.50 µm 522.90 µm
BM03M10D BM03M10T	14	255.40 µm 175.00 µm	283.50 µm 522.90 µm
BM05M05D BM05M05T	24	295.60 µm 175.00 µm	283.50 µm 522.90 µm
BM05M10D BM05M10T	14	255.40 µm 175.00 µm	283.50 µm 522.90 µm
BM05M15D BM05M15T	12	249.40 µm 175.00 µm	283.50 µm 522.90 µm
BM10M05D BM10M05T	24	295.60 µm 175.00 µm	283.50 µm 522.90 µm
BM10M10D BM10M10T	14	255.40 µm 175.00 µm	283.50 µm 522.90 µm
BM10M15D BM10M15T	12	249.40 µm 175.00 µm	283.50 µm 522.90 µm

Bi-Directional Buffer

BN*idTod[D,T]*

BIN- Input Stage, BOT- Output Stage

FUNCTIONAL DESCRIPTION:

Non-Inverting, TTL-Level, Input Stage,
Non-Inverting, TTL-Level, 3-State, Output Stage

CELL NAME DEFINITIONS:

id = WCS input-stage delay in ns @ 5pF load
od = WCS output-stage delay in ns @ 50pF load
[D,T] = available layout formats

EXAMPLE: BN06T08D

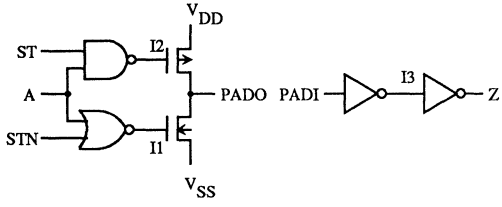
INPUTS: A, ST, STN, PADI
OUTPUTS: Z, PADO
MOTIS Gate Count: 5

5

Truth Table

Inputs				Outputs	
A	ST	STN	PADI	Z	PADO
0	X	0	0	0	0
0	X	1	0	0	HI-Z
0	X	1	1	1	HI-Z
1	0	X	0	0	HI-Z
1	0	X	1	1	HI-Z
1	1	X	1	1	1

MOTIS Model



Circuit Capacitances

Cell Name	Node				
	A	ST	STN	PAD[D]*	PAD[T]*
BN04T06	0.884 pF	0.461 pF	0.426 pF	4.381 pF	5.644 pF
BN04T10	0.307 pF	0.166 pF	0.143 pF	3.782 pF	5.073 pF
BN06T08	0.488 pF	0.267 pF	0.233 pF	3.637 pF	4.933 pF
BN06T15	0.191 pF	0.103 pF	0.091 pF	3.225 pF	4.476 pF
BN10T06	0.884 pF	0.461 pF	0.426 pF	4.249 pF	5.507 pF
BN10T10	0.307 pF	0.166 pF	0.143 pF	3.650 pF	4.937 pF
BN10T20	0.193 pF	0.104 pF	0.091 pF	3.186 pF	4.503 pF
BN15T08	0.488 pF	0.267 pF	0.233 pF	3.649 pF	4.934 pF
BN15T15	0.191 pF	0.103 pF	0.091 pF	3.237 pF	4.479 pF
BN15T30	0.154 pF	0.084 pF	0.082 pF	3.071 pF	4.506 pF
BN20T10	0.307 pF	0.166 pF	0.143 pF	3.797 pF	5.061 pF
BN20T20	0.193 pF	0.104 pF	0.091 pF	3.333 pF	4.625 pF
BN20T40	0.160 pF	0.086 pF	0.086 pF	3.088 pF	4.507 pF
BN25T15	0.191 pF	0.103 pF	0.091 pF	3.362 pF	4.584 pF
BN25T30	0.154 pF	0.084 pF	0.082 pF	3.196 pF	4.596 pF
BN25T80	0.164 pF	0.088 pF	0.088 pF	2.997 pF	4.405 pF

* Pad capacitance varies with layout format.

Input-Stage Circuit Performance

Cell Name	DC Power [1]	Propagation Delay [2]				Input Slew [1]
		T_{PHH}		T_{PLL}		
		Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BN04T06D BN04T06T	6.70 mW	0.251 ns/pF 0.249 ns/pF	0.801 ns 0.796 ns	0.168 ns/pF 0.168 ns/pF	1.393 ns 1.385 ns	>3.0 V/ms
BN04T10D BN04T10T	6.70 mW	0.251 ns/pF 0.249 ns/pF	0.801 ns 0.796 ns	0.168 ns/pF 0.168 ns/pF	1.393 ns 1.385 ns	>3.0 V/ms
BN06T08D BN06T08T	3.35 mW	0.365 ns/pF 0.364 ns/pF	0.788 ns 0.783 ns	0.319 ns/pF 0.318 ns/pF	1.691 ns 1.684 ns	>2.4 V/ms
BN06T15D BN06T15T	3.35 mW	0.365 ns/pF 0.364 ns/pF	0.788 ns 0.783 ns	0.319 ns/pF 0.318 ns/pF	1.691 ns 1.684 ns	>2.4 V/ms
BN10T06D BN10T06T	1.53 mW	0.822 ns/pF 0.821 ns/pF	0.912 ns 0.912 ns	0.676 ns/pF 0.675 ns/pF	2.077 ns 2.078 ns	>1.3 V/ms
BN10T10D BN10T10T	1.53 mW	0.822 ns/pF 0.821 ns/pF	0.912 ns 0.912 ns	0.676 ns/pF 0.675 ns/pF	2.077 ns 2.078 ns	>1.3 V/ms
BN10T20D BN10T20T	1.53 mW	0.822 ns/pF 0.821 ns/pF	0.912 ns 0.912 ns	0.676 ns/pF 0.675 ns/pF	2.077 ns 2.078 ns	>1.3 V/ms
BN15T08D BN15T08T	0.82 mW	1.312 ns/pF 1.312 ns/pF	1.185 ns 1.189 ns	1.040 ns/pF 1.041 ns/pF	2.972 ns 2.976 ns	>0.63 V/ms
BN15T15D BN15T15T	0.82 mW	1.312 ns/pF 1.312 ns/pF	1.185 ns 1.189 ns	1.040 ns/pF 1.041 ns/pF	2.972 ns 2.976 ns	>0.63 V/ms
BN15T30D BN15T30T	0.82 mW	1.312 ns/pF 1.312 ns/pF	1.185 ns 1.189 ns	1.040 ns/pF 1.041 ns/pF	2.972 ns 2.976 ns	>0.63 V/ms
BN20T10D BN20T10T	0.53 mW	1.813 ns/pF 1.811 ns/pF	1.656 ns 1.671 ns	1.329 ns/pF 1.329 ns/pF	4.401 ns 4.396 ns	>0.36 V/ms
BN20T20D BN20T20T	0.53 mW	1.813 ns/pF 1.811 ns/pF	1.656 ns 1.671 ns	1.329 ns/pF 1.329 ns/pF	4.401 ns 4.396 ns	>0.36 V/ms
BN20T40D BN20T40T	0.53 mW	1.813 ns/pF 1.811 ns/pF	1.656 ns 1.671 ns	1.329 ns/pF 1.329 ns/pF	4.401 ns 4.396 ns	>0.36 V/ms
BN25T15D BN25T15T	0.37 mW	2.215 ns/pF 2.213 ns/pF	1.992 ns 2.013 ns	1.657 ns/pF 1.659 ns/pF	5.384 ns 5.381 ns	>0.29 V/ms
BN25T30D BN25T30T	0.37 mW	2.215 ns/pF 2.213 ns/pF	1.992 ns 2.013 ns	1.657 ns/pF 1.659 ns/pF	5.384 ns 5.381 ns	>0.29 V/ms
BN25T80D BN25T80T	0.37 mW	2.215 ns/pF 2.213 ns/pF	1.992 ns 2.013 ns	1.657 ns/pF 1.659 ns/pF	5.384 ns 5.381 ns	>0.29 V/ms

1) Fast process, V_{DD} = 5.5 V, T = 0 ° C.
2) Nominal process, V_{DD} = 5.0 V, T = 25 ° C.

V_{LO} [3]	V_{HI} [4]
1.1 V	1.7 V

3) Fast N process, slow P process, V_{DD} = 4.5 V, T = 125 ° C
4) Slow N process, fast P process, V_{DD} = 5.5 V, T = 0 ° C

Output-Stage Circuit Performance

Cell Name	Propagation Delay [1]				3-State	DC Current [2]
	T_{PHH}		T_{PLL}			
	Extrinsic	Intrinsic	Extrinsic	Intrinsic		Sink/Source
BN04T06D	0.319 ns/10pF	1.432 ns	0.282 ns/10pF	1.904 ns	0.480 ns	24.0 mA
BN04T06T	0.319 ns/10pF	1.483 ns	0.281 ns/10pF	1.951 ns	0.480 ns	
BN04T10D	0.751 ns/10pF	1.716 ns	0.615 ns/10pF	2.328 ns	0.743 ns	10.0 mA
BN04T10T	0.751 ns/10pF	1.817 ns	0.615 ns/10pF	2.418 ns	0.744 ns	
BN06T08D	0.582 ns/10pF	1.401 ns	0.495 ns/10pF	1.880 ns	0.576 ns	12.0 mA
BN06T08T	0.582 ns/10pF	1.439 ns	0.495 ns/10pF	1.941 ns	0.577 ns	
BN06T15D	0.986 ns/10pF	2.433 ns	0.808 ns/10pF	3.102 ns	1.050 ns	8.0 mA
BN06T15T	0.986 ns/10pF	2.550 ns	0.808 ns/10pF	3.202 ns	1.050 ns	
BN10T06D	0.319 ns/10pF	1.428 ns	0.282 ns/10pF	1.900 ns	0.480 ns	24.0 mA
BN10T06T	0.319 ns/10pF	1.478 ns	0.281 ns/10pF	1.947 ns	0.480 ns	
BN10T10D	0.751 ns/10pF	1.706 ns	0.615 ns/10pF	2.320 ns	0.743 ns	10.0 mA
BN10T10T	0.751 ns/10pF	1.807 ns	0.615 ns/10pF	2.409 ns	0.744 ns	
BN10T20D	2.016 ns/10pF	1.725 ns	1.716 ns/10pF	2.019 ns	0.609 ns	4.0 mA
BN10T20T	2.016 ns/10pF	1.974 ns	1.716 ns/10pF	2.239 ns	0.610 ns	
BN15T08D	0.582 ns/10pF	1.401 ns	0.495 ns/10pF	1.881 ns	0.576 ns	12.0 mA
BN15T08T	0.582 ns/10pF	1.439 ns	0.495 ns/10pF	1.941 ns	0.577 ns	
BN15T15D	0.986 ns/10pF	2.434 ns	0.808 ns/10pF	3.103 ns	1.050 ns	8.0 mA
BN15T15T	0.986 ns/10pF	2.550 ns	0.808 ns/10pF	3.203 ns	1.050 ns	
BN15T30D	2.866 ns/10pF	1.544 ns	2.399 ns/10pF	2.610 ns	0.739 ns	3.0 mA
BN15T30T	2.866 ns/10pF	1.919 ns	2.399 ns/10pF	2.930 ns	0.740 ns	
BN20T10D	0.751 ns/10pF	1.717 ns	0.615 ns/10pF	2.329 ns	0.743 ns	10.0 mA
BN20T10T	0.751 ns/10pF	1.816 ns	0.615 ns/10pF	2.417 ns	0.744 ns	
BN20T20D	2.016 ns/10pF	1.755 ns	1.716 ns/10pF	2.044 ns	0.609 ns	4.0 mA
BN20T20T	2.016 ns/10pF	1.998 ns	1.716 ns/10pF	2.260 ns	0.610 ns	
BN20T40D	4.278 ns/10pF	1.692 ns	3.613 ns/10pF	2.450 ns	0.582 ns	2.0 mA
BN20T40T	4.278 ns/10pF	2.230 ns	3.613 ns/10pF	2.912 ns	0.583 ns	
BN25T15D	0.986 ns/10pF	2.446 ns	0.808 ns/10pF	3.113 ns	1.050 ns	8.0 mA
BN25T15T	0.986 ns/10pF	2.561 ns	0.808 ns/10pF	3.211 ns	1.050 ns	
BN25T30D	2.866 ns/10pF	1.580 ns	2.399 ns/10pF	2.640 ns	0.739 ns	3.0 mA
BN25T30T	2.866 ns/10pF	1.945 ns	2.399 ns/10pF	2.952 ns	0.740 ns	
BN25T80D	7.359 ns/10pF	7.727 ns	7.425 ns/10pF	2.784 ns	0.421 ns	1.0 mA
BN25T80T	7.359 ns/10pF	9.484 ns	7.425 ns/10pF	3.694 ns	0.421 ns	

1) Nominal process, V_{DD} = 5.0 V, T = 25 ° C.
2) Slow process, V_{DD} = 4.5 V, T = 125 ° C.

Layout Information

Cell Name	Transistors	Cell Dimensions	
		X	Y
BN04T06D BN04T06T	24	294.70 µm 175.00 µm	283.50 µm 522.90 µm
BN04T10D BN04T10T	18	273.30 µm 175.00 µm	283.50 µm 522.90 µm
BN06T08D BN06T08T	20	279.30 µm 175.00 µm	283.50 µm 522.90 µm
BN06T15D BN06T15T	16	263.90 µm 175.00 µm	283.50 µm 522.90 µm
BN10T06D BN10T06T	24	295.20 µm 175.00 µm	283.50 µm 522.90 µm
BN10T10D BN10T10T	18	273.80 µm 175.00 µm	283.50 µm 522.90 µm
BN10T20D BN10T20T	14	258.40 µm 175.00 µm	283.50 µm 522.90 µm
BN15T08D BN15T08T	20	280.80 µm 175.00 µm	283.50 µm 522.90 µm
BN15T15D BN15T15T	16	265.40 µm 175.00 µm	283.50 µm 522.90 µm
BN15T30D BN15T30T	14	259.40 µm 175.00 µm	283.50 µm 522.90 µm
BN20T10D BN20T10T	18	276.80 µm 175.00 µm	283.50 µm 522.90 µm
BN20T20D BN20T20T	14	261.40 µm 175.00 µm	283.50 µm 522.90 µm
BN20T40D BN20T40T	14	261.40 µm 175.00 µm	283.50 µm 522.90 µm
BN25T15D BN25T15T	16	268.40 µm 175.00 µm	283.50 µm 522.90 µm
BN25T30D BN25T30T	14	262.40 µm 175.00 µm	283.50 µm 522.90 µm
BN25T80D BN25T80T	14	262.40 µm 175.00 µm	283.50 µm 522.90 µm

Bi-Directional Buffer

BN*idXod[D,T]*

BIN- Input Stage, BOX- Output Stage

FUNCTIONAL DESCRIPTION:

Non-Inverting, TTL-Level, Input Stage with Hysteresis,
Driver Transistors Only, (No Inherent Logic) Output Stage

CELL NAME DEFINITIONS:

id = WCS input-stage delay in ns @ 5pF load
od = WCS output-stage delay in ns @ 50pF load
[D,T] = available layout formats

EXAMPLE: BN06X08D

INPUTS: N, P, PADI
OUTPUTS: Z, PADO
MOTIS Gate Count: 3

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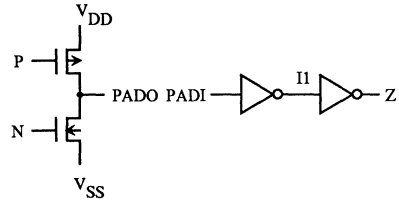
Truth Table

Inputs			Outputs	
N	P	PADI	Z	PADO
0	0	1	1	1
0	1	0	0	HI-Z
0	1	1	1	HI-Z
1	1	0	0	0

MOTIS Model



Circuit Capacitances

Cell Name	Node			
	N	P	PAD[D]*	PAD[T]*
BN04X06	1.663 pF	1.914 pF	4.381 pF	5.644 pF
BN04X10	0.821 pF	0.820 pF	3.791 pF	5.082 pF
BN06X08	1.073 pF	1.072 pF	3.637 pF	4.933 pF
BN06X15	0.601 pF	0.615 pF	3.225 pF	4.476 pF
BN10X06	1.662 pF	1.914 pF	4.249 pF	5.508 pF
BN10X10	0.821 pF	0.820 pF	3.659 pF	4.945 pF
BN10X20	0.282 pF	0.302 pF	3.186 pF	4.503 pF
BN15X08	1.073 pF	1.072 pF	3.649 pF	4.934 pF
BN15X15	0.601 pF	0.615 pF	3.237 pF	4.479 pF
BN15X30	0.211 pF	0.223 pF	3.071 pF	4.506 pF
BN20X10	0.821 pF	0.820 pF	3.806 pF	5.069 pF
BN20X20	0.282 pF	0.302 pF	3.333 pF	4.625 pF
BN20X40	0.155 pF	0.162 pF	3.079 pF	4.498 pF
BN25X15	0.601 pF	0.615 pF	3.362 pF	4.584 pF
BN25X30	0.211 pF	0.223 pF	3.196 pF	4.596 pF
BN25X80	0.098 pF	0.100 pF	2.988 pF	4.396 pF

* Pad capacitance varies with layout format.

Input-Stage Circuit Performance

Cell Name	DC Power [1]	Propagation Delay [2]				Input Slew [1]
		T_{PHH}		T_{PLL}		
		Extrinsic	Intrinsic	Extrinsic	Intrinsic	
BN04X06D BN04X06T	6.70 mW	0.251 ns/pF 0.249 ns/pF	0.801 ns 0.796 ns	0.168 ns/pF 0.168 ns/pF	1.393 ns 1.385 ns	>3.0 V/ms
BN04X10D BN04X10T	6.70 mW	0.251 ns/pF 0.249 ns/pF	0.801 ns 0.796 ns	0.168 ns/pF 0.168 ns/pF	1.393 ns 1.385 ns	>3.0 V/ms
BN06X08D BN06X08T	3.35 mW	0.365 ns/pF 0.364 ns/pF	0.788 ns 0.783 ns	0.319 ns/pF 0.318 ns/pF	1.691 ns 1.684 ns	>2.4 V/ms
BN06X15D BN06X15T	3.35 mW	0.365 ns/pF 0.364 ns/pF	0.788 ns 0.783 ns	0.319 ns/pF 0.318 ns/pF	1.691 ns 1.684 ns	>2.4 V/ms
BN10X06D BN10X06T	1.53 mW	0.822 ns/pF 0.821 ns/pF	0.912 ns 0.912 ns	0.676 ns/pF 0.675 ns/pF	2.077 ns 2.078 ns	>1.3 V/ms
BN10X10D BN10X10T	1.53 mW	0.822 ns/pF 0.821 ns/pF	0.912 ns 0.912 ns	0.676 ns/pF 0.675 ns/pF	2.077 ns 2.078 ns	>1.3 V/ms
BN10X20D BN10X20T	1.53 mW	0.822 ns/pF 0.821 ns/pF	0.912 ns 0.912 ns	0.676 ns/pF 0.675 ns/pF	2.077 ns 2.078 ns	>1.3 V/ms
BN15X08D BN15X08T	0.82 mW	1.312 ns/pF 1.312 ns/pF	1.185 ns 1.189 ns	1.040 ns/pF 1.041 ns/pF	2.972 ns 2.976 ns	>0.63 V/ms
BN15X15D BN15X15T	0.82 mW	1.312 ns/pF 1.312 ns/pF	1.185 ns 1.189 ns	1.040 ns/pF 1.041 ns/pF	2.972 ns 2.976 ns	>0.63 V/ms
BN15X30D BN15X30T	0.82 mW	1.312 ns/pF 1.312 ns/pF	1.185 ns 1.189 ns	1.040 ns/pF 1.041 ns/pF	2.972 ns 2.976 ns	>0.63 V/ms
BN20X10D BN20X10T	0.53 mW	1.813 ns/pF 1.811 ns/pF	1.656 ns 1.671 ns	1.329 ns/pF 1.329 ns/pF	4.401 ns 4.396 ns	>0.36 V/ms
BN20X20D BN20X20T	0.53 mW	1.813 ns/pF 1.811 ns/pF	1.656 ns 1.671 ns	1.329 ns/pF 1.329 ns/pF	4.401 ns 4.396 ns	>0.36 V/ms
BN20X40D BN20X40T	0.53 mW	1.813 ns/pF 1.811 ns/pF	1.656 ns 1.671 ns	1.329 ns/pF 1.329 ns/pF	4.401 ns 4.396 ns	>0.36 V/ms
BN25X15D BN25X15T	0.37 mW	2.215 ns/pF 2.213 ns/pF	1.992 ns 2.013 ns	1.657 ns/pF 1.659 ns/pF	5.384 ns 5.381 ns	>0.29 V/ms
BN25X30D BN25X30T	0.37 mW	2.215 ns/pF 2.213 ns/pF	1.992 ns 2.013 ns	1.657 ns/pF 1.659 ns/pF	5.384 ns 5.381 ns	>0.29 V/ms
BN25X80D BN25X80T	0.37 mW	2.215 ns/pF 2.213 ns/pF	1.992 ns 2.013 ns	1.657 ns/pF 1.659 ns/pF	5.384 ns 5.381 ns	>0.29 V/ms

1) Fast process, V_{DD} = 5.5 V, T = 0 ° C.
2) Nominal process, V_{DD} = 5.0 V, T = 25 ° C.

V_{LO} [3]	V_{HI} [4]
1.1 V	1.7 V

3) Fast N process, slow P process, V_{DD} = 4.5 V, T = 125 ° C
4) Slow N process, fast P process, V_{DD} = 5.5 V, T = 0 ° C

Output-Stage Circuit Performance

Cell Name	Propagation Delay [1]				DC Current [2]
	T_{PHL}		T_{PLH}		
	Extrinsic	Intrinsic	Extrinsic	Intrinsic	Sink/Source
BN04X06D BN04X06T	0.317 ns/10pF 0.317 ns/10pF	1.584 ns 1.636 ns	0.303 ns/10pF 0.302 ns/10pF	1.557 ns 1.615 ns	24.0 mA
BN04X10D BN04X10T	0.748 ns/10pF 0.748 ns/10pF	0.826 ns 0.928 ns	0.611 ns/10pF 0.611 ns/10pF	1.066 ns 1.151 ns	10.0 mA
BN06X08D BN06X08T	0.582 ns/10pF 0.581 ns/10pF	0.964 ns 1.046 ns	0.500 ns/10pF 0.499 ns/10pF	1.142 ns 1.228 ns	12.0 mA
BN06X15D BN06X15T	0.984 ns/10pF 0.984 ns/10pF	0.652 ns 0.765 ns	0.800 ns/10pF 0.799 ns/10pF	0.892 ns 0.991 ns	8.0 mA
BN10X06D BN10X06T	0.317 ns/10pF 0.317 ns/10pF	1.580 ns 1.631 ns	0.303 ns/10pF 0.302 ns/10pF	1.553 ns 1.611 ns	24.0 mA
BN10X10D BN10X10T	0.748 ns/10pF 0.748 ns/10pF	0.816 ns 0.918 ns	0.611 ns/10pF 0.611 ns/10pF	1.058 ns 1.143 ns	10.0 mA
BN10X20D BN10X20T	2.016 ns/10pF 2.016 ns/10pF	0.709 ns 0.951 ns	1.710 ns/10pF 1.710 ns/10pF	0.832 ns 1.037 ns	4.0 mA
BN15X08D BN15X08T	0.582 ns/10pF 0.581 ns/10pF	0.964 ns 1.046 ns	0.500 ns/10pF 0.499 ns/10pF	1.143 ns 1.228 ns	12.0 mA
BN15X15D BN15X15T	0.984 ns/10pF 0.984 ns/10pF	0.653 ns 0.765 ns	0.800 ns/10pF 0.799 ns/10pF	0.892 ns 0.991 ns	8.0 mA
BN15X30D BN15X30T	2.866 ns/10pF 2.866 ns/10pF	0.840 ns 1.206 ns	2.339 ns/10pF 2.338 ns/10pF	1.153 ns 1.478 ns	3.0 mA
BN20X10D BN20X10T	0.748 ns/10pF 0.748 ns/10pF	0.827 ns 0.927 ns	0.611 ns/10pF 0.611 ns/10pF	1.067 ns 1.151 ns	10.0 mA
BN20X20D BN20X20T	2.016 ns/10pF 2.016 ns/10pF	0.739 ns 0.976 ns	1.710 ns/10pF 1.710 ns/10pF	0.857 ns 1.058 ns	4.0 mA
BN20X40D BN20X40T	4.285 ns/10pF 4.285 ns/10pF	1.135 ns 1.660 ns	3.181 ns/10pF 3.173 ns/10pF	3.225 ns 3.702 ns	2.0 mA
BN25X15D BN25X15T	0.984 ns/10pF 0.984 ns/10pF	0.665 ns 0.775 ns	0.800 ns/10pF 0.799 ns/10pF	0.902 ns 0.999 ns	8.0 mA
BN25X30D BN25X30T	2.866 ns/10pF 2.866 ns/10pF	0.876 ns 1.232 ns	2.339 ns/10pF 2.338 ns/10pF	1.182 ns 1.499 ns	3.0 mA
BN25X80D BN25X80T	8.582 ns/10pF 8.582 ns/10pF	1.968 ns 2.980 ns	3.723 ns/10pF 3.694 ns/10pF	20.022 ns 20.863 ns	1.0 mA

1) Nominal process, V_{DD} = 5.0 V, T = 25 ° C.
2) Slow process, V_{DD} = 4.5 V, T = 125 ° C.

Layout Information

Cell Name	Transistors	Cell Dimensions	
		X	Y
BN04X06D BN04X06T	16	275.90 µm 175.00 µm	283.50 µm 522.90 µm
BN04X10D BN04X10T	10	254.50 µm 175.00 µm	283.50 µm 522.90 µm
BN06X08D BN06X08T	12	260.50 µm 175.00 µm	283.50 µm 522.90 µm
BN06X15D BN06X15T	8	245.10 µm 175.00 µm	283.50 µm 522.90 µm
BN10X06D BN10X06T	16	276.40 µm 175.00 µm	283.50 µm 522.90 µm
BN10X10D BN10X10T	10	255.00 µm 175.00 µm	283.50 µm 522.90 µm
BN10X20D BN10X20T	6	239.60 µm 175.00 µm	283.50 µm 522.90 µm
BN15X08D BN15X08T	12	262.00 µm 175.00 µm	283.50 µm 522.90 µm
BN15X15D BN15X15T	8	246.60 µm 175.00 µm	283.50 µm 522.90 µm
BN15X30D BN15X30T	6	240.60 µm 175.00 µm	283.50 µm 522.90 µm
BN20X10D BN20X10T	10	258.00 µm 175.00 µm	283.50 µm 522.90 µm
BN20X20D BN20X20T	6	242.60 µm 175.00 µm	283.50 µm 522.90 µm
BN20X40D BN20X40T	6	242.60 µm 175.00 µm	283.50 µm 522.90 µm
BN25X15D BN25X15T	8	249.60 µm 175.00 µm	283.50 µm 522.90 µm
BN25X30D BN25X30T	6	243.60 µm 175.00 µm	283.50 µm 522.90 µm
BN25X80D BN25X80T	6	243.60 µm 175.00 µm	283.50 µm 522.90 µm

Output Buffer

BOC*od[D,T]*

FUNCTIONAL DESCRIPTION:

Non-Inverting, TTL-Level, Open-Collector, Output Buffer

CELL NAME DEFINITIONS:

od = WCS delay in ns @ 50pF load
[D,T] = available layout formats

EXAMPLE: BOC06D

INPUTS: A
OUTPUTS: Z
MOTIS Gate Count: 2

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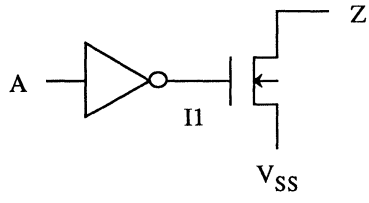
Truth Table

Input	Output
A	Z
0	0
1	HI-Z

MOTIS Model



Circuit Capacitances

Cell Name	Node		
	A	Z[D]*	Z[T]*
BOC06	0.409 pF	3.990 pF	4.842 pF
BOC08	0.170 pF	3.362 pF	4.232 pF
BOC10	0.119 pF	3.394 pF	4.280 pF
BOC15	0.077 pF	2.950 pF	3.864 pF
BOC20	0.078 pF	2.931 pF	3.864 pF
BOC30	0.067 pF	2.786 pF	3.719 pF
BOC40	0.068 pF	2.686 pF	3.619 pF
BOC80	0.070 pF	2.586 pF	3.520 pF

* Pad capacitance varies with layout format.

Circuit Performance

Cell Name	Propagation Delay [1] T_{PLL}		DC Current [2]
	Extrinsic	Intrinsic	Sink
BOC06D BOC06T	0.272 ns/10pF 0.272 ns/10pF	0.945 ns 0.990 ns	24.0 mA
BOC08D BOC08T	0.487 ns/10pF 0.488 ns/10pF	1.126 ns 1.176 ns	12.0 mA
BOC10D BOC10T	0.606 ns/10pF 0.608 ns/10pF	1.335 ns 1.398 ns	10.0 mA
BOC15D BOC15T	0.798 ns/10pF 0.799 ns/10pF	1.841 ns 1.913 ns	8.0 mA
BOC20D BOC20T	1.708 ns/10pF 1.711 ns/10pF	1.207 ns 1.354 ns	4.0 mA
BOC30D BOC30T	2.389 ns/10pF 2.392 ns/10pF	1.625 ns 1.818 ns	3.0 mA
BOC40D BOC40T	3.602 ns/10pF 3.615 ns/10pF	1.564 ns 1.844 ns	2.0 mA
BOC80D BOC80T	7.407 ns/10pF 7.411 ns/10pF	1.918 ns 2.463 ns	1.0 mA

1) Nominal process, V_{DD} = 5.0 V, T = 25 ° C.
2) Slow process, V_{DD} = 4.5 V, T = 125 °C.

Layout Information

Cell Name	Transistors	Cell Dimensions	
		X	Y
BOC06D BOC06T	14	245.35 µm 175.00 µm	283.50 µm 522.90 µm
BOC08D BOC08T	10	229.95 µm 175.00 µm	283.50 µm 522.90 µm
BOC10D BOC10T	8	223.95 µm 175.00 µm	283.50 µm 522.90 µm
BOC15D BOC15T	6	214.55 µm 175.00 µm	283.50 µm 522.90 µm
BOC20D BOC20T	4	208.55 µm 175.00 µm	283.50 µm 522.90 µm
BOC30D BOC30T	4	208.55 µm 175.00 µm	283.50 µm 522.90 µm
BOC40D BOC40T	4	208.55 µm 175.00 µm	283.50 µm 522.90 µm
BOC80D BOC80T	4	208.55 µm 175.00 µm	283.50 µm 522.90 µm

Output Buffer

BOM*od[D,T]*

FUNCTIONAL DESCRIPTION:

Non-Inverting, MOS-Level, 3-State, Output Buffer

CELL NAME DEFINITIONS:

od = WCS delay in ns @ 50pF load

[D,T] = available layout formats

EXAMPLE: BOM05D

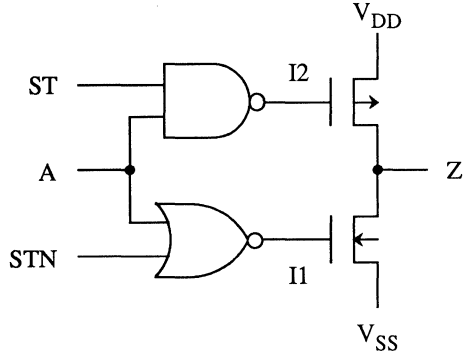
INPUTS: A, ST, STN
OUTPUTS: Z
MOTIS Gate Count: 3

5

Truth Table

Inputs			Output
A	ST	STN	Z
0	X	0	0
0	X	1	HI-Z
1	0	X	HI-Z
1	1	X	1

MOTIS Model



Circuit Capacitances

Cell Name	Node				
	A	ST	STN	Z[D]*	Z[T]*
BOM05	0.754 pF	0.368 pF	0.389 pF	3.837 pF	4.897 pF
BOM10	0.457 pF	0.229 pF	0.231 pF	2.749 pF	3.620 pF
BOM15	0.284 pF	0.150 pF	0.137 pF	2.828 pF	3.720 pF

* Pad capacitance varies with layout format.

Circuit Performance

Cell Name	Propagation Delay [1]					DC Current [2]
	T_{PHH}		T_{PLL}		3-State	
	Extrinsic	Intrinsic	Extrinsic	Intrinsic		Sink/Source
BOM05D	0.266 ns/10pF	1.433 ns	0.226 ns/10pF	1.821 ns	0.685 ns	11.0 mA
BOM05T	0.266 ns/10pF	1.474 ns	0.226 ns/10pF	1.864 ns	0.686 ns	
BOM10D	0.959 ns/10pF	0.812 ns	0.894 ns/10pF	1.234 ns	0.551 ns	3.0 mA
BOM10T	0.959 ns/10pF	0.890 ns	0.894 ns/10pF	1.316 ns	0.551 ns	
BOM15D	1.459 ns/10pF	1.727 ns	1.446 ns/10pF	1.168 ns	0.507 ns	2.0 mA
BOM15T	1.456 ns/10pF	1.877 ns	1.446 ns/10pF	1.305 ns	0.507 ns	

1) Nominal process, V_{DD} = 5.0 V, T = 25 ° C.
2) Slow process, V_{DD} = 4.5 V, T = 125 ° C.

5

Layout Information

Cell Name	Transistors	Cell Dimensions	
		X	Y
BOM05D	22	269.95 µm	283.50 µm
BOM05T		175.00 µm	522.90 µm
BOM10D	12	229.75 µm	283.50 µm
BOM10T		175.00 µm	522.90 µm
BOM15D	10	223.75 µm	283.50 µm
BOM15T		175.00 µm	522.90 µm

Output Buffer

BON*od[D,T]*

FUNCTIONAL DESCRIPTION:

Non-Inverting, TTL-Level, Output Buffer

CELL NAME DEFINITIONS:

od = WCS delay in ns @ 50pF load
[D,T] = available layout formats

EXAMPLE: BON06D

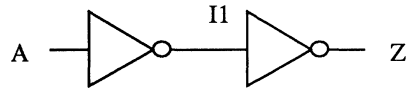
INPUTS: A
OUTPUTS: Z
MOTIS Gate Count: 2

5

Truth Table

Input	Output
A	Z
0	0
1	1

MOTIS Model



Circuit Capacitances

Cell Name	Node		
	A	Z[D]*	Z[T]*
BON06	0.409 pF	3.989 pF	4.841 pF
BON08	0.170 pF	3.362 pF	4.232 pF
BON10	0.119 pF	3.393 pF	4.280 pF
BON15	0.077 pF	2.950 pF	3.864 pF
BON20	0.078 pF	2.931 pF	3.864 pF
BON30	0.067 pF	2.786 pF	3.720 pF
BON40	0.068 pF	2.686 pF	3.619 pF
BON80	0.070 pF	2.586 pF	3.519 pF

* Pad capacitance varies with layout format.

Circuit Performance

Cell Name	Propagation Delay [1]				DC Current [2]
	T_{PHH}		T_{PLL}		
	Extrinsic	Intrinsic	Extrinsic	Intrinsic	Sink/Source
BON06D BON06T	0.317 ns/10pF 0.316 ns/10pF	1.693 ns 1.732 ns	0.275 ns/10pF 0.275 ns/10pF	1.358 ns 1.403 ns	24.0 mA
BON08D BON08T	0.581 ns/10pF 0.581 ns/10pF	1.614 ns 1.670 ns	0.493 ns/10pF 0.493 ns/10pF	1.955 ns 1.995 ns	12.0 mA
BON10D BON10T	0.750 ns/10pF 0.750 ns/10pF	1.799 ns 1.869 ns	0.612 ns/10pF 0.612 ns/10pF	2.444 ns 2.499 ns	10.0 mA
BON15D BON15T	0.983 ns/10pF 0.983 ns/10pF	2.816 ns 2.897 ns	0.806 ns/10pF 0.806 ns/10pF	3.621 ns 3.692 ns	8.0 mA
BON20D BON20T	2.016 ns/10pF 2.016 ns/10pF	1.739 ns 1.909 ns	1.716 ns/10pF 1.716 ns/10pF	2.056 ns 1.209 ns	4.0 mA
BON30D BON30T	2.866 ns/10pF 2.866 ns/10pF	1.537 ns 1.762 ns	2.398 ns/10pF 2.398 ns/10pF	2.764 ns 2.963 ns	3.0 mA
BON40D BON40T	4.285 ns/10pF 4.285 ns/10pF	1.539 ns 1.859 ns	3.613 ns/10pF 3.613 ns/10pF	2.356 ns 2.635 ns	2.0 mA
BON80D BON80T	8.303 ns/10pF 8.303 ns/10pF	3.365 ns 4.011 ns	7.425 ns/10pF 7.425 ns/10pF	2.361 ns 2.904 ns	1.0 mA

1) Nominal process, V_{DD} = 5.0 V, T = 25 ° C.
2) Slow process, V_{DD} = 4.5 V, T = 125 ° C.

Layout Information

Cell Name	Transistors	Cell Dimensions	
		X	Y
BON06D BON06T	14	245.35 µm 175.00 µm	283.50 µm 522.90 µm
BON08D BON08T	10	229.95 µm 175.00 µm	283.50 µm 522.90 µm
BON10D BON10T	8	223.95 µm 175.00 µm	283.50 µm 522.90 µm
BON15D BON15T	6	214.55 µm 175.00 µm	283.50 µm 522.90 µm
BON20D BON20T	4	208.55 µm 175.00 µm	283.50 µm 522.90 µm
BON30D BON30T	4	208.55 µm 175.00 µm	283.50 µm 522.90 µm
BON40D BON40T	4	208.55 µm 175.00 µm	283.50 µm 522.90 µm
BON80D BON80T	4	208.55 µm 175.00 µm	283.50 µm 522.90 µm

Output Buffer

BOT*od[D,T]*

FUNCTIONAL DESCRIPTION:

Non-Inverting, TTL-Level, 3-State, Output Buffer

CELL NAME DEFINITIONS:

od = WCS delay in ns @ 50pF load
[D,T] = available layout formats

EXAMPLE: BOT06D

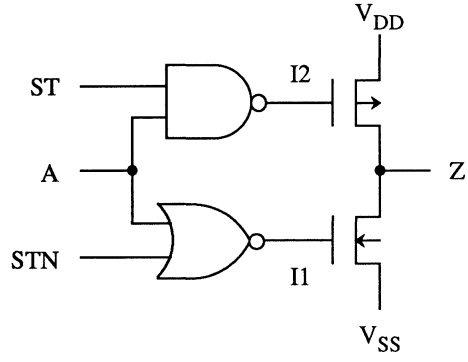
INPUTS: A, ST, STN
OUTPUTS: Z
MOTIS Gate Count: 3

5

Truth Table

Inputs			Output
A	ST	STN	Z
0	X	0	0
0	X	1	HI-Z
1	0	X	HI-Z
1	1	X	1

MOTIS Model



Circuit Capacitances

Cell Name	Node				
	A	ST	STN	Z[D]*	Z[T]*
BOT06	0.884 pF	0.461 pF	0.426 pF	3.990 pF	4.953 pF
BOT08	0.488 pF	0.267 pF	0.233 pF	3.362 pF	4.221 pF
BOT10	0.307 pF	0.166 pF	0.143 pF	3.393 pF	4.239 pF
BOT15	0.191 pF	0.103 pF	0.091 pF	2.950 pF	3.823 pF
BOT20	0.193 pF	0.104 pF	0.091 pF	2.931 pF	3.823 pF
BOT30	0.154 pF	0.084 pF	0.082 pF	2.786 pF	3.678 pF
BOT40	0.160 pF	0.086 pF	0.086 pF	2.686 pF	3.578 pF
BOT80	0.164 pF	0.088 pF	0.088 pF	2.586 pF	3.478 pF

* Pad capacitance varies with layout format.

Circuit Performance

Cell Name	Propagation Delay [1]					DC Current [2]
	T_{PHH}		T_{PLL}		3-State	
	Extrinsic	Intrinsic	Extrinsic	Intrinsic		Sink/Source
BOT06D	0.319 ns/10pF	1.420 ns	0.282 ns/10pF	1.893 ns	0.480 ns	24.0 mA
BOT06T	0.319 ns/10pF	1.461 ns	0.281 ns/10pF	1.932 ns	0.480 ns	
BOT08D	0.582 ns/10pF	1.385 ns	0.495 ns/10pF	1.867 ns	0.576 ns	12.0 mA
BOT08T	0.582 ns/10pF	1.398 ns	0.495 ns/10pF	1.906 ns	0.577 ns	
BOT10D	0.751 ns/10pF	1.687 ns	0.615 ns/10pF	2.305 ns	0.743 ns	10.0 mA
BOT10T	0.751 ns/10pF	1.755 ns	0.615 ns/10pF	2.367 ns	0.744 ns	
BOT15D	0.986 ns/10pF	2.406 ns	0.808 ns/10pF	3.080 ns	1.050 ns	8.0 mA
BOT15T	0.986 ns/10pF	2.486 ns	0.808 ns/10pF	3.150 ns	1.050 ns	
BOT20D	2.016 ns/10pF	1.674 ns	1.716 ns/10pF	1.976 ns	0.609 ns	4.0 mA
BOT20T	2.016 ns/10pF	1.837 ns	1.716 ns/10pF	2.123 ns	0.610 ns	
BOT30D	2.866 ns/10pF	1.463 ns	2.399 ns/10pF	2.542 ns	0.739 ns	3.0 mA
BOT30T	2.866 ns/10pF	1.682 ns	2.399 ns/10pF	2.732 ns	0.740 ns	
BOT40D	4.278 ns/10pF	1.521 ns	3.613 ns/10pF	2.305 ns	0.582 ns	2.0 mA
BOT40T	4.278 ns/10pF	1.833 ns	3.613 ns/10pF	2.577 ns	0.583 ns	
BOT80D	7.359 ns/10pF	7.425 ns	7.425 ns/10pF	2.479 ns	0.421 ns	1.0 mA
BOT80T	7.359 ns/10pF	8.802 ns	7.425 ns/10pF	3.006 ns	0.421 ns	

1) Nominal process, V_{DD} = 5.0 V, T = 25 ° C.
2) Slow process, V_{DD} = 4.5 V, T = 125 ° C.

Layout Information

Cell Name	Transistors	Cell Dimensions	
		X	Y
BOT06D	20	260.55 µm	283.50 µm
BOT06T		175.00 µm	522.90 µm
BOT08D	16	245.15 µm	283.50 µm
BOT08T		175.00 µm	522.90 µm
BOT10D	14	239.15 µm	283.50 µm
BOT10T		175.00 µm	522.90 µm
BOT15D	12	229.75 µm	283.50 µm
BOT15T		175.00 µm	522.90 µm
BOT20D	10	223.75 µm	283.50 µm
BOT20T		175.00 µm	522.90 µm
BOT30D	10	223.75 µm	283.50 µm
BOT30T		175.00 µm	522.90 µm
BOT40D	10	223.75 µm	283.50 µm
BOT40T		175.00 µm	522.90 µm
BOT80D	10	223.75 µm	283.50 µm
BOT80T		175.00 µm	522.90 µm

FUNCTIONAL DESCRIPTION:

Driver Transistors Only (No Inherent Logic) Output Buffer

CELL NAME DEFINITIONS:

od = WCS delay in ns @ 50pF load
[D,T] = available layout formats

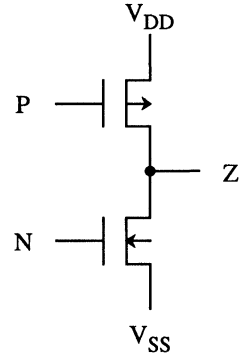
EXAMPLE: BOX06D

INPUTS: N, P
OUTPUTS: Z
MOTIS Gate Count: 1

Truth Table

Inputs		Outputs
N	P	Z
0	0	1
0	1	HI-Z
1	1	0

MOTIS Model



Circuit Capacitances

Cell Name	Node			
	N	P	Z[D]*	Z[T]*
BOX06	1.663 pF	1.914 pF	3.990 pF	4.821 pF
BOX08	1.074 pF	1.072 pF	3.362 pF	4.242 pF
BOX10	0.821 pF	0.829 pF	3.402 pF	4.298 pF
BOX15	0.601 pF	0.615 pF	2.950 pF	3.874 pF
BOX20	0.282 pF	0.302 pF	2.931 pF	3.874 pF
BOX30	0.211 pF	0.223 pF	2.786 pF	3.729 pF
BOX40	0.155 pF	0.162 pF	2.677 pF	3.620 pF
BOX80	0.098 pF	0.100 pF	2.578 pF	3.521 pF

* Pad capacitance varies with layout format.

Circuit Performance

Cell Name	Propagation Delay [1]				DC Current [2]
	T_{PHL}		T_{PLH}		
	Extrinsic	Intrinsic	Extrinsic	Intrinsic	Sink/Source
BOX06D BOX06T	0.317 ns/10pF 0.317 ns/10pF	1.572 ns 1.610 ns	0.303 ns/10pF 0.302 ns/10pF	1.546 ns 1.591 ns	24.0 mA
BOX08D BOX08T	0.582 ns/10pF 0.581 ns/10pF	0.948 ns 1.006 ns	0.500 ns/10pF 0.499 ns/10pF	1.129 ns 1.194 ns	12.0 mA
BOX10D BOX10T	0.748 ns/10pF 0.748 ns/10pF	0.797 ns 0.870 ns	0.611 ns/10pF 0.611 ns/10pF	1.043 ns 1.104 ns	10.0 mA
BOX15D BOX15T	0.984 ns/10pF 0.984 ns/10pF	0.625 ns 0.706 ns	0.800 ns/10pF 0.799 ns/10pF	0.870 ns 0.943 ns	8.0 mA
BOX20D BOX20T	2.016 ns/10pF 2.016 ns/10pF	0.658 ns 0.825 ns	1.710 ns/10pF 1.710 ns/10pF	0.789 ns 0.930 ns	4.0 mA
BOX30D BOX30T	2.866 ns/10pF 2.866 ns/10pF	0.759 ns 0.984 ns	2.339 ns/10pF 2.338 ns/10pF	1.087 ns 1.297 ns	3.0 mA
BOX40D BOX40T	4.285 ns/10pF 4.285 ns/10pF	0.963 ns 1.284 ns	3.181 ns/10pF 3.173 ns/10pF	3.098 ns 3.424 ns	2.0 mA
BOX80D BOX80T	8.582 ns/10pF 8.582 ns/10pF	1.617 ns 2.230 ns	3.723 ns/10pF 3.694 ns/10pF	19.87 ns 20.54 ns	1.0 mA

1) Nominal process, V_{DD} = 5.0 V, T = 25 ° C.
2) Slow process, V_{DD} = 4.5 V, T = 125 °C.

Layout Information

Cell Name	Transistors	Cell Dimensions	
		X	Y
BOX06D BOX06T	12	241.75 µm 175.00 µm	283.50 µm 522.90 µm
BOX08D BOX08T	8	226.35 µm 175.00 µm	283.50 µm 522.90 µm
BOX10D BOX10T	6	220.35 µm 175.00 µm	283.50 µm 522.90 µm
BOX15D BOX15T	4	210.95 µm 175.00 µm	283.50 µm 522.90 µm
BOX20D BOX20T	2	204.95 µm 175.00 µm	283.50 µm 522.90 µm
BOX30D BOX30T	2	204.95 µm 175.00 µm	283.50 µm 522.90 µm
BOX40D BOX40T	2	204.95 µm 175.00 µm	283.50 µm 522.90 µm
BOX80D BOX80T	2	204.95 µm 175.00 µm	283.50 µm 522.90 µm

Logic Cells

Section 6

Contents - Section 6

Introduction

Logic Cell Information

This section contains data sheets that provide details about the logic cells in the 0.9 µm CMOS Catalog. What follows here is some background information about the logic cell family that should help in guiding you through the wide selection of cells available.

Some of the salient features of the logic cell family are noted as follows:

- There are 197 cells described in this section, broken down by function as follows:

Cell Type	# of Cells	Page Number
AND*n* gates	9	6-10
And-Or-Invert gates (AOI***abcd***)	70	6-11 to 6-14
Built in Self Test Logic (BIST1)	1	6-15
Full Adder (FA)	1	6-16
Inverters (INRB*n*)	5	6-17
Nand gates (ND*n*)	9	6-18
Nor gates (NR*n*)	9	6-19
Or-And-Invert gates (OAI***abcd***)	67	6-20 to 6-23
OR*n* gates	9	6-24
Select Data (SD***abc***)	4	6-25 to 6-28
3-state bus drivers (TBDI)	2	6-29
3-state bus drivers (TBUS*I*)	4	6-30 to 6-31
Transmission gates (TG*n*)	3	6-32
XNOR and XOR gates	4	6-33 to 6-34

A complete description of the cell-naming convention is provided on the following pages.

- A complete set of And-Or-Invert and Or-And-Invert gates are available. The library has been designed with a complete set of cells to get the maximum efficiency out of logic synthesis tools (see, for example, the description of the FDS functions available in Section 10.) If you are capturing your schematic manually, having a complete set of cells available also means that you will not need to have any cells with unused inputs (that would otherwise require connection to one of the power supplies.) This saves silicon area and improves circuit performance.
- Both area-optimized and performance-optimized versions of each cell are available. Thus, if your performance requirements do not tax the limits of the technology, you will be able to save area by using the area-optimized library. (See, for example, guidelines to the calculation of chip area in Section 2.)
- Many of the simpler cells are provided with a number of drive capabilities. For example, in this section you will find a ND2, ND2H, and ND2S. These names refer to 2-input Nand gates with 1X, 2X and 4X drive capability, respectively.

AND***n*** The AND cell provides the logical AND of two or more inputs as specified by the parameter ***n***.

Example: AND3 would be a cell whose output is the logical AND of all three of its inputs.

AOI***abcd*** These cells provide the inverted OR of two to four AND groups. The parameters ***a***, ***b***, ***c***, and ***d*** specify how many inputs make up each AND group. These parameters are always specified in descending order and parameters ***c*** and ***d*** are omitted when their values are zero.

Example: AOI422 would be a cell whose output is the inversion of (A1 and A2 and A3 and A4) or (B1 and B2) or (C1 and C2).

BIST1 This cell provides the logic function required for Built in Self Test applications. This function is already present in the BIST flip-flops FB1S2AX AND FB1S3AX. The BIST1 cell can be used in conjunction with any other flip-flop to create additional BIST compatible flip-flops.

FA This cell is a two-bit adder with carry in and carry out in addition to the sum output. FA cells can be combined to make arbitrary length adders.

INRB***n*** The INRB cells provide the logical inversion of the input signal. This cell can also be used as an inverting buffer, and for this purpose many high-power varieties exist. The parameter ***n*** will define the power of the cell in multiples of a standard INRB. It is worthwhile to note that the suffix H implies twice the standard INRB while the S suffix implies a four-fold ratio.

Example: INRB12 would be an inverter that is twelve times the power of a standard INRB.

ND***n*** The ND cell provides the inversion of the logical AND of two or more inputs as specified by the parameter ***n***.

Example: ND3 would be a cell whose output is the logical NAND of all three of its inputs.

NR***n*** The NR cell provides the inversion of the logical OR of two or more inputs as specified by the parameter ***n***.

Example: NR3 would be a cell whose output is the logical NOR of all three of its inputs.

OAI***abcd*** These cells provide the inverted AND of two to four OR groups. The parameters ***a***, ***b***, ***c***, and ***d*** specify how many inputs make up each OR group. These parameters are always specified in descending order, and parameters ***c*** and ***d*** are omitted when their values are zero.

Example: OAI422 would be a cell whose output is the inversion of (A1 or A2 or A3 or A4) and (B1 or B2) and (C1 or C2).

ONE The ONE cell is a direct connection to the V_{DD} power supply. The output signal can be used as a logical ONE in other areas of the circuit.

OR***n*** The OR cell provides the logical OR of two or more inputs as specified by the parameter ***n***.

Example: OR3 would be a cell whose output is the logical OR of all three of its inputs.

SD***abc*** The SD (Select Data) cells have been generated to standardize cells which simply select one of a number of inputs to the output. The inputs themselves may be groups of bits rather than single bits, and in this case, the output would be the selected group of bits. It is also advantageous to allow some of these groups to be inverted when they are selected. The type of cell supplied in the library assigns each group of bits an address, and these inputs are then chosen by applying the address value to the select lines. The naming convention for Select Data cells is as follows:

SD***abc*** ***a***= Number of addresses
b= Number of bits per address
c= Value indicating which addresses are inverted

Values greater than 9 are not permitted for ***a*** and ***b***.

The value of ***c*** is calculated by forming a binary number with each bit representing the polarity of an address. The lowest-order bit represents the zero address, and a bit value of 1 indicates an inverted address. The choice of 1 to indicate an inversion has the benefit of a zero value for ***c*** for all non-inverting selectors.

Example: SD212 is the name of a cell which selects one of two data addresses which are one bit wide with address one inverted.

SD212 ***a=2*** There are two addresses - 0 and 1.
b=1 There is one bit per address.
c=2 The decimal value of 10 (address 1 inverted).

TBDI The TBDI cells are 3-state inverters. These cells are meant for use in internal bus structures.

TBUS***I*** The TBUS cells are 3-state buffers. The presence of the parameter ***i*** indicates that the cell is an inverting buffer. These cells are meant for use in internal bus structures.

TG***n*** The TG cells contain one or more transmission gates whose outputs are connected to form a common bus output. The parameter ***n*** defines the exact number of transmission gates present in the cell. Transmission gates that are used consist of both an N- and a P-type transistor.

Example: TG2 contains two transmission gates whose outputs form a common bus.

XNOR The XNOR cell performs the logical EXCLUSIVE NOR function. Additionally, since this function requires two gates to generate an XNOR function, the NAND of the two inputs is also provided as an output.

XOR The XOR cell performs the logical EXCLUSIVE OR function. Additionally, since this function requires two gates to generate an XOR function, the NOR of the two inputs is also provided as an output.

ZERO The ZERO cell is a direct connection to the Vss power supply. The output signal can be used as a logical ZERO in other areas of the circuit.

Cell Drive Capability

The 0.9 µm CMOS Library contains variations of the same function that differ only in drive capability. These higher-power versions are commonly denoted by a suffix of H or S. The high-power or H version has double the drive of the normal version where S indicates a factor of four. All of the conventions described allow for the possibility of a higher-power version.

If you turn to page 6-17, which is the data sheet for the INRB family, you will find this table of capacitances:

Capacitances - INRB*n*

	INRB	INRBH	INRBS	INRB8	INRB12
Area	0.027pF	0.054pF	0.109pF	0.220pF	0.330pF
Perf.	0.102pF	0.205pF	0.410pF	0.821pF	1.232pF

These are the input capacitances for the INRB family from both the area-optimized and performance-optimized libraries. The capacitances have been tabulated in terms of picofarads and since there are two libraries of cells (area-optimized and performance-optimized), a different input capacitance is supplied for each.

The capacitive load, 0.027 pF, is the input capacitance of an area-optimized version of the INRB (a 1X inverter gate.) This capacitance is comprised of a 1X P-transistor, a 1X N-transistor and some internal cell routing. Similarly, the capacitive load, which equals 0.102 pF, is the input capacitance of a performance-optimized version of the INRB.

Knowing these two values, it becomes easy to compare the input capacitances of different gates to one another. For example, if we look at the capacitance table for the AOI***abcd*** family, we see:

Capacitances - AOI*abcd*

	Normal Power	High Power	Super Power
Area	0.027pF	0.056pF	0.116pF
Perf.	0.102pF	0.206pF	0.416pF

6

It is now easy to see the input capacitance for all high-power AOI***abcd*** gates is approximately twice that of an INRB. The numbers do not, in this case, work out to exact integer ratios because of internal cell routing. Similarly, the input capacitances for super-power gates is approximately four times that of a standard INRB

When calculating delays, remember to include estimated routing capacitance. A value of 0.10 pF per fan-out is the autoroute factor suggested for simulation.

An example of a delay calculation using these input capacitances is provided in the section that follows.

If we turn to the SD210 as an example, it can be seen that the following delay information has been tabulated on page 6-25:

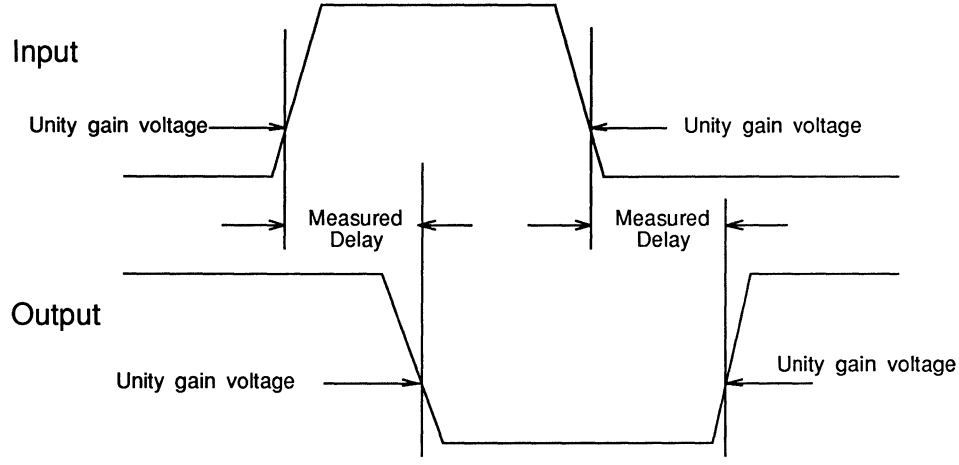
Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	Z ↓	2.05 ns/pF	0.97 ns	0.53 ns/pF	0.60 ns
D0 ↑	Z ↑	3.24 ns/pF	0.81 ns	0.70 ns/pF	0.45 ns
D1 ↓	Z ↓	2.05 ns/pF	0.97 ns	0.58 ns/pF	0.52 ns
D1 ↑	Z ↑	3.24 ns/pF	0.75 ns	0.66 ns/pF	0.47 ns
SD ↓	Z ↓	2.05 ns/pF	0.97 ns	0.58 ns/pF	0.52 ns
SD ↓	Z ↑	3.24 ns/pF	0.81 ns	0.66 ns/pF	0.59 ns
SD ↑	Z ↓	1.98 ns/pF	1.40 ns	0.53 ns/pF	0.78 ns
SD ↑	Z ↑	3.24 ns/pF	0.75 ns	0.70 ns/pF	0.45 ns

V_{DD} =5V, T=25°C, Nominal Process.

A similar set of delay information is provided for all 197 logic cells in this section. These tables contain linear equations used to approximate the cell delay characteristics.

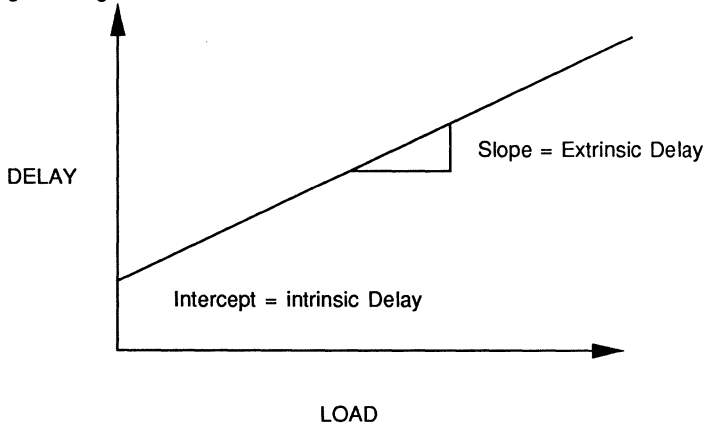
The INRB unity-gain point was used to define where the delays were measured as illustrated in the diagram below. The unity-gain voltage is defined as the point on the INRB DC transfer curve where the output voltage is equal to the applied input voltage. The area-optimized and performance-optimized libraries were characterized by using the INRB cell from the respective library.



The terms and symbols used in the Delay Information tables are defined as follows:

The first two columns indicate the input and output signal names and also indicate rising or falling transitions. The propagation delay values in the first entry of the SD210 Delay Information table, D0 ↓ to Z ↓, specify the path delay from the D0 input falling to the Z output falling.

An *intrinsic* and *extrinsic* delay value is provided in the Delay Information Table. These two values are terms for a linear equation used to approximate the cell delay characteristics. In graphical terms, they have the following meaning:



Thus, the delay characteristics for the path D0 ↓ to Z ↓ of an area-optimized SD210 can be written as the sum of the intrinsic delay and the extrinsic delay, as follows:

Delay = 0.97 ns + (2.05 ns/pF) times total load in picofarads

In physical terms, the *intrinsic delay* represents the *zero-load* delay of the cell. The *extrinsic delay* is related to the cell's output impedance and is a measure of how the delay will vary with increasing load. Because all of the cells in the library have purely capacitive inputs, dc loading on the outputs is not a concern (some notable exceptions, of course, are output buffers which may interface with TTL). Thus, given enough time, a CMOS logic gate will always reach a valid logic level regardless of the number of gates being driven. However, that time will increase as the load on the output increases.

The delay information was obtained by simulating each cell with AT&T's MOTIS3 Timing simulator under worst-case slow conditions (4.5 V, 100 °C, and slow process conditions). Subsequently, each delay value was derated by a factor of 0.578, which was obtained from the derating tables presented in Section 2, to convert the numbers to Nominal conditions (5.0 V, 25 °C, and nominal process conditions). This allows nominal delays to be used in the catalog while providing the most accurate predictions for worst-case behavior.

The required derating factor was calculated as follows:

Nominal delay*1.26 (slow process conditions) * 1.39 (4.5V and 100 °C) = worst-case slow delay

Therefore,

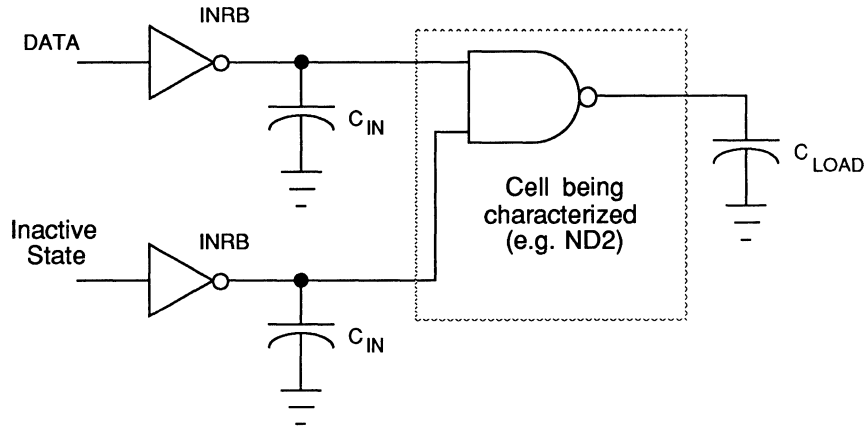
Nominal delay = 0.571 worst-case slow delay

Process Conditions	Derating Factor
Slow	1.26
Nominal	1.0
Fast	0.83

Power Supply and Temperature Derating

		POWER SUPPLY VOLTAGE (V_{DD})				
		4.50V	4.75V	5.00V	5.25V	5.50V
TEMPERATURE	-40°	0.81	0.77	0.74	0.72	0.70
	0°	0.98	0.94	0.90	0.87	0.85
	25°	1.09	1.04	1.00	0.96	0.94
	85°	1.33	1.28	1.23	1.18	1.14
	100°	1.39	1.33	1.28	1.23	1.18
	125°	1.48	1.41	1.35	1.31	1.26

The following circuit was used for all delay simulations.



Notice that in addition to a load being applied to the output of the cell being characterized, a capacitive load equal to a three fan-outs was connected to the cell's *input*. A value of three fan-outs was chosen because this has been found to be quite typical in many designs. Estimated routing capacitance equal to 0.10 pF per fan-out has been included, both on the outputs and the inputs.

(Of course, one can only use estimated capacitances before layout; early in the circuit design phase, exact layout capacitances are not available. The factor of 0.10 pF/fan-out is a conservative one - on a typical 0.9 µm CMOS design, 90% of all signals will have less than 0.10 pF/fan-out.)

The inputs of the cells were loaded for delay characterization because the slope of the waveform on the input of a gate has a very noticeable effect on its propagation delay. Had this effect been neglected, the delay information provided would have been optimistic by about 10%.

To obtain the cell-delay equations, two MOTIS3 simulations were performed for each cell. One simulation was performed with a CLOAD equivalent to a fan-out of three, and another simulation was performed with CLOAD equivalent to a fan-out of ten. In both cases, the input of the cell was loaded with a capacitance equivalent to a fan-out of three, including estimated routing capacitance. These capacitances work out as follows:

C_{LOAD} = 3 × (0.027 pF/gate + 0.10 pF/autoroute) = 0.38 pF (Fan-out = 3)

C_{LOAD} = 10 × (0.027 pF/gate + 0.10 pF/autoroute) = 1.27 pF (Fan-out = 10)

for the area-optimized library, and:

3 × (0.102 pF/gate + 0.10 pF/autoroute) = 0.606 pF (Fan-out = 3)

10 × (0.102 pF/gate + 0.10 pF/autoroute) = 2.020 pF (Fan-out = 10)

for the performance-optimized library.

The delay values obtained from these simulations were derated by 0.571 (see above) and then used to obtain a line intercept (intrinsic delay) and slope (extrinsic delay).

By now, it has probably become apparent how the delay information provided in this catalog was obtained, and how it can be used to an advantage. The delay information was calculated with the intent of allowing one to use it to do a circuit design on paper, and then go on with confidence to

MOTIS3 simulations knowing that there will be few surprises. Most designers like to avoid surprises since they can often result in design delays.

On the other hand, if you need to squeeze every nanosecond out of the technology, the delay information provided here will only get you started. For the highest degree of simulation accuracy, real layout capacitances should be included, and either MOTIS3 gate-level timing simulation or ADVICE device-level simulation should be used (with ADVICE being the most accurate and CPU hungry).

Calculating Gate Delays - An Example

A ND2 drives three loads. Consider the following problems:

1) *What are the gate delays under nominal conditions for the performance-optimized version of the cell?*
2) *For the area-optimized version?*
3) *What happens if T=100 ° C, VDD=4.5 V and worst-case slow wafer processing are assumed?*

To solve this problem, we need to look at the Delay Information Table for the ND2:

Delay Information - ND2

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
ND2	3	4	Z ↓	4.10ns/pF	0.83ns	1.07ns/pF	0.28ns
			Z ↑	3.24ns/pF	0.29ns	0.66ns/pF	0.18ns

6

VDD = 5 V, T = 25 ° C, nominal process

NOTE: When calculating delays, remember to include estimated routing capacitance. A value of 0.10 pF per fan-out is the autoroute factor suggested for simulation.

Solutions:

As we noted before, it's easiest to take the intrinsic and extrinsic delays and write the delay characteristics out as an equation. For the performance-optimized ND2, we have:

Z ↓ delay = 0.28 ns + (1.07 ns/pF) * Total Load in picofarads

And:

Z ↑ delay = 0.18 ns + (0.66 ns/pF) * Total Load in picofarads

For a fan-out of three, the total capacitive load works out to:

3* (0.102 pF/INRB gate capacitance) + 3 * (0.10 pF/fan-out capacitance) = 0.606 pF

Putting this back into our equations for Z ↓ delay and Z ↑ delay:

Z ↓ delay = 0.28 ns + (1.07 ns/pF) * 0.606 pF = 0.93 ns

And:

Z ↑ delay = 0.18 ns + (0.66 ns/pF) * 0.606 pF = 0.58 ns

To solve the problem for the area-optimized library, we must re-calculate the capacitive load:

3 * (0.027 pF/INRB gate capacitance) + 3 * (0.10 pF/fan-out capacitance) = 0.381 pF

Putting this value into the characteristic delay equations for the area-optimized ND2, we get:

Z ↓ delay = 0.83 ns + (4.10 ns/pF) * 0.381 pF = 2.39 ns

And:

Z ↑ delay = 0.29 ns + (3.24 ns/pF) * 0.381 pF = 1.52 ns

The next part of the problem is to derate these numbers from nominal conditions to the more severe conditions stated in Part 3 of the problem, namely T = 100 °C, VDD = 5 V and worst-case slow processing. To do this, we need the derating factors that were presented in Section 2:

Process Conditions	Derating Factor
Slow	1.26
Nominal	1.0
Fast	0.83

Power Supply and Temperature Derating

		POWER SUPPLY VOLTAGE (VDD) 4.50V	4.75V	5.00V	5.25V	5.50V
TEMPERATURE	-40°	0.81	0.77	0.74	0.72	0.70
	0°	0.98	0.94	0.90	0.87	0.85
	25°	1.09	1.04	1.00	0.96	0.94
	85°	1.33	1.28	1.23	1.18	1.14
	100°	1.39	1.33	1.28	1.23	1.18
	125°	1.48	1.41	1.35	1.31	1.26

The derating factor we need can be seen to be:

D = 1.26 (Slow Process) * 1.39 (VDD = 4.5 V, T = 100 ° C) = 1.75

Accordingly, the gate delays for the performance-optimized ND2 become:

Z ↓ delay = 0.93 ns * 1.75 = 1.63 ns (T=100 ° C, VDD = 4.5 V, slow process)

And:

Z ↑ delay = 0.58 ns * 1.75 = 1.02 ns (T=100 ° C, VDD = 4.5 V, slow process)

Similarly, for the area-optimized version of the ND2:

Z ↓ delay = 2.39 ns * 1.75 = 4.18 ns (T=100 ° C, VDD = 4.5 V, slow process)

And:

Z ↑ delay = 1.52 ns * 1.75 = 2.66 ns (T=100 ° C, VDD = 4.5 V, slow process)

And

AND*n*

The AND cells provide a logical AND of two to four inputs as specified by the parameter *n*.

High power and super power AND cells are available. A suffix of *H* indicates high power (2x) where an *S* suffix denotes super power (4x).

Example: AND3

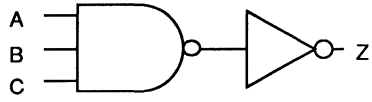
Inputs
A,B,C

Outputs
Z

Logic Equation

Z = (A•B•C)

Motis Model



Capacitances

The input terminal capacitance for all AND cells is provided in the following table and is identical for all AND cells and all higher power versions.

	Terminal Capacitance
Area	0.027pF
Perf.	0.102pF

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
AND2	4	6	Z ↓	1.98ns/pF	0.53ns	0.53ns/pF	0.31ns
			Z ↑	3.24ns/pF	0.75ns	0.66ns/pF	0.47ns
AND2H	6	8	Z ↓	1.06ns/pF	0.70ns	0.29ns/pF	0.40ns
			Z ↑	1.65ns/pF	0.94ns	0.33ns/pF	0.61ns
AND2S	8	12	Z ↓	0.66ns/pF	0.91ns	0.16ns/pF	0.59ns
			Z ↑	0.79ns/pF	1.32ns	0.21ns/pF	0.80ns
AND3	5	8	Z ↓	1.98ns/pF	0.64ns	0.53ns/pF	0.37ns
			Z ↑	3.24ns/pF	0.98ns	0.66ns/pF	0.64ns
AND3H	7	10	Z ↓	1.06ns/pF	0.76ns	0.29ns/pF	0.46ns
			Z ↑	1.59ns/pF	1.26ns	0.33ns/pF	0.84ns
AND3S	9	14	Z ↓	0.66ns/pF	0.97ns	0.21ns/pF	0.57ns
			Z ↑	0.86ns/pF	1.64ns	0.21ns/pF	1.15ns
AND4	6	10	Z ↓	1.98ns/pF	0.64ns	0.53ns/pF	0.37ns
			Z ↑	3.17ns/pF	1.24ns	0.70ns/pF	0.73ns
AND4H	8	12	Z ↓	0.99ns/pF	0.84ns	0.29ns/pF	0.46ns
			Z ↑	1.65ns/pF	1.46ns	0.37ns/pF	0.99ns
AND4S	10	16	Z ↓	0.66ns/pF	0.97ns	0.16ns/pF	0.65ns
			Z ↑	0.86ns/pF	1.99ns	0.21ns/pF	1.44ns

VDD=5V, T=25°C, Nominal Process.

And-Or-Invert — AOI*abcd*

These cells provide the inverted OR of two to four AND groups. The parameters *a, b, c,* and *d* specify how many inputs make up each AND group. These parameters are always specified in descending order and parameters *c* and *d* are omitted when their values are zero.

A small amount of higher power AOI cells are available. A suffix of *H* indicates high power (2x) where an *S* suffix denotes super power (4x).

Example: AOI221

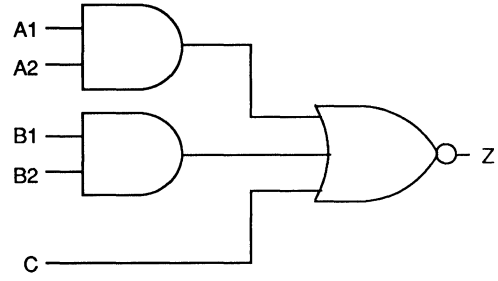
Inputs
A1,A2,B1,B2,C

Outputs
Z

Logic Equation

$$Z = \overline{(A1*A2)+(B1*B2)+C}$$

Motis Model



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Capacitances

The input terminal capacitance for all AOI cells is provided in the following table and is a function of the power of the cell.

	Normal Power	High Power	Super Power
Area	0.027pF	0.056pF	0.116pF
Perf.	0.102pF	0.206pF	0.416pF

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
AOI21	4	6	Z↓	4.03ns/pF	0.92ns	1.07ns/pF	0.28ns
			Z↑	6.47ns/pF	0.29ns	1.36ns/pF	0.17ns
AOI21H	7	12	Z↓	2.16ns/pF	0.69ns	0.53ns/pF	0.26ns
			Z↑	3.17ns/pF	0.31ns	0.66ns/pF	0.18ns
AOI211	5	8	Z↓	4.03ns/pF	0.92ns	1.07ns/pF	0.34ns
			Z↑	9.64ns/pF	0.49ns	2.05ns/pF	0.26ns
AOI2111	6	10	Z↓	3.90ns/pF	0.97ns	1.07ns/pF	0.34ns
			Z↑	12.95ns/pF	0.58ns	2.75ns/pF	0.36ns
AOI22	5	8	Z↓	4.10ns/pF	0.89ns	1.07ns/pF	0.28ns
			Z↑	6.41ns/pF	0.37ns	1.40ns/pF	0.14ns
AOI22H	9	16	Z↓	2.16ns/pF	0.74ns	0.53ns/pF	0.31ns
			Z↑	3.17ns/pF	0.37ns	0.70ns/pF	0.16ns

VDD=5V, T=25°C, Nominal Process.

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
AOI22S	17	32	Z ↓	1.26ns/pF	0.57ns	0.29ns/pF	0.23ns
			Z ↑	1.59ns/pF	0.33ns	0.33ns/pF	0.21ns
AOI221	7	10	Z ↓	4.03ns/pF	0.97ns	1.07ns/pF	0.34ns
			Z ↑	9.71ns/pF	0.52ns	2.05ns/pF	0.32ns
AOI2211	7	12	Z ↓	3.90ns/pF	1.02ns	1.03ns/pF	0.42ns
			Z ↑	12.88ns/pF	0.78ns	2.75ns/pF	0.42ns
AOI2211H	15	24	Z ↓	2.18ns/pF	0.80ns	0.58ns/pF	0.29ns
			Z ↑	6.47ns/pF	0.64ns	1.36ns/pF	0.40ns
AOI222	8	12	Z ↓	4.03ns/pF	0.97ns	1.03ns/pF	0.42ns
			Z ↑	9.71ns/pF	0.58ns	2.05ns/pF	0.38ns
AOI2221	9	14	Z ↓	3.83ns/pF	1.11ns	1.07ns/pF	0.40ns
			Z ↑	12.95ns/pF	0.81ns	2.71ns/pF	0.56ns
AOI2222	10	16	Z ↓	3.90ns/pF	1.08ns	1.07ns/pF	0.40ns
			Z ↑	12.95ns/pF	0.87ns	2.75ns/pF	0.54ns
AOI2222H	18	32	Z ↓	2.18ns/pF	0.86ns	0.58ns/pF	0.35ns
			Z ↑	6.41ns/pF	0.89ns	1.40ns/pF	0.49ns
AOI31	5	8	Z ↓	5.95ns/pF	0.83ns	1.56ns/pF	0.33ns
			Z ↑	6.47ns/pF	0.29ns	1.40ns/pF	0.14ns
AOI311	6	10	Z ↓	5.88ns/pF	0.92ns	1.56ns/pF	0.39ns
			Z ↑	9.71ns/pF	0.46ns	2.01ns/pF	0.35ns
AOI3111	7	12	Z ↓	5.75ns/pF	0.97ns	1.56ns/pF	0.39ns
			Z ↑	12.88ns/pF	0.66ns	2.75ns/pF	0.36ns
AOI32	6	10	Z ↓	5.95ns/pF	0.89ns	1.56ns/pF	0.33ns
			Z ↑	6.47ns/pF	0.35ns	1.36ns/pF	0.22ns
AOI321	7	12	Z ↓	5.88ns/pF	0.97ns	1.56ns/pF	0.39ns
			Z ↑	9.71ns/pF	0.52ns	2.05ns/pF	0.32ns
AOI3211	8	14	Z ↓	5.68ns/pF	1.05ns	1.56ns/pF	0.45ns
			Z ↑	12.95ns/pF	0.69ns	2.75ns/pF	0.42ns
AOI322	9	14	Z ↓	5.88ns/pF	1.03ns	1.56ns/pF	0.45ns
			Z ↑	9.71ns/pF	0.64ns	2.05ns/pF	0.38ns
AOI322H	16	28	Z ↓	3.10ns/pF	0.86ns	0.78ns/pF	0.45ns
			Z ↑	4.82ns/pF	0.62ns	1.03ns/pF	0.36ns
AOI3221	10	16	Z ↓	5.61ns/pF	1.25ns	1.56ns/pF	0.50ns
			Z ↑	12.95ns/pF	0.98ns	2.71ns/pF	0.68ns
AOI3222	11	18	Z ↓	5.68ns/pF	1.16ns	1.56ns/pF	0.50ns
			Z ↑	12.95ns/pF	0.92ns	2.75ns/pF	0.59ns
AOI33	7	12	Z ↓	5.95ns/pF	0.95ns	1.56ns/pF	0.39ns
			Z ↑	6.47ns/pF	0.40ns	1.36ns/pF	0.28ns
AOI33H	14	24	Z ↓	3.04ns/pF	0.88ns	0.78ns/pF	0.40ns
			Z ↑	3.17ns/pF	0.49ns	0.66ns/pF	0.30ns
AOI331	8	14	Z ↓	5.88ns/pF	1.03ns	1.56ns/pF	0.45ns
			Z ↑	9.71ns/pF	0.58ns	2.05ns/pF	0.38ns
AOI3311	9	16	Z ↓	5.68ns/pF	1.11ns	1.56ns/pF	0.45ns
			Z ↑	12.88ns/pF	0.83ns	2.75ns/pF	0.48ns
AOI332	9	16	Z ↓	5.88ns/pF	1.09ns	1.56ns/pF	0.50ns
			Z ↑	9.64ns/pF	0.72ns	2.05ns/pF	0.44ns

VDD=5V, T=25°C, Nominal Process.

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
AOI3321	10	18	Z↓	5.68ns/pF	1.16ns	1.56ns/pF	0.50ns
			Z↑	12.88ns/pF	0.95ns	2.75ns/pF	0.54ns
AOI3322	12	20	Z↓	5.61ns/pF	1.25ns	1.56ns/pF	0.56ns
			Z↑	12.88ns/pF	1.07ns	2.75ns/pF	0.65ns
AOI333	10	18	Z↓	5.88ns/pF	1.15ns	1.56ns/pF	0.56ns
			Z↑	9.64ns/pF	0.83ns	2.05ns/pF	0.50ns
AOI333H	22	36	Z↓	3.04ns/pF	1.06ns	0.78ns/pF	0.57ns
			Z↑	4.82ns/pF	0.85ns	1.03ns/pF	0.54ns
AOI3331	11	20	Z↓	5.68ns/pF	1.16ns	1.56ns/pF	0.50ns
			Z↑	12.95ns/pF	0.98ns	2.75ns/pF	0.59ns
AOI3332	12	22	Z↓	5.68ns/pF	1.22ns	1.56ns/pF	0.56ns
			Z↑	12.88ns/pF	1.12ns	2.75ns/pF	0.65ns
AOI3333	13	24	Z↓	5.68ns/pF	1.28ns	1.56ns/pF	0.62ns
			Z↑	12.95ns/pF	1.21ns	2.75ns/pF	0.77ns
AOI41	6	10	Z↓	7.93ns/pF	0.90ns	2.10ns/pF	0.41ns
			Z↑	6.41ns/pF	0.43ns	1.40ns/pF	0.20ns
AOI411	7	12	Z↓	7.79ns/pF	1.07ns	2.10ns/pF	0.47ns
			Z↑	9.64ns/pF	0.66ns	2.05ns/pF	0.38ns
AOI4111	8	14	Z↓	7.53ns/pF	1.16ns	2.05ns/pF	0.55ns
			Z↑	12.88ns/pF	0.83ns	2.71ns/pF	0.56ns
AOI42	7	12	Z↓	7.86ns/pF	0.92ns	2.05ns/pF	0.44ns
			Z↑	6.41ns/pF	0.43ns	1.36ns/pF	0.22ns
AOI421	9	14	Z↓	7.79ns/pF	1.07ns	2.10ns/pF	0.47ns
			Z↑	9.64ns/pF	0.66ns	2.05ns/pF	0.38ns
AOI4211	10	16	Z↓	7.53ns/pF	1.28ns	2.05ns/pF	0.67ns
			Z↑	12.95ns/pF	1.04ns	2.75ns/pF	0.65ns
AOI422	10	16	Z↓	7.79ns/pF	1.12ns	2.10ns/pF	0.53ns
			Z↑	9.64ns/pF	0.72ns	2.05ns/pF	0.44ns
AOI4221	11	18	Z↓	7.46ns/pF	1.30ns	2.10ns/pF	0.59ns
			Z↑	12.95ns/pF	0.98ns	2.75ns/pF	0.59ns
AOI4222	13	20	Z↓	7.46ns/pF	1.42ns	2.05ns/pF	0.73ns
			Z↑	12.95ns/pF	1.16ns	2.75ns/pF	0.71ns
AOI43	8	14	Z↓	7.86ns/pF	1.04ns	2.10ns/pF	0.47ns
			Z↑	6.47ns/pF	0.46ns	1.36ns/pF	0.28ns
AOI431	9	16	Z↓	7.79ns/pF	1.18ns	2.10ns/pF	0.59ns
			Z↑	9.71ns/pF	0.75ns	2.01ns/pF	0.52ns
AOI4311	10	18	Z↓	7.46ns/pF	1.30ns	2.10ns/pF	0.59ns
			Z↑	12.95ns/pF	0.98ns	2.75ns/pF	0.59ns
AOI432	11	18	Z↓	7.79ns/pF	1.18ns	2.05ns/pF	0.61ns
			Z↑	9.64ns/pF	0.78ns	2.05ns/pF	0.44ns
AOI4321	12	20	Z↓	7.53ns/pF	1.28ns	2.05ns/pF	0.67ns
			Z↑	12.88ns/pF	1.07ns	2.75ns/pF	0.65ns
AOI4322	13	22	Z↓	7.53ns/pF	1.34ns	2.10ns/pF	0.64ns
			Z↑	12.95ns/pF	1.10ns	2.75ns/pF	0.71ns
AOI433	11	20	Z↓	7.79ns/pF	1.24ns	2.10ns/pF	0.64ns
			Z↑	9.64ns/pF	0.89ns	2.05ns/pF	0.55ns

VDD=5V, T=25°C, Nominal Process.

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
AOI4331	12	22	Z↓	7.46ns/pF	1.42ns	2.05ns/pF	0.73ns
			Z↑	12.95ns/pF	1.16ns	2.75ns/pF	0.71ns
AOI4332	14	24	Z↓	7.46ns/pF	1.48ns	2.05ns/pF	0.78ns
			Z↑	12.88ns/pF	1.35ns	2.75ns/pF	0.83ns
AOI4333	14	26	Z↓	7.46ns/pF	1.48ns	2.05ns/pF	0.78ns
			Z↑	12.88ns/pF	1.35ns	2.75ns/pF	0.83ns
AOI44	9	16	Z↓	7.86ns/pF	1.10ns	2.05ns/pF	0.55ns
			Z↑	6.41ns/pF	0.54ns	1.40ns/pF	0.26ns
AOI441	11	18	Z↓	7.79ns/pF	1.18ns	2.10ns/pF	0.59ns
			Z↑	9.64ns/pF	0.78ns	2.05ns/pF	0.44ns
AOI4411	12	20	Z↓	7.53ns/pF	1.34ns	2.10ns/pF	0.64ns
			Z↑	12.95ns/pF	1.10ns	2.71ns/pF	0.73ns
AOI442	12	20	Z↓	7.79ns/pF	1.24ns	2.05ns/pF	0.67ns
			Z↑	9.71ns/pF	0.81ns	2.05ns/pF	0.50ns
AOI4421	13	22	Z↓	7.46ns/pF	1.42ns	2.05ns/pF	0.73ns
			Z↑	12.95ns/pF	1.16ns	2.75ns/pF	0.71ns
AOI4422	15	24	Z↓	7.46ns/pF	1.54ns	2.10ns/pF	0.76ns
			Z↑	12.95ns/pF	1.33ns	2.75ns/pF	0.83ns
AOI443	13	22	Z↓	7.79ns/pF	1.30ns	2.10ns/pF	0.70ns
			Z↑	9.64ns/pF	0.95ns	2.01ns/pF	0.64ns
AOI4431	14	24	Z↓	7.46ns/pF	1.48ns	2.10ns/pF	0.76ns
			Z↑	12.88ns/pF	1.35ns	2.75ns/pF	0.83ns
AOI4432	15	26	Z↓	7.46ns/pF	1.48ns	2.05ns/pF	0.78ns
			Z↑	12.95ns/pF	1.27ns	2.75ns/pF	0.83ns
AOI4433	16	28	Z↓	7.40ns/pF	1.73ns	2.10ns/pF	0.88ns
			Z↑	12.88ns/pF	1.64ns	2.75ns/pF	1.00ns
AOI444	14	24	Z↓	7.79ns/pF	1.35ns	2.05ns/pF	0.78ns
			Z↑	9.71ns/pF	0.98ns	2.05ns/pF	0.61ns
AOI4441	15	26	Z↓	7.46ns/pF	1.54ns	2.05ns/pF	0.84ns
			Z↑	12.95ns/pF	1.39ns	2.75ns/pF	0.88ns
AOI4442	17	28	Z↓	7.40ns/pF	1.73ns	2.05ns/pF	0.96ns
			Z↑	12.95ns/pF	1.62ns	2.71ns/pF	1.08ns
AOI4443	17	30	Z↓	7.46ns/pF	1.65ns	2.05ns/pF	0.90ns
			Z↑	12.88ns/pF	1.59ns	2.71ns/pF	1.02ns
AOI4444	19	32	Z↓	7.46ns/pF	1.77ns	2.05ns/pF	1.02ns
			Z↑	12.95ns/pF	1.73ns	2.75ns/pF	1.11ns

VDD=5V, T=25°C, Nominal Process.

Built in Self Test

BIST1

This cell provides the required data select logic to convert any flip-flop to a BIST-style circuit. The BIST1 cell is used to generate the flip-flop data input.

Grids 11, **Transistors** 18

Inputs

D0,D1,B0,B1

Outputs

Z

Capacitances

	D0	D1	B0	B1
Area	0.028pF	0.027pF	0.027pF	0.028pF
Perf	0.103pF	0.102pF	0.102pF	0.103pF

Truth Table

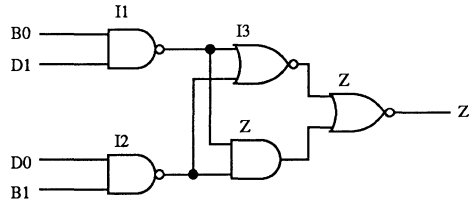
INPUTS				OUTPUT
D0	D1	B0	B1	Z
X	X	0	0	0
1	X	0	1	1
0	X	0	1	0
X	1	1	0	1
X	0	1	0	0
0	0	1	1	0
0	1	1	1	1
1	0	1	1	1
1	1	1	1	0

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
B0 ↓	Z ↓	3.96ns/pF	0.77ns	1.03ns/pF	0.48ns
B0 ↓	Z ↑	6.47ns/pF	0.92ns	1.40ns/pF	0.54ns
B0 ↑	Z ↓	1.98ns/pF	1.63ns	0.53ns/pF	1.01ns
B0 ↑	Z ↑	6.47ns/pF	1.04ns	1.36ns/pF	0.63ns
B1 ↓	Z ↓	3.90ns/pF	0.79ns	1.03ns/pF	0.48ns
B1 ↓	Z ↑	6.47ns/pF	0.87ns	1.40ns/pF	0.54ns
B1 ↑	Z ↓	1.98ns/pF	1.63ns	0.53ns/pF	1.01ns
B1 ↑	Z ↑	6.47ns/pF	1.04ns	1.36ns/pF	0.63ns
D0 ↓	Z ↓	3.90ns/pF	0.79ns	1.03ns/pF	0.48ns
D0 ↓	Z ↑	6.47ns/pF	0.87ns	1.40ns/pF	0.54ns
D0 ↑	Z ↓	1.98ns/pF	1.63ns	0.53ns/pF	1.01ns
D0 ↑	Z ↑	6.47ns/pF	1.04ns	1.36ns/pF	0.63ns
D1 ↓	Z ↓	3.96ns/pF	0.77ns	1.03ns/pF	0.48ns
D1 ↓	Z ↑	6.47ns/pF	0.92ns	1.40ns/pF	0.54ns
D1 ↑	Z ↓	1.98ns/pF	1.63ns	0.53ns/pF	1.01ns
D1 ↑	Z ↑	6.47ns/pF	1.04ns	1.36ns/pF	0.63ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Full Adder

FA

This cell is a 2-bit full adder which provides inverted sum and carry outputs. FA cells can be combined to make arbitrary length adders.

Grids 15, **Transistors** 24

Inputs

A,B,C

Outputs

ZCN,ZSN

Capacitances

	A	B	C
Area	0.114pF	0.115pF	0.089pF
Perf	0.415pF	0.416pF	0.315pF

Truth Table

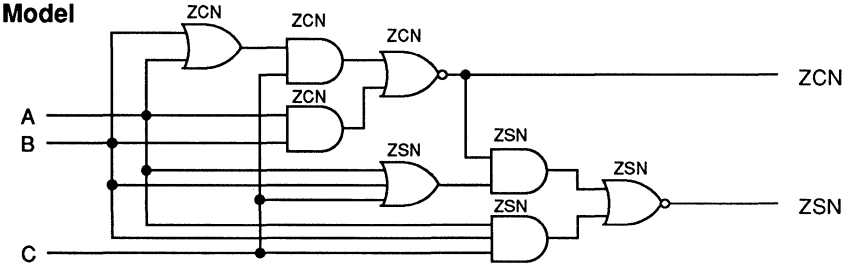
INPUTS			OUTPUTS	
A	B	C	ZSN	ZCN
0	0	0	1	1
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	0

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
A ↓	ZCN ↑	8.06ns/pF	0.73ns	1.68ns/pF	0.49ns
A ↓	ZSN ↓	16.45ns/pF	1.23ns	3.57ns/pF	0.85ns
A ↓	ZSN ↑	10.77ns/pF	0.70ns	2.30ns/pF	0.40ns
A ↑	ZCN ↓	4.03ns/pF	1.09ns	1.07ns/pF	0.45ns
A ↑	ZSN ↓	5.95ns/pF	1.01ns	1.56ns/pF	0.45ns
A ↑	ZSN ↑	11.10ns/pF	1.50ns	2.59ns/pF	0.81ns
B ↓	ZCN ↑	8.06ns/pF	0.73ns	1.68ns/pF	0.49ns
B ↓	ZSN ↓	16.45ns/pF	1.23ns	3.57ns/pF	0.85ns
B ↓	ZSN ↑	10.77ns/pF	0.70ns	2.30ns/pF	0.40ns
B ↑	ZCN ↓	4.03ns/pF	1.09ns	1.07ns/pF	0.45ns
B ↑	ZSN ↓	5.95ns/pF	1.01ns	1.56ns/pF	0.45ns
B ↑	ZSN ↑	11.10ns/pF	1.50ns	2.59ns/pF	0.81ns
C ↓	ZCN ↑	6.47ns/pF	0.58ns	1.36ns/pF	0.40ns
C ↓	ZSN ↓	14.14ns/pF	1.11ns	3.12ns/pF	0.72ns
C ↓	ZSN ↑	10.77ns/pF	0.70ns	2.30ns/pF	0.40ns
C ↑	ZCN ↓	4.03ns/pF	1.09ns	1.07ns/pF	0.45ns
C ↑	ZSN ↓	5.88ns/pF	1.03ns	1.56ns/pF	0.45ns
C ↑	ZSN ↑	11.10ns/pF	1.50ns	2.59ns/pF	0.81ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Inverter INRB*n*

The INRB cells provide the logical inversion of the input signal. This cell can also be used as an inverting buffer and for this purpose many higher power varieties exist.
The parameter *n* indicates the power of the cell in multiples of a standard INRB. A suffix of H indicates high power (2x) where an S suffix denotes super power (4x). Otherwise the parameter *n* specifies the multiple as a numeric value.

Inputs
A

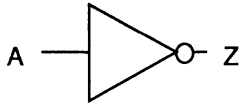
Outputs
Z

Logic Equation

$Z = \overline{A}$

Example: INRB12

Motis Model



Capacitances

The input terminal capacitance for all INRB cells is provided in the following table.

Capacitances

	INRB	INRBH	INRBS	INRB8	INRB12
Area	0.027pF	0.054pF	0.109pF	0.220pF	0.330pF
Perf.	0.102pF	0.205pF	0.410pF	0.821pF	1.232pF

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
INRB	2	2	Z ↓	2.31ns/pF	0.92ns	0.58ns/pF	0.29ns
			Z ↑	3.24ns/pF	0.29ns	0.70ns/pF	0.10ns
INRBH	3	4	Z ↓	1.45ns/pF	0.61ns	0.33ns/pF	0.21ns
			Z ↑	1.59ns/pF	0.27ns	0.37ns/pF	0.07ns
INRBS	5	8	Z ↓	0.86ns/pF	0.49ns	0.21ns/pF	0.17ns
			Z ↑	0.86ns/pF	0.20ns	0.21ns/pF	0.05ns
INRB8	9	16	Z ↓	0.59ns/pF	0.30ns	0.12ns/pF	0.10ns
			Z ↑	0.46ns/pF	0.17ns	0.12ns/pF	0.04ns
INRB12	13	24	Z ↓	0.40ns/pF	0.31ns	0.08ns/pF	0.12ns
			Z ↑	0.33ns/pF	0.17ns	0.08ns/pF	0.07ns

VDD=5V, T=25°C, Nominal Process.

Nand

NDn

The ND cells provide a logical NAND of two to four inputs as specified by the parameter *n*.

High power and super power NAND cells are available. A suffix of *H* indicates high power (2x) where an *S* suffix denotes super power (4x).

Example: ND3

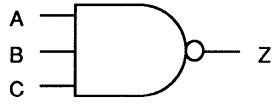
Inputs
A,B,C

Outputs
Z

Logic Equation

$Z = \overline{(A \cdot B \cdot C)}$

Motis Model



Capacitances

The input terminal capacitance for all ND cells is provided in the following table.

	ND2,ND3,ND4	ND2H	ND2S	ND3H	ND3S	ND4H	ND4S
Area	0.027pF	0.056pF	0.112pF	0.055pF	0.110pF	0.055pF	0.111pF
Perf.	0.102pF	0.206pF	0.413pF	0.205pF	0.411pF	0.102pF	0.412pF

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
ND2	3	4	Z ↓	4.10ns/pF	0.83ns	1.07ns/pF	0.28ns
			Z ↑	3.24ns/pF	0.29ns	0.66ns/pF	0.18ns
ND2H	5	8	Z ↓	2.18ns/pF	0.69ns	0.53ns/pF	0.26ns
			Z ↑	1.65ns/pF	0.25ns	0.33ns/pF	0.15ns
ND2S	9	16	Z ↓	1.19ns/pF	0.59ns	0.29ns/pF	0.23ns
			Z ↑	0.86ns/pF	0.20ns	0.16ns/pF	0.13ns
ND3	4	6	Z ↓	5.95ns/pF	0.89ns	1.56ns/pF	0.33ns
			Z ↑	3.17ns/pF	0.37ns	0.70ns/pF	0.16ns
ND3H	8	12	Z ↓	3.04ns/pF	0.77ns	0.78ns/pF	0.28ns
			Z ↑	1.65ns/pF	0.25ns	0.33ns/pF	0.15ns
ND3S	14	24	Z ↓	1.59ns/pF	0.68ns	0.41ns/pF	0.27ns
			Z ↑	0.79ns/pF	0.28ns	0.16ns/pF	0.13ns
ND4	5	8	Z ↓	7.86ns/pF	0.92ns	2.10ns/pF	0.36ns
			Z ↑	3.24ns/pF	0.35ns	0.70ns/pF	0.16ns
ND4H	8	14	Z ↓	0.99ns/pF	1.65ns	0.29ns/pF	1.04ns
			Z ↑	1.65ns/pF	0.71ns	0.33ns/pF	0.55ns
ND4S	18	32	Z ↓	1.98ns/pF	0.82ns	0.53ns/pF	0.31ns
			Z ↑	0.86ns/pF	0.26ns	0.21ns/pF	0.11ns

VDD=5V, T=25°C, Nominal Process.

Nor

NR*n*

The NR cells provide a logical NOR of two to four inputs as specified by the parameter *n*.

High power and super power NOR cells are available. A suffix of *H* indicates high power (2x) where an *S* suffix denotes super power (4x).

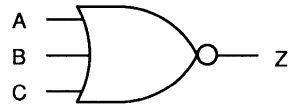
Example: NR3

Inputs
A,B,C

Outputs
Z

Logic Equation

$Z = \overline{(A+B+C)}$



Capacitances

The input terminal capacitance for all NR cells is provided in the following table.

	NR2,NR3,NR4	NR2H	NR2S	NR3H	NR3S	NR4H	NR4S
Area	0.027pF	0.056pF	0.112pF	0.057pF	0.114pF	0.055pF	0.111pF
Perf.	0.102pF	0.206pF	0.412pF	0.207pF	0.415pF	0.206pF	0.412pF

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
NR2	3	4	Z↓	2.31ns/pF	0.92ns	0.58ns/pF	0.29ns
			Z↑	6.47ns/pF	0.23ns	1.36ns/pF	0.17ns
NR2H	5	8	Z↓	1.45ns/pF	0.61ns	0.33ns/pF	0.21ns
			Z↑	3.17ns/pF	0.26ns	0.70ns/pF	0.10ns
NR2S	9	16	Z↓	0.86ns/pF	0.49ns	0.21ns/pF	0.17ns
			Z↑	1.59ns/pF	0.27ns	0.33ns/pF	0.15ns
NR3	4	6	Z↓	2.25ns/pF	0.95ns	0.58ns/pF	0.35ns
			Z↑	9.64ns/pF	0.43ns	2.01ns/pF	0.29ns
NR3H	7	12	Z↓	1.39ns/pF	0.69ns	0.33ns/pF	0.26ns
			Z↑	4.82ns/pF	0.33ns	1.03ns/pF	0.19ns
NR3S	13	24	Z↓	0.92ns/pF	0.46ns	0.21ns/pF	0.17ns
			Z↑	2.38ns/pF	0.38ns	0.49ns/pF	0.22ns
NR4	5	8	Z↓	1.98ns/pF	1.05ns	0.58ns/pF	0.35ns
			Z↑	12.88ns/pF	0.54ns	2.75ns/pF	0.31ns
NR4H	10	16	Z↓	1.39ns/pF	0.69ns	0.33ns/pF	0.26ns
			Z↑	6.47ns/pF	0.46ns	1.36ns/pF	0.28ns
NR4S	18	32	Z↓	0.86ns/pF	0.54ns	0.21ns/pF	0.17ns
			Z↑	3.17ns/pF	0.54ns	0.70ns/pF	0.27ns

VDD=5V, T=25°C, Nominal Process.

Or-And-Invert — OAI*abcd*

These cells provide the inverted AND of two to four OR groups. The parameters *a, b, c,* and *d* specify how many inputs make up each OR group. These parameters are always specified in descending order and parameters *c* and *d* are omitted when their values are zero.

A small amount of higher power OAI cells are available. A suffix of *H* indicates high power (2x) where an *S* suffix denotes super power (4x).

Example: OAI221

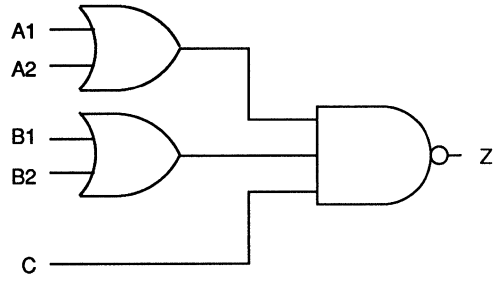
Inputs
A1,A2,B1,B2,C

Outputs
Z

Logic Equation

$$Z = \overline{(A1+A2)*(B1+B2)*C}$$

Motis Model



6

Capacitances

The input terminal capacitance for all OAI cells is provided in the following table and is a function of the power of the cell.

	Normal Power	High Power	Super Power
Area	0.027pF	0.056pF	0.113pF
Perf.	0.102pF	0.206pF	0.413pF

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
OAI21	4	6	Z ↓	4.03ns/pF	0.92ns	1.07ns/pF	0.28ns
			Z ↑	6.47ns/pF	0.29ns	1.36ns/pF	0.17ns
OAI21H	7	12	Z ↓	2.18ns/pF	0.69ns	0.53ns/pF	0.26ns
			Z ↑	3.24ns/pF	0.23ns	0.70ns/pF	0.10ns
OAI21S	13	24	Z ↓	1.26ns/pF	0.51ns	0.29ns/pF	0.23ns
			Z ↑	1.59ns/pF	0.27ns	0.33ns/pF	0.15ns
OAI211	5	8	Z ↓	5.95ns/pF	0.89ns	1.56ns/pF	0.39ns
			Z ↑	6.47ns/pF	0.35ns	1.36ns/pF	0.22ns
OAI2111	6	10	Z ↓	7.86ns/pF	0.92ns	2.05ns/pF	0.44ns
			Z ↑	6.41ns/pF	0.43ns	1.36ns/pF	0.22ns
OAI22	5	8	Z ↓	4.03ns/pF	0.92ns	1.03ns/pF	0.36ns
			Z ↑	6.41ns/pF	0.37ns	1.40ns/pF	0.14ns

VDD=5V, T=25°C, Nominal Process.

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
OAI22H	9	16	Z↓	2.18ns/pF	0.74ns	0.53ns/pF	0.31ns
			Z↑	3.17ns/pF	0.37ns	0.70ns/pF	0.16ns
OAI221	7	10	Z↓	5.95ns/pF	0.95ns	1.56ns/pF	0.39ns
			Z↑	6.47ns/pF	0.40ns	1.40ns/pF	0.20ns
OAI2211	8	12	Z↓	7.86ns/pF	1.04ns	2.05ns/pF	0.55ns
			Z↑	6.47ns/pF	0.46ns	1.40ns/pF	0.26ns
OAI222	8	12	Z↓	5.88ns/pF	1.03ns	1.56ns/pF	0.45ns
			Z↑	6.47ns/pF	0.46ns	1.36ns/pF	0.28ns
OAI222H	14	24	Z↓	3.04ns/pF	0.88ns	0.78ns/pF	0.40ns
			Z↑	3.24ns/pF	0.40ns	0.70ns/pF	0.21ns
OAI2221	9	14	Z↓	7.86ns/pF	1.10ns	2.05ns/pF	0.55ns
			Z↑	6.41ns/pF	0.54ns	1.40ns/pF	0.26ns
OAI2222	10	16	Z↓	7.86ns/pF	1.10ns	2.10ns/pF	0.53ns
			Z↑	6.47ns/pF	0.52ns	1.36ns/pF	0.34ns
OAI2222H	18	32	Z↓	3.96ns/pF	1.06ns	1.03ns/pF	0.54ns
			Z↑	3.17ns/pF	0.54ns	0.70ns/pF	0.27ns
OAI31	5	8	Z↓	3.83ns/pF	0.99ns	1.07ns/pF	0.28ns
			Z↑	9.71ns/pF	0.35ns	2.05ns/pF	0.21ns
OAI311	6	10	Z↓	5.61ns/pF	1.02ns	1.56ns/pF	0.39ns
			Z↑	9.64ns/pF	0.49ns	2.05ns/pF	0.26ns
OAI3111	7	12	Z↓	7.46ns/pF	1.07ns	2.10ns/pF	0.41ns
			Z↑	9.64ns/pF	0.54ns	2.05ns/pF	0.32ns
OAI32	6	10	Z↓	3.90ns/pF	0.97ns	1.03ns/pF	0.36ns
			Z↑	9.71ns/pF	0.40ns	2.05ns/pF	0.26ns
OAI321	7	12	Z↓	5.61ns/pF	1.07ns	1.56ns/pF	0.39ns
			Z↑	9.71ns/pF	0.52ns	2.05ns/pF	0.32ns
OAI3211	8	14	Z↓	7.46ns/pF	1.13ns	2.05ns/pF	0.50ns
			Z↑	9.64ns/pF	0.60ns	2.05ns/pF	0.32ns
OAI322	9	14	Z↓	5.61ns/pF	1.13ns	1.56ns/pF	0.45ns
			Z↑	9.71ns/pF	0.64ns	2.05ns/pF	0.38ns
OAI3221	10	16	Z↓	7.40ns/pF	1.33ns	2.10ns/pF	0.59ns
			Z↑	9.71ns/pF	0.75ns	2.05ns/pF	0.50ns
OAI3222	11	18	Z↓	7.40ns/pF	1.33ns	2.05ns/pF	0.61ns
			Z↑	9.64ns/pF	0.78ns	2.05ns/pF	0.44ns
OAI33	7	12	Z↓	3.83ns/pF	1.05ns	1.03ns/pF	0.42ns
			Z↑	9.71ns/pF	0.52ns	2.05ns/pF	0.32ns
OAI331	8	14	Z↓	5.61ns/pF	1.13ns	1.56ns/pF	0.45ns
			Z↑	9.71ns/pF	0.58ns	2.05ns/pF	0.38ns
OAI3311	9	16	Z↓	7.46ns/pF	1.19ns	2.05ns/pF	0.55ns
			Z↑	9.64ns/pF	0.66ns	2.05ns/pF	0.38ns
OAI332	9	16	Z↓	5.61ns/pF	1.13ns	1.56ns/pF	0.50ns
			Z↑	9.71ns/pF	0.64ns	2.05ns/pF	0.44ns
OAI3321	10	18	Z↓	7.40ns/pF	1.27ns	2.10ns/pF	0.53ns
			Z↑	9.71ns/pF	0.69ns	2.05ns/pF	0.44ns
OAI3322	12	20	Z↓	7.33ns/pF	1.47ns	2.05ns/pF	0.73ns
			Z↑	9.71ns/pF	0.87ns	2.05ns/pF	0.55ns

VDD=5V, T=25°C, Nominal Process.

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
OAI333	10	18	Z ↓	5.55ns/pF	1.27ns	1.56ns/pF	0.56ns
			Z ↑	9.64ns/pF	0.83ns	2.05ns/pF	0.50ns
OAI3331	11	20	Z ↓	7.40ns/pF	1.33ns	2.10ns/pF	0.59ns
			Z ↑	9.71ns/pF	0.75ns	2.05ns/pF	0.50ns
OAI3332	12	22	Z ↓	7.40ns/pF	1.39ns	2.10ns/pF	0.64ns
			Z ↑	9.71ns/pF	0.81ns	2.05ns/pF	0.50ns
OAI3333	13	24	Z ↓	7.33ns/pF	1.53ns	2.10ns/pF	0.70ns
			Z ↑	9.64ns/pF	1.01ns	2.05ns/pF	0.61ns
OAI41	6	10	Z ↓	3.30ns/pF	1.25ns	1.07ns/pF	0.34ns
			Z ↑	12.88ns/pF	0.72ns	2.71ns/pF	0.45ns
OAI411	7	12	Z ↓	4.82ns/pF	1.43ns	1.56ns/pF	0.45ns
			Z ↑	12.88ns/pF	0.83ns	2.75ns/pF	0.48ns
OAI4111	8	14	Z ↓	6.41ns/pF	1.59ns	2.05ns/pF	0.55ns
			Z ↑	12.88ns/pF	0.89ns	2.71ns/pF	0.56ns
OAI42	7	12	Z ↓	3.37ns/pF	1.16ns	1.07ns/pF	0.34ns
			Z ↑	12.95ns/pF	0.58ns	2.71ns/pF	0.39ns
OAI421	9	14	Z ↓	4.76ns/pF	1.51ns	1.56ns/pF	0.50ns
			Z ↑	12.95ns/pF	0.87ns	2.75ns/pF	0.54ns
OAI4211	10	16	Z ↓	6.28ns/pF	1.75ns	2.05ns/pF	0.67ns
			Z ↑	12.88ns/pF	1.07ns	2.75ns/pF	0.65ns
OAI422	10	16	Z ↓	4.82ns/pF	1.43ns	1.60ns/pF	0.42ns
			Z ↑	12.88ns/pF	0.89ns	2.75ns/pF	0.54ns
OAI4221	11	18	Z ↓	6.28ns/pF	1.75ns	2.10ns/pF	0.59ns
			Z ↑	12.88ns/pF	1.07ns	2.75ns/pF	0.59ns
OAI4222	13	20	Z ↓	6.28ns/pF	1.81ns	2.05ns/pF	0.73ns
			Z ↑	12.88ns/pF	1.18ns	2.75ns/pF	0.71ns
OAI43	8	14	Z ↓	3.30ns/pF	1.30ns	1.03ns/pF	0.42ns
			Z ↑	12.88ns/pF	0.83ns	2.75ns/pF	0.48ns
OAI431	9	16	Z ↓	4.76ns/pF	1.51ns	1.56ns/pF	0.50ns
			Z ↑	12.95ns/pF	0.98ns	2.75ns/pF	0.59ns
OAI4311	10	18	Z ↓	6.28ns/pF	1.75ns	2.10ns/pF	0.59ns
			Z ↑	12.88ns/pF	1.07ns	2.71ns/pF	0.68ns
OAI432	11	18	Z ↓	4.76ns/pF	1.51ns	1.56ns/pF	0.50ns
			Z ↑	12.95ns/pF	0.92ns	2.75ns/pF	0.59ns
OAI4321	12	20	Z ↓	6.28ns/pF	1.75ns	2.05ns/pF	0.67ns
			Z ↑	12.95ns/pF	1.04ns	2.75ns/pF	0.65ns
OAI4322	13	22	Z ↓	6.28ns/pF	1.81ns	2.10ns/pF	0.64ns
			Z ↑	12.88ns/pF	1.18ns	2.75ns/pF	0.71ns
OAI433	11	20	Z ↓	4.76ns/pF	1.57ns	1.56ns/pF	0.56ns
			Z ↑	12.95ns/pF	1.10ns	2.71ns/pF	0.73ns
OAI4331	12	22	Z ↓	6.21ns/pF	1.89ns	2.05ns/pF	0.73ns
			Z ↑	12.95ns/pF	1.21ns	2.71ns/pF	0.79ns
OAI4332	14	24	Z ↓	6.21ns/pF	1.89ns	2.10ns/pF	0.70ns
			Z ↑	12.95ns/pF	1.21ns	2.75ns/pF	0.77ns
OAI4333	14	26	Z ↓	6.14ns/pF	2.03ns	2.10ns/pF	0.76ns
			Z ↑	12.95ns/pF	1.33ns	2.75ns/pF	0.83ns

VDD=5V, T=25°C, Nominal Process.

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
OAI44	9	16	Z ↓	3.30ns/pF	1.30ns	1.07ns/pF	0.40ns
			Z ↑	12.88ns/pF	0.89ns	2.71ns/pF	0.56ns
OAI441	11	18	Z ↓	4.76ns/pF	1.51ns	1.56ns/pF	0.50ns
			Z ↑	12.95ns/pF	0.92ns	2.75ns/pF	0.59ns
OAI4411	12	20	Z ↓	6.28ns/pF	1.81ns	2.10ns/pF	0.64ns
			Z ↑	12.95ns/pF	1.04ns	2.71ns/pF	0.73ns
OAI442	12	20	Z ↓	4.69ns/pF	1.65ns	1.56ns/pF	0.56ns
			Z ↑	12.95ns/pF	1.16ns	2.75ns/pF	0.71ns
OAI4421	13	22	Z ↓	6.21ns/pF	1.89ns	2.05ns/pF	0.73ns
			Z ↑	12.88ns/pF	1.24ns	2.75ns/pF	0.71ns
OAI4422	15	24	Z ↓	6.14ns/pF	2.03ns	2.10ns/pF	0.76ns
			Z ↑	12.88ns/pF	1.35ns	2.75ns/pF	0.83ns
OAI443	13	22	Z ↓	4.69ns/pF	1.65ns	1.56ns/pF	0.62ns
			Z ↑	12.88ns/pF	1.24ns	2.71ns/pF	0.79ns
OAI4431	14	24	Z ↓	6.14ns/pF	2.03ns	2.10ns/pF	0.76ns
			Z ↑	12.88ns/pF	1.41ns	2.75ns/pF	0.83ns
OAI4432	15	26	Z ↓	6.14ns/pF	2.03ns	2.05ns/pF	0.78ns
			Z ↑	12.88ns/pF	1.35ns	2.75ns/pF	0.83ns
OAI4433	16	28	Z ↓	6.08ns/pF	2.17ns	2.10ns/pF	0.88ns
			Z ↑	12.88ns/pF	1.64ns	2.75ns/pF	1.00ns
OAI444	14	24	Z ↓	4.62ns/pF	1.73ns	1.56ns/pF	0.62ns
			Z ↑	12.95ns/pF	1.27ns	2.71ns/pF	0.85ns
OAI4441	15	26	Z ↓	6.08ns/pF	2.11ns	2.05ns/pF	0.84ns
			Z ↑	12.95ns/pF	1.45ns	2.75ns/pF	0.88ns
OAI4442	17	28	Z ↓	6.01ns/pF	2.25ns	2.05ns/pF	0.96ns
			Z ↑	12.95ns/pF	1.62ns	2.71ns/pF	1.08ns
OAI4443	17	30	Z ↓	6.08ns/pF	2.17ns	2.10ns/pF	0.88ns
			Z ↑	12.95ns/pF	1.56ns	2.71ns/pF	1.02ns
OAI4444	19	32	Z ↓	5.95ns/pF	2.34ns	2.05ns/pF	1.02ns
			Z ↑	12.95ns/pF	1.73ns	2.75ns/pF	1.11ns

VDD=5V, T=25°C, Nominal Process.

The OR cells provide a logical OR of two to four inputs as specified by the parameter *n*.

High power and super power OR cells are available. A suffix of *H* indicates high power (2x) where an *S* suffix denotes super power (4x).

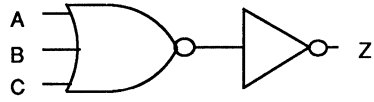
Example: OR3

Inputs
A,B,C

Outputs
Z

Logic Equation
Z = (A+B+C)

Motis Model



Capacitances

The input terminal capacitance for all OR cells is provided in the following table and is identical for all OR cells and all higher power versions.

	Terminal Capacitance
Area	0.027pF
Perf.	0.102pF

Cell Size and Delay Information

Cell	Grids	Transistors	Propagation Delay	Area		Performance	
				Extrinsic	Intrinsic	Extrinsic	Intrinsic
OR2	4	6	Z↓	1.98ns/pF	0.82ns	0.53ns/pF	0.49ns
			Z↑	3.17ns/pF	0.60ns	0.66ns/pF	0.36ns
OR2H	6	8	Z↓	1.06ns/pF	1.11ns	0.29ns/pF	0.69ns
			Z↑	1.65ns/pF	0.71ns	0.33ns/pF	0.44ns
OR2S	8	12	Z↓	0.79ns/pF	1.38ns	0.25ns/pF	0.89ns
			Z↑	0.79ns/pF	1.03ns	0.21ns/pF	0.57ns
OR3	5	8	Z↓	2.05ns/pF	1.31ns	0.58ns/pF	0.81ns
			Z↑	3.24ns/pF	0.64ns	0.70ns/pF	0.33ns
OR3H	7	10	Z↓	1.26ns/pF	1.55ns	0.37ns/pF	0.99ns
			Z↑	1.65ns/pF	0.77ns	0.33ns/pF	0.50ns
OR3S	9	14	Z↓	0.92ns/pF	2.02ns	0.29ns/pF	1.33ns
			Z↑	0.79ns/pF	1.09ns	0.16ns/pF	0.65ns
OR4	6	10	Z↓	2.18ns/pF	1.67ns	0.62ns/pF	1.02ns
			Z↑	3.24ns/pF	0.64ns	0.70ns/pF	0.33ns
OR4H	8	12	Z↓	1.39ns/pF	1.97ns	0.41ns/pF	1.26ns
			Z↑	1.65ns/pF	0.77ns	0.33ns/pF	0.50ns
OR4S	10	16	Z↓	1.06ns/pF	2.55ns	0.29ns/pF	1.79ns
			Z↑	0.79ns/pF	1.09ns	0.16ns/pF	0.65ns

VDD=5V, T=25°C, Nominal Process.

Select Data

SD210

Select either D0 or D1 to the output.

Grids 7, **Transistors** 12

Inputs
D0,D1,SD

Outputs
Z

Truth Table

INPUTS			OUTPUTS
D0	D1	SD	Z
0	X	0	0
1	X	0	1
X	0	1	0
X	1	1	1

Capacitances

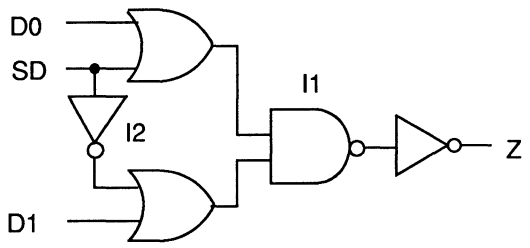
	D0	D1	SD
Area	0.029pF	0.027pF	0.054pF
Perf	0.104pF	0.102pF	0.204pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	Z ↓	2.05ns/pF	0.97ns	0.53ns/pF	0.60ns
D0 ↑	Z ↑	3.24ns/pF	0.81ns	0.70ns/pF	0.45ns
D1 ↓	Z ↓	2.05ns/pF	0.97ns	0.58ns/pF	0.52ns
D1 ↑	Z ↑	3.24ns/pF	0.75ns	0.66ns/pF	0.47ns
SD ↓	Z ↓	2.05ns/pF	0.97ns	0.58ns/pF	0.52ns
SD ↓	Z ↑	3.24ns/pF	0.81ns	0.66ns/pF	0.59ns
SD ↑	Z ↓	1.98ns/pF	1.40ns	0.53ns/pF	0.78ns
SD ↑	Z ↑	3.24ns/pF	0.75ns	0.70ns/pF	0.45ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Select Data

SD211

Select either D1 or the inversion of D0 to the output.

Grids 6, **Transistors** 10

Inputs
D0,D1,SD

Outputs
Z

Truth Table

INPUTS			OUTPUTS
D0	D1	SD	Z
0	X	0	1
1	X	0	0
X	0	1	0
X	1	1	1

Capacitances

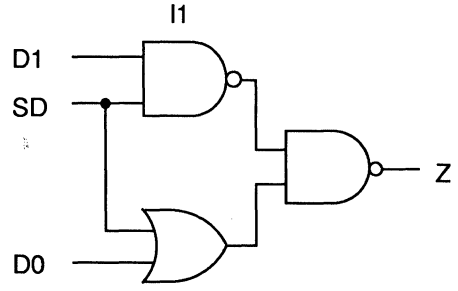
	D0	D1	SD
Area	0.027pF	0.027pF	0.058pF
Perf	0.102pF	0.102pF	0.208pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	Z ↑	6.47ns/pF	0.29ns	1.36ns/pF	0.17ns
D0 ↑	Z ↓	4.03ns/pF	0.92ns	1.07ns/pF	0.28ns
D1 ↓	Z ↓	3.96ns/pF	0.59ns	1.03ns/pF	0.36ns
D1 ↑	Z ↑	3.24ns/pF	0.81ns	0.70ns/pF	0.45ns
SD ↓	Z ↓	3.96ns/pF	0.59ns	1.03ns/pF	0.36ns
SD ↓	Z ↑	6.47ns/pF	0.29ns	1.36ns/pF	0.17ns
SD ↑	Z ↓	4.03ns/pF	0.92ns	1.07ns/pF	0.28ns
SD ↑	Z ↑	3.24ns/pF	0.81ns	0.70ns/pF	0.45ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Select Data

SD212

Select either D0 or the inversion of D1 to the output.

Grids 6, **Transistors** 10

Inputs
D0,D1,SD

Outputs
Z

Truth Table

INPUTS			OUTPUTS
D0	D1	SD	Z
0	X	0	0
1	X	0	1
X	0	1	1
X	1	1	0

Capacitances

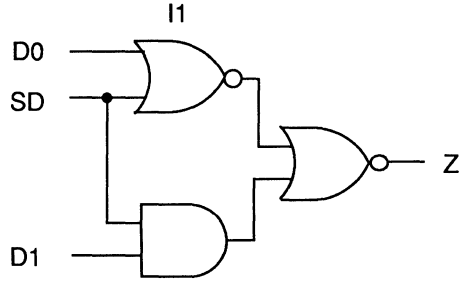
	D0	D1	SD
Area	0.027pF	0.027pF	0.058pF
Perf	0.102pF	0.102pF	0.208pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	Z ↓	1.98ns/pF	0.93ns	0.53ns/pF	0.54ns
D0 ↑	Z ↑	4.82ns/pF	0.68ns	1.03ns/pF	0.36ns
D1 ↓	Z ↑	6.41ns/pF	0.26ns	1.36ns/pF	0.17ns
D1 ↑	Z ↓	4.03ns/pF	0.92ns	1.07ns/pF	0.28ns
SD ↓	Z ↓	1.98ns/pF	0.93ns	0.53ns/pF	0.54ns
SD ↓	Z ↑	6.47ns/pF	0.29ns	1.36ns/pF	0.17ns
SD ↑	Z ↓	4.03ns/pF	0.92ns	1.07ns/pF	0.28ns
SD ↑	Z ↑	6.47ns/pF	0.64ns	1.36ns/pF	0.40ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Select Data

SD213

Select either the inversion of D0 or the inversion of D1 to the output.

Grids 6, **Transistors** 10

Inputs
D0,D1,SD

Outputs
Z

Truth Table

INPUTS			OUTPUTS
D0	D1	SD	Z
0	X	0	1
1	X	0	0
X	0	1	1
X	1	1	0

Capacitances

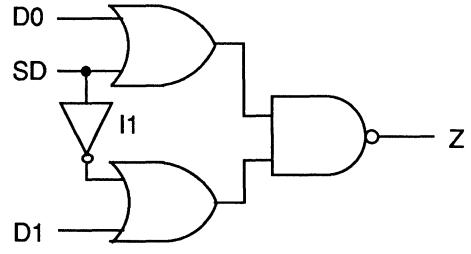
	D0	D1	SD
Area	0.027pF	0.028pF	0.058pF
Perf	0.102pF	0.103pF	0.208pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	Z ↑	6.47ns/pF	0.29ns	1.40ns/pF	0.14ns
D0 ↑	Z ↓	4.03ns/pF	0.92ns	1.07ns/pF	0.28ns
D1 ↓	Z ↑	6.47ns/pF	0.29ns	1.40ns/pF	0.14ns
D1 ↑	Z ↓	3.17ns/pF	1.01ns	0.82ns/pF	0.31ns
SD ↓	Z ↓	3.96ns/pF	0.59ns	1.03ns/pF	0.36ns
SD ↓	Z ↑	6.47ns/pF	0.29ns	1.40ns/pF	0.14ns
SD ↑	Z ↓	4.03ns/pF	0.92ns	1.07ns/pF	0.28ns
SD ↑	Z ↑	6.47ns/pF	0.75ns	1.36ns/pF	0.40ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



3-State Bus Driver — TBDI

The TBDI cells are 3-statable inverters. These cells are intended for internal bus structures.

A high power TBDI cell is available. The suffix of *H* indicates high power (2x).

Inputs
D,CK,CKN

Outputs
QN

Truth Table

INPUTS			OUTPUT
D	CK	CKN	QN
0	1	0	1
1	1	0	0
X	0	1	High Impedance

Capacitances

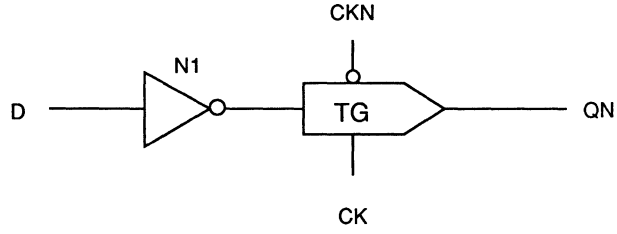
	TBDI			TBDIH		
	D	CK	CKN	D	CK	CKN
Area	0.027pF	0.012pF	0.013pF	0.055pF	0.026pF	0.028pF
Perf	0.102pF	0.012pF	0.017pF	0.205pF	0.025pF	0.036pF

Cell Size and Delay Information

					Propagation Delay			
			From	To	Area		Performance	
Cell	Grids	Transistors	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
TBDI	4	4	CK ↑	QN ↓	3.04ns/pF	0.65ns	1.81ns/pF	0.30ns
			CK ↑	QN ↑	2.97ns/pF	0.56ns	1.44ns/pF	0.35ns
			D ↓	QN ↑	3.37ns/pF	0.36ns	1.44ns/pF	0.17ns
			D ↑	QN ↓	3.04ns/pF	0.88ns	1.81ns/pF	0.24ns
TBDIH	7	8	CK ↑	QN ↓	1.78ns/pF	0.31ns	0.90ns/pF	0.26ns
			CK ↑	QN ↑	1.92ns/pF	0.03ns	0.78ns/pF	0.22ns
			D ↓	QN ↑	1.72ns/pF	0.34ns	0.70ns/pF	0.16ns
			D ↑	QN ↓	1.65ns/pF	0.71ns	0.94ns/pF	0.12ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



3-State Bus Driver — TBUS

The TBUS cells are 3-statable buffers. These cells are intended for internal bus structures.

A high power TBUS cell is available. The suffix of *H* indicates high power (2x).

Inputs
D,CK,CKN

Outputs
Q

Truth Table

INPUTS			OUTPUT
D	CK	CKN	Q
0	X	0	0
1	1	X	1
X	0	1	High Impedance

Capacitances

	TBUS			TBUSH		
	D	CK	CKN	D	CK	CKN
Area	0.057pF	0.028pF	0.028pF	0.057pF	0.028pF	0.028pF
Perf	0.107pF	0.103pF	0.103pF	0.207pF	0.103pF	0.103pF

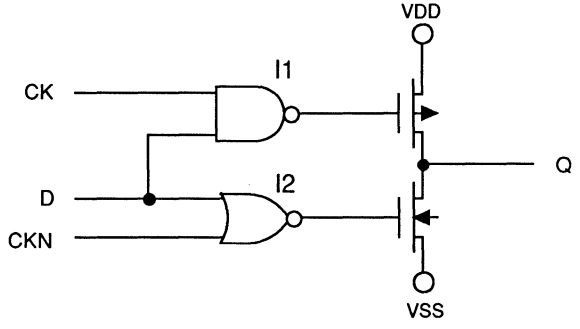
6

Cell Size and Delay Information

					Propagation Delay			
			From	To	Area		Performance	
Cell	Grids	Transistors	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
TBUS	7	10	CK ↑	Q ↓	1.98ns/pF	0.18ns	0.53ns/pF	0.26ns
			CK ↑	Q ↑	3.24ns/pF	0.64ns	0.70ns/pF	0.33ns
			D ↓	Q ↓	1.98ns/pF	0.70ns	0.53ns/pF	0.37ns
			D ↑	Q ↑	3.24ns/pF	0.64ns	0.70ns/pF	0.33ns
TBUSH	7	12	CK ↑	Q ↓	1.06ns/pF	0.24ns	0.29ns/pF	0.29ns
			CK ↑	Q ↑	1.65ns/pF	0.71ns	0.37ns/pF	0.41ns
			D ↓	Q ↓	1.06ns/pF	0.76ns	0.29ns/pF	0.40ns
			D ↑	Q ↑	1.65ns/pF	0.71ns	0.37ns/pF	0.41ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



3-State Bus Driver

TBUSI

The TBUSI cells are 3-statable inverting buffers and are intended for internal bus structures.

A high power TBUSI cell is available. The suffix of *H* indicates high power (2x).

Inputs
D,CK,CKN

Outputs
Q

Truth Table

INPUTS			OUTPUT
D	CK	CKN	Q
0	1	X	1
1	X	0	0
X	0	1	High Impedance

Capacitances

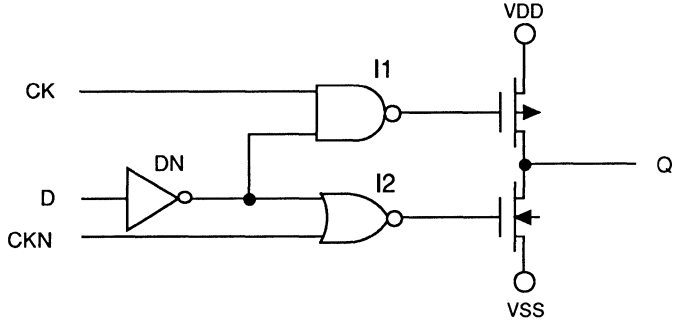
	TBUSI			TBUSIH		
	D	CK	CKN	D	CK	CKN
Area	0.027pF	0.027pF	0.028pF	0.027pF	0.027pF	0.028pF
Perf	0.102pF	0.102pF	0.103pF	0.102pF	0.102pF	0.103pF

Cell Size and Delay Information

Cell	Grids	Transistors	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
TBUSI	8	12	CK ↑	Q ↓	1.98ns/pF	0.12ns	0.49ns/pF	0.28ns
			CK ↑	Q ↑	3.24ns/pF	0.64ns	0.70ns/pF	0.33ns
			D ↓	Q ↑	3.24ns/pF	0.81ns	0.66ns/pF	0.59ns
			D ↑	Q ↓	1.98ns/pF	1.22ns	0.53ns/pF	0.66ns
TBUSIH	9	14	CK ↑	Q ↓	1.06ns/pF	0.24ns	0.29ns/pF	0.29ns
			CK ↑	Q ↑	1.65ns/pF	0.71ns	0.37ns/pF	0.41ns
			D ↓	Q ↑	1.65ns/pF	0.83ns	0.37ns/pF	0.59ns
			D ↑	Q ↓	1.06ns/pF	1.28ns	0.33ns/pF	0.67ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Transmission Gate TG*n*

The TG cells contain one or more transmission gates whose outputs are connected to form a common bus output. The parameter *n* specifies the number of transmission gates and each transmission gate consists of both an N- and P- type transistor.

Example: TG2

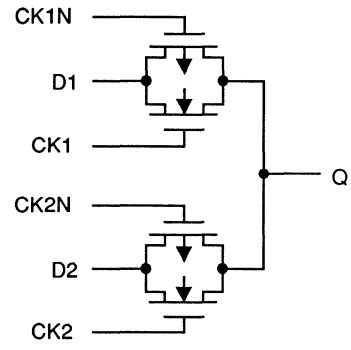
Inputs
D1,D2,CK1,CK1N,CK2,CK2N

Outputs
Q

Truth Table

INPUTS						OUTPUT
D1	D2	CK1	CK1N	CK2	CK2N	Q
0	X	1	0	0	1	0
1	X	1	0	0	1	1
X	0	0	1	1	0	0
X	1	0	1	1	0	1
X	X	0	1	0	1	High Impedance

Motis Model



6

Capacitances
The input terminal capacitance for all TG cells is provided in the following table.

	D1,D2,D3	CK1,CK2,CK3	CK1N,CK2N,CK3N
Area	0.019pF	0.012pF	0.013pF
Perf.	0.020pF	0.012pF	0.017pF

Cell Size and Delay Information

Cell	Grids	Transistors	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
TG1	4	2	CK ↑	Q ↓	3.04ns/pF	0.59ns	1.81ns/pF	0.30ns
			CK ↑	Q ↑	2.64ns/pF	0.34ns	1.48ns/pF	0.26ns
			D ↓	Q ↓	2.71ns/pF	0.03ns	1.81ns/pF	0.01ns
			D ↑	Q ↑	1.26ns/pF	0.05ns	1.40ns/pF	0.08ns
TG2	6	4	CK ↑	Q ↓	2.97ns/pF	0.68ns	1.77ns/pF	0.38ns
			CK ↑	Q ↑	2.64ns/pF	0.40ns	1.44ns/pF	0.35ns
			D ↓	Q ↓	2.77ns/pF	0.06ns	1.81ns/pF	0.07ns
			D ↑	Q ↑	1.32ns/pF	0.02ns	1.44ns/pF	0.06ns
TG3	9	6	CK ↑	Q ↓	2.97ns/pF	0.68ns	1.81ns/pF	0.36ns
			CK ↑	Q ↑	2.64ns/pF	0.40ns	1.44ns/pF	0.35ns
			D ↓	Q ↓	2.77ns/pF	0.06ns	1.81ns/pF	0.07ns
			D ↑	Q ↑	1.32ns/pF	0.02ns	1.44ns/pF	0.06ns

VDD=5V, T=25°C, Nominal Process.

Exclusive Nor

XNOR

The XNOR and XNORH cells provide the EXCLUSIVE NOR function. Additionally, since two gates are required for the XNOR function the NAND of the inputs is also provided as an output. The suffix of *H* on the XNORH indicates high power (2x).

Inputs

A,B

Outputs

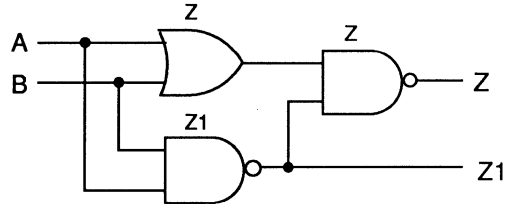
Z,Z1

Logic Equations

$$Z = (A * B) + (\overline{A} * \overline{B})$$

$$Z1 = \overline{(A * B)}$$

Motis Model



Capacitances

	XNOR		XNORH	
	A	B	A	B
Area	0.058pF	0.058pF	0.114pF	0.112pF
Perf	0.209pF	0.211pF	0.415pF	0.413pF

Cell Size and Delay Information

Cell	Grids	Transistors	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
XNOR	7	10	A ↓	Z ↓	9.45ns/pF	0.56ns	2.18ns/pF	0.31ns
			A ↓	Z ↑	6.47ns/pF	0.29ns	1.36ns/pF	0.17ns
			A ↓	Z1 ↑	3.24ns/pF	0.35ns	0.66ns/pF	0.24ns
			A ↑	Z ↓	4.03ns/pF	0.92ns	1.07ns/pF	0.28ns
			A ↑	Z ↑	8.26ns/pF	1.18ns	2.05ns/pF	0.50ns
			A ↑	Z1 ↓	4.10ns/pF	0.95ns	1.03ns/pF	0.42ns
			B ↓	Z ↓	9.45ns/pF	0.56ns	2.18ns/pF	0.31ns
			B ↓	Z ↑	6.47ns/pF	0.29ns	1.36ns/pF	0.17ns
			B ↓	Z1 ↑	3.24ns/pF	0.35ns	0.66ns/pF	0.24ns
			B ↑	Z ↓	4.03ns/pF	0.92ns	1.07ns/pF	0.28ns
			B ↑	Z ↑	8.26ns/pF	1.18ns	2.05ns/pF	0.50ns
			B ↑	Z1 ↓	4.10ns/pF	0.95ns	1.03ns/pF	0.42ns
XNORH	11	20	A ↓	Z ↓	4.69ns/pF	0.55ns	1.07ns/pF	0.34ns
			A ↓	Z ↑	3.24ns/pF	0.23ns	0.70ns/pF	0.10ns
			A ↓	Z1 ↑	1.59ns/pF	0.39ns	0.33ns/pF	0.21ns
			A ↑	Z ↓	2.18ns/pF	0.69ns	0.53ns/pF	0.26ns
			A ↑	Z ↑	4.29ns/pF	0.93ns	1.07ns/pF	0.40ns
			A ↑	Z1 ↓	2.18ns/pF	0.80ns	0.53ns/pF	0.37ns
			B ↓	Z ↓	4.69ns/pF	0.55ns	1.07ns/pF	0.34ns
			B ↓	Z ↑	3.24ns/pF	0.23ns	0.70ns/pF	0.10ns
			B ↓	Z1 ↑	1.59ns/pF	0.39ns	0.33ns/pF	0.21ns
			B ↑	Z ↓	2.18ns/pF	0.69ns	0.53ns/pF	0.26ns
			B ↑	Z ↑	4.29ns/pF	0.93ns	1.07ns/pF	0.40ns
			B ↑	Z1 ↓	2.18ns/pF	0.80ns	0.53ns/pF	0.37ns

VDD=5V, T=25°C, Nominal Process.

Exclusive Or

XOR

The XOR and XORH cells provide the EXCLUSIVE OR function. Additionally, since two gates are required for the XOR function, the NOR of the inputs is also provided as an output. The suffix of *H* on the XORH indicates high power (2x).

Inputs
A,B

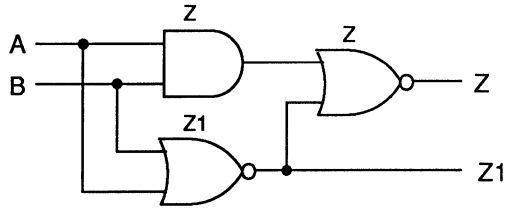
Outputs
Z,Z1

Logic Equations

$Z = (A * \overline{B}) + (\overline{A} * B)$

$Z1 = \overline{(A + B)}$

Motis Model



Capacitances

	XOR		XORH	
	A	B	A	B
Area	0.058pF	0.058pF	0.114pF	0.112pF
Perf	0.211pF	0.209pF	0.415pF	0.413pF

Cell Size and Delay Information

Cell	Grids	Transistors	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
XOR	7	10	A ↓	Z ↓	12.68ns/pF	0.62ns	2.71ns/pF	0.45ns
			A ↓	Z ↑	6.47ns/pF	0.29ns	1.36ns/pF	0.17ns
			A ↓	Z1 ↑	6.47ns/pF	0.40ns	1.36ns/pF	0.28ns
			A ↑	Z ↓	4.03ns/pF	0.92ns	1.07ns/pF	0.28ns
			A ↑	Z ↑	8.98ns/pF	1.20ns	2.01ns/pF	0.52ns
			A ↑	Z1 ↓	2.31ns/pF	0.98ns	0.58ns/pF	0.35ns
			B ↓	Z ↓	12.68ns/pF	0.62ns	2.71ns/pF	0.45ns
			B ↓	Z ↑	6.47ns/pF	0.29ns	1.36ns/pF	0.17ns
			B ↓	Z1 ↑	6.47ns/pF	0.40ns	1.36ns/pF	0.28ns
			B ↑	Z ↓	4.03ns/pF	0.92ns	1.07ns/pF	0.28ns
			B ↑	Z ↑	8.98ns/pF	1.20ns	2.01ns/pF	0.52ns
			B ↑	Z1 ↓	2.31ns/pF	0.98ns	0.58ns/pF	0.35ns
XORH	11	20	A ↓	Z ↓	6.28ns/pF	0.65ns	1.36ns/pF	0.40ns
			A ↓	Z ↑	3.17ns/pF	0.31ns	0.66ns/pF	0.18ns
			A ↓	Z1 ↑	3.24ns/pF	0.40ns	0.66ns/pF	0.30ns
			A ↑	Z ↓	2.18ns/pF	0.69ns	0.53ns/pF	0.26ns
			A ↑	Z ↑	4.69ns/pF	0.96ns	1.03ns/pF	0.42ns
			A ↑	Z1 ↓	1.39ns/pF	0.75ns	0.29ns/pF	0.35ns
			B ↓	Z ↓	6.28ns/pF	0.65ns	1.36ns/pF	0.40ns
			B ↓	Z ↑	3.17ns/pF	0.31ns	0.66ns/pF	0.18ns
			B ↓	Z1 ↑	3.24ns/pF	0.40ns	0.66ns/pF	0.30ns
			B ↑	Z ↓	2.18ns/pF	0.69ns	0.53ns/pF	0.26ns
			B ↑	Z ↑	4.69ns/pF	0.96ns	1.03ns/pF	0.42ns
			B ↑	Z1 ↓	1.39ns/pF	0.75ns	0.29ns/pF	0.35ns

VDD=5V, T=25°C, Nominal Process.

Sequential Cells

Section 7

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Introduction

Flip-Flop Information

This section contains data sheets that provide detailed information on the flip-flops and latches in the 0.9 µm CMOS Library. What follows here is some background about the flip-flop family and should help with the selection and use of these cells.

- There are 131 flip-flops and latches described in this guide.
- If scan-testing is to be used as a test strategy, many of the flip-flops have scan-test replacements available. Flip-flops that have scan-test replacements are indicated in the functional index that follows.
- A complete set of flip-flops has been provided for your use. Included in the 0.9 µm CMOS Library are flip-flops and latches with all reasonable combinations of:
  - Presets (both polarities)
  - Clears (both polarities)
  - Sample inputs
  - Clock edge- or level-triggering (both polarities)

  Having a complete set of flip-flops and latches available means that you will always be able to find the cell you need and will not need to tie off any unused inputs to either VSS or VDD. Synthesis tools also realize improved efficiency; for example, see FDS in Section 10. This saves silicon area and improves circuit performance.
- All static flip-flops and latches have both Q and QN available as outputs. This makes the library easy to use and avoids the need to add inverters to the flip-flops when inverted signals are required.
- Both area-optimized and performance-optimized versions of each cell are available. Thus, if your performance requirements do not tax the limits of the technology, you will be able to save some area by using the area-optimized library.

The convention for naming all of the sequential elements is shown in the following table. Each cell is identified via a seven-character name.

	Name = abcdefg	
a=	F	Static implementation.
b=	B	These cells contain a BIST select front end for use with the built in self test methodology.
	D	D type Flip-Flop.
	L	These cells contain a scan select front end for use with the scan testable design methodology.
	S	R-S type Flip-Flop.
c=	value	Number of clocks, not the number of phases.
d=		This parameter identifies the sample capablity.
	S	No sample input.
	P	Positive level sample.
	N	Negative level sample.
e=		When the cell has no clock inputs (**c=0**), this specifies the polarity of the S and R inputs. Otherwise, this refers to the clock inputs.
		Cells with no clock or *c=0.*
	1	Positive level S input and positive level R input.
	2	Negative level S input and negative level R input.
	7	Positive level S input and negative level R input.
	8	Negative level S input and positive level R input.
		Cells with clock inputs.
	1	Positive level sense or Master-Slave clock inputs.
	2	Negative edge triggered.
	3	Positive edge triggered.
	5	Negative level sense.

continued on next page.

(continued from previous page)

	Name = abcdefg	
f=	A	No clear or preset inputs.
	B	Positive level asynchronous preset.
	C	Positive level asynchronous preset and positive level asynchronous clear.
	D	Positive level asynchronous clear.
	E	Negative level asynchronous clear.
	F	Positive level asynchronous preset and negative level asynchronous clear.
	G	Negative level asynchronous preset.
	I	Positive level synchronous clear.
	J	Positive level synchronous preset.
	K	Negative level asynchronous preset and negative level asynchronous clear.
	L	Negative level synchronous preset.
	M	Negative level synchronous clear.
	N	Negative level asynchronous preset and positive level asynchronous clear.
	O	Positive level synchronous preset and positive level synchronous clear.
	P	Positive level synchronous preset and negative level synchronous clear.
	Q	Negative level synchronous preset and negative level synchronous clear.
	R	Negative level synchronous preset and positive level synchronous clear.
g=	X	This cell requires more than one connection for one or more of the inputs. This technique allows circuits designed with one library to be easily converted to any other library.

Example: FD1P3Q is a single clock positive edge triggered Static D type Flip-Flop with a positive level sample, a negative level synchronous preset and a negative level synchronous clear.

	a =	F	Static cell.
	b =	D	D type.
FD1P3Q	**c =**	1	Single clock.
	d =	P	Positive level sample.
	e =	3	Positive edge triggered.
	f =	Q	Synchronous negative level preset and synchronous negative level clear.

Example: FD2S1J is a Static Master-Slave D type Flip-Flop with a positive level synchronous preset.

	a =	F	Static cell.
	b =	D	D type.
FD2S1J	**c =**	2	Two clocks.
	d =	S	No sample input.
	e =	1	Master-Slave clocking.
	f =	J	Positive level synchronous preset.

The following pages tabulate the flip-flops and latches into a functional index.

Static Flip-Flops and Latches

Cell	Page	Grids	Transistors	Clocking	Preset	Clear	Sample	Scan Equivalent
FB1S2AX	7-11	23	36	NE	--	--	--	--
FB1S3AX	7-12	23	36	PE	--	--	--	--
FD1N2AX	7-13	19	26	NE	--	--	NL	FL1N2AX
FD1N2JX	7-14	21	32	NE	SPL	--	NL	FL1N2JX
FD1N2MX	7-15	21	32	NE	--	SNL	NL	FL1N2MX
FD1N3AX	7-16	19	26	PE	--	--	NL	FL1N3AX
FD1N3JX	7-17	21	32	PE	SPL	--	NL	FL1N3JX
FD1N3MX	7-18	21	32	PE	--	SNL	NL	FL1N3MX
FD1P2AX	7-19	19	26	NE	--	--	PL	FL1P2AX
FD1P2JX	7-20	21	32	NE	SPL	--	PL	FL1P2JX
FD1P2MX	7-21	21	32	NE	--	SNL	PL	FL1P2MX
FD1P3AX	7-22	19	26	PE	--	--	PL	FL1P3AX
FD1P3JX	7-23	21	32	PE	SPL	--	PL	FL1P3JX
FD1P3MX	7-24	21	32	PE	--	SNL	PL	FL1P3MX
FD1S1A	7-25	9	10	PL	--	--	--	--
FD1S1B	7-26	9	12	PL	PL	--	--	--
FD1S1D	7-27	10	14	PL	--	PL	--	--
FD1S1E	7-28	9	12	PL	--	NL	--	--
FD1S1F	7-29	11	14	PL	PL	NL	--	--
FD1S1G	7-30	10	14	PL	NL	--	--	--
FD1S2AX	7-31	13	18	NE	--	--	--	FL1S2AX
FD1S2BX	7-32	16	22	NE	PL	--	--	FL1S2BX
FD1S2CX	7-33	21	28	NE	PL	PL	--	FL1S2CX
FD1S2DX	7-34	17	24	NE	--	PL	--	FL1S2DX
FD1S2EX	7-35	16	22	NE	--	NL	--	FL1S2EX
FD1S2FX	7-36	19	26	NE	PL	NL	--	FL1S2FX
FD1S2GX	7-37	17	24	NE	NL	--	--	FL1S2GX
FD1S2IX	7-38	18	24	NE	--	SPL	--	FL1S2IX
FD1S2JX	7-39	16	22	NE	SPL	--	--	FL1S2JX
FD1S2KX	7-40	22	30	NE	NL	NL	--	FL1S2KX
FD1S2LX	7-41	18	24	NE	SNL	--	--	FL1S2LX
FD1S2MX	7-42	15	22	NE	--	SNL	--	FL1S2MX
FD1S2NX	7-43	20	28	NE	NL	PL	--	FL1S2NX
FD1S2OX	7-44	19	26	NE	SPL	SPL	--	FL1S2OX
FD1S3AX	7-45	13	18	PE	--	--	--	FL1S3AX
FD1S3BX	7-46	16	22	PE	PL	--	--	FL1S3BX
FD1S3CX	7-47	21	28	PE	PL	PL	--	FL1S3CX
FD1S3DX	7-48	17	24	PE	--	PL	--	FL1S3DX
FD1S3EX	7-49	16	22	PE	--	NL	--	FL1S3EX
FD1S3FX	7-50	19	26	PE	PL	NL	--	FL1S3FX
FD1S3GX	7-51	17	24	PE	NL	--	--	FL1S3GX

MS = Master-Slave, NE = Negative Edge-Triggered, NL = Negative Level,
PE = Positive Edge-Triggered, PL = Positive Level,
SNL = Synchronous Negative Level, SPL = Synchronous Positive Level

Static Flip-Flops and Latches

Cell	Page	Grids	Transistors	Clocking	Preset	Clear	Sample	Scan Equivalent
FD1S3IX	7-52	18	24	PE	--	SPL	--	FL1S3IX
FD1S3JX	7-53	16	22	PE	SPL	--	--	FL1S3JX
FD1S3KX	7-54	22	30	PE	NL	NL	--	FL1S3KX
FD1S3LX	7-55	18	24	PE	SNL	--	--	FL1S3LX
FD1S3MX	7-56	15	22	PE	--	SNL	--	FL1S3MX
FD1S3NX	7-57	20	28	PE	NL	PL	--	FL1S3NX
FD1S3OX	7-58	19	26	PE	SPL	SPL	--	FL1S3OX
FD1S5A	7-59	9	10	NL	--	--	--	--
FD1S5B	7-60	9	12	NL	PL	--	--	--
FD1S5D	7-61	10	14	NL	--	PL	--	--
FD1S5E	7-62	9	12	NL	--	NL	--	--
FD1S5F	7-63	11	14	NL	PL	NL	--	--
FD1S5G	7-64	10	14	NL	NL	--	--	--
FD2N1A	7-65	20	28	MS	--	--	NL	--
FD2N1J	7-66	23	34	MS	SPL	--	NL	--
FD2N1M	7-67	23	34	MS	--	SNL	NL	--
FD2P1A	7-68	20	28	MS	--	--	PL	--
FD2P1J	7-69	23	34	MS	SPL	--	PL	--
FD2P1M	7-70	23	34	MS	--	SNL	PL	--
FD2S1A	7-71	14	20	MS	--	--	--	FL2S1A
FD2S1B	7-72	17	24	MS	PL	--	--	FL2S1B
FD2S1CX	7-73	20	30	MS	PL	PL	--	FL2S1CX
FD2S1D	7-74	18	26	MS	--	PL	--	FL2S1D
FD2S1E	7-75	17	24	MS	--	NL	--	FL2S1E
FD2S1FX	7-76	19	28	MS	PL	NL	--	FL2S1FX
FD2S1G	7-77	18	26	MS	NL	--	--	FL2S1G
FD2S1I	7-78	17	26	MS	--	SPL	--	FL2S1I
FD2S1J	7-79	16	24	MS	SPL	--	--	FL2S1J
FD2S1KX	7-80	21	32	MS	NL	NL	--	FL2S1KX
FD2S1L	7-81	17	26	MS	SNL	--	--	FL2S1L
FD2S1M	7-82	16	24	MS	--	SNL	--	FL2S1M
FD2S1NX	7-83	20	30	MS	NL	PL	--	FL2S1NX
FL1N2AX	7-84	26	36	NE	--	--	NL	(FD1N2AX)
FL1N2JX	7-85	27	38	NE	SPL	--	NL	(FD1N2JX)
FL1N2MX	7-86	27	38	NE	--	SNL	NL	(FD1N2MX)
FL1N3AX	7-87	26	36	PE	--	--	NL	(FD1N3AX)
FL1N3JX	7-88	27	38	PE	SPL	--	NL	(FD1N3JX)
FL1N3MX	7-89	27	38	PE	--	SNL	NL	(FD1N3MX)
FL1P2AX	7-90	26	36	NE	--	--	PL	(FD1P2AX)
FL1P2JX	7-91	27	38	NE	SPL	--	PL	(FD1P2JX)
FL1P2MX	7-92	27	38	NE	--	SNL	PL	(FD1P2MX)
FL1P3AX	7-93	26	36	PE	--	--	PL	(FD1P3AX)
FL1P3JX	7-94	27	38	PE	SPL	--	PL	(FD1P3JX)
FL1P3MX	7-95	27	38	PE	--	SNL	PL	(FD1P3MX)

MS = Master-Slave, NE = Negative Edge-Triggered, NL = Negative Level,
PE = Positive Edge-Triggered, PL = Positive Level,
SNL = Synchronous Negative Level, SPL = Synchronous Positive Level

Static Flip-Flops and Latches

Cell	Page	Grids	Transistors	Clocking	Preset	Clear	Sample	Scan Equivalent
FL1S2AX	7-96	19	30	NE	--	--	--	(FD1S2AX)
FL1S2BX	7-97	22	34	NE	PL	--	--	(FD1S2BX)
FL1S2CX	7-98	28	40	NE	PL	PL	--	(FD1S2CX)
FL1S2DX	7-99	22	32	NE	--	PL	--	(FD1S2DX)
FL1S2EX	7-100	22	34	NE	--	NL	--	(FD1S2EX)
FL1S2FX	7-101	25	38	NE	PL	NL	--	(FD1S2FX)
FL1S2GX	7-102	22	32	NE	NL	--	--	(FD1S2GX)
FL1S2IX	7-103	23	32	NE	--	SPL	--	(FD1S2IX)
FL1S2JX	7-104	21	30	NE	SPL	--	--	(FD1S2JX)
FL1S2KX	7-105	27	38	NE	NL	NL	--	(FD1S2KX)
FL1S2LX	7-106	23	32	NE	SNL	--	--	(FD1S2LX)
FL1S2MX	7-107	20	30	NE	--	SNL	--	(FD1S2MX)
FL1S2NX	7-108	25	36	NE	NL	PL	--	(FD1S2NX)
FL1S2OX	7-109	24	34	NE	SPL	SPL	--	(FD1S2OX)
FL1S3AX	7-110	19	30	PE	--	--	--	(FD1S3AX)
FL1S3BX	7-111	22	34	PE	PL	--	--	(FD1S3BX)
FL1S3CX	7-112	28	40	PE	PL	PL	--	(FD1S3CX)
FL1S3DX	7-113	22	32	PE	--	PL	--	(FD1S3DX)
FL1S3EX	7-114	22	34	PE	--	NL	--	(FD1S3EX)
FL1S3FX	7-115	25	38	PE	PL	NL	--	(FD1S3FX)
FL1S3GX	7-116	22	32	PE	NL	--	--	(FD1S3GX)
FL1S3IX	7-117	23	32	PE	--	SPL	--	(FD1S3IX)
FL1S3JX	7-118	21	30	PE	SPL	--	--	(FD1S3JX)
FL1S3KX	7-119	27	38	PE	NL	NL	--	(FD1S3KX)
FL1S3LX	7-120	23	32	PE	SNL	--	--	(FD1S3LX)
FL1S3MX	7-121	20	30	PE	--	SNL	--	(FD1S3MX)
FL1S3NX	7-122	25	36	PE	NL	PL	--	(FD1S3NX)
FL1S3OX	7-123	24	34	PE	SPL	SPL	--	(FD1S3OX)
FL2S1A	7-124	20	32	MS	--	--	--	(FD2S1A)
FL2S1B	7-125	23	36	MS	PL	--	--	(FD2S1B)
FL2S1CX	7-126	26	42	MS	PL	PL	--	(FD2S1CX)
FL2S1D	7-127	23	34	MS	--	PL	--	(FD2S1D)
FL2S1E	7-128	23	36	MS	--	NL	--	(FD2S1E)
FL2S1FX	7-129	25	40	MS	PL	NL	--	(FD2S1FX)
FL2S1G	7-130	23	34	MS	NL	--	--	(FD2S1G)
FL2S1I	7-131	23	34	MS	--	SPL	--	(FD2S1I)
FL2S1J	7-132	21	32	MS	SPL	--	--	(FD2S1J)
FL2S1KX	7-133	26	40	MS	NL	NL	--	(FD2S1KX)
FL2S1L	7-134	23	34	MS	SNL	--	--	(FD2S1L)
FL2S1M	7-135	21	32	MS	--	SNL	--	(FD2S1M)
FL2S1NX	7-136	25	38	MS	NL	PL	--	(FD2S1NX)
FS0S1A	7-137	5	8	--	--	--	--	--
FS0S1D	7-138	6	10	--	--	PL	--	--
FS0S7A	7-139	5	8	--	--	--	--	--
FS1S1A	7-140	7	12	PL	--	--	--	--
FS1S3A	7-141	15	24	PE	--	--	--	--

MS = Master-Slave, NE = Negative Edge-Triggered, NL = Negative Level,
PE = Positive Edge-Triggered, PL = Positive Level,
SNL = Synchronous Negative Level, SPL = Synchronous Positive Level

If we turn to the FD1S2AX as an example, the following setup and propagation delay information has been provided on page 7-31.

Delay Information - FD1S2AX

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	0.58ns	0.64ns	CK ↓	Q ↓	1.98ns/pF	1.16ns	0.58ns/pF	0.98ns
D ↑	0.75ns	0.64ns	CK ↓	Q ↑	3.24ns/pF	0.98ns	0.70ns/pF	0.91ns
			CK ↓	QN ↓	7.93ns/pF	1.13ns	1.73ns/pF	1.04ns
			CK ↓	QN ↑	5.75ns/pF	1.26ns	1.40ns/pF	1.12ns

V_{DD} =5V, T=25°C, nominal process.

NOTE:

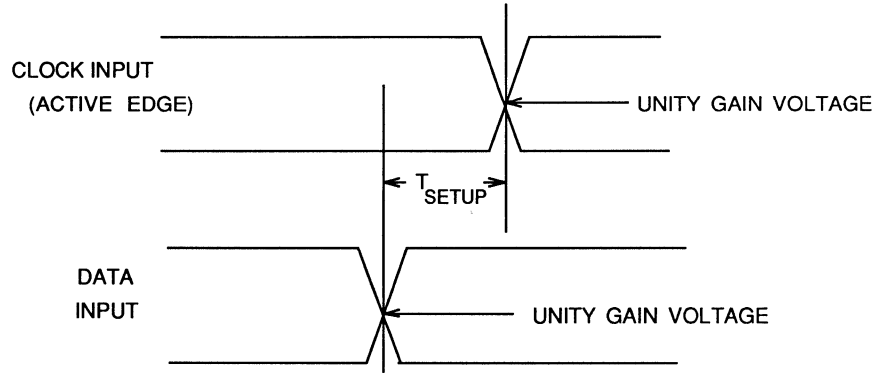
1) *Both Q and QN were equally loaded when this delay information was calculated.*
2) *When calculating estimated delay values, remember to include estimated routing capacitance. A value of 0.10 pF per fan-out is the autoroute suggested for simulation. See section 6 for a detailed description of how the delay information was calculated.*

IMPORTANT NOTE:

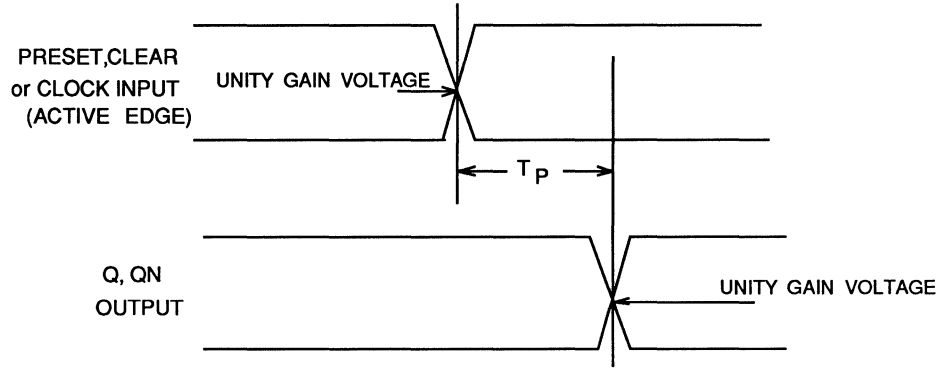
3) ***The signal name CK refers to the common connection of CKA and CKB. The X suffix in any cell name indicates that some input signals require more than one connection to the cell. The delay and truth tables always refer to the common connection of these inputs.***

A similar delay table is provided for all 131 flip-flops and latches described in this section.

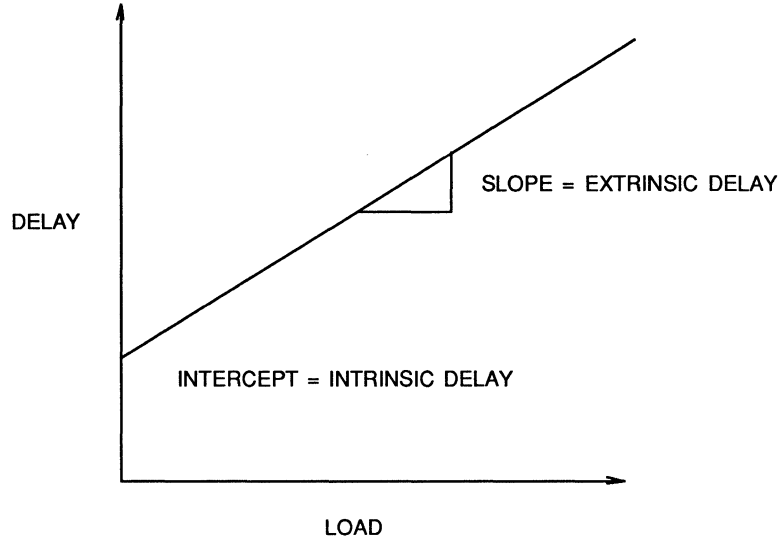
The setup times in the delay information tables are measured according to the following diagram:



Similarly, the delays from CLOCK, asynchronous PRESET or asynchronous CLEAR to OUTPUT is measured according to the following diagram:



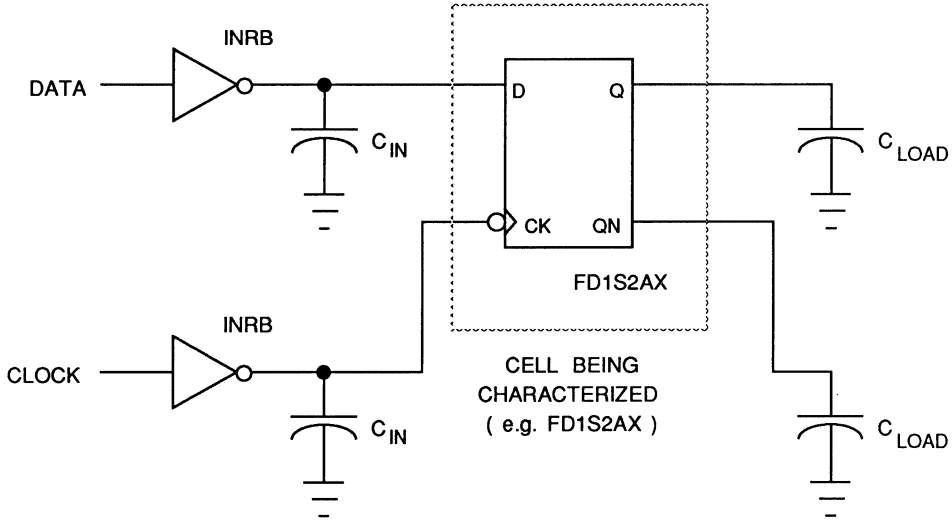
As with the logic cells, both intrinsic and extrinsic delays are specified for the output propagation delays. In graphical terms, they have the following meaning:



In physical terms, the *intrinsic* delay represents the *zero-load* delay of the output stage. The *extrinsic* delay is related to the cell's output impedance and is a measure of how the delay of the cell will vary under different loading conditions.

As with the logic cells, MOTIS3 was used to characterize the flip-flops and latches to prepare the delay information tables in this catalog. The methodology used was very similar: two sets of simulations for each flip-flop were performed, one with a fan-out of three and another with a fan-out of ten. The two delay values were then used to obtain a line intercept (an intrinsic delay) and slope (an extrinsic delay), (See pages 6-4 to 6-9 for a more detailed description of the cell characterization methodology.)

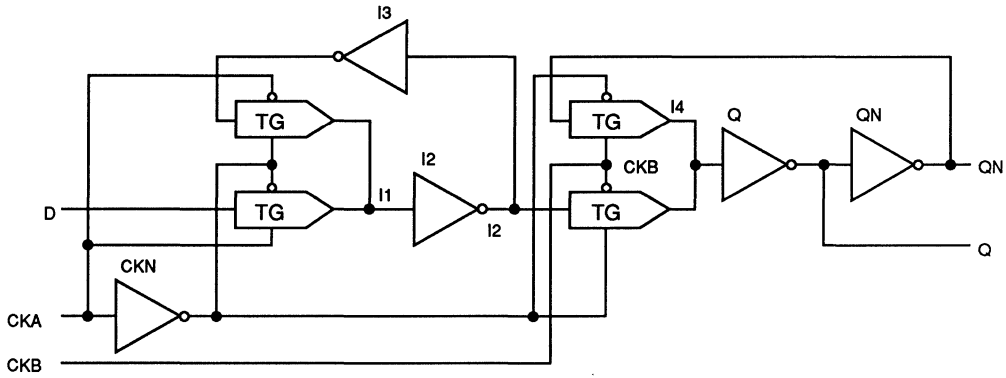
The circuit used for characterization is illustrated below:



IMPORTANT NOTE:

The signal name CK refers to the common connection of CKA and CKB. The X suffix in any cell name indicates that some input signals require more than one connection to the cell. The delay and truth tables always refer to the common connection of these inputs.

Notice that both Q and QN were loaded with CLOAD during the characterization. This is a conservative approach, because in most flip-flops, Q and QN are directly related to one another. This can be seen in the schematic of the FD1S2AX, below,



In this case, QN is an inverted version of Q. As the load on Q increases, the CK→QN delay will increase even if there is no load on QN. Thus, characterization of the FD1S2AX with identical loading on both Q and QN makes the CK→QN delay increase much more quickly than if you were to increase the load on either Q or QN alone.

If we return to the delay information table for the FD1S2AX, it can be seen that the effect of loading both Q and QN is reflected in both the intrinsic and extrinsic delay values for this cell.

The intrinsic and extrinsic delays for the area-optimized FD1S2AX can be used to write the characteristic CK→Q and CK→QN delay equations:

$T_{CK \rightarrow Q\uparrow}$ = 0.98 ns + (3.24 ns/pF) times the total load in picofarads

$T_{CK \rightarrow Q\downarrow}$ = 1.16 ns + (1.98 ns/pF) times the total load in picofarads

$T_{CK \rightarrow QN\uparrow}$ = 1.26 ns + (5.75 ns/pF) times the total load in picofarads

$T_{CK \rightarrow QN\downarrow}$ = 1.13 ns + (7.93 ns/pF) times the total load in picofarads

The intrinsic and extrinsic delays for the performance-optimized FD1S2AX can be used in a similar set of equations.

The characteristic equations can be used to estimate the output delay of flip-flops and latches. An example of their use is detailed on Pages 6-4 to 6-9.

Static D-Type Flip-Flop FB1S2AX

Negative edge triggered, BIST select front end.

Grids 23, **Transistors** 36

Inputs
D0,D1,B0,B1,CKA,CKB

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	B0	B1	CK	Q	QN	Q	QN
X	X	0	0	↓	X	X	0	1
0	X	0	X	↓	X	X	0	1
1	X	0	1	↓	X	X	1	0
X	0	X	0	↓	X	X	0	1
X	1	1	0	↓	X	X	1	0
0	0	X	X	↓	X	X	0	1
0	1	1	X	↓	X	X	1	0
1	0	X	1	↓	X	X	1	0
1	1	1	1	↓	X	X	0	1

X = Don't care

Capacitances

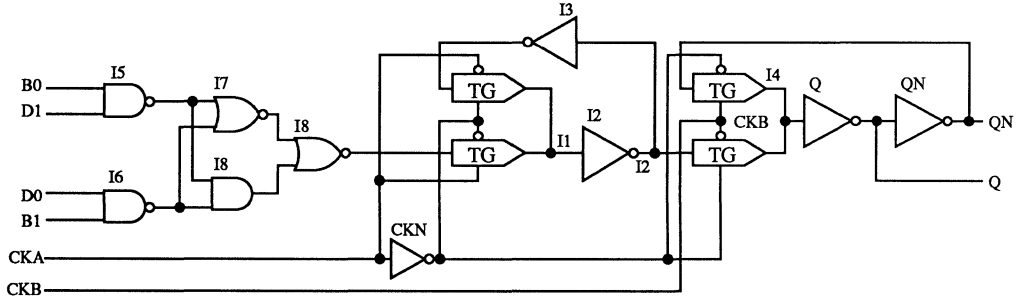
	D0	D1	B0	B1	CKA	CKB
Area	0.028pF	0.027pF	0.027pF	0.028pF	0.056pF	0.029pF
Perf	0.103pF	0.102pF	0.102pF	0.103pF	0.065pF	0.033pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
B0 ↓	2.02ns	1.33ns	CK ↓	Q ↓	1.98ns/pF	1.16ns	0.58ns/pF	0.98ns
B0 ↑	2.20ns	1.50ns	CK ↓	Q ↑	3.24ns/pF	0.98ns	0.70ns/pF	0.91ns
B1 ↓	2.02ns	1.33ns	CK ↓	QN ↓	7.93ns/pF	1.13ns	1.73ns/pF	1.04ns
B1 ↑	2.20ns	1.50ns	CK ↓	QN ↑	5.75ns/pF	1.26ns	1.40ns/pF	1.12ns
D0 ↓	2.02ns	1.33ns						
D0 ↑	2.20ns	1.50ns						
D1 ↓	2.02ns	1.33ns						
D1 ↑	2.20ns	1.50ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



7

Static D-Type Flip-Flop

FB1S3AX

Positive edge triggered, BIST select front end.

Grids 23, **Transistors** 36

Inputs
D0,D1,B0,B1,CKA,CKB

Outputs
Q,QN

Capacitances

	D0	D1	B0	B1	CKA	CKB
Area	0.028pF	0.027pF	0.027pF	0.028pF	0.057pF	0.028pF
Perf	0.103pF	0.102pF	0.102pF	0.103pF	0.065pF	0.032pF

Truth Table

INPUTS					OUTPUTS OLD		OUTPUTS NEW	
D0	D1	B0	B1	CK	Q	QN	Q	QN
X	X	0	0	↑	X	X	0	1
0	X	0	X	↑	X	X	0	1
1	X	0	1	↑	X	X	1	0
X	0	X	0	↑	X	X	0	1
X	1	1	0	↑	X	X	1	0
0	0	X	X	↑	X	X	0	1
0	1	1	X	↑	X	X	1	0
1	0	X	1	↑	X	X	1	0
1	1	1	1	↑	X	X	0	1

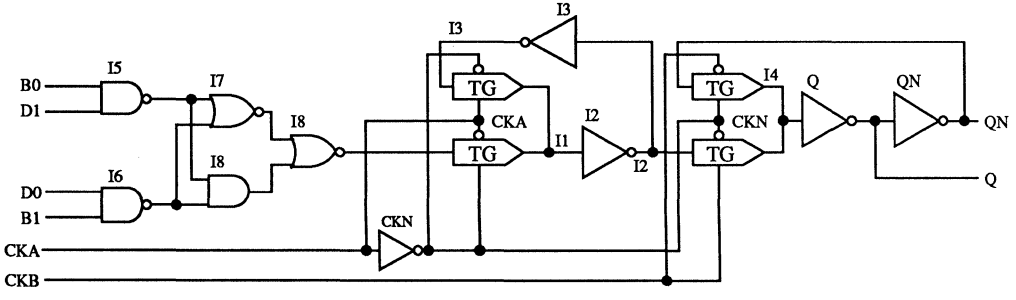
X = Don't care

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
B0 ↓	2.02ns	1.33ns	CK ↑	Q ↓	2.05ns/pF	1.54ns	0.58ns/pF	1.10ns
B0 ↑	2.20ns	1.50ns	CK ↑	Q ↑	3.24ns/pF	1.04ns	0.66ns/pF	0.88ns
B1 ↓	2.02ns	1.33ns	CK ↑	QN ↓	7.99ns/pF	1.11ns	1.73ns/pF	0.98ns
B1 ↑	2.20ns	1.50ns	CK ↑	QN ↑	5.81ns/pF	1.63ns	1.40ns/pF	1.24ns
D0 ↓	2.02ns	1.33ns						
D0 ↑	2.20ns	1.50ns						
D1 ↓	2.02ns	1.33ns						
D1 ↑	2.20ns	1.50ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1N2AX

Negative edge triggered, negative level sample.

Grids 19, **Transistors** 26

Inputs
D,SPN,CKA,CKB

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	SPN	CK	Q	QN	Q	QN
X	1	↓	1	0	1	0
X	1	↓	0	1	0	1
0	0	↓	X	X	0	1
1	0	↓	X	X	1	0

X = Don't care

Capacitances

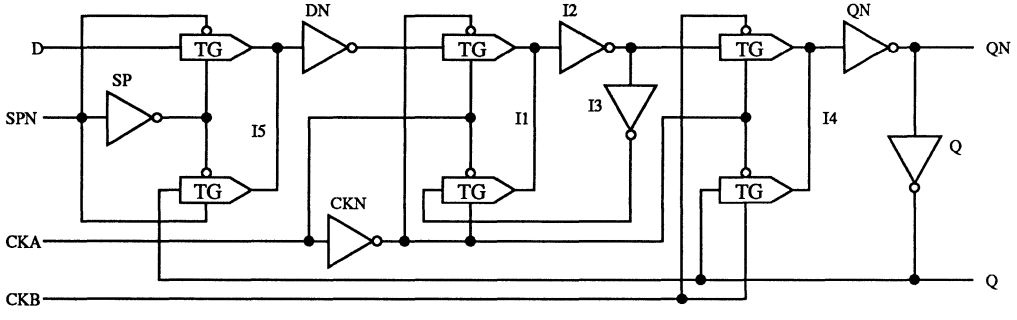
	D	SPN	CKA	CKB
Area	0.019pF	0.056pF	0.060pF	0.029pF
Perf	0.058pF	0.207pF	0.070pF	0.033pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.10ns	0.87ns	CK ↓	Q ↓	7.93ns/pF	1.19ns	1.73ns/pF	1.10ns
D ↑	1.39ns	0.92ns	CK ↓	Q ↑	5.75ns/pF	1.37ns	1.44ns/pF	1.10ns
SPN ↓	1.39ns	1.10ns	CK ↓	QN ↓	2.05ns/pF	1.14ns	0.58ns/pF	0.98ns
SPN ↑	1.56ns	1.16ns	CK ↓	QN ↑	3.24ns/pF	0.98ns	0.70ns/pF	0.91ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1N2JX

Negative edge triggered, negative level sample, positive synchronous preset.

Grids 21, **Transistors** 32

Inputs
D,SPN,CKA,CKB,PD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS OLD		OUTPUTS NEW	
D	SPN	CK	PD	Q	QN	Q	QN
X	1	↓	0	0	1	0	1
X	1	↓	X	1	0	1	0
X	X	↓	1	X	X	1	0
0	0	↓	0	X	X	0	1
1	0	↓	X	X	X	1	0

X = Don't care

Capacitances

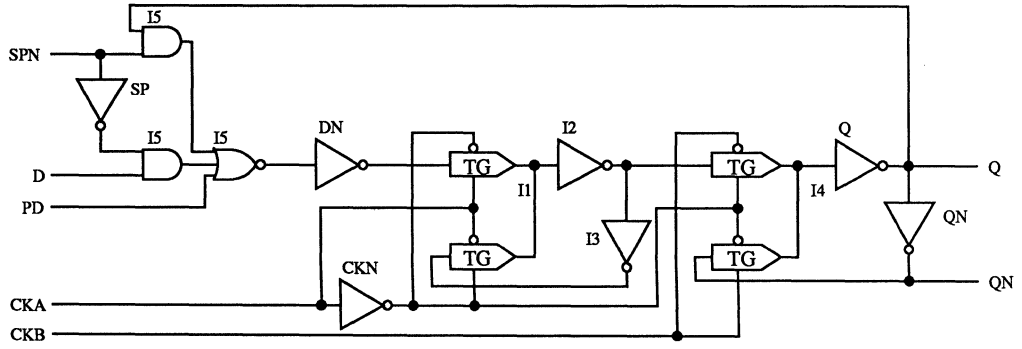
	D	SPN	CKA	CKB	PD
Area	0.029pF	0.058pF	0.057pF	0.029pF	0.027pF
Perf	0.104pF	0.208pF	0.065pF	0.033pF	0.102pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D ↓	1.85ns	1.33ns	CK ↓	Q ↓	2.05ns/pF	1.20ns	0.58ns/pF	1.04ns
D ↑	1.56ns	1.10ns	CK ↓	Q ↑	3.24ns/pF	1.10ns	0.66ns/pF	1.05ns
PD ↓	1.91ns	1.33ns	CK ↓	QN ↓	7.93ns/pF	1.30ns	1.73ns/pF	1.16ns
PD ↑	1.39ns	0.98ns	CK ↓	QN ↑	5.75ns/pF	1.37ns	1.40ns/pF	1.18ns
SPN ↓	1.85ns	1.27ns						
SPN ↑	2.20ns	1.50ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1N2MX

Negative edge triggered, negative level sample, negative synchronous clear.

Grids 21, **Transistors** 32

Inputs
D,SPN,CKA,CKB,CDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	SPN	CK	CDN	Q	QN	Q	QN
X	1	↓	X	0	1	0	1
X	1	↓	1	1	0	1	0
X	X	↓	0	X	X	0	1
0	0	↓	X	X	X	0	1
1	0	↓	1	X	X	1	0

X = Don't care

Capacitances

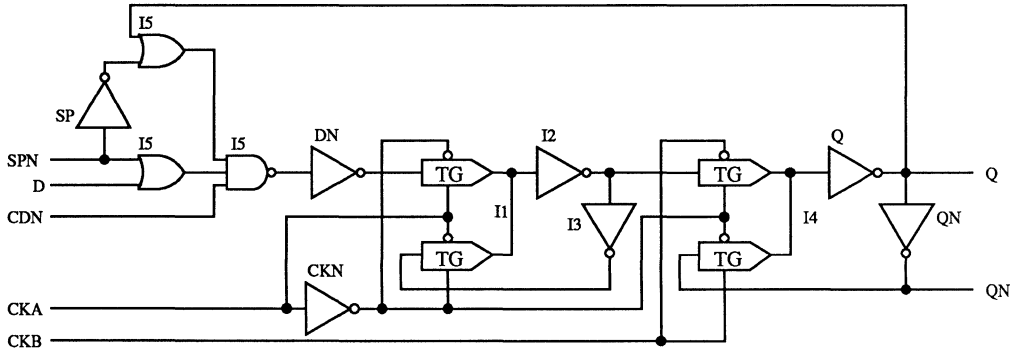
	D	SPN	CKA	CKB	CDN
Area	0.029pF	0.057pF	0.057pF	0.029pF	0.027pF
Perf	0.104pF	0.207pF	0.065pF	0.033pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	1.21ns	0.92ns	CK ↓	Q ↓	2.05ns/pF	1.20ns	0.58ns/pF	1.04ns
CDN ↑	1.73ns	1.21ns	CK ↓	Q ↑	3.24ns/pF	1.10ns	0.66ns/pF	1.05ns
D ↓	1.50ns	1.10ns	CK ↓	QN ↓	7.93ns/pF	1.30ns	1.73ns/pF	1.16ns
D ↑	1.68ns	1.16ns	CK ↓	QN ↑	5.75ns/pF	1.37ns	1.40ns/pF	1.18ns
SPN ↓	1.68ns	1.33ns						
SPN ↑	1.85ns	1.33ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1N3AX

Positive edge triggered, negative level sample.

Grids 19, **Transistors** 26

Inputs
D,SPN,CKA,CKB

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	SPN	CK	Q	QN	Q	QN
X	1	↑	0	1	0	1
X	1	↑	1	0	1	0
0	0	↑	X	X	0	1
1	0	↑	X	X	1	0

X = Don't care

Capacitances

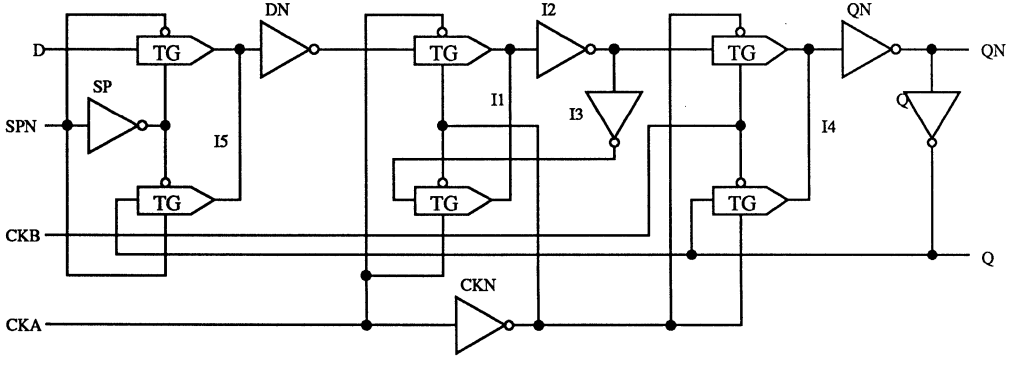
	D	SPN	CKA	CKB
Area	0.019pF	0.056pF	0.060pF	0.029pF
Perf	0.058pF	0.207pF	0.068pF	0.033pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.10ns	0.87ns	CK ↑	Q ↓	7.99ns/pF	1.16ns	1.73ns/pF	0.98ns
D ↑	1.39ns	0.92ns	CK ↑	Q ↑	5.75ns/pF	1.78ns	1.44ns/pF	1.21ns
SPN ↓	1.39ns	1.04ns	CK ↑	QN ↓	2.05ns/pF	1.54ns	0.58ns/pF	1.10ns
SPN ↑	1.56ns	1.16ns	CK ↑	QN ↑	3.24ns/pF	1.04ns	0.66ns/pF	0.88ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1N3JX

Positive edge triggered, negative level sample, positive synchronous preset.

Grids 21, **Transistors** 32

Inputs
D,SPN,CKA,CKB,PD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	SPN	CK	PD	Q	QN	Q	QN
X	1	↑	0	0	1	0	1
X	1	↑	X	1	0	1	0
X	X	↑	1	X	X	1	0
0	0	↑	0	X	X	0	1
1	0	↑	X	X	X	1	0

X = Don't care

Capacitances

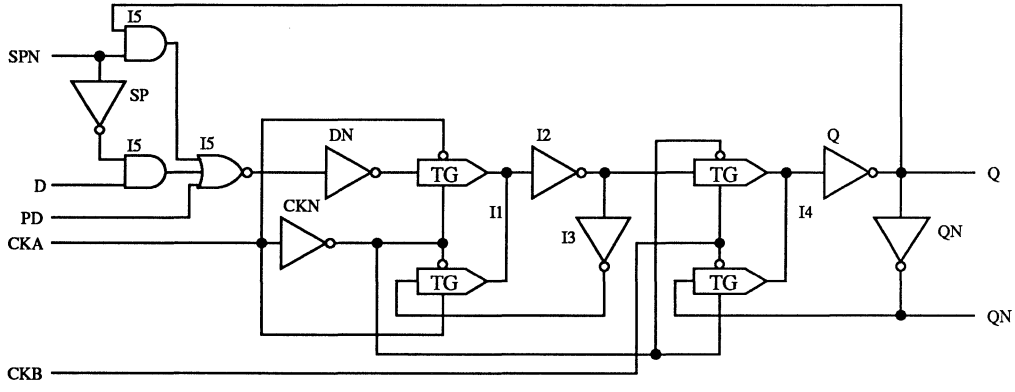
	D	SPN	CKA	CKB	PD
Area	0.029pF	0.058pF	0.057pF	0.029pF	0.027pF
Perf	0.104pF	0.208pF	0.065pF	0.033pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.85ns	1.33ns	CK ↑	Q ↓	2.05ns/pF	1.60ns	0.58ns/pF	1.16ns
D ↑	1.56ns	1.10ns	CK ↑	Q ↑	3.24ns/pF	1.10ns	0.70ns/pF	0.91ns
PD ↓	1.91ns	1.33ns	CK ↑	QN ↓	7.99ns/pF	1.28ns	1.77ns/pF	1.02ns
PD ↑	1.39ns	0.98ns	CK ↑	QN ↑	5.75ns/pF	1.78ns	1.44ns/pF	1.27ns
SPN ↓	1.85ns	1.27ns						
SPN ↑	2.20ns	1.50ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1N3MX

Positive edge triggered, negative level sample, negative synchronous clear.

Grids 21, **Transistors** 32

Inputs
D,SPN,CKA,CKB,CDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	SPN	CK	CDN	Q	QN	Q	QN
X	1	↑	X	0	1	0	1
X	1	↑	1	1	0	1	0
X	X	↑	0	X	X	0	1
0	0	↑	X	X	X	0	1
1	0	↑	1	X	X	1	0

X = Don't care

Capacitances

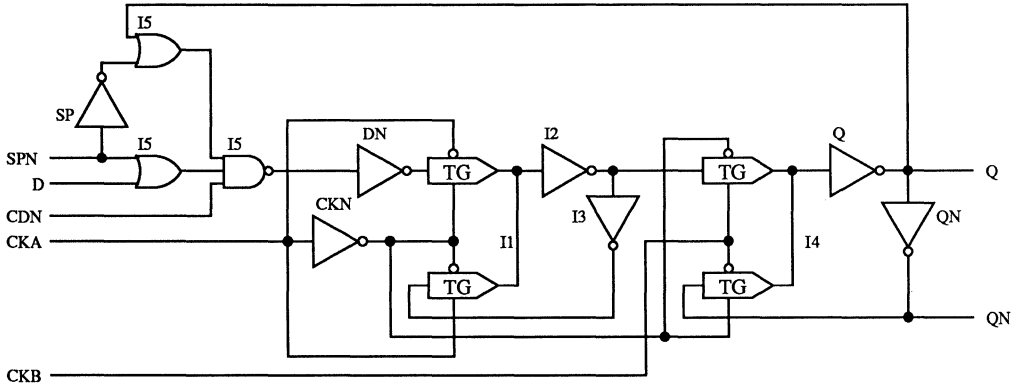
	D	SPN	CKA	CKB	CDN
Area	0.029pF	0.057pF	0.057pF	0.029pF	0.027pF
Perf	0.104pF	0.207pF	0.065pF	0.033pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	1.21ns	0.92ns	CK ↑	Q ↓	2.05ns/pF	1.60ns	0.58ns/pF	1.16ns
CDN ↑	1.73ns	1.21ns	CK ↑	Q ↑	3.24ns/pF	1.10ns	0.70ns/pF	0.91ns
D ↓	1.50ns	1.10ns	CK ↑	QN ↓	7.99ns/pF	1.28ns	1.77ns/pF	1.02ns
D ↑	1.68ns	1.16ns	CK ↑	QN ↑	5.75ns/pF	1.78ns	1.44ns/pF	1.27ns
SPN ↓	1.68ns	1.33ns						
SPN ↑	1.85ns	1.33ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1P2AX

Negative edge triggered, positive level sample.

Grids 19, **Transistors** 26

Inputs
D,SP,CKA,CKB

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	SP	CK	Q	QN	Q	QN
X	0	↓	0	1	0	1
X	0	↓	1	0	1	0
0	1	↓	X	X	0	1
1	1	↓	X	X	1	0

X = Don't care

Capacitances

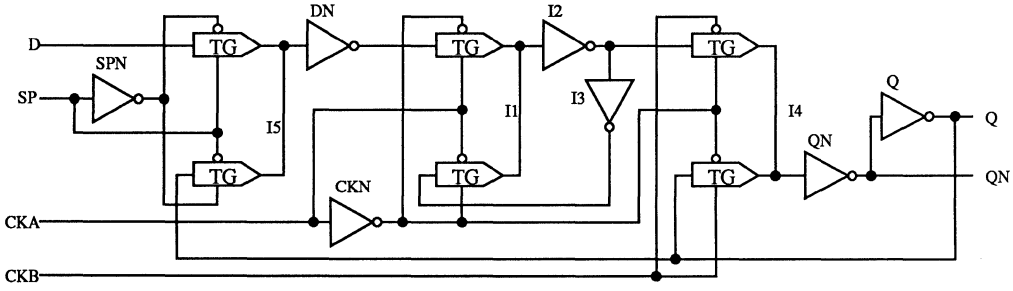
	D	SP	CKA	CKB
Area	0.019pF	0.056pF	0.060pF	0.029pF
Perf	0.058pF	0.207pF	0.070pF	0.033pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.10ns	0.87ns	CK ↓	Q ↓	7.93ns/pF	1.19ns	1.73ns/pF	1.10ns
D ↑	1.39ns	0.92ns	CK ↓	Q ↑	5.75ns/pF	1.37ns	1.44ns/pF	1.10ns
SP ↓	1.39ns	1.04ns	CK ↓	QN ↓	2.05ns/pF	1.14ns	0.58ns/pF	0.98ns
SP ↑	1.62ns	1.16ns	CK ↓	QN ↑	3.24ns/pF	0.98ns	0.70ns/pF	0.91ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1P2JX

Negative edge triggered, positive level sample, positive synchronous preset.

Grids 21, **Transistors** 32

Inputs
D,SP,CKA,CKB,PD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	SP	CK	PD	Q	QN	Q	QN
X	0	↓	0	0	1	0	1
X	0	↓	X	1	0	1	0
X	X	↓	1	X	X	1	0
0	1	↓	0	X	X	0	1
1	1	↓	X	X	X	1	0

X = Don't care

Capacitances

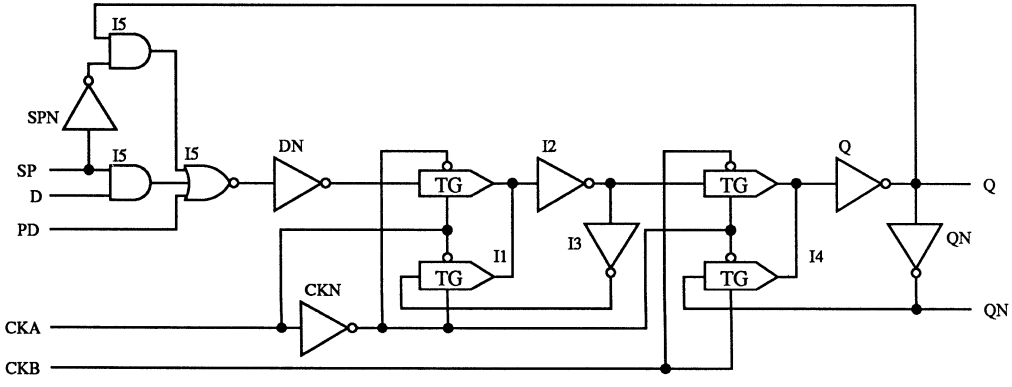
	D	SP	CKA	CKB	PD
Area	0.029pF	0.057pF	0.057pF	0.029pF	0.027pF
Perf	0.104pF	0.207pF	0.065pF	0.033pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.85ns	1.33ns	CK ↓	Q ↓	2.05ns/pF	1.20ns	0.58ns/pF	1.04ns
D ↑	1.56ns	1.10ns	CK ↓	Q ↑	3.24ns/pF	1.10ns	0.66ns/pF	1.05ns
PD ↓	1.85ns	1.33ns	CK ↓	QN ↓	7.93ns/pF	1.30ns	1.73ns/pF	1.16ns
PD ↑	1.39ns	0.98ns	CK ↓	QN ↑	5.75ns/pF	1.37ns	1.40ns/pF	1.18ns
SP ↓	1.85ns	1.27ns						
SP ↑	2.20ns	1.50ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1P2MX

Negative edge triggered, positive level sample, negative synchronous clear.

Grids 21, **Transistors** 32

Inputs
D,SP,CKA,CKB,CDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	SP	CK	CDN	Q	QN	Q	QN
X	0	↓	X	0	1	0	1
X	0	↓	1	1	0	1	0
X	X	↓	0	X	X	0	1
0	1	↓	X	X	X	0	1
1	1	↓	1	X	X	1	0

X = Don't care

Capacitances

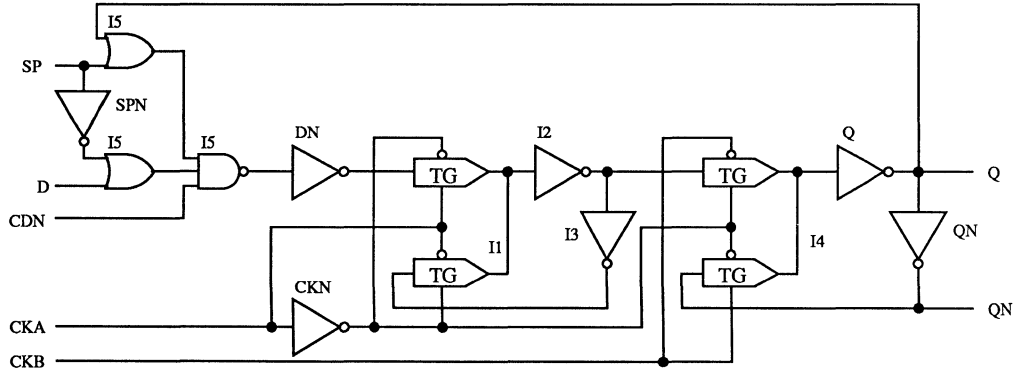
	D	SP	CKA	CKB	CDN
Area	0.029pF	0.058pF	0.057pF	0.029pF	0.027pF
Perf	0.104pF	0.208pF	0.065pF	0.033pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	1.21ns	0.92ns	CK ↓	Q ↓	2.05ns/pF	1.20ns	0.58ns/pF	1.04ns
CDN ↑	1.73ns	1.21ns	CK ↓	Q ↑	3.24ns/pF	1.10ns	0.66ns/pF	1.05ns
D ↓	1.50ns	1.10ns	CK ↓	QN ↓	7.93ns/pF	1.30ns	1.73ns/pF	1.16ns
D ↑	1.68ns	1.16ns	CK ↓	QN ↑	5.75ns/pF	1.37ns	1.40ns/pF	1.18ns
SP ↓	1.68ns	1.33ns						
SP ↑	1.85ns	1.33ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



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Static D-Type Flip-Flop

FD1P3AX

Positive edge triggered, positive level sample.

Grids 19, **Transistors** 26

Inputs
D,SP,CKA,CKB

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	SP	CK	Q	QN	Q	QN
X	0	↑	0	1	0	1
X	0	↑	1	0	1	0
0	1	↑	X	X	0	1
1	1	↑	X	X	1	0

X = Don't care

Capacitances

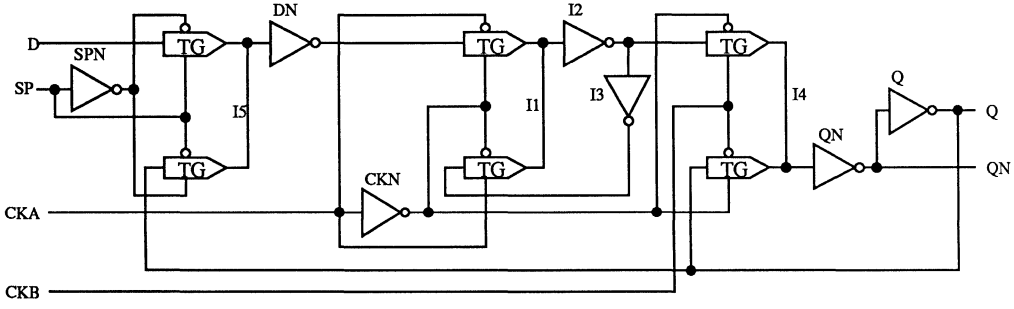
	D	SP	CKA	CKB
Area	0.019pF	0.056pF	0.060pF	0.029pF
Perf	0.058pF	0.207pF	0.068pF	0.033pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.10ns	0.87ns	CK ↑	Q ↓	7.99ns/pF	1.16ns	1.73ns/pF	0.98ns
D ↑	1.39ns	0.92ns	CK ↑	Q ↑	5.75ns/pF	1.78ns	1.44ns/pF	1.21ns
SP ↓	1.39ns	1.04ns	CK ↑	QN ↓	2.05ns/pF	1.54ns	0.58ns/pF	1.10ns
SP ↑	1.62ns	1.16ns	CK ↑	QN ↑	3.24ns/pF	1.04ns	0.66ns/pF	0.88ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1P3JX

Positive edge triggered, positive level sample, positive synchronous preset.

Grids 21, **Transistors** 32

Inputs
D,SP,CKA,CKB,PD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	SP	CK	PD	Q	QN	Q	QN
X	0	↑	0	0	1	0	1
X	0	↑	X	1	0	1	0
X	X	↑	1	X	X	1	0
0	1	↑	0	X	X	0	1
1	1	↑	X	X	X	1	0

X = Don't care

Capacitances

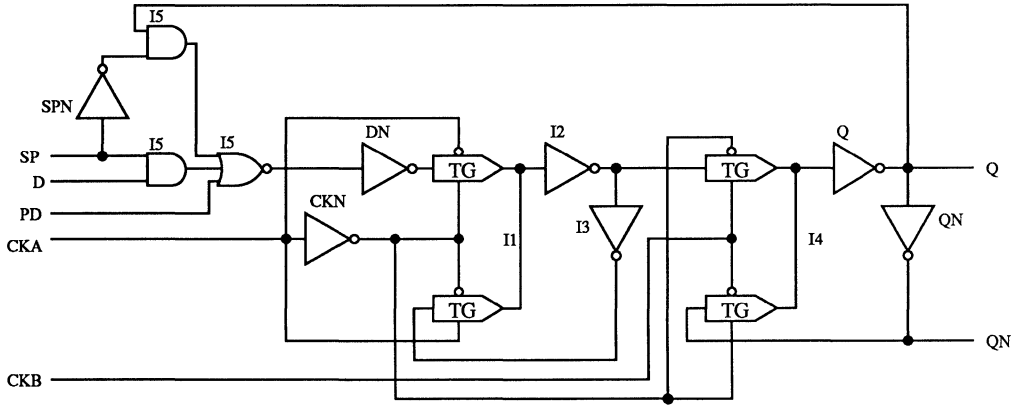
	D	SP	CKA	CKB	PD
Area	0.029pF	0.057pF	0.057pF	0.029pF	0.027pF
Perf	0.104pF	0.207pF	0.065pF	0.033pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.85ns	1.33ns	CK ↑	Q ↓	2.05ns/pF	1.60ns	0.58ns/pF	1.16ns
D ↑	1.56ns	1.10ns	CK ↑	Q ↑	3.24ns/pF	1.10ns	0.70ns/pF	0.91ns
PD ↓	1.85ns	1.33ns	CK ↑	QN ↓	7.99ns/pF	1.28ns	1.77ns/pF	1.02ns
PD ↑	1.39ns	0.98ns	CK ↑	QN ↑	5.75ns/pF	1.78ns	1.44ns/pF	1.27ns
SP ↓	1.85ns	1.27ns						
SP ↑	2.20ns	1.50ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1P3MX

Positive edge triggered, positive level sample, negative synchronous clear.

Grids 21, **Transistors** 32

Inputs
D,SP,CKA,CKB,CDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	SP	CK	CDN	Q	QN	Q	QN
X	0	↑	X	0	1	0	1
X	0	↑	1	1	0	1	0
X	X	↑	0	X	X	0	1
0	1	↑	X	X	X	0	1
1	1	↑	1	X	X	1	0

X = Don't care

Capacitances

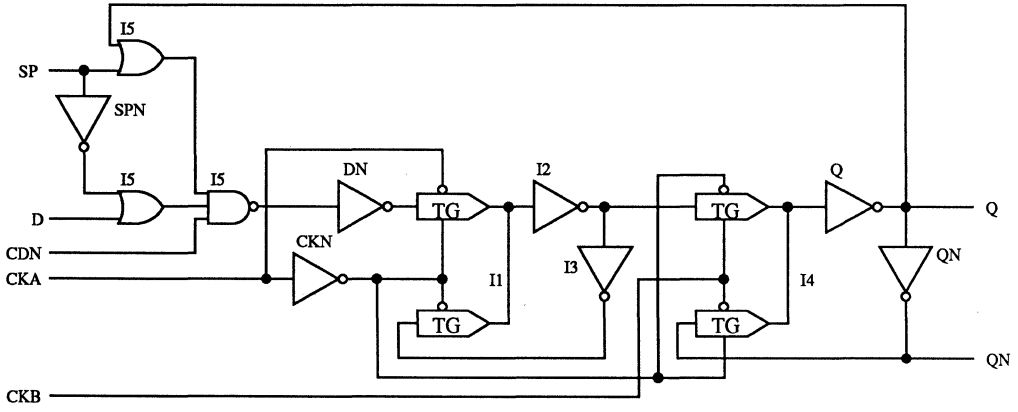
	D	SP	CKA	CKB	CDN
Area	0.029pF	0.058pF	0.057pF	0.029pF	0.027pF
Perf	0.104pF	0.208pF	0.065pF	0.033pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	1.21ns	0.92ns	CK ↑	Q ↓	2.05ns/pF	1.60ns	0.58ns/pF	1.16ns
CDN ↑	1.73ns	1.21ns	CK ↑	Q ↑	3.24ns/pF	1.10ns	0.70ns/pF	0.91ns
D ↓	1.50ns	1.10ns	CK ↑	QN ↓	7.99ns/pF	1.28ns	1.77ns/pF	1.02ns
D ↑	1.68ns	1.16ns	CK ↑	QN ↑	5.75ns/pF	1.78ns	1.44ns/pF	1.27ns
SP ↓	1.68ns	1.33ns						
SP ↑	1.85ns	1.33ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S1A

Positive level sense.

Grids 9, **Transistors** 10

Inputs
D,CK

Outputs
Q,QN

Truth Table

INPUTS		OUTPUTS			
		OLD		NEW	
D	CK	Q	QN	Q	QN
X	0	0	1	0	1
X	0	1	0	1	0
0	1	X	X	0	1
1	1	X	X	1	0

X = Don't care

Capacitances

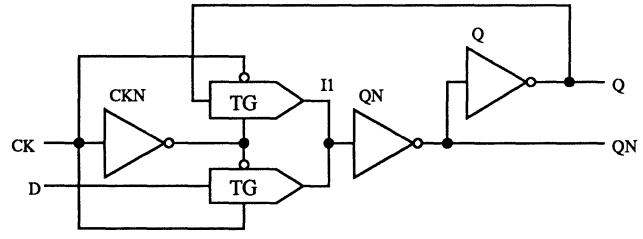
	D	CK
Area	0.019pF	0.057pF
Perf	0.020pF	0.065pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CK ↑	Q ↓	7.93ns/pF	1.19ns	1.73ns/pF	0.98ns
CK ↑	Q ↑	5.88ns/pF	1.44ns	1.40ns/pF	1.18ns
CK ↑	QN ↓	2.18ns/pF	1.26ns	0.58ns/pF	1.04ns
CK ↑	QN ↑	3.24ns/pF	1.04ns	0.66ns/pF	0.88ns
D ↓	Q ↓	7.93ns/pF	0.73ns	1.73ns/pF	0.69ns
D ↓	QN ↑	3.24ns/pF	0.52ns	0.70ns/pF	0.56ns
D ↑	Q ↑	6.14ns/pF	1.57ns	1.44ns/pF	0.92ns
D ↑	QN ↓	2.38ns/pF	1.36ns	0.62ns/pF	0.78ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S1B

Positive level sense, positive asynchronous preset.

Grids 9, **Transistors** 12

Inputs
D,CK,PD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PD	Q	QN	Q	QN
X	0	0	0	1	0	1
X	0	X	1	0	1	0
X	X	1	X	X	1	0
0	1	0	X	X	0	1
1	1	X	X	X	1	0

X = Don't care

Capacitances

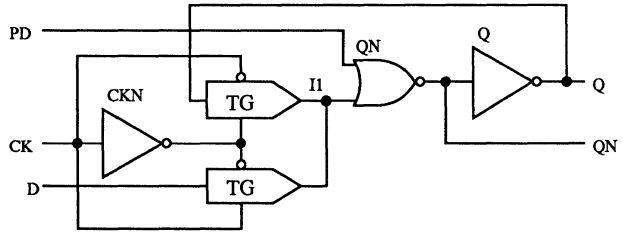
	D	CK	PD
Area	0.019pF	0.057pF	0.027pF
Perf	0.020pF	0.065pF	0.102pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CK ↑	Q ↓	12.82ns/pF	1.21ns	2.75ns/pF	1.00ns
CK ↑	Q ↑	5.88ns/pF	1.38ns	1.44ns/pF	1.10ns
CK ↑	QN ↓	2.18ns/pF	1.21ns	0.62ns/pF	0.96ns
CK ↑	QN ↑	6.47ns/pF	1.04ns	1.31ns/pF	0.94ns
D ↓	Q ↓	12.75ns/pF	0.77ns	2.71ns/pF	0.79ns
D ↓	QN ↑	6.41ns/pF	0.60ns	1.36ns/pF	0.63ns
D ↑	Q ↑	6.14ns/pF	1.45ns	1.48ns/pF	0.84ns
D ↑	QN ↓	2.44ns/pF	1.28ns	0.62ns/pF	0.78ns
PD ↑	Q ↑	6.01ns/pF	1.39ns	1.44ns/pF	0.52ns
PD ↑	QN ↓	2.31ns/pF	0.98ns	0.58ns/pF	0.35ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S1D

Positive level sense, positive asynchronous clear.

Grids 10, **Transistors** 14

Inputs
D,CK,CD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CD	Q	QN	Q	QN
X	0	X	0	1	0	1
X	0	0	1	0	1	0
X	X	1	X	X	0	1
0	1	X	X	X	0	1
1	1	0	X	X	1	0

X = Don't care

Capacitances

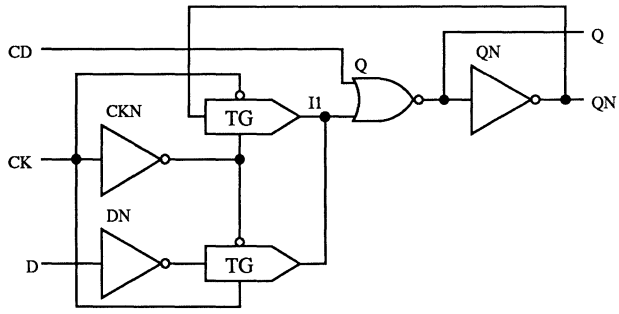
	D	CK	CD
Area	0.027pF	0.060pF	0.027pF
Perf	0.102pF	0.069pF	0.102pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CD ↑	Q ↓	2.31ns/pF	0.98ns	0.58ns/pF	0.35ns
CD ↑	QN ↑	6.01ns/pF	1.39ns	1.44ns/pF	0.52ns
CK ↑	Q ↓	2.05ns/pF	1.37ns	0.58ns/pF	1.04ns
CK ↑	Q ↑	6.47ns/pF	1.10ns	1.36ns/pF	0.92ns
CK ↑	QN ↓	12.75ns/pF	1.29ns	2.75ns/pF	1.00ns
CK ↑	QN ↑	5.75ns/pF	1.54ns	1.44ns/pF	1.10ns
D ↓	Q ↓	2.05ns/pF	1.02ns	0.58ns/pF	0.75ns
D ↓	QN ↑	5.75ns/pF	1.20ns	1.40ns/pF	0.89ns
D ↑	Q ↑	6.41ns/pF	1.12ns	1.36ns/pF	0.74ns
D ↑	QN ↓	12.75ns/pF	1.29ns	2.75ns/pF	0.83ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop FD1S1E

Positive level sense, negative asynchronous clear.

Grids 9, **Transistors** 12

Inputs
D,CK,CDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CDN	Q	QN	Q	QN
X	0	X	0	1	0	1
X	0	1	1	0	1	0
X	X	0	X	X	0	1
0	1	X	X	X	0	1
1	1	1	X	X	1	0

X = Don't care

Capacitances

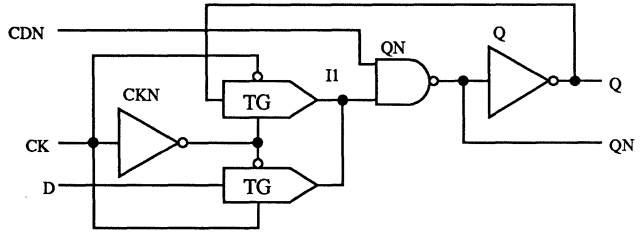
	D	CK	CDN
Area	0.019pF	0.057pF	0.027pF
Perf	0.020pF	0.065pF	0.102pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	Q ↓	7.93ns/pF	0.73ns	1.77ns/pF	0.38ns
CDN ↓	QN ↑	3.24ns/pF	0.35ns	0.66ns/pF	0.24ns
CK ↑	Q ↓	7.99ns/pF	1.11ns	1.73ns/pF	0.92ns
CK ↑	Q ↑	8.32ns/pF	1.39ns	2.05ns/pF	1.13ns
CK ↑	QN ↓	4.03ns/pF	1.26ns	1.07ns/pF	1.03ns
CK ↑	QN ↑	3.24ns/pF	0.98ns	0.70ns/pF	0.79ns
D ↓	Q ↓	7.99ns/pF	0.64ns	1.73ns/pF	0.69ns
D ↓	QN ↑	3.24ns/pF	0.52ns	0.66ns/pF	0.59ns
D ↑	Q ↑	8.32ns/pF	1.50ns	2.05ns/pF	0.90ns
D ↑	QN ↓	4.10ns/pF	1.30ns	1.07ns/pF	0.80ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S1F

Positive level sense, negative asynchronous clear, positive asynchronous preset.

Grids 11, **Transistors** 14

Inputs
D,CK,PD,CDN

Outputs
Q,QN

Capacitances

	D	CK	PD	CDN
Area	0.019pF	0.057pF	0.027pF	0.027pF
Perf	0.020pF	0.065pF	0.102pF	0.102pF

Truth Table

INPUTS				OUTPUTS OLD		OUTPUTS NEW	
D	CK	PD	CDN	Q	QN	Q	QN
X	0	0	X	0	1	0	1
X	0	X	1	1	0	1	0
X	X	X	0	X	X	0	1
X	X	1	1	X	X	1	0
0	1	0	X	X	X	0	1
1	1	X	1	X	X	1	0

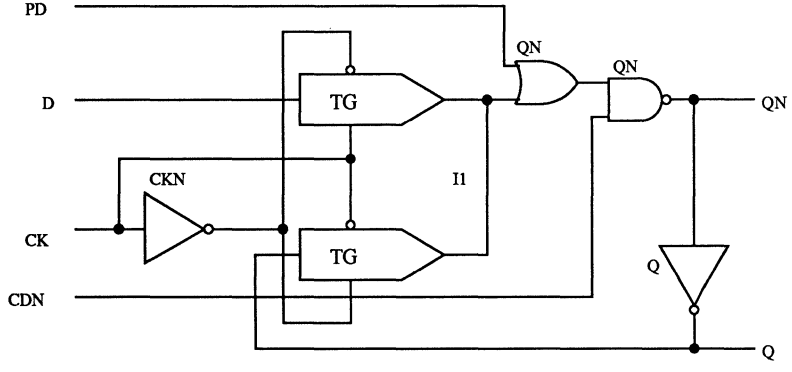
X = Don't care

Delay Information

From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
CDN ↓	Q ↓	7.93ns/pF	0.78ns	1.77ns/pF	0.38ns
CDN ↓	QN ↑	3.24ns/pF	0.40ns	0.70ns/pF	0.21ns
CK ↑	Q ↓	12.75ns/pF	1.35ns	2.71ns/pF	1.08ns
CK ↑	Q ↑	8.32ns/pF	1.39ns	2.05ns/pF	1.19ns
CK ↑	QN ↓	4.03ns/pF	1.26ns	1.07ns/pF	1.03ns
CK ↑	QN ↑	6.47ns/pF	1.10ns	1.36ns/pF	0.92ns
D ↓	Q ↓	12.75ns/pF	0.83ns	2.75ns/pF	0.77ns
D ↓	QN ↑	6.47ns/pF	0.58ns	1.36ns/pF	0.63ns
D ↑	Q ↑	8.32ns/pF	1.50ns	2.05ns/pF	0.96ns
D ↑	QN ↓	4.16ns/pF	1.27ns	1.07ns/pF	0.80ns
PD ↑	Q ↑	8.32ns/pF	1.39ns	2.05ns/pF	0.61ns
PD ↑	QN ↓	4.03ns/pF	1.03ns	1.07ns/pF	0.40ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S1G

Positive level sense, negative asynchronous preset.

Grids 10, **Transistors** 14

Inputs
D,CK,PDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PDN	Q	QN	Q	QN
X	0	1	0	1	0	1
X	0	X	1	0	1	0
X	X	0	X	X	1	0
0	1	1	X	X	0	1
1	1	X	X	X	1	0

X = Don't care

Capacitances

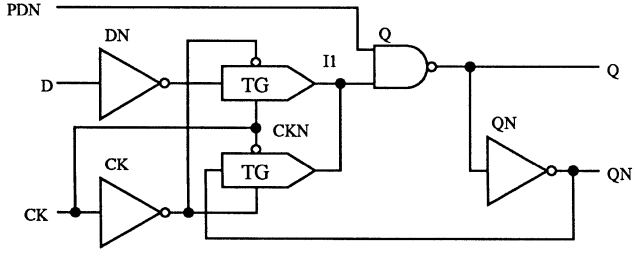
	D	CK	PDN
Area	0.027pF	0.060pF	0.027pF
Perf	0.102pF	0.069pF	0.102pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CK ↑	Q ↓	3.96ns/pF	1.35ns	1.07ns/pF	1.03ns
CK ↑	Q ↑	3.24ns/pF	1.04ns	0.70ns/pF	0.79ns
CK ↑	QN ↓	7.93ns/pF	1.19ns	1.73ns/pF	0.92ns
CK ↑	QN ↑	8.26ns/pF	1.47ns	2.05ns/pF	1.13ns
D ↓	Q ↓	3.96ns/pF	1.00ns	1.07ns/pF	0.74ns
D ↓	QN ↑	8.26ns/pF	1.12ns	2.01ns/pF	0.92ns
D ↑	Q ↑	3.24ns/pF	0.98ns	0.66ns/pF	0.70ns
D ↑	QN ↓	7.93ns/pF	1.19ns	1.77ns/pF	0.73ns
PDN ↓	Q ↑	3.24ns/pF	0.35ns	0.66ns/pF	0.24ns
PDN ↓	QN ↓	7.93ns/pF	0.73ns	1.77ns/pF	0.38ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2AX

Negative edge triggered.

Grids 13, **Transistors** 18

Inputs
D,CKA,CKB

Outputs
Q,QN

Truth Table

INPUTS		OUTPUTS			
		OLD		NEW	
D	CK	Q	QN	Q	QN
0	↓	X	X	0	1
1	↓	X	X	1	0

X = Don't care

Capacitances

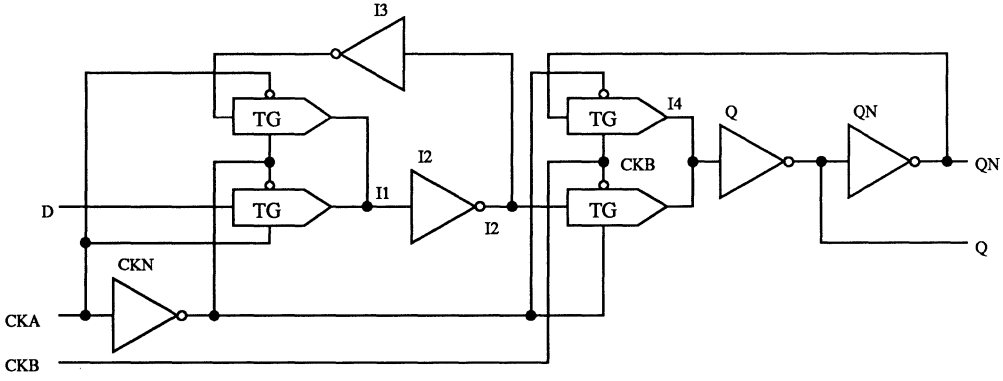
	D	CKA	CKB
Area	0.018pF	0.056pF	0.029pF
Perf	0.020pF	0.065pF	0.033pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	0.58ns	0.64ns	CK ↓	Q ↓	1.98ns/pF	1.16ns	0.58ns/pF	0.98ns
D ↑	0.75ns	0.64ns	CK ↓	Q ↑	3.24ns/pF	0.98ns	0.70ns/pF	0.91ns
			CK ↓	QN ↓	7.93ns/pF	1.13ns	1.73ns/pF	1.04ns
			CK ↓	QN ↑	5.75ns/pF	1.26ns	1.40ns/pF	1.12ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2BX

Negative edge triggered, positive asynchronous preset.

Grids 16, **Transistors** 22

Inputs
D,CKA,CKB,PD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PD	Q	QN	Q	QN
X	X	1	X	X	1	0
0	↓	0	X	X	0	1
1	↓	X	X	X	1	0

X = Don't care

Capacitances

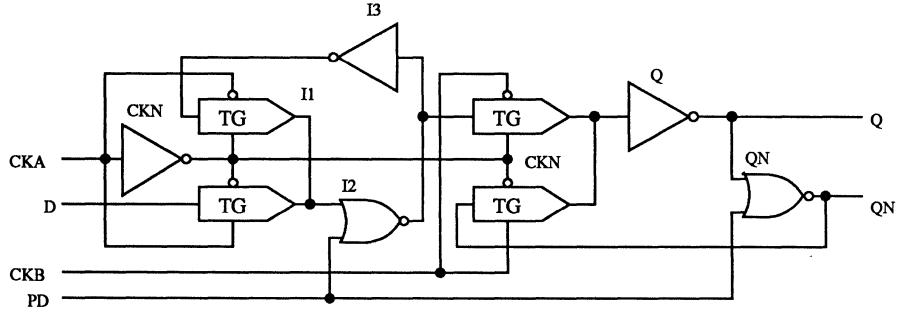
	D	CKA	CKB	PD
Area	0.019pF	0.057pF	0.029pF	0.059pF
Perf	0.020pF	0.065pF	0.033pF	0.209pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	0.87ns	0.75ns	CK ↓	Q ↓	2.11ns/pF	1.23ns	0.58ns/pF	1.04ns
D ↑	0.81ns	0.64ns	CK ↓	Q ↑	3.17ns/pF	1.01ns	0.70ns/pF	0.91ns
			CK ↓	QN ↓	7.93ns/pF	1.07ns	1.73ns/pF	1.04ns
			CK ↓	QN ↑	8.85ns/pF	1.48ns	2.05ns/pF	1.19ns
			PD ↑	Q ↑	6.01ns/pF	1.44ns	1.40ns/pF	0.78ns
			PD ↑	QN ↓	2.31ns/pF	1.10ns	0.62ns/pF	0.32ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2CX

Negative edge triggered, positive asynchronous clear, positive asynchronous preset.

Grids 21, **Transistors** 28

Inputs
D,CKA,CKB,PDA,PDB,CD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS OLD		OUTPUTS NEW	
D	CK	PD	CD	Q	QN	Q	QN
X	X	X	1	X	X	0	1
X	X	1	0	X	X	1	0
0	↓	0	X	X	X	0	1
1	↓	X	0	X	X	1	0

X = Don't care

Capacitances

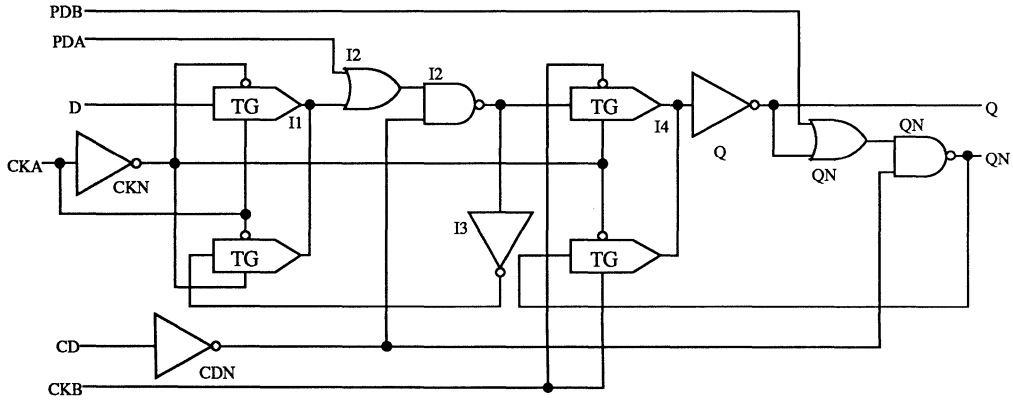
	D	CKA	CKB	PDA	PDB	CD
Area	0.019pF	0.057pF	0.028pF	0.027pF	0.027pF	0.027pF
Perf	0.020pF	0.065pF	0.032pF	0.102pF	0.102pF	0.102pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
D ↓	0.92ns	0.81ns	CD ↑	Q ↓	7.93ns/pF	1.59ns	1.77ns/pF	1.02ns
D ↑	1.04ns	0.81ns	CD ↑	QN ↑	3.24ns/pF	1.10ns	0.70ns/pF	0.56ns
			CK ↓	Q ↓	2.18ns/pF	1.21ns	0.62ns/pF	0.96ns
			CK ↓	Q ↑	3.24ns/pF	1.10ns	0.70ns/pF	0.97ns
			CK ↓	QN ↓	9.38ns/pF	1.34ns	2.14ns/pF	1.14ns
			CK ↓	QN ↑	8.79ns/pF	1.62ns	2.05ns/pF	1.19ns
			PD ↑	Q ↑	8.26ns/pF	1.64ns	2.05ns/pF	0.84ns
			PD ↑	QN ↓	4.03ns/pF	1.26ns	1.07ns/pF	0.45ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



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Static D-Type Flip-Flop

FD1S2DX

Negative edge triggered, positive asynchronous clear.

Grids 17, **Transistors** 24

Inputs
D,CKA,CKB,CD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CD	Q	QN	Q	QN
X	X	1	X	X	0	1
0	↓	X	X	X	0	1
1	↓	0	X	X	1	0

X = Don't care

Capacitances

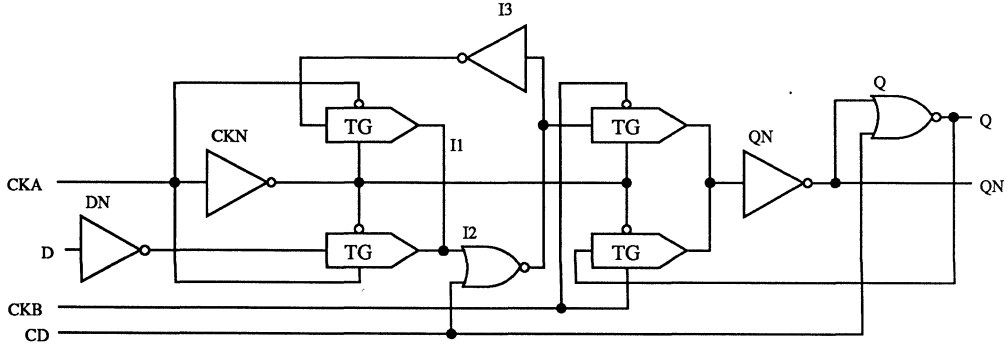
	D	CKA	CKB	CD
Area	0.027pF	0.060pF	0.029pF	0.059pF
Perf	0.102pF	0.069pF	0.033pF	0.209pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	0.98ns	0.69ns	CD ↑	Q ↓	2.31ns/pF	1.10ns	0.62ns/pF	0.32ns
D ↑	1.39ns	0.87ns	CD ↑	QN ↑	6.01ns/pF	1.44ns	1.40ns/pF	0.78ns
			CK ↓	Q ↓	7.93ns/pF	1.07ns	1.73ns/pF	1.04ns
			CK ↓	Q ↑	8.85ns/pF	1.48ns	2.05ns/pF	1.19ns
			CK ↓	QN ↓	2.11ns/pF	1.23ns	0.62ns/pF	0.96ns
			CK ↓	QN ↑	3.17ns/pF	1.01ns	0.70ns/pF	0.91ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2EX

Negative edge triggered, negative asynchronous clear.

Grids 16, **Transistors** 22

Inputs
D,CKA,CKB,CDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CDN	Q	QN	Q	QN
X	X	0	X	X	0	1
0	↓	X	X	X	0	1
1	↓	1	X	X	1	0

X = Don't care

Capacitances

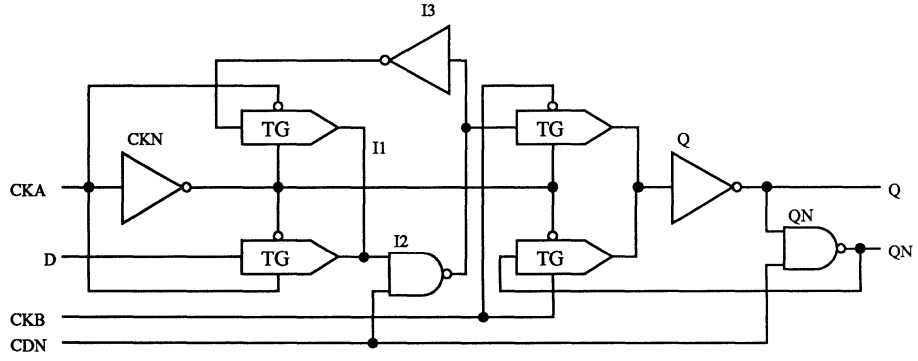
	D	CKA	CKB	CDN
Area	0.019pF	0.057pF	0.028pF	0.057pF
Perf	0.020pF	0.065pF	0.032pF	0.208pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	0.64ns	0.64ns	CDN ↓	Q ↓	7.99ns/pF	0.93ns	1.77ns/pF	0.73ns
D ↑	1.04ns	0.81ns	CDN ↓	QN ↑	3.24ns/pF	0.52ns	0.70ns/pF	0.21ns
			CK ↓	Q ↓	2.05ns/pF	1.02ns	0.58ns/pF	0.92ns
			CK ↓	Q ↑	3.24ns/pF	1.10ns	0.66ns/pF	0.99ns
			CK ↓	QN ↓	9.38ns/pF	1.34ns	2.14ns/pF	1.14ns
			CK ↓	QN ↑	5.75ns/pF	1.20ns	1.40ns/pF	1.07ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2FX

Negative edge triggered, negative asynchronous clear, positive asynchronous preset.

Grids 19, **Transistors** 26

Inputs
D,CKA,CKB,PDA,PDB,CDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	CK	PD	CDN	Q	QN	Q	QN
X	X	X	0	X	X	0	1
X	X	1	1	X	X	1	0
0	↓	0	X	X	X	0	1
1	↓	X	1	X	X	1	0

X = Don't care

Capacitances

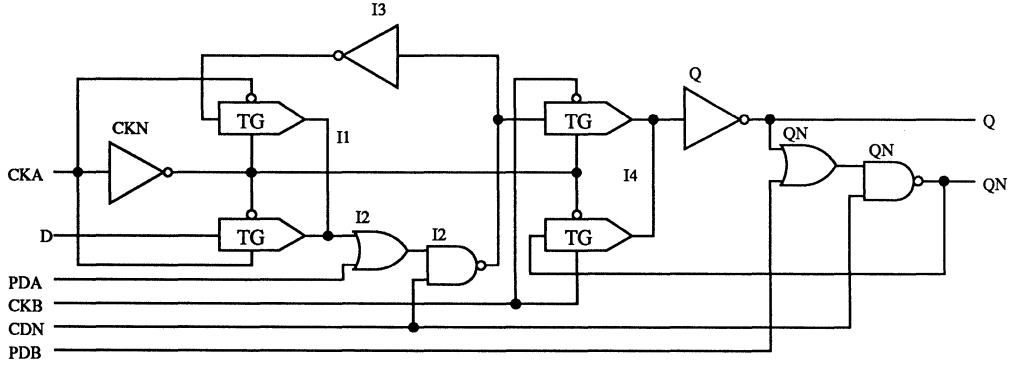
	D	CKA	CKB	PDA	PDB	CDN
Area	0.019pF	0.057pF	0.028pF	0.027pF	0.027pF	0.057pF
Perf	0.020pF	0.065pF	0.032pF	0.102pF	0.103pF	0.207pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	0.92ns	0.81ns	CDN ↓	Q ↓	7.93ns/pF	1.07ns	1.77ns/pF	0.78ns
D ↑	1.04ns	0.81ns	CDN ↓	QN ↑	3.24ns/pF	0.58ns	0.70ns/pF	0.27ns
			CK ↓	Q ↓	2.11ns/pF	1.29ns	0.58ns/pF	1.04ns
			CK ↓	Q ↑	3.24ns/pF	1.10ns	0.70ns/pF	0.97ns
			CK ↓	QN ↓	9.38ns/pF	1.34ns	2.14ns/pF	1.20ns
			CK ↓	QN ↑	8.72ns/pF	1.70ns	2.05ns/pF	1.25ns
			PD ↑	Q ↑	8.26ns/pF	1.64ns	2.05ns/pF	0.90ns
			PD ↑	QN ↓	4.03ns/pF	1.26ns	1.07ns/pF	0.45ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2GX

Negative edge triggered, negative asynchronous preset.

Grids 17, **Transistors** 24

Inputs
D,CKA,CKB,PDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PDN	Q	QN	Q	QN
X	X	0	X	X	1	0
0	↓	1	X	X	0	1
1	↓	X	X	X	1	0

X = Don't care

Capacitances

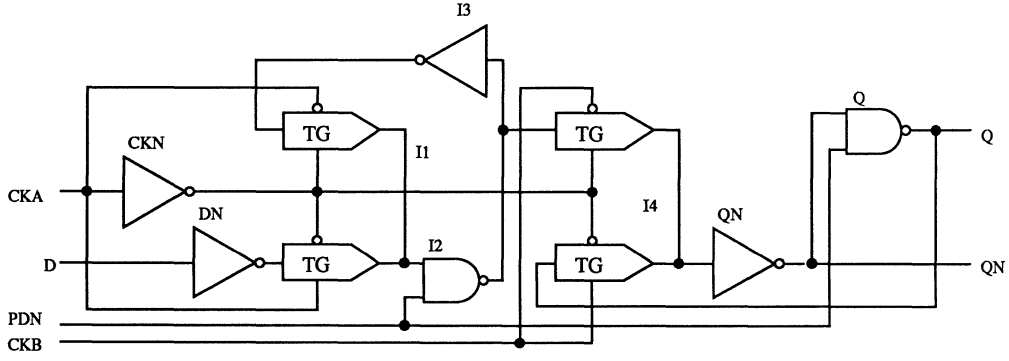
	D	CKA	CKB	PDN
Area	0.027pF	0.061pF	0.028pF	0.057pF
Perf	0.102pF	0.071pF	0.032pF	0.208pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.04ns	0.81ns	CK ↓	Q ↓	9.38ns/pF	1.34ns	2.14ns/pF	1.14ns
D ↑	1.16ns	0.75ns	CK ↓	Q ↑	5.75ns/pF	1.20ns	1.40ns/pF	1.07ns
			CK ↓	QN ↓	2.05ns/pF	1.02ns	0.58ns/pF	0.92ns
			CK ↓	QN ↑	3.24ns/pF	1.10ns	0.66ns/pF	0.99ns
			PDN ↓	Q ↑	3.24ns/pF	0.52ns	0.70ns/pF	0.21ns
			PDN ↓	QN ↓	7.99ns/pF	0.93ns	1.77ns/pF	0.73ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2IX

Negative edge triggered, positive synchronous clear.

Grids 18, **Transistors** 24

Inputs
D,CKA,CKB,CD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CD	Q	QN	Q	QN
X	↓	1	X	X	0	1
0	↓	X	X	X	0	1
1	↓	0	X	X	1	0

X = Don't care

Capacitances

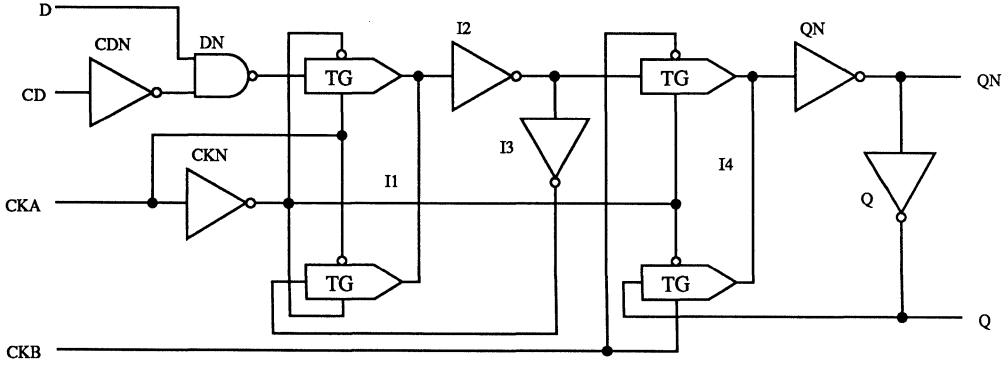
	D	CKA	CKB	CD
Area	0.027pF	0.057pF	0.029pF	0.027pF
Perf	0.102pF	0.065pF	0.033pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CD ↓	1.27ns	0.92ns	CK ↓	Q ↓	7.93ns/pF	1.13ns	1.73ns/pF	1.04ns
CD ↑	1.33ns	0.92ns	CK ↓	Q ↑	5.75ns/pF	1.26ns	1.44ns/pF	1.04ns
D ↓	1.04ns	0.69ns	CK ↓	QN ↓	1.98ns/pF	1.16ns	0.58ns/pF	0.98ns
D ↑	1.44ns	0.87ns	CK ↓	QN ↑	3.24ns/pF	0.98ns	0.70ns/pF	0.91ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2JX

Negative edge triggered, positive synchronous preset.

Grids 16, **Transistors** 22

Inputs
D,CKA,CKB,PD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PD	Q	QN	Q	QN
X	↓	1	X	X	1	0
0	↓	0	X	X	0	1
1	↓	X	X	X	1	0

X = Don't care

Capacitances

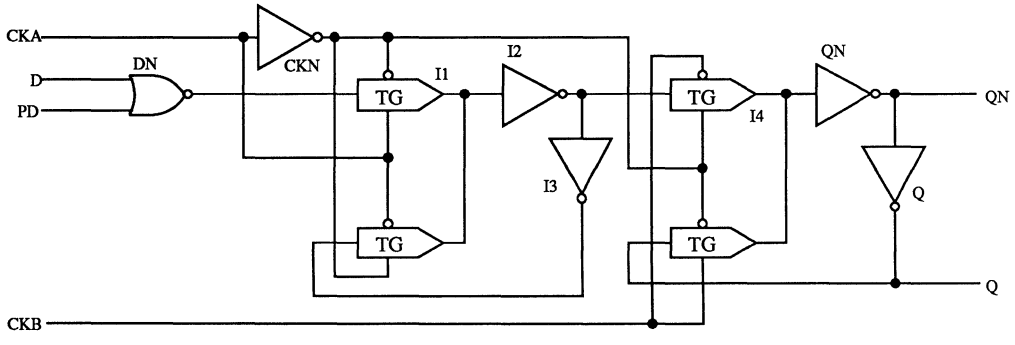
	D	CKA	CKB	PD
Area	0.027pF	0.058pF	0.028pF	0.027pF
Perf	0.102pF	0.066pF	0.032pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.33ns	0.92ns	CK ↓	Q ↓	7.93ns/pF	1.13ns	1.73ns/pF	1.04ns
D ↑	1.16ns	0.75ns	CK ↓	Q ↑	5.75ns/pF	1.26ns	1.44ns/pF	1.04ns
PD ↓	1.33ns	0.92ns	CK ↓	QN ↓	1.98ns/pF	1.16ns	0.58ns/pF	0.98ns
PD ↑	1.16ns	0.75ns	CK ↓	QN ↑	3.24ns/pF	0.98ns	0.70ns/pF	0.91ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2MX

Negative edge triggered, negative synchronous clear.

Grids 15, **Transistors** 22

Inputs
D,CKA,CKB,CDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CDN	Q	QN	Q	QN
X	↓	0	X	X	0	1
0	↓	X	X	X	0	1
1	↓	1	X	X	1	0

X = Don't care

Capacitances

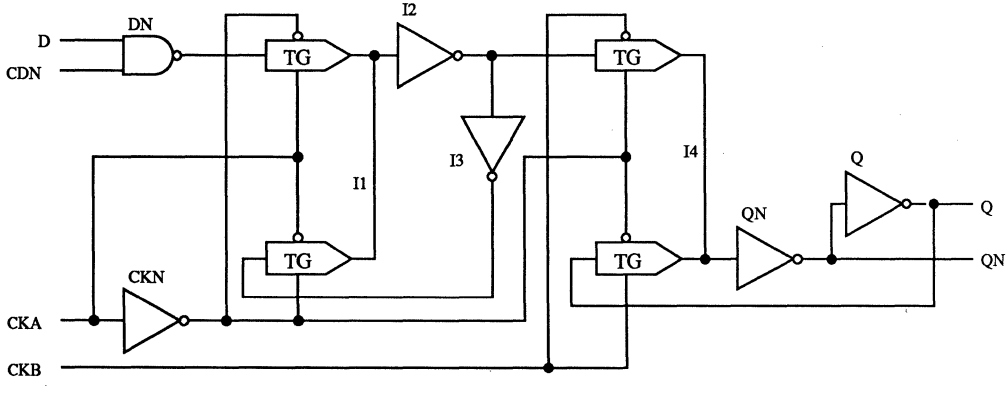
	D	CKA	CKB	CDN
Area	0.027pF	0.058pF	0.028pF	0.027pF
Perf	0.102pF	0.066pF	0.032pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	0.98ns	0.75ns	CK ↓	Q ↓	7.93ns/pF	1.07ns	1.73ns/pF	1.04ns
CDN ↑	1.44ns	0.92ns	CK ↓	Q ↑	5.75ns/pF	1.14ns	1.44ns/pF	0.98ns
D ↓	0.98ns	0.75ns	CK ↓	QN ↓	2.05ns/pF	0.97ns	0.58ns/pF	0.92ns
D ↑	1.44ns	0.92ns	CK ↓	QN ↑	3.24ns/pF	0.92ns	0.66ns/pF	0.93ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2NX

Negative edge triggered, positive asynchronous clear, negative asynchronous preset.

Grids 20, **Transistors** 28

Inputs
D,CKA,CKB,PDNA,PDNB,CD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	CK	PDN	CD	Q	QN	Q	QN
X	X	X	1	X	X	0	1
X	X	0	0	X	X	1	0
0	↓	1	X	X	X	0	1
1	↓	X	0	X	X	1	0

X = Don't care

Capacitances

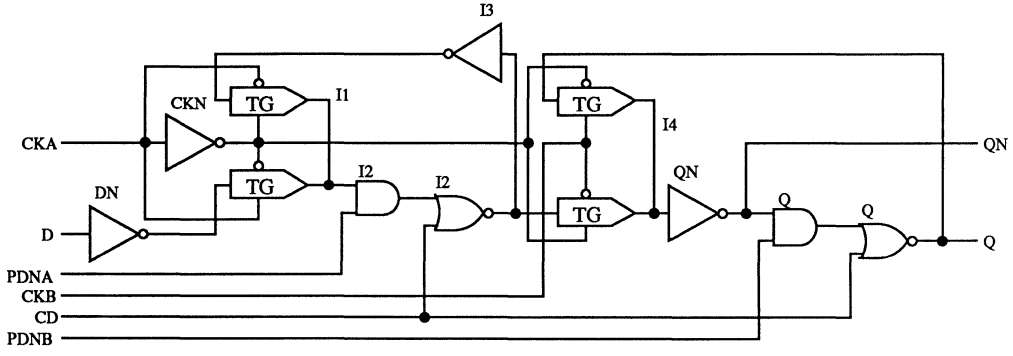
	D	CKA	CKB	PDNA	PDNB	CD
Area	0.027pF	0.058pF	0.029pF	0.027pF	0.027pF	0.057pF
Perf	0.102pF	0.066pF	0.033pF	0.102pF	0.103pF	0.207pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.16ns	0.87ns	CD ↑	Q ↓	2.25ns/pF	1.18ns	0.58ns/pF	0.40ns
D ↑	1.44ns	0.98ns	CD ↑	QN ↑	6.01ns/pF	1.50ns	1.40ns/pF	0.83ns
			CK ↓	Q ↓	9.31ns/pF	1.42ns	2.14ns/pF	1.20ns
			CK ↓	Q ↑	8.85ns/pF	1.65ns	2.05ns/pF	1.25ns
			CK ↓	QN ↓	2.11ns/pF	1.35ns	0.58ns/pF	1.04ns
			CK ↓	QN ↑	3.24ns/pF	1.10ns	0.70ns/pF	0.97ns
			PDN ↓	Q ↑	6.47ns/pF	0.81ns	1.36ns/pF	0.45ns
			PDN ↓	QN ↓	12.75ns/pF	1.46ns	2.75ns/pF	1.00ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S2OX

Negative edge triggered, positive synchronous clear, positive synchronous preset.

Grids 19, **Transistors** 26

Inputs
D,CKA,CKB,PD,CD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	CK	PD	CD	Q	QN	Q	QN
X	↓	X	1	X	X	0	1
X	↓	1	0	X	X	1	0
0	↓	0	X	X	X	0	1
1	↓	X	0	X	X	1	0

X = Don't care

Capacitances

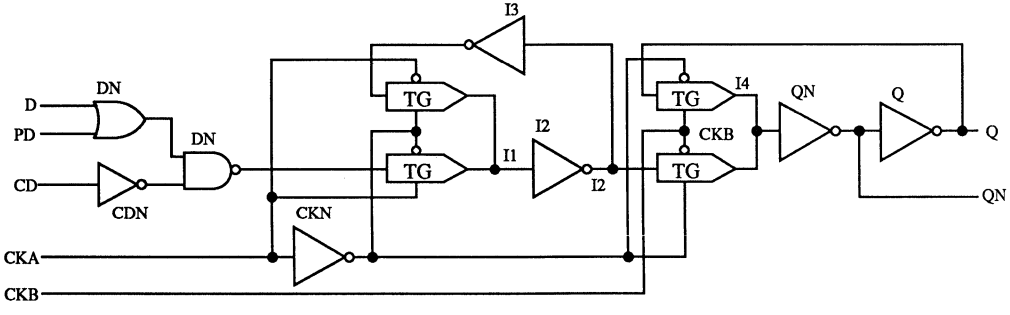
	D	CKA	CKB	PD	CD
Area	0.027pF	0.057pF	0.029pF	0.027pF	0.027pF
Perf	0.102pF	0.065pF	0.033pF	0.102pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CD ↓	1.33ns	0.98ns	CK ↓	Q ↓	7.93ns/pF	1.13ns	1.73ns/pF	1.04ns
CD ↑	1.39ns	0.92ns	CK ↓	Q ↑	5.75ns/pF	1.26ns	1.44ns/pF	1.04ns
D ↓	1.44ns	0.92ns	CK ↓	QN ↓	1.98ns/pF	1.16ns	0.58ns/pF	0.98ns
D ↑	1.44ns	0.87ns	CK ↓	QN ↑	3.24ns/pF	0.98ns	0.70ns/pF	0.91ns
PD ↓	1.44ns	0.92ns						
PD ↑	1.44ns	0.87ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3AX

Positive edge triggered.

Grids 13, **Transistors** 18

Inputs
D,CKA,CKB

Outputs
Q,QN

Truth Table

INPUTS		OUTPUTS			
		OLD		NEW	
D	CK	Q	QN	Q	QN
0	↑	X	X	0	1
1	↑	X	X	1	0

X = Don't care

Capacitances

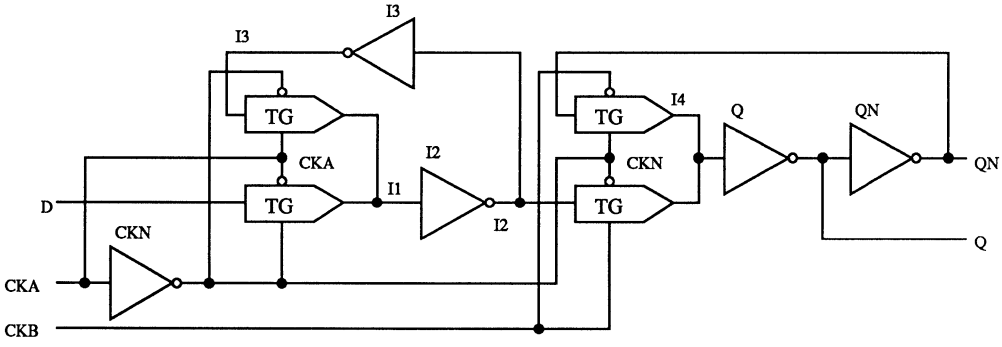
	D	CKA	CKB
Area	0.019pF	0.056pF	0.028pF
Perf	0.020pF	0.065pF	0.032pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	0.58ns	0.64ns	CK ↑	Q ↓	1.98ns/pF	1.51ns	0.58ns/pF	1.04ns
D ↑	0.81ns	0.64ns	CK ↑	Q ↑	3.24ns/pF	0.92ns	0.70ns/pF	0.79ns
			CK ↑	QN ↓	7.93ns/pF	1.07ns	1.73ns/pF	0.92ns
			CK ↑	QN ↑	5.75ns/pF	1.60ns	1.40ns/pF	1.18ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3BX

Positive edge triggered, positive asynchronous preset.

Grids 16, **Transistors** 22

Inputs
D,CKA,CKB,PD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PD	Q	QN	Q	QN
X	X	1	X	X	1	0
0	↑	0	X	X	0	1
1	↑	X	X	X	1	0

X = Don't care

Capacitances

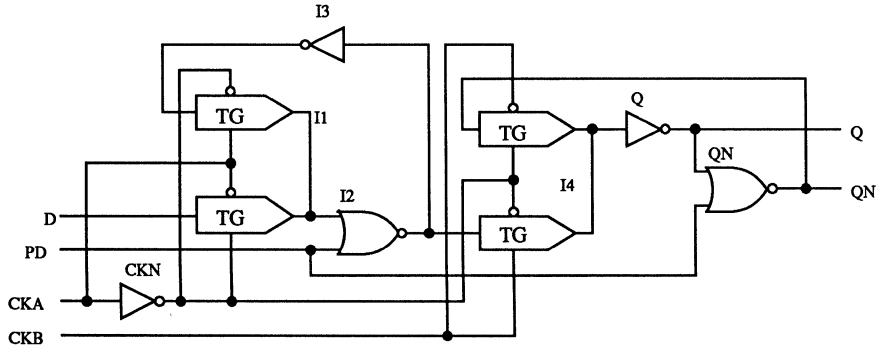
	D	CKA	CKB	PD
Area	0.019pF	0.057pF	0.028pF	0.057pF
Perf	0.020pF	0.065pF	0.032pF	0.208pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D ↓	0.87ns	0.75ns	CK ↑	Q ↓	2.18ns/pF	1.73ns	0.62ns/pF	1.13ns
D ↑	0.81ns	0.64ns	CK ↑	Q ↑	3.24ns/pF	0.92ns	0.70ns/pF	0.79ns
			CK ↑	QN ↓	7.93ns/pF	1.07ns	1.73ns/pF	0.92ns
			CK ↑	QN ↑	8.85ns/pF	2.00ns	2.01ns/pF	1.39ns
			PD ↑	Q ↑	6.01ns/pF	1.44ns	1.40ns/pF	0.78ns
			PD ↑	QN ↓	2.31ns/pF	1.10ns	0.62ns/pF	0.32ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3CX

Positive edge triggered, positive asynchronous clear, positive asynchronous preset.

Grids 21, **Transistors** 28

Inputs
D,CKA,CKB,PDA,PDB,CD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	CK	PD	CD	Q	QN	Q	QN
X	X	X	1	X	X	0	1
X	X	1	0	X	X	1	0
0	↑	0	X	X	X	0	1
1	↑	X	0	X	X	1	0

X = Don't care

Capacitances

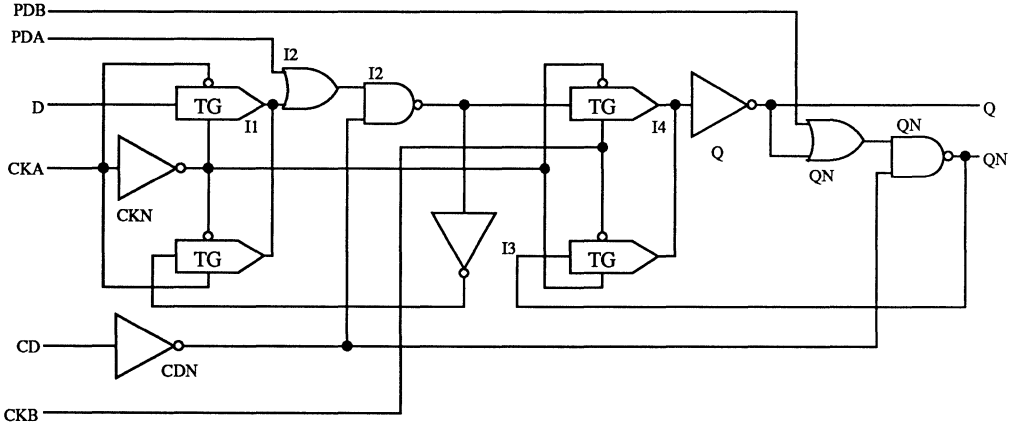
	D	CKA	CKB	PDA	PDB	CD
Area	0.019pF	0.057pF	0.029pF	0.027pF	0.027pF	0.027pF
Perf	0.020pF	0.065pF	0.033pF	0.102pF	0.102pF	0.102pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D ↓	0.92ns	0.81ns	CD ↑	Q ↓	7.93ns/pF	1.59ns	1.77ns/pF	1.02ns
D ↑	1.04ns	0.81ns	CD ↑	QN ↑	3.24ns/pF	1.10ns	0.70ns/pF	0.56ns
			CK ↑	Q ↓	2.18ns/pF	1.73ns	0.62ns/pF	1.13ns
			CK ↑	Q ↑	3.24ns/pF	1.10ns	0.70ns/pF	0.85ns
			CK ↑	QN ↓	9.38ns/pF	1.40ns	2.10ns/pF	1.11ns
			CK ↑	QN ↑	8.72ns/pF	2.16ns	2.01ns/pF	1.39ns
			PD ↑	Q ↑	8.26ns/pF	1.64ns	2.05ns/pF	0.84ns
			PD ↑	QN ↓	4.03ns/pF	1.26ns	1.07ns/pF	0.45ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3DX

Positive edge triggered, positive asynchronous clear.

Grids 17, **Transistors** 24

Inputs
D,CKA,CKB,CD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CD	Q	QN	Q	QN
X	X	1	X	X	0	1
0	↑	X	X	X	0	1
1	↑	0	X	X	1	0

X = Don't care

Capacitances

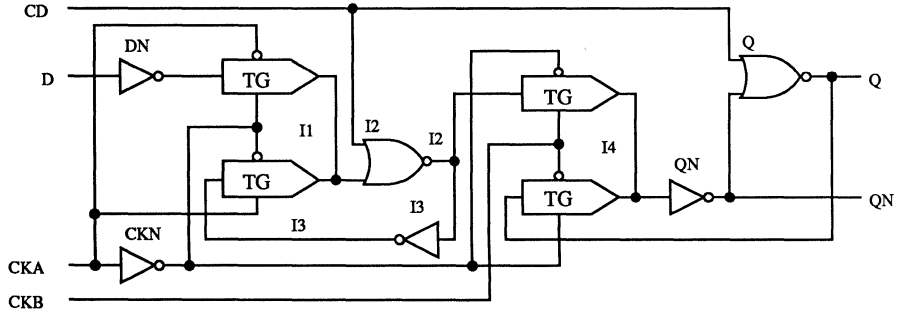
	D	CKA	CKB	CD
Area	0.027pF	0.061pF	0.028pF	0.057pF
Perf	0.102pF	0.070pF	0.032pF	0.208pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	0.98ns	0.69ns	CD ↑	Q ↓	2.31ns/pF	1.10ns	0.58ns/pF	0.35ns
D ↑	1.39ns	0.87ns	CD ↑	QN ↑	6.01ns/pF	1.44ns	1.40ns/pF	0.78ns
			CK ↑	Q ↓	7.93ns/pF	1.07ns	1.73ns/pF	0.92ns
			CK ↑	Q ↑	8.85ns/pF	2.00ns	2.01ns/pF	1.39ns
			CK ↑	QN ↓	2.18ns/pF	1.73ns	0.62ns/pF	1.13ns
			CK ↑	QN ↑	3.24ns/pF	0.92ns	0.70ns/pF	0.79ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3EX

Positive edge triggered, negative asynchronous clear.

Grids 16, **Transistors** 22

Inputs
D,CKA,CKB,CDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CDN	Q	QN	Q	QN
X	X	0	X	X	0	1
0	↑	X	X	X	0	1
1	↑	1	X	X	1	0

X = Don't care

Capacitances

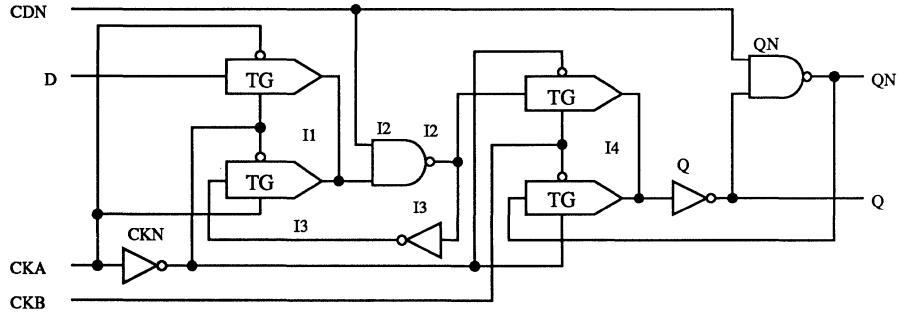
	D	CKA	CKB	CDN
Area	0.019pF	0.057pF	0.029pF	0.059pF
Perf	0.020pF	0.065pF	0.033pF	0.209pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	0.64ns	0.64ns	CDN ↓	Q ↓	7.99ns/pF	0.93ns	1.77ns/pF	0.73ns
D ↑	1.04ns	0.81ns	CDN ↓	QN ↑	3.24ns/pF	0.52ns	0.70ns/pF	0.21ns
			CK ↑	Q ↓	2.05ns/pF	1.49ns	0.58ns/pF	1.10ns
			CK ↑	Q ↑	3.24ns/pF	1.16ns	0.70ns/pF	0.85ns
			CK ↑	QN ↓	9.38ns/pF	1.40ns	2.14ns/pF	1.02ns
			CK ↑	QN ↑	5.68ns/pF	1.68ns	1.40ns/pF	1.24ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3FX

Positive edge triggered, negative asynchronous clear, positive asynchronous preset.

Grids 19, **Transistors** 26

Inputs
D,CKA,CKB,PDA,PDB,CDN

Outputs
Q,QN

Capacitances

	D	CKA	CKB	PDA	PDB	CDN
Area	0.019pF	0.057pF	0.029pF	0.027pF	0.027pF	0.057pF
Perf	0.020pF	0.065pF	0.033pF	0.102pF	0.103pF	0.207pF

Truth Table

INPUTS				OUTPUTS OLD		OUTPUTS NEW	
D	CK	PD	CDN	Q	QN	Q	QN
X	X	X	0	X	X	0	1
X	X	1	1	X	X	1	0
0	↑	0	X	X	X	0	1
1	↑	X	1	X	X	1	0

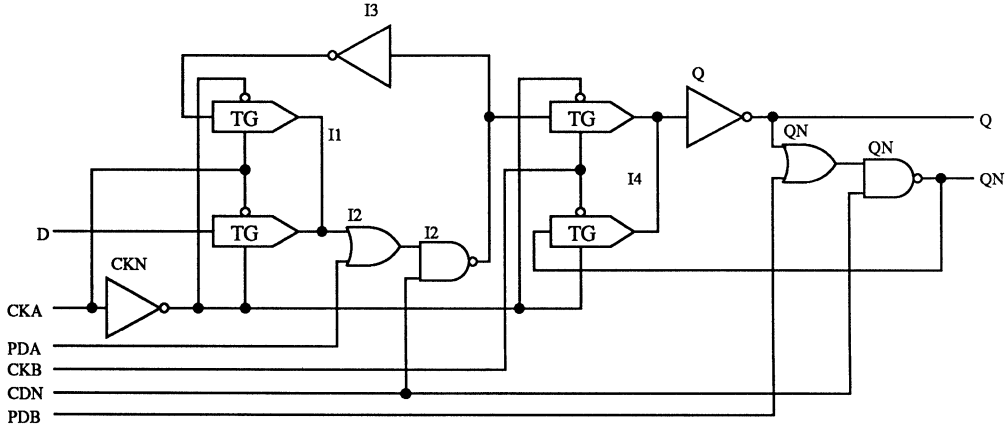
X = Don't care

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
D ↓	0.92ns	0.81ns	CDN ↓	Q ↓	7.93ns/pF	1.07ns	1.77ns/pF	0.78ns
D ↑	1.04ns	0.81ns	CDN ↓	QN ↑	3.24ns/pF	0.58ns	0.70ns/pF	0.27ns
			CK ↑	Q ↓	2.25ns/pF	1.70ns	0.62ns/pF	1.13ns
			CK ↑	Q ↑	3.30ns/pF	1.07ns	0.70ns/pF	0.85ns
			CK ↑	QN ↓	9.38ns/pF	1.40ns	2.14ns/pF	1.08ns
			CK ↑	QN ↑	8.79ns/pF	2.14ns	2.01ns/pF	1.44ns
			PD ↑	Q ↑	8.32ns/pF	1.62ns	2.05ns/pF	0.90ns
			PD ↑	QN ↓	4.03ns/pF	1.26ns	1.07ns/pF	0.45ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3GX

Positive edge triggered, negative asynchronous preset.

Grids 17, **Transistors** 24

Inputs
D,CKA,CKB,PDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PDN	Q	QN	Q	QN
X	X	0	X	X	1	0
0	↑	1	X	X	0	1
1	↑	X	X	X	1	0

X = Don't care

Capacitances

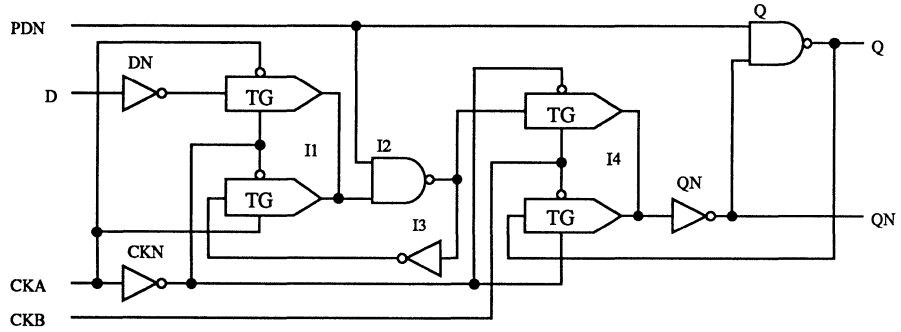
	D	CKA	CKB	PDN
Area	0.027pF	0.060pF	0.029pF	0.059pF
Perf	0.102pF	0.070pF	0.033pF	0.209pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D ↓	1.04ns	0.81ns	CK ↑	Q ↓	9.38ns/pF	1.40ns	2.14ns/pF	1.02ns
D ↑	1.16ns	0.75ns	CK ↑	Q ↑	5.68ns/pF	1.68ns	1.40ns/pF	1.24ns
			CK ↑	QN ↓	2.05ns/pF	1.49ns	0.58ns/pF	1.10ns
			CK ↑	QN ↑	3.24ns/pF	1.16ns	0.70ns/pF	0.85ns
			PDN ↓	Q ↑	3.24ns/pF	0.52ns	0.70ns/pF	0.21ns
			PDN ↓	QN ↓	7.99ns/pF	0.93ns	1.77ns/pF	0.73ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3IX

Positive edge triggered, positive synchronous clear.

Grids 18, **Transistors** 24

Inputs
D,CKA,CKB,CD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CD	Q	QN	Q	QN
X	↑	1	X	X	0	1
0	↑	X	X	X	0	1
1	↑	0	X	X	1	0

X = Don't care

Capacitances

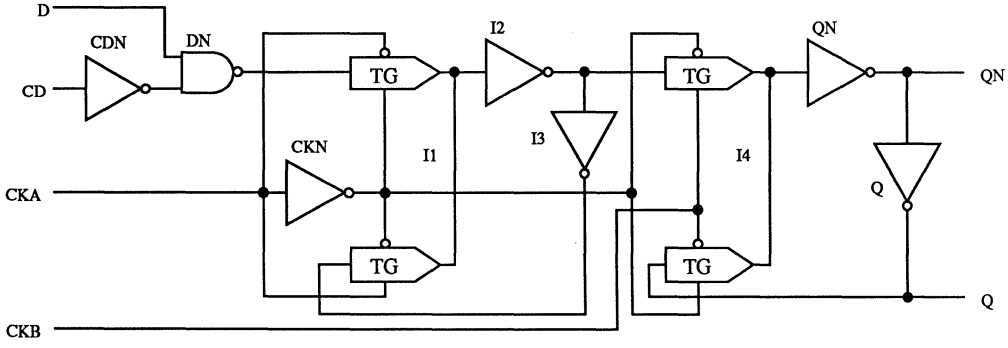
	D	CKA	CKB	CD
Area	0.027pF	0.057pF	0.028pF	0.027pF
Perf	0.102pF	0.065pF	0.033pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CD ↓	1.27ns	0.92ns	CK ↑	Q ↓	7.93ns/pF	1.13ns	1.77ns/pF	0.90ns
CD ↑	1.33ns	0.92ns	CK ↑	Q ↑	5.81ns/pF	1.63ns	1.40ns/pF	1.24ns
D ↓	1.04ns	0.69ns	CK ↑	QN ↓	2.05ns/pF	1.54ns	0.58ns/pF	1.10ns
D ↑	1.44ns	0.87ns	CK ↑	QN ↑	3.24ns/pF	0.98ns	0.66ns/pF	0.88ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3JX

Positive edge triggered, positive synchronous preset.

Grids 16, **Transistors** 22

Inputs
D,CKA,CKB,PD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PD	Q	QN	Q	QN
X	↑	1	X	X	1	0
0	↑	0	X	X	0	1
1	↑	X	X	X	1	0

X = Don't care

Capacitances

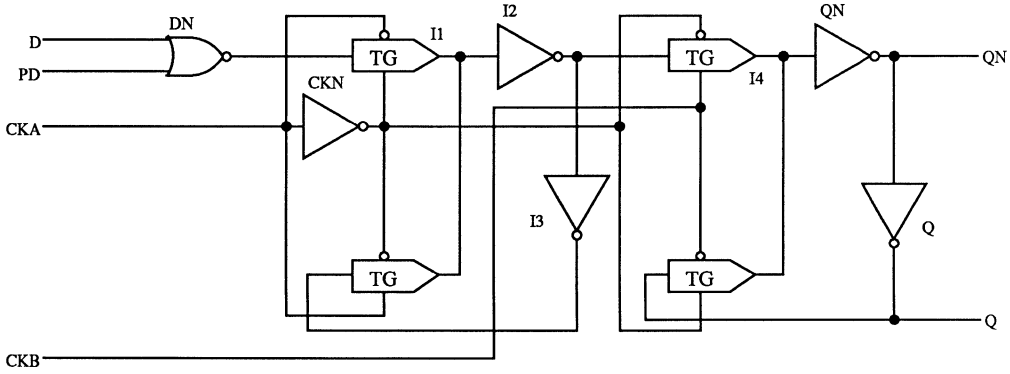
	D	CKA	CKB	PD
Area	0.027pF	0.058pF	0.028pF	0.027pF
Perf	0.102pF	0.066pF	0.033pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.33ns	0.92ns	CK ↑	Q ↓	7.93ns/pF	1.13ns	1.77ns/pF	0.90ns
D ↑	1.16ns	0.75ns	CK ↑	Q ↑	5.75ns/pF	1.72ns	1.40ns/pF	1.24ns
PD ↓	1.33ns	0.92ns	CK ↑	QN ↓	2.05ns/pF	1.54ns	0.58ns/pF	1.10ns
PD ↑	1.16ns	0.75ns	CK ↑	QN ↑	3.24ns/pF	0.98ns	0.66ns/pF	0.88ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3KX

Positive edge triggered, negative asynchronous clear, negative asynchronous preset.

Grids 22, **Transistors** 30

Inputs
D,CKA,CKB,PDNA,PDNB,CDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	CK	PDN	CDN	Q	QN	Q	QN
X	X	X	0	X	X	0	1
X	X	0	1	X	X	1	0
0	↑	1	X	X	X	0	1
1	↑	X	1	X	X	1	0

X = Don't care

Capacitances

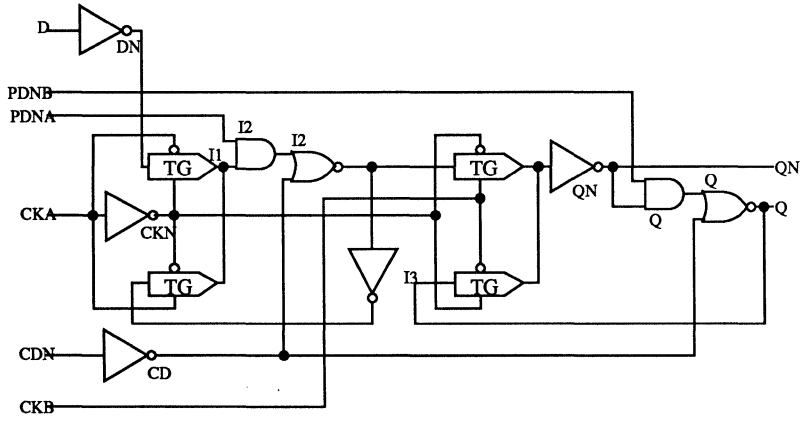
	D	CKA	CKB	PDNA	PDNB	CDN
Area	0.027pF	0.057pF	0.028pF	0.027pF	0.027pF	0.027pF
Perf	0.102pF	0.065pF	0.032pF	0.102pF	0.102pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.16ns	0.87ns	CDN ↓	Q ↓	2.05ns/pF	0.91ns	0.53ns/pF	0.54ns
D ↑	1.44ns	0.92ns	CDN ↓	QN ↑	5.75ns/pF	1.26ns	1.36ns/pF	0.97ns
			CK ↑	Q ↓	9.38ns/pF	1.40ns	2.10ns/pF	1.11ns
			CK ↑	Q ↑	8.79ns/pF	2.20ns	2.05ns/pF	1.36ns
			CK ↑	QN ↓	2.25ns/pF	1.76ns	0.62ns/pF	1.13ns
			CK ↑	QN ↑	3.24ns/pF	1.16ns	0.70ns/pF	0.85ns
			PDN ↓	Q ↑	6.47ns/pF	0.81ns	1.36ns/pF	0.40ns
			PDN ↓	QN ↓	12.75ns/pF	1.46ns	2.79ns/pF	0.86ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3LX

Positive edge triggered, negative synchronous preset.

Grids 18, **Transistors** 24

Inputs
D,CKA,CKB,PDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PDN	Q	QN	Q	QN
X	↑	0	X	X	1	0
0	↑	1	X	X	0	1
1	↑	X	X	X	1	0

X = Don't care

Capacitances

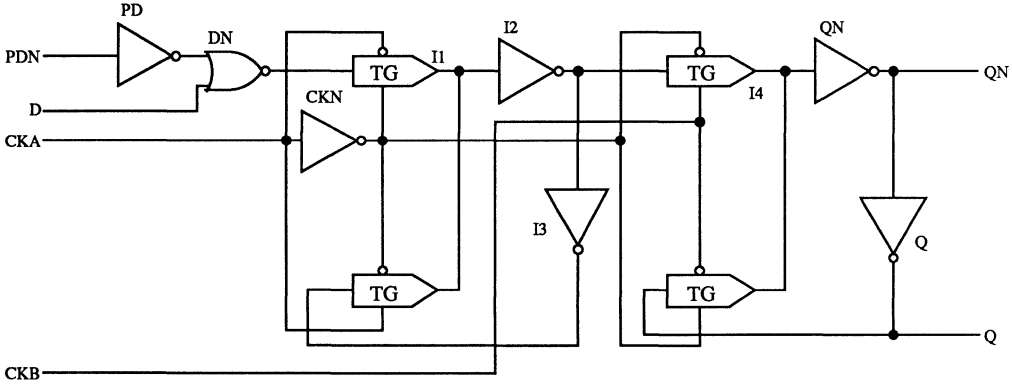
	D	CKA	CKB	PDN
Area	0.027pF	0.057pF	0.029pF	0.027pF
Perf	0.102pF	0.065pF	0.033pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.39ns	0.87ns	CK ↑	Q ↓	7.93ns/pF	1.13ns	1.77ns/pF	0.90ns
D ↑	1.21ns	0.75ns	CK ↑	Q ↑	5.81ns/pF	1.63ns	1.40ns/pF	1.24ns
PDN ↓	1.10ns	0.87ns	CK ↑	QN ↓	2.05ns/pF	1.54ns	0.58ns/pF	1.10ns
PDN ↑	1.73ns	1.10ns	CK ↑	QN ↑	3.24ns/pF	0.98ns	0.66ns/pF	0.88ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



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Static D-Type Flip-Flop

FD1S3MX

Positive edge triggered, negative synchronous clear.

Grids 15, **Transistors** 22

Inputs
D,CKA,CKB,CDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CDN	Q	QN	Q	QN
X	↑	0	X	X	0	1
0	↑	X	X	X	0	1
1	↑	1	X	X	1	0

X = Don't care

Capacitances

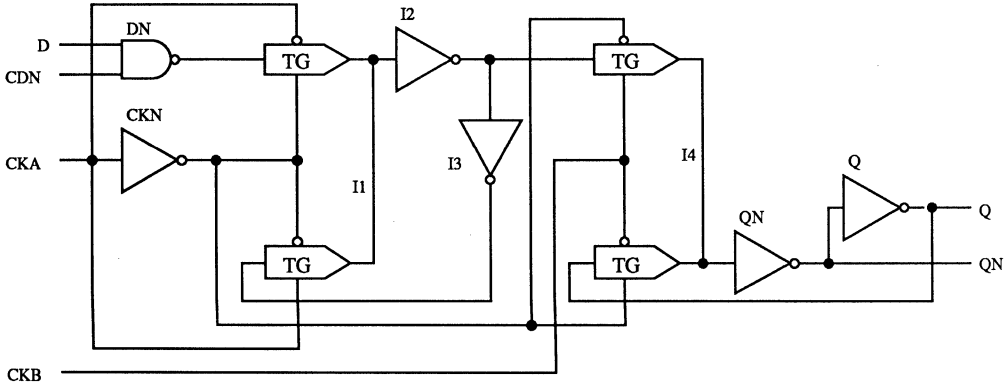
	D	CKA	CKB	CDN
Area	0.027pF	0.058pF	0.028pF	0.027pF
Perf	0.102pF	0.066pF	0.032pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	0.98ns	0.75ns	CK ↑	Q ↓	7.93ns/pF	1.07ns	1.73ns/pF	0.92ns
CDN ↑	1.44ns	0.92ns	CK ↑	Q ↑	5.75ns/pF	1.60ns	1.44ns/pF	1.16ns
D ↓	0.98ns	0.75ns	CK ↑	QN ↓	2.05ns/pF	1.49ns	0.58ns/pF	1.10ns
D ↑	1.44ns	0.92ns	CK ↑	QN ↑	3.24ns/pF	0.92ns	0.70ns/pF	0.79ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3LX

Positive edge triggered, negative synchronous preset.

Grids 18, **Transistors** 24

Inputs
D,CKA,CKB,PDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PDN	Q	QN	Q	QN
X	↑	0	X	X	1	0
0	↑	1	X	X	0	1
1	↑	X	X	X	1	0

X = Don't care

Capacitances

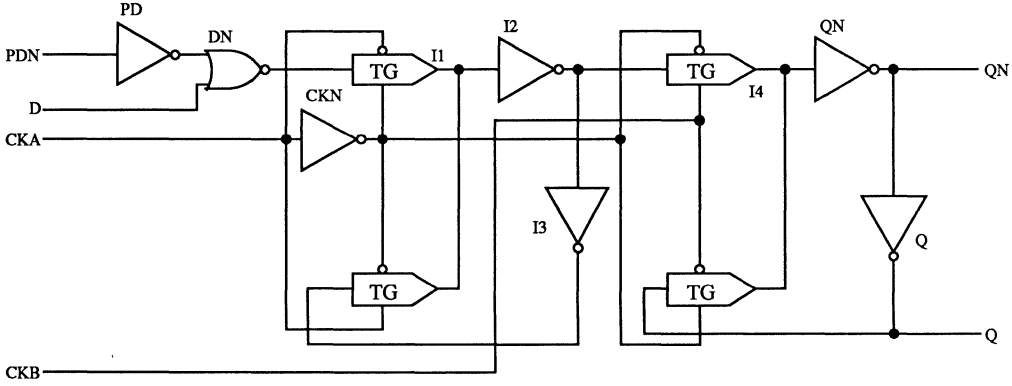
	D	CKA	CKB	PDN
Area	0.027pF	0.057pF	0.029pF	0.027pF
Perf	0.102pF	0.065pF	0.033pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.39ns	0.87ns	CK ↑	Q ↓	7.93ns/pF	1.13ns	1.77ns/pF	0.90ns
D ↑	1.21ns	0.75ns	CK ↑	Q ↑	5.81ns/pF	1.63ns	1.40ns/pF	1.24ns
PDN ↓	1.10ns	0.87ns	CK ↑	QN ↓	2.05ns/pF	1.54ns	0.58ns/pF	1.10ns
PDN ↑	1.73ns	1.10ns	CK ↑	QN ↑	3.24ns/pF	0.98ns	0.66ns/pF	0.88ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3MX

Positive edge triggered, negative synchronous clear.

Grids 15, **Transistors** 22

Inputs
D,CKA,CKB,CDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CDN	Q	QN	Q	QN
X	↑	0	X	X	0	1
0	↑	X	X	X	0	1
1	↑	1	X	X	1	0

X = Don't care

Capacitances

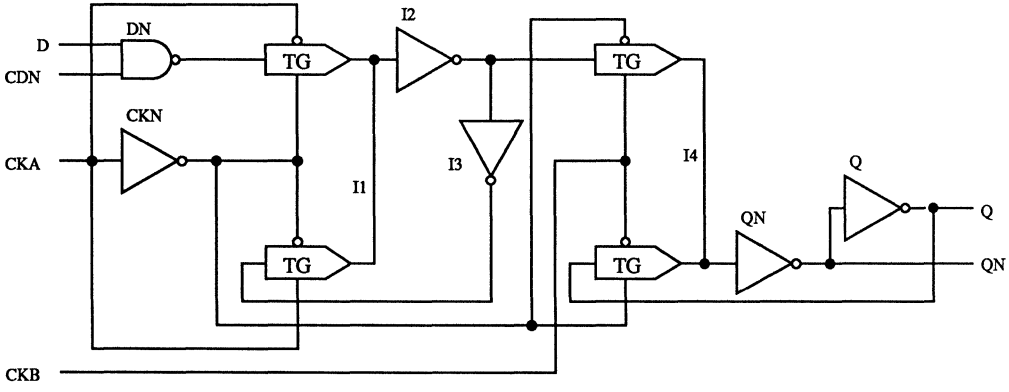
	D	CKA	CKB	CDN
Area	0.027pF	0.058pF	0.028pF	0.027pF
Perf	0.102pF	0.066pF	0.032pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	0.98ns	0.75ns	CK ↑	Q ↓	7.93ns/pF	1.07ns	1.73ns/pF	0.92ns
CDN ↑	1.44ns	0.92ns	CK ↑	Q ↑	5.75ns/pF	1.60ns	1.44ns/pF	1.16ns
D ↓	0.98ns	0.75ns	CK ↑	QN ↓	2.05ns/pF	1.49ns	0.58ns/pF	1.10ns
D ↑	1.44ns	0.92ns	CK ↑	QN ↑	3.24ns/pF	0.92ns	0.70ns/pF	0.79ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3NX

Positive edge triggered, positive asynchronous clear, negative asynchronous preset.

Grids 20, **Transistors** 28

Inputs
D,CKA,CKB,PDNA,PDNB,CD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	CK	PDN	CD	Q	QN	Q	QN
X	X	X	1	X	X	0	1
X	X	0	0	X	X	1	0
0	↑	1	X	X	X	0	1
1	↑	X	0	X	X	1	0

X = Don't care

Capacitances

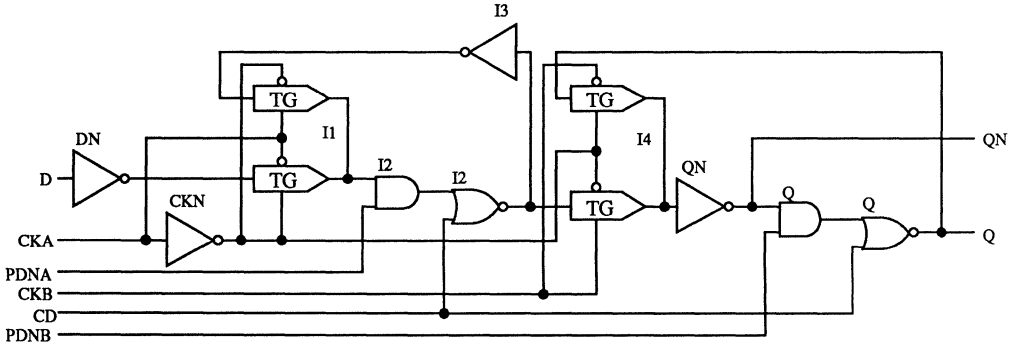
	D	CKA	CKB	PDNA	PDNB	CD
Area	0.027pF	0.060pF	0.028pF	0.027pF	0.027pF	0.057pF
Perf	0.102pF	0.071pF	0.032pF	0.102pF	0.103pF	0.207pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D ↓	1.10ns	0.87ns	CD ↑	Q ↓	2.25ns/pF	1.18ns	0.58ns/pF	0.40ns
D ↑	1.44ns	0.92ns	CD ↑	QN ↑	6.01ns/pF	1.50ns	1.40ns/pF	0.83ns
			CK ↑	Q ↓	9.31ns/pF	1.48ns	2.10ns/pF	1.16ns
			CK ↑	Q ↑	8.79ns/pF	2.20ns	2.05ns/pF	1.42ns
			CK ↑	QN ↓	2.18ns/pF	1.84ns	0.62ns/pF	1.13ns
			CK ↑	QN ↑	3.24ns/pF	1.16ns	0.70ns/pF	0.85ns
			PDN ↓	Q ↑	6.47ns/pF	0.81ns	1.36ns/pF	0.45ns
			PDN ↓	QN ↓	12.75ns/pF	1.46ns	2.75ns/pF	1.00ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S3OX

Positive edge triggered, positive synchronous clear, positive synchronous preset.

Grids 19, **Transistors** 26

Inputs
D,CKA,CKB,PD,CD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	CK	PD	CD	Q	QN	Q	QN
X	↑	X	1	X	X	0	1
X	↑	1	0	X	X	1	0
0	↑	0	X	X	X	0	1
1	↑	X	0	X	X	1	0

X = Don't care

Capacitances

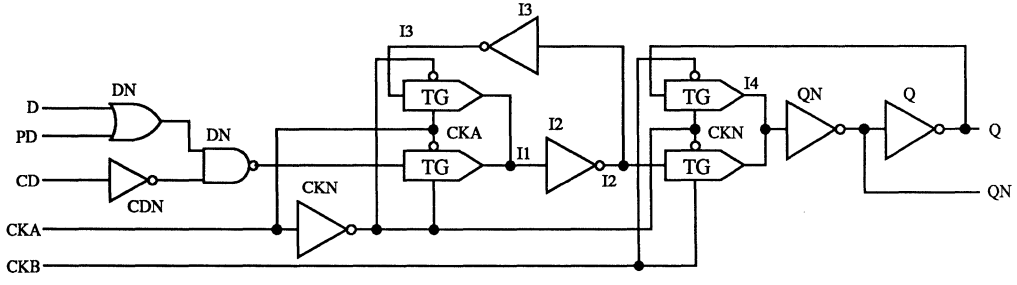
	D	CKA	CKB	PD	CD
Area	0.027pF	0.057pF	0.028pF	0.027pF	0.027pF
Perf	0.102pF	0.065pF	0.033pF	0.102pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CD ↓	1.33ns	0.98ns	CK ↑	Q ↓	7.93ns/pF	1.13ns	1.77ns/pF	0.90ns
CD ↑	1.39ns	0.92ns	CK ↑	Q ↑	5.81ns/pF	1.63ns	1.40ns/pF	1.24ns
D ↓	1.44ns	0.92ns	CK ↑	QN ↓	2.05ns/pF	1.54ns	0.58ns/pF	1.10ns
D ↑	1.44ns	0.87ns	CK ↑	QN ↑	3.24ns/pF	0.98ns	0.66ns/pF	0.88ns
PD ↓	1.44ns	0.92ns						
PD ↑	1.44ns	0.87ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop FD1S5A

Negative level sense.

Grids 9, **Transistors** 10

Inputs
D,CK

Outputs
Q,QN

Truth Table

INPUTS		OUTPUTS			
		OLD		NEW	
D	CK	Q	QN	Q	QN
X	1	0	1	0	1
X	1	1	0	1	0
0	0	X	X	0	1
1	0	X	X	1	0

X = Don't care

Capacitances

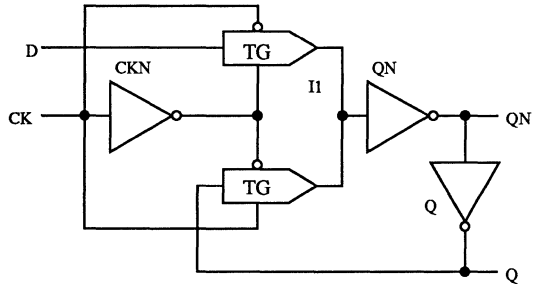
	D	CK
Area	0.019pF	0.057pF
Perf	0.020pF	0.065pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CK ↓	Q ↓	7.93ns/pF	1.02ns	1.73ns/pF	0.92ns
CK ↓	Q ↑	5.88ns/pF	1.09ns	1.44ns/pF	0.98ns
CK ↓	QN ↓	2.11ns/pF	0.94ns	0.62ns/pF	0.84ns
CK ↓	QN ↑	3.24ns/pF	0.81ns	0.70ns/pF	0.79ns
D ↓	Q ↓	7.93ns/pF	0.73ns	1.73ns/pF	0.69ns
D ↓	QN ↑	3.24ns/pF	0.52ns	0.66ns/pF	0.59ns
D ↑	Q ↑	6.14ns/pF	1.51ns	1.48ns/pF	0.84ns
D ↑	QN ↓	2.44ns/pF	1.28ns	0.66ns/pF	0.70ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S5B

Negative level sense, positive asynchronous preset.

Grids 9, **Transistors** 12

Inputs
D,CK,PD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PD	Q	QN	Q	QN
X	1	0	0	1	0	1
X	1	X	1	0	1	0
X	X	1	X	X	1	0
0	0	0	X	X	0	1
1	0	X	X	X	1	0

X = Don't care

Capacitances

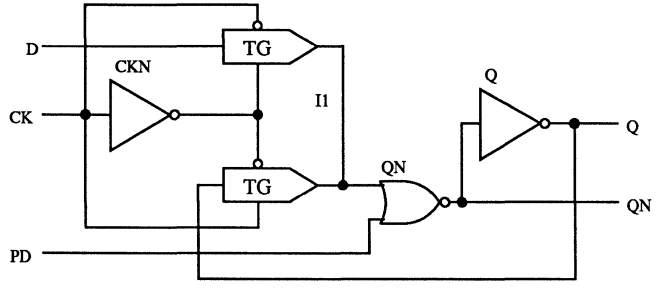
	D	CK	PD
Area	0.019pF	0.057pF	0.027pF
Perf	0.020pF	0.065pF	0.102pF

Delay Information

From	To	Propagation Delay			
		Area		Performance	
Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CK ↓	Q ↓	12.75ns/pF	1.11ns	2.71ns/pF	1.02ns
CK ↓	Q ↑	5.88ns/pF	1.03ns	1.44ns/pF	0.98ns
CK ↓	QN ↓	2.11ns/pF	0.94ns	0.58ns/pF	0.92ns
CK ↓	QN ↑	6.47ns/pF	0.92ns	1.36ns/pF	0.86ns
D ↓	Q ↓	12.75ns/pF	0.77ns	2.71ns/pF	0.79ns
D ↓	QN ↑	6.41ns/pF	0.60ns	1.36ns/pF	0.63ns
D ↑	Q ↑	6.14ns/pF	1.45ns	1.48ns/pF	0.84ns
D ↑	QN ↓	2.44ns/pF	1.28ns	0.62ns/pF	0.78ns
PD ↑	Q ↑	6.01ns/pF	1.39ns	1.44ns/pF	0.52ns
PD ↑	QN ↓	2.31ns/pF	0.98ns	0.58ns/pF	0.35ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S5D

Negative level sense, positive asynchronous clear.

Grids 10, **Transistors** 14

Inputs
D,CK,CD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CD	Q	QN	Q	QN
X	1	X	0	1	0	1
X	1	0	1	0	1	0
X	X	1	X	X	0	1
0	0	X	X	X	0	1
1	0	0	X	X	1	0

X = Don't care

Capacitances

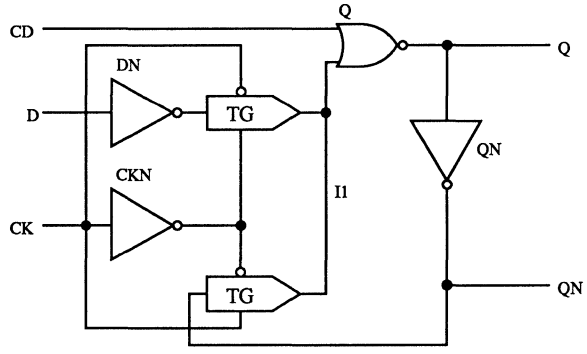
	D	CK	CD
Area	0.027pF	0.060pF	0.027pF
Perf	0.102pF	0.070pF	0.102pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CD ↑	Q ↓	2.31ns/pF	0.98ns	0.58ns/pF	0.35ns
CD ↑	QN ↑	6.01ns/pF	1.39ns	1.44ns/pF	0.52ns
CK ↓	Q ↓	1.98ns/pF	1.16ns	0.58ns/pF	0.92ns
CK ↓	Q ↑	6.47ns/pF	0.92ns	1.36ns/pF	0.86ns
CK ↓	QN ↓	12.75ns/pF	1.11ns	2.71ns/pF	1.02ns
CK ↓	QN ↑	5.75ns/pF	1.26ns	1.40ns/pF	1.07ns
D ↓	Q ↓	2.05ns/pF	1.02ns	0.58ns/pF	0.75ns
D ↓	QN ↑	5.75ns/pF	1.20ns	1.40ns/pF	0.89ns
D ↑	Q ↑	6.41ns/pF	1.12ns	1.36ns/pF	0.74ns
D ↑	QN ↓	12.75ns/pF	1.29ns	2.75ns/pF	0.83ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



7

Static D-Type Flip-Flop

FD1S5E

Negative level sense, negative asynchronous clear.

Grids 9, **Transistors** 12

Inputs
D,CK,CDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	CDN	Q	QN	Q	QN
X	1	X	0	1	0	1
X	1	1	1	0	1	0
X	X	0	X	X	0	1
0	0	X	X	X	0	1
1	0	1	X	X	1	0

X = Don't care

Capacitances

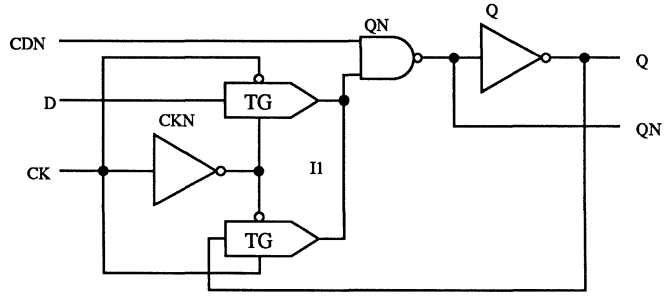
	D	CK	CDN
Area	0.019pF	0.057pF	0.027pF
Perf	0.020pF	0.065pF	0.102pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	Q ↓	7.93ns/pF	0.73ns	1.77ns/pF	0.38ns
CDN ↓	QN ↑	3.24ns/pF	0.35ns	0.66ns/pF	0.24ns
CK ↓	Q ↓	7.93ns/pF	1.02ns	1.73ns/pF	0.92ns
CK ↓	Q ↑	8.32ns/pF	1.04ns	2.05ns/pF	1.02ns
CK ↓	QN ↓	4.03ns/pF	0.92ns	1.07ns/pF	0.92ns
CK ↓	QN ↑	3.24ns/pF	0.87ns	0.70ns/pF	0.79ns
D ↓	Q ↓	7.99ns/pF	0.64ns	1.73ns/pF	0.69ns
D ↓	QN ↑	3.24ns/pF	0.52ns	0.66ns/pF	0.59ns
D ↑	Q ↑	8.32ns/pF	1.50ns	2.05ns/pF	0.90ns
D ↑	QN ↓	4.10ns/pF	1.30ns	1.07ns/pF	0.80ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD1S5F

Negative level sense, negative asynchronous clear, positive asynchronous preset.

Grids 11, **Transistors** 14

Inputs
D,CK,PD,CDN

Outputs
Q,QN

Capacitances

	D	CK	PD	CDN
Area	0.019pF	0.057pF	0.027pF	0.027pF
Perf	0.020pF	0.065pF	0.102pF	0.102pF

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	CK	PD	CDN	Q	QN	Q	QN
X	1	0	X	0	1	0	1
X	1	X	1	1	0	1	0
X	X	X	0	X	X	0	1
X	X	1	1	X	X	1	0
0	0	0	X	X	X	0	1
1	0	X	1	X	X	1	0

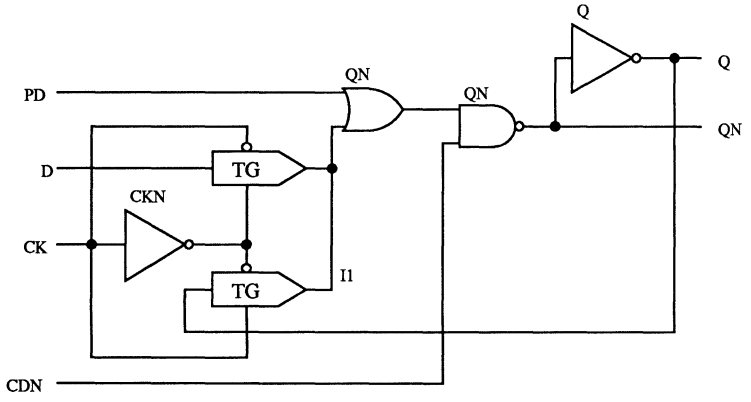
X = Don't care

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	Q ↓	7.93ns/pF	0.78ns	1.77ns/pF	0.38ns
CDN ↓	QN ↑	3.24ns/pF	0.40ns	0.70ns/pF	0.21ns
CK ↓	Q ↓	12.75ns/pF	1.17ns	2.75ns/pF	1.00ns
CK ↓	Q ↑	8.26ns/pF	1.12ns	2.05ns/pF	1.07ns
CK ↓	QN ↓	4.03ns/pF	0.97ns	1.07ns/pF	0.92ns
CK ↓	QN ↑	6.47ns/pF	0.98ns	1.36ns/pF	0.92ns
D ↓	Q ↓	12.75ns/pF	0.83ns	2.75ns/pF	0.77ns
D ↓	QN ↑	6.47ns/pF	0.58ns	1.36ns/pF	0.63ns
D ↑	Q ↑	8.32ns/pF	1.50ns	2.05ns/pF	0.96ns
D ↑	QN ↓	4.16ns/pF	1.27ns	1.07ns/pF	0.80ns
PD ↑	Q ↑	8.32ns/pF	1.39ns	2.05ns/pF	0.61ns
PD ↑	QN ↓	4.03ns/pF	1.03ns	1.07ns/pF	0.40ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



7

Static D-Type Flip-Flop

FD1S5G

Negative level sense, negative asynchronous preset.

Grids 10, **Transistors** 14

Inputs
D,CK,PDN

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	CK	PDN	Q	QN	Q	QN
X	1	1	0	1	0	1
X	1	X	1	0	1	0
X	X	0	X	X	1	0
0	0	1	X	X	0	1
1	0	X	X	X	1	0

X = Don't care

Capacitances

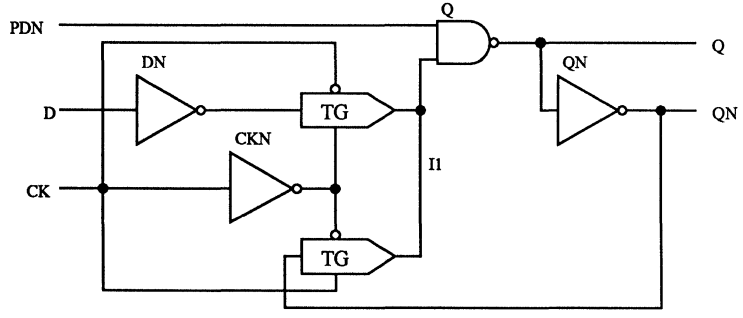
	D	CK	PDN
Area	0.027pF	0.060pF	0.027pF
Perf	0.102pF	0.070pF	0.102pF

Delay Information

From	To	Propagation Delay			
		Area		Performance	
Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CK ↓	Q ↓	3.96ns/pF	1.11ns	1.07ns/pF	0.92ns
CK ↓	Q ↑	3.17ns/pF	0.89ns	0.66ns/pF	0.82ns
CK ↓	QN ↓	7.93ns/pF	1.02ns	1.73ns/pF	0.92ns
CK ↓	QN ↑	8.19ns/pF	1.26ns	2.01ns/pF	1.10ns
D ↓	Q ↓	3.96ns/pF	1.00ns	1.07ns/pF	0.74ns
D ↓	QN ↑	8.26ns/pF	1.12ns	2.01ns/pF	0.92ns
D ↑	Q ↑	3.24ns/pF	0.98ns	0.66ns/pF	0.70ns
D ↑	QN ↓	7.93ns/pF	1.19ns	1.77ns/pF	0.73ns
PDN ↓	Q ↑	3.24ns/pF	0.35ns	0.66ns/pF	0.24ns
PDN ↓	QN ↓	7.93ns/pF	0.73ns	1.77ns/pF	0.38ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop FD2N1A

Master-Slave clocking, negative level sample.

Grids 20, **Transistors** 28

Inputs
D,SPN,MCK,SCK

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS OLD		OUTPUTS NEW	
D	SPN	MCK	SCK	Q	QN	Q	QN
X	1	↓	↑	1	0	1	0
X	1	↓	↑	0	1	0	1
0	0	↓	↑	X	X	0	1
1	0	↓	↑	X	X	1	0

X = Don't care

Capacitances

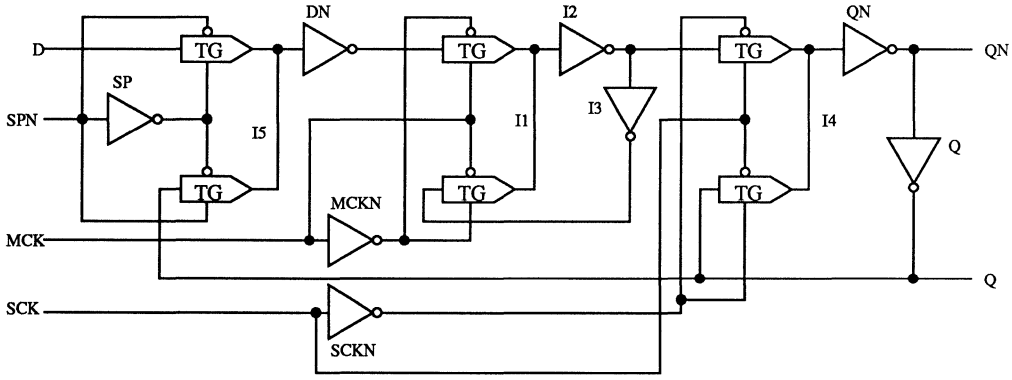
	D	SPN	MCK	SCK
Area	0.019pF	0.057pF	0.058pF	0.057pF
Perf	0.058pF	0.208pF	0.066pF	0.065pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D ↓	1.10ns	0.87ns	SCK ↑	Q ↓	7.99ns/pF	1.05ns	1.73ns/pF	0.92ns
D ↑	1.39ns	0.92ns	SCK ↑	Q ↑	5.75ns/pF	1.43ns	1.40ns/pF	1.12ns
SPN ↓	1.39ns	1.10ns	SCK ↑	QN ↓	2.05ns/pF	1.14ns	0.58ns/pF	0.92ns
SPN ↑	1.56ns	1.16ns	SCK ↑	QN ↑	3.24ns/pF	0.87ns	0.70ns/pF	0.73ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2N1J

Master-Slave clocking, negative level sample, positive synchronous preset.

Grids 23, **Transistors** 34

Inputs
D,SPN,MCK,SCK,PD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D	SPN	MCK	SCK	PD	Q	QN	Q	QN
X	1	↓	↑	0	0	1	0	1
X	1	↓	↑	X	1	0	1	0
X	X	↓	↑	1	X	X	1	0
0	0	↓	↑	0	X	X	0	1
1	0	↓	↑	X	X	X	1	0

X = Don't care

Capacitances

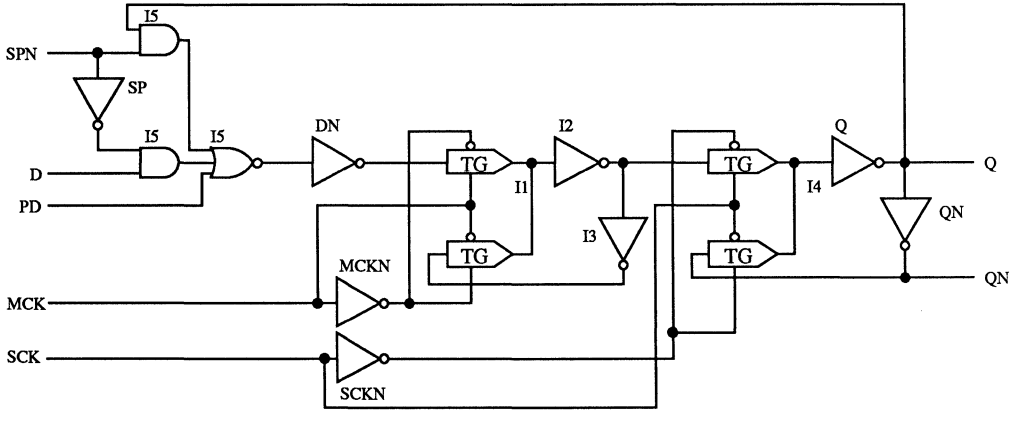
	D	SPN	MCK	SCK	PD
Area	0.029pF	0.057pF	0.057pF	0.057pF	0.027pF
Perf	0.104pF	0.208pF	0.065pF	0.065pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.85ns	1.33ns	SCK ↑	Q ↓	1.98ns/pF	1.51ns	0.58ns/pF	1.10ns
D ↑	1.56ns	1.10ns	SCK ↑	Q ↑	3.24ns/pF	1.16ns	0.66ns/pF	0.93ns
PD ↓	1.85ns	1.33ns	SCK ↑	QN ↓	7.99ns/pF	1.34ns	1.73ns/pF	1.04ns
PD ↑	1.39ns	0.98ns	SCK ↑	QN ↑	5.81ns/pF	1.63ns	1.40ns/pF	1.24ns
SPN ↓	1.79ns	1.27ns						
SPN ↑	2.20ns	1.50ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2N1M

Master-Slave clocking, negative level sample, negative synchronous clear.

Grids 23, **Transistors** 34

Inputs
D,SPN,MCK,SCK,CDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D	SPN	MCK	SCK	CDN	Q	QN	Q	QN
X	1	↓	↑	X	0	1	0	1
X	1	↓	↑	1	1	0	1	0
X	X	↓	↑	0	X	X	0	1
0	0	↓	↑	X	X	X	0	1
1	0	↓	↑	1	X	X	1	0

X = Don't care

Capacitances

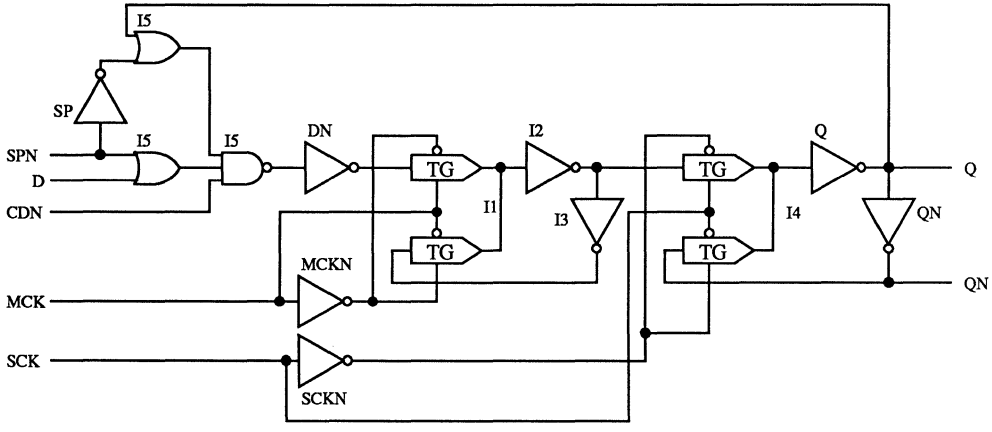
	D	SPN	MCK	SCK	CDN
Area	0.027pF	0.057pF	0.057pF	0.057pF	0.027pF
Perf	0.102pF	0.207pF	0.065pF	0.065pF	0.102pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
CDN ↓	1.16ns	0.92ns	SCK ↑	Q ↓	2.05ns/pF	1.49ns	0.58ns/pF	1.10ns
CDN ↑	1.73ns	1.21ns	SCK ↑	Q ↑	3.24ns/pF	1.16ns	0.66ns/pF	0.93ns
D ↓	1.50ns	1.10ns	SCK ↑	QN ↓	7.99ns/pF	1.34ns	1.73ns/pF	1.04ns
D ↑	1.68ns	1.16ns	SCK ↑	QN ↑	5.81ns/pF	1.63ns	1.40ns/pF	1.24ns
SPN ↓	1.68ns	1.33ns						
SPN ↑	1.85ns	1.33ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2P1A

Master-Slave clocking, positive level sample.

Grids 20, **Transistors** 28

Inputs
D,SP,MCK,SCK

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	SP	MCK	SCK	Q	QN	Q	QN
X	0	↓	↑	0	1	0	1
X	0	↓	↑	1	0	1	0
0	1	↓	↑	X	X	0	1
1	1	↓	↑	X	X	1	0

X = Don't care

Capacitances

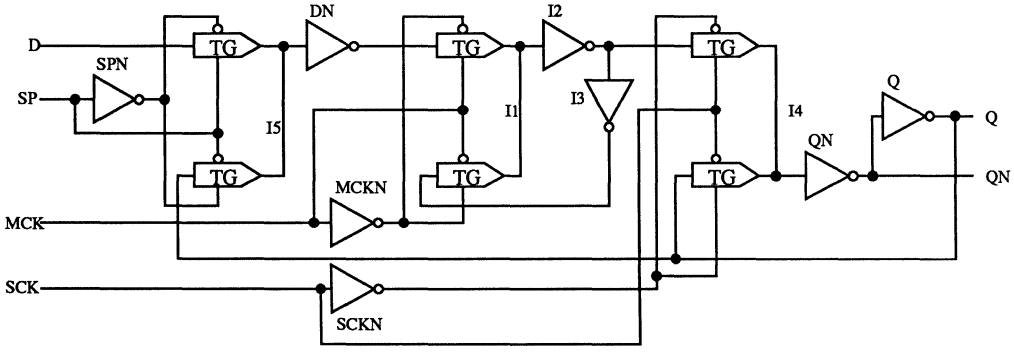
	D	SP	MCK	SCK
Area	0.019pF	0.057pF	0.058pF	0.057pF
Perf	0.058pF	0.207pF	0.066pF	0.065pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.10ns	0.87ns	SCK ↑	Q ↓	7.99ns/pF	1.05ns	1.73ns/pF	0.92ns
D ↑	1.39ns	0.92ns	SCK ↑	Q ↑	5.75ns/pF	1.43ns	1.40ns/pF	1.12ns
SP ↓	1.39ns	1.04ns	SCK ↑	QN ↓	2.05ns/pF	1.14ns	0.58ns/pF	0.92ns
SP ↑	1.62ns	1.16ns	SCK ↑	QN ↑	3.24ns/pF	0.87ns	0.70ns/pF	0.73ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2P1J

Master-Slave clocking, positive level sample, positive synchronous preset.

Grids 23, **Transistors** 34

Inputs
D,SP,MCK,SCK,PD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D	SP	MCK	SCK	PD	Q	QN	Q	QN
X	0	↓	↑	0	0	1	0	1
X	0	↓	↑	X	1	0	1	0
X	X	↓	↑	1	X	X	1	0
0	1	↓	↑	0	X	X	0	1
1	1	↓	↑	X	X	X	1	0

X = Don't care

Capacitances

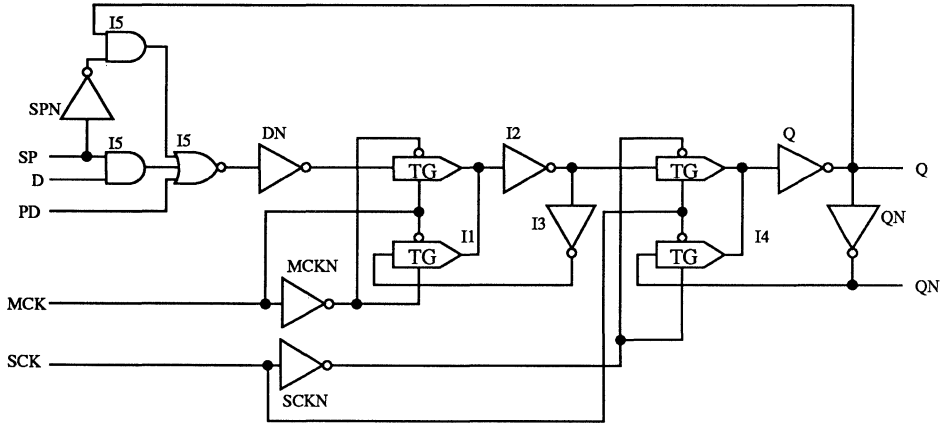
	D	SP	MCK	SCK	PD
Area	0.029pF	0.057pF	0.057pF	0.057pF	0.027pF
Perf	0.104pF	0.207pF	0.065pF	0.065pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.85ns	1.33ns	SCK ↑	Q ↓	1.98ns/pF	1.51ns	0.58ns/pF	1.10ns
D ↑	1.56ns	1.10ns	SCK ↑	Q ↑	3.24ns/pF	1.16ns	0.66ns/pF	0.93ns
PD ↓	1.85ns	1.33ns	SCK ↑	QN ↓	7.99ns/pF	1.34ns	1.73ns/pF	1.04ns
PD ↑	1.39ns	0.98ns	SCK ↑	QN ↑	5.81ns/pF	1.63ns	1.40ns/pF	1.24ns
SP ↓	1.79ns	1.27ns						
SP ↑	2.20ns	1.50ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop FD2P1M

Master-Slave clocking, positive level sample, negative synchronous clear.

Grids 23, **Transistors** 34

Inputs
D,SP,MCK,SCK,CDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D	SP	MCK	SCK	CDN	Q	QN	Q	QN
X	0	↓	↑	X	0	1	0	1
X	0	↓	↑	1	1	0	1	0
X	X	↓	↑	0	X	X	0	1
0	1	↓	↑	X	X	X	0	1
1	1	↓	↑	1	X	X	1	0

X = Don't care

Capacitances

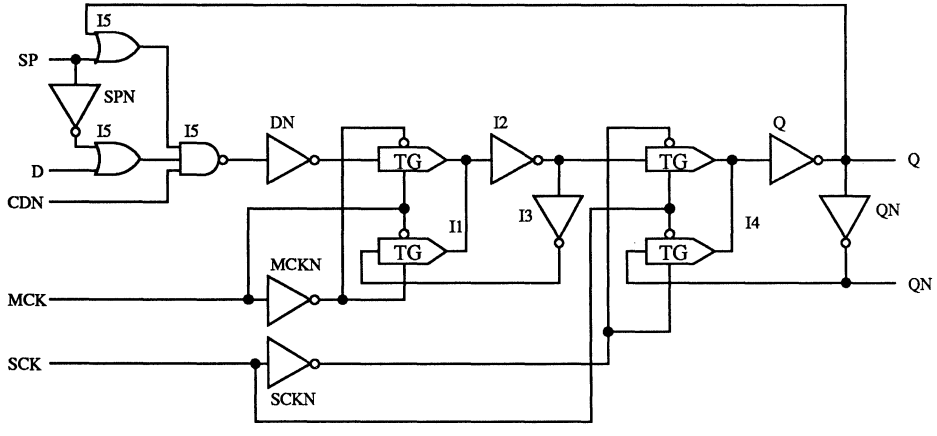
	D	SP	MCK	SCK	CDN
Area	0.027pF	0.057pF	0.057pF	0.057pF	0.027pF
Perf	0.102pF	0.207pF	0.065pF	0.065pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	1.16ns	0.92ns	SCK ↑	Q ↓	2.05ns/pF	1.49ns	0.58ns/pF	1.10ns
CDN ↑	1.73ns	1.21ns	SCK ↑	Q ↑	3.24ns/pF	1.16ns	0.66ns/pF	0.93ns
D ↓	1.50ns	1.10ns	SCK ↑	QN ↓	7.99ns/pF	1.34ns	1.73ns/pF	1.04ns
D ↑	1.68ns	1.16ns	SCK ↑	QN ↑	5.81ns/pF	1.63ns	1.40ns/pF	1.24ns
SP ↓	1.68ns	1.33ns						
SP ↑	1.85ns	1.33ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop FD2S1A

Master-Slave clocking.

Grids 14, **Transistors** 20

Inputs
D,MCK,SCK

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
D	MCK	SCK	Q	QN	Q	QN
0	↓	↑	X	X	0	1
1	↓	↑	X	X	1	0

X = Don't care

Capacitances

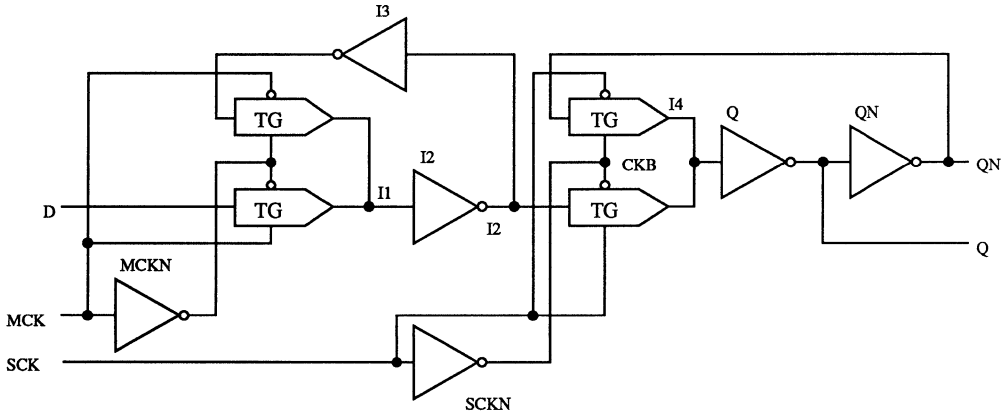
	D	MCK	SCK
Area	0.018pF	0.056pF	0.056pF
Perf	0.020pF	0.064pF	0.065pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	0.58ns	0.64ns	SCK ↑	Q ↓	1.98ns/pF	1.22ns	0.58ns/pF	0.92ns
D ↑	0.75ns	0.64ns	SCK ↑	Q ↑	3.24ns/pF	0.87ns	0.70ns/pF	0.73ns
			SCK ↑	QN ↓	7.99ns/pF	0.99ns	1.73ns/pF	0.87ns
			SCK ↑	QN ↑	5.75ns/pF	1.37ns	1.40ns/pF	1.07ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



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Static D-Type Flip-Flop

FD2S1B

Master-Slave clocking, positive asynchronous preset.

Grids 17, **Transistors** 24

Inputs
D,MCK,SCK,PD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	MCK	SCK	PD	Q	QN	Q	QN
X	X	X	1	X	X	1	0
0	↓	↑	0	X	X	0	1
1	↓	↑	X	X	X	1	0

X = Don't care

Capacitances

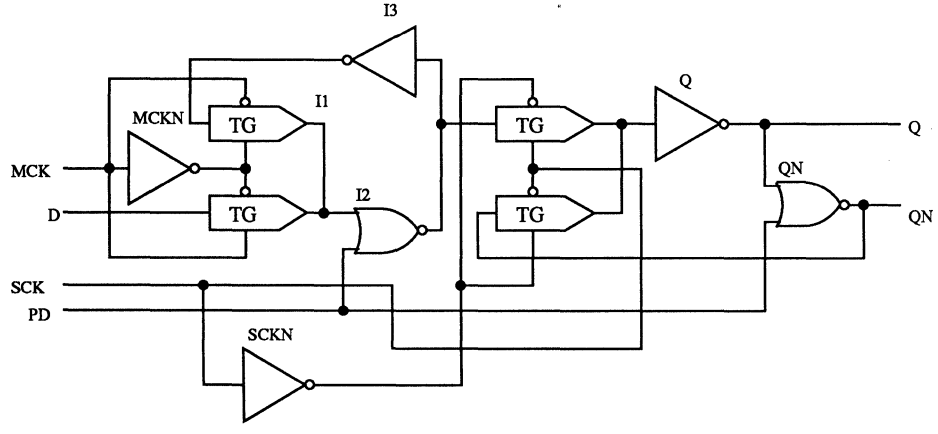
	D	MCK	SCK	PD
Area	0.019pF	0.056pF	0.059pF	0.057pF
Perf	0.020pF	0.065pF	0.068pF	0.207pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	0.87ns	0.81ns	PD ↑	Q ↑	6.01ns/pF	1.44ns	1.40ns/pF	0.78ns
D ↑	0.87ns	0.69ns	PD ↑	QN ↓	2.25ns/pF	1.12ns	0.58ns/pF	0.35ns
			SCK ↑	Q ↓	2.11ns/pF	1.46ns	0.58ns/pF	1.04ns
			SCK ↑	Q ↑	3.24ns/pF	0.87ns	0.70ns/pF	0.73ns
			SCK ↑	QN ↓	7.93ns/pF	1.02ns	1.73ns/pF	0.87ns
			SCK ↑	QN ↑	8.79ns/pF	1.73ns	2.05ns/pF	1.19ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2S1CX

Master-Slave clocking, positive asynchronous clear, positive asynchronous preset.

Grids 20, **Transistors** 30

Inputs
D,MCK,SCK,PDA,PDB,CD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D	MCK	SCK	PD	CD	Q	QN	Q	QN
X	X	X	X	1	X	X	0	1
X	X	X	1	0	X	X	1	0
0	↓	↑	0	X	X	X	0	1
1	↓	↑	X	0	X	X	1	0

X = Don't care

Capacitances

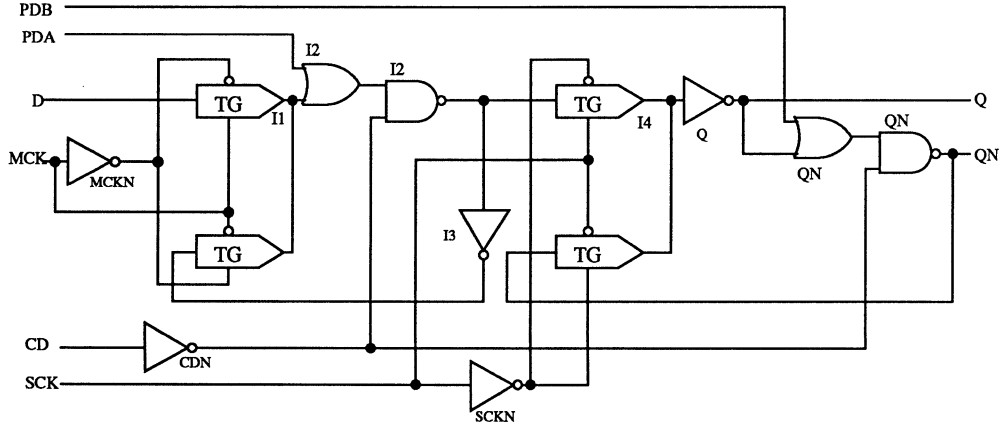
	D	MCK	SCK	PDA	PDB	CD
Area	0.028pF	0.057pF	0.057pF	0.027pF	0.027pF	0.027pF
Perf	0.031pF	0.065pF	0.065pF	0.102pF	0.102pF	0.102pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D ↓	0.92ns	0.75ns	CD ↑	Q ↓	7.99ns/pF	1.45ns	1.73ns/pF	1.04ns
D ↑	1.10ns	0.75ns	CD ↑	QN ↑	3.24ns/pF	1.04ns	0.66ns/pF	0.59ns
			PD ↑	Q ↑	8.32ns/pF	1.50ns	2.01ns/pF	0.87ns
			PD ↑	QN ↓	4.03ns/pF	1.21ns	1.07ns/pF	0.40ns
			SCK ↑	Q ↓	2.11ns/pF	1.40ns	0.62ns/pF	0.96ns
			SCK ↑	Q ↑	3.24ns/pF	0.98ns	0.70ns/pF	0.79ns
			SCK ↑	QN ↓	9.45ns/pF	1.20ns	2.14ns/pF	0.97ns
			SCK ↑	QN ↑	8.72ns/pF	1.76ns	2.01ns/pF	1.21ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



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Static D-Type Flip-Flop

FD2S1D

Master-Slave clocking, positive asynchronous clear.

Grids 18, **Transistors** 26

Inputs
D,MCK,SCK,CD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	MCK	SCK	CD	Q	QN	Q	QN
X	X	X	1	X	X	0	1
0	↓	↑	X	X	X	0	1
1	↓	↑	0	X	X	1	0

X = Don't care

Capacitances

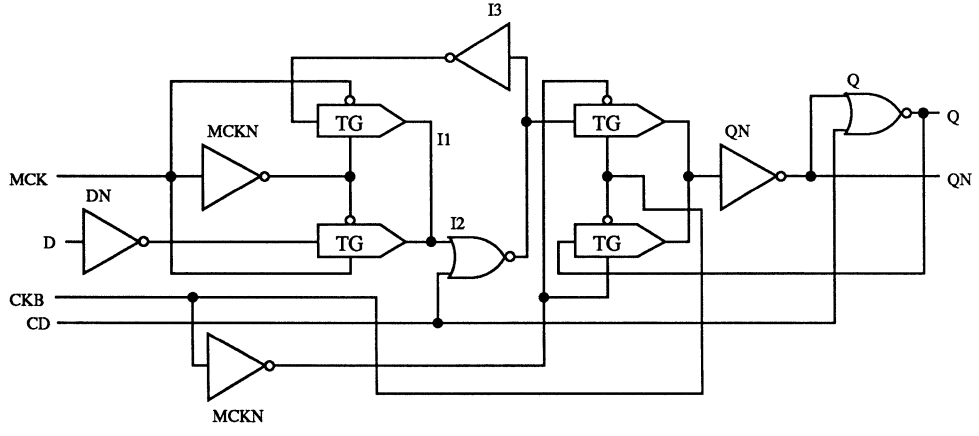
	D	MCK	SCK	CD
Area	0.028pF	0.057pF	0.059pF	0.057pF
Perf	0.103pF	0.065pF	0.068pF	0.207pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	0.98ns	0.69ns	CD ↑	Q ↓	2.25ns/pF	1.12ns	0.58ns/pF	0.35ns
D ↑	1.39ns	0.92ns	CD ↑	QN ↑	6.01ns/pF	1.44ns	1.40ns/pF	0.78ns
			SCK ↑	Q ↓	7.93ns/pF	1.02ns	1.73ns/pF	0.87ns
			SCK ↑	Q ↑	8.79ns/pF	1.73ns	2.05ns/pF	1.19ns
			SCK ↑	QN ↓	2.11ns/pF	1.46ns	0.58ns/pF	1.04ns
			SCK ↑	QN ↑	3.24ns/pF	0.87ns	0.70ns/pF	0.73ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop FD2S1E

Master-Slave clocking, negative asynchronous clear.

Grids 17, **Transistors** 24

Inputs
D,MCK,SCK,CDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS OLD		OUTPUTS NEW	
D	MCK	SCK	CDN	Q	QN	Q	QN
X	X	X	0	X	X	0	1
0	↓	↑	X	X	X	0	1
1	↓	↑	1	X	X	1	0

X = Don't care

Capacitances

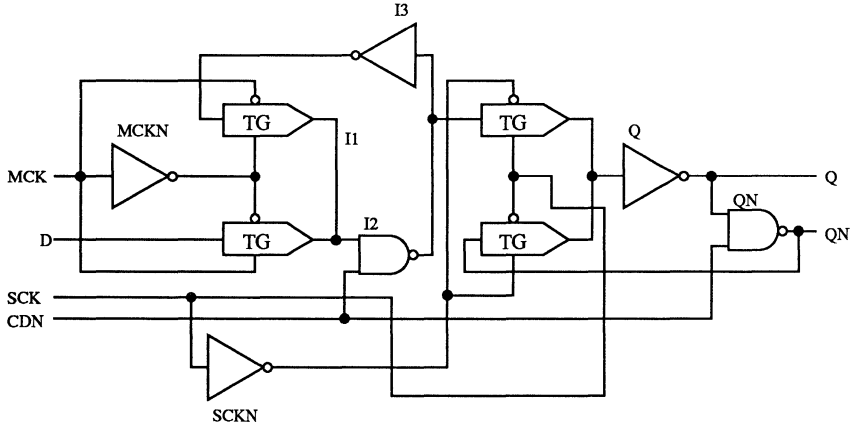
	D	MCK	SCK	CDN
Area	0.019pF	0.056pF	0.059pF	0.057pF
Perf	0.020pF	0.065pF	0.068pF	0.207pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
D ↓	0.64ns	0.69ns	CDN ↓	Q ↓	7.93ns/pF	0.90ns	1.77ns/pF	0.67ns
D ↑	1.04ns	0.81ns	CDN ↓	QN ↑	3.24ns/pF	0.46ns	0.70ns/pF	0.21ns
			SCK ↑	Q ↓	2.05ns/pF	1.20ns	0.58ns/pF	0.92ns
			SCK ↑	Q ↑	3.24ns/pF	1.04ns	0.70ns/pF	0.79ns
			SCK ↑	QN ↓	9.45ns/pF	1.26ns	2.14ns/pF	0.97ns
			SCK ↑	QN ↑	5.68ns/pF	1.40ns	1.40ns/pF	1.07ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2S1FX

Master-Slave clocking, negative asynchronous clear, positive asynchronous preset.

Grids 19, **Transistors** 28

Inputs
D,MCK,SCK,PDA,PDB,CDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D	MCK	SCK	PD	CDN	Q	QN	Q	QN
X	X	X	X	0	X	X	0	1
X	X	X	1	1	X	X	1	0
0	↓	↑	0	X	X	X	0	1
1	↓	↑	X	1	X	X	1	0

X = Don't care

Capacitances

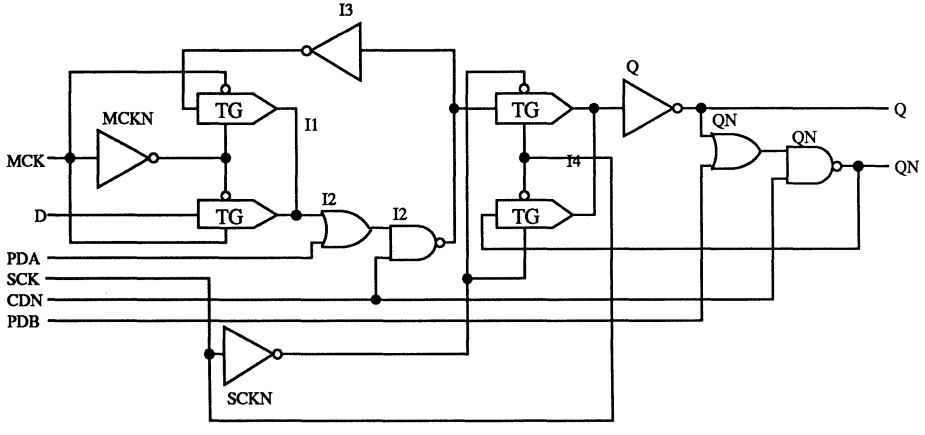
	D	MCK	SCK	PDA	PDB	CDN
Area	0.028pF	0.057pF	0.057pF	0.027pF	0.027pF	0.060pF
Perf	0.031pF	0.065pF	0.065pF	0.102pF	0.103pF	0.210pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	0.92ns	0.75ns	CDN ↓	Q ↓	7.99ns/pF	0.93ns	1.77ns/pF	0.67ns
D ↑	1.10ns	0.75ns	CDN ↓	QN ↑	3.24ns/pF	0.52ns	0.70ns/pF	0.21ns
			PD ↑	Q ↑	8.32ns/pF	1.50ns	2.01ns/pF	0.87ns
			PD ↑	QN ↓	4.03ns/pF	1.21ns	1.07ns/pF	0.40ns
			SCK ↑	Q ↓	2.11ns/pF	1.40ns	0.62ns/pF	0.96ns
			SCK ↑	Q ↑	3.24ns/pF	0.98ns	0.70ns/pF	0.79ns
			SCK ↑	QN ↓	9.38ns/pF	1.28ns	2.14ns/pF	0.97ns
			SCK ↑	QN ↑	8.72ns/pF	1.76ns	2.01ns/pF	1.21ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2S1G

Master-Slave clocking, negative asynchronous preset.

Grids 18, **Transistors** 26

Inputs
D,MCK,SCK,PDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	MCK	SCK	PDN	Q	QN	Q	QN
X	X	X	0	X	X	1	0
0	↓	↑	1	X	X	0	1
1	↓	↑	X	X	X	1	0

X = Don't care

Capacitances

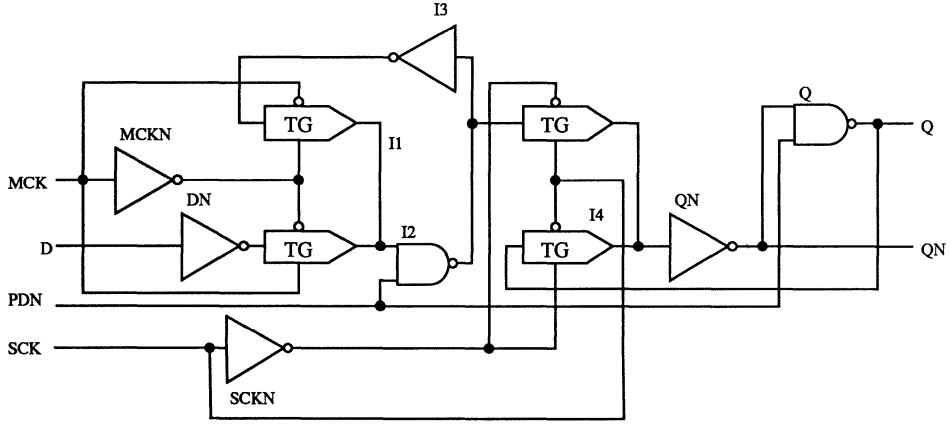
	D	MCK	SCK	PDN
Area	0.028pF	0.057pF	0.059pF	0.057pF
Perf	0.103pF	0.065pF	0.068pF	0.207pF

Delay Information

Input Signal	Setup Time		From	To	Propagation Delay			
					Area		Performance	
Name	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.10ns	0.81ns	PDN ↓	Q ↑	3.24ns/pF	0.46ns	0.70ns/pF	0.21ns
D ↑	1.21ns	0.75ns	PDN ↓	QN ↓	7.93ns/pF	0.90ns	1.77ns/pF	0.67ns
			SCK ↑	Q ↓	9.38ns/pF	1.28ns	2.14ns/pF	0.97ns
			SCK ↑	Q ↑	5.68ns/pF	1.40ns	1.40ns/pF	1.07ns
			SCK ↑	QN ↓	2.05ns/pF	1.20ns	0.58ns/pF	0.92ns
			SCK ↑	QN ↑	3.24ns/pF	1.04ns	0.70ns/pF	0.79ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2S1I

Master-Slave clocking, positive synchronous clear.

Grids 17, **Transistors** 26

Inputs
D,MCK,SCK,CD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	MCK	SCK	CD	Q	QN	Q	QN
X	↓	↑	1	X	X	0	1
0	↓	↑	X	X	X	0	1
1	↓	↑	0	X	X	1	0

X = Don't care

Capacitances

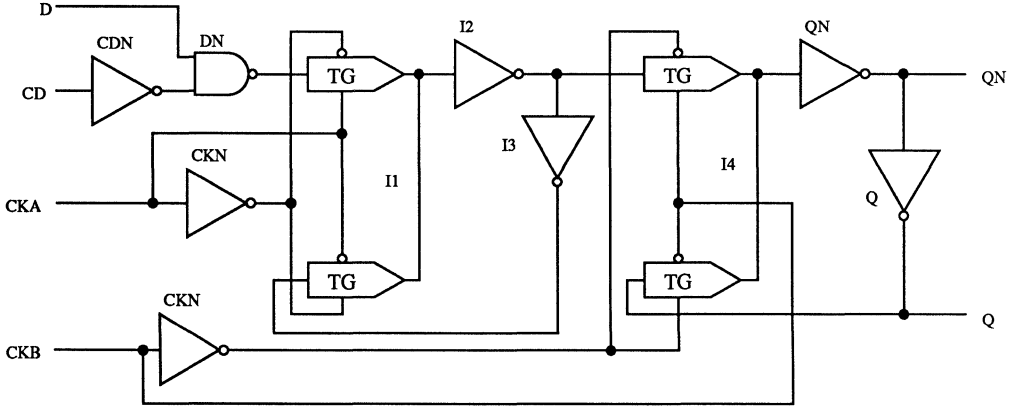
	D	MCK	SCK	CD
Area	0.028pF	0.057pF	0.056pF	0.027pF
Perf	0.103pF	0.065pF	0.065pF	0.102pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
CD ↓	1.21ns	0.92ns	SCK ↑	Q ↓	7.99ns/pF	0.99ns	1.73ns/pF	0.87ns
CD ↑	1.27ns	0.92ns	SCK ↑	Q ↑	5.75ns/pF	1.37ns	1.40ns/pF	1.07ns
D ↓	0.92ns	0.69ns	SCK ↑	QN ↓	1.98ns/pF	1.22ns	0.58ns/pF	0.92ns
D ↑	1.33ns	0.87ns	SCK ↑	QN ↑	3.24ns/pF	0.87ns	0.70ns/pF	0.73ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2S1J

Master-Slave clocking, positive synchronous preset.

Grids 16, **Transistors** 24

Inputs
D,MCK,SCK,PD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	MCK	SCK	PD	Q	QN	Q	QN
X	↓	↑	1	X	X	1	0
0	↓	↑	0	X	X	0	1
1	↓	↑	X	X	X	1	0

X = Don't care

Capacitances

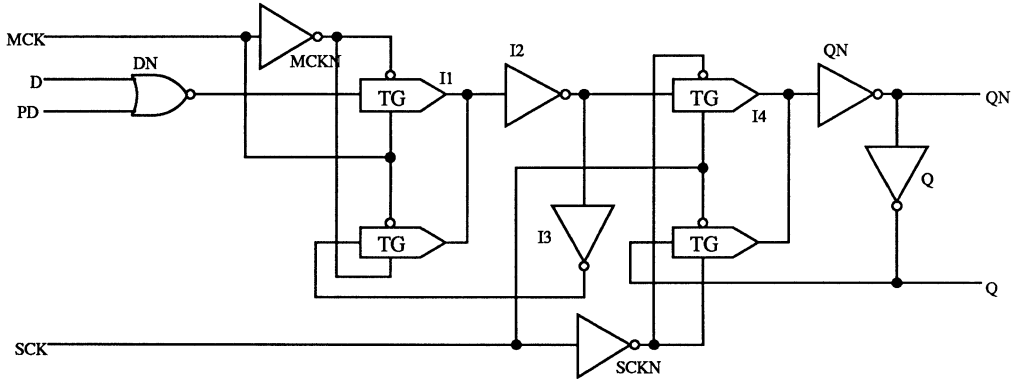
	D	MCK	SCK	PD
Area	0.027pF	0.058pF	0.056pF	0.027pF
Perf	0.102pF	0.066pF	0.065pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.33ns	0.92ns	SCK ↑	Q ↓	7.99ns/pF	0.99ns	1.73ns/pF	0.87ns
D ↑	1.16ns	0.75ns	SCK ↑	Q ↑	5.75ns/pF	1.37ns	1.40ns/pF	1.07ns
PD ↓	1.33ns	0.92ns	SCK ↑	QN ↓	1.98ns/pF	1.22ns	0.58ns/pF	0.92ns
PD ↑	1.16ns	0.75ns	SCK ↑	QN ↑	3.24ns/pF	0.87ns	0.70ns/pF	0.73ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2S1KX

Master-Slave clocking, negative asynchronous clear, negative asynchronous preset.

Grids 21, **Transistors** 32

Inputs
D,MCK,SCK,PDNA,PDNB,CDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D	MCK	SCK	PDN	CDN	Q	QN	Q	QN
X	X	X	X	0	X	X	0	1
X	X	X	0	1	X	X	1	0
0	↓	↑	1	X	X	X	0	1
1	↓	↑	X	1	X	X	1	0

X = Don't care

Capacitances

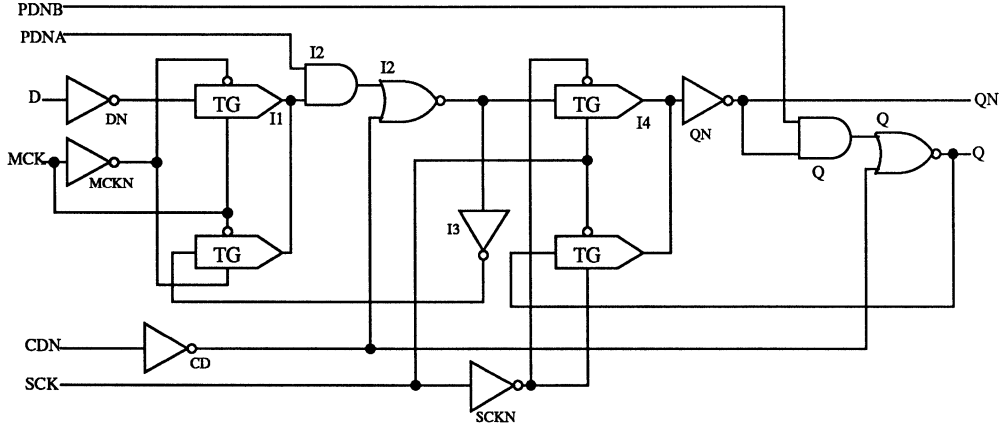
	D	MCK	SCK	PDNA	PDNB	CDN
Area	0.028pF	0.058pF	0.057pF	0.027pF	0.027pF	0.027pF
Perf	0.103pF	0.066pF	0.065pF	0.102pF	0.103pF	0.102pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
D ↓	1.10ns	0.81ns	CDN ↓	Q ↓	1.98ns/pF	0.93ns	0.53ns/pF	0.54ns
D ↑	1.44ns	0.92ns	CDN ↓	QN ↑	5.75ns/pF	1.20ns	1.36ns/pF	0.92ns
			PDN ↓	Q ↑	6.47ns/pF	0.69ns	1.40ns/pF	0.31ns
			PDN ↓	QN ↓	12.75ns/pF	1.23ns	2.79ns/pF	0.80ns
			SCK ↑	Q ↓	9.38ns/pF	1.22ns	2.14ns/pF	0.97ns
			SCK ↑	Q ↑	8.72ns/pF	1.76ns	2.01ns/pF	1.21ns
			SCK ↑	QN ↓	2.11ns/pF	1.40ns	0.62ns/pF	0.96ns
			SCK ↑	QN ↑	3.24ns/pF	0.98ns	0.70ns/pF	0.79ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2S1L

Master-Slave clocking, negative synchronous preset.

Grids 17, **Transistors** 26

Inputs
D,MCK,SCK,PDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	MCK	SCK	PDN	Q	QN	Q	QN
X	↓	↑	0	X	X	1	0
0	↓	↑	1	X	X	0	1
1	↓	↑	X	X	X	1	0

X = Don't care

Capacitances

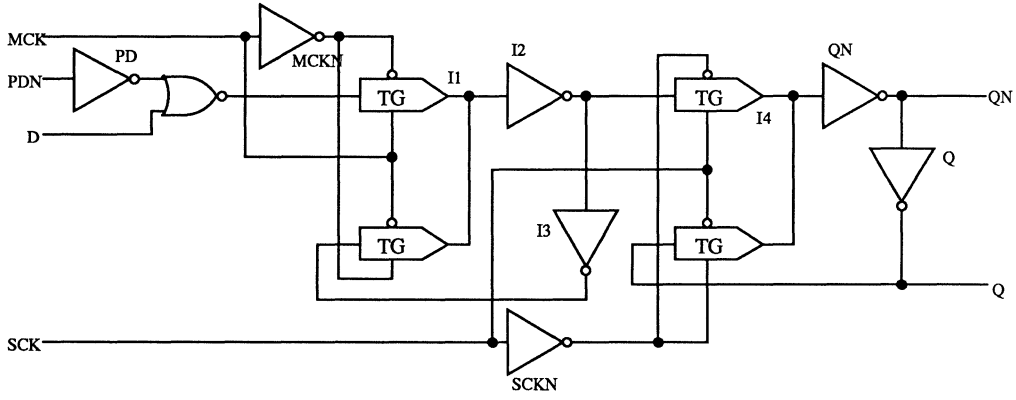
	D	MCK	SCK	PDN
Area	0.028pF	0.058pF	0.056pF	0.027pF
Perf	0.103pF	0.066pF	0.065pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D ↓	1.21ns	0.81ns	SCK ↑	Q ↓	7.99ns/pF	0.99ns	1.73ns/pF	0.87ns
D ↑	1.10ns	0.69ns	SCK ↑	Q ↑	5.75ns/pF	1.37ns	1.40ns/pF	1.07ns
PDN ↓	1.04ns	0.81ns	SCK ↑	QN ↓	1.98ns/pF	1.22ns	0.58ns/pF	0.92ns
PDN ↑	1.56ns	1.04ns	SCK ↑	QN ↑	3.24ns/pF	0.87ns	0.70ns/pF	0.73ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



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Static D-Type Flip-Flop

FD2S1M

Master-Slave clocking, negative synchronous clear.

Grids 16, **Transistors** 24

Inputs
D,MCK,SCK,CDN

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D	MCK	SCK	CDN	Q	QN	Q	QN
X	↓	↑	0	X	X	0	1
0	↓	↑	X	X	X	0	1
1	↓	↑	1	X	X	1	0

X = Don't care

Capacitances

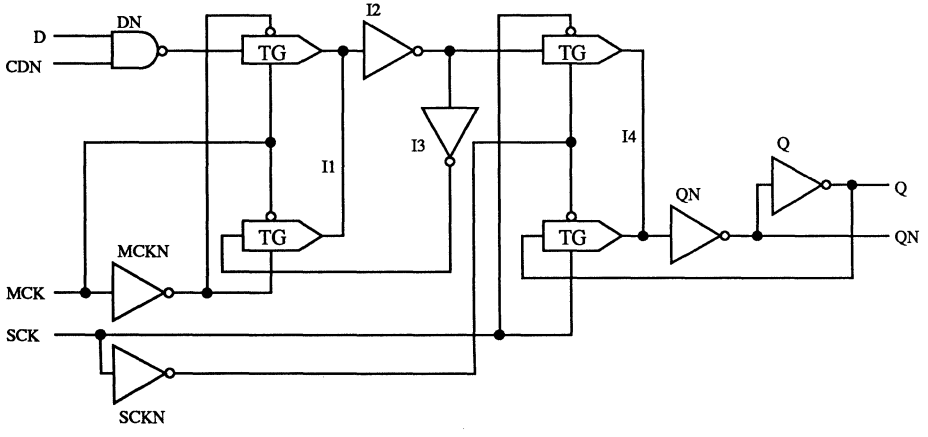
	D	MCK	SCK	CDN
Area	0.027pF	0.058pF	0.056pF	0.027pF
Perf	0.103pF	0.066pF	0.065pF	0.103pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	0.98ns	0.75ns	SCK ↑	Q ↓	7.99ns/pF	0.99ns	1.73ns/pF	0.87ns
CDN ↑	1.39ns	0.87ns	SCK ↑	Q ↑	5.75ns/pF	1.37ns	1.40ns/pF	1.07ns
D ↓	0.98ns	0.75ns	SCK ↑	QN ↓	1.98ns/pF	1.22ns	0.58ns/pF	0.92ns
D ↑	1.39ns	0.87ns	SCK ↑	QN ↑	3.24ns/pF	0.87ns	0.70ns/pF	0.73ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FD2S1NX

Master-Slave clocking, positive asynchronous clear, negative asynchronous preset.

Grids 20, **Transistors** 30

Inputs
D,MCK,SCK,PDNA,PDNB,CD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS OLD		OUTPUTS NEW	
D	MCK	SCK	PDN	CD	Q	QN	Q	QN
X	X	X	X	1	X	X	0	1
X	X	X	0	0	X	X	1	0
0	↓	↑	1	X	X	X	0	1
1	↓	↑	X	0	X	X	1	0

X = Don't care

Capacitances

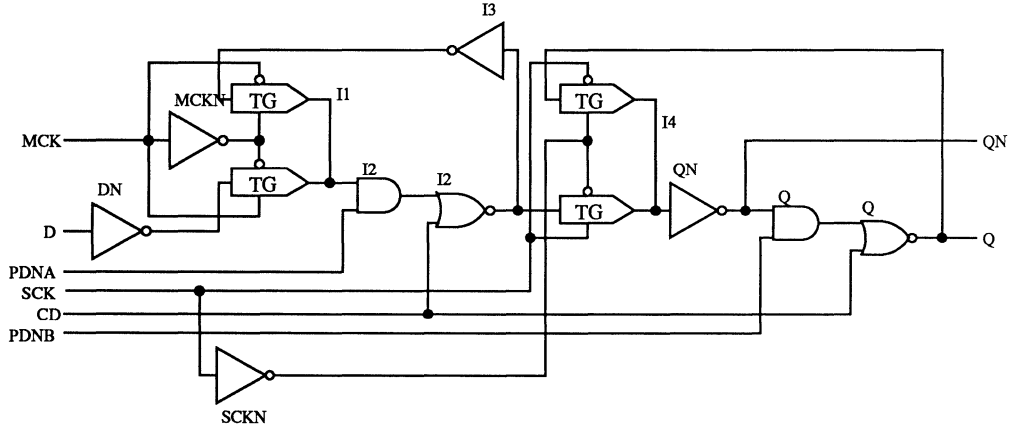
	D	MCK	SCK	PDNA	PDNB	CD
Area	0.028pF	0.058pF	0.057pF	0.027pF	0.027pF	0.060pF
Perf	0.103pF	0.066pF	0.065pF	0.102pF	0.103pF	0.210pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
D ↓	1.10ns	0.81ns	CD ↑	Q ↓	2.31ns/pF	1.10ns	0.58ns/pF	0.40ns
D ↑	1.44ns	0.92ns	CD ↑	QN ↑	6.01ns/pF	1.44ns	1.40ns/pF	0.78ns
			PDN ↓	Q ↑	6.47ns/pF	0.69ns	1.40ns/pF	0.31ns
			PDN ↓	QN ↓	12.75ns/pF	1.23ns	2.79ns/pF	0.80ns
			SCK ↑	Q ↓	9.45ns/pF	1.20ns	2.14ns/pF	0.97ns
			SCK ↑	Q ↑	8.72ns/pF	1.76ns	2.01ns/pF	1.21ns
			SCK ↑	QN ↓	2.11ns/pF	1.40ns	0.62ns/pF	0.96ns
			SCK ↑	QN ↑	3.24ns/pF	1.98ns	0.70ns/pF	0.79ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1N2AX

Negative edge triggered, data select front end, negative level sample.

Grids 26, **Transistors** 36

Inputs
D0,D1,SPN,CKA,CKB,SD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	SPN	CK	SD	Q	QN	Q	QN
0	X	X	↓	0	X	X	0	1
1	X	X	↓	0	X	X	1	0
X	0	0	↓	1	X	X	0	1
X	1	0	↓	1	X	X	1	0
X	X	1	↓	1	0	1	0	1
X	X	1	↓	1	1	0	1	0

X = Don't care

Capacitances

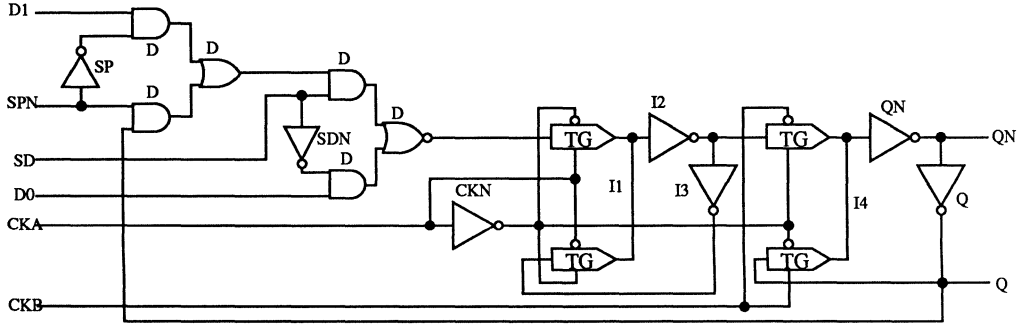
	D0	D1	SPN	CKA	CKB	SD
Area	0.027pF	0.027pF	0.057pF	0.057pF	0.029pF	0.056pF
Perf	0.102pF	0.102pF	0.207pF	0.065pF	0.033pF	0.206pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.73ns	1.10ns	CK ↓	Q ↓	7.93ns/pF	1.30ns	1.73ns/pF	1.16ns
D0 ↑	1.73ns	1.04ns	CK ↓	Q ↑	5.81ns/pF	1.40ns	1.40ns/pF	1.18ns
D1 ↓	1.97ns	1.21ns	CK ↓	QN ↓	2.05ns/pF	1.14ns	0.58ns/pF	0.98ns
D1 ↑	1.97ns	1.21ns	CK ↓	QN ↑	3.17ns/pF	1.07ns	0.70ns/pF	0.91ns
SD ↓	1.68ns	1.10ns						
SD ↑	2.60ns	1.56ns						
SPN ↓	2.25ns	1.33ns						
SPN ↑	2.66ns	1.56ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1N2JX

Negative edge triggered, data select front end, negative level sample, positive synchronous preset.

Grids 27, **Transistors** 38

Inputs

D0,D1,SPN,CKA,CKB,SD,PD

Outputs

Q,QN

Capacitances

	D0	D1	SPN	CKA	CKB	SD	PD
Area	0.027pF	0.027pF	0.055pF	0.057pF	0.029pF	0.055pF	0.027pF
Perf	0.102pF	0.102pF	0.205pF	0.065pF	0.033pF	0.206pF	0.102pF

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	SPN	CK	SD	PD	Q	QN	Q	QN
0	X	X	↓	0	X	X	X	0	1
1	X	X	↓	0	X	X	X	1	0
X	X	X	↓	1	1	X	X	1	0
X	0	0	↓	1	0	X	X	0	1
X	1	0	↓	1	X	X	X	1	0
X	X	1	↓	1	0	0	1	0	1
X	X	1	↓	1	X	1	0	1	0

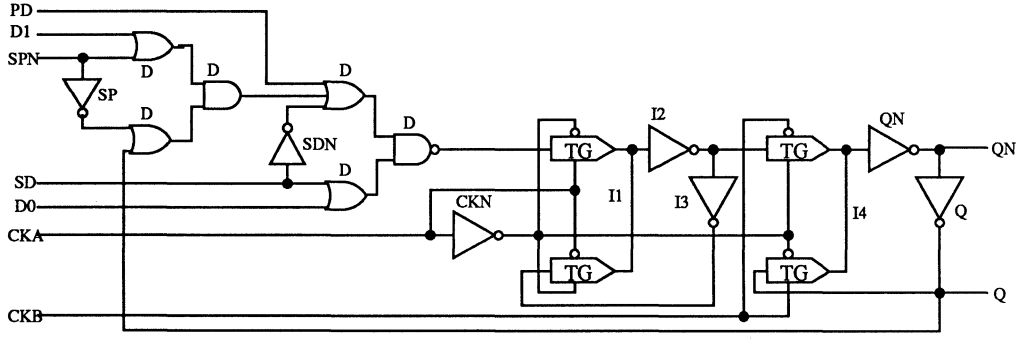
X = Don't care **Note: PD does not function while SD=0**

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	1.73ns	1.10ns	CK ↓	Q ↓	7.93ns/pF	1.30ns	1.73ns/pF	1.16ns
D0 ↑	1.62ns	0.98ns	CK ↓	Q ↑	5.81ns/pF	1.40ns	1.44ns/pF	1.16ns
D1 ↓	2.83ns	1.62ns	CK ↓	QN ↓	2.05ns/pF	1.14ns	0.58ns/pF	0.98ns
D1 ↑	1.79ns	1.10ns	CK ↓	QN ↑	3.17ns/pF	1.07ns	0.70ns/pF	0.91ns
PD ↓	2.83ns	1.62ns						
PD ↑	1.56ns	0.92ns						
SD ↓	1.73ns	1.10ns						
SD ↑	3.24ns	1.85ns						
SPN ↓	2.83ns	1.62ns						
SPN ↑	3.18ns	1.85ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1N2MX

Negative edge triggered, data select front end, negative level sample, negative synchronous clear.

Grids 27, **Transistors** 38

Inputs
D0,D1,SPN,CKA,CKB,SD,CDN

Outputs
Q,QN

Capacitances

Truth Table

INPUTS						OUTPUTS OLD		OUTPUTS NEW	
D0	D1	SPN	CK	SD	CDN	Q	QN	Q	QN
0	X	X	↓	0	X	X	X	0	1
1	X	X	↓	0	X	X	X	1	0
X	X	X	↓	1	0	X	X	0	1
X	0	0	↓	1	X	X	X	0	1
X	1	0	↓	1	1	X	X	1	0
X	X	1	↓	1	X	0	1	0	1
X	X	1	↓	1	1	1	0	1	0

X = Don't care **Note: CDN does not function while SD=0**

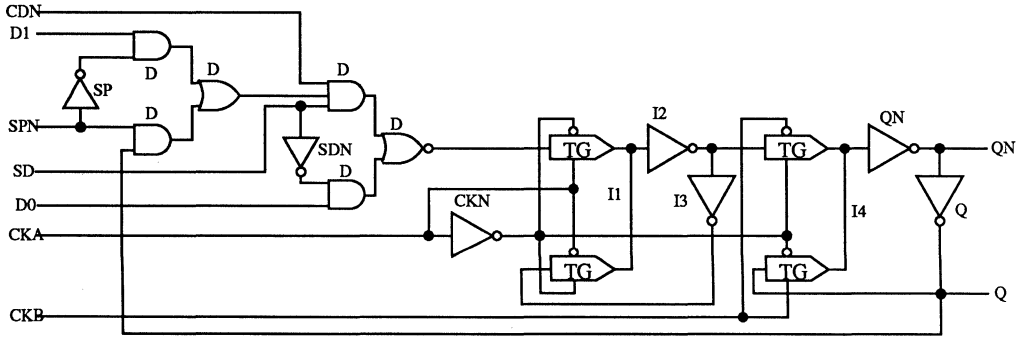
	D0	D1	SPN	CKA	CKB	SD	CDN
Area	0.027pF	0.027pF	0.057pF	0.057pF	0.029pF	0.056pF	0.027pF
Perf	0.102pF	0.102pF	0.207pF	0.065pF	0.033pF	0.206pF	0.102pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
CDN ↓	1.79ns	1.10ns	CK ↓	Q ↓	7.93ns/pF	1.30ns	1.73ns/pF	1.16ns
CDN ↑	2.31ns	1.44ns	CK ↓	Q ↑	5.81ns/pF	1.40ns	1.40ns/pF	1.18ns
D0 ↓	1.79ns	1.16ns	CK ↓	QN ↓	2.05ns/pF	1.14ns	0.58ns/pF	0.98ns
D0 ↑	1.73ns	1.10ns	CK ↓	QN ↑	3.17ns/pF	1.07ns	0.70ns/pF	0.91ns
D1 ↓	2.02ns	1.21ns						
D1 ↑	2.31ns	1.44ns						
SD ↓	1.73ns	1.10ns						
SD ↑	2.66ns	1.62ns						
SPN ↓	2.31ns	1.50ns						
SPN ↑	2.72ns	1.62ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1N3AX

Positive edge triggered, data select front end, negative level sample.

Grids 26, **Transistors** 36

Inputs
D0,D1,SPN,CKA,CKB,SD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	SPN	CK	SD	Q	QN	Q	QN
0	X	X	↑	0	X	X	0	1
1	X	X	↑	0	X	X	1	0
X	0	0	↑	1	X	X	0	1
X	1	0	↑	1	X	X	1	0
X	X	1	↑	1	0	1	0	1
X	X	1	↑	1	1	0	1	0

X = Don't care

Capacitances

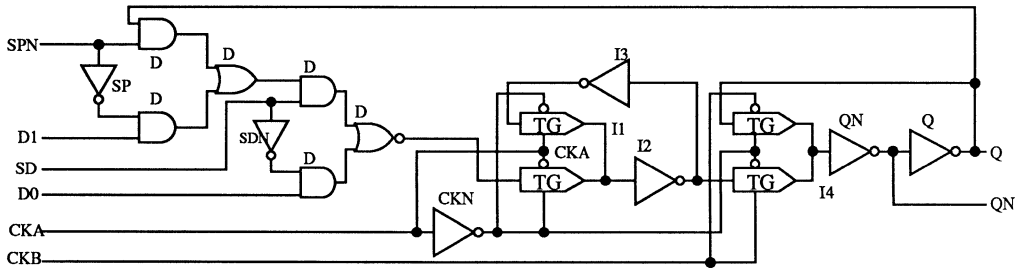
	D0	D1	SPN	CKA	CKB	SD
Area	0.027pF	0.027pF	0.057pF	0.057pF	0.029pF	0.056pF
Perf	0.102pF	0.102pF	0.207pF	0.065pF	0.033pF	0.206pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.73ns	1.10ns	CK ↑	Q ↓	7.93ns/pF	1.30ns	1.73ns/pF	1.04ns
D0 ↑	1.68ns	1.04ns	CK ↑	Q ↑	5.81ns/pF	1.81ns	1.44ns/pF	1.27ns
D1 ↓	1.97ns	1.21ns	CK ↑	QN ↓	2.05ns/pF	1.54ns	0.58ns/pF	1.10ns
D1 ↑	1.97ns	1.21ns	CK ↑	QN ↑	3.24ns/pF	1.04ns	0.66ns/pF	0.88ns
SD ↓	1.68ns	1.10ns						
SD ↑	2.54ns	1.56ns						
SPN ↓	2.20ns	1.33ns						
SPN ↑	2.60ns	1.56ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1N3JX

Positive edge triggered, data select front end, negative level sample, positive synchronous preset.

Grids 27, **Transistors** 38

Inputs
D0,D1,SPN,CKA,CKB,SD,PD

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	SPN	CK	SD	PD	Q	QN	Q	QN
0	X	X	↑	0	X	X	X	0	1
1	X	X	↑	0	X	X	X	1	0
X	X	X	↑	1	1	X	X	1	0
X	0	0	↑	1	0	X	X	0	1
X	1	0	↑	1	X	X	X	1	0
X	X	1	↑	1	0	0	1	0	1
X	X	1	↑	1	X	1	0	1	0

X = Don't care **Note: PD does not function while SD=0**

Capacitances

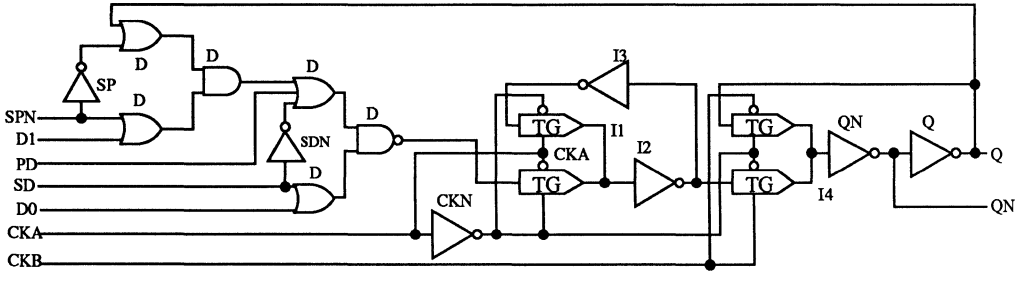
	D0	D1	SPN	CKA	CKB	SD	PD
Area	0.027pF	0.027pF	0.055pF	0.057pF	0.029pF	0.055pF	0.027pF
Perf	0.102pF	0.102pF	0.205pF	0.065pF	0.033pF	0.206pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.73ns	1.10ns	CK ↑	Q ↓	7.93ns/pF	1.30ns	1.73ns/pF	1.04ns
D0 ↑	1.62ns	0.98ns	CK ↑	Q ↑	5.75ns/pF	1.89ns	1.44ns/pF	1.27ns
D1 ↓	2.83ns	1.62ns	CK ↑	QN ↓	1.98ns/pF	1.63ns	0.58ns/pF	1.10ns
D1 ↑	1.79ns	1.10ns	CK ↑	QN ↑	3.24ns/pF	1.04ns	0.66ns/pF	0.88ns
PD ↓	2.83ns	1.62ns						
PD ↑	1.56ns	0.92ns						
SD ↓	1.73ns	1.10ns						
SD ↑	3.24ns	1.85ns						
SPN ↓	2.83ns	1.62ns						
SPN ↑	3.24ns	1.85ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1N3MX

Positive edge triggered, data select front end, negative level sample, negative synchronous clear.

Grids 27, **Transistors** 38

Inputs
D0,D1,SPN,CKA,CKB,SD,CDN

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	SPN	CK	SD	CDN	Q	QN	Q	QN
0	X	X	↑	0	X	X	X	0	1
1	X	X	↑	0	X	X	X	1	0
X	X	X	↑	1	0	X	X	0	1
X	0	0	↑	1	X	X	X	0	1
X	1	0	↑	1	1	X	X	1	0
X	X	1	↑	1	X	0	1	0	1
X	X	1	↑	1	1	1	0	1	0

X = Don't care **Note: CDN does not function while SD=0**

Capacitances

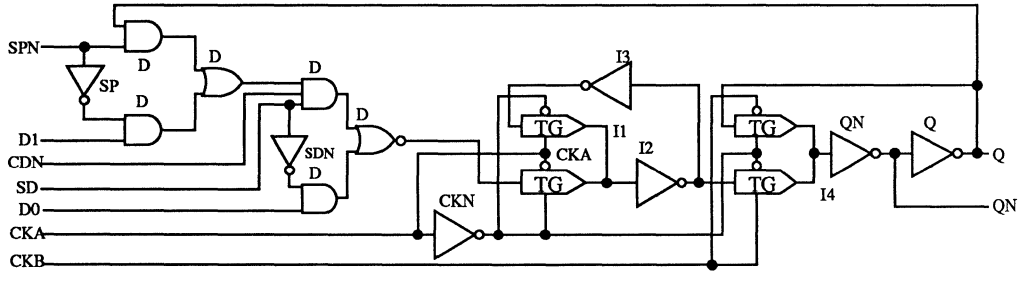
	D0	D1	SPN	CKA	CKB	SD	CDN
Area	0.027pF	0.027pF	0.057pF	0.057pF	0.029pF	0.056pF	0.027pF
Perf	0.102pF	0.102pF	0.207pF	0.065pF	0.033pF	0.206pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	1.73ns	1.10ns	CK ↑	Q ↓	7.93ns/pF	1.30ns	1.73ns/pF	1.04ns
CDN ↑	2.31ns	1.44ns	CK ↑	Q ↑	5.81ns/pF	1.81ns	1.44ns/pF	1.27ns
D0 ↓	1.79ns	1.16ns	CK ↑	QN ↓	2.05ns/pF	1.54ns	0.58ns/pF	1.10ns
D0 ↑	1.73ns	1.10ns	CK ↑	QN ↑	3.24ns/pF	1.04ns	0.66ns/pF	0.88ns
D1 ↓	2.02ns	1.21ns						
D1 ↑	2.31ns	1.44ns						
SD ↓	1.73ns	1.10ns						
SD ↑	2.66ns	1.62ns						
SPN ↓	2.25ns	1.50ns						
SPN ↑	2.72ns	1.62ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1P2AX

Negative edge triggered, data select front end, positive level sample.

Grids 26, **Transistors** 36

Inputs
D0,D1,SP,CKA,CKB,SD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	SP	CK	SD	Q	QN	Q	QN
0	X	X	↓	0	X	X	0	1
1	X	X	↓	0	X	X	1	0
X	0	1	↓	1	X	X	0	1
X	1	1	↓	1	X	X	1	0
X	X	0	↓	1	0	1	0	1
X	X	0	↓	1	1	0	1	0

X = Don't care

Capacitances

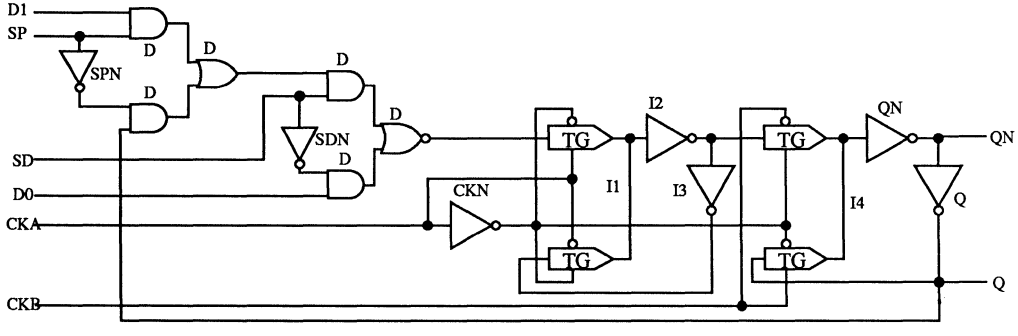
	D0	D1	SP	CKA	CKB	SD
Area	0.027pF	0.027pF	0.055pF	0.057pF	0.029pF	0.056pF
Perf	0.102pF	0.102pF	0.206pF	0.065pF	0.033pF	0.206pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.73ns	1.10ns	CK ↓	Q ↓	7.93ns/pF	1.30ns	1.73ns/pF	1.16ns
D0 ↑	1.73ns	1.04ns	CK ↓	Q ↑	5.81ns/pF	1.40ns	1.40ns/pF	1.18ns
D1 ↓	1.97ns	1.21ns	CK ↓	QN ↓	2.05ns/pF	1.14ns	0.58ns/pF	0.98ns
D1 ↑	1.97ns	1.21ns	CK ↓	QN ↑	3.17ns/pF	1.07ns	0.70ns/pF	0.91ns
SD ↓	1.68ns	1.10ns						
SD ↑	2.60ns	1.56ns						
SP ↓	2.20ns	1.33ns						
SP ↑	2.66ns	1.56ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1P2JX

Negative edge triggered, data select front end, positive level sample, positive synchronous preset.

Grids 27, **Transistors** 38

Inputs
D0,D1,SP,CKA,CKB,SD,PD

Outputs
Q,QN

Capacitances

Truth Table

INPUTS						OUTPUTS OLD		OUTPUTS NEW	
D0	D1	SP	CK	SD	PD	Q	QN	Q	QN
0	X	X	↓	0	X	X	X	0	1
1	X	X	↓	0	X	X	X	1	0
X	X	X	↓	1	1	X	X	1	0
X	0	1	↓	1	0	X	X	0	1
X	1	1	↓	1	X	X	X	1	0
X	X	0	↓	1	0	0	1	0	1
X	X	0	↓	1	X	1	0	1	0

X = Don't care **Note: PD does not function while SD=0**

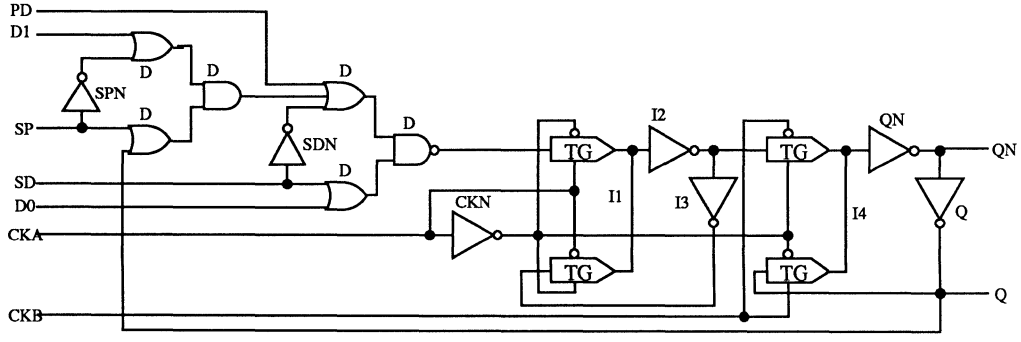
	D0	D1	SP	CKA	CKB	SD	PD
Area	0.027pF	0.027pF	0.057pF	0.057pF	0.029pF	0.055pF	0.027pF
Perf	0.102pF	0.102pF	0.207pF	0.065pF	0.033pF	0.206pF	0.102pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	1.73ns	1.10ns	CK ↓	Q ↓	7.93ns/pF	1.30ns	1.73ns/pF	1.16ns
D0 ↑	1.62ns	0.98ns	CK ↓	Q ↑	5.81ns/pF	1.40ns	1.44ns/pF	1.16ns
D1 ↓	2.83ns	1.62ns	CK ↓	QN ↓	2.05ns/pF	1.14ns	0.58ns/pF	0.98ns
D1 ↑	1.79ns	1.10ns	CK ↓	QN ↑	3.17ns/pF	1.07ns	0.70ns/pF	0.91ns
PD ↓	2.83ns	1.62ns						
PD ↑	1.56ns	0.92ns						
SD ↓	1.73ns	1.10ns						
SD ↑	3.24ns	1.85ns						
SP ↓	2.83ns	1.62ns						
SP ↑	3.24ns	1.85ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1P2MX

Negative edge triggered, data select front end, positive level sample, negative synchronous clear.

Grids 27, **Transistors** 38

Inputs
D0,D1,SP,CKA,CKB,SD,CDN

Outputs
Q,QN

Capacitances

	D0	D1	SP	CKA	CKB	SD	CDN
Area	0.027pF	0.027pF	0.055pF	0.057pF	0.029pF	0.056pF	0.027pF
Perf	0.102pF	0.102pF	0.205pF	0.065pF	0.033pF	0.206pF	0.102pF

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	**D1**	**SP**	**CK**	**SD**	**CDN**	**Q**	**QN**	**Q**	**QN**
0	X	X	↓	0	X	X	X	0	1
1	X	X	↓	0	X	X	X	1	0
X	X	X	↓	1	0	X	X	0	1
X	0	1	↓	1	X	X	X	0	1
X	1	1	↓	1	1	X	X	1	0
X	X	0	↓	1	X	0	1	0	1
X	X	0	↓	1	1	1	0	1	0

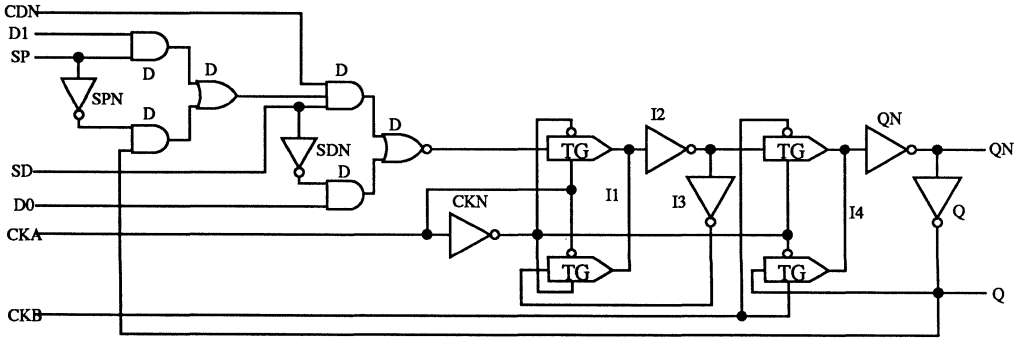
X = Don't care **Note: CDN does not function while SD=0**

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	1.79ns	1.10ns	CK ↓	Q ↓	7.93ns/pF	1.30ns	1.73ns/pF	1.16ns
CDN ↑	2.31ns	1.44ns	CK ↓	Q ↑	5.81ns/pF	1.40ns	1.44ns/pF	1.16ns
D0 ↓	1.79ns	1.10ns	CK ↓	QN ↓	2.05ns/pF	1.14ns	0.58ns/pF	0.98ns
D0 ↑	1.73ns	1.10ns	CK ↓	QN ↑	3.24ns/pF	0.98ns	0.70ns/pF	0.91ns
D1 ↓	2.02ns	1.21ns						
D1 ↑	2.31ns	1.44ns						
SD ↓	1.73ns	1.10ns						
SD ↑	2.66ns	1.62ns						
SP ↓	2.31ns	1.50ns						
SP ↑	2.72ns	1.62ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1P3AX

Positive edge triggered, data select front end, positive level sample.

Grids 26, **Transistors** 36

Inputs
D0,D1,SP,CKA,CKB,SD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	SP	CK	SD	Q	QN	Q	QN
0	X	X	↑	0	X	X	0	1
1	X	X	↑	0	X	X	1	0
X	0	1	↑	1	X	X	0	1
X	1	1	↑	1	X	X	1	0
X	X	0	↑	1	0	1	0	1
X	X	0	↑	1	1	0	1	0

X = Don't care

Capacitances

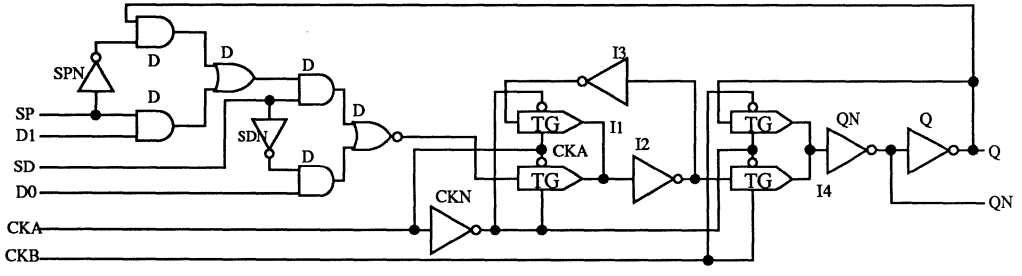
	D0	D1	SP	CKA	CKB	SD
Area	0.027pF	0.027pF	0.055pF	0.057pF	0.029pF	0.056pF
Perf	0.102pF	0.102pF	0.206pF	0.065pF	0.033pF	0.206pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.73ns	1.10ns	CK ↑	Q ↓	7.93ns/pF	1.30ns	1.73ns/pF	1.04ns
D0 ↑	1.68ns	1.04ns	CK ↑	Q ↑	5.81ns/pF	1.81ns	1.44ns/pF	1.27ns
D1 ↓	1.97ns	1.21ns	CK ↑	QN ↓	2.05ns/pF	1.54ns	0.58ns/pF	1.10ns
D1 ↑	1.97ns	1.21ns	CK ↑	QN ↑	3.24ns/pF	1.04ns	0.66ns/pF	0.88ns
SD ↓	1.68ns	1.10ns						
SD ↑	2.54ns	1.56ns						
SP ↓	2.20ns	1.33ns						
SP ↑	2.60ns	1.56ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1P3JX

Positive edge triggered, data select front end, positive level sample, positive synchronous preset.

Grids 27, **Transistors** 38

Inputs
D0,D1,SP,CKA,CKB,SD,PD

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS OLD		OUTPUTS NEW	
D0	D1	SP	CK	SD	PD	Q	QN	Q	QN
0	X	X	↑	0	X	X	X	0	1
1	X	X	↑	0	X	X	X	1	0
X	X	X	↑	1	1	X	X	1	0
X	0	1	↑	1	0	X	X	0	1
X	1	1	↑	1	X	X	X	1	0
X	X	0	↑	1	0	0	1	0	1
X	X	0	↑	1	X	1	0	1	0

X = Don't care **Note: PD does not function while SD=0**

Capacitances

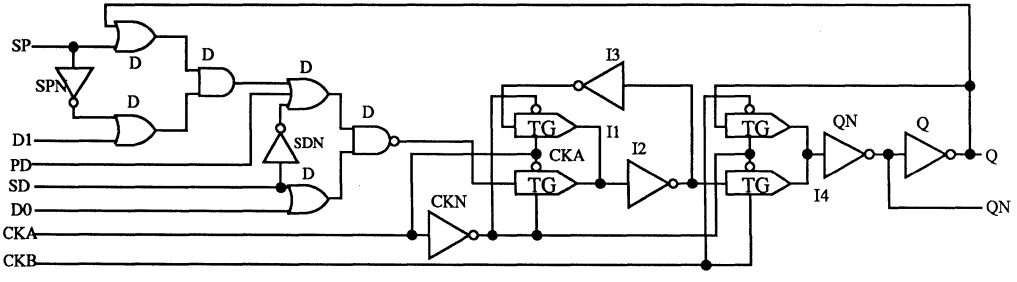
	D0	D1	SP	CKA	CKB	SD	PD
Area	0.027pF	0.027pF	0.057pF	0.057pF	0.029pF	0.055pF	0.027pF
Perf	0.102pF	0.102pF	0.207pF	0.065pF	0.033pF	0.206pF	0.102pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	1.73ns	1.10ns	CK ↑	Q ↓	7.93ns/pF	1.30ns	1.73ns/pF	1.04ns
D0 ↑	1.62ns	0.98ns	CK ↑	Q ↑	5.75ns/pF	1.89ns	1.44ns/pF	1.27ns
D1 ↓	2.83ns	1.62ns	CK ↑	QN ↓	1.98ns/pF	1.63ns	0.58ns/pF	1.10ns
D1 ↑	1.79ns	1.10ns	CK ↑	QN ↑	3.24ns/pF	1.04ns	0.66ns/pF	0.88ns
PD ↓	2.83ns	1.62ns						
PD ↑	1.56ns	0.92ns						
SD ↓	1.73ns	1.10ns						
SD ↑	3.24ns	1.85ns						
SP ↓	2.83ns	1.62ns						
SP ↑	3.24ns	1.85ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1P3MX

Positive edge triggered, data select front end, positive level sample, negative synchronous clear.

Grids 27, **Transistors** 38

Inputs
D0,D1,SP,CKA,CKB,SD,CDN

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	SP	CK	SD	CDN	Q	QN	Q	QN
0	X	X	↑	0	X	X	X	0	1
1	X	X	↑	0	X	X	X	1	0
X	X	X	↑	1	0	X	X	0	1
X	0	1	↑	1	X	X	X	0	1
X	1	1	↑	1	1	X	X	1	0
X	X	0	↑	1	X	0	1	0	1
X	X	0	↑	1	1	1	0	1	0

X = Don't care **Note: CDN does not function while SD=0**

Capacitances

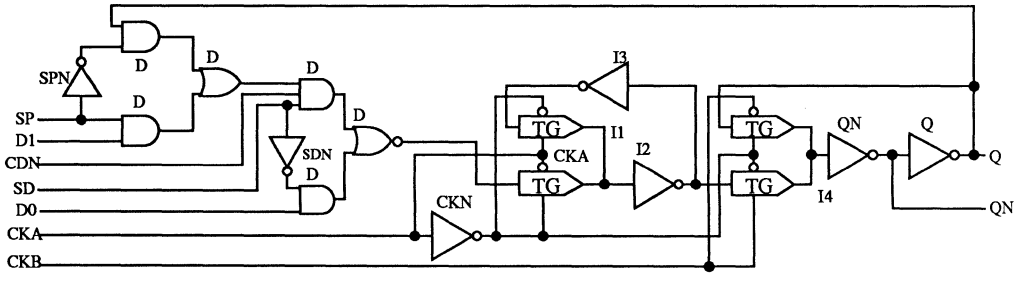
	D0	D1	SP	CKA	CKB	SD	CDN
Area	0.027pF	0.027pF	0.055pF	0.057pF	0.029pF	0.056pF	0.027pF
Perf	0.102pF	0.102pF	0.205pF	0.065pF	0.033pF	0.206pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	1.73ns	1.10ns	CK ↑	Q ↓	7.93ns/pF	1.30ns	1.73ns/pF	1.04ns
CDN ↑	2.31ns	1.44ns	CK ↑	Q ↑	5.81ns/pF	1.81ns	1.44ns/pF	1.27ns
D0 ↓	1.79ns	1.16ns	CK ↑	QN ↓	2.05ns/pF	1.54ns	0.58ns/pF	1.10ns
D0 ↑	1.73ns	1.10ns	CK ↑	QN ↑	3.24ns/pF	1.04ns	0.66ns/pF	0.88ns
D1 ↓	2.02ns	1.21ns						
D1 ↑	2.31ns	1.44ns						
SD ↓	1.73ns	1.10ns						
SD ↑	2.66ns	1.62ns						
SP ↓	2.25ns	1.50ns						
SP ↑	2.72ns	1.62ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2AX

Negative edge triggered, data select front end.

Grids 19, **Transistors** 30

Inputs
D0,D1,CKA,CKB,SD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D0	D1	CK	SD	Q	QN	Q	QN
0	X	↓	0	X	X	0	1
1	X	↓	0	X	X	1	0
X	0	↓	1	X	X	0	1
X	1	↓	1	X	X	1	0

X = Don't care

Capacitances

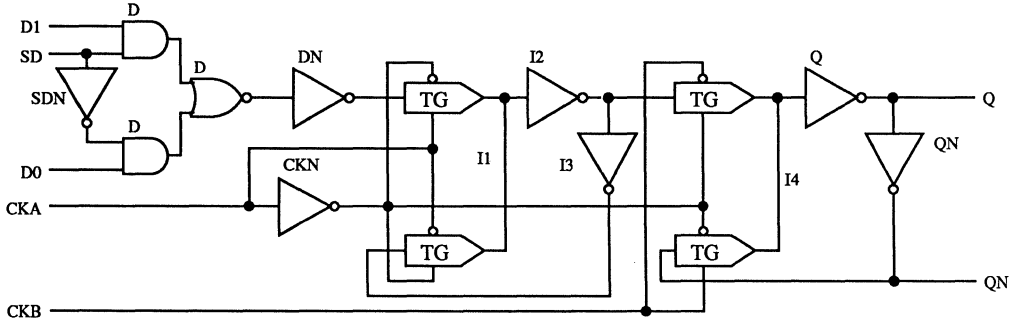
	D0	D1	CKA	CKB	SD
Area	0.027pF	0.029pF	0.057pF	0.028pF	0.054pF
Perf	0.102pF	0.104pF	0.065pF	0.032pF	0.204pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.39ns	1.04ns	CK ↓	Q ↓	2.05ns/pF	0.97ns	0.58ns/pF	0.92ns
D0 ↑	1.50ns	1.04ns	CK ↓	Q ↑	3.24ns/pF	0.92ns	0.66ns/pF	0.93ns
D1 ↓	1.27ns	0.92ns	CK ↓	QN ↓	7.93ns/pF	1.07ns	1.73ns/pF	1.04ns
D1 ↑	1.50ns	1.04ns	CK ↓	QN ↑	5.75ns/pF	1.14ns	1.44ns/pF	0.98ns
SD ↓	1.44ns	1.10ns						
SD ↑	1.73ns	1.21ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2BX

Negative edge triggered, data select front end, positive asynchronous preset.

Grids 22, **Transistors** 34

Inputs
D0,D1,CKA,CKB,SD,PD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	PD	Q	QN	Q	QN
X	X	X	X	1	X	X	1	0
0	X	↓	0	0	X	X	0	1
1	X	↓	0	X	X	X	1	0
X	0	↓	1	0	X	X	0	1
X	1	↓	1	X	X	X	1	0

X = Don't care

Capacitances

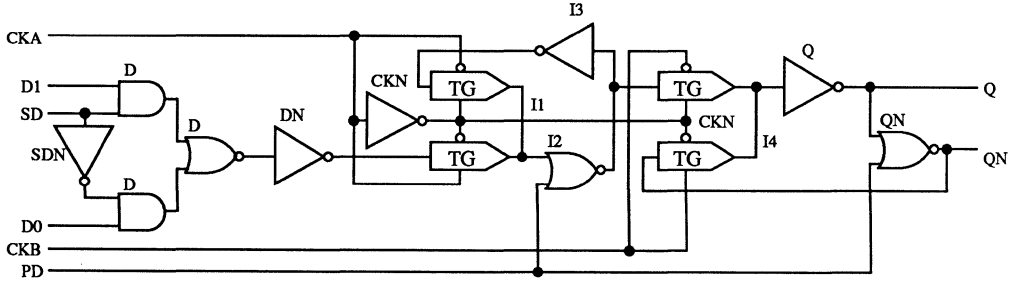
	D0	D1	CKA	CKB	SD	PD
Area	0.027pF	0.029pF	0.058pF	0.029pF	0.054pF	0.059pF
Perf	0.102pF	0.104pF	0.066pF	0.033pF	0.204pF	0.209pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.62ns	1.16ns	CK ↓	Q ↓	2.11ns/pF	1.23ns	0.58ns/pF	1.04ns
D0 ↑	1.50ns	1.04ns	CK ↓	Q ↑	3.24ns/pF	0.98ns	0.70ns/pF	0.91ns
D1 ↓	1.50ns	1.10ns	CK ↓	QN ↓	7.86ns/pF	1.16ns	1.73ns/pF	1.04ns
D1 ↑	1.56ns	1.04ns	CK ↓	QN ↑	8.85ns/pF	1.48ns	2.05ns/pF	1.19ns
SD ↓	1.56ns	1.16ns	PD ↑	Q ↑	6.01ns/pF	1.44ns	1.40ns/pF	0.78ns
SD ↑	2.02ns	1.39ns	PD ↑	QN ↓	2.31ns/pF	1.10ns	0.62ns/pF	0.32ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2CX

Negative edge triggered, data select front end, positive asynchronous clear, positive asynchronous preset.

Grids 28, **Transistors** 40

Inputs

D0,D1,CKA,CKB,SD,PDA,PDB,CD

Outputs

Q,QN

Capacitances

	D0	D1	CKA	CKB	SD	PDA	PDB	CD
Area	0.027pF	0.029pF	0.060pF	0.028pF	0.056pF	0.027pF	0.027pF	0.027pF
Perf	0.103pF	0.104pF	0.069pF	0.032pF	0.206pF	0.102pF	0.102pF	0.102pF

Truth Table

INPUTS						OUTPUTS OLD		OUTPUTS NEW	
D0	D1	CK	SD	PD	CD	Q	QN	Q	QN
X	X	X	X	X	1	X	X	0	1
X	X	X	X	1	0	X	X	1	0
0	X	↓	0	0	X	X	X	0	1
1	X	↓	0	X	0	X	X	1	0
X	0	↓	1	0	X	X	X	0	1
X	1	↓	1	X	0	X	X	1	0

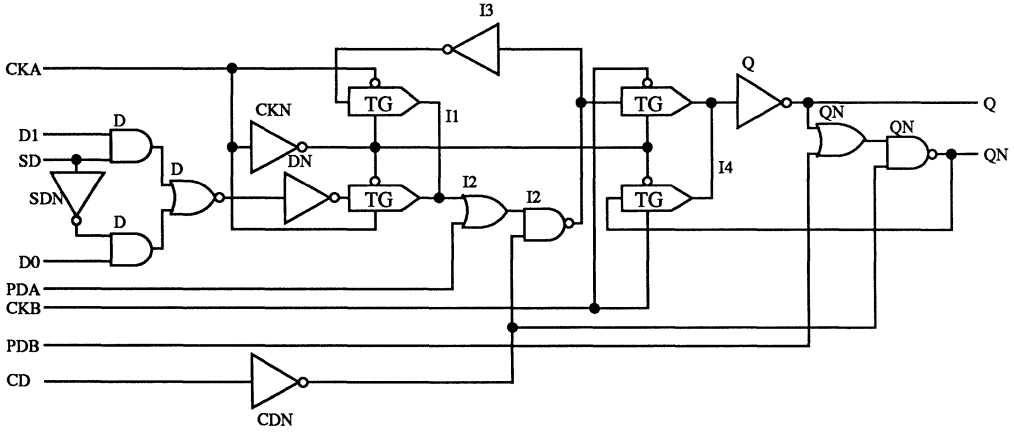
X = Don't care

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
D0 ↓	1.68ns	1.27ns	CD ↑	Q ↓	7.93ns/pF	1.59ns	1.77ns/pF	1.02ns
D0 ↑	1.68ns	1.21ns	CD ↑	QN ↑	3.24ns/pF	1.10ns	0.70ns/pF	0.56ns
D1 ↓	1.56ns	1.16ns	CK ↓	Q ↓	2.18ns/pF	1.21ns	0.58ns/pF	1.04ns
D1 ↑	1.68ns	1.21ns	CK ↓	Q ↑	3.24ns/pF	1.10ns	0.70ns/pF	0.97ns
SD ↓	1.62ns	1.27ns	CK ↓	QN ↓	9.38ns/pF	1.34ns	2.14ns/pF	1.14ns
SD ↑	2.02ns	1.44ns	CK ↓	QN ↑	8.79ns/pF	1.62ns	2.05ns/pF	1.19ns
			PD ↑	Q ↑	8.26ns/pF	1.64ns	2.05ns/pF	0.84ns
			PD ↑	QN ↓	4.03ns/pF	1.26ns	1.07ns/pF	0.45ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2DX

Negative edge triggered, data select front end, positive asynchronous clear.

Grids 22, **Transistors** 32

Inputs
D0,D1,CKA,CKB,SD,CD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	CD	Q	QN	Q	QN
X	X	X	X	1	X	X	0	1
0	X	↓	0	X	X	X	0	1
1	X	↓	0	0	X	X	1	0
X	0	↓	1	X	X	X	0	1
X	1	↓	1	0	X	X	1	0

X = Don't care

Capacitances

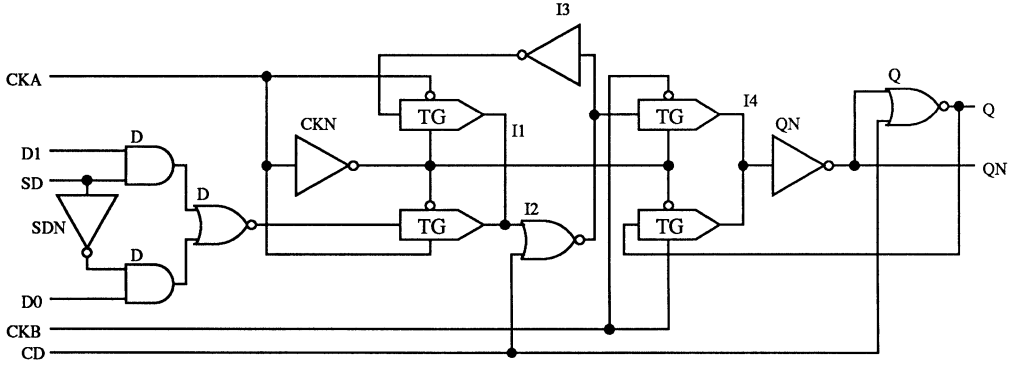
	D0	D1	CKA	CKB	SD	CD
Area	0.027pF	0.029pF	0.057pF	0.029pF	0.055pF	0.059pF
Perf	0.103pF	0.104pF	0.065pF	0.033pF	0.206pF	0.209pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.56ns	0.92ns	CD ↑	Q ↓	2.31ns/pF	1.10ns	0.62ns/pF	0.32ns
D0 ↑	1.79ns	1.10ns	CD ↑	QN ↑	6.01ns/pF	1.44ns	1.40ns/pF	0.78ns
D1 ↓	1.33ns	0.87ns	CK ↓	Q ↓	7.86ns/pF	1.16ns	1.73ns/pF	1.04ns
D1 ↑	1.79ns	1.10ns	CK ↓	Q ↑	8.85ns/pF	1.48ns	2.05ns/pF	1.19ns
SD ↓	1.62ns	1.16ns	CK ↓	QN ↓	2.11ns/pF	1.23ns	0.62ns/pF	0.96ns
SD ↑	1.91ns	1.16ns	CK ↓	QN ↑	3.24ns/pF	0.98ns	0.66ns/pF	0.93ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2EX

Negative edge triggered, data select front end, negative asynchronous clear.

Grids 22, **Transistors** 34

Inputs
D0,D1,CKA,CKB,SD,CDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	CDN	Q	QN	Q	QN
X	X	X	X	0	X	X	0	1
0	X	↓	0	X	X	X	0	1
1	X	↓	0	1	X	X	1	0
X	0	↓	1	X	X	X	0	1
X	1	↓	1	1	X	X	1	0

X = Don't care

Capacitances

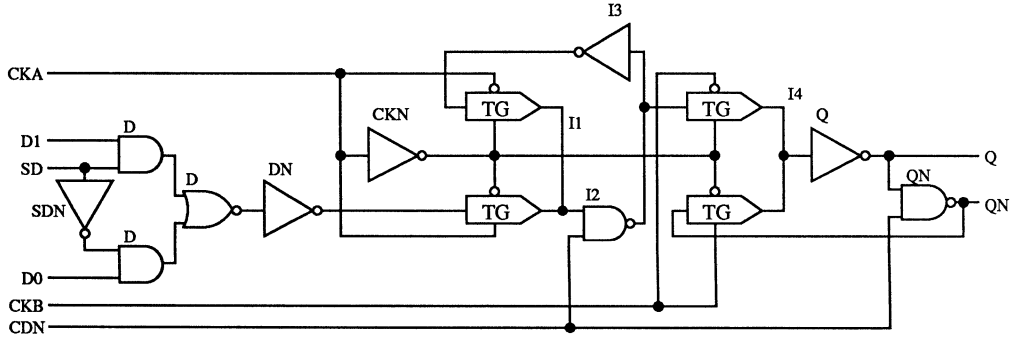
	D0	D1	CKA	CKB	SD	CDN
Area	0.027pF	0.029pF	0.058pF	0.028pF	0.054pF	0.057pF
Perf	0.102pF	0.104pF	0.066pF	0.032pF	0.204pF	0.208pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.44ns	1.04ns	CDN ↓	Q ↓	7.99ns/pF	0.93ns	1.77ns/pF	0.73ns
D0 ↑	1.62ns	1.16ns	CDN ↓	QN ↑	3.24ns/pF	0.52ns	0.70ns/pF	0.21ns
D1 ↓	1.27ns	0.92ns	CK ↓	Q ↓	2.05ns/pF	1.02ns	0.58ns/pF	0.92ns
D1 ↑	1.62ns	1.16ns	CK ↓	Q ↑	3.24ns/pF	1.10ns	0.70ns/pF	0.97ns
SD ↓	1.62ns	1.21ns	CK ↓	QN ↓	9.38ns/pF	1.34ns	2.14ns/pF	1.14ns
SD ↑	1.79ns	1.21ns	CK ↓	QN ↑	5.75ns/pF	1.20ns	1.40ns/pF	1.07ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2FX

Negative edge triggered, data select front end, negative asynchronous clear, positive asynchronous preset.

Grids 25, **Transistors** 38

Inputs
D0,D1,CKA,CKB,SD,PDA,PDB,CDN

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS OLD		OUTPUTS NEW	
D0	D1	CK	SD	PD	CDN	Q	QN	Q	QN
X	X	X	X	X	0	X	X	0	1
X	X	X	X	1	1	X	X	1	0
0	X	↓	0	0	X	X	X	0	1
1	X	↓	0	X	1	X	X	1	0
X	0	↓	1	0	X	X	X	0	1
X	1	↓	1	X	1	X	X	1	0

X = Don't care

Capacitances

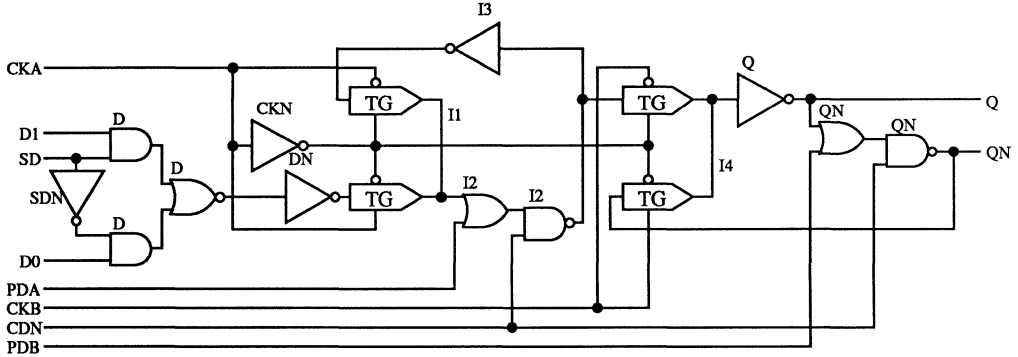
	D0	D1	CKA	CKB	SD	PDA	PDB	CDN
Area	0.027pF	0.029pF	0.057pF	0.028pF	0.056pF	0.027pF	0.027pF	0.057pF
Perf	0.102pF	0.104pF	0.065pF	0.032pF	0.206pF	0.102pF	0.103pF	0.207pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
D0 ↓	1.68ns	1.27ns	CDN ↓	Q ↓	7.93ns/pF	1.07ns	1.77ns/pF	0.78ns
D0 ↑	1.68ns	1.21ns	CDN ↓	QN ↑	3.24ns/pF	0.58ns	0.70ns/pF	0.27ns
D1 ↓	1.56ns	1.16ns	CK ↓	Q ↓	2.11ns/pF	1.29ns	0.58ns/pF	1.04ns
D1 ↑	1.68ns	1.21ns	CK ↓	Q ↑	3.24ns/pF	1.10ns	0.70ns/pF	0.97ns
SD ↓	1.62ns	1.27ns	CK ↓	QN ↓	9.38ns/pF	1.34ns	2.14ns/pF	1.20ns
SD ↑	2.02ns	1.44ns	CK ↓	QN ↑	8.79ns/pF	1.68ns	2.05ns/pF	1.25ns
			PD ↑	Q ↑	8.32ns/pF	1.62ns	2.05ns/pF	0.90ns
			PD ↑	QN ↓	4.03ns/pF	1.26ns	1.07ns/pF	0.45ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2GX

Negative edge triggered, data select front end, negative asynchronous preset.

Grids 22, **Transistors** 32

Inputs
D0,D1,CKA,CKB,SD,PDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	PDN	Q	QN	Q	QN
X	X	X	X	0	X	X	1	0
0	X	↓	0	1	X	X	0	1
1	X	↓	0	X	X	X	1	0
X	0	↓	1	1	X	X	0	1
X	1	↓	1	X	X	X	1	0

X = Don't care

Capacitances

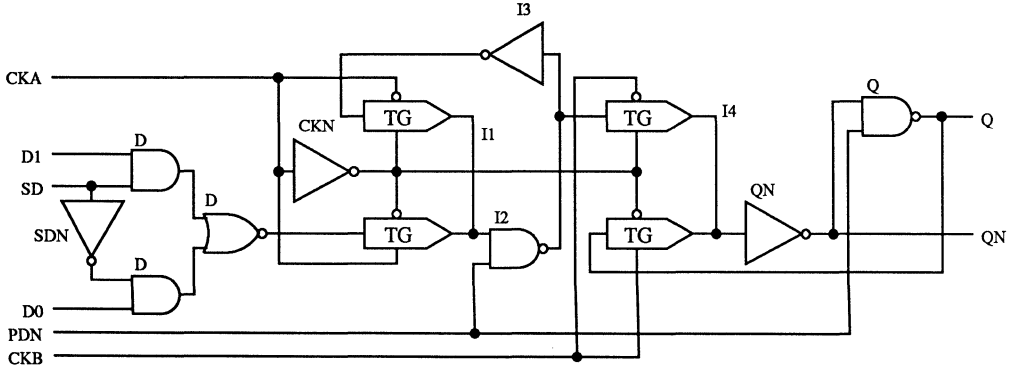
	D0	D1	CKA	CKB	SD	PDN
Area	0.027pF	0.029pF	0.057pF	0.028pF	0.055pF	0.057pF
Perf	0.103pF	0.104pF	0.065pF	0.032pF	0.206pF	0.208pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	1.68ns	1.04ns	CK ↓	Q ↓	9.38ns/pF	1.34ns	2.14ns/pF	1.14ns
D0 ↑	1.56ns	0.92ns	CK ↓	Q ↑	5.75ns/pF	1.20ns	1.40ns/pF	1.07ns
D1 ↓	1.44ns	0.98ns	CK ↓	QN ↓	2.05ns/pF	1.02ns	0.58ns/pF	0.92ns
D1 ↑	1.56ns	0.92ns	CK ↓	QN ↑	3.24ns/pF	1.10ns	0.66ns/pF	0.99ns
SD ↓	1.62ns	1.04ns	PDN ↓	Q ↑	3.24ns/pF	0.52ns	0.70ns/pF	0.21ns
SD ↑	2.02ns	1.27ns	PDN ↓	QN ↓	7.99ns/pF	0.93ns	1.77ns/pF	0.73ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2IX

Negative edge triggered, data select front end, positive synchronous clear.

Grids 23, **Transistors** 32

Inputs
D0,D1,CKA,CKB,SD,CD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	CD	Q	QN	Q	QN
X	X	↓	1	1	X	X	0	1
0	X	↓	0	X	X	X	0	1
1	X	↓	0	X	X	X	1	0
X	0	↓	1	X	X	X	0	1
X	1	↓	1	0	X	X	1	0

X = Don't care **Note: CD does not function while SD=0**

Capacitances

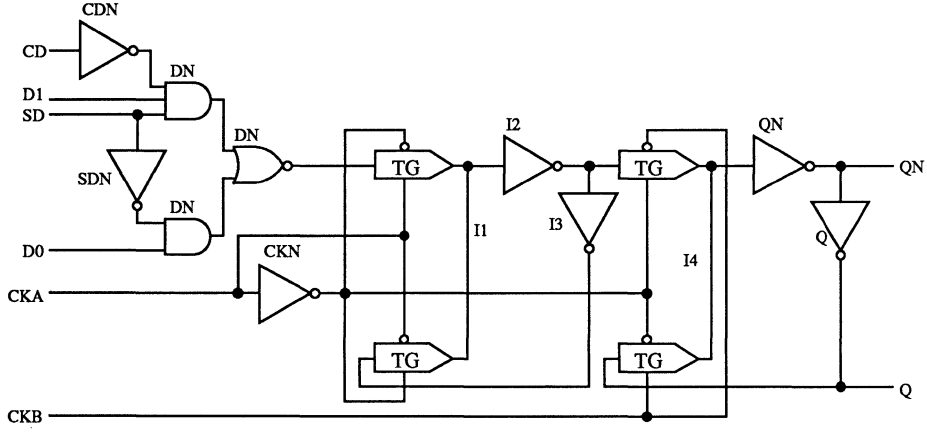
	D0	D1	CKA	CKB	SD	CD
Area	0.027pF	0.027pF	0.057pF	0.028pF	0.057pF	0.027pF
Perf	0.102pF	0.102pF	0.065pF	0.032pF	0.207pF	0.102pF

Delay Information

Input Signal	Setup Time		From	To	Propagation Delay			
					Area		Performance	
Name	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CD ↓	1.62ns	1.16ns	CK ↓	Q ↓	7.93ns/pF	1.13ns	1.73ns/pF	1.04ns
CD ↑	1.91ns	1.16ns	CK ↓	Q ↑	5.75ns/pF	1.26ns	1.44ns/pF	1.04ns
D0 ↓	1.56ns	0.98ns	CK ↓	QN ↓	1.98ns/pF	1.16ns	0.58ns/pF	0.98ns
D0 ↑	1.56ns	0.92ns	CK ↓	QN ↑	3.24ns/pF	0.98ns	0.70ns/pF	0.91ns
D1 ↓	1.33ns	0.87ns						
D1 ↑	1.85ns	1.10ns						
SD ↓	1.50ns	1.04ns						
SD ↑	1.91ns	1.16ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2JX

Negative edge triggered, data select front end, positive synchronous preset.

Grids 21, **Transistors** 30

Inputs
D0,D1,CKA,CKB,SD,PD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	PD	Q	QN	Q	QN
X	X	↓	1	1	X	X	1	0
0	X	↓	0	X	X	X	0	1
1	X	↓	0	X	X	X	1	0
X	0	↓	1	0	X	X	0	1
X	1	↓	1	X	X	X	1	0

X = Don't care **Note: PD does not function while SD=0**

Capacitances

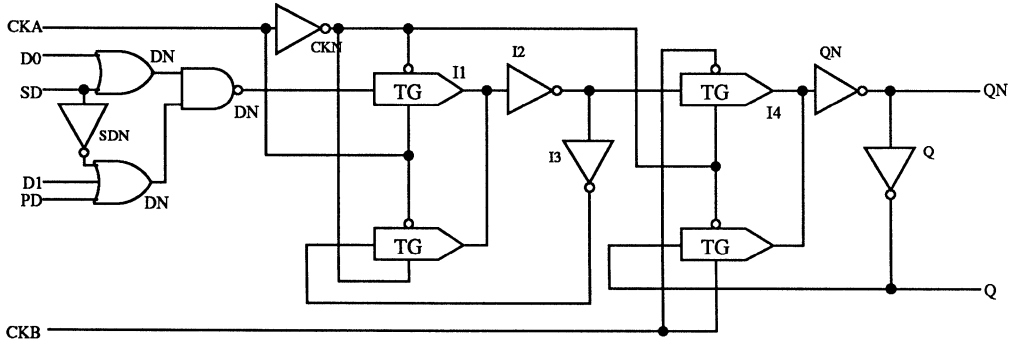
	D0	D1	CKA	CKB	SD	PD
Area	0.027pF	0.027pF	0.057pF	0.028pF	0.056pF	0.027pF
Perf	0.102pF	0.102pF	0.065pF	0.032pF	0.206pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.56ns	0.98ns	CK ↓	Q ↓	7.93ns/pF	1.13ns	1.73ns/pF	1.04ns
D0 ↑	1.44ns	0.87ns	CK ↓	Q ↑	5.75ns/pF	1.26ns	1.44ns/pF	1.04ns
D1 ↓	2.02ns	1.16ns	CK ↓	QN ↓	1.98ns/pF	1.16ns	0.58ns/pF	0.98ns
D1 ↑	1.50ns	0.92ns	CK ↓	QN ↑	3.24ns/pF	0.98ns	0.70ns/pF	0.91ns
PD ↓	2.02ns	1.21ns						
PD ↑	1.39ns	0.87ns						
SD ↓	1.56ns	1.04ns						
SD ↑	2.37ns	1.39ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2KX

Negative edge triggered, data select front end, negative asynchronous clear, negative asynchronous preset.

Grids 27, **Transistors** 38

Inputs
D0,D1,CKA,CKB,SD,PDNA,PDNB,CDN

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS OLD		OUTPUTS NEW	
D0	D1	CK	SD	PDN	CDN	Q	QN	Q	QN
X	X	X	X	X	0	X	X	0	1
X	X	X	X	0	1	X	X	1	0
0	X	↓	0	1	X	X	X	0	1
1	X	↓	0	X	1	X	X	1	0
X	0	↓	1	1	X	X	X	0	1
X	1	↓	1	X	1	X	X	1	0

X = Don't care

Capacitances

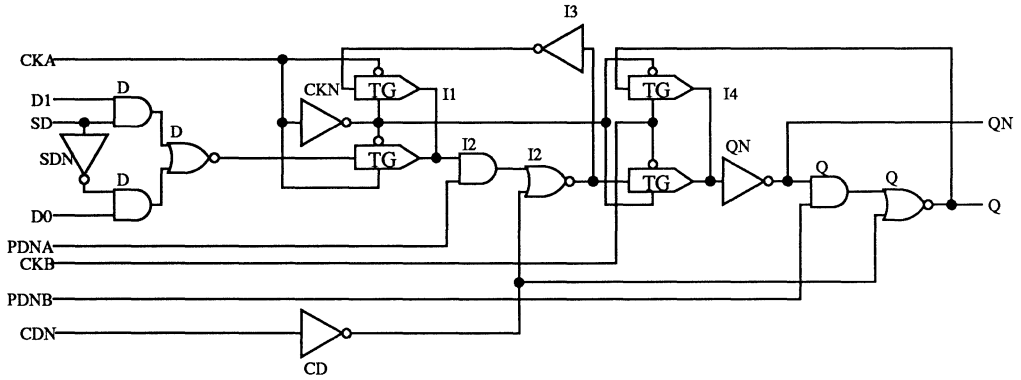
	D0	D1	CKA	CKB	SD	PDNA	PDNB	CDN
Area	0.027pF	0.029pF	0.057pF	0.029pF	0.056pF	0.027pF	0.027pF	0.027pF
Perf	0.103pF	0.104pF	0.065pF	0.033pF	0.206pF	0.102pF	0.102pF	0.102pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	1.73ns	1.10ns	CDN ↓	Q ↓	2.05ns/pF	0.91ns	0.53ns/pF	0.54ns
D0 ↑	1.79ns	1.10ns	CDN ↓	QN ↑	5.75ns/pF	1.26ns	1.36ns/pF	0.97ns
D1 ↓	1.50ns	1.04ns	CK ↓	Q ↓	9.38ns/pF	1.34ns	2.14ns/pF	1.14ns
D1 ↑	1.85ns	1.16ns	CK ↓	Q ↑	8.79ns/pF	1.68ns	2.05ns/pF	1.19ns
SD ↓	1.68ns	1.21ns	CK ↓	QN ↓	2.18ns/pF	1.26ns	0.58ns/pF	1.04ns
SD ↑	2.08ns	1.33ns	CK ↓	QN ↑	3.24ns/pF	1.10ns	0.70ns/pF	0.97ns
			PDN ↓	Q ↑	6.47ns/pF	0.81ns	1.36ns/pF	0.40ns
			PDN ↓	QN ↓	12.75ns/pF	1.46ns	2.79ns/pF	0.86ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



7

Static D-Type Flip-Flop

FL1S2LX

Negative edge triggered, data select front end, negative synchronous preset.

Grids 23, **Transistors** 32

Inputs
D0,D1,CKA,CKB,SD,PDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	PDN	Q	QN	Q	QN
X	X	↓	1	0	X	X	1	0
0	X	↓	0	X	X	X	0	1
1	X	↓	0	X	X	X	1	0
X	0	↓	1	1	X	X	0	1
X	1	↓	1	X	X	X	1	0

X = Don't care **Note: PDN does not function while SD=0**

Capacitances

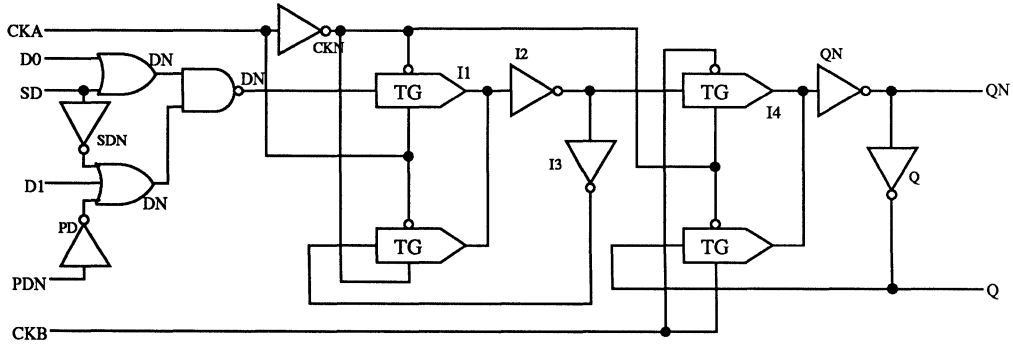
	D0	D1	CKA	CKB	SD	PDN
Area	0.027pF	0.027pF	0.057pF	0.028pF	0.056pF	0.027pF
Perf	0.102pF	0.102pF	0.065pF	0.032pF	0.206pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.56ns	0.98ns	CK ↓	Q ↓	7.93ns/pF	1.13ns	1.73ns/pF	1.04ns
D0 ↑	1.44ns	0.87ns	CK ↓	Q ↑	5.75ns/pF	1.26ns	1.44ns/pF	1.04ns
D1 ↓	2.02ns	1.16ns	CK ↓	QN ↓	1.98ns/pF	1.16ns	0.58ns/pF	0.98ns
D1 ↑	1.50ns	0.92ns	CK ↓	QN ↑	3.24ns/pF	0.98ns	0.70ns/pF	0.91ns
PDN ↓	1.27ns	0.92ns						
PDN ↑	2.37ns	1.39ns						
SD ↓	1.56ns	1.04ns						
SD ↑	2.37ns	1.39ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2MX

Negative edge triggered, data select front end, negative synchronous clear.

Grids 20, **Transistors** 30

Inputs
D0,D1,CKA,CKB,SD,CDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	CDN	Q	QN	Q	QN
X	X	↓	1	0	X	X	0	1
0	X	↓	0	X	X	X	0	1
1	X	↓	0	X	X	X	1	0
X	0	↓	1	X	X	X	0	1
X	1	↓	1	1	X	X	1	0

X = Don't care **Note: CDN does not function while SD=0**

Capacitances

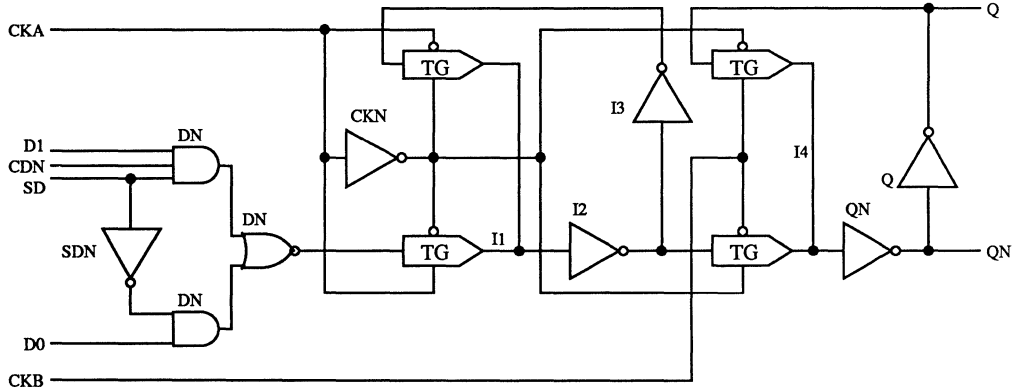
	D0	D1	CKA	CKB	SD	CDN
Area	0.027pF	0.027pF	0.057pF	0.028pF	0.057pF	0.027pF
Perf	0.102pF	0.102pF	0.065pF	0.032pF	0.207pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	1.50ns	0.98ns	CK ↓	Q ↓	7.93ns/pF	1.07ns	1.73ns/pF	0.98ns
CDN ↑	1.79ns	1.10ns	CK ↓	Q ↑	5.75ns/pF	1.14ns	1.44ns/pF	0.98ns
D0 ↓	1.56ns	0.98ns	CK ↓	QN ↓	2.05ns/pF	0.97ns	0.58ns/pF	0.92ns
D0 ↑	1.56ns	0.92ns	CK ↓	QN ↑	3.24ns/pF	0.92ns	0.66ns/pF	0.93ns
D1 ↓	1.33ns	0.87ns						
D1 ↑	1.79ns	1.10ns						
SD ↓	1.50ns	1.04ns						
SD ↑	1.85ns	1.21ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2NX

Negative edge triggered, data select front end, positive asynchronous clear, negative asynchronous preset.

Grids 25, **Transistors** 36

Inputs
D0,D1,CKA,CKB,SD,PDNA,PDNB,CD

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	CK	SD	PDN	CD	Q	QN	Q	QN
X	X	X	X	X	1	X	X	0	1
X	X	X	X	0	0	X	X	1	0
0	X	↓	0	1	X	X	X	0	1
1	X	↓	0	X	0	X	X	1	0
X	0	↓	1	1	X	X	X	0	1
X	1	↓	1	X	0	X	X	1	0

X = Don't care

Capacitances

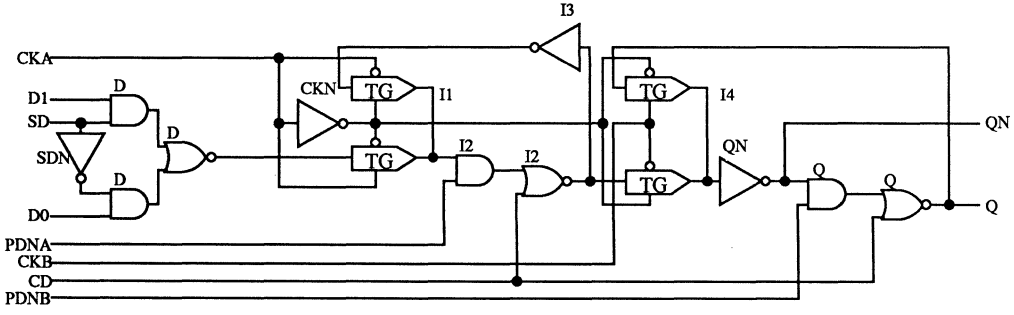
	D0	D1	CKA	CKB	SD	PDNA	PDNB	CD
Area	0.027pF	0.029pF	0.057pF	0.029pF	0.056pF	0.027pF	0.027pF	0.057pF
Perf	0.103pF	0.104pF	0.065pF	0.033pF	0.206pF	0.102pF	0.103pF	0.207pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
D0 ↓	1.73ns	1.10ns	CD ↑	Q ↓	2.25ns/pF	1.18ns	0.58ns/pF	0.40ns
D0 ↑	1.85ns	1.16ns	CD ↑	QN ↑	6.01ns/pF	1.50ns	1.40ns/pF	0.83ns
D1 ↓	1.50ns	1.04ns	CK ↓	Q ↓	9.31ns/pF	1.42ns	2.14ns/pF	1.20ns
D1 ↑	1.85ns	1.16ns	CK ↓	Q ↑	8.85ns/pF	1.65ns	2.05ns/pF	1.25ns
SD ↓	1.68ns	1.21ns	CK ↓	QN ↓	2.11ns/pF	1.35ns	0.58ns/pF	1.04ns
SD ↑	2.08ns	1.33ns	CK ↓	QN ↑	3.24ns/pF	1.10ns	0.70ns/pF	0.97ns
			PDN ↓	Q ↑	6.47ns/pF	0.81ns	1.36ns/pF	0.45ns
			PDN ↓	QN ↓	12.75ns/pF	1.46ns	2.75ns/pF	1.00ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S2OX

Negative edge triggered, data select front end, positive synchronous clear, positive synchronous preset.

Grids 24, **Transistors** 34

Inputs

D0,D1,CKA,CKB,SD,PD,CD

Outputs

Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	CK	SD	PD	CD	Q	QN	Q	QN
0	X	↓	0	X	X	X	X	0	1
1	X	↓	0	X	X	X	X	1	0
X	X	↓	1	X	1	X	X	0	1
X	X	↓	1	1	0	X	X	1	0
X	0	↓	1	0	X	X	X	0	1
X	1	↓	1	X	0	X	X	1	0

X = Don't care **Note: PD/CD do not function while SD=0**

Capacitances

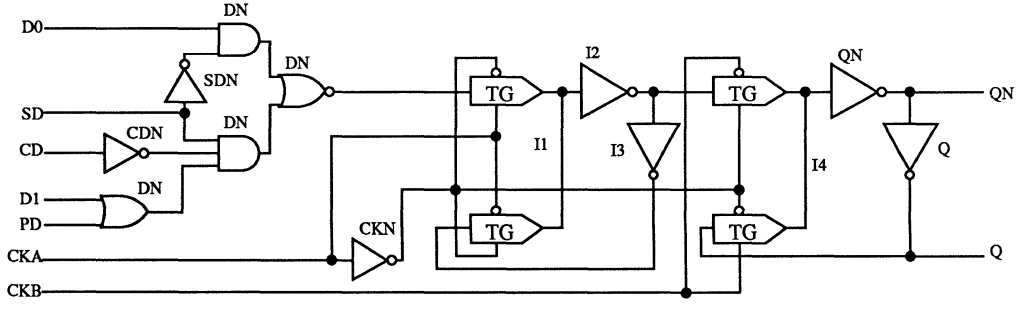
	D0	D1	CKA	CKB	SD	PD	CD
Area	0.027pF	0.027pF	0.057pF	0.028pF	0.057pF	0.027pF	0.027pF
Perf	0.102pF	0.102pF	0.065pF	0.032pF	0.207pF	0.102pF	0.102pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
CD ↓	1.68ns	1.21ns	CK ↓	Q ↓	7.93ns/pF	1.13ns	1.73ns/pF	1.04ns
CD ↑	1.97ns	1.21ns	CK ↓	Q ↑	5.75ns/pF	1.26ns	1.44ns/pF	1.04ns
D0 ↓	1.62ns	0.98ns	CK ↓	QN ↓	1.98ns/pF	1.16ns	0.58ns/pF	0.98ns
D0 ↑	1.62ns	0.98ns	CK ↓	QN ↑	3.24ns/pF	0.98ns	0.70ns/pF	0.91ns
D1 ↓	1.85ns	1.10ns						
D1 ↑	1.85ns	1.16ns						
PD ↓	2.08ns	1.21ns						
PD ↑	1.79ns	1.10ns						
SD ↓	1.56ns	1.04ns						
SD ↑	2.37ns	1.44ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3AX

Positive edge triggered, data select front end.

Grids 19, **Transistors** 30

Inputs
D0,D1,CKA,CKB,SD

Outputs
Q,QN

Truth Table

INPUTS				OUTPUTS			
				OLD		NEW	
D0	D1	CK	SD	Q	QN	Q	QN
0	X	↑	0	X	X	0	1
1	X	↑	0	X	X	1	0
X	0	↑	1	X	X	0	1
X	1	↑	1	X	X	1	0

X = Don't care

Capacitances

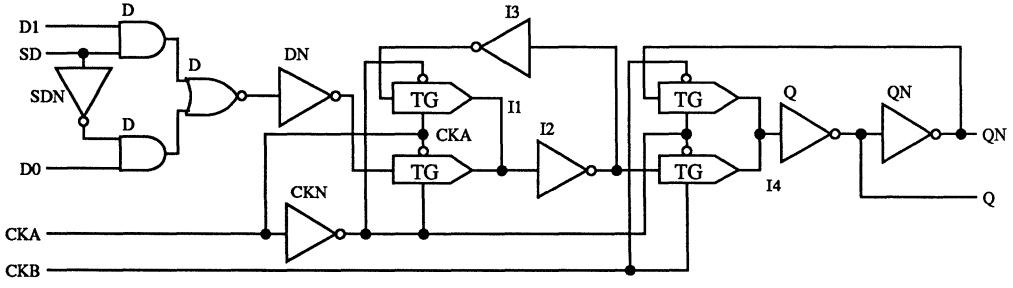
	D0	D1	CKA	CKB	SD
Area	0.027pF	0.029pF	0.057pF	0.028pF	0.054pF
Perf	0.102pF	0.104pF	0.065pF	0.032pF	0.204pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.39ns	1.04ns	CK ↑	Q ↓	1.98ns/pF	1.51ns	0.58ns/pF	1.10ns
D0 ↑	1.50ns	1.04ns	CK ↑	Q ↑	3.24ns/pF	0.92ns	0.70ns/pF	0.79ns
D1 ↓	1.27ns	0.92ns	CK ↑	QN ↓	7.93ns/pF	1.07ns	1.73ns/pF	0.92ns
D1 ↑	1.50ns	1.04ns	CK ↑	QN ↑	5.75ns/pF	1.60ns	1.44ns/pF	1.16ns
SD ↓	1.44ns	1.10ns						
SD ↑	1.73ns	1.21ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3BX

Positive edge triggered, data select front end, positive asynchronous preset.

Grids 22, **Transistors** 34

Inputs
D0,D1,CKA,CKB,SD,PD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	PD	Q	QN	Q	QN
X	X	X	X	1	X	X	1	0
0	X	↑	0	0	X	X	0	1
1	X	↑	0	X	X	X	1	0
X	0	↑	1	0	X	X	0	1
X	1	↑	1	X	X	X	1	0

X = Don't care

Capacitances

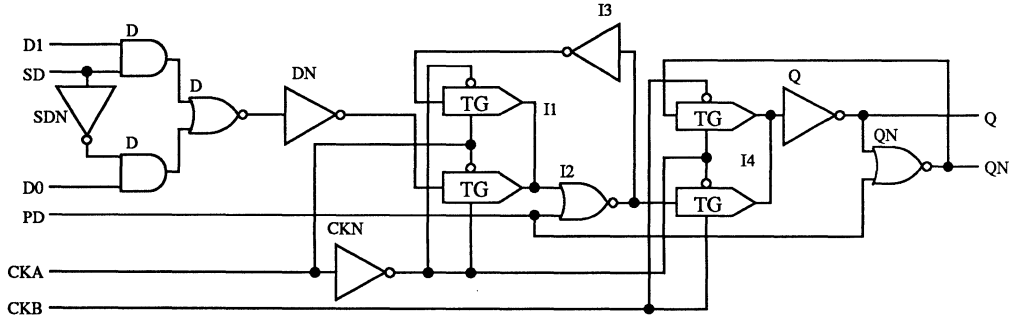
	D0	D1	CKA	CKB	SD	PD
Area	0.027pF	0.029pF	0.058pF	0.028pF	0.054pF	0.058pF
Perf	0.102pF	0.104pF	0.066pF	0.032pF	0.204pF	0.208pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.62ns	1.16ns	CK ↑	Q ↓	2.18ns/pF	1.73ns	0.62ns/pF	1.13ns
D0 ↑	1.50ns	1.04ns	CK ↑	Q ↑	3.24ns/pF	0.92ns	0.70ns/pF	0.79ns
D1 ↓	1.50ns	1.10ns	CK ↑	QN ↓	7.93ns/pF	1.07ns	1.73ns/pF	0.92ns
D1 ↑	1.56ns	1.04ns	CK ↑	QN ↑	8.85ns/pF	2.00ns	2.01ns/pF	1.39ns
SD ↓	1.56ns	1.16ns	PD ↑	Q ↑	6.01ns/pF	1.44ns	1.40ns/pF	0.78ns
SD ↑	2.02ns	1.39ns	PD ↑	QN ↓	2.31ns/pF	1.10ns	0.62ns/pF	0.32ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3CX

Positive edge triggered, data select front end, positive asynchronous clear, positive asynchronous preset.

Grids 28, **Transistors** 40

Inputs
D0,D1,CKA,CKB,SD,PDA,PDB,CD

Outputs
Q,QN

Capacitances

Truth Table

INPUTS						OUTPUTS OLD		OUTPUTS NEW	
D0	D1	CK	SD	PD	CD	Q	QN	Q	QN
X	X	X	X	X	1	X	X	0	1
X	X	X	X	1	0	X	X	1	0
0	X	↑	0	0	X	X	X	0	1
1	X	↑	0	X	0	X	X	1	0
X	0	↑	1	0	X	X	X	0	1
X	1	↑	1	X	0	X	X	1	0

X = Don't care

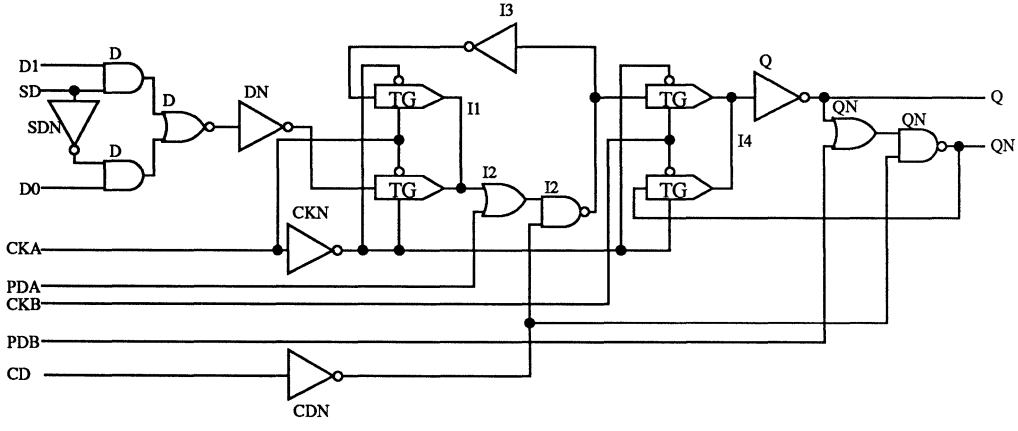
	D0	D1	CKA	CKB	SD	PDA	PDB	CD
Area	0.027pF	0.029pF	0.061pF	0.029pF	0.056pF	0.027pF	0.027pF	0.027pF
Perf	0.103pF	0.104pF	0.070pF	0.033pF	0.206pF	0.102pF	0.102pF	0.102pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	1.68ns	1.27ns	CD ↑	Q ↓	7.93ns/pF	1.59ns	1.77ns/pF	1.02ns
D0 ↑	1.68ns	1.21ns	CD ↑	QN ↑	3.24ns/pF	1.10ns	0.70ns/pF	0.56ns
D1 ↓	1.56ns	1.16ns	CK ↑	Q ↓	2.18ns/pF	1.78ns	0.62ns/pF	1.13ns
D1 ↑	1.68ns	1.21ns	CK ↑	Q ↑	3.24ns/pF	1.10ns	0.70ns/pF	0.85ns
SD ↓	1.62ns	1.27ns	CK ↑	QN ↓	9.38ns/pF	1.40ns	2.10ns/pF	1.11ns
SD ↑	2.02ns	1.44ns	CK ↑	QN ↑	8.79ns/pF	2.14ns	2.05ns/pF	1.36ns
			PD ↑	Q ↑	8.32ns/pF	1.62ns	2.05ns/pF	0.84ns
			PD ↑	QN ↓	4.03ns/pF	1.26ns	1.07ns/pF	0.45ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3DX

Positive edge triggered, data select front end, positive asynchronous clear.

Grids 22, **Transistors** 32

Inputs
D0,D1,CKA,CKB,SD,CD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	CD	Q	QN	Q	QN
X	X	X	X	1	X	X	0	1
0	X	↑	0	X	X	X	0	1
1	X	↑	0	0	X	X	1	0
X	0	↑	1	X	X	X	0	1
X	1	↑	1	0	X	X	1	0

X = Don't care

Capacitances

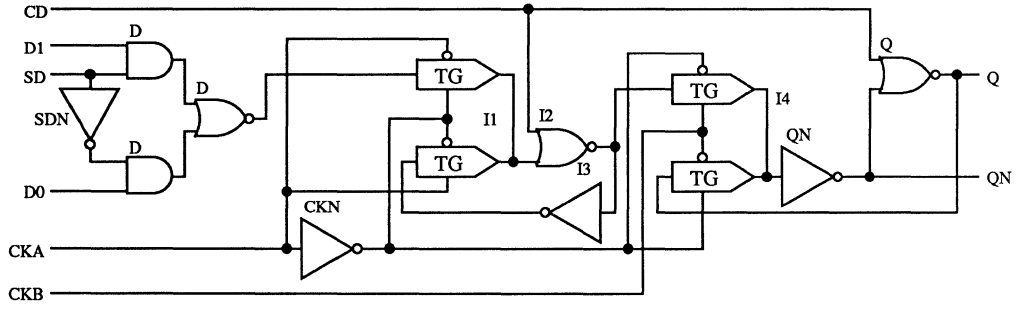
	D0	D1	CKA	CKB	SD	CD
Area	0.027pF	0.029pF	0.057pF	0.028pF	0.055pF	0.057pF
Perf	0.103pF	0.104pF	0.065pF	0.032pF	0.206pF	0.208pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	1.56ns	0.92ns	CD ↑	Q ↓	2.31ns/pF	1.10ns	0.62ns/pF	0.32ns
D0 ↑	1.79ns	1.10ns	CD ↑	QN ↑	6.01ns/pF	1.44ns	1.40ns/pF	0.78ns
D1 ↓	1.33ns	0.87ns	CK ↑	Q ↓	7.93ns/pF	1.07ns	1.73ns/pF	0.92ns
D1 ↑	1.79ns	1.10ns	CK ↑	Q ↑	8.85ns/pF	2.00ns	2.05ns/pF	1.30ns
SD ↓	1.62ns	1.16ns	CK ↑	QN ↓	2.18ns/pF	1.73ns	0.62ns/pF	1.13ns
SD ↑	1.91ns	1.16ns	CK ↑	QN ↑	3.24ns/pF	0.92ns	0.70ns/pF	0.79ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3EX

Positive edge triggered, data select front end, negative asynchronous clear.

Grids 22, **Transistors** 34

Inputs
D0,D1,CKA,CKB,SD,CDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	CDN	Q	QN	Q	QN
X	X	X	X	0	X	X	0	1
0	X	↑	0	X	X	X	0	1
1	X	↑	0	1	X	X	1	0
X	0	↑	1	X	X	X	0	1
X	1	↑	1	1	X	X	1	0

X = Don't care

Capacitances

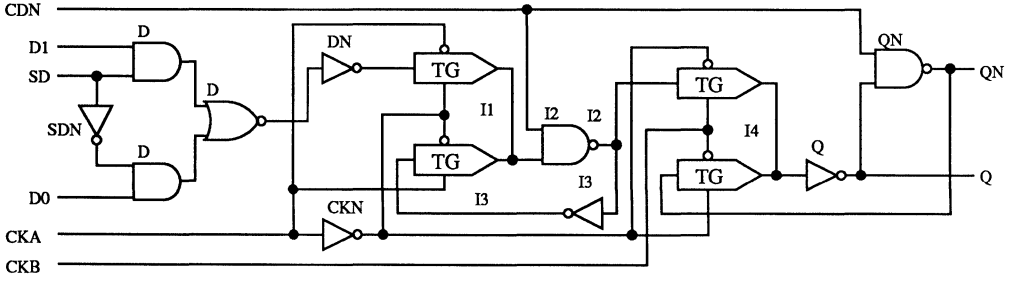
	D0	D1	CKA	CKB	SD	CDN
Area	0.027pF	0.029pF	0.058pF	0.029pF	0.054pF	0.059pF
Perf	0.102pF	0.104pF	0.066pF	0.033pF	0.204pF	0.209pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.44ns	1.04ns	CDN ↓	Q ↓	7.99ns/pF	0.93ns	1.77ns/pF	0.73ns
D0 ↑	1.62ns	1.16ns	CDN ↓	QN ↑	3.24ns/pF	0.52ns	0.70ns/pF	0.21ns
D1 ↓	1.27ns	0.98ns	CK ↑	Q ↓	2.05ns/pF	1.49ns	0.58ns/pF	1.10ns
D1 ↑	1.62ns	1.16ns	CK ↑	Q ↑	3.24ns/pF	1.16ns	0.70ns/pF	0.85ns
SD ↓	1.62ns	1.21ns	CK ↑	QN ↓	9.38ns/pF	1.40ns	2.10ns/pF	1.11ns
SD ↑	1.79ns	1.21ns	CK ↑	QN ↑	5.68ns/pF	1.68ns	1.40ns/pF	1.24ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3FX

Positive edge triggered, data select front end, negative asynchronous clear, positive asynchronous preset.

Grids 25, **Transistors** 38

Inputs
D0,D1,CKA,CKB,SD,PDA,PDB,CDN

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	CK	SD	PD	CDN	Q	QN	Q	QN
X	X	X	X	X	0	X	X	0	1
X	X	X	X	1	1	X	X	1	0
0	X	↑	0	0	X	X	X	0	1
1	X	↑	0	X	1	X	X	1	0
X	0	↑	1	0	X	X	X	0	1
X	1	↑	1	X	1	X	X	1	0

X = Don't care

Capacitances

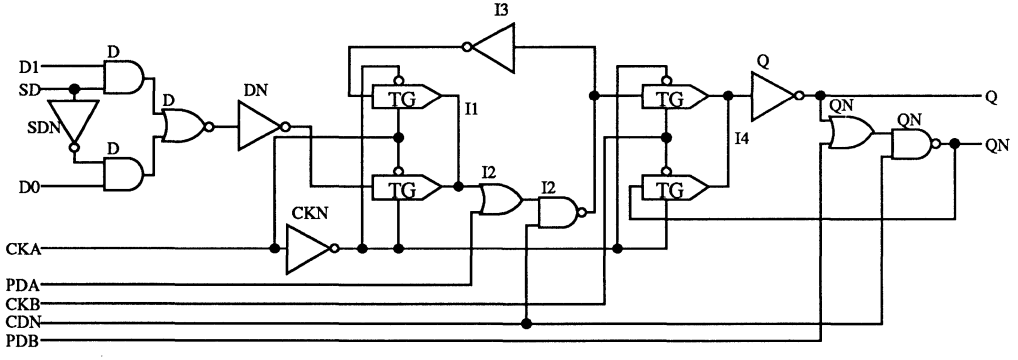
	D0	D1	CKA	CKB	SD	PDA	PDB	CDN
Area	0.027pF	0.029pF	0.057pF	0.029pF	0.056pF	0.027pF	0.027pF	0.057pF
Perf	0.102pF	0.104pF	0.065pF	0.033pF	0.206pF	0.102pF	0.103pF	0.208pF

Delay Information

Input Signal Name	Setup Time		From Input	To Output	Propagation Delay			
					Area		Performance	
	Area	Perf.			Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.68ns	1.27ns	CDN ↓	Q ↓	7.99ns/pF	1.05ns	1.77ns/pF	0.78ns
D0 ↑	1.68ns	1.21ns	CDN ↓	QN ↑	3.24ns/pF	0.58ns	0.70ns/pF	0.27ns
D1 ↓	1.56ns	1.16ns	CK ↑	Q ↓	2.25ns/pF	1.70ns	0.62ns/pF	1.13ns
D1 ↑	1.68ns	1.21ns	CK ↑	Q ↑	3.30ns/pF	1.07ns	0.70ns/pF	0.85ns
SD ↓	1.62ns	1.27ns	CK ↑	QN ↓	9.38ns/pF	1.40ns	2.14ns/pF	1.08ns
SD ↑	2.02ns	1.44ns	CK ↑	QN ↑	8.79ns/pF	2.14ns	2.01ns/pF	1.44ns
			PD ↑	Q ↑	8.32ns/pF	1.62ns	2.05ns/pF	0.90ns
			PD ↑	QN ↓	4.03ns/pF	1.26ns	1.07ns/pF	0.45ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3GX

Positive edge triggered, data select front end, negative asynchronous preset.

Grids 22, **Transistors** 32

Inputs
D0,D1,CKA,CKB,SD,PDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	PDN	Q	QN	Q	QN
X	X	X	X	0	X	X	1	0
0	X	↑	0	1	X	X	0	1
1	X	↑	0	X	X	X	1	0
X	0	↑	1	1	X	X	0	1
X	1	↑	1	X	X	X	1	0

X = Don't care

Capacitances

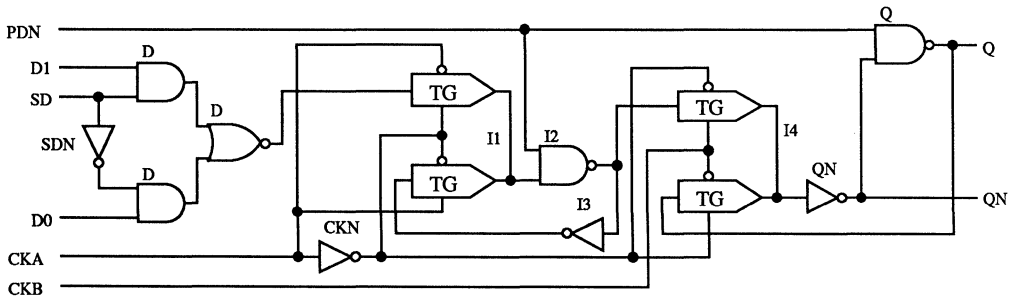
	D0	D1	CKA	CKB	SD	PDN
Area	0.027pF	0.029pF	0.058pF	0.029pF	0.055pF	0.059pF
Perf	0.103pF	0.104pF	0.066pF	0.033pF	0.206pF	0.209pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.68ns	1.04ns	CK ↑	Q ↓	9.38ns/pF	1.40ns	2.14ns/pF	1.02ns
D0 ↑	1.56ns	0.92ns	CK ↑	Q ↑	5.68ns/pF	1.68ns	1.40ns/pF	1.24ns
D1 ↓	1.44ns	0.98ns	CK ↑	QN ↓	2.05ns/pF	1.49ns	0.62ns/pF	1.02ns
D1 ↑	1.56ns	0.92ns	CK ↑	QN ↑	3.24ns/pF	1.16ns	0.70ns/pF	0.85ns
SD ↓	1.62ns	1.04ns	PDN ↓	Q ↑	3.24ns/pF	0.52ns	0.70ns/pF	0.21ns
SD ↑	2.02ns	1.27ns	PDN ↓	QN ↓	7.99ns/pF	0.93ns	1.77ns/pF	0.73ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3IX

Positive edge triggered, data select front end, positive synchronous clear.

Grids 23, **Transistors** 32

Inputs
D0,D1,CKA,CKB,SD,CD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	CD	Q	QN	Q	QN
X	X	↑	1	1	X	X	0	1
0	X	↑	0	X	X	X	0	1
1	X	↑	0	X	X	X	1	0
X	0	↑	1	X	X	X	0	1
X	1	↑	1	0	X	X	1	0

X = Don't care **Note: CD does not function while SD=0**

Capacitances

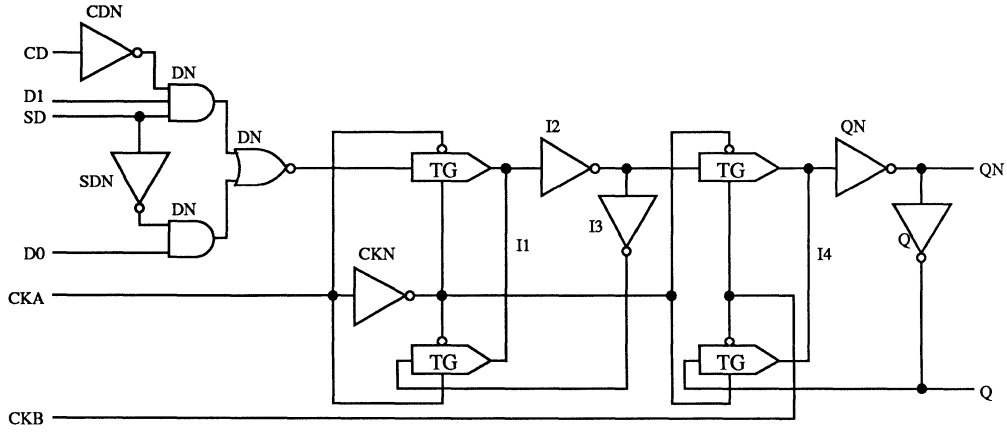
	D0	D1	CKA	CKB	SD	CD
Area	0.027pF	0.027pF	0.057pF	0.028pF	0.057pF	0.027pF
Perf	0.102pF	0.102pF	0.065pF	0.032pF	0.207pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CD ↓	1.62ns	1.16ns	CK ↑	Q ↓	7.93ns/pF	1.13ns	1.77ns/pF	0.90ns
CD ↑	1.91ns	1.16ns	CK ↑	Q ↑	5.81ns/pF	1.63ns	1.40ns/pF	1.24ns
D0 ↓	1.56ns	0.98ns	CK ↑	QN ↓	2.05ns/pF	1.54ns	0.58ns/pF	1.10ns
D0 ↑	1.56ns	0.92ns	CK ↑	QN ↑	3.24ns/pF	0.98ns	0.66ns/pF	0.88ns
D1 ↓	1.33ns	0.87ns						
D1 ↑	1.85ns	1.10ns						
SD ↓	1.50ns	1.04ns						
SD ↑	1.91ns	1.16ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3JX

Positive edge triggered, data select front end, positive synchronous preset.

Grids 21, **Transistors** 30

Inputs
D0,D1,CKA,CKB,SD,PD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	PD	Q	QN	Q	QN
X	X	↑	1	1	X	X	1	0
0	X	↑	0	X	X	X	0	1
1	X	↑	0	X	X	X	1	0
X	0	↑	1	0	X	X	0	1
X	1	↑	1	X	X	X	1	0

X = Don't care **Note: PD does not function while SD=0**

Capacitances

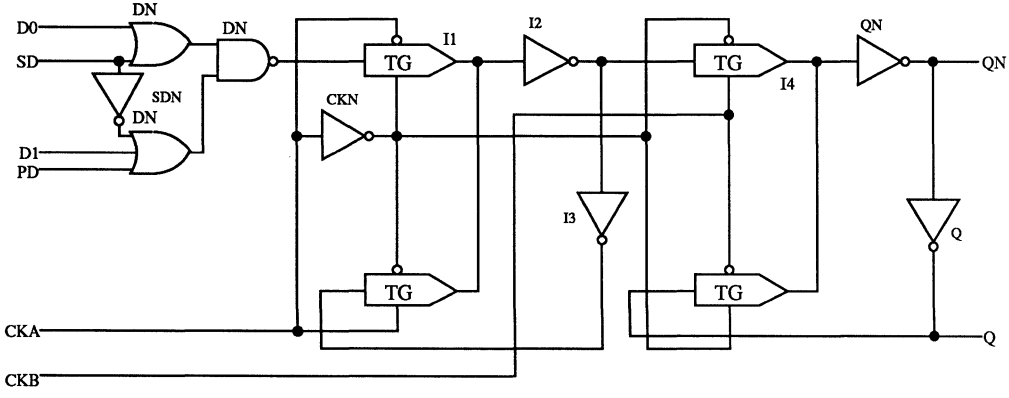
	D0	D1	CKA	CKB	SD	PD
Area	0.027pF	0.027pF	0.056pF	0.028pF	0.056pF	0.027pF
Perf	0.102pF	0.102pF	0.065pF	0.033pF	0.206pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.56ns	0.98ns	CK ↑	Q ↓	7.93ns/pF	1.13ns	1.77ns/pF	0.90ns
D0 ↑	1.44ns	0.87ns	CK ↑	Q ↑	5.81ns/pF	1.63ns	1.40ns/pF	1.24ns
D1 ↓	2.02ns	1.16ns	CK ↑	QN ↓	2.05ns/pF	1.54ns	0.58ns/pF	1.10ns
D1 ↑	1.50ns	0.92ns	CK ↑	QN ↑	3.24ns/pF	0.98ns	0.66ns/pF	0.88ns
PD ↓	2.02ns	1.21ns						
PD ↑	1.39ns	0.87ns						
SD ↓	1.56ns	1.04ns						
SD ↑	2.37ns	1.39ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3KX

Positive edge triggered, data select front end, negative asynchronous clear, negative asynchronous preset.

Grids 27, **Transistors** 38

Inputs
D0,D1,CKA,CKB,SD,PDNA,PDNB,CDN

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	CK	SD	PDN	CDN	Q	QN	Q	QN
X	X	X	X	X	0	X	X	0	1
X	X	X	X	0	1	X	X	1	0
0	X	↑	0	1	X	X	X	0	1
1	X	↑	0	X	1	X	X	1	0
X	0	↑	1	1	X	X	X	0	1
X	1	↑	1	X	1	X	X	1	0

X = Don't care

Capacitances

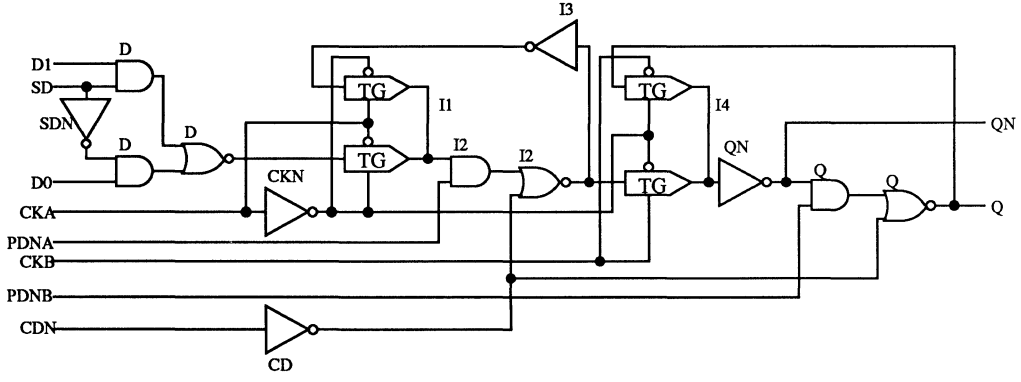
	D0	D1	CKA	CKB	SD	PDNA	PDNB	CDN
Area	0.027pF	0.029pF	0.057pF	0.028pF	0.056pF	0.027pF	0.027pF	0.027pF
Perf	0.103pF	0.104pF	0.065pF	0.032pF	0.206pF	0.102pF	0.102pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.73ns	1.10ns	CDN ↓	Q ↓	2.05ns/pF	0.91ns	0.53ns/pF	0.54ns
D0 ↑	1.79ns	1.10ns	CDN ↓	QN ↑	5.75ns/pF	1.26ns	1.36ns/pF	0.97ns
D1 ↓	1.50ns	1.04ns	CK ↑	Q ↓	9.38ns/pF	1.40ns	2.10ns/pF	1.11ns
D1 ↑	1.85ns	1.16ns	CK ↑	Q ↑	8.79ns/pF	2.20ns	2.05ns/pF	1.36ns
SD ↓	1.68ns	1.21ns	CK ↑	QN ↓	2.25ns/pF	1.76ns	0.62ns/pF	1.13ns
SD ↑	2.08ns	1.33ns	CK ↑	QN ↑	3.24ns/pF	1.16ns	0.70ns/pF	0.85ns
			PDN ↓	Q ↑	6.47ns/pF	0.81ns	1.36ns/pF	0.40ns
			PDN ↓	QN ↓	12.75ns/pF	1.46ns	2.79ns/pF	0.86ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3LX

Positive edge triggered, data select front end, negative synchronous preset.

Grids 23, **Transistors** 32

Inputs
D0,D1,CKA,CKB,SD,PDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	PDN	Q	QN	Q	QN
X	X	↑	1	0	X	X	1	0
0	X	↑	0	X	X	X	0	1
1	X	↑	0	X	X	X	1	0
X	0	↑	1	1	X	X	0	1
X	1	↑	1	X	X	X	1	0

X = Don't care **Note: PDN does not function while SD=0**

Capacitances

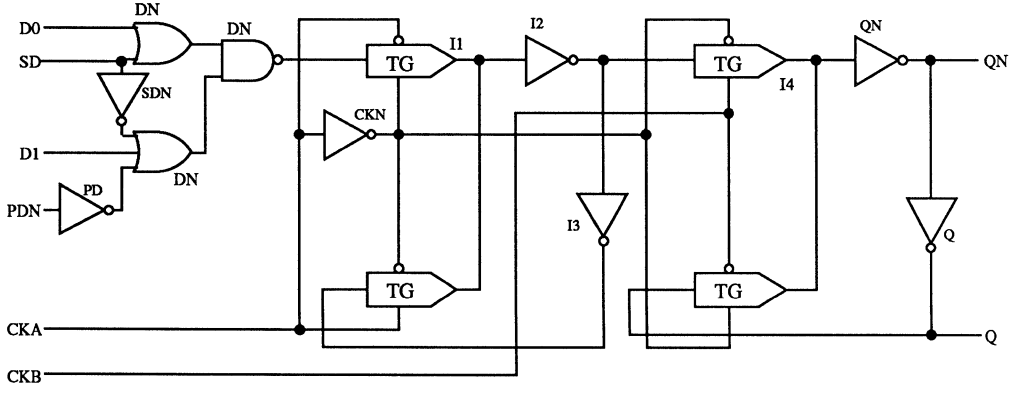
	D0	D1	CKA	CKB	SD	PDN
Area	0.027pF	0.027pF	0.057pF	0.028pF	0.056pF	0.027pF
Perf	0.102pF	0.102pF	0.065pF	0.033pF	0.206pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.56ns	0.98ns	CK ↑	Q ↓	7.93ns/pF	1.13ns	1.77ns/pF	0.90ns
D0 ↑	1.44ns	0.87ns	CK ↑	Q ↑	5.81ns/pF	1.63ns	1.40ns/pF	1.24ns
D1 ↓	2.02ns	1.16ns	CK ↑	QN ↓	2.05ns/pF	1.54ns	0.58ns/pF	1.10ns
D1 ↑	1.50ns	0.92ns	CK ↑	QN ↑	3.24ns/pF	0.98ns	0.66ns/pF	0.88ns
PDN ↓	1.27ns	0.92ns						
PDN ↑	2.37ns	1.39ns						
SD ↓	1.56ns	1.04ns						
SD ↑	2.37ns	1.39ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3MX

Positive edge triggered, data select front end, negative synchronous clear.

Grids 20, **Transistors** 30

Inputs
D0,D1,CKA,CKB,SD,CDN

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	CK	SD	CDN	Q	QN	Q	QN
X	X	↑	1	0	X	X	0	1
0	X	↑	0	X	X	X	0	1
1	X	↑	0	X	X	X	1	0
X	0	↑	1	X	X	X	0	1
X	1	↑	1	1	X	X	1	0

X = Don't care **Note: CDN does not function while SD=0**

Capacitances

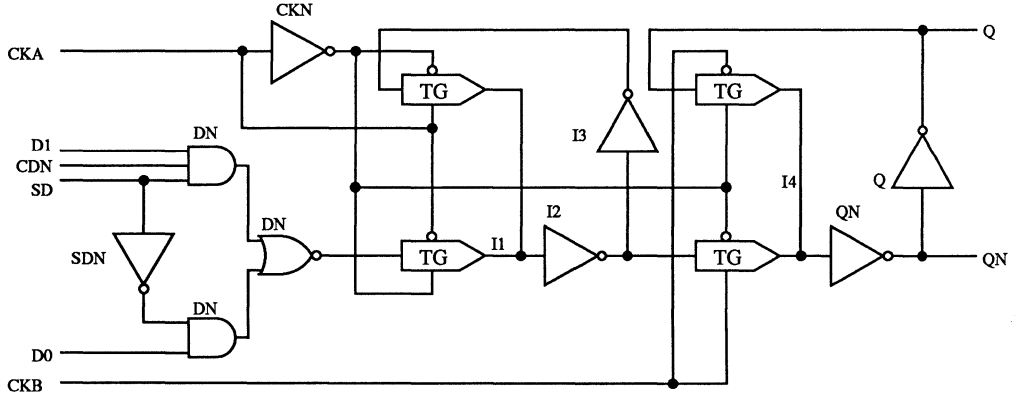
	D0	D1	CKA	CKB	SD	CDN
Area	0.027pF	0.027pF	0.057pF	0.028pF	0.057pF	0.027pF
Perf	0.102pF	0.102pF	0.065pF	0.032pF	0.207pF	0.102pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
CDN ↓	1.50ns	0.98ns	CK ↑	Q ↓	7.93ns/pF	1.07ns	1.73ns/pF	0.92ns
CDN ↑	1.79ns	1.10ns	CK ↑	Q ↑	5.75ns/pF	1.60ns	1.40ns/pF	1.18ns
D0 ↓	1.56ns	0.98ns	CK ↑	QN ↓	1.98ns/pF	1.51ns	0.58ns/pF	1.04ns
D0 ↑	1.56ns	0.92ns	CK ↑	QN ↑	3.24ns/pF	0.92ns	0.70ns/pF	0.79ns
D1 ↓	1.33ns	0.87ns						
D1 ↑	1.79ns	1.10ns						
SD ↓	1.50ns	1.04ns						
SD ↑	1.85ns	1.21ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3NX

Positive edge triggered, data select front end, positive asynchronous clear, negative asynchronous preset.

Grids 25, **Transistors** 36

Inputs
D0,D1,CKA,CKB,SD,PDNA,PDNB,CD

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	CK	SD	PDN	CD	Q	QN	Q	QN
X	X	X	X	X	1	X	X	0	1
X	X	X	X	0	0	X	X	1	0
0	X	↑	0	1	X	X	X	0	1
1	X	↑	0	X	0	X	X	1	0
X	0	↑	1	1	X	X	X	0	1
X	1	↑	1	X	0	X	X	1	0

X = Don't care

Capacitances

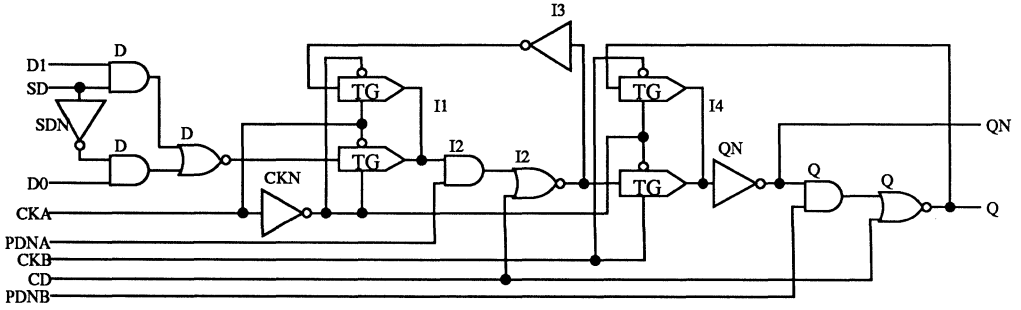
	D0	D1	CKA	CKB	SD	PDNA	PDNB	CD
Area	0.027pF	0.029pF	0.057pF	0.028pF	0.056pF	0.027pF	0.027pF	0.057pF
Perf	0.102pF	0.104pF	0.064pF	0.032pF	0.206pF	0.102pF	0.103pF	0.207pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	1.73ns	1.10ns	CD ↑	Q ↓	2.25ns/pF	1.18ns	0.58ns/pF	0.40ns
D0 ↑	1.85ns	1.16ns	CD ↑	QN ↑	6.01ns/pF	1.50ns	1.40ns/pF	0.83ns
D1 ↓	1.50ns	1.04ns	CK ↑	Q ↓	9.38ns/pF	1.45ns	2.10ns/pF	1.16ns
D1 ↑	1.85ns	1.16ns	CK ↑	Q ↑	8.79ns/pF	2.20ns	2.01ns/pF	1.44ns
SD ↓	1.68ns	1.21ns	CK ↑	QN ↓	2.18ns/pF	1.84ns	0.62ns/pF	1.13ns
SD ↑	2.08ns	1.33ns	CK ↑	QN ↑	3.24ns/pF	1.16ns	0.70ns/pF	0.85ns
			PDN ↓	Q ↑	6.47ns/pF	0.81ns	1.36ns/pF	0.45ns
			PDN ↓	QN ↓	12.75ns/pF	1.46ns	2.75ns/pF	1.00ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL1S3OX

Positive edge triggered, data select front end, positive synchronous clear, positive synchronous preset.

Grids 24, **Transistors** 34

Inputs
D0,D1,CKA,CKB,SD,PD,CD

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	CK	SD	PD	CD	Q	QN	Q	QN
0	X	↑	0	X	X	X	X	0	1
1	X	↑	0	X	X	X	X	1	0
X	X	↑	1	X	1	X	X	0	1
X	X	↑	1	1	0	X	X	1	0
X	0	↑	1	0	X	X	X	0	1
X	1	↑	1	X	0	X	X	1	0

X = Don't care **Note: PD/CD do not function while SD=0**

Capacitances

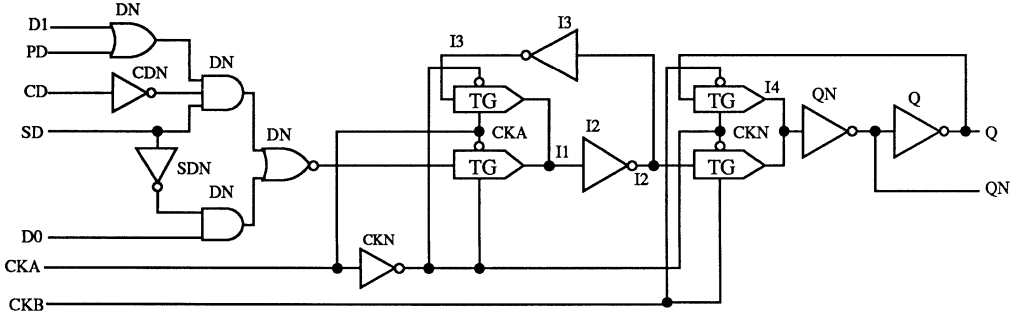
	D0	D1	CKA	CKB	SD	PD	CD
Area	0.027pF	0.027pF	0.058pF	0.028pF	0.057pF	0.027pF	0.027pF
Perf	0.102pF	0.102pF	0.066pF	0.032pF	0.207pF	0.102pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CD ↓	1.68ns	1.21ns	CK ↑	Q ↓	7.93ns/pF	1.13ns	1.77ns/pF	0.90ns
CD ↑	1.97ns	1.21ns	CK ↑	Q ↑	5.81ns/pF	1.63ns	1.40ns/pF	1.24ns
D0 ↓	1.62ns	0.98ns	CK ↑	QN ↓	2.05ns/pF	1.54ns	0.58ns/pF	1.10ns
D0 ↑	1.62ns	0.98ns	CK ↑	QN ↑	3.24ns/pF	0.98ns	0.66ns/pF	0.88ns
D1 ↓	1.85ns	1.10ns						
D1 ↑	1.85ns	1.10ns						
PD ↓	2.08ns	1.21ns						
PD ↑	1.79ns	1.10ns						
SD ↓	1.56ns	1.04ns						
SD ↑	2.37ns	1.44ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1A

Master-Slave clocking, data select front end.

Grids 20, **Transistors** 32

Inputs
D0,D1,MCK,SCK,SD

Outputs
Q,QN

Truth Table

INPUTS					OUTPUTS			
					OLD		NEW	
D0	D1	MCK	SCK	SD	Q	QN	Q	QN
0	X	↓	↑	0	X	X	0	1
1	X	↓	↑	0	X	X	1	0
X	0	↓	↑	1	X	X	0	1
X	1	↓	↑	1	X	X	1	0

X = Don't care

Capacitances

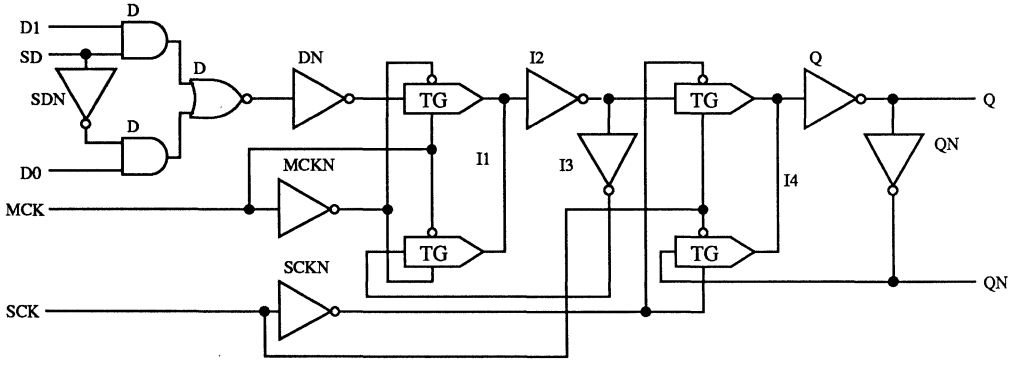
	D0	D1	MCK	SCK	SD
Area	0.027pF	0.029pF	0.059pF	0.056pF	0.054pF
Perf	0.102pF	0.104pF	0.068pF	0.065pF	0.204pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.39ns	1.04ns	SCK ↑	Q ↓	1.98ns/pF	1.22ns	0.58ns/pF	0.92ns
D0 ↑	1.50ns	1.04ns	SCK ↑	Q ↑	3.24ns/pF	0.87ns	0.70ns/pF	0.73ns
D1 ↓	1.27ns	0.92ns	SCK ↑	QN ↓	7.99ns/pF	0.99ns	1.73ns/pF	0.87ns
D1 ↑	1.50ns	1.04ns	SCK ↑	QN ↑	5.75ns/pF	1.37ns	1.40ns/pF	1.07ns
SD ↓	1.44ns	1.10ns						
SD ↑	1.73ns	1.21ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1B

Master-Slave clocking, data select front end, positive asynchronous preset.

Grids 23, **Transistors** 36

Inputs
D0,D1,MCK,SCK,SD,PD

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	MCK	SCK	SD	PD	Q	QN	Q	QN
X	X	X	X	X	1	X	X	1	0
0	X	↓	↑	0	0	X	X	0	1
1	X	↓	↑	0	X	X	X	1	0
X	0	↓	↑	1	0	X	X	0	1
X	1	↓	↑	1	X	X	X	1	0

X = Don't care

Capacitances

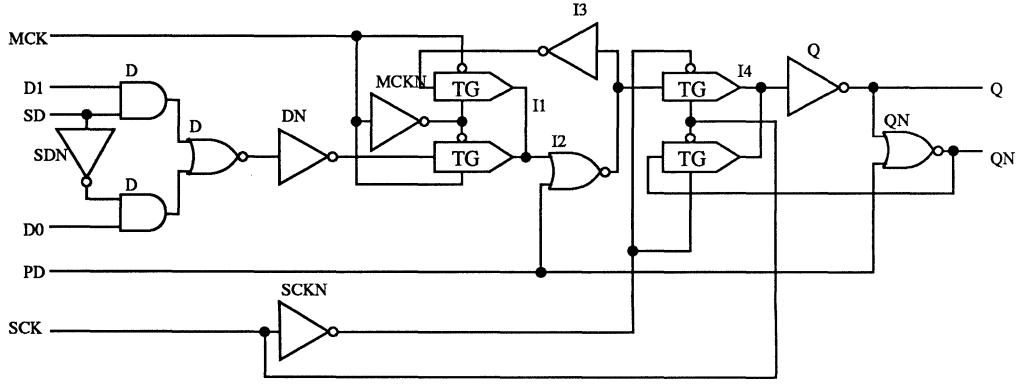
	D0	D1	MCK	SCK	SD	PD
Area	0.027pF	0.029pF	0.057pF	0.059pF	0.054pF	0.057pF
Perf	0.102pF	0.104pF	0.065pF	0.067pF	0.204pF	0.207pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	1.68ns	1.21ns	PD ↑	Q ↑	6.01ns/pF	1.44ns	1.40ns/pF	0.78ns
D0 ↑	1.56ns	1.10ns	PD ↑	QN ↓	2.25ns/pF	1.12ns	0.58ns/pF	0.35ns
D1 ↓	1.50ns	1.16ns	SCK ↑	Q ↓	2.11ns/pF	1.46ns	0.58ns/pF	1.04ns
D1 ↑	1.56ns	1.10ns	SCK ↑	Q ↑	3.24ns/pF	0.87ns	0.70ns/pF	0.73ns
SD ↓	1.62ns	1.21ns	SCK ↑	QN ↓	7.93ns/pF	1.02ns	1.73ns/pF	0.87ns
SD ↑	2.02ns	1.44ns	SCK ↑	QN ↑	8.79ns/pF	1.73ns	2.05ns/pF	1.19ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1CX

Master-Slave clocking, data select front end, positive asynchronous clear, positive asynchronous preset.

Grids 26, **Transistors** 42

Inputs
D0,D1,MCK,SCK,SD,PDA,PDB,CD

Outputs
Q,QN

Capacitances

	D0	D1	MCK	SCK	SD	PDA	PDB	CD
Area	0.027pF	0.029pF	0.058pF	0.057pF	0.056pF	0.027pF	0.027pF	0.027pF
Perf	0.102pF	0.104pF	0.065pF	0.065pF	0.206pF	0.102pF	0.103pF	0.102pF

Truth Table

INPUTS							OUTPUTS OLD		OUTPUTS NEW	
D0	D1	MCK	SCK	SD	PD	CD	Q	QN	Q	QN
X	X	X	X	X	X	1	X	X	0	1
X	X	X	X	X	1	0	X	X	1	0
0	X	↓	↑	0	0	X	X	X	0	1
1	X	↓	↑	0	X	0	X	X	1	0
X	0	↓	↑	1	0	X	X	X	0	1
X	1	↓	↑	1	X	0	X	X	1	0

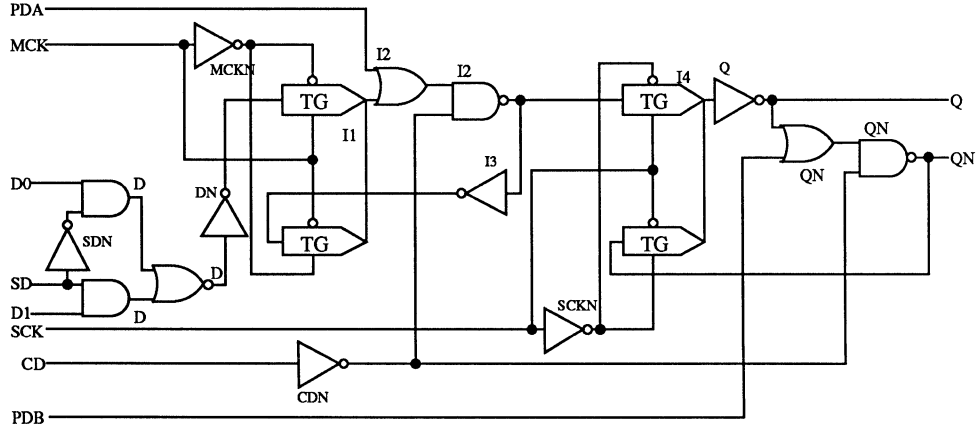
X = Don't care

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
D0 ↓	1.68ns	1.21ns	CD ↑	Q ↓	7.99ns/pF	1.45ns	1.73ns/pF	1.04ns
D0 ↑	1.68ns	1.21ns	CD ↑	QN ↑	3.24ns/pF	1.04ns	0.70ns/pF	0.50ns
D1 ↓	1.56ns	1.16ns	PD ↑	Q ↑	8.32ns/pF	1.50ns	2.05ns/pF	0.84ns
D1 ↑	1.68ns	1.21ns	PD ↑	QN ↓	4.03ns/pF	1.21ns	1.07ns/pF	0.40ns
SD ↓	1.68ns	1.27ns	SCK ↑	Q ↓	2.11ns/pF	1.40ns	0.62ns/pF	0.96ns
SD ↑	2.08ns	1.44ns	SCK ↑	Q ↑	3.24ns/pF	0.98ns	0.70ns/pF	0.79ns
			SCK ↑	QN ↓	9.38ns/pF	1.28ns	2.14ns/pF	0.97ns
			SCK ↑	QN ↑	8.72ns/pF	1.76ns	2.01ns/pF	1.21ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1D

Master-Slave clocking, data select front end, positive asynchronous clear.

Grids 23, **Transistors** 34

Inputs
D0,D1,MCK,SCK,SD,CD

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	MCK	SCK	SD	CD	Q	QN	Q	QN
X	X	X	X	X	1	X	X	0	1
0	X	↓	↑	0	X	X	X	0	1
1	X	↓	↑	0	0	X	X	1	0
X	0	↓	↑	1	X	X	X	0	1
X	1	↓	↑	1	0	X	X	1	0

X = Don't care

Capacitances

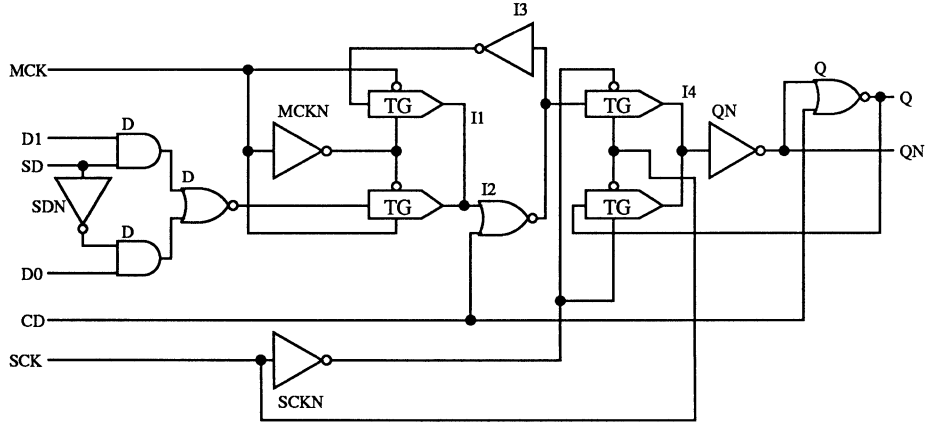
	D0	D1	MCK	SCK	SD	CD
Area	0.027pF	0.029pF	0.057pF	0.059pF	0.054pF	0.057pF
Perf	0.102pF	0.104pF	0.065pF	0.067pF	0.204pF	0.207pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	1.56ns	0.98ns	CD ↑	Q ↓	2.25ns/pF	1.12ns	0.58ns/pF	0.35ns
D0 ↑	1.79ns	1.10ns	CD ↑	QN ↑	6.01ns/pF	1.44ns	1.40ns/pF	0.78ns
D1 ↓	1.39ns	0.87ns	SCK ↑	Q ↓	7.93ns/pF	1.02ns	1.73ns/pF	0.87ns
D1 ↑	1.85ns	1.10ns	SCK ↑	Q ↑	8.79ns/pF	1.73ns	2.05ns/pF	1.19ns
SD ↓	1.68ns	1.21ns	SCK ↑	QN ↓	2.11ns/pF	1.46ns	0.58ns/pF	1.04ns
SD ↑	1.97ns	1.16ns	SCK ↑	QN ↑	3.24ns/pF	0.87ns	0.70ns/pF	0.73ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1E

Master-Slave clocking, data select front end, negative asynchronous clear.

Grids 23, **Transistors** 36

Inputs
D0,D1,MCK,SCK,SD,CDN

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	MCK	SCK	SD	CDN	Q	QN	Q	QN
X	X	X	X	X	0	X	X	0	1
0	X	↓	↑	0	X	X	X	0	1
1	X	↓	↑	0	1	X	X	1	0
X	0	↓	↑	1	X	X	X	0	1
X	1	↓	↑	1	1	X	X	1	0

X = Don't care

Capacitances

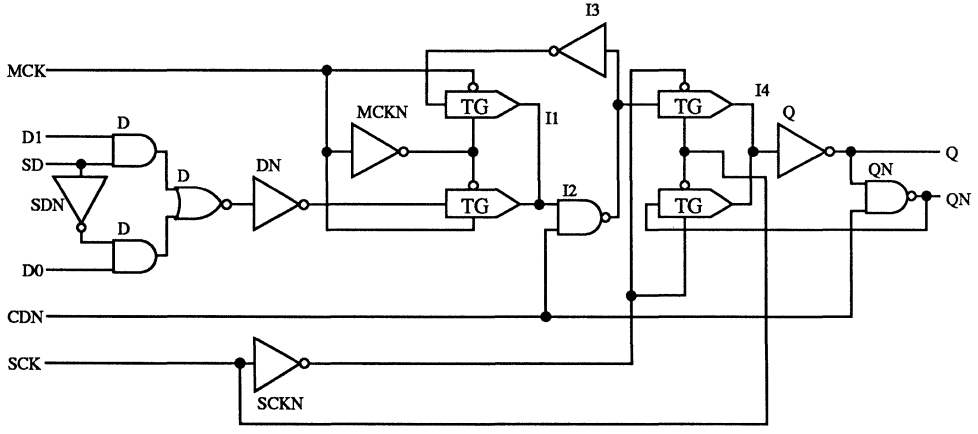
	D0	D1	MCK	SCK	SD	CDN
Area	0.027pF	0.029pF	0.057pF	0.059pF	0.054pF	0.057pF
Perf	0.102pF	0.104pF	0.065pF	0.067pF	0.204pF	0.207pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.44ns	1.04ns	CDN ↓	Q ↓	7.93ns/pF	0.90ns	1.77ns/pF	0.67ns
D0 ↑	1.62ns	1.21ns	CDN ↓	QN ↑	3.24ns/pF	0.46ns	0.70ns/pF	0.21ns
D1 ↓	1.33ns	0.98ns	SCK ↑	Q ↓	2.05ns/pF	1.20ns	0.58ns/pF	0.92ns
D1 ↑	1.68ns	1.21ns	SCK ↑	Q ↑	3.24ns/pF	1.04ns	0.70ns/pF	0.79ns
SD ↓	1.62ns	1.27ns	SCK ↑	QN ↓	9.38ns/pF	1.28ns	2.14ns/pF	0.97ns
SD ↑	1.79ns	1.27ns	SCK ↑	QN ↑	5.68ns/pF	1.40ns	1.40ns/pF	1.07ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1FX

Master-Slave clocking, data select front end, negative asynchronous clear, positive asynchronous preset.

Grids 25, **Transistors** 40

Inputs
D0,D1,MCK,SCK,SD,PDA,PDB,CDN

Outputs
Q,QN

Capacitances

Truth Table

INPUTS							OUTPUTS OLD		OUTPUTS NEW	
D0	D1	MCK	SCK	SD	PD	CDN	Q	QN	Q	QN
X	X	X	X	X	X	0	X	X	0	1
X	X	X	X	X	1	1	X	X	1	0
0	X	↓	↑	0	0	X	X	X	0	1
1	X	↓	↑	0	X	1	X	X	1	0
X	0	↓	↑	1	0	X	X	X	0	1
X	1	↓	↑	1	X	1	X	X	1	0

X = Don't care

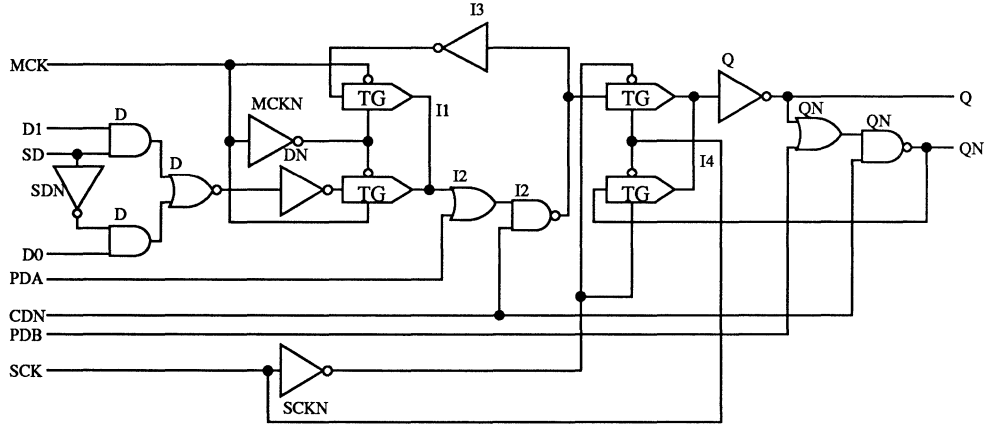
	D0	D1	MCK	SCK	SD	PDA	PDB	CDN
Area	0.027pF	0.029pF	0.058pF	0.057pF	0.056pF	0.027pF	0.027pF	0.060pF
Perf	0.102pF	0.104pF	0.065pF	0.065pF	0.206pF	0.102pF	0.103pF	0.210pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Area Intrinsic	Performance Extrinsic	Performance Intrinsic
D0 ↓	1.68ns	1.21ns	CDN ↓	Q ↓	7.99ns/pF	0.93ns	1.77ns/pF	0.67ns
D0 ↑	1.68ns	1.21ns	CDN ↓	QN ↑	3.24ns/pF	0.52ns	0.70ns/pF	0.21ns
D1 ↓	1.56ns	1.16ns	PD ↑	Q ↑	8.32ns/pF	1.50ns	2.01ns/pF	0.87ns
D1 ↑	1.68ns	1.21ns	PD ↑	QN ↓	4.03ns/pF	1.21ns	1.07ns/pF	0.40ns
SD ↓	1.68ns	1.27ns	SCK ↑	Q ↓	2.11ns/pF	1.40ns	0.62ns/pF	0.96ns
SD ↑	2.08ns	1.44ns	SCK ↑	Q ↑	3.24ns/pF	0.98ns	0.70ns/pF	0.79ns
			SCK ↑	QN ↓	9.38ns/pF	1.28ns	2.14ns/pF	0.97ns
			SCK ↑	QN ↑	8.72ns/pF	1.76ns	2.01ns/pF	1.21ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop FL2S1G

Master-Slave clocking, data select front end, negative asynchronous preset.

Grids 23, **Transistors** 34

Inputs
D0,D1,MCK,SCK,SD,PDN

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS OLD		OUTPUTS NEW	
D0	D1	MCK	SCK	SD	PDN	Q	QN	Q	QN
X	X	X	X	X	0	X	X	1	0
0	X	↓	↑	0	1	X	X	0	1
1	X	↓	↑	0	X	X	X	1	0
X	0	↓	↑	1	1	X	X	0	1
X	1	↓	↑	1	X	X	X	1	0

X = Don't care

Capacitances

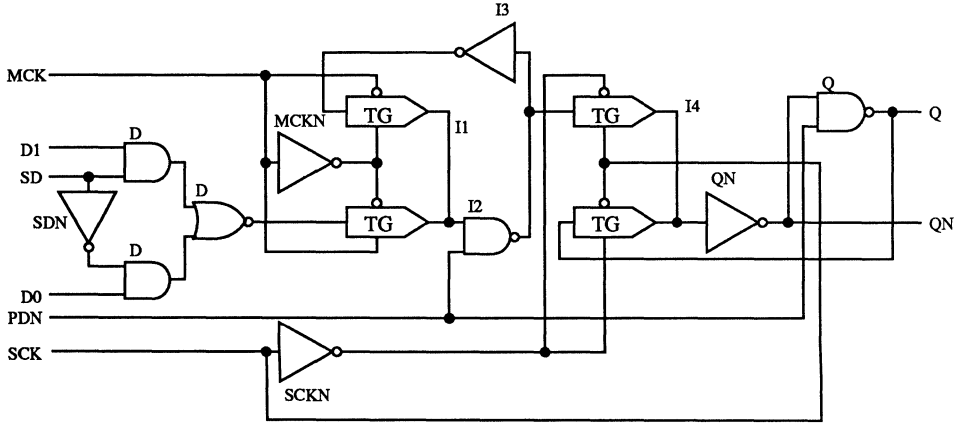
	D0	D1	MCK	SCK	SD	PDN
Area	0.027pF	0.029pF	0.057pF	0.059pF	0.054pF	0.057pF
Perf	0.102pF	0.104pF	0.065pF	0.067pF	0.204pF	0.207pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	1.73ns	1.10ns	PDN ↓	Q ↑	3.24ns/pF	0.46ns	0.70ns/pF	0.21ns
D0 ↑	1.56ns	0.98ns	PDN ↓	QN ↓	7.93ns/pF	0.90ns	1.77ns/pF	0.67ns
D1 ↓	1.50ns	0.98ns	SCK ↑	Q ↓	9.45ns/pF	1.26ns	2.14ns/pF	0.97ns
D1 ↑	1.62ns	0.98ns	SCK ↑	Q ↑	5.68ns/pF	1.40ns	1.40ns/pF	1.07ns
SD ↓	1.68ns	1.04ns	SCK ↑	QN ↓	2.05ns/pF	1.20ns	0.58ns/pF	0.92ns
SD ↑	2.08ns	1.33ns	SCK ↑	QN ↑	3.24ns/pF	1.04ns	0.70ns/pF	0.79ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop FL2S1I

Master-Slave clocking, data select front end, positive synchronous clear.

Grids 23, **Transistors** 34

Inputs
D0,D1,MCK,SCK,SD,CD

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	MCK	SCK	SD	CD	Q	QN	Q	QN
X	X	↓	↑	1	1	X	X	0	1
0	X	↓	↑	0	X	X	X	0	1
1	X	↓	↑	0	X	X	X	1	0
X	0	↓	↑	1	X	X	X	0	1
X	1	↓	↑	1	0	X	X	1	0

X = Don't care **Note: CD does not function while SD=0**

Capacitances

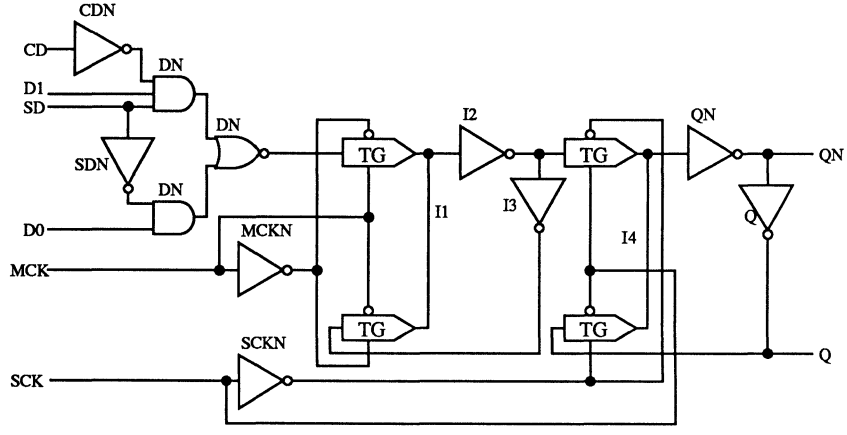
	D0	D1	MCK	SCK	SD	CD
Area	0.027pF	0.027pF	0.057pF	0.056pF	0.057pF	0.027pF
Perf	0.102pF	0.102pF	0.065pF	0.065pF	0.207pF	0.102pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
CD ↓	1.62ns	1.16ns	SCK ↑	Q ↓	7.99ns/pF	0.99ns	1.73ns/pF	0.87ns
CD ↑	1.91ns	1.21ns	SCK ↑	Q ↑	5.75ns/pF	1.37ns	1.40ns/pF	1.07ns
D0 ↓	1.56ns	0.98ns	SCK ↑	QN ↓	1.98ns/pF	1.22ns	0.58ns/pF	0.92ns
D0 ↑	1.56ns	0.92ns	SCK ↑	QN ↑	3.24ns/pF	0.87ns	0.70ns/pF	0.73ns
D1 ↓	1.33ns	0.87ns						
D1 ↑	1.79ns	1.10ns						
SD ↓	1.50ns	1.04ns						
SD ↑	1.85ns	1.21ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1J

Master-Slave clocking, data select front end, positive synchronous preset.

Grids 21, **Transistors** 32

Inputs
D0,D1,MCK,SCK,SD,PD

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	MCK	SCK	SD	PD	Q	QN	Q	QN
X	X	↓	↑	1	1	X	X	1	0
0	X	↓	↑	0	X	X	X	0	1
1	X	↓	↑	0	X	X	X	1	0
X	0	↓	↑	1	0	X	X	0	1
X	1	↓	↑	1	X	X	X	1	0

X = Don't care **Note: PD does not function while SD=0**

Capacitances

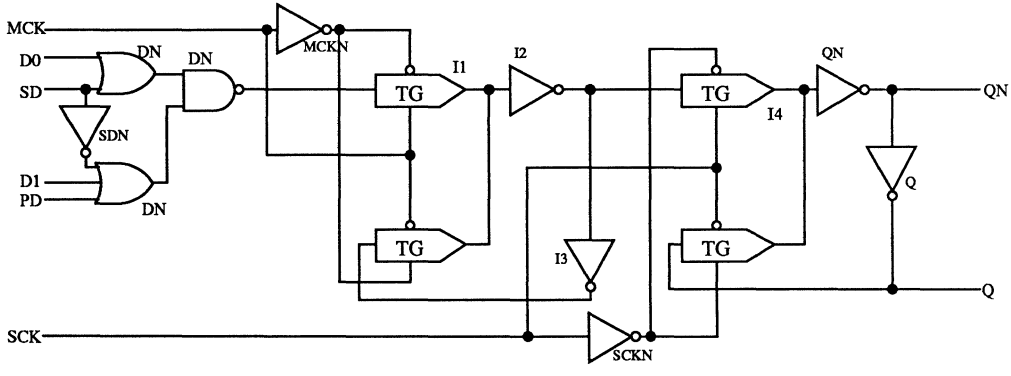
	D0	D1	MCK	SCK	SD	PD
Area	0.027pF	0.027pF	0.057pF	0.056pF	0.055pF	0.027pF
Perf	0.102pF	0.102pF	0.065pF	0.065pF	0.206pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.56ns	0.98ns	SCK ↑	Q ↓	7.99ns/pF	0.99ns	1.73ns/pF	0.87ns
D0 ↑	1.44ns	0.87ns	SCK ↑	Q ↑	5.75ns/pF	1.37ns	1.40ns/pF	1.07ns
D1 ↓	1.97ns	1.16ns	SCK ↑	QN ↓	1.98ns/pF	1.22ns	0.58ns/pF	0.92ns
D1 ↑	1.50ns	0.92ns	SCK ↑	QN ↑	3.24ns/pF	0.87ns	0.70ns/pF	0.73ns
PD ↓	1.97ns	1.21ns						
PD ↑	1.39ns	0.87ns						
SD ↓	1.50ns	1.04ns						
SD ↑	2.37ns	1.39ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1KX

Master-Slave clocking, data select front end, negative asynchronous clear, negative asynchronous preset.

Grids 26, **Transistors** 40

Inputs
D0,D1,MCK,SCK,SD,PDNA,PDNB,CDN

Outputs
Q,QN

Capacitances

Truth Table

INPUTS							OUTPUTS OLD		OUTPUTS NEW	
D0	D1	MCK	SCK	SD	PDN	CDN	Q	QN	Q	QN
X	X	X	X	X	X	0	X	X	0	1
X	X	X	X	X	0	1	X	X	1	0
0	X	↓	↑	0	1	X	X	X	0	1
1	X	↓	↑	0	X	1	X	X	1	0
X	0	↓	↑	1	1	X	X	X	0	1
X	1	↓	↑	1	X	1	X	X	1	0

X = Don't care

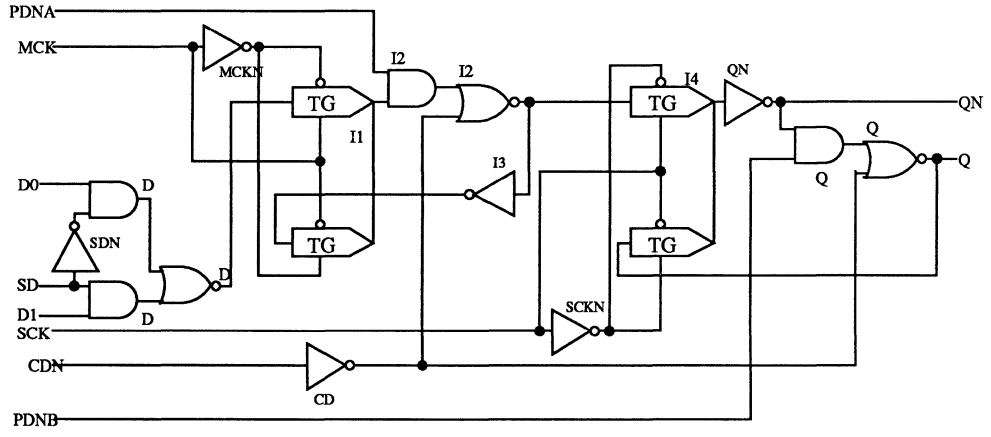
	D0	D1	MCK	SCK	SD	PDNA	PDNB	CDN
Area	0.027pF	0.029pF	0.057pF	0.057pF	0.056pF	0.027pF	0.027pF	0.027pF
Perf	0.102pF	0.104pF	0.065pF	0.065pF	0.206pF	0.102pF	0.103pF	0.102pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	1.62ns	1.04ns	CDN ↓	Q ↓	1.98ns/pF	0.93ns	0.53ns/pF	0.54ns
D0 ↑	1.73ns	1.10ns	CDN ↓	QN ↑	5.75ns/pF	1.20ns	1.36ns/pF	0.92ns
D1 ↓	1.44ns	0.98ns	PDN ↓	Q ↑	6.47ns/pF	0.69ns	1.40ns/pF	0.31ns
D1 ↑	1.79ns	1.10ns	PDN ↓	QN ↓	12.75ns/pF	1.23ns	2.79ns/pF	0.80ns
SD ↓	1.68ns	1.16ns	SCK ↑	Q ↓	9.45ns/pF	1.20ns	2.14ns/pF	0.97ns
SD ↑	1.97ns	1.27ns	SCK ↑	Q ↑	8.72ns/pF	1.76ns	2.01ns/pF	1.21ns
			SCK ↑	QN ↓	2.11ns/pF	1.40ns	0.62ns/pF	0.96ns
			SCK ↑	QN ↑	3.24ns/pF	0.98ns	0.70ns/pF	0.79ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1L

Master-Slave clocking, data select front end, negative synchronous preset.

Grids 23, **Transistors** 34

Inputs
D0,D1,MCK,SCK,SD,PDN

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	MCK	SCK	SD	PDN	Q	QN	Q	QN
X	X	↓	↑	1	0	X	X	1	0
0	X	↓	↑	0	X	X	X	0	1
1	X	↓	↑	0	X	X	X	1	0
X	0	↓	↑	1	1	X	X	0	1
X	1	↓	↑	1	X	X	X	1	0

X = Don't care **Note: PDN does not function while SD=0**

Capacitances

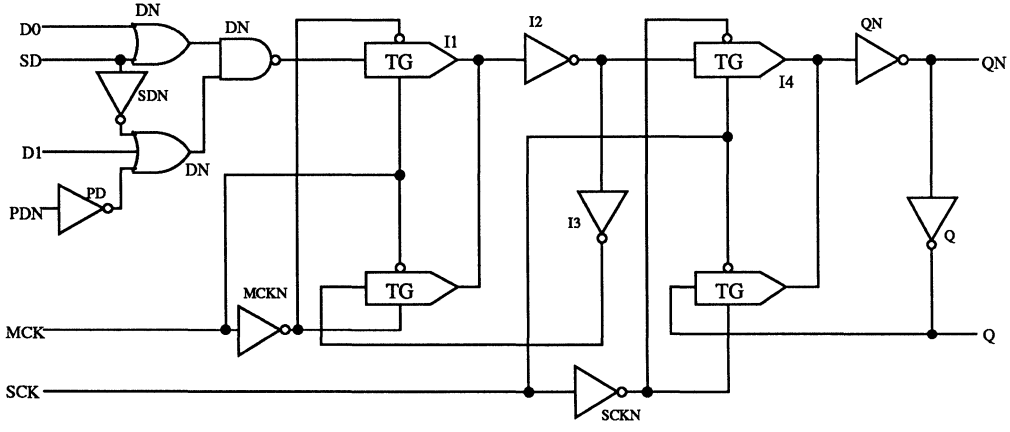
	D0	D1	MCK	SCK	SD	PDN
Area	0.027pF	0.027pF	0.057pF	0.056pF	0.056pF	0.027pF
Perf	0.102pF	0.102pF	0.065pF	0.065pF	0.206pF	0.102pF

Delay Information

Input Signal Name	Setup Time Area	Setup Time Perf.	From Input	To Output	Propagation Delay Area Extrinsic	Propagation Delay Area Intrinsic	Propagation Delay Performance Extrinsic	Propagation Delay Performance Intrinsic
D0 ↓	1.62ns	1.04ns	SCK ↑	Q ↓	7.99ns/pF	0.99ns	1.73ns/pF	0.87ns
D0 ↑	1.50ns	0.92ns	SCK ↑	Q ↑	5.75ns/pF	1.37ns	1.40ns/pF	1.07ns
D1 ↓	2.08ns	1.27ns	SCK ↑	QN ↓	1.98ns/pF	1.22ns	0.58ns/pF	0.92ns
D1 ↑	1.56ns	0.98ns	SCK ↑	QN ↑	3.24ns/pF	0.87ns	0.70ns/pF	0.73ns
PDN ↓	1.27ns	0.98ns						
PDN ↑	2.49ns	1.44ns						
SD ↓	1.62ns	1.04ns						
SD ↑	2.49ns	1.44ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1M

Master-Slave clocking, data select front end, negative synchronous clear.

Grids 21, **Transistors** 32

Inputs
D0,D1,MCK,SCK,SD,CDN

Outputs
Q,QN

Truth Table

INPUTS						OUTPUTS			
						OLD		NEW	
D0	D1	MCK	SCK	SD	CDN	Q	QN	Q	QN
X	X	↓	↑	1	0	X	X	0	1
0	X	↓	↑	0	X	X	X	0	1
1	X	↓	↑	0	X	X	X	1	0
X	0	↓	↑	1	X	X	X	0	1
X	1	↓	↑	1	1	X	X	1	0

X = Don't care **Note: CDN does not function while SD=0**

Capacitances

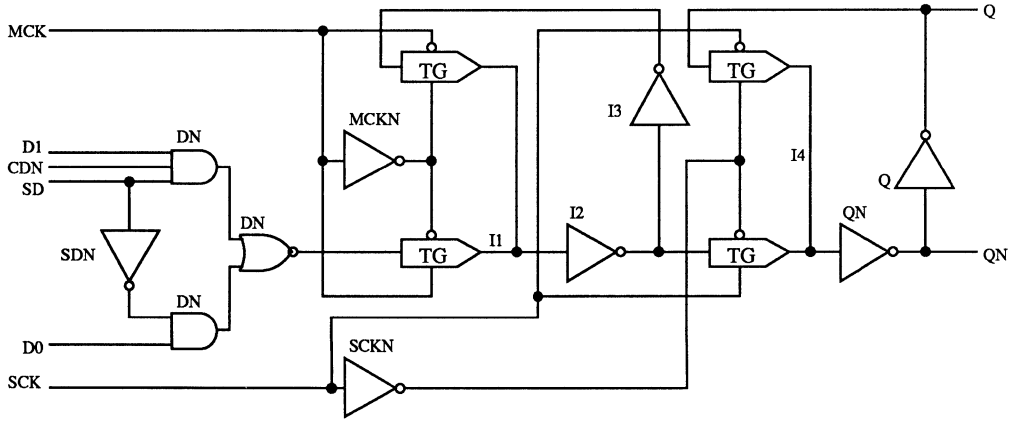
	D0	D1	MCK	SCK	SD	CDN
Area	0.027pF	0.027pF	0.057pF	0.056pF	0.057pF	0.027pF
Perf	0.102pF	0.102pF	0.065pF	0.065pF	0.207pF	0.102pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CDN ↓	1.50ns	0.98ns	SCK ↑	Q ↓	7.99ns/pF	0.99ns	1.73ns/pF	0.87ns
CDN ↑	1.79ns	1.10ns	SCK ↑	Q ↑	5.75ns/pF	1.37ns	1.40ns/pF	1.07ns
D0 ↓	1.50ns	0.98ns	SCK ↑	QN ↓	1.98ns/pF	1.22ns	0.58ns/pF	0.92ns
D0 ↑	1.56ns	0.92ns	SCK ↑	QN ↑	3.24ns/pF	0.87ns	0.70ns/pF	0.73ns
D1 ↓	1.33ns	0.87ns						
D1 ↑	1.79ns	1.10ns						
SD ↓	1.50ns	1.04ns						
SD ↑	1.85ns	1.21ns						

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static D-Type Flip-Flop

FL2S1NX

Master-Slave clocking, data select front end, positive asynchronous clear, negative asynchronous preset.

Grids 25, **Transistors** 38

Inputs
D0,D1,MCK,SCK,SD,PDNA,PDNB,CD

Outputs
Q,QN

Truth Table

INPUTS							OUTPUTS			
							OLD		NEW	
D0	D1	MCK	SCK	SD	PDN	CD	Q	QN	Q	QN
X	X	X	X	X	X	1	X	X	0	1
X	X	X	X	X	0	0	X	X	1	0
0	X	↓	↑	0	1	X	X	X	0	1
1	X	↓	↑	0	X	0	X	X	1	0
X	0	↓	↑	1	1	X	X	X	0	1
X	1	↓	↑	1	X	0	X	X	1	0

X = Don't care

Capacitances

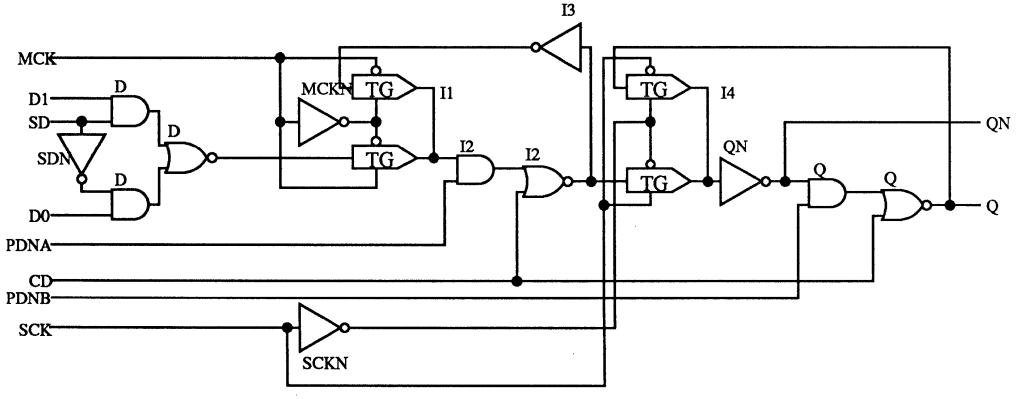
	D0	D1	MCK	SCK	SD	PDNA	PDNB	CD
Area	0.027pF	0.029pF	0.057pF	0.057pF	0.056pF	0.027pF	0.027pF	0.060pF
Perf	0.102pF	0.104pF	0.065pF	0.065pF	0.206pF	0.102pF	0.103pF	0.210pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
D0 ↓	1.62ns	1.04ns	CD ↑	Q ↓	2.31ns/pF	1.10ns	0.58ns/pF	0.40ns
D0 ↑	1.73ns	1.10ns	CD ↑	QN ↑	6.01ns/pF	1.44ns	1.40ns/pF	0.78ns
D1 ↓	1.44ns	0.98ns	PDN ↓	Q ↑	6.47ns/pF	0.69ns	1.40ns/pF	0.31ns
D1 ↑	1.79ns	1.10ns	PDN ↓	QN ↓	12.75ns/pF	1.23ns	2.79ns/pF	0.80ns
SD ↓	1.68ns	1.16ns	SCK ↑	Q ↓	9.45ns/pF	1.20ns	2.14ns/pF	0.97ns
SD ↑	1.97ns	1.27ns	SCK ↑	Q ↑	8.72ns/pF	1.76ns	2.01ns/pF	1.21ns
			SCK ↑	QN ↓	2.11ns/pF	1.40ns	0.62ns/pF	0.96ns
			SCK ↑	QN ↑	3.24ns/pF	0.98ns	0.70ns/pF	0.79ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static R-S Flip-Flop

FS0S1A

Positive level S input, positive level R input.

Grids 5, **Transistors** 8

Inputs
S,R

Outputs
Q,QN

Truth Table

INPUTS		OUTPUTS			
		OLD		NEW	
S	R	Q	QN	Q	QN
0	X	0	1	0	1
X	0	1	0	1	0
0	1	X	X	0	1
1	0	X	X	1	0
1	1	X	X	0	0

X = Don't care

Capacitances

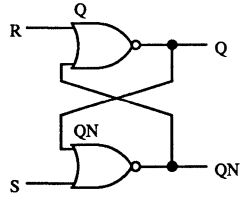
	S	R
Area	0.027pF	0.027pF
Perf	0.102pF	0.102pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
R ↑	Q ↓	2.31ns/pF	0.98ns	0.58ns/pF	0.35ns
R ↑	QN ↑	8.98ns/pF	1.31ns	2.01ns/pF	0.64ns
S ↑	Q ↑	8.98ns/pF	1.31ns	2.01ns/pF	0.64ns
S ↑	QN ↓	2.31ns/pF	0.98ns	0.58ns/pF	0.35ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static R-S Flip-Flop

FS0S1D

Positive level S input, positive level R input, positive asynchronous clear.

Grids 6, **Transistors** 10

Inputs
S,R,CD

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
S	R	CD	Q	QN	Q	QN
0	X	X	0	1	0	1
X	0	0	1	0	1	0
0	X	1	X	X	0	1
0	1	X	X	X	0	1
1	0	0	X	X	1	0
1	X	1	X	X	0	0
1	1	X	X	X	0	0

X = Don't care

Capacitances

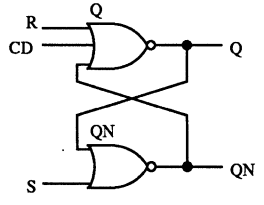
	S	R	CD
Area	0.027pF	0.027pF	0.027pF
Perf	0.102pF	0.102pF	0.102pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
CD ↑	Q ↓	2.31ns/pF	0.98ns	0.53ns/pF	0.43ns
CD ↑	QN ↑	8.98ns/pF	1.37ns	2.01ns/pF	0.64ns
R ↑	Q ↓	2.31ns/pF	0.98ns	0.53ns/pF	0.43ns
R ↑	QN ↑	8.98ns/pF	1.37ns	2.01ns/pF	0.64ns
S ↑	Q ↑	12.02ns/pF	1.62ns	2.63ns/pF	0.84ns
S ↑	QN ↓	2.31ns/pF	0.98ns	0.58ns/pF	0.35ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static R-S Flip-Flop

FS0S7A

Positive level S input, negative level R input.

Grids 5, **Transistors** 8

Inputs
S,RN

Outputs
Q,QN

Truth Table

INPUTS		OUTPUTS			
		OLD		NEW	
S	RN	Q	QN	Q	QN
0	X	0	1	0	1
X	1	1	0	1	0
0	0	X	X	0	1
1	X	X	X	1	0

X = Don't care

Capacitances

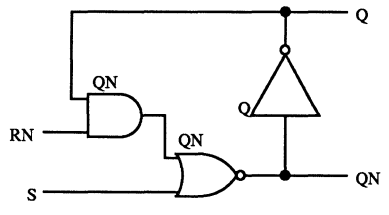
	S	RN
Area	0.027pF	0.027pF
Perf	0.102pF	0.102pF

Delay Information

From Input	To Output	Propagation Delay			
		Area		Performance	
		Extrinsic	Intrinsic	Extrinsic	Intrinsic
RN ↓	Q ↓	12.68ns/pF	0.79ns	2.75ns/pF	0.54ns
RN ↓	QN ↑	6.41ns/pF	0.49ns	1.40ns/pF	0.26ns
S ↑	Q ↑	6.01ns/pF	1.27ns	1.44ns/pF	0.52ns
S ↑	QN ↓	2.31ns/pF	0.98ns	0.58ns/pF	0.35ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static R-S Flip-Flop

FS1S1A

Positive level sense.

Grids 7, **Transistors** 12

Inputs
S,R,CK

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
S	R	CK	Q	QN	Q	QN
X	X	0	0	1	0	1
X	X	0	1	0	1	0
0	0	X	0	1	0	1
0	0	X	1	0	1	0
0	1	1	X	X	0	1
1	0	1	X	X	1	0

X = Don't care

Capacitances

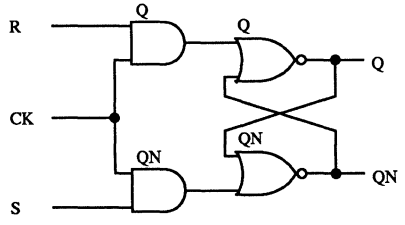
	S	R	CK
Area	0.027pF	0.027pF	0.056pF
Perf	0.102pF	0.103pF	0.206pF

Delay Information

From	To	Propagation Delay			
		Area		Performance	
Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
CK ↑	Q ↓	4.03ns/pF	1.03ns	1.07ns/pF	0.40ns
CK ↑	Q ↑	11.03ns/pF	1.47ns	2.63ns/pF	0.73ns
CK ↑	QN ↓	4.03ns/pF	1.03ns	1.07ns/pF	0.40ns
CK ↑	QN ↑	11.03ns/pF	1.47ns	2.63ns/pF	0.73ns
R ↑	Q ↓	4.03ns/pF	1.03ns	1.07ns/pF	0.40ns
R ↑	QN ↑	11.03ns/pF	1.47ns	2.63ns/pF	0.73ns
S ↑	Q ↑	11.03ns/pF	1.47ns	2.63ns/pF	0.73ns
S ↑	QN ↓	4.03ns/pF	1.03ns	1.07ns/pF	0.40ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Static R-S Flip-Flop

FS1S3A

Positive edge triggered.

Grids 15, **Transistors** 24

Inputs
SN,RN,CK

Outputs
Q,QN

Truth Table

INPUTS			OUTPUTS			
			OLD		NEW	
SN	RN	CK	Q	QN	Q	QN
1	1	↑	0	1	0	1
1	1	↑	1	0	1	0
1	0	↑	X	X	0	1
0	1	↑	X	X	1	0

X = Don't care

Capacitances

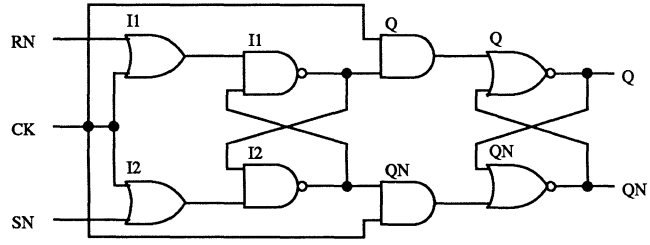
	SN	RN	CK
Area	0.028pF	0.027pF	0.114pF
Perf	0.103pF	0.102pF	0.415pF

Delay Information

Input Signal Name	Setup Time		From	To	Propagation Delay			
					Area		Performance	
	Area	Perf.	Input	Output	Extrinsic	Intrinsic	Extrinsic	Intrinsic
RN ↓	1.50ns	1.10ns	CK ↑	Q ↓	4.10ns/pF	0.95ns	1.07ns/pF	0.40ns
SN ↓	1.50ns	1.04ns	CK ↑	Q ↑	11.10ns/pF	1.39ns	2.59ns/pF	0.75ns
			CK ↑	QN ↓	4.10ns/pF	0.95ns	1.07ns/pF	0.40ns
			CK ↑	QN ↑	11.10ns/pF	1.39ns	2.59ns/pF	0.75ns

VDD=5V, T=25°C, Nominal Process.

Motis Model



Parameterized Macrocells

Section 8

Contents - Section 8

Parameterized Macrocells Introduction

This section describes the selection of parameterized macrocells available in the 0.9µm CMOS Standard-Cell Library. These are functions that are customized into complete, functional building blocks to satisfy the requirements of the circuit at hand. Depending on the function, the final building block will be implemented as a densely-packed, pitch-matched array either stand-alone or in conjunction with a standard-cell circuit layout. Using a complex function block layout generator, many functions can be realized in a much more efficient manner than is possible with a standard-cell approach. Some examples of such functions are:

- FIFO
- Register File
- SRAM
- ROM
- PLA
- Shift Register
- Multiplier

Accessing Macrocells Through *MACLOG*

These complex functions can be customized through *MACLOG*. *MACLOG* is a menu-driven program that allows you to configure a macrocell through specific variables. *MACLOG* provides general information about any of the macrocells and specific information about the characteristics and timing of your particular configuration. This will allow you to select and customize any of these macrocells to meet the specific circuit requirements.

When the variables have been fully specified, you may automatically synthesize any or all of the following items:

- A customized symbol for the macrocell, suitable for placement into the overall schematic diagram
- A customized circuit model that will accurately simulate the behavior of the macrocell
- A customized fault simulation model
- A customized model for circuit hazard analysis
- A symbolic description of the block, suitable for use in circuit layout for automatic placement and routing
- The mask artwork for the macrocell, to be included in the final chip layout

For more detailed information regarding the generation and use of these cells, contact your AT&T representative.

MACROCELL SELECTION GUIDE

NAME	DESCRIPTION
CAM	Content Addressable Memory
CAMB	Content Addressable Memory withBIST
FIFO	First-in First-out Memory
MULTP	Multiplier
PLAC2B	Programmable Logic Array
SRAM	Static Random Access Memory with BIST
REGFILE	Register File, sync. write, async. read
REGFILEB	Register File, sync. write, async. read with BIST
ROM	Read Only Memory
SRGEN	Dynamic Shift Register

CHARACTERISTICS AND TIMING

The macrocells in this section have been characterized using worst case slow processing model files and 4.5 volts supply(V_{DD}) at 125° C. The values as reported in the tables in this section, including coefficients to equations, have been converted to nominal processing and 5.0 V supply at 25 ° C using the derating factors provided in section 2. Using these derating factors will yield accurate results when converting to any of the worst case conditions previously mentioned.

The switching characteristics for the macrocells reported in the tables were measured from 40% of the high input voltage to 40% of the high output voltage with a one nanosecond rise or fall time slope on the input signal as indicated in Figure 1. The timing requirements reported in the tables were also taken from 40% voltage levels with one nanosecond rise and fall times for input signals as indicated in Figure 2

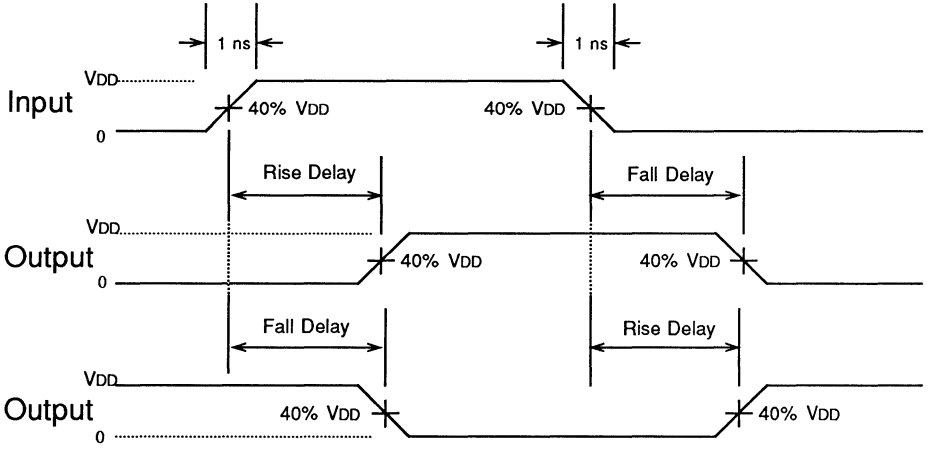


Figure 1. Switching Characteristics

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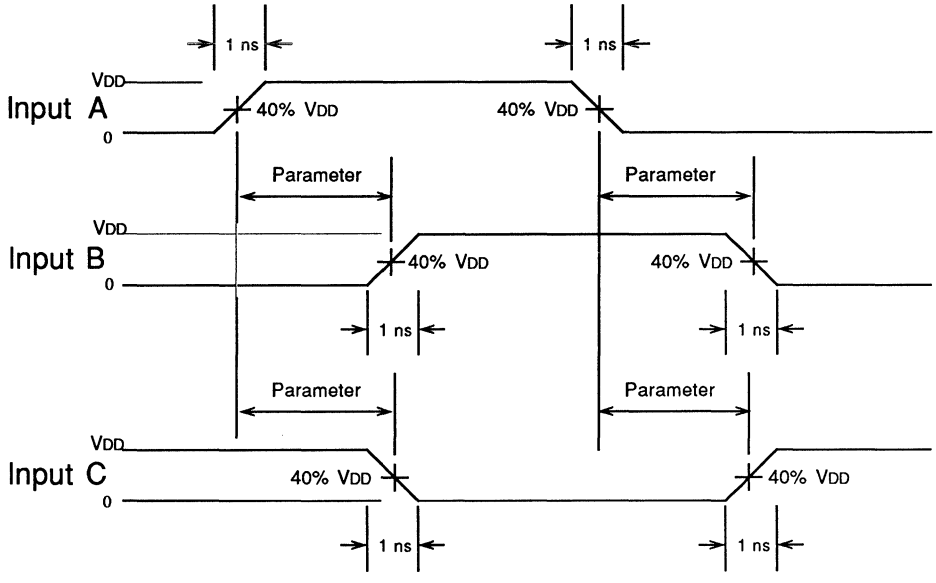


Figure 2. Timing Requirements

8

FUNCTIONAL DESCRIPTION AND FEATURES

CAM is a parameterized static (Content Addressable Memory) function supported by automatic mask layout generation software. The layout of the CAM is implemented as a custom, pitch-matched array of cells that uses two-level metal and is very area-efficient.

The CAM is also available with BIST implemented with standard cells.

The CAM has been designed specifically for use on standard-cell chips, and as such, has overhead circuitry already built-in including:

- Negative edge-triggered data input latches
- Negative edge-triggered address latches
- Negative edge-triggered read-write latch
- Positive edge-triggered latch on SM (Select Macro) input
- Positive edge-triggered data output latches
- Row decoding
- Address match encoder
- Low capacitance single clock input
- Low power wild card inputs to match any contents within a data bit
- "Select macrocell (SM) mode"
- 3-statable data out and address match outputs

CAM FUNCTION

Two functions can be achieved by the CAM. One is a standard memory operation such as read/write data from/to the memory location specified by address inputs. Another is the search function. Any content stored in the CAM can be searched directly without using address input. The read/write operation is similar to SRAM.

Match operation

Inside the CAM, the search function is realized by a match operation. The match operation uses the Match input (M[**N**-1:0]) and generates the Address Match output (AM[**M**-1:0]) and Match output(M). The value of the Match input is compared to each word in the CAM. If a match exists between the Match input and any of the memory content, the Match output goes HIGH, and the Address match output will change to the address location where the match occurred. If a match does not occur, Match stays LOW.

In the case of more than one match, the Match output still goes HIGH but the Address Match output will be invalid. The user must guarantee that multiple matches do not occur. This can be done by doing a match prior to writing new data.

During the write mode, the contents of memory are changing, therefore the Match output may be unpredictable.

Wild Card Operation

The Wild Card operation allows the user to ignore bits of the data in the match operation. For example, if the n-th bit of WC is high, the n-th bit of M[**N**-1:0] will not be compared. The rest of the **N**-1 bits will be used for comparison.

WC can be used to turn on/off match operation. If all bits of WC[N-1:0] are LOW the match operation is on. If all bits of WC[N-1:0] are HIGH the match operation is off. It is important to note that if all bits of WC are HIGH (i.e. match operation is off), Match out will go HIGH since a match will occur on each bit that is wild carded.

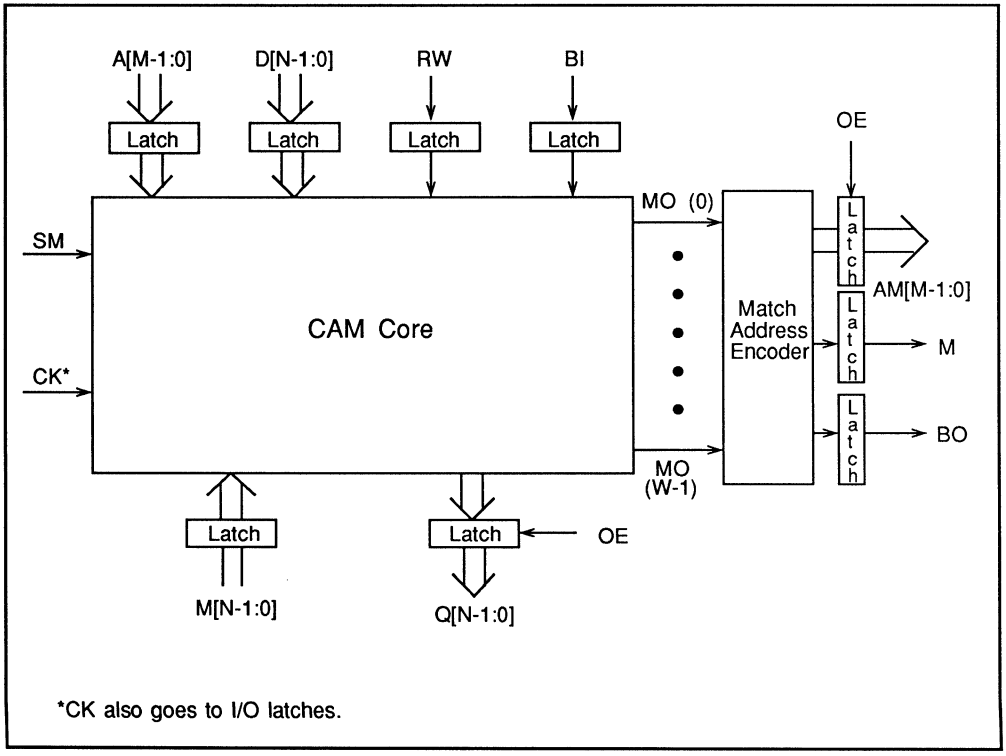
WC can be used to save power. If a user is not interested in the match operation during a CAM operation, it is recommended that WC[N-1:0] be set HIGH.

CAM can be customized by the number of words, **W**, and the number of bits/word, **N**. The valid range for these parameters are specified in the following table.

Parameters	Descriptions	Limits		
		Increment	Min	Max
W	Words	2	2	256
N	Bits/Word	1	3	32
M†	Address Bits	1	1	8

† The number of address bits, **M** = integer(log(**W**) / log(2)) + 1

BLOCK DIAGRAM



*CK also goes to I/O latches.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: BIST,BFC,A[**M**-1:0],D[**N**-1:0],M[**N**-1:0],RW,SM,CK,OE,WC[**N**-1:0]
OUTPUTS: Q[**N**-1:0],AM[**M**-1:0],M,BF,BC

Inputs

A[**M**-1:0]	Address in (A0 = LSB)
D[**N**-1:0]	Data in
M[**N**-1:0]	Match in
RW	Read/write (read = '1')
SM	Select macrocell (1 = active)
CK	Clock
OE	Output enable (1 = active; 0 = 3-stated)
WC[**N**-1:0]	Wild card (1 = active)
BI	BIST input - for use with BIST, BI = 0 for functional operation

Outputs

Q[**N**-1:0]	Data out
AM[**M**-1:0]	Address match
M	Match (1= match, 0 = no match)
BO	BIST output

CHARACTERISTICS

The parameters **N**, **M**, **W**, and **L** are used in the following equations, which can be used to estimate the characteristics for a CAM that is **W** words by **N** bits per word with **M** address bits. **L** is the number of matching words.

Parameter	Value	Unit
Height	14.6**W**+712.65	µm
Width	31.6**N**+43.75**M**+366.75	µm
Transistors	9**NW**+**NM**+210**N**+47**W**+115**M**+560	
Power: **L** matches	$(8.8\times10^{-5}\,\mathbf{NW}+0.00095\mathbf{W}+0.0063\mathbf{N}+0.043)\times F\times V_{DD}^{\,2}-6.3\times10^{-4}\times\mathbf{NL}\times F\times V_{DD}^{\,2}$	mW
Power: deselected	$(0.21\mathbf{N}+0.11\mathbf{M}+0.39)\times F\times V_{DD}^{\,2}/1000$	mW
Input Capacitance		
A[**M**-1:0]	0.011	
D[**N**-1:0]	0.011	
M[**N**-1:0]	0.031	
RW	0.015	
CK	0.683+0.14**M**+0.23**N**	pF
SM	0.053	
OE	0.163+0.052**M**+0.062**N**	
WC[**N**-1:0]	0.017**N**	
BI	0.047	
Output Capacitance		
Q[**N**-1:0]	0.064	
AM[**M**-1:0]	0.060	pF
M	0.077	
BO	0.077	

where V_{DD} = the power supply voltage, and **F** = the clock frequency, in MHz.

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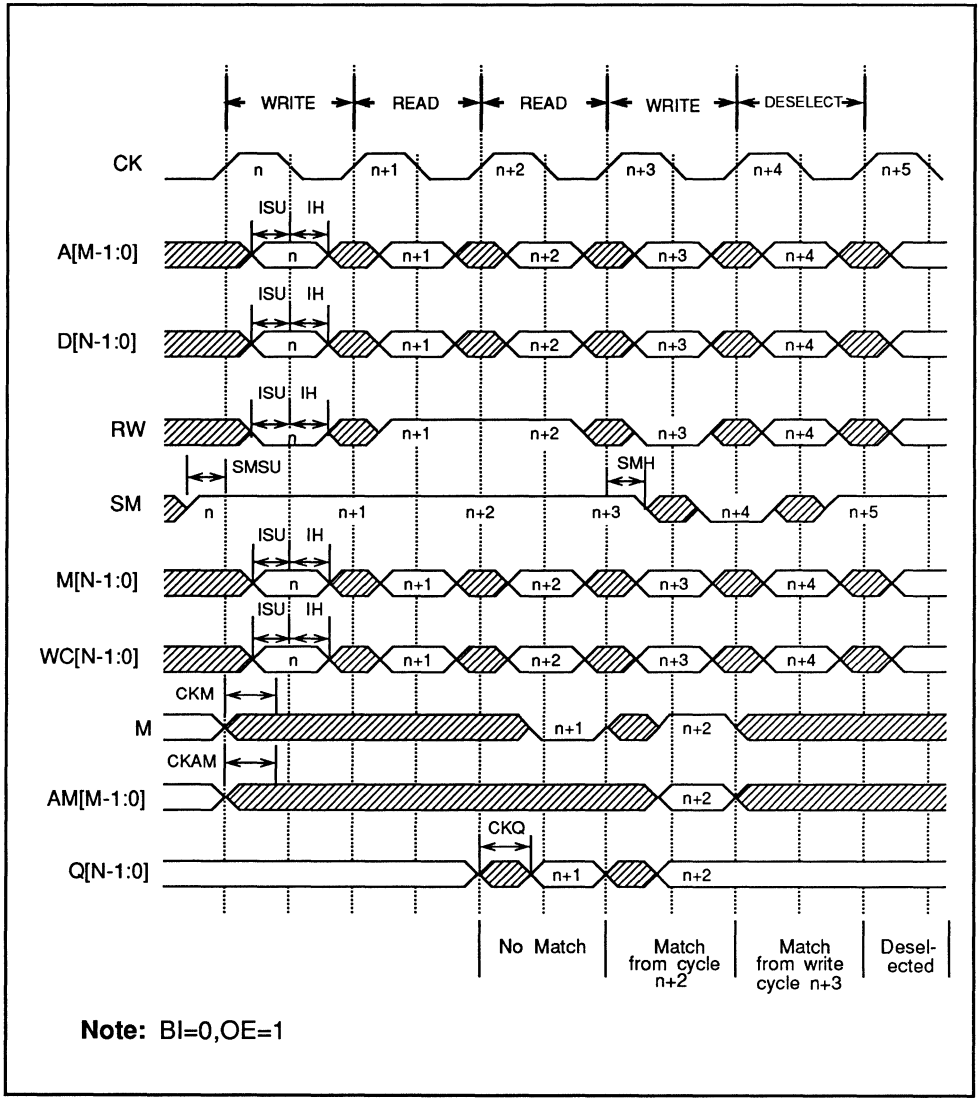
SWITCHING CHARACTERISTICS VDD=5.0V,T=25°C,NOM Processing				
Symbol	**From INPUT**	**To OUTPUT**	**Intrinsic ns**	**Extrinsic ns/pF**
CKAM	CK↑	AM[M-1:0]	3.8	0.5
CKM	CK↑	M	4.1	1.4
CKBO	CK↑	BO	5.2	0.6
CKQ	CK↑	Q[N-1:0]	2.2	0.5
OEDR	OE↑	Q[N-1:0],AM[M-1:0]	‡	‡
OEHZ	OE↓	Q[N-1:0],AM[M-1:0]	‡	NA

‡ Unavailable at time of publication

TIMING REQUIREMENTS VDD=5.0V,T=25°C,Nom Processing			
Symbol	**Description**	**Value**	**Unit**
ISU	All inputs except SM setup before CK↓	1.6	ns
ISU	All inputs except SM hold after CK↓	0.0	
SMSU	SM setup before CK↑	1.6	
SMH	SM hold after CK↑	0.0	
CKPL	Minimum CK pulse low	13.4	
CKPH	Minimum CK pulse high	13.4	

TIMING DIAGRAM



Note: BI=0,OE=1

USER NOTES

Characterization - For specific information on conditions of characterization, please refer to the introduction to this chapter under CHARACTERISTICS AND TIMING.

Select Macrocell - The SM lead can be used for several applications:

- Reduction of power. When the internal clocking is not activated, the power is greatly reduced while the memory contents and the data outputs are unaffected. Only the I/O latches are allowed to clock data in or out.
- Sub-dividing a large CAM into several smaller CAMs for speed enhancement. Here, only one of the smaller CAMs needs to be activated at any one time. Common data and address input busses can be shared by using the SM inputs to multiplex.
- Leaving a CAM in the write mode as a default may easily modify the CAM contents. Leaving a CAM in the read mode as a default may easily modify the CAM outputs. Leaving a CAM in the deselect mode with SM off ensures that the CAM contents and data outputs remain unmodified.

Output Enable - The OE affects both the Q[**N**-1:0] and AM[**M**-1:0] outputs. OE = 1 yields a valid output, while OE = 0 gives a high impedance state.

No Match - When no matches occur, the AM[**M**-1:0] outputs will all go to a logic "1". The user must use the Match output to determine if the AM is valid.

Interfacing - The CAM is designed to operate synchronously with negative edge-triggered flip-flops on all of the inputs except the SM lead. The SM is edge-triggered off of the positive edge. The SM can be driven from a negative edge flip-flop, but care must be exercised in meeting the necessary setup time.

The outputs become valid on the next positive edge after the inputs are latched. This can be used to drive positive edge flip-flops. If negative edge flip-flops are driven by the outputs, timing constraints must be carefully checked.

Clock generator - The internal clock generator for the CAM triggers off the negative edge of CK.

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FUNCTIONAL DESCRIPTION AND FEATURES

BIST CAM (Content Addressable Memory) is a parameterized static function supported by automatic mask layout generation software. The layout of the CAMB is implemented as a CAM core surrounded by standard-cell BIST logic. The output produced by this generator is an XYMASK of a CAM and an LSL which describes the interconnection of the core and the surrounding BIST logic. Specifics on the normal function of the CAMB can be found in the CAM data sheet.

The CAMB has been designed specifically for use on standard-cell chips, and as such, has overhead circuitry already built-in including:

- Fully tested memory array
- Negative edge-triggered data input latches
- Negative edge-triggered address latches
- Negative edge-triggered read-write latch
- Positive edge-triggered latch on SM (Select Macro) input
- Positive edge-triggered data output latches
- Row decoding
- Address match encoder
- Low capacitance, single clock input
- Low power wild card inputs to match any contents within a data bit
- "Select macrocell (SM) mode"
- 3-statable data out and address match outputs

CAMB can be customized by the number of words, **W**, and the number of bits/word, **N**. The valid range for these parameters are specified in the following table.

Parameters	Descriptions	Limits		
		Increment	Min	Max
W	Words	2	8	256
N	Bits/Word	1	3	32
M†	Address Bits	1	3	8

† The number of address bits, **M** = integer(log(**W**) / log(2)) + 1

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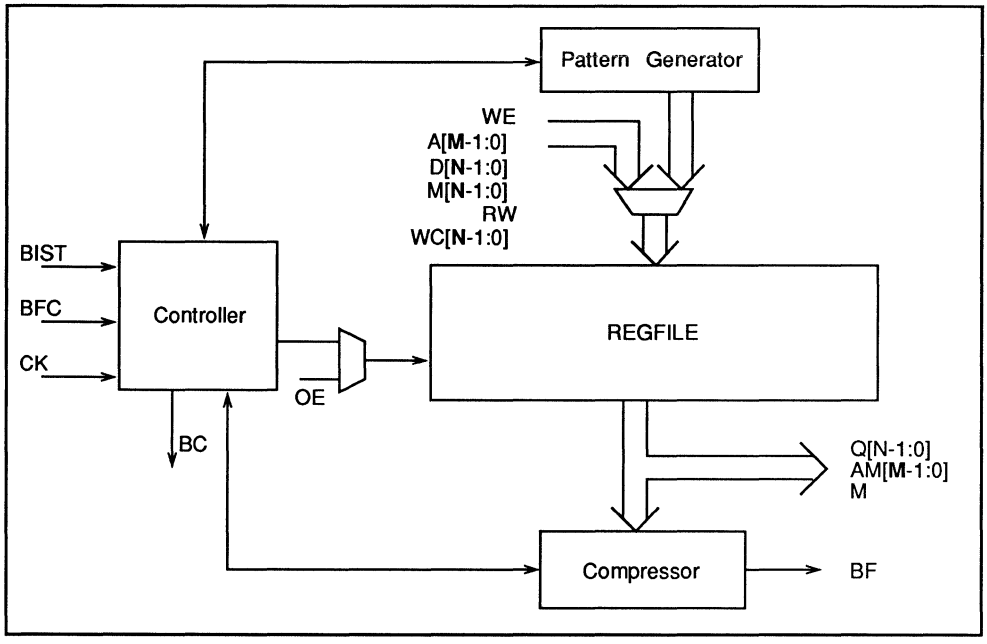
BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: BIST,BFC,A[M-1:0],D[N-1:0],M[N-1:0],RW,SM,CK,OE,WC[N-1:0]
OUTPUTS: Q[N-1:0],AM[M-1:0],M,BF,BC

Inputs

BIST	BIST control (BIST=1 active)
BFC	BIST flag check (BFC=1 active)
A[M-1:0]	Address in (A0 = LSB)
D[N-1:0]	Data in
M[N-1:0]	Match in
RW	Read/write (read = '1')
SM	Select macrocell (SM=1 active)
CK	Clock
OE	Output enable (OE=1 active; OE=0 3-stated)
WC[N-1:0]	Wild card (active-high)

Outputs

Q[N-1:0]	Data out
AM[M-1:0]	Address match
M	Match (1= match, 0 = no match)
BF	BIST flag
BC	BIST complete (BC=1 BIST complete)

CHARACTERISTICS

Since the BIST portion of the CAM consists of standard cells that are placed and routed during the normal layout of the entire device, it is not possible to precisely define all of the timing characteristics of this block. All of the BIST logic is synchronous, minimizing the hazards in layout. The final characterization is done in a manner consistent with the bulk of the standard-cell logic, namely, using CRITIC or timing simulation. All of the characteristic numbers given below are approximate, and may be either better or worse depending on the layout.

The parameters **N**, **M** and **W** are used in the following equations, which can be used to estimate the characteristics for a CAMB that is **W** words by **N** bits per word with **M** address bits, and **L** is the number of matching words.

Parameter	Value	Unit
Grids	836 + 48.4**N** + 53**M** (+ /-3)	Grids
BIST Test Length	$17 \times 2^{M} + 6N + 9$	CK Cycles
Block Height	14.6**W** + 712.65	µm
Block Width	31.6**N** + 43.75**M** + 366.75	µm
Block Transistors	9**NW** + **NM** + 210**N** + 47**W** + 115**M** + 560	
Block Power: **L** matches	$(8.8 \times 10^{-5}$ **NW** + 0.00095**W** + 0.0063**N** + 0.043) $\times F \times V_{DD}{}^{2}$ -6.3 $\times 10^{-4} \times$ **NL** $\times F \times V_{DD}{}^{2}$	mW
Block Power: deselected	(0.21**N** + 0.11**M** + 0.39) $\times F \times V_{DD}{}^{2}/1000$	mW
Input Capacitance		
A[**M**-1:0]	0.104	
D[**N**-1:0]	0.104	
M[**N**-1:0]	0.104	
RW	0.104	
CK†	2.1 + 0.4**M**+0.5**N**	
SM	0.104	
OE	0.104	
WC[**N**-1:0]	0.017**N**	pF
BIST†	0.9 + 0.9N + 0.3M	
BFC†	0.8	
Output Capacitance		
Q[**N**-1:0]	0.4	
AM[**M**-1:0]	0.4	
M	0.4	
BO	0.4	
BF	0.3	
BC	0.16	

† Capacitance includes 0.1 pF for each fanout within the standard cells.
All capacitances for performance-optimized standard cells.
V_{DD} = the power supply voltage, and **F** = the clock frequency, in MHz.

SWITCHING CHARACTERISTICS VDD=5.0V,T=25°C,NOM Processing				
Symbol	**From INPUT**	**To OUTPUT**	**Intrinsic ns**	**Extrinsic ns/pF**
CKAM	CK↑	AM[M-1:0]	3.9	0.5
CKM	CK↑	M	4.2	1.4
CKBO	CK↑	BO	5.3	0.6
CKQ	CK↑	Q[N-1:0]	2.3	0.5
OEDR	OE↑	Q[N-1:0],AM[M-1:0]	‡	‡
OEHZ	OE↓	Q[N-1:0],AM[M-1:0]	‡	NA
BFRF	CK↑	BF	1.2	0.7
BCRF	CK↑	BC	1.1	0.7

Above timing for performance-optimized standard cells.

‡ Unavailable at time of publication

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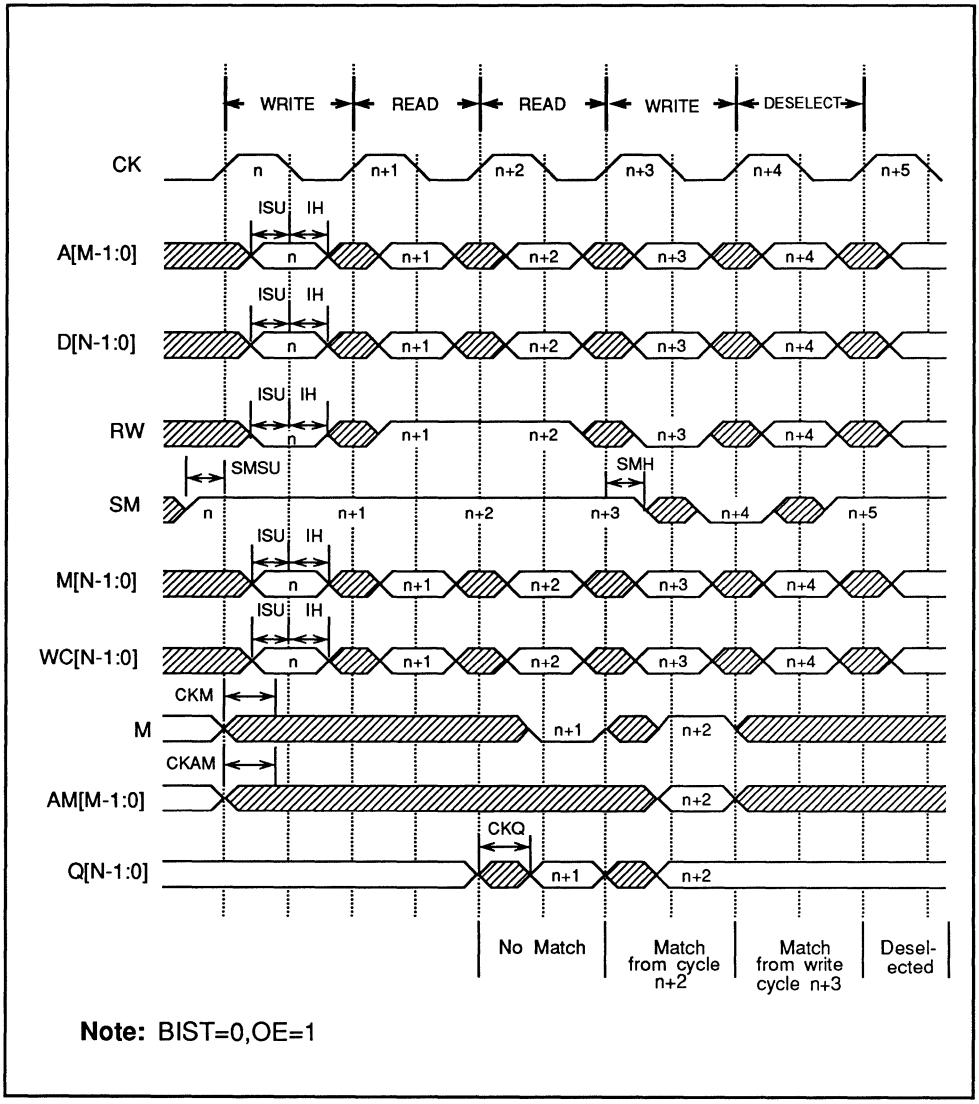
TIMING REQUIREMENTS VDD=5.0V,T=25°C,Nom Processing			
Symbol	**Description**	**Value**	**Unit**
ISU	A[M-1:0],D[N-1:0],M[N-1:0],RW setup before CK↓	2.6	
IH	A[M-1:0],D[N-1:0],M[N-1:0],RW hold after CK↓	0.0	
SMSU	SM setup before CK↑	2.6	
SMH	SM hold after CK↑	0.0	
CKPL	Minimum CK pulse low	13.4	
CKPH	Minimum CK pulse high	13.4	ns
BSU	BIST setup before CK↑	‡	
BH	BIST hold after CK↑	‡	
BFCSU	BFC setup before CK↑	‡	
BFCH	BFC hold after CK↑	‡	

Above timing for performance-optimized standard cells.

‡ Unavailable at time of publication

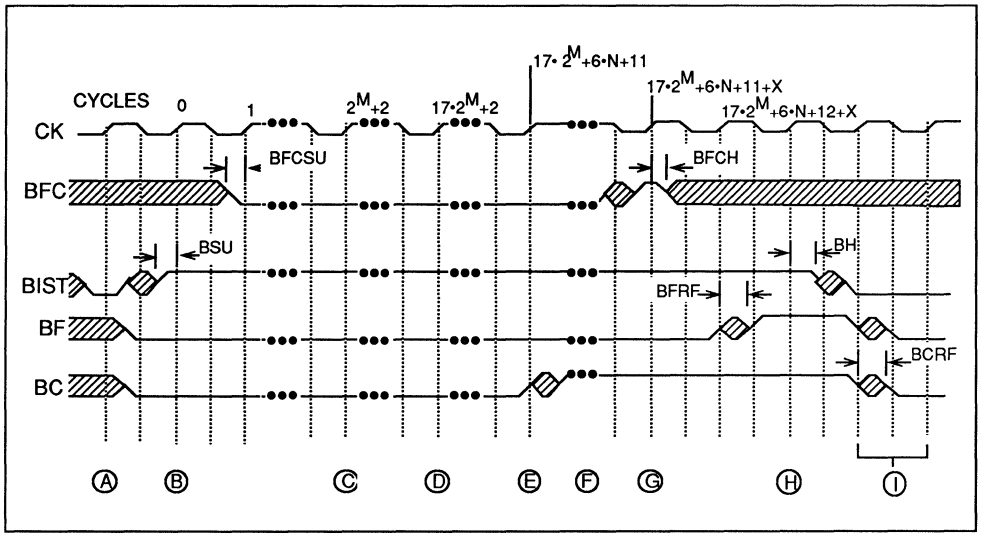
TIMING DIAGRAM

FUNCTIONAL OPERATION



Note: BIST=0,OE=1

BIST OPERATION



Ⓐ A low BIST signal must be latched into the CAM to properly start initializing it for BIST.

Ⓑ CAM is placed in the BIST mode.

Ⓒ The CAM contents have all been initialized by this clock cycle. This fact can be used to initialize all of the CAMs in a chip circuit. One can then take the CAM out of BIST mode and begin testing the entire circuit with known CAM contents.

Ⓓ Internal memory test is completed. BF may go high at anytime up to this point. If BF goes high, it will remain high. BIST checking now begins.

Ⓔ BIST overhead checking is now complete. BC will toggle high at this time. BF will also go high if any faults are detected here. As before, if BF goes high, it will remain high.

Ⓕ BF should be checked at this time. If it is high, the CAM is bad. One can wait any amount of time to make this check (call it X cycles).

Ⓖ BFC is toggled high to check for a stuck-at-0 fault on the BF output.

Ⓗ One cycle after a high BFC input has been latched into the CAM, the BF output should toggle high.

Ⓘ First valid access of the CAM after coming out of BIST should occur at this time

The remaining input signals not found above may have any logic value "0 or 1".

Outputs Q[N-1:0] will change with each read that occurs with the BIST vectors providing that the input OE is held at a logic value of "1". These outputs will also change on the positive edge of the clock CK.

USER NOTES

Characterization - For specific information on conditions of characterization, please refer to the introduction to this chapter under CHARACTERISTICS AND TIMING.

Function - Consult USER NOTES for the CAM for functional information.

BIST Algorithm - The BIST algorithm provides 100% fault coverage for stuck-at faults, transition faults, coupling faults, and addressing (decoder) faults. A more detailed explanation of the BIST algorithm is available through MACLOG.

Timing Issues - The layout of the BIST standard-cell circuitry will affect the performance during the application of the BIST test as well as the timing parameters in the normal mode. The BIST circuitry is synchronous, and therefore the layout will only affect the speed of the block, not its function.

The BIST places SD210 multiplexers in front of the normal I/O of the REGFILE to gain access during the BIST test. The clock (CK) does not get delayed.

BIST Interface - The BIST interface is identical to all of the macrocell BIST interfaces in terms of pins and logical timing. The interface is clocked from the positive edge of the clock, so there are half cycle timing considerations that must be accounted for when using the BIST at high clock rates.

Boundary Scan - This block can be interface with the BSBRIC if JTAG Boundary Scan is being used. See the Boundary Scan section of this catalog.

FUNCTIONAL DESCRIPTION AND FEATURES

FIFO is a parameterized first-in first-out memory function supported by automatic layout generation software. The synthesis of the FIFO is accomplished in two sections. The FIFO memory array is implemented as a custom, pitch-matched array of cells that is very area-efficient. The FIFO control and status logic is implemented as a standard-cell layout using performance-optimized cells.

FIFO has been designed specifically for use on standard-cell chips and has the following features:

- First-in first-out buffer memory
- Independent asynchronous inputs and outputs
- 3-state outputs
- Organized as W words of N bits
- Dual port RAM architecture
- Empty and full status flags

The FIFO can be customized with the following parameters:

Parameter	Description	Limit		
		Increment	Min	Max
N	Bits/Word	1	1	21
W	Words	8	16	512

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NOTE: This is a preliminary Data Sheet. Contact your AT&T representative for current information.

Parallel Multiplier MULTP

FUNCTIONAL DESCRIPTION AND FEATURES

MULTP is a parameterized, two's complement, parallel multiplier function supported by automatic layout generation software. The layout of the MULTP is implemented as a custom, pitch-matched array of cells that is very area-efficient.

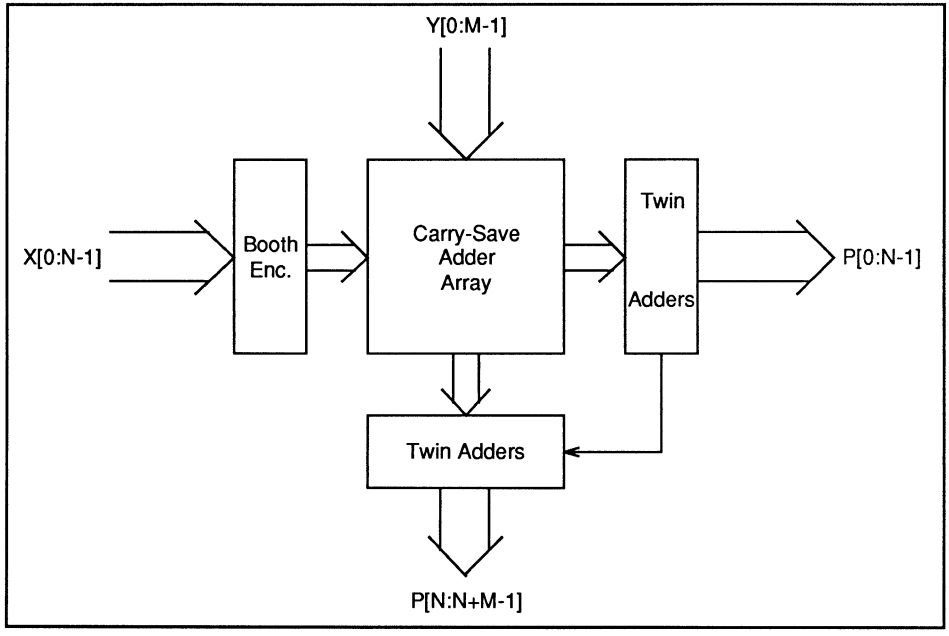
MULTP has been designed specifically for use on standard-cell chips and has the following features:

- Asynchronous operation
- Organized as N multiplier bits by M multiplicand bits
- Two's complement data format
- Three-bit Booth encoding of multiplier bits which halves the number of shift-adds needed
- Carry-save adder array generates partial products in parallel
- Fast twin adders using two-bit look-ahead technique are used for carry-propagate and final product generation

The MULTP can be customized with the following parameters:

Parameter	Description	Limit		
		Increment	Min	Max
N	Multiplier Bits	2	6	32
M	Multiplicand Bits	2	2	32

BLOCK DIAGRAM



NOTE: This is a preliminary Data Sheet. Contact your AT&T representative for current information.

FUNCTIONAL DESCRIPTION AND FEATURES

PLAC2B is a parameterized clocked PLA function supported by automatic mask layout generation software. The layout of the PLAC2B is implemented as a custom, pitch-matched array of cells that is very area-efficient.

The PLAC2B has been designed specifically for use on standard-cell chips, and has overhead circuitry already built-in including negative edge-triggered output latches and negative level-sense input latches. The PLAC2B can be used to implement sequential state machines.

The PLAC2B can be customized with the following parameters:

Parameter	Description	Limit		
		Increment	Min	Max
N	Data Inputs	1	1	N + M < 100
M	Data Outputs	1	1	N + M < 100
P	Product Terms	1	1	P < 200

NOTE: This is a preliminary Data Sheet. Contact your AT&T representative for current information

Register File REGFILE

FUNCTIONAL DESCRIPTION AND FEATURES

REGFILE is a parameterized, register file function supported by automatic mask layout generation software. The layout of the REGFILE is implemented as a custom, pitch-matched array of cells designed to be area-efficient.

REGFILE has been designed specifically for use on standard-cell chips and has the following features:

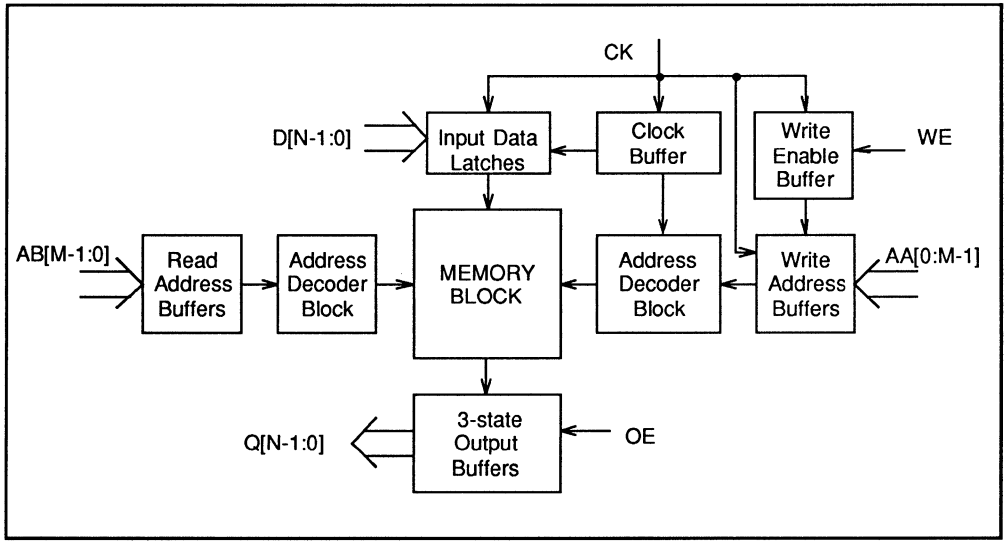
- Dual-port addressing permits simultaneous reading and writing
- Synchronous write operation through port A
- Asynchronous read operation through port B
- Negative edge-triggered input latches on port A for address, data, and write enable
- 3-statable outputs
- Requires a single clock for proper synchronous write operation

REGFILE can be customized by its number of words, **W**, and number of bits per word **N**. The valid range for these parameters is specified in the following table.

Parameters	Descriptions	Limits		
		Increment	Min	Max
W	Words	2	2	128
N	Bits/Word	1	1	32
M†	Address Bits	1	1	7

† The number of address bits, **M** = integer(log(**W**) / log(2)) + 1

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS:AA[**M**-1:0],D[**N**-1:0],WE,AB[**M**-1:0],OE,CK

OUTPUTS:Q[**N**-1:0]

Functional Descriptions

Inputs

AA[**M**-1:0]	Address bits on port A (write)
D[**N**-1:0]	Data inputs
WE	Write enable
AB[**M**-1:0]	Address bits on port B (read)
OE	Output enable
CK	Write clock

Outputs

Q[**N**-1:0]	Data outputs

CHARACTERISTICS

The parameters **W**, **N** and **M** can be used to estimate the characteristics for a REGFILE that is **W** words by **N** bits per word with **M** address bits.

Parameter	Value	Unit
Height	388+13**W**	µm
Width	205+28**N**+36**M**	µm
Transistors	90+19**W**+55**N**+84**M**+8**WN**+3**WM**	
Power†	(V_{DD} ^{2}/1000)×(69 +Fr(1.3+0.040**W**+1.3**N**+1.1**M**+0.008**WN**+0.034**WM**) +Fw(2.0+0.034**W**+0.7**N**+1.0**M**+0.010**WN**+0.037**WM**))	mW
Input Capacitance		
AA[**M**-1:0]	0.023	pF
D[**N**-1:0]	0.032	
WE	0.058	
AB[**M**-1:0]	0.192	
OE	0.078**N**	
CK	0.216+0.058**N**+0.046**M**	
Output Capacitance		
Q[**N**-1:0]	0.080	

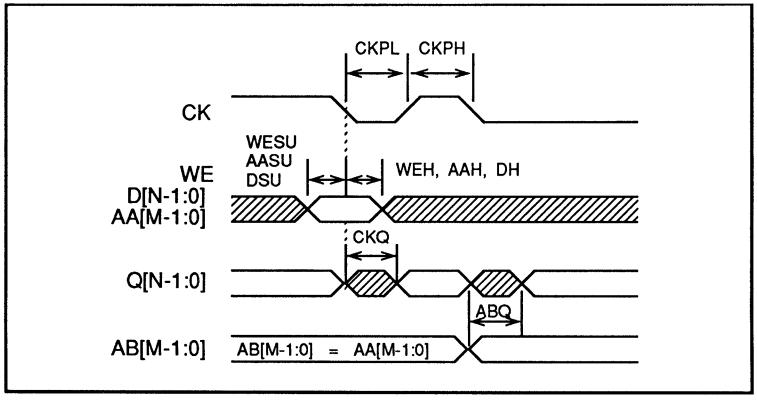
† V_{DD}=power supply potential (Volt), Fr=frequency of read access (MHz), and Fw=write clock frequency (MHz)

SWITCHING CHARACTERISTICS VDD=5.0V,T=25°C,Nom Processing				
Symbol	**From INPUT**	**To OUTPUT**	**Intrinsic ns**	**Extrinsic ns/pF**
ABQ	AB[**M**-1:0]	Q[**N**-1:0]	9.0+0.016**W**+0.04**N**+0.2**M**	0.24
CKQ	CK↓	Q[**N**-1:0]	6.6+0.05**W**+0.05**N**+0.02**M**	0.24
OEQ	OE	Q[**N**-1:0]	1.0	0.24
OEHIZ†	OE	Q[**N**-1:0]	1.0	

† OEHIZ is the time required before Q[**N**-1:0] is in the high impedance state.

TIMING REQUIREMENTS VDD=5.0V,T=25°C,Nom Processing			
Symbol	**Description**	**Value**	**Unit**
WESU	WE setup before CK↓	1.8+0.016**W**+0.1**M**	ns
WEH	WE hold after CK↓	0.0	
AASU	AA[**M**-1:0] setup before CK↓	1.8+0.016**W**+0.1**M**	
AAH	AA[**M**-1:0] hold after CK↓	0.0	
DSU	D[**N**-1:0] setup before CK↓	1.8+0.016**W**+0.03**N**	
DH	D[**N**-1:0] hold after CK↓	0.0	
CKPL	Minimum CK pulse low	1.5+0.006**W**+0.06**N**	
CKPH	Minimum CK pulse high	2.6+0.016**W**	

TIMING DIAGRAM



USER NOTES

Characterization - For specific information on conditions of characterization, please refer to the introduction to this chapter under CHARACTERISTICS AND TIMING.

BIST Availability - A standard-cell implementation of BIST circuit is available for REGFILE. The BIST version of the REGFILE is described under REGFILEB in this section of the catalog.

Test - If BIST is not used, the BIST algorithm is available from MACLOG to assist in vector writing. It is recommended that the entire BIST algorithm be used to test non BISTed REGFILEs.

Interfacing - The REGFILE is designed for synchronous operation with negative edge-triggered flip-flops driving the write port. The write port could also be driven by positive edge-triggered flip-flops, but care needs to be given to set up and hold times with the half-cycle clocking scheme. Since the READ port is not clocked, it may be driven by either asynchronous signals, or from internally derived addresses from either negative or positive edge flip-flops. The delay before data out (Q[**N**-1:0]) is valid, and is measured from the last READ ADDRESS that changed.

Single Port RAM mode - If the AA and AB address busses are tied together, the REGFILE acts like a single-port RAM. The write is synchronous, and the read is asynchronous. The output data Q[**N**-1:0] will change twice for every write; once when the address changes, and again when the new data is written.

BIST Register File REGFILEB

FUNCTIONAL DESCRIPTION AND FEATURES

BIST REGFILE is a parameterized register file function supported by automatic mask layout generation software. The layout of the BIST REGFILE is implemented as a REGFILE core, surrounded by standard-cell BIST logic. The output produced from this generator is XYMASK of a REGFILE, and an LSL which describes the interconnection of the core and the surrounding BIST logic.

BIST REGFILE has been designed specifically for use on standard-cell chips and has the following features:

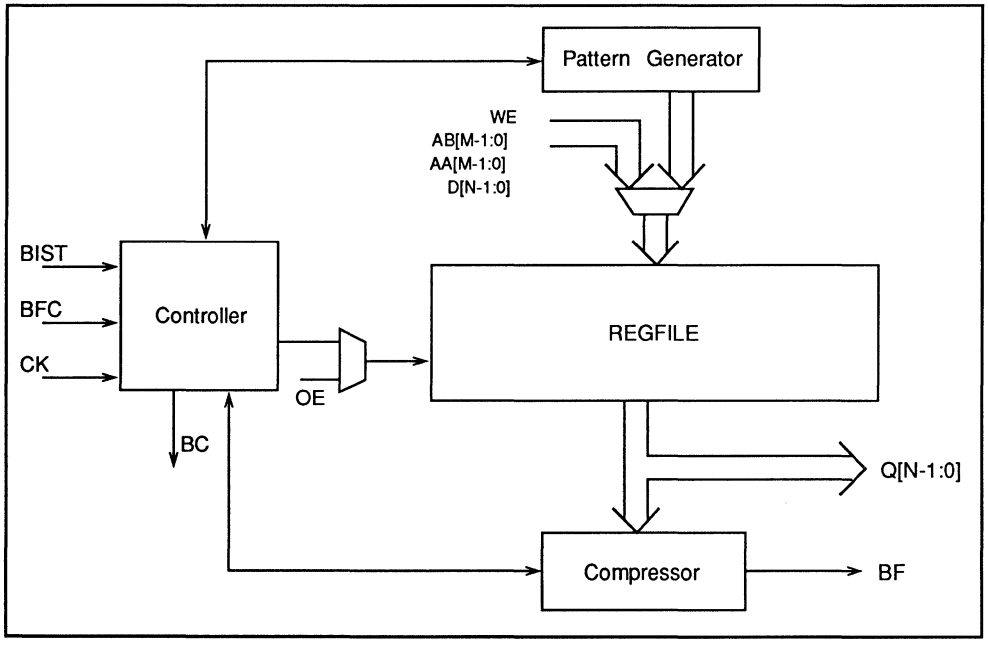
- Automatically generated BIST logic which tests itself and the core Register File
- Separate Read/Write addressing permits simultaneous reading and writing
- Asynchronous read operation
- 3-statable outputs
- Synchronous write operation requiring a single clock
- Organized as **W** words of **N** bits
- Negative edge-triggered address and input data registers

REGFILE can be customized with parameters **N** and **W** of the following table:

Parameters	Descriptions	Limits		
		Increment	Min	Max
W	Words	1	8	128
N	Bits/Word	1	3	32
M†	Address Bits	1	3	7

† The number of address bits, **M** = integer(log(**W**) / log(2)) + 1

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: BIST,BFC,AA[M-1:0],D[N-1:0],WE,AB[M-1:0],OE,CK

OUTPUTS: Q[N-1:0],BF,BC

Functional Descriptions

Inputs

BIST	BIST test mode (active-high)
BFC	BIST flag check (active-high)
AA[M-1:0]	Address bits on port A (write)
D[N-1:0]	Data inputs
WE	Write enable
AB[M-1:0]	Address bits on port B (read)
OE	Output enable
CK	Write clock

Outputs

Q[N-1:0]	Data outputs
BF	BIST flag
BC	BIST complete (BIST test complete = '1')

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CHARACTERISTICS

Since the BIST portion of the REGFILE consists of standard cells that are placed and routed during the normal layout of the entire device, it is not possible to precisely define all of the characteristics of this block. All of the BIST logic is synchronous, minimizing the hazards in layout. The final characterization is done in a manner consistent with the bulk of the standard-cell logic, namely, using CRITIC or timing simulation. All of the characteristic numbers given below are approximate, and may be either better or worse depending on the layout.

Parameter	Value	Unit
Grids	462+29**N**+45**M**+3.52**N**+1.76**M** (+/- 3)	Grids
BIST Test Length	17*(2**M)+4*N+2	CK Cycles
Block Height	388+13**W**	µm
Block Width	205+28**N**+36**M**	µm
Block Transistors	90+19**W**+55**N**+84**M**+8**WN**+3**WM**	
Block Power††	(V_{DD} ^{2}/1000)×(69.1 +Fr(1.3+0.040**W**+1.3**N**+1.1**M**+0.008**WN**+0.034**WM**) +Fw(2.0+0.034**W**+0.7**N**+1.0**M**+0.010**WN**+0.037**WM**))	mW
Input Capacitance		
BIST	3.7+0.6**M**†	
BFC	0.104	
AA[**M**-1:0]	0.104	
D[**N**-1:0]	0.102	pF
WE	0.104	
AB[**M**-1:0]	0.104	
OE	0.102	
CK	2.7+0.36(**M**+**N**)†	
Output Capacitance		
Q[**N**-1:0]	0.4†	
BF	0.171	pF
BC	0.160	

†† V_{DD}=power supply potential (Volt), Fr=frequency of read access (MHz), and Fw=write clock frequency (MHz)

† Includes ~.1pF routing capacitance per fan-out

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SWITCHING CHARACTERISTICS VDD=5.0V,T=25°C,Nom Processing				
Symbol	**From INPUT**	**To OUTPUT**	**Intrinsic ns**	**Extrinsic ns/pF**
ABQ	AB[**M**-1:0]	Q[**N**-1:0]	9.1+0.016**W**+0.04**N**+0.2**M**†	0.24
CKQ	CK↓	Q[**N**-1:0]	6.7+0.05**W**+0.05**N**+0.02**M**†	0.24
BFRF	CK↑	BF	1.2	0.7
BCRF	CK↑	BC	1.1	0.7
OEQ	OE	Q[**N**-1:0]	1.0	0.24
OEHIZ††	OE	Q[**N**-1:0]	1.0	

† Includes 0.1pF routing capacitance

†† OEHIZ is the time required before Q[**N**-1:0] is in the high impedance state.
Above timing for performance-optimized standard cells only

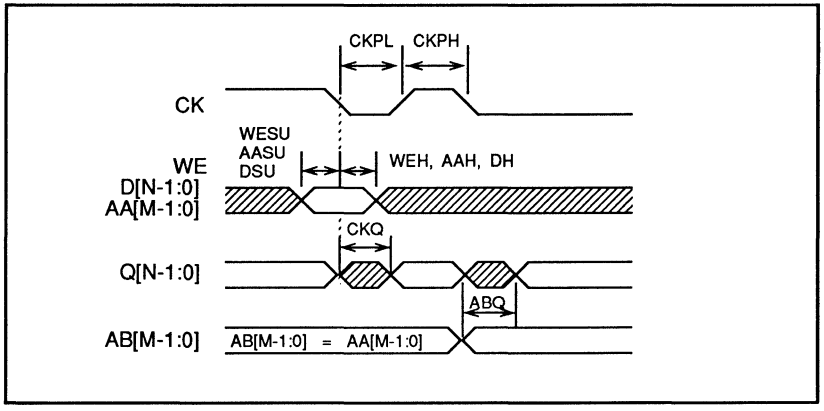
TIMING REQUIREMENTS VDD=5.0V,T=25°C,Nom Processing			
Symbol	**Description**	**Value**	**Unit**
WESU	WE setup before CK†	2.8+0.016**W**+0.1**M**†	ns
WEH	WE hold after CK†	0.0	
AASU	AA[**M**-1:0] setup before CK†	2.8+0.016**W**+0.1**M**†	
AAH	AA[**M**-1:0] hold after CK†	0.0	
DSU	D[**N**-1:0] setup before CK†	2.8+0.016**W**+0.03**N**†	
DH	D[**N**-1:0] hold after CK†	0.0	
BFCSU	BFC setup before CK↑	3.0	
BFCH	BFC hold after CK↓	0.0	
BSU	BIST setup before CK↑	7.0	
BH	BIST hold after CK↑	0.0	
CKPL	Minimum CK pulse low	1.5+0.006**W**+0.06**N**††	
CKPH	Minimum CK pulse high	2.6+0.016**W**††	

† Includes 1 ns delay to account for the routing dependent BIST circuitry

†† BIST circuitry may require powering up to obtain this Minimum CK Pulse Width.
Above timing for performance-optimized standard cells only

TIMING DIAGRAMS

FUNCTIONAL OPERATION



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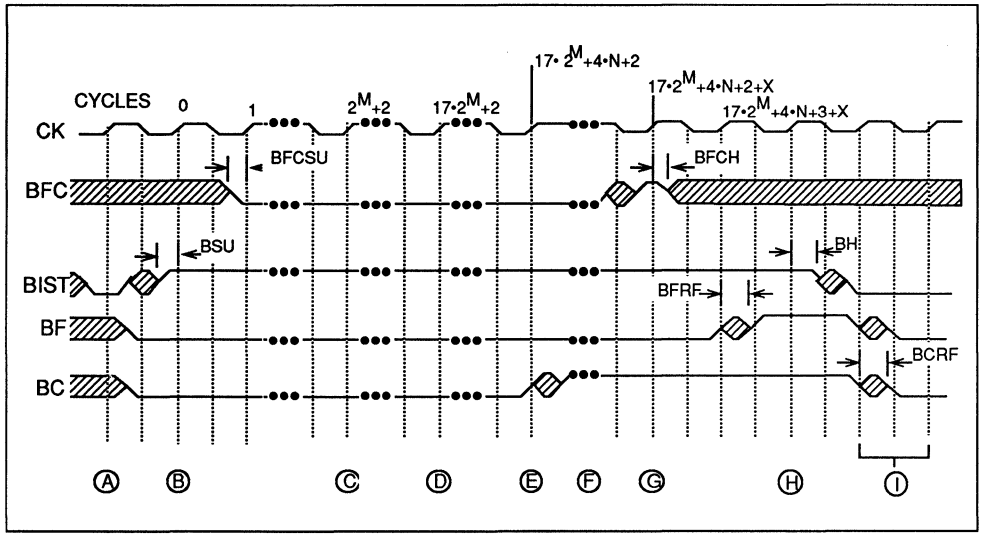
BIST OPERATION



Ⓐ A low BIST signal must be latched into the REGFILE to properly start initializing it for BIST.

Ⓑ REGFILE is placed in the BIST mode.

Ⓒ The REGFILE contents have all been initialized by this clock cycle. This fact can be used to initialize all of the REGFILEs in a chip circuit. One can then take the REGFILE out of BIST mode and begin testing the entire circuit with known REGFILE contents.

Ⓓ Internal memory test is completed. BF may go high at anytime up to this point. If BF goes high, it will remain high. BIST checking now begins.

Ⓔ BIST overhead checking is now complete. BC will toggle high at this time. BF will also go high if any faults are detected here. As before, if BF goes high, it will remain high.

Ⓕ BF should be checked at this time. If it is high, the REGFILE is bad. One can wait any amount of time to make this check (call it X cycles).

Ⓖ BFC is toggled high to check for a stuck-at-0 fault on the BF output.

Ⓗ One cycle after a high BFC input has been latched into the REGFILE, the BF output should toggle high.

Ⓘ First valid access of the REGFILE after coming out of BIST should occur at this time

The remaining input signals not found above may have any logic value "0 or 1".

Outputs Q[N-1:0] will change with each read that occurs with the BIST vectors providing that the input OE is held at a logic value of "1". These outputs will also change on the positive edge of the clock CK.

USER NOTES

Characterization - For specific information on conditions of characterization, please refer to the introduction to this chapter under CHARACTERISTICS AND TIMING.

BIST Algorithm - The BIST algorithm provides 100% fault coverage for stuck-at faults, transition faults, coupling faults, and addressing (decoder) faults. A more detailed explanation of the BIST algorithm is available through MACLOG.

Timing Issues - Since the internodal capacitances are determined during layout, the layout of the BIST circuitry will affect the performance of the BIST mode as well as the timing parameters in the normal mode. Since the BIST circuitry is synchronous the layout will only affect the speed of the block, not its function.

The BIST places SD210 and SD211 multiplexers in front of the normal I/O of the REGFILE to gain access during the BIST test. The clock (CK) does not get delayed.

BIST Interface - The BIST interface is standardized in terms of pins and logical timing for all macrocells. The interface is clocked from the positive edge of the clock, so there are half-cycle timing considerations that must be looked at when using the BIST at high clock rates.

Boundary Scan - This block can be interface to the BSBRIC if Boundary Scan is used.

Multicell BIST - The BIST standard-cell logic may be shared between more than one REGFILE of the same configuration. The user must modify the BIST circuitry to take advantage of this.

FUNCTIONAL DESCRIPTION AND FEATURES

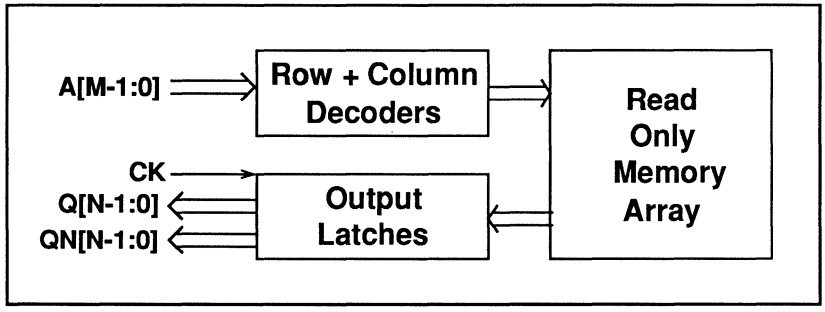
ROMS1A is a parameterized static fully decoded ROM function supported by automatic layout generation software. The layout of the ROMS1A is implemented as a custom, pitch-matched array of cells that is very area-efficient.

The ROMS1A has been designed specifically for use on standard-cell chips, and as such, has overhead circuitry already built-in including positive edge-triggered output latches and full column and row decoding. Input latches are NOT included with the ROMS1A. Addresses should be latched with standard-cell flip-flops.

The ROMS1A can be customized with the following parameters:

Parameter	Description	Limit		
		Increment	Min	Max
N	Bits/Word	1	2	32
M	Address bits	1	6	11
W	Words	2^M	64	2048

BLOCK DIAGRAM



NOTE: This is a preliminary Data Sheet. Contact your AT&T representative for current information

STATIC RANDOM ACCESS MEMORY SRAM

FUNCTIONAL DESCRIPTION AND FEATURES

SRAM is a parameterized static RAM function supported by automatic mask layout generation software. The layout of the SRAM is implemented as a custom, pitch-matched array of cells that uses two-level metal and is very area-efficient.

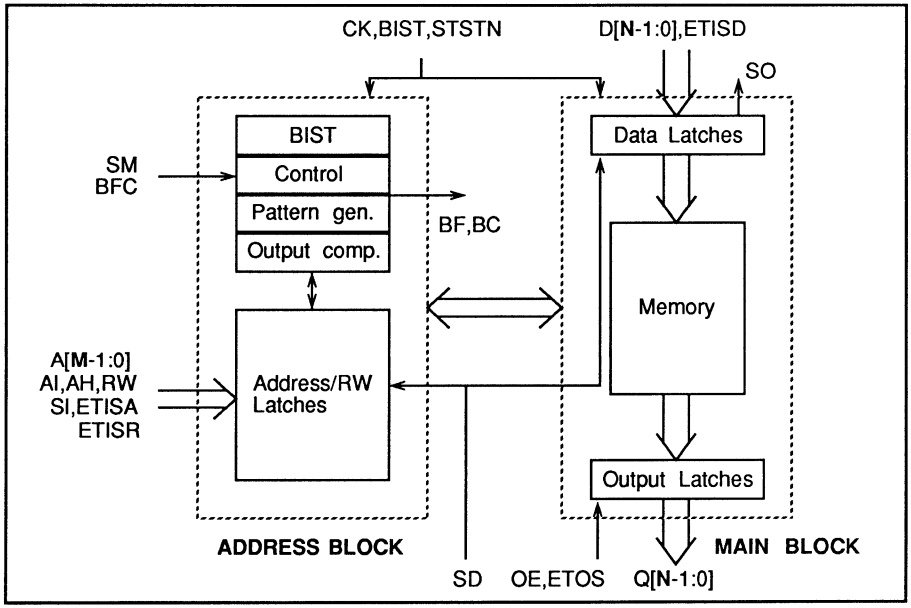
The SRAM has been designed specifically for use on standard-cell chips, and as such, has overhead circuitry already built-in including:

- Built-In self-test mode
- Selectable positive/negative edge-triggered input latches
- Selectable positive/negative edge-triggered address latches
- Selectable positive/negative edge-triggered read-write latch
- Selectable positive/negative edge-triggered output latches
- Column and row decoding
- A single clock
- Address increment (AI) mode
- Address hold (AH) mode
- Select macrocell (SM) mode
- 3-statable outputs
- Scan-test mode

SRAM can be customized by its number of words, **W**, and number of bits per word **N**. The valid range for these parameters are specified in the following table.

Parameters	Descriptions	Limits		
		Increment	Min	Max
W	Words	8	8	1,024
N	Bits/Word	1	2	64
M	Address Bits	1	3	10

BLOCK DIAGRAM



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TERMINAL DESCRIPTIONS

Netlist Order

INPUTS:	A[M-1:0],D[N-1:0],RW,SM,CK,OE,ETISA,ETISD,ETISR,ETOS, AI,AH,BFC,BIST,SI,SD,STSTN
OUTPUTS:	Q[N-1:0],BF,BC,SO

Inputs

A[M-1:0]	Address in (A0 = LSB)
D[N-1:0]	Data in
RW	Read/write (Read = '1')
SM	Select macrocell (active-high)
CK	Clock
OE	Output enable (active-high; output 3-stated when low)
ETISA	Positive edge-triggered input select for addresses (active-high)
ETISD	Positive edge-triggered input select for data (active-high)
ETISR	Positive edge-triggered input select for read/write (active-high)
ETOS	Positive edge-triggered output select (active-high)
AI	Address increment (active-high)
AH	Address hold (active-high)
BFC	BIST flag check (active-high)
BIST	BIST test mode (active-high)
SI	Scan-in data
SD	Select data (active-high)
STSTN	Scan-test mode (active-low)

Outputs

Q[N-1:0]	Data out
BF	BIST flag (good device)
BC	BIST complete (BIST test completed = '1')
SO	Scan-out data

CHARACTERISTICS

The parameters **W**, **N** and **M** can be used to estimate the characteristics for an SRAM that is **W** words by **N** bits per word with **M** address bits.

Parameter	Value	Unit
Address block		
Height	254.25	µm
Width	840.30+61.4**M**	µm
Transistors	1840+191**M**	
Main block		
Height	740.10+(31.7/8)**W**	µm
Width	204.80+53.2**N**+7.1**M**	µm
Transistors	488+490**N**+46**M**+4.25**W**+6**NW**+0.25**MW**	
Power†		
Functional Mode	$(VDD^2F/1000)\times$(17.0 +2.64**M**+0.17**W**+10.2**N**+0.00845**NW** +0.00455**MW**+2.96/**W**)	mW
Deselected Mode	$(VDD^2F/1000)\times$(0.768 +0.0052**M**+0.000407**W**+2.552**N**)	mW
BIST Test Length	10×2^{M}+4**N**+12	CK cycles
Input Capacitance		
A[**M**-1:0]	0.241	
D[**N**-1:0]	0.144	
RW	0.280	
SM	0.136	
CK	3.400+0.440**N**+0.323**M**	
OE	0.049+0.191**N**+0.001**M**	
ETISA	0.112**M**	
ETISD	0.058+0.033**N**+0.001**M**	
ETISR	0.126	pF
ETOS	0.061+0.090**N**+0.001**M**	
AI	0.091	
AH	0.080	
BFC	0.040	
BIST	1.398+0.241**N**+0.002**M**	
SI	0.060	
SD	0.125+0.124**N**+0.073**M**	
STSTN	0.240+0.073**N**+0.001**M**	
Output Capacitance		
Q[**N**-1:0]	0.097	
BF	0.119	
BC	0.209+0.008**M**	pF
SO	0.180	

† V_{DD}=power supply potential (Volt) and F=frequency of clock (MHz).

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°, Nom Processing					
Symbol	**From INPUT**	**To OUTPUT**	**ETOS Logic Value**	**Intrinxic ns**	**Extrinsic ns/pF**
QRF	CK↑	Q[**N**-1:0]	1	1.6†	0.13
	CK↓	Q[**N**-1:0]	0	7.75+0.041**N**+0.0013(**W-NM**)	0.13
SORF	CK↑	SO	N/A	1.0	0.72
BFRF	CK↑	BF	N/A	1.2	0.51
BCRF	CK↑	BC	N/A	1.3+0.004**M**	0.51
OEQRF	OE↑	Q[**N**-1:0]	N/A	0.8	N/A
OEQZ	OE↓	Q[**N**-1:0] Tri-State	N/A	1.3	N/A

† In situations where the actual clock pulse width low (call it PWL) is less than (CORR=7.75+0.041**N**+0.0013**W** - 00013**NM**), then add (CORR - PWL).

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Timing Requirements VDD = 5.0V, T = 25° C, Nom Process						
Symbol	**Definition**	**ETIS[A,D,R] Logic Value**	**From**	**To**	**Value**	**Units**
CKPH	Minimum CK Pulse High	N/A	CK↑	CK↓	5	ns
CKPL	Minimum CK Pulse Low	N/A	CK↓	CK↑	6	
CKP	Minimum CK Period	N/A	CK↓	CK↓	10.1+0.079N+0.003W -0.0055NM+0.000016NW	
CKSR	Minimum CK Slope for Rise	N/A	20% CK↑	80% CK↑	15	
CKSF	Minimum CK Slope for Fall	N/A	20% CK↓	80% CK↓	15	
ASU	A[M-1:0] setup before CK↑	ETISA=1	A[M-1:0]	CK↑	1.7	ns
	A[M-1:0] setup before CK↓	ETISA=0	A[M-1:0]	CK↓	4.2	
AH	A[M-1:0] hold after CK↑	ETISA=1	A[M-1:0]	CK↑	0.0	ns
	A[M-1:0] hold after CK↓	ETISA=0	A[M-1:0]	CK↓	0.0	
DSU	D[N-1:0] setup before CK↑	ETISD=1	D[N-1:0]	CK↑	1.7	ns
	D[N-1:0] setup before CK↓	ETISD=0	D[N-1:0]	CK↓	1.1	
DH	D[N-1:0] hold after CK↑	ETISD=1	D[N-1:0]	CK↑	0.0	ns
	D[N-1:0] hold after CK↓	ETISD=0	D[N-1:0]	CK↓	0.0	
RWSU	RW setup before CK↑	ETISR=1	RW	CK↑	1.6	ns
	RW setup before CK↓	ETISR=0	RW	CK↓	2.6	
RWH	RW hold after CK↑	ETISR=1	RW	CK↑	0.0	ns
	RW hold after CK↓	ETISR=0	RW	CK↓	0.0	
SMSU	SM setup before CK↑	N/A	SM	CK↑	1.8	ns
SMH	SM hold after CK↑	N/A	SM	CK↑	0.0	
EISU	ETIS[A,D,R] setup before CK↓	N/A	ETIS[A,D,R]	CK↓	†	ns
EIH	ETIS[A,D,R] hold after CK↓	N/A	ETIS[A,D,R]	CK↓	†	
EOSU	ETOS setup before CK	N/A	ETOS	CK	†	ns
EOH	ETOS hold after CK	N/A	ETOS	CK	†	
AISU	AI setup before CK↑	N/A	AI	CK↑	2.3+0.35M	ns
AIH	AI hold after CK↑	N/A	AI	CK↑	0.0	
AHSU	AH setup before CK↑	N/A	AH	CK↑	2.8+0.43M	ns
AHH	AH hold after CK↑	N/A	AH	CK↑	0.0	
BFCSU	BFC setup before CK↑	N/A	BFC	CK↑	1.0	ns
BFCH	BFC hold after CK↑	N/A	BFC	CK↑	0.0	
BSU	BIST setup before CK↑	N/A	BIST	CK↑	1.9	ns
BH	BIST hold after CK↑	N/A	BIST	CK↑	0.0	
SISU	SI setup before CK↑	N/A	SI	CK↑	1.7	ns
SIH	SI hold after CK↑	N/A	SI	CK↑	0.0	
SDSU	SD setup before CK↑	N/A	SD	CK↑	2.0	ns
SDH	SD hold after CK↑	N/A	SD	CK↑	0.0	
SSU	STSTN setup before CK	N/A	STSTN	CK	†	ns
SH	STSTN hold after CK	N/A	STSTN	CK	†	

† ETIS[A,D,R], ETOS, and STSTN are normally DC control signals. They can be toggled with some care if the need arises.

MODE SELECTIONS

The SRAM can be set up in several modes with the combined use of mode selection inputs AI, AH, ETIS, ETOS, STSTN, and BIST. The following table summarizes these modes and directs the user to the corresponding timing diagram:

Mode Selection	Input Settings								Timing
	AI	AH	ETISA	ETISD	ETISR	ETOS	STSTN	BIST	Diag.
Func.: + edge-trig A,D,RW inputs; + edge-trig Q	0	0	1	1	1	1	1	0	1
Func.: + edge-trig A,D inputs; - edge-trig RW input; + edge-trig Q	0	0	1	1	0	1	1	0	2
Func.: + edge-trig A,RW inputs; - edge-trig D input; + edge-trig Q	0	0	1	0	1	1	1	0	3
Func.: + edge-trig A input; - edge-trig D,RW inputs; + edge-trig Q	0	0	1	0	0	1	1	0	4
Func.: + edge-trig D,RW inputs; - edge-trig A input; + edge-trig Q	0	0	0	1	1	1	1	0	5
Func.: + edge-trig D input; - edge-trig A,RW inputs; + edge-trig Q	0	0	0	1	0	1	1	0	6
Func.: + edge-trig RW input; - edge-trig A,D inputs; + edge-trig Q	0	0	0	0	1	1	1	0	7
Func.: - edge-trig A,D,RW inputs; + edge-trig Q	0	0	0	0	0	1	1	0	8
Func.: + edge-trig A,D,RW inputs; - edge-trig Q	0	0	1	1	1	0	1	0	9
Func.: + edge-trig A,D inputs; - edge-trig RW input; - edge-trig Q	0	0	1	1	0	0	1	0	10
Func.: + edge-trig A,RW inputs; - edge-trig D input; - edge-trig Q	0	0	1	0	1	0	1	0	11
Func.: + edge-trig A input; - edge-trig D,RW inputs; - edge-trig Q	0	0	1	0	0	0	1	0	12
Func.: + edge-trig D,RW inputs; - edge-trig A input; - edge-trig Q	0	0	0	1	1	0	1	0	13
Func.: + edge-trig D input; - edge-trig A,RW inputs; - edge-trig Q	0	0	0	1	0	0	1	0	14
Func.: + edge-trig RW input; - edge-trig A,D inputs; - edge-trig Q	0	0	0	0	1	0	1	0	15
Func.: - edge-trig A,D,RW inputs; - edge-trig Q	0	0	0	0	0	0	1	0	16
Func.: + edge-trig A input with add. increment	1	0	1	X	X	X	1	0	17
Func.: + edge-trig A input with constant address	X	1	1	X	X	X	1	0	17
Func.: + edge-trig A,D,RW inputs; + edge-trig Q with add increment	1	0	1	1	1	1	1	0	17
Func.: + edge-trig A,D inputs; - edge-trig RW inputs; + edge-trig Q with add increment	1	0	1	1	0	1	1	0	18
Func.: + edge-trig A,RW inputs; - edge-trig D inputs; + edge-trig Q with add increment	1	0	1	0	1	1	1	0	19
Func.: + edge-trig A inputs; - edge-trig D,RW inputs; + edge-trig Q with add increment	1	0	1	0	0	1	1	0	20
Func.: + edge-trig A,D,RW inputs; - edge-trig Q with add increment	1	0	1	1	1	0	1	0	21
Func.: + edge-trig A,D inputs; - edge-trig RW inputs; - edge-trig Q with add increment	1	0	1	1	0	0	1	0	22
Func.: + edge-trig A,RW inputs; - edge-trig D inputs; - edge-trig Q with add increment	1	0	1	0	1	0	1	0	23
Func.: + edge-trig A inputs; - edge-trig D,RW inputs; - edge-trig Q with add increment	1	0	1	0	0	0	1	0	24
Scan-Test:	X	X	0	0	0	X	0	0	25
Built-In Self-Test:	X	X	X	X	X	X	X	1	26
Initialization of SRAM on power-up:	X	X	X	X	X	X	X	1	27

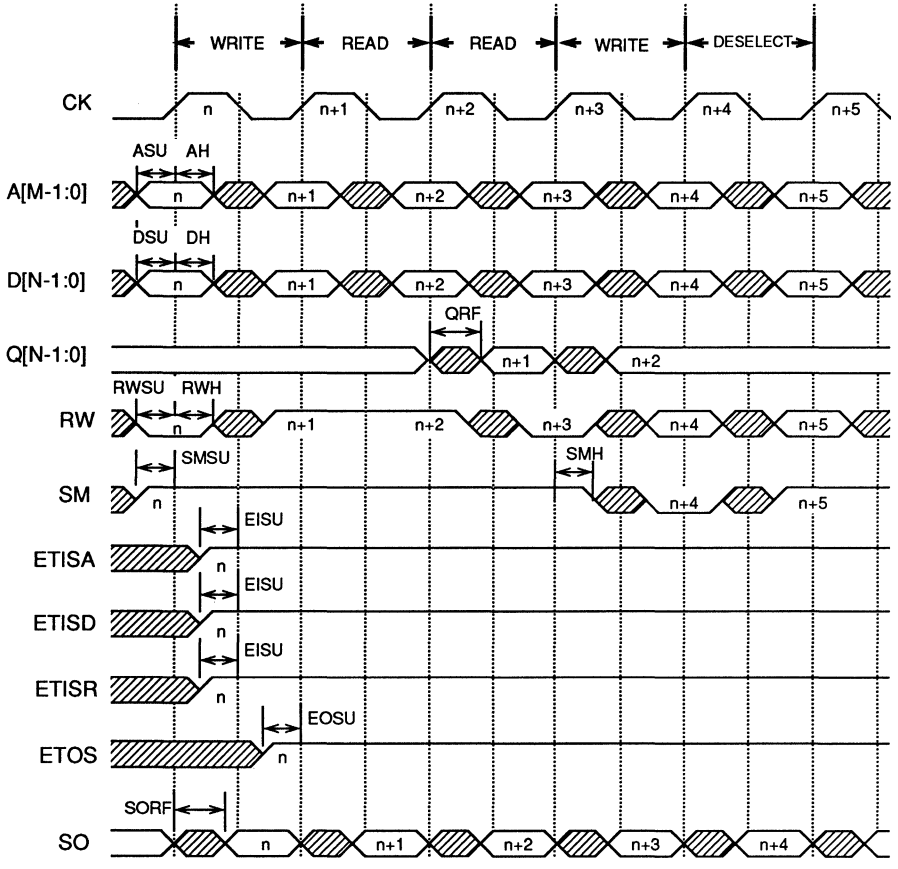
8

CROSS-REFERENCE GUIDE TO PREVIOUS CMOS TECHNOLOGIES

Several versions or subtypes of SRAMs were available in the 1.25, 1.75, and 2.5 µm CMOS technologies. A cross-reference guide is provided here for those familiar with the previous versions, and for those who wish to convert or borrow from a previous design. The outputs are assumed to be continuously enabled (OE is set high).

Subtype	Input Settings						Additional External Requirements
	AI	AH	ETISA ETISD ETISR	ETOS	STSTN	BIST	
RAMS1A	0	0	1	1	1	0	None
RAMS1B	0	0	0	1	1	0	None
RAMS1C	0	0	1	0	1	0	None
RAMS1D	0	0	0	0	1	0	None
RAMS1E	0	0	1	1	X	0	None
RAMS1F	0	0	1	0	X	0	None
RAMS2A	0	0	1	1	1	0	Invert clock to SRAM and add FD1S1As (clocked by original non-inverted clock) before the A[**M**-1:0], D[**N**-1:0], and RW inputs
RAMS2B	0	0	0	1	1	0	Invert clock to SRAM and add FDIS5As (clocked by original non-inverted clock) before the A[**M**-1:0], D[**N**-1:0], and RW inputs
RAMS2C	0	0	1	0	1	0	Invert clock to SRAM and add FD1S1As (clocked by original non-inverted clock) before the A[**M**-1:0], D[**N**-1:0], and RW inputs
RAMS2D	0	0	0	0	1	0	Invert clock to SRAM and add FD1S5As (clocked by original non-inverted clock) before the A[**M**-1:0], D[**N**-1:0], and RW inputs
RAMS2E	0	0	1	1	X	0	Invert clock to SRAM and add FD1S1As (clocked by original non-inverted clock) before the A[**M**-1:0], D[**N**-1:0], and RW inputs
RAMS2F	0	0	1	0	X	0	Invert clock to SRAM and add FD1S5As (clocked by original non-inverted clock) before the A[**M**-1:0], D[**N**-1:0], and RW inputs
RAMS1AT	0	0	1	1	1	X	None
RAMS1CT	0	0	1	0	1	X	None
RAMS1ET	0	0	1	1	X	X	None

Timing Diagram 1
Functional: + edge-trig A,D,RW inputs; + edge-trig Q



The remaining input signals not found above should have the following logic values:

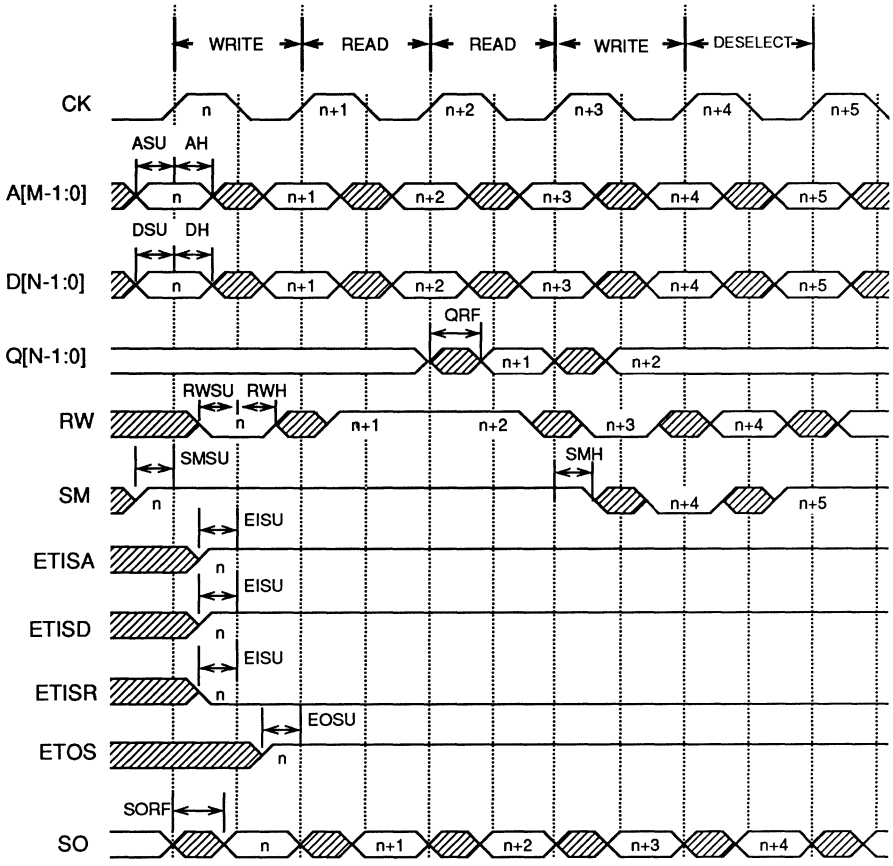
"0": AI, AH, BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

Output SO is the latched output of the most significant data input bit D[N-1:N -1]. It should be used only during scan testing.

Timing Diagram 2

Functional: + edge-trig A,D inputs;
- edge-trig RW input; + edge-trig Q



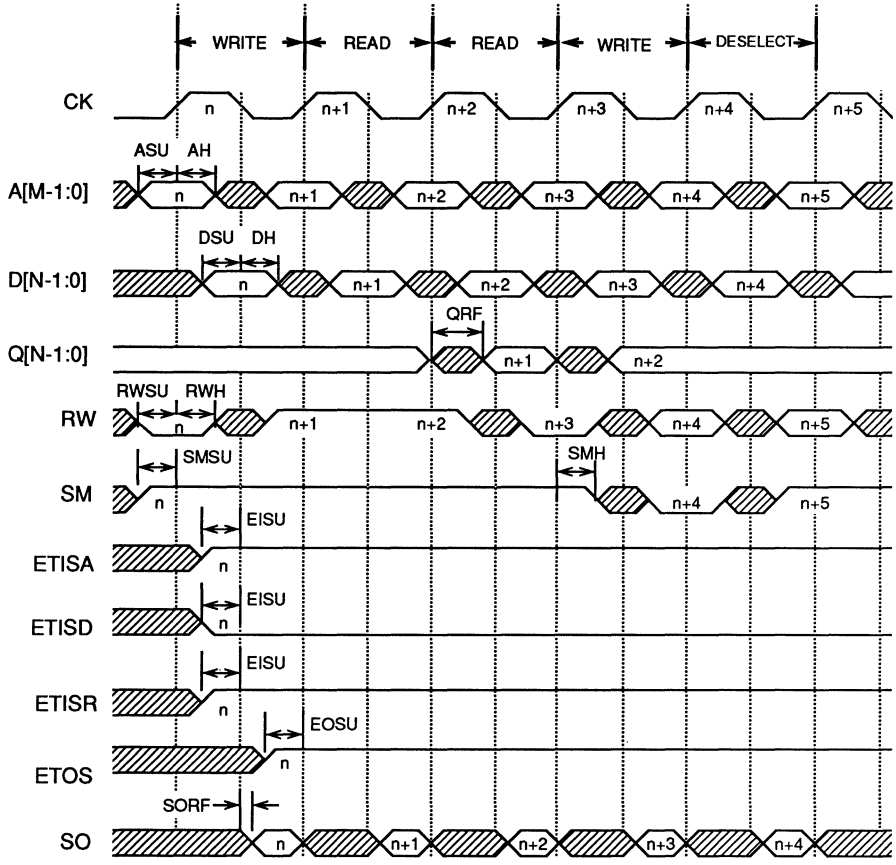
The remaining input signals not found above should have the following logic values:

"0": AI, AH, BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

Output SO is the latched output of the most significant data input bit D[N-1:N -1]. It should be used only during scan testing.

Timing Diagram 3
Functional: + edge-trig A,RW inputs;
- edge-trig D input; + edge-trig Q



The remaining input signals not found above should have the following logic values:

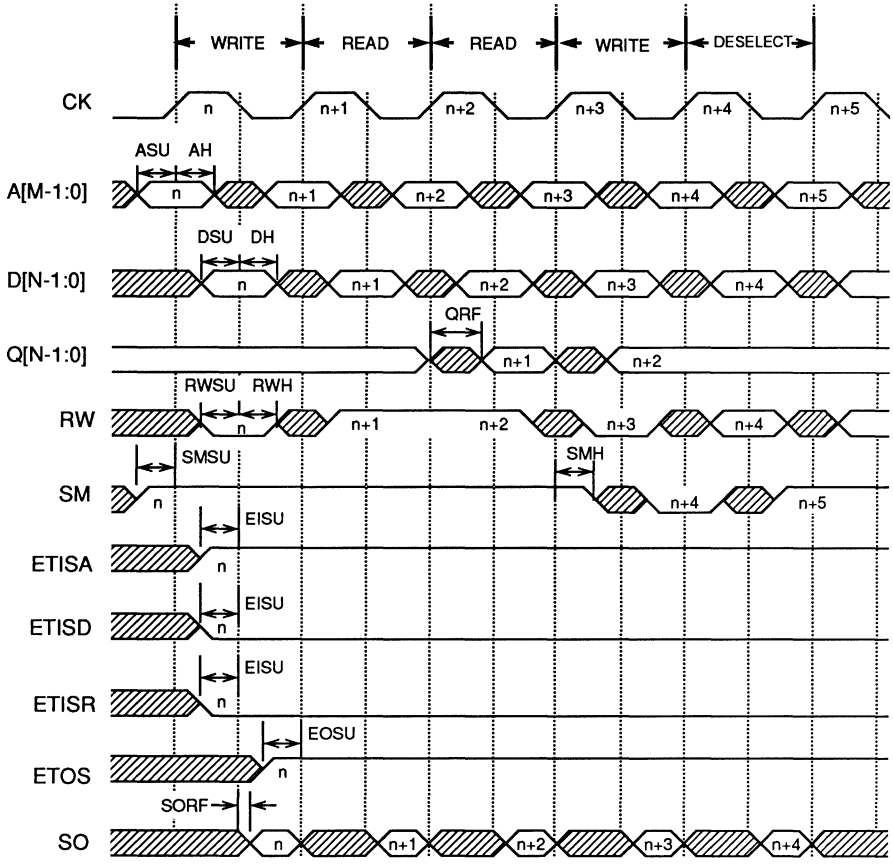
"0": AI, AH, BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

Output SO is the latched output of the most significant data input bit D[N-1:N -1]. It should be used only during scan testing.

Timing Diagram 4

Functional: + edge-trig A input;
- edge-trig D,RW inputs; + edge-trig Q



The remaining input signals not found above should have the following logic values:

"0": AI, AH, BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

Output SO is the latched output of the most significant data input bit D[N-1:N -1]. It should be used only during scan testing.

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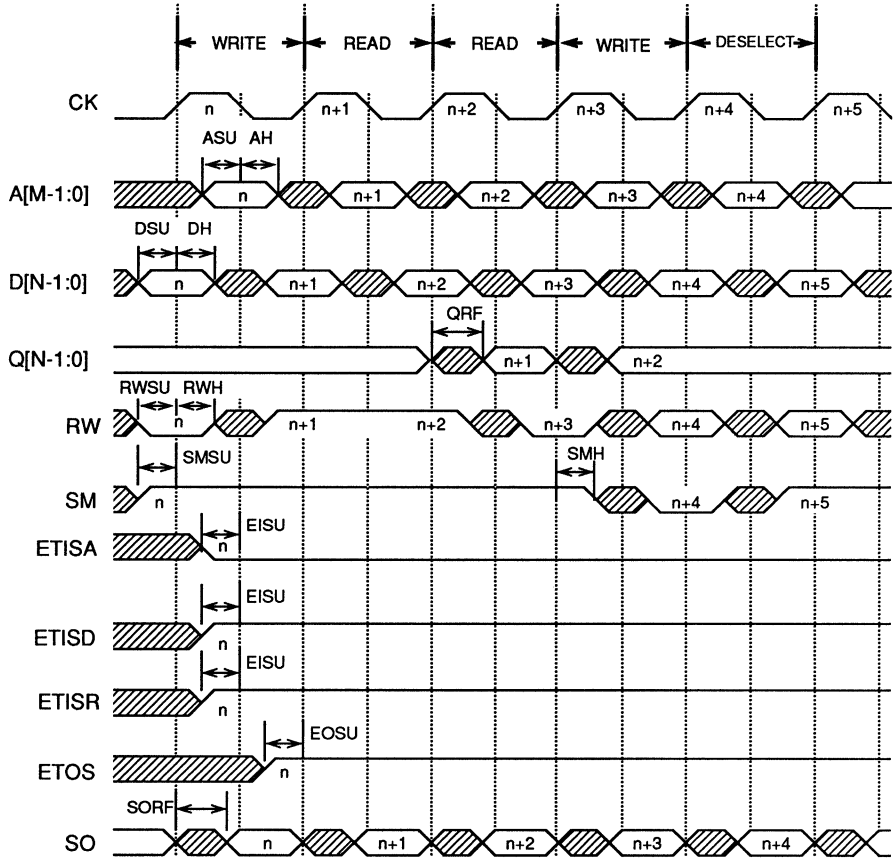
Timing Diagram 5
Functional: + edge-trig D,RW inputs;
- edge-trig A input; + edge-trig Q



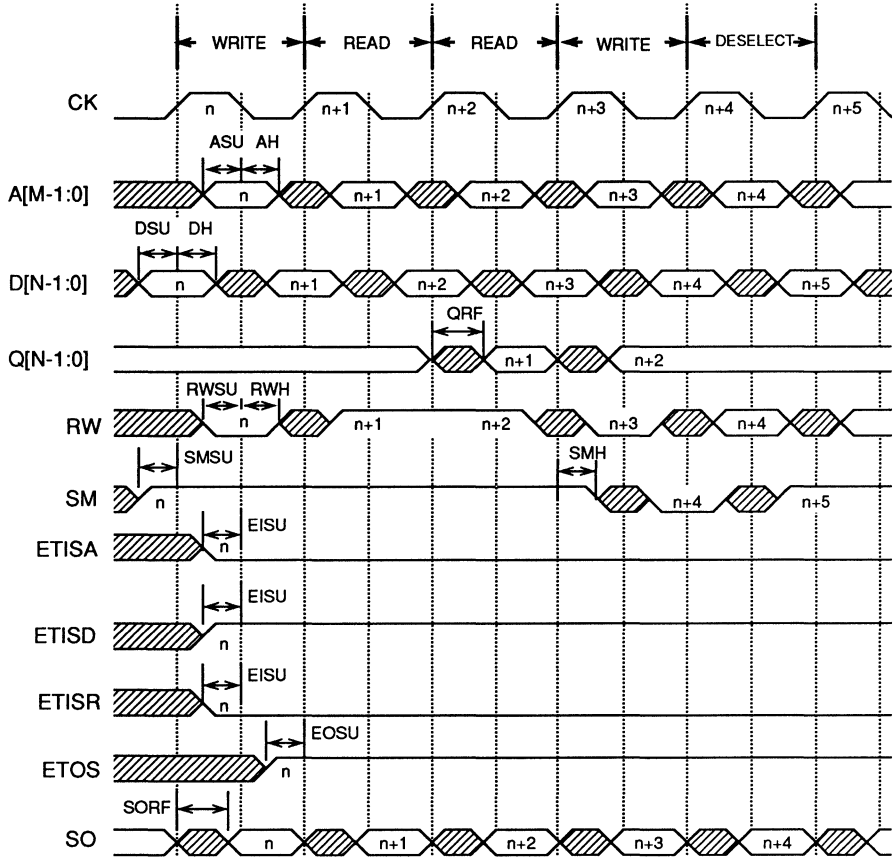
The remaining input signals not found above should have the following logic values:

"0": AI, AH, BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

Output SO is the latched output of the most significant data input bit D[N-1:N -1]. It should be used only during scan testing.

Timing Diagram 6
Functional: + edge-trig D input;
- edge-trig A,RW inputs; + edge-trig Q



The remaining input signals not found above should have the following logic values:

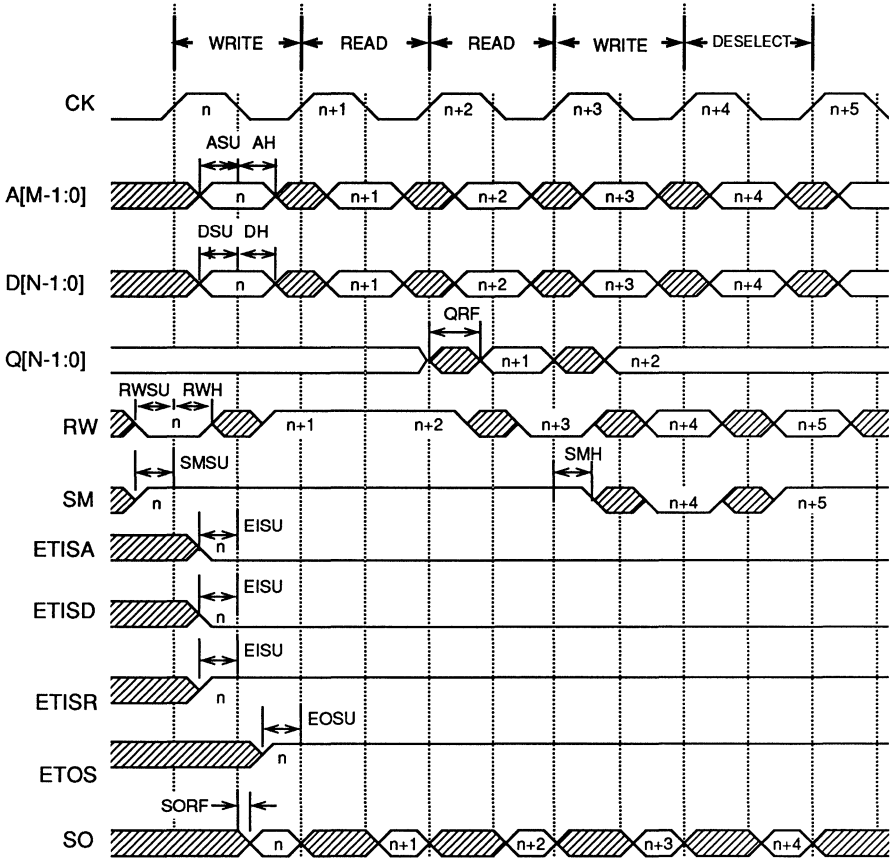
"0": AI, AH, BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

Output SO is the latched output of the most significant data input bit D[N-1:N -1]. It should be used only during scan testing.

8

Timing Diagram 7
Functional: + edge-trig RW input;
- edge-trig A,D inputs; + edge-trig Q



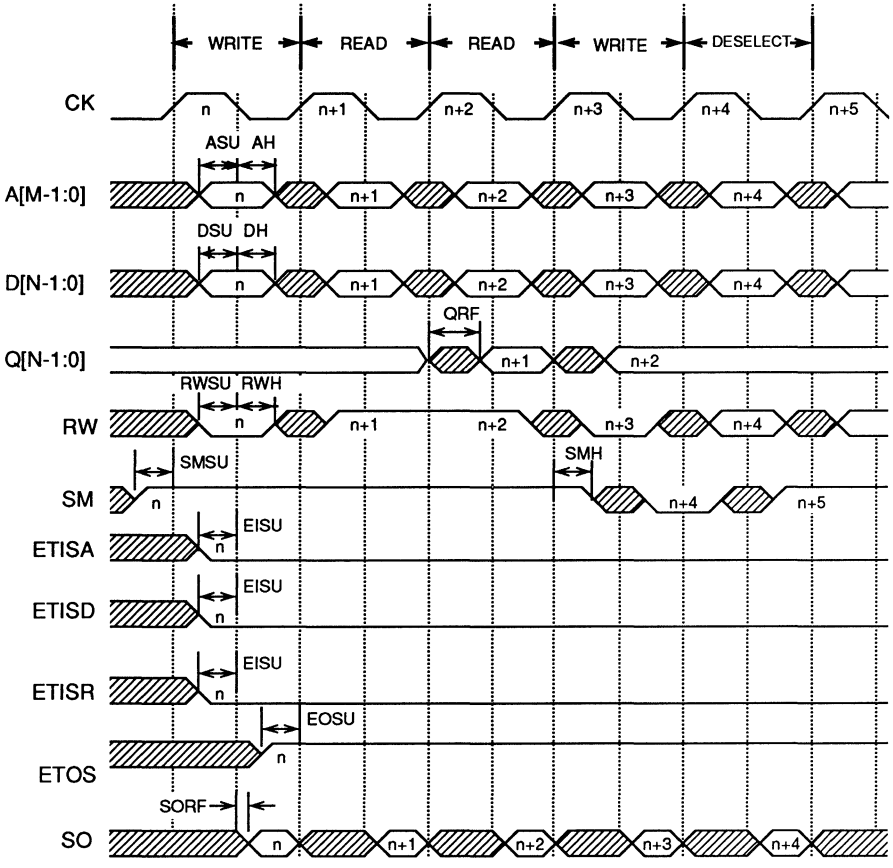
The remaining input signals not found above should have the following logic values:

"0": AI, AH, BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

Output SO is the latched output of the most significant data input bit D[N-1:N -1]. It should be used only during scan testing.

Timing Diagram 8
Functional: - edge-trig A,D,RW inputs;
+ edge-trig Q



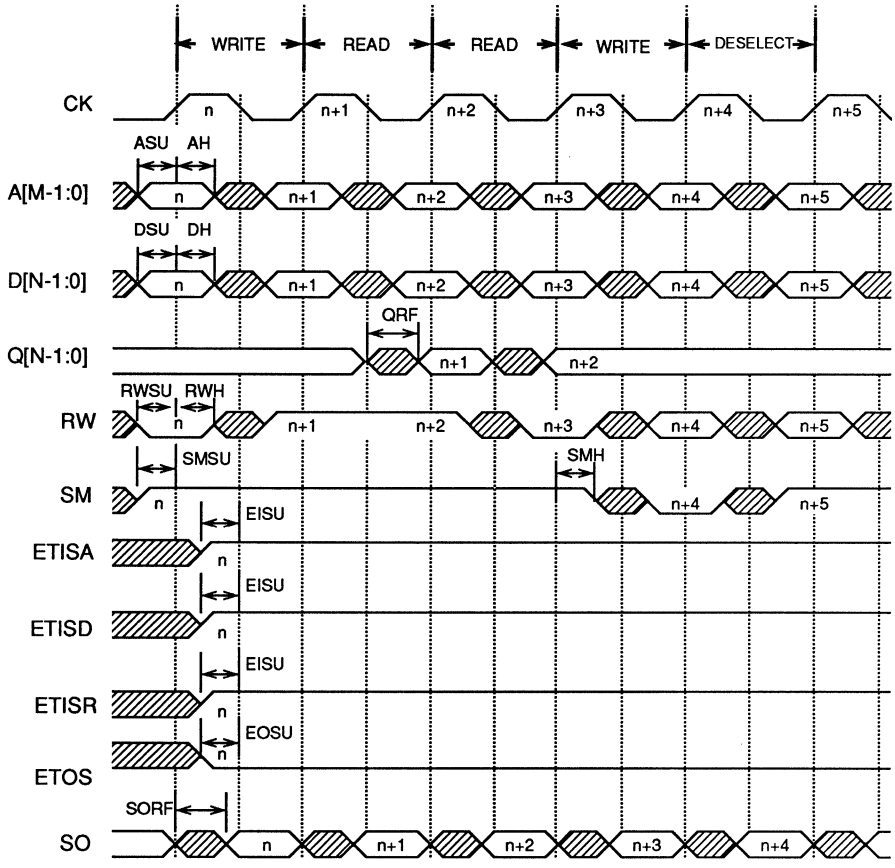
The remaining input signals not found above should have the following logic values:

"0": AI, AH, BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

Output SO is the latched output of the most significant data input bit D[N-1:N -1]. It should be used only during scan testing.

Timing Diagram 9
Functional: + edge-trig A,D,RW inputs;
- edge-trig Q



The remaining input signals not found above should have the following logic values:

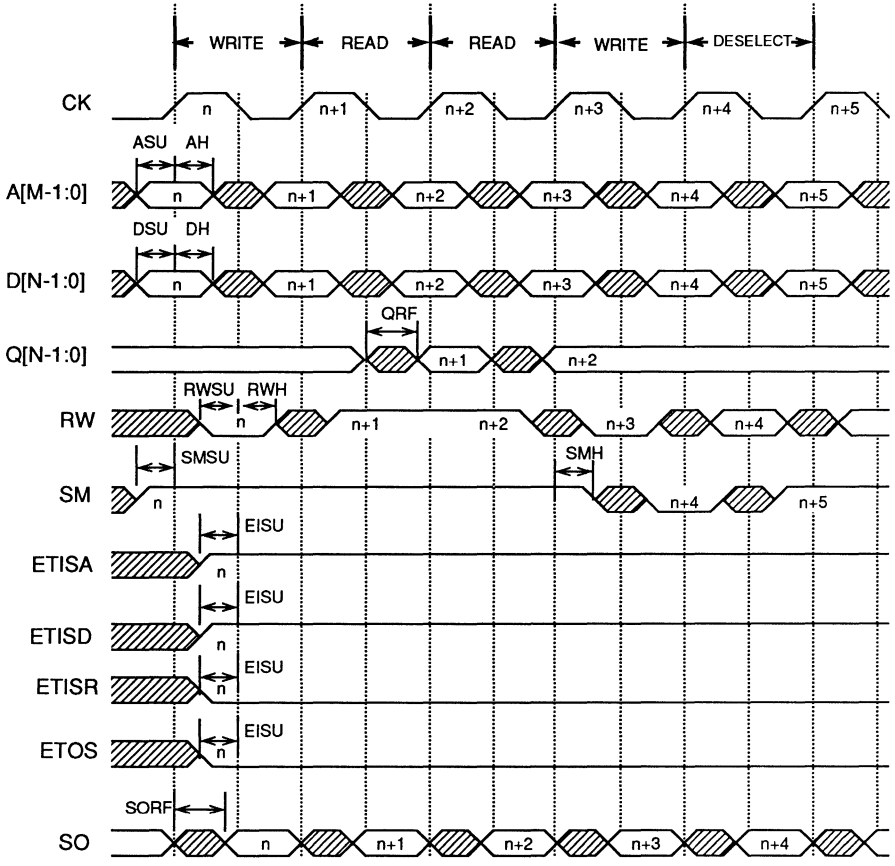
"0": AI, AH, BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

Output SO is the latched output of the most significant data input bit D[N-1:N -1]. It should be used only during scan testing.

Timing Diagram 10

Functional: + edge-trig A,D inputs;
- edge-trig RW input; - edge-trig Q



The remaining input signals not found above should have the following logic values:

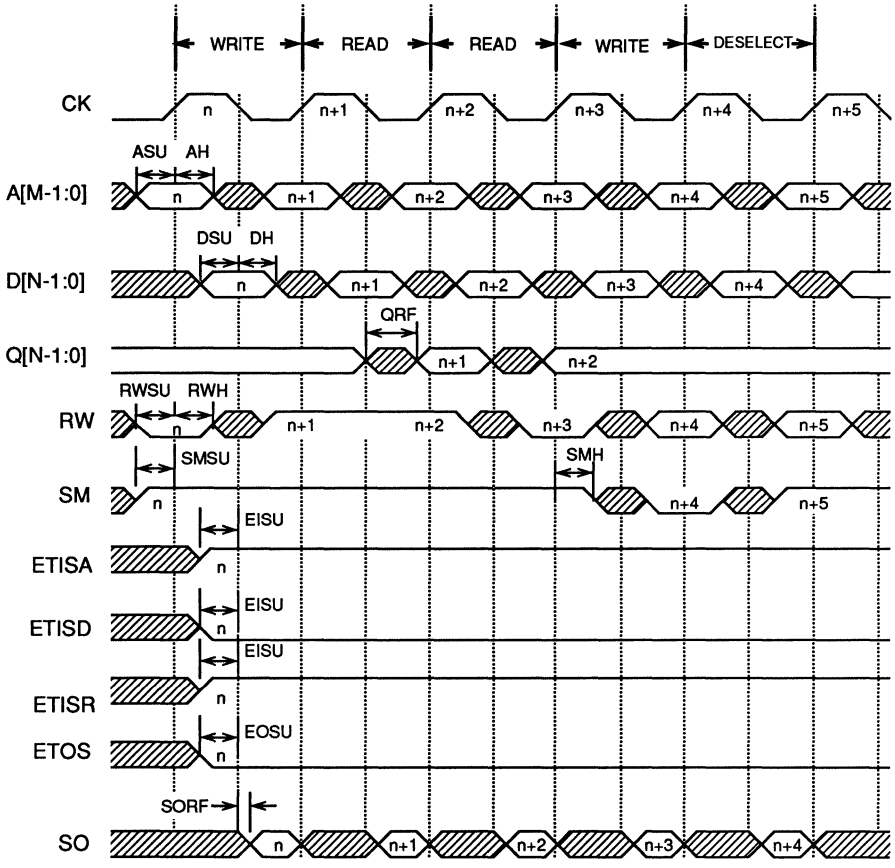
"0": AI, AH, BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

Output SO is the latched output of the most significant data input bit D[N-1:N -1]. It should be used only during scan testing.

8

Timing Diagram 11
Functional: + edge-trig A,RW inputs;
- edge-trig D input; - edge-trig Q



The remaining input signals not found above should have the following logic values:

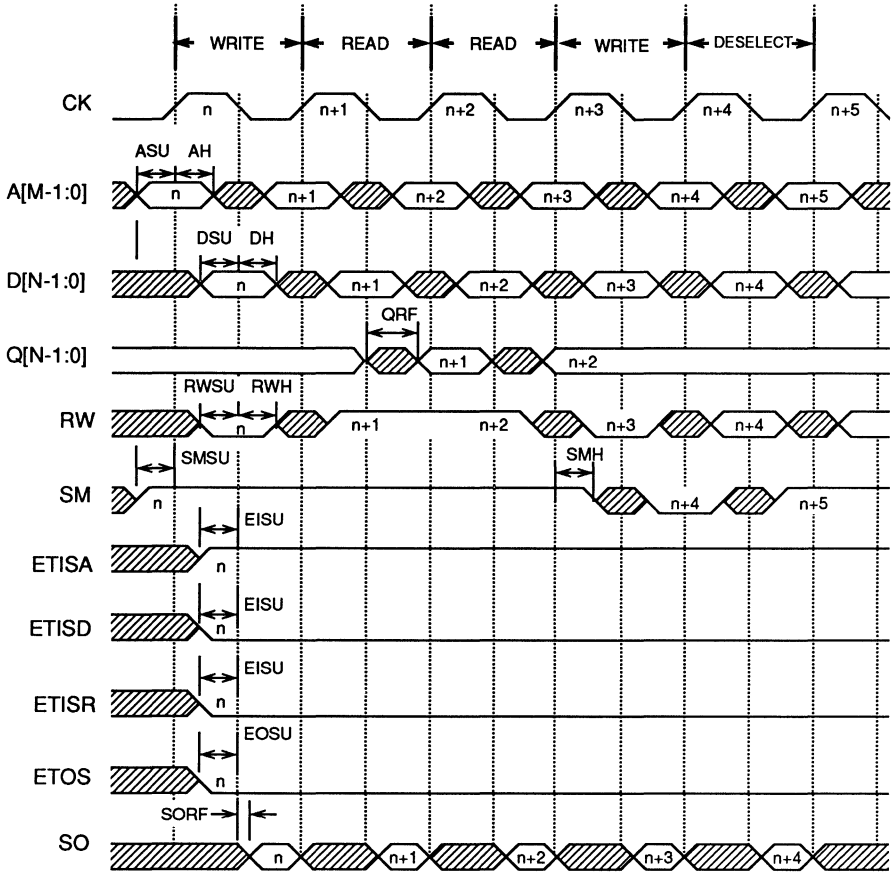
"0": AI, AH, BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

Output SO is the latched output of the most significant data input bit D[N-1:N -1]. It should be used only during scan testing.

8

Timing Diagram 12
Functional: + edge-trig A input;
- edge-trig D,RW inputs; - edge-trig Q



The remaining input signals not found above should have the following logic values:

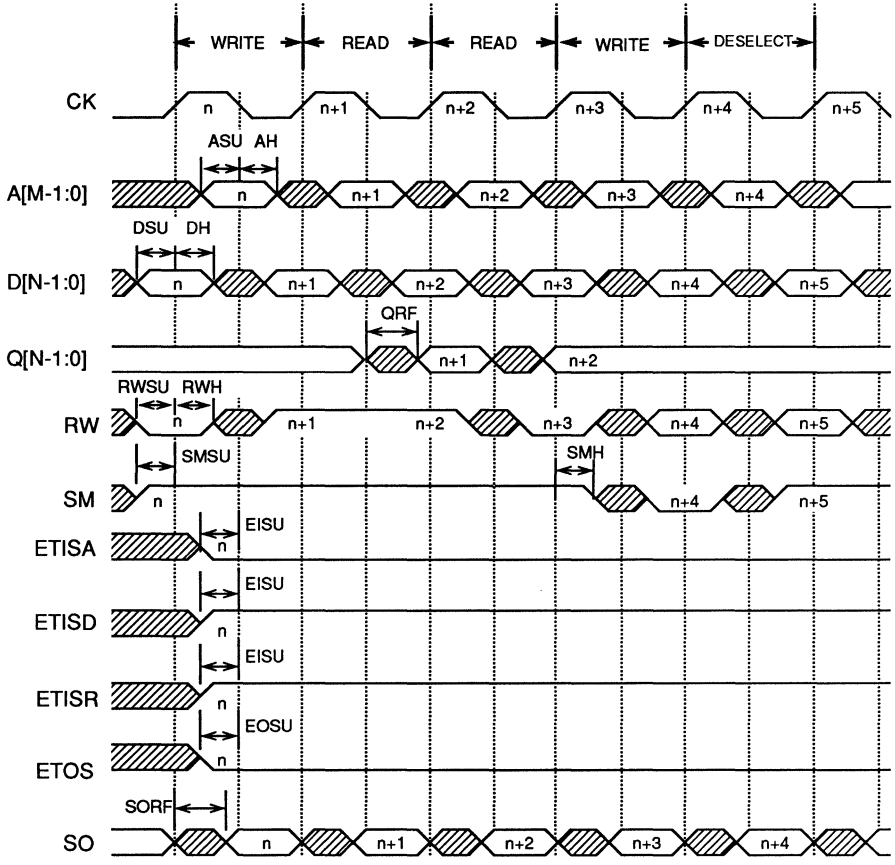
"0": AI, AH, BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

Output SO is the latched output of the most significant data input bit D[N-1:N -1]. It should be used only during scan testing.

8

Timing Diagram 13
Functional: + edge-trig D,RW inputs;
- edge-trig A input; - edge-trig Q



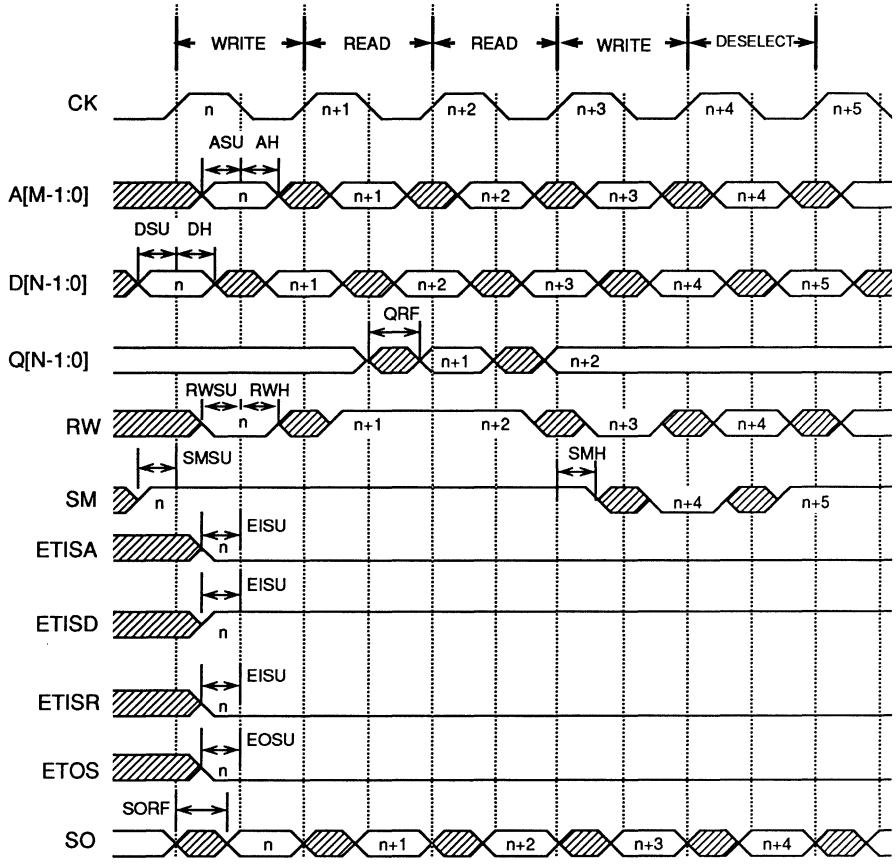
The remaining input signals not found above should have the following logic values:

"0": AI, AH, BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

Output SO is the latched output of the most significant data input bit D[N-1:N -1]. It should be used only during scan testing.

Timing Diagram 14
Functional: + edge-trig D input;
- edge-trig A,RW inputs; - edge-trig Q



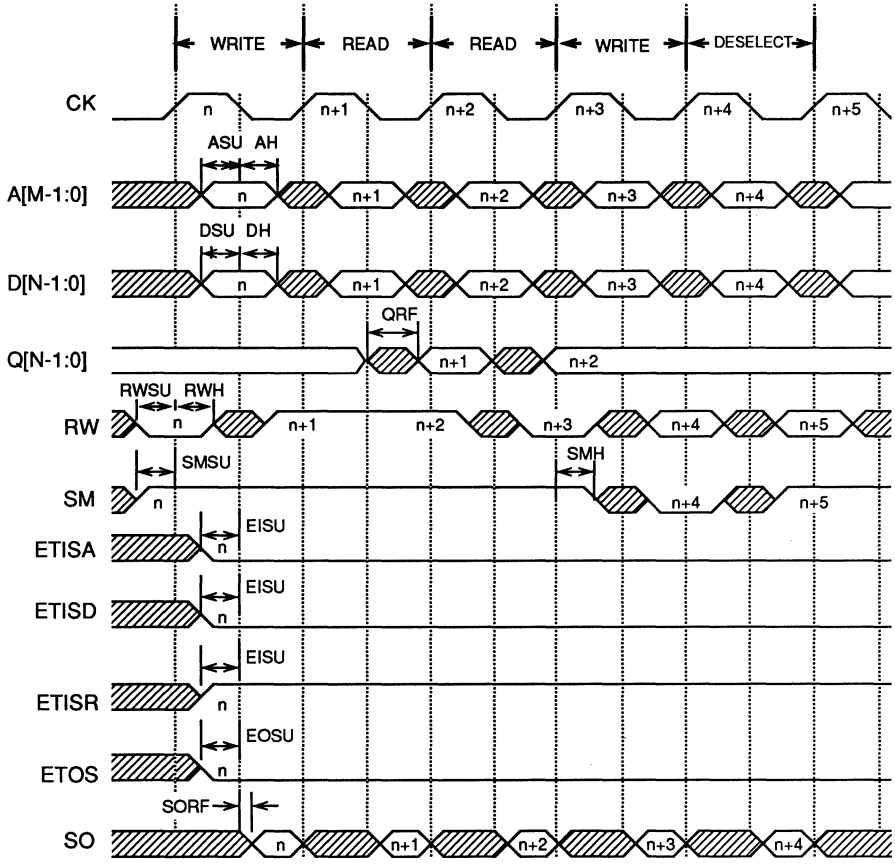
The remaining input signals not found above should have the following logic values:

"0": AI, AH, BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

Output SO is the latched output of the most significant data input bit D[N-1:N -1]. It should be used only during scan testing.

Timing Diagram 15
Functional: + edge-trig RW input;
- edge-trig A,D inputs; - edge-trig Q



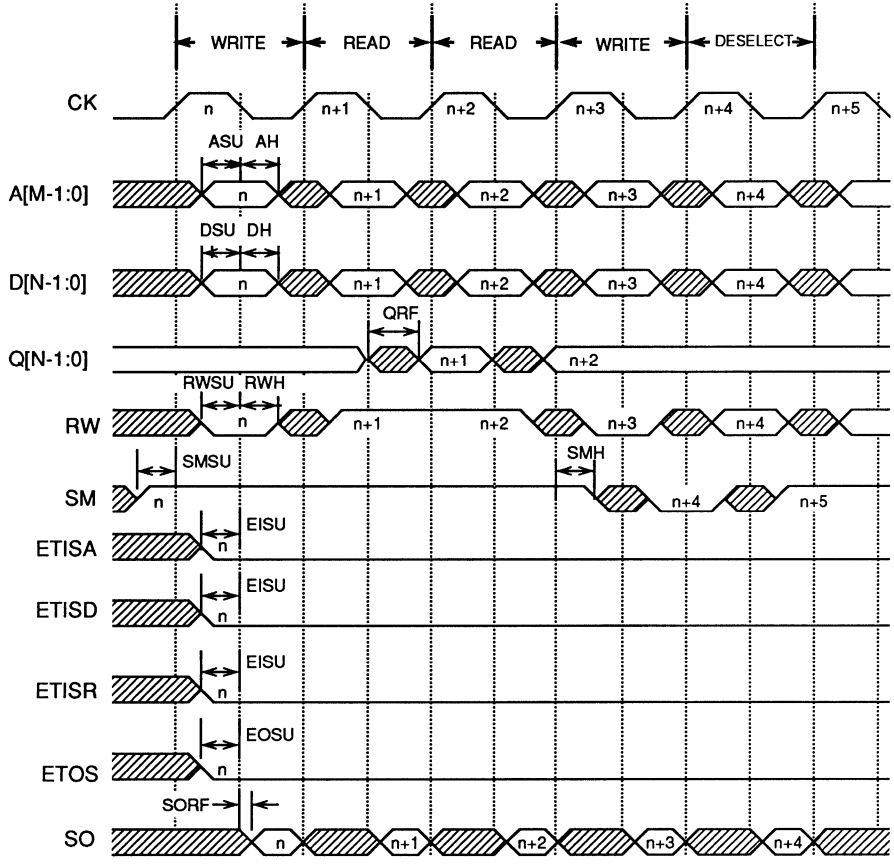
The remaining input signals not found above should have the following logic values:

"0": AI, AH, BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

Output SO is the latched output of the most significant data input bit D[N-1:N -1]. It should be used only during scan testing.

Timing Diagram 16
Functional: - edge-trig A,D,RW inputs;
- edge-trig Q



The remaining input signals not found above should have the following logic values:

"0": AI, AH, BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

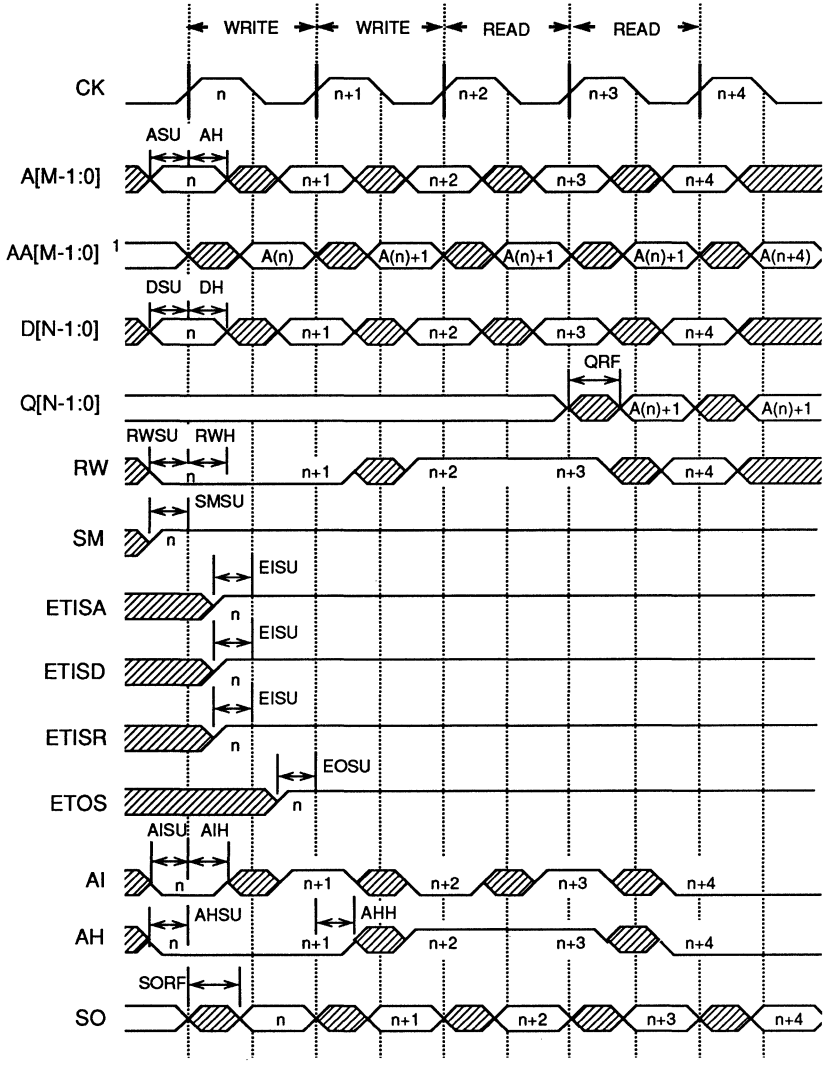
Outputs BF and BC will default to "0" for this mode.

Output SO is the latched output of the most significant data input bit D[N-1:N -1]. It should be used only during scan testing.

8

Timing Diagram 17

Functional: + edge-trig A,D,RW inputs; + edge-trig Q with add increment
Functional: + edge-trig A,D inputs; - edge-trig RW inputs;



[1] AA[M-1:0] is the internally latched address within the SRAM macrocell to indicate what address is being applied to the memory array. "A(n)" is the address latched on the n_{th} clock cycle. "A(n)+1" is that same address incremented by 1.

The remaining input signals not found above should have the following logic values:

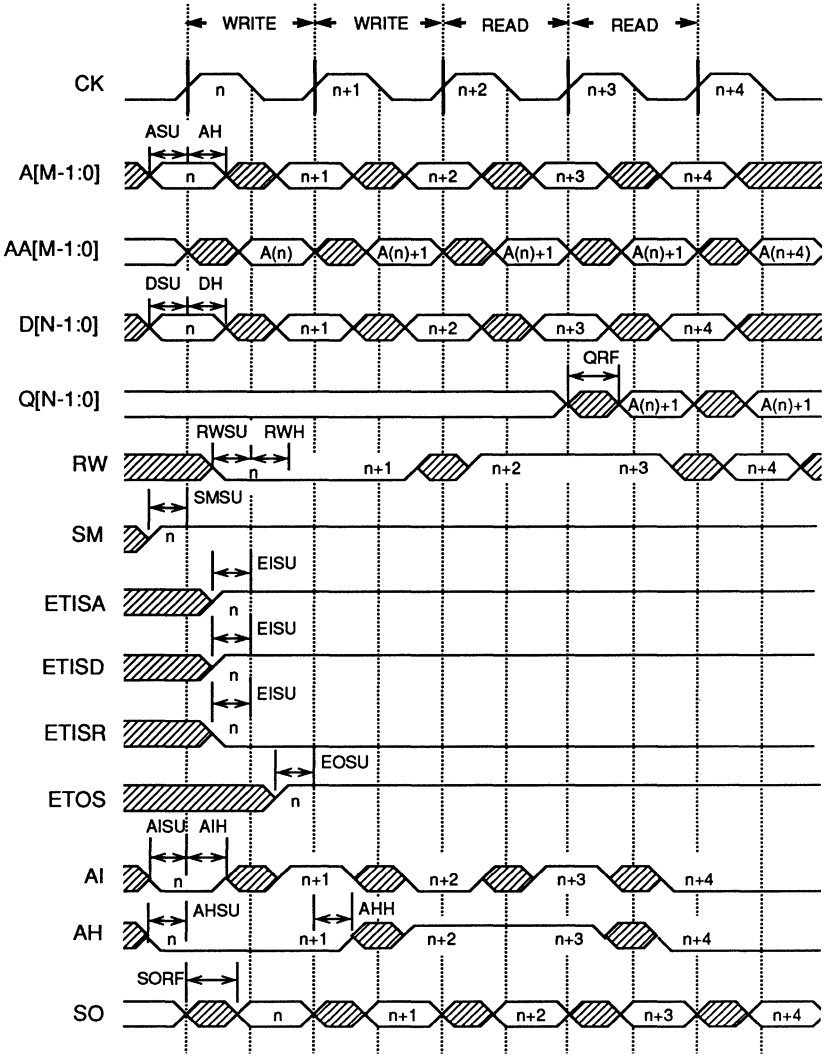
"0": BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

Timing Diagram 18

+ edge-trig Q with add increment

Functional: + edge-trig A,RW inputs; - edge-trig D inputs;



[1] AA[M-1:0] is the internally latched address within the SRAM macrocell to indicate what address is being applied to the memory array. "A(n)" is the address latched on the n^{th} clock cycle. "A(n)+1" is that same address incremented by 1.

The remaining input signals not found above should have the following logic values:

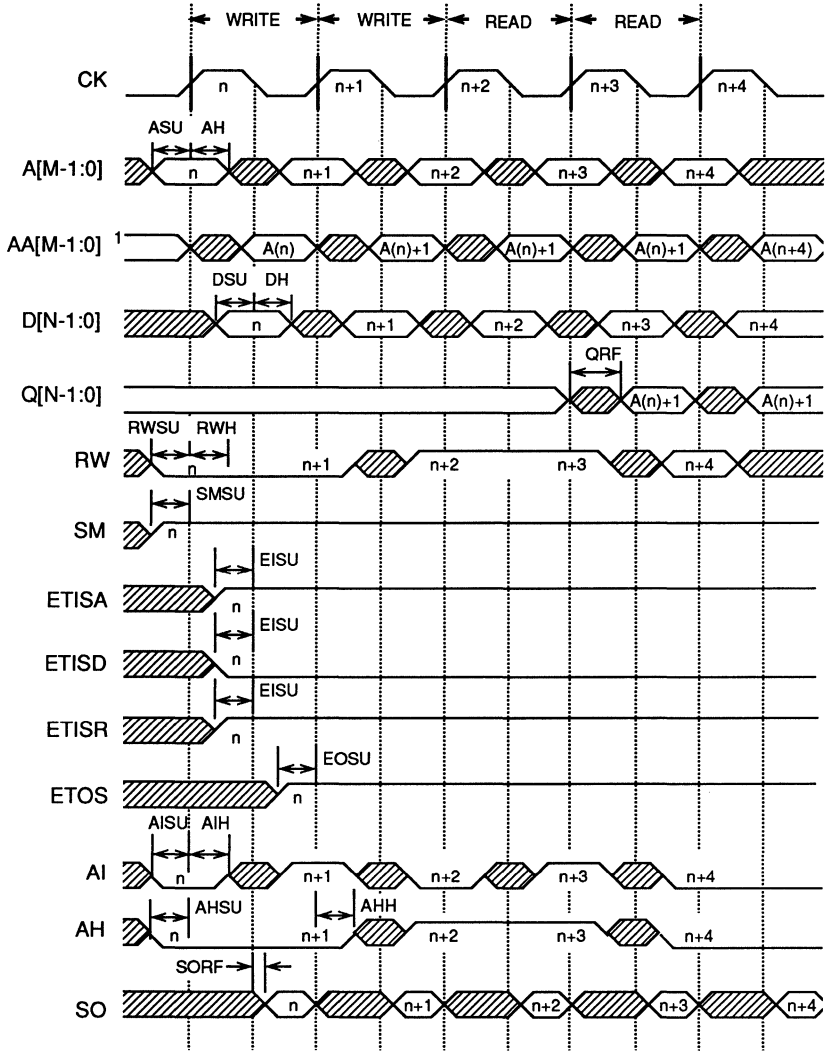
"0": BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

Timing Diagram 19

+ edge-trig Q with add increment

Functional: + edge-trig A inputs; - edge-trig D,RW inputs;



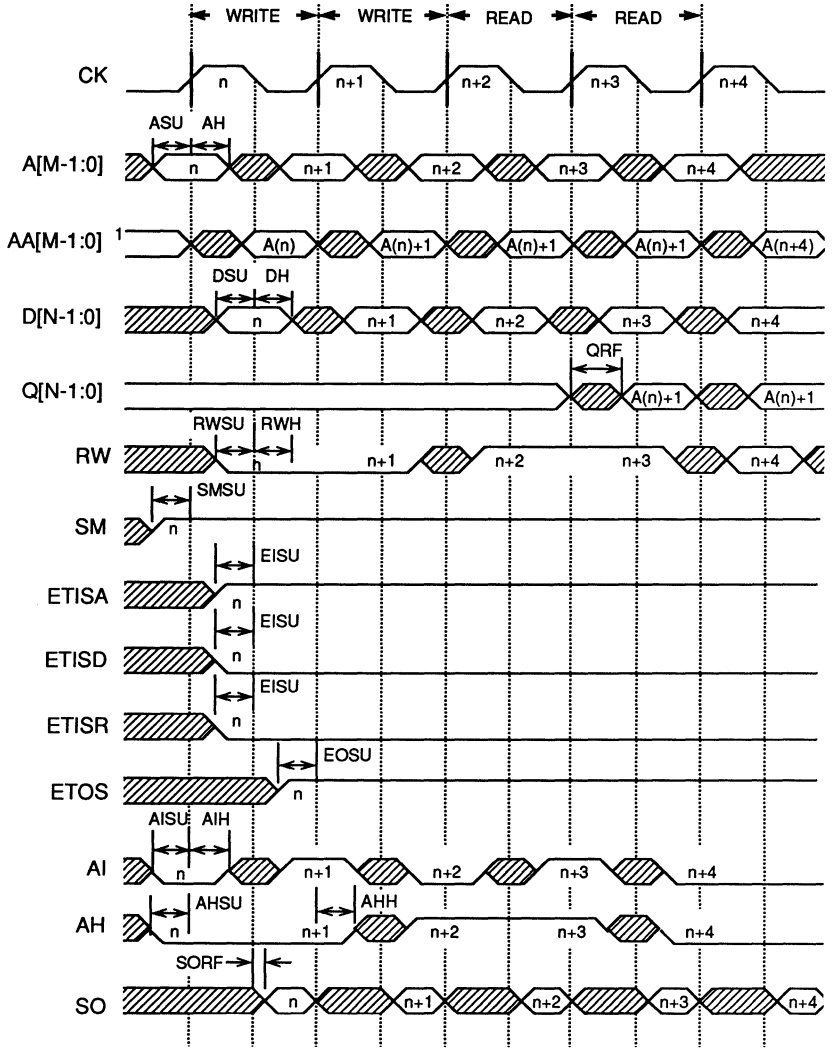
[1] AA[M-1:0] is the internally latched address within the SRAM macrocell to indicate what address is being applied to the memory array. "A(n)" is the address latched on the n^{th} clock cycle. "A(n)+1" is that same address incremented by 1.

The remaining input signals not found above should have the following logic values:

"0": BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

Timing Diagram 20
+ edge-trig Q with add increment



[1] AA[M-1:0] is the internally latched address within the SRAM macrocell to indicate what address is being applied to the memory array. "A(n)" is the address latched on the n^{th} clock cycle. "A(n)+1" is that same address incremented by 1.

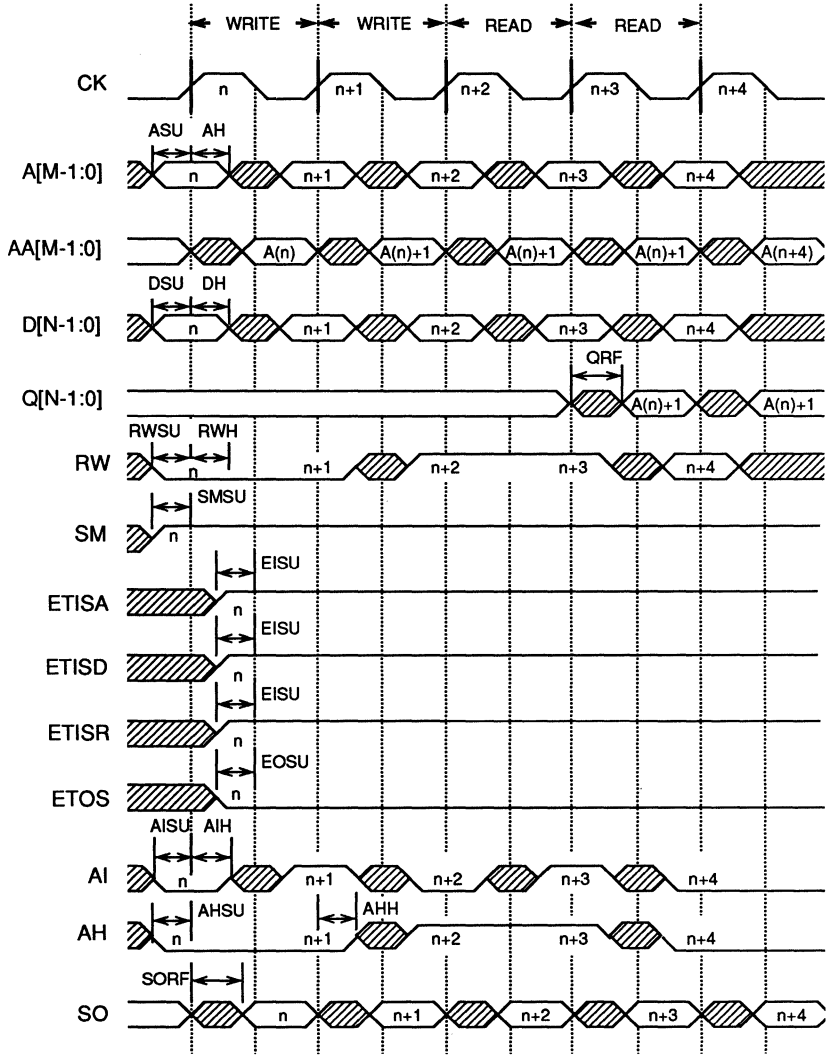
The remaining input signals not found above should have the following logic values:

"0": BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

Timing Diagram 21

Functional: + edge-trig A,D,RW inputs; - edge-trig Q with add increment
Functional: + edge-trig A,D inputs; - edge-trig RW inputs;



[1] AA[M-1:0] is the internally latched address within the SRAM macrocell to indicate what address is being applied to the memory array. "A(n)" is the address latched on the n^{th} clock cycle. "A(n)+1" is that same address incremented by 1.

The remaining input signals not found above should have the following logic values:

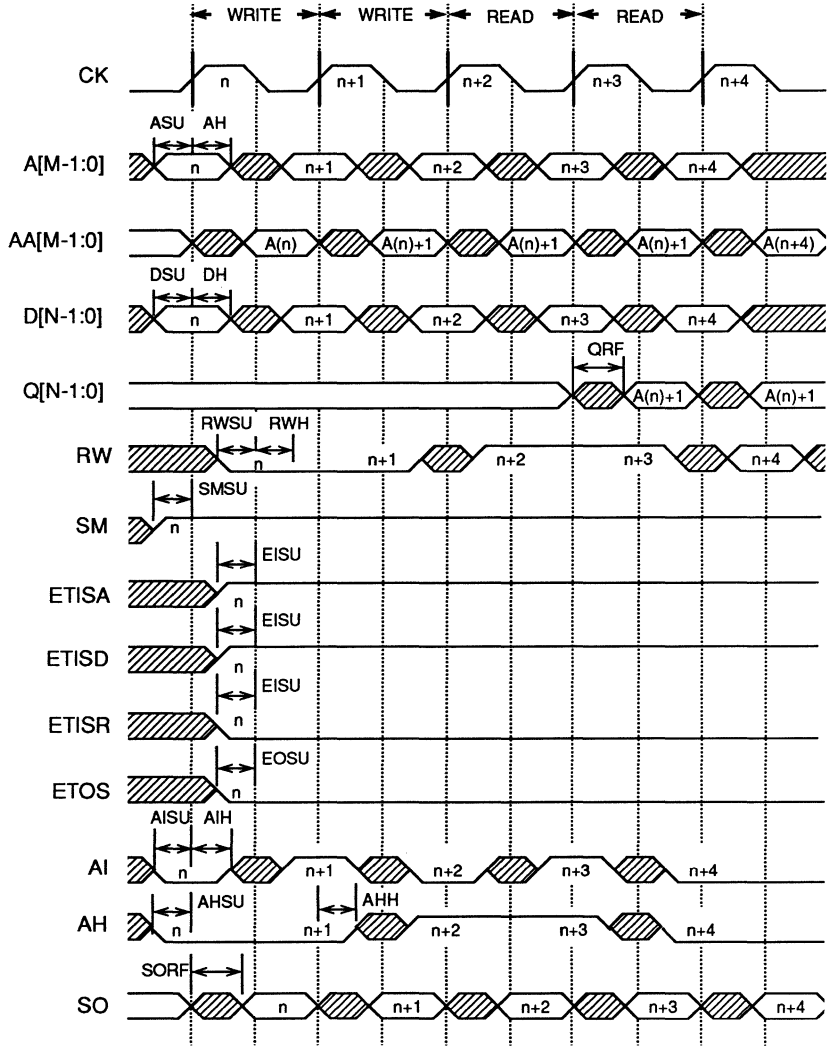
"0": BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

Timing Diagram 22

- edge-trig Q with add increment

Functional: + edge-trig A,RW inputs; - edge-trig D inputs;



[1] AA[M-1:0] is the internally latched address within the SRAM macrocell to indicate what address is being applied to the memory array. "A(n)" is the address latched on the n^{th} clock cycle. "A(n)+1" is that same address incremented by 1.

The remaining input signals not found above should have the following logic values:

"0": BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

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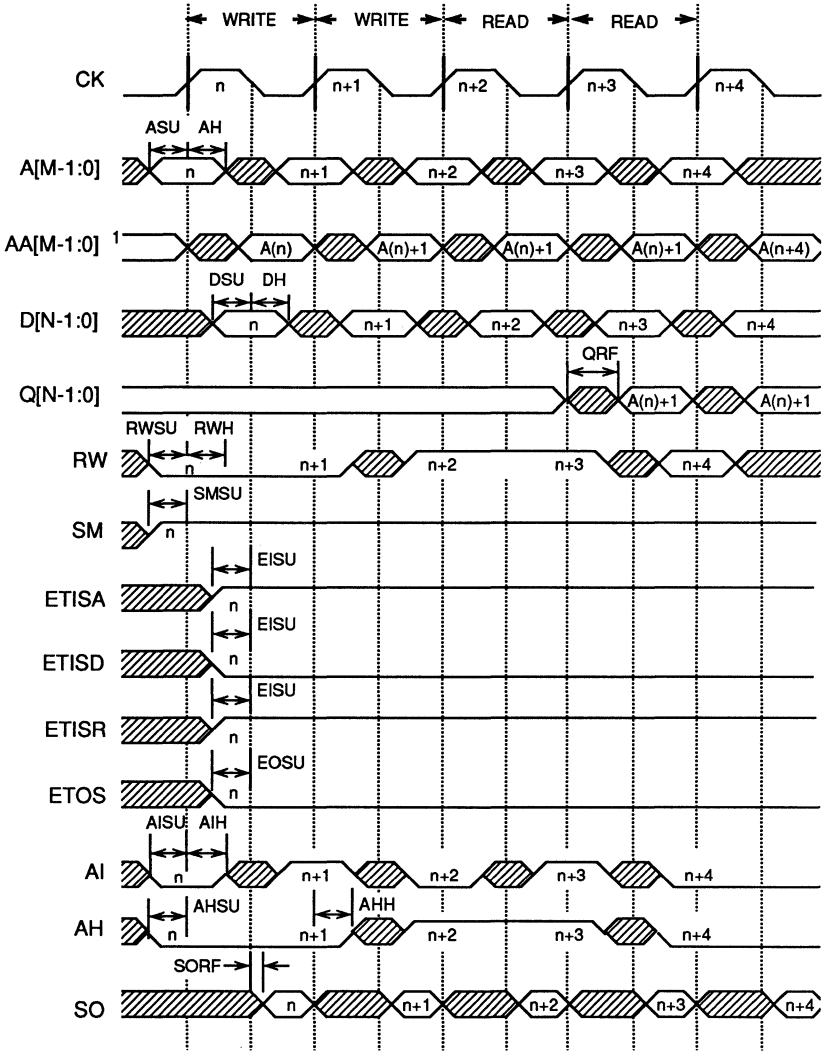
Timing Diagram 23
- edge-trig Q with add increment
Functional: + edge-trig A inputs; - edge-trig D,RW inputs;



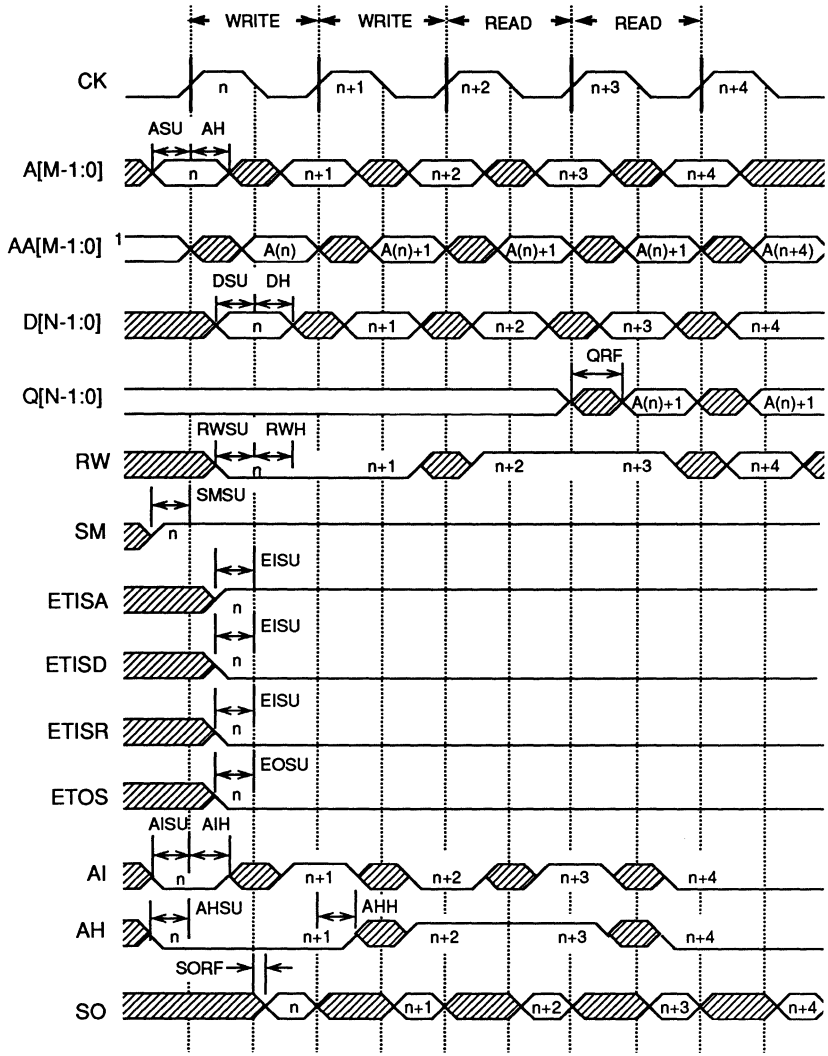
[1] AA[M-1:0] is the internally latched address within the SRAM macrocell to indicate what address is being applied to the memory array. "A(n)" is the address latched on the n^{th} clock cycle. "A(n)+1" is that same address incremented by 1.

The remaining input signals not found above should have the following logic values:

"0": BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

Timing Diagram 24
- edge-trig Q with add increment



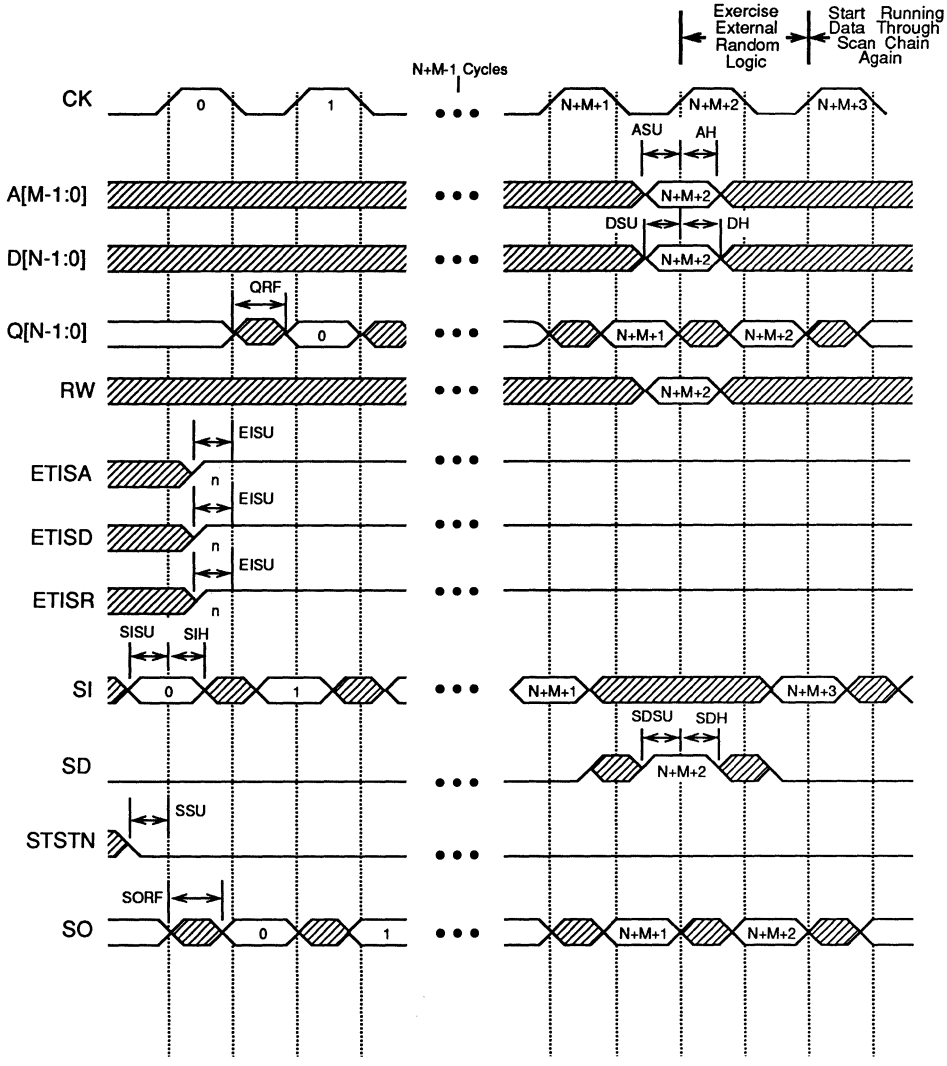
[1] AA[M-1:0] is the internally latched address within the SRAM macrocell to indicate what address is being applied to the memory array. "A(n)" is the address latched on the n^{th} clock cycle. "A(n)+1" is that same address incremented by 1.

The remaining input signals not found above should have the following logic values:

"0": BIST
"1": OE, SD, STSTN
"Don't Care": BFC, SI

Outputs BF and BC will default to "0" for this mode.

Timing Diagram 25
Scan-Test

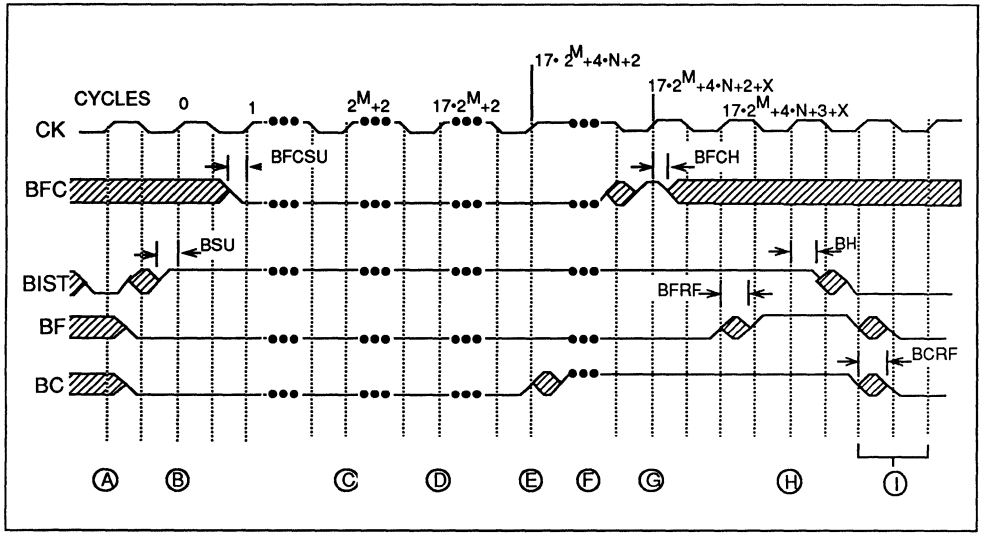


The remaining input signals not found above should have the following logic values:

"0": BIST
"1": SM, OE
"Don't Care": ETOS, BFC, AI, AH

Outputs BF and BC will defaul to "0" for this mode.

Timing Diagram 26
Built-In Self-Test:



Ⓐ A low BIST signal must be latched into the SRAM to properly start initializing it for BIST.

Ⓑ SRAM is placed in the BIST mode.

Ⓒ The SRAM contents have all been initialized by this clock cycle. This fact can be used to initialize all of the SRAMs in a chip circuit. One can then take the SRAM out of BIST mode and begin testing the entire circuit with known SRAM contents.

Ⓓ Internal memory test is completed. BF may go high at anytime up to this point. If BF goes high, it will remain high. BIST checking now begins.

Ⓔ BIST overhead checking is now complete. BC will toggle high at this time. BF will also go high if any faults are detected here. As before, if BF goes high, it will remain high.

Ⓕ BF should be checked at this time. If it is high, the SRAM is bad. One can wait any amount of time to make this check (call it X cycles).

Ⓖ BFC is toggled high to check for a stuck-at-0 fault on the BF output.

Ⓗ One cycle after a high BFC input has been latched into the SRAM, the BF output should toggle high.

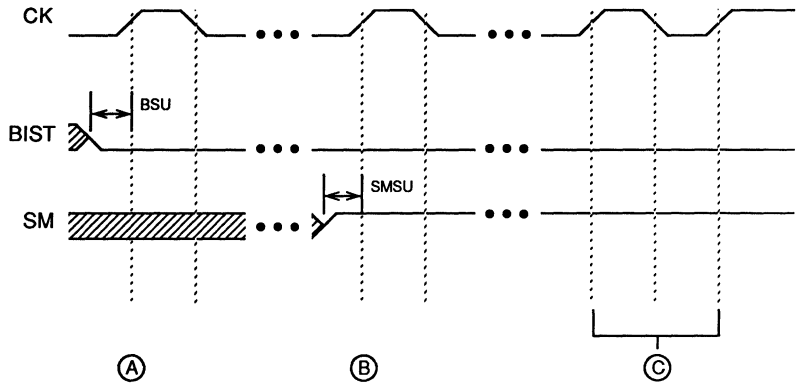
Ⓘ First valid access of the SRAM after coming out of BIST should occur at this time

The remaining input signals not found above may have any logic value "0 or 1".

Outputs Q[N-1:0] will change with each read that occurs with the BIST vectors providing that the input OE is held at a logic value of "1". These outputs will also change on the positive edge of the clock CK.

Output SO is the latched output of the most significant data input bit D[N-1:N-1]. It should be used only during scan testing.

Timing Diagram 27
Initialization of SRAM on power-up:



A. A low BIST signal must be latched in to the SRAM. One clock cycle is used for this.

B. A high SM signal must be latched in next. This can occur any number of clock cycles after the first step (A). At least one more clock cycle is used for this.

C. First valid access to the SRAM should occur for the first clock cycle after the second step (B) that latches in a high SM signal.

USER NOTES

Layout - The layout for the SRAM consists of two blocks : the address block and the main block. The address block contains the address, read/write, and SM input latches while the main block contains the remaining SRAM features. By definition, the BIST circuitry must be distributed throughout both blocks. Capacitance on the interconnect between these blocks may have an affect on performance.

Built-In Self-Test - Built-In Self-Test (BIST) is self contained in the SRAM layout. It provides >99% fault coverage of the faults within the SRAM. The BIST circuitry overrides the AI, AH, SM, and scan-test modes. The built-in self-test circuitry tests:

- stuck-at-0/stuck-at-1 for each memory cell
- 0(->1/1(->0 transitions for each memory cell
- Read destruction of memory contents 0/1
- Row decoder faults
- Column decoder faults
- Read/write clocking faults
- Coupling and/or bridging
- Adjacent memory cells
- Adjacent I/O data paths
- Internal clock generator
- I/O latches for data, address, and read/write.
- Built-In Self-Test circuitry

Scan Chain - During scan-testing the faults in the external random logic around the SRAM are tested. STSTN is low. When ETISA, ETISD, and ETISR are all high, only the read/write, address, and data input latches are connected together to form a scan chain; the output latches are by-passed to allow quick access to the external random logic connected at the outputs. In terms of the primary inputs for the input latches, the following specifies the ordering of the scan chain:

RW,A[0:**M**-1],D[0:**N**-1]

When ETISA, ETISD, and ETISR are all low while STSTN is low, none of the input latches are connected together to form a scan chain. The output latches are still by-passed to allow quick access to the external random logic connected at the outputs.

Interfacing - The SRAM can be interfaced in a number of different modes. It may be used synchronously with either positive or negative edge-triggered flip-flops. The user must insure that the inputs are properly set up for the mode of operation desired.

Initialization - The BIST mode can be used to initialize the RAM contents. A description of the BIST algorithm is available through MACLOG.

Characterization - The characterization has been done using 2 pFs and 1,000 ohms for the routing of signals between the address and main blocks. These should be pessimistic numbers. Most layouts should have values below these.

Address Increment - Address increment (AI) mode automatically increments the address regardless of the address inputs. The address latch must be in the positive edge-triggered mode. If the macrocell is deselected with SM, the address will be incremented, but not applied to the memory contents. Several applications can be accommodated:

- Sequentially accessing the SRAM. No external counter is required.
- Initializing the SRAM.

Address hold - Address hold (AH) mode freezes the address regardless of the address inputs. One application is in doing a "read - modify write". The contents of an address location can be overwritten immediately after a read. AH overrides AI.

Select macrocell - Select macrocell (SM) mode activates the internal clocking of the SRAM. Several applications can be accomodated:

- Reduction of power. When the internal clocking is not activated, the power is greatly reduced while the memory contents and the data outputs are unaffected. Only the I/O latches are allowed to clock data in or out. When either the AI or the AH mode is activated, the address latches will be updated, but not applied.
- Sub-dividing a large SRAM into several smaller SRAMs for speed enhancement. Here, only one of the smaller SRAMs needs to be activated at any one time. Common data and address input busses can be shared by using the SM inputs to multiplex.
- Deselecting an SRAM that's not in use. Leaving an SRAM in the write mode as a default may easily modify the SRAM contents. Leaving an SRAM in the read mode as a default may easily modify the SRAM outputs. Leaving an SRAM in the deselect mode with SM off ensures that the SRAM contents and outputs remain unmodified.

Scan-test - Scan-test circuitry overrides the AI, AH, and SM modes. The scan-test circuitry tests:

- Random logic external to the SRAM's data inputs, address inputs, read/write input, and data outputs
- Stuck-at-0/stuck-at-1 faults at the SRAM's data inputs, address inputs, read/write input

FUNCTIONAL DESCRIPTION AND FEATURES:

SRGEN is a parameterized, Shift Register function supported by automatic layout generation software. The layout of SRGEN is implemented as a custom, pitch-matched array of cells that is very area-efficient.

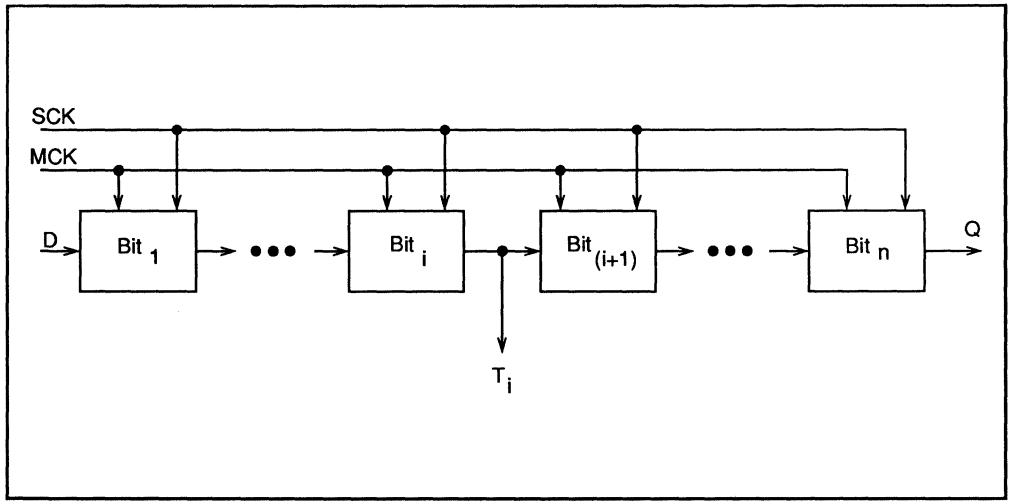
SRGEN has been designed specifically for use on standard-cell chips and has the following features:

- Requires non-overlapping master and slave clocks
- Can be implemented with multiple tap bits
- Tap Bits can be automatically placed along the shift register
- Outputs, including tap bits, are properly buffered to interface with standard-cell circuitry
- The aspect ratio of the shift register can be easily modified to suit the needs of the chip layout

The Shift Register can be customized with the following parameters:

Parameter	Description	Limit		
		Increment	Min	Max
N	Bits in depth	1	1	65,000
$T_1,...,T_n$	Tapped locations	1	0	65,000
M	Rows to fold the array	1	1	N/205

BLOCK DIAGRAM



NOTE: This is a preliminary Data Sheet. Contact your AT&T representative for current information.

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: MCK, SCK, D

OUTPUTS: T_i,...,T_n, Q

Functional Descriptions

Inputs

MCK	Master clock
SCK	Slave clock
D	Data input

Outputs

T_i,...,T_n	Tapped data out (subscript corresponds to the register position tapped)
Q	Data out (tap of last register)

CHARACTERISTICS

The parameters **N**, **T** and **M** can be used to estimate the characteristics for a shift register that is **N** bits deep, has **T** tapped locations and is folded into **M** rows. .

Parameter	Value	Unit
Number of Transistors	Not Currently Available	
Height		µm
Width		
Worst Case Power		µW
Input Capacitance:		
D		pF
MCK		
SCK		
Output Capacitance:		
Q		pF
T_i,...,T_n		

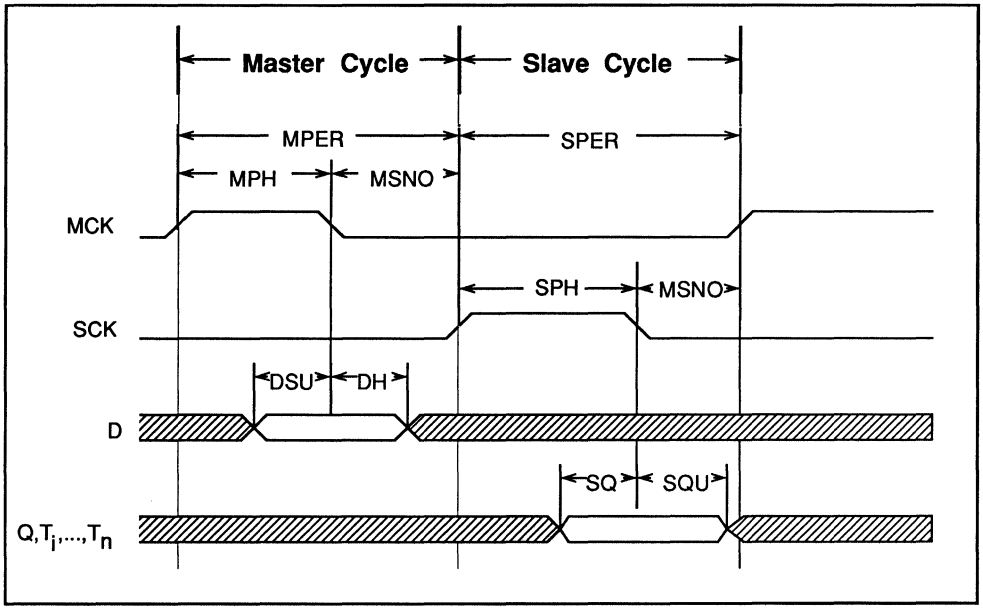
NOTE: This is a preliminary Data Sheet. Contact your AT&T representative for current information.

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing				
Symbol	**From INPUT**	**To OUTPUT**	**Intrinsic (ns)**	**Extrinsic (ns/pF)**
SQ	SCK↑	Q↑	Not Currently Available	
	SCK↑	Q↓		
	SCK↑	T_i,...,T_n↑		
	SCK↑	T_i,...,T_n↓		

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Symbol	**Description**	**Value**	**Unit**
MPH	Minimum master clock pulse high	Not Currently Available	ns
MPER	Minimum master clock cycle		ns
	Maximum master clock cycle		µs
SPH	Minimum slave clock pulse high		ns
SPER	Minimum slave clock cycle		ns
	Maximum slave clock cycle		µs
MSNO	Minimum time between master and slave pulses		ns
	Maximum time between master and slave pulses		µs
DSU	Minimum data in setup time		ns
DH	Minimum data in hold time		
SQU	Maximum hold time for data out		µs

NOTE: This is a preliminary Data Sheet. Contact your AT&T representative for current information.

TIMING DIAGRAM



USER NOTES

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In order to reduce leakage current from the dynamic nodes, every effort should be made to reduce noise on the clocks and insure that they are indeed non-overlapping.

The propagation delay shown in the tables is worst case for the cell furthest from the slave clock input terminal. There is some skew, due to routing parasitics, in the clock delay to different tapped locations.

The dynamic shift register is inherently subject to alpha induced soft errors. This macrocell should not be used to store critical data.

NOTE: This is a preliminary Data Sheet. Contact your AT&T representative for current information.

Linear Cells

Section 9

Contents - Section 9

Note: Schmitt Trigger buffers are located in Section 5 (I/O Buffers).

Introduction

This section describes the Linear CMOS cells that are available for use with the 0.9 µm Standard-Cell Library. The reason for the introduction of linear cells into an otherwise digital world is to add versatility to the digital chips by providing functions that cannot be done with strictly digital circuits.

The linear cells are designed to be as similar to the digital standard cells and buffers as possible. The digital CMOS process, with only a single level of polysilicon, is standard. The software for circuit simulation, netlist capture, and layout is identical to that used on digital cells. The linear cells are also testable in a digital environment. The linear cells form a small part of the entire chip, typically less than 10% of the area.

Since most linear CMOS cells in this library are I/O intensive, they are placed in the buffer area on the periphery of the chip. Many of them will fit into the standard I/O buffer ring and connect to the buffer power supplies. Some linear cells, however, are too noise-sensitive to use these digital power supplies, and they require their own power and ground connections.

Many VLSI CMOS chips are designed to be retrofits of existing SSI boards. The linear chips on these boards are mostly bipolar. Bipolar linear circuits usually have some performance characteristics not obtainable with linear CMOS. It may not be possible for a linear CMOS cell to meet the specs of a (bipolar) part that is currently in use. Therefore, consult with your AT&T representative about what specs are realistic.

CAD Support Files

The CAD support files for linear CMOS are modeled as closely as possible after those used for digital circuits.

ADVICE

The standard process files used for ADVICE simulations of digital circuits (***apronc.dat***, ***aprolc.dat***, and ***aprohc.dat***) are also used with the linear cells.

All of the linear cells have been characterized using ADVICE, and the resulting characteristics are presented in the following pages. Unless otherwise specified, the worst-case simulations were all done assuming V_{DD} = 5 V ± 10%, a temperature range of 0 °C to 100 °C, standard (digital) fast and slow process files, and a ± 22% variation from nominal resistor values. Any circuit parameters that are not specified cannot be guaranteed.

MOTIS3

Simulations with MOTIS3 models are ***not*** intended to replace ADVICE simulations. The true analog nature of these circuits cannot be simulated in the current MOTIS3 environment. The real reason to use the MOTIS3 models is that they allow the designer to use a single netlist throughout the design process. However, ADVICE is still required to simulate the detailed analog behavior and timing, by using the circuit descriptions found in the file ***advlc.dat*** from the linear library.

Loss of Signal Detector LOT[15U,250N]

Functional Description

The function of the LOT circuits is to detect the loss of a signal which, under proper operating conditions, regularly changes its state. This would most often be used with a clock, but can be used with any signal.

The cells detect either a stuck-high or stuck-low condition. It will work with any signal whose duty cycle is between 30% and 70%.

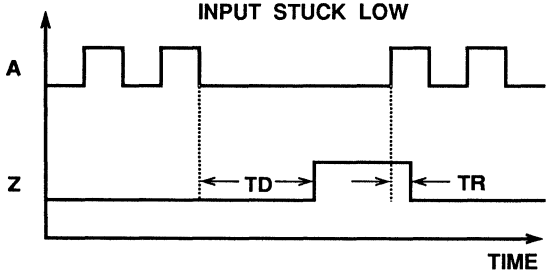
The cell height is the same as digital D- and P-style buffers. This cell does not contain a bonding pad.

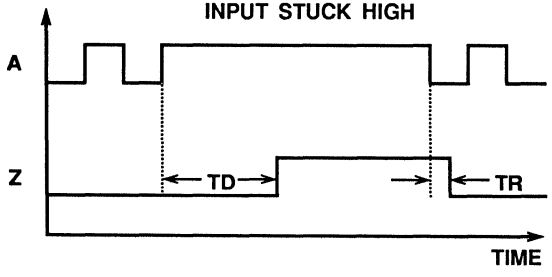
Netlist Order

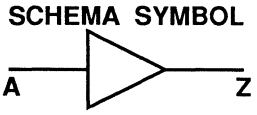
Inputs: A
Outputs: Z

Circuit Information

Parameter	LOT15U	LOT250N
Max Power	1 mW	5 mW
Detect Time TD		
Minimum	8 µs	150 ns
Nominal	15 µs	250 ns
Maximum	30 µs	550 ns
Recovery Time TR		
Maximum	20 ns	8 ns
Frequency of Operation		
Minimum	0.2 MHz	10 MHz
Maximum	100 MHz	200 MHz
Cell Size	252.25 µ × 283.5 µ	252.25 µ × 283.5 µ







Power-Up Reset

PURA[*3M,300U,30U*]

3 ms, 300 µs, 30 µs Nominal Pulse Width with Test Mode

Functional Description

These circuits provide a clear pulse immediately upon chip power-up. After a time TP, the clear pulse goes low and stays low as long as V_{DD} stays high and the test input TST is low.

The cell heights are the same as digital D- and P-style buffers. These cells do not contain bonding pads.

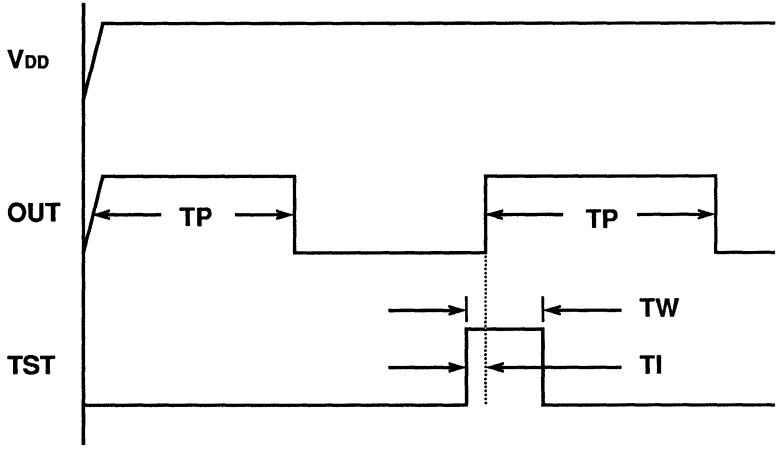
Netlist Order

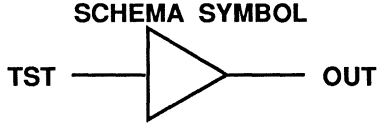
Inputs: TST
Outputs: OUT

Circuit Information

Parameter	PURA3M			PURA300U			PURA30U		
	TW	TP	TI	TW	TP	TI	TW	TP	TI
Maximum	N/A	7 ms*	200 ns	N/A	700 µs†	70 ns	N/A	70 µs‡	70 ns
Nominal	N/A	3 ms	90 ns	N/A	300 µs	30 ns	N/A	30 µs	30 ns
Minimum	300 ns	1.5 ms	45 ns	100 ns	150 µs	15 ns	100 ns	15 µs	15 ns
Max Power	0.5 mW			0.5 mW			0.5 mW		
Cell Size	483.35 µ × 283.5 µ			364.3 µ × 283.5 µ			364.3 µ × 283.5 µ		

* As long as $V_{DD} \geq 4$ V within 1 ms of start-up
† As long as $V_{DD} \geq 4$ V within 100 µs of start-up
‡ As long as $V_{DD} \geq 4$ V within 20 µs of start-up





Introduction

The crystal oscillators available in the AT&T 0.9 µm CMOS Standard-Cell library are of the Pierce type. An inverter is used as the amplifying element, the crystal is connected between input and output terminals, and capacitors are connected from input to ground and from output to ground, respectively. The generic circuit topology is shown in Figure 1. This circuit configuration operates the crystal in a parallel resonant condition, which means that the operating frequency will be several hundred parts per million (ppm) above the crystal's series resonant frequency and will be dependent on the capacitances present in the circuit.

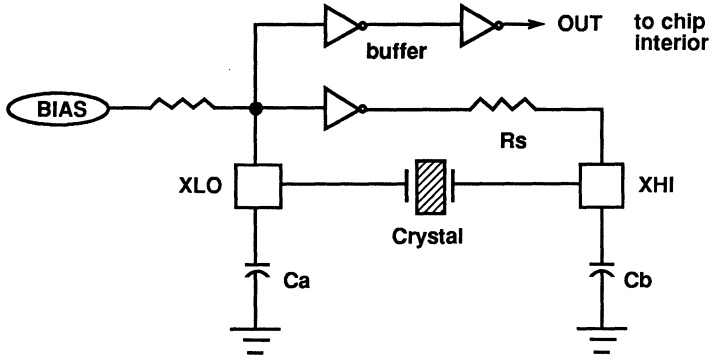


Figure 1. Pierce Crystal Oscillator Based on CMOS Inverter

As shown in Figure 1, the crystal terminals are XLO and XHI. XLO is the input side of the amplifier and XHI is the output side. Because these terminals are pads for external connections, the usual protection circuitry is in place (adding approximately 2 picofarads of shunt capacitance and 450 Ω of series resistance to each pad). Capacitors ***Ca*** and ***Cb*** may be on- or off-chip. Resistor ***Rs*** is on-chip and has a nominal value of 600 Ω. The signal from the oscillator is taken from the XLO terminal and buffered by two inverter stages before passing into the chip interior.

Crystal Considerations

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The operation of the oscillator is influenced to a great extent by the characteristics of the particular crystal being used. For a specific application, the crystal and the oscillator circuit must be considered (and possibly simulated) together to verify acceptability of performance.

The crystal chosen for operation with any of these oscillators must be a *fundamental-mode* unit. The frequency should be specified under parallel resonance conditions, with a load capacitance which is approximately 2 pF more than the series combination of capacitors ***Ca*** and ***Cb***. (***Ca*** and ***Cb*** include any stray capacitances present on their respective nodes). The frequency tolerance and stability should be specified according to the needs of the application; ± 100 ppm is commonly available at reasonable cost, with tighter specs available at higher cost.

A ceramic resonator behaves like a low-Q crystal and may be used as a less-expensive alternative to the quartz crystal with any of these oscillators. Generally, this substitution trades off some degree of frequency stability for lower component cost and faster oscillator startup.

The Negative Resistance Plot

It is convenient to characterize an oscillator circuit in terms of its negative resistance. The impedance seen looking into the oscillator terminals (with the crystal removed) consists of a negative imaginary part (indicating net capacitance) and a negative real part (see Figure 2). The negative real part is in-

dicative of the circuit's potential for oscillation. A parallel resonant crystal appears as an equivalent resistance-inductance series combination. If the magnitude of negative resistance (at the crystal frequency) is greater than the crystal resistance, the net resistance will be negative, and the circuit will oscillate at the frequency where the crystal's inductance cancels the circuit's capacitance.

The oscillator cell datasheet displays its negative resistance versus frequency. To produce a more useful graph, we have included the shunt capacitance of the crystal (***C0***) and the capacitors ***Ca*** and ***Cb*** with the oscillator in plotting the negative resistance characteristics shown in the oscillator data sheets. This way, the series resistance (***R1***) of the crystal may be directly compared to the negative-resistance plot. Not shown, but also included in the simulation which produced the negative resistance plots are typical stray capacitances of 5 pF from each crystal terminal (XLO, XHI) to ground and 2 pF between the crystal terminals.

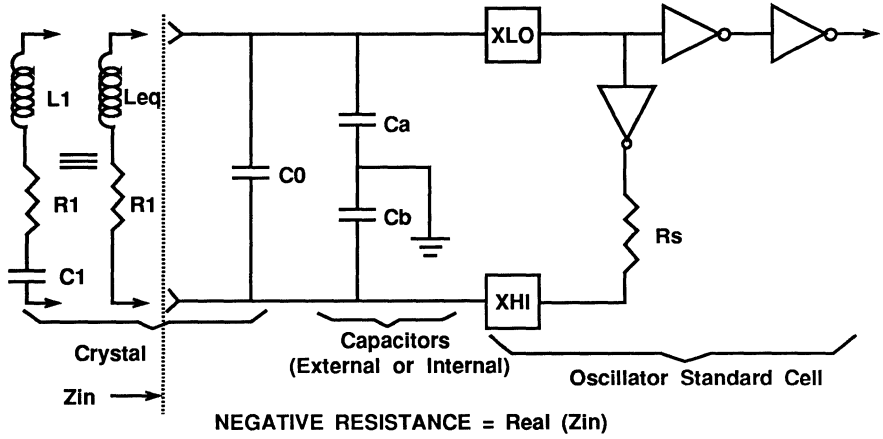


Figure 2. Comparison of Crystal Series Branch Impedance with Oscillator Impedance

Oscillator Operation

To determine whether oscillation is possible with a given crystal and oscillator, obtain the negative resistance at the crystal frequency from the plot in the data sheet. Compare the magnitude of negative resistance with the maximum resistance (***R1***) specified on the crystal data sheet. The crystal resistance should be smaller by at least a factor of two for reasonable loop-gain margin (reliable oscillation under a variety of conditions).

A capacitor (***Ca,Cb***) must be connected from each pad to circuit-ground for proper operation. External capacitors may be used, or the optional on-chip capacitors may be selected by choosing the proper oscillator. In the latter case, the only required external component is the crystal. For the XC20MSD oscillator, the two external capacitors should be the same value.

The oscillator frequency stability is primarily governed by the crystal but can be affected by any perturbation in the capacitances of the circuit. Generally, larger capacitances (at ***Ca*** and ***Cb***) produce better frequency stability, because unknown (e.g. stray) capacitances can be kept to a smaller fraction of the total.

A crystal behaves like a tuned circuit with a very high Q (quality factor). Because of this, many thousands of cycles are required for the amplitude of the oscillation to grow to its steady-state level after power is applied. Up to 20 ms should be allowed for oscillations to reach steady-state at lower (< 10 MHz) frequencies. Start-up time generally increases with increasing crystal Q, increasing capacitive load, and decreasing frequency.

Input Buffer Operation

If an external clock signal is available, the oscillator cell may be used as a noninverting input buffer. The XC20MSD is CMOS compatible. During input buffer operation, the input signal must be applied at the XLO pad, and the XHI pad must be left unconnected. External components (crystal, capacitors) should not be used during operation as an input buffer.

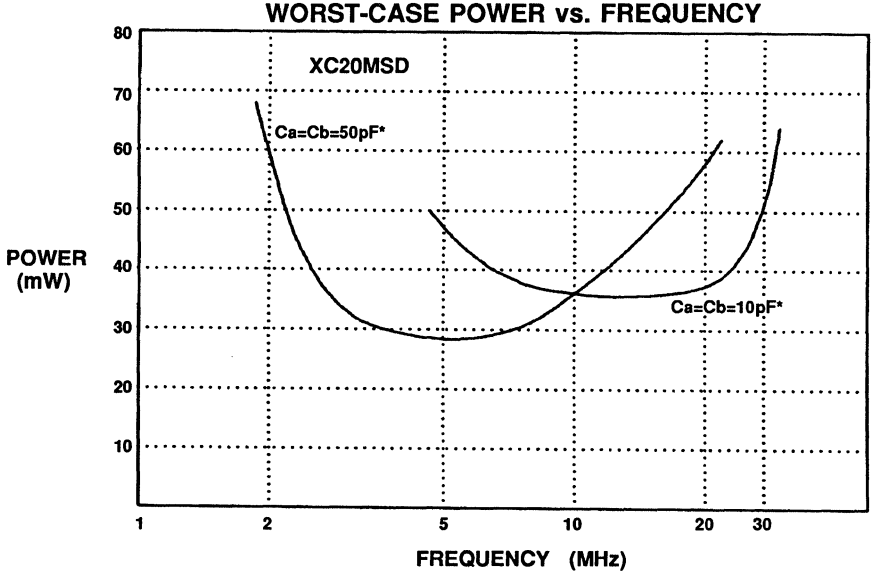
Standard Characterization Conditions

Worst-case characterization of the crystal oscillator cells has been performed under those conditions which minimize negative resistance and, separately, under those conditions which maximize power consumption:

- For negative resistance: maximum capacitance at XLO (***Ca***) and at XHI (***Cb***), worst-case slow processing, high (100 °C) temperature and low V_{DD} (4.5 V).
- For power consumption: maximum capacitance at XLO (***Ca***) and at XHI (***Cb***), worst-case fast processing, low (0 °C) temperature and high V_{DD} (5.5 V).

Power Consumption

The curves below display the worst-case simulated power consumption of the oscillator cell XC20MSD as a function of frequency for selected external capacitor values at XLO and XHI. Note that for each set of capacitor values, there is an optimum frequency for power consumption. Above this frequency, power increases with capacitance and frequency, as is usual for CMOS. However, at lower frequencies, power again increases because of increasing attenuation in the feedback network. A smaller signal level is available at the input of the CMOS inverter. This causes the P- and N-channel devices to remain simultaneously on during more of the waveform cycle, consuming higher dc power. Often, the power at low frequencies can be reduced by increasing capacitors ***Ca*** and ***Cb***. This increases the amplitude of the waveform at the inverter input and operates the stage in more of a switching mode, reducing the power consumption.



*External Capacitors

Crystal Oscillator

5 MHz - 32 MHz

XC20MS[*D,1D,2D*]

Functional Description

The XC20MSD family of oscillators provides stable rail-to-rail output waveforms suitable for clocking on-chip digital circuitry. The allowable frequency range, with proper capacitor selection, is from 5 MHz to 32 MHz. XC20MSD requires off-chip capacitors connected from each pad (XLO and XHI) to ground. XC20MS1D has on-chip 10pF capacitors connected from each pad to ground. XC20MS2D has on-chip 20pF capacitors connected from each pad to ground.

A fundamental-mode quartz crystal of the desired frequency must be connected between pads XLO and XHI. The crystal is operated in parallel resonance.

XC20MS[D,1D,2D] may also be used as a non-inverting input buffer by applying an external CMOS-level clock to XLO. XHI must remain unconnected.

The frequency of oscillation of this cell depends on the crystal used and the total capacitance appearing at the crystal terminals. This capacitance includes wiring and package parasitics, as well as capacitors Ca and Cb (whether external or internal).

The oscillator cell heights are compatible with digital D- and P-style buffers.

Netlist Order

Inputs: XLO
Outputs: XHI,OUT

Functional Description Of Inputs And Outputs

XLO: Oscillator input; connection of one crystal terminal and capacitor if used as an oscillator; CMOS-level input if used as an input buffer

XHI: Oscillator output; connection of one crystal terminal and capacitor if used as an oscillator; remains open if used as an input buffer

OUT: Output to clock on-chip circuitry

Circuit Information

Parameter	XC20MS[D,1D,2D]		
Frequency Range	5 MHz* to 32 MHz†		
Oscillator Power	SEE GENERAL INFORMATION, Page 9-6		
Duty Cycle	40% to 60%		
Freq Stability vs. V_{DD}‡	5 ppm/V		
Delay (Rising)§	0.66 ns + 0.10 ns/pF		
Delay (Falling)§	0.65 ns + 0.15 ns/pF		
Cell Size	529.2 µ × 283.5 µ		
On-Chip Capacitance	**XC20MSD**	**XC20MS1D**	**XC20MS2D**
Node XLO	3.9 pF	15.5 pF	26.9 pF
Node XHI	2.5 pF	14.0 pF	25.4 pF

* Ca=Cb=50 pF (Lower operating frequencies can be obtained with larger Ca and Cb).

† Ca=Cb=10 pF (off-chip capacitors with XC20MSD) The maximum frequency for XC20MS1D is 21MHz, and the maximum frequency for XC20MS2D is 12 MHz.

‡ Simulated with a typical 20MHz crystal having C1=0.02 pF, C0=4 pF, over a voltage range of 4.5 to 5.5 V at 25 °C, nominal process, and Ca=Cb=10 pF. Actual stability depends on the crystal and values of Ca and Cb.

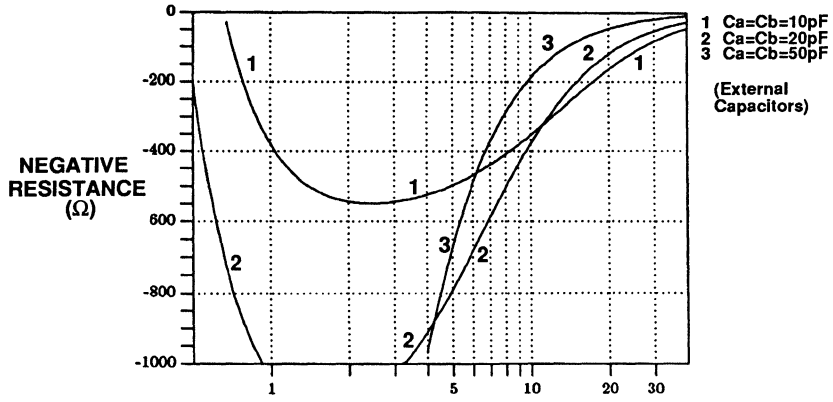
§ From XLO to OUT when used as an input buffer with V_{DD}=5 V, T=25 °C, nominal process.

5 MHz - 32 MHz

Negative Resistance - XC20MSD with 10 pF, 20 pF, and 50 pF External Capacitors

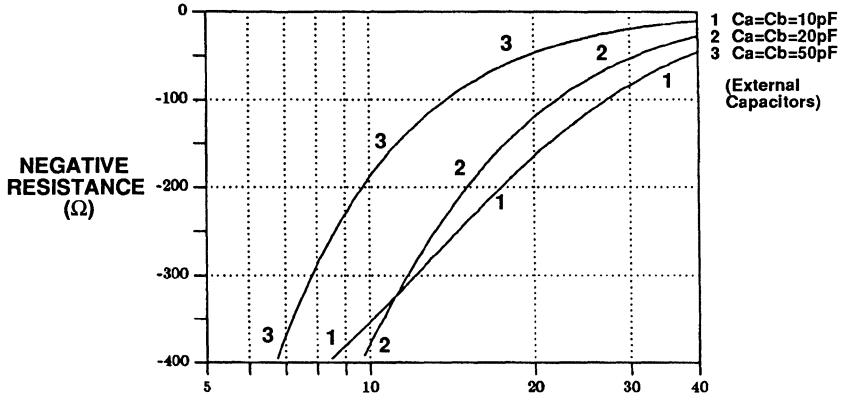
The real part of oscillator input impedance (including crystal shunt capacitance C0=7 pF, oscillator capacitors Ca and Cb, and stray capacitances) is displayed as a function of frequency.

WORST-CASE* NEGATIVE RESISTANCE vs. FREQUENCY



Negative Resistance (Expanded)

WORST-CASE* NEGATIVE RESISTANCE vs. FREQUENCY

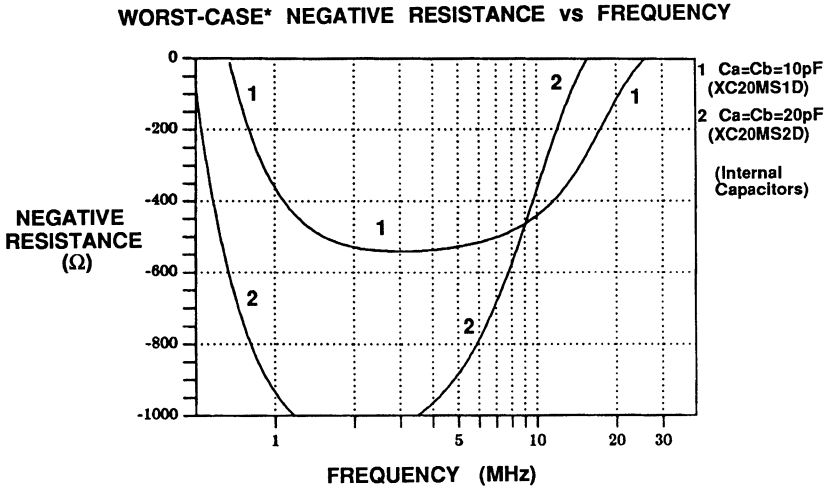


* Slow processing, V_{DD}=4.5 V, T=100 °C

5 MHz - 32 MHz

Negative Resistance - XC20MS1D and XC20MS2D - Internal Capacitors

The real part of oscillator input impedance (including crystal shunt capacitance C0=7 pF, oscillator capacitors Ca and Cb, and stray capacitances) is displayed as a function of frequency.



* Slow processing, VDD=4.5 V, T=100 °C

Capacitors CAP[*2A,3A,5A,10A,2P,3P,5P,10P*]

For Area- and Performance-Optimized Standard Cells

Functional Description

Unlike most linear standard cells, these capacitors are meant to be used in standard-cell rows rather than in the I/O buffer region. *The rows occupied by these cells must be separated by at least five routing tracks (≥ 9.5 μm) from other rows, or any special cells.*

The normal process-induced variation is ± 5%.

The capacitors are modeled in ADVICE as transistors. The transistor width and length is selected such that the gate area gives the desired value of capacitance. Process variation of the capacitance is caused by gate-oxide variation. The gate oxide, TOX, is defined in the process files; thus, using the worst-case fast and slow transistor files, aprohc.dat and aprolc.dat, automatically gives the proper capacitance variation due to processing.

The bottom plate of the capacitor is tied to Vss. Thus, physically, capacitors have only one terminal. A second terminal has been appended, though, in order to make the capacitors more amenable to digital CAD tools.

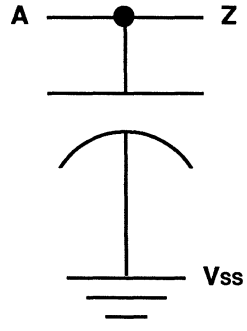
Netlist Order

Inputs: A
Outputs: Z

Cell Information

Cell Name	Cap Value	Number Of Grids
Area-Optimized		
CAP2A	2 pF	21
CAP3A	3 pF	27
CAP5A	5 pF	38
CAP10A	10 pF	67
Performance-Optimized		
CAP2P	2 pF	16
CAP3P	3 pF	21
CAP5P	5 pF	29
CAP10P	10 pF	51

SCHEMA SYMBOL



Delay Cells

DEL[*5A,10A,5P,10P*]

For Area- and Performance-Optimized Standard Cells

Functional Description

The delay cells are designed to fit into the standard-cell rows. Those ending in "A" fit into the area-optimized rows; those ending with "P" fit into the performance-optimized rows. The purpose of these cells is to provide a (non-inverting) delay to any digital signal. The delay times are shown in the table.

The delay function can be performed by a string of inverters. This has been done on many designs in the past, but the delay cells accomplish this using much less area for a comparable delay, from as little as 14% of the inverter's area for the DEL10P, to 37% for the DEL5A.

The rows occupied by these cells must be separated by at least five routing tracks (≥ 9.5 μm) from other rows or any special cells.

Netlist Order

Inputs: A
Outputs: Z

Cell Information

Cell Name	Minimum* Delay	Nominal Delay	Maximum† Delay	Cell Size (Grids)
Area-Optimized				
DEL5A	3.7 ns+0.8 ns/pF	4.9 ns+1.1 ns/pF	8.2 ns+2.0 ns/pF	21
DEL10A	7.1 ns+1.1 ns/pF	9.4 ns+1.5 ns/pF	15.8 ns+2.8 ns/pF	26
Performance-Optimized				
DEL5P	3.4 ns+0.8 ns/pF	4.5 ns+1.1 ns/pF	7.7 ns+2.0 ns/pF	16
DEL10P	6.9 ns+1.1 ns/pF	9.0 ns+1.5 ns/pF	15.1 ns+2.8 ns/pF	19

* Minimum delay: fast process, V_{DD}=5.5 V, T=0 °C

† Maximum delay: slow process, V_{DD}=4.5 V, T=100 °C

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Resistors

For Area- and Performance-Optimized Standard Cells

RES[*5A,10A,20A, 5P,10P,20P*]

Functional Description

Unlike most linear standard cells, these resistors are meant to be used in standard-cell rows rather than in the I/O buffer region.

The normal process-induced variation is ±22%, **not** including temperature variation. The best way to do worst-case fast and slow ADVICE runs with resistors is to change the resistor-model parameter. The resistor model, RNTUB, is defined so that all resistors can be globally scaled with a single command:

.MODEL RNTUB SCAL=3800 ("slow resistors," default value in aprolc.dat)

or

.MODEL RNTUB SCAL=2400 ("fast resistors," default value in aprohc.dat)

The default value of ***SCAL*** is 3100 in the process file apronc.dat. Unfortunately, the process-induced resistor variation does not correlate with the transistor speed. This means that while the use of aprolc.dat and .MODEL RNTUB SCAL=3800 will give the maximum delay, and aprohc.dat and .MODEL RNTUB SCAL=2400 will give the minimum delay, the other two combinations of transistor and resistor speeds may have to be investigated for paths where critical races are possible. Temperature variation is included in the RNTUB model.

Netlist Order

Inputs: A

Outputs: Z

Cell Information

Cell Name	Nominal Resistor Value	Number Of Grids
Area-Optimized		
RES5A	5 KΩ	17
RES10A	10 KΩ	26
RES20A	20 KΩ	44
Performance-Optimized		
RES5P	5 KΩ	17
RES10P	10 KΩ	26
RES20P	20 KΩ	44

SCHEMA SYMBOL

FDS Synthesized Macrocells

Section 10

Contents - Section 10

Functional Design System — Introduction

The FDS is a logic-synthesis system that automatically generates the netlist implementation in standard cells of several parameterizable functional primitives. For each primitive, a wide range of user-definable features is available.
The following primitives are supported in FDS:

- Adders
- Arithmetic and logic units
- Combinational blocks
- Comparators
- Counters
- Decoders
- Finite-state machines
- Multiplexers
- Parity generators
- Registers

The FDS also features a friendly interface for capturing the design parameters and the external view of desired primitives. In addition, schematics corresponding to the netlist of the primitive may be generated. The FDS consists of standard cells from either the performance- or area-optimized library. All of the FDS functional primitives' features are user-selectable, creating a large variety of possible configurations. For more information on how to generate these cells, consult the FDS manual.

Specifically, the following functions are available:

Capture symbol	Prompts the user to define an external view and specify the applicable options of a funtional primitive
Simulation model	Produces a simulation model for MOTIS3
Synthesize	Implements the captured functional primitive
Draw schematic	Displays the internal schematic of the synthesized, standard-cell, functional primitive

A functional primitive in the FDS may be added to a schematic diagram in SCHEMA, which may then be used to generate a connectivity list incorporating the primitive as part of an integrated circuit design. The connectivity list is available in two formats: the LSL format, which may be used for simulation in MOTIS3, and the ADVICE format, used as input to ADVICE program. Hard copies of the final schematics can be produced on an off-line plotter.

Functional Description and Features

The FDS **adder** is a netlist that can be parameterized with many options.

The ADDER has the following features:

- Bus or non-bus pin notation
- Optional carry-input
- Optional carry-output
- Inverted/noninverted inputs and outputs
- Optional ripple carry
- Optional carry-look-ahead
- Optional mixture of ripple-carry and carry-look-ahead
- Fully combinatorial

ADDER can be customized with the parameter N, as shown in the following table:

Parameter	Description	Limit		
		Increment	Min	Max
N	Bits	1	2	128

Terminal Descriptions

Netlist Order

Option-dependent; consult the FDS manual.

Functional Descriptions

INPUTS:

A[N-1:0]	First input to add
B[N-1:0]	Second input to add
CI	Optional carry-in

OUTPUTS:

S[N-1:0]	Sum of A[N-1:0] and B[N-1:0]
CO	Optional carry-out

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Characterization

Because of the large number of possible configurations, no attempt was made to characterize the ADDER cell. It is advisable to run CRITIC after generating any FDS block to verify that the performance matches your requirements.

Functional Description and Features

The FDS **arithmetic and logic unit** allows the user to select one or more operations from a variety of supported arithmetic, boolean, and comparison operations. The size of an ALU may vary from 2 to 128 bits.

An ALU may contain two input ports (A and B), an input port for select lines (SEL), an output port (D), and a line (F) which contains the carry/borrow results of arithmetic operations and the results of comparison operations. Bus notation is available for the lines of ports A, B, and D.

The ALU may be customized by selecting one or more of the following operations. The description of each operation includes its function and the input port(s) and output(s) used.

Arithmetic operations:

- ADD D = A + B ; carry ignored
- ADDC D = A + B ; F = carry
- SUB D = A - B ; carry ignored
- SUBC D = A - B ; F = borrow
- INCRA D = A + 1 ; carry ignored
- INCRAC D = A + 1 ; F = carry
- DECRA D = A - 1 ; borrow ignored
- DECRAC D = A - 1 ; F = borrow
- UMINUSB D = -B = two's complement of B; borrow ignored
- UMINUSBC D = -B = two's complement of B; F = borrow

Boolean operations:

- AND D = A and B
- OR D = A or B
- NAND D = **not** (A and B)
- NOR D = **not** (A or B)
- XOR D = A xor B
- XNOR D = **not** (A xor B)
- NOTA D = **not** (A)
- NOTB D = **not** (B)

Comparison operations:

- EQL F = 1 if A = B, else F = 0
- NEQ F = 1 if A! = B, else F = 0
- LT F = 1 if A < B, else F = 0
- LE F = 1 if A <= B, else F = 0
- GT F = 1 if A >B, else F = 0
- GE F = 1 if A >= B, else F = 0

10

Terminal Descriptions

Netlist Order

Dependent on the number of operations; consult the FDS manual.

Functional Descriptions

INPUTS:

A[N-1:0]	Signals of the A input port
B[N-1:0]	Signals of the B input port
SEL[8:0]	Select lines; dependent on the operations selected

OUTPUTS:

D[N-1:0]	Signals of the output port
F	Contains borrow/carry result for applicable arithmetic operations and the result of comparison operations

Characterization

Because of the large number of possible configurations, no attempt was made to characterize the ALU cell. It is advisable to run CRITIC after generating any FDS block to verify that the performance matches your requirements.

FDS Combinational Block CMB

Functional Description and Features

The FDS **combinational block** allows the user to specify multiple output combinational circuits. The output functions are defined with either truth table or Boolean equation format.

The CMB has the following features:

- Various logic minimization techniques
- Use of complements as candidates for synthesis
- Optional user-specified input and output names
- Optional user-specified, maximum fan-in for gates (a value less than nine fan-ins, the default)

CMB can be customized with the parameters M and N as shown in the following table:

Parameter	Description	Limit		
		Increment	Min	Max
M	Input Pins	1	1	128-N
N	Output Pins	1	1	128-M

Terminal Descriptions

Netlist Order

Option-dependent; consult the FDS manual.

Functional Descriptions

INPUTS:

IN_NAME_1, IN_NAME_2,..... IN_NAME_M
User-defined, no default name

OUTPUTS:

OUT_NAME_1, OUT_NAME_2,..... OUT_NAME_N
User-defined, no default name

Characterization

Because of the large number of possible configurations, no attempt was made to characterize the CMB cell. It is advisable to run CRITIC after generating any FDS block to verify that the performance matches your requirements.

FDS Comparator COMP

Functional Description and Features

The FDS **comparator** compares two binary or decimal numbers for logical conditions selected by the user. Logical conditions include magnitude (greater-than/less-than), equality (inequality), and combinations of magnitude and equality.

The COMP has the following features:

- Optional decimal or binary comparator structure
- BCD, EXCESS-3, or EXCESS-3-GRAY codes are available for the decimal decoder
- Bus or non-bus pin notation
- One or more comparison criteria can be chosen
- Optional active-low or active-high output signals
- Optional inverted inputs

COMP can be customized with the parameter N, as shown in the following table:

Parameter	Description	Limit		
		Increment	Min	Max
N	Binary Bits	1	2	256
N	Decimal Bits	4	4	256

Terminal Descriptions

Netlist Order

Option-dependent; consult the FDS manual.

Functional Descriptions

INPUTS:

A[N-1:0]	Operand A
B[N-1:0]	Operand B

OUTPUTS:

LT	A < B
EQ	A = B
GT	A > B
LE	A <= B
GE	A >= B
NE	A ! = B

Characterization

Because of the large number of possible configurations, no attempt was made to characterize the COMP cell. It is advisable to run CRITIC after generating any FDS block to verify that the performance matches your requirements.

Functional Description and Features

The FDS **counter** is a binary up-or-down counter. The size of counter may vary from 2 to 128 bits. Counters with more than 16 bits use ripple carry.

The COUNTER has the following features:

- Optional parallel load
- Bus or non-bus pin notation
- Optional bits tapped as Q (QN) outputs
- Optional up, down, or up-down counting scheme
- Optional decode-binary counter
- Optional fast or ripple-carry scheme
- Optional PRESET, PRECLEAR, or INITIALIZATION control signal
- Optional asynchronous or synchronous control timing
- Optional inhibit signal
- Optional dynamic or static clocking scheme
- Optional rising or falling edge-triggered static clock

COUNTER can be customized with the parameter N, as shown in the following table:

Optional Condition	Parameter	Description	Limit		
			Increment	Min	Max
Ripple Carry	**N**	Bits	1	2	128
Fast Carry	**N**	Bits	1	2	16
Initial Signal	**N**	Bits	1	2	30
Decade Counter	**N**	Bits	_	4	4

Terminal Descriptions

Netlist Order

Option-dependent; consult the FDS manual.

Functional Descriptions

INPUTS:

PI[N-1:0]	Parallel-loaded input signals
CTLD	Count/load control
CUCD	Counter up/down control
CI	Carry-In
INH	Control input clock inhibit signal
PS	Preset sets each bit in the counter to 1
PC	Preclear sets each bit in the counter to 0
INIT	Initialization sets the counter to a bit pattern specified by the user
CK	Static clocking is triggered by the rising edge or the falling edge of the clock
MCK,SCK,MCKN,SCKN	Four clocks for dynamic clocking

OUTPUTS:

Q[N-1:0]	Output signals of the counter
QN[N-1:0]	Complementary output signals of the counter
CO	Carry-out

Characterization

Because of the large number of possible configurations, no attempt was made to characterize the COUNTER cell. It is advisable to run CRITIC after generating any FDS block to verify that the performance matches your requirements.

Functional Description and Features

The FDS **decoder** is a select-line to output-line decoder. Select lines (inputs) jointly represent a binary or decimal-encoded number.

The DECODER has the following features:

- Optional decimal and binary decoder structure
- BCD, EXCESS-3 or EXCESS-3-GRAY codes are available for decimal decoders
- Bus or non-bus pin notation
- User-specified number of select and output lines, using guidelines given below
- Optional inverted select lines
- Optional active-low or active-high output signal
- Optional enable signal

DECODER can be customized with the parameters M and N as shown in the following table:

Decoder	Parameter	Description	Limit		
			Increment	Min	Max
Binary	M	Select Lines	1	1	10
	N	Output Lines	1	$2^{M-1}+1$	2^{M}

Decoder	Output Lines	Select Lines	Limit		
			Increment	Min	Max
Decimal*	N	M=4	1	2	10
	N	M=8	1	11	100

*For decimal decoder, the select lines must equal 4 or 8; the number of output lines for each configuration is specified above.

10

Terminal Descriptions

Netlist Order

Option-dependent; consult the FDS manual.

Functional Descriptions

INPUTS:

S[**M**-1:0]	Select lines
EN	Enable signal

OUTPUTS:

Y[**N**-1:0]	It sets the output line that has the same numeric value as the encoded number to its active voltage level.

Characterization

Because of the large number of possible configurations, no attempt was made to characterize the DECODER cell. It is advisable to run CRITIC after generating any FDS block to verify that the performance matches your requirements.

FDS Finite-State Machine FSM

Functional Description and Features

The FDS **finite-state machine** synthesizer models circuit behavior in terms of a number of states, state transitions, and output functions. The FSM synthesizer produces implementation in standard cells, and input files for MOTIS3 functional simulation.

The FSM has the following features:

- Support of vector format for inputs and outputs
- User-specified inputs and outputs
- Specification of state transitions and output functions via state-transition diagram
- User-specified INITIALIZATION signal
- Optional asynchronous or synchronous control scheme
- Optional dynamic or static clocking scheme
- Optional rising edge or falling edge of static clock
- Create a simulation model for input to MOTIS3
- State-based simulation

FSM has the following constrain:

Inputs + outputs + present-state signals + next-state signals ≤ 128

Terminal Descriptions

Netlist Order

Option-dependent; consult the FDS manual.

Functional Descriptions

INPUTS:

User-defined

CK	Static clocking is triggered by the rising edge or the falling edge of the clock
MCK,SCK,MCKN,SCKN	Four clocks for dynamic clocking
INIT	Initializationl signal

OUTPUTS:

User-defined

Characterization

Because of the large number of possible configurations, no attempt was made to characterize the FSM. It is advisable to run CRITIC after generating any FDS block to verify that the performance matches your requirements.

Functional Description and Features

The FDS **multiplexer** is a multi-word-to-one-word or multi-line-to-one-line multiplexer.

The MUX has the following features:

- Bus or non-bus pin notation
- Optional encoded select lines
- User-specified number of words and number of bits per word
- Optional inverted select lines
- Optional enable signal
- Optional forced outputs to high, low, or 3-state when enable signal is inactive
- Optional complementary outputs
- Optional use of large cells (e.g. AOI3333)

MUX(N,M) can be customized with the parameters K, M, and N as shown in the following table:

Parameter	Description	Limit		
		Increment	Min	Max
N	Words	1	2	M*N ≤ 512
M	Bits/word	1	2	16

Parameter	Description	Value
K	Select lines (nonencoded)	N
K	Select lines (encoded)	$\log_2 N$

10

Terminal Descriptions

Netlist Order

Option-dependent; consult the FDS manual.

Functional Descriptions

INPUTS:

D[**N**-1:0, **M**-1:0]	The root name for the input signals
S[**K**-1:0]	Select lines
EN	Optional enable line

OUTPUTS:

Y[**N**-1:0]	Normal output
YN[**N**-1:0]	Complementary output

Characterization

Because of the large number of possible configurations, no attempt was made to characterize the MUX cell. It is advisable to run CRITIC after generating any FDS block to verify that the performance matches your requirements.

FDS Parity Generator PAR

Functional Description and Features

The FDS **parity generator** can generate odd, even, or odd and even parity via the implementation of a tree of XOR cells.

PAR has the following features:

- Bus or non-bus pin notation
- User-specified number of bits
- Optional inverted inputs
- Optional parity generated of ODD, EVEN, or BOTH
- Optional active-low or active-high output signals

PAR can be customized with the parameter N as shown in the following table:

Parameter	Description	Limit		
		Increment	Min	Max
N	Bits	1	2	512

Terminal Descriptions

Netlist Order

Option-dependent; consult the FDS manual.

Functional Descriptions

INPUTS:

D[N-1:0]	N bits inputs

OUTPUTS:

ODD	When ODD or BOTH parity is selected
EVEN	When EVEN or BOTH parity is selected

10

Characterization

Because of the large number of possible configurations, no attempt was made to characterize the PAR cell. It is advisable to run CRITIC after generating any FDS block to verify that the performance matches your requirements.

Functional Description and Features

The FDS **uni**versal **reg**ister can be an ordinary latch (parallel-in, parallel-out) or a shift (serial-in, parallel-out) register. It also accommodates combined parallel and serial input to parallel output.

The UNREG has the following features:

- Shift can be right-to-left, left-to-right, or bidirectional
- Optional parallel, serial or both of data input mode
- Bus or non-bus pin notation
- Optional bits tapped as Q (QN) outputs, also allow the user to enter the specified bit-pattern for tapping Q (QN) output signals
- PRESET, PRECLEAR, and INITIALIZATION are available with asynchronous or synchronous control
- Optional inhibit signal INH
- Optional dynamic or static clocking scheme
- Optional rising or falling edge of static clock

UNREG can be customized with the parameter N as shown in the following table:

Condition	Parameter	Description	Limit		
			Increment	Min	Max
Normal	N	Bits	1	2	128
With Initialization Signal	N	Bits	1	2	30

Terminal Descriptions

Netlist Order

Option-dependent; consult the FDS manual.

Functional Descriptions

INPUTS:

PI[N-1:0]	The root name of input signal
LE	Left entry (right shift)
RE	Right entry (left shift)
RL	Bidirectional shift
SHLD	Shift/Load
INH	Inhibit signal
PS	Preset
PC	Preclear
INIT	Initialization signal
CK	Static clocking is triggered by the rising edge or the falling edge of the clock
MCK,SCK,MCKN,SCKN	Four clocks for dynamic clocking

OUTPUTS:

Q[N-1:0]	Normal outputs
QN[N-1:0]	Complementary outputs

Characterization

Because of the large number of possible configurations, no attempt was made to characterize the UNREG cell. It is advisable to run CRITIC after generating any FDS block to verify that the performance matches your requirements.

MSI/LSI Functions

Section 11

Contents - Section 11

Introduction

This section describes a variety of digital functions that are available in the 0.9µm CMOS Library. Many of the functions are provided as standard-cell netlists and can either be used 'as-is' or can be modified to suit your particular needs. Using one of these netlists as a starting point could save you some time compared to starting from scratch.

The *CM*-series of cells in this section is very similar to some 74XX-series functions. For example, the CM42 is functionally equivalent to the 7442 4-Line-to-10-Line, BCD-to-Decimal Decoder.

The functionality for these cells is described either in detailed schematics (for simple functions) or in the block diagrams (for more complex functions).

Timing characteristics provided in this section are obtained with AT&T's static timing analyzer, CRITIC. They are estimated with an average routing capacitance of 0.10 pF per fanout. The more accurate circuit simulator, GSIM, should be used to verify the proper timing for your final designs.

For more detailed information regarding the use of these functions, please contact your AT&T representative.

2-Bit Arithmetic Logic Unit — ALU2

146 grids, 214 transistors

Functional Description and Features

The ALU2 performs arithmetic and logic operations on two 2-bit words. These operations are selected by four function-select lines (S0, S1, S2, S3). The operation mode is controlled by the LAN input. It is implemented with standard-cells.

- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Other arithmetic operations
- Logic function modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Other logic operations

Terminal Descriptions

Netlist Order

INPUTS: A0, A1, B0, B1, S0, S1, S2, S3, CN0, LAN

OUTPUTS: F0, F1, XN, YN, CNP2, AEB

Functional Descriptions

Inputs:

A[0:1]	Word A inputs
B[0:1]	Word B inputs
S[0:3]	Function-select inputs
CN0	Inverted carry input
LAN	Mode control input

Outputs:

F[0:1]	Function outputs
XN	Carry PROPAGATE output
YN	Carry GENERATE output
CNP2	Inverted carry output
AEB	Comparator output

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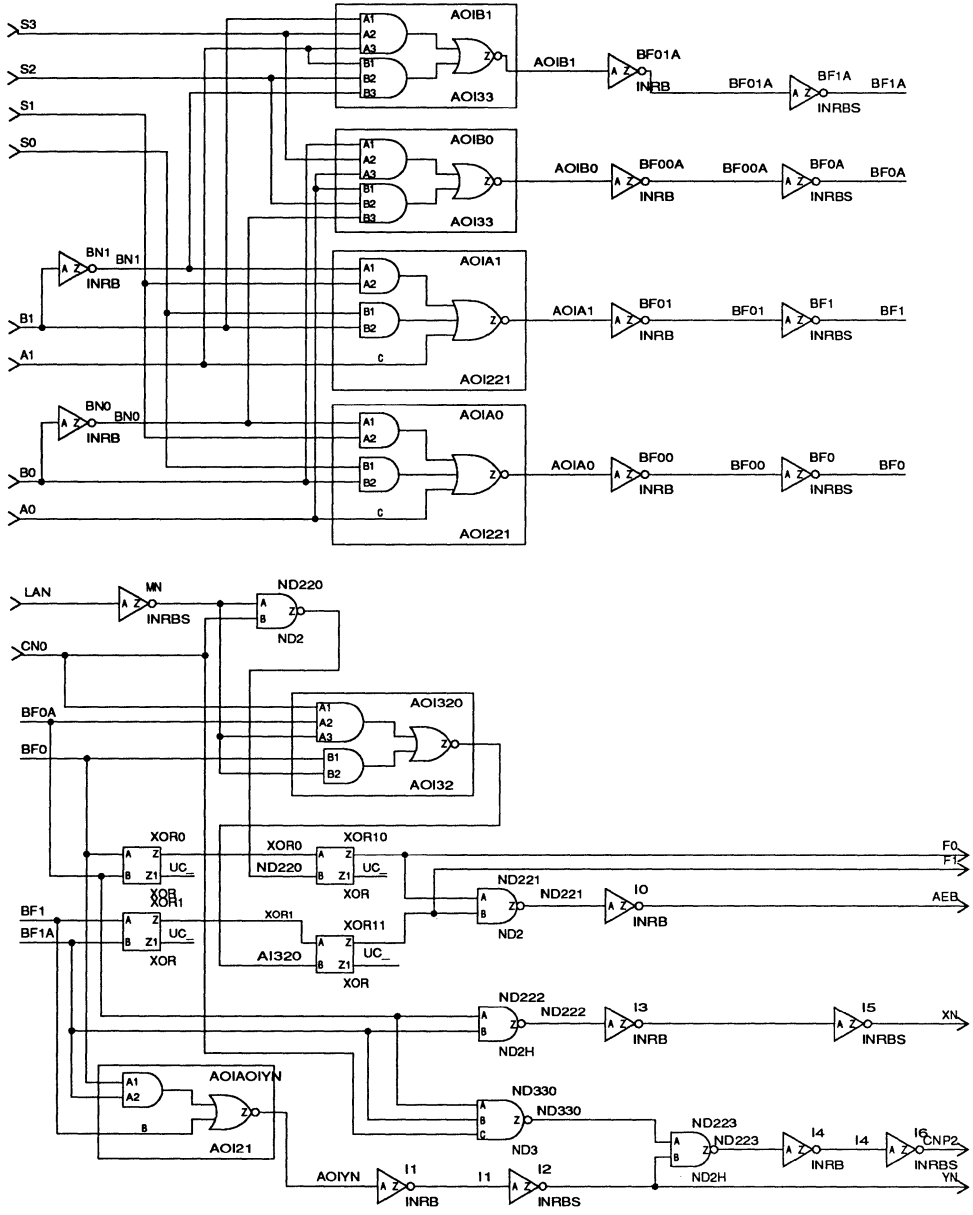
Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
A[0:1],B[0:1],S[0:3]	AEB↑	8.86	3.24	4.11	0.77
A[0:1],B[0:1],S[0:3]	AEB↓	8.23	2.31	3.83	0.58
A[0:1],B[0:1],S[0:3]	CNP2↑	7.94	0.86	3.71	0.21
A[0:1],B[0:1],S[0:3]	CNP2↓	8.57	0.86	4.17	0.21
A[0:1],B[0:1],S[0:3]	F[0:1]↑	7.43	8.98	3.49	2.01
A[0:1],B[0:1],S[0:3]	F[0:1]↓	7.31	12.68	3.43	2.71
A[0:1],B[0:1],S[0:3]	XN↑	5.71	0.86	2.74	0.21
A[0:1],B[0:1],S[0:3]	XN↓	5.60	0.86	2.69	0.21
A[0:1],B[0:1],S[0:3]	YN↑	7.09	0.86	3.37	0.21
A[0:1],B[0:1],S[0:3]	YN↓	6.80	0.86	3.14	0.21
CN0	AEB↑	4.11	3.24	1.94	0.70
CN0	AEB↓	3.54	2.31	1.83	0.58
CN0	CNP2↑	2.46	0.86	1.37	0.21
CN0	CNP2↓	2.40	0.86	1.20	0.21
CN0	F[0:1]↑	2.69	8.98	1.31	2.01
CN0	F[0:1]↓	2.63	12.68	1.43	2.71
LAN	AEB↑	4.34	3.24	2.06	0.70
LAN	AEB↓	3.77	2.31	1.83	0.58
LAN	F[0:1]↑	2.91	8.98	1.43	2.01
LAN	F[0:1]↓	2.86	12.68	1.43	2.71

Functional Modes

SELECTION				ACTIVE HIGH DATA		
				LAN=H	LAN=L ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	CN0=H (no carry)	CN0=L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A plus 1
L	L	L	H	F = $\overline{A+B}$	F = A+B	F = (A+B) plus 1
L	L	H	L	F = $\overline{A}$B	F = A+$\overline{B}$	F = (A+$\overline{B}$) plus 1
L	L	H	H	F = zero	F = minus 1 (2's Compl)	F = zero
L	H	L	L	F = $\overline{AB}$	F = A plus A$\overline{B}$	F = A plus A$\overline{B}$ plus 1
L	H	L	H	F = $\overline{B}$	F = (A+B) plus A$\overline{B}$	F = (A+B) plus A$\overline{B}$ plus 1
L	H	H	L	F = A⊕B	F = A minus B minus 1	F = A minus B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ minus 1	F = $\overline{A}$B
H	L	L	L	F = $\overline{A}$+B	F = A plus AB	F = A plus AB plus 1
H	L	L	H	F = $\overline{A⊕B}$	F = A plus B	F = A plus B plus 1
H	L	H	L	F = B	F = (A+$\overline{B}$) plus AB	F = (A+$\overline{B}$) plus AB plus 1
H	L	H	H	F = AB	F = AB minus 1	F = AB
H	H	L	L	F = 1	F = A plus A*	F = A plus A plus 1
H	H	L	H	F = A+$\overline{B}$	F = (A+B) plus A	F = (A+B) plus A plus 1
H	H	H	L	F = A+B	F + (A+$\overline{B}$) plus A	F = (A+$\overline{B}$) plus A plus 1
H	H	H	H	F = A	F = A minus 1	F = A

* Means LEFT SHIFT operation on A.

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4-Bit Arithmetic Logic Unit — ALU4

316 grids, 462 transistors

Functional Description and Features

The ALU4 is functionally equivalent to the 74181 Arithmetic Logic Unit/Functional Generator within the standard 74XX Series logic families of devices. The ALU4 performs arithmetic and logic operations on two 4-bit words. These operations are selected by four function-select lines (S0, S1, S2, S3). The operation mode is controlled by the LAN input. It is implemented with standard-cells.

- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Other arithmetic operations
- Logic function modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Other logic operations

Terminal Descriptions

Netlist Order

INPUTS: A0, A1, A2, A3, B0, B1, B2, B3, S0, S1, S2, S3, CN0, LAN

OUTPUTS: F0, F1, F2, F3, XN, YN, CNP4, AEB

Functional Descriptions

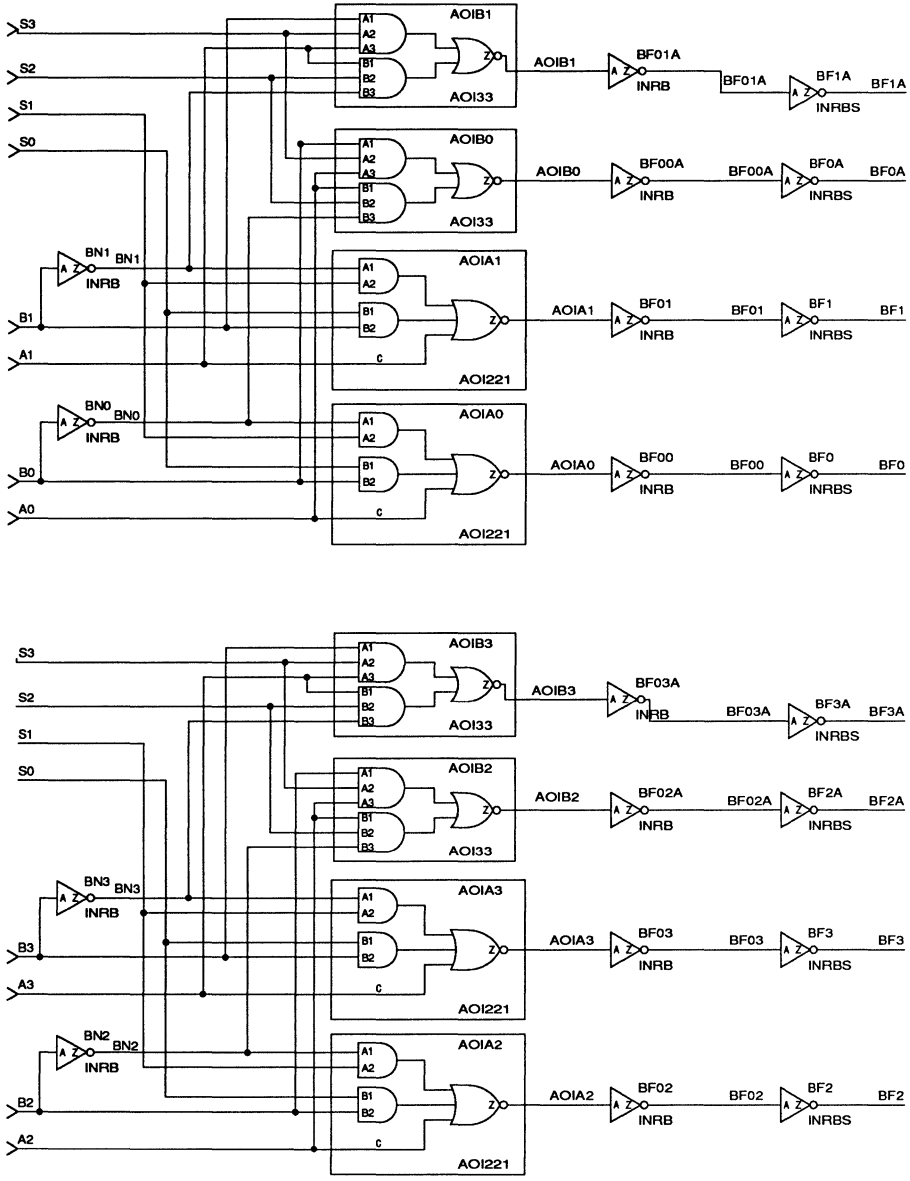
Inputs:

A[0:3]	Word A inputs
B[0:3]	Word B inputs
S[0:3]	Function-select inputs
CN0	Inverted carry input
LAN	Mode control input

Outputs:

F[0:3]	Function outputs
XN	Carry PROPAGATE output
YN	Carry GENERATE output
CNP4	Inverted carry output
AEB	Comparator output

Detailed Schematic



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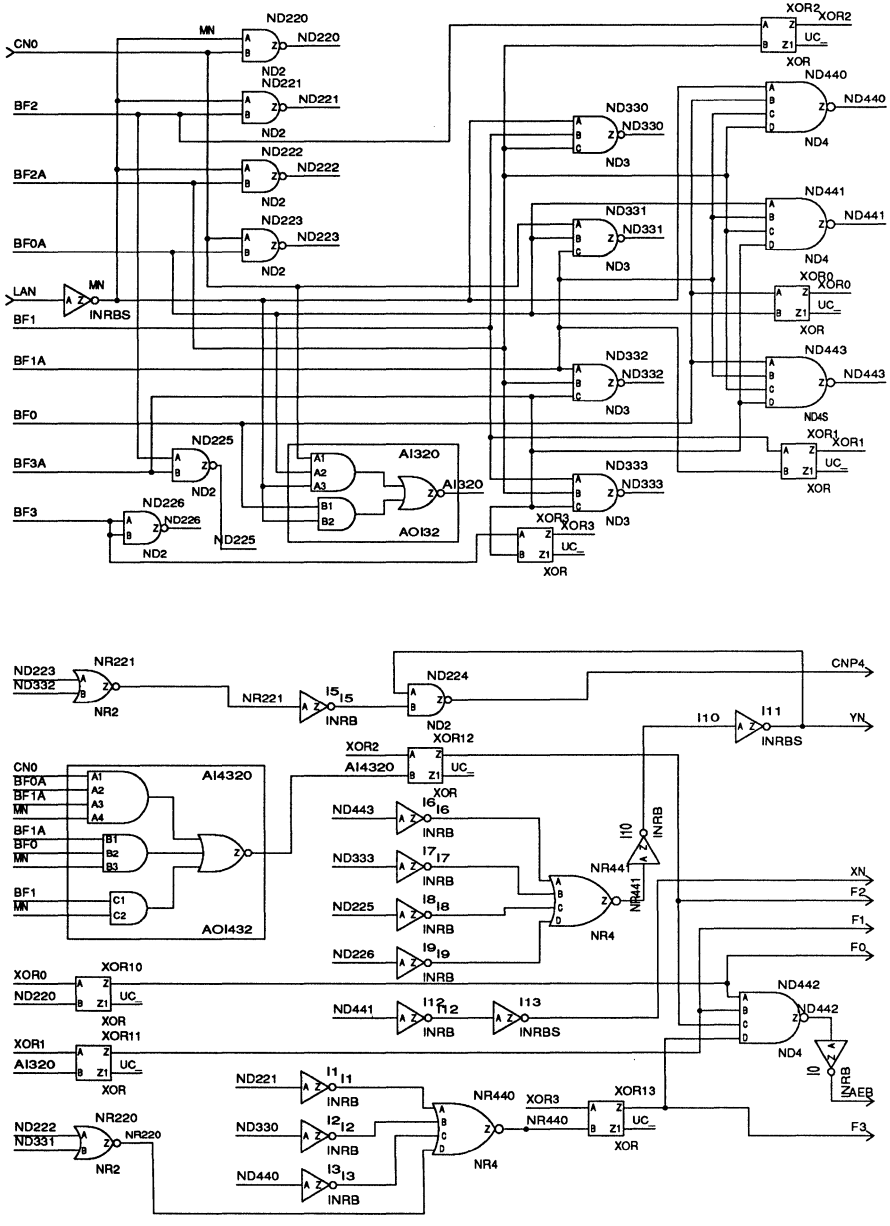
Detailed Schematic (continued)



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
A[0:3],B[0:3],S[0:3]	AEB↑	12.74	3.24	6.00	0.70
A[0:3],B[0:3],S[0:3]	AEB↓	11.66	2.31	5.37	0.58
A[0:3],B[0:3],S[0:3]	CNP4↑	8.80	3.24	4.00	0.66
A[0:3],B[0:3],S[0:3]	CNP4↓	10.69	4.10	4.91	1.07
A[0:3],B[0:3],S[0:3]	F[0:3]↑	10.57	8.98	4.97	2.01
A[0:3],B[0:3],S[0:3]	F[0:3]↓	10.69	12.68	4.91	2.71
A[0:3],B[0:3],S[0:3]	XN↑	6.74	0.86	3.26	0.21
A[0:3],B[0:3],S[0:3]	XN↓	7.54	0.86	3.60	0.21
A[0:3],B[0:3],S[0:3]	YN↑	10.51	0.86	4.80	0.21
A[0:3],B[0:3],S[0:3]	YN↓	8.69	0.86	3.94	0.21
CN0	AEB↑	7.60	3.24	3.54	0.70
CN0	AEB↓	6.51	2.31	2.91	0.58
CN0	CNP4↑	2.80	3.24	1.20	0.66
CN0	CNP4↓	2.11	4.10	0.86	1.07
CN0	F[0:3]↑	5.43	8.98	2.51	2.01
CN0	F[0:3]↓	5.54	12.68	2.46	2.71
LAN	AEB↑	8.46	3.24	3.94	0.70
LAN	AEB↓	7.37	2.31	3.31	0.58
LAN	F[0:3]↑	6.29	8.98	2.91	2.01
LAN	F[0:3]↓	6.40	12.68	2.86	2.71

Functional Modes

SELECTION				ACTIVE HIGH DATA		
				LAN=H	LAN=L ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	CN0=H (no carry)	CN0=L (with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A plus 1
L	L	L	H	$F = \overline{A+B}$	F = A+B	F = (A+B) plus 1
L	L	H	L	$F = \overline{A}B$	$F = A+\overline{B}$	$F = (A+\overline{B})$ plus 1
L	L	H	H	F = zero	F = minus 1(2's Compl)	F = zero
L	H	L	L	$F = \overline{AB}$	$F = A$ plus $\overline{AB}$	$F = A$ plus $\overline{AB}$ plus 1
L	H	L	H	$F = \overline{B}$	$F = (A+B)$ plus $\overline{AB}$	$F = (A+B)$ plus $\overline{AB}$ plus 1
L	H	H	L	$F = A \oplus B$	F = A minus B minus 1	F = A minus B
L	H	H	H	$F = A\overline{B}$	$F = A\overline{B}$ minus 1	$F = A\overline{B}$
H	L	L	L	$F = \overline{A}+B$	F = A plus AB	F = A plus AB plus 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A plus B	F = A plus B plus 1
H	L	H	L	F = B	$F = (A+\overline{B})$ plus AB	$F = (A+\overline{B})$ plus AB plus 1
H	L	H	H	F = AB	F = AB minus 1	F = AB
H	H	L	L	F = 1	F = A plus A*	F = A plus A plus 1
H	H	L	H	$F = A+\overline{B}$	F = (A+B) plus A	F = (A+B) plus A plus 1
H	H	H	L	F = A+B	$F + (A+\overline{B})$ plus A	$F = (A+\overline{B})$ plus A plus 1
H	H	H	H	F = A	F = A minus 1	F = A

* Means LEFT SHIFT operation on A.

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UART

ARTI

7736 grids, 11268 transistors

Functional Description and Features

The ARTI is an asynchronous receiver/transmitter interface. The device is used as a single-channel, half-duplex or full-duplex interface with data communication equipment (DCE) and data terminal equipment (DTE). The ARTI is compatible with the bus protocol and timing specifications of the Intel 8051 Microcontroller and the Intel 8088 Microprocessor and can be used in a polled or interrupt-driven system.

To reduce the interrupt overhead and potential for overruns, the transmitter has four data buffers and the receiver has six.

This netlist is a circuit that can also be obtained as a stand-alone IC. Two package styles are available; a 24-pin, plastic DIP and a 28-pin SOJ. Contact your AT&T Representative for more information.

- Programmable data format:
  - Seven data bits plus parity
  - Odd, even, no parity
  - One or two stop bits
- Six receive and four transmit data buffers
- Receive break detection and transmit break generation.
- Intel 8088 and 8051 Microprocessor interface without wait-states.
- Clear-to-send/request-to-send selectable signals for DTE or DCE modes and EIA flow control.
- Programmable interrupt system:
  - Fill-level interrupt of receive FIFOs (first-in, first-out).
  - Receive break detection and error-interrupt.
  - Empty level of transmit FIFO.
- Transmit/receive FIFO status bits indicate FIFO levels.
- Flexible polling capabilities.
- On-chip, programmable baud rate generator.
- Speed-matching (autobaud) capability.

Terminal Descriptions

Netlist Order

INPUTS: ADI0, ADI1, ADI2, ADI3, ADI4, ADI5, ADI6, ADI7, RDN, WRN, ALE, CSN, HWRESET, CLK1, SERDATIN, RTS, DTR

OUTPUTS: DFC0, DFC1, DFC2, DFC3, DFC4, DFC5, DFC6, DFC7, SERDAT, CTS, DSR, RXI, TXI

Functional Descriptions

Inputs:

RDN	Read enable (microprocessor interface)
WRN	Write enable (microprocessor interface)
ALE	Address latch enable (microprocessor interface)
CSN	Chip select (microprocessor interface)
HWRESET	Power-up reset
CLK1	Clock
SERDATIN	Serial receive data
RTS	Request to send
DTR	Data terminal ready

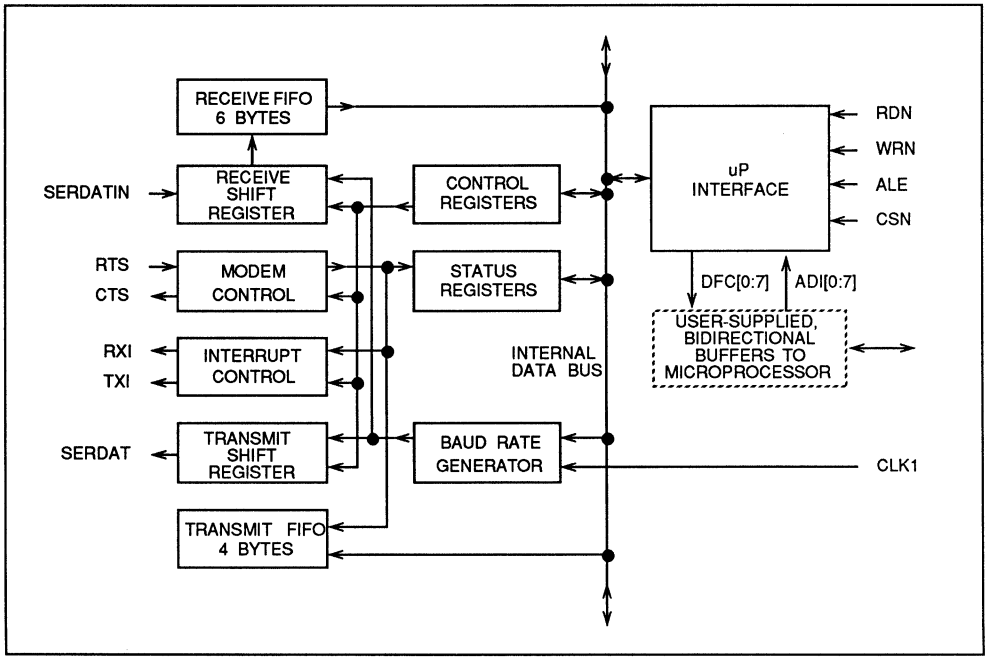
Outputs:

SERDAT	Serial transmit data
CTS	Clear to send
DSR	Data set ready
RXI	Receive interrupt
TXI	Transmit interrupt
REGREAD(N)	3-state control signals for user-supplied, bidirectional buffers

Bidirectionals:

ADI[0:7],DFC[0:7]	Address and data bus (microprocessor interface)

Block Diagram



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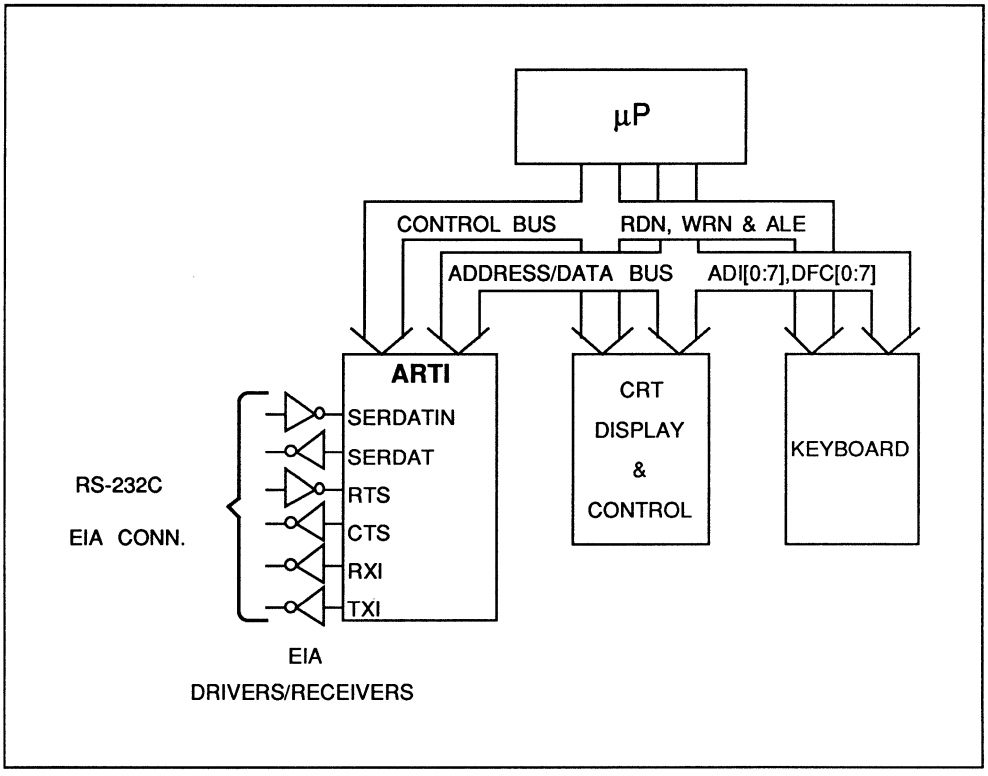
Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
ALE	DFC[0:7]↑	19.43	3.24	9.43	0.66
ALE	DFC[0:7]↓	11.49	4.10	6.46	1.07
CLK1	DFC[0:7]↑	35.37	3.24	15.54	0.66
CLK1	DFC[0:7]↓	31.77	4.10	14.46	1.07
CSN	DFC[0:7]↑	31.94	3.24	15.60	0.66
CSN	DFC[0:7]↓	31.77	4.10	15.26	1.07
RDN	DFC[0:7]↑	31.94	3.24	15.60	0.66
RDN	DFC[0:7]↓	31.77	4.10	15.26	1.07

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum ADI[0:7] Setup before ALE	1.31	0.80
Minimum ADI[0:7] Setup before CSN	1.31	0.80
Minimum CLK1 Setup before CSN	7.14	2.63

Application Notes



Bit-Slice Microprocessor BL29C01

2593 grids, 3230 transistors

Functional Description and Features

The BL29C01 is the functional equivalent of AMD's 2901 four-bit microprocessor slice. AMD describes the 2901 as follows: "The 2901 is a high-speed, cascadable ALU intended for use in CPUs, peripheral controllers, and programmable microprocessors. The microinstruction flexibility of the 2901 permits efficient emulation of almost any digital computing machine."

The device, as shown in the block diagram, consists of a 16-word by 4-bit-per-word dual-port RAM, an eight function ALU, and associated shifting, decoding, and multiplexing circuitry. The 9-bit microinstruction word is organized into three groups of three bits each that select the ALU source operands, the ALU function, and the ALU destination register. The 2901 is cascadable with full look-ahead or with ripple carry, has 3-state outputs, and provides various status flag outputs from the ALU.

Terminal Descriptions

Netlist Order

INPUTS: I8, I7, I6, I5, I4, I3, I2, I1, I0, A3, A2, A1, A0, B3, B2, B1, B0, D3, D2, D1, D0, RAM0I, RAM3I, Q0I, Q3I, CN, CP, OEN

OUTPUTS: Y3, Y2, Y1, Y0, GN, PN, OVR, FEQ0, F3, CN4, RAM0O, RAM3O, Q0O, Q3O

Functional Descriptions

Inputs:

I[8:0]	The nine instruction control lines. Used to determine what data sources will be applied to the ALU (I[0:2]), what function the ALU will perform (I[3:5]), and what data is to be deposited in the Q-register or the register stack (I[6:8]).
A[3:0]	The four address inputs to the register stack used to select one register whose contents are displayed through the A port.
B[3:0]	The four address inputs to the register stack used to select one register whose contents are displayed through the B port and into which new data can be written when the clock goes low.
D[3:0]	Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the device.
CN	The carry-in to the internal ALU.
CP	The clock input.
OEN	Output enable, active-low.

Outputs:

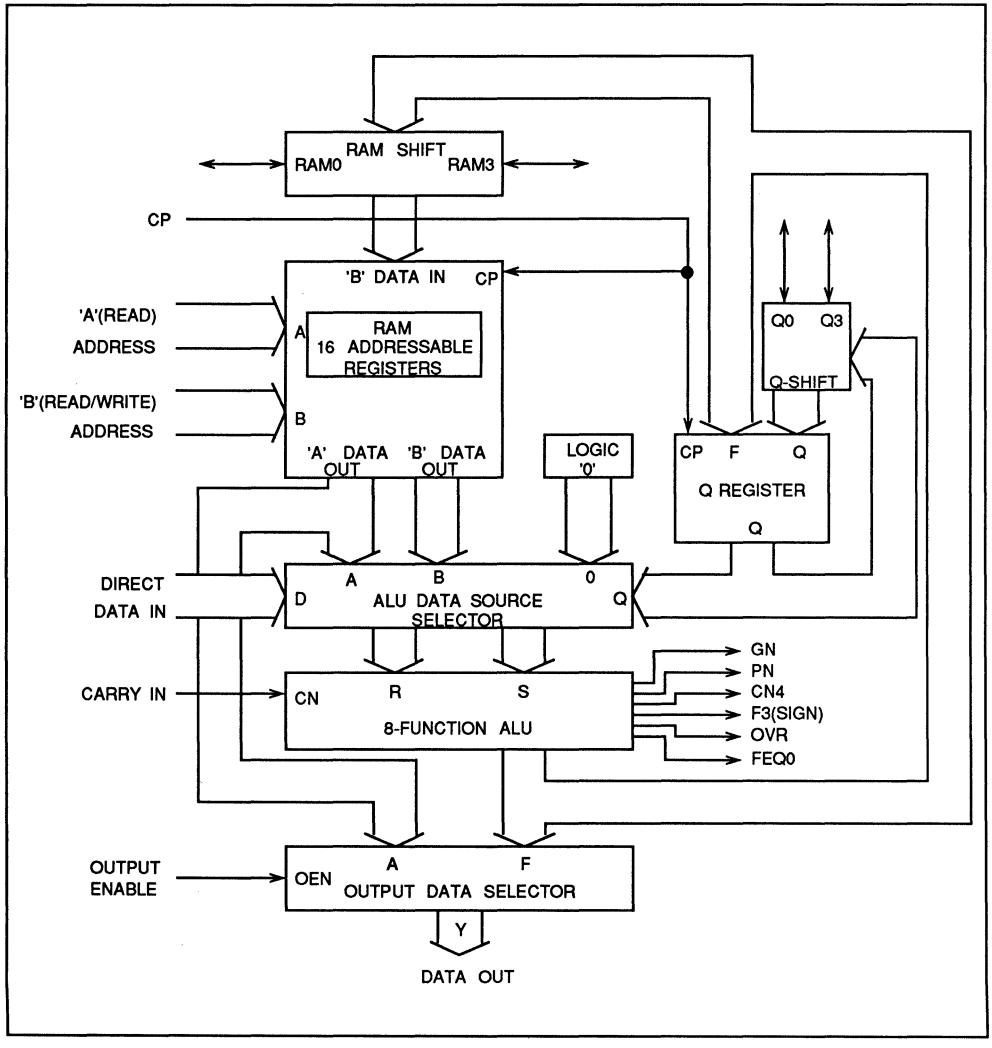
Y[3:0]	The four data outputs. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack.
GN	The carry-generate output of the internal ALU.
PN	The carry-propagate output of the internal ALU.
OVR	Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU.
FEQ0	Indicates the result of an ALU operation is zero.
F3	The most significant ALU bit.
CN4	The carry-out of the internal ALU.

Functional Descriptions (continued)

Bidirectionals:

RAM0	A shift line at the LSB of the register stack.
RAM3	A shift line at the MSB of the register stack.
Q0	A shift line at the LSB of the Q register.
Q3	A shift line at the MSB of the Q register.

Block Diagram



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Characteristics

AREA-OPTIMIZED SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing								
	Intrinsic Delay To Output (ns)							
From Input	Y[0:3]	F3	CN4	GN,PN	FEQ0	OVR	RAM[0,3]O	Q[0,3]O
CN	25.14	21.37	7.54	-	23.37	12.69	23.60	-
CP↑	42.74	38.97	26.29	26.00	40.97	30.29	41.20	1.66
D[0:3]	38.29	34.51	21.94	21.66	36.51	25.83	36.74	-
I[0:2]	43.94	40.17	27.60	27.31	42.17	31.49	42.40	-
I[3:5]	45.20	41.43	27.31	28.57	43.43	32.74	43.66	-
I[6:8]	10.57	-	-	-	-	-	10.46	10.46
Extrinsic (ns/pF)	3.24	7.86	7.86	7.86	12.88	7.86	3.24	3.24

PERFORMANCE-OPTIMIZED SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing								
	Intrinsic Delay To Output (ns)							
From Input	Y[0:3]	F3	CN4	GN,PN	FEQ0	OVR	RAM[0,3]O	Q[0,3]O
CN	10.34	8.69	2.86	-	9.83	5.20	9.71	-
CP↑	19.20	17.54	12.34	12.29	18.69	14.06	18.57	1.66
D[0:3]	15.89	14.23	8.91	8.86	15.37	10.74	15.26	-
I[0:2]	17.94	16.29	10.97	10.91	17.43	12.80	17.31	-
I[3:5]	18.23	16.57	11.49	11.20	17.71	13.09	17.60	-
I[6:8]	4.11	-	-	-	-	-	3.54	3.54
Extrinsic (ns/pF)	0.70	2.10	2.10	2.10	2.75	2.10	0.70	0.70

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum A[0:3],B[0:3] Setup before CP	21.43	9.43
Minimum CN Setup before CP↑	27.03	11.26
Minimum D[0:3] Setup before CP↑	40.17	16.80
Minimum I[0:2] Setup before CP↑	45.83	18.86
Minimum I[3:5] Setup before CP↑	47.09	19.14
Minimum I[6:8] Setup before CP↓	13.03	5.26
Minimum Q[0,3]I Setup before CP↑	3.66	1.94
Minimum RAM[0,3]I Setup before CP↑	4.40	1.89

Microprogram Sequencer BL29C09

733 grids, 1016 transistors

Functional Description and Features

The BL29C09 is the functional equivalent of AMD's 2909 microprogram sequencer. The 2909 is a 4-bit-wide address controller intended for sequencing through a series of microinstructions contained in a ROM. Two or more 2909's can be connected to form eight-bit or larger addresses.

The device can be used to select an address from any of four sources. They are:

- A set of external inputs(D)
- External data from the R inputs, stored in an internal register
- A four-word-deep push/pop stack
- A program counter register which usually contains the last address plus one.

The push/pop stack includes control lines that enable it to efficiently execute nested subroutine linkages. Each of the four outputs can be OR'ed with an external input for conditional skip or branch instructions, and a separate line forces all of the outputs to 0. The outputs are 3-statable.

Terminal Descriptions

Netlist Order

INPUTS: CK, R0, R1, R2, R3, REB, D0, D1, D2, D3, S0, S1, OR0, OR1, OR2, OR3, ZEROB, OEB, CN, FEB, PUP

OUTPUTS: Y0, Y1, Y2, Y3, CN4

Functional Descriptions

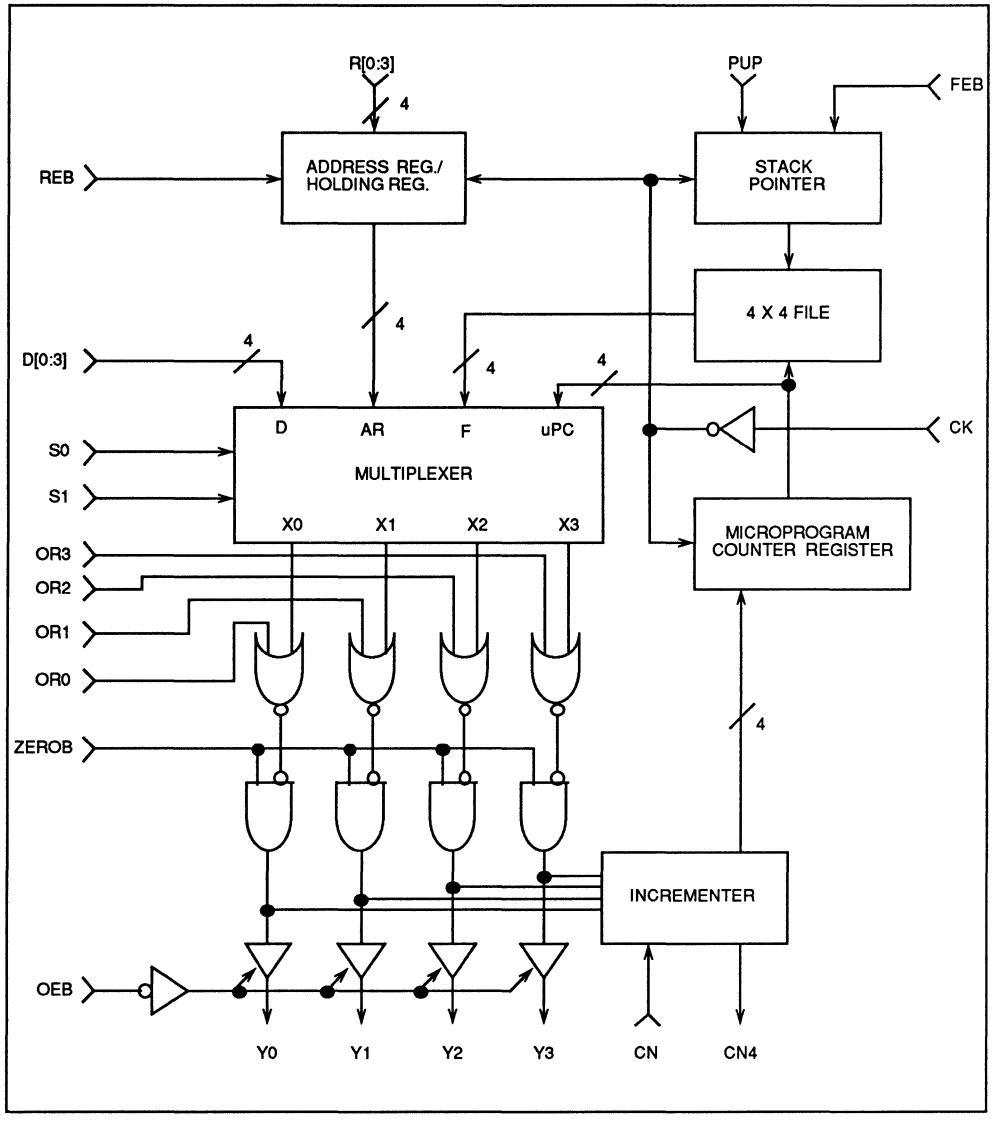
Inputs:

CK	Clock
R[0:3]	Inputs to the internal address register
REB	Enable line for internal address register, active-low
D[0:3]	Direct inputs to the multiplexer
S[0:1]	Control lines for address source selection
OR[0:3]	Logic OR inputs on each address output line
ZEROB	Logic AND input on the output lines, active-low
OEB	Output enable, active-low
CN	Carry-in to the incrementer
FEB	Control line for the push/pop stack, active-low
PUP	Control line for the push/pop stack

Outputs:

Y[0:3]	Address outputs
CN4	Carry-out from the incrementer

BLOCK DIAGRAM



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
CK↑	CN4↑	15.66	3.24	7.20	0.70
CK↑	CN4↓	11.94	2.31	6.00	0.58
CK↑	Y[0:3]↑	11.60	3.24	5.89	0.70
CK↑	Y[0:3]↓	9.43	2.31	5.20	0.58
D[0:3]	CN4↑	11.71	3.24	4.57	0.70
D[0:3]	CN4↓	9.03	2.31	3.77	0.58
D[0:3]	Y[0:3]↑	8.63	3.24	3.26	0.70
D[0:3]	Y[0:3]↓	6.91	2.31	2.97	0.58
OEB	Y[0:3]↑	2.29	3.24	0.69	0.70
OEB	Y[0:3]↓	2.29	2.31	0.63	0.58
OR[0:3]	CN4↑	9.89	3.24	3.77	0.70
OR[0:3]	CN4↓	6.63	2.31	2.69	0.58
OR[0:3]	Y[0:3]↑	6.80	3.24	2.46	0.70
OR[0:3]	Y[0:3]↓	4.51	2.31	1.89	0.58
S[0:1]	CN4↑	17.26	3.24	6.75	0.70
S[0:1]	CN4↓	12.34	2.31	5.09	0.58
S[0:1]	Y[0:3]↑	14.17	3.24	5.26	0.70
S[0:1]	Y[0:3]↓	10.23	2.31	4.29	0.58
ZEROB	CN4↑	10.11	3.24	3.89	0.70
ZEROB	CN4↓	6.46	2.31	2.51	0.58
ZEROB	Y[0:3]↑	7.03	3.24	2.57	0.70
ZEROB	Y[0:3]↓	4.34	2.31	1.71	0.58

Characteristics (continued)

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CN Setup before CK↑	4.06	2.40
Minimum D[0:3] Setup before CK↑	12.40	5.49
Minimum FEB Setup before CK↑	4.06	2.11
Minimum OR[0:3] Setup before CK↑	9.54	4.69
Minimum PUP Setup before CK↑	7.66	3.37
Minimum R[0:3] Setup before CK↑	2.00	1.26
Minimum REB Setup before CK↑	3.03	1.71
Minimum S[0:1] Setup before CK↑	17.94	7.49
Minimum ZEROB Setup before CK↑	10.80	4.80

4-Phase Clock Generator — CKGEN

128 grids, 218 transistors

Functional Description and Features

The CKGEN is a 4-phase, non-overlapping clock generator. It is designed for logic verification and not meant to drive large capacitive loads.

- NAND NOR implementation
- Minimum built-in non-overlap

Terminal Descriptions

Netlist Order

INPUTS: CKI

OUTPUTS: MCK, SCK, MCKN, SCKN

Functional Descriptions

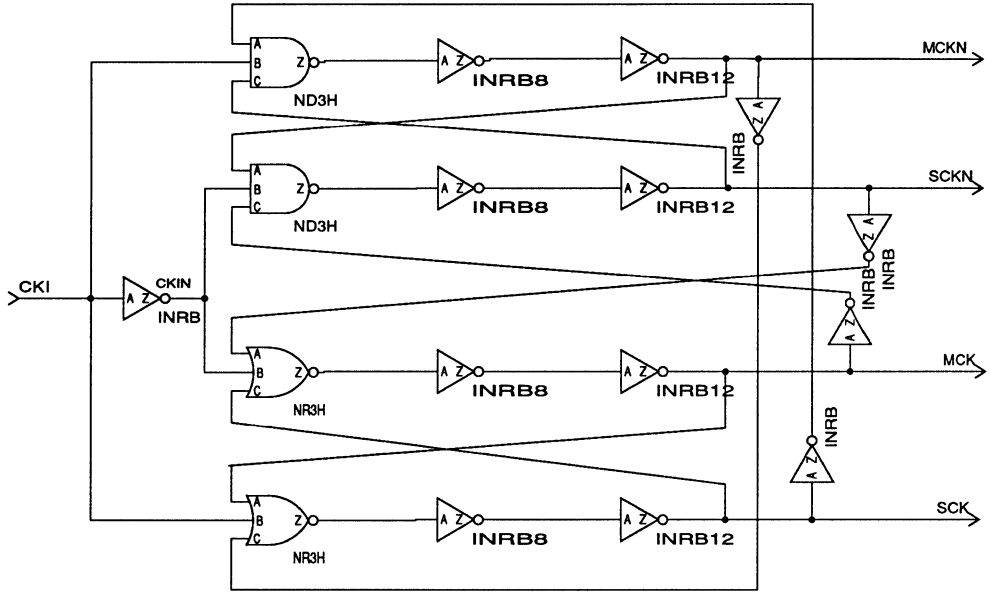
Inputs:

CKI	Input clock

Outputs:

MCK	Master clock
SCK	Slave clock
MCKN	Complement of MCK
SCKN	Complement of SCK

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
CKI↑	MCK↑	9.60	0.33	5.40	0.08
CKI↓	MCK↓	4.80	0.40	2.60	0.08
CKI↓	SCK↑	9.70	0.33	5.50	0.08
CKI↑	SCK↓	1.60	0.40	1.10	0.08
CKI↓	MCKN↑	2.20	0.33	1.30	0.08
CKI↑	MCKN↓	7.20	0.40	4.50	0.08
CKI↑	SCKN↑	3.90	0.33	2.20	0.08
CKI↓	SCKN↓	9.80	0.40	5.60	0.08

BCD-to-Decimal Decoder CM42

58 grids, 80 transistors

Functional Description and Features

The CM42 is functionally equivalent to the 7442 4-Line-TO-10-Line, BCD-to-Decimal Decoder within the standard 74XX Series logic families of devices.

Terminal Descriptions

Netlist Order

INPUTS: A, B, C, D

OUTPUTS: Z0, Z1, Z2, Z3, Z4, Z5, Z6, Z7, Z8, Z9

Functional Descriptions

Inputs:

A, B, C, D	BCD inputs

Outputs:

Z[0:9]	Decimal output

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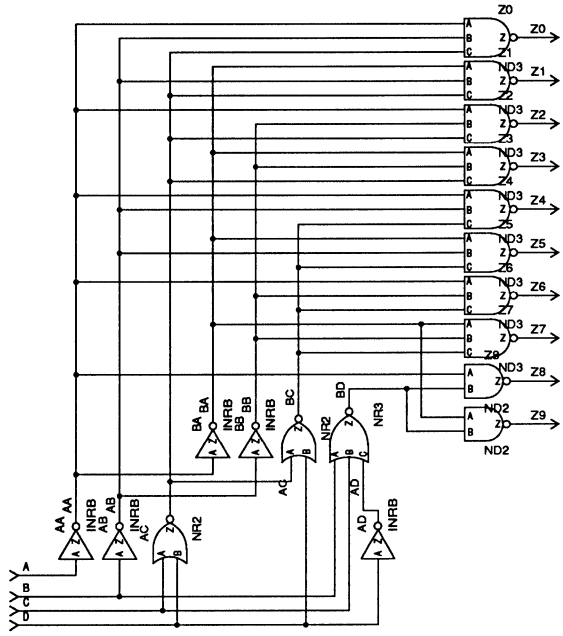
Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
A,B,C,D	Z[0:9]↑	8.23	3.24	2.91	0.70
A,B,C,D	Z[0:9]↓	6.11	5.95	2.46	1.56

11

2-Bit, Binary Full Adder — CM82

48 grids, 68 transistors

Functional Description and Features

The CM82 is functionally equivalent to the 7482 2-Bit, Binary FULL ADDER within the standard 74XX Series logic families of devices.

Terminal Descriptions

Netlist Order

INPUTS: C0, A0, B0, A1, B1

OUTPUTS: S0, S1, C2

Functional Descriptions

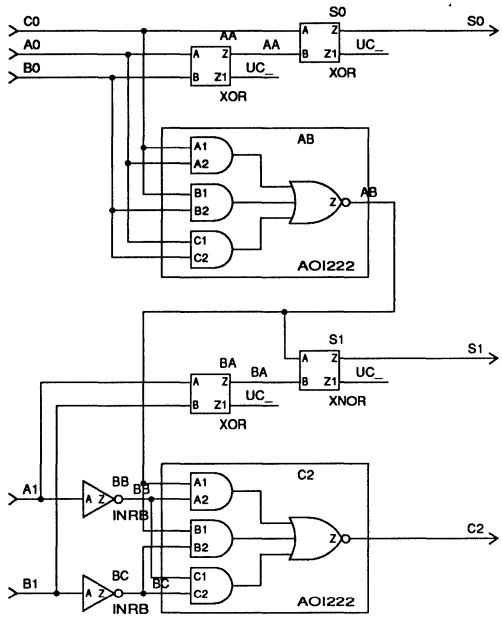
Inputs:

C0	Carry input
A[0:1], B[0:1]	Data input

Outputs:

S[0:1]	Sum output
C2	Carry output

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
A0,B0	C2↑	2.69	9.71	1.43	2.05
A0,B0	C2↓	5.43	4.03	2.34	1.03
A0,B0	S[0:1]↑	5.94	8.98	2.57	2.05
A0,B0	S[0:1]↓	5.37	12.68	2.23	2.71
A1,B1	C2↑	1.14	9.71	0.57	2.05
A1,B1	C2↓	1.49	4.03	0.69	1.03
A1,B1	S1↑	2.11	8.26	1.20	2.05
A1,B1	S1↓	1.77	9.45	0.97	2.18
C0	C2↑	2.69	9.71	1.43	2.05
C0	C2↓	5.43	4.03	2.34	1.03
C0	S[0:1]↑	5.94	8.98	2.57	2.05
C0	S[0:1]↓	5.37	12.68	2.23	2.71

4-Bit Magnitude Comparator CM85

104 grids, 144 transistors

Functional Description and Features

The CM85 is functionally equivalent to the 7485 4-Bit Magnitude Comparator within the standard 74XX Series logic families of devices.

Terminal Descriptions

Netlist Order

INPUTS: ALBI, AEBI, AGBI, A3, B3, A2, B2, A1, B1, A0, B0

OUTPUTS: ALBO, AEBO, AGBO

Functional Descriptions

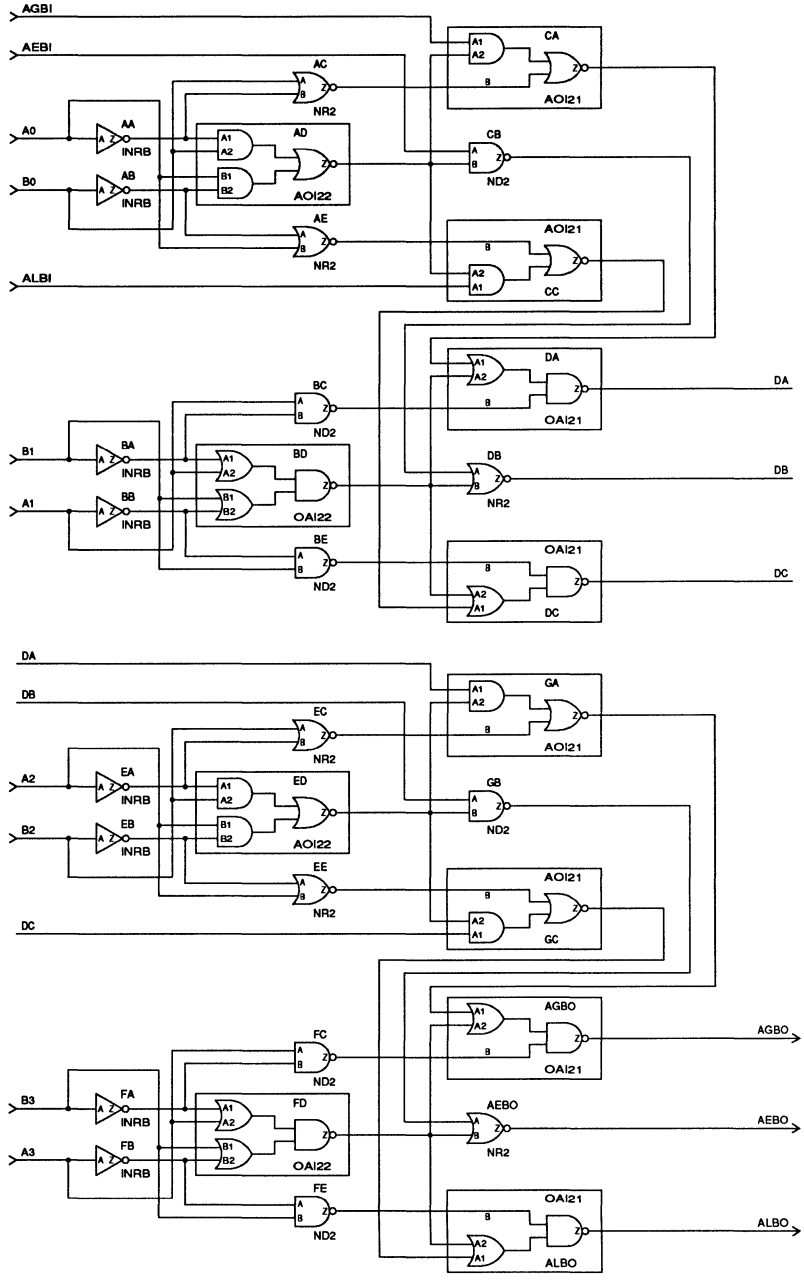
Inputs:

A[L,E,G]BI	Cascading inputs
A[3:0], B[3:0]	Data inputs

Outputs:

ALBO	A less than B output
AEBO	A equal to B output
AGBO	A greater than B output

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
A[0:3],B[0:3]	AEBO↑	7.83	6.47	3.03	1.36
A[0:3],B[0:3]	AEBO↓	5.77	2.31	2.29	0.58
A[0:3],B[0:3]	ALBO,AGBO↑	7.77	6.47	3.14	1.36
A[0:3],B[0:3]	ALBO,AGBO↓	7.60	4.03	3.20	1.07
AEBI	AEBO↑	3.26	6.47	1.31	1.36
AEBI	AEBO↓	2.06	2.31	0.74	0.58
AGBI	AGBO↑	3.26	6.47	1.43	1.36
AGBI	AGBO↓	3.83	4.03	1.66	1.07
ALBI	ALBO↑	3.26	6.47	1.43	1.36
ALBI	ALBO↓	3.83	4.03	1.66	1.07

3-to-8-Line Decoder/Demultiplexer CM138

56 grids, 82 transistors

Functional Description and Features

The CM138 is functionally equivalent to the 74138 3-to-8-Line Decoder/Demultiplexer within the standard 74XX Series logic families of devices.

Terminal Descriptions

Netlist Order

INPUTS: A, B, C, G1, G2A, G2B

OUTPUTS: Z0, Z1, Z2, Z3, Z4, Z5, Z6, Z7

Functional Descriptions

Inputs:

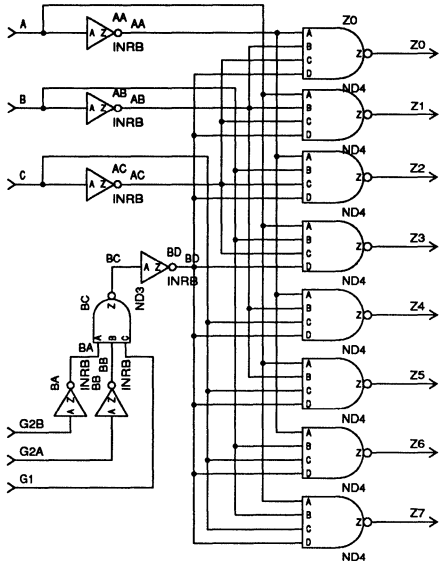
A, B, C,	Select inputs
G1, G2[A,B]	Enable inputs

Outputs:

Z[0:7]	Data outputs

11

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
A,B,C	Z[0:7]↑	1.31	3.24	0.63	0.70
A,B,C	Z[0:7]↓	2.63	7.86	1.09	2.10
G1,G2A,G2B	Z[0:7]↑	4.11	3.24	1.77	0.70
G1,G2A,G2B	Z[0:7]↓	6.86	7.86	2.80	2.10

11

1-of-16 Gated Data Select/Multiplexer CM150

88 grids, 134 transistors

Functional Description and Features

The CM150 is functionally equivalent to the 74150 1-of-16 Gated Data Select/Multiplexer within the standard 74XX Series logic families of devices.

Terminal Descriptions

Netlist Order

INPUTS: D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, A, B, C, D, SN

OUTPUTS: Z

Functional Descriptions

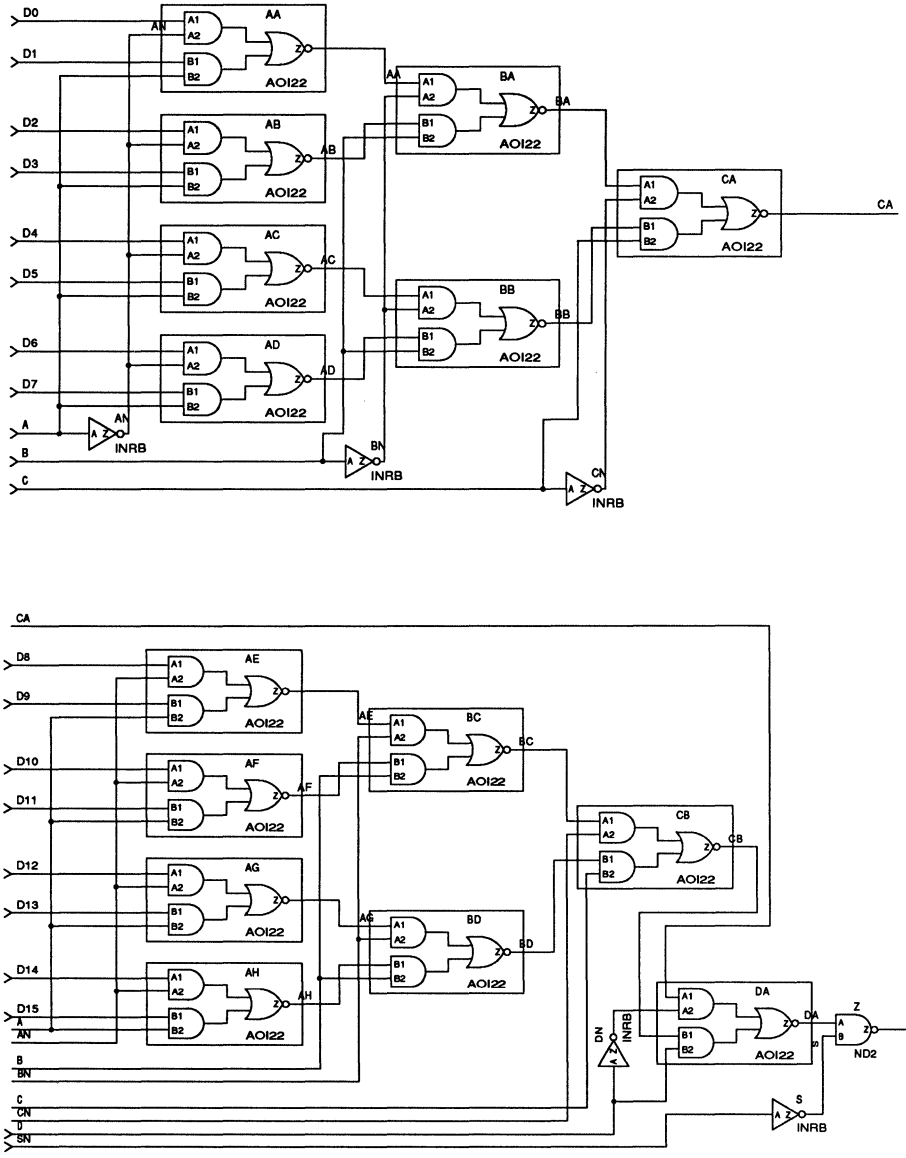
Inputs:

D[0:15]	Data inputs
A, B, C, D	Data-select inputs
SN	Strobe input, active-low

Outputs:

Z	Inverted data output

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
A,B,C,D	Z↑	7.66	3.24	3.31	0.66
A,B,C,D	Z↓	9.60	4.10	3.66	1.07
D[0:15]	Z↑	5.03	3.24	2.17	0.66
D[0:15]	Z↓	4.80	4.10	2.00	1.07
SN	Z↑	0.40	3.24	0.17	0.66
SN	Z↓	0.74	4.10	0.29	1.07

1-of-8 Gated Data Select/Multiplexer CM151

46 grids, 68 transistors

Functional Description and Features

The CM151 is functionally equivalent to the 74151 1-of-8 Gated Data Select/Multiplexer within the standard 74XX Series logic families of devices.

Terminal Descriptions

Netlist Order

INPUTS: D0, D1, D2, D3, D4, D5, D6, D7, A, B, C, SN

OUTPUTS: Y, W

Functional Descriptions

Inputs:

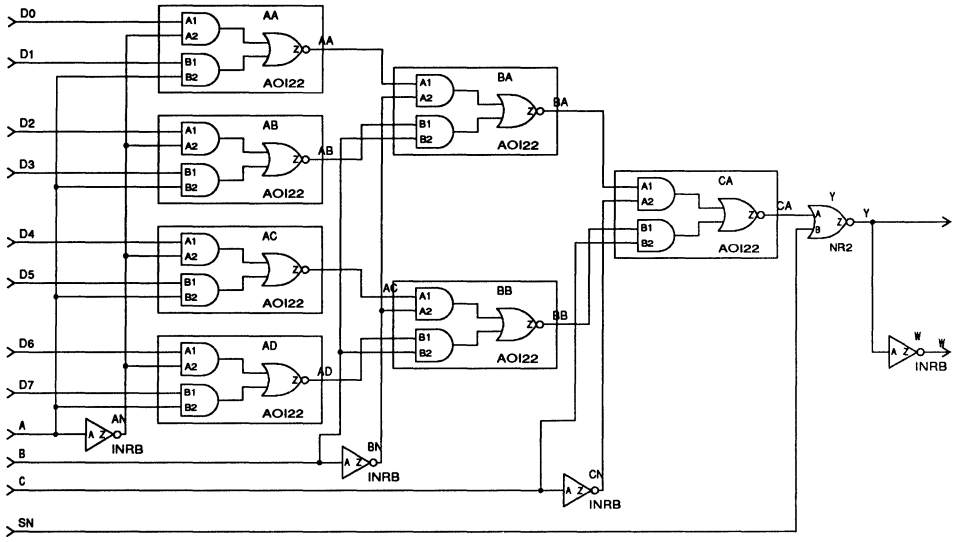
D[0:7]	Data inputs
A, B, C	Data-select inputs
SN	Strobe input, active-low

Outputs:

W	Inverted output
Y	Output

11

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
A,B,C	Y↑	6.91	6.47	2.80	1.36
A,B,C	Y↓	5.94	2.31	2.40	0.58
A,B,C	W↑	6.06	3.24	2.46	0.70
A,B,C	W↓	7.31	2.31	2.97	0.58
D[0:7]	Y↑	4.17	6.47	1.83	1.36
D[0:7]	Y↓	4.57	2.31	1.77	0.58
D[0:7]	W↑	4.69	3.24	1.83	0.70
D[0:7]	W↓	4.57	2.31	2.00	0.58
SN	Y↑	0.86	6.47	0.34	1.36
SN	Y↓	0.29	2.31	0.11	0.58
SN	W↑	0.40	3.24	0.17	0.70
SN	W↓	1.26	2.31	0.51	0.58

1-of-8 Data Select/Multiplexer CM152

41 grids, 62 transistors

Functional Description and Features

The CM152 is functionally equivalent to the 74152 1-of-8 Data Select/Multiplexer within the standard 74XX Series logic families of devices.

Terminal Descriptions

Netlist Order

INPUTS: D0, D1, D2, D3, D4, D5, D6, D7, A, B, C

OUTPUTS: Z

Functional Descriptions

Inputs:

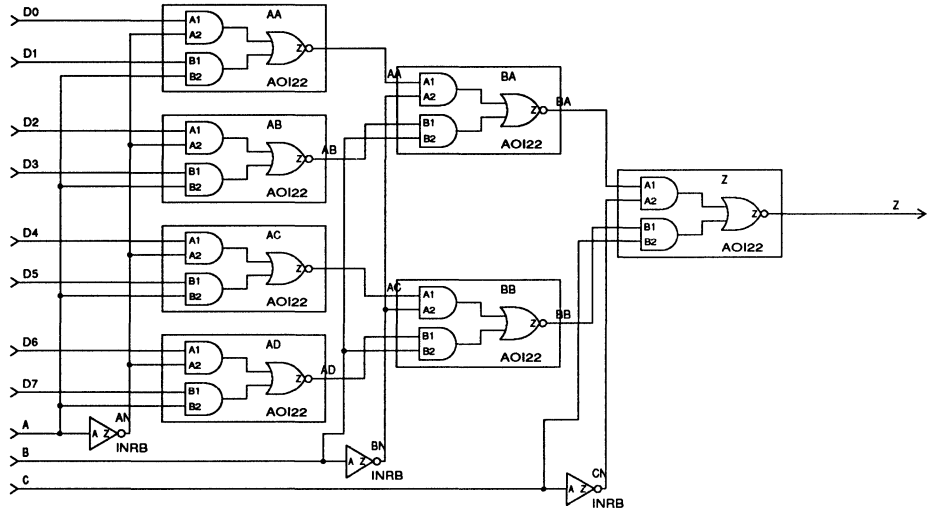
D[0:7]	Data inputs
A, B, C	Select inputs

Outputs:

Z	Inverted output

11

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
A,B,C	Z↑	4.11	6.41	1.77	1.40
A,B,C	Z↓	5.03	4.10	2.06	1.07
D[0:7]	Z↑	2.74	6.41	1.14	1.40
D[0:7]	Z↓	2.29	4.10	1.09	1.07

11

4-Line-to-1 Data Select/Multiplexer CM153X

24 grids, 34 transistors

Functional Description and Features

The CM153X is functionally equivalent to one-half of the 74153 Dual, 4-Line-to-1-Line Data Select/Multiplexer within the standard 74XX Series logic families of devices.

Terminal Descriptions

Netlist Order

INPUTS: 1GN, 1D0, 1D1, 1D2, 1D3, A, B

OUTPUTS: 1Z

Functional Descriptions

Inputs:

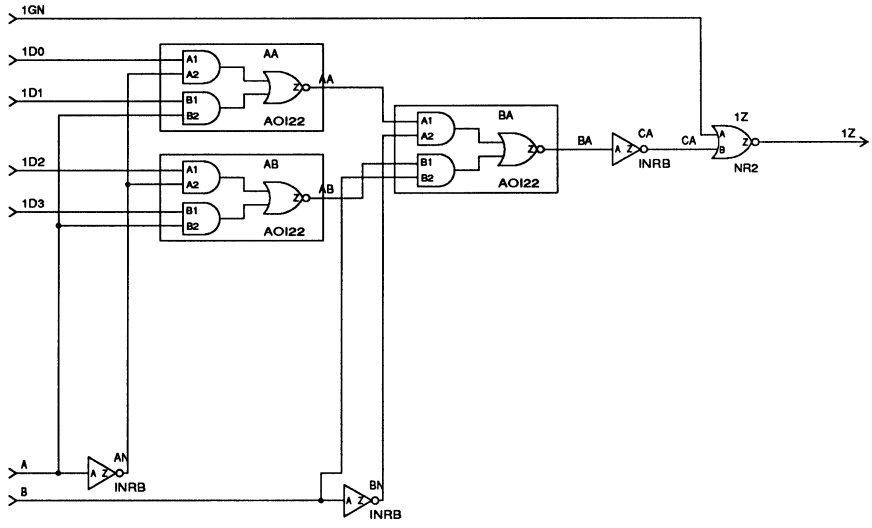
1GN	Strobe input, active-low
1D[0:3]	Data inputs
A, B	Select inputs

Outputs:

1Z	Data output

11

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
1D[0:3]	1Z↑	3.03	6.47	1.26	1.36
1D[0:3]	1Z↓	3.26	2.31	1.31	0.58
1GN	1Z↑	0.23	6.47	0.17	1.36
1GN	1Z↓	0.92	2.31	0.29	0.58
A,B	1Z↑	4.57	6.47	1.83	1.36
A,B	1Z↓	4.00	2.31	1.66	0.58

2-Line-to-1-Line Data Select/Multiplexer CM157X

10 grids, 14 transistors

Functional Description and Features

The CM157X is functionally equivalent to one-fourth of the 74157 Quadruple, 2-Line-to-1-Line Data Select/Multiplexer within the standard 74XX Series logic families of devices.

Terminal Descriptions

Netlist Order

INPUTS: A1, B1, S, GN

OUTPUTS: Z1

Functional Descriptions

Inputs:

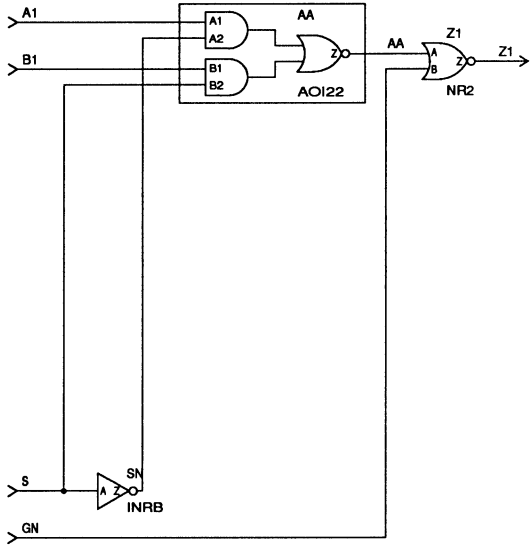
A1, B1	Data inputs
S	Select input
GN	Strobe input, active-low

Outputs:

Z1	Data output

11

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
A1,B1	Z1↑	0.97	6.47	0.46	1.36
A1,B1	Z1↓	1.31	2.31	0.57	0.58
GN	Z1↑	0.23	6.47	0.17	1.36
GN	Z1↓	0.92	2.31	0.29	0.58
S	Z1↑	1.83	6.47	0.80	1.36
S	Z1↓	1.71	2.31	0.80	0.58

2-Line-to-1-Line Data Select/Multiplexer CM158X

13 grids, 18 transistors

Functional Description and Features

The CM158X is functionally equivalent to one-fourth of the 74158 Quadruple, 2-Line-to-1-Line, Inverting Data Select/Multiplexer within the standard 74XX Series logic families of devices.

Terminal Descriptions

Netlist Order

INPUTS: A1, B1, GN, S

OUTPUTS: Z1

Functional Descriptions

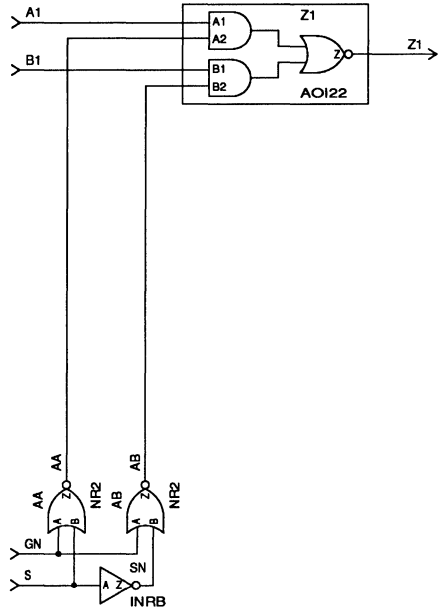
Inputs:

A1, B1	Data inputs
GN	Strobe input, active-low
S	Select input

Outputs:

Z1	Inverted data output

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
A1,B1	Z1↑	0.23	6.41	0.11	1.40
A1,B1	Z1↓	0.11	4.10	0.11	1.07
GN	Z1↑	0.63	6.41	0.34	1.40
GN	Z1↓	1.49	4.10	0.63	1.07
S	Z1↑	1.49	6.41	0.63	1.40
S	Z1↓	1.83	4.10	0.80	1.07

Synchronous, 4-Bit Decade Counter CM160

150 grids, 216 transistors

Functional Description and Features

The CM160 is functionally equivalent to the 74160 Synchronous, 4-Bit Decade Counter with Asynchronous CLEAR within the standard 74XX Series logic families of devices.

Terminal Descriptions

Netlist Order

INPUTS: A, B, P, L, T, CK, CD, C, D

OUTPUTS: QA, QAN, QB, QBN, QC, QCN, QD, QDN, CO

Functional Descriptions

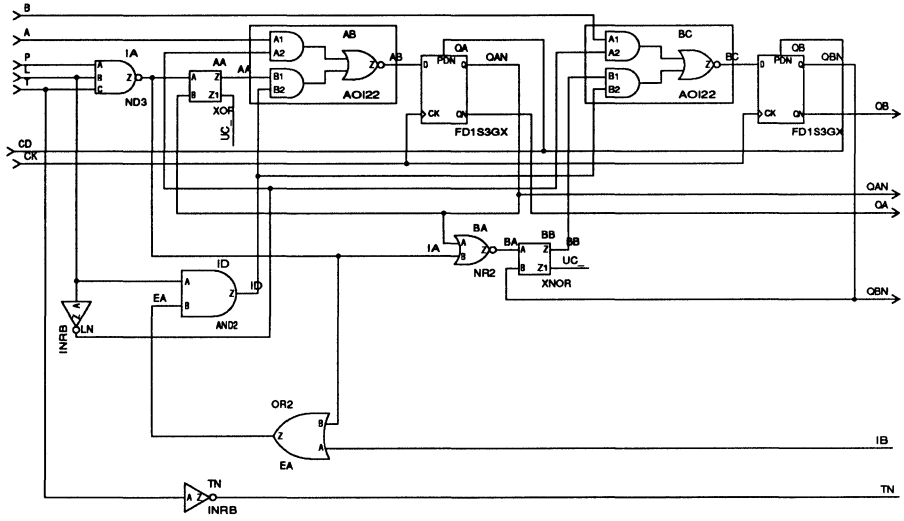
Inputs:

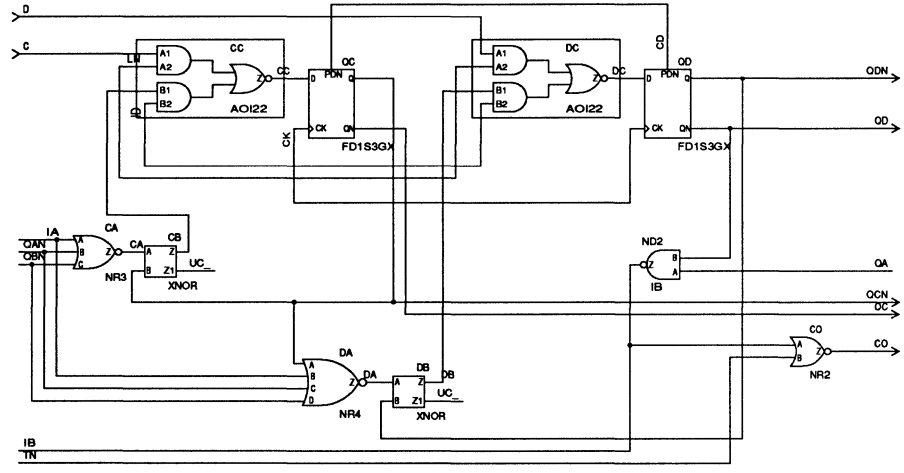
A, B, C, D	Data inputs
P, T	Enable inputs
L	Load input, active-low
CK	Clock input
CD	Asynchronous clear input, active-low

Outputs:

Q[A,B,C,D]	Data outputs
Q[A,B,C,D]N	Complimentary data outputs
CO	Carry output

Detailed Schematic





11

Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
CD↓	ANY Q↓	2.10	3.24	1.60	0.21
CD↓	ANY QN↑	3.40	7.99	1.30	0.73
CK↑	ANY Q↑	1.20	5.68	1.20	1.24
CK↑	ANY Q↓	1.03	9.38	1.37	1.02
CK↑	CO↑	3.37	6.47	2.69	1.36
CK↑	CO↓	2.46	2.31	2.23	0.58
T	CO↑	0.51	6.47	0.23	1.36
T	CO↓	0.69	2.31	0.29	0.58

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum A,B,C,D Setup before CK↑	2.34	1.31
Minimum L Setup before CK↑	12.06	5.94
Minimum P Setup before CK↑	12.06	5.94
Minimum T Setup before CK↑	12.06	5.94

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Synchronous, 4-Bit Binary Counter CM161

143 grids, 206 transistors

Functional Description and Features

The CM161 is functionally equivalent to the 74161 Synchronous, 4-Bit Binary Counter with Asynchronous CLEAR within the standard 74XX Series logic families of devices.

Terminal Descriptions

Netlist Order

INPUTS: A, B, P, T, CK, CD, L, C, D

OUTPUTS: QA, QAN, QB, QBN, QC, QCN, QD, QDN, CO

Functional Descriptions

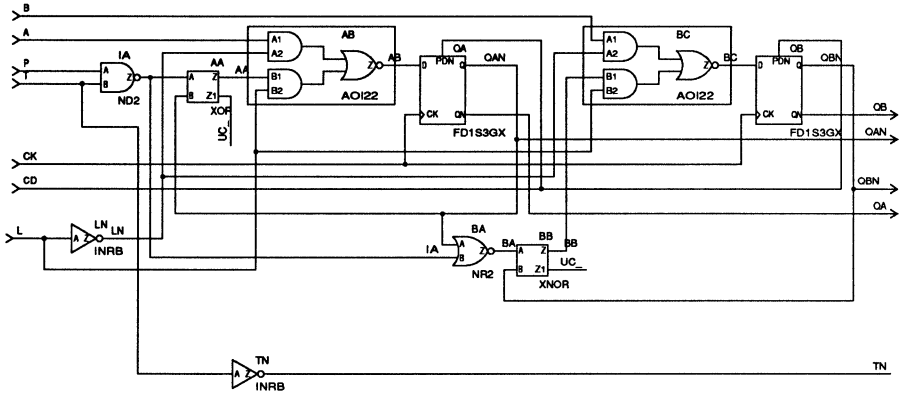
Inputs:

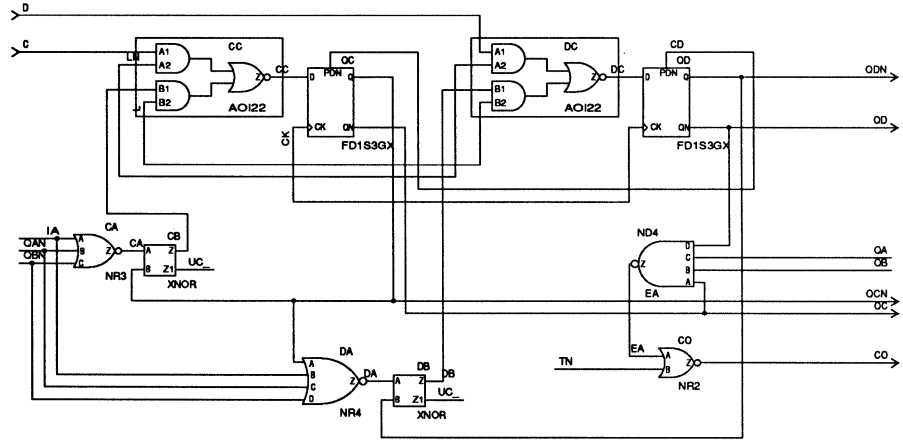
A, B, C, D	Data inputs
P, T	Enable inputs
CK	Clock input
CD	Asynchronous clear input, active-low
L	Load input, active-low

Outputs:

Q[A,B,C,D]	Data outputs
Q[A,B,C,D]N	Complimentary data outputs
CO	Carry output

Detailed Schematic





Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
CD↓	ANY Q↓	2.10	3.24	1.60	0.21
CD↓	ANY QN↑	3.40	7.99	1.30	0.73
CK↑	ANY Q↑	1.20	5.68	1.20	1.24
CK↑	ANY Q↓	1.03	9.38	1.37	1.02
CK↑	CO↑	3.31	6.47	2.69	1.36
CK↑	CO↓	2.00	2.31	2.00	0.58
T	CO↑	0.46	6.47	0.23	1.36
T	CO↓	0.69	2.31	0.29	0.58

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum A,B,C,D Setup before CK↑	2.34	1.31
Minimum L Setup before CK↑	4.69	2.23
Minimum P Setup before CK↑	9.66	4.86
Minimum T Setup before CK↑	9.66	4.86

Synchronous, 4-Bit Decade Counter CM162

141 grids, 200 transistors

Functional Description and Features

The CM162 is functionally equivalent to the 74162 Synchronous, 4-Bit Decade Counter with Synchronous CLEAR within the standard 74XX Series logic families of devices.

Terminal Descriptions

Netlist Order

INPUTS: A, B, P, L, T, CK, CL, C, D

OUTPUTS: QA, QAN, QB, QBN, QC, QCN, QD, QDN, CO

Functional Descriptions

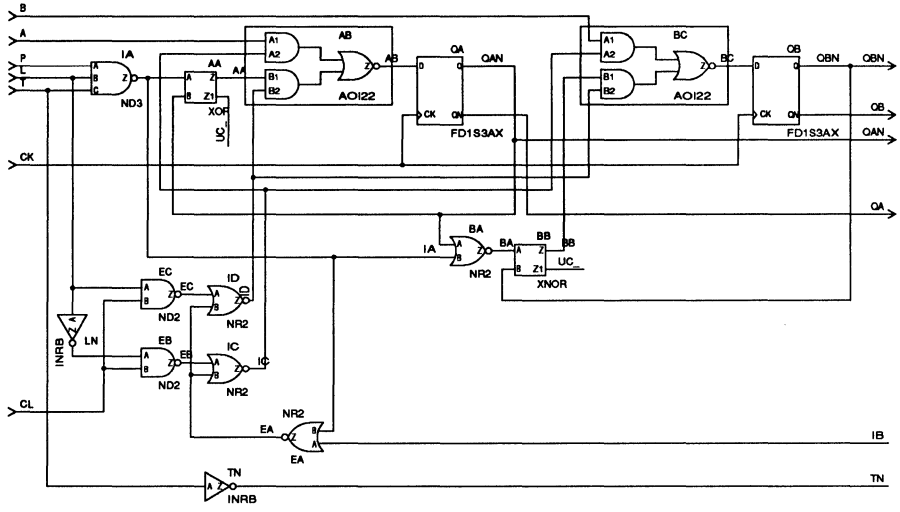
Inputs:

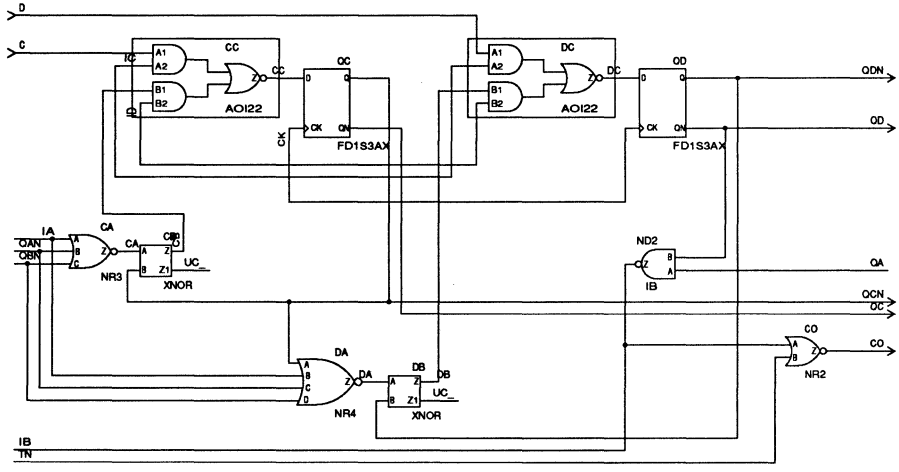
A, B, C, D	Data inputs
P, T	Enable inputs
L	Load input, active-low
CK	Clock input
CL	Synchronous clear input, active-low

Outputs:

Q[A,B,C,D]	Data outputs
Q[A,B,C,D]N	Complimentary data outputs
CO	Carry output

Detailed Schematic





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Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
CK↑	ANY Q↑	3.26	5.75	2.34	1.40
CK↑	ANY Q↓	4.00	7.93	2.29	1.73
CK↑	CO↑	5.37	6.47	3.71	1.36
CK↑	CO↓	5.43	2.31	3.09	0.58
T	CO↑	0.51	6.47	0.23	1.36
T	CO↓	0.69	2.31	0.29	0.58

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum A,B,C,D Setup before CK↑	2.23	1.09
Minimum CL Setup before CK↑	7.43	3.03
Minimum L Setup before CK↑	12.06	5.66
Minimum P Setup before CK↑	12.06	5.66
Minimum T Setup before CK↑	12.06	5.66

Synchronous, 4-Bit Binary Counter CM163

135 grids, 194 transistors

Functional Description and Features

The CM163 is functionally equivalent to the 74163 Synchronous, 4-Bit Decade Counter with Synchronous CLEAR within the standard 74XX Series logic families of devices.

Terminal Descriptions

Netlist Order

INPUTS: A, B, P, T, CK, L, CL, C, D

OUTPUTS: QA, QAN, QB, QBN, QC, QCN, QD, QDN, CO

Functional Descriptions

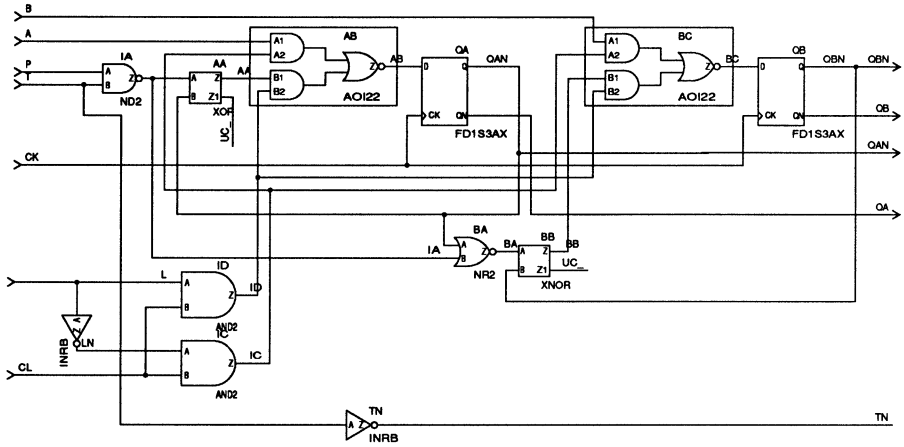
Inputs:

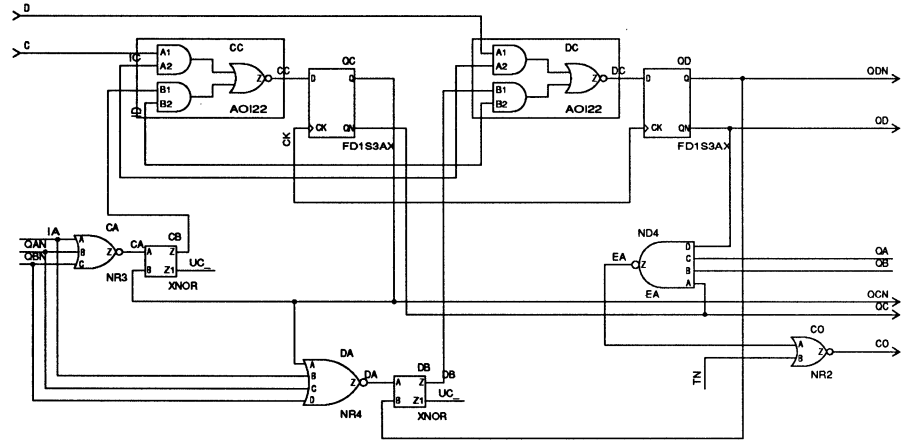
A, B, C, D	Data inputs
P, T	Enable inputs
CK	Clock input
L	Load input, active-low
CL	Synchronous clear input, active-low

Outputs:

Q[A,B,C,D]	Data outputs
Q[A,B,C,D]N	Complimentary data outputs
CO	Carry output

Detailed Schematic





Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
CK↑	ANY Q↑	3.26	5.75	2.34	1.40
CK↑	ANY Q↓	4.00	7.93	2.29	1.73
CK↑	CO↑	5.31	6.47	3.71	1.36
CK↑	CO↓	4.97	2.31	2.86	0.58
T	CO↑	0.46	6.47	0.23	1.36
T	CO↓	0.69	2.31	0.29	0.58

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum A,B,C,D Setup before CK↑	2.17	1.09
Minimum CL Setup before CK↑	4.74	2.17
Minimum L Setup before CK↑	5.49	2.46
Minimum P Setup before CK↑	9.49	4.46
Minimum T Setup before CK↑	9.49	4.46

Synchronous, 4-Bit Up/Down Counter CM169

161 grids, 228 transistors

Functional Description and Features

The CM169 is functionally equivalent to the 74169 Synchronous, 4-Bit Up/Down Counter within the standard 74XX Series logic families of devices.

Terminal Descriptions

Netlist Order

INPUTS: A, B, PN, TN, CK, UP, L, C, D

OUTPUTS: QA, QB, QC, QD, CON

Functional Descriptions

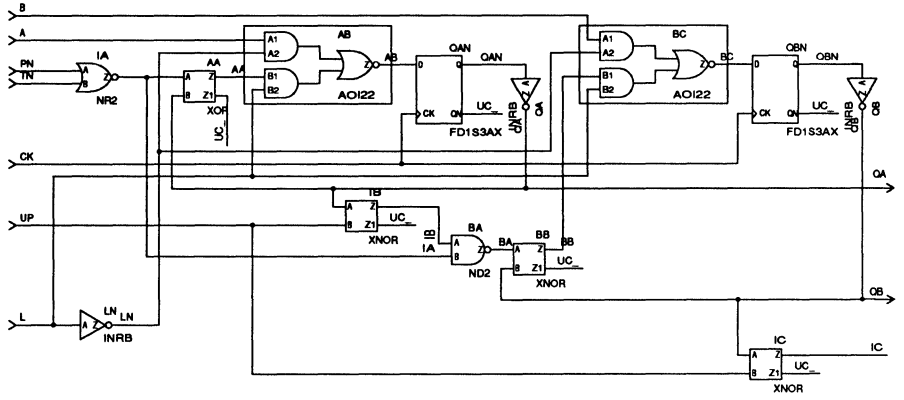
Inputs:

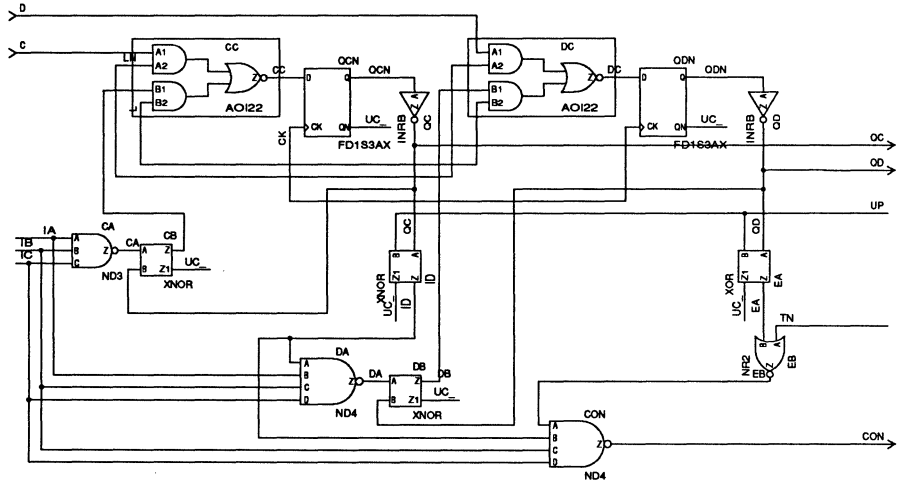
A, B, C, D	Data inputs
PN, TN	Count enable inputs, active-low
CK	Clock input
UP	Up/Down-select input
L	Load input, active-low

Outputs:

Q[A,B,C,D]	Data outputs
CON	Inverted carry output

Detailed Schematic





Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
CK↑	ANY Q↑	1.66	3.24	1.31	0.70
CK↑	ANY Q↓	2.00	2.31	1.83	0.58
CK↑	CON↑	5.14	3.24	3.20	0.70
CK↑	CON↓	6.86	7.86	3.77	2.10
TN	CON↑	0.40	3.24	0.23	0.70
TN	CON↓	1.66	7.86	0.74	2.10
UP	CON↑	2.80	3.24	1.26	0.70
UP	CON↓	4.57	7.86	1.83	2.10

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum A,B,C,D Setup before CK↑	2.17	1.09
Minimum L Setup before CK↑	4.51	1.94
Minimum PN Setup before CK↑	10.74	4.69
Minimum TN Setup before CK↑	10.74	4.69
Minimum UP Setup before CK↑	10.34	4.46

Cyclic Redundancy Checker CRC

1620 grids, 2434 transistors

Functional Description and Features

This subcircuit is used to check or generate the CCITT Cyclic Redundancy Check when connected to a parallel bus (8- or 16-bits wide). The design operates with INTEL 8051, 80186 (8 MHz) and MC68010 (10 MHz) microprocessors. The subcircuit receives asynchronous signals from the microprocessor and synchronizes them to the internal chip clock of the semi-custom circuit.

Terminal Descriptions

Netlist Order

INPUTS: CLK, READ, OVRDCSN, CSN, AD1, AD0, WORDN, QUAL, BLDATI0, BLDATI1, BLDATI2, BLDATI3, BLDATI4, BLDATI5, BLDATI6, BLDATI7, BHDATI0, BHDATI1, BHDATI2, BHDATI3, BHDATI4, BHDATI5, BHDATI6, BHDATI7

OUTPUTS: LMCRC0, LMCRC1, LMCRC2, LMCRC3, LMCRC4, LMCRC5, LMCRC6, LMCRC7, HMCRC0, HMCRC1, HMCRC2, HMCRC3, HMCRC4, HMCRC5, HMCRC6, HMCRC7, CRCCKN

Functional Descriptions

Inputs:

CLK	Clock
READ	Read/$\overline{\text{Write}}$
OVRDCSN	Override chip select (active-low)
CSN	Chip select (active-low)
AD[1:0]	Address leads
WORDN	Byte/ $\overline{\text{Word}}$ Mode
QUAL	Qualifier
BLDATI[0:7]	Lower-order data bus
BHDATI[0:7]	Higher-order data bus

Outputs:

LMCRC[0:7]	Lower-order data bus
HMCRC[0:7]	Higher-order data bus
CRCCKN	CRC check (active-low)

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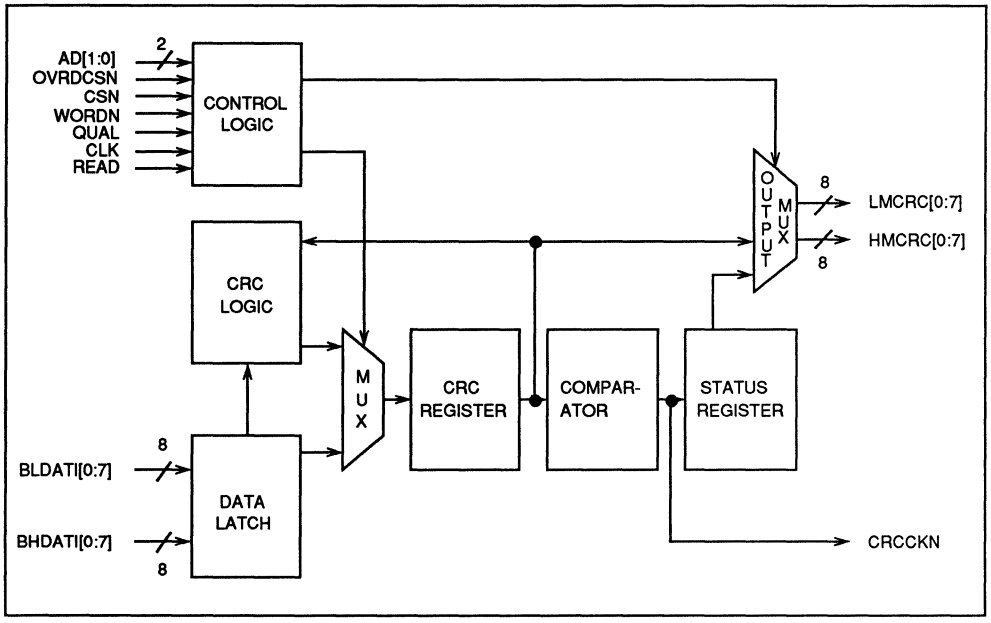
Block Diagram



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
AD[0:1]	LMCRC[0:7]↑	9.89	3.24	4.00	0.66
AD[0:1]	LMCRC[0:7]↓	9.09	4.10	3.77	1.07
AD[0:1]	HMCRC[0:7]↑	5.54	3.24	2.40	0.70
AD[0:1]	HMCRC[0:7]↓	6.29	2.31	2.57	0.58
CLK	CRCCKN↑	12.17	0.86	6.46	0.16
CLK	CRCCKN↓	13.54	1.19	7.37	0.29
CLK	LMCRC[0:7]↑	13.14	3.24	6.97	0.66
CLK	LMCRC[0:7]↓	15.14	4.10	8.00	1.07
CLK	HMCRC[0:7]↑	10.97	3.24	5.89	0.70
CLK	HMCRC[0:7]↓	11.09	2.31	5.20	0.58
WORDN	LMCRC[0:7]↑	8.06	3.24	3.49	0.66
WORDN	LMCRC[0:7]↓	8.17	4.10	3.43	1.07

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum AD[0:1] Setup before CLK	1.26	0.80
Minimum BLDATI[0:7] Setup before CLK	1.26	0.80
Minimum BHDATI[0:7] Setup before CLK	1.26	0.80
Minimum CSN Setup before CLK	1.26	0.80
Minimum OVRDCSN Setup before CLK	1.26	0.80
Minimum READ Setup before CLK	1.26	0.80

Divide-by-4 Counter DIV4

43 grids, 58 transistors

Functional Description and Features

DIV4 is a twisted-ring, divide-by-4 counter with a data-select front end. For frequency division the SC input should be high.

Terminal Descriptions

Netlist Order

INPUTS: DI, SC, CK, CD

OUTPUTS: Q1

Functional Descriptions

Inputs:

DI	Test data input
SC	Mode select
CK	Clock input
CD	Synchronous clear input

Outputs:

Q1	Divide-by-4 output

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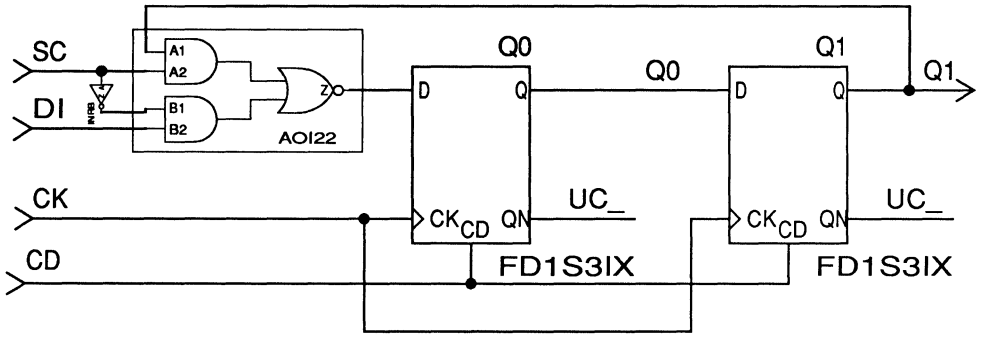
Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
CK↑	Q1↑	1.54	5.81	1.71	1.40
CK↑	Q1↓	1.66	7.93	1.60	1.77

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.14
Minimum DI Setup before CK↑	2.69	1.54
Minimum SC Setup before CK↑	3.20	1.77

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Divide-by-6 Counter DIV6

61 grids, 82 transistors

Functional Description and Features

DIV6 is a twisted-ring, divide-by-6 counter with a data-select front end. For frequency division the SC input should be high.

Terminal Descriptions

Netlist Order

INPUTS: DI, SC, CK, CD

OUTPUTS: Q2

Functional Descriptions

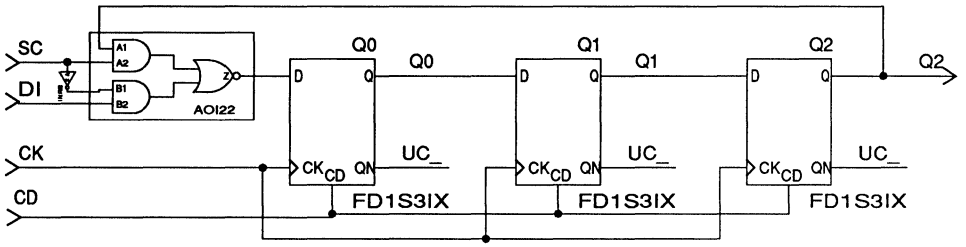
Inputs:

DI	Test data input
SC	Mode select
CK	Clock input
CD	Synchronous clear input

Outputs:

Q2	Divide-by-6 output

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
CK↑	Q2↑	1.54	5.81	1.71	1.40
CK↑	Q2↓	1.66	7.93	1.60	1.77

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.14
Minimum DI Setup before CK↑	2.69	1.54
Minimum SC Setup before CK↑	3.20	1.77

Divide-by-8 Counter DIV8

79 grids, 106 transistors

Functional Description and Features

DIV8 is a twisted-ring, divide-by-8 counter with a data-select front end. For frequency division the SC input should be high.

Terminal Descriptions

Netlist Order

INPUTS: DI, SC, CK, CD

OUTPUTS: Q3

Functional Descriptions

Inputs:

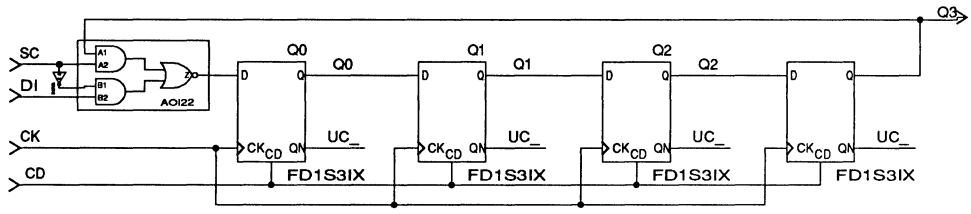
DI	Test data input
SC	Mode select
CK	Clock input
CD	Synchronous clear input

Outputs:

Q3	Divide-by-8 output

Divide-by-8 Counter DIV8

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
CK↑	Q3↑	1.54	5.81	1.71	1.40
CK↑	Q3↓	1.66	7.93	1.60	1.77

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.14
Minimum DI Setup before CK↑	2.69	1.54
Minimum SC Setup before CK↑	3.20	1.77

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4-Bit Fast Adder FA4

143 grids, 212 transistors

Functional Description and Features

The FA4 is functionally equivalent to the 7483 4-Bit Binary Full Adder With Fast Carry within the standard 74XX Series logic families of devices. This full-adder circuit provides binary addition of two 4-bit binary numbers, with internal carry look-ahead across all four bits for fast operation. The corresponding outputs for each bit are: SUM1, SUM2, SUM3 and SUM4. The carry-out is C4.

Terminal Descriptions

Netlist Order

INPUTS: A1, A2, A3, A4, B1, B2, B3, B4, C0

OUTPUTS: SUM1, SUM2, SUM3, SUM4, C4

Functional Descriptions

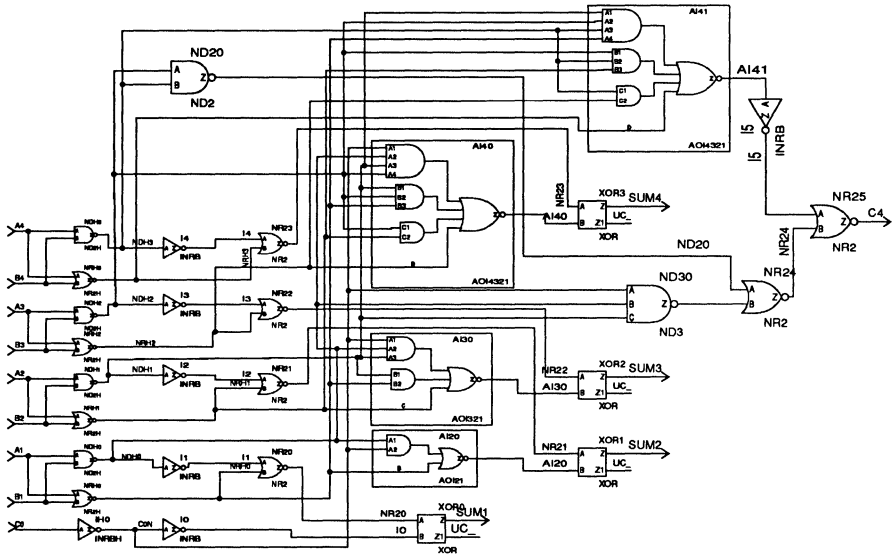
Inputs:

A[1:4]	Word 'A' inputs
B[1:4]	Word 'B' inputs
C0	Carry in

Outputs:

SUM[1:4]	Sum outputs
C4	Carry out

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
A[1:4],B[1:4]	C4↑	6.57	6.47	2.91	1.36
A[1:4],B[1:4]	C4↓	5.83	2.31	2.46	0.58
A[1:4],B[1:4]	SUM[1:4]↑	6.11	8.98	3.03	2.01
A[1:4],B[1:4]	SUM[1:4]↓	5.77	12.68	2.86	2.71
C0	C4↑	2.29	6.47	0.91	1.36
C0	C4↓	4.23	2.31	1.66	0.58
C0	SUM[1:4]↑	4.74	8.98	2.46	2.01
C0	SUM[1:4]↓	4.40	12.68	2.34	2.71

4-Bit Look Ahead Carry Generator — LACG4

98 grids, 152 transistors

Functional Description and Features

The LACG4 is functionally equivalent to the 74182 Look-Ahead Carry Generator within the standard 74XX Series logic families of devices. LACG4 provides carry, generate-carry function, and propagate-carry function with fast carry look-ahead.

Terminal Descriptions

Netlist Order

INPUTS: X0, X1, X2, X3, Y0, Y1, Y2, Y3, CN0

OUTPUTS: XA, YA, CNPX, CNPY, CNPZ

Functional Descriptions

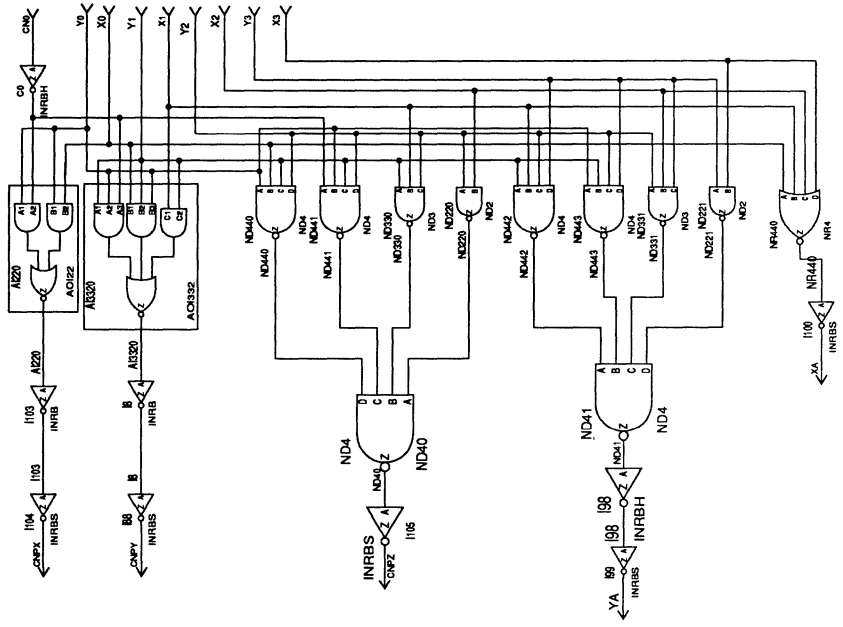
Inputs:

X[0:3]	Carry-propagate inputs, active-low
Y[0:3]	Carry-generate inputs, active-low
CN0	Carry input

Outputs:

XA	Carry-propagate output, active-low
YA	Carry-generate output, active-low
CNP[X,Y,Z]	Carry outputs

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
CN0	CNP[X,Y,Z]↑	4.11	0.86	2.06	0.21
CN0	CNP[X,Y,Z]↓	3.77	0.86	1.83	0.21
X[0:3],Y[0:3]	CNP[X,Y,Z]↑	3.71	0.86	1.77	0.21
X[0:3],Y[0:3]	CNP[X,Y,Z]↓	2.74	0.86	1.49	0.21
X[0:3]	XA↑	0.63	0.86	0.40	0.21
X[0:3]	XA↓	3.54	0.86	1.94	0.21
X[1:3],Y[0:3]	YA↑	3.09	0.86	1.60	0.21
X[1:3],Y[0:3]	YA↓	3.26	0.86	1.77	0.21

16 X 16 Multiplier

MUL16X16

5443 grids, 8100 transistors

Functional Description and Features

The MUL16X16 is a high-speed, 16 X 16 multiplier in 2's complement arithmetic implemented as a standard-cell netlist. It has been designed with static combinatorial logic without pipelining. True high-performance and ease of use are achieved by eliminating complicated timing requirements and latency associated with pipe-lined structures. The design is suitable for a wide range of computation-intensive applications, for example, digital signal processing.

The partial products to be summed are generated from the M-inputs by the Booth Selector, which is controlled by the outputs of the Booth Encoder that operate on the N-inputs. The partial products are summed by carry-save adders arranged in a Wallace Tree structure. The final carry-propagate is performed by an optimally partitioned carry-select adder stage.

Terminal Descriptions

Netlist Order

INPUTS: M0, M1, M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, M12, M13, M14, M15, N0, N1, N2, N3, N4, N5, N6, N7, N8, N9, N10, N11, N12, N13, N14, N15

OUTPUTS: P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, P17, P18, P19, P20, P21, P22, P23, P24, P25, P26, P27, P28, P29, P30, P31

Functional Descriptions

Inputs:

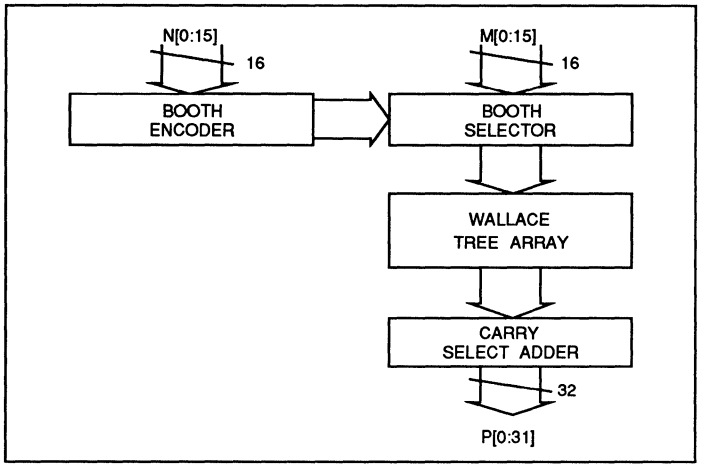
M[0:15], N[0:15]	Inputs

Outputs:

P[0:31]	Outputs

11

Block Diagram



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
M[0:15],N[0:15]	P[0:31]	71.9	3.24	37.6	0.70

11

3-Bit Majority Vote — MV3

13 grids, 18 transistors

Functional Description and Features

MV3 is a 3-bit, majority-vote circuit. The output is high when a majority is present at the inputs.

Terminal Descriptions

Netlist Order

INPUTS: V1, V2, V3

OUTPUTS: MVI

Functional Descriptions

Inputs:

V[1:3]	Data inputs

Outputs:

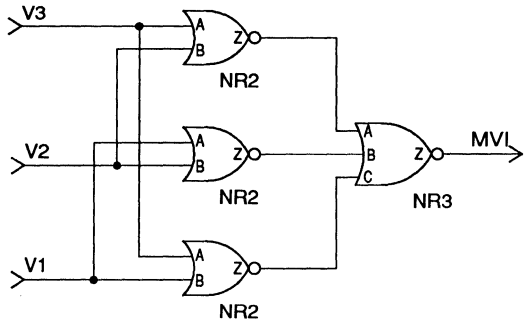
MVI	Majority indicator

TRUTH TABLE

V1	V2	V3	MVI
0	0	X	0
0	X	0	0
X	0	0	0
1	1	X	1
1	X	1	1
X	1	1	1

X = don't care.

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From Input	To Output	Area		Performance	
		Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
V[1:3]	MVI↑	0.63	9.64	0.40	2.01
V[1:3]	MVI↓	1.37	2.25	0.57	0.58

11

5-Bit Majority Vote

MV5

41 grids, 62 transistors

Functional Description and Features

MV5 is a 5-bit, majority-vote circuit. The output is high when a majority is present at the inputs.

Terminal Descriptions

Netlist Order

INPUTS: V1, V2, V3, V4, V5

OUTPUTS: MVI

Functional Descriptions

Inputs:

V[1:5]	Data inputs

Outputs:

MVI	Majority indicator

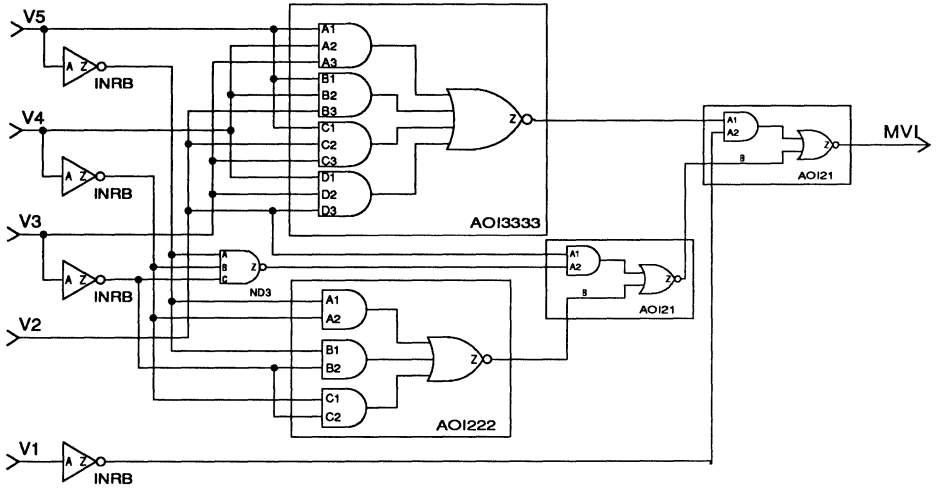
TRUTH TABLE

V1	V2	V3	V4	V5	MVI
0	0	0	X	X	0
0	0	X	X	0	0
0	X	X	0	0	0
X	X	0	0	0	0
X	0	0	0	X	0
1	1	1	X	X	1
1	1	X	X	1	1
1	X	X	1	1	1
X	X	1	1	1	1
X	1	1	1	X	1

X = don't care.

5-Bit Majority Vote MV5

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
V1	MVI↑	0.51	6.47	0.29	1.36
V1	MVI↓	0.80	4.03	0.34	1.07
V2	MVI↑	1.71	6.47	1.09	1.36
V2	MVI↓	3.49	4.03	1.71	1.07
V[3:5]	MVI↑	4.29	6.47	1.89	1.36
V[3:5]	MVI↓	4.69	4.03	1.94	1.07

11

3-Bit, Programmable Counter/Timer — PCLE3

96 grids, 140 transistors

Functional Description and Features

PCLE3 is a programmable counter/timer with positive load, enable, and synchronous clear. The counter has linear feedback and counts in a pseudo-random sequence. The timer generates a positive-going pulse when the last state is reached. The enable input should be kept high for counting or loading a starting value. The counter can be set to any non-zero starting value by applying a 3-bit binary code to inputs D[0:2] and keeping the load input high. The value is loaded after the next clock cycle. The counter will count from the loaded value until it reaches a value of (001). If a new value is not loaded and the counter is not disabled, it will recycle and generate a positive-going pulse after seven counts.

- Programmable
- Positive load and count enable
- Synchronous clear

Terminal Descriptions

Netlist Order

INPUTS: D0, D1, D2, LD, EN, CK, CD

OUTPUTS: Z

Functional Descriptions

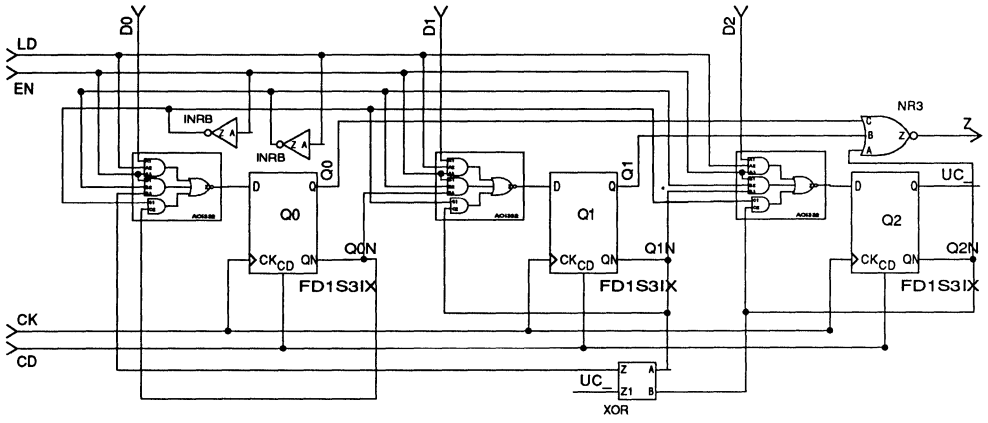
Inputs:

D[0:2]	Parallel data inputs
LD	Load input, active-high
EN	Count enable, active-high
CK	Clock input
CD	Clear input, active-high

Outputs:

Z	Output

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
CK↑	Z↑	4.74	9.64	3.09	2.01
CK↑	Z↓	4.40	2.25	3.43	0.58

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.14
Minimum D[0:2] Setup before CK↑	3.43	1.89
Minimum EN Setup before CK↑	4.69	2.34
Minimum LD Setup before CK↑	4.97	2.51

11

4-Bit, Programmable Counter/Timer PCLE4

124 grids, 182 transistors

Functional Description and Features

PCLE4 is a programmable counter/timer with positive load, enable, and synchronous clear. The counter has linear feedback and counts in a pseudo-random sequence. The timer generates a positive-going pulse when the last state is reached. The enable input should be kept high for counting or loading a starting value. The counter can be set to any non-zero starting value by applying a 4-bit binary code to inputs D[0:3] and keeping the load input high. The value is loaded after the next clock cycle. The counter will count from the loaded value until it reaches a value of (0001). If a new value is not loaded and the counter is not disabled, it will recycle and generate a positive-going pulse after 15 counts.

- Programmable
- Positive load and count enable
- Synchronous clear

Terminal Descriptions

Netlist Order

INPUTS: D0, D1, D2, D3, LD, EN, CK, CD

OUTPUTS: Z

Functional Descriptions

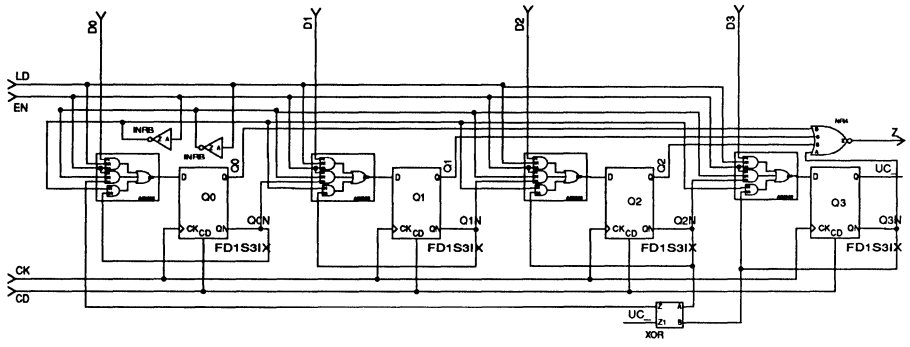
Inputs:

D[0:3]	Parallel data inputs
LD	Load input, active-high
EN	Count enable, active-high
CK	Clock input
CD	Clear input, active-high

Outputs:

Z	Output

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
CK↑	Z↑	4.86	12.88	3.14	2.75
CK↑	Z↓	4.40	1.98	3.49	0.58

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.14
Minimum D[0:3] Setup before CK↑	3.42	1.89
Minimum EN Setup before CK↑	5.26	2.57
Minimum LD Setup before CK↑	5.54	2.69

11

5-Bit, Programmable Counter/Timer PCLE5

156 grids, 228 transistors

Functional Description and Features

PCLE5 is a programmable counter/timer with positive load, enable, and synchronous clear. The counter has linear feedback and counts in a pseudo-random sequence. The timer generates a positive-going pulse when the last state is reached. The enable input should be kept high for counting or loading a starting value. The counter can be set to any non-zero starting value by applying a 5-bit binary code to inputs D[0:4] and keeping the load input high. The value is loaded after the next clock cycle. The counter will count from the loaded value until it reaches a value of (00001). If a new value is not loaded and the counter is not disabled, it will recycle and generate a positive-going pulse after 31 counts.

- Programmable
- Positive load and count enable
- Synchronous clear

Terminal Descriptions

Netlist Order

INPUTS: D0, D1, D2, D3, D4, LD, EN, CK, CD

OUTPUTS: Z

Functional Descriptions

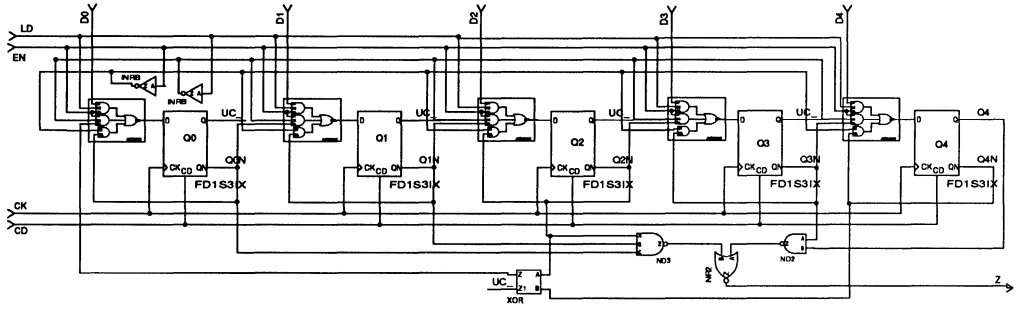
Inputs:

D[0:4]	Parallel data inputs
LD	Load input, active-high
EN	Count enable, active-high
CK	Clock input
CD	Clear input, active-high

Outputs:

Z	Output

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
CK↑	Z↑	5.89	6.47	3.71	1.36
CK↑	Z↓	4.63	2.31	3.20	0.58

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.14
Minimum D[0:4] Setup before CK↑	3.37	1.94
Minimum EN Setup before CK↑	5.77	2.74
Minimum LD Setup before CK↑	6.11	2.91

11

6-Bit, Programmable Counter/Timer — PCLE6

184 grids, 270 transistors

Functional Description and Features

PCLE6 is a programmable counter/timer with positive load, enable, and synchronous clear. The counter has linear feedback and counts in a pseudo-random sequence. The timer generates a positive-going pulse when the last state is reached. The enable input should be kept high for counting or loading a starting value. The counter can be set to any non-zero starting value by applying a 6-bit binary code to inputs D[0:5] and keeping the load input high. The value is loaded after the next clock cycle. The counter will count from the loaded value until it reaches a value of (000001). If a new value is not loaded and the counter is not disabled, it will recycle and generate a positive-going pulse after 63 counts.

- Programmable
- Positive load and count enable
- Synchronous clear

Terminal Descriptions

Netlist Order

INPUTS: D0, D1, D2, D3, D4, D5, LD, EN, CK, CD

OUTPUTS: Z

Functional Descriptions

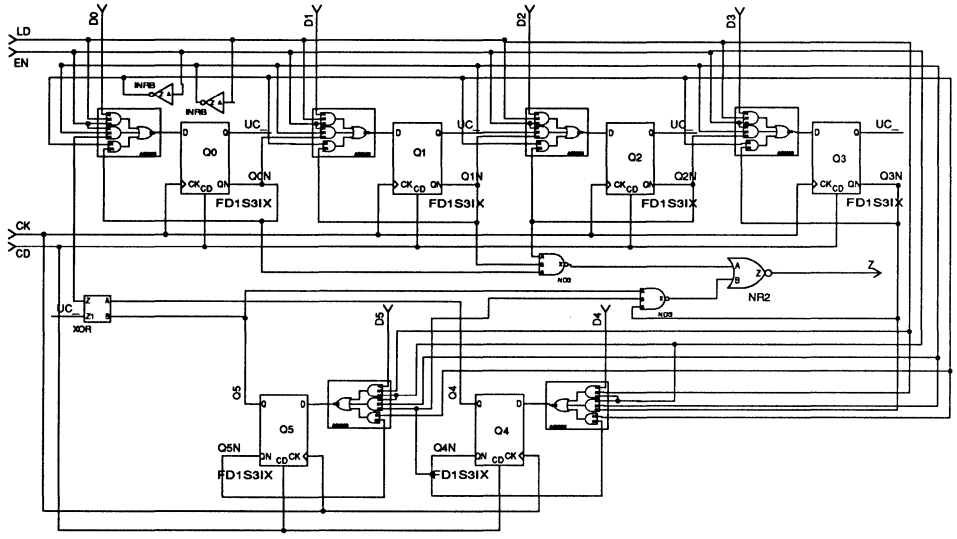
Inputs:

D[0:5]	Parallel data inputs
LD	Load input, active-high
EN	Count enable, active-high
CK	Clock input
CD	Clear input, active-high

Outputs:

Z	Output

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
CK↑	Z↑	5.49	6.47	4.69	1.36
CK↑	Z↓	4.69	2.31	3.66	0.58

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.14
Minimum D[0:5] Setup before CK↑	3.43	1.89
Minimum EN Setup before CK↑	6.29	2.86
Minimum LD Setup before CK↑	6.63	3.03

11

8-Bit, Programmable Counter/Timer — PCLE8

240 grids, 354 transistors

Functional Description and Features

PCLE8 is a programmable counter/timer with positive load, enable, and synchronous clear. The counter has linear feedback and counts in a pseudo-random sequence. The timer generates a positive-going pulse when the last state is reached. The enable input should be kept high for counting or loading a starting value. The counter can be set to any non-zero starting value by applying an 8-bit binary code to inputs D[0:7] and keeping the load input high. The value is loaded after the next clock cycle. The counter will count from the loaded value until it reaches a value of (00000001). If a new value is not loaded and the counter is not disabled, it will recycle and generate a positive-going pulse after 217 counts.

- Programmable
- Positive load and count enable
- Synchronous clear

Terminal Descriptions

Netlist Order

INPUTS: D0, D1, D2, D3, D4, D5, D6, D7, LD, EN, CK, CD

OUTPUTS: Z

Functional Descriptions

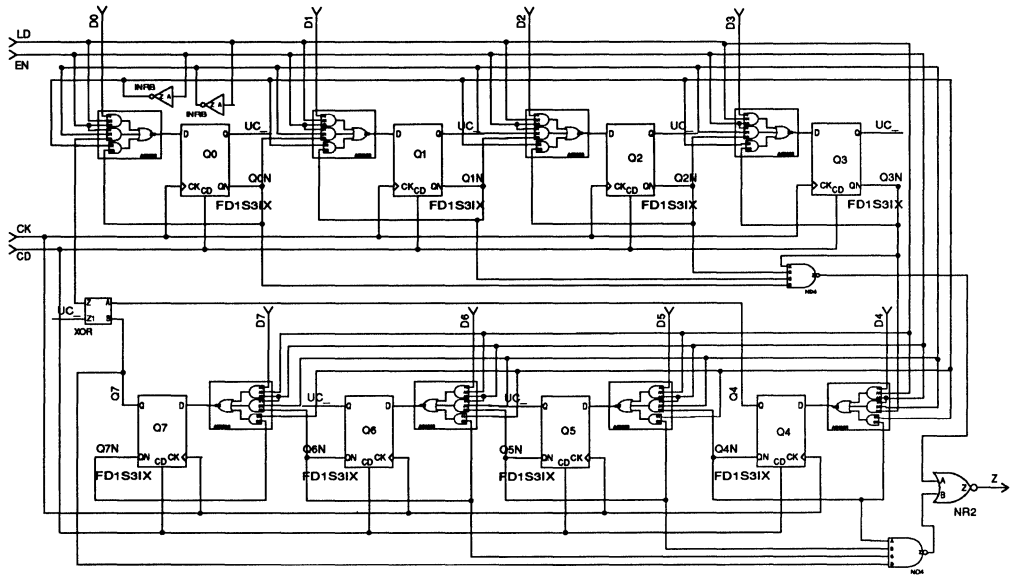
Inputs:

D[0:7]	Parallel data inputs
LD	Load input, active-high
EN	Count enable, active-high
CK	Clock input
CD	Clear input, active-high

Outputs:

Z	Output

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
CK↑	Z↑	5.94	6.47	4.86	1.36
CK↑	Z↓	4.69	2.31	3.71	0.58

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.14
Minimum D[0:7] Setup before CK↑	3.37	1.89
Minimum EN Setup before CK↑	7.26	3.26
Minimum LD Setup before CK↑	7.60	3.37

11

3-Bit, Programmable Counter/Timer PCLER3

99 grids, 144 transistors

Functional Description and Features

PCLER3 is a programmable counter/timer with positive load, enable, and synchronous clear. The counter has linear feedback and counts in a pseudo-random sequence. The timer generates a positive-going pulse when the last state is reached. The enable input should be kept high for counting or loading a starting value. The counter can be set to any non-zero starting value by applying a 3-bit binary code to inputs D[0:2] and keeping the load input high. The value is loaded after the next clock cycle. The counter will count from the loaded value until it reaches a value of (001). If a new value is not loaded and the counter is not disabled, it will reload the value at its D[0:2] inputs. The maximum count is seven.

- Programmable
- Positive load and count enable
- Synchronous clear
- Recycle from last loaded value

Terminal Descriptions

Netlist Order

INPUTS: D0, D1, D2, LD, EN, CK, CD

OUTPUTS: Z

Functional Descriptions

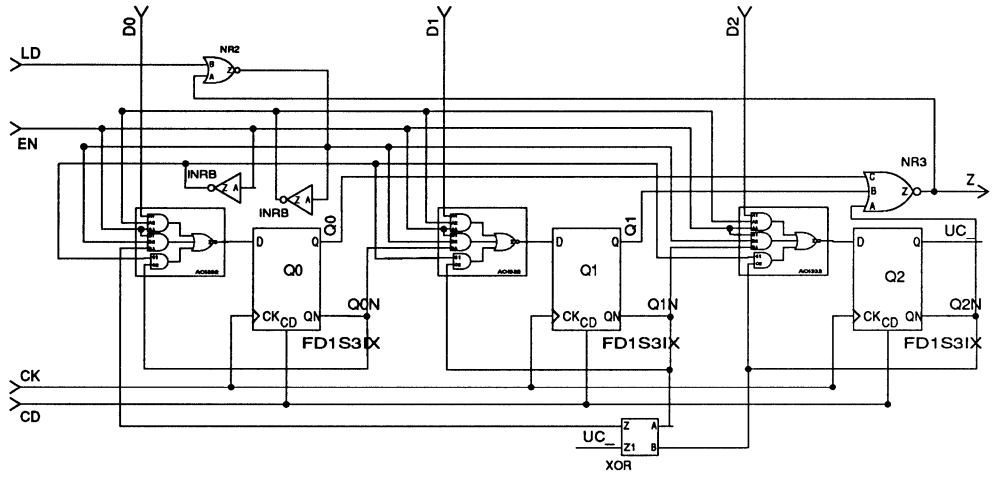
Inputs:

D[0:2]	Parallel data inputs
LD	Load input, active-high
EN	Count enable, active-high
CK	Clock input
CD	Clear input, active-high

Outputs:

Z	Output

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
CK↑	Z↑	5.83	9.64	3.43	2.01
CK↑	Z↓	4.97	2.25	3.89	0.58

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.14
Minimum D[0:2] Setup before CK↑	3.43	1.89
Minimum EN Setup before CK↑	4.69	2.34
Minimum LD Setup before CK↑	9.94	4.23

4-Bit, Programmable Counter/Timer — PCLER4

127 grids, 186 transistors

Functional Description and Features

PCLER4 is a programmable counter/timer with positive load, enable, and synchronous clear. The counter has linear feedback and counts in a pseudo-random sequence. The timer generates a positive-going pulse when the last state is reached. The enable input should be kept high for counting or loading a starting value. The counter can be set to any non-zero starting value by applying a 4-bit binary code to inputs D[0:3] and keeping the load input high. The value is loaded after the next clock cycle. The counter will count from the loaded value until it reaches a value of (0001). If a new value is not loaded and the counter is not disabled, it will reload the value at its D[0:3] inputs. The maximum count is fifteen.

- Programmable
- Positive load and count enable
- Synchronous clear
- Recycle from last loaded value

Terminal Descriptions

Netlist Order

INPUTS: D0, D1, D2, D3, LD, EN, CK, CD

OUTPUTS: Z

Functional Descriptions

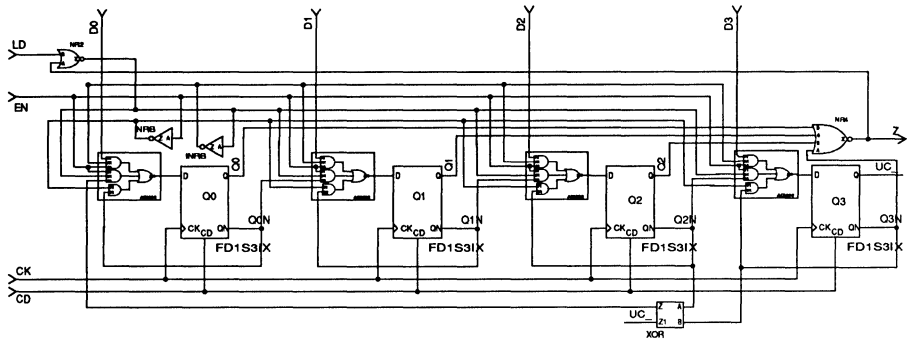
Inputs:

D[0:3]	Parallel data inputs
LD	Load input, active-high
EN	Count enable, active-high
CK	Clock input
CD	Clear input, active-high

Outputs:

Z	Output

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
CK↑	Z↑	6.06	12.88	3.54	2.75
CK↑	Z↓	5.09	1.98	3.94	0.58

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.14
Minimum D[0:3] Setup before CK↑	3.43	1.89
Minimum EN Setup before CK↑	5.20	2.57
Minimum LD Setup before CK↑	11.54	4.91

11

5-Bit, Programmable Counter/Timer PCLER5

159 grids, 232 transistors

Functional Description and Features

PCLER5 is a programmable counter/timer with positive load, enable, and synchronous clear. The counter has linear feedback and counts in a pseudo-random sequence. The timer generates a positive-going pulse when the last state is reached. The enable input should be kept high for counting or loading a starting value. The counter can be set to any non-zero starting value by applying a 5-bit binary code to inputs D[0:4] and keeping the load input high. The value is loaded after the next clock cycle. The counter will count from the loaded value until it reaches a value of (.00001). If a new value is not loaded and the counter is not disabled, it will reload the value at its D[0:4] inputs. The maximum count is 31.

- Programmable
- Positive load and count enable
- Synchronous clear
- Recycle from last loaded value

Terminal Descriptions

Netlist Order

INPUTS: D0, D1, D2, D3, D4, LD, EN, CK, CD

OUTPUTS: Z

Functional Descriptions

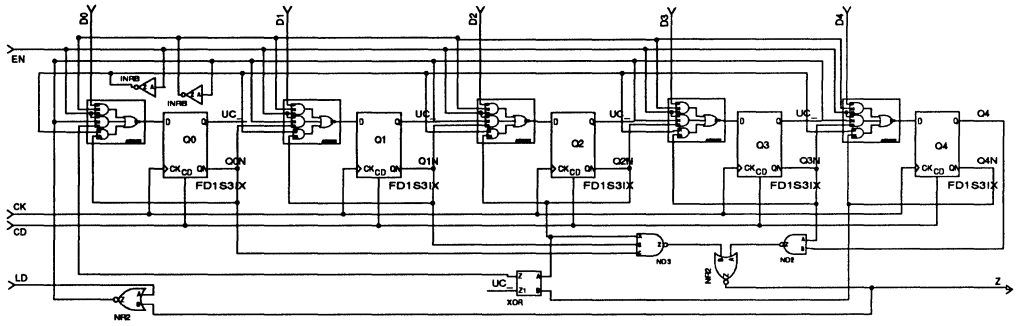
Inputs:

D[0:4]	Parallel data inputs
LD	Load input, active-high
EN	Count enable, active-high
CK	Clock input
CD	Clear input, active-high

Outputs:

Z	Output

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
CK↑	Z↑	6.74	6.47	4.00	1.36
CK↑	Z↓	5.14	2.31	3.37	0.58

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.14
Minimum D[0:4] Setup before CK↑	3.37	1.94
Minimum EN Setup before CK↑	5.77	2.74
Minimum LD Setup before CK↑	13.26	5.37

6-Bit, Programmable Counter/Timer PCLER6

187 grids, 274 transistors

Functional Description and Features

PCLER6 is a programmable counter/timer with positive load, enable, and synchronous clear. The counter has linear feedback and counts in a pseudo-random sequence. The timer generates a positive-going pulse when the last state is reached. The enable input should be kept high for counting or loading a starting value. The counter can be set to any non-zero starting value by applying a 6-bit binary code to inputs D[0:5] and keeping the load input high. The value is loaded after the next clock cycle. The counter will count from the loaded value until it reaches a value of (000001). If a new value is not loaded and the counter is not disabled, it will reload the value at its D[0:5] inputs. The maximum count is 63.

- Programmable
- Positive load and count enable
- Synchronous clear
- Recycle from last loaded value

Terminal Descriptions

Netlist Order

INPUTS: D0, D1, D2, D3, D4, D5, LD, EN, CK, CD

OUTPUTS: Z

Functional Descriptions

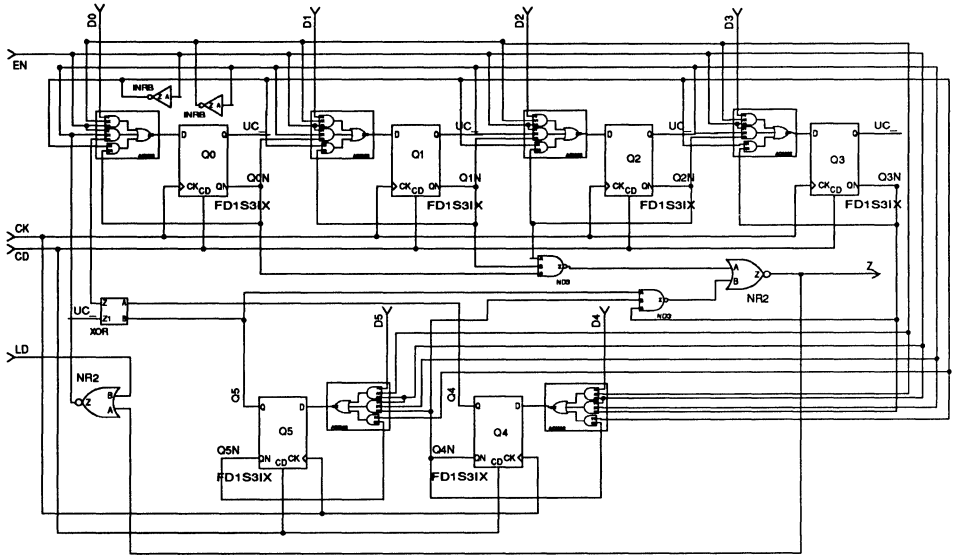
Inputs:

D[0:5]	Parallel data inputs
LD	Load input, active-high
EN	Count enable, active-high
CK	Clock input
CD	Clear input, active-high

Outputs:

Z	Output

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
CK↑	Z↑	6.34	6.47	4.97	1.36
CK↑	Z↓	5.20	2.31	3.83	0.58

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.14
Minimum D[0:5] Setup before CK↑	3.43	1.89
Minimum EN Setup before CK↑	6.23	2.86
Minimum LD Setup before CK↑	14.86	6.06

8-Bit, Programmable Counter/Timer PCLER8

243 grids, 358 transistors

Functional Description and Features

PCLER8 is a programmable counter/timer with positive load, enable, and synchronous clear. The counter has linear feedback and counts in a pseudo-random sequence. The timer generates a positive-going pulse when the last state is reached. The enable input should be kept high for counting or loading a starting value. The counter can be set to any non-zero starting value by applying an 8-bit binary code to inputs D[0:7] and keeping the load input high. The value is loaded after the next clock cycle. The counter will count from the loaded value until it reaches a value of (00000001). If a new value is not loaded and the counter is not disabled, it will reload the value at its D[0:7] inputs. The maximum count is 217.

- Programmable
- Positive load and count enable
- Synchronous clear
- Recycle from last loaded value

Terminal Descriptions

Netlist Order

INPUTS: D0, D1, D2, D3, D4, D5, D6, D7, LD, EN, CK, CD

OUTPUTS: Z

Functional Descriptions

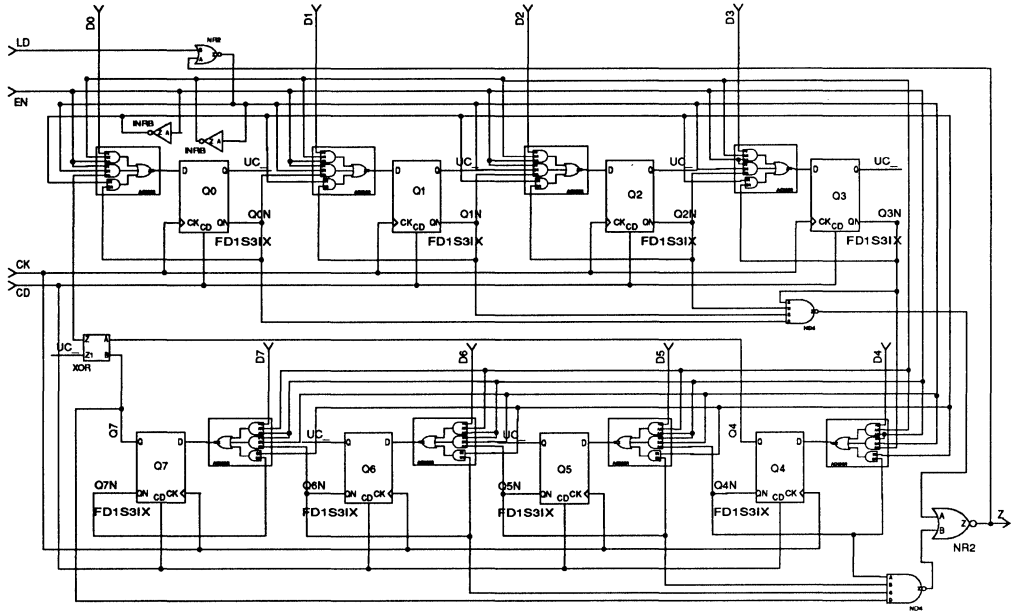
Inputs:

D[0:7]	Parallel data inputs
LD	Load input, active-high
EN	Count enable, active-high
CK	Clock input
CD	Clear input, active-high

Outputs:

Z	Output

Detailed Schematic



Characteristics

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From Input	To Output	Area		Performance	
		Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
CK↑	Z↑	6.80	6.47	5.14	1.36
CK↑	Z↓	5.26	2.31	3.89	0.58

TIMING REQUIREMENTS VDD=5.0V, T=25°C, Nominal Processing		
Description	Area value (ns)	Perf. value (ns)
Minimum CD Setup before CK↑	1.71	1.14
Minimum D[0:7] Setup before CK↑	3.37	1.89
Minimum EN Setup before CK↑	7.20	3.26
Minimum LD Setup before CK↑	17.94	7.14

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Boundary Scan Cells

Section 12

Contents - Section 12

Boundary-Scan Introduction

Because of the increasing complexity of Integrated circuits, surface-mount interconnection technology has created significant new problems in the development and application of tests for printed circuit boards. To cope with this problem, a proposal has been prepared by an *ad hoc* international standards body, the Joint Test Action Group (JTAG), to standardize board interconnect tests by using Boundary-Scan (B-S). The IEEE Standard P1149.1, as proposed, will accomplish two major goals: 1) to simplify testing of high-density circuit boards through B-S, and 2) to provide a common access to the various chip-level BIST resources for test and diagnosis at all levels of assembly.

JTAG is an international group representing companies in Europe and North America seeking solutions for the test problems in hybrid and PCB products created by the combination of complex integrated circuits and surface-mount technology.

A schematic overview of BIST & Boundary-Scan on a board is shown on the next page.

The B-S cells for the pins of a chip are interconnected to perform a shift register chain around the border of the device. This path is provided with serial input and output connections and appropriate clock and control signals. The serial path can be used for three purposes:

- External B-S Test allows the interconnections between the various chips to be tested. Test data can be shifted into the BSOUT cell associated with chip outputs pins and then loaded in parallel through the chip interconnections into those BSIN[1-3] cells associated with input pins;
- Internal B-S Test allows chips on a board to be tested. The B-S register can be used as a means of isolating system logic from stimuli received from surrounding chips while an internal self-test is performed;
- Sample Test occurs by parallel loading the BSIN[1-3] cells at inputs and the BSOUT cell at outputs of a chip and shifting out the results. The B-S register provides a means of 'sampling' the data flowing through a chip without interfering with its normal function. This sample B-S test is valuable for design debugging and fault diagnosis.

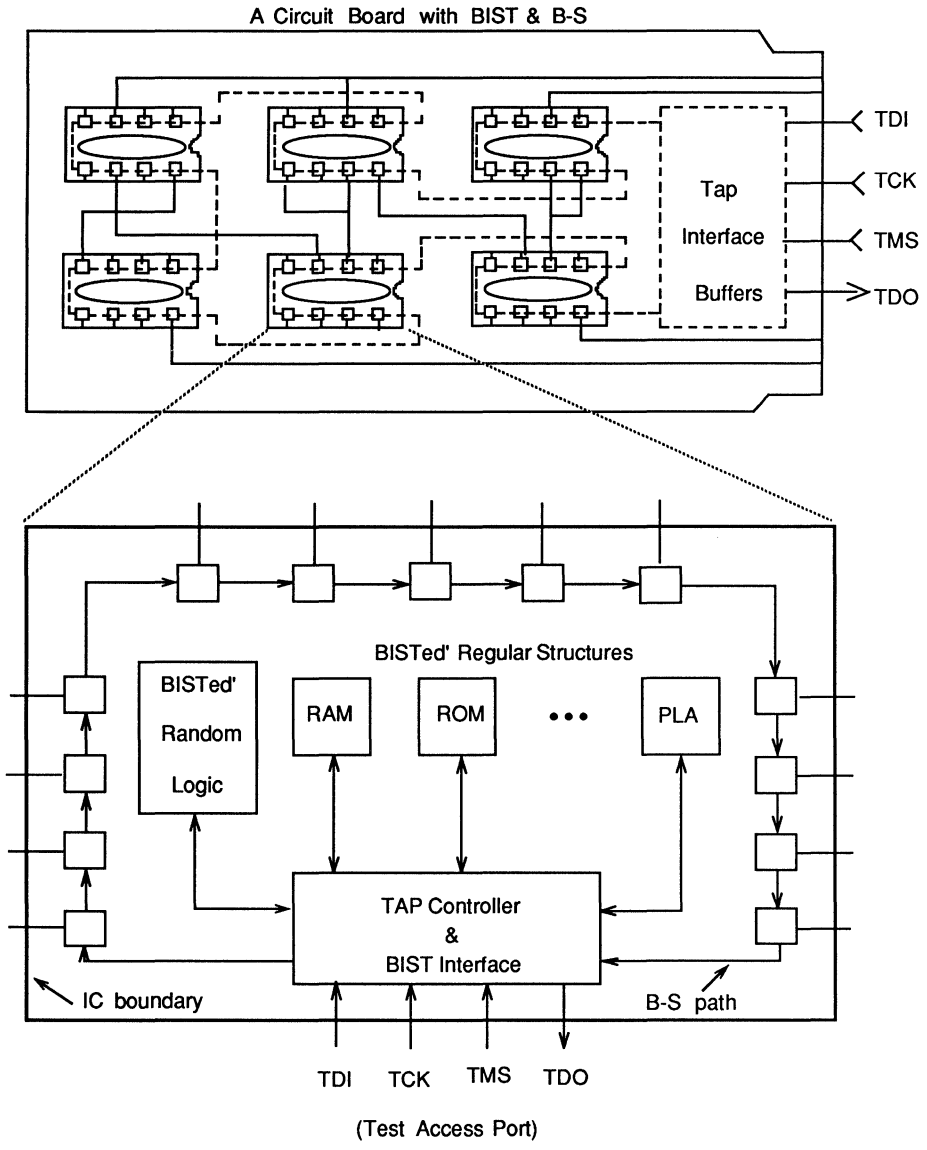
BOUNDARY-SCAN TEST-MODE DEFINITION

TEST MODE	*LOGIC VALUE (MODE)*
SAMPLE, NORMAL	**0**
INTERNAL, EXTERNAL	**1**

The performance, or maximum clock frequency of B-S circuitry is usually dictated by that of the TAP controller (BSTAP).

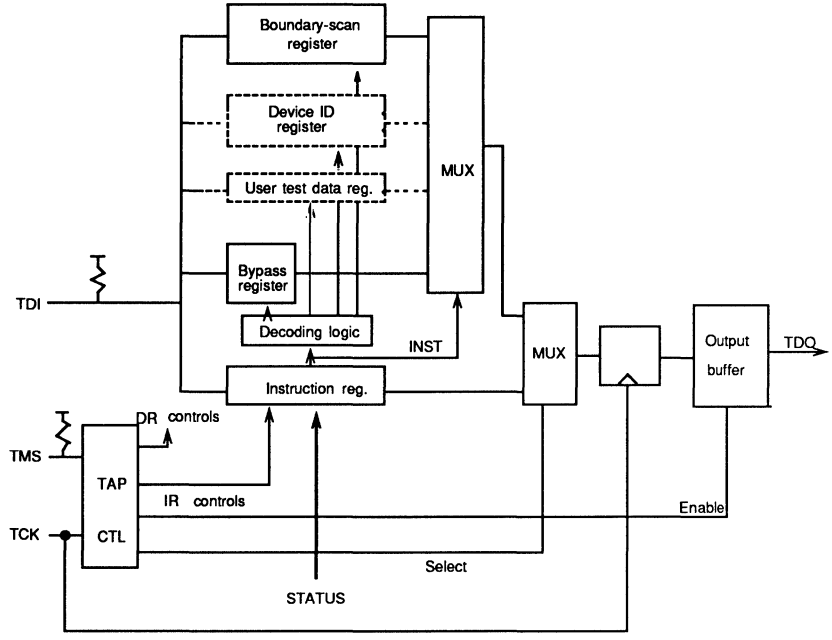
Timing characteristics provided in this section were obtained with AT&T's static timing analyzer, CRITIC. They are estimated with an average routing capacitance of 0.1 pF per fanout. The more accurate circuit simulator, GSIM, should be used to verify the proper timing for your final design.

BIST & BOUNDARY-SCAN OVERVIEW



12

BLOCK DIAGRAM



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B-S Identification Register BSATT

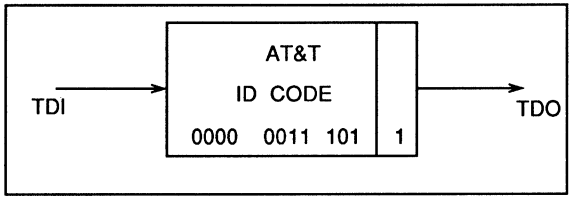
228 grids, 360 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSATT is the 12 least significant bits of the manufacturer's ID register for AT&T. It is compatible to JTAG standard.

- When the CAPTURE pin is high, this register is loaded with/initialized to "0000 0011 1011" (or hex 03B) which is the official JTAG code assigned to AT&T. The code can be shifted out towards TDO when the SHIFTN pin is low.

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: TDI,TCK,CAPTURE,SHIFTN
OUTPUT: TDO

Functional Descriptions

Inputs:

TDI	Serial test data input
TCK	Boundary Scan test clock
CAPTURE	Capture/load scan-register; Derived from BSTAP controller
SHIFTN	Derived from SHIFTDR signal generated by BSTAP controller; active low

Output:

TDO	Serial test data output

CHARACTERISTICS

SWITCHING CHARACTERISTICS
VDD=5.0V, T=25°C, Nominal Processing

From Input	To Output	Area		Performance	
		Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
TCK↑	TDO↓	0.17	2.05	0.40	0.58
TCK↑	TDO↑	0.23	3.24	0.40	0.70

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Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area Value	Perf. Value	Unit
Minimum TDI Setup before TCK↑ Minimum SHIFTN Setup before TCK↑	2.5 2.5	1.7 1.7	ns

B-S, Bidirectional Cell BSBD

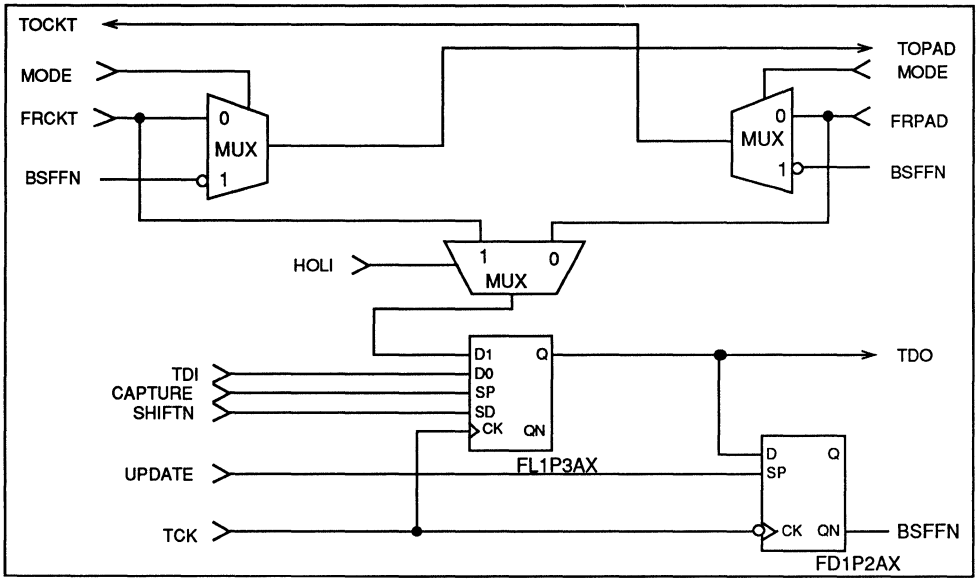
64 grids, 94 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSBD is a JTAG compatible, boundary scan, bidirectional cell.

- Used along with bidirectional I/O buffer
- Direction control line (HOLI) is controlled by BSDC
- Acts as a BSIN when HOLI = 0
- Acts as a BSOUT when HOLI = 1

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: FRCKT,TDI,TCK,HOLI,MODE,CAPTURE,SHIFTN,UPDATE,FRPAD

OUTPUTS: TOCKT,TOPAD,TDO

Functional Descriptions

Inputs:

FRCKT	Input from chip internal circuitry (to output pad)
TDI	Serial test data input (from previous boundary scan cell)
TCK	Boundary scan test clock
HOLI	Direction control signal from BSDC cell (High:Output, Low:Input)
MODE	N0rmal/test-mode, control asserted in Internal or External Mode
CAPTURE	Capture/load scan-register; Derived from BSTAP controller
SHIFTN	Shift scan-register (active-low); Derived from BSTAP controller
UPDATE	Update parallel output register; Derived from BSTAP controller
FRPAD	Input from chip-input pad (to internal circuit)

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B-S Bidirectional Cell BSBD

Outputs:

TOCKT	Output to chip internal circuit (from input pad, or update latch)
TOPAD	Output to chip output pad (from internal circuit, or update latch)
TDO	Serial test data output (to next boundary scan cell)

CHARACTERISTICS

SWITCHING CHARACTERISTICS
VDD=5.0V, T=25°C, Nominal Processing

From Input	To Output	Area		Performance	
		Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
TCK↓	TOCKT↓	2.97	4.03	2.57	1.07
TCK↓	TOCKT↑	2.69	6.41	2.23	1.36
TCK↓	TOPAD↓	2.97	4.03	2.57	1.07
TCK↓	TOPAD↑	2.69	6.41	2.23	1.36
TCK↑	TDO↓	2.40	7.93	2.17	1.73
TCK↑	TDO↑	2.23	5.81	2.34	1.44
FRCKT	TOPAD↓	0.63	1.98	0.40	0.53
FRCKT	TOPAD↑	0.29	4.82	0.23	1.03
MODE	TOCKT↓	0.63	1.98	0.40	0.53
MODE	TOCKT↑	0.29	6.47	0.23	1.36
MODE	TOPAD↓	0.63	1.98	0.40	0.53
MODE	TOPAD↑	0.29	6.47	0.23	1.36
FRPAD	TOCKT↓	0.63	1.98	0.40	0.53
FRPAD	TOCKT↑	0.29	4.82	0.23	1.03

Timing Requirements
VDD=5.0V, T=25°C, Nominal Processing

Description	Area value	Perf. value	Unit
Minimum FRCKT Setup before TCK↑	4.2	2.3	ns
Minimum TDI Setup before TCK↑	3.2	1.7	
Minimum HOLI Setup before TCK↑	4.4	2.4	
Minimum MODE Setup before TCK↑	4.2	2.3	
Minimum CAPTURE Setup before TCK↑	3.2	1.7	
Minimum SHIFTN Setup before TCK↑	3.2	1.7	
Minimum UPDATE Setup before TCK↓	1.9	1.3	
Minimum FRPAD Setup before TCK↑	4.2	2.3	

B-S, Bypass Cell

BSBP

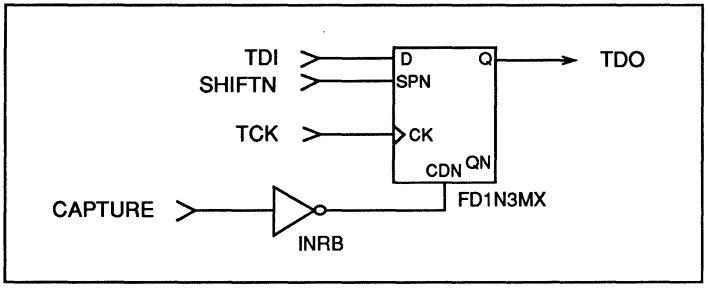
23 grids, 34 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSBP is a JTAG compatible, boundary scan, bypass cell.

- Provides a short-circuit route for test data in scanning cycle especially during board diagnosis

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: TDI,TCK,CAPTURE,SHIFTN
OUTPUT: TDO

Functional Descriptions

Inputs:

TDI	Serial test data input (from TDI input pad)
TCK	Boundary scan test clock
CAPTURE	Capture/ load (logic 0) into bypass register; Derived from BSTAP controller
SHIFTN	Shift DR signal (active-low); Derived from BSTAP controller

Output:

TDO	Serial test data output (to the DR MUX)

CHARACTERISTICS

SWITCHING CHARACTERISTICS
VDD=5.0V, T=25°C, Nominal Processing

From Input	To Output	Area		Performance	
		Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
TCK↑	TDO↓	0.17	7.93	0.40	1.73
TCK↑	TDO↑	0.23	5.75	0.40	1.44

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Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area Value	Perf. Value	Unit
Minimum TDI Setup before TCK↑	2.2	1.5	ns
Minimum CAPTURE Setup before TCK↑	2.6	1.7	
Minimum SHIFTN Setup before TCK↑	2.2	1.5	

BIST Resource Interface Controller BSBRIC

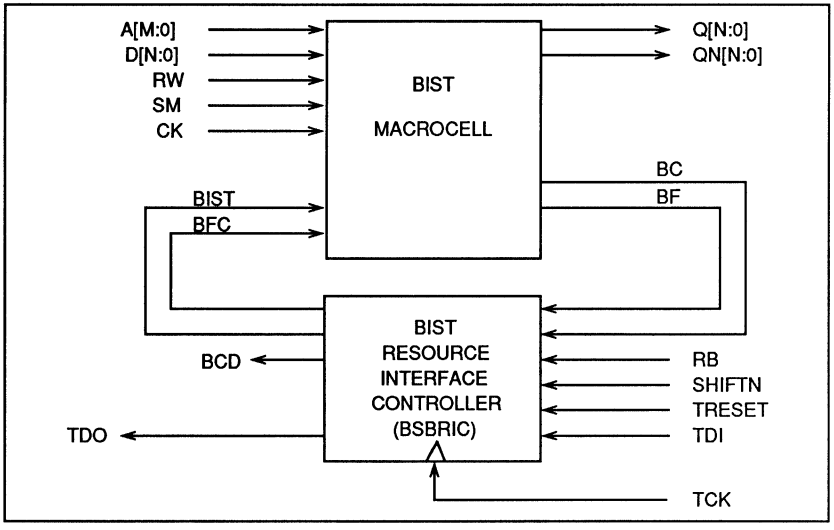
86 grids, 132 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

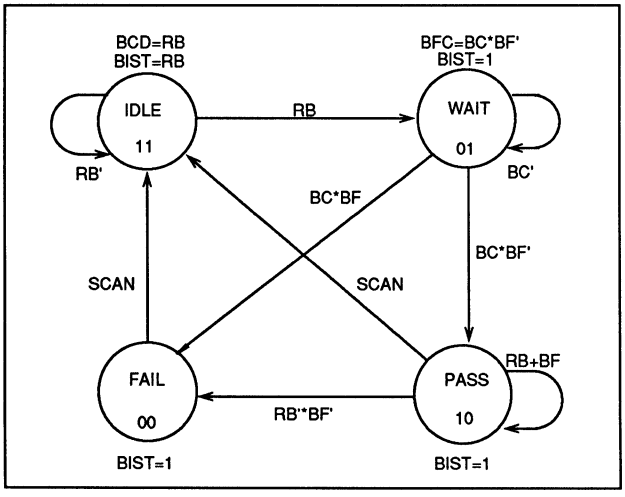
BSBRIC is a JTAG compatible circuit.

- Uses the JTAG boundary scan protocol to actuate the built-in self-test features of the AT&T BIST Macrocell and then to shift out the results over the boundary scan output pin
- BSBRIC forms a 2-bit user test data register which is connected in parallel with the B-S register and bypass register.

BLOCK DIAGRAM



STATE DIAGRAM



12

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: TDI,TCK,SHIFTN,RB,BC,BF,TRESET
OUTPUTS: BCD,BFC,BIST,TDO

Functional Descriptions

Inputs:

TDI	Serial test data input
TCK	Boundary scan test clock also used for BIST MACROCELL
SHIFTN	Shift out results (active-low); Derived from BSTAP controller
RB	Start BIST command input
BC	BIST complete from BIST MACROCELL
BF	BIST flag from BIST MACROCELL indicating PASS/FAIL
TRESET	Asynchronous reset command from BSTAP

Outputs:

BCD	BIST clear (Not used for 0.9µ Macrocells)
BFC	BIST flag check to BIST MACROCELL, high checks for BF stuck at 0
BIST	BIST test mode to BIST MACROCELL
TDO	Serial test data output (to next boundary scan cell)

CHARACTERISTICS

SWITCHING CHARACTERISTICS
VDD=5.0V, T=25°C, Nominal Processing

From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
TCK↑	BCD↓	3.66	1.98	2.74	0.53
TCK↑	BCD↑	5.09	3.24	3.26	0.66
TCK↑	BFC↓	5.14	1.98	4.11	0.53
TCK↑	BFC↑	8.34	3.17	5.94	0.70
TCK↑	BIST↓	7.77	2.05	4.46	0.58
TCK↑	BIST↑	8.74	3.24	5.83	0.70
TCK↑	TDO↓	0.69	2.18	1.60	0.62
TCK↑	TDO↑	0.80	3.24	1.37	0.70

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area Value	Perf. Value	Unit
Minimum TDI Setup before TCK↑	2.4	1.4	ns
Minimum SHIFTN Setup before TCK↑	2.4	1.4	
Minimum RB Setup before TCK↑	5.2	2.6	
Minimum BC Setup before TCK↑	5.0	2.5	
Minimum BF Setup before TCK↑	5.1	2.5	
Minimum TRESET Setup before TCK↑	2.4	1.4	

System/Test Clock Multiplexer BSCKMUX

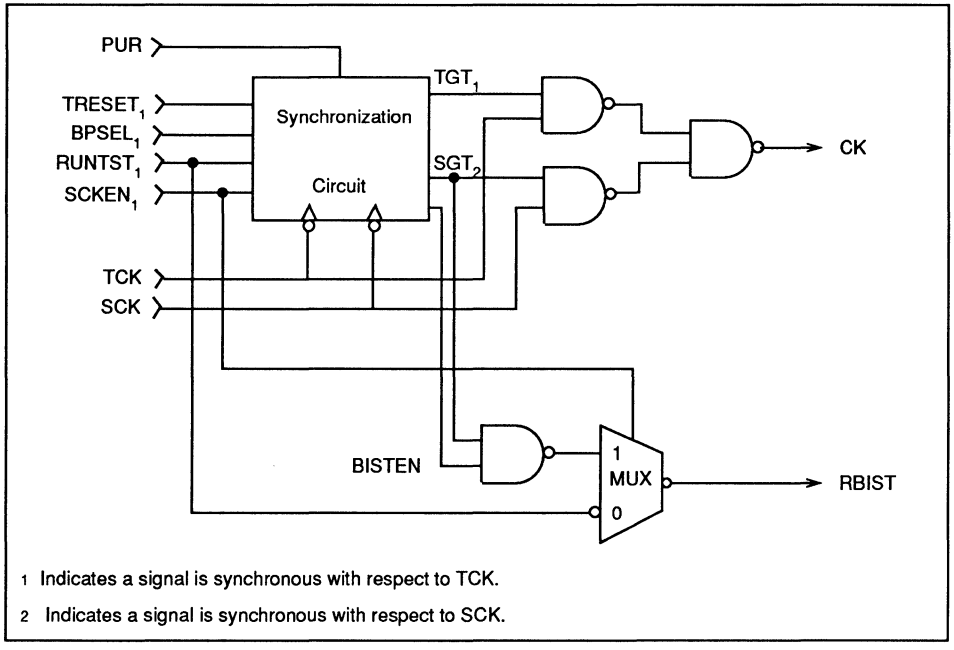
118 grids,168 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSCKMUX is a system/test clock multiplexer for chip designs with boundary scan. It features:

- Two synchronizing D-type FFs are used for each input clock gating signal (SGT or TGT) to help ensure metastable-free multiplexing.
- A Run BIST (RBIST) signal which assures synchronous activation of built-in self-test (e.g. BILBO; circular BIST) by the BSTAP. Note that when BIST runs on TCK (SCK), RBIST is simply driven by the RUNTST (SGT) signal, assuring its synchronization with respect to BSCKMUX output clock (CK).
- Input clock waveform duty-cycle is maintained by using multiplexing NAND gates which provide equivalent delay paths for both the rising and falling edges.

BLOCK DIAGRAM



1 Indicates a signal is synchronous with respect to TCK.

2 Indicates a signal is synchronous with respect to SCK.

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System/Test Clock Switching Conditions

CK Outputs	Conditions
SCK	1. TAP is in Test-Logic-Reset state (TRESET = 1), or 2. Bypass path is selected by an instruction in IR (BPSEL = 1), or 3. TAP is in Run-Test/Idle state AND system clock is enabled by an instruction in IR (RUNTST = SCKEN = 1) [NOTE: RBIST, synchronous with respect to SCK, is asserted if RUNTST = 1]
TCK	1. TRESET = BPSEL = RUNTST = 0, or 2. TRESET = BPSEL = SCKEN = 0 [NOTE: RBIST, synchronous with respect to TCK, is asserted if RUNTST = 1]

TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: SCK,TCK,TRESET,RUNTST,SCKEN,BPSEL,PUR
OUTPUTS: CK,RBIST

FUNCTIONAL DESCRIPTIONS

Inputs:

SCK	System clock to be multiplexed
TCK	Test clock to be multiplexed
TRESET	Test-logic reset signal Derived from BSTAP
RUNTST	Run-test signal Derived from BSTAP
SCKEN	Enable system clock (during BIST); decoded from B-S IR
BPSEL	Bypass path select signal; decoded from BSIR
[NOTE: SCK is always selected in bypass mode according to JTAG spec.]	
PUR	Power-Up Reset (e.g. from PUR40U); preset TRESET high

Outputs:

CK	Hazard-free clock signal (driven by SCK or TCK)
RBIST	Synchronized control signal for activating BIST; issued on falling edge of CK

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
TCK,SCK↓	CK↓	0.80	4.10	0.29	1.07
TCK,SCK↓	CK↑	0.74	3.24	0.40	0.66
SCK↓	RBIST↓	2.86	0.86	2.74	0.21
SCK↓	RBIST↑	3.60	0.86	3.26	0.21
TCK↑	RBIST↓	5.83	0.86	4.23	0.21
TCK↑	RBIST↑	7.31	0.86	5.43	0.21
RUNTST	RBIST↓	2.57	0.86	1.31	0.21
RUNTST	RBIST↑	2.06	0.86	1.14	0.21
SCKEN	RBIST↓	2.69	0.86	1.43	0.21
SCKEN	RBIST↑	2.86	0.86	1.54	0.21
PUR↓	CK↓	5.21	4.10	2.74	1.07
PUR↓	CK↑	8.74	3.24	4.42	0.66

Since BSCKMUX operates asynchronously, specification of setup times is meaningless here.

B-S Bidirectional Control Cell BSDC

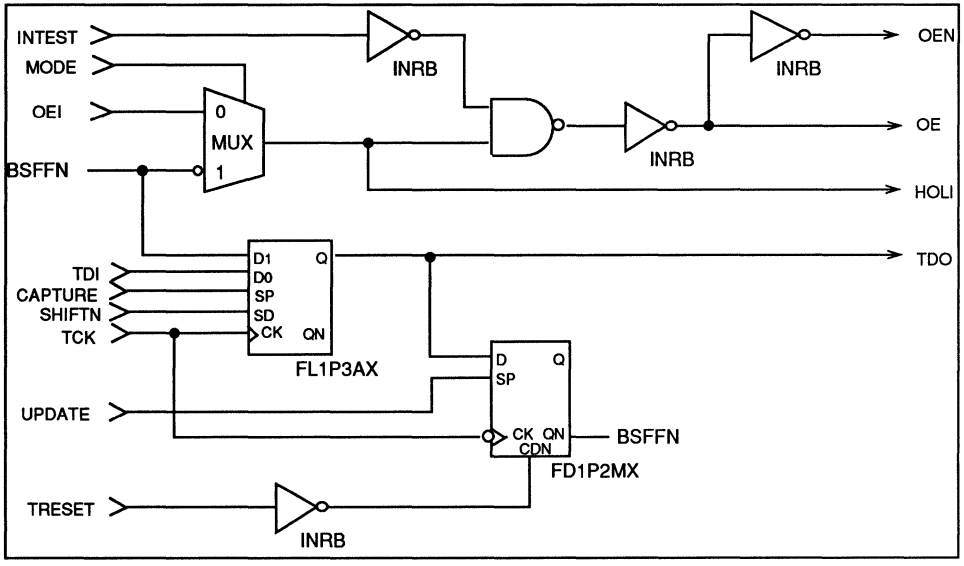
64 grids, 90 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSDC is a JTAG compatible, boundary scan, bidirectional control cell.

- Shift register with capture for controlling the 3-state buffer in a bidirectional pin
- Bidirectional pin configured as input, (OE=0), during internal mode

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: CAPTURE,INTEST,MODE,OEI,SHIFTN,TCK,TDI,TRESET,UPDATE

OUTPUTS: HOLI,OE,OEN,TDO

Functional Descriptions

Inputs:

CAPTURE	Capture/load scan register; Derived from BSTAP controller
INTEST	Internal test signal; Asserted during INTEST instruction
MODE	Input/output mode, control asserted in Internal or External mode
OEI	Output enable input signal, deployed in normal/system mode
SHIFTN	Shift scan-register, active low; Derived from BSTAP controller
TCK	Boundary scan test clock
TDI	Serial test data input, (from previous boundary scan cell)
TRESET	Test logic reset signal; Derived from BSTAP controller
UPDATE	Update parallel output register; Derived from BSTAP controller

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B-S Bidirectional Control Cell BSDC

Outputs:

HOLI	Direction control signal to BSBD cell; (High = output, Low = input)
OE	Output Enable signal to 3-state buffer
OEN	Negated output signal to 3-state buffer
TDO	Serial test data output (to next boundary scan cell)

CHARACTERISTICS

SWITCHING CHARACTERISTICS
VDD=5.0V, T=25°C, Nominal Processing

From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
TCK↓	OE↓	3.31	2.31	0.58	1.07
TCK↓	OE↑	3.94	3.24	0.70	1.36
TCK↓	OEN↓	4.17	2.31	0.58	1.07
TCK↓	OEN↑	3.43	3.24	0.70	1.36
TCK↑	TDO↓	2.46	7.93	2.34	1.73
TCK↑	TDO↑	2.34	5.81	2.51	1.44
OEI	OEN↓	3.26	2.31	0.58	0.53
OEI	OEN↑	2.57	3.24	0.70	1.03
MODE	OE↓	2.46	2.31	0.58	0.53
MODE	OE↑	3.03	3.24	0.70	1.36
MODE	OEN↓	3.26	2.31	0.58	0.53
MODE	OEN↑	2.57	3.24	0.70	1.36
MODE	HOLI↓	1.09	4.03	0.57	1.07
MODE	HOLI↑	1.09	6.47	0.51	1.36

Timing Requirements
VDD=5.0V, T=25°C, Nominal Processing

Description	Area Value	Perf. Value	Unit
Minimum TRESET Setup before TCK↑	2.6	1.8	ns
Minimum TDI Setup before TCK↑	3.2	1.7	
Minimum OEI Setup before TCK↑	3.2	1.7	
Minimum CAPTURE Setup before TCK↑	3.2	1.7	
Minimum SHIFTN Setup before TCK↑	3.2	1.7	
Minimum UPDATE Setup before TCK↓	2.2	1.6	

B-S Input 1 BSIN1

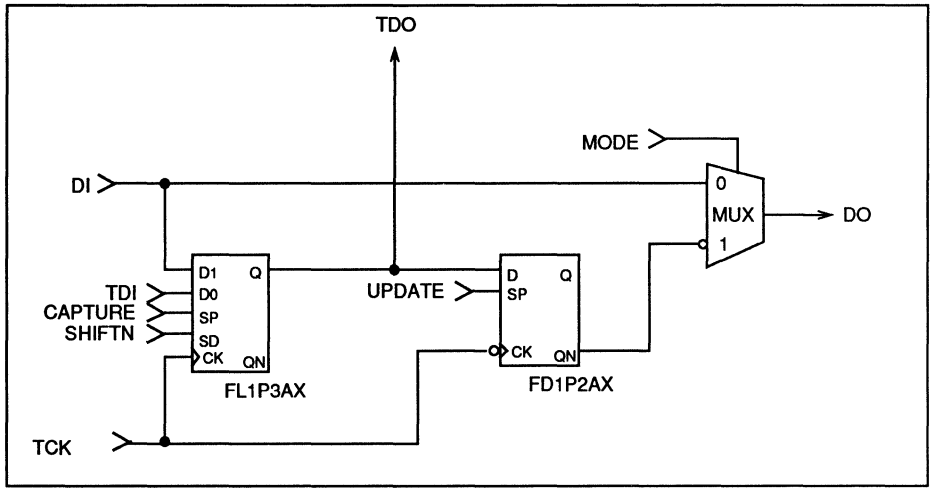
51 grids, 72 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSIN1 is a JTAG compatible, boundary scan input cell.

- Standard boundary scan input cell with input-pin signal controllable by the update register
- Chip logic shielded from disturbances during boundary scan external test, (by setting MODE=1)
- Totally synchronous operation

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: DI,TDI,TCK,MODE,CAPTURE,SHIFTN,UPDATE

OUTPUTS: DO,TDO

Functional Descriptions

Inputs:

DI	Normal input from chip input pad
TDI	Serial test data input (from previous boundary scan cell)
TCK	Boundary scan test clock
MODE	Input-mode control (asserted in Internal or External Mode)
CAPTURE	Capture/ load scan-register; Derived from BSTAP controller
SHIFTN	Shift scan-register (active-low); Derived from BSTAP controller
UPDATE	Update parallel output register; Derived from BSTAP controller

Outputs:

DO	Output from boundary scan input cell; drives normal input or scanned input to chip internal circuitry when MODE = 0
TDO	Serial test data output (to next boundary scan cell)

B-S Input 1 BSIN1

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
DI	DO↓	0.57	1.98	0.40	0.53
DI	DO↑	0.29	4.82	0.23	1.43
TCK↓	DO↓	1.43	4.03	1.54	1.07
TCK↓	DO↑	1.09	6.41	1.31	1.36
TCK↑	TDO↓	2.40	7.93	2.17	1.73
TCK↑	TDO↑	2.23	5.81	2.34	1.44
MODE	DO↓	0.57	4.03	0.40	1.07
MODE	DO↑	0.29	6.47	0.23	1.36

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area Value	Perf. Value	Unit
Minimum DI Setup before TCK↑	3.2	1.7	ns
Minimum TDI Setup before TCK↑	3.2	1.7	
Minimum UPDATE Setup before TCK↓	1.9	1.3	
Minimum CAPTURE Setup before TCK↑	3.2	1.7	
Minimum SHIFTN Setup before TCK↑	3.2	1.7	

B-S Input 2 BSIN2

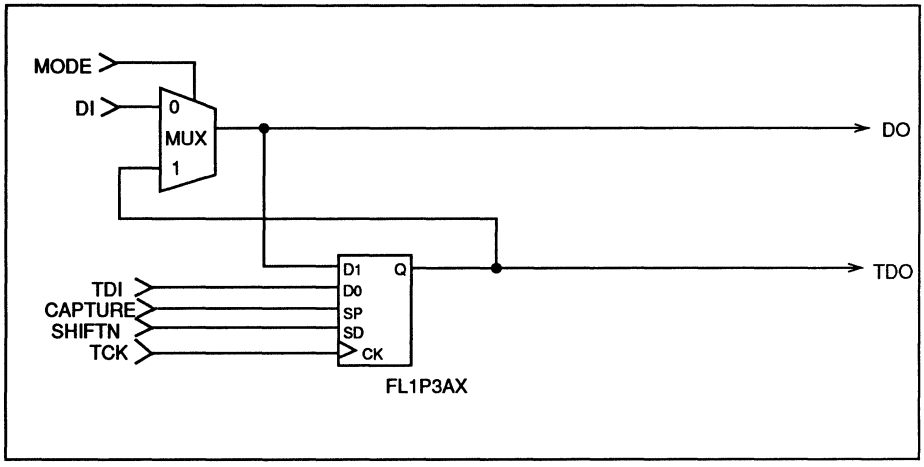
32 grids, 46 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSIN2 is a JTAG compatible, boundary scan input cell.

- Boundary scan input cell without "update" register
- Totally synchronous operation

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: DI,TDI,TCK,MODE,CAPTURE,SHIFTN

OUTPUTS: DO,TDO

Functional Descriptions

Inputs:

DI	Normal input from chip-input pad
TDI	Serial test data input (from previous boundary scan cell)
TCK	Boundary scan test clock
MODE	Input-mode control (asserted in Internal or External Mode)
CAPTURE	Capture/load scan-register; Derived from BSTAP controller
SHIFTN	Shift scan-register (active-low); Derived from BSTAP controller

Outputs:

DO	Output from boundary scan input cell; drives normal input or scanned input to chip internal circuitry when MODE = 0
TDO	Serial test data output (to next boundary scan cell)

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CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
DI	DO↓	1.03	1.98	0.51	0.53
DI	DO↑	1.03	4.82	0.51	1.43
TCK↑	DO↓	2.51	4.03	2.34	1.07
TCK↑	DO↑	2.11	6.41	2.00	1.36
TCK↑	TDO↓	2.46	7.93	2.29	1.73
TCK↑	TDO↑	2.06	5.81	2.40	1.44
MODE	DO↓	1.03	4.03	0.51	1.07
MODE	DO↑	1.03	6.47	0.51	1.36

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area Value	Perf. Value	Unit
Minimum DI Setup before TCK↑	4.2	2.2	ns
Minimum TDI Setup before TCK↑	3.2	1.7	
Minimum MODE Setup before TCK↑	4.2	2.2	
Minimum CAPTURE Setup before TCK↑	3.2	1.7	
Minimum SHIFTN Setup before TCK↑	3.2	1.7	

B-S Input 3 BSIN3

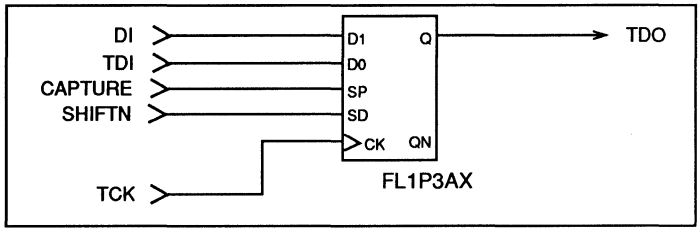
26 grids, 36 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSIN3 is a JTAG compatible, boundary scan input cell, used only for clock or critical input pins.

- Boundary scan input cell without "update" output latch; JTAG "External" and "Sample" mode are supported
- Totally synchronous operation

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: DI,TDI,TCK,CAPTURE,SHIFTN

OUTPUT: TDO

Functional Descriptions

Inputs:

DI	Normal input from chip-input pad
TDI	Serial test data input (from previous boundary scan cell)
TCK	Boundary scan test clock
CAPTURE	Capture/load-scan register; Derived from BSTAP controller
SHIFTN	Shift scan-register (active-low); Derived from BSTAP controller

Output:

TDO	Serial test data output (to next boundary scan cell)

CHARACTERISTICS

SWITCHING CHARACTERISTICS
VDD=5.0V, T=25°C, Nominal Processing

From Input	To Output	Area		Performance	
		Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
TCK↑	TDO↓	1.54	7.93	1.54	1.73
TCK↑	TDO↑	1.31	5.81	1.66	1.44

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B-S Input 3

BSIN3

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area Value	Perf. Value	Unit
Minimum DI Setup before TCK↑	3.2	1.7	ns
Minimum TDI Setup before TCK↑	3.2	1.7	
Minimum CAPTURE Setup before TCK↑	3.2	1.7	
Minimum SHIFTN Setup before TCK↑	3.2	1.7	

B-S Instruction Register 1 BSIR

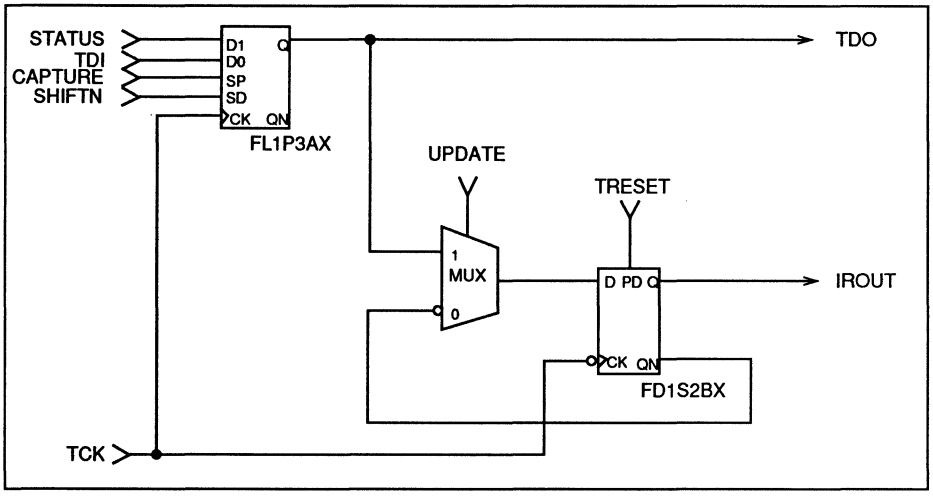
48 grids, 68 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSIR is a JTAG compatible, boundary scan instruction register.

- Output flip-flop preset by TRESET signal
- Fault isolation of the board-level, serial test data path is supported. A constant '01' pattern must be loaded into the two least significant bits of the instruction register at the start of the instruction scan cycle.
- Includes shift register and parallel output register
- Instruction register with status input during capture

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: STATUS,TDI,TCK,TRESET,CAPTURE,SHIFTN,UPDATE
OUTPUTS: IROUT,TDO

Functional Descriptions

Inputs:

STATUS	Status data to be loaded with IR capture
TDI	Serial test data input (from previous boundary scan IR cell)
TCK	Boundary scan test clock
TRESET	Test-logic-preset signal from BSTAP controller
CAPTURE	Capture/load scan-register; Derived from BSTAP controller
SHIFTN	Shift scan-register (active-low); Derived from BSTAP controller
UPDATE	Update parallel output register; Derived from BSTAP controller

Outputs:

IROUT	Output from instruction register
TDO	Serial test data output (to next boundary scan IR cell)

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CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
TCK↓	IROUT↓	0.06	2.11	0.17	0.58
TCK↓	IROUT↑	0.06	3.17	0.11	0.70
TCK↑	TDO↓	2.46	7.93	2.34	1.73
TCK↑	TDO↑	2.29	5.81	2.51	1.44

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area Value	Perf. Value	Unit
Minimum STATUS Setup before TCK↑	3.2	1.7	ns
Minimum TDI Setup before TCK↑	3.2	1.7	
Minimum TRESET Setup before TCK↓	1.4	0.8	
Minimum CAPTURE Setup before TCK↑	3.2	1.7	
Minimum SHIFTN Setup before TCK↑	3.2	1.7	
Minimum UPDATE Setup before TCK↓	2.3	1.2	

B-S Instruction Register 1 BSIRN

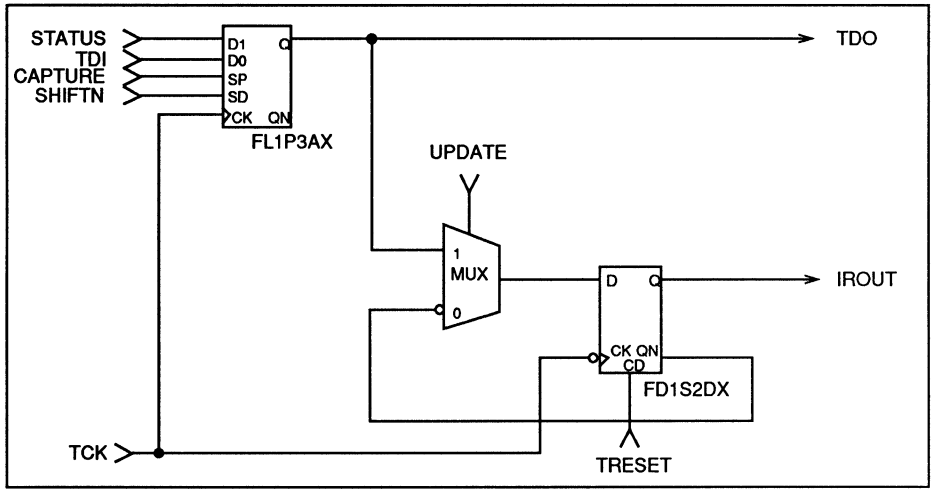
49 grids, 70 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSIRN is a JTAG compatible, boundary scan instruction register.

- Output flip-flop cleared by TRESET signal
- Fault isolation of the board-level serial test data path is supported. A constant '01' pattern must be loaded into the 2 least significant bits of the instruction register at the start of the instruction scan cycle.
- Includes shift register and parallel output register
- Instruction register with status input during capture

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: STATUS,TDI,TCK,TRESET,CAPTURE,SHIFTN,UPDATE
OUTPUTS: IROUT,TDO

Functional Descriptions

Inputs:

STATUS	Status data to be loaded with IR capture
TDI	Serial test data input (from previous boundary scan IR cell)
TCK	Boundary scan test clock
TRESET	Test-logic-reset signal from BSTAP controller
CAPTURE	Capture/load scan-register; Derived from BSTAP controller
SHIFTN	Shift scan-register (active low); Derived from BSTAP controller
UPDATE	Update parallel output register; Derived from BSTAP controller

Outputs:

IROUT	Output from instruction register
TDO	Serial test data output (to next boundary scan IR cell)

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B-S Instruction Register 1 BSIRN

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
TCK↑	IROUT↓	1.66	7.93	1.43	1.73
TCK↑	IROUT↑	1.60	8.85	1.71	2.05
TCK↑	TDO↓	2.46	7.93	2.34	1.73
TCK↑	TDO↑	2.29	5.81	2.51	1.44

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area Value	Perf. Value	Unit
Minimum TDI Setup before TCK↑	3.2	1.7	ns
Minimum TRESET Setup before TCK↓	1.7	1.0	
Minimum SHIFTN Setup before TCK↑	3.2	1.7	
Minimum UPDATE Setup before TCK↓	2.7	1.4	

B-S Output Enable Control BSOE

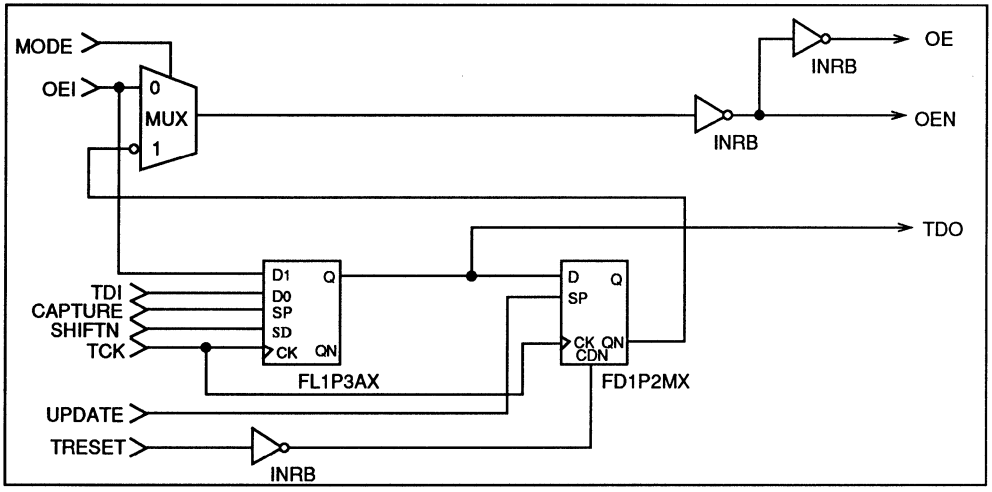
59 grids, 84 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSOE is a JTAG compatible, boundary scan, output-enable control cell

- Shift register with capture for controlling the 3-state output pin

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: OEI,TDI,TCK,TRESET,MODE,CAPTURE,SHIFTN,UPDATE
OUTPUTS: OE,OEN,TDO

Functional Descriptions

Inputs:

OEI	Output-enable input signal (deployed in normal/system mode)
TDI	Serial test data input (from previous boundary scan cell)
TCK	Boundary scan test clock
TRESET	Test-logic-reset signal; Derived from BSTAP controller
MODE	Output-mode control (asserted in Internal or External Mode)
CAPTURE	Capture/load scan-register; Derived from BSTAP controller
SHIFTN	Shift scan-register (active low); Derived from BSTAP controller
UPDATE	Update parallel output register; Derived from BSTAP controller

Outputs

OE	Output-enable signal to 3-state buffer
OEN	Negated output enable to 3-state buffer
TDO	Serial test data output (to next boundary scan cell)

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B-S Output Enable Control

BSOE

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
OEI	OE↓	2.00	2.31	0.97	0.58
OEI	OE↑	2.23	3.24	1.03	0.70
OEI	OEN↓	2.11	2.31	0.91	0.58
OEI	OEN↑	1.77	3.24	0.86	0.70
TCK↑	TDO↓	2.46	7.93	2.34	1.73
TCK↑	TDO↑	2.34	5.81	2.51	1.44
TCK↓	OE↓	2.86	2.31	2.11	0.58
TCK↓	OE↑	3.14	3.24	1.89	0.70
TCK↓	OEN↓	3.03	2.31	1.77	0.58
TCK↓	OEN↑	2.63	3.24	2.00	0.70
MODE	OEN↓	2.11	2.31	0.91	0.58
MODE	OEN↑	1.77	3.24	0.86	0.70
MODE	OE↓	2.00	2.31	0.97	0.58
MODE	OE↑	2.23	3.24	1.03	0.70

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area Value	Perf. Value	Unit
Minimum OEI Setup before TCK↑	3.2	1.7	ns
Minimum TDI Setup before TCK↑	3.2	1.7	
Minimum TRESET Setup before TCK↓	2.6	1.8	
Minimum CAPTURE Setup before TCK↑	3.2	1.7	
Minimum SHIFTN Setup before TCK↑	3.2	1.7	
Minimum UPDATE Setup before TCK↓	2.2	1.6	

B-S Output BSOUT

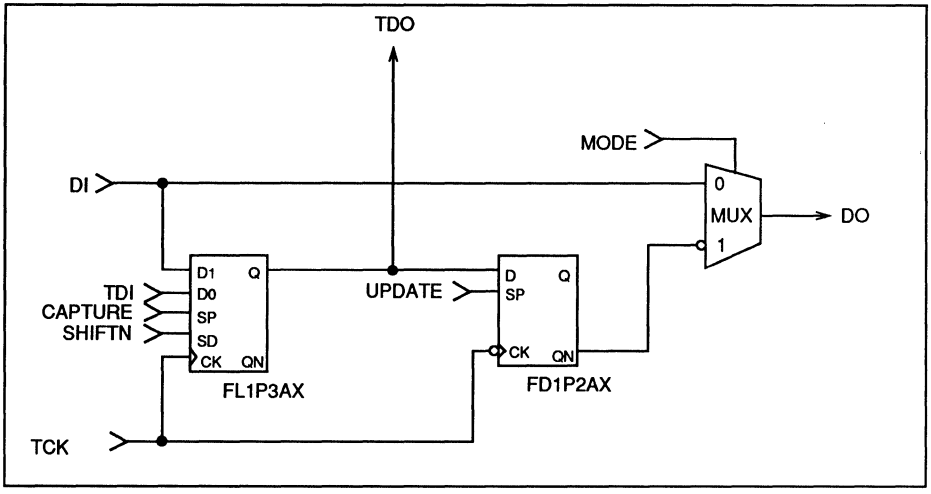
51 grids, 72 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSOUT is a JTAG compatible, boundary scan output cell.

- Standard boundary scan output cell with output pin controllable by update register
- Shield outside circuitry from disturbances during boundary scan Internal Test (by setting MODE=1).

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: DI,TDI,TCK,MODE,CAPTURE,SHIFTN,UPDATE
OUTPUTS: DO,TDO

Functional Descriptions

Inputs:

DI	Input from chip internal circuitry
TDI	Serial test data input (from previous boundary scan cell)
TCK	Boundary scan test clock
MODE	Output-mode control (asserted in Internal or External Mode)
CAPTURE	Capture/load scan-register; Derived from BSTAP controller
SHIFTN	Shift scan-register (active low); Derived from BSTAP controller
UPDATE	Update parallel output register; Derived from BSTAP controller

Outputs:

DO	Output to normal chip-output pad
TDO	Serial test data output (to next boundary scan cell)

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
DI	DO↓	0.57	1.93	0.40	0.53
DI	DO↑	0.29	4.82	0.23	1.03
TCK↓	DO↓	1.43	4.03	1.54	1.07
TCK↓	DO↑	1.09	6.41	1.31	1.36
TCK↑	TDO↓	2.40	7.93	2.17	1.73
TCK↑	TDO↑	2.23	5.81	2.34	1.44
MODE	DO↓	0.57	4.03	0.40	1.07
MODE	DO↑	0.29	6.47	0.23	1.36

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area Value	Perf. Value	Unit
Minimum DI Setup before TCK↑	3.2	1.7	ns
Minimum TDI Setup before TCK↑	3.2	1.7	
Minimum MODE Setup before TCK↑	3.2	1.7	
Minimum CAPTURE Setup before TCK↑	3.2	1.7	
Minimum SHIFTN Setup before TCK↑	3.2	1.7	
Minimum UPDATE Setup before TCK↓	1.9	1.3	

Test Access Port Controller BSTAP

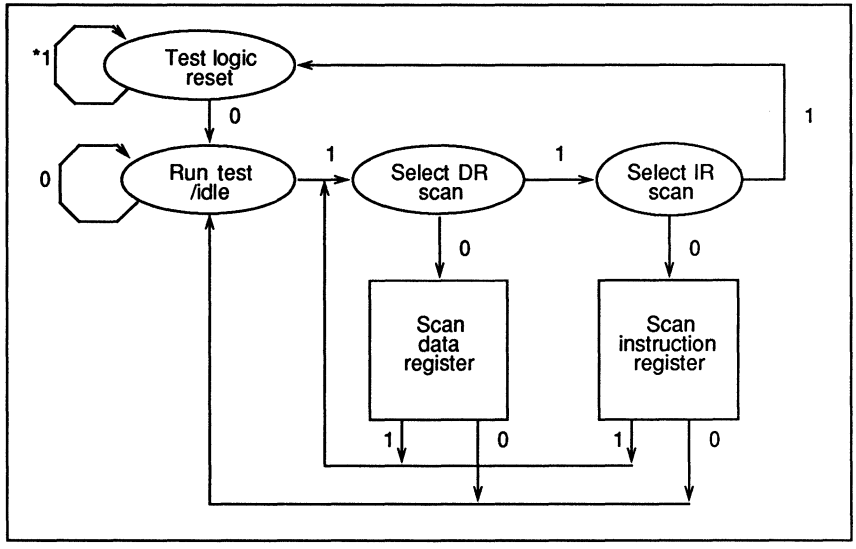
227 grids, 342 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSTAP is a P1149.1 compatible, test access port (BSTAP) controller. State assignments used are from JTAG specifications. All control signals are issued on the rising edge of TCK, except ENABLE, which changes on the falling edge. This is to conform to the JTAG requirement that TDO should be updated on the falling edge of TCK. SELECT signal is asserted in RESET and RUNTEST states to reduce logic. The following features of BSTAP contribute to the viability of P1149.1 as an international standard.

- A fixed set of pins: Test Data Input (TDI), Test Data Output (TDO), Test Mode Select (TMS), Test Clock (TCK), and an optional asynchronous reset pin for initializing test logic upon power up.
- A well-defined protocol ensuring inter-operability among all B-S equipped devices from different vendors.
- A set of internal control signals which separate a single serial bit stream (applied on TDI) into test data and test instructions. This provides great design flexibility to the chip designer.
- A unified scan mechanism for controlling and accessing on-chip BIST structures.

MAIN STATE DIAGRAM



* The logic value adjacent to a state-transition arc corresponds to the value of TMS.

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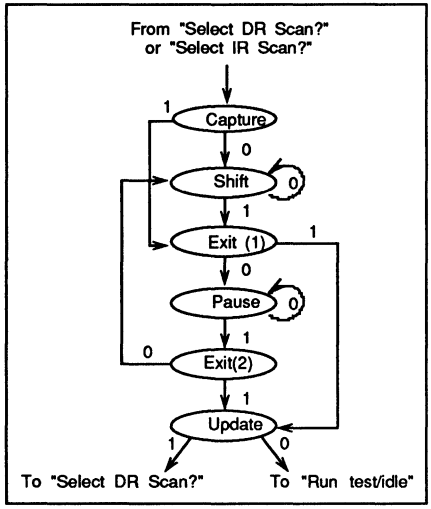
SCAN STATE DIAGRAM



Function Table

STATE	State Assignment (HEX)	Control Signals Asserted
RESET	(F)	TRESET, SELECT
RUNTEST	(3)	RUNTST, SELECT
SCAN DR	(E)	N/A *
CAPTURE DR	(6)	CAPTUREDR
SHIFT DR	(4)	SHIFTDR, ENABLE
EXIT1 DR	(8)	N/A *
UPDATE DR	(A)	UPDATEDR
EXIT2 DR	(0)	N/A *
PAUSE DR	(C)	N/A *
SCAN IR	(2)	N/A *
CAPTURE IR	(7)	CAPTUREIR, SELECT
SHIFT IR	(5)	SHIFTIR, ENABLE, SELECT
EXIT1 IR	(9)	SELECT
UPDATE IR	(B)	UPDATEIR, SELECT
EXIT2 IR	(1)	SELECT
PAUSE IR	(D)	SELECT

* Not Applicable, no control signals asserted.

TERMINAL DESCRIPTION

Netlist Order

Inputs: TMS, TCK, PUR

Outputs: TRESET, RUNTST, SELECT, ENABLE, CAPTUREDR, CAPTUREIR, SHIFTDR,SHIFTIR, UPDATEDR, UPDATEIR

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FUNCTIONAL DESCRIPTIONS

Inputs:

TMS	Test- mode Select
TCK	Test clock
PUR	Power Up Reset (e.g., from PUR40U) forces TRESET high

Outputs:

TRESET	Test-logic reset
RUNTST	Run test (start internal BIST tests)
SELECT	HI: select IR; LO: select DR
ENABLE	Test data output pin (TDO) enable; issued on falling TCK
CAPTUREDR	Capture/parallel load DR
CAPTUREIR	Capture/parallel load IR
SHIFTDR	Shift DR
SHIFTIR	Shift IR
UPDATEDR	Update/parallel load DR output buffer FFs
UPDATEIR	Update/parallel load IR output buffer FFs

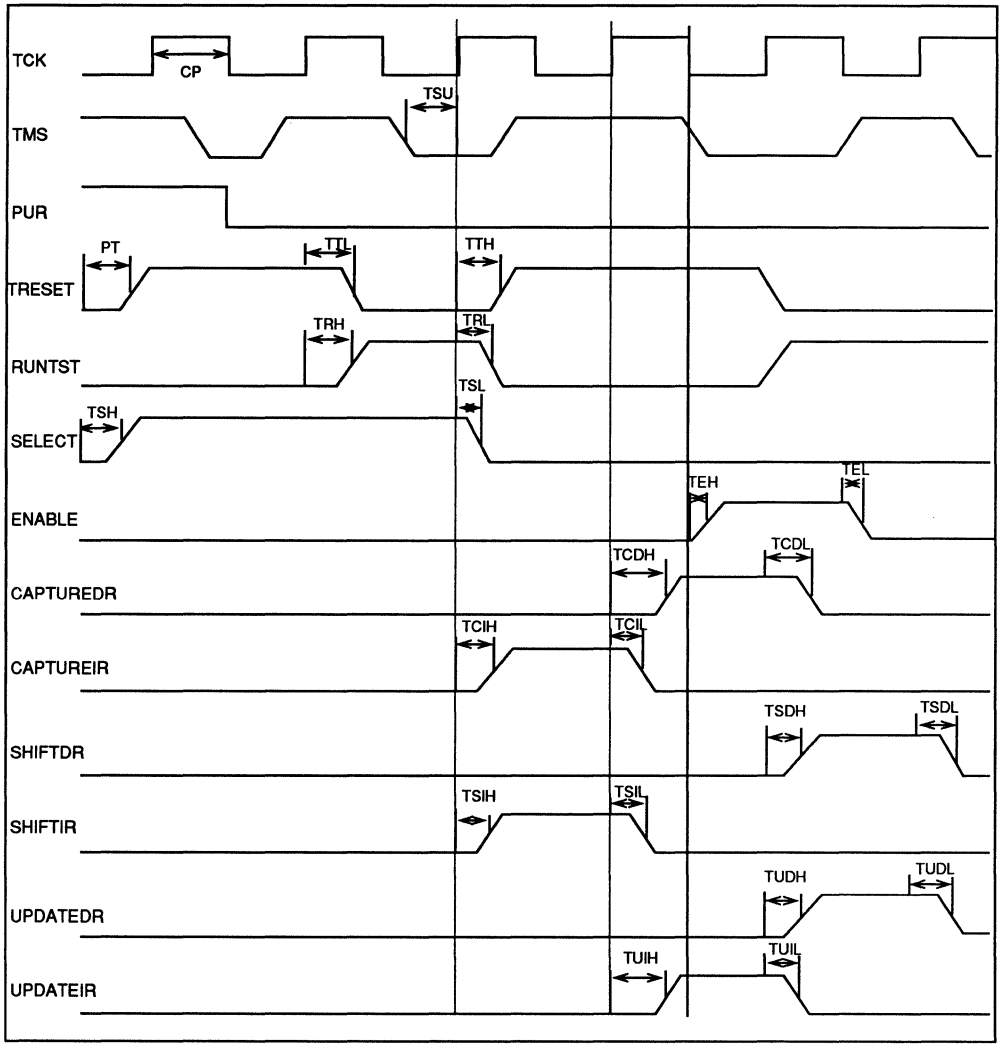
CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing						
Symbol	From Input	To Output	Area		Performance	
			Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
TTL	TCK↑	TRESET↓	2.51	1.98	2.86	0.58
TTH	TCK↑	TRESET↑	3.20	12.9	3.54	2.75
TRL	TCK↑	RUNTST↓	3.94	1.98	3.66	0.58
TRH	TCK↑	RUNTST↑	3.89	12.9	3.54	2.75
TSL	TCK↑	SELECT↓	2.46	2.31	2.80	0.58
TSH	TCK↑	SELECT↑	2.80	3.24	3.31	0.70
TEL	TCK↓	ENABLE↓	0.06	1.98	0.17	0.58
TEH	TCK↓	ENABLE↑	0.06	3.24	0.17	0.70
TCDL	TCK↑	CAPTUREDR↓	3.83	1.98	3.71	0.58
TCDH	TCK↑	CAPTUREDR↑	3.71	12.9	3.54	2.75
TCIL	TCK↑	CAPTUREIR↓	3.83	1.98	3.60	0.58
TCIH	TCK↑	CAPTUREIR↑	3.71	12.9	3.54	2.75
TSDL	TCK↑	SHIFTDR↓	4.11	1.98	3.83	0.58
TSDH	TCK↑	SHIFTDR↑	4.11	12.9	3.49	2.75
TSIL	TCK↑	SHIFTIR↓	4.11	1.98	3.83	0.58
TSIH	TCK↑	SHIFTIR↑	4.06	12.9	3.54	2.75
TUDL	TCK↑	UPDATEDR↓	3.94	1.98	3.71	0.58
TUDH	TCK↑	UPDATEDR↑	3.89	12.9	3.54	2.75
TUIL	TCK↑	UPDATEIR↓	3.94	1.98	3.66	0.58
TUIH	TCK↑	UPDATEIR↑	3.89	12.9	3.54	2.75
PT	PUR↑	TRESET↑	3.20	17.0	3.54	2.89

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing				
Symbol	Description	Area Value	Perf. Value	Unit
TSU	Minimum TMS Setup before TCK↑	5.1	2.3	ns
CP	Minimum Clock Pulse High [1]	5.9	4.7	

1 50% duty cycle required by JTAG

TIMING DIAGRAM



12

B-S Serial Output Cell BSTDO

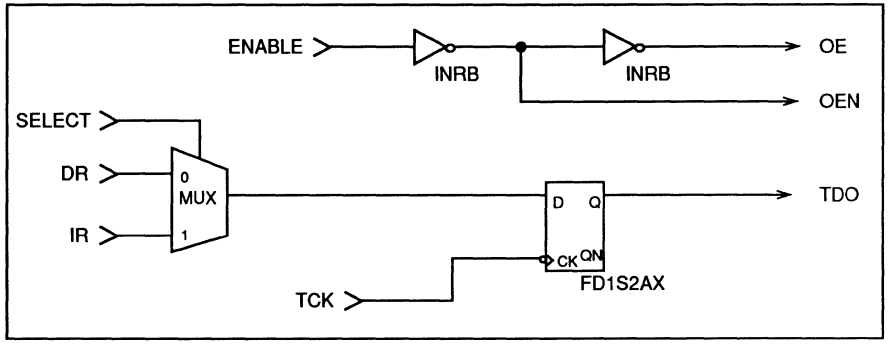
24 grids, 34 transistors

FUNCTIONAL DESCRIPTION AND FEATURES

BSTDO is a JTAG compatible, TDO, output buffer cell.

- Generates TDO signal on the falling edge of TCK according to JTAG specifications
- Contains an input MUX for selecting the LSB of either the Data register or the Instruction register as serial output
- Generates the 3-state buffer control signal for TDO
- Used with standard tri-state output buffer

BLOCK DIAGRAM



TERMINAL DESCRIPTIONS

Netlist Order

INPUTS: DR,IR,TCK,SELECT,ENABLE
OUTPUTS: OE,OEN,TDO

Functional Descriptions

Inputs:

DR	LSB of a data register
IR	LSB of the instruction register
TCK	Boundary scan test clock
SELECT	Select (IR) signal; Directly from BSTAP controller
ENABLE	Enable (TDO) signal; Directly from BSTAP controller

Outputs:

OE	Output-enable signal (to TDO 3-state buffer)
OEN	Negated output-enable signal (to TDO 3-state buffer)
TDO	Serial test data output (to TDO output pad)

CHARACTERISTICS

SWITCHING CHARACTERISTICS VDD=5.0V, T=25°C, Nominal Processing					
From	To	Area		Performance	
Input	Output	Intrinsic (ns)	Extrinsic (ns/pF)	Intrinsic (ns)	Extrinsic (ns/pF)
TCK↓	TDO↓	0.06	1.98	0.17	0.58
TCK↓	TDO↑	0.06	3.24	0.17	0.70
ENABLE	OE↓	0.69	2.31	0.29	0.58
ENABLE	OE↑	0.40	3.24	0.23	0.70
ENABLE	OEN↓	0.29	2.31	0.11	0.58
ENABLE	OEN↑	0.46	3.24	0.17	0.70

Timing Requirements VDD=5.0V, T=25°C, Nominal Processing			
Description	Area Value	Perf. Value	Unit
Minimum DR Setup before TCK↓	2.3	1.3	ns
Minimum IR Setup before TCK↑	2.3	1.3	
Minimum SELECT Setup before TCK↑	2.5	1.5	

Numerics

A

B

C

D

E

F

G

H

I

J

L

M

U

W

X

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