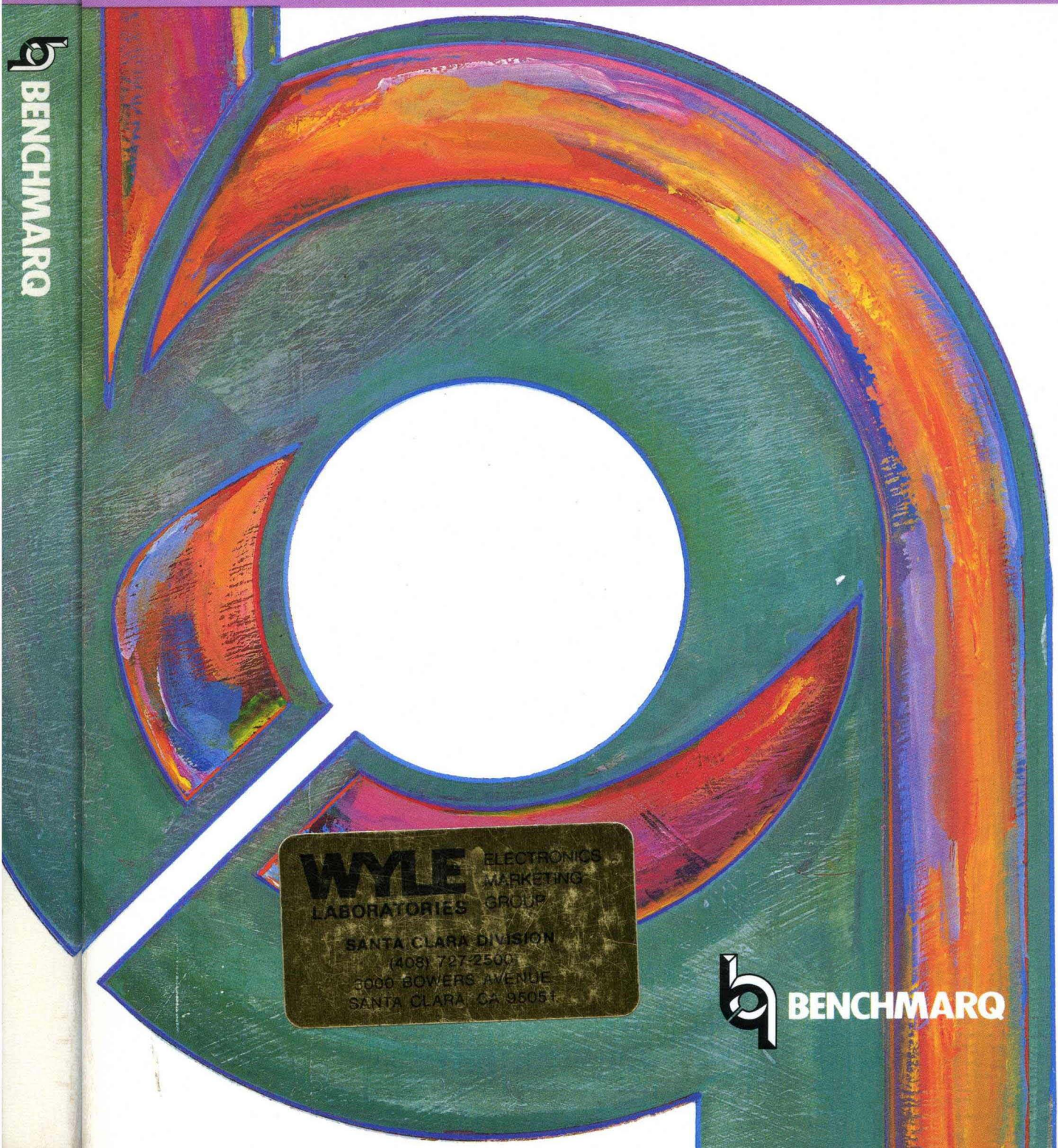
90/91
DATA BOOK

BENCHMARQ

1990 1991 DATA BOOK



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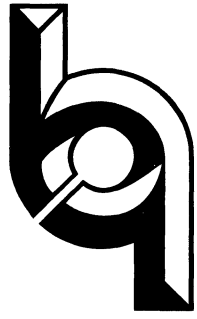

BENCHMARQ

1990/91
Data Book

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Benchmarq 1990/91 Data Book

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About Benchmarq

Our Products

At Benchmarq, we provide integrated ciruit and module solutions for power-sensitive and portable electronic systems.

Power-sensitive AC-powered systems in the office and industry must gracefully deal with the loss of power, maintaining the integrity of important data and selfsufficiently continuing critical operation. Portable systems share the design requirements of their powercord-bound counterparts, but add entirely new challenges—including power supervision, energy management, data security, and size minimization.

The product families described in this data book directly address these requirements, taking full advantage of advanced analog and digital VLSI technologies and state-of-the-art battery and packaging expertise. Power supervision, energy management, size reduction, nonvolatility, data security, and retrofit capability are integral to Benchmarq's product line.

Our Commitment

When you choose to integrate Benchmarq products within your own, be assured that Benchmarq is committed to providing the specific solutions you need today and to developing creative solutions to the growing challenges of tomorrow—supported by the best customer service and the highest overall quality.

The drive for excellence in all dimensions of quality is a cornerstone of our company.

Data Book Organization

This data book is organized into general information sections and product family sections.

You can locate information in this book in several ways.

To locate information by:	See pages:
Table of Contents	v
Alphanumeric Product Index	vi
Family Summary and Selection Guides	1-2 through 1-6
Product Cross-Reference Tables	1-7

Detailed product information is included in Chapters 2 through 6. Each product family section includes product data sheets and applicable design notes:

- Each data sheet provides the device specifications for one family member.
- Design notes at the end of applicable family sections provide important hardware and software information to aid in the application of family members.

Packaging information is included in Chapter 7, and sales offices and distributors are listed in Chapter 8.

For More Information ...

If you haven't found it here . . . **Ask!**

Contact your local sales office, listed in the back of this data book, for help or more information.

Additional Benchmarq information is available from your Benchmarq distributor or sales office, or by contacting Benchmarq Customer Service at (214) 407-0011.

Factory technical assistance is available by phone or fax.

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Alphanumeric Product Index

Data Sheet Types

Product information data sheets progress in detail as the product goes from design to full production.

The three types of data sheets are defined below.

- **Advance Information**: Benchmarq Advance Information data sheets provide information for early product planning. These data sheets describe a product in the design or development stage. Specifications may change in any manner.
- **Preliminary**: Benchmarq Preliminary data sheets provide preliminary specifications for product design. They describe a product through its early production stage. Supplementary data may be published at a later date.
- **Final**: Benchmarq data sheets not labeled Advance Information or Preliminary are considered Final. They describe a product in full production and provide specifications for product design.

Engineering Prototype

Prior to full production, Benchmarq may provide limited quantities of Engineering Prototypes. Engineering Prototypes are suitably tested for evaluation and restricted use. Any necessary errata data accompanies engineering prototype parts. They are marked with the part number and an EP or Engineering Prototype identification.

Electrostatic Discharge (ESD) and Integrated Circuit (IC) Handling

Benchmarq ICs, as all ICs, are sensitive to electrostatic discharge (ESD). Although Benchmarq ICs are designed to withstand high ESD voltages, improper handling may cause damage. Standard ESD-prevention handling procedures should be followed. ESD-prevention considerations include proper grounding of operators, work surfaces and chip-handling equipment; appropriately high relative humidity levels; and use of antistatic handling and packaging materials. The ICs should be stored and shipped in antistatic tubes. The antistatic tubes containing the ICs must be brought to the same potential as the work area/operator before the individual ICs are handled.

The Benchmarq Quality Policy

It is the policy of Benchmarq to provide the highest quality products in support of our customers' needs. We recognize that we are in the business of providing not only the physical product, but also documentation, technical support, sales and marketing support, and timely product delivery. Our commitment to our customers begins with product concept and must extend long after actual product purchase and receipt.

We are dedicated to establishing partnerships with our customers and know that to succeed we must help our customers succeed. We will do this by:

- Holding ourselves and our vendors accountable for establishing carefully considered methods and procedures for design, test and production with clear and concise documentation,
- Responding professionally and expeditiously to customer or vendor problems that arise, bringing to bear the company's strongest resources,
- Developing an industry-leading "Quality Technology" to drive incremental improvements in all the products we provide, and to contribute to a continuous reduction in new product time to market, and
- Continuously providing products and services to meet or exceed the best expectations of our customers.

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Rev. 1.02
From Page 1 of Benchmarq Quality Manual

Processor Management Unit (PMU) Summary and Selection Guide

Single-chip "soft landing" solutions for power-sensitive microprocessor and microcontroller systems.

Dual threshold voltage microprocessor supervisor

- Programmable NMI voltage threshold for power-fail early warning and power-recovery notification
- Programmable Reset voltage threshold for power-down/power-up microprocessor control

  -5% or -10% voltage trigger point
- Programmable microprocessor watchdog monitor

and

Battery-backup nonvolatile fast SRAM

- 2K bytes for storage of critical data during power-down/power-up cycles
- Complete nonvolatile control: automatic write-protection and switching to battery backup on power loss

  Simultaneous nonvolatile control for optional external CMOS SRAM
- Memory speeds of 45 or 70 ns; data-retention current under 1 µA
- "Cloaked" mode allows overlapped memory address map.

PMU Selection Guide

Bus Interface	Read/Write Cycle Times	NMI Voltage Threshold Input	Pins / Package	Part Number	Page Number
Non-muxed	45, 70 ns	V_{CC} or V_{TH}	40 / DIP 44 / PLCC	bq1001	2-1
Muxed (address latch)	45, 70 ns	V_{CC}	28 / DIP 28 / PLCC	bq1002	2-23

Energy Management Unit (EMU) Summary and Selection Guide

Compact single-chip energy monitoring, recharge control, and energy management solutions for battery-powered systems.

- "Gas Gauge" for direct measurement of battery consumption and capacity
- Programmable fast charge and conditioning control for nominal 3.6V–12V NiCd, lead acid and Ni/MH batteries

  Programmed constant charge, pulsed charge, or "burp" charge

  Full charge determined by -ΔV, programmed maximum voltage, and programmed maximum charge time
- Backup voltage supply output regulated from the main battery
- Programmable open-drain outputs for power management or status indication
- Operates from 4.5V–18V battery charger supply or 4.5V–5.5V system V_{CC}
- Direct microprocessor bus interface, operation to 12 MHz

EMU Selection Guide

Configuration	Backup Supply Output Voltage	Pins / Package	Part Number	Page Number
Microprocessor peripheral	3.3V	24 / .300" SDIP, SOIC	bq2001	3-1
	5.3V	24 / .300" SDIP, SOIC	bq2002	3-27

Nonvolatile SRAM Summary and Selection Guide

Fast access time, unlimited read/write cycles, and internal lithium backup battery provide simple CMOS SRAM operation and reliable automatic nonvolatility. Eliminates the slow write time and limited write cycles of EEPROM.

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Industry-standard pinout
- Conventional SRAM operation; unlimited write cycles
- 10 or 5 years minimum data retention in the absence of power
- Battery internally isolated until power is first supplied

Nonvolatile SRAM Selection Guide

Density	Config-uration	Access Time (ns)	Minimum Data-Retention Time	Pins / Package	Part Number	Page Number
64 Kb	8 Kb x 8	85, 150, 200	10 years	28 / DIP	bq4010	6-1
256 Kb	32 Kb x 8	100, 150, 200	10 years	28 / DIP	bq4011	6-11
		35, 45	10 years	28 / DIP	bq4011H	6-21
		20, 25	10 years	28 / DIP	bq4011H	6-31
1 Mb	128 Kb x 8	85, 120	10 years	32 / DIP	bq4013	6-33
2 Mb	256 Kb x 8	85, 120	10 years	32 / DIP	bq4014	6-43
	128 Kb x 16	85, 120	10 years	40 / DIP	bq4024	6-63
4 Mb	512 Kb x 8	85, 120	5 years	32 / DIP	bq4015	6-53
	256 Kb x 16	85, 120	5 years	40 / DIP	bq4025	6-73

Protects standard CMOS SRAMs against unexpected power loss by write-protecting the memory and automatically switching to a 3V backup battery.

- Power monitoring and switching for 3 volt battery-backup applications
- Automatic write-protection during power-up/power-down cycles
- Automatic switching from V_{CC} to first backup battery and from first backup battery to second backup battery
- Less than 10 ns chip enable propagation delay
- 5% or 10% supply operation
- Control up to 4 banks of SRAM
- DIP or SOIC packages

Nonvolatile Controller Selection Guide

Banks Controlled	$\overline{CE}$ Delay (Max.)	Standby Current (Max.)	I_{OUT} (Typ.)	Pins / Package	Part Number	Page Number
1	10 ns	100 nA	150 mA	8 / DIP, SOIC	bq2201	4-1
4	10 ns	100 nA	150 mA	16 / DIP, SOIC	bq2204	4-9

Real-Time Clock Summary and Selection Guide

Space-saving nonvolatile PC-compatible real-time clock family eliminates unpredictable user lifetimes and the need for external circuitry.

- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Functionally compatible with the MC146818A
- Completely self-contained modules operate for more than 10 years in the absence of power
- IC versions only require a crystal and battery
- 160 ns cycle time allows fast bus operation
- Selectable Intel or Motorola bus timing
- BCD or binary format representation of clock and calendar
- Calendar in days, day of the week, months, and years, with automatic leap-year adjustment
- Time of day in seconds, minutes, and hours

  12- or 24-hour format

  Optional daylight-saving adjustment
- Three individually maskable interrupt event flags.
- Better than one minute per month clock accuracy

Real-Time Clock Module Selection Guide

User RAM (bytes)	Bus Interface	Pins / Package	Part Number	Page Number
50	Intel/Motorola	24 / DIP	bq3287	5-19
50	Intel/Motorola	24 / DIP	bq3287A	5-19
50 + 4K	Intel	24 / DIP	bq3387	5-39
50 + 8K	Intel	24 / DIP	bq3487	5-43

Real-Time Clock IC Selection Guide

User RAM (bytes)	Bus Interface	Clock Standby Current	Pins / Package	Part Number	Page Number
50	Intel/Motorola	0.5 µA	24 / DIP, SOIC 28 / PLCC	bq3285	5-1
50 + 4K	Intel	1.0 µA	24 / DIP, SOIC 28 / PLCC	bq3385	5-37
50 + 8K	Intel	1.0 µA	24 / DIP, SOIC 28 / PLCC	bq3485	5-41

NVSRAM Cross-Reference

Density	Dallas Semiconductor	SGS-Thomson	Benchmarq
64Kb	-	MK48Z08-10	bq4010-85
	-	MK48Z18-10	bq4010Y-85
	DS1225AB-150	MK48Z08-15	bq4010-150
	DS1225AD-150 DS1225Y-150	MK48Z18-15	bq4010Y-150
	DS1225AB-200	MK48Z08-20	bq4010-200
	DS1225AD-200 DS1225Y-200	MK48Z18-20	bq4010Y-200
256Kb	DS1230AB-100	-	bq4011-100
	DS1230Y-100	-	bq4011Y-100
	DS1235AB-150	-	bq4011-150
	DS1235Y-150	-	bq4011Y-150
	DS1235AB-200	-	bq4011-200
	DS1235Y-200	-	bq4011Y-200
1Mb	DS1245AB-100	-	bq4013-85
	DS1245Y-100	-	bq4013Y-85
	DS1245AB-120	-	bq4013-120
	DS1245Y-120	-	bq4013Y-120

Real-Time Clock Cross-Reference

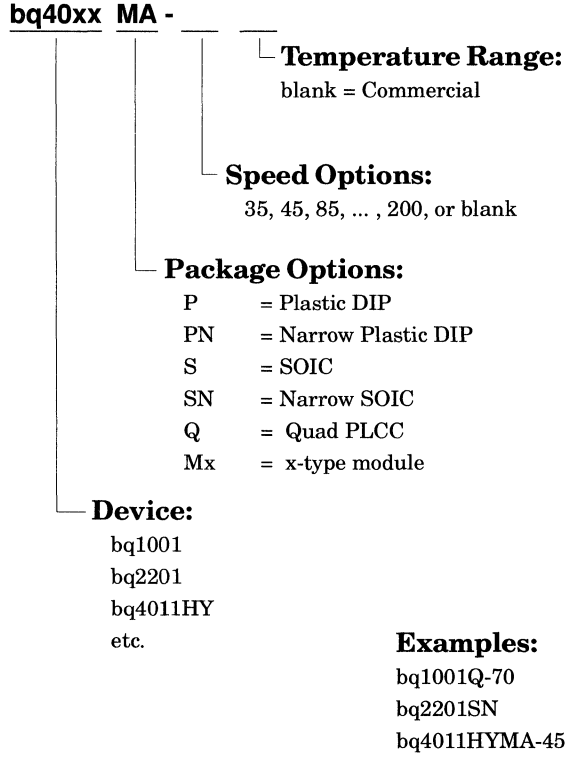
Dallas Semiconductor	SGS-Thomson	Benchmarq
DS1285	MK48T85	bq3285
DS1287	MK48T87	bq3287
DS1287A	MK48T87A	bq3287A
DS1385	-	bq3385
DS1387	-	bq3387

Ordering Information

Benchmarq's standard products are available in several packages and operating ranges. A valid order number is a sequence of:

- **Device**
- **Package Options**
- **Speed Options**
- **Temperature Range**

Valid options for a specific device are defined in the ordering information section at the end of its data sheet. Contact your Benchmarq sales office about non-standard requirements or to place an order. Sales offices are listed at the end of this data book.



Processor Management Unit (PMU)

Features

- 2K bytes of SRAM
  - Power-down write protection
  - "Cloaked" SRAM may share address space with system memory
- Two supply thresholds for power failure "soft landing"
  - Impending power-fail/power-restored notification
  - Power-down/power-up microprocessor reset
- Automatic switching to backup power
- Microprocessor watchdog monitor
- Access times of 45 and 70 ns
- 40-pin plastic DIP; 44-pin PLCC

General Description

The CMOS bq1001 Processor Management Unit (PMU) is a specialized battery-backup static RAM that provides all functions required for graceful power-down/power-up sequencing in applications where uninterrupted processing is essential.

Early power-fail detection is provided via a user-definable threshold input that gates a non-maskable interrupt output. A reset is produced as the power supply decays to an out-of-tolerance condition.

During a power failure, the time period between the non-maskable interrupt and the reset allows for a "soft landing." Critical information held in registers, counters, pointers, etc. may be stored into the special SRAM, which operates as a true nonvolatile memory when connected to a 3V backup supply.

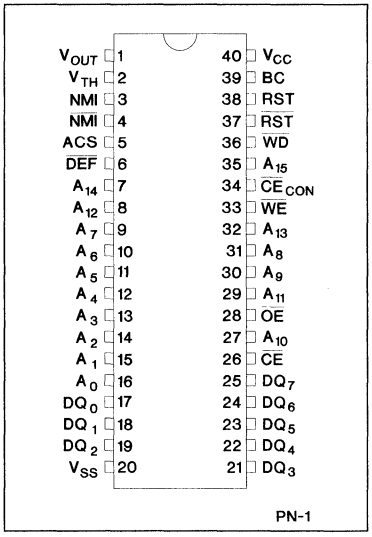
With its "cloaked" mode of access, the 2K byte PMU memory can be transparent to the system memory map, or it can occupy a nonoverlapped address block.

On power-up, the reset is held active for processor initialization. Critical information from the nonvolatile memory may be retrieved, and processing may resume at the point of the previous power-fail detection and/or in a manner incorporating specific information stored at power fail.

A watchdog function is also provided to verify valid execution during normal operation. The bq1001 is managed through eight control/status registers, which occupy the upper eight bytes of its internal 2K memory.

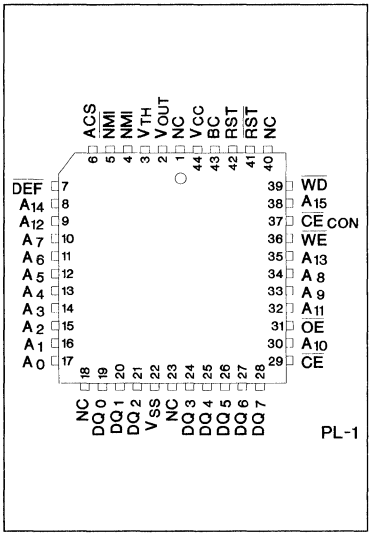
Pin Connections

40-Pin PDIP



PN-1

44-Pin PLCC



PL-1

Pin Names

A_0–A_{15}	Address inputs
DQ_0–DQ_7	Data input/output
V_{TH}	Threshold voltage input
ACS	Address compare strobe input
$\overline{WD}$	Watchdog strobe input
$\overline{DEF}$	Default setting override input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
$\overline{CE}$	Chip enable input
$\overline{CE}_{CON}$	Conditioned chip enable output
NMI, $\overline{NMI}$	Non-maskable interrupt outputs
RST, $\overline{RST}$	Reset outputs
BC	3 volt backup cell input
NC	No connect
V_{OUT}	Supply output
V_{CC}	+5 volt supply input
V_{SS}	Ground

Pin Descriptions

A_0–A_{15} **Address inputs**

DQ_0–DQ_7 **Data input/output**

V_{TH} **Threshold voltage input**

When the V_{TH} input voltage goes below the internal 2.50V reference voltage, and this is the selected V_{NMI} input, the NMI and $\overline{NMI}$ signals are asserted.

ACS **Address compare strobe input, active low**

ACS latches addresses on a high-to-low transition. The latched address is used for PMU memory "open" and "close" address comparison.

$\overline{WD}$ **Watchdog strobe input, active low**

$\overline{DEF}$ **Default setting override input, active low**

$\overline{DEF}$ is intended to be used as a user-interface input (pushbutton to ground). $\overline{DEF}$ pulled low forces the RST and $\overline{RST}$ outputs active for time t_{RSW} and returns all control and status registers to the default setting.

$\overline{OE}$ **Output enable input, active low**

$\overline{WE}$ **Write enable input, active low**

$\overline{CE}$ **Chip enable input, active low**

$\overline{CE}_{CON}$ **Conditioned chip enable output**

NMI **Non-maskable interrupt output, active high**

$\overline{NMI}$ **Non-maskable interrupt output, active low**

$\overline{RST}$ **Reset output, active low**

RST **Reset output, active high**

BC **3 volt backup cell input**

V_{OUT} **Supply output**

V_{OUT} provides the higher of V_{CC} or BC, switched internally, to supply external RAM.

V_{CC} **+5V supply input**

V_{CC} provides the operating supply and is also the voltage comparison input for the V_{RST} and (if selected) the V_{NMI} thresholds.

V_{SS} **Ground**

Truth Table

Memory Mode	Memory State	Memory Address	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	$\overline{CE}_{CON}$	Power
Read	Open	PMU	L	H	L	D_{OUT}	H	Active
Write	Open	PMU	L	L	X	D_{IN}	H	Active
Output disabled	Open	PMU	L	H	H	High Z	H	Active
Not selected	Open	PMU	H	X	X	High Z	H	Standby
Not selected	Open	External	L	X	X	High Z	L	Standby
Not selected	Open	External	H	X	X	High Z	H	Standby
Not selected	Closed	X	L	X	X	High Z	L	Standby
Not selected	Closed	X	H	X	X	High Z	H	Standby

Functional Description

Special Internal Memory

The PMU contains 2K bytes of special static RAM that can be operated as nonvolatile memory and as "cloaked" memory. The upper 8 bytes of this memory are used for control and status monitoring. The remaining 2040 bytes of memory can be used to store critical data or program information during a power-down cycle. Cloaked memory, which is transparent from the main system memory map, can be used for general memory map expansion or for secure data fields.

Mapping PMU Memory

The 2K byte PMU memory can be mapped in several ways, depending on the system's physical address range. When used by a system that addresses a maximum of 64K bytes, the PMU is mapped as shown in Figure 1.

When used by a system that addresses greater than 64K bytes, the PMU memory may reside in any 64K byte segment starting on a 2K byte boundary. In either case, the PMU memory can occupy the upper (default) 2K or the lower 2K bytes of the 64K segment.

Accessing PMU Memory

The PMU memory may be accessed any time after it is opened. Opening the PMU memory involves performing three consecutive read or write cycles to a user-definable address location in the system I/O map or memory map, followed by $\overline{CE}$ high. Note that if a write cycle is used to open PMU memory, data integrity at the accessed locations is not guaranteed.

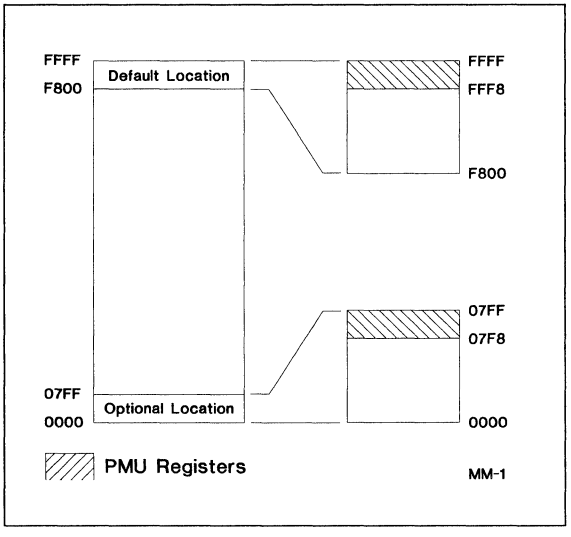


Figure 1. Memory Map

As address inputs A_0 to A_{15} are held valid, a high-to-low transition on the address compare strobe input, ACS, latches the 16-bit address location into a compare register, independent of chip enable. The 2K byte PMU memory is accessible after three consecutive address matches are made, followed by $\overline{CE}$ high. The PMU memory occupies 2K of the 64K segment controlled by the PMU $\overline{CE}$ input.

Once opened, the PMU disables access to any external memory occupying the same 2K bytes address space as its internal memory. This is achieved by unconditionally deactivating the $\overline{CE}_{CON}$ output. Access to memory locations outside the PMU memory space is available as usual.

Closing PMU Memory

PMU memory must be closed for either of the following purposes:

- To access external memory locations within PMU address space when:
  - PMU memory is open.
  - PMU memory address space overlaps that particular location of the external memory.
- To update contents of registers when:
  - PMU memory is open.
  - Registers are written.

Closing the PMU memory involves issuing a set of three consecutive read or write cycles to the same address used during the PMU open process, followed by $\overline{CE}$ high. The open and close address location is user-definable as described in the PMU Registers section. The default open and close address location is 07FF.

Any updates to PMU memory, including the PMU registers, are retained when PMU memory is closed. The PMU is reconfigured based on register updates only when the PMU memory is closed with a valid update pattern in the access control registers.

When the PMU is configured based on control register bit 3 = 1 (non-automatic open, default), and power-down occurs with the PMU memory open, the PMU memory is not accessible on power-up. To access the PMU memory from this state, a complete close cycle (three address matches followed by $\overline{CE}$ high) must precede the open cycle.

PMU Memory Nonvolatility

Nonvolatility is achieved by connecting a 3V backup supply to the PMU BC input pin. When V_{CC} falls to an out-of-tolerance condition, the PMU unconditionally write-protects its internal SRAM, independent of the state of the chip enable input, $\overline{CE}$. If a valid access is in process during power-fail detection, that memory cycle may continue to completion before the memory is write-protected. If the memory cycle is not terminated, the PMU unconditionally write-protects its memory within time t_{WPT}.

The out-of-tolerance voltage level is V_{RST}, which is the same level as set for the reset output. As the supply continues to fall below V_{RST}, the PMU memory is sustained by the external 3V source (lithium cell). On power-up, the PMU memory is held inactive for time t_{CER} (120 ms maximum) after the supply has reached V_{RST} to allow for processor initialization, independent of the state of the $\overline{CE}$ input.

Note that if no battery is provided, the BC pin must be grounded.

Power Failure Detection

Non-Maskable Interrupt Threshold

The PMU warns the host processor of an impending power failure and a return to full power via an output that can be used as a non-maskable interrupt. An internal precision comparator monitors the threshold voltage input (V_{TH}) or supply input (V_{CC}) relative to an accurate internal voltage reference. Once the V_{TH} or V_{CC} pin passes this reference voltage, the non-maskable interrupt is forced active for the time period t_{NMW}. The V_{TH} or V_{CC} input must be beyond the reference voltage for three consecutive 25µsec samples. The threshold voltage input can be derived from the 5V supply, or from a higher DC voltage upstream of the supply. Both an active high NMI and an active low $\overline{NMI}$ output are made available to the user.

Because the comparator threshold voltage is user-selectable (as described in the PMU Registers section), the PMU can directly monitor V_{CC} if a higher voltage supply is not available or is not needed. If a higher-voltage DC level is chosen for early power-fail detection, a simple resistor divider network can be used to set the V_{TH} voltage input to the desired threshold (see Figure 2). The internal reference voltage is set to 2.50V.

Note: The active low $\overline{NMI}$ normally slews down with V_{CC}, but can be programmed to be held high as described in the PMU Registers section.

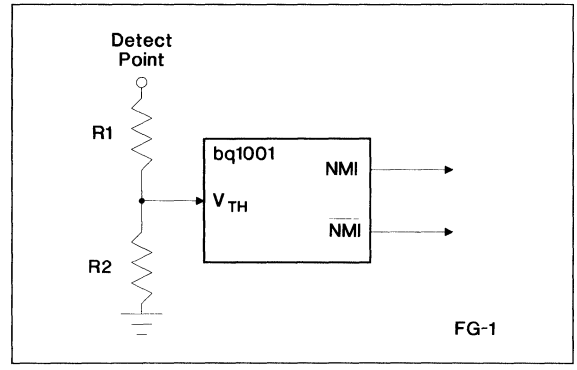


Figure 2. Threshold Voltage Monitor

Power-Down/Power-Up Reset Threshold

The bq1001 also provides reset outputs when the supply voltage (V_{CC}) passes an out-of-tolerance threshold below which the system performance is questionable. A precision comparator monitors the supply at the V_{CC} pin relative to an internal reset voltage level (V_{RST}). The level of V_{RST} is user-selectable at nominal thresholds of 4.50V and 4.30V. V_{CC} must be beyond V_{RST} for three consecutive 25µsec samples. During power-down, the reset outputs are forced active as the supply falls below V_{RST}, and are held active as the supply continues to fall. Both an active-high RST and an active-low $\overline{RST}$ are made available to the user. The active-high output slews down with the supply. During power-up, the reset outputs are held active for time t_{RSW} after $V_{CC} = V_{RST}$.

The reset outputs can be inhibited for nonvolatile processor operation as described in the PMU Registers section.

Watchdog

The bq1001 provides a watchdog function to monitor processor execution during power-valid operation. If the watchdog timer is enabled, then a high-to-low transition at the watchdog strobe input $\overline{WD}$ must occur during t_{WTO}, or the watchdog timeout will take place.

The watchdog timer can also be reset under software control by opening or closing PMU memory (see the PMU Registers section). If this open or close is completed before time t_{WTO}, the timer is reset, and the outputs are not forced active.

The timeout period t_{WTO} is user-selectable as 125 ms, 500 ms, 2 sec, or infinity (i.e., disabled). The default setting configures a disabled watchdog monitor.

The watchdog timer can be programmed to output a NMI/$\overline{NMI}$ instead of the default RST/$\overline{RST}$ (as defined in the PMU Registers section).

External Nonvolatile SRAM Control

An external CMOS static RAM can be battery-backed using the control output pins from the bq1001. As with the reset control feature, the bq1001 monitors the voltage level at the 5V V_{CC} input. As this voltage input decays to below V_{RST}, the conditioned chip enable pin $\overline{CE}_{CON}$ is forced inactive independent of the chip enable input $\overline{CE}$. This activity unconditionally write-protects external SRAM as V_{CC} falls below V_{RST}. If a valid access is in progress during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated, the $\overline{CE}_{CON}$ output unconditionally write-protects the memory within time t_{WPT}.

The voltage level defined as out-of-tolerance is the same level as set for the reset output V_{RST}. As the supply falls below V_{BC} during an out-of-tolerance condition, an internal switching device forces V_{OUT} and $\overline{CE}_{CON}$ to the external 3V source. During power-up, V_{OUT} and $\overline{CE}_{CON}$ are switched back to the +5V supply as V_{CC} rises above V_{BC}. The $\overline{CE}_{CON}$ output is held inactive for time t_{CER} (120 ms max) after the supply has reached V_{RST}, independent of the $\overline{CE}$ input, to allow for processor initialization. During normal 5V operation, the $\overline{CE}$ input is passed through to $\overline{CE}_{CON}$ with a typical propagation delay of 7 ns. Nonvolatility is achieved by hardware hookup as shown in Figure 3. If external SRAM nonvolatility is not required, the V_{OUT} and $\overline{CE}_{CON}$ outputs can be disabled as described in the PMU Registers section.

Default Setting Override

The $\overline{DEF}$ input provides a manual override that changes all settings in control registers back to default. It is intended to be used as a user-interface input (pushbutton to ground) and should not be driven by or connected to any active component. See the PMU Registers section.

When the $\overline{DEF}$ pin is forced active, the RST and $\overline{RST}$ outputs are forced active. The RST and $\overline{RST}$ outputs remain active for time t_{RSW} after $\overline{DEF}$ returns inactive.

The $\overline{DEF}$ input can be used during valid 5V operation, or can be used in the data-retention mode ($V_{CC} < V_{BC}$). If the $\overline{DEF}$ pin is forced to ground while in data-retention mode, however, the external energy source at BC is loaded (approximately 10K ohms) while this pin is forced low.

PMU Registers

The PMU registers occupy the top eight bytes of the 2K bq1001 memory as shown in Figure 4. Once configured, these registers maintain valid settings in the event of power loss—provided the BC pin has a valid input. Table 1 shows the PMU registers and their default settings. The PMU configures itself per the contents of these registers when closed with the valid update pattern in the access control registers.

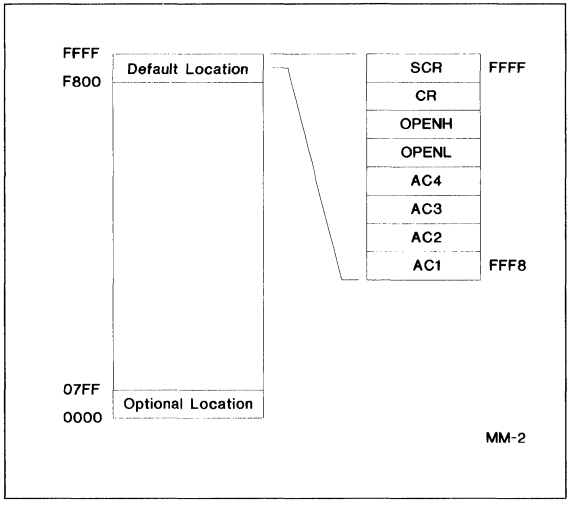


Figure 4. Default PMU Registers Location

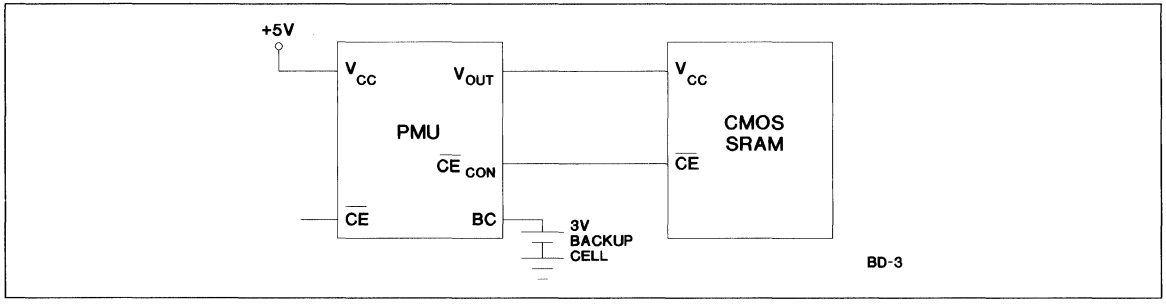


Figure 3. Hardware Hookup

Table 1. PMU Registers

Symbol	Name	Default Address	Default Bit Settings							
			7 (MSB)	6	5	4	3	2	1	0 (LSB)
AC1	Access control byte 1	FFF8	1	1	0	0	0	1	0	1
AC2	Access control byte 2	FFF9	1	0	1	0	0	1	1	0
AC3	Access control byte 3	FFFA	0	0	1	1	1	0	0	1
AC4	Access control byte 4	FFFB	0	0	1	0	1	0	1	1
OPENL	Open and close low byte	FFFC	1	1	1	1	1	1	1	1
OPENH	Open and close high byte	FFFD	0	0	0	0	0	1	1	1
CR	Control register	FFFE	0	0	1	1	1	0	1	-
SCR	Status/control register	FFFF	-	-	-	1	1	1	1	1

Access Control Registers (AC1–AC4)

Access control bytes 1 through 4 (AC1–AC4) contain access control information. All settings of other PMU registers are held to existing definitions until the PMU memory is closed with the access control registers written with the update pattern shown in Table 2.

The upper four PMU registers (SCR, CR, OPENH, and OPENL) can be read or written at any time, but the PMU does not recognize register updates until the PMU memory is closed with a valid update pattern in the access control registers. When the PMU is closed with a valid update pattern, AC1–AC4 are reset to the default settings.

During a control register update, at least one access control byte should be written prior to any changes to the upper four control bytes. If the update is disrupted before completion, the non-default access control pattern subsequently indicates that the control register data may not be the active setting. The update pattern for the remaining access control bytes should be written after the control registers are modified. This ensures that only a completed register update is recognized on closing.

Open and Close Location Registers (OPENH and OPENL)

Registers OPENH and OPENL contain the address location for opening and closing the PMU memory. Register OPENH contains the high address byte; that is, address bits A_{15}–A_8. Register OPENL contains the low address byte, address bits A_7–A_0. Although these two bytes can be read or written at any time while the PMU memory is open, they do not become active unless a valid update pattern is present as PMU memory is closed. Any new programmed address location becomes valid only after the PMU memory has been closed. The address location used to open the PMU memory must also be used to close it.

Table 2. Access Control Registers Update Pattern

Symbol	Name	Default Address	Valid Update Bit Settings							
			7 (MSB)	6	5	4	3	2	1	0 (LSB)
AC1	Access control byte 1	FFF8	0	0	1	1	1	0	1	0
AC2	Access control byte 2	FFF9	0	1	0	1	1	0	0	1
AC3	Access control byte 3	FFFA	1	1	0	0	0	1	1	0
AC4	Access control byte 4	FFFB	1	1	0	1	0	1	0	0

Control Register (CR)

The control register CR is used to program:

- NMI threshold voltage V_{NMI}
- Out-of-tolerance voltage V_{RST}
- Assertions of NMI and Reset
- PMU memory location

CR Bit 1								
7	6	5	4	3	2	1	0	
-	-	-	-	-	-	1	-	Normal RST/-$\overline{RST}$ assertions
-	-	-	-	-	-	0	-	RST/$\overline{RST}$ outputs disabled

The least-significant bit, bit 0, is not used.

Bit 1 is used to inhibit the RST and $\overline{RST}$ outputs from being active. The default setting of 1 in this bit provides normal operation for the reset outputs. If nonvolatility of the host processor is required, this bit can be cleared. This prevents the RST and $\overline{RST}$ outputs from being active.

CR Bit 2								
7	6	5	4	3	2	1	0	
-	-	-	-	-	0	-	-	PMU memory at upper block
-	-	-	-	-	1	-	-	PMU memory at lower block

Bit 2 determines the location of the PMU memory within the 64K byte segment. If this bit is set to 0, the default setting, the PMU memory resides at the upper block. If set to 1, the PMU memory resides at the lower block.

CR Bit 3								
7	6	5	4	3	2	1	0	
-	-	-	-	1	-	-	-	Normal operation
-	-	-	-	0	-	-	-	Automatic open

Bit 3 enables the automatic opening of PMU memory. If this bit is set to 0, PMU memory is automatically opened on power-down when the monitored supply falls below V_{NMI}. If this method of operation is chosen, and a valid access to memory is in progress when power failure occurs, PMU memory is not opened until the user terminates the access to memory. PMU memory is also opened on subsequent power-up and must be closed for normal memory map allocation. The default setting of 1 at bit 3 presents normal operation during power-down/power-up, which necessitates the use of the PMU opening procedure if user access to PMU memory is required.

CR Bit 4								
7	6	5	4	3	2	1	0	
-	-	-	1	-	-	-	-	Normal operation
-	-	-	0	-	-	-	-	Output control

Bit 4 is used to control the $\overline{RST}$ and $\overline{NMI}$ outputs during power-down. When bit 4 is set to the default setting of 1, these outputs behave as described previously, and any output with a high level slews down with V_{CC}.

If bit 4 is written to 0:

- When V_{CC} is below V_{BC}, the battery holds the active-low outputs high, and the active-high outputs slew down with V_{CC}.
- NMI/$\overline{NMI}$ is asserted on power-down and power-up as described previously.
- RST/$\overline{RST}$ is not asserted on power-down, but is asserted on power-up.

For nonvolatile microprocessor operation, writing both bit 1 and bit 4 to 0 may be necessary.

CR Bit 5								
7	6	5	4	3	2	1	0	
-	-	1	-	-	-	-	-	V_{RST} = 4.30 V
-	-	0	-	-	-	-	-	V_{RST} = 4.50 V

Bit 5 is used to define the out-of-tolerance voltage, V_{RST}. The default setting of 1 in bit 5 defines V_{RST} as 4.30 volts. If a 0 is written into this bit, V_{RST} is 4.50 volts.

CR Bits 6 and 7								
7	6	5	4	3	2	1	0	
0	0	-	-	-	-	-	-	V_{NMI} = 4.60 V
0	1	-	-	-	-	-	-	V_{NMI} = 4.75 V
1	0	-	-	-	-	-	-	V_{NMI} = 2.50 V
1	1	-	-	-	-	-	-	V_{NMI} = 2.50 V

Bits 6 and 7 are used to define the voltage V_{NMI}. As determined by these bits, when the V_{TH} or V_{CC} input pin falls below V_{NMI}, the NMI and $\overline{NMI}$ outputs are forced active. A value of 1 in these bits selects the V_{TH} pin threshold. This value for V_{NMI} allows the use of an external voltage divider network to sense power-fail conditions on the V_{TH} pin. Bits 6 and 7 may alternatively be programmed to detect early power-fail using either of two V_{NMI} thresholds directly at V_{CC}. The default value of 0 in both bits selects a V_{NMI} threshold on V_{CC} of 4.60V. The three combinations are user-selectable as shown.

Status/Control Register (SCR)

The status/control register SCR contains NMI status bits, controls watchdog timeout and outputs, and sets the condition of the $\overline{CE}_{CON}$ and V_{OUT} outputs.

SCR Bit 0								
7	6	5	4	3	2	1	0	
-	-	-	-	-	-	-	1	V_{OUT} not forced high
-	-	-	-	-	-	-	0	External nonvolatile device

The least-significant bit, bit 0, determines the condition of the V_{OUT} output. The default setting of 1 defines V_{OUT} as not being used for an external nonvolatile device. That is, the V_{OUT} pin is not forced high by the battery after a power failure. If an external device (processor, SRAM, etc.) is to be made nonvolatile, this bit should be set to 0. If this setting is chosen, the V_{OUT} pin is held high by the battery as V_{CC} slews below the BC input.

SCR Bit 1								
7	6	5	4	3	2	1	0	
-	-	-	-	-	-	1	-	$\overline{CE}_{CON}$ not forced high
-	-	-	-	-	-	0	-	$\overline{CE}_{CON}$ forced high

Bit 1 is used to set the level of the conditioned chip enable signal $\overline{CE}_{CON}$ during power failure. If this bit is set to 1 (default), the $\overline{CE}_{CON}$ output is not held high by the battery during power failure. If $\overline{CE}_{CON}$ is to be held high (for write-protection of an SRAM designed for nonvolatility) during and throughout an out-of-tolerance condition, this bit must be set to 0.

SCR Bit 2								
7	6	5	4	3	2	1	0	
-	-	-	-	-	1	-	-	RST/$\overline{RST}$ output
-	-	-	-	-	0	-	-	NMI/$\overline{NMI}$ output

Bit 2 of this control byte is used for defining which outputs are forced active when the watchdog timer is violated. If this bit is set to 1, the RST and $\overline{RST}$ outputs are forced active at watchdog violation. If this bit is set to 0, the NMI and $\overline{NMI}$ outputs are forced active. The default setting is 1.

SCR Bits 3 and 4								
7	6	5	4	3	2	1	0	
-	-	-	1	1	-	-	-	Disabled
-	-	-	1	0	-	-	-	2 sec
-	-	-	0	1	-	-	-	500 msec
-	-	-	0	0	-	-	-	125 msec

Bits 3 and 4 of the control byte are used for setting the timeout period t_{WTO} for the watchdog monitor. The default setting of 11 disables the watchdog monitor so that no input at $\overline{WD}$ is required for valid operation. Other timeout periods are defined above.

SCR Bits 5, 6, and 7								
7	6	5	4	3	2	1	0	
1	-	-	-	-	-	-	-	Power fail
-	1	-	-	-	-	-	-	Watchdog violation
-	-	1	-	-	-	-	-	Power valid

The three most-significant bits, bits 5, 6, and 7, are real-time status bits that indicate the current power condition and software-execution condition of a given system.

Bits 5 and 7 are read-only bits that indicate the current power condition. If the V_{TH} or V_{CC} input pin (as selected) is above V_{NMI}, bit 5 is 1 and bit 7 is 0. If the input pin voltage falls below V_{NMI}, bit 5 is 0 and bit 7 is 1. That is, bits 5 and 7 are always complementary.

Bit 6 is a read/write bit that indicates whether or not a watchdog failure has occurred.

If the NMI outputs are forced active from a watchdog violation, and power failure is detected during the active NMI output pulse, the NMI outputs return to the inactive state following the NMI pulse width t_{NMW}, and are automatically forced active again within $t_{NMW}/2$. This automatic additional active pulse interrupts the processor due to a loss of power when this loss of power occurred during an active NMI condition as a result of the watchdog violation. If bit 6 is automatically written to a 1 due to a watchdog failure, it can subsequently be cleared only by the user writing a 0 to this location. The user cannot write a 1.

2

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
I_{OUT}	V_{OUT} current	150	mA	
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-10 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	V_{RST}	5.0	5.5	V	V_{RST} is user-selectable per PMU Registers section
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	
V_{BC}	Backup cell voltage	2.0	-	4.0	V	
V_{TH}	Threshold voltage input	-0.3	-	V_{CC} + 0.3	V	

DC Electrical Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 2	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 2	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -2.0 mA
V_{OHB}	V_{OH}, BC supply	V_{BC} - 0.3	-	-	V	$V_{BC} > V_{CC}$, I_{OH} = -10µA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{SB1}	Standby supply current (TTL)	-	7	15	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current (CMOS)	-	1	3	mA	$\overline{CE} \geq V_{CC}$ - 0.2V, 0V ≤ $V_{IN} \leq$ 0.2V, or $V_{IN} \geq V_{CC}$ - 0.2V
I_{CC}	Operating supply current	-	45	70	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, I_{OH} = 0mA, I_{OL} = 0mA
V_{RST}	Reset trip point	V_{RST} - 0.06	V_{RST}	V_{RST} + 0.06	V	V_{RST} is user-selectable per PMU Registers section
V_{NMI}	NMI trip point	V_{NMI} - 0.06	V_{NMI}	V_{NMI} + 0.06	V	V_{NMI} is user-selectable per PMU Registers section and is monitored at V_{CC} or V_{TH}.
V_{SO}	Supply switch-over voltage	-	V_{BC}	-	V	
I_{CCDR}	Data-retention current	-	0.1	1.0	µA	Does not include data-retention current provided through V_{OUT} to additional memory. T_A = 25°C, V_{BC} = 3V
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.3	-	-	V	I_{OUT} = 100mA
V_{OUT2}	V_{OUT} voltage	V_{BC} - 0.3	-	-	V	$V_{CC} < V_{BC}$, V_{OUT} enabled per PMU Registers section, I_{OUT} = 100µA
I_{OUT1}	V_{OUT} current	-	100	-	mA	$V_{OUT} > V_{CC}$ -0.3V
I_{OUT2}	V_{OUT} current	-	100	-	µA	$V_{OUT} > V_{BC}$ -0.3V, V_{OUT} enabled per PMU Registers section

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC} = 3V.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	10	pF	$V_{I/O}$ = 0V
C_{IN}	Input capacitance	-	-	8	pF	V_{IN} = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 5 and 6

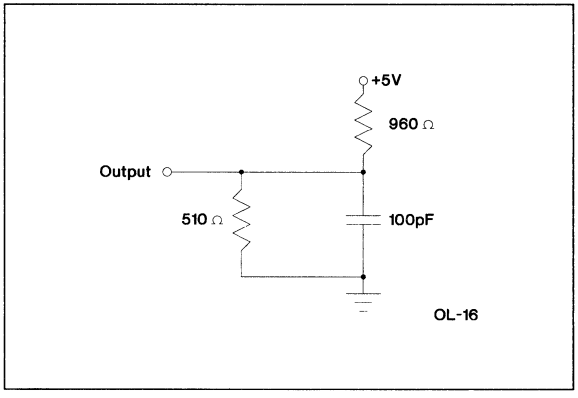


Figure 5. Output Load A

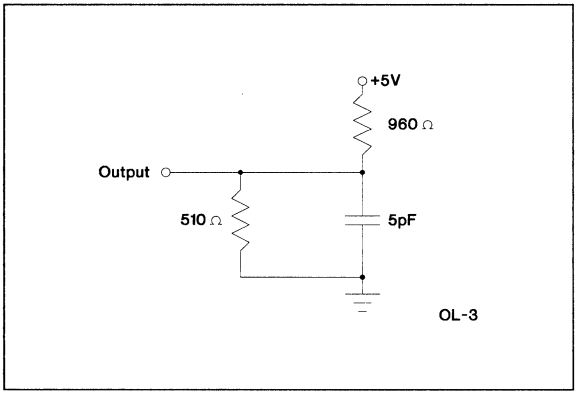
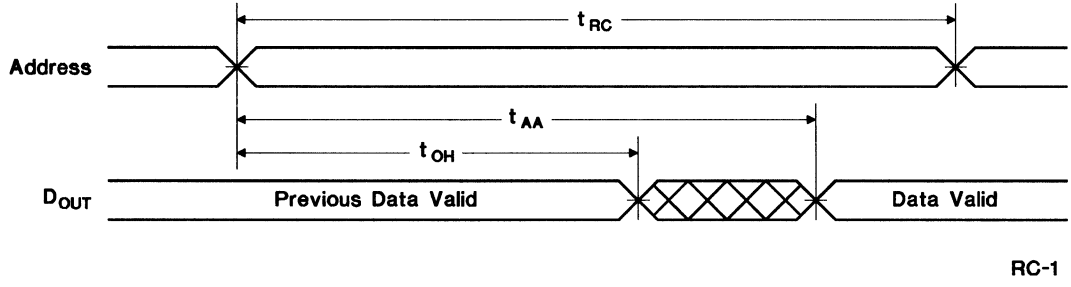


Figure 6. Output Load B

Read Cycle (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	-45		-70		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	45	-	70	-	ns	
t_{AA}	Address access time	-	45	-	70	ns	Output load A
t_{ACE}	Chip enable access time	-	45	-	70	ns	Output load A
t_{OE}	Output enable access time	-	20	-	35	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	5	-	5	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	15	0	25	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	15	0	25	ns	Output load B
t_{OH}	Output hold from address change	5	-	5	-	ns	Output load A

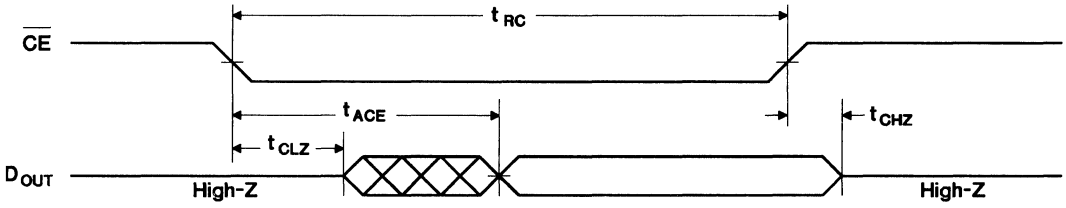
Read Cycle No. 1 (Address Access) [1,2]



RC-1

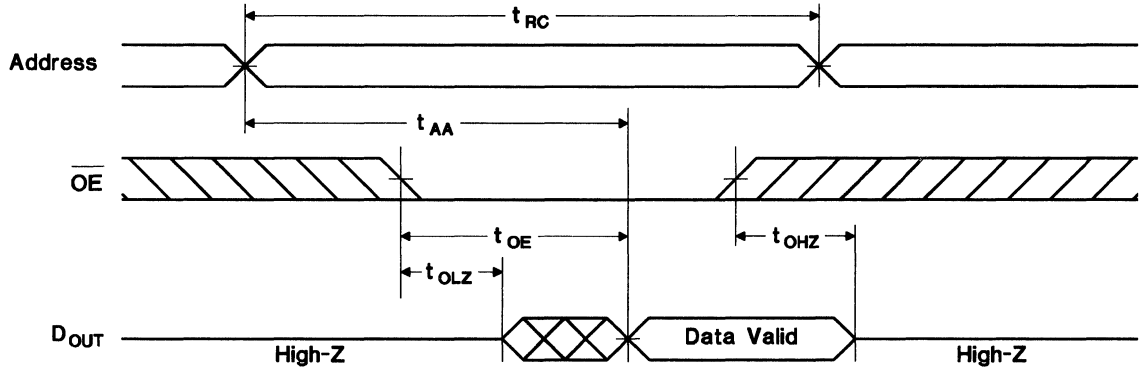
Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE}$ = $\overline{OE}$ = V_{IL}.

Read Cycle No. 2 ($\overline{CE}$ Access) [1,2,3]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access) [1,4]



RC-3

Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Address is valid prior to or coincident with $\overline{CE}$ transition low.
3. $\overline{OE} = V_{IL}$.
4. Device is continuously selected: $\overline{CE} = V_{IL}$.

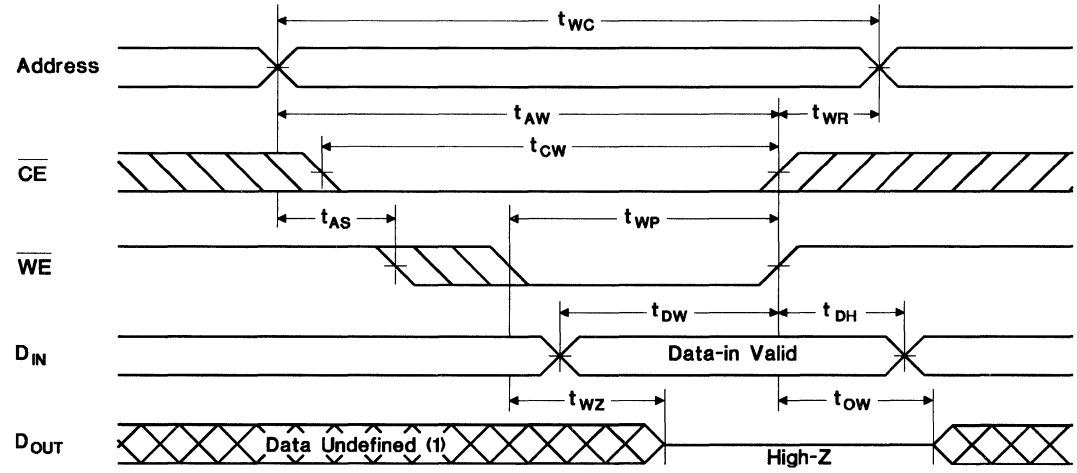
Write Cycle (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	-45		-70		Units	Conditions/ Notes
		Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	45	-	70	-	ns	
t_{CW}	Chip enable to end of write	40	-	60	-	ns	(1)
t_{AW}	Address valid to end of write	40	-	60	-	ns	(1)
t_{AS}	Address setup time	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	35	-	55	-	ns	Measured from beginning of write to end of write. (1)
t_{WR}	Write recovery time	3	-	5	-	ns	Measured from earlier of $\overline{CE}$ or $\overline{WE}$ going high to end of write cycle.
t_{DW}	Data valid to end of write	20	-	30	-	ns	Measured from first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH}	Data hold time	0	-	0	-	ns	Measured from first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{WZ}	Write enable to output in high Z	0	15	0	25	ns	I/O pins are in output state. (3)
t_{OW}	Output active from end of write	5	-	5	-	ns	I/O pins are in output state. (3)

Notes:

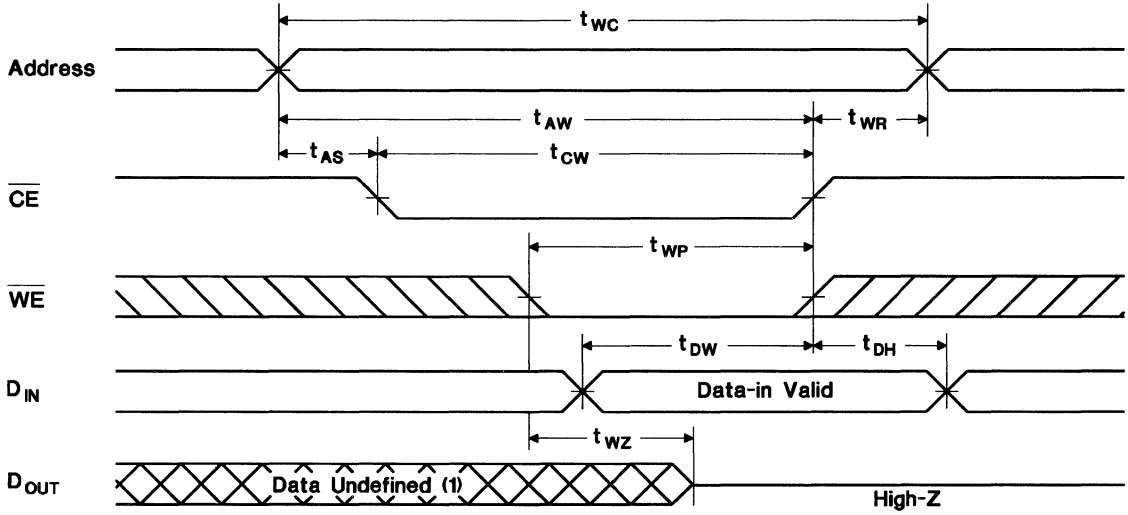
1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled)[1,2,3]



WC-1

Write Cycle No. 2 ($\overline{CE}$-Controlled)[1,2,3]



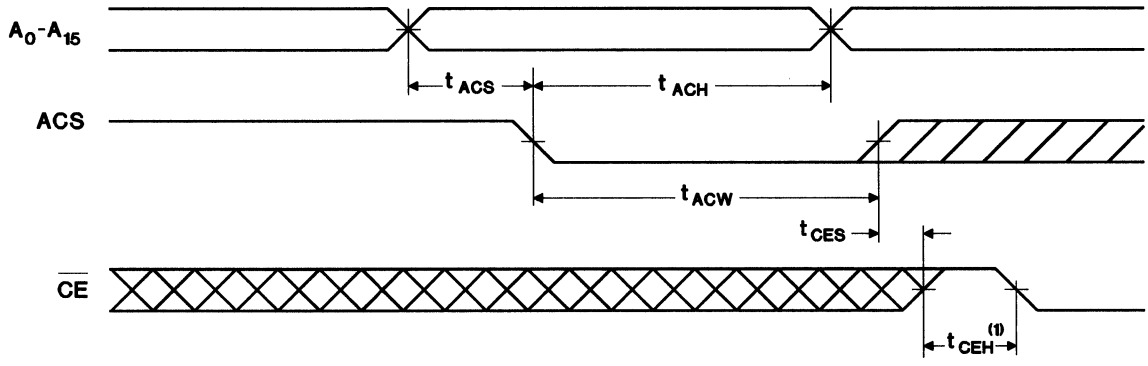
WC-2

Notes:
1. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
2. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

Open and Close Cycle Timing

Symbol	Parameter	-45		-70		Unit
		Min.	Max.	Min.	Max.	
t_{ACS}	Address valid to ACS fall	10	-	10	-	ns
t_{ACW}	Address compare strobe width	25	-	25	-	ns
t_{ACH}	Address hold from ACS fall	0	-	0	-	ns
t_{CEH}	Chip enable high following third strobe	5	-	5	-	ns
t_{CES}	Chip enable setup time	0	-	0	-	ns

Open and Close Cycle Timing



OC-1

Note: 1. $\overline{CE}$ high following the third compare strobe completes the PMU open or close operation.

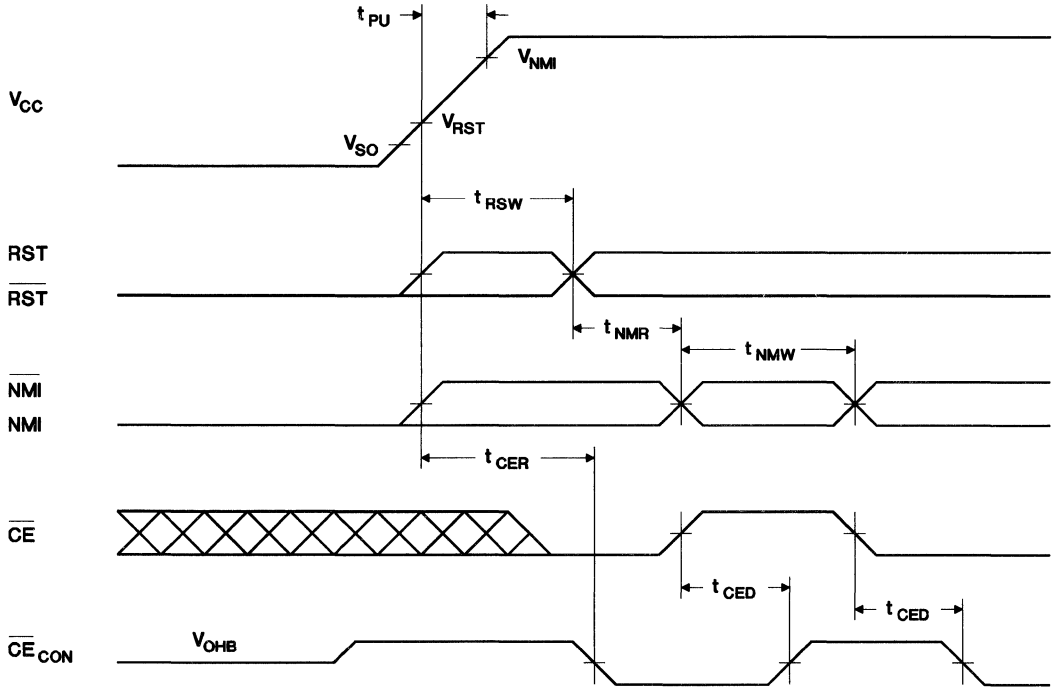
Power-Down/Power-Up Timing (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{PFD}	V_{NMI} detect to NMI, $\overline{NMI}$	25	75	150	µs	
t_{NMW}	NMI, $\overline{NMI}$ pulse width	12	25	40	µs	
t_{NMR}	NMI, $\overline{NMI}$ asserted after RST, $\overline{RST}$ inactive	50	150	200	µs	$V_{CC} > V_{NMI}$ or $V_{TH} > V_{NMI}$
t_{RST}	V_{RST} detect to RST, $\overline{RST}$	25	75	150	µs	Power-down/up sequencing per PMU Registers section.
t_{RSW}	RST, $\overline{RST}$ pulse width	40	80	120	ms	
t_{PF}	V_{CC} slew, V_{NMI} to V_{RST}	40	-	400,000	µs	
t_{FS}	V_{CC} slew, 4.25V to V_{SO}	10	-	-	µs	
t_{VRS}	V_{CC} valid to RST, $\overline{RST}$	25	75	150	µs	Power-down/up sequencing per PMU Registers section.
t_{PU}	V_{CC} slew, V_{RST} to V_{NMI}	0	-	-	µs	
t_{CED}	Chip enable propagation delay	-	7	10	ns	
t_{CER}	Chip enable recovery	-	t_{RSW}	-	ms	t_{CER} is time required after power-valid to allow for processor stabilization.
t_{WPT}	Write-protect time	40	100	150	µs	Write-protect occurs internally and by bringing $\overline{CE}_{CON}$ high.
t_{VTHF}	V_{TH} slew, 3.0V to 2.0V	40	-	400,000	µs	
t_{VTHR}	V_{TH} slew, 2.0V to 3.0V	0	-	-	µs	

Note: Typical values indicate operation at T_A = 25°C.

Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

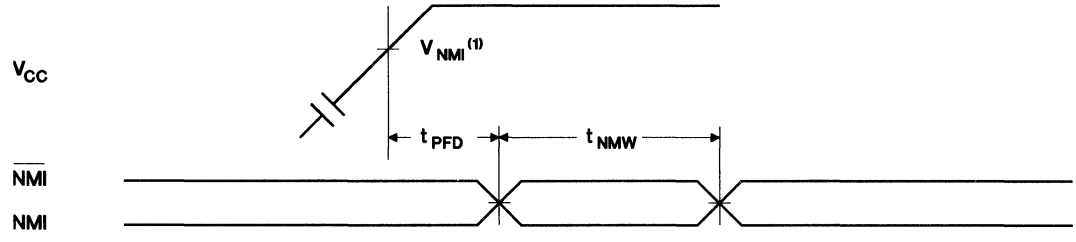
Power-Up Case 1: NMI/$\overline{\text{NMI}}$ Delayed by RST/$\overline{\text{RST}}$ Active



PU-2

Note: 1. SCR bit 1 = 0.

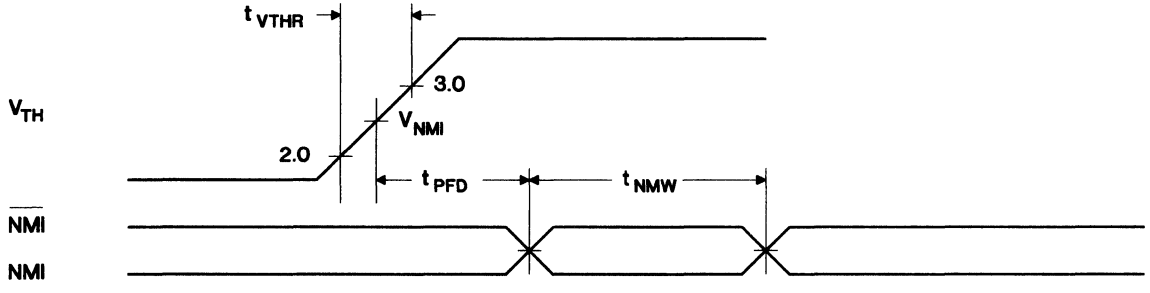
Power-Up Case 2: NMI/$\overline{\text{NMI}}$ Not Delayed



PU-3

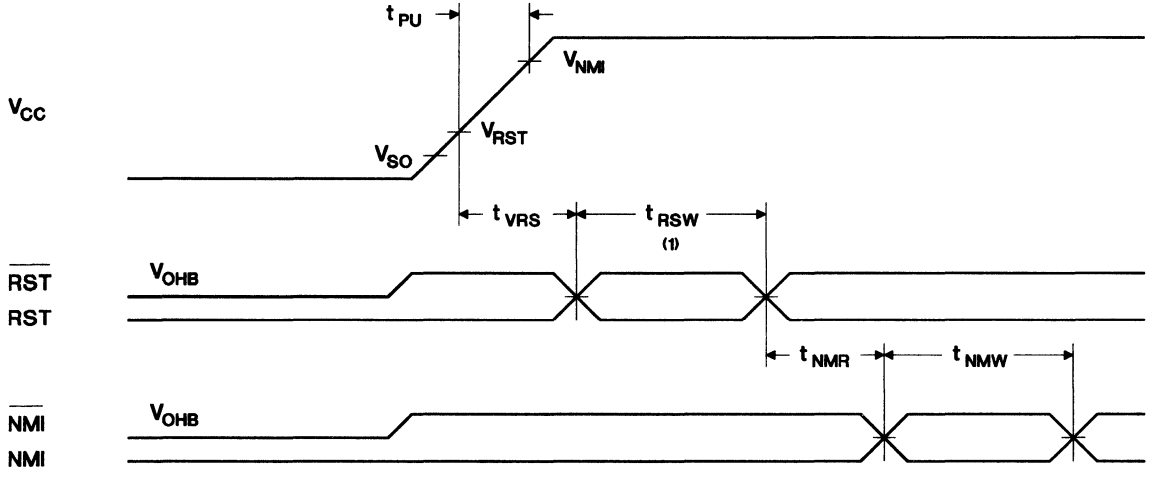
Note: 1. RST and $\overline{\text{RST}}$ are inactive before V_{NMI} is reached.

Power-Up Case 3: Under V_{TH} Sensing



PU-5

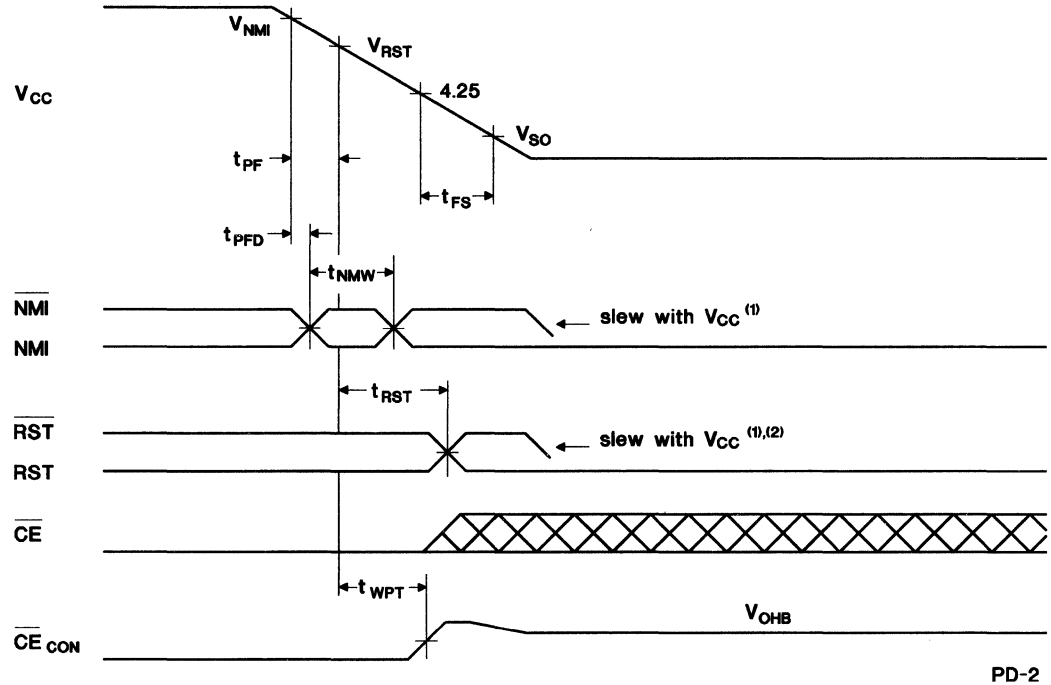
Power-Up Case 4: Power-Up With CR Bit 4 = 0



PU-4

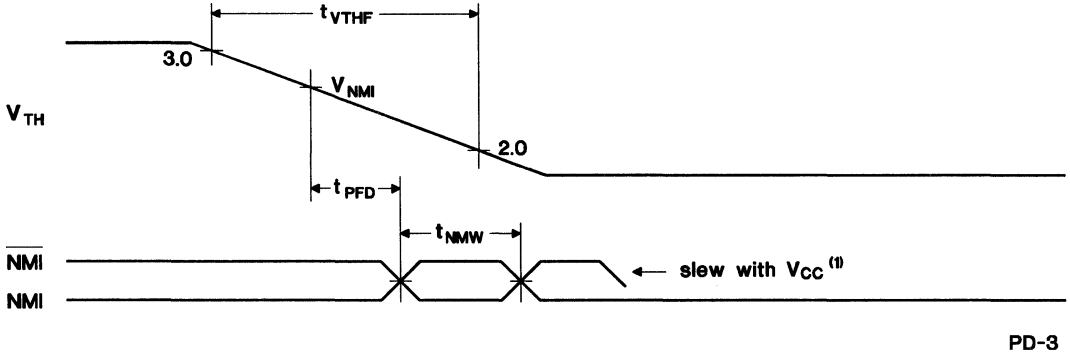
Note: 1. CR bit 1 = 1; RST/$\overline{\text{RST}}$ goes active on power-up.
If CR bit 1 = 0, RST/$\overline{\text{RST}}$ is disabled.

Power-Down Case 1: Under V_{CC} Sensing



Note:
1. CR bit 4 = 1.
2. CR bit 1 = 1.
3. SCR bit 1 = 0.

Power-Down Case 2: Under V_{TH} Sensing



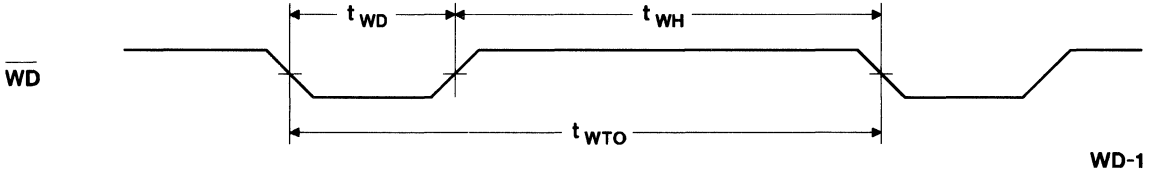
Note: 1. CR bit 4 = 1.

Watchdog/Default Timing (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{RSW}	RST, $\overline{RST}$ pulse width	40	80	120	ms	
t_{WD}	$\overline{WD}$ pulse width	25	-	-	ns	
t_{WH}	$\overline{WD}$ high time	50	-	-	ns	
t_{WTO}	Watchdog timeout period	0.5 t_{WTO}	t_{WTO}	1.5 t_{WTO}	-	t_{WTO} is user-selectable per PMU Registers section.

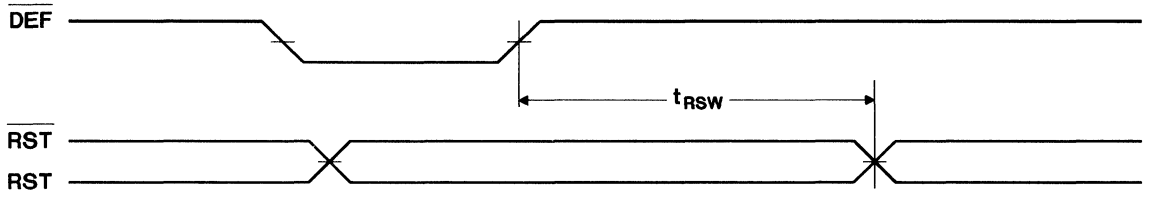
Note: Typical values indicate operation at T_A = 25°C.

Watchdog Timing



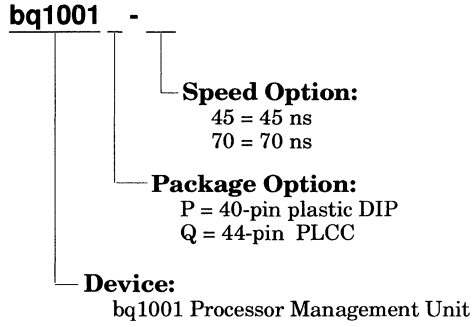
WD-1

$\overline{DEF}$ Timing



DEF-1

Ordering Information



Processor Management Unit (PMU)

Features

- 2K bytes of SRAM with latched address
  - Power-down write protection
  - "Cloaked" SRAM may share address space with system memory
- Two supply thresholds for power failure "soft landing"
  - Impending power-fail/power-restored notification
  - Power-down/power-up microprocessor reset
- Automatic switching to backup power
- Microprocessor watchdog monitor
- Access times of 45 and 70 ns
- Multiplexed address/data bus
- 28-pin plastic DIP; 28-pin PLCC

General Description

The CMOS bq1002 Processor Management Unit (PMU) is a specialized battery-backup static RAM that provides all functions required for graceful power-down/power-up sequencing in applications where uninterrupted processing is essential. Internally latched address provides a low-pin-count interface to multiplexed microprocessor address/data buses.

Early power-fail detection is provided via a user-definable threshold input that gates a non-maskable interrupt output. A reset is produced as the power supply decays to an out-of-tolerance condition.

During a power failure, the time period between the non-maskable interrupt and the reset allows for a "soft landing." Critical information held in registers, counters, pointers, etc. may be stored into the special SRAM, which operates as a true nonvolatile memory when connected to a 3V backup supply.

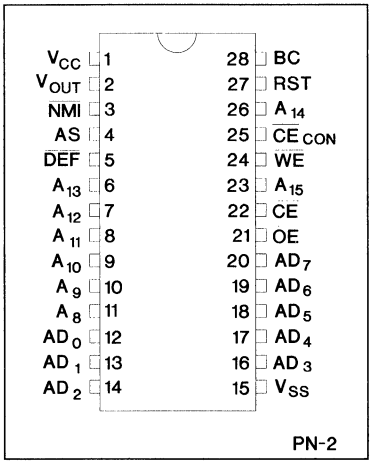
With its "cloaked" mode of access, the 2K byte PMU memory can be transparent to the system memory map, or it can occupy a nonoverlapped address block.

On power-up, the reset is held active for processor initialization. Critical information from the nonvolatile memory may be retrieved, and processing may resume at the point of the previous power-fail detection and/or in a manner incorporating specific information stored at power fail.

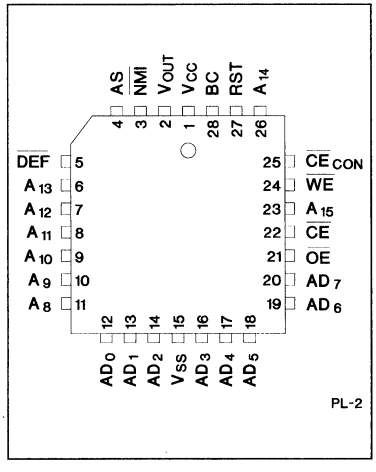
A watchdog function is also provided to verify valid execution during normal operation. The PMU is managed through eight control/status registers, which occupy the upper eight bytes of its internal 2K memory.

Pin Connections

28-Pin PDIP



28-Pin PLCC



Pin Names

AD_0–AD_7	Multiplexed address/data input/output
A_8–A_{15}	Address inputs
AS	Address strobe input
$\overline{DEF}$	Default setting override input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
$\overline{CE}$	Chip enable input
$\overline{CE}_{CON}$	Conditioned chip enable output
$\overline{NMI}$	Non-maskable interrupt output
RST	Reset output
BC	3 volt backup cell input
V_{OUT}	Supply output
V_{CC}	+5 volt supply input
V_{SS}	Ground

Pin Descriptions

AD_0–AD_7 Multiplexed address/data input/output

The bq1002 bus cycle consists of two phases: the address phase and the data-transfer phase. The address phase precedes the data transfer phase. During the address phase, low-byte address placed on AD_0–AD_7 is latched into the bq1002 on the falling edge of the AS signal. During the data-transfer phase, the AD_0–AD_7 pins serve as a bidirectional data bus.

A_8–A_{15} Address inputs

AS Address strobe input

For memory access operations, a falling edge on AS latches the address on AD_0–AD_7, demultiplexing the address data bus. For PMU memory "open" and "close" operations, a falling edge on AS is used to latch address data on AD_0–AD_7 and A_8–A_{15} into the address compare register (see Accessing PMU Memory).

$\overline{DEF}$ Default setting override input, active low

$\overline{DEF}$ is intended to be used as a user-interface input (pushbutton to ground). $\overline{DEF}$ pulled low forces the RST output active and returns all control and status registers to the default setting. The RST output remains active for time t_{RSW} after $\overline{DEF}$ returns inactive.

$\overline{OE}$ Output enable input, active low

$\overline{WE}$ Write enable input, active low

$\overline{CE}$ Chip enable input, active low

$\overline{CE}_{CON}$ Conditioned chip enable output

$\overline{NMI}$ Non-maskable interrupt output, active low

RST Reset output, active high

BC 3 volt backup cell input

V_{OUT} Supply output

V_{OUT} provides the higher of V_{CC} or BC, switched internally, to supply external RAM.

V_{CC} +5V supply input

V_{CC} provides the operating supply and is also the voltage comparison input for the V_{RST} and the V_{NMI} thresholds.

V_{SS} Ground.

Truth Table

Memory Mode	Memory State	Memory Address	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	$\overline{CE}_{CON}$	Power
Read	Open	PMU	L	H	L	D_{OUT}	H	Active
Write	Open	PMU	L	L	X	D_{IN}	H	Active
Output disabled	Open	PMU	L	H	H	High Z	H	Active
Not selected	Open	PMU	H	X	X	High Z	H	Standby
Not selected	Open	External	L	X	X	High Z	L	Standby
Not selected	Open	External	H	X	X	High Z	H	Standby
Not selected	Closed	X	L	X	X	High Z	L	Standby
Not selected	Closed	X	H	X	X	High Z	H	Standby

Functional Description

Special Internal Memory

The PMU contains 2K bytes of special static RAM that can be operated as nonvolatile memory and as "cloaked" memory. The upper 8 bytes of this memory are used for control and status monitoring. The remaining 2040 bytes of memory can be used to store critical data or program information during a power-down cycle. Cloaked memory, which is transparent from the main system memory map, can be used for general memory map expansion or for secure data fields.

Mapping PMU Memory

The 2K byte PMU memory can be mapped in several ways, depending on the system's physical address range. When used by a system that addresses a maximum of 64K bytes, the PMU is mapped as shown in Figure 1.

When used by a system that addresses greater than 64K bytes, the PMU memory may reside in any 64K byte segment starting on a 2K byte boundary. In either case, the PMU memory can occupy the upper (default) 2K or the lower 2K bytes of the 64K segment.

Accessing PMU Memory

The PMU memory may be accessed any time after it is opened. Opening the PMU memory involves performing three consecutive read or write cycles to a user-definable address location, followed by $\overline{CE}$ high. Note that if a write cycle is used to open PMU memory, data integrity at the accessed locations is not guaranteed.

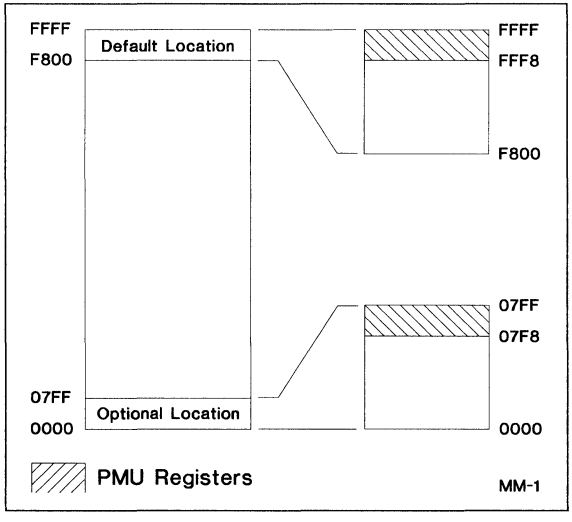


Figure 1. Memory Map

As address inputs AD_0 to AD_7 and A_8 to A_{15} are held valid, a high-to-low transition on the address strobe input, AS, latches the 16-bit address location into a compare register, independent of chip enable. The 2K byte PMU memory is accessible after three consecutive address matches are made, followed by $\overline{CE}$ high. The PMU memory occupies 2K of the 64K segment controlled by the PMU $\overline{CE}$ input.

Once opened, the PMU disables access to any external memory occupying the same 2K byte address space as its internal memory. This is achieved by unconditionally deactivating the $\overline{CE}_{CON}$ output. Access to memory locations outside the PMU memory space is available as usual.

Closing PMU Memory

PMU memory must be closed for either of the following purposes:

- To access external memory locations within PMU address space when:
  - PMU memory is open.
  - PMU memory address space overlaps that particular location of the external memory.
- To update contents of registers when:
  - PMU memory is open.
  - Registers are written.

Closing the PMU memory involves issuing a set of three consecutive read or write cycles to the same address used during the PMU open process, followed by $\overline{CE}$ high. The open and close address location is user-definable as described in the PMU Registers section. The default open and close address location is 07FF.

Any updates to PMU memory, including the PMU registers, are retained when PMU memory is closed. The PMU is reconfigured based on register updates only when the PMU memory is closed with a valid update pattern in the access control registers.

When the PMU is configured based on control register bit 3 = 1 (non-automatic open, default), and power-down occurs with the PMU memory open, the PMU memory is not accessible on power-up. To access the PMU memory from this state, a complete close cycle (three address matches followed by $\overline{CE}$ high) must precede the open cycle.

PMU Memory Nonvolatility

Nonvolatility is achieved by connecting a 3V backup supply to the PMU BC input pin. When V_{CC} falls to an out-of-tolerance condition, the PMU unconditionally write-protects its internal SRAM, independent of the state of the chip enable input, $\overline{CE}$. If a valid access is in process during power-fail detection, that memory cycle may continue to completion before the memory is write-protected. If the memory cycle is not terminated, the PMU unconditionally write-protects its memory within time t_{WPT}.

The out-of-tolerance voltage level is V_{RST}, which is the same level as set for RST. As the supply continues to fall below V_{RST}, the PMU memory is sustained by the external 3V source (lithium cell). On power-up, the PMU memory is held inactive for time t_{CER} (120 ms maximum) after the supply has reached V_{RST} to allow for processor initialization, independent of the state of the $\overline{CE}$ input.

Note that if no battery is provided, the BC pin must be grounded.

Power Failure Detection

Non-Maskable Interrupt Threshold

The PMU warns the host processor of an impending power failure and a return to full power via an output that can be used as a non-maskable interrupt. An internal precision comparator monitors supply input V_{CC} relative to an accurate internal voltage reference. Once the V_{CC} pin passes this reference voltage, $\overline{NMI}$ is forced active for the time period t_{NMW}. The V_{CC} input must be beyond the reference voltage for three consecutive 25µsec samples. The reference voltage is user-selectable as described in the PMU Registers section.

Note: $\overline{NMI}$ normally slews down with V_{CC}, but can be programmed to be held high as described in the PMU Registers section.

Power-Down/Power-Up Reset Threshold

The PMU also provides reset outputs when the supply voltage (V_{CC}) passes an out-of-tolerance threshold below which the system performance is questionable. A precision comparator monitors the supply at the V_{CC} pin relative to an internal reset voltage level (V_{RST}). The level of V_{RST} is user-selectable at nominal thresholds of 4.50V and 4.30V. V_{CC} must be beyond V_{RST} for three consecutive 25µsec samples. During power-down, RST is forced active as the supply falls below V_{RST}, and is held active as the supply continues to fall. RST slews down with the supply. During power-up, RST is held active for time t_{RSW} after $V_{CC} = V_{RST}$.

RST can be inhibited for nonvolatile processor operation as described in the PMU Registers section.

Watchdog

The PMU provides a watchdog function to monitor processor execution during power-valid operation. If the watchdog timer is enabled, then the PMU memory must be opened or closed during time t_{WTO}, or the watchdog timeout will take place.

The timeout period t_{WTO} is user-selectable as 125 ms, 500 ms, 2 sec, or infinity (i.e., disabled). The default setting configures a disabled watchdog monitor.

The watchdog timer can be programmed to output $\overline{NMI}$ instead of the default RST (as defined in the PMU Registers section).

External Nonvolatile SRAM Control

An external CMOS static RAM can be battery-backed using the control output pins from the PMU. As with the reset control feature, the PMU monitors the voltage level at the 5V V_{CC} input. As this voltage input decays below V_{RST}, the conditioned chip enable pin $\overline{CE}_{CON}$ is forced inactive independent of the chip enable input $\overline{CE}$. This activity unconditionally write-protects external SRAM as V_{CC} falls below V_{RST}. If a valid access is in progress during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated, the $\overline{CE}_{CON}$ output unconditionally write-protects the memory within time t_{WPT}.

The voltage level defined as out-of-tolerance is the same level as set for the reset output V_{RST}. As the supply falls below V_{BC} during an out-of-tolerance condition, an internal switching device forces V_{OUT} and $\overline{CE}_{CON}$ to the external 3V source. During power-up, V_{OUT} and $\overline{CE}_{CON}$ are switched back to the +5V supply as V_{CC} rises above V_{BC}. The $\overline{CE}_{CON}$ output is held inactive for time t_{CER} (120 ms max) after the supply has reached V_{RST}, independent of the $\overline{CE}$ input, to allow for processor initialization. During normal 5V operation, the $\overline{CE}$ input is passed through to $\overline{CE}_{CON}$ with a typical propagation delay of 7 ns.

Nonvolatility is achieved by hardware hookup as shown in Figure 2. If external SRAM nonvolatility is not required, the V_{OUT} and $\overline{CE}_{CON}$ outputs can be disabled as described in the PMU Registers section.

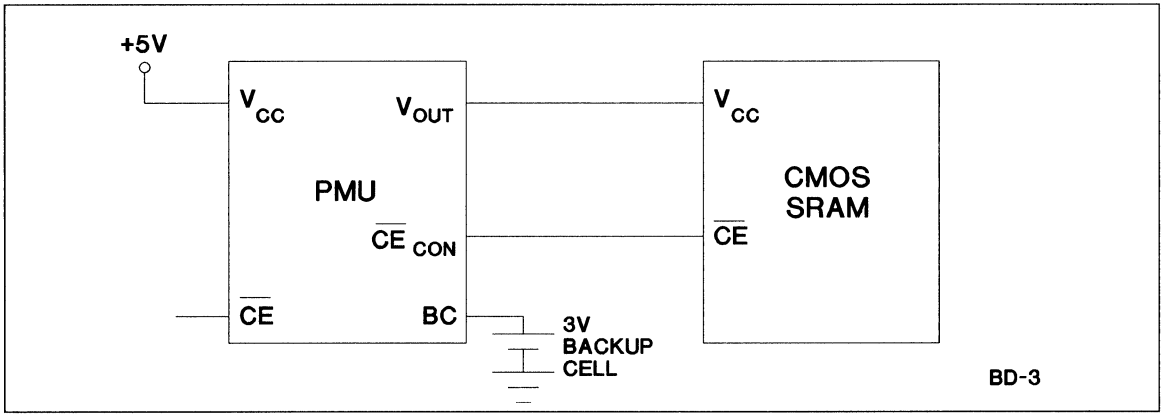


Figure 2. Hardware Hookup

Default Setting Override

The $\overline{DEF}$ input provides a manual override that changes all settings in control registers back to their defaults. It is intended to be used as a user-interface input (pushbutton to ground) and should not be driven by or connected to any active component. See the PMU Registers section.

When the $\overline{DEF}$ pin is forced active, the RST output is forced active. The RST output remains active for time t_{RSW} after $\overline{DEF}$ returns inactive. The $\overline{DEF}$ input can be used during valid 5V operation, or can be used in the data-retention mode ($V_{CC} < V_{BC}$). If the $\overline{DEF}$ pin is forced to ground while in data-retention mode, however, the external energy source at BC is loaded (approximately 10K ohms) while this pin is forced low.

PMU Registers

The PMU registers occupy the top eight bytes of the 2K PMU memory as shown in Figure 3. Once configured, these registers maintain valid settings in the event of power loss—provided the BC pin has a valid input.

Table 1 shows the PMU registers and their default settings. The PMU configures itself per the contents of these registers when closed with the valid update pattern in the access control registers.

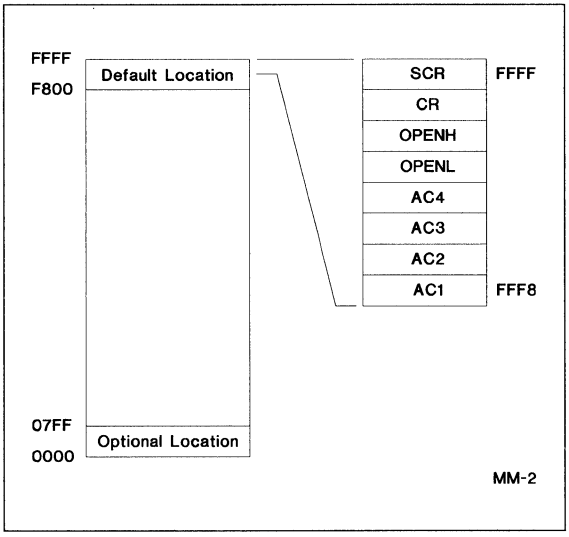


Figure 3. Default PMU Registers Location

Table 1. PMU Registers

Symbol	Name	Default Address	Default Bit Settings							
			7 (MSB)	6	5	4	3	2	1	0 (LSB)
AC1	Access control byte 1	FFF8	1	1	0	0	0	1	0	1
AC2	Access control byte 2	FFF9	1	0	1	0	0	1	1	0
AC3	Access control byte 3	FFFA	0	0	1	1	1	0	0	1
AC4	Access control byte 4	FFFB	0	0	1	0	1	0	1	1
OPENL	Open and close low byte	FFFC	1	1	1	1	1	1	1	1
OPENH	Open and close high byte	FFFD	0	0	0	0	0	1	1	1
CR	Control register	FFFE	0	0	1	1	1	0	1	-
SCR	Status/control register	FFFF	-	-	-	1	1	1	1	1

Access Control Registers (AC1–AC4)

Access control bytes 1–4 (AC1–AC4) contain access control information. All settings of other PMU registers are held to existing definitions until the PMU memory is closed with the access control registers written with the update pattern shown in Table 2.

The upper four PMU registers (SCR, CR, OPENH, and OPENL) can be read or written at any time, but the PMU does not recognize register updates until the PMU memory is closed with a valid update pattern in the access control registers. When the PMU is closed with a valid update pattern, AC1–AC4 are reset to the default settings.

During a control register update, at least one access control byte should be written prior to any changes to the upper four control bytes. If the update is disrupted before completion, the non-default access control pattern subsequently indicates that the control register data may not be the active setting. The update pattern for the remaining access control bytes should be written after the control registers are modified. This ensures that only a completed register update is recognized on closing.

Open and Close Location Registers (OPENH and OPENL)

Registers OPENH and OPENL contain the address location for opening and closing PMU memory. Register OPENH contains the high address byte; that is, address bits A_{15}–A_8. Register OPENL contains the low address byte, address bits A_7–A_0. Although these two bytes can be read or written at any time while PMU memory is open, they do not become active unless a valid update pattern is present as PMU memory is closed. Any new programmed address location becomes valid only after the PMU memory has been closed. The address location used to open the PMU memory must also be used to close it.

Table 2. Access Control Registers Update Pattern

Symbol	Name	Default Address	Valid Update Bit Settings							
			7 (MSB)	6	5	4	3	2	1	0 (LSB)
AC1	Access control byte 1	FFF8	0	0	1	1	1	0	1	0
AC2	Access control byte 2	FFF9	0	1	0	1	1	0	0	1
AC3	Access control byte 3	FFFA	1	1	0	0	0	1	1	0
AC4	Access control byte 4	FFFB	1	1	0	1	0	1	0	0

Control Register (CR)

The control register CR is used to program:

- $\overline{\text{NMI}}$ threshold voltage V_{NMI}
- Out-of-tolerance voltage V_{RST}
- Assertions of $\overline{\text{NMI}}$ and RST
- PMU memory location

The least-significant bit, bit 0, is not used.

CR Bit 1								
7	6	5	4	3	2	1	0	
-	-	-	-	-	-	1	-	Normal RST assertions
-	-	-	-	-	-	0	-	RST disabled

Bit 1 is used to inhibit the RST output from being active. The default setting of 1 in this bit provides normal operation for the reset output. If nonvolatility of the host processor is required, this bit can be cleared. This prevents the RST output from being active.

CR Bit 2								
7	6	5	4	3	2	1	0	
-	-	-	-	-	0	-	-	PMU memory at upper block
-	-	-	-	-	1	-	-	PMU memory at lower block

Bit 2 determines the location of the PMU memory within the 64K byte segment. If this bit is set to 0, the default setting, the PMU memory resides at the upper block. If set to 1, the PMU memory resides at the lower block.

CR Bit 3								
7	6	5	4	3	2	1	0	
-	-	-	-	1	-	-	-	Normal operation
-	-	-	-	0	-	-	-	Automatic open

Bit 3 enables the automatic opening of PMU memory. If this bit is set to 0, PMU memory is automatically opened on power-down when the monitored supply falls below V_{NMI}. If this method of operation is chosen, and a valid access to memory is in progress when power failure occurs, PMU memory is not opened until $\overline{\text{CE}}$ is high. PMU memory is also opened on subsequent power-up and must be closed for normal memory map allocation. The default setting of 1 at bit 3 presents normal operation during power-down/power-up, which necessitates the use of the PMU opening procedure if user access to PMU memory is required.

CR Bit 4								
7	6	5	4	3	2	1	0	
-	-	-	1	-	-	-	-	Normal operation
-	-	-	0	-	-	-	-	Output control

Bit 4 is used to control the RST and $\overline{\text{NMI}}$ outputs during power-down. When bit 4 is set to the default setting of 1, these outputs behave as described previously, and RST slews down with V_{CC}.

If bit 4 is written to 0:

- When V_{CC} is below V_{BC}, the battery holds $\overline{\text{NMI}}$ high.
- $\overline{\text{NMI}}$ is asserted on power-down and power-up as described previously.
- RST is not asserted on power-down, but is asserted on power-up.

For nonvolatile microprocessor operation, writing both bit 1 and bit 4 to 0 may be necessary.

CR Bit 5								
7	6	5	4	3	2	1	0	
-	-	1	-	-	-	-	-	V_{RST} = 4.30 V
-	-	0	-	-	-	-	-	V_{RST} = 4.50 V

Bit 5 is used to define the out-of-tolerance voltage, V_{RST}. The default setting of 1 in bit 5 defines V_{RST} as 4.30 volts. If this bit is set to 0, V_{RST} is 4.50 volts.

CR Bits 6 and 7								
7	6	5	4	3	2	1	0	
0	0	-	-	-	-	-	-	V_{NMI} = 4.60V
0	1	-	-	-	-	-	-	V_{NMI} = 4.75V
1	0	-	-	-	-	-	-	$\overline{NMI}$ disabled
1	1	-	-	-	-	-	-	$\overline{NMI}$ disabled

Bits 6 and 7 are used to define the voltage V_{NMI}. As determined by these bits, when the V_{CC} input pin falls below V_{NMI}, the $\overline{NMI}$ output is forced active. The default value of 0 in both bits selects V_{NMI} = 4.60V. The combinations are user-selectable as shown.

Status/Control Register (SCR)

The status/control register SCR contains $\overline{NMI}$ status bits, controls watchdog timeout and outputs, and sets the condition of the $\overline{CE}_{CON}$ and V_{OUT} outputs.

SCR Bit 0								
7	6	5	4	3	2	1	0	
-	-	-	-	-	-	-	1	V_{OUT} not forced high
-	-	-	-	-	-	-	0	External nonvolatile device

The least-significant bit, bit 0, determines the condition of the V_{OUT} output. The default setting of 1 defines V_{OUT} as not being used for an external nonvolatile device. That is, the V_{OUT} pin is not forced high by the battery after a power failure. If an external device (processor, SRAM, etc.) is to be made nonvolatile, this bit should be set to 0. If this setting is chosen, the V_{OUT} pin is held high by the battery as V_{CC} slews below the BC input.

SCR Bit 1								
7	6	5	4	3	2	1	0	
-	-	-	-	-	-	1	-	$\overline{CE}_{CON}$ not forced high
-	-	-	-	-	-	0	-	$\overline{CE}_{CON}$ forced high

Bit 1 is used to set the level of the conditioned chip enable signal $\overline{CE}_{CON}$ during power failure. If this bit is set to 1 (default), the $\overline{CE}_{CON}$ output is not held high by the battery during power failure. If $\overline{CE}_{CON}$ is to be held high (for write-protection of an SRAM designed for nonvolatility) during and throughout an out-of-tolerance condition, this bit must be set to 0.

SCR Bit 2								
7	6	5	4	3	2	1	0	
-	-	-	-	-	1	-	-	RST output
-	-	-	-	-	0	-	-	$\overline{NMI}$ output

Bit 2 of this control byte is used for defining which outputs are forced active when the watchdog timer is violated. If this bit is set to 1, the RST output is forced active at watchdog violation. If this bit is set to 0, the $\overline{NMI}$ output is forced active. The default setting is 1.

SCR Bits 3 and 4								
7	6	5	4	3	2	1	0	
-	-	-	1	1	-	-	-	Disabled
-	-	-	1	0	-	-	-	2 sec
-	-	-	0	1	-	-	-	500 msec
-	-	-	0	0	-	-	-	125 msec

Bits 3 and 4 of the control byte are used for setting the timeout period t_{WTO} for the watchdog monitor. The default setting of 11 disables the watchdog monitor. Other timeout periods are defined above.

SCR Bits 5, 6, and 7								
7	6	5	4	3	2	1	0	
1	-	-	-	-	-	-	-	Power fail
-	1	-	-	-	-	-	-	Watchdog violation
-	-	1	-	-	-	-	-	Power valid

The three most-significant bits, bits 5, 6, and 7, are real-time status bits that indicate the current power condition and software-execution condition of a given system.

Bits 5 and 7 are read-only bits that indicate the current power condition. If the V_{TH} or V_{CC} input pin (as selected) is above V_{NMI}, bit 5 is 1 and bit 7 is 0. If the input pin voltage falls below V_{NMI}, bit 5 is 0 and bit 7 is 1. That is, bits 5 and 7 are always complementary.

Bit 6 is a read/write bit that indicates whether or not a watchdog failure has occurred.

If the $\overline{NMI}$ output is forced active from a watchdog violation, and power failure is detected during the active $\overline{NMI}$ output pulse, the $\overline{NMI}$ output returns high following the $\overline{NMI}$ pulse width t_{NMW}, and is automatically forced low again within $t_{NMW}/2$. This automatic additional active pulse interrupts the processor due to a loss of power when this loss of power occurred during an active $\overline{NMI}$ condition as a result of the watchdog violation. If bit 6 is automatically written to 1 due to a watchdog failure, it can subsequently be cleared only by the user writing 0 to this location. The user cannot write a 1.

2

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
I_{OUT}	V_{OUT} current	150	mA	
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-10 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	V_{RST}	5.0	5.5	V	V_{RST} is user-selectable per PMU Registers section
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	
V_{BC}	Backup cell voltage	2.0	-	4.0	V	

DC Electrical Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 2	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 2	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -2.0 mA
V_{OHB}	V_{OH}, BC supply	V_{BC} - 0.3	-	-	V	$V_{BC} > V_{CC}$, I_{OH} = -10µA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{SB1}	Standby supply current (TTL)	-	7	15	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current (CMOS)	-	1	3	mA	$\overline{CE} \geq V_{CC}$ - 0.2V, $0V \leq V_{IN} \leq 0.2V$, or $V_{IN} \geq V_{CC}$ - 0.2V
I_{CC}	Operating supply current	-	45	70	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, I_{OH} = 0mA, I_{OL} = 0mA
V_{RST}	Reset trip point	V_{RST} - 0.06	V_{RST}	V_{RST} + 0.06	V	V_{RST} is user-selectable per PMU Registers section
V_{NMI}	NMI trip point	V_{NMI} - 0.06	V_{NMI}	V_{NMI} + 0.06	V	V_{NMI} is user-selectable per PMU Registers section and is monitored at V_{CC}.
V_{SO}	Supply switch-over voltage	-	V_{BC}	-	V	
I_{CCDR}	Data-retention current	-	0.1	1.0	µA	Does not include data-retention current provided through V_{OUT} to additional memory. T_A = 25°C, V_{BC} = 3V
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.3	-	-	V	I_{OUT} = 100mA
V_{OUT2}	V_{OUT} voltage	V_{BC} - 0.3	-	-	V	$V_{CC} < V_{BC}$, V_{OUT} enabled per PMU Registers section, I_{OUT} = 100µA
I_{OUT1}	V_{OUT} current	-	100	-	mA	$V_{OUT} > V_{CC}$ -0.3V
I_{OUT2}	V_{OUT} current	-	100	-	µA	$V_{OUT} > V_{BC}$ -0.3V, V_{OUT} enabled per PMU Registers section

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC} = 3V.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	10	pF	$V_{I/O}$ = 0V
C_{IN}	Input capacitance	-	-	8	pF	V_{IN} = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

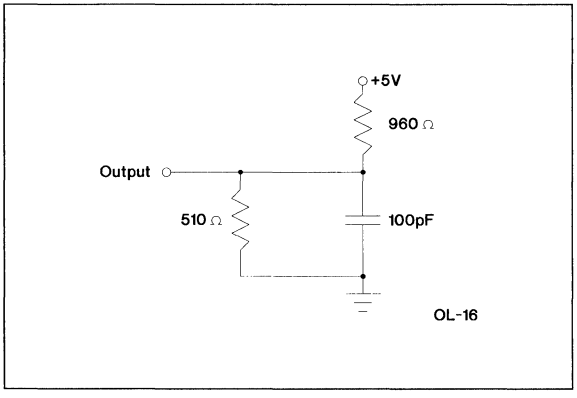


Figure 4. Output Load A

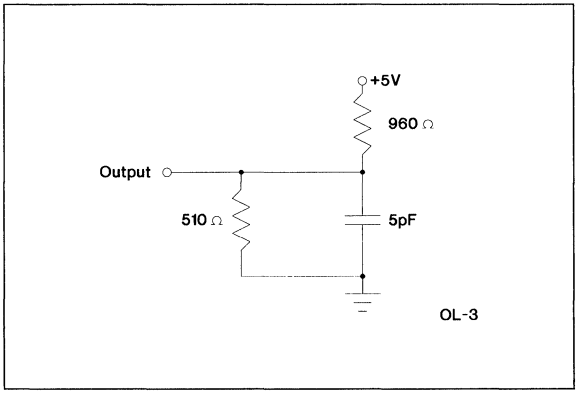
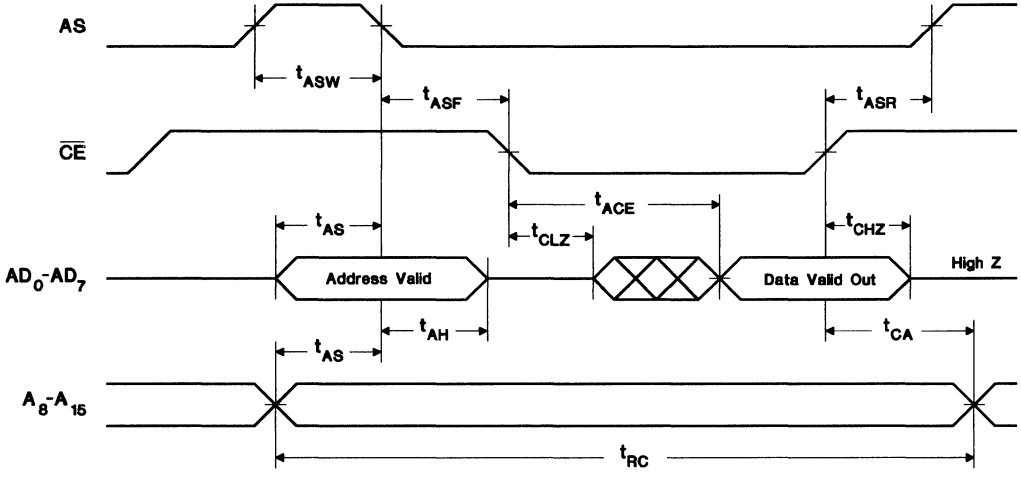


Figure 5. Output Load B

Read Cycle (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

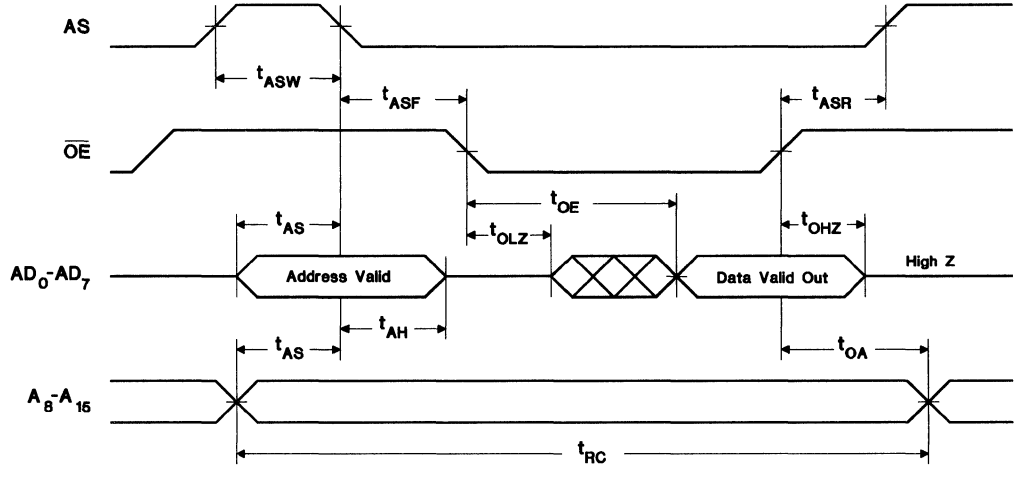
Symbol	Parameter	-45		-70		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	45	-	70	-	ns	
t_{ACE}	Chip enable access time	-	45	-	70	ns	Output load A
t_{OE}	Output enable access time	-	20	-	35	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	5	-	5	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	15	0	25	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	15	0	25	ns	Output load B
t_{ASW}	Address strobe width	20	-	20	-	ns	
t_{AS}	Address setup time	10	-	10	-	ns	
t_{AH}	Address hold time	0	-	0	-	ns	
t_{ASF}	Delay, AS fall to $\overline{CE}$, $\overline{OE}$	0	-	0	-	ns	
t_{ASR}	Delay, $\overline{CE}$, $\overline{OE}$ to AS rise	0	-	0	-	ns	
t_{OA}	Delay, $\overline{OE}$ to address change	0	-	0	-	ns	
t_{CA}	Delay, $\overline{CE}$ to address change	0	-	0	-	ns	

Read Cycle No. 1 ($\overline{CE}$ Access)[1,2]



RC-6

Read Cycle No. 2 ($\overline{OE}$ Access)[1,3]



RC-7

Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. $\overline{OE}$ = V_{IL}.
3. Device is continuously selected: $\overline{CE}$ = V_{IL}.

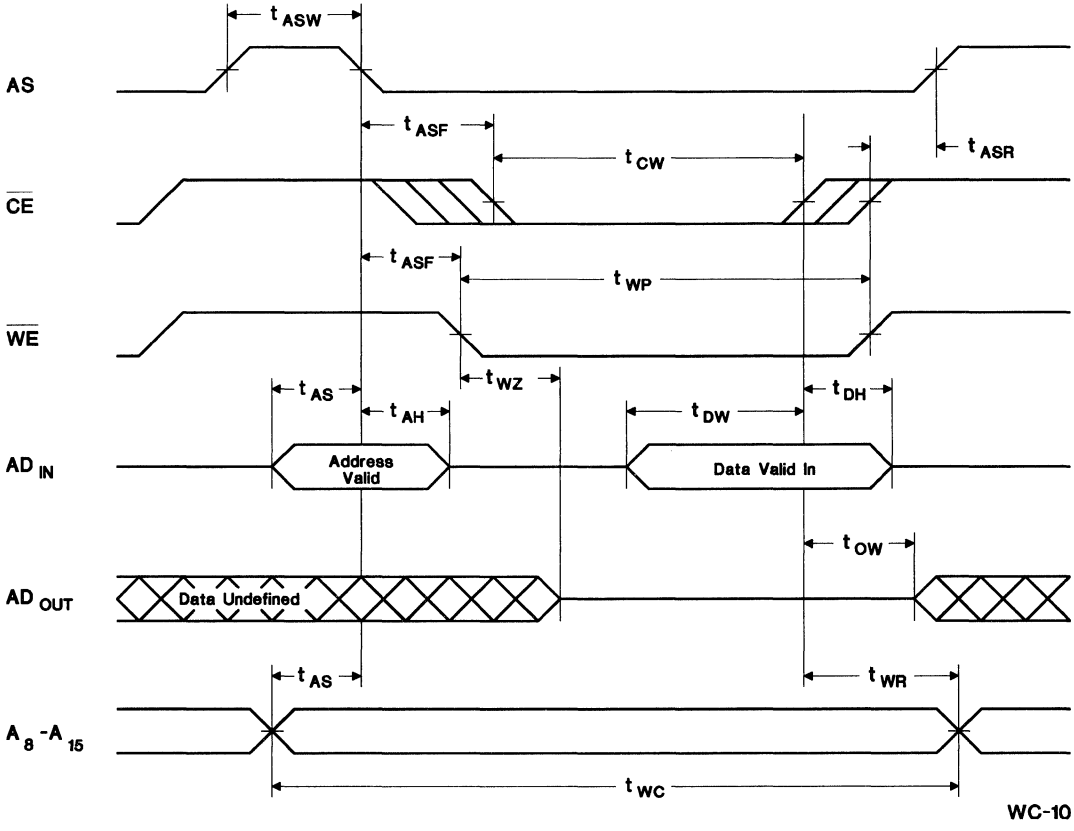
Write Cycle (TA = 0 to 70°C, VCC = 5V ± 10%)

Symbol	Parameter	-45		-70		Units	Conditions/ Notes
		Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	45	-	70	-	ns	
t_{CW}	Chip enable to end of write	40	-	60	-	ns	(1)
t_{WP}	Write pulse width	35	-	55	-	ns	Measured from beginning of write to end of write. (1)
t_{WR}	Write recovery time	3	-	5	-	ns	Measured from earlier of $\overline{CE}$ or $\overline{WE}$ going high to end of write cycle.
t_{DW}	Data valid to end of write	20	-	30	-	ns	Measured from first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH}	Data hold time	0	-	0	-	ns	Measured from first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{WZ}	Write enable to output in high Z	0	15	0	25	ns	I/O pins are in output state. (3)
t_{OW}	Output active from end of write	5	-	5	-	ns	I/O pins are in output state. (3)
t_{ASW}	Address strobe width	20	-	20	-	ns	
t_{AS}	Address setup	10	-	10	-	ns	
t_{AH}	Address hold time	0	-	0	-	ns	
t_{ASF}	Delay, AS fall to $\overline{CE}$, $\overline{WE}$	0	-	0	-	ns	
t_{ASR}	Delay, $\overline{CE}$, $\overline{WE}$ to AS rise	0	-	0	-	ns	

Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

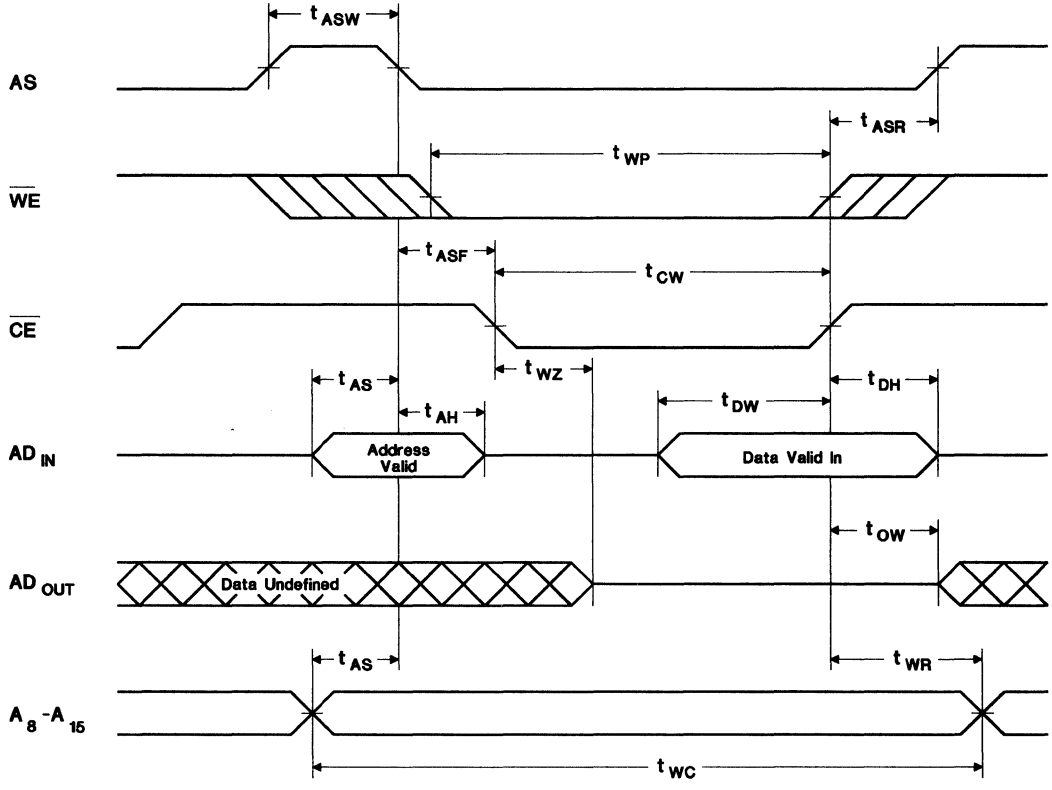
Write Cycle No. 1 ($\overline{WE}$-Controlled)



Notes:

1. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
2. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

Write Cycle No. 2 ($\overline{CE}$-Controlled)



WC-11

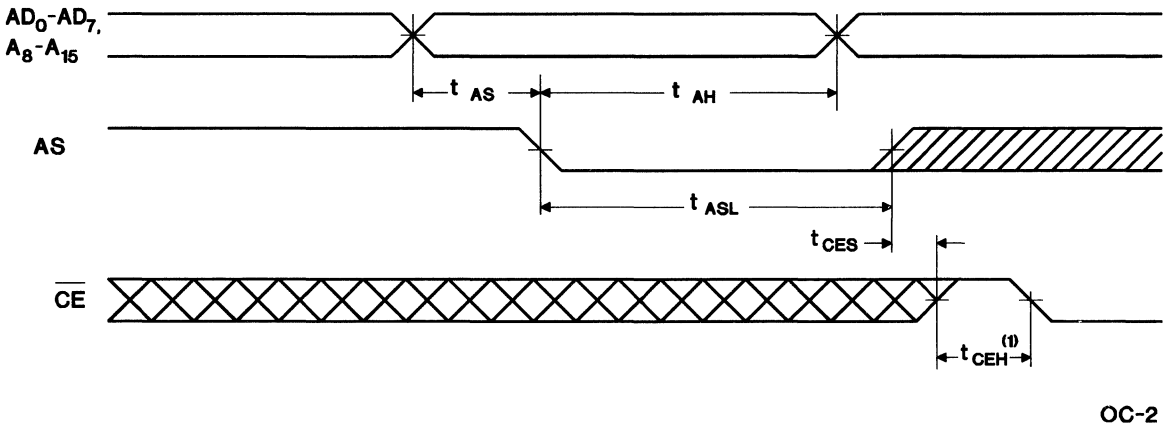
Notes:

1. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
2. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

Open and Close Cycle Timing

Symbol	Parameter	-45		-70		Unit
		Min.	Max.	Min.	Max.	
t_{AS}	Address setup time	10	-	10	-	ns
t_{ASL}	Address strobe low time	25	-	25	-	ns
t_{AH}	Address hold time	0	-	0	-	ns
t_{CEH}	Chip enable high following third strobe	5	-	5	-	ns
t_{CES}	Chip enable setup time	0	-	0	-	ns

Open and Close Cycle Timing



OC-2

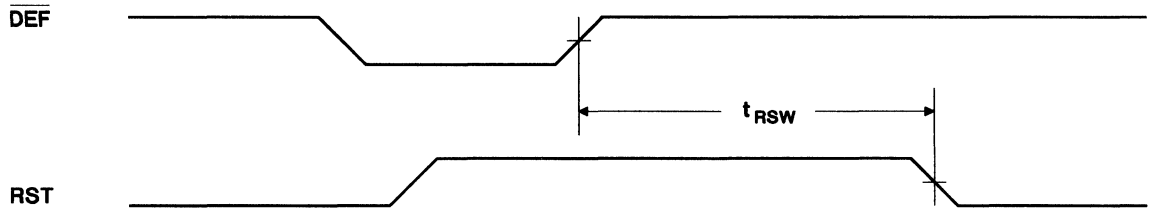
Note: 1. $\overline{CE}$ high following the third strobe completes the PMU open or close operation.

Power-Down/Power-Up and Watchdog Timing (TA = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{PFD}	V_{NMI} detect to $\overline{NMI}$	25	75	150	µs	
t_{NMW}	$\overline{NMI}$ pulse width	12	25	40	µs	
t_{NMR}	$\overline{NMI}$ asserted after RST inactive	50	150	200	µs	$V_{CC} > V_{NMI}$
t_{RST}	V_{RST} detect to RST	25	75	150	µs	Power-down/up sequencing per PMU Registers section.
t_{RSW}	RST pulse width	40	80	120	ms	
t_{PF}	V_{CC} slew, V_{NMI} to V_{RST}	40	-	400,000	µs	
t_{FS}	V_{CC} slew, 4.25V to V_{SO}	10	-	-	µs	
t_{VRS}	V_{CC} valid to RST	25	75	150	µs	Power-down/up sequencing per PMU Registers section.
t_{PU}	V_{CC} slew, V_{RST} to V_{NMI}	0	-	-	µs	
t_{CED}	Chip enable propagation delay	-	7	10	ns	
t_{CER}	Chip enable recovery	-	t_{RSW}	-	ms	t_{CER} is time required after power-valid to allow for processor stabilization.
t_{WPT}	Write-protect time	40	100	150	µs	Write-protect occurs internally and by bringing $\overline{CE}_{CON}$ high.
t_{WTO}	Watchdog timeout period	0.5 t_{WTO}	t_{WTO}	1.5 t_{WTO}	-	t_{WTO} is user-selectable per PMU Registers section.

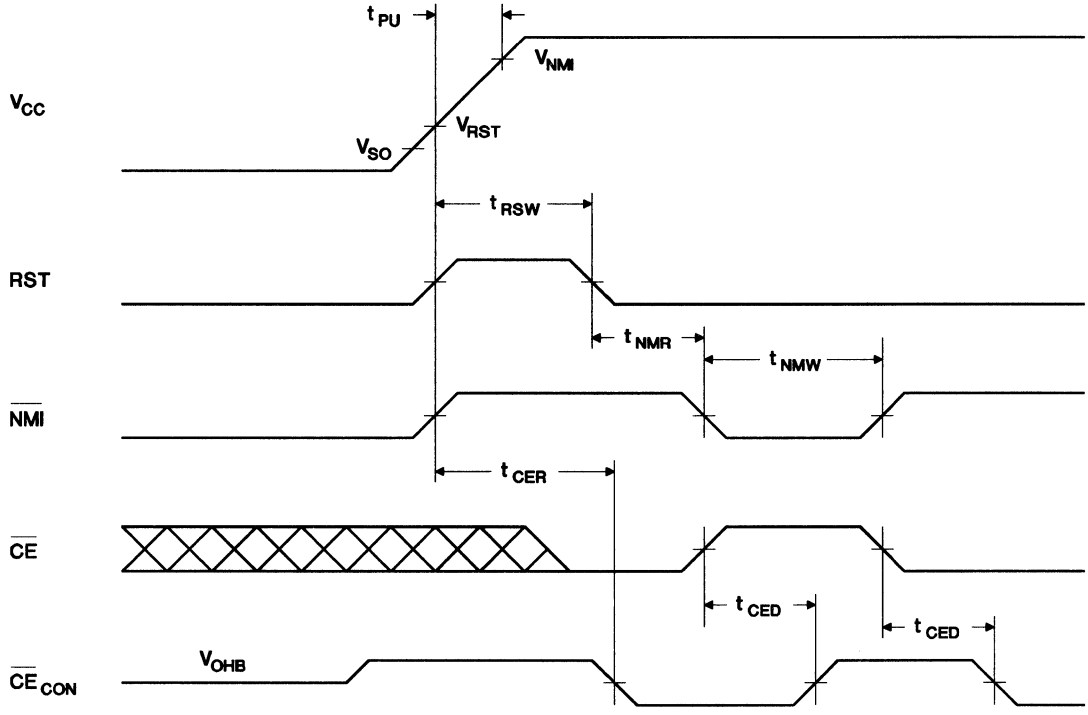
Note: Typical values indicate operation at T_A = 25°C.

$\overline{DEF}$ Timing



DEF-2

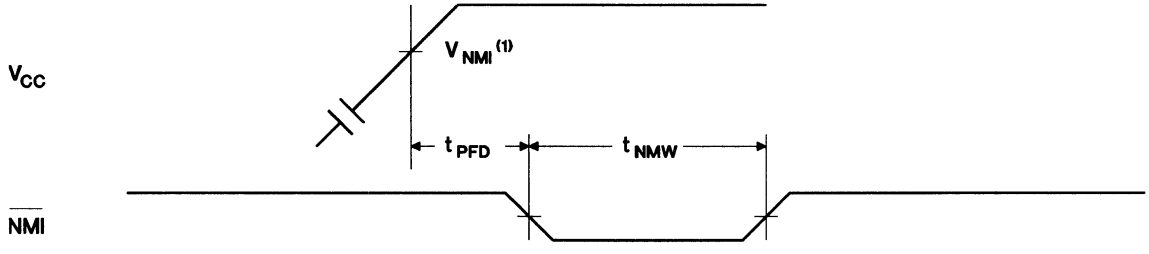
Power-Up Case 1: $\overline{NMI}$ Delayed by RST Active



PU-6

Note: 1. SCR bit 1 = 0.

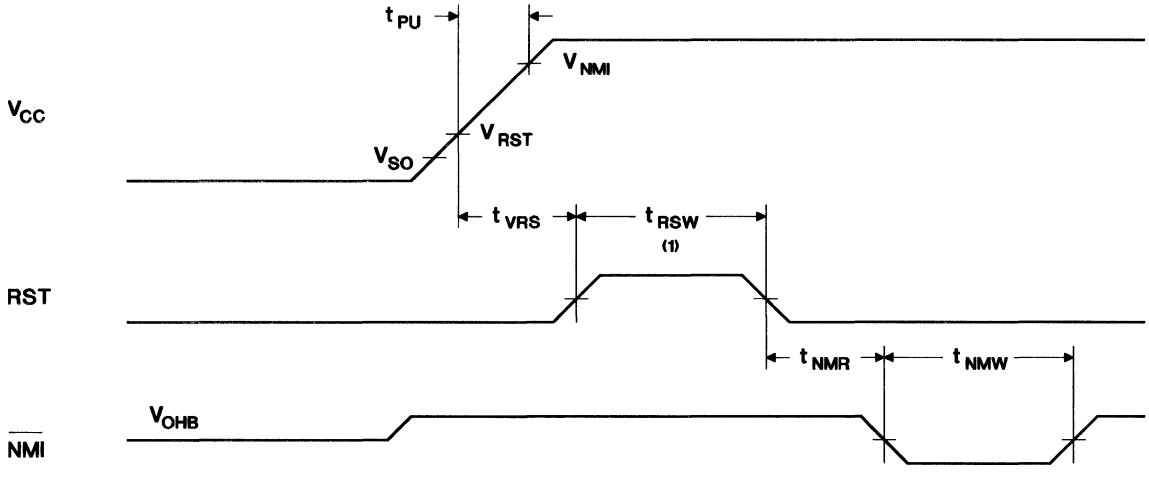
Power-Up Case 2: $\overline{NMI}$ Not Delayed



PU-7

Note: 1. RST is inactive before V_{NMI} is reached.

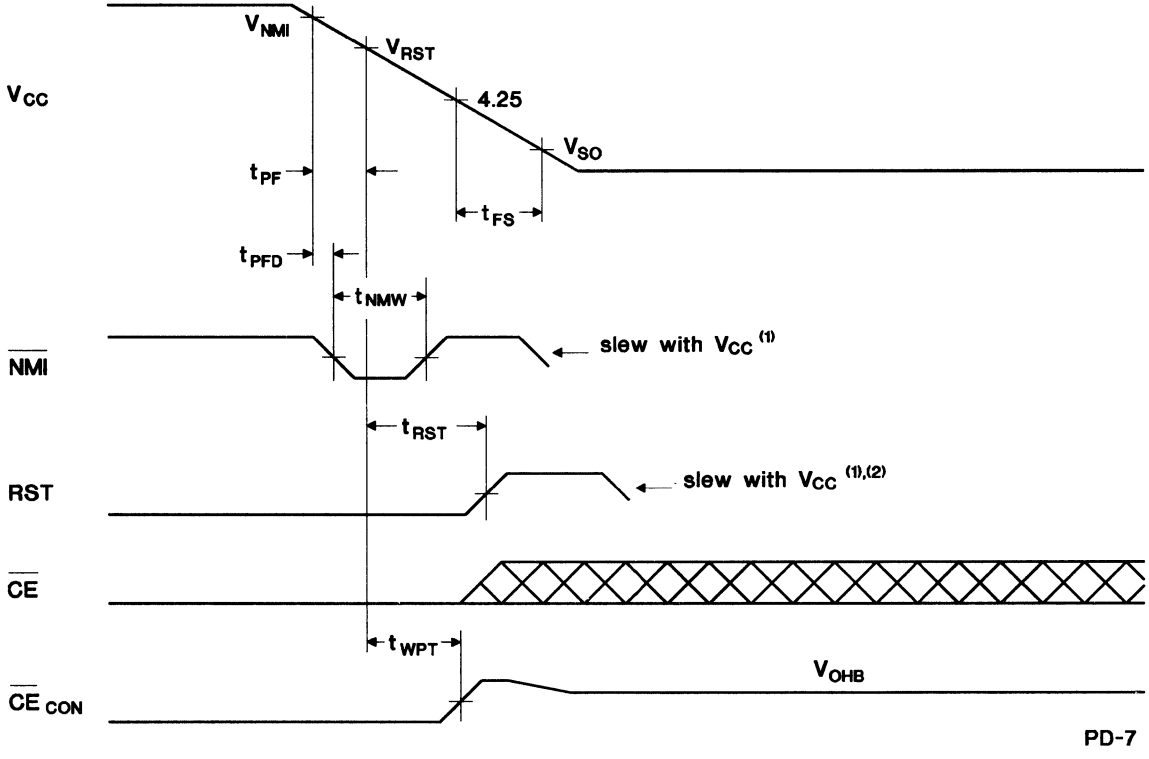
Power-Up Case 3: Power-Up With CR Bit 4 = 0



PU-8

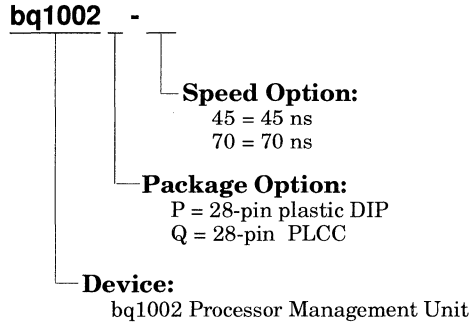
Note: 1. CR bit 1 = 1; RST goes active on power-up.
If CR bit 1 = 0, RST is disabled.

Power-Down Case: Under V_{CC} Sensing



Note:
1. CR bit 4 = 1.
2. CR bit 1 = 1.
3. SCR bit 1 = 0.

Ordering Information



BENCHMARQ

Designing With the PMU

Using the bq1001/bq1002

Introduction

This design note is provided to simplify the design of systems using the bq1001 or bq1002 Processor Management Unit (PMU). Use this note with the bq1001 or bq1002 data sheet.

The PMU provides the functionality of a microprocessor supervisory circuit and 2K bytes of nonvolatile SRAM. Unlike other supervisory circuits, the PMU operation is configured and controlled through a set of eight control/status registers. These registers occupy the top eight bytes of the 2K byte PMU memory. This makes accessing PMU memory a significant aspect of the design.

The design issues discussed here are grouped under the following topics:

- Memory interface
  - Hardware
  - Software
- Microprocessor supervisor interface
  - Power-fail/power-recovery detection
  - Reset generation
  - Nonvolatile memory control
  - Watchdog monitor

Wherever necessary, design concepts are supported by logical diagrams and assembly-code listings for representative microprocessors and microcontrollers. Numbers related to address space are expressed in hexadecimal.

Memory Interface

The 2K byte PMU memory has the following characteristics:

- 2040 bytes for general storage and 8 bytes for control registers
- Nonvolatile when operated with a 3V backup source
- Relocatable within a 64K address space
- Controlled access

Nonvolatility of PMU memory is essential for proper device operation through power-down/power-up cycles. Integral control circuitry makes PMU memory nonvolatile when the BC pin is connected to a 3V backup source.

PMU memory can be located at the top or bottom 2K block of the 64K segment as shown in Figure 1. The 64K segment is any segment within the system address space that starts on a 2K boundary. The default PMU memory location is at the top of the 64K segment.

PMU memory can exist in either "open" or "closed" state. PMU memory is accessible only in the open state. PMU memory is not accessible in the closed state.

PMU memory is opened or closed by performing three consecutive address match cycles followed by $\overline{CE}$ high. During an address match, address data on the 16 address lines is latched into a 16-bit compare register on the falling edge of ACS (AS for bq1002). The 16 address lines of the bq1001 are A_0–A_{15}; the bq1002 address lines are AD_0–AD_7 and A_8–A_{15}. The latched address is compared with the configured open/close address in registers OPENH and OPENL. When three consecutive matches are made, the PMU memory switches states following $\overline{CE}$ high.

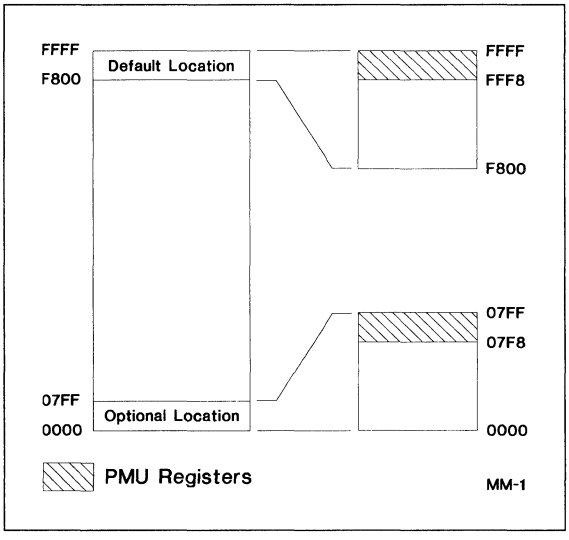


Figure 1. Memory Map

Memory Interface Hardware

The bq1001 memory interface is typical of that for an SRAM. The interface for the bq1002 is similar to that of an SRAM with an integral address latch. In either case, the logic for generating $\overline{CE}$ and ACS (AS for bq1002) requires some special consideration.

$\overline{CE}$ Logic

The logic circuit for generating $\overline{CE}$ is dictated by two PMU memory attributes.

- Ability to exist in either open or close state.
- Ability to decode its own address space within the 64K segment.

These attributes suggest two distinct logic circuits for $\overline{CE}$ depending on system address space.

- For systems that address a maximum of 64K bytes, drive $\overline{CE}$ of PMU with either a data strobe or an address strobe, whichever is easily available. This follows from the open/close requirement that $\overline{CE}$ must be high at the end of an open/close cycle. When used this way, any address decode logic required for other devices in the system should gate the $\overline{CE}_{CON}$ output of the PMU to avoid bus contention.
- For systems that address beyond 64K, the address decode logic for the PMU should ensure that $\overline{CE}$ is low for the PMU 64K segment. Any address decode logic required for devices that are mapped within the 64K segment should gate the $\overline{CE}_{CON}$ output of the PMU to avoid bus contention.

Regardless of the address space, if the PMU and external SRAM are the only devices that share the PMU 64K address space, then $\overline{CE}_{CON}$ can directly drive the $\overline{CE}$ of the external memory device.

ACS/AS Logic

The ACS pin on the bq1001 is responsible only for the PMU memory open/close operation. On the bq1002, AS serves two purposes: latching the open/close address and demultiplexing the address/data bus, AD_0–AD_7. To keep hardware/software overhead to the minimum, it is suggested that a write data strobe signal ($\overline{WR}$ for the Intel bus) be used to drive the logic for ACS/AS during an open/close operation.

"Cloaking" PMU Memory

The ability to open/close allows PMU memory to reside within the same address space as external memory. This is accomplished by using the conditioned chip-enable output ($\overline{CE}_{CON}$) of the PMU to drive the $\overline{CE}$ logic of external memory (see Figures 2 and 3). PMU memory is cloaked (or transparent) when used in this way.

Table 1 summarizes PMU memory cloaked operation for the circuit shown in Figure 2. As shown in the last row of Table 1, PMU memory shadows the top 2K bytes of the 8K x 8 SRAM.

Cloaked mode of operation requires that:

- $\overline{CE}$ of the PMU is active for both the PMU and external SRAM address space
- $\overline{CE}$ logic of external SRAM is driven by the $\overline{CE}_{CON}$ output of the PMU.

Table 1. PMU Memory Cloaked Operation

PMU Memory	Address Space	PMU Memory	External Memory
Closed	XXXX-XXXX	Not accessible	Accessible if addressed
Open	E000-F7FF	Not accessible	Accessible
Open	F800-FFFF	Accessible	Not accessible

X = Any hexadecimal digit.

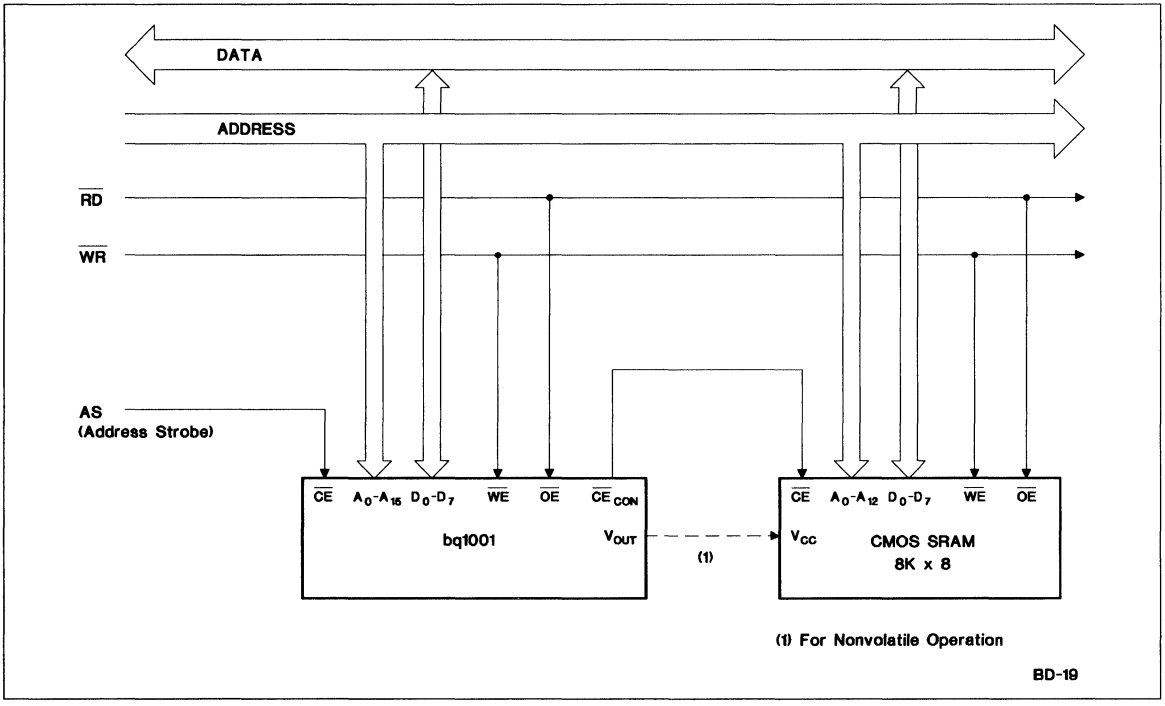


Figure 2. Example of PMU Setup in Cloaked Mode

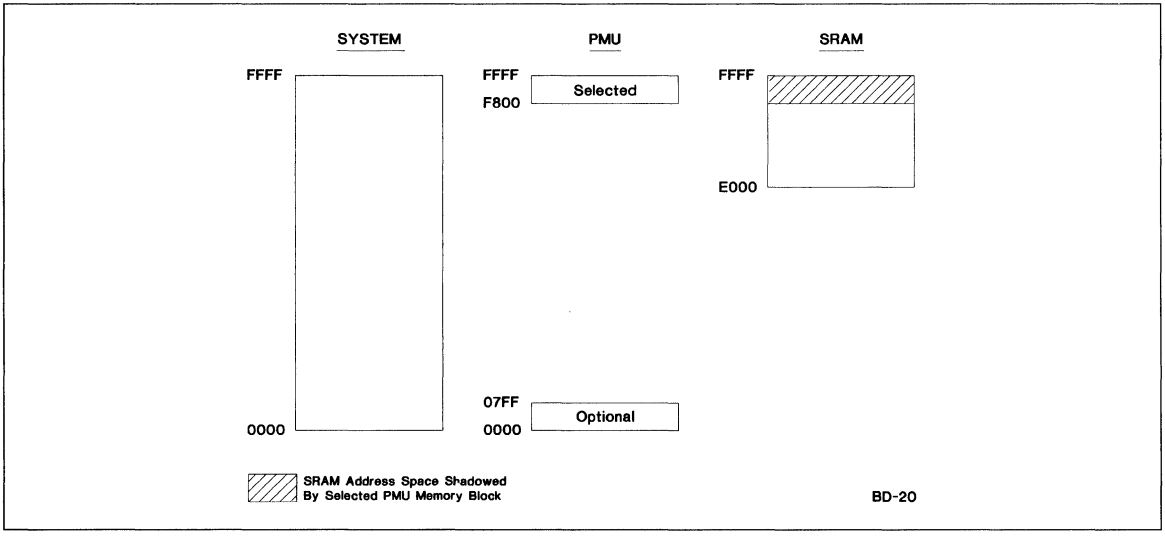
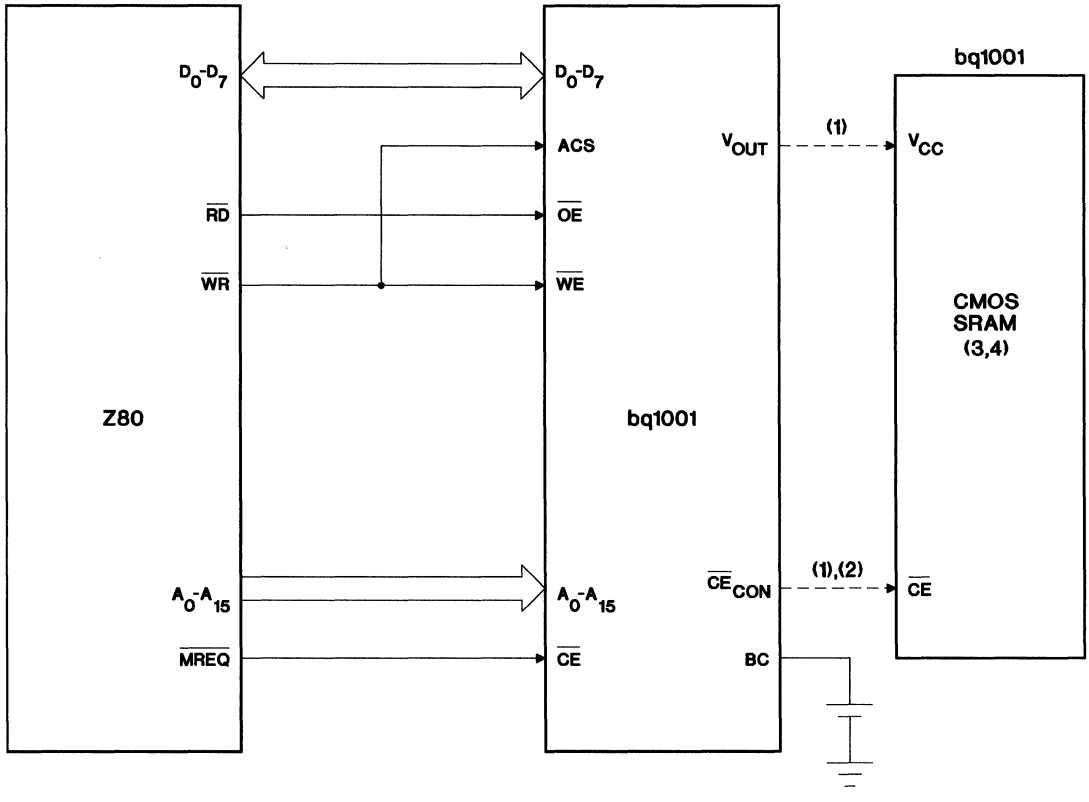


Figure 3. Address Map of Circuit Shown in Figure 2

Microprocessor Interfaces

The following figures illustrate typical PMU interfaces to common microprocessors.

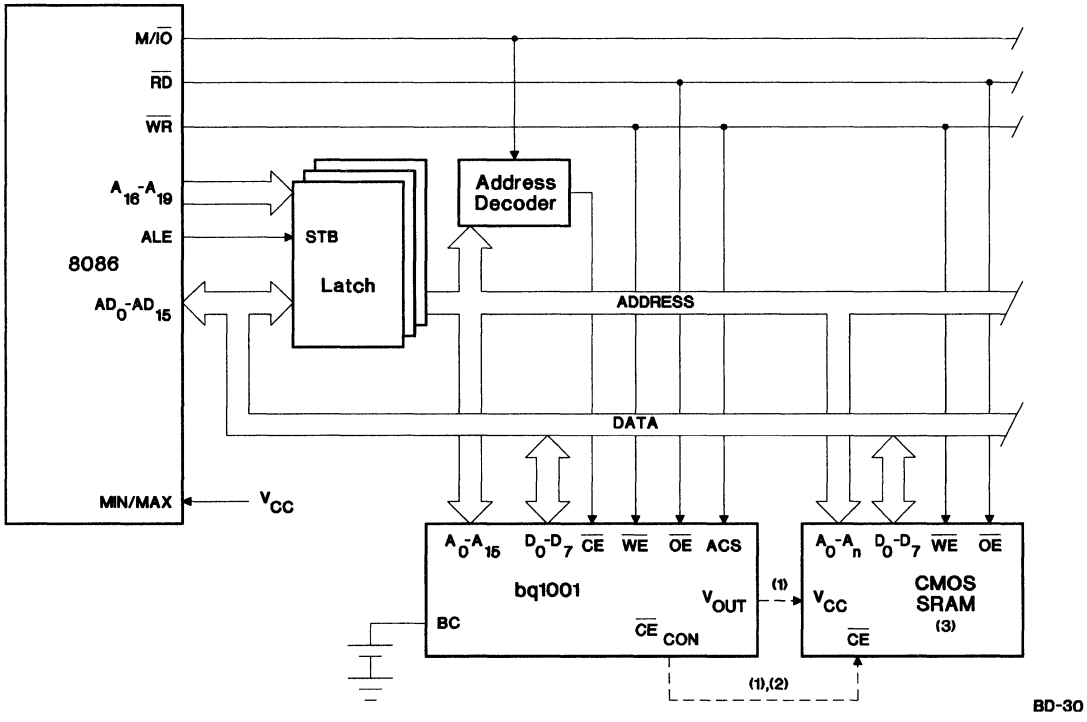
bq1001 to 8-Bit Microprocessors: Zilog Z80®



BD-21

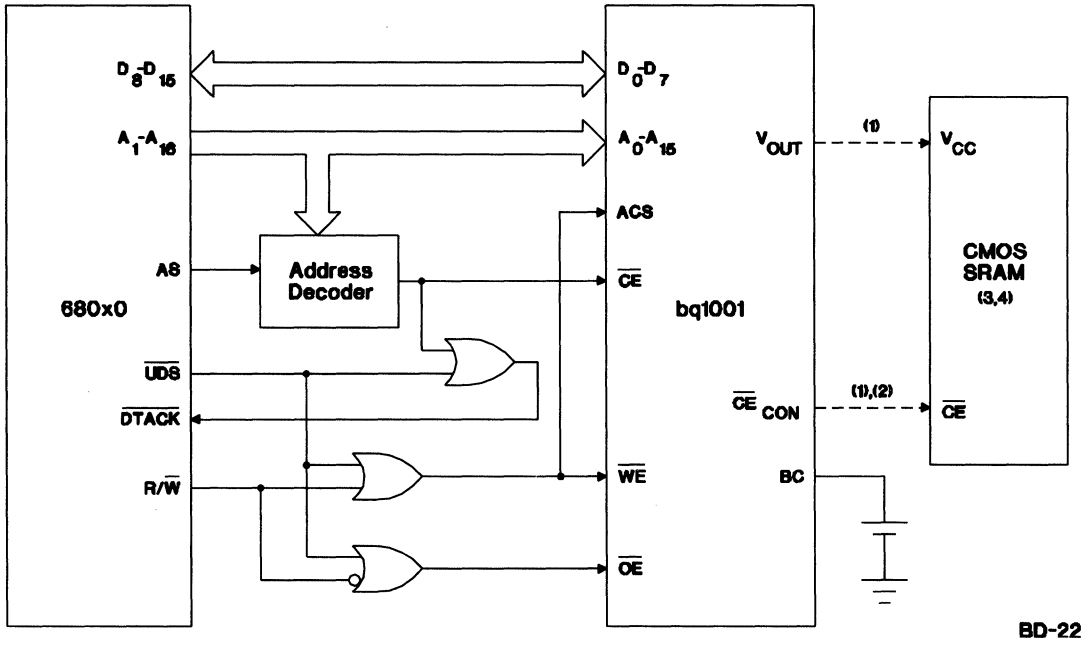
Notes:
1. For nonvolatile control of external SRAM.
2. For cloaked mode of operation.
3. If this is not the only device, an address decoder gated with $\overline{CE}_{CON}$ should be used.
4. Address and data bus per standard connection to CMOS SRAM.

bq1001 to 16-Bit Microprocessors: Intel® 80x86



Notes:
1. For nonvolatile control of external SRAM.
2. For cloaked mode of operation.
3. If this is not the only device, an address decoder gated with $\overline{CE}_{CON}$ should be used.

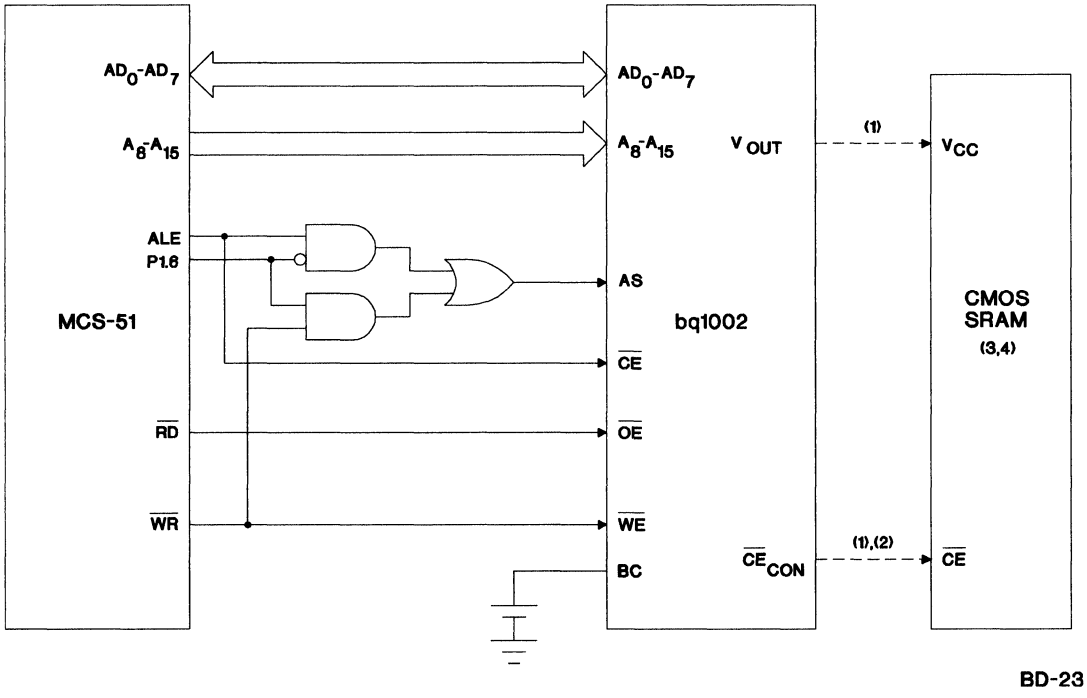
bq1001 to 16-Bit Microprocessors: Motorola 680x0



Notes:

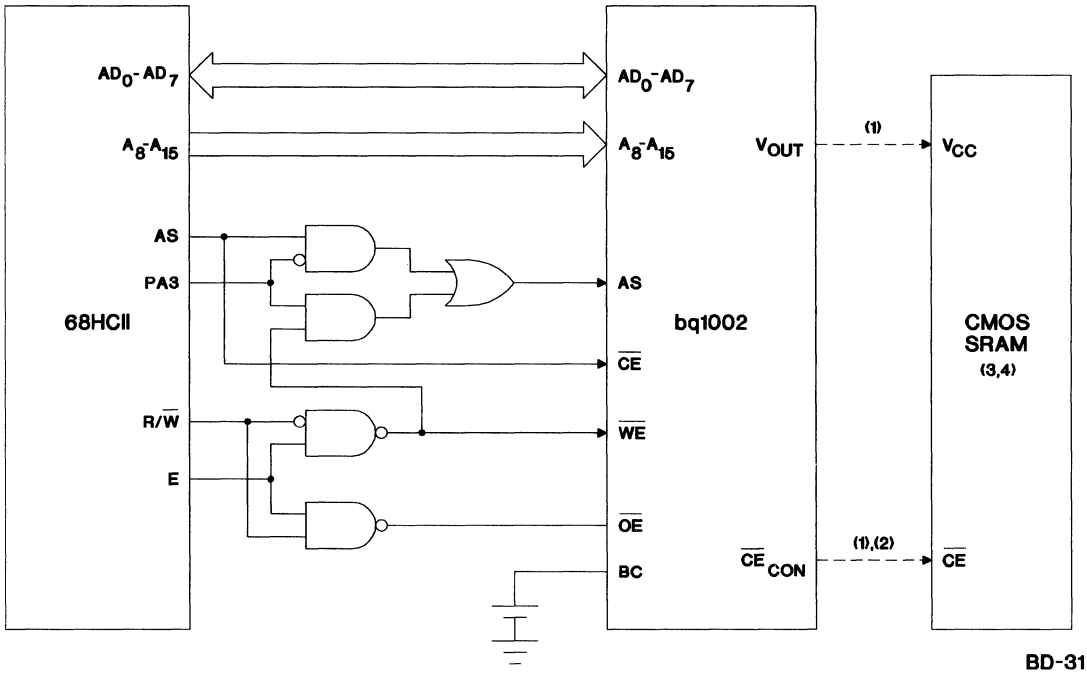
1. For nonvolatile control of external SRAM.
2. For cloaked mode of operation.
3. If this is not the only device, an address decoder gated with $\overline{CE}_{CON}$ should be used.
4. Address and data bus per standard connection to CMOS SRAM.

bq1002 to 8-Bit Microcontrollers: Intel® MCS®-51



Notes:
1. For nonvolatile control of external SRAM.
2. For cloaked mode of operation.
3. If this is not the only device, an address decoder gated with $\overline{CE}_{CON}$ should be used.
4. Address and data bus per standard connection to CMOS SRAM.

bq1002 to 8-Bit Microcontrollers: Motorola 68HC11



Notes:

1. For nonvolatile control of external SRAM.
2. For cloaked mode of operation.
3. If this is not the only device, an address decoder gated with $\overline{CE}_{CON}$ should be used.
4. Address and data bus per standard connection to CMOS SRAM.

Memory Interface Software

The software design for the PMU memory interface is concerned with:

- PMU initialization
- Power-fail operation
- Opening and closing PMU memory

The control/status registers occupy the top eight bytes of the 2K PMU memory, as shown in the memory map of Figure 4. These registers control the following:

- Location of the 2K PMU memory block
- Open/close address and auto-open mode of PMU memory
- Nonvolatile control of external SRAM
- Microprocessor supervisory functions

When power is first applied, these registers are set to their default values, and PMU memory comes up in a closed state. The default open/close address is set at 07FF. The default PMU memory location is the top 2K block of the 64K segment.

PMU Initialization

On first power-up, the PMU may be initialized to meet application and system requirements. This may also be necessary when the $\overline{DEF}$ pin has been activated or when the PMU needs to be reconfigured at any time after power-up.

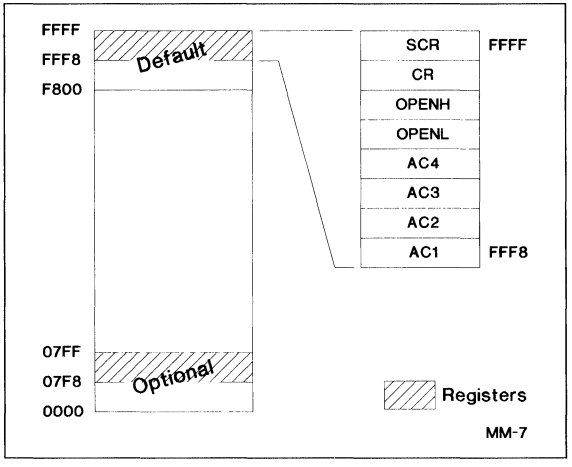


Figure 4. Memory Map of PMU Registers

The following steps are recommended to accomplish PMU initialization/configuration:

1. Open PMU memory.
2. Write the valid update pattern (see the data sheet) in register AC1.
3. Write new values to SCR, CR, OPENH, and OPENL as required.
4. Write the valid update patterns to the remaining registers AC2–AC4.
5. Close PMU memory.

After the last step, registers AC1–AC4 are returned to their default pattern. This default pattern in the AC1–AC4 registers indicates that PMU operation conforms to existing settings in the top four control registers. If the above steps are followed, any other pattern in AC1–AC4 indicates that values in the control registers may not be as intended.

Power-Fail Operation

The power-fail notification signal (NMI) generated by the PMU may initiate the following:

1. Open PMU memory.
2. Save the contents of registers, counters, and other critical data in the 2040 bytes of PMU memory or external nonvolatile memory.
3. Close PMU memory.

If the PMU is configured for auto-open (bit 3 of CR = 0), step 1 is not necessary; PMU memory is automatically opened after the NMI threshold is detected on power-down and after Vcc reaches V_{RST} on power-up (see sections on microprocessor supervisor interface).

If PMU memory is not configured for auto-open and PMU memory is open when V_{CC} becomes invalid, then PMU memory enters a semi-closed state.

To access PMU memory not configured for auto-open after the PMU has cycled through power-fail and recovery, follow this procedure.

1. Call the open/close routine described in the following section.
2. Read the PMU OPENH, OPENL registers.
   - If the contents match the configured open/close address, then PMU memory is open.
   - If the contents don't match, then PMU memory is closed. Repeat step 1 to open PMU memory.
3. Set a flag, say open_close_flag, to indicate status of PMU memory: 1 = open 0 = closed.

Once the PMU memory state is established on power-up, successive calls to the open/close routine should toggle the flag bit, to avoid inadvertent problems related to PMU memory access.

Opening and Closing PMU Memory

One subroutine is called to perform both the open and close operations.

The assembly-language code in each of the five following listings opens or closes PMU memory when used with the corresponding hardware interface illustrated in the logic diagrams.

For the memory interface between the bq1002 to 8-bit microcontrollers, ensure that the open/close address is outside the PMU memory address space. If this is not observed, data at the open/close address may be corrupted.

bq1001 to 8-Bit Microprocessors: Zilog Z80®

```
1
2                PUBLIC   OPENCLOSE
3
4   OPNCLSADR    EQU 07FFH          ;default open/close address
5                                   ;
6   OPENCLOSE:                      ;open/close routine begins here
7                DI                 ;disable interrupts
8                LD  HL,OPNCLSADR   ;load HL with open/close address
9                LD  A,(HL)         ;save contents at open/close address
10               LD  (HL),A         ;write contents of reg. A
11               LD  (HL),A         ;to the open/close address three
12               LD  (HL),A         ;consecutive times, restoring data
13               EI                 ;enable interrupts
14               RET                ;return
15
```

bq1001 to 16-Bit Microprocessors: Intel®80x86

```
1     _TEXT    SEGMENT
2                                          ;
3   OPENCLOSE  PROC                        ;open/close routine begins here
4      CLI                                 ;inhibit interrupts
5      PUSH  DS                            ;save contents of DS
6      LDS   BX,DWORD PTR CS:OPNCLSADR     ;load DS:BX with open/close address
7      MOV   AL,[BX]                       ;save the contents at OPNCLSADR
8      MOV   [BX],AL                       ;write the saved contents
9      MOV   [BX],AL                       ;to open/close address
10     MOV   [BX],AL                       ;three consecutive times
11     POP   DS                            ;restore DS
12     STI                                 ;enable interrupts
13     RET                                 ;return
14  OPENCLOSE  ENDP                        ;
15                                         ;
16  OPNCLSADR:  DW   07FFH * 2             ;allign open/close address
17              DW   0000H                 ;to fall on even boundary
18                                         ;
19    _TEXT     ENDS
```

bq1001 to 16-Bit Microprocessors: Motorola 680x0

```
 1
 2  OPNCLSADR   EQU   $07FF * 2          ;align open/close address
 3                                       ;to fall on even boundary
 4                                       ;
 5                                       ;
 6  OPENCLOSE   LINK    A6,#0            ;open/close routine begins here
 7              ORI     #$0700,SR        ;disable interrupts
 8              MOVEA   #OPNCLSADR,A0    ;
 9              MOVE.B  (A0),D0          ;save contents at OPNCLSADR
10              MOVE.B  D0,(A0)          ;write saved contents back
11              MOVE.B  D0,(A0)          ;to open/close address
12              MOVE.B  D0,(A0)          ;three consecutive times
13              ANDI    #$F8FF,SR        ;enable interrupts
14              UNLK    A6               ;delete stack frame
15              RTS                      ;return
```

bq1002 to 8-Bit Microcontrollers: Intel®MCS®-51

```
 1  OPENCLOSE:                          ;open/close routine begins here
 2          ORL   PSW,#18H              ;switch to alternate register set
 3  ;
 4          MOV   DPTR,#07FFH           ;open/close address
 5  ;
 6          MOV   R1,IE                 ;clear interrupt
 7          MOV   IE,#0                 ;enables__
 8          SETB  P1.6                  ;select WR
 9          MOVX  A,@DPTR               ;save contents at
10          MOV   RO,A                  ;open/close address
11          MOV   A,#0FFH               ;low byte of open/close address
12  ;
13          MOVX  @DPTR,A               ;write to open/close
14          MOVX  @DPTR,A               ;address three
15          MOVX  @DPTR,A               ;times
16  ;
17          MOV   A,R0                  ;restore contents at
18          MOVX  @DPTR,A               ;open/close address
19  ;
20          CLR   P1.6                  ;select ALE
21          MOV   IE,R1                 ;enable interrupts
22  ;
23          ANL   PSW,#OE7H             ;restore register set
24          RET                         ;return
```

bq1002 to 8-Bit Microcontrollers: Motorola 68HC11

```
 1
 2   OPNCLSADR     EQU     $07FF        ;default open/close address
 3   REGBASE       EQU     $1000        ;SFR base address
 4                                      ;
 5   OPCLINIT      EQU     *            ;set up port A bit 3 for open/close
 6                 LDX     #REGBASE     ;load reg X with SFR base address
 7                 BCLR    $20,X $03    ;disconnect timer from PA3
 8                 RTS                  ;return
 9                                      ;
10   OPENCLOSE     EQU     *            ;open/close routine begins here
11                 SEI                  ;inhibit interrupts
12                 LDAB    OPNCLSADR    ;save the contents at OPNCLSADR
13                 LDAA    #$FF         ;load acc. A with the l.s.byte of $07FF
14                 BSET    0,X $08      ;set port A bit 3, PA3-select write strobe
15                 STAA    OPNCLSADR    ;write contents of acc. A to
16                 STAA    OPNCLSADR    ;location OPNCLSADR, three
17                 STAA    OPNCLSADR    ;consecutive times
18                 BCLR    0,X $08      ;clear port A bit 3, PA3-select address strobe
19                 STAB    OPNCLSADR    ;restore contents at OPNCLSADR
20                 CLI                  ;enable interrupts
21                 RTS                  ;return
22                                      ;
```

Summary

The following is a list of situations where closing PMU memory is necessary for proper operation:

- Need to access external memory location within PMU address space:
  - PMU memory is already open.
  - PMU memory address space overlaps that particular location of external memory.
- Need to update contents of PMU registers:
  - PMU memory is already open.
  - PMU registers have been modified.
- Need to recover PMU memory from a semi-closed state:
  - PMU memory was open.
  - PMU memory is not configured for auto-open (bit 3 of CR = 1).
  - Power failed and recovered.
- Need to prevent watchdog time-out (using software signal):
  - PMU memory is open.

The following is a list of situations where opening PMU memory is necessary for proper operation:

- Need to access PMU memory:
  - PMU memory is closed.
- Need to configure PMU:
  - PMU memory is closed.
- Need to prevent watchdog time-out (using software signal):
  - PMU memory is closed.

There are two situations where $\overline{CE}_{CON}$ should be used to drive the $\overline{CE}$ logic of external memory:

- For nonvolatile control of external SRAM.
- When address space of external memory overlaps that of PMU memory.

Microprocessor Supervisor Interface

The PMU offers the following supervisory functions:

- Power-fail warning and power-recovery notification
- Reset generation
- Nonvolatile memory control
- Watchdog monitor

Power-Fail/Power-Recovery Detection

The PMU notifies the host processor of an impending power-failure or power-recovery by asserting a non-maskable interrupt, NMI. The PMU may be configured to generate this signal under V_{CC} (default) or V_{TH} sensing.

V_{CC} Sensing

Clearing bit 7 of register CR selects V_{CC} sensing for NMI generation.

Two programmable thresholds are available to accommodate power supply tolerances. The selected threshold is detected during power-down and power-up as shown in the power-up/power-down timing diagrams in the data sheet.

During a power failure, the user has the time between V_{NMI} and V_{RST} to save critical data in nonvolatile memory (for example, PMU memory). During power-up, NMI is generated to allow the processor to recover data saved earlier.

V_{TH} Sensing

This mode of sensing is available on the bq1001 only.

A 1 in bit 7 of register CR selects this mode of power-fail/power-recovery sensing. A voltage-divider network, illustrated in the following section, should be used to generate a threshold voltage of 2.5V at V_{TH}.

This mode is used for early power-fail detection upstream of the power supply or for monitoring a supply independent of V_{CC}.

Power-Fail Sensing Hardware

Follow these guidelines when using the PMU for power-fail sensing.

Proximity of PMU

The PMU should be physically located as near to the processor as possible. This is necessary to detect true V_{CC} conditions that directly affect processor operation.

Slew rate of V_{CC}

The PMU generates early power-fail warning by sampling the V_{CC} or V_{TH} input every 25 µs (typical) and comparing the result with the programmed V_{NMI} threshold. If the sampled value is below V_{NMI} for each of the three consecutive sampling periods, NMI is generated. The same technique is followed for NMI generation during power-up, except that sampled values should be greater than V_{NMI} for each of the three consecutive sample periods.

To avoid multiple NMI generation, the V_{CC} fall time t_{PF} (slew time between V_{NMI} and V_{RST}) must not exceed the maximum value specified in the data sheet. This maximum value was determined for a 200mV peak-peak random noise on V_{CC}. The V_{CC} fall time is dictated by the power supply hold time and the bypass capacitor on the PMU. The dominant factor is the power-supply hold time parameter. A bypass capacitor in the range of 0.01 to 0.1 µF is recommended.

If V_{CC} slews down at the t_{PF} (minimum) rate, then the time between V_{NMI} and V_{RST} is one sample period (40 µs maximum).

Slew rate of V_{TH}

The above restrictions on V_{CC} slew time apply to the V_{TH} slew time, t_{VTHF}.

The lower limit on t_{VTHF} requires special consideration. If V_{CC} is independent of the supply monitored at V_{TH}, NMI is generated even if V_{TH} slews down in less than t_{VTHF} time. If V_{CC} and V_{TH} are derived from the same supply source, then the minimum slew time on V_{TH} should be such that V_{TH} slews down to the internal V_{TH} reference of 2.5V at least one sample period (40 µs maximum) before V_{CC} slews past V_{RST}.

Hardware Setup Figures

Figure 5 illustrates the hardware setup for V_{CC} sensing.

Figure 6 illustrates the hardware setup for V_{TH} sensing. Diodes D1 and D2 are used to prevent the V_{TH} voltage from falling below 1.0V. This prevents spurious NMI generation when V_{TH} has slewed down past 1.0V and V_{CC} is still valid.

The ratio, R1/R2 is related to the trip point voltage, V_{TP} and diode drop, V_D:

$V_{TP} = R1/R2\ (2.5 - 2V_D) + 2.5$

Example: $V_{TP} = 7.0\ V; V_D = 0.7\ V$

Inserting values into the above equation gives:

$R1/R2 = 4.1$

Selecting a value of 100K for R2 gives R1 as 410K.

The values for R1 and R2 can be large enough to reduce power dissipation and at the same time should maintain the forward bias current for diodes D1 and D2.

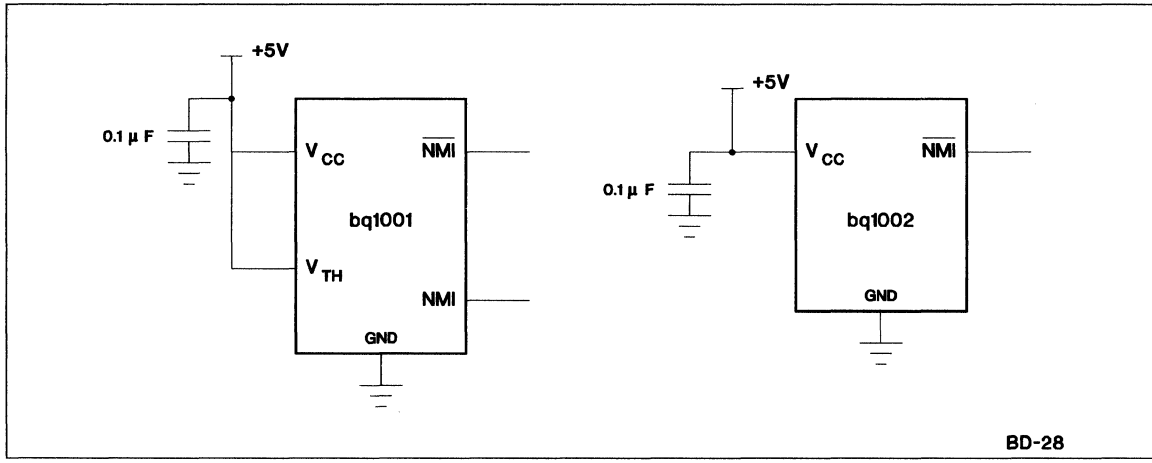


Figure 5. Hardware Setup for V_{CC} Sensing

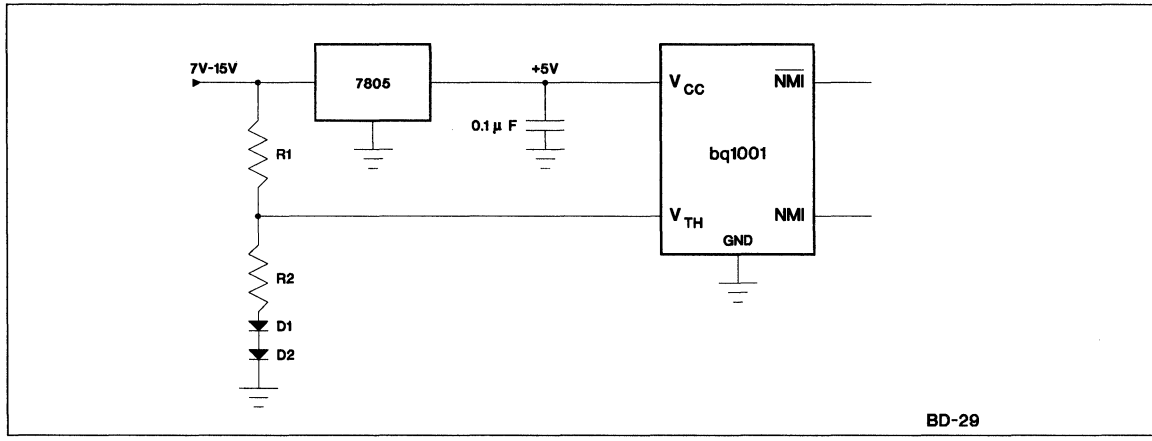


Figure 6. Hardware Setup for V_{TH} Sensing

Power-Fail Sensing Software

The following steps may be added to the PMU initialization procedure described previously.

1. If V_{CC} sensing is required, set bit 7 to 0 and bit 6 per system requirements.

   Bits 7,6 : 00 - V_{NMI} = 4.60V (default)

   Bits 7,6 : 01 - V_{NMI} = 4.75V

2. If V_{TH} sensing is required, set bit 7 to 1 (for bq1001 only).

The interrupt-handler routine for NMI is invoked under the following conditions:

- On power-down, when V_{CC} or V_{TH} (bq1001 only) falls below the V_{NMI} threshold
- On power-up, when V_{CC} or V_{TH} (bq1001 only) rises above the V_{NMI} threshold
- On watchdog time-out, if programmed to generate NMI

The NMI interrupt-handler routine may do the following:

1. Open PMU memory (if not already open).
2. Read register SCR to determine what caused NMI:
   - If bit 7 = 1 (NMI on power-down), then store critical data into PMU memory. Skip to step 3.
   - If bit 6 = 1 (NMI due to watchdog time-out), clear bit 6 and perform the watchdog recovery procedure (described below). Skip to step 3.
   - If bit 7 = 0 (NMI on power-up), then retrieve data saved earlier. Skip to step 3.
3. Close PMU memory.
4. Perform other NMI handler tasks.

For the bq1001, NMI due to power-fail/recovery can be disabled by tying V_{TH} to V_{CC} and writing a 1 in bit 7 of register CR. For the bq1002, V_{NMI} detection is disabled by writing a 1 in bit 7 of register CR.

Reset Generation

The PMU generates a reset when V_{CC} falls below or rises above the configured out-of-tolerance threshold, V_{RST}.

On power-up, when V_{CC} slews up past V_{RST}, a reset pulse (100ms typical) is generated. This puts the processor in an initialized state while V_{CC} stabilizes. During power-down, a reset is generated after V_{CC} slews past V_{RST}, inhibiting any processor activity.

For nonvolatile processor operation, reset generation during power-down/power-up may be disabled, and $\overline{NMI}$ may be configured to be pulled high to the battery voltage during periods of invalid V_{CC}.

Reset Generation Hardware

The bq1001 provides an active-low and an active-high reset, while the bq1002 only provides an active-high reset. Using a pushbutton to strobe the $\overline{DEF}$ pin provides manual reset generation.

Reset Generation Software

The following steps may be added to the PMU initialization procedure:

1. Enable reset by writing a 1 in bit 1 of register CR.
2. Set bit 5 of CR according to the out-of-tolerance threshold required:

   Bit 5 : 1 ; V_{RST} = 4.30V (default)

   Bit 5 : 0 ; V_{RST} = 4.50V
3. For nonvolatile processor operation, clear bits 1 and 4 of register CR.

The system initialization routine invoked after reset should do the following :

1. Open PMU memory (if not already open).
2. Read register SCR:
   - If bit 6 = 1, then a watchdog time-out caused the reset. Clear bit 6 and perform the watchdog recovery procedure (described below). Skip to step 4.
3. Perform system initialization tasks.
4. Close PMU memory (if not already closed).

Nonvolatile Memory Control

The PMU integral control circuitry write-protects its internal memory and switches it to the backup energy source at BC during power-down. If enabled, V_{OUT} and $\overline{CE}_{CON}$ outputs provide this functionality for external SRAM.

Nonvolatile Memory Control Hardware

The hardware hookup is shown in Figure 7.

Nonvolatile Memory Control Software

For nonvolatile control of external memory, clear bits 0 and 1 of register SCR as part of the PMU initialization procedure described previously.

Watchdog Monitor

The PMU watchdog monitor is used to supervise processor operation. The watchdog monitor incorporates a timer, which generates a reset (default) or NMI at the programmed time-out period.

This time-out period is user-selectable. The default setting is watchdog disabled. NMI may be substituted for reset as the watchdog time-out output.

Two ways to prevent a time-out are available:

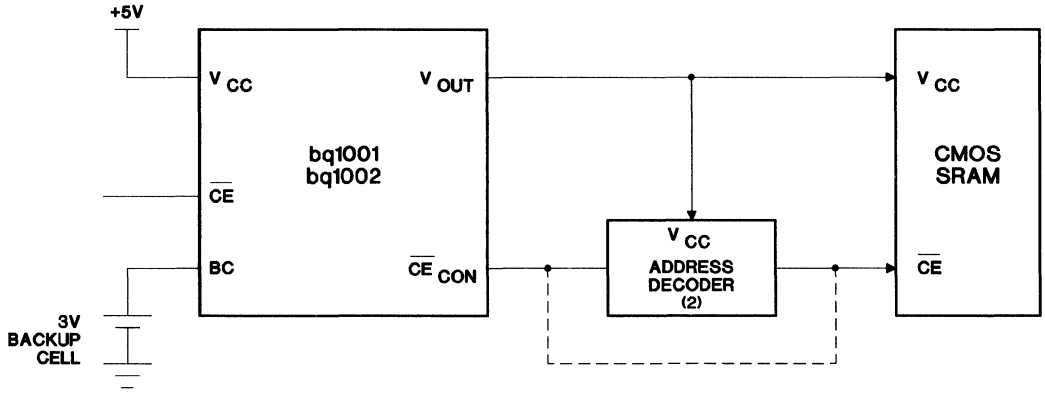
- Strobing the $\overline{WD}$ input
- Opening/closing PMU memory under software control

The bq1001 has a $\overline{WD}$ input that, when toggled low once every t_{WTO} time, prevents the watchdog timer from timing out.

The software approach is recommended when hardware is not available to toggle the $\overline{WD}$ input. The software approach prevents a watchdog time-out by opening or closing PMU memory within the configured time-out period (t_{WTO}). This is the only way to reset the watchdog timer on the bq1002.

Watchdog Monitor Hardware

The strobing of the $\overline{WD}$ input can be performed using a port pin from a microcontroller. To reduce hardware overhead, where a port pin is not available, the software approach is recommended.



Notes:
1. Address, data, and control pins are per standard hookup.
2. The address decoder logic must be of the 74HC type. If PMU and external SRAM are the only devices sharing the PMU 64K address space, the decoder is not required.
3. If SRAM has an active-high chip enable pin, this pin must be tied to V_{OUT}.

Figure 7. Nonvolatile Memory Hookup

Watchdog Monitor Software

The following steps may be added to the PMU initialization procedure:

1. Set bits 4,3 of register SCR according to the time-out period required:

   Bits 4,3 : 00 ; t_{WTO} = 125 ms

   Bits 4,3 : 01 ; t_{WTO} = 500 ms

   Bits 4,3 : 10 ; t_{WTO} = 2 seconds

   Bits 4,3 : 11 ; t_{WTO} = infinity (timer disabled)

2. If NMI is required on watchdog time-out, then clear bit 2 of register SCR.

Watchdog Recovery Procedure

The watchdog timer generates either a reset or an NMI if not reset within the programmed time-out period, t_{WTO}. A system initialization routine or an NMI interrupt handler is invoked depending on which output was selected for the watchdog time-out. If the run time of either routine is greater than the configured t_{WTO} time, the system may never recover from the watchdog time-out condition.

The following procedure may be added to the system initialization routine and the NMI interrupt handler to avoid such a situation:

1. Configure the PMU to disable the watchdog timer by setting bits 4 and 3 of register SCR.
2. Perform the remaining tasks in the system initialization routine or NMI interrupt handler.
3. Configure the PMU according to system requirements. This may involve enabling the watchdog timer by setting bits 4 and 3 of register SCR to the desired time-out period.

Summary

The following paragraphs present example procedures for PMU initialization, system initialization, and NMI handling. The procedures reflect only the steps required to perform supervisory functions for a target system using a bq1001.

The system specifications for supervisory functions are:

- Detect and generate power-fail warning and power-recovery notification:
  - The detect point is the unregulated DC supply.
  - The trip point is 7V (2.5V at V_{TH}).
- Generate a reset when V_{CC} cycles through out-of-tolerance conditions:
  - Valid V_{CC} operating range is 5V +/- 10%.
- Provide for nonvolatile control of external SRAM
- Detect and recover from abnormal system operation:
  - Longest loop execution time or inactive time is less than 125 milliseconds.

PMU Initialization Procedure

1. Open PMU memory (if not already open).
2. Write the valid update pattern in register AC1.
3. Set register CR as follows:

Register CR Bits								Meaning
7	6	5	4	3	2	1	0	
1	0							V_{NMI} = 2.5V (V_{TH} sensing)
		1						V_{RST} = 4.3V
			1					Normal NMI/ reset operation
				1				Normal PMU memory operation
					0			PMU memory at top block
						1	-	Reset enabled

4. Set register SCR as follows:

Register SCR Bits								Meaning
7	6	5	4	3	2	1	0	
X	X	X						Status bits
			0	0				Watchdog time-out: 125 ms
					1			Reset signals watchdog time-out
						0	0	External non-volatile control

5. Write the update patterns to the remaining registers, AC2-AC4.
6. Close PMU memory

System Initialization Procedure

This procedure describes PMU management within the system initialization routine.

1. Open PMU memory as explained in the power-fail operation section.
2. Read register SCR; if bit 6 = 1, then clear bit 6 and disable watchdog timer:

   a. Write update pattern to AC1.

   b. Set bits 4 and 3 of register SCR.

   c. Write remaining update patterns to AC2–AC4.

   d. Close PMU memory.
3. Perform system initialization tasks.
4. Enter PMU initialization procedure (described above).

NMI Handler Procedure

1. Open PMU memory (if not already open).
2. Read register SCR:

   - If bit 7 = 1, then store critical data to PMU memory. Available locations are F800-FFF7.

   - If bit 7 = 0, then retrieve data stored at PMU memory locations F800-FFF7.
3. Close PMU memory.
4. Perform other NMI handler tasks.

Energy Management Unit (EMU)

Features

- Microprocessor peripheral for the total energy management of battery-operated systems
- Direct measurement of battery consumption and capacity
- Fast charging and conditioning control for nominal 3.6V to 12V nickel cadmium, lead acid, or nickel hydride batteries
- Full-charge detection by negative delta voltage method, maximum voltage, and maximum time
- Register-controlled outputs for energy management
- Provides and controls 3V battery-backup supply
- Operates from 4.5–18V DC or 4.5–5.5V V_{CC} supplies
- 24-pin SDIP or SOIC

General Description

The CMOS bq2001 Energy Management Unit (EMU) is a low-power microprocessor peripheral providing battery and energy management services for systems using rechargeable (secondary) batteries. The bq2001 works directly from the DC charging supply, operating as programmed, or from 5V V_{CC}, operating as a microprocessor peripheral. bq2001-based systems can easily incorporate sophisticated capacity monitoring, battery management, backup supply services, and power-conservation capabilities.

The "gas gauge" register provides the actual charge consumption from the secondary battery and allows measurement of the battery capacity. The programmed end-of-discharge voltage (EDV) threshold determines full discharge.

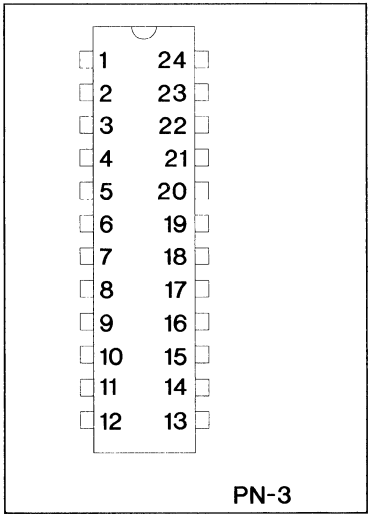
Battery management includes charge control at standard to fast charge rates, with full charge determined using the preferred negative delta voltage (-ΔV) method, a maximum voltage threshold, and a maximum time limit. Trickle charge control begins after full charge is determined. Non-operational discharge before charge may be selected for cell conditioning or capacity measurement. Charge patterns may be programmed to be constant, pulsed, or "burp" (alternating charge/discharge).

For the power-off condition, the bq2001 regulates the secondary battery input to maintain its own programmed state while it simultaneously sources a backup cell output to maintain a real-time clock or other 3V battery-backed ICs. A 3V backup cell provides system data-retention current when the secondary battery is depleted or removed.

Power management is supported by seven open-drain outputs controlled by the EMU or the host processor. These may be allocated for subsystem control, LED activation, EMU status indication, and system power switch control.

3

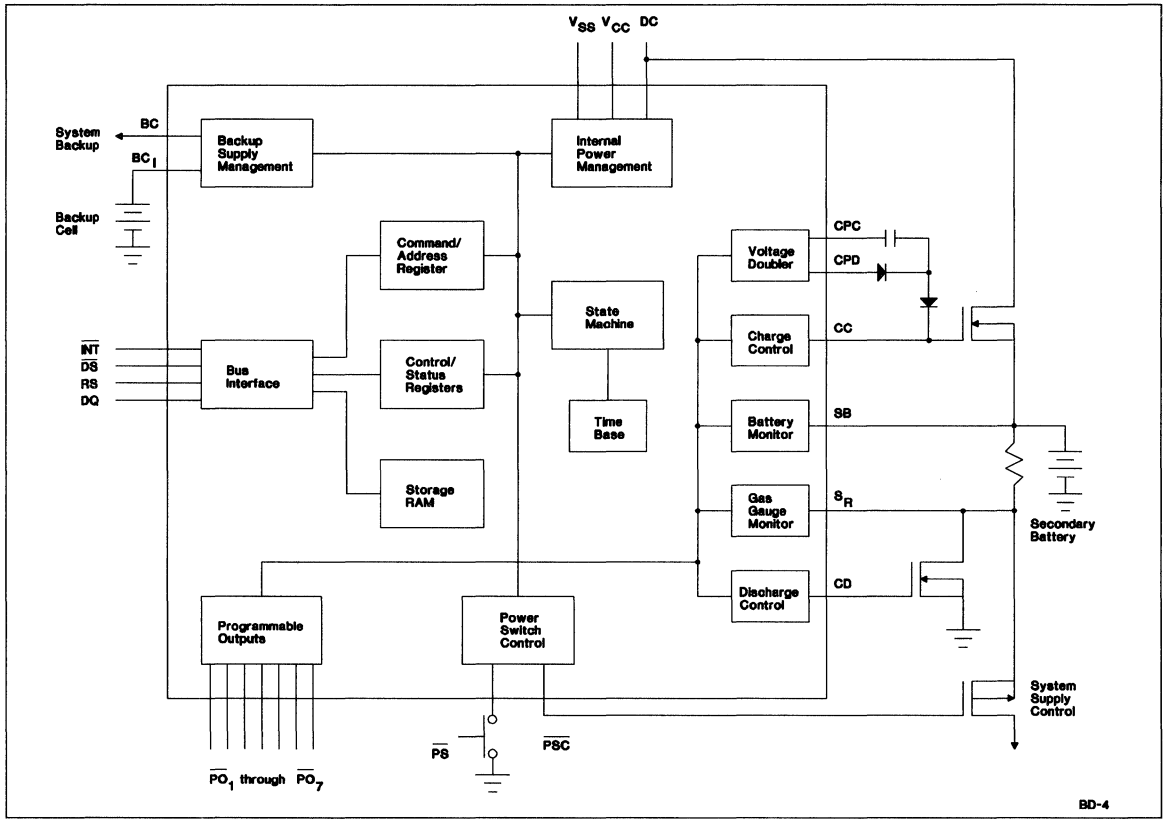
Pin Connections



Pin Names

$\overline{DS}$	Data strobe input
RS	Register select input
DQ	Data input/output
$\overline{INT}$	Interrupt request output
DC	Charging supply input
SB	Secondary battery input
BC	Backup cell output
BC_I	Backup cell input
CC	Charge control output
CPC	Charge pump capacitor output
CPD	Charge pump diode output
CD	Discharge control output
S_R	Sense resistor input
$\overline{PS}$	Power switch input
$\overline{PSC}$	Power switch control output
$\overline{PO_1}$	Charging indicator or programmable output 1
$\overline{PO_2}$	End-of-discharge voltage indicator or programmable output 2
$\overline{PO_3}$	Backup cell low indicator or programmable output 3
$\overline{PO_4}$	DC valid indicator or programmable output 4
$\overline{PO_5}$	Gas gauge threshold indicator or programmable output 5
$\overline{PO_6}$	Secondary battery fault or programmable output 6
$\overline{PO_7}$	Programmable output 7
V_{CC}	+5V system supply input
V_{SS}	System ground

Block Diagram



Pin Descriptions

$\overline{DS}$ **Data strobe TTL input**

$\overline{DS}$ is used to identify the time when read data is used to drive DQ or for latching write data present on DQ. During read cycles, valid data is output on DQ after time t_{ACS} following $\overline{DS}$ asserted low. During write cycles, the rising edge on $\overline{DS}$ latches the input data on DQ into the bq2001.

RS **Register select TTL input**

RS is used during an access cycle to identify the data byte type. RS low identifies the data bit as part of a command byte to be written to the command register, CMR. RS high identifies the data bit as part of a read or write data byte for the control and status register or storage RAM as addressed in the preceding CMR read or write command. An incomplete data byte being transferred to or from the bq2001 is terminated if a low is present on RS when $\overline{DS}$ becomes active, allowing synchronization of a data-byte transfer (return to CMR to restart the sequence).

DQ **Data bit bidirectional TTL input/output**

DQ is used to transfer one bit of data from or to the bq2001. During a read cycle, the bq2001 outputs one bit of data on the DQ pin at time t_{ACS} after the falling edge of $\overline{DS}$ and returns the output driver to the high-impedance state t_{DHR} time after $\overline{DS}$ rises. Valid write data must be presented for time t_{DW} before the rising edge of the $\overline{DS}$ pulse.

$\overline{INT}$ **Interrupt request output**

$\overline{INT}$, an open-drain output, goes low for time t_{INT} to indicate an interrupt request. The interrupt request is activated by secondary battery low, the gas gauge threshold, or a low transition on the $\overline{PS}$ pin. $\overline{INT}$ may be tied to the NMI of the host processor so that the system can not overlook this request. $\overline{INT}$ goes to high impedance in the absence of V_{CC}.

DC **DC supply input**

DC is the secondary battery charging supply input. DC must be provided a valid voltage during charge actions. The DC input powers the bq2001 during charge actions in the absence of V_{CC}.

SB **Secondary battery supply input**

SB is the secondary battery input pin. SB is monitored for negative delta voltage (-ΔV), maximum battery voltage, end-of-discharge voltage (EDV), secondary battery inoperable, and secondary battery replaced. SB also powers the BC output and bq2001 data retention.

BC **Backup cell output**

BC is the backup cell supply output pin. A voltage regulated from SB is output on BC as a backup source for a real-time clock, data retention, and other battery-backed requirements (see Figure 1).

BC_I **Backup cell input**

BC_I is the supply input for a 3V backup cell. No protective circuits are required between the backup cell and BC_I (see Figure 1).

When the BC output voltage regulated from SB falls below the backup cell voltage, the backup cell is switched directly through the bq2001 to the BC output.

BC_I is monitored for the backup cell low-voltage threshold.

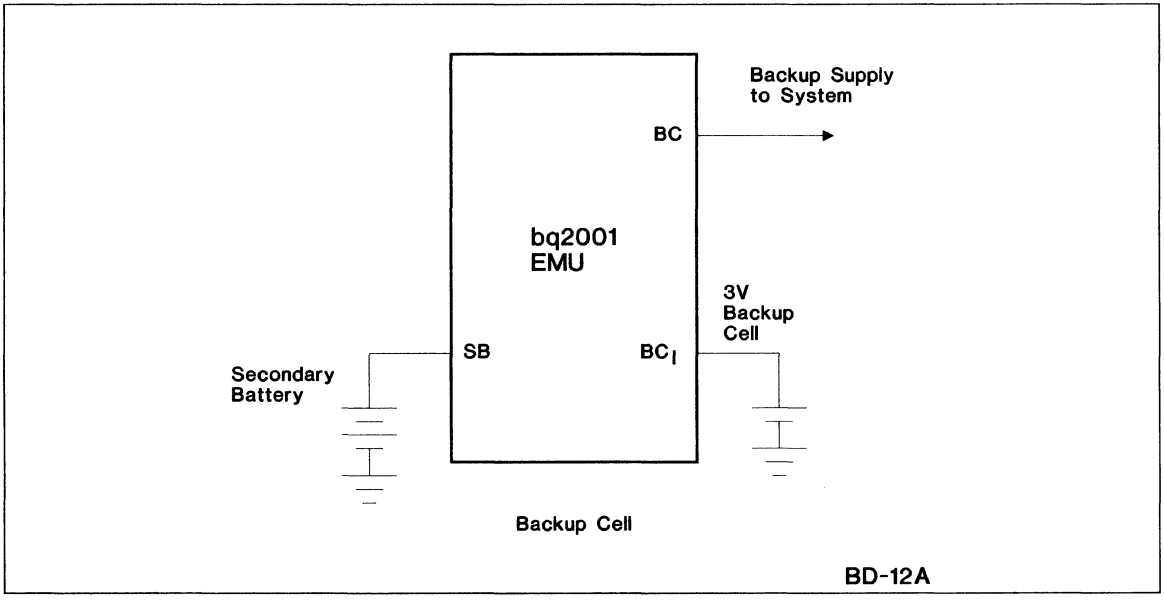


Figure 1. Backup Supply and Sources

CC **Charge control output**

CC is an open drain output that is high impedance during the charging period of a charge action interval. CC provides charge control if used to switch an external n-channel power FET. For full n-FET turn-on, the voltage at CC may be two times the voltage at DC.

CPC **Charge pump capacitor output**

CPC is part of the voltage-doubler circuit. The voltage-doubler output is only available to pin CC. This pin should be connected to one end of a capacitor. The capacitor value must be as large as the input capacitance of the n-FET being controlled and may be a maximum of 1µF. (See Figure 2.)

If the voltage doubler is not used, CPC must be left open.

CPD **Charge pump diode output**

CPD is part of the voltage-doubler circuitry. The CPD pin supplies the charge pump for the voltage doubler. This output is inactive when CC is low.

CD **Discharge control output**

CD is an open drain output used to control an n-channel power FET during a bq2001-controlled discharge. CD is high impedance during the discharge phase of a charge action or during the discharge period of a charge action interval. (See Charge Action.)

S_R **Sense resistor input**

S_R, part of the gas gauge subsystem, is used along with SB to measure the voltage across the sense resistor. The sense resistor should be chosen by fitting it to the profile of the secondary battery discharge rate, allowing the highest gas gauge accuracy. Typical applications achieve the highest accuracy when the voltage drop across the sense resistor is in the range of 50 to 125 mV during the discharge periods that dominate battery drain. (See Capacity Monitoring for details.)

***Caution*: To avoid damaging the device, the sense resistor must be in the discharge path and must *not* be in the charge path. See Figure 3.**

$\overline{PS}$ **Power switch input**

$\overline{PS}$ indicates system on/off status to the bq2001. $\overline{PS}$ is pulled to V_{BC} by a 100K ohm resistor. In conjunction with $\overline{PSC}$ output, $\overline{PS}$ may be used as the control input of a FET switch.

$\overline{PS}$ low causes the following actions:

1. Activates $\overline{PSC}$ if $\overline{PSC}$ is inactive.
2. Discontinues any existing charging action prior to $\overline{PSC}$ being activated.

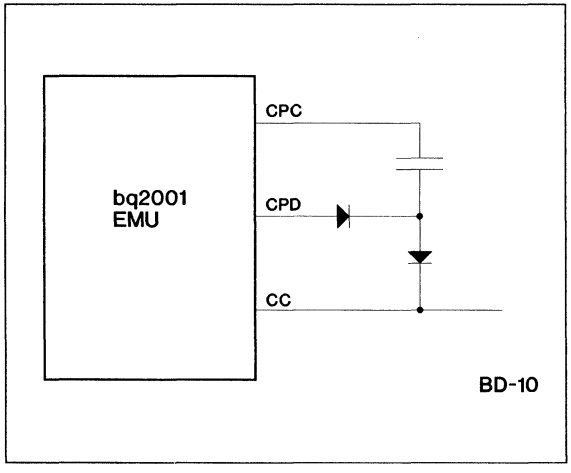


Figure 2. Voltage Doubler and Charge Control

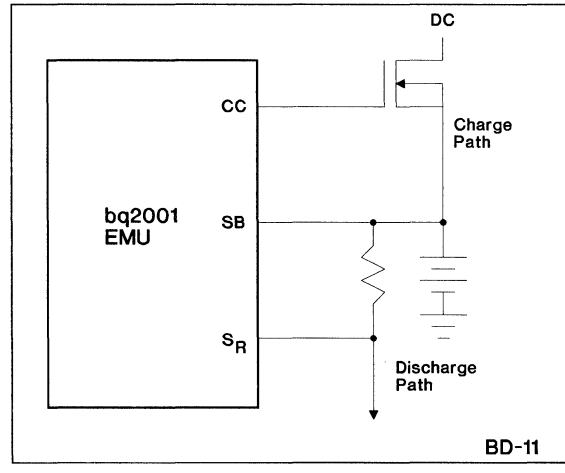


Figure 3. Sense Resistor in Discharge Path

3. Sets the power switch state bit, status register bit 7, to 1.

4. Generates an $\overline{INT}$ low output for time t_{INT}.

$\overline{PSC}$ **Power switch control output**

$\overline{PSC}$ is an open-drain output that may be used for turning system power on or off. $\overline{PSC}$ is activated (low impedance to V_{SS}) following $\overline{PS}$ low and deactivated by writing the power-off command to the command register (CMR). The polarity is meant to drive a p-channel FET.

When $\overline{PSC}$ is active, a charge action may only be initiated through the command register, CMR.

When $\overline{PSC}$ is inactive, a charge action may be initiated by the appearance of DC.

The status of $\overline{PSC}$ is reflected in the status register (SR) power switch state bit.

$\overline{PO_1}$ **Charging indicator or programmable output 1**

$\overline{PO_1}$ is an open-drain output that may be programmed to indicate the condition of status register (SR) bit 1, charging (mask register bit 0 = 1). When mask register bit 0 = 0, $\overline{PO_1}$ is controlled by output control register (OCR) bit 0.

$\overline{PO_2}$ **End-of-discharge voltage indicator or programmable output 2**

$\overline{PO_2}$ is an open-drain output that may be programmed to indicate the condition of status register (SR) bit 2, end-of-discharge voltage (mask register bit 1 = 1). When mask register bit 1 = 0, $\overline{PO_2}$ is controlled by output control register (OCR) bit 1.

$\overline{PO_3}$ **Backup cell low indicator or programmable output 3**

$\overline{PO_3}$ is an open-drain output that may be programmed to indicate the condition of status register (SR) bit 3, backup cell low (mask register bit 2 = 1). When mask register bit 2 = 0, $\overline{PO_3}$ is controlled by output control register (OCR) bit 2.

$\overline{PO_4}$ **DC valid indicator or programmable output 4**

$\overline{PO_4}$ is an open-drain output that may be programmed to indicate the condition of status register (SR) bit 4, DC valid (mask register bit 3 = 1). When mask register bit 3 = 0, $\overline{PO_4}$ is controlled by output control register (OCR) bit 3.

$\overline{PO_5}$ **Gas gauge threshold or programmable output 5**

$\overline{PO_5}$ is an open-drain output that may be programmed to indicate the condition of status register (SR) bit 5, gas gauge notification (mask register bit 4 = 1). When mask register bit 4 = 0, $\overline{PO_5}$ is controlled by output control register (OCR) bit 4.

$\overline{PO_6}$ **Secondary battery fault indicator or programmable output 6**

$\overline{PO_6}$ is an open-drain output that may be programmed to indicate the condition of status register (SR) bit 6, secondary battery fault (mask register bit 5 = 1). When mask register bit 5 = 0, $\overline{PO_6}$ is controlled by output control register (OCR) bit 5.

$\overline{PO_7}$ **Programmable output 7**

$\overline{PO_7}$ is an open-drain output. When mask register bit 6 = 0, $\overline{PO_7}$ is controlled by output control register (OCR) bit 6.

V_{CC} **V_{CC} supply input**

V_{CC}, 5V system supply, must be valid during system operation to operate the microprocessor interface and—in the absence of DC—the gas gauge.

V_{SS} **Ground**

V_{SS} is the system ground pin. All bq2001 supplies are defined relative to this pin.

3

Functional Description

Microprocessor Interface

The bq2001 provides a simple and space-efficient three-pin serial data interface to Intel, Motorola, and other bus architectures. This interface is active only when V_{CC} is valid. Table 1 shows the microprocessor interface truth table.

The interface uses command bytes (written to command register, CMR) that direct access to 17 data bytes used for control and status, and to 32 data bytes provided for nonvolatile storage of programmer-defined information. CMR is used to directly write any of three direct control commands or to manage subsequent data-byte access.

Data-byte access through CMR involves writing one of the four access commands. Two of the commands direct access to the control and status registers, and two direct access to the storage RAM. Each of the four data-byte access commands includes the internal data-byte address.

The physical interface uses bidirectional DQ (data I/O pin) to read or write data one bit at a time. The logic level on RS (register select input pin) identifies the byte currently being accessed as CMR (command register) or a data byte.

$\overline{DS}$ (data strobe input pin) is used during write cycles to latch the data at DQ into memory, and during read cycles to clock the EMU data out on DQ. $\overline{DS}$ should be gated with the chip select generated for the bq2001. Input data is accepted as valid only after the last bit of a complete byte is written.

A fourth microprocessor interface pin, $\overline{INT}$ (interrupt request output), allows the EMU to generate interrupt requests to the host processor. The interrupt flag bit (INTF) in the status register (SR) is set to 1 when $\overline{INT}$ goes active. Powered by V_{CC}, $\overline{INT}$ becomes active for any of three reasons:

- $\overline{PS}$ (power switch input) is pulled low, indicating a power-on or power-off request.
- Gas gauge notification (GGN) status is set, indicating the secondary battery has discharged to the programmed gas gauge threshold.
- End-of-discharge voltage (EDV) status is set, indicating the secondary battery has discharged to the programmed voltage threshold. Specific actions may be called for to avoid disruption of work in progress.

Table 1. Microprocessor Interface Truth Table

Mode	RS	$\overline{DS}$	Immediately Prior Command Byte		I/O Operation
			Command Field	Address Field	
Output disable	X	H	XXX	XXXXX	High Z
Command	L	L	XXX	XXXXX	D_{IN}
Control and Status Register:					
Read	H	L	011	XXXXX	D_{OUT}
Write	H	L	101	XXXXX	D_{IN}
Storage RAM:					
Read	H	L	010	XXXXX	D_{OUT}
Write	H	L	100	XXXXX	D_{IN}

Capacity Monitoring

The bq2001 incorporates a "gas gauge" that provides a real measurement of the charge drawn from the secondary battery. When DC or V_{CC} is valid, the gas gauge monitors current from the secondary battery, incrementing the value in the gas gauge register pair, GG. The gas gauge is reset by a full recharge, by the host processor, or by battery replacement.

The secondary battery discharge rate is monitored by measuring the voltage across a sense resistor using S_R, sense resistor input, and SB, secondary battery input. The sense resistor should be chosen by fitting it to the system battery discharge rate profile to achieve the highest gas gauge accuracy. Figure 4 indicates the gas gauge error with respect to a range of voltage drops across the sense resistor.

The sense resistor should be carefully selected to minimize total error, especially for systems that include significant battery discharge across a wide range of currents. Typical applications achieve the highest accuracy when the voltage drop across the sense resistor is in the range of 50mV to 125mV around the dominant battery discharge rates.

The gas gauge count rate is proportional to the voltage drop, except for the error shown in Figure 4. A time-averaged 100mV signal causes the gas gauge counter to wrap around after 14 hours. A time-averaged 200mV signal wraps around after 7 hours.

Removed capacity is determined as follows:

$$\text{Removed capacity (mAh)} = \frac{\text{gas gauge value}}{46 \times S_R\ \Omega}$$

A gas gauge measurement to full battery discharge (end-of-discharge voltage, EDV) is a measure of the actual secondary battery capacity. When the battery discharges to EDV, the last gas gauge value is automatically loaded into the last capacity register pair.

The system may poll the gas gauge to read actual consumption. The system compares the reading to the previous actual or the nominal capacity for that battery. Additionally, when the gas gauge has passed the gas gauge threshold (programmed in the gas gauge threshold register pair), an interrupt request is generated on $\overline{INT}$, and the status register (SR) interrupt flag and gas gauge notification bits are set to 1. Mask register bit 5 may be programmed so that passing the gas gauge threshold also activates $\overline{PO_5}$.

The gas gauge register is reset to 0 by:

- Charge action termination due to -ΔV, maximum charge time, or maximum voltage determination, any of which indicates full charge.
- An abort charge actions command written to CMR (command register).
- The reappearance of a valid voltage at SB, which indicates the battery was removed and replaced.

The gas gauge register may be interpreted in conjunction with charge setup register 2 (CSR2) bit 6, gas gauge not valid (GGNV), and CSR2 bit 7, battery replaced (BR).

GGNV = 1 indicates to the host that the gas gauge register value does not reflect discharge from bq2001-determined full charge, and may not be valid.

GGNV is set to 1 by:

- The start of a charge phase.
- The reappearance of a valid voltage at SB, which indicates the battery was removed and replaced.

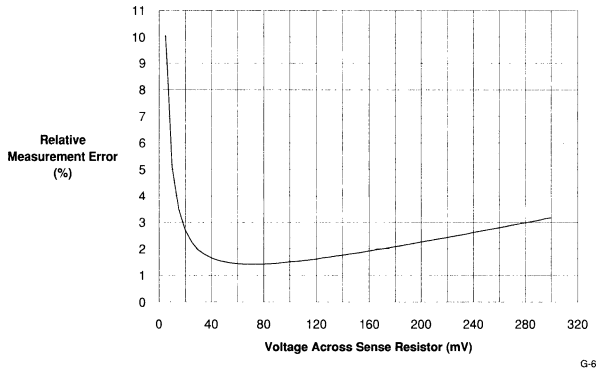


Figure 4. Gas Gauge Measurement Error

GGNV is only reset to 0 by:

- Charge action termination due to -ΔV, maximum charge time, or maximum voltage determination, any of which indicates full charge.

BR = 1 indicates to the host that the battery has been removed and replaced; it is used to validate a new last capacity register value following DC-initiated charge. The battery replaced bit is set to 1 with the reappearance of a valid voltage at SB and is reset by an abort charge action command.

GGNV and BR values are interpreted as follows:

Values		Interpretation
GGNV	BR	
0	0	Full charge completed; new last capacity is valid.
0	1	Battery replaced; full charge completed; new last capacity is not valid.
1	0	Charge action terminated before full charge; unknown charge state.
1	1	Battery replaced; unknown charge state.

Charge Action

The bq2001 initiates a charge action as programmed. A charge action may consist of two phases. The first phase may be a non-operational discharge, draining the secondary battery for conditioning or capacity determination purposes. The second phase is the charge phase. The status register (SR) charging bit is 1 through both phases.

If $\overline{PSC}$ is active (power switch state bit = 1), a programmed charge action will only initiate following a start charge action command written to the command register, CMR.

If $\overline{PSC}$ is inactive (power switch state bit = 0), a programmed charge action is initiated by the presence of valid DC. DC-initiated charge action may be qualified to occur only if the CSR2 GGNV status bit is 1 by setting CSR1 bit 7 (GGNV qualified charge) to 1. This qualification allows the system to prevent DC-initiated charge actions with a battery of known charge (GGNV = 0). Replacing the battery sets GGNV, allowing DC-initiated charge.

When $\overline{PS}$ is toggled low to activate $\overline{PSC}$, any charge action is discontinued before $\overline{PSC}$ goes active. Charge action may be reinitiated after $\overline{PSC}$ is active, through CMR.

Charge action is prevented from starting when any of the following conditions occurs (see Table 2, Charge Action Initiation Truth Table):

- CSR1 bit 6 (charge action enable) is 0.
- SR bit 7 (power switch state) is 0, CSR1 bit 7 (GGNV qualified charge) is 1, and the CSR2 GGNV status bit is 0. This only prevents DC-initiated charge action.
- Status register (SR) bit 4 (DC valid) is 0.
- Status register (SR) bit 6 (secondary battery fault) is 1.

Table 2. Charge Action Initiation Truth Table

Charge Action, as Programmed		SR Bit 4	SR Bit 6	CSR1 Bit 6	CSR1 Bit 7	CSR2 Bit 6	SR Bit 7
Discharge Phase	Charge Phase	DC Valid	Secondary Battery Fault	Charge Action Enable	GGNV Qualified Charge	Gas Gauge Not Valid	Power Switch State
Disabled		0	X	X	X	X	X
Disabled		X	1	X	X	X	X
Disabled		X	X	0	X	X	X
Ignored	DC Initiated	1	0	1	X	1	0
Disabled		1	0	1	1	0	0
DC Initiated		1	0	1	0	0	0
Command Initiated		1	0	1	X	X	1

Any charge action is stopped when any of the following occurs (see Table 3, Charge Action Termination Truth Table):

- $\overline{PS}$ is toggled low to activate $\overline{PSC}$.
- Abort charge actions command is written to CMR.
- Status register (SR) bit 4 (DC valid) is 0.
- Status register (SR) bit 6 (secondary battery fault) is 1.
- Full charge is determined.

Discharge Phase

The discharge phase of a charge action consists of the bq2001 activating the CD output, turning on a discharge path for the secondary battery. The gas gauge is operational during the discharge phase. The discharge phase continues until a programmed threshold is reached or charge action is terminated.

The bq2001 is programmed for discharge in CSR1 to:

- Not discharge prior to charge,
- Discharge to the value in the gas gauge threshold register (to full discharge if it occurs first), or
- Discharge fully if the gas gauge is already beyond the gas gauge threshold register value.

The second option may be used for periodic cell conditioning to avoid any voltage-depression effect or for a forced full discharge to measure battery capacity. The last option may be used to force full discharge for conditioning or to measure capacity. It may also be used to allow full discharge only when the battery is near empty.

The full discharge threshold is the end-of-discharge voltage (EDV) determined from the number of cells programmed in charge setup register 1 and the end-of-discharge cell voltage register value. At EDV, the gas gauge value is written to the last capacity register.

At completion of the programmed discharge phase, the charge action enters the charge phase.

In a DC-initiated charge action (power switch state bit = 0), when the gas gauge not valid (GGNV) bit = 1, any programmed discharge phase is ignored, and the charge action commences with the charge phase.

Charge Phase

The charge phase of a charge action consists of the bq2001 modulating the CC output and optionally the CD output. The charge phase may be continuous, pulsed, or "burp" (alternating charge/discharge pulses).

The charge phase consists of eight-second charge intervals, which repeat until charge termination. The bq2001 is programmed for periods of charge, no action, and discharge, which occur during each eight-second interval.

The CC output controls charging by switching an n-channel power FET. This pulses the DC supply at a duty cycle that results in the desired average charging current. To minimize heat generation in high charging current applications, two pins are available to build a charge pump that doubles the DC voltage, allowing full turn-on of an n-channel FET.

The period for the full charging rate is programmed into the charging period register, with time specified in units of 1/32 seconds. The charging period register can be programmed for continuous charging (charging period = 256 units) or for pulsed charging (charging period < 256 units). See Figure 5.

Table 3. Charge Action Termination Truth Table

Cause of Termination	Gas Gauge Reset	CSR2 Bit 6 (GGNV)	Trickle Charge (if enabled)
$\overline{PS}$ low to activate $\overline{PSC}$ (SR bit 7 from 0 to 1)	No	1	No
DC not valid (SR bit 4 = 0)	No	1	No
Secondary battery fault (SR bit 6 = 1)	No	1	No
Abort charge action command	Yes	1	No
-ΔV detected	Yes	0	Yes
Maximum charge time	Yes	0	Yes
Maximum charge voltage	Yes	0	Yes

For burp charging, the discharge period register can be programmed with a discharge-after-charge period, which is programmed as in the charging period register. See Figure 5. In operation, the charging period takes precedence over the discharge period. The discharge period may be no longer than the remainder of the eight-second interval following completion of the charge period.

Full charge is normally determined by negative delta voltage (-ΔV) sensing, with a voltage sensitivity of less than 10mV per cell. The sampling period for the -ΔV determination is defined in charge setup register 2. Longer sampling periods may be necessary for slower charge rates.

The host processor can use the -ΔV enable control field in charge setup register 2 to disable -ΔV full charge determination. In applications where the host processor uses subsystem power switching for power management, the charging current provided to the battery may vary with subsystem activity. Briefly disabling -ΔV response coincident with each charging current decrement prevents false full charge determination.

Full charge is also determined if the charge phase exceeds the maximum charge time register value or the cell voltage exceeds the maximum charge voltage per cell.

Note: For -ΔV determination, the charging voltage per cell (with the number of cells as programmed in the CSR1 register) must be above the end-of-discharge cell voltage (EDCV) and less than EDCV plus 1.0V. For example, if a five-cell battery has an end-of-discharge voltage of 1.0V per cell, -ΔV detection requires a charging voltage between 5V and 10V.

Trickle Charge

When the trickle enable bit in charge setup register 2 is set, on full charge the EMU initiates the charge-sustaining trickle charge defined by the period in the trickle period register. See Figure 5. Full charge is indicated by charge action termination due to -ΔV determination, maximum charge time, or maximum voltage determination. When DC-initiated charge action is blocked by GGNV qualified charge bit = 1 and GGNV = 0, and trickle is enabled, DC-initiated trickle charge will occur.

Trickle charge is terminated if:

- Status register (SR) bit 4 (DC valid) is 0 or
- $\overline{PS}$ is pulsed low to activate $\overline{PSC}$ (status register power switch state bit switches from 0 to 1).

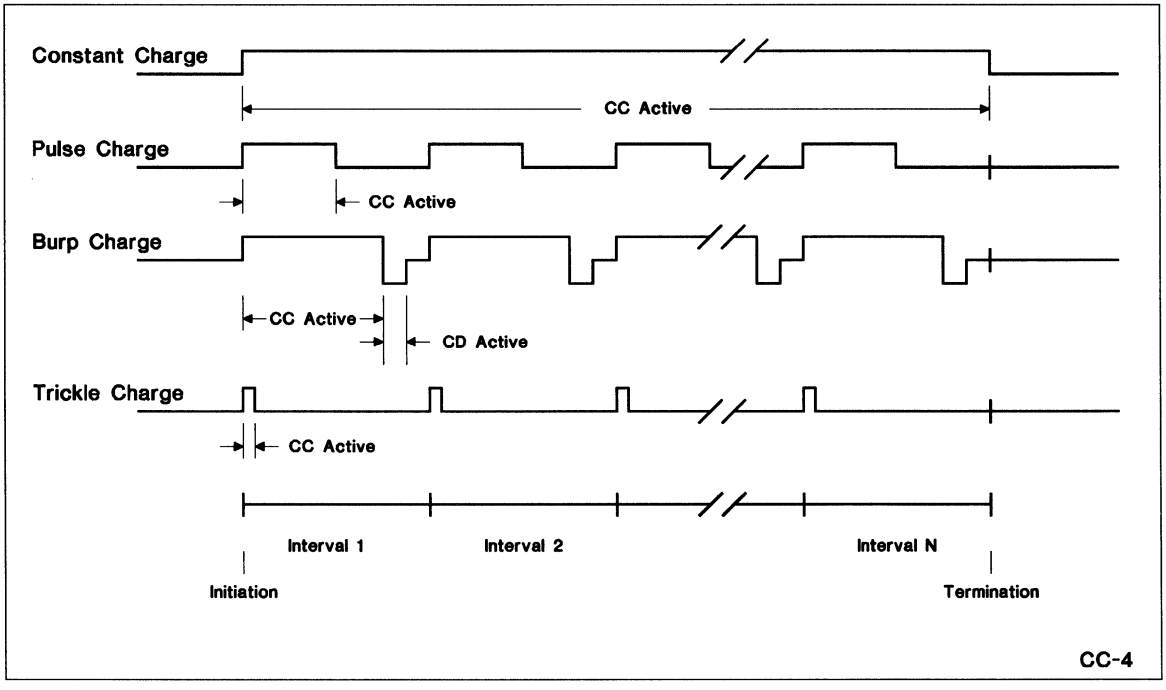


Figure 5. Charge Phase and Trickle Charge Modulation

Backup Power Management

The bq2001 sources the external 3V battery-backed integrated circuits through BC, backup cell output. The bq2001 regulates power from the secondary battery for internal data retention and for output at BC. The BC output can be used in the absence of system power as a battery-backup source for static CMOS devices such as a real-time clock or static RAM.

When the secondary battery is removed or becomes depleted, an external power source must support the bq2001 and external data retention. This source may be a lithium cell directly connected to BC_I. This backup automatically switches in as the data-retention power source for the bq2001 and the circuits sustained by BC as an output. (See Figure 1.)

Power Management Annunciation

Programmable open-drain outputs $\overline{PO_1}$ through $\overline{PO_7}$ may be used to activate annunciators such as LEDs. These seven outputs are programmable to become active (low impedance to V_{SS}) based on internal EMU status or as written by the host processor.

- Writing any of mask register bits 0 to 5 to a value of 1 causes the associated output pin $\overline{PO_1}$ to $\overline{PO_6}$ to become active whenever the EMU sets the corresponding status register bit to a value of 1.
- Writing any of mask register bits 0 to 6 to a value of 0 sets the associated output pin $\overline{PO_1}$ to $\overline{PO_7}$ to become active whenever the corresponding control bit in the output control register is written to 1.

Thus $\overline{PO_1}$ to $\overline{PO_6}$ can be selected to be activated by the host processor (with system power on) or by internal EMU status. $\overline{PO_7}$ is activated only by the host processor.

Rewriting a mask register bit between power-on and power-off may allow the corresponding output pin to be active as written by the processor when power is on and active reflecting EMU status when power is off (and DC is valid).

Power Conservation

Microprocessor control of open-drain output pins $\overline{PO_1}$ to $\overline{PO_7}$ allows any one of them to be used to switch a p-channel FET or PNP transistor controlling the power supply to various subsystems (such as the display, backlight, hard disk, serial port, and coprocessor). Each output supports a maximum voltage of 18V. Subsystem on/off switching to conserve power may be part of a configuration routine or may be dynamic. Dynamic power conservation based on software activity monitoring and timeout periods may be part of a power-management BIOS.

These outputs are not restricted in use. For example, one of these outputs may also be used to switch to a second (lower) charging current for charging actions when the system is on.

Writing any of mask register bits 0 to 6 to a value of 0 sets the associated output pin $\overline{PO_1}$ to $\overline{PO_7}$ to become active whenever its corresponding control bit in the output control register is written to 1.

On/Off Control

The bq2001 may be used for system on/off control by hardware and software inputs. $\overline{PS}$ and $\overline{PSC}$ may be used to control an external pFET.

$\overline{PS}$ is the power switch input, pulled high internally. $\overline{PS}$ may be toggled to turn the system on, and may be toggled to initiate a request to turn off.

$\overline{PSC}$, power switch control output, is an open-drain output intended to drive a p-channel FET, which may control the system supply. $\overline{PSC}$ is activated by $\overline{PS}$ toggled low and deactivated by a system off command written to CMR.

When $\overline{PS}$ is pulled low and $\overline{PSC}$ is inactive, the bq2001 sets the status register power switch state bit to 1, turns off any charge action or trickle charge, and activates $\overline{PSC}$. The power switch state bit is reset to 0 when the system off command is written to CMR.

When $\overline{PS}$ is pulled low, the bq2001 generates an eight-microsecond pulse on $\overline{INT}$, and the status register (SR) interrupt flag bit is set.

Note: Because the state of $\overline{PSC}$ determines the means of charge action initiation (see Charge Action), $\overline{PSC}$ may need to reflect system power status even if $\overline{PSC}$ is left open.

Register Description

The bq2001 has two data groups independently addressable through the write-only command and address register, CMR: (1) storage RAM and (2) control and status registers.

CMR is accessed with RS low. CMR may be written with command bytes that serve as direct commands or that control the access of a subsequent data byte.

The storage RAM provides 32 data bytes of general-purpose nonvolatile RAM storage capability, accessed with RS high.

The control and status registers consist of 17 bytes, also accessed with RS high.

Command Register (CMR)

The write-only CMR register is accessed when register select, RS, is zero during a write access. CMR is used to start an action such as charge a battery or abort charging. The CMR register is also used to select the address and action to be performed on any data byte.

The address field (bits 0-4) contains the address of the data byte to be accessed. The values for this field may range from 00000 to 11111 for the storage RAM and from 00000 to 10000 for the control and status registers, with all other values not allowed.

The command field (bits 5-7) of this register indicates the action to be taken. Acceptable command field values are:

Bits			Command Field Values
7	6	5	
0	0	0	No operation
0	0	1	System off command
0	1	0	Read from address AAAAA of the bq2001 storage RAM
0	1	1	Read from address AAAAA of the bq2001 control and status registers
1	0	0	Write to address AAAAA of the bq2001 storage RAM
1	0	1	Write to address AAAAA of the bq2001 control and status registers
1	1	0	Start charge action command
1	1	1	Abort charge action command

The ***system off command*** may be used to shut the system down. When the system issues this command, the power switch control output, PSC, becomes high impedance, and the status register power switch state bit is cleared to 0.

The ***start charge action command*** starts a charge action if all other conditions are met (see Charge Action). This command begins a charge action when DC is valid or later becomes valid. This command is the only way to start a charge action if PSC is on (power switch state bit = 1).

The ***abort charge action command*** causes any charge action to be discontinued. The bq2001 resets the gas gauge and goes into a current-monitoring (gas gauging) state. This command may be used to reset the gas gauge to 0 or to stop a charge cycle.

Storage RAM

One of the 32 bytes of storage RAM is written following a CMR command of 100AAAAA and read following a CMR command of 010AAAAA. AAAAA is the byte address, from 00000 to 11111. This RAM is intended for storing cycle history and charge capacity for one or more batteries, and for recording power-management configuration settings and other data for a power-management BIOS. Data in the storage RAM is nonvolatile in the presence of a valid secondary battery or backup cell.

Control and Status Registers

One of the 17 bytes of control and status registers is written following a CMR command of 101AAAAA and read following a CMR command of 011AAAAA. AAAAA is the byte address, with only 00000 to 10000 allowed. Data in the control and status registers is nonvolatile in the presence of a valid secondary battery or backup cell. Table 4 summarizes the control and status registers.

Charge Period Register (CPR)

The charge period register (CPR) is programmed to define the charge period of a charge phase interval. The eight-second charge phase interval consists of a charge period and optional off and discharge periods. Each period may be programmed to be 1 to 256 of the 256 time segments per interval. The charge period is one plus the programmed value. The programmed value may be 0 to 255.

The following are examples of charge period duty cycle values:

CPR	Result
0FFH	Provides continuous current during charging.
63H	Provides for 3.13 seconds of full charge current out of every 8 seconds.

Values less than 0FFH are used to reduce the effective current during a charge and/or to provide time for a depolarization action by allowing time for a period of discharge (see Discharge Period Register).

Table 4. Control and Status Registers (X=Don't Care)

Symbol	Register Name	Address (TBD)	Read/ Write	Control Field or Status Bit								Units
				7(MSB)	6	5	4	3	2	1	0	
CPR	Charge period register		R/W	-	-	-	-	-	-	-	-	1/32 sec
CSR1	Charge setup register 1		R/W	GGNV quald	CA enable	discharge method		number of cells				
CSR2	Charge setup register 2		R/W	BR	GGNV	X	X	-ΔV sample time		-ΔV enable	trickle enable	
DPR	Discharge period register		R/W	-	-	-	-	-	-	-	-	1/32 sec
EDCV	End-of-discharge cell voltage register		R/W	-	-	-	-	-	-	-	-	10mV
GGH	Gas gauge, high byte		Read	-	-	-	-	-	-	-	-	$\frac{1}{46}$mVh
GGL	Gas gauge, low byte		Read	-	-	-	-	-	-	-	-	$\frac{1}{46}$mVh
GGTH	Gas gauge threshold, high byte		R/W	-	-	-	-	-	-	-	-	$\frac{1}{46}$mVh
GGTL	Gas gauge threshold, low byte		R/W	-	-	-	-	-	-	-	-	$\frac{1}{46}$mVh
LCRH	Last capacity register, high byte		Read	-	-	-	-	-	-	-	-	$\frac{1}{46}$mVh
LCRL	Last capacity register, low byte		Read	-	-	-	-	-	-	-	-	$\frac{1}{46}$mVh
MCT	Maximum charge time register		R/W	-	-	-	-	-	-	-	-	8 min
MCV	Maximum cell voltage register		R/W	-	-	-	-	-	-	-	-	10mV
MR	Mask register		R/W	-	-	-	-	-	-	-	X	
OCR	Output control register		R/W	-	-	-	-	-	-	-	X	
SR	Status register		Read	PS	SBF	GGN	DCV	BCL	EDV	CHG	INTF	
TPR	Trickle period register		R/W	-	-	-	-	-	-	-	-	1/32 sec

Charge Setup Register 1 (CSR1)

Charge setup register 1 (CSR1) contains four configuration fields.

The ***number of cells field*** (bits 0-3) contains the number of cells used to make up the battery. This register is programmed with a scale factor, typically the number of cells, to relate the measured battery voltage back to the single-cell voltage.

CSR1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	N	N	N	N

The maximum cell number is 10 (the initial default), and the minimum is 1. The value need not be the real number of cells, but must be scaled such that this value times the values in registers EDCV and MCV, respectively, are the EDV and maximum charge voltage limits.

Caution:

Using the EMU with improperly programmed voltage thresholds may damage the device.

The ***discharge method field*** (bits 4-5) is the nonoperational discharge method selector. Discharge-before-charge may be initiated on application of a valid DC level or when a charge action command is issued in the CMR.

The discharge method field is programmed to define the discharge method as follows:

CSR1 Bits							
7	6	5	4	3	2	1	0
-	-	D	D	-	-	-	-

Where DD is:

00 Never discharge (the initial default value).

01 Discharge until the gas gauge register value is greater than or equal to the gas gauge threshold register value or EDV is reached. This method may be used to provide battery conditioning cycles by deliberately controlling discharge depth. If full discharge (EDV) occurs, the final gas gauge value is stored in the last capacity register.

10 Discharge fully if the gas gauge value is greater than the gas gauge threshold. The discharge is terminated by the EDV limit. This method may be used to determine the battery capacity. At the end of this cycle, the final gas gauge value is stored in the last capacity register.

11 Never discharge.

The ***charge action enable field*** (bit 6) is programmed to 0 when charging and discharging are not to be performed. This bit may be set to 0 for the use of non-rechargeable batteries.

The E field values are:

CSR1 Bits							
7	6	5	4	3	2	1	0
-	E	-	-	-	-	-	-

Where E is:

0 Inhibits charge action initiation (the initial default value).

1 Allows charge action.

The ***GGNV qualified charge field*** (bit 7) is programmed to 1 to force GGNV to qualify DC initiation of charge action (power switch status bit = 0). When this bit is one and the power switch status bit is 0, charge action is initiated only if the CSR2 GGNV status bit = 1. This allows the host processor to block DC-initiated charge actions on a known fully charged battery. If enabled in CSR2, trickle charge occurs.

The Q field values are:

CSR1 Bits							
7	6	5	4	3	2	1	0
Q	-	-	-	-	-	-	-

Where Q is:

0 No GGNV qualification of charge action.

1 DC-initiated charge action only if GGNV = 1.

Charge Setup Register 2 (CSR2)

Charge setup register 2 (CSR2) contains three configuration fields and two read-only status bits. Bits 4 and 5 are not used.

The ***trickle enable field*** (bit 0) is programmed to 1 to enable trickle charge. When this bit is 1, trickle charge follows charge action termination due to full charge (indicated by -ΔV, maximum time, or maximum voltage).

The trickle enable field values are:

CSR2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	T

Where T is:

0 Trickle charge disabled

1 Trickle charge enabled

The ***-ΔV enable field*** (bit 1) is programmed to 1 to enable -ΔV sensing for full charge determination. When this bit is 1, a -ΔV observation is interpreted as full charge. When this bit is 0, a -ΔV observation is ignored.

The -ΔV enable fields are:

CSR2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	V	-

Where V is:

0 Ignore -ΔV.

1 Interpret -ΔV as full charge.

The ***sample time field*** (bits 2–3) is programmed to select the time between voltage samples used to determine -ΔV. Shorter times may be chosen when a rapid charge is required and the end of charge must be detected as soon as possible. Longer times may be chosen when slow charge rates are required.

The sample time field values are :

CSR2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	S	S	-	-

Where SS is:

00 8 seconds between samples

01 32 seconds between samples

10 128 seconds between samples

11 512 seconds between samples

The ***gas gauge not valid*** read-only status bit (GGNV) is set to indicate to the host processor that the gas gauge value does not reflect discharge from bq2001-determined full charge and is potentially invalid.

GGNV values are:

CSR2 Bits							
7	6	5	4	3	2	1	0
-	GGNV	-	-	-	-	-	-

Where GGNV is:

0 Gas gauge value reflects discharge from bq2001-determined full charge

1 Charge state not known; battery replaced or charge action not completed.

GGNV is set to 1 by either the start of a charge action or by SB going valid. GGNV is reset to 0 on charge action termination due to -ΔV, maximum voltage, or maximum time determination.

If GGNV is 1 and the power switch state bit equals 0, any discharge phase of a charge action is skipped.

The ***battery replaced*** read-only status bit (BR) indicates to the host that the battery has been removed and replaced; it is used to validate a new last capacity register value following DC-initiated charge. The battery replaced bit is set to 1 with the reappearance of a valid voltage at SB and is reset by an abort charge action command.

BR values are:

CSR2 Bits							
7	6	5	4	3	2	1	0
BR	-	-	-	-	-	-	-

Where BR is:

0 Battery has not been replaced since last reset.

1 Battery has been replaced.

Discharge Period Register (DPR)

The discharge period register (DPR) is programmed to define the optional discharge period—used for depolarization—of each charge phase interval. DPR is non-zero for burp charging. Each period may be programmed to be 0 to 254 of the 256 time segments per interval. The number of segments in the period is the same as the programmed value. The value in CPR has precedence over DPR. This means that within any eight-second interval, the charge period is completed before the discharge period is started, such that the maximum period allowed for discharge is 255 minus the CPR value.

The gas gauge is not valid during discharge periods within charge phase intervals.

End-of-Discharge Cell Voltage Register (EDCV)

The end-of-discharge cell voltage register (EDCV) is programmed with the value used to determine the secondary battery end-of-discharge voltage (EDV) threshold during operational or non-operational discharge. This value need not be the real single-cell voltage, but must multiply by the number of cells value in CSR1 to equal the EDV. Discharging to the EDV threshold generates an interrupt request on $\overline{INT}$, sets the status register interrupt flag and EDV bits, loads the value from GG into LCR, and—if selected—activates $\overline{PO_2}$.

Example:

For a termination voltage of 1.0V per cell, the value placed in EDCV should be 64H.

Gas Gauge Registers (GG)

The read-only gas gauge register pair (GG) indicates the capacity that has been removed from the battery. The GG value is interpreted by:

$$GG = S_R(\text{ohms}) \times \text{Removed Capacity(mAh)} \times 46$$

The gas gauge register pair is reset to 0 by:

- Charge action termination due to negative delta voltage, maximum charge time, or maximum voltage determination, any of which indicates full charge.
- An abort charge actions command written to CMR (command register).
- The reappearance of a valid voltage at SB, which indicates the battery was removed and replaced.

Gas Gauge Threshold Registers (GGT)

The gas gauge threshold register pair (GGT) is programmed to set the gas gauge threshold. At initiation of a charge action, this limit may determine the discharge phase activity (see CSR1, discharge method field). During operational discharge, reaching this limit generates an interrupt request on $\overline{INT}$, sets the status register interrupt flag and gas gauge notification bits and, if selected, activates $\overline{PO_5}$.

Last Capacity Registers (LCR)

The read-only last capacity register pair (LCR) is used to keep a copy of the most recently measured battery capacity. LCR is automatically loaded with the gas gauge value when the EDV limit is reached.

Maximum Cell Voltage Register (MCV)

The maximum cell voltage register (MCV) is programmed to define the maximum voltage per cell limit. This is one of three determinants of full charge. If the maximum voltage is reached before the -ΔV determination or maximum charge time is obtained, then the charge action is terminated, and the gas gauge and GGNV are reset. The MCV value need not be the real single-cell voltage, but—with the number of cells value in CSR1—defines the maximum battery voltage.

Maximum Charge Time Register (MCT)

The maximum charge time register (MCT) is programmed to define the maximum time for the charge phase of a charge action. This is one of three determinants of full charge. If this time value is reached before the -ΔV determination or maximum battery voltage is obtained, then the charge action is terminated and the gas gauge and GGNV are reset. The units for this register are eight minutes, for a maximum time of 34 hours.

Mask Register (MR)

The mask register (MR) is programmed to define which output pins—PO_1 to $\overline{PO_7}$—are controlled by specific bits of the status register (SR) or by specific bits of the output control register (OCR). Each of these open drain output pins can be set up to follow internally generated status bits or to reflect bits set by the host processor. See Table 5.

Output Control Register (OCR)

The output control register (OCR) is the control register by which the host processor can activate any of outputs $\overline{PO_1}$ to $\overline{PO_7}$. $\overline{PO_1}$ to $\overline{PO_7}$ reflect the status of OCR bits 0 to 6, respectively (1=output active), provided that host control is enabled (the appropriate masking bit in the mask register, MR, is set to 0). See Table 5.

Table 5. Mask Register

Bit	Value	Result
0	0	Not valid.
	1	Not valid.
1	0	$\overline{PO_1}$ follows OCR bit 1.
	1	$\overline{PO_1}$ follows SR charging bit.
2	0	$\overline{PO_2}$ follows OCR bit 2.
	1	$\overline{PO_2}$ follows SR end-of-discharge voltage bit.
3	0	$\overline{PO_3}$ follows OCR bit 3.
	1	$\overline{PO_3}$ follows SR backup cell low bit.
4	0	$\overline{PO_4}$ follows OCR bit 4.
	1	$\overline{PO_4}$ follows SR DC valid bit.
5	0	$\overline{PO_5}$ follows OCR bit 5.
	1	$\overline{PO_5}$ follows SR gas gauge notification bit.
6	0	$\overline{PO_6}$ follows OCR bit 6.
	1	$\overline{PO_6}$ follows SR secondary battery fault bit.
7	0	$\overline{PO_7}$ follows OCR bit 7.
	1	Not valid.

Status Register (SR)

The read-only status register (SR) indicates the status of various battery operations and conditions. The bits are defined as:

SR Bit	Bit Name	If Set to 1
0	INTF	Interrupt flag
1	CHG	Charging
2	EDV	End-of-discharge voltage
3	BCL	Backup cell low
4	DCV	DC valid
5	GGN	Gas gauge notification
6	SBF	Secondary battery fault
7	PS	Power switch state equals ON

Interrupt flag (INTF) is set when $\overline{INT}$ becomes active. INTF is reset to 0 when a CMR read command causes the SR byte to be loaded into the read buffer. INTF is output from the buffer with the subsequent bit access. INTF is only set when PS = 1.

Charging (CHG) is set whenever a charge action is in progress. CHG equals 0 during no action or during trickle charge.

End-of-discharge voltage (EDV) is set when the secondary battery voltage is at or below the threshold defined by the CSR1 number of cells field value and the EDCV register value. Otherwise, this bit is 0.

Backup cell low (BCL) is set to indicate low backup cell voltage. If the voltage at BC_I is less than or equal to 2.1 (± 0.1)V, then BCL is set to 1. Otherwise this bit is 0.

DC valid (DCV) is set to indicate valid DC. The bit is set to 1, allowing charge action to occur, if DC is greater than 4.5V. The bit is set to 0 whenever DC is less than 4.4V (100mV hysteresis). If this bit is 0, no charge action may occur.

Gas gauge notification (GGN) is set when the gas gauge reaches or exceeds the programmed gas gauge threshold.

Secondary battery fault (SBF) is set to indicate a possible open or short cell. This bit is set to 1 if the voltage monitored at SB is less than 0.5V times the number of cells defined in CSR1. If this bit is set, no charge action may occur.

Power switch state (PS) indicates $\overline{PSC}$ status. This bit is set to one by a $\overline{PS}$ input that activates $\overline{PSC}$ and set to 0 by execution of the CMR power-off command to deactivate $\overline{PSC}$. The application may need to ensure that the power switch state bit reflects the system power status.

Trickle Period Register (TPR)

The trickle period register (TPR) is programmed to define the charge period during trickle charge. This register is used following full charge determination to provide a lower effective current for charge maintenance. Each period may be programmed to be 1 to 256 of the 256 time segments per interval. The charge period is one plus the programmed value. The programmed value may be 0 to 255.

TPR examples include:

TPR	Result
7	Provides for an average current of about 1/32 of the maximum charge current.
0	Provides for an average current of 1/256 of the maximum charge current.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{DC}	DC voltage applied on DC relative to V_{SS}	-0.3 to 18	V	
V_{SB}	DC voltage applied on SB relative to V_{SS}	-0.3 to 18	V	
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_{BCI}	DC voltage applied on BC_I relative to V_{SS}	-0.3 to 7.0	V	
V_{OP}	DC voltage applied on all open drain outputs relative to V_{SS}	-0.3 to 36	V	
V_{SR}	DC voltage applied on S_R relative to V_{SS}	-0.3 to 18	V	$V_{SR} \leq V_{SB} + 0.3$
V_{IF}	DC voltage applied on $\overline{DS}$, RS, DQ, and $\overline{INT}$ relative to V_{SS}	-0.3 to 7.0	V	
I_{BC}	Output current on BC	20	mA	
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-10 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameters	Minimum	Typical	Maximum	Unit	Notes
V_{DC}	DC supply voltage	4.5	-	18	V	
V_{SB}	SB supply voltage	3.0	-	18	V	
V_{CC}	V_{CC} supply voltage	4.5	5.0	5.5	V	
V_{BCI}	BC_I supply voltage	2.0	-	6.0	V	
V_{BC}	BC output supply voltage	V_{BCI}-0.01	V_{BCI}	V_{BCI}+0 .01	V	Regulated $V_{SB} > V_{BCI}$
		V_{BCI} - 0.3	-	V_{BCI}	V	Regulated $V_{SB} < V_{BCI}$
V_{SS}	Supply voltage	0	0	0	V	
V_{SR}	Sense resistor input voltage	V_{SS}	-	V_{SB} + 0.3	V	
V_{IL}	Logic low-level input voltage for $\overline{DS}$, RS, DQ	-0.3	-	0.8	V	
V_{IH}	Logic high-level input voltage for $\overline{DS}$, RS, DQ	2.2	-	V_{CC} + 0.3	V	
V_{OL}	Logic low-level output voltage for DQ	-	-	0.4	V	I_{OL} = 4.0mA
V_{OH}	Logic high-level output voltage for DQ	2.4	-	-	V	I_{OH} = -2.0mA
V_{OCC}	Charge control output voltage	-	-	36	V	I_{OD} = 0
V_{OD}	Open-drain output voltage	-	-	18	V	All open-drain outputs other than charge control, I_{OD} = 0
I_{OD}	Open-drain sink current for $\overline{PO_1}$–$\overline{PO_7}$, CC, CD, $\overline{PSC}$, $\overline{INT}$	-	-	20	mA	V_{OD} = 2V
I_{LI}	Input leakage current for $\overline{DS}$, RS, DQ	-	-	± 1	µA	
I_{LO}	Output leakage current for DQ	-	-	± 1	µA	Outputs in high impedance
I_{CC}	Operating current, DC or V_{CC} supply	-	3	5	mA	
I_{CCDR}	Data-retention current from BC_I input	-	0.1	1	µA	I_{BC} = 0, I_{PS} = 0
I_{CCSB}	Data-retention current from SB input	-	1	10	µA	I_{BC} = 0, I_{PS} = 0
I_{BC}	Output current on BC	-	-	1	mA	SB or BC_I supplied; V_{BC} = 3.0V, T_A = 25°C
I_{PS}	$\overline{PS}$ active input current	20	30	45	µA	Internal 100K ohm pullup to V_{BCI}

DC Thresholds

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{SBF}	Secondary battery fault	0.45 x N	0.5 N	0.55 N	V	N = number of cells per CSR1
V_{MAXC}	Maximum charge voltage	MCV x (0.99 x N)	MCV x N	MCV x (1.01 x N)	V	N = number of cells per CSR1
V_{EDCV}	End-of-discharge voltage	EDCV x (0.99 x N)	EDCV x N	EDCV x (1.01 x N)	V	N = number of cells per CSR1
V_{BCL}	Backup cell low voltage	2.0	2.1	2.2	V	
V_{DCV}	DC valid voltage (on)	4.4	4.5	4.6	V	100mV hysteresis
	DC valid voltage (off)	4.3	4.4	4.5	V	

Note: Typical values indicate operation at T_A = 25°C.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{SB}	SB input resistance	400	500	600	KΩ

Notes: Typical values indicate operation at T_A = 25°C.
This parameter is sampled and not 100% tested.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Logic input/output capacitance (DQ)	-	-	10	pF	$V_{I/O}$ = 0V
C_{IN}	Logic input capacitance ($\overline{DS}$, RS)	-	-	8	pF	V_{IN} = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 V to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load for DQ (including scope and jig)	See Figures 6 and 7
Output load for all open-drain outputs	See Figure 8

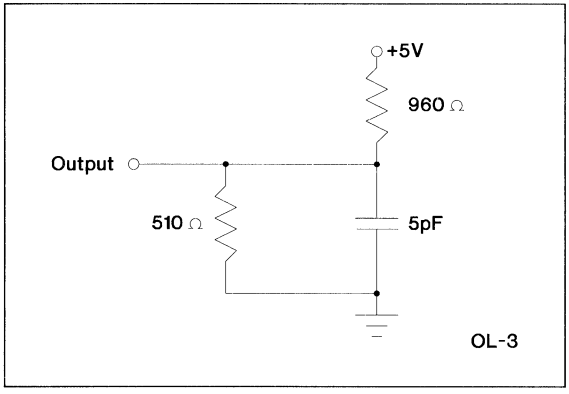


Figure 6. Output Load A

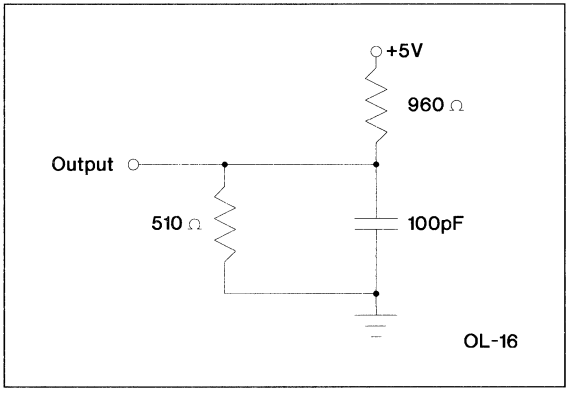


Figure 7. Output Load B

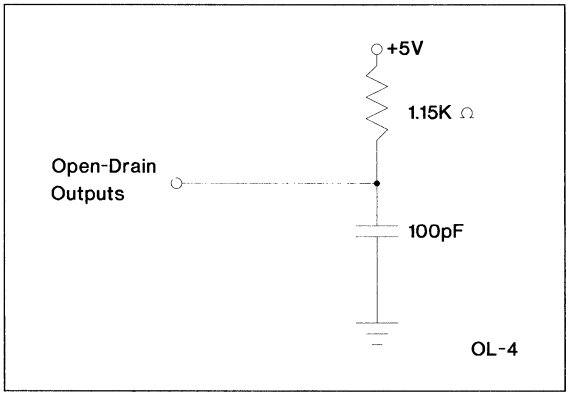


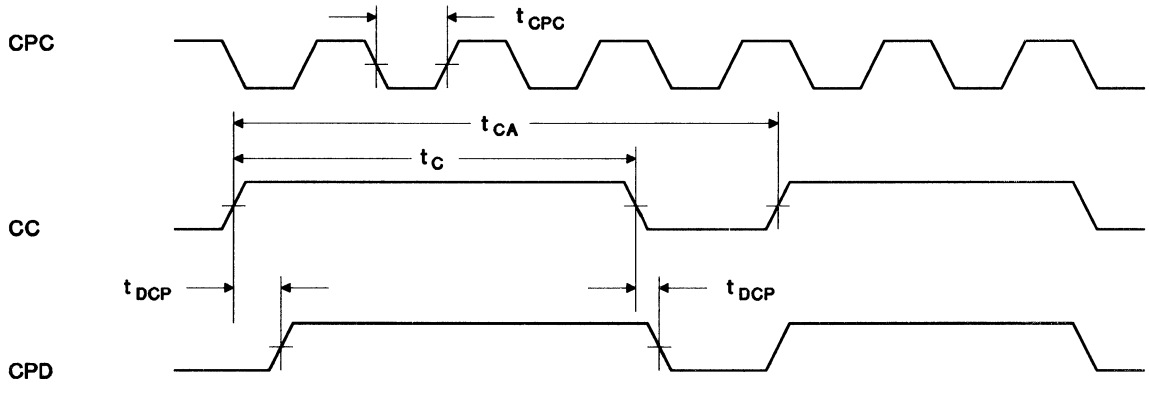
Figure 8. Output Load C

Charge Action Timing (T_A = 0 to 70°C, DC = 4.5V to 18V)

Signal	Characteristic	Minimum	Typical	Maximum	Units
t_{DCS}	DC slew rate	-	-	18	mV/µs
t_{CPC}	Charge pump time	6	8	10	µs
t_{DCP}	Diode out after CC high	4	-	-	µs
t_{DTC}	Discharge phase to charge phase transition time	6	8	10	µs
t_{CA}	Charge action interval	6	8	10	s
t_C	Charge period	$\frac{t_{CA}}{256}$	-	t_{CA}	s
t_I	Charge period to discharge period transition time	-	$\frac{t_{CA}}{128}$	-	s
t_D	Discharge period	0	-	$\left(t_{CA} \times \frac{254}{256}\right) - t_C$	s
t_T	Trickle charge period	$\frac{t_{CA}}{256}$	-	t_{CA}	s
t_{CT}	Charge time	0	-	255(60 x t_{CA})	s

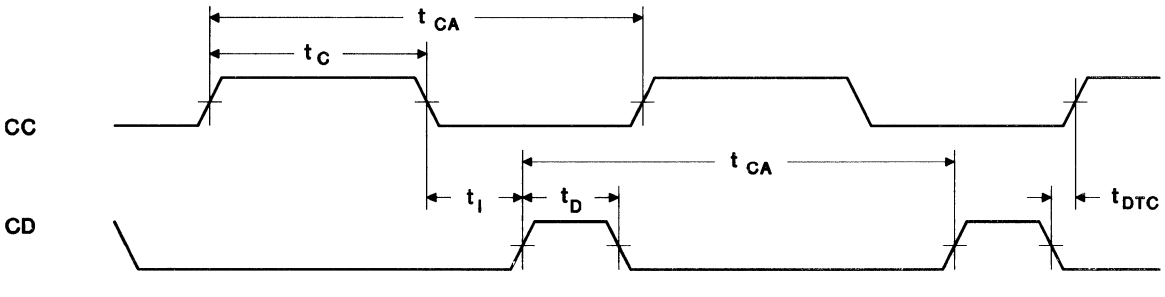
Note: Typical values indicate operation at T_A = 25°C.

Charge Pump Timing



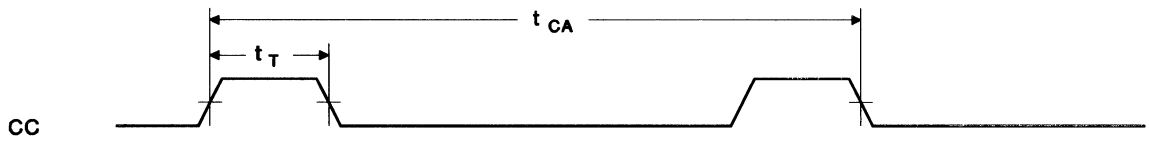
CC-1

Charge Action Timing



CC-2

Trickle Charge Timing



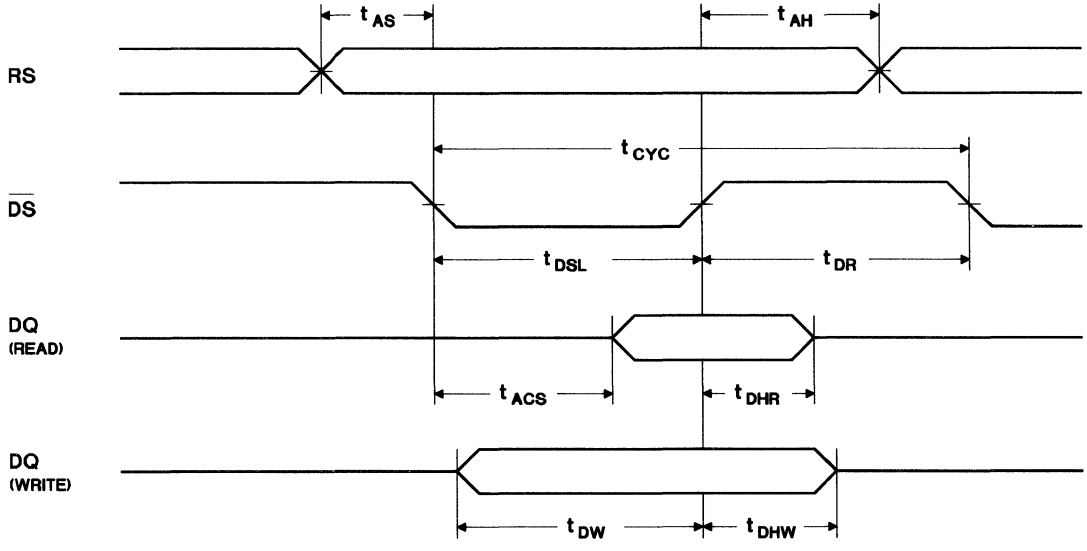
CC-3

Bus Timing (T_A = 0 to 70°C, V_{CC} = 5V± 10%)

Signal	Characteristic	Minimum	Typical	Maximum	Unit	Conditions
t_{CYC}	Cycle time	250	-	-	ns	
t_{DR}	$\overline{DS}$ recovery time	155	-	-	ns	
t_{DSL}	Data strobe low time	80	-	-	ns	
t_{ACS}	Read data access time	-	-	30	ns	Output load A
t_{DHZ}	Read data to high Z	0	-	30	ns	Output load B
t_{DW}	Write data setup time	40	-	-	ns	
t_{DHW}	Write data hold time	0	-	-	ns	
t_{AS}	RS setup time	0	-	-	ns	
t_{AH}	RS hold time	0	-	-	ns	
t_{INT}	Interrupt pulse width	6	8	10	µs	Output load C
t_{IRT}	Interrupt recovery time	6	8	10	µs	Output load C

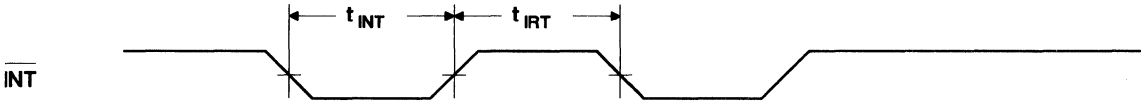
Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5.0V.

Read/Write Timing



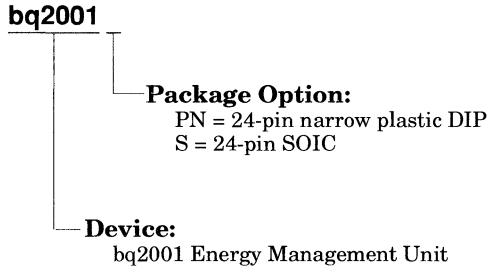
RC-8

Interrupt Timing



INT-2A

Ordering Information



Energy Management Unit (EMU)

Features

- Microprocessor peripheral for the total energy management of battery-operated systems
- Direct measurement of battery consumption and capacity
- Fast charging and conditioning control for nominal 3.6V to 12V nickel cadmium, lead acid, or nickel hydride batteries
- Full-charge detection by negative delta voltage method, maximum voltage, and maximum time
- Register-controlled outputs for energy management
- Regulated 5V output to sustain DRAM sleep mode
- Operates from 4.5–18V DC or 4.5–5.5V V_{CC} supplies
- 24-pin SDIP or SOIC

General Description

The CMOS bq2002 Energy Management Unit (EMU) is a low-power microprocessor peripheral providing battery and energy management services for systems using rechargeable (secondary) batteries. The bq2002 works directly from the DC charging supply, operating as programmed, or from 5V V_{CC}, operating as a microprocessor peripheral. bq2002-based systems can easily incorporate sophisticated capacity monitoring, battery management, DRAM sleep mode supply services, and power-conservation capabilities.

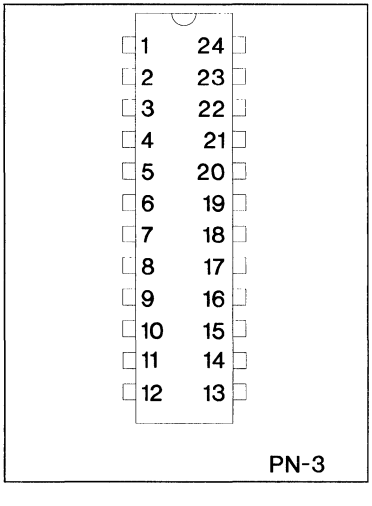
The "gas gauge" register provides the actual charge consumption from the secondary battery and allows measurement of the battery capacity. The programmed end-of-discharge voltage (EDV) threshold determines full discharge.

Battery management includes charge control at standard to fast charge rates, with full charge determined using the preferred negative delta voltage ($-\Delta V$) method, a maximum voltage threshold, and a maximum time limit. Trickle charge control begins after full charge is determined. Non-operational discharge before charge may be selected for cell conditioning or capacity measurement. Charge patterns may be programmed to be constant, pulsed, or "burp" (alternating charge/discharge).

When system power is off, the bq2002 may power DRAM sleep mode operation through the battery backup output (BB). The bq2002 regulates 6.5V to 18V from the secondary battery to a 5.3V output on BB. When system power is on, the 5.3V supply may be used to charge a backup battery that sustains the DRAM when the secondary battery is absent or depleted. To prevent overdepletion, the battery backup output is shut off when the secondary battery voltage falls below 0.9V per cell.

Power management is supported by eight open-drain outputs controlled by the EMU or the host processor. These may be allocated for subsystem control, LED activation, EMU status indication, and system power switch control.

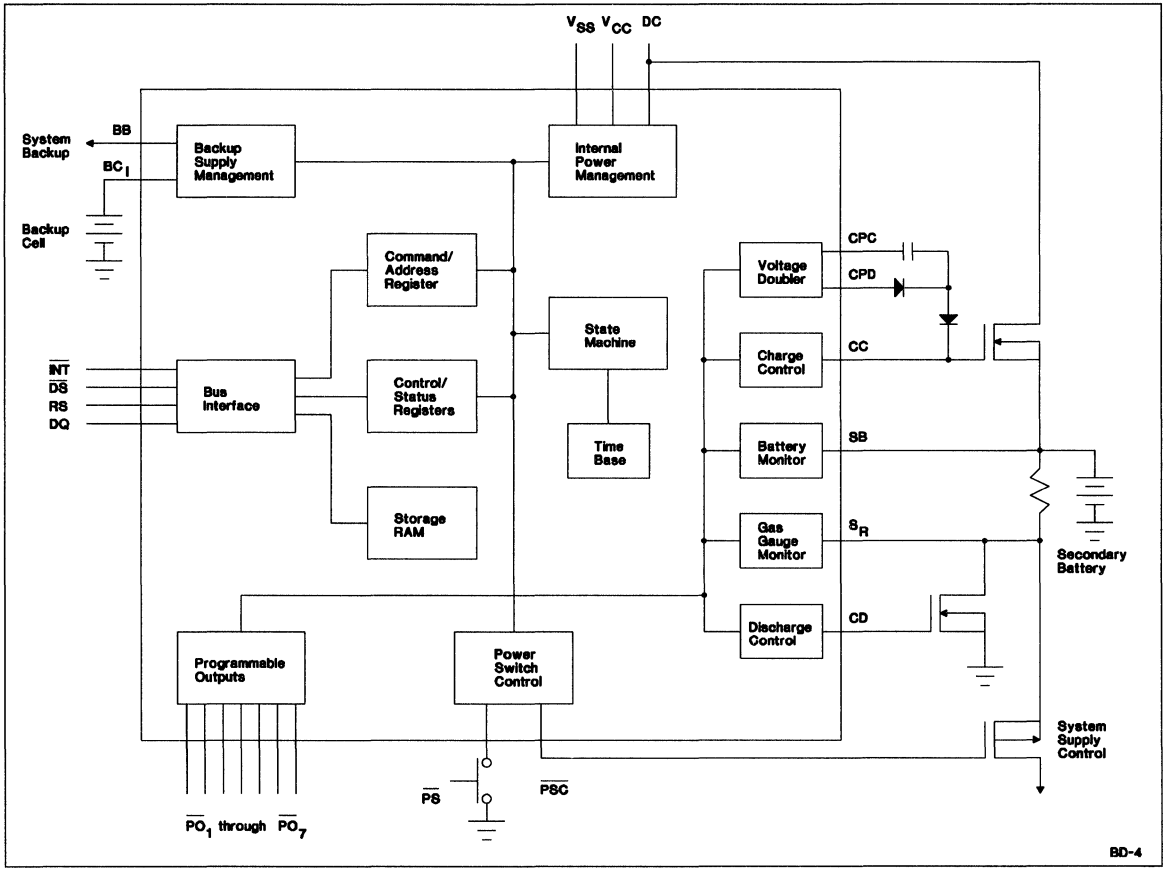
Pin Connections



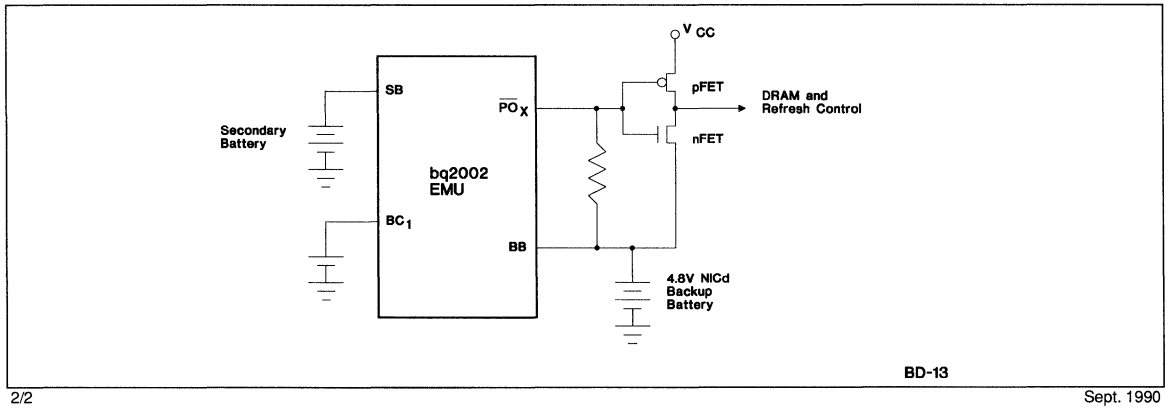
Pin Names

$\overline{DS}$	Data strobe input
RS	Register select input
DQ	Data input/output
$\overline{INT}$	Interrupt request output
DC	Charging supply input
SB	Secondary battery input
BB	Battery-backup output
BC_I	Backup cell input
CC	Charge control output
CPC	Charge pump capacitor output
CPD	Charge pump diode output
CD	Discharge control output
S_R	Sense resistor input
$\overline{PS}$	Power switch input
$\overline{PSC}$	Power switch control output
$\overline{PO_1}$	Charging indicator or programmable output 1
$\overline{PO_2}$	End-of-discharge voltage indicator or programmable output 2
$\overline{PO_3}$	Backup cell low indicator or programmable output 3
$\overline{PO_4}$	DC valid indicator or programmable output 4
$\overline{PO_5}$	Gas gauge threshold indicator or programmable output 5
$\overline{PO_6}$	Secondary battery fault or programmable output 6
$\overline{PO_7}$	Programmable output 7
V_{CC}	+5V system supply input
V_{SS}	System ground

Block Diagram



5V Backup Management



Designing With the EMU

Using the bq2001

Introduction

This design note provides information to simplify the integration of the bq2001 EMU within microprocessor and microcomputer systems. It is to be used with the bq2001 data sheet. Battery monitoring and charging are discussed to provide a framework for understanding EMU functionality. EMU application strategies and hardware and software interfaces are outlined.

Battery application manuals, engineering handbooks, and specifications should be obtained from the battery supplier.

The EMU functional blocks are shown in Figure 1. The EMU application normally involves four energy sources, as described in Table 1 and discussed below.

Table 1. Energy Sources

Source	Functions Powered
DC input	All except micro interface and backup cell output
V_{CC} input	All except voltage doubler and backup cell output
SB input	Only backup cell output and nonvolatile memory
BC_I input	Only backup cell output and nonvolatile memory

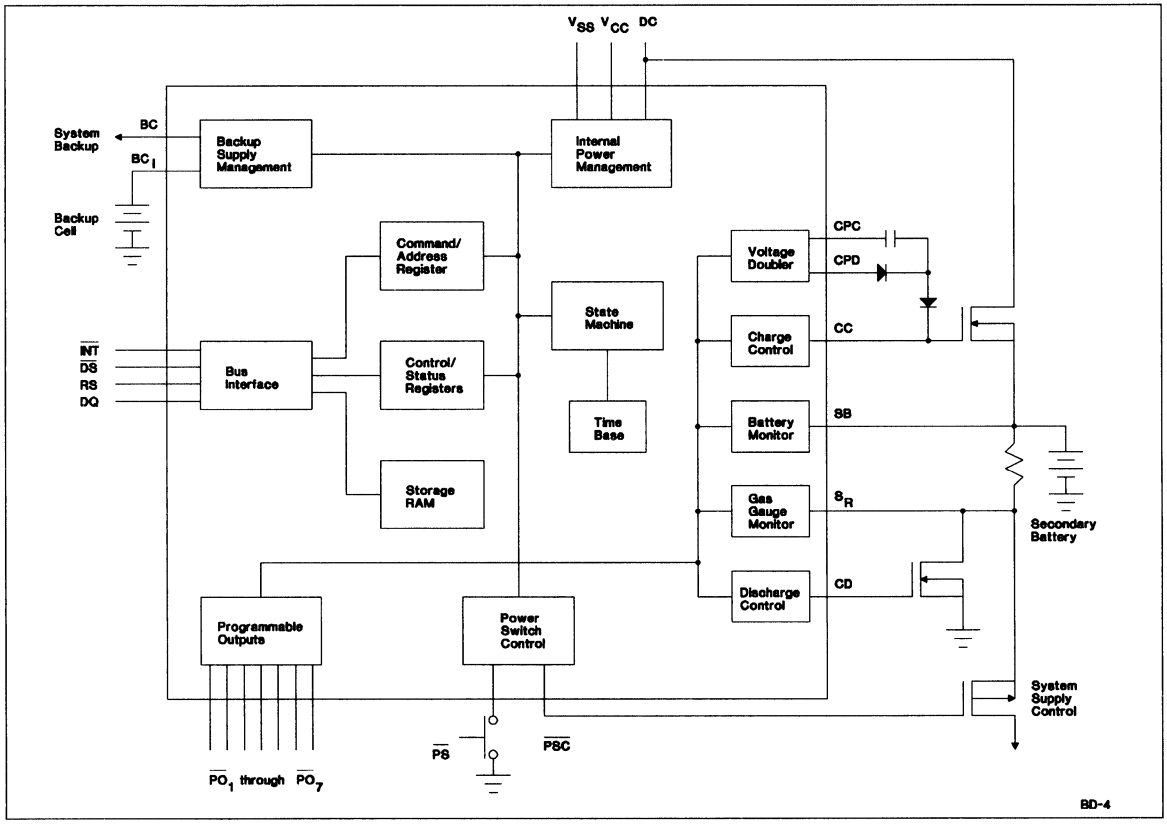


Figure 1. EMU Block Diagram

Energy Sources

The DC charging supply input must be from 4.5V to 18V. Voltages below 4.5V are not considered valid. The DC input powers all the EMU's operations except for the microprocessor interface and the backup cell output, BC. When the EMU is powered from DC, capacity monitoring and programmed charge actions may occur.

The Vcc input powers all blocks of the EMU except the voltage doubler outputs, CPC and CPD, and the backup cell output, BC. When the EMU is powered from Vcc, any charge actions require a valid DC input.

The secondary battery input, SB, must be greater than 0.5 V per cell to be valid. The secondary battery input is the primary input for EMU nonvolatility and for powering the backup cell output, BC.

The backup cell input, BC_I, must be at least 2V to be valid. When the voltage at SB can no longer provide a BC output greater than the BC_I input, the backup cell input becomes the input for EMU nonvolatility and for powering the backup cell output, BC.

Microprocessor Interface

The EMU is a microprocessor peripheral with control and storage registers that are programmed to perform various energy management functions. The state and condition of the secondary battery may be determined by reading the EMU registers.

Microprocessor Hardware Design

Figure 2 shows a typical interface between a microprocessor and the EMU. The microprocessor communication with the EMU is performed using a three-line serial interface to a standard microprocessor bus. The EMU interface is powered by Vcc.

Microprocessor Software Design

The serial software interface to the EMU is best described by example. The code in Listing 1 is an example of EMU interface software for a PC environment. Other systems have similar requirements.

When a command, read, or write operation is performed, the system must inhibit interrupts from the EMU during the complete transfer time.

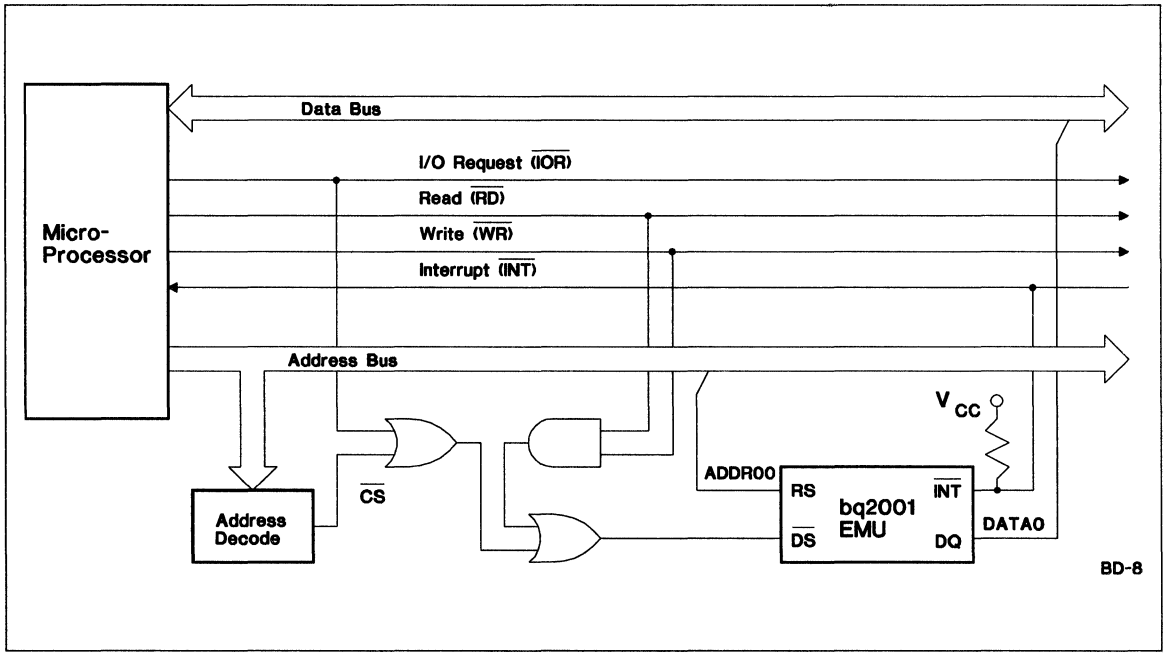


Figure 2. Microprocessor Interface

Listing 1. EMU Communication Functions (1 of 3)

```
.LIST
   PAGE   50,130
   TITLE  EMU Utilities
   NAME    EMU_Util
.MODEL COMPACT
;
;*************************************************************
;
;  DESCRIPTION: Provides READ, WRITE, and COMMAND access to EMU
;
;  PROTOTYPE: unsigned char emu_read(unsigned char command)
;           void emu_cmd(unsigned char command)
;           void emu_wrt(unsigned char command, unsigned char emu_data)
;
;  FUNCTION:  emu_read returns the requested data from the EMU.
;           emu_cmd writes the requested command to the EMU.
;           emu_wrt writes the requested data to the EMU.
;
;  ENTRY:     command is an unsigned char containing the command
;           or command plus address to be sent to the EMU.
;For emu_read, command should contain either:
;     1. 011AAAAA for read a control or
;        status register at location AAAAA.
;     2. 010AAAAA for read a storage register
;        at location AAAAA.
;For emu_cmd, command should contain any one of
;the following commands where XXXXX is don't
;care:
;1. 000XXXXX for a no operation.
;2. 001XXXXX for system-off command.
;3. 110XXXXX for start a charge action.
;4. 111XXXXX for abort a charge action.
;For emu_wrt, command should contain either:
;     1. 011AAAAA for write a control or
;        status register at location AAAAA.
;     2. 010AAAAA for write a storage register
;        at location AAAAA.
;emu_data is an unsigned character containing the data
;to be written to a control/status or storage
;register.
;
;  RETURN: emu_read returns an unsigned character that contains
;the data from a control/status or storage
;register.
;           emu_cmd returns a void.
;           emu_wrt returns a void.
;
;*************************************************************
;
  _TEXT     SEGMENT  WORD PUBLIC 'CODE'
  _TEXT     ENDS
```

Listing 1. EMU Communication Functions (2 of 3)

```
52    ;
53    ;*******************************
54    ;
55    ;EMU I/O port address
56    ;
57      EMU_CMD_REG     EQU   710H
58      EMU_DAT_REG     EQU   711H
59    ;
60    ;*******************************
61    ;
62      _TEXT     SEGMENT
63    ;
64      _emu_read PROC
65    ;
66                Public      _emu_read
67    ;
68                Push  BP
69                Mov   BP,SP
70    ;
71    ;     Send command to EMU
72    ;
73                Mov   CX,8              ;eight bits
74                Mov     AL,[BP+6]       ;of command
75                Mov     DX,EMU_CMD_REG  ;at this port
76                Cli                     ;disable interupts
77      send_rc:
78                Out     DX,AL           ;one bit at a
79                Shr     AL,1            ;time through
80                Loop    send_rc         ;data bit 0
81    ;
82    ;       Get EMU data
83    ;
84                Mov     CX,8            ;eight bits
85                Inc     DX              ;of data from EMU
86    get_rd:
87                In      AL,DX           ;get a bit
88                ROR     AX,1            ;save it
89                Loop    get_rd          ;get the next
90    ;
91                Sti                     ;enable interrupts
92                Mov     AL,AH           ;return byte
93                Xor     AH,AH
94                Pop     BP
95                Ret
96    _emu_read   ENDP
97    ;
98    _emu_cmd    PROC
99    ;
100               Public        _emu_cmd
101   ;
102               Push    BP
```

Listing 1. EMU Communication Functions (3 of 3)

```
103                 Mov     BP,SP
104     ;
105     ;       Send command to EMU
106     ;
107                 Mov     CX,8                ;eight bits
108                 Mov     AL,[BP+6]           ;of command
109                 Mov     DX,EMU_CMD_REG      ;at this port
110                 Cli                         ;disable interupts
111     send_cmd:
112                 Out     DX,AL               ;one bit at a
113                 Shr     AL,1                ;time through
114                 Loop    send_cmd            ;data bit 0
115     ;
116                 Sti                         ;enable interrupts
117                 Pop     BP
118                 Ret
119     _emu_cmd    ENDP
120     ;
121     _emu_wrt    PROC
122     ;
123                 Public      _emu_wrt
124     ;
125                 Push    BP
126                 Mov     BP,SP
127     ;
128     ;       Send command to EMU
129     ;
130                 Mov     CX,8                ;eight bits
131                 Mov     AL,[BP+6]           ;of command
132                 Mov     DX,EMU_CMD_REG      ;at this port
133                 Cli                         ;disable interupts
134     send_wrt:
135                 Out     DX,AL               ;one bit at a
136                 Shr     AL,1                ;time through
137                 Loop    send_wrt            ;data bit 0
138     ;
139     ;         Get EMU data
140     ;
141                 Mov     CX,8                ;eight bits
142                 Inc     DX                  ;of data
143                 Mov   AL,[BP+8]             ;to EMU
144     send_wr:
145                 In      AL,DX               ;get a bit
146                 Shr     AL,1                ;save it
147                 Loop    send_wr             ;get the next
148     ;
149                 Sti                         ;enable interrupts
150                 Pop     BP
151                 Ret
152     _emu_wrt    ENDP
153     _TEXT       ENDS
154                 END
```

Command Request

As shown, all communications with the EMU must start with a command written to the command register, CMR. There are two groups of commands, the action commands and the data commands.

The transmission of a command is shown in Listing 1, lines 73 through 80, lines 107 through 114, and lines 130 through 137. A command is sent one bit at a time through data bit 0 using an OUT instruction. The RS input is made low by connecting it to address line A0 and using an OUT instruction to an even EMU address. The complete command transmission requires eight out instructions. The least-significant bit is sent first. Seven arithmetic shifts are used to position the next data bit in bit 0. Within the transmission loop, software delay time may be required depending on execution speed.

Action Command

Each action command instructs the EMU to perform one of the following actions:

- Start a charge action
- Stop a charge action
- Turn the system off
- No operation

The actual command codes required to initiate these actions are listed in Listing 1, lines 29 through 32.

Data Commands

The four data commands instruct the EMU to prepare to receive or send data from a particular EMU register. The EMU has two register sets. One set contains 17 bytes dedicated to the control and status of the EMU. The other register set contains 32 bytes for general nonvolatile storage. Each register set has its own pair of commands for read and write. The four data command codes are listed in Listing 1, lines 22 through 25 and lines 34 through 37.

Read Data Operation

The read data command is sent first during a read operation, identifying the register set and containing the address of the data to be retrieved. The read operation code is shown in Listing 1, lines 84 through 89. The data is read using an IN instruction to an odd EMU address, causing RS to be high during each access. The least-significant bit is read first. Each data bit is rotated to the high byte of AX. At the end of eight INs and RORs, the EMU data is in the AH register. This data is then returned back to the calling routine.

Write Data Operation

The write data command is sent first during a write operation, identifying the register set and containing the address of the register to be written. The write operation is similar to the read operation and is shown in Listing 1, lines 141 through 147. After the write command, data is sent bit by bit using data bit 0 and an OUT instruction to an odd EMU address. The odd address makes the RS input high during each bit transfer. The data transfer takes eight OUT instructions. The least-significant bit is sent first. An arithmetic shift right is used to place the next data bit into bit 0 after each OUT instruction.

Interrupt Request Service

The $\overline{\text{INT}}$ pin, if used, requires software service. Three events can cause an interrupt request:

- Power switch request
- End-of-discharge voltage reached
- Gas gauge threshold reached

Each event requires its own particular service. Each interrupt event sets the interrupt flag, INTF, to 1.

The INTF is a read-once flag and is automatically cleared after each read. The EMU interrupt service routine should check the state of INTF in the EMU status register SR. INTF is read by first issuing a control and status register read command with the SR address and then reading the SR data (described above in Read Data Operation).

INTF should be checked as part of the system initialization routine. INTF is set if the $\overline{\text{PS}}$ input is toggled during system startup. INTF is cleared after it is read, freeing it for future interrupt request indications. The system should also retain the status of the gas gauge notification bit, GGN, and the end-of-discharge voltage bit, EDV. Determination of a gas-gauge-threshold-reached or end-of-discharge-voltage-reached event is accomplished by reading the GGN and EDV bits at the same time as the INTF bit, and comparing their values to their previous states. Appropriate actions in response to these events are discussed later.

Determination of a power switch event is also done by examining the GGN and EDV bits. If neither GGN nor EDV has become active, then the system should assume that a power switch service request has been issued. The system must then take the appropriate action for the power switch service. This action may be either accept that the system has been powered up (that is, take no action) or issue a command to the EMU to turn off the $\overline{\text{PSC}}$ (power switch control) output.

Secondary Battery Monitoring

The EMU provides real-time monitoring of the secondary battery when powered by the DC input or the V_{CC} input. The secondary battery capacity consumption and the voltage per cell are determined so that the system may take appropriate action.

Battery-Monitoring Hardware Design

SB and S_R are the two inputs to the secondary battery monitor.

Secondary Battery Input

SB, the secondary battery input pin, is used to monitor the secondary battery voltage. The secondary battery voltage is internally divided by the number of cells as programmed in charge setup register 1 (CSR1) to determine the voltage per cell. The voltage per cell is used to determine:

- Secondary battery fault (less than 0.5V per cell)
- End-of-discharge cell voltage threshold (as programmed in the EDCV register)
- Maximum voltage per cell (as programmed in the MCV register)
- Delta voltage

The SB input also monitors the secondary battery voltage to determine that the secondary battery has been replaced. As the SB input rises through 1V, the battery replacement bit, BR, and gas gauge not valid bit, GGNV, are set to 1, and the gas gauge register pair is reset.

The charge control aspect of the SB input is discussed in greater detail in the Battery Charging and Condition section.

Sense Resistor Input

S_R, the sense resistor input pin, is the other voltage input for secondary battery monitoring. The voltage across the sense resistor is determined between the SB and S_R inputs. This voltage drop is used to determine the rate of discharge from the secondary battery. This timed rate of discharge is summed by the EMU and is available in the gas gauge register pair.

Sense Resistor Selection

The voltage across the sense resistor is determined by the resistance of the sense resistor and the current through the resistor. The sense resistor should be chosen such that the capacity measurement error is minimized over the range of system operating currents.

Figure 3 shows the relative error in the determination of the voltage across the sense resistor versus the voltage being measured. This should be considered when choosing the proper resistor for capacity determination. The least relative error occurs around 70 mV. The EMU provides less than 2 percent relative measurement error over the range from 30 to 170 mV, nearly a 6-to-1 supply current ratio.

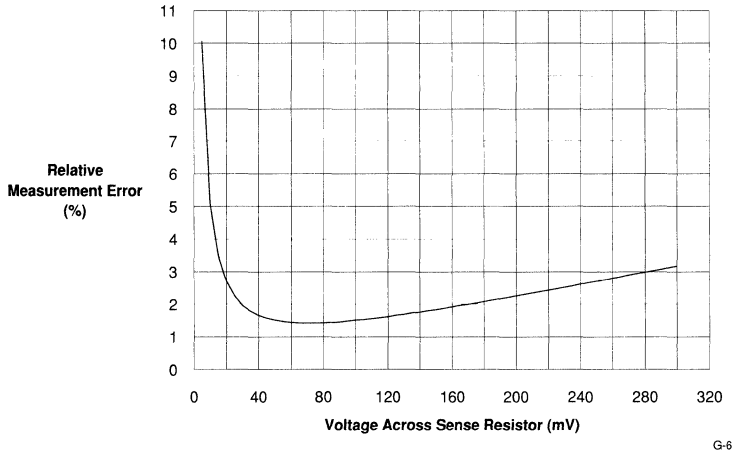


Figure 3. Gas Gauge Measurement Error

The resistor value may be selected following determination of typical system operating current profiles and applying one of the two following equations.

For many applications, particularly if the system has a narrow range of operating current, the resistor choice can be made using the average current method of Equation 1.

Equation 1. Simple Method for Sense Resistor Choice

$$R = \frac{0.0707}{I_{avg}}$$

where:

R = Sense resistance (ohms)

I_{avg} = Time-average system operating current (amperes)

For those systems where the minimum absolute capacity error is desired, Equation 2 can be used.

Equation 2. Optimum Sense Resistor Determination

$$R = 0.0707 \left(\sum_{i=0}^{n} t_i \Big/ \sum_{i=0}^{n} t_i I_i^{\,2} \right)^{\frac{1}{2}}$$

where:

R = Sense resistance (ohms)

t_i = Relative operating time when the current is I_i

I_i = A particular operating current associated with time t_i (amperes)

Equation 2 can be used to account for a wide range of operating currents associated with the various system operations. The designer may partition the current usage and estimate the active time for that usage. This data is then used in Equation 2 to determine the sense resistor value for minimum capacity error.

The following example demonstrates Equations 1 and 2 methods, as applied to two different use conditions:

System Capacity = 1.0 Ah

Use Condition	Current Level	Time (%)	Capacity (%)
Use A (3:1)	0.5 A	30	15
	1.0 A	40	40
	1.5 A	30	45
Use B (6:1)	0.5 A	30	9
	1.5 A	40	36
	3.0 A	30	55

Results are shown in the tables below.

Equation 1 Results

Use Condition	Time Avg Current (A)	Resistance (mΩ)	V_{min} (mV)	V_{max} (mV)	V_{avg} (mV)	Relative Error (%)
Use A	1.0	70.7	35.4	106	81.3	1.520
Use B	1.65	42.9	21.4	129	95.6	1.662

Equation 2 Results

Use Condition	RMS Current (A)	Resistance (mΩ)	V_{min} (mV)	V_{max} (mV)	V_{rms} (mV)	Relative Error (%)
Use A	1.07	65.9	33.0	98.9	70.7	1.516
Use B	1.92	36.9	18.5	112	70.7	1.642

Observations

- Wide operating supply ranges can be supported at low average error.
- Current levels contributing small portions of capacity drain may operate at relatively high error to achieve lowest average error.

Either analysis might similarly be performed on "nominal," "low drain," and "high drain" capacity usage profiles to select a compromise sense resistor well-suited to a range of system applications having different supply current profiles.

Other Selection Factors

The maximum voltage drop across the sense resistor must also be considered when choosing the resistor value. The sense resistor voltage drop reduces the effective battery voltage to the system. The maximum voltage drop occurs at maximum system supply current, plus any simultaneous EMU-controlled discharge current. Voltage drop may be minimized by designing to monitor only current consumption across a reasonable range of currents. Extremely low currents typically do not contribute significantly to system discharge and may be reasonably estimated based on duration.

Average voltage drop may also be considered when choosing the resistor value for applications where the monitoring is desired over long periods of time. The average voltage drop determines the time to rollover in the gas gauge register pair (see below). An average voltage drop of 70 mV results in rollover after 20 hours of active monitoring, and an average voltage drop of 140 mV results in rollover after 10 hours.

The measurement error associated with the voltage drop during EMU-controlled discharge may be considered separately, depending on system strategy for such discharge. Typically this discharge only applies to a small portion of the capacity.

Capacity-Monitoring Software Design

The system software can determine the secondary battery condition whenever Vcc is supplied to the EMU. The EMU provides the following capacity and diagnostic information for use in capacity monitoring:

- Capacity removed
- Gas gauge threshold notification
- Last capacity measured
- End-of-discharge voltage status
- Secondary battery fault
- Battery replaced
- Gas gauge not valid

In general, battery capacity monitoring should be considered as relative and approximate, despite the accuracy discussed above. A reasonable parallel might be the gas gauge of a car.

The key difference is that for cars, the auto gas gauge is the source of inaccuracy while the gas tank capacity is constant; for battery applications, the EMU gas gauge is accurate but the battery capacity fluctuates. The capacity of a single battery varies significantly with the rate of discharge (see Figure 4) and the temperature at charge and discharge (see manufacturers' battery specifications). For specific conditions, the minimum capacity for a new battery is per the data sheet, but capacity variations across a battery population can be large.

Gas Gauge Registers

The gas gauge, gas gauge threshold, and the last capacity register pairs record capacity removed. They are used to monitor the remaining capacity of the secondary battery, as determined from discharge current.

The gas gauge is a 16-bit totalizer that maintains the total discharge from the battery through the sense resistor. The gas gauge rolls over and continues counting if the 16-bit capacity is exceeded. Rollover should be avoided, however, because with rollover, the gas gauge threshold and the last capacity values may be difficult or impossible to use. At the optimum sense resistor drop, 70 mV, the gas gauge rolls over after 20 hours. If the inputs to Equation 1 or 2 define the current drain profile, the maximum capacity measured without rollover is about $1.4/R_s$ amp-hours, where R_s is the sense resistor value in ohms.

Last Capacity Register Pair

The last capacity register pair contains the gas gauge value when the last EDCV threshold was reached. This value should be qualified by the battery replaced bit, BR (see the capacity reference management discussion below). When a battery is monitored from full charge to full discharge (final EDV), the value recorded in the last capacity register represents the measured capacity of that battery.

Gas Gauge Threshold Register Pair and GGN

The gas gauge threshold register pair provides the system with a convenient method of monitoring battery consumption. When the threshold is met or exceeded, an interrupt is generated and GGN is set.

Options include:

- Selection of a specific critical notification threshold.
- Interrupt-driven capacity monitoring. Each time the threshold is reached and GGN is set, the threshold is incremented by a fixed amount. This allows the processor to easily note the usage of fixed capacity amounts.

End-of-Discharge Voltage Status, EDV

The end-of-discharge voltage status bit, EDV, is a voltage monitor of the battery capacity. When this bit is 1, the per-cell voltage of the secondary battery is below the value in the EDCV register. When EDV becomes 1, the EMU generates an interrupt, and loads the last capacity register pair.

Figure 4 shows a typical discharge for a NiCd battery. The rapid decline of the voltage toward the end of discharge points out the critical nature of EDV. The system must be warned when the voltage drops into the discharge knee so that the user can take action. The value in EDCV determines the per cell voltage that activates EDV. "C" is the battery capacity, and is commonly used to express charge and discharge per-hour rates.

Typical final end-of-discharge voltages are:

- NiCd 0.9 to 1.0 volts/cell
- Lead-acid 1.6 to 1.8 volts/cell

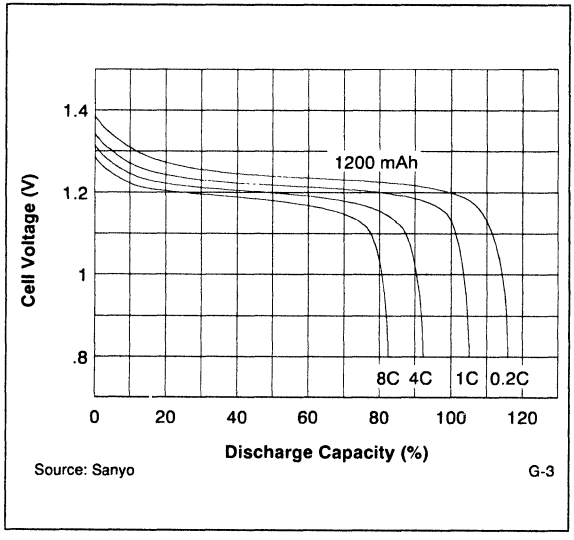


Figure 4. Cell Voltage Versus Capacity at Various Discharge Rates

- Nickel-metal hydride 0.9 to 1.0 volts/cell

The EDV threshold may be repeatedly adjusted during system operation to provide remaining capacity information. For example, a specific NiCd battery type may be characterized so that the user is provided one or more early warnings at reasonable times prior to the final, or forced reset, voltage. EDV may also be used to manage the capacity reference, as discussed below. The last capacity registers are rewritten after each EDV decision. The software may need to monitor the gas gauge capacity usage between EDV thresholds.

Before the system is shut down, the final EDCV should be programmed. This is required when the EMU is programmed for a DC-input-initiated charge action that includes a discharge phase.

Adjustments in discharge rate affect the battery voltage. After an EDCV threshold has been reached, a decrease or cutoff of the battery discharge may allow the voltage to recover to above the threshold. This should not typically impact decisions based on reaching this threshold. Appendix A describes factors affecting the secondary battery voltage.

Secondary Battery Faults

A secondary battery fault indicates that the battery is not capable of sustaining system operation. Such faults are monitored using the EDV threshold and the secondary battery fault bit, SBF.

EDV sensing may be used by appropriately programming EDCV and using EDV as a general-purpose voltage monitor.

EDV may be used to monitor for shorted cells and for voltage depression. A single shorted cell causes the battery voltage to drop by a one-cell increment. EDV may be used on power-up and power-down to verify battery voltage. If the battery voltage is one cell voltage or more below the final EDV threshold, charging may be disabled, and the user should be notified. If the battery voltage of a newly charged battery (GGNV=0, gas gauge=0) is one cell voltage or more below nominal, charging should be disabled, and the user should be notified.

Voltage depression, a NiCd phenomonen colloquially referred to as "memory effect," may cause an early EDV. Voltage depression is characterized by an early step down in voltage during discharge (see Figure 10). This voltage decrease may be misinterpreted as full discharge by the system. The tendency toward voltage depression varies with different batteries, but generally is caused by repeated shallow discharge/charge cycles. Conditioning (discussed in Appendix D) may restore the battery capacity. The system may consider it a probable voltage depression fault when the expected capacity is only partially consumed but the final EDV threshold is reached.

The secondary battery fault bit, SBF, may indicate an open or short within the secondary battery. SBF is set to 1 when the input to SB is less than 0.5 V per cell. The EMU prohibits charging, and the system should notify the user.

Capacity Reference Management

When using the gas gauge register information, the system must subtract the capacity used from an appropriate capacity reference. The base reference may be the measured capacity of the specific battery, a nominal battery capacity, or a user-defined capacity. The base reference may be adjusted to take into account self-discharge.

When the measured battery capacity is used, a reasonable guardband should be selected to account for the probability that the present charge/discharge cycle conditions differ from the conditions during the measurement cycle. The amount of guardband depends on the battery specifications, the previous and present system use conditions, and the precision and variety of the capacity reference adjustments to be undertaken (discussed below).

The base capacity reference in use, precisely measured capacities for one or more batteries, and capacity adjustments may be stored in the 32 nonvolatile general-purpose storage registers.

Secondary Battery Replaced (BR) and Gas Gauge Not Valid (GGNV) Interpretation

The system uses these two bits to decide on a base capacity reference, and possibly to implement parallel monitoring routines. See Table 2.

BR=1 indicates that the secondary battery may have been replaced. This may invalidate use of the value in the last capacity register pair as the basis of the capacity reference.

GGNV=1 indicates that the gas gauge value is not measured against a battery fully charged under EMU control.

Table 2. BR and GGNV Capacity Reference

BR	GGNV	Capacity Reference	EDV Early Warning
0	0	Last capacity register or previous capacity reference	Optional
1	0	Nominal capacity	Optional
X	1	User-selected or estimated using EDV	Recommended

In all cases, the system may select an EDCV that will provide the user with an early EDV warning well before the final EDV.

EDV may also be used within a parallel capacity monitoring routine, particularly for occasions when GGNV=1. The EDV threshold may be repeatedly reprogrammed to provide a best approximation of capacity monitoring. EDV capacity monitoring is most effective for batteries characterized by a sloping voltage profile during discharge, such as lead acid. This approach may still be of value for batteries such as NiCd, because it may be able to determine full charge. This is indicated by a rapid voltage drop to a stable voltage above EDV (see the early discharge voltage region curves in Figure 4).

EDV Capacity Monitoring Procedure

1. Increment EDCV by 10 mV.
2. Check EDV status. If 0, then go to 1.
3. Appropriately interpret and store the EDCV value and store the gas gauge value.
4. Decrement EDCV by 10 mV. If EDCV is less than or equal to the EDCV indicating low capacity, then go to 9.
5. Wait on EDV interrupt.
6. On EDV interrupt, interpret voltage.
7. Compare current gas gauge value to last recorded value.
8. Record difference; then go to step 3. For NiCd-like batteries, a difference smaller than a critical value may indicate discharge at the full charge or full discharge ends of the discharge curve.
9. Enter end-of-capacity EDV routine.

Capacity Reference Adjustment

Regardless of the base reference, the system may use a calculated capacity adjustment factor in addition to the actual measured discharge. Self-discharge, discharge rate, and temperature may all be significant factors.

For a NiCd battery, room temperature self-discharge is about 1% per day. When the battery has not been removed or charged, self-discharge is readily calculated by summing the periods of time the system is off and calculating the appropriate adjustment factor. One means to monitor system-off time is for the power-down routine to place a "time stamp" into the general-purpose nonvolatile registers, for later retrieval and comparison within the power-up routine.

For precise self-discharge estimates, the system may monitor the temperature during power-down periods, at very slight current drains. The designer should be aware that very slight current drains are more additive than

substitutive for the self-drain. The few electrode charge sites supporting the active load are not self-discharging, but the many electrode sites not being worked continue to self-discharge.

A second base reference adjustment to consider is the discharge rate. For example, a 0.2C NiCd discharge provides approximately 110% of the capacity of a 1C NiCd discharge. An application with discharge at a very fast rate has less available capacity than an application discharging at a much lower rate (see Figure 4). Rate of discharge may be readily monitored by adding a fixed increment to the gas gauge threshold following each GGN interrupt.

Two last considerations are the charge temperature and discharge temperature, which affect battery capacity in a moderately deterministic manner.

Capacity References for Multiple Batteries

Implementing some method of battery identification allows actual measured capacity to be used as the reference for more than the one battery discharged and charged within the system. The 32 general-purpose nonvolatile registers or other nonvolatile storage may be used to maintain precise capacity references for multiple batteries. Identification may be manual (user input) or automatic.

Automatic ID may be implemented similar to the DIN code on film. (Three electrical or optical contacts would allow management of eight unique batteries.) Resistive ID is another option.

The system could store the last measured capacity for each battery, as well as calculate a self-discharge decrement to be considered for application each time the battery is reinstalled but not recharged.

As an added benefit, such a battery ID system might also allow identification of battery type (manufacturer, nominal capacity, battery chemistry, etc.) to allow the system to adjust the EMU program as needed. Cycle history might also be maintained to determine conditioning requirements.

Battery Charging and Conditioning

Many methods are available for charging batteries (see Appendix B). The most common methods are passive and rely on battery manufacturers to build batteries that tolerate overcharging. These types of charging may have lower charger cost, but this small savings advantage must be considered along with the incompatibility of such chargers for fast charge, and with the excess overcharge leading to premature death of the rechargable battery.

Fast charging rates require an active charging method. When a battery is undergoing a fast charge, the early full-charge detection and charge current adjustment are required to prevent severe damage. The sensitivity of the full-charge detection is also critical because cumulative overcharging reduces the life of a battery.

Conditioning may be applied to a battery to recover from certain kinds of operational degradation, including the voltage depression effect.

The EMU provides the system designer with flexible and efficient methods allowing battery conditioning and fast charge control with minimal overcharge.

The EMU controls a constant current charger, and can be used to control the charging of any type of rechargeable battery, including NiCd, nickel-metal hydride, lead acid, and lithium. For some chemistries, the voltage must be limited to avoid permanent electrolyte disassociation.

Battery Charging Hardware Design

The hardware design should support all aspects of charging including non-operational discharge and trickle charge. The EMU charge action hardware consists of:

- Charging power supply
- Charge control FET
- Voltage doubler components
- Discharge FET

Charging Power Supply

The charging power supply provides the required current and voltage for battery charging. The EMU monitors the charging supply availability on the DC input pin. A valid DC input is from 4.5V to 18V. The supply must provide voltages within these limits and sufficient to charge the battery, while under the applicable loads.

Charge Control FET and Voltage Doubler

The charging control is provided by the charge control pin, CC. This pin is an open-drain output that provides the signal polarity to control an n-channel MOSFET. The gate voltage for the MOSFET can be provided by the EMU voltage doubler. This provides voltages of twice the DC input. The voltage doubler requires three external components—two diodes, and one capacitor with values similar to:

- Capacitor 1000pF, 50V
- Diodes 1N914

The CC pin is connected to the cathode end of the output diode as shown in Figure 1. The CC pin is also connected to the gate of the n-channel MOSFET used for charge control. Table 3 lists recommended MOSFETs.

The MOSFETs listed in Table 3 are all logic-level devices, requiring 5V gate-to-source to turn full on. The voltage doubler output provides the required gate-to-source voltage.

Table 3. Charge Control n-Channel MOSFET

Charge Current	Suggested Part Numbers
< 1 A	IRLD024
< 10 A	IRLR024, IRLU024
< 20 A	IRLZ34, IRLZ44

Discharge FET

The discharge FET is controlled by the discharge control pin, CD (see Figure 1). The CD pin is an open-drain output that is controlled by the EMU during programmed discharge and during the discharge interval of "burp" charging. The control polarity is correct for an n-channel MOSFET. The designer must provide the proper current-limiting device in the discharge path. The limiting device should be sized for continuos dissipation if EMU-controlled conditioning or capacity discharges are to be used.

Consideration should also be given to whether discharging occurs during system operation. If EMU-controlled discharge periods occur while the system is operational, the discharge current should be limited so as to not greatly alter the measured capacity. For NiCd batteries at discharge rates above 0.2C, the available capacity may decrease from 5 to 7 percent for every doubling of the discharge rate (see Figure 4).

Charge Termination on Full Charge

The EMU full-charge determination is on the first of: maximum elapsed time, maximum voltage per cell, or -ΔV determination. The system designer must define these limits. Appendix C provides additional information on full-charge determination.

Maximum Elapsed Time

The maximum time termination presumes the battery reaches full charge before the programmed maximum charge time expires. The maximum value for maximum charge time is 34 hours. The time covers charge rates down to 0.05C.

A reasonable maximum time should always be programmed, if only as a fail-safe measure.

A maximum time of 0 may be programmed to cause immediate entry into trickle charge mode.

Maximum Voltage Termination

The maximum voltage per cell termination is based on the average voltage per cell from the SB input voltage and the number of cells indicated in CSR1. The maximum value for the maximum voltage per cell is 2.55V, and the minimum value must be above 0.5V. Per-cell values below 0.5V do not allow a charge action to start.

A reasonable maximum voltage should always be programmed, if only as a fail-safe measure.

A reasonable maximum voltage is also important in applications where multiple batteries are to be charged with the system off, with the continous presence of charging current. If a battery is removed, the charging supply open circuit voltage should exceed the maximum voltage, ensuring charge action termination. Charge termination due to full charge of the battery in the system or due to reaching maximum voltage after the battery is removed resets the charge action state. When the battery is replaced, the charge action initiates as programmed (and BR and GGNV are set to 1).

-ΔV Termination

The secondary battery voltage at SB is used to determine -ΔV. The -ΔV termination occurs when three consecutive voltage samples indicate decreasing battery voltage.

The system designer should consider the noise level at SB. The -ΔV termination is sensitive to noise, as is any other differentiating method.

A suitable RC filter can be used on the SB input pin. The SB input impedance is 500K ohms. A RC filter with a 1K ohm input resistor and a 10 μF capacitor should be adequate for most noise problems. If very low-frequency (< 1 Hz) noise is a problem, however, the system may require other changes.

Battery Charging Software Design

The EMU provides very flexible charging and conditioning ability. The system programs the EMU to provide the desired charging and conditioning routine. System control allows an adaptive approach to battery management.

Charge Action Selection

A charge action consists of an optional discharge phase followed by a charge phase. The EMU must be programmed to perform charging and conditioning. The initial defaults prevent charge or discharge. Program-

ming the EMU control registers is described in the microprocessor software design section.

Discharge Method

The EMU discharge phase provides three different services:

- Battery conditioning (see Appendix D)
- Battery capacity determination (described previously)
- Depolarization (see Appendices A and B)

The conditioning and capacity services take place as the discharge phase of a charge action, which precedes the actual charge phase. The discharge phase is not performed if GGNV is set to 1.

The depolarization discharge occurs within the charge phase to improve charge efficiency.

A battery conditioning discharge procedure may be programmed by:

1. Writing the EMU discharge method field in CSR1 to 01.
2. Writing the gas gauge threshold value above the gas gauge value.

   Recent depth-of-discharge-before-recharge values for the battery should be considered. If the depths are shallow and repetitive, then the gas gauge threshold value should be written to a value above the recent discharge gas gauge values.
3. If the system is operational during this discharge, the GGN interrupt may require special service.

This method starts each charge action with a discharge phase if the gas gauge threshold value is above the current gas gauge value and GGNV is 0. This discharge method discharges the battery to the gas gauge threshold value or to the end-of-discharge voltage, whichever comes first. This discharge method saves time compared to doing a full discharge and can prevent voltage depression effects, or moves the effects out of the recent operating range of the battery.

A capacity discharge or deep discharge conditioning may be programmed by:

1. Writing the EMU discharge method field in CSR1 to 10.
2. Writing the gas gauge threshold value below the gas gauge value.
3. Writing the final EDCV value.

The battery capacity determination discharge brings the battery to full discharge. Each charge action begins with a full discharge if the gas gauge value is greater than the gas gauge threshold value and GGNV is 0. This discharge method discharges the battery to the end-of-discharge voltage. The termination of this discharge updates the last capacity register pair. With the appropriate gas gauge threshold, this discharge method provides a convienent measure of capacity by discharging only when the battery is near the capacity limit.

A forced full discharge can be obtained using the first method with a very high gas gauge threshold, or by using the second method with a threshold below the current value. In either case, the last capacity register is written when the final EDV threshold is reached.

Charge Method

The EMU provides three different charge current modulation methods:

- Continous charge
- Pulsed charge
- "Burp" charge

These methods are programmed by writing the charge and discharge period registers to the appropriate value. The principles behind these methods are discussed in Appendix B. Charging is only available when DC valid, DCV, in register SR is 1 and charge action enable in register CSR1 is written to 1.

DC-Initiated Charging

DC-initiated charging occurs when the power switch state bit, PS, in register SR is 0 and DCV becomes 1. The charging is performed as previously programmed. The important parameters for DC initiated charging are:

1. Charge action enable written to 1 in CSR1.
2. -ΔV enable written to 1 in CSR2.
3. -ΔV sample time is selected in CSR2:

   The -ΔV sample time choice should be based on charge rate. For high rates, use 8-second sample times. The sample time chosen should allow detection of a 10 mV per cell drop after full charge has occurred.
4. Maximum cell voltage written to maximum cell voltage register, MCV.
5. Maximum charge time written to maximum charge time register, MCT.
6. Charge period written to CPR.
7. Discharge period written to DPR.

8. Discharge method chosen in CSR1:

   Final end-of-discharge voltage written to EDCV.

   Appropriate gas gauge threshold value written to GGTH and GGTL.

9. Trickle charge enable set in register CSR2:

   Appropriate trickle charge period written to TPR.

The DC-initiated charge action terminates on any of the following:

- DCV in SR becomes 0; terminates with GGNV set to 1.
- BR in SR becomes 1; terminates with GGNV set to 1.
- SBF in SR becomes 1; terminates with GGNV set to 1.
- PS in SR becomes 1; terminates with GGNV set to 1.
- Charge time exceeds MCT value; terminates with GGNV set to 0 and begins trickle charge if enabled.
- SB voltage input exceeds MCV value; terminates with GGNV set to 0 and begins trickle charge if enabled.
- -ΔV condition determined; terminates with GGNV set to 0 and begins trickle charge if enabled.

Command-Initiated Charging

The command-initiated charging allows the system to set the charge action parameters so as not to interfere with normal system operation.

The system operation may cause charging current fluctuations. If this happens, the -ΔV condition may be satisfied erroneously. To prevent false full-charge determinations, the -ΔV test should be disabled during the transitions in charging current by clearing the -ΔV enable bit to 0. The system should reenable -ΔV determination as soon as the charging current becomes stable.

Another consideration is that a faster discharge occurs when the system is operating under battery power and the discharge control is simultaneously actuated (see the Discharge FET section above). This impacts available capacity.

The initialization for command-initiated charging is similar to the DC-initiated charging (described in the previous section). The exceptions are:

- A charge action command is required before any charge action can begin. A commanded charge action begins when DCV is 1.
- The charge action command is ignored if PS is 0.

The termination of a command-initiated charge action is similar to DC-initiated charging termination except the charge action can also be terminated by the abort command.

System Software Strategy

The EMU contains data RAM for use in managing the secondary battery system. This RAM is meant to provide nonvolatile storage for battery reference data.

On system startup, the operating system should check the status of the current secondary battery. The following is an outline of one system startup strategy:

1. Read SR from the EMU.
2. Retain the status of EDV and GGN.
3. If PS is 0, then toggle power switch input (low then high).
4. If GGNV is 0, then go to 5; else:
   a. Enter capacity reference determination routine.
   b. If BR is 1, then reset with an abort charge command.
   c. Issue charge command. This might require reduced current selection using an optional EMU output.
   d. Go to 7.
5. If BR is 0, then go to 6; else:
   a. Enter capacity reference determination routine.
   b. Reset BR to 0 with an abort charge command.
   c. If charging is desired, issue charge command and go to 7. Otherwise go to 8.
6. If the last capacity register value has not changed, then use prior capacity reference:
   a. Use time stamp to estimate self-discharge.
   b. If gas gauge is below the shallow discharge threshold for this battery (25 percent of capacity), then go to 9.
   c. Issue charge command. This might require reduced current selection using an optional EMU output.
7. Set system to monitor charging activity.

a. If the charging current is to vary with system activity, then write -ΔV enable to 0 during charging current transitions.

b. During the charging phase of a charge action, the end-of-discharge cell voltage can be set to provide interrupt notification of low voltage during charging; i.e., DC unavailable or fallen low (perhaps due to excessive system load).

8. Save the current charge history.

9. Monitor gas gauge using threshold notification.

10. Monitor end-of-discharge cell voltage.

11. Monitor power switch input, if used.

System shutdown should set the EMU to the desired unattended charging method. A suggested shutdown outline is:

1. Store the following information in EMU data storage:

   Last capacity value.

   Gas gauge and time stamp value.

   Cycle life count.

2. If CHG is 1, then issue an abort charge command.

3. Configure EMU charging action by:

   a. Writing discharge mode.

   b. Writing EDCV value.

   c. Writing gas gauge threshold value.

   d. Writing maximum cell voltage value.

   e. Writing maximum charge time value.

   f. Writing -ΔV enable to 1.

   g. Writing GGNV-qualified charge bit (if desired).

4. Issue system power-off command.

After the system power-off command is issued, the EMU enters the system-off state. This is indicated by PS set to 0. At this time, DCV = 1 initiates a charge.

Backup Supply Management

The EMU requires a backup cell when the secondary battery becomes unavailable. If the backup cell is not available, then nonvolatile memory and programmed settings are lost. The EMU also provides a backup cell output regulated down from the secondary battery. See Figure 5.

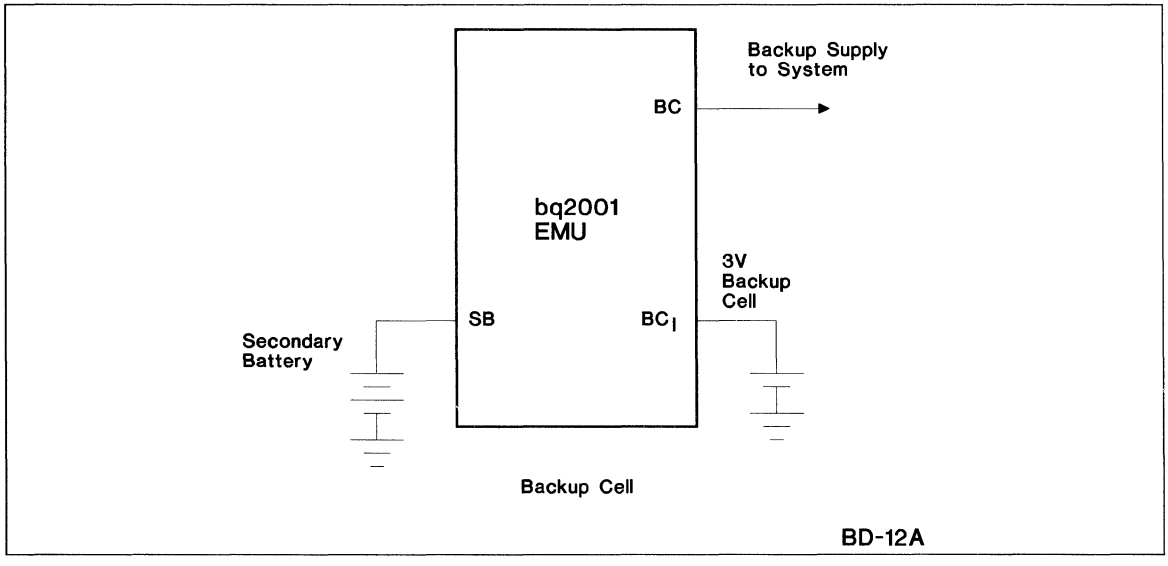


Figure 5. Backup Supply

Backup Supply Management Hardware Design

The backup supply hardware design centers arround proper choice of the backup cell or battery. The backup cell supply output is on the BC pin. The maximum BC output current is 1 mA for 3 V. The designer should limit the typical BC output current to values that will not overdischarge the secondary battery. The system should supply at least a 100K ohm load on the BC output. The maximum capacitance on the BC pin should not exceed 1 μF.

The backup cell is connected to BC_I input. The backup cell must provide at least 2.0V.

The cell capacity requirements are set by the system considerations:

- Total 3V backup load (EMU, RTC, configuration RAM, etc.)
- Time where the secondary battery can not provide the system backup, i.e., during removal or depletion.

The designer should be aware that the switch-over from the secondary battery to the backup cell input occurs when the secondary battery regulated output drops below the backup cell input. The secondary battery may be brought to very deep discharge if the secondary battery is allowed to provide significant system backup power over a very long period. The typical 3V backup load should be extremely small—only a fraction of the battery self-discharge.

Backup Supply Management Software Design

The backup cell software issues concern the backup cell low, BCL, status bit. This status bit is set to 1 when BC_I is below 2.1V typical . This diagnostic should be reported to the user so that the backup cell can be serviced.

Resource Management

The EMU provides the system with a variety of resource management options. The system designer may choose to use these options as best fits the system.

Resource Management Hardware Design

System Power Control

System power control is provided by the $\overline{PS}$ input and $\overline{PSC}$ output. The $\overline{PS}$ input is pulled to V_{BC} by 100K ohms. The EMU power control is activated when the $\overline{PS}$ input is brought to Vss. This action causes the EMU to:

1. If PS is 0:
   a. Set $\overline{PSC}$ to 1.
   b. Activate the $\overline{PSC}$ output.
   b. Discontinue charge action.
   d. Activate $\overline{INT}$.
   e. Set INTF to 1.
2. If PS is 1:
   a. Activate $\overline{INT}$.
   b. Set INTF to 1.

The designer may use the $\overline{PSC}$ output to enable the system power supply. The $\overline{PSC}$ output may also operate an LED for system power indication. The $\overline{PSC}$ output remains active while PS in SR is 1.

Annunciators

The designer may configure the EMU to output the state of certain status bits. These outputs provide indicators and/or annunciators without system supervision. The available status bits are:

- CHG
- EDV
- BCL
- DCV
- GGN
- SBF

Each of the status bits can control an open-drain output.

Subsystem Control

The designer may choose host control of the EMU outputs. There are seven configurable open-drain outputs, including six selectable between host control or status bit control.

Resource Management Software Design

The software design issues for resource management include system-on and system-off operation. During the system-off operation, the EMU status bits control those outputs configured for such control, while the system-controlled outputs remain in their last programmed state. During system-on operation, all outputs may be actively controlled by the system.

System Power Control

The system power control software should respond to either a power-on or power-off request. If the EMU is providing the power switching function, the system need only to respond to the power-off request. With EMU power control, the system must issue a power off command to instruct the EMU to power the system down. The system response is discussed in the battery charging, system software strategy section.

Even if the $\overline{PSC}$ output is not used, the PS bit should be controlled to reflect system power. If PS is 1, the EMU charging action must be commanded by the system. If PS is 0, any programmed charge action is initiated by valid DC.

EMU Status Annunciators

The EMU can support the six status bits listed above as outputs. The state of these outputs are indicated in SR. The system enables the status bit control of its output through the mask register, MR. Writing a 1 to a MR bit selects status bit control of a particular open-drain output. If an output is under status bit control, the output is controlled regardless of the system power state.

System-Controlled Outputs

System control of an output is selected by writing its bit in MR to 0. This action places an open-drain output under the control of the output control register, OCR. The system may set the bits in OCR to control certain subsystems (i.e., fixed disk, floppy disk, back-lighting) or to control an annunciator (LED). As the system controls the operation of subsystems to minimize battery consumption, the effect of changing available charge current should be considered, as discussed in the command-initiated charging section.

The system software should set the OCR bits to the proper power-down state before issuing the power-down command. If system power is off, the EMU maintains the OCR-controlled outputs in their last programmed state. If system power is on, the system may continue to control the outputs (independent of the PS bit status).

Appendix A Characteristics Impacting Secondary Battery Voltage Measurement

Cell voltage is affected by discharge rate, capacity reduction, and temperature. Although this discussion refers to NiCd, this can be generally applied to other chemistries with similar characteristics.

The discharge rate affect on a NiCd cell is shown in Figure 4. The separations of the discharge curves are caused by the internal resistance of the cell.

The internal resistance is itself a function of the discharge current. Figure 6 shows the equivalent circuit of a cell. The R_O in this circuit is a function of the cell geometry, including effective electrode area and electrode separation. R_O is also a function of the electrolyte conductivity, which depends on ion concentration and temperature.

The R_P in Figure 6 is a complex function of discharge rate. The higher the discharge rate, the greater the R_P. R_P is the resistance due to polarization at the electrodes. Polarization is a state where the ion concentration within a battery varies across the plate separation. This polarization is shown in Figure 4 by comparing the voltage separation between the initial 1C and 4C rates and to the 4C and 8C separation. Figure 4 shows that the voltage difference for a factor of 4 change in rate at the lower discharge rates is about equal to the voltage difference for a factor 2 change in rate at the higher rates.

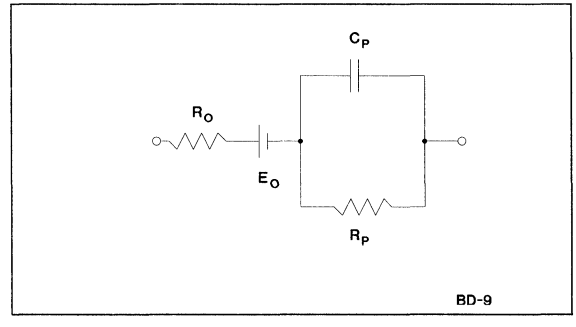


Figure 6. Battery Equivalent Circuit

The C_P is the capacitance associated with polarization. This term becomes important if the discharge is a pulse. In a pulse discharge, C_P provides an effective reduction in the impedance due to polarization.

Figure 7 shows the change in internal resistance as a function of spent capacity for two different NiCd cells. The internal resistance of NiCd cells is low, about 10 to 20 milli-ohms, and fairly flat over a good range of spent capacity. For lead-acid batteries, the electrolyte participates actively in the discharge reaction, so the internal resistance has a much larger change with spent capacity.

The capacity-reduction effect is due to the change in concentration/activity of the various ions within the electrolyte as the cell is discharged. During the discharge of a cell, ion activity changes. This effect reduces the open-circuit voltage during discharge, for a NiCd typically by 100 to 200 mV (see Figure 4).

Figure 8 shows the operating temperature effect on internal resistance. These curves are typical for the operative range of NiCd cells.

Temperature effects on battery voltage are documented by the battery manufacturers. Within the specified battery operation temperature range, the open-circuit voltage increases with temperature.

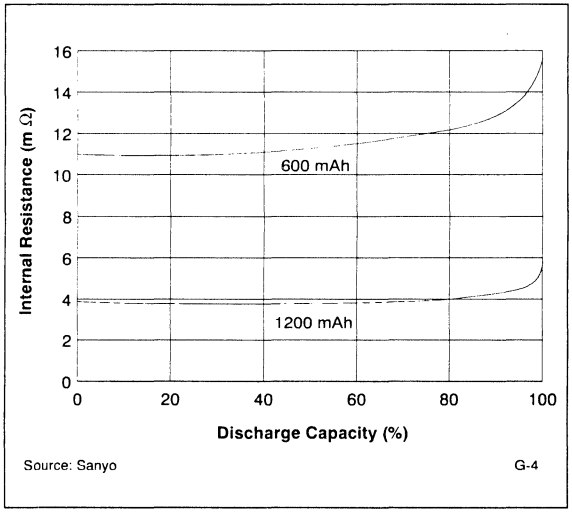


Figure 7. NiCd Internal Resistance Versus Discharge Capacity

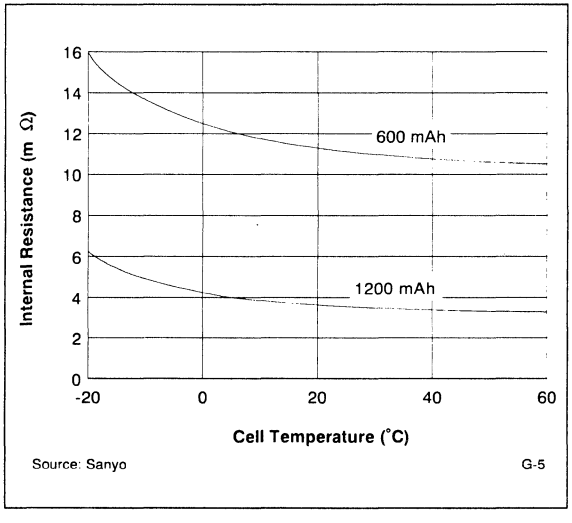


Figure 8. NiCd Internal Resistance Versus Cell Temperature

Appendix B
Battery Charging Methods

Two basic supply types are used in chargers:

- Constant current
- Constant potential

The actual charge provided to the battery is a modulation of the outputs from these supplies.

Constant Current

Constant current charging can be performed on any rechargeable battery, but requires an appropriate maximum voltage limit for those batteries where voltages above a certain level cause permanent disassociation of the electrolyte, i.e., some rechargeable lithium batteries. The constant current supply maintains the charge to the battery within a finite voltage range. Constant current charging provides an efficient method because the charge rate does not change due to the changes in internal resistance or open cell voltage of the battery.

Constant current charging methods require either a battery designed for continous charging or a feedback mechanism to determine the full-charge condition. For example, standard sealed NiCd cells may be charged continuously at rates of 0.05C to 0.1C, and quick-charge batteries can handle rates of 0.2C to 0.33C. Fast-charge batteries under feedback control may be charged at rates up to 4C.

Constant current charging does not have to be continous over the charging period. Pulse charging may provide high charging efficiencies. Pulse charging provides a period of high rate followed by a period of no current. The current duty cycle can be modulated so that the average charge rate does not exceed that allowable for a particular battery. During the no-current period, the battery recovers from the polarization due to high current. The pulse charge efficiency is achieved from the higher charge rate voltage and the reduction in polarization.

"Burp" charging is an extension beyond pulse charging. This method uses a short period of discharge between charge pulses to aid in depolarization. This reduction in polarization improves the charging efficiency, and is used in very sophisticated battery maintenance chargers. There are claims that "burp" charging can rehabilitate degraded cells.

Constant current charging may be done at a low level, C/20 to C/30. This type of charging, often called trickle charging, is used to maintain charge by replacing the capacity lost due to self-discharge.

Pulse trickle charging is another option to replenish self-discharge. Continuous trickle charging at low current tends to work the most accessible charge sites continuously. Pulse trickle charging with a periodic full current efficiently exercises most of the charge sites and allows a depolarization period in between.

Constant Potential

Constant potential (voltage regulated) charging is used primarily on systems where the battery is vented or when voltage above a certain level causes permanent disassociation of the electrolyte, i.e., some rechargeable lithium batteries. The regulated voltage charger provides a constant potential to a battery and is current-limited. When applicable, the constant voltage charger provides a rapid charge in the early times. As the charging progresses and the battery potential comes closer to the charging potential, the rate of charge diminishes.

The system designer has two primary input decisions when designing a constant potential charger: the charging voltage and the current limit. The higher voltage should be accompanied with a higher current limit. The values of these two parameters determines the time that the battery system charges at constant current. Initially, due to the current limit and the voltage applied, the battery is charged at the current limit. As the battery voltage gets close to the charging potential, the charging current decreases. The final current is determined by the internal resistance and the open cell voltage of the battery. This current is the maintenance charge or trickle charge level for the battery.

Using higher charging voltages results in a higher maintenance current. This may reduce the life of the battery. Due to decay in charging current toward the end of charging, series cell batteries may experience loss of capacity unless the charge time is extended. Vented batteries typically have a greater increase in internal resistance at full charge compared to sealed batteries. This increased internal resistance reduces the trickle current under constant potential charging.

Constant potential charging is not recommended for sealed NiCd or nickel-metal hydride. These batteries are designed to minimize polarization and consume the oxygen produced during over charging. This results in smaller increase in battery internal resistance during charging as compared to the vented cells. Therefore the constant potential maintenance charge may be too large and may result in damage to the battery.

Appendix C
Charge Termination

Full battery charge may be determined by several methods.

- Time
- Battery temperature
- Delta temperature, ΔT
- Battery voltage
- Negative delta voltage, -ΔV

Time Termination

Time termination may be applied to constant potential or constant current charging. Time should not be used as the only termination control when charging at high rates. Such control results in overcharging of a partially discharged battery. Time may, however, provide a fail-safe mechanism when using other charge-termination methods.

Temperature Termination

Battery temperature may be used to terminate constant potential or constant current charging. The battery temperature increases due to the energy conversion by the internal resistance of the battery. Other controlling factors are:

- Temperature dissipation ability of the battery
- Ambient temperature
- Thermal conductivity of the battery
- Thermal mass of the battery

When the temperature is measured on the outside of the battery, the lag due to the above list can result in overcharging. A temperature that ensures full charge will always involve some overcharge. Also, charging cold or hot batteries can result, respectively, in either overcharging or terminating before full charge. The ambient temperature presents a similar problem.

Delta Temperature

The delta temperature method, ΔT, is similar to the temperature cutoff method described above except that the ambient temperature effect is removed. This method uses the change in battery temperature to determine full charge. The ΔT method requires two temperature sensors, one for the battery and one for the ambient condition. When the difference between these temperatures reaches a predetermined value (typically 10°C), the charging is terminated.

The drawbacks of this approach are:

- The continuing overcharge while the temperature increase conducts to the sensor.
- The overcharge or undercharge error that may result if the base battery temperature is below or above the ambient temperature.

Voltage Termination

The battery voltage termination method can be used only with constant current charging. The voltage across a battery is determined by the open-circuit battery voltage and the voltage drop due to the charging current through the internal resistance of the battery (see Figure 6). The open-circuit battery voltage increases during charging due to the change in activity of the electrolyte ions.

The internal resistance of the battery changes due to polarization, ion concentration, and temperature of the electrolyte. As polarization increases, the internal resistance increases. Under constant current charging, as the internal resistance increases so does the voltage across the battery.

The voltage termination method depends on the ability to choose a termination voltage that will be achieved after the battery has become fully charged. This choice is difficult to make considering the parameters that influence the battery charging voltage. If a voltage is chosen such that full charge is not reached, the battery looses capacity. If full charge is exceeded, overcharging occurs. Maximum battery charging voltage may, however, provide a good fail-safe termination.

Negative Delta Voltage

The -ΔV method is applicable only to constant current charging. This method is equivalent to the ΔT approach, taking advantage of cell heating at full charge. The -ΔV method has the benefits of faster response (no heat conduction to a sensor) and no need for comparison to a reference. Where the voltage termination method depends on the voltage increase during charging, the -ΔV method uses the voltage decrease immediately after full charge.

As the battery becomes fully charged, more and more energy is dissipated by the battery's internal resistance, even as the voltage continues to rise. This energy raises the temperature of the battery. As the temperature increases, the internal resistance decreases. Immediately after full charge, this temperature effect overcomes the polarization effect, and the constant current charging voltage decreases (see Figure 9). The -ΔV method uses this phenomena to determine full charge.

This method uses the temperature effect on the conductivity of the electrolyte to predict end of charge. Therefore, this method is similar to the ΔT method but reacts to the *internal* temperature of the batteries, providing faster response and not requiring the addition of precision temperature-sensing devices.

The key difficulty of the -ΔV method is the risk of false full-charge determination due to a voltage drop unrelated to full charge. This is a significant issue with charging during system operation if the charging current fluctuates with subsystem activity. In such cases, -ΔV observations coincident with charging current decreases should be ignored.

Appendix D
Battery Conditioning

The conditioning of rechargeable batteries is a corrective action meant to restore the full-charge capacity of the battery.

A NiCd battery may exhibit a phenomena called "voltage depression." Voltage depression is a reduction in available voltage from the battery (see Figure 10). Voltage depression, sometimes referred to as "memory effect," may cause a false end-of-discharge voltage (EDV) determination. A significant charge may remain, but at too low a voltage.

Continuous trickle charging above the maintenance level for prolonged periods leads to overcharging and possibly voltage depression. High temperatures magnify this problem.

Repetitive charge and shallow discharge cycles also lead to voltage depression. These cycles expose the non-discharged electrode materials to repeated overcharge.

Conditioning may be done by one or more full discharge and charge cycles. This action recovers the lost energy capacity. Periodically choosing an EDCV below the usual operating EDCV removes the voltage depression that develops near the usual operating EDCV. Implementing a "burp" charge pattern may also result in recovery from voltage depression.

Lead-acid batteries that are allowed to have the open-circuit voltage drop below 1.98V undergo sulfation. Sulfation greatly increases the internal resistance of the battery. If the open-circuit voltage does not go below 1.8V, this sulfation may be reversed by charging the battery at constant current, 0.05C, with an increased maximum voltage limit. This breaks down the lead sulfate crystals and returns the battery to normal internal resistance.

References:

1. Gates Energy Products, Inc., Sealed Rechargeable Batteries Application Manual.
2. Sanyo Electric Co., Ltd., CADNICA® Sealed Type Nickel-Cadmium Batteries Engineering Handbook, SF-6336.

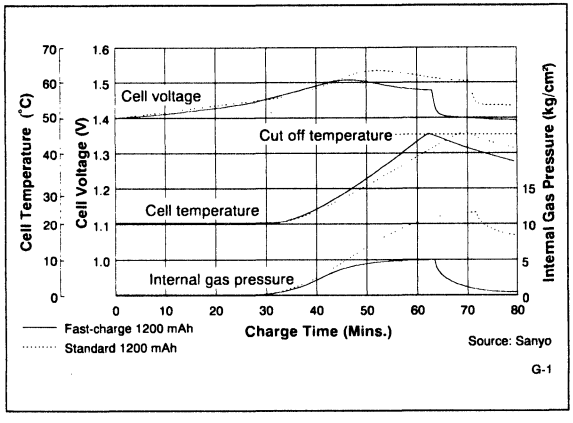


Figure 9. Rapid Charge Characteristics

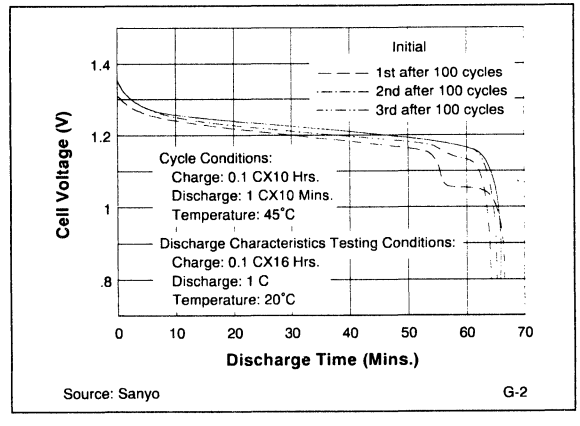


Figure 10. Voltage Depression

BENCHMARQ

bq2201

SRAM Nonvolatile Controller Unit

Features

- Power monitoring and switching for 3 volt battery-backup applications
- Write-protect control
- 3 volt primary cell inputs
- Less than 10 ns chip enable propagation delay
- 5% or 10% supply operation
- 8-pin plastic DIP or SOIC

General Description

The CMOS bq2201 SRAM Nonvolatile Controller Unit provides all necessary functions for converting a standard CMOS SRAM into nonvolatile read/write memory.

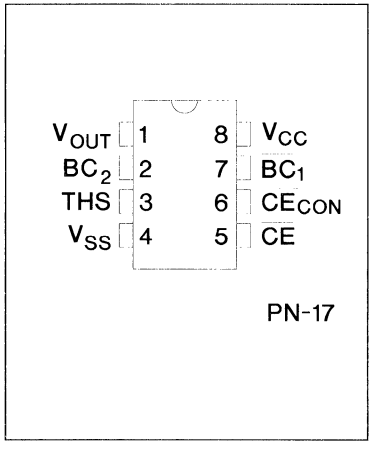
A precision comparator monitors the 5V V_{CC} input for an out-of-tolerance condition. When out of tolerance is detected, a conditioned chip enable output is forced inactive to write-protect any standard CMOS SRAM.

During a power failure, the external SRAM is switched from the V_{CC} supply to one of two 3V backup supplies. On a subsequent power-up, the SRAM is write-protected until a power-valid condition exists.

The bq2201 is footprint- and timing-compatible with industry standards with the added benefit of a chip enable propagation delay of less than 10 ns.

4

Pin Connections



Pin Names

V_{OUT}	Supply output
BC_1–BC_2	3 volt primary backup cell inputs
THS	Threshold select input
$\overline{CE}$	Chip enable active low input
$\overline{CE}_{CON}$	Conditioned chip enable output
V_{CC}	+5 volt supply input
V_{SS}	Ground

Functional Description

An external CMOS static RAM can be battery-backed using the Vout and the conditioned chip enable output pin from the bq2201. As V_{CC} slews down during a power failure, the conditioned chip enable output $\overline{CE}_{CON}$ is forced inactive independent of the chip enable input $\overline{CE}$.

This activity unconditionally write-protects external SRAM as V_{CC} falls to an out-of-tolerance threshold V_{PFD}. V_{PFD} is selected by the threshold select input pin, THS.

If THS is tied to V_{SS}, power-fail detection occurs at 4.62V typical for 5% supply operation. If THS is tied to V_{OUT}, power-fail detection occurs at 4.37V typical for 10% supply operation. The THS pin must be tied to V_{SS} or V_{OUT} for proper operation.

If a memory access is in process during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT}, the $\overline{CE}_{CON}$ output is unconditionally driven high, write-protecting the memory.

As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to one of the two external backup energy sources. $\overline{CE}_{CON}$ is held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the V_{CC} supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. The $\overline{CE}_{CON}$ output is held inactive for time t_{CER} (120 ms maximum) after the supply has reached V_{PFD}, independent of the $\overline{CE}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}$ input is fed through to the $\overline{CE}_{CON}$ output with a propagation delay of less than 10 ns. Nonvolatility is achieved by hardware hookup as shown in Figure 1.

Energy Cell Inputs—BC_1, BC_2

Two primary backup energy source inputs are provided on the bq2201. The BC_1 and BC_2 inputs accept a 3V primary battery, typically some type of lithium chemistry. If no primary cell is to be used on either BC_1 or BC_2, the unused input should be tied to Vss.

If both inputs are used, during power failure the V_{OUT} output is fed only by BC_1 as long as it is greater than 2.5V. If the voltage at BC_1 falls below 2.5V, an internal isolation switch automatically switches V_{OUT} from BC_1 to BC_2.

To prevent battery drain when there is no valid data to retain, V_{OUT} is internally isolated from BC_1 and BC_2 by either:

- Initial connection of a battery to BC_1 or BC_2, or
- Presentation of an isolation signal on $\overline{CE}$.

A valid isolation signal requires $\overline{CE}$ low as V_{CC} crosses both V_{PFD} and V_{SO} during a power-down. Between these two points in time, $\overline{CE}$ must be brought to (0.48 to 0.52)* V_{CC} and held for at least 700ns. The isolation signal is invalid if $\overline{CE}$ exceeds 0.54*V_{CC} at any point between V_{CC} crossing V_{PFD} and V_{SO}. See Figure 2.

The appropriate battery is connected to V_{OUT} immediately on subsequent application and removal of V_{CC}.

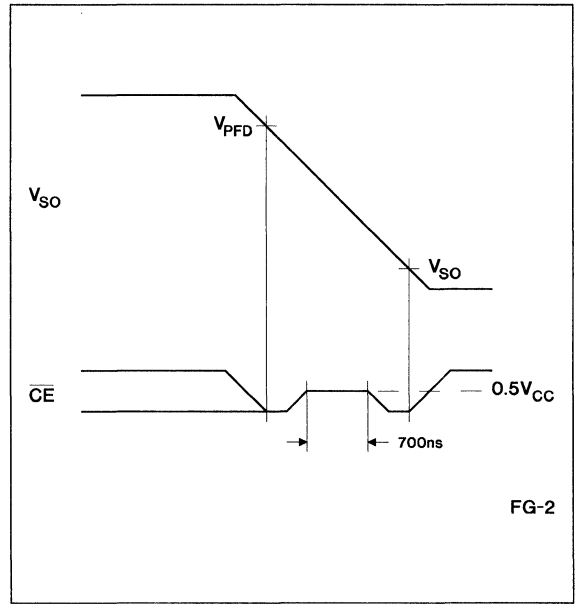


Figure 2. Battery Isolation Signal

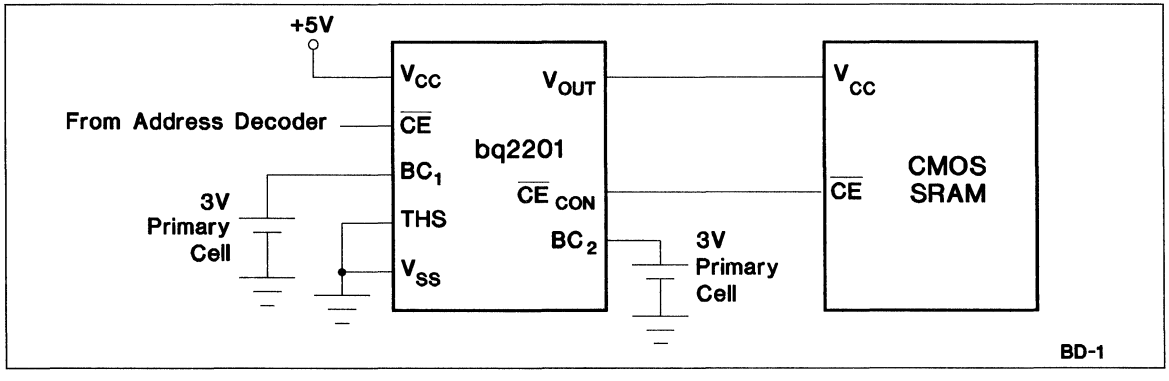


Figure 1. Hardware Hookup (5% Supply Operation)

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to 70	°C	
T_{STG}	Storage temperature	-55 to 125	°C	
T_{BIAS}	Temperature under bias	-10 to 85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds
I_{OUT}	V_{OUT} current	200	mA	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.75	5.0	5.5	V	THS = V_{SS}
		4.50	5.0	5.5	V	THS = V_{OUT}
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	
V_{BC1}, V_{BC2}	Backup cell voltage	2.0	-	4.0	V	
THS	Threshold select	-0.3	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

DC Electrical Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -2.0 mA
V_{OHB}	V_{OH}, BC supply	V_{BC} - 0.3	-	-	V	$V_{BC} > V_{CC}$, I_{OH} = -10µA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current	-	3	5	mA	No load on V_{OUT} and $\overline{CE}_{CON}$.
V_{PFD}	Power-fail detect voltage	4.55	4.62	4.75	V	THS = V_{SS}
		4.30	4.37	4.50	V	THS = V_{OUT}
V_{SO}	Supply switch-over voltage	-	V_{BC}	-	V	
I_{CCDR}	Data-retention mode current	-	-	100	nA	V_{OUT} data-retention current to additional memory not included.
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.2	-	-	V	$V_{CC} > V_{BC}$, I_{OUT} = 100mA
		V_{CC} - 0.3	-	-	V	$V_{CC} > V_{BC}$, I_{OUT} = 150mA
V_{OUT2}	V_{OUT} voltage	V_{BC} - 0.3	-	-	V	$V_{CC} < V_{BC}$, I_{OUT} = 100µA
V_{BC}	Active backup cell voltage	-	V_{BC2}	-	V	$V_{BC1} < 2.5V$
		-	V_{BC1}	-	V	$V_{BC1} > 2.5V$
I_{OUT1}	V_{OUT} current	-	-	160	mA	$V_{OUT} > V_{CC}$ - 0.3V
I_{OUT2}	V_{OUT} current	-	100	-	µA	$V_{OUT} > V_{BC}$ - 0.2V

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
C_{IN}	Input capacitance	-	-	8	pF	Input voltage = 0V
C_{OUT}	Output capacitance	-	-	10	pF	Output voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 V to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figure 3

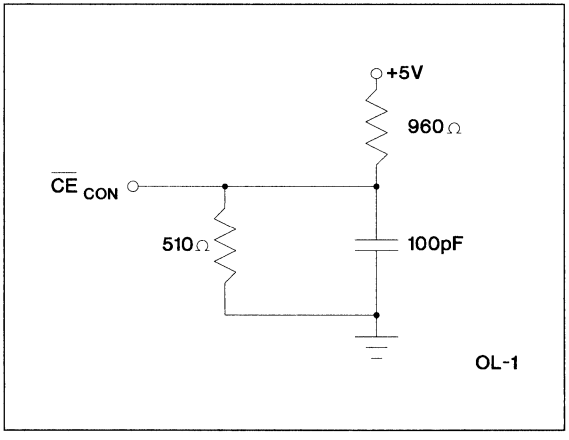


Figure 3. Output Load

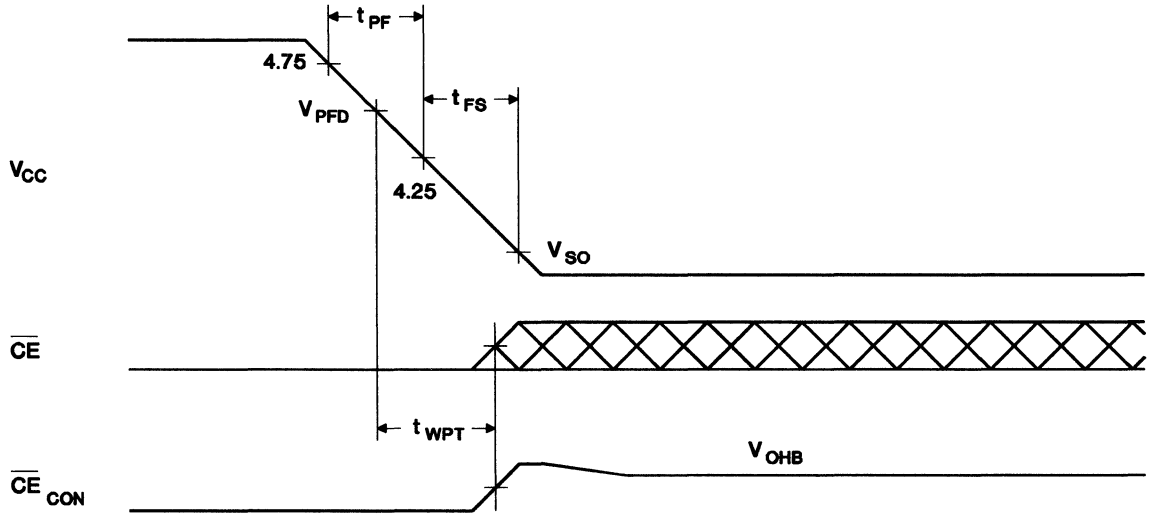
Power-Fail Control (TA = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{PF}	V_{CC} slew, 4.75V to 4.25V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25V to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, 4.25V to 4.75V	0	-	-	µs	
t_{CED}	Chip enable propagation delay	-	7	10	ns	
t_{CER}	Chip enable recovery	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Note: Typical values indicate operation at T_A = 25°C.

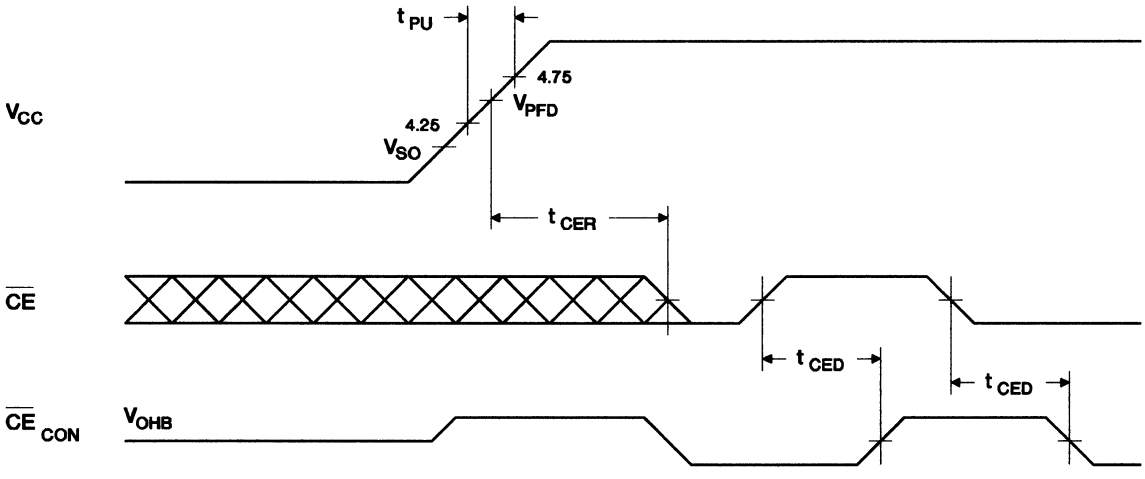
Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

Power-Down Timing



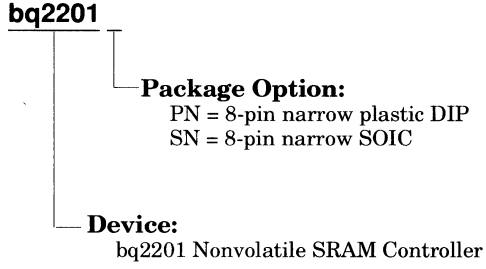
PD-1

Power-Up Timing



PU-1

Ordering Information



BENCHMARQ

bq2204

X4 SRAM Nonvolatile Controller Unit

Features

- Power monitoring and switching for 3 volt battery-backup applications
- Write-protect control
- 2-input decoder allows control for up to 4 banks of SRAM
- 3 volt primary cell inputs
- Less than 10 ns chip enable propagation delay
- 5% or 10% supply operation
- 16-pin plastic DIP or SOIC

General Description

The CMOS bq2204 SRAM Nonvolatile Controller Unit provides all necessary functions for converting up to four banks of standard CMOS SRAM into nonvolatile read/write memory.

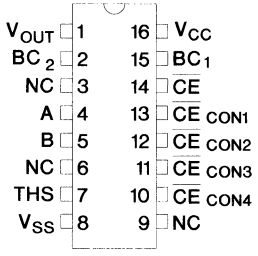
A precision comparator monitors the 5V V_{CC} input for an out-of-tolerance condition. When out of tolerance is detected, the four conditioned chip enable outputs are forced inactive to write-protect up to four banks of SRAM.

During a power failure, the external SRAMs are switched from the V_{CC} supply to one of two 3V backup supplies. On a subsequent power-up, the SRAMs are write-protected until a power-valid condition exists.

During power-valid operation, a two-input decoder transparently selects one of up to four banks of SRAM.

4

Pin Connections



PN-18

Pin Names

V_{OUT}	Supply output
BC_1–BC_2	3 volt primary backup cell inputs
THS	Threshold select input
$\overline{CE}$	Chip enable active low input
$\overline{CE}_{CON1}$–$\overline{CE}_{CON4}$	Conditioned chip enable outputs
A–B	Decoder inputs
NC	No connect
V_{CC}	+5 volt supply input
V_{SS}	Ground

Functional Description

Up to four banks of CMOS static RAM can be battery-backed using the Vout and conditioned chip enable output pins from the bq2204. As V_{CC} slews down during a power failure, the conditioned chip enable outputs $\overline{CE}_{CON1}$ through $\overline{CE}_{CON4}$ are forced inactive independent of the chip enable input $\overline{CE}$.

This activity unconditionally write-protects external SRAM as V_{CC} falls to an out-of-tolerance threshold V_{PFD}. V_{PFD} is selected by the threshold select input pin, THS. If THS is tied to V_{SS}, the power-fail detection occurs at 4.62V typical for 5% supply operation. If THS is tied to V_{OUT}, power-fail detection occurs at 4.37V typical for 10% supply operation. The THS pin must be tied to V_{SS} or V_{OUT} for proper operation.

If a memory access is in process to any of the four external banks of SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT}, all four chip enable outputs are unconditionally driven high, write-protecting the controlled SRAMs.

As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to one of the two external backup energy sources. $\overline{CE}_{CON1}$ through $\overline{CE}_{CON4}$ are held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the 5V supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. Outputs $\overline{CE}_{CON1}$ through $\overline{CE}_{CON4}$ are held inactive for time t_{CER} (120 ms maximum) after the power supply has reached V_{PFD}, independent of the $\overline{CE}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}$ input is passed through to one of the four $\overline{CE}_{CON}$ outputs with a propagation delay of less than 10 ns. The $\overline{CE}$ input is output on one of the four $\overline{CE}_{CON}$ output pins depending on the level of the decode inputs at A and B as shown in the Truth Table.

The A and B inputs are usually tied to high-order address pins so that a large nonvolatile memory can be designed using lower-density memory devices. Nonvolatility and decoding are achieved by hardware hookup as shown in Figure 1.

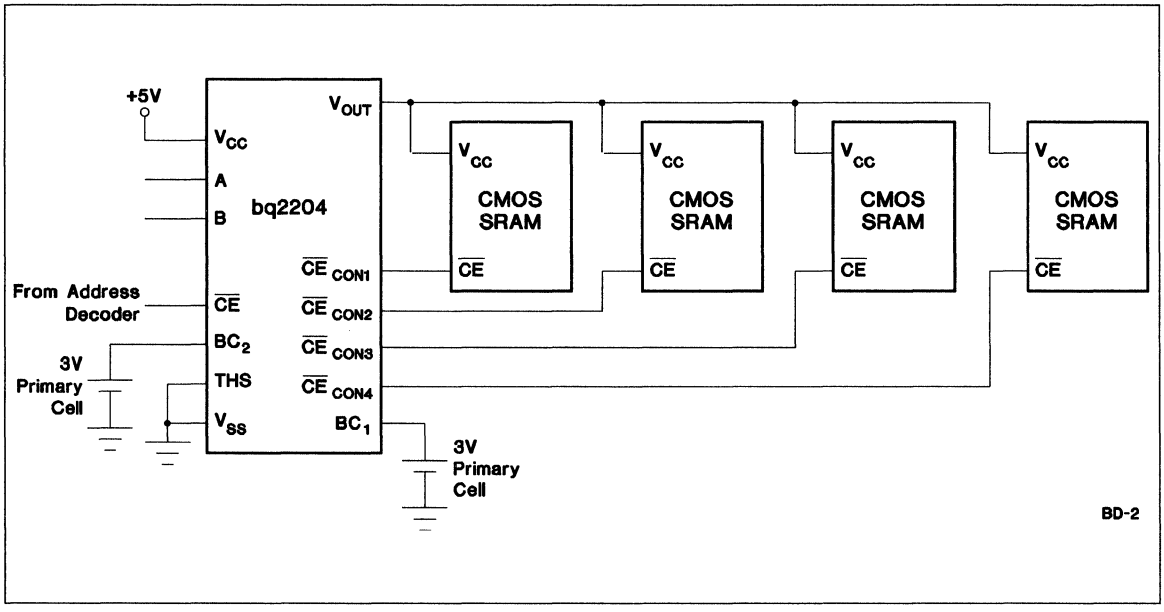


Figure 1. Hardware Hookup (5% Supply Operation)

Energy Cell Inputs—BC_1, BC_2

Two backup energy source inputs are provided on the bq2204. The BC_1 and BC_2 inputs accept a 3V primary battery, typically some type of lithium chemistry. If no primary cell is to be used on either BC_1 or BC_2, the unused input should be tied to Vss.

If both inputs are used, during power failure the V_{OUT} output is fed only by BC_1 as long as it is greater than 2.5V. If the voltage at BC_1 falls below 2.5V, an internal isolation switch automatically switches V_{OUT} from BC_1 to BC_2.

To prevent battery drain when there is no valid data to retain, V_{OUT} is internally isolated from BC_1 and BC_2 by either:

- Initial connection of a battery to BC_1 or BC_2, or
- Presentation of an isolation signal on $\overline{CE}$.

A valid isolation signal requires $\overline{CE}$ low as V_{CC} crosses both V_{PFD} and V_{SO} during a power-down. Between these two points in time, $\overline{CE}$ must be brought to (0.48 to 0.52)*V_{CC} and held for at least 700ns. The isolation signal is invalid if $\overline{CE}$ exceeds 0.54V_{CC} at any point between V_{CC} crossing V_{PFD} and V_{SO}. See Figure 2.

The appropriate battery is connected to V_{OUT} immediately on subsequent application and removal of V_{CC}.

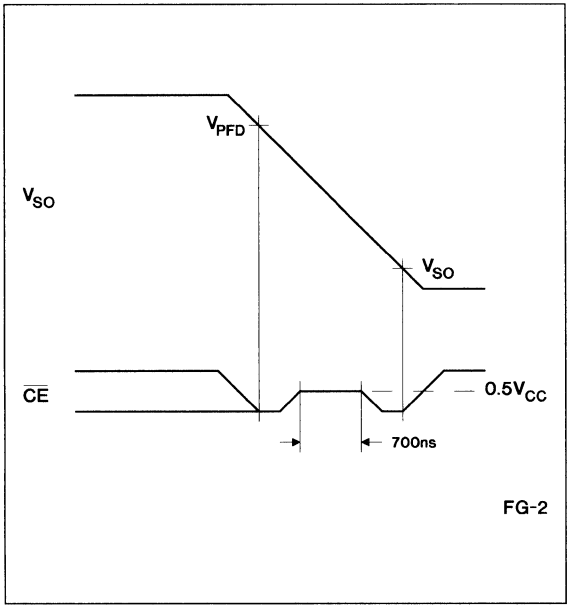


Figure 2. Battery Isolation Signal

Truth Table

Inputs			Outputs			
$\overline{CE}$	A	B	$\overline{CE}_{CON1}$	$\overline{CE}_{CON2}$	$\overline{CE}_{CON3}$	$\overline{CE}_{CON4}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to 70	°C	
T_{STG}	Storage temperature	-55 to 125	°C	
T_{BIAS}	Temperature under bias	-10 to 85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds
I_{OUT}	V_{OUT} current	200	mA	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.75	5.0	5.5	V	THS = V_{SS}
		4.50	5.0	5.5	V	THS = V_{OUT}
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	
V_{BC1}, V_{BC2}	Backup cell voltage	2.0	-	4.0	V	
THS	Threshold select	-0.3	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

DC Electrical Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -2.0 mA
V_{OHB}	V_{OH}, BC supply	V_{BC} - 0.3	-	-	V	$V_{BC} > V_{CC}$, I_{OH} = -10µA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current	-	3	6	mA	No load on V_{OUT}, and $\overline{CE}_{CON1}$–$\overline{CE}_{CON4}$.
V_{PFD}	Power-fail detect voltage	4.55	4.62	4.75	V	THS = V_{SS}
		4.30	4.37	4.50	V	THS = V_{OUT}
V_{SO}	Supply switch-over voltage	-	V_{BC}	-	V	
I_{CCDR}	Data-retention mode current	-	-	100	nA	V_{OUT} data-retention current to additional memory not included.
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.2	-	-	V	$V_{CC} > V_{BC}$, I_{OUT} = 100mA
		V_{CC} - 0.3	-	-	V	$V_{CC} > V_{BC}$, I_{OUT} = 150mA
V_{OUT2}	V_{OUT} voltage	V_{BC} - 0.2	-	-	V	$V_{CC} < V_{BC}$, I_{OUT} = 100µA
V_{BC}	Active backup cell voltage	-	V_{BC2}	-	V	V_{BC1} < 2.5V
		-	V_{BC1}	-	V	V_{BC1} > 2.5V
I_{OUT1}	V_{OUT} current	-	-	160	mA	$V_{OUT} > V_{CC}$ - 0.3V
I_{OUT2}	V_{OUT} current	-	100	-	µA	$V_{OUT} > V_{BC}$ - 0.2V

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
C_{IN}	Input capacitance	-	-	8	pF	Input voltage = 0V
C_{OUT}	Output capacitance	-	-	10	pF	Output voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 V to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figure 3

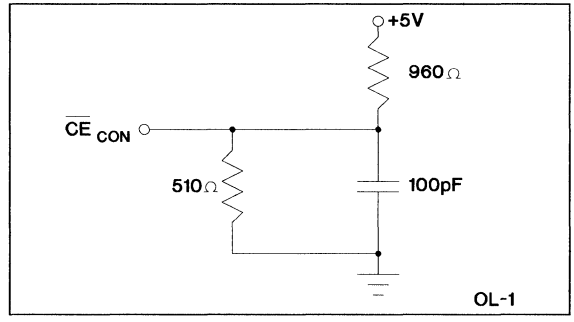


Figure 3. Output Load

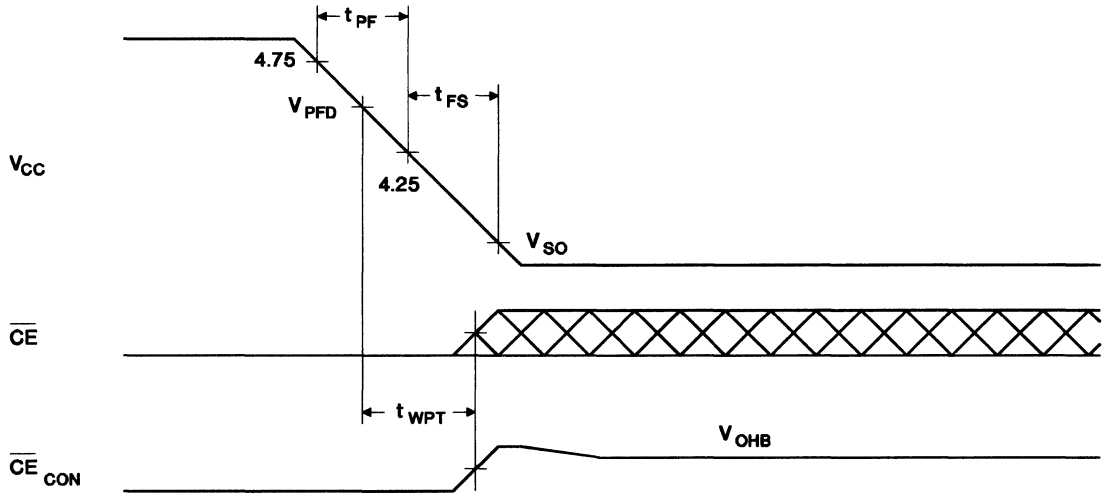
Power-Fail Control (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{PF}	V_{CC} slew, 4.75V to 4.25V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25V to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, 4.25V to 4.75V	0	-	-	µs	
t_{CED}	Chip enable propagation delay	-	7	10	ns	
t_{AS}	A,B set up to $\overline{CE}$	0	-	-	ns	
t_{CER}	Chip enable recovery	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

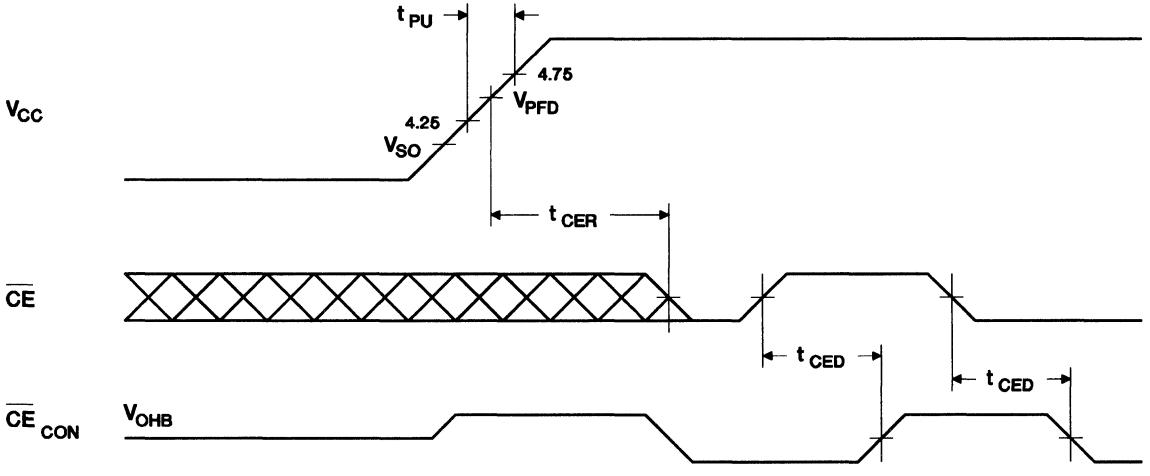
Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down Timing



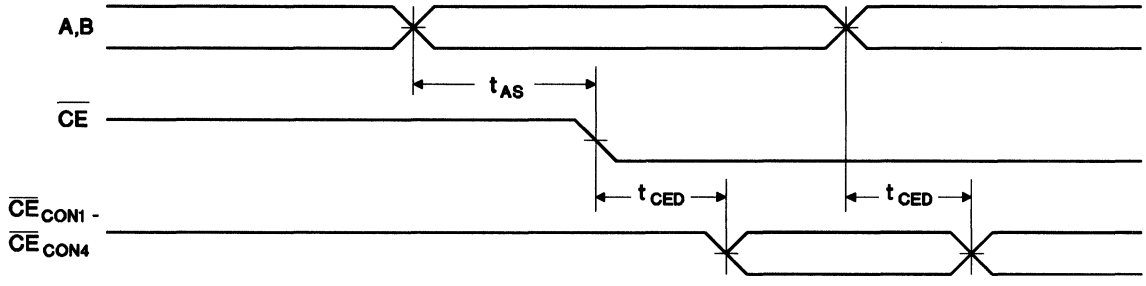
PD-1

Power-Up Timing



PU-1

Address-Decode Timing



AD-1

Ordering Information

bq2204 _

Package Option:
PN = 16-pin narrow plastic DIP
SN = 16-pin narrow SOIC

Device:
bq2204 Nonvolatile SRAM Controller

BENCHMARQ

Preliminary **bq3285**

Real-Time Clock (RTC)

Features

- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Socket and functionally compatible with the DS1285
  - Closely matches MC146818A pin configuration
- 160 ns cycle time allows fast bus operation
- Selectable Intel or Motorola bus timing
- Less than 0.5 µA load under battery operation
- 14 bytes for clock/calendar and control
- 50 bytes of general nonvolatile storage
- Calendar in days, day of the week, months, and years, with automatic leap-year adjustment
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- BCD or binary format for clock and calendar data
- Programmable square wave output
- Three individually maskable interrupt event flags:
  - Periodic rates from 122 µs to 500 ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle
- 24-pin plastic DIP or SOIC and 28-pin PLCC

General Description

The CMOS bq3285 is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. Other features include three maskable interrupt sources, square wave output, and 50 bytes of general nonvolatile storage.

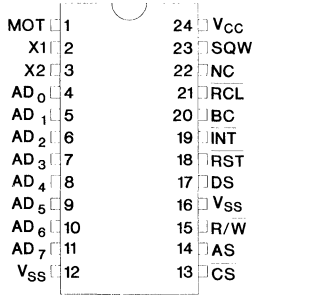
The bq3285 write-protects the clock, calendar, and storage registers during power failure. A backup battery then maintains data and operates the clock and calendar.

The bq3285 is a fully compatible real-time clock for IBM AT-compatible computers and other applications. The only external components are a 32.768 KHz crystal and a backup battery.

5

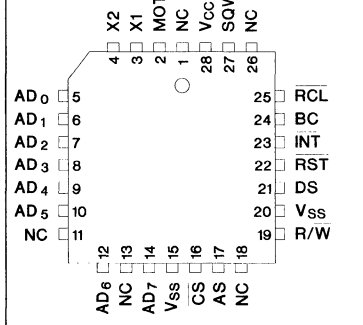
Pin Connections

24-Pin DIP or SOIC



PN-13

28-Pin PLCC

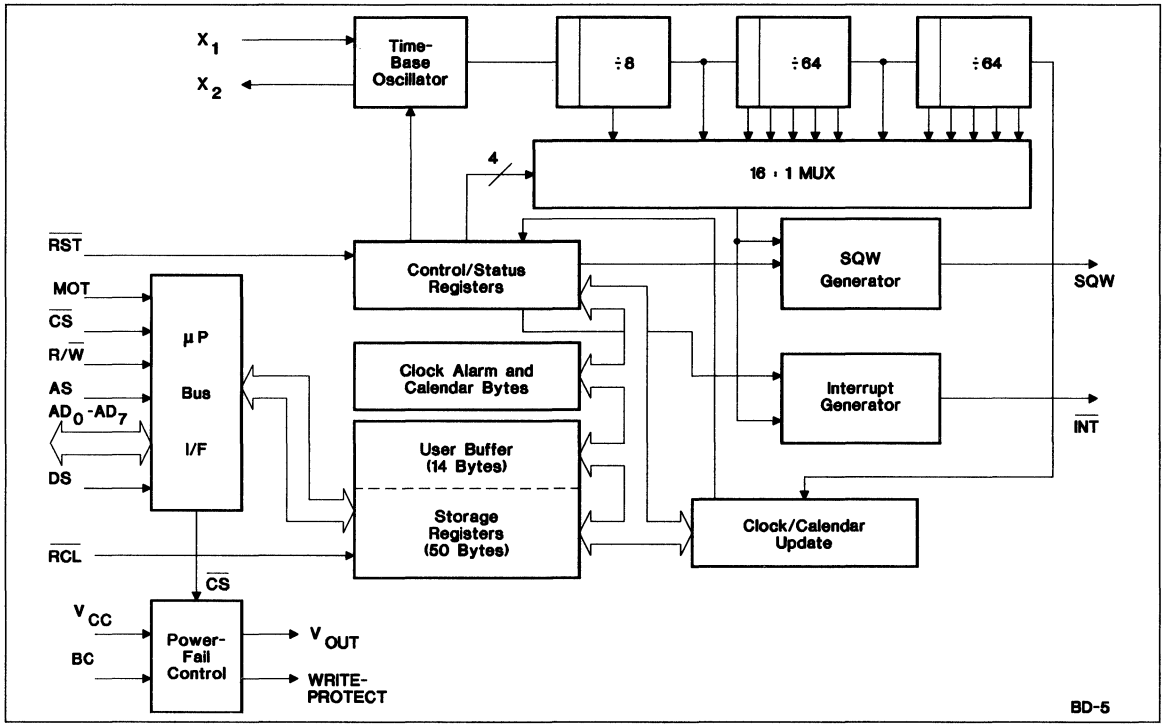


PL-3

Pin Names

AD_0–AD_7	Multiplexed address/data input/output
MOT	Bus type select input
$\overline{CS}$	Chip select input
AS	Address strobe input
DS	Data strobe input
R/$\overline{W}$	Read/write input
$\overline{INT}$	Interrupt request output
$\overline{RST}$	Reset input
SQW	Square wave output
$\overline{RCL}$	RAM clear input
BC	3V backup cell input
X1, X2	Crystal inputs
NC	No connect
V_{CC}	+5V supply
V_{SS}	Ground

Block Diagram



Pin Descriptions

MOT **Bus type select input**

MOT selects bus timing for either Motorola or Intel architecture. This pin should be tied to V_{CC} for Motorola timing or to V_{SS} for Intel timing (see Table 1). The setting should not be changed during system operation. MOT is internally pulled low by a 20K ohm resistor.

Table 1. Bus Setup

Bus Type	MOT Level	DS Equivalent	R/$\overline{W}$ Equivalent	AS Equivalent
Motorola	V_{CC}	DS, E, or Φ2	R/$\overline{W}$	AS
Intel	V_{SS}	$\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$	$\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$	ALE

AD_0–AD_7 **Multiplexed address/data input/output**

The bq3285 bus cycle consists of two phases: the address phase and the data-transfer phase. The address phase precedes the data-transfer phase. During the address phase, address placed on AD_0–AD_7 is latched into the bq3285 on the falling edge of the AS signal. During the data-transfer phase of the bus cycle, the AD_0–AD_7 pins serve as a bidirectional data bus.

AS **Address strobe input**

AS serves to demultiplex the address/data bus. The falling edge of AS latches the address on AD_0–AD_7. This demultiplexing process is independent of the $\overline{CS}$ signal.

DS **Data strobe input**

When MOT = V_{CC}, DS controls data transfer during a bq3285 bus cycle. During a read cycle, the bq3285 drives the bus after the rising edge on DS. During a write cycle, the falling edge on DS is used to latch write data into the chip.

When MOT = V_{SS}, the DS input is provided a signal similar to $\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$ in an Intel-based system. The falling edge on DS is used to enable the outputs during a read cycle.

R/$\overline{W}$ **Read/write input**

When MOT = V_{CC}, the level on R/$\overline{W}$ identifies the direction of data transfer. A high level on R/$\overline{W}$ indicates a read bus cycle, whereas a low on this pin indicates a write bus cycle.

When MOT = V_{SS}, R/$\overline{W}$ is provided a signal similar to $\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$ in an Intel-based system. The rising edge on R/$\overline{W}$ latches data into the bq3285.

$\overline{CS}$ **Chip select input**

$\overline{CS}$ should be driven low and held stable during the data-transfer phase of a bus cycle accessing the bq3285.

$\overline{INT}$ **Interrupt request output**

$\overline{INT}$ is an open-drain output. $\overline{INT}$ is asserted low when any event flag is set and the corresponding event enable bit is also set. $\overline{INT}$ becomes high-impedance whenever register C is read (see the Control/Status Registers section).

SQW **Square wave output**

SQW may output a programmable frequency square wave signal during normal (V_{CC} valid) system operation. Any one of the 13 specific frequencies may be selected through register A. This pin is held low when the square wave enable bit (SQE) in register B is 0 (see the Control/Status Registers section).

$\overline{RCL}$ **RAM clear input**

A low level on the $\overline{RCL}$ pin causes the contents of each of the 50 storage bytes to be set to FF(hex). The contents of the clock and control registers are unaffected. This pin should be used as a user-interface input (pushbutton to ground) and not connected to the output of any active component. $\overline{RCL}$ input is only recognized when held low for at least 100 ms in the presence of V_{CC} when the oscillator is running. Using RAM clear does not affect the battery load.

BC **3V backup cell input**

BC should be connected to a 3V backup cell for RTC operation and storage register nonvolatility in the absence of power. When V_{CC} slews down past V_{BC} (3V typical), the integral control circuitry switches the power source to BC. When V_{CC} returns above V_{BC}, the power source is switched to V_{CC}.

$\overline{RST}$ **Reset input**

The bq3285 is reset when $\overline{RST}$ is pulled low. When reset, $\overline{INT}$ becomes high-impedance, and the bq3285 is not accessible. Table 4 in the Control/Status Registers section lists the register bits that are cleared by a reset.

Reset may be disabled by connecting $\overline{RST}$ to V_{CC}. This allows the control bits to retain their states through power-down/power-up cycles.

X1, X2 **Crystal input**

The X1, X2 inputs are provided for an external 32.768Khz quartz crystal, Daiwa DT-26S or equivalent. A trimming capacitor may be necessary for extremely precise time-base generation.

5

Functional Description

Address Map

The bq3285 provides 14 bytes of clock and control/status registers and 50 bytes of general nonvolatile storage. Figure 1 illustrates the address map for the bq3285.

Update Period

The update period for the bq3285 is one second. The bq3285 updates the contents of the clock and calendar locations during the update cycle at the end of each update period (see Figure 2). The alarm flag bit may also be set during the update cycle.

The bq3285 copies the local register updates into the user buffer accessed by the host processor. When a 1 is written to the update transfer inhibit bit (UTI) in register B, the user copy of the clock and calendar bytes remains unchanged, while the local copy of the same bytes continues to be updated every second.

The update-in-progress bit (UIP) in register A is set t_{BUC} time before the beginning of an update cycle (see Figure 2). This bit is cleared and the update-complete flag (UF) is set at the end of the update cycle.

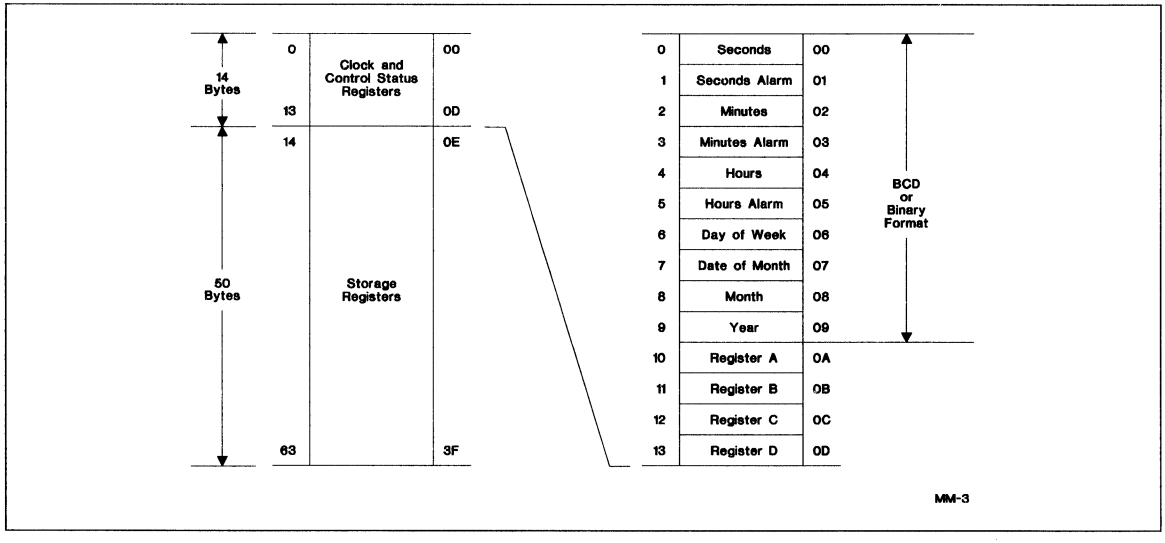


Figure 1. Address Map

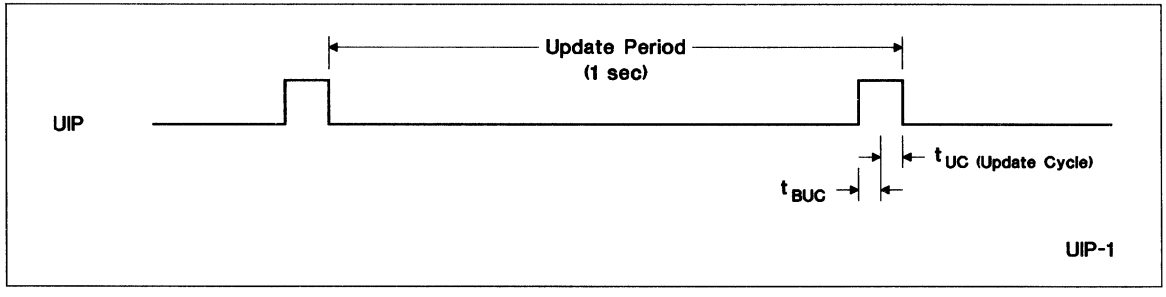


Figure 2. Update Period Timing and UIP

Programming the RTC

The time-of-day, alarm, and calendar bytes can be written in either the BCD or binary format (see Table 2).

These steps may be followed to program the time, alarm, and calendar:

1. Modify the contents of register B:
   a. Write a 1 to the UTI bit to prevent transfers between RTC bytes and user buffer.
   b. Write the appropriate value to the data format (DF) bit to select BCD or binary format for all time, alarm, and calendar bytes.
   c. Write the appropriate value to the hour format (HF) bit.
2. Write new values to all the time, alarm, and calendar locations.
3. Clear the UTI bit to allow update transfers.

On the next update cycle, the RTC updates all 10 bytes in the selected format.

Table 2. Time, Alarm, and Calendar Formats

Address	RTC Bytes	Range		
		Decimal	Binary	Binary-Coded Decimal
0	Seconds	0–59	00H–3BH	00H–59H
1	Seconds alarm	0–59	00H–3BH	00H–59H
2	Minutes	0–59	00H–3BH	00H–59H
3	Minutes alarm	0–59	00H–3BH	00H–59H
4	Hours, 12-hour format	1–12	01H–OCH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours, 24-hour format	0–23	00H–17H	00H–23H
5	Hours alarm, 12-hour format	1–12	01H–OCH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours alarm, 24-hour format	0–23	00H–17H	00H–23H
6	Day of week (1=Sunday)	1–7	01H–07H	01H–07H
7	Day of month	1–31	01H–1FH	01H–31H
8	Month	1–12	01H–0CH	01H–12H
9	Year	0–99	00H–63H	00H–99H

Square Wave Output

The bq3285 divides the 32.768 KHz oscillator frequency to produce the 1 Hz update frequency for the clock and calendar. Thirteen taps from the frequency divider are fed to a 16:1 multiplexer circuit. The output of this mux is fed to the SQW output and periodic interrupt generation circuitry. The four least significant bits of register A, RS0–RS3, select among the 13 taps (see Table 3). The square wave output is enabled by writing a 1 to the square wave enable bit (SQE) in register B.

Interrupts

The bq3285 allows three individually selected interrupt events to generate an interrupt request. These three interrupt events are:

- The periodic interrupt, programmable to occur once every 122 µs to 500 ms
- The alarm interrupt, programmable to occur once per second to once per day
- The update-ended interrupt, which occurs at the end of each update cycle

Each of the three interrupt events is enabled by an individual interrupt-enable bit in register B. When an event occurs, its event flag bit in register C is set. If the corresponding event enable bit is also set, then an interrupt request is generated. The interrupt request flag bit (INTF) of register C is set with every interrupt request. Reading register C clears all flag bits, including INTF, and makes $\overline{INT}$ high-impedance.

Two methods can be used to process bq3285 interrupt events:

- Enable interrupt events and use the interrupt request output to invoke an interrupt service routine.
- Do not enable the interrupts and use a polling routine to periodically check the status of the flag bits.

The individual interrupt sources are described in detail in the following sections.

Table 3. Square Wave Frequency/Periodic Interrupt Rate

Register A Bits				Square Wave		Periodic Interrupt	
RS3	RS2	RS1	RS0	Frequency	Units	Period	Units
0	0	0	0	None		None	
0	0	0	1	256	Hz	3.90625	ms
0	0	1	0	128	Hz	7.8125	ms
0	0	1	1	8.192	KHz	122.070	µs
0	1	0	0	4.096	KHz	244.141	µs
0	1	0	1	2.048	KHz	488.281	µs
0	1	1	0	1.024	KHz	976.5625	µs
0	1	1	1	512	Hz	1.953125	ms
1	0	0	0	256	Hz	3.90625	ms
1	0	0	1	128	Hz	7.8125	ms
1	0	1	0	64	Hz	15.625	ms
1	0	1	1	32	Hz	31.25	ms
1	1	0	0	16	Hz	62.5	ms
1	1	0	1	8	Hz	125	ms
1	1	1	0	4	Hz	250	ms
1	1	1	1	2	Hz	500	ms

Periodic Interrupt

The mux output used to drive the SQW output also drives the interrupt-generation circuitry. If the periodic interrupt event is enabled by writing a 1 to the periodic interrupt enable bit (PIE) in register C, an interrupt request is generated once every 122µs to 500ms. The period between interrupts is selected by the same bits in register A that select the square wave frequency (see Table 3).

Alarm Interrupt

During each update cycle, the RTC compares the hours, minutes, and seconds bytes with the three corresponding alarm bytes. If a match of all bytes is found, the alarm interrupt event flag bit, AF in register C, is set to 1. If the alarm event is enabled, an interrupt request is generated.

An alarm byte may be removed from the comparison by setting it to a "don't care" state. An alarm byte is set to a "don't care" state by writing a 1 to each of its two most-significant bits. A "don't care" state may be used to select the frequency of alarm interrupt events as follows:

- If none of the three alarm bytes is "don't care," the frequency is once per day, when hours, minutes, and seconds match.
- If only the hour alarm byte is "don't care," the frequency is once per hour, when minutes and seconds match.
- If only the hour and minute alarm bytes are "don't care," the frequency is once per minute, when seconds match.
- If the hour, minute, and second alarm bytes are "don't care," the frequency is once per second.

Update Cycle Interrupt

The update cycle ended flag bit (UF) in register C is set to a 1 at the end of an update cycle. If the update interrupt enable bit (UIE) of register B is 1, and the update transfer inhibit bit (UTI) in register B is 0, then an interrupt request is generated at the end of each update cycle.

Accessing RTC bytes

Time and calendar bytes read during an update cycle may be in error. Three methods to access the time and calendar bytes without ambiguity are:

- Enable the update interrupt event to generate interrupt requests at the end of the update cycle. The interrupt handler has a maximum of 999ms to access the clock bytes before the next update cycle begins (see Figure 3).
- Poll the update-in-progress bit (UIP) in register A. If UIP = 0, the polling routine has a minimum of t_{BUC} time to access the clock bytes (see Figure 3).
- Use the periodic interrupt event to generate interrupt requests every t_{PI} time, such that UIP = 1 always occurs between the periodic interrupts. The interrupt handler will have a minimum of $t_{PI}/2 + t_{BUC}$ time to access the clock bytes (see Figure 3).

Oscillator Control

When power is first applied to the bq3285 and V_{CC} is above V_{PFD}, the internal oscillator and frequency divider are turned on by writing a 010 pattern to bits 4 through 6 of register A. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. Any other pattern to these bits keeps the oscillator off.

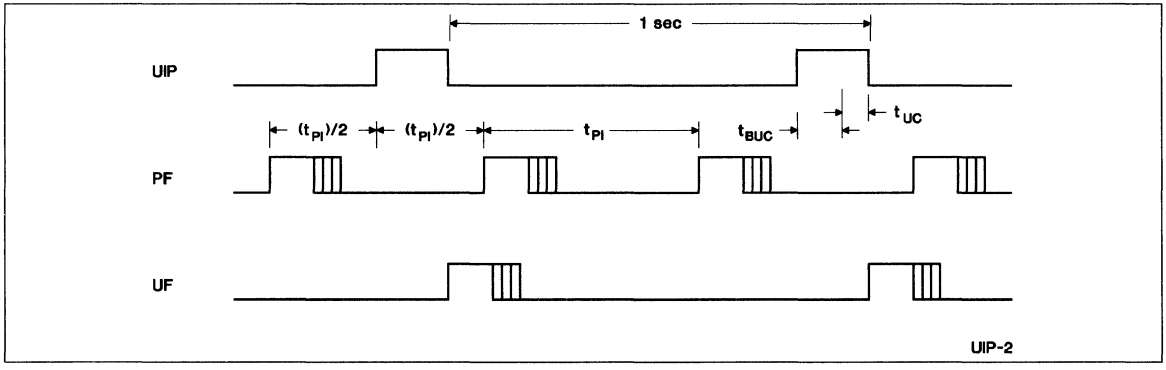


Figure 3. Update-Ended/Periodic Interrupt Relationship

Power-Down/Power-Up Cycle

The bq3285 continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD} (4.37V typical), the bq3285 write-protects the clock and storage registers. When V_{CC} is below V_{BC} (3V typical), the power source is switched to BC. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{BC}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

Control/Status Registers

The four control/status registers of the bq3285 are accessible regardless of the status of the update cycle (see Table 4).

Register A

Register A programs:

Register A Bits							
7	6	5	4	3	2	1	0
UIP	OS2	OS1	OS0	RS3	RS2	RS1	RS0

- The frequency of the square wave and the periodic event rate.
- Oscillator operation.

Register A provides:

- Status of the update cycle.

RS0–RS3 - Frequency Select

7	6	5	4	3	2	1	0
-	-	-	-	RS3	RS2	RS1	RS0

These bits select one of the 13 frequencies for the SQW output and the periodic interrupt rate, as shown in Table 3.

OS0–OS2 - Oscillator Control

7	6	5	4	3	2	1	0
-	OS2	OS1	OS0	-	-	-	-

These three bits control the state of the oscillator and divider stages. A pattern of 010 enables RTC operation by turning on the oscillator and enabling the frequency divider. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. When 010 is written, the RTC begins its first update after 500ms.

UIP - Update Cycle Status

7	6	5	4	3	2	1	0
UIP	-	-	-	-	-	-	-

This read-only bit is set prior to the update cycle. When UIP equals 1, an RTC update cycle may be in progress. UIP is cleared at the end of each update cycle. This bit is also cleared when the update transfer inhibit (UTI) bit in register B is 1.

Table 4. Control/Status Registers

Reg.	Loc. (Hex)	Read	Write	Bit Name and State on Reset															
				7 (MSB)		6		5		4		3		2		1		0 (LSB)	
A	0A	Yes	Yes[1]	UIP	na	OS2	na	OS2	na	OS0	na	RS3	na	RS2	na	RS1	na	RS0	na
B	0B	Yes	Yes	UTI	na	PIE	0	AIE	0	UIE	0	SQWE	0	DF	na	HF	na	DSE	na
C	0C	Yes	No	INTF	0	PF	0	AF	0	UF	0	-	0	-	0	-	0	-	0
D	0C	Yes	No	VRT	na	-	0	-	0	-	0	-	0	-	0	-	0	-	0

Notes: na = not affected.
1. Except bit 7.

Register B

Register B Bits							
7	6	5	4	3	2	1	0
UTI	PIE	AIE	UIE	SQWE	DF	HF	DSE

Register B enables:

- Update cycle transfer operation
- Square wave output
- Interrupt events
- Daylight saving adjustment

Register B selects:

- Clock and calendar data formats

All bits of register B are read/write.

DSE - Daylight Saving Enable

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DSE

This bit enables daylight-saving time adjustments when written to 1:

- On the last Sunday in October, the first time the bq3285 increments past 1:59:59 AM, the time falls back to 1:00:00 AM.
- On the first Sunday in April, the time springs forward from 2:00:00 AM to 3:00:00 AM.

HF - Hour Format

7	6	5	4	3	2	1	0
-	-	-	-	-	-	HF	-

This bit selects the time-of-day and alarm hour format:

1 = 24-hour format

0 = 12-hour format

DF - Data Format

7	6	5	4	3	2	1	0
-	-	-	-	-	DF	-	-

This bit selects the numeric format in which the time, alarm, and calendar bytes are represented:

1 = Binary

0 = BCD

SQWE - Square Wave Enable

7	6	5	4	3	2	1	0
-	-	-	-	SQWE	-	-	-

This bit enables the square wave output:

1 = Enabled

0 = Disabled and held low

UIE - Update Cycle Interrupt Enable

7	6	5	4	3	2	1	0
-	-	-	UIE	-	-	-	-

This bit enables an interrupt request due to an update ended interrupt event:

1 = Enabled

0 = Disabled

The UIE bit is automatically cleared when the UTI bit equals 1.

AIE - Alarm Interrupt Enable

7	6	5	4	3	2	1	0
-	-	AIE	-	-	-	-	-

This bit enables an interrupt request due to an alarm interrupt event:

1 = Enabled

0 = Disabled

PIE - Periodic Interrupt Enable

7	6	5	4	3	2	1	0
-	PIE	-	-	-	-	-	-

This bit enables an interrupt request due to a periodic interrupt event:

1 = Enabled

0 = Disabled

UTI - Update Transfer Inhibit

This bit inhibits the transfer of RTC bytes to the user buffer:

7	6	5	4	3	2	1	0
UTI	-	-	-	-	-	-	-

1 = Inhibits transfer and clears UIE

0 = Allows transfer

Register C

Register C Bits							
7	6	5	4	3	2	1	0
INTF	PF	AF	UF	0	0	0	0

Register C is the read-only event status register.

Bits 0–3 - Unused Bits

7	6	5	4	3	2	1	0
-	-	-	-	0	0	0	0

These bits are always set to 0.

UF - Update Event Flag

7	6	5	4	3	2	1	0
-	-	-	UF	-	-	-	-

This bit is set to a 1 at the end of the update cycle. Reading register C clears this bit.

AF - Alarm Event Flag

7	6	5	4	3	2	1	0
-	-	AF	-	-	-	-	-

This bit is set to a 1 when an alarm event occurs. Reading register C clears this bit.

PF - Periodic Event Flag

7	6	5	4	3	2	1	0
-	PF	-	-	-	-	-	-

This bit is set to a 1 every t_{PI} time, where t_{PI} is the time period selected by the settings of RS0–RS3 in register A. Reading register C clears this bit.

INTF - Interrupt Request Flag

7	6	5	4	3	2	1	0
INTF	-	-	-	-	-	-	-

This flag is set to a 1 when any of the following is true:

AIE = 1 and AF = 1

PIE = 1 and PF = 1

UIE = 1 and UF = 1

Reading register C clears this bit.

Register D

Register D Bits							
7	6	5	4	3	2	1	0
VRT	0	0	0	0	0	0	0

Register D is the read-only data integrity status register.

Bits 0–6 - Unused Bits

7	6	5	4	3	2	1	0
-	0	0	0	0	0	0	0

These bits are always set to 0.

VRT - Valid RAM and Time

7	6	5	4	3	2	1	0
VRT	-	-	-	-	-	-	-

1 = Valid backup energy source

0 = Backup energy source is depleted

When the backup energy source is depleted (VRT = 0), data integrity of the RTC and storage registers is not guaranteed.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-10 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

5

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IL}	Input low voltage	-0.3	-	0.8	V
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V
V_{BC}	Backup cell voltage	2.0	-	4.0	V

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	AD_0–AD_7, $\overline{INT}$, and SQW in high impedance, V_{OUT} = V_{SS} to V_{CC}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -2.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current	-	7	15	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
V_{SO}	Supply switch-over voltage	-	V_{BC}	-	V	
I_{CCB}	Battery operation current	-	0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C
V_{PFD}	Power-fail-detect voltage	4.30	4.37	4.45	V	
I_{RCL}	Input current when $\overline{RCL}$ = V_{SS}.	-	-	550	µA	Internal 20K pull-up
I_{MOTH}	Input current when MOT = V_{CC}	-	-	-550	µA	Internal 20K pull-down

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC} = 3V.

Crystal Specifications (DT-26S or Equivalent)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_O	Oscillation frequency	-	32.768	-	KHz
C_L	Load capacitance	-	6	-	pF
T_P	Temperature turnover point	20	25	30	°C
k	Parabolic curvature constant	-	-	-0.042	ppm/°C
Q	Quality factor	40,000	70,000	-	
R_1	Series resistance	-	-	45	KΩ
C_0	Shunt capacitance	-	1.1	1.8	pF
C_0/C_1	Capacitance ratio	-	430	600	
D_L	Drive level	-	-	1	µW
$\Delta f/f_O$	Aging (first year at 25°C)	-	1	-	ppm

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	7	pF	V_{OUT} = 0V
C_{IN}	Input capacitance	-	-	5	pF	V_{IN} = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

5

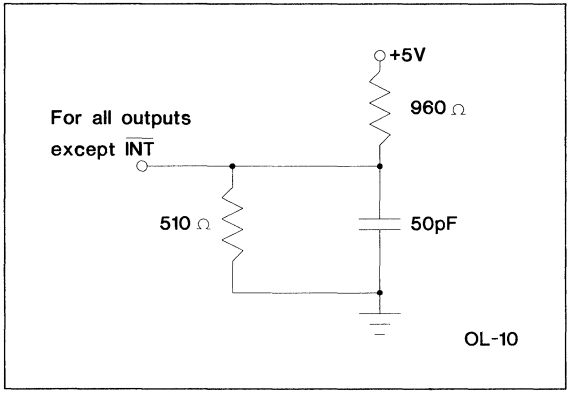


Figure 4. Output Load A

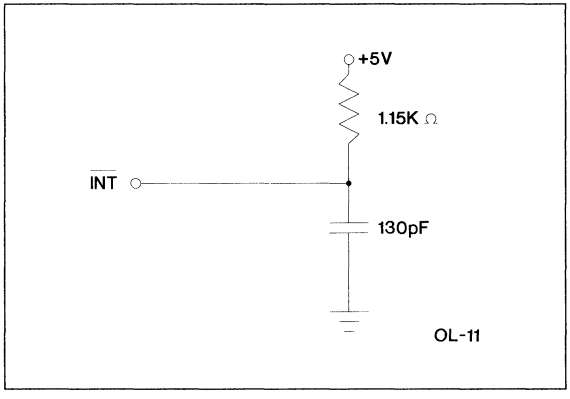
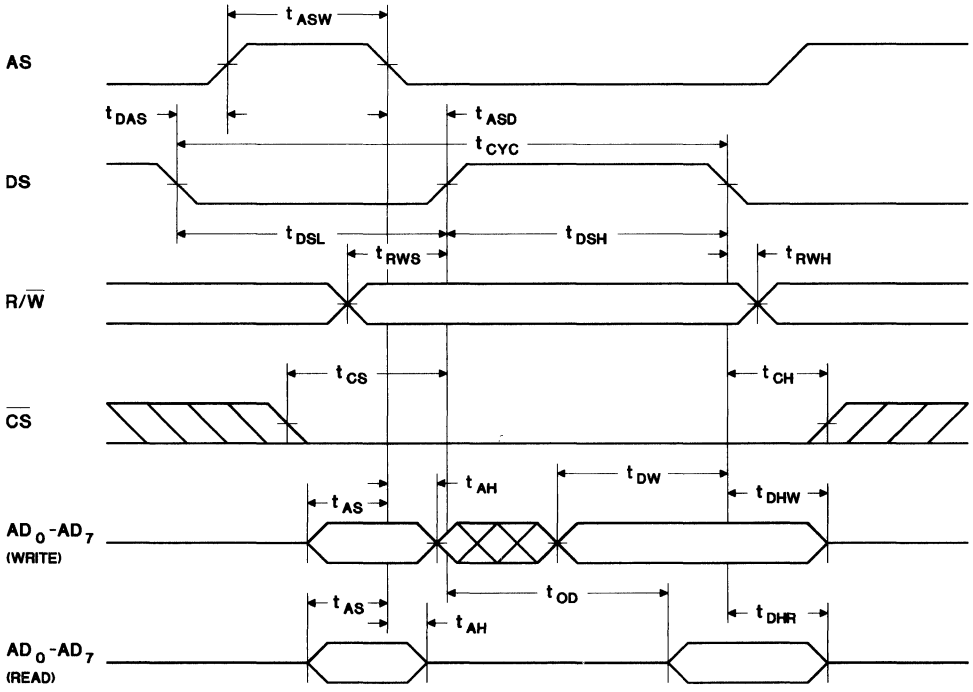


Figure 5. Output Load B

Read/Write Timing (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

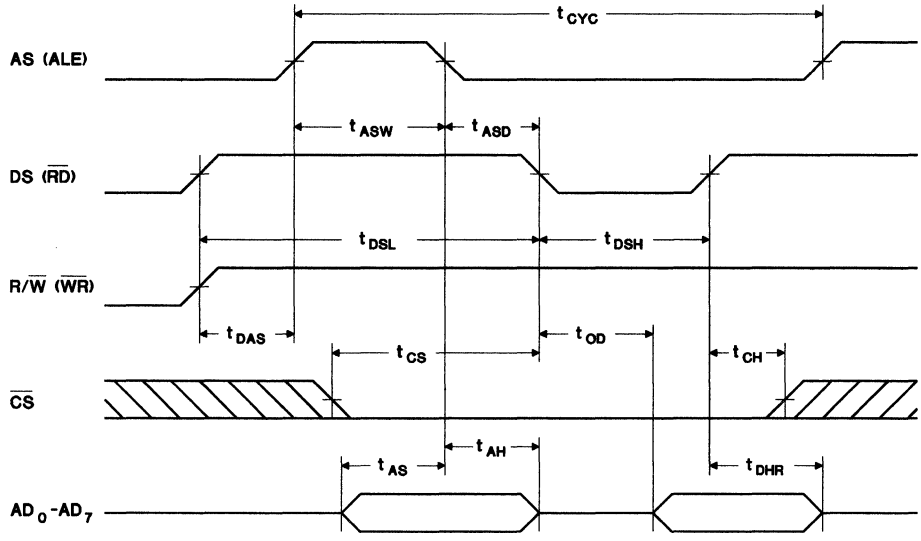
Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{CYC}	Cycle time	160	-	-	ns
t_{DSL}	DS low or $\overline{RD}/\overline{WR}$ high time	80	-	-	ns
t_{DSH}	DS high or $\overline{RD}/\overline{WR}$ low time	55	-	-	ns
t_{RWH}	R/$\overline{W}$ hold time	0	-	-	ns
t_{RWS}	R/$\overline{W}$ setup time	10	-	-	ns
t_{CS}	Chip select setup time	5	-	-	ns
t_{CH}	Chip select hold time	0	-	-	ns
t_{DHR}	Read data hold time	0	-	25	ns
t_{DHW}	Write data hold time	0	-	-	ns
t_{AS}	Address setup time	20	-	-	ns
t_{AH}	Address hold time	5	-	-	ns
t_{DAS}	Delay time, DS to AS rise	10	-	-	ns
t_{ASW}	Pulse width, AS high	30	-	-	ns
t_{ASD}	Delay time, AS to DS rise ($\overline{RD}/\overline{WR}$ fall)	35	-	-	ns
t_{OD}	Output data delay time from DS rise ($\overline{RD}$ fall)	-	-	35	ns
t_{DW}	Write data setup time	30	-	-	ns

Motorola Bus Read/Write Timing



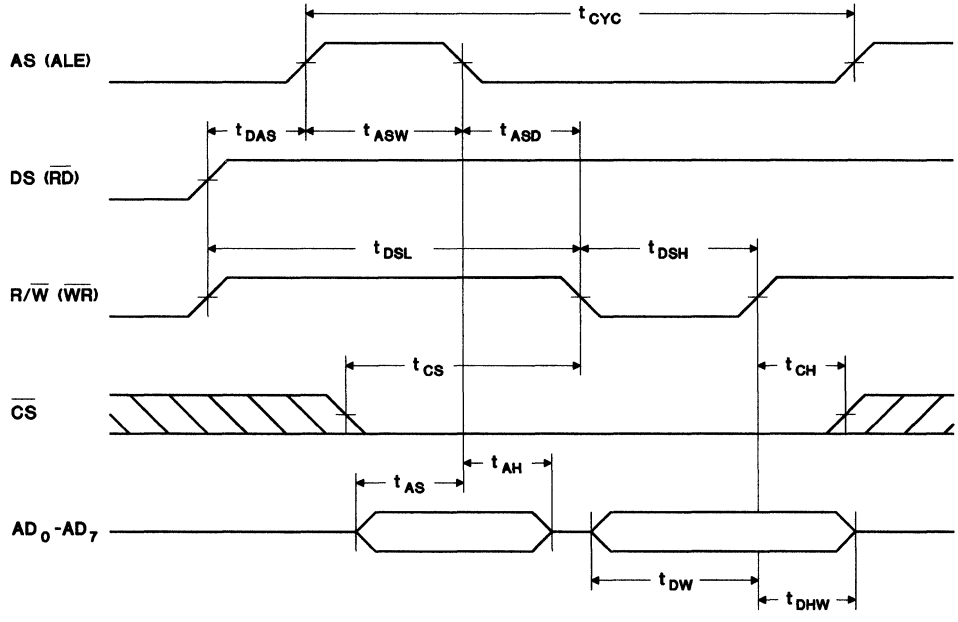
RC-4

Intel Bus Read Timing



RC-5

Intel Bus Write Timing



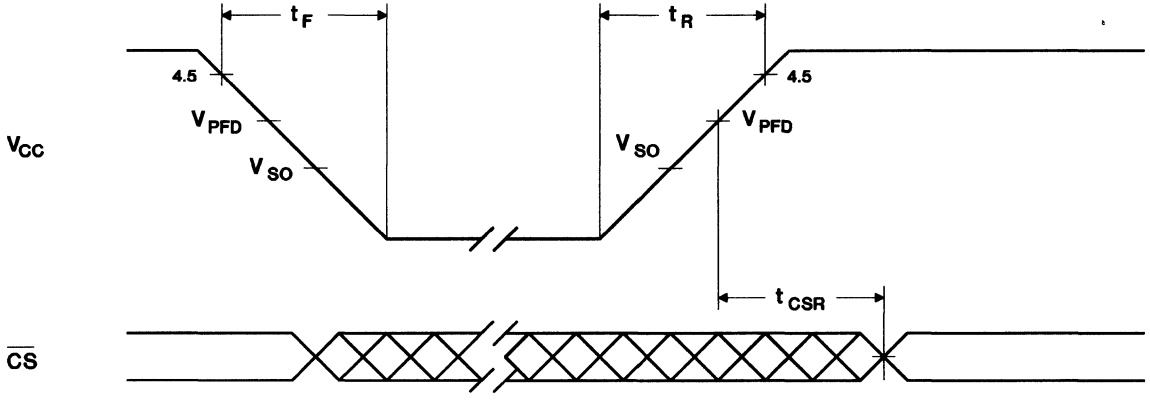
WC-5

Power-Down/Power-Up Timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.5V to 0V	300	-	-	µs	
t_R	V_{CC} slew from 0V to 4.5V	100	-	-	µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20	-	200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing

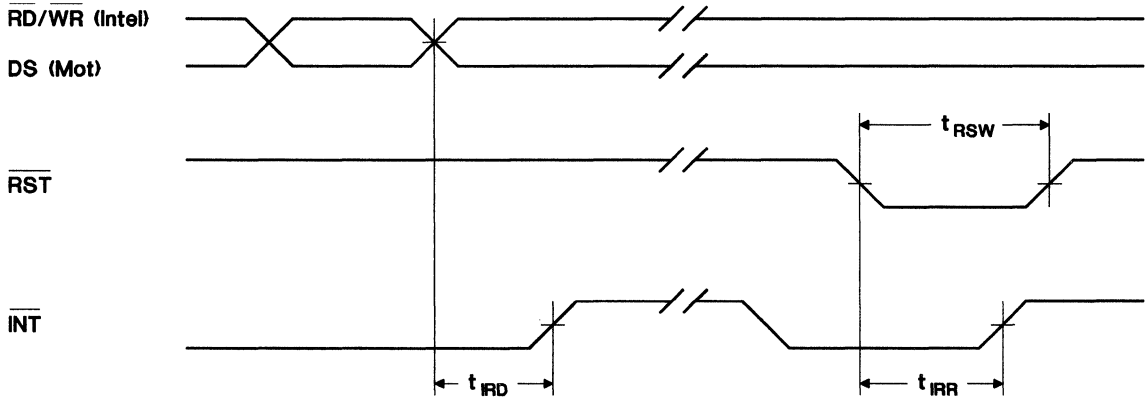


PD-4A

Interrupt Delay Timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{RSW}	Reset pulse width	5	-	-	µs
t_{IRR}	$\overline{INT}$ release from $\overline{RST}$	-	-	2	µs
t_{IRD}	$\overline{INT}$ release from DS	-	-	2	µs

Interrupt Delay Timing



INT-1

Ordering Information

bq3285 _

Package Option:
P = 24-pin plastic DIP (0.600)
S = 24-pin SOIC (0.300)
Q = 28-pin quad PLCC

Device:
bq3285 Real-Time Clock with 50 bytes of general storage

BENCHMARQ

Preliminary **bq3287/bq3287A**

Real-Time Clock (RTC) Module

Features

- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Pin-compatible with the DS1287/DS1287A and MC146818A
- Integral lithium cell and crystal
- 160 ns cycle time allows fast bus operation
- Selectable Intel or Motorola bus timing
- 14 bytes for clock/calendar and control
- 50 bytes of general nonvolatile storage
- Calendar in days, day of the week, months, and years with automatic leap-year adjustment
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- BCD or binary format for clock and calendar data
- Programmable square wave output
- Three individually maskable interrupt event flags:
  - Periodic rates from 122 µs to 500 ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle
- Better than one minute per month clock accuracy

General Description

The CMOS bq3287/bq3287A is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. Other features include three maskable interrupt sources, square wave output, and 50 bytes of general nonvolatile storage. The bq3287A version is identical to the bq3287, with the addition of the RAM clear input.

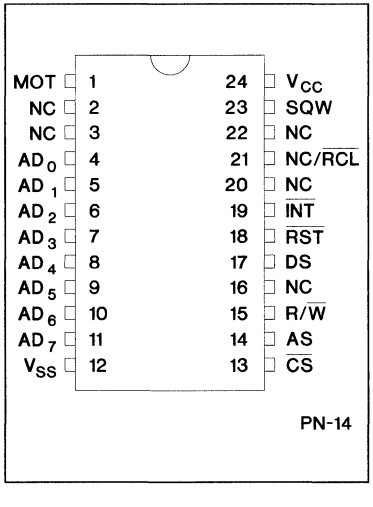
The bq3287 write-protects the clock, calendar, and storage registers during power failure. The integral backup energy source then maintains data and operates the clock and calendar.

The bq3287 is a fully compatible real-time clock for IBM AT-compatible computers and other applications.

As shipped from Benchmarq, the backup cell is electrically isolated from the memory. Following the first application of V_{CC}, this isolation is broken, and the backup cell provides data retention on subsequent power-downs.

5

Pin Connections

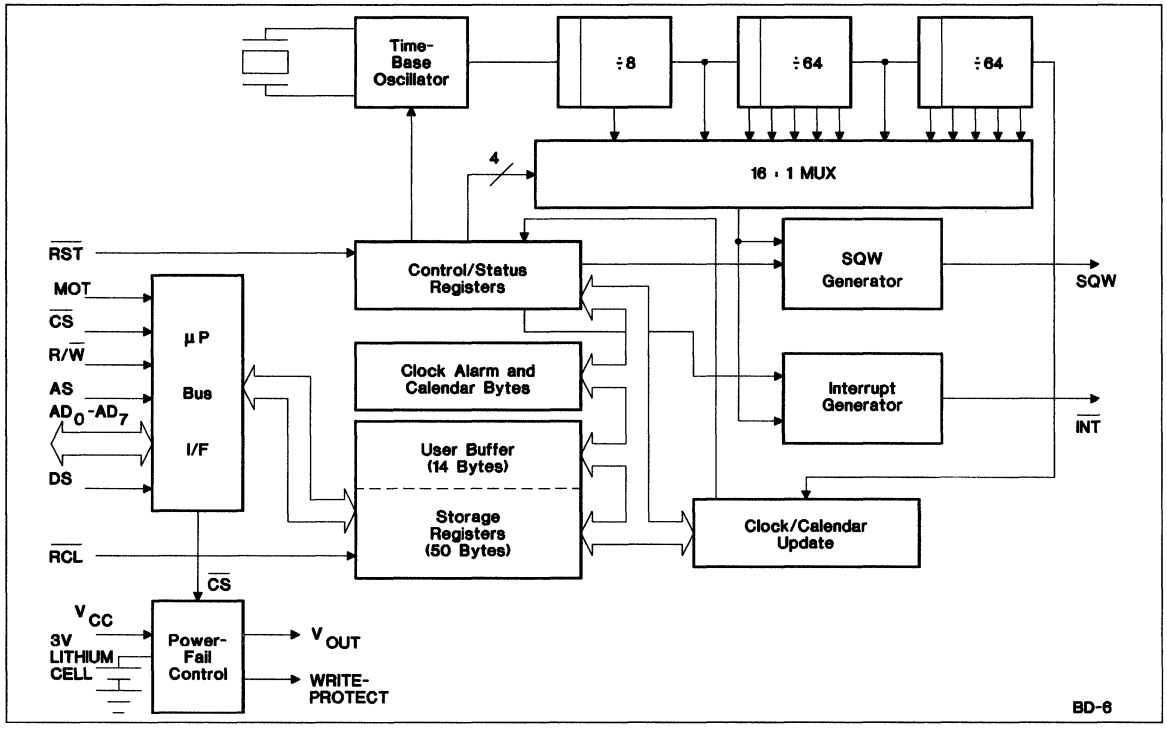


PN-14

Pin Names

AD_0–AD_7	Multiplexed address/data input/output
MOT	Bus type select input
$\overline{CS}$	Chip select input
AS	Address strobe input
DS	Data strobe input
R/$\overline{W}$	Read/write input
$\overline{INT}$	Interrupt request output
$\overline{RST}$	Reset input
SQW	Square wave output
$\overline{RCL}$	RAM clear input (bq3287A only)
NC	No connect
V_{CC}	+5V supply
V_{SS}	Ground

Block Diagram



Pin Descriptions

MOT **Bus type select input**

MOT selects bus timing for either Motorola or Intel architecture. This pin should be tied to V_{CC} for Motorola timing or to V_{SS} for Intel timing (see Table 1). The setting should not be changed during system operation. MOT is internally pulled low by a 20K ohm resistor.

Table 1. Bus Setup

Bus Type	MOT Level	DS Equivalent	R/$\overline{W}$ Equivalent	AS Equivalent
Motorola	V_{CC}	DS, E, or Φ2	R/$\overline{W}$	AS
Intel	V_{SS}	$\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$	$\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$	ALE

AD_0–AD_7 **Multiplexed address/data input/output**

The bq3287 bus cycle consists of two phases: the address phase and the data-transfer phase. The address phase precedes the data-transfer phase. During the address phase, address placed on AD_0–AD_7 is latched into the bq3287 on the falling edge of the AS signal. During the data-transfer phase of the bus cycle, the AD_0–AD_7 pins act as a bidirectional data bus.

AS **Address strobe input**

AS serves to demultiplex the address/data bus. The falling edge of AS latches the address on AD_0–AD_7. This demultiplexing process is independent of the $\overline{CS}$ signal.

DS **Data strobe input**

When MOT = V_{CC}, DS controls data transfer during a bq3287 bus cycle. During a read cycle, the bq3287 drives the bus after the rising edge on DS. During a write cycle, the falling edge on DS is used to latch write data into the chip.

When MOT = V_{SS}, the DS input is provided a signal similar to $\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$ in an Intel-based system. The falling edge on DS is used to enable the outputs during a read cycle.

R/$\overline{W}$ **Read/write input**

When MOT = V_{CC}, the level on R/$\overline{W}$ identifies the direction of data transfer. A high level on R/$\overline{WR}$ indicates a read bus cycle, whereas a low on this pin indicates a write bus cycle.

When MOT = V_{SS}, R/$\overline{W}$ is provided a signal similar to $\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$ in an Intel-based system. The rising edge on R/$\overline{W}$ latches data into the bq3287.

$\overline{CS}$ **Chip select input**

$\overline{CS}$ should be driven low and held stable during the data-transfer phase of a bus cycle accessing the bq3287.

$\overline{INT}$ **Interrupt request output**

$\overline{INT}$ is an open-drain output. $\overline{INT}$ is asserted low when any event flag is set and the corresponding event enable bit is also set. $\overline{INT}$ becomes high-impedance whenever register C is read (see the Control/Status Registers section).

SQW **Square wave output**

SQW may output a programmable frequency square wave signal during normal (V_{CC} valid) system operation. Any one of the 13 specific frequencies may be selected through register A. This pin is held low when the square wave enable bit (SQE) in register B is 0 (see the Control/Status Registers section).

$\overline{RCL}$ **RAM clear input** (bq3287A only)

A low level on the $\overline{RCL}$ pin causes the contents of each of the 50 storage bytes to be set to FF(hex). The contents of the clock and control registers are unaffected. This pin should be used as a user-interface input (pushbutton to ground) and not connected to the output of any active component. $\overline{RCL}$ is recognized when held low for at least 100 ms in the presence of V_{CC} when the oscillator is running. Using RAM clear does not affect the battery load. This pin is a no connect on the bq3287.

$\overline{RST}$ **Reset input**

The bq3287 is reset when $\overline{RST}$ is pulled low. When reset, $\overline{INT}$ becomes high-impedance, and the bq3287 is not accessible. Table 4 in the Control/Status Registers section lists the register bits that are cleared by a reset.

Reset may be disabled by connecting $\overline{RST}$ to V_{CC}. This allows the control bits to retain their states through power-down/power-up cycles.

5

Functional Description

The bq3287A differs from the bq3287 only by the presence of $\overline{RCL}$ on pin 21. Otherwise, the two devices are identical.

Address Map

The bq3287 provides 14 bytes of clock and control/status registers and 50 bytes of general nonvolatile storage. Figure 1 illustrates the address map for the bq3287.

Update Period

The update period for the bq3287 is one second. The bq3287 updates the contents of the clock and calendar locations during the update cycle at the end of each update period (see Figure 2). The alarm flag bit may also be set during the update cycle.

The bq3287 copies the local register updates into the user buffer accessed by the host processor. When a 1 is written to the update transfer inhibit bit (UTI) in register B, the user copy of the clock and calendar bytes is frozen, while the local copy of the same bytes continues to be updated every second.

The update-in-progress bit (UIP) in register A is set t_{BUC} time before the beginning of an update cycle (see Figure 2). This bit is cleared and the update-complete flag (UF) is set at the end of the update cycle.

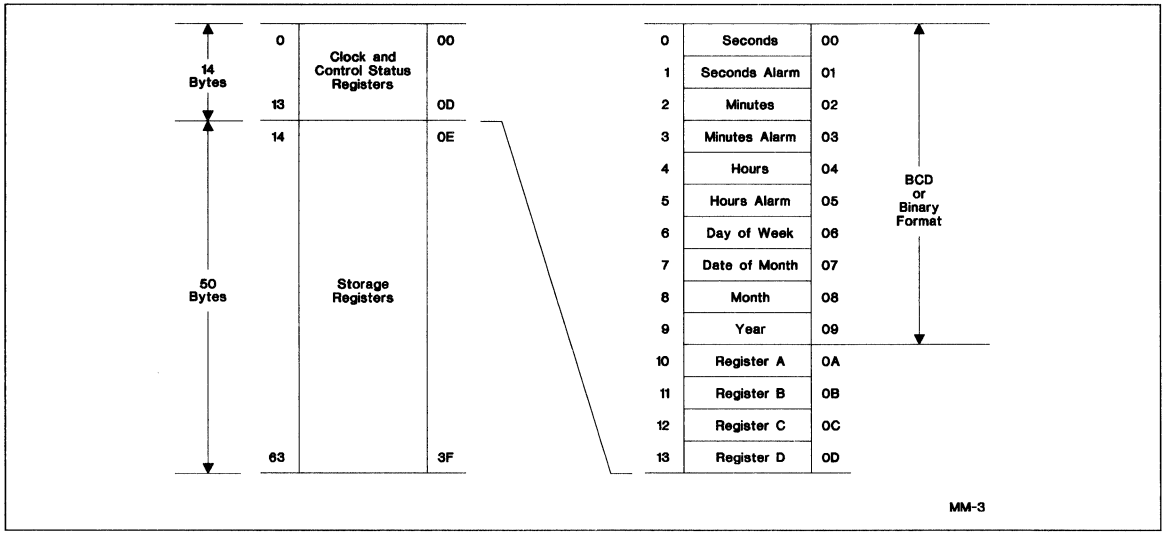


Figure 1. Address Map

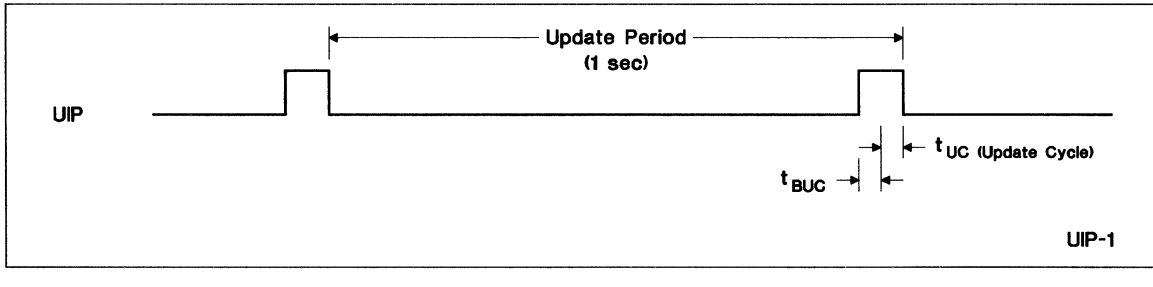


Figure 2. Update Period Timing and UIP

Programming the RTC

The time-of-day, alarm, and calendar bytes can be written in either the BCD or binary format (see Table 2).

These steps may be followed to program the time, alarm, and calendar:

1. Modify the contents of register B:
   a. Write a 1 to the UTI bit to prevent transfers between RTC bytes and user buffer.
   b. Write the appropriate value to the data format bit (DF) to select BCD or binary format for all clock and calendar bytes.
   c. Write the appropriate value to the hour format bit (HR).
2. Write new values to all the time, alarm, and calendar locations.
3. Clear the UTI bit to allow update transfers.

On the next update cycle, the RTC updates all 10 bytes in the selected format.

Table 2. Time, Alarm, and Calendar Formats

Address	RTC Bytes	Range		
		Decimal	Binary	Binary-Coded Decimal
0	Seconds	0–59	00H–3BH	00H–59H
1	Seconds alarm	0–59	00H–3BH	00H–59H
2	Minutes	0–59	00H–3BH	00H–59H
3	Minutes alarm	0–59	00H–3BH	00H–59H
4	Hours, 12-hour format	1–12	01H–OCH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours, 24-hour format	0–23	00H–17H	00H–23H
5	Hours alarm, 12-hour format	1–12	01H–OCH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours alarm, 24-hour format	0–23	00H–17H	00H–23H
6	Day of week (1=Sunday)	1–7	01H–07H	01H–07H
7	Day of month	1–31	01H–1FH	01H–31H
8	Month	1–12	01H–0CH	01H–12H
9	Year	0–99	00H–63H	00H–99H

Square Wave Output

The bq3287 divides the 32.768 KHz oscillator frequency to produce the 1 Hz update frequency for the clock and calendar. Thirteen taps from the frequency divider are fed to a 16:1 multiplexer circuit. The output of this mux is fed to the SQW output and periodic interrupt generation circuitry. The four least-significant bits of register A, RS0–RS3, select among the 13 taps (see Table 3). The square wave output is enabled by writing a 1 to the square wave enable bit (SQE) in register B.

Interrupts

The bq3287 allows three individually selected interrupt events to generate an interrupt request. These three interrupt events are:

- The periodic interrupt, programmable to occur once every 122 µs to 500 ms
- The alarm interrupt, programmable to occur once per second to once per day
- The update-ended interrupt, which occurs at the end of an RTC update cycle

Each of the three interrupt events is enabled by an individual interrupt-enable bit in register B. When an event occurs, its event flag bit in register C is set. If the corresponding event enable bit is also set, then an interrupt request is generated. The interrupt request flag bit (INTF) of register C is set with every interrupt request. Reading register C clears all flag bits, including INTF, and makes $\overline{INT}$ high-impedance.

Two methods can be used to process bq3287 interrupt events:

- Enable interrupt events and use the interrupt request output to invoke an interrupt service routine.
- Do not enable the interrupts and use a polling routine to periodically check the status of the flag bits.

The individual interrupt sources are described in detail in the following sections.

Table 3. Square Wave Frequency/Periodic Interrupt Rate

Register A Bits				Square Wave		Periodic Interrupt	
RS3	RS2	RS1	RS0	Frequency	Units	Period	Units
0	0	0	0	None		None	
0	0	0	1	256	Hz	3.90625	ms
0	0	1	0	128	Hz	7.8125	ms
0	0	1	1	8.192	KHz	122.070	µs
0	1	0	0	4.096	KHz	244.141	µs
0	1	0	1	2.048	KHz	488.281	µs
0	1	1	0	1.024	KHz	976.5625	µs
0	1	1	1	512	Hz	1.953125	ms
1	0	0	0	256	Hz	3.90625	ms
1	0	0	1	128	Hz	7.8125	ms
1	0	1	0	64	Hz	15.625	ms
1	0	1	1	32	Hz	31.25	ms
1	1	0	0	16	Hz	62.5	ms
1	1	0	1	8	Hz	125	ms
1	1	1	0	4	Hz	250	ms
1	1	1	1	2	Hz	500	ms

Periodic Interrupt

The mux output used to drive the SQW output also drives the interrupt-generation circuitry. If the periodic interrupt event is enabled by writing a 1 to the periodic interrupt enable bit (PIE) in register C, an interrupt request is generated once every 122µs to 500ms. The period between interrupts is selected by the same bits in register A that select the square wave frequency (see Table 3).

Alarm Interrupt

During each update cycle, the RTC compares the hours, minutes, and seconds bytes with the three corresponding alarm bytes. If a match of all bytes is found, the alarm interrupt event flag bit, AF in register C, is set to 1. If the alarm event is enabled, an interrupt request is generated.

An alarm byte may be removed from the comparison by setting it to a "don't care" state. An alarm byte is set to a "don't care" state by writing a 1 to each of its two most-significant bits. A "don't care" state may be used to select the frequency of alarm interrupt events as follows:

- If none of the three alarm bytes is "don't care," the frequency is once per day, when hours, minutes, and seconds match.
- If only the hour alarm byte is "don't care," the frequency is once per hour, when minutes and seconds match.
- If only the hour and minute alarm bytes are "don't care," the frequency is once per minute, when seconds match.
- If the hour, minute, and second alarm bytes are "don't care," the frequency is once per second.

Update Cycle Interrupt

The update cycle ended flag bit (UF) in register C is set to a 1 at the end of an update cycle. If the update interrupt enable bit (UIE) of register B is 1, and the update transfer inhibit bit (UTI) in register B is 0, then an interrupt request is generated at the end of each update cycle.

Accessing RTC bytes

Time and calendar readings may be in error. Three methods to access the RTC bytes without ambiguity are available:

- Enable the update interrupt event to generate interrupt requests at the end of the update cycle. The interrupt handler has a maximum of 999ms to access the clock bytes before the next update cycle begins (see Figure 3).
- Poll the update-in-progress bit (UIP) in register A. If UIP = 0, the polling routine has a minimum of t_{BUC} time to access the clock bytes (see Figure 3).
- Use the periodic interrupt event to generate interrupt requests every t_{PI} time, such that UIP = 1 always occurs between the periodic interrupts. The interrupt handler will finish accessing the clock bytes in $t_{PI}/2 + t_{BUC}$ time (see Figure 3).

Oscillator Control

The bq3287 is shipped from Benchmarq with its internal oscillator turned off. The internal oscillator and frequency divider are turned on by writing a 010 pattern to bits 4 through 6 of register A. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. Any other pattern to these bits keeps the oscillator off.

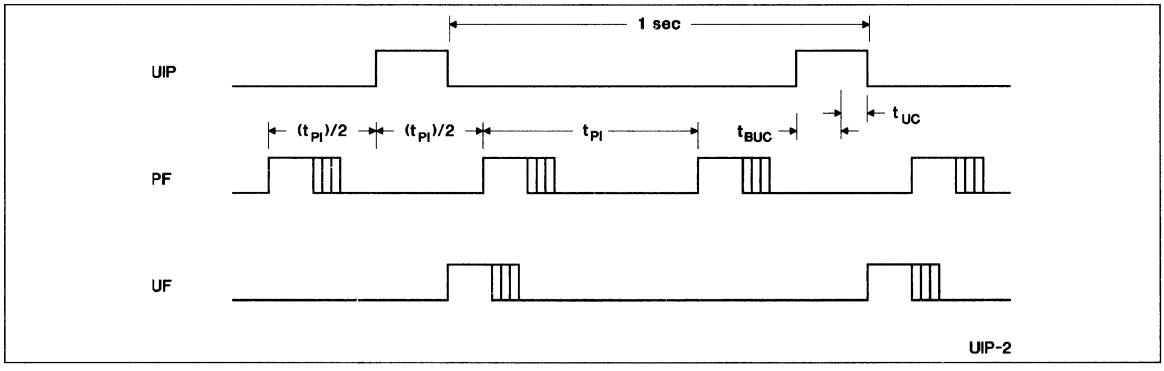


Figure 3. Update-Ended/Periodic Interrupt Relationship

Power-Down/Power-Up Cycle

The bq3287 continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD} (4.37V typical), the bq3287 write-protects the clock and storage registers. When V_{CC} is below V_{SO} (3V typical), the power source is switched to the internal lithium cell. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{SO}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

Control/Status Registers

The four control/status registers of the bq3287 are accessible regardless of the status of the update cycle (see Table 4).

Register A

Register A Bits							
7	6	5	4	3	2	1	0
UIP	OS2	OS1	OS0	RS3	RS2	RS1	RS0

Register A programs:

- The frequency of the square wave and the periodic event rate.
- Oscillator operation.

Register A provides:

- Status of the update cycle.

RS0–RS3 - Frequency Select

7	6	5	4	3	2	1	0
-	-	-	-	RS3	RS2	RS1	RS0

These bits select one of the 13 frequencies for the SQW output and the periodic interrupt rate, as shown in Table 3.

OS0–OS2 - Oscillator Control

7	6	5	4	3	2	1	0
-	OS2	OS1	OS0	-	-	-	-

These three bits control the state of the oscillator and divider stages. A pattern of 010 enables RTC operation by turning on the oscillator and enabling the frequency divider. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. The bq3287 is shipped from Benchmarq with its oscillator turned off. When 010 is written, the RTC begins its first update after 500ms.

UIP - Update Cycle Status

7	6	5	4	3	2	1	0
UIP	-	-	-	-	-	-	-

This read-only bit is set prior to the update cycle. When UIP equals 1, an RTC update cycle may be in progress. UIP is cleared at the end of each update cycle. This bit is also cleared when the update transfer inhibit (UTI) bit in register B is 1.

Table 4. Control/Status Registers

Reg.	Loc. (Hex)	Read	Write	Bit Name and State on Reset															
				7 (MSB)		6		5		4		3		2		1		0 (LSB)	
A	0A	Yes	Yes[1]	UIP	na	OS2	na	OS1	na	OS0	na	RS3	na	RS2	na	RS1	na	RS0	na
B	0B	Yes	Yes	UTI	na	PIE	0	AIE	0	UIE	0	SQWE	0	DF	na	HF	na	DSE	na
C	0C	Yes	No	INTF	0	PF	0	AF	0	UF	0	-	0	-	0	-	0	-	0
D	0C	Yes	No	VRT	na	-	0	-	0	-	0	-	0	-	0	-	0	-	0

Notes: na = not affected.

1. Except bit 7.

Register B

Register B Bits							
7	6	5	4	3	2	1	0
UTI	PIE	AIE	UIE	SQWE	DF	HF	DSE

Register B enables:

- Update cycle transfer operation
- Square wave output
- Interrupt events
- Daylight saving adjustment

Register B selects:

- Clock and calendar data formats

All bits of register B are read/write.

DSE - Daylight Saving Enable

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DSE

This bit enables daylight-saving time adjustments when written to 1:

- On the last Sunday in October, the first time the bq3285 increments past 1:59:59 AM, the time falls back to 1:00:00 AM.
- On the first Sunday in April, the time springs forward from 2:00:00 AM to 3:00:00 AM.

HF - Hour Format

7	6	5	4	3	2	1	0
-	-	-	-	-	-	HF	-

This bit selects the time-of-day and alarm hour format:

1 = 24-hour format

0 = 12-hour format

DF - Data Format

7	6	5	4	3	2	1	0
-	-	-	-	-	DF	-	-

This bit selects the numeric format in which the time, alarm, and calendar bytes are represented:

1 = Binary

0 = BCD

SQWE - Square Wave Enable

7	6	5	4	3	2	1	0
-	-	-	-	SQWE	-	-	-

This bit enables the square wave output:

1 = Enabled

0 = Disabled and held low

UIE - Update Cycle Interrupt Enable

7	6	5	4	3	2	1	0
-	-	-	UIE	-	-	-	-

This bit enables an interrupt request due to an update ended interrupt event:

1 = Enabled

0 = Disabled

The UIE bit is automatically cleared when the UTI bit equals 1.

AIE - Alarm Interrupt Enable

7	6	5	4	3	2	1	0
-	-	AIE	-	-	-	-	-

This bit enables an interrupt request due to an alarm interrupt event:

1 = Enabled

0 = Disabled

PIE - Periodic Interrupt Enable

7	6	5	4	3	2	1	0
-	PIE	-	-	-	-	-	-

This bit enables an interrupt request due to a periodic interrupt event:

1 = Enabled

0 = Disabled

UTI - Update Transfer Inhibit

7	6	5	4	3	2	1	0
UTI	-	-	-	-	-	-	-

This bit inhibits the transfer of RTC bytes to the user buffer:

1 = Inhibits transfer and clears UIE

0 = Allows transfer

Register C

Register C Bits							
7	6	5	4	3	2	1	0
INTF	PF	AF	UF	0	0	0	0

Register C is the read-only event status register.

Bits 0–3 - Unused Bits

7	6	5	4	3	2	1	0
-	-	-	-	0	0	0	0

These bits are always set to 0.

UF - Update-Event Flag

7	6	5	4	3	2	1	0
-	-	-	UF	-	-	-	-

This bit is set to a 1 at the end of the update cycle. Reading register C clears this bit.

AF - Alarm Event Flag

7	6	5	4	3	2	1	0
-	-	AF	-	-	-	-	-

This bit is set to a 1 when an alarm event occurs. Reading register C clears this bit.

PF - Periodic Event Flag

7	6	5	4	3	2	1	0
-	PF	-	-	-	-	-	-

This bit is set to a 1 every t_{PI} time, where t_{PI} is the time period selected by the settings of RS0–RS3 in register A. Reading register C clears this bit.

INTF - Interrupt Request Flag

7	6	5	4	3	2	1	0
INTF	-	-	-	-	-	-	-

This flag is set to a 1 when any of the following is true:

AIE = 1 and AF = 1

PIE = 1 and PF = 1

UIE = 1 and UF = 1

Reading register C clears this bit.

Register D

Register D Bits							
7	6	5	4	3	2	1	0
VRT	0	0	0	0	0	0	0

Register D is the read-only data integrity status register.

Bits 0–6 - Unused Bits

7	6	5	4	3	2	1	0
-	0	0	0	0	0	0	0

These bits are always set to 0.

VRT - Valid RAM and Time

7	6	5	4	3	2	1	0
VRT	-	-	-	-	-	-	-

1 = Valid backup energy source

0 = Backup energy source is depleted

When the backup energy source is depleted (VRT = 0), data integrity of the RTC and storage registers is not guaranteed.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IL}	Input low voltage	-0.3	-	0.8	V
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V

Note: Typical values indicate operation at T_A = 25°.

DC Electrical Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	AD_0–AD_7, $\overline{INT}$ and SQW in high impedance
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current	-	7	15	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
V_{SO}	Supply switch-over voltage	-	3.0	-	V	
V_{PFD}	Power-fail-detect voltage	4.30	4.37	4.45	V	
I_{RCL}	Input current when $\overline{RCL}$ = V_{SS}	-	-	550	µA	Internal 20K pull-up (bq3287A only)
I_{MOTH}	Input current when MOT = V_{CC}	-	-	-550	µA	Internal 20K pull-down

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	7	pF	V_{OUT} = 0V
C_{IN}	Input capacitance	-	-	5	pF	V_{IN} = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

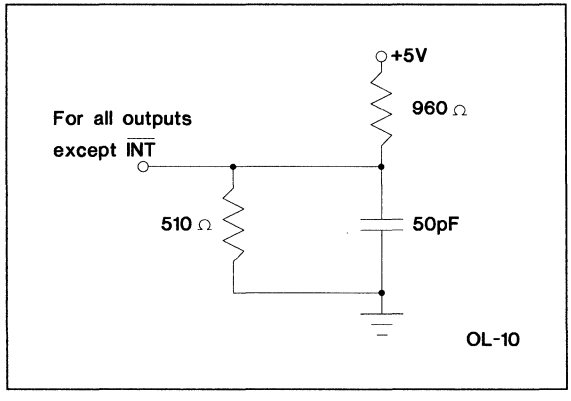


Figure 4. Output Load A

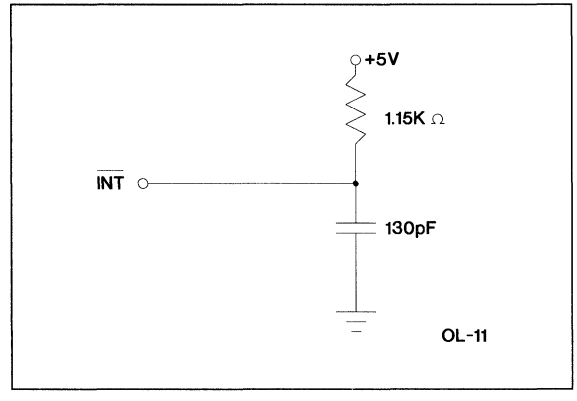


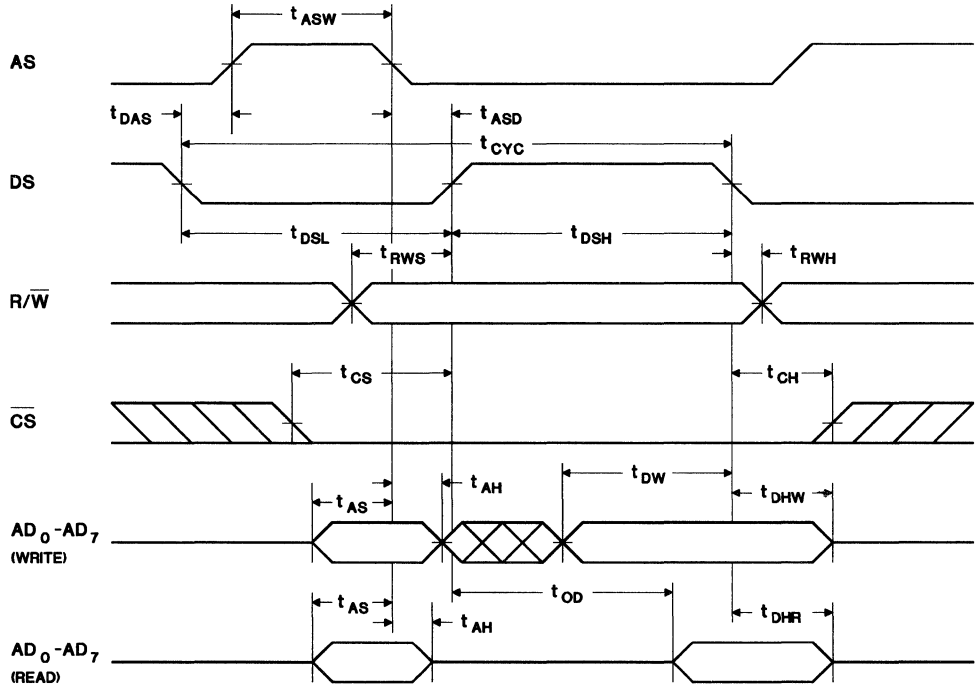
Figure 5. Output Load B

Read/Write Timing (TA = 0 to 70°C, VCC = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{CYC}	Cycle time	160	-	-	ns
t_{DSL}	DS low or $\overline{RD}/\overline{WR}$ high time	80	-	-	ns
t_{DSH}	DS high or $\overline{RD}/\overline{WR}$ low time	55	-	-	ns
t_{RWH}	R/$\overline{W}$ hold time	0	-	-	ns
t_{RWS}	R/$\overline{W}$ setup time	10	-	-	ns
t_{CS}	Chip select setup time	5	-	-	ns
t_{CH}	Chip select hold time	0	-	-	ns
t_{DHR}	Read data hold time	0	-	25	ns
t_{DHW}	Write data hold time	0	-	-	ns
t_{AS}	Address setup time	20	-	-	ns
t_{AH}	Address hold time	5	-	-	ns
t_{DAS}	Delay time, DS to AS rise	10	-	-	ns
t_{ASW}	Pulse width, AS high	30	-	-	ns
t_{ASD}	Delay time, AS to DS rise ($\overline{RD}/\overline{WR}$ fall)	35	-	-	ns
t_{OD}	Output data delay time time from DS rise ($\overline{RD}$ fall)	-	-	35	ns
t_{DW}	Write data setup time	30	-	-	ns

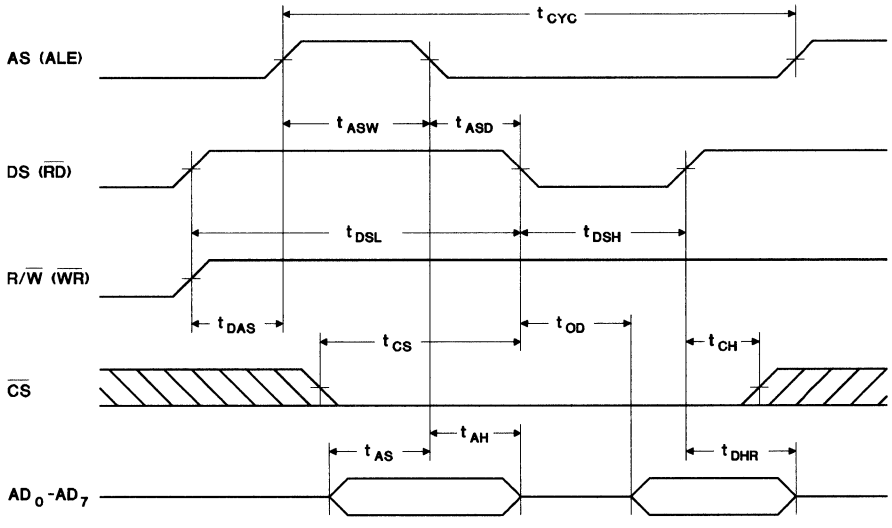
5

Motorola Bus Read/Write Timing



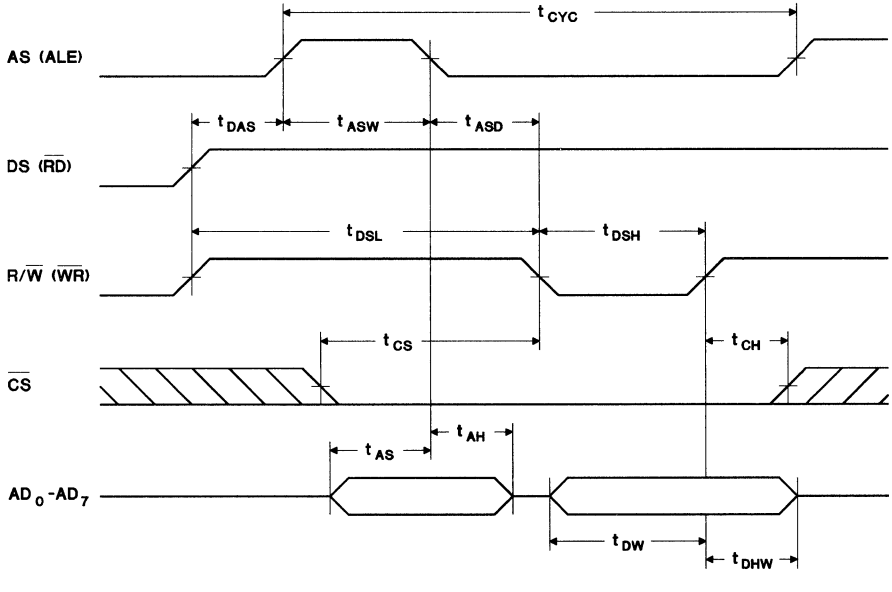
RC-4

Intel Bus Read Timing



RC-5

Intel Bus Write Timing



WC-5

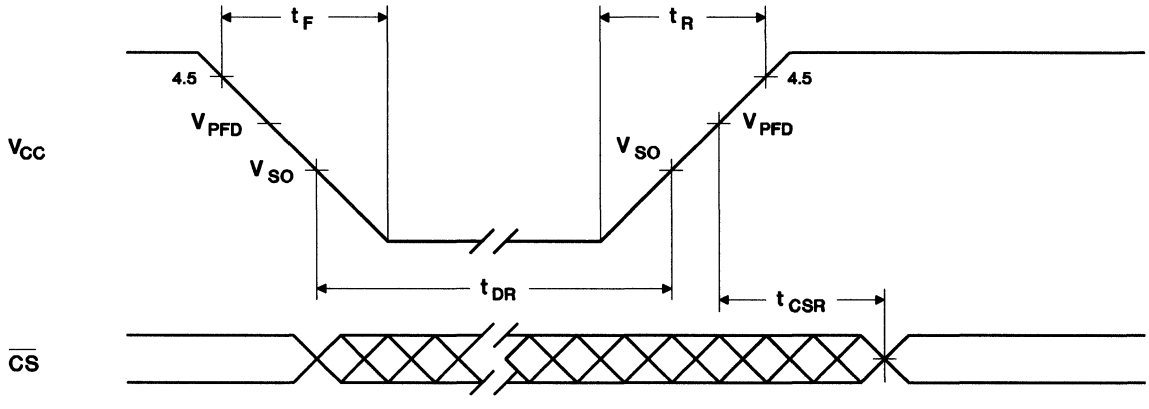
Power-Down/Power-Up Timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.5V to 0V	300	-	-	µs	
t_R	V_{CC} slew from 0V to 4.5V	100	-	-	µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20	-	200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention and timekeeping time between charges	10	-	-	years	T_A = 25°C

Note: Clock accuracy is better than ± 1 minute per month at 25°C for the period of t_{DR}.

Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

Power-Down/Power-Up Timing

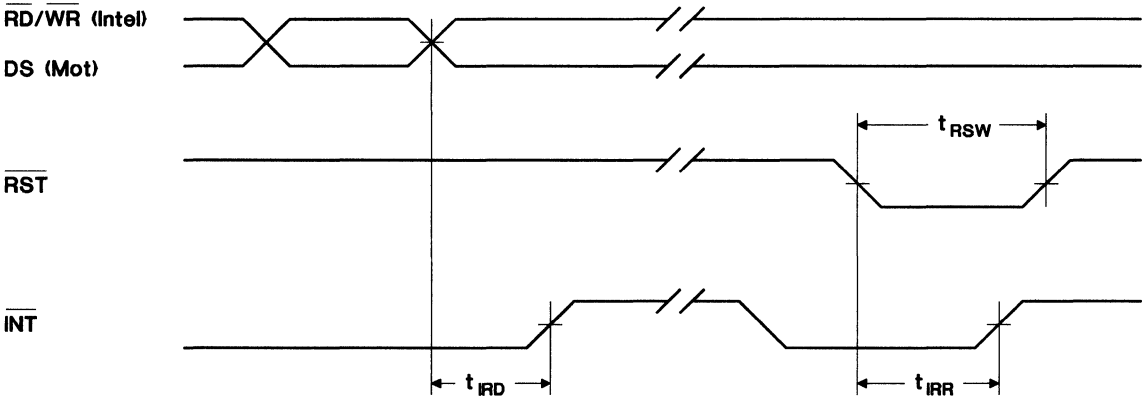


PD-4

Interrupt Delay Timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{RSW}	Reset pulse width	5	-	-	µs
t_{IRR}	$\overline{INT}$ release from $\overline{RST}$	-	-	2	µs
t_{IRD}	$\overline{INT}$ release from DS	-	-	2	µs

Interrupt Delay Timing



INT-1

Ordering Information

bq3287 MT

Package Option:
MT = T-type module

RAM Clear Option:
A = RAM clear on pin 21
no mark = No connect on pin 21

Device:
bq3287 Real-Time Clock Module

Notes

BENCHMARQ

Advance Information **bq3385**

Real-Time Clock (RTC) With 4Kx8 RAM

Features

- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- 160 ns cycle time allows fast bus operation
- Less than 1.0 µA load under battery operation
- 14 bytes for clock/calendar and control
- 50 bytes of general nonvolatile storage
- Additional 4K x 8 nonvolatile SRAM, accessed using RAM control pins
- Programmable square wave output
- Calendar in days, day of the week, months, and years, with automatic leap-year adjustment
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- BCD or binary format for clock and calendar data
- Three individually maskable interrupt event flags:
  - Periodic rates from 122 µs to 500 ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle
- 24-pin plastic DIP or SOIC and 28-pin PLCC

General Description

The CMOS bq3385 is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. Other features of the bq3385 include three maskable interrupt sources, square wave output, 50 bytes of general nonvolatile storage, and an additional 4K x 8 of user-programmable nonvolatile SRAM.

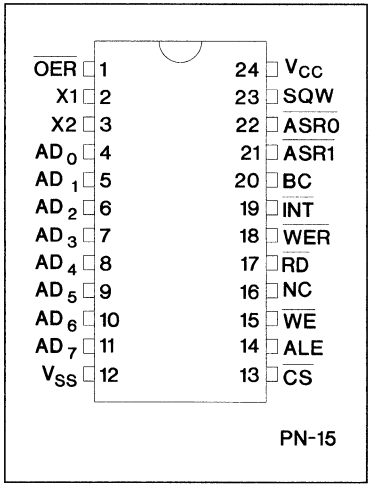
The bq3385 write-protects the clock, calendar, storage registers, and RAM during power failure. An external backup battery then maintains data and operates the clock and calendar.

The bq3385 is a fully compatible real-time clock for IBM AT-compatible computers and other applications. The only external components are a 32.768 KHz crystal and a backup battery.

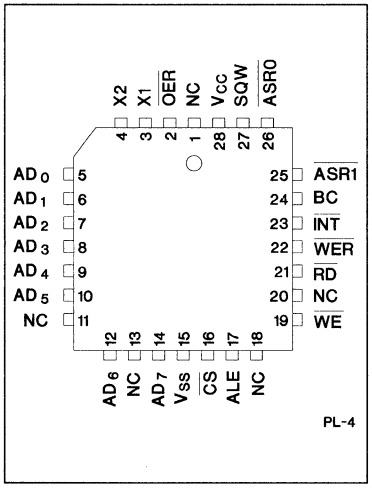
5

Pin Connections

24-Pin DIP or SOIC



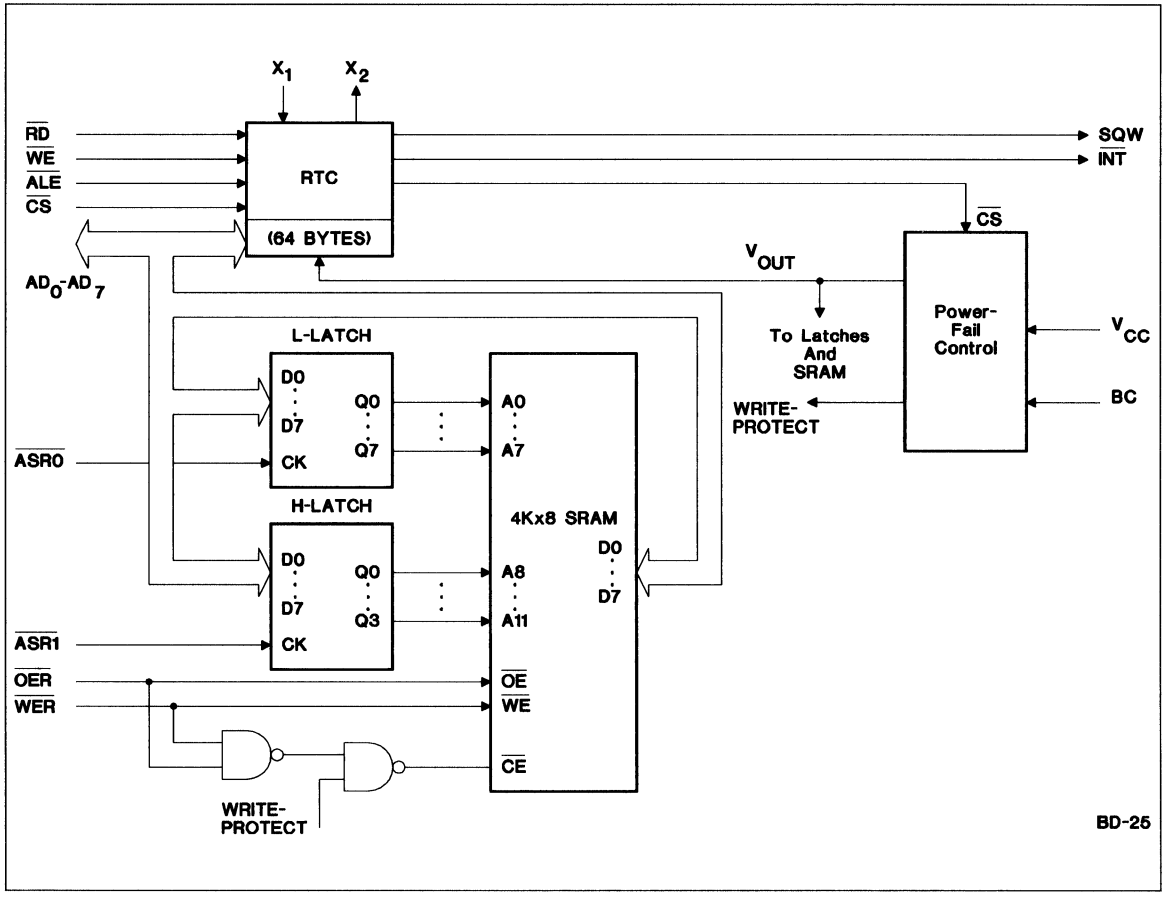
28-Pin PLCC



Pin Names

AD0–AD7	Multiplexed address/data input/output
$\overline{CS}$	RTC chip select input
ALE	RTC address strobe input
$\overline{RD}$	RTC read enable input
$\overline{WE}$	RTC write enable input
$\overline{INT}$	Interrupt request output
SQW	Square wave output
BC	Backup cell input
X1, X2	Crystal inputs
$\overline{OER}$	RAM output enable
$\overline{WER}$	RAM write enable
$\overline{ASR0}$–$\overline{ASR1}$	RAM address strobe
NC	No connect
VCC	+5V supply
VSS	Ground

Block Diagram



BENCHMARQ

Advance Information **bq3387**

Real-Time Clock Module With 4Kx8 RAM

Features

- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- 160 ns cycle time allows fast bus operation
- 14 bytes for clock/calendar and control
- 50 bytes of general nonvolatile storage
- Additional 4K x 8 nonvolatile SRAM, accessed using RAM control pins
- Integral lithium cell and crystal
- Calendar in days, day of the week, months, and years, with automatic leap-year adjustment
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- BCD or binary format for clock and calendar data
- Better than one minute per month clock accuracy
- Programmable square wave output
- Three individually maskable interrupt event flags
- 24-pin plastic clock module

General Description

The CMOS bq3387 is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and integrated battery operation. Other features of the bq3387 include three maskable interrupt sources, square wave output, 50 bytes of general nonvolatile storage, and an additional 4K x 8 of user-programmable nonvolatile SRAM.

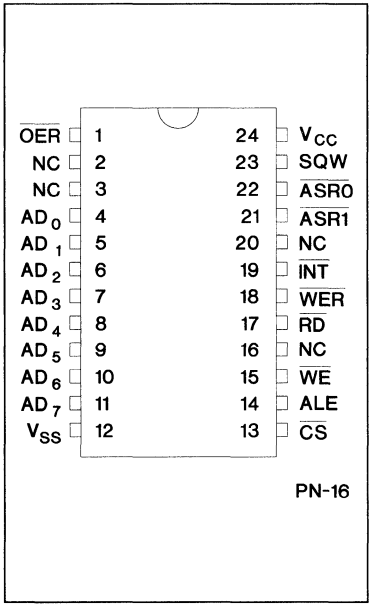
The bq3387 write-protects the clock, calendar, storage registers, and RAM during power failure. An internal lithium backup battery then maintains data and operates the clock and calendar.

The bq3387 is a fully compatible real-time clock for IBM AT-compatible computers and other applications.

As shipped from Benchmarq, the backup cell is electrically isolated from the memory. Following the first application of V_{CC}, this isolation is broken, and the backup cell provides data retention on subsequent power-downs.

5

Pin Connections

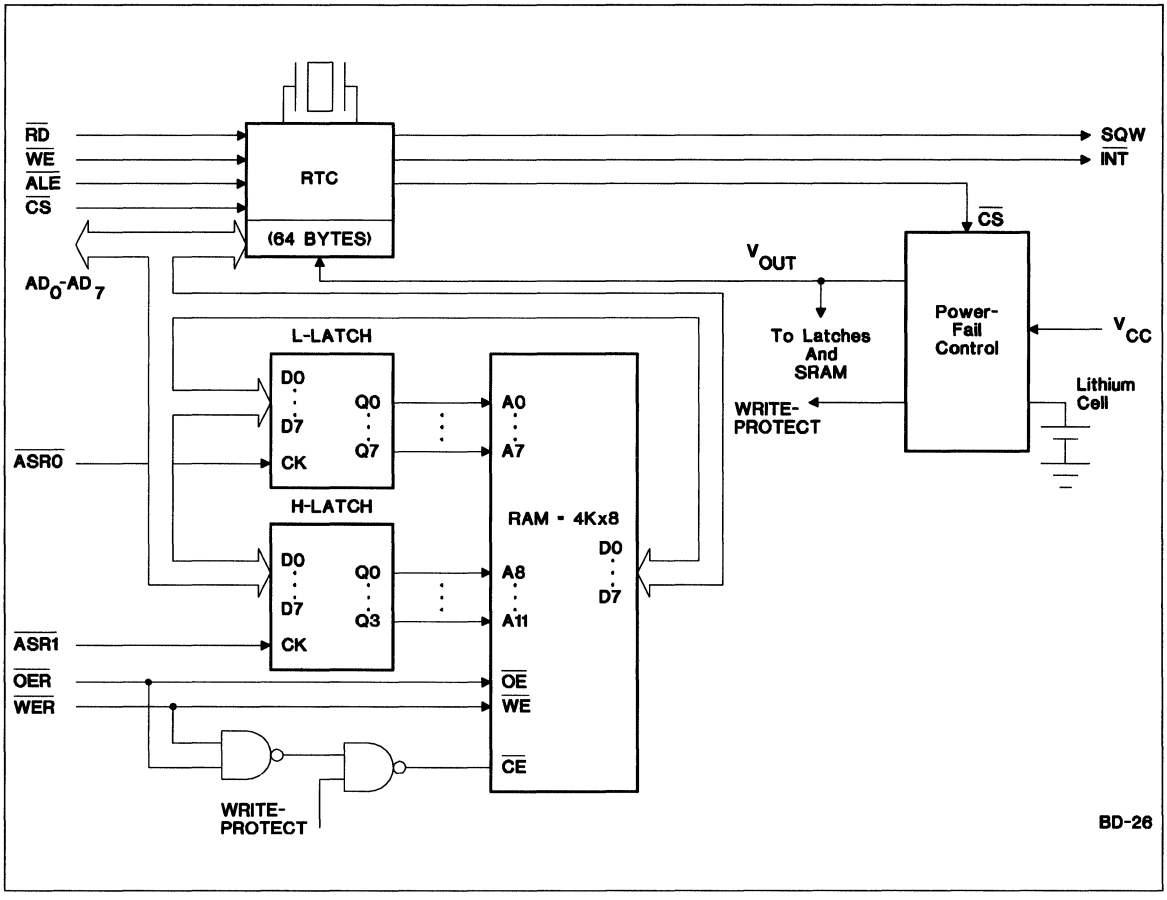


PN-16

Pin Names

AD_0–AD_7	Multiplexed address/data input/output
$\overline{CS}$	RTC chip select input
ALE	RTC address strobe input
$\overline{RD}$	RTC read enable input
$\overline{WE}$	RTC write enable input
$\overline{INT}$	Interrupt request output
SQW	Square wave output
$\overline{OER}$	RAM output enable
$\overline{WER}$	RAM write enable
$\overline{ASR0}$–$\overline{ASR1}$	RAM address strobe
NC	No connect
V_{CC}	+5V supply
V_{SS}	Ground

Block Diagram



BENCHMARQ

Advance Information **bq3485**

Real-Time Clock (RTC) With 8Kx8 RAM

Features

- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Density upgrade of the bq3385R
- 160 ns cycle time allows fast bus operation
- Less than 1.0 µA load under battery operation
- 14 bytes for clock/calendar and control
- 50 bytes of general nonvolatile storage
- Additional 8K x 8 nonvolatile SRAM, accessed using RAM control pins
- 3 volt battery-backup input
- Programmable square wave output
- Calendar in days, day of the week, months, and years, with automatic leap-year adjustment
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- BCD or binary format for clock and calendar data
- Three individually maskable interrupt event flags:
  - Periodic rates from 122 µs to 500 ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle
- 24-pin plastic DIP or SOIC and 28-pin PLCC

General Description

The CMOS bq3485 is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. Other features of the bq3485 include three maskable interrupt sources, square wave output, 50 bytes of general nonvolatile storage, and an additional 8K x 8 of user-programmable nonvolatile SRAM.

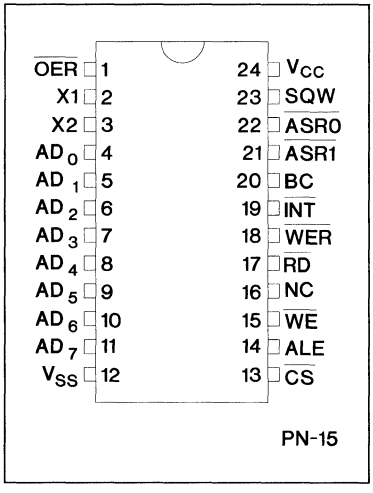
The bq3485 write-protects the clock, calendar, storage registers, and RAM during power failure. A back-up battery then maintains data and operates the clock and calendar.

The bq3485 is a fully compatible real-time clock for IBM AT-compatible computers and other applications. The only external components are a 32.768 KHz crystal and a backup battery.

5

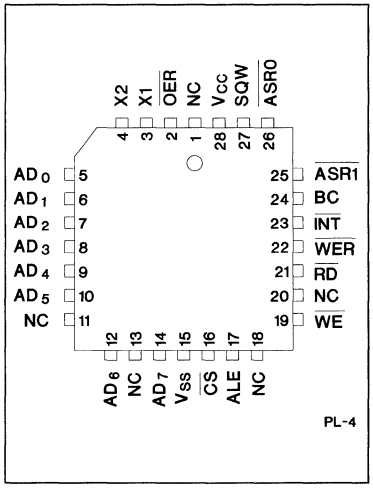
Pin Connections

24-Pin DIP or SOIC



PN-15

28-Pin PLCC

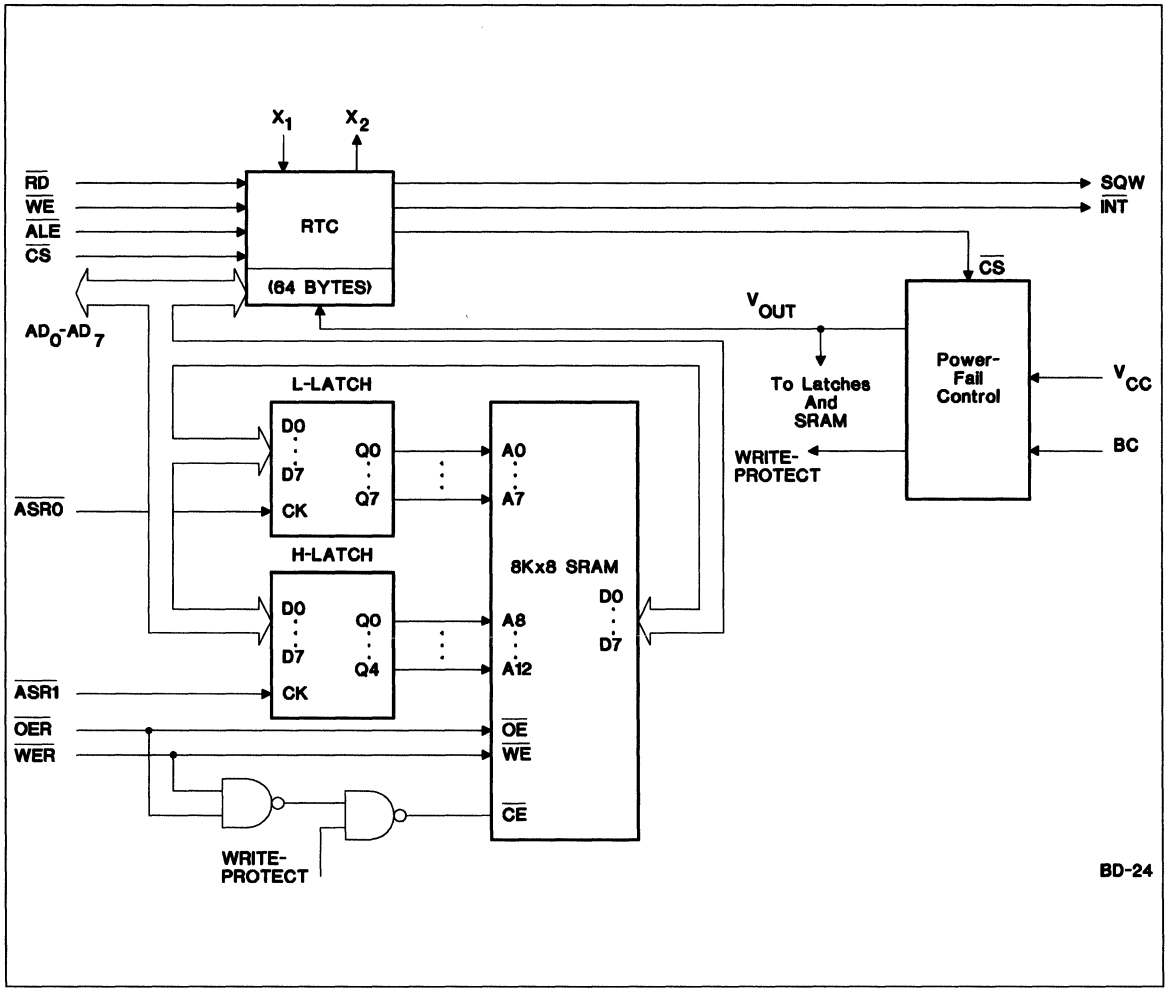


PL-4

Pin Names

AD_0–AD_7	Multiplexed address/data input/output
$\overline{CS}$	RTC chip select input
ALE	RTC address strobe input
$\overline{RD}$	RTC read enable input
$\overline{WE}$	RTC write enable input
$\overline{INT}$	Interrupt request output
SQW	Square wave output
BC	Backup cell input
X1, X2	Crystal inputs
$\overline{OER}$	RAM output enable
$\overline{WER}$	RAM write enable
$\overline{ASR0}$–$\overline{ASR1}$	RAM address strobe
NC	No connect
V_{CC}	+5V supply
V_{SS}	Ground

Block Diagram



Real-Time Clock Module With 8Kx8 RAM

Features

- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Density upgrade of the bq3387
- 160 ns cycle time allows fast bus operation
- 14 bytes for clock/calendar and control
- 50 bytes of general nonvolatile storage
- Additional 8K x 8 nonvolatile SRAM, accessed using RAM control pins
- Integral lithium cell and crystal
- Calendar in days, day of the week, months, and years, with automatic leap-year adjustment
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- BCD or binary format for clock and calendar data
- Better than one minute per month accuracy
- Programmable square wave output
- Three individually maskable interrupt event flags
- 24-pin plastic clock module

General Description

The CMOS bq3487 is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and integrated battery operation. Other features of the bq3487 include three maskable interrupt sources, square wave output, 50 bytes of general nonvolatile storage, and an additional 8K x 8 of user-programmable nonvolatile SRAM.

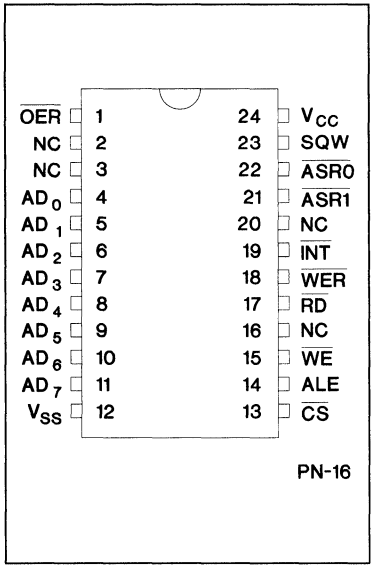
The bq3487 write-protects the clock, calendar, storage registers, and RAM during power failure. An internal backup battery then maintains data and operates the clock and calendar.

The bq3487 is a fully compatible real-time clock for IBM AT-compatible computers and other applications.

As shipped from Benchmarq, the backup cell is electrically isolated from the memory. Following the first application of V_{CC}, this isolation is broken, and the backup cell provides data retention on subsequent power-downs.

5

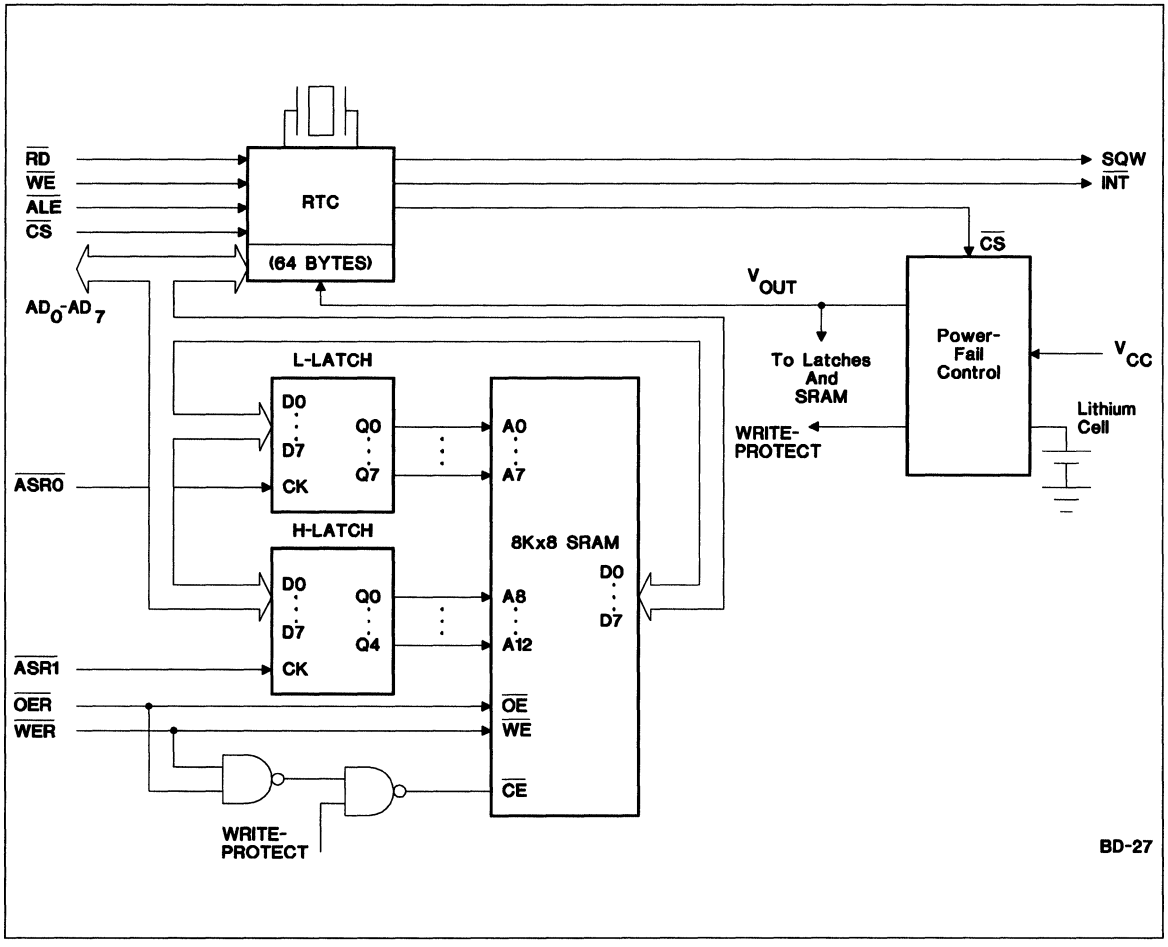
Pin Connections



Pin Names

AD_0–AD_7	Multiplexed address/data input/output
$\overline{CS}$	RTC chip select input
ALE	RTC address strobe input
$\overline{RD}$	RTC read enable input
$\overline{WE}$	RTC write enable input
$\overline{INT}$	Interrupt request output
SQW	Square wave output
$\overline{OER}$	RAM output enable
$\overline{WER}$	RAM write enable
$\overline{ASR0}$–$\overline{ASR1}$	RAM address strobe
NC	No connect
V_{CC}	+5V supply
V_{SS}	Ground

Block Diagram



bq4010/bq4010Y

8Kx8 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Industry-standard 28-pin 8K x 8 pinout
- Conventional SRAM operation; unlimited write cycles
- 10-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

The CMOS bq4010 is a nonvolatile 65,536-bit static RAM organized as 8,192 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

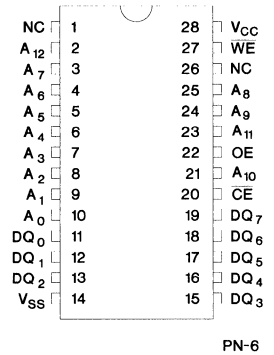
The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4010 uses an extremely low standby current CMOS SRAM, coupled with a small lithium coin cell to provide nonvolatility without long write cycle times and the write cycle limitations associated with EEPROM.

The bq4010 requires no external circuitry and is socket-compatible with industry-standard SRAMs and most EPROMs and EEPROMs.

Pin Connections

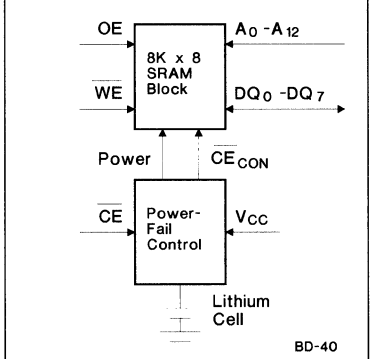


PN-6

Pin Names

A_0 –A_{12}	Address inputs
DQ_0–DQ_7	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
V_{CC}	+5 volt supply input
V_{SS}	Ground

Block Diagram



BD-40

Selection Guide

Part Number	Minimum Access Time (ns)	Negative Supply Tolerance	Part Number	Minimum Access Time (ns)	Negative Supply Tolerance
bq4010 -85	85	-5%	bq4010Y -85	85	-10%
bq4010 -150	150	-5%	bq4010Y -150	150	-10%
bq4010 -200	200	-5%	bq4010Y -200	200	-10%

Functional Description

When power is valid, the bq4010 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4010 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4010 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4010Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120 ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cell used by the bq4010 has an extremely long shelf life and provides data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cell is electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup cell provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4010Y
		4.75	5.0	5.5	V	bq4010
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = 0 to 70°C, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current	-	4	7	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current	-	2.5	4	mA	$\overline{CE} \geq V_{CC}$ - 0.2V, $0V \leq V_{IN} \leq 0.2V$, or $V_{IN} \geq V_{CC}$ - 0.2V
I_{CC}	Operating supply current	-	65	75	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4010
		4.30	4.37	4.50	V	bq4010Y
V_{SO}	Supply switch-over voltage	-	3	-	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC} = 3V.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	10	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	10	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

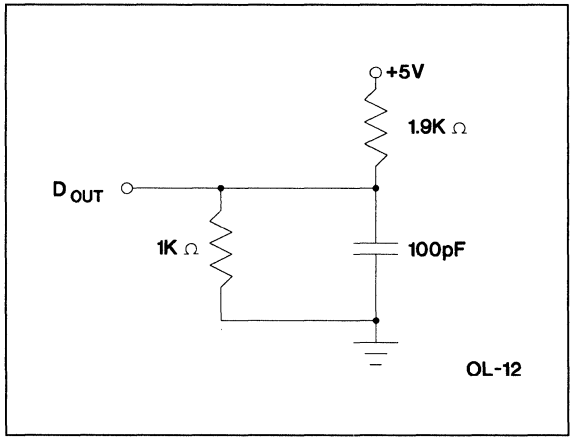


Figure 1. Output Load A

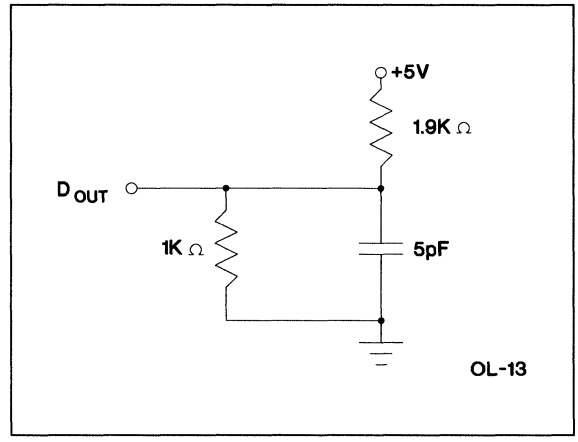
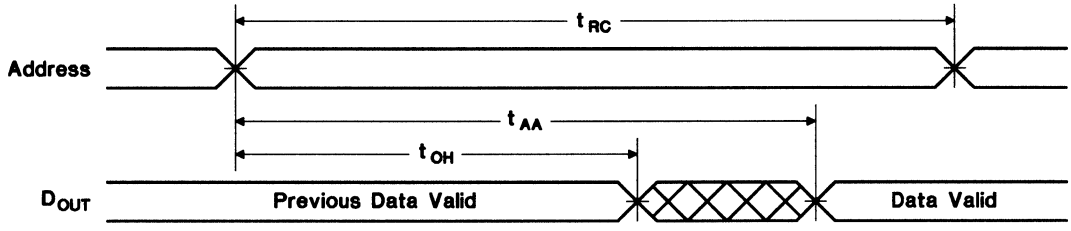


Figure 2. Output Load B

Read Cycle (T_A = 0 to 70°C, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

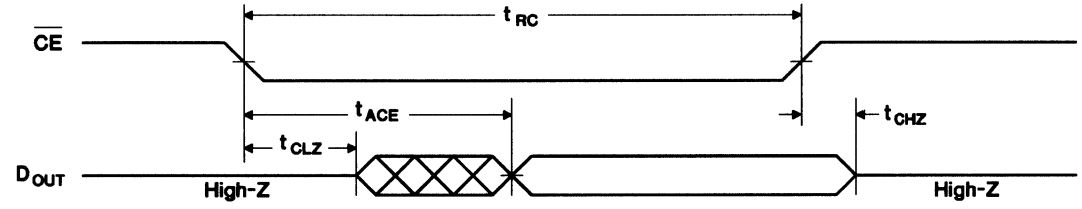
Symbol	Parameter	-85		-150		-200		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	85	-	150	-	200	-	ns	
t_{AA}	Address access time	-	85	-	150	-	200	ns	Output load A
t_{ACE}	Chip enable access time	-	85	-	150	-	200	ns	Output load A
t_{OE}	Output enable to output valid	-	45	-	70	-	90	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	10	-	10	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	5	-	5	-	5	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	40	0	60	0	70	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	30	0	50	0	70	ns	Output load B
t_{OH}	Output hold from address change	10	-	10	-	10	-	ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



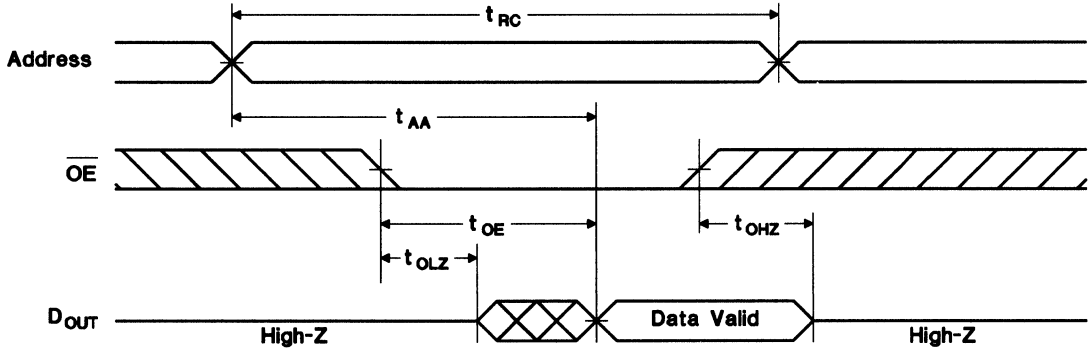
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



RC-3

Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE}$ = $\overline{OE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Device is continuously selected: $\overline{CE}$ = V_{IL}.

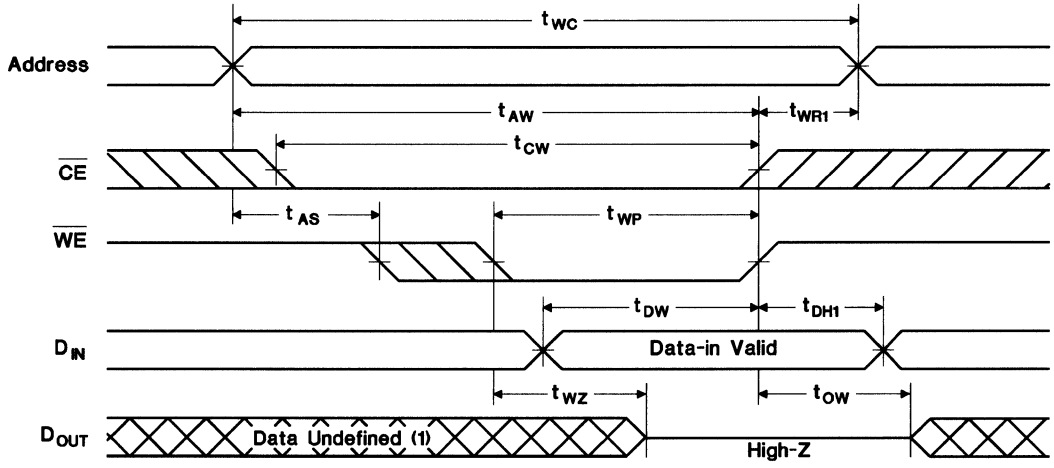
Write Cycle (T_A = 0 to 70°C, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	-85		-150		-200		Units	Conditions/ Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	85	-	150	-	200	-	ns	
t_{CW}	Chip enable to end of write	85	-	100	-	150	-	ns	(1)
t_{AW}	Address valid to end of write	75	-	90	-	150	-	ns	(1)
t_{AS}	Address setup time	0	-	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	75	-	90	-	130	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	5	-	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	15	-	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	35	-	50	-	70	-	ns	Measured from first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	0	-	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	10	-	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	30	0	50	0	70	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	5	-	5	-	5	-	ns	I/O pins are in output state. (5)

Notes:

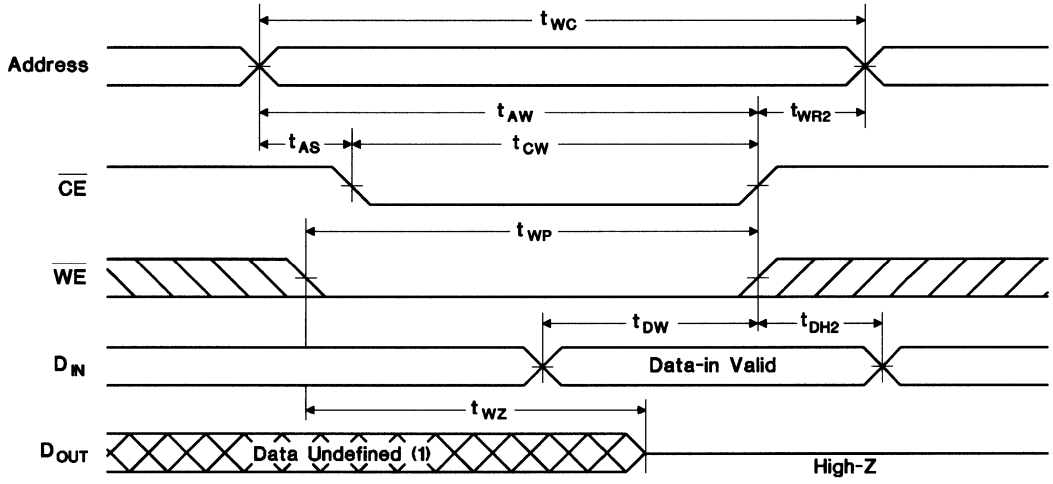
1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



WC-3

Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



WC-4

Notes:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

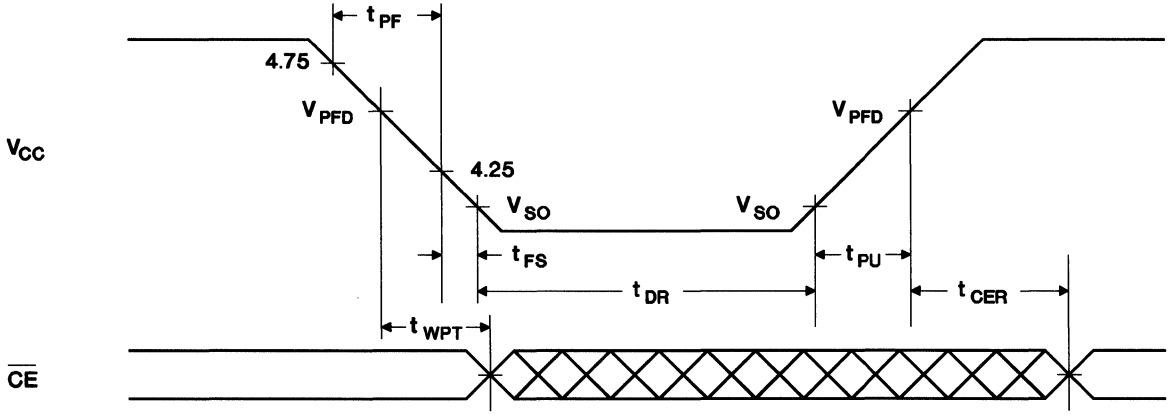
Power-Down/Power-Up Cycle (T_A = 0 to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10	-	-	years	T_A = 25°C. (2)
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Battery is disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

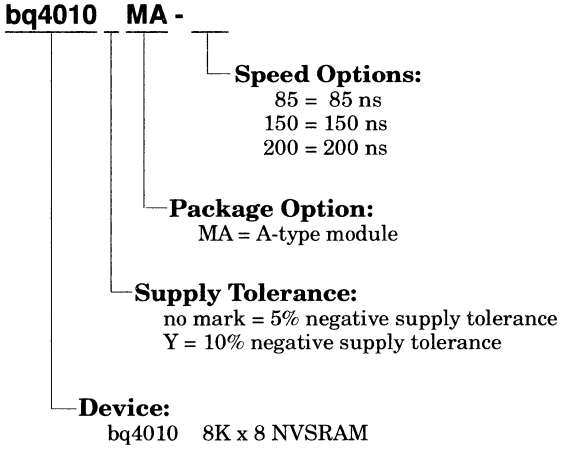
Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

Power-Down/Power-Up Timing



PD-B

Ordering Information



6

Notes

bq4011/bq4011Y

32Kx8 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Industry-standard 28-pin 32K x 8 pinout
- Conventional SRAM operation; unlimited write cycles
- 10-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

The CMOS bq4011 is a nonvolatile 262,144-bit static RAM organized as 32,768 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

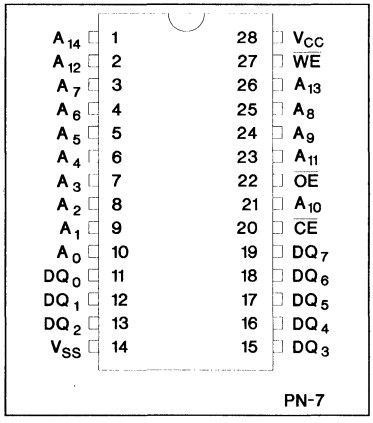
The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4011 uses an extremely low standby current CMOS SRAM, coupled with a small lithium coin cell to provide nonvolatility without long write cycle times and the write cycle limitations associated with EEPROM.

The bq4011 requires no external circuitry and is socket-compatible with industry-standard SRAMs and most EPROMs and EEPROMs.

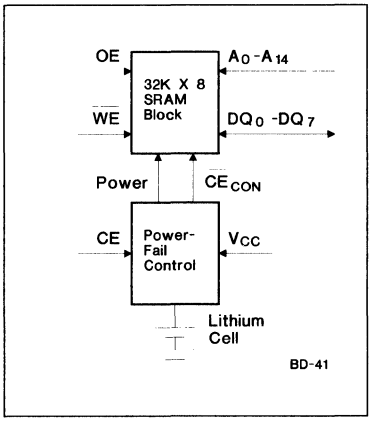
Pin Connections



Pin Names

$A_0 - A_{14}$	Address inputs
$DQ_0 - DQ_7$	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
V_{CC}	+5 volt supply input
V_{SS}	Ground

Block Diagram



Selection Guide

Part Number	Minimum Access Time (ns)	Negative Supply Tolerance	Part Number	Minimum Access Time (ns)	Negative Supply Tolerance
bq4011 -100	100	-5%	bq4011Y -100	100	-10%
bq4011 -150	150	-5%	bq4011Y -150	150	-10%
bq4011 -200	200	-5%	bq4011Y -200	200	-10%

Functional Description

When power is valid, the bq4011 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4011 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4011 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4011Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120 ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cell used by the bq4011 has an extremely long shelf life and provides data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cell is electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup cell provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4011Y
		4.75	5.0	5.5	V	bq4011
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = 0 to 70°C, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current	-	4	7	mA	$\overline{CE}$ = V_{IH}
I_{SB2}	Standby supply current	-	2.5	4	mA	$\overline{CE}$ ≥ V_{CC} - 0.2V, 0V ≤ V_{IN} ≤ 0.2V, or V_{IN} ≥ V_{CC} - 0.2V
I_{CC}	Operating supply current	-	55	75	mA	Min. cycle, duty = 100%, $\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4011
		4.30	4.37	4.50	V	bq4011Y
V_{SO}	Supply switch-over voltage	-	3	-	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC} = 3V.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	10	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	10	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

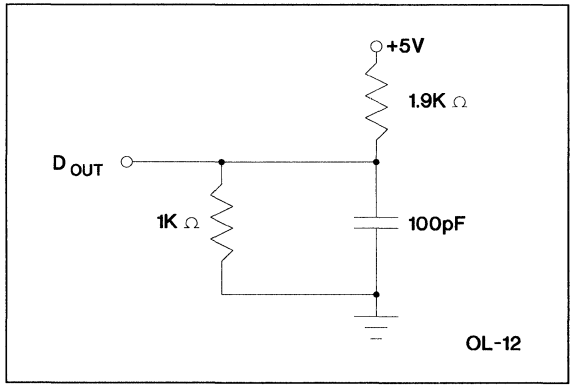


Figure 1. Output Load A

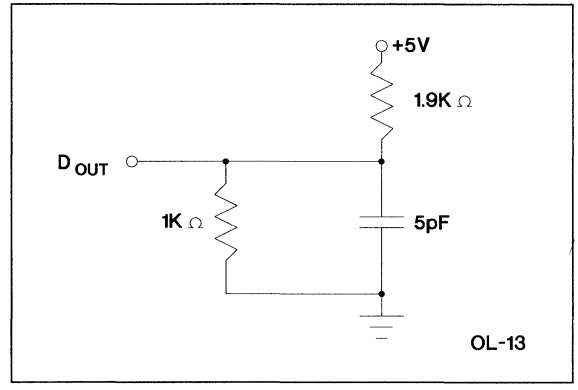
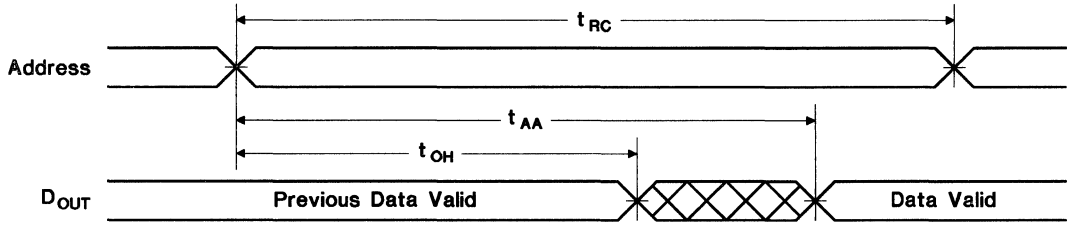


Figure 2. Output Load B

Read Cycle (T_A = 0 to 70°C, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

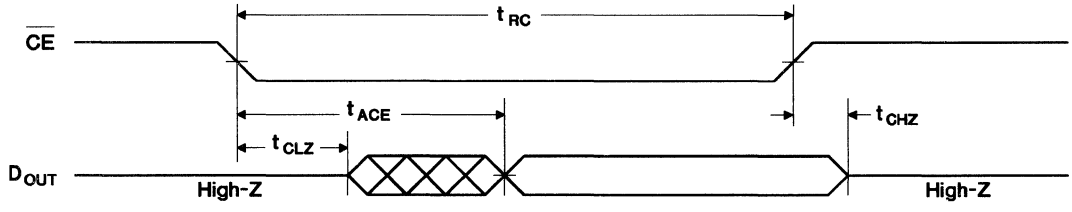
Symbol	Parameter	-100		-150		-200		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	100	-	150	-	200	-	ns	
t_{AA}	Address access time	-	100	-	150	-	200	ns	Output load A
t_{ACE}	Chip enable access time	-	100	-	150	-	200	ns	Output load A
t_{OE}	Output enable to output valid	-	50	-	70	-	90	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	10	-	10	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	5	-	5	-	5	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	40	0	60	0	70	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	35	0	50	0	70	ns	Output load B
t_{OH}	Output hold from address change	10	-	10	-	10	-	ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



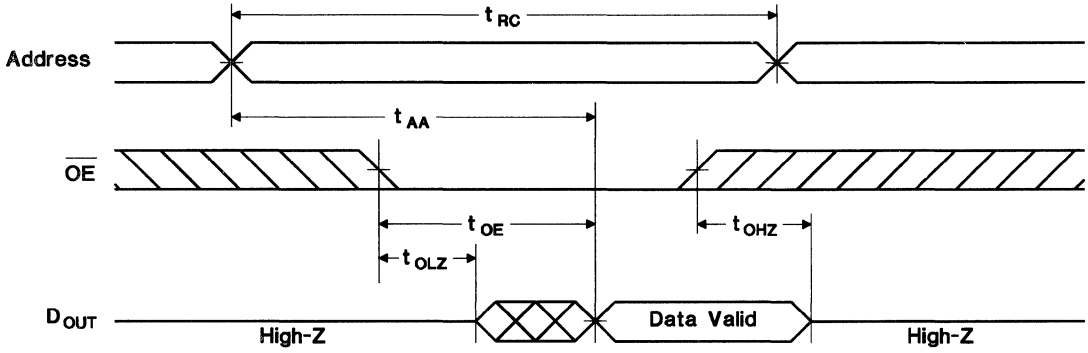
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



RC-3

Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

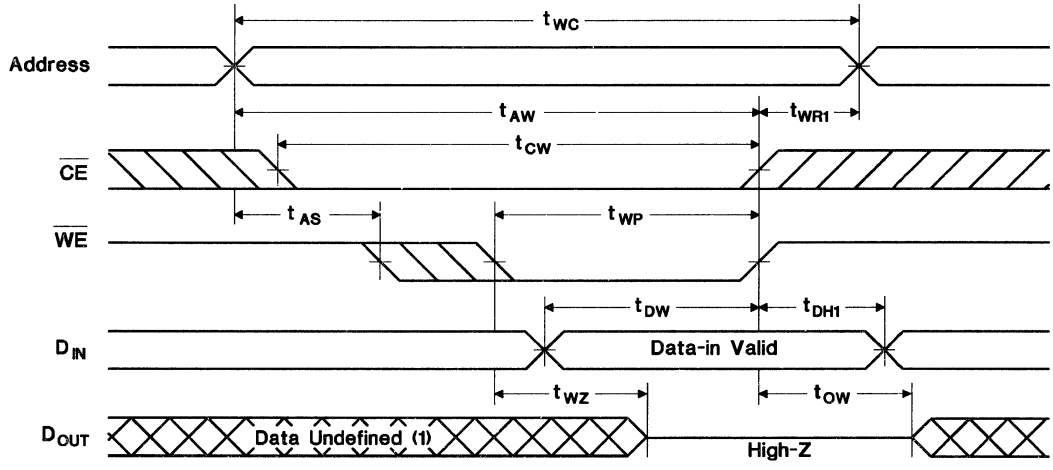
Write Cycle (TA = 0 to 70°C, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	-100		-150		-200		Units	Conditions/ Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	100	-	150	-	200	-	ns	
t_{CW}	Chip enable to end of write	90	-	100	-	150	-	ns	(1)
t_{AW}	Address valid to end of write	80	-	90	-	150	-	ns	(1)
t_{AS}	Address setup time	0	-	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	75	-	90	-	130	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	5	-	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	15	-	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	40	-	50	-	70	-	ns	Measured from first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	0	-	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	10	-	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle.(4)
t_{WZ}	Write enabled to output in high Z	0	35	0	50	0	70	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	5	-	5	-	5	-	ns	I/O pins are in output state. (5)

Notes:

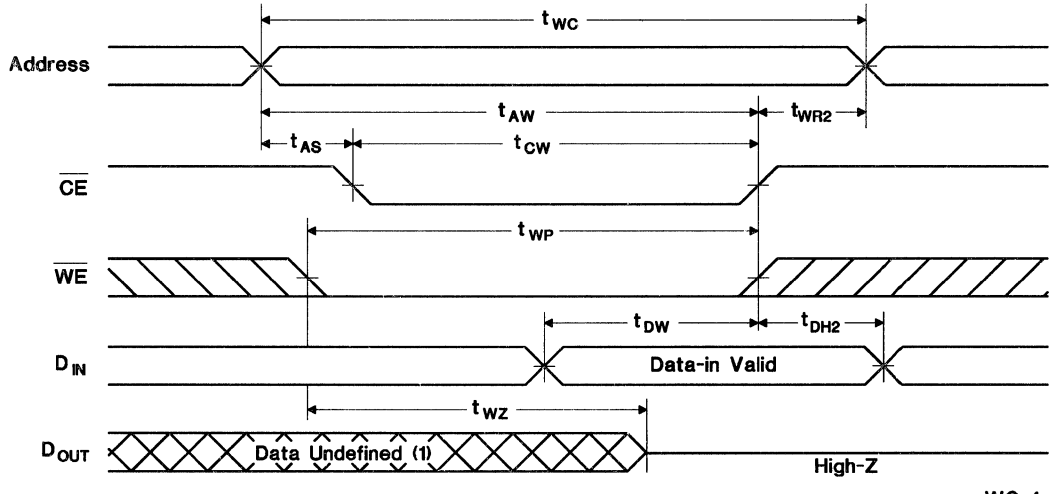
1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



WC-3

Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



WC-4

Notes:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

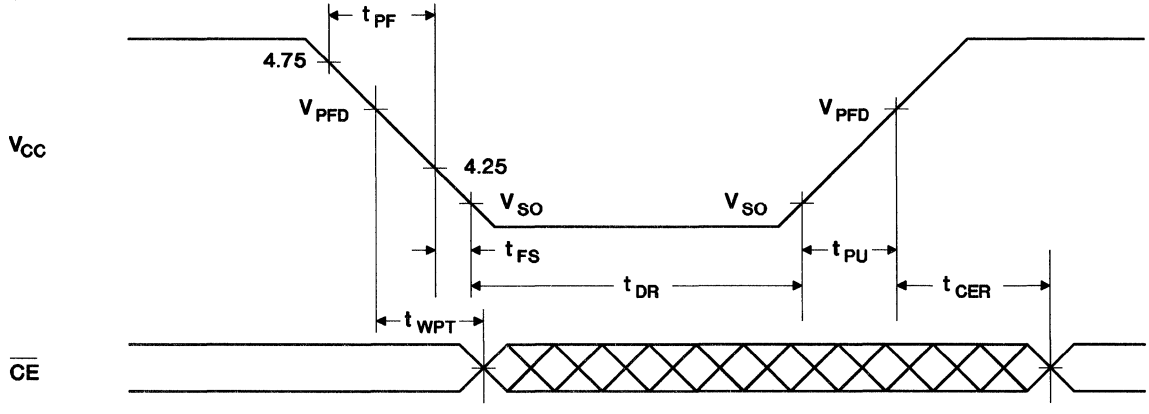
Power-Down/Power-Up Cycle (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10	-	-	years	T_A = 25°C (2)
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Battery is disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

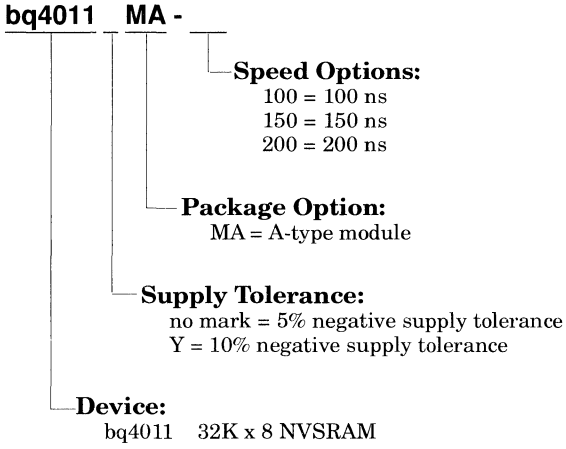
Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

Power-Down/Power-Up Timing



PD-B

Ordering Information



6

Notes

bq4011H/bq4011HY

32Kx8 Nonvolatile Fast SRAM

Features

- Data retention in the absence of power
- Access/cycle times of 35 and 45 ns
- Automatic write-protection during power-up/power-down cycles
- Industry-standard 28-pin 32K x 8 pinout
- Conventional SRAM operation; unlimited write cycles
- 10-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

The CMOS bq4011H is a nonvolatile 262,144-bit fast static RAM organized as 32,768 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM. Access times as fast as 35 ns are available.

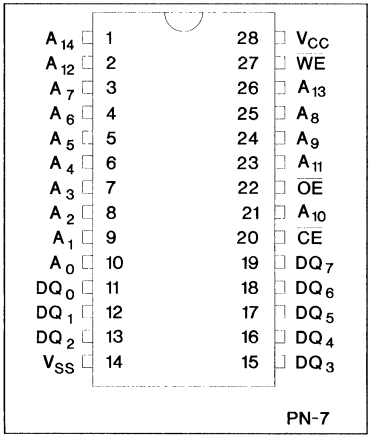
The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4011H uses an extremely low standby current CMOS SRAM, coupled with a small lithium coin cell to provide nonvolatility without long write cycle times and the write cycle limitations associated with EEPROM.

The bq4011H requires no external circuitry and is socket-compatible with industry-standard SRAMs and most EPROMs and EEPROMs.

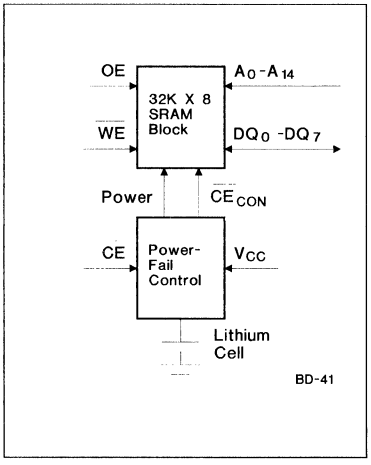
Pin Connections



Pin Names

A_0–A_{14}	Address inputs
DQ_0–DQ_7	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
V_{CC}	+5 volt supply input
V_{SS}	Ground

Block Diagram



Selection Guide

Part Number	Minimum Access Time (ns)	Negative Supply Tolerance	Part Number	Minimum Access Time (ns)	Negative Supply Tolerance
bq4011H -35	35	-5%	bq4011HY -35	35	-10%
bq4011H -45	45	-5%	bq4011HY -45	45	-10%

Functional Description

When power is valid, the bq4011H operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4011H acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4011H monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4011HY monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write protection continues for a time t_{CER} (120 ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cell used by the bq4011H has an extremely long shelf life and provides data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cell is electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup cell provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4011HY
		4.75	5.0	5.5	V	bq4011H
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = 0 to 70°C, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 2	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 2	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -4.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 8.0 mA
I_{SB1}	Standby supply current	-	18	34	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current	-	2.5	4	mA	$\overline{CE} \geq V_{CC}$ - 0.2V, $0V \leq V_{IN} \leq 0.2V$, or $V_{IN} \geq V_{CC}$ - 0.2V
I_{CC}	Operating supply current	-	65	125	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4011H
		4.30	4.37	4.50	V	bq4011HY
V_{SO}	Supply switch-over voltage	-	3	-	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC} = 3V.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	10	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	8	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

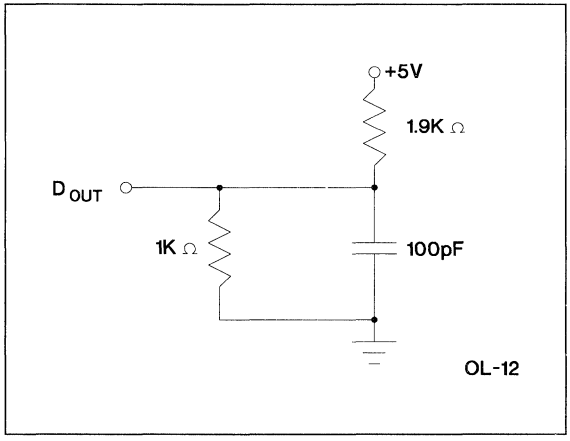


Figure 1. Output Load A

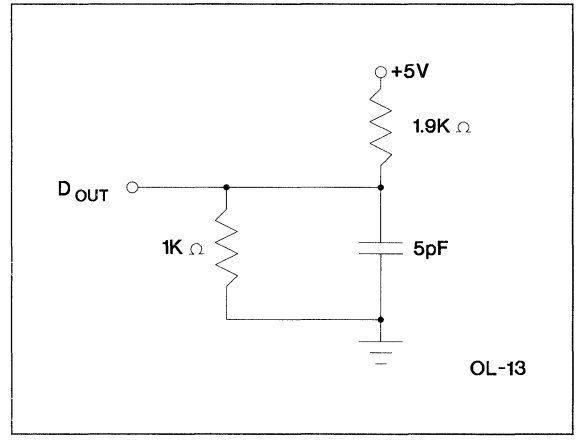
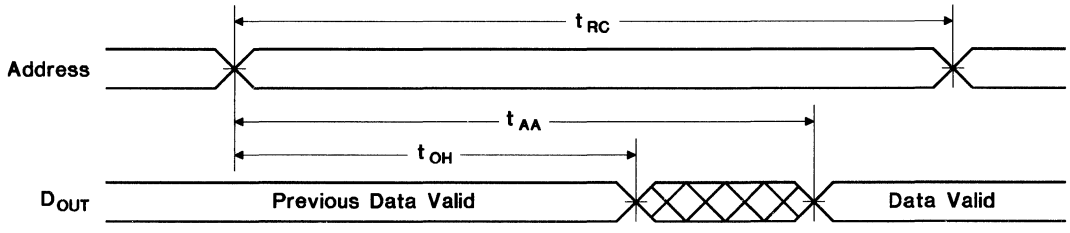


Figure 2. Output Load B

Read Cycle (TA = 0 to 70°C, VCCmin ≤ VCC ≤ VCCmax)

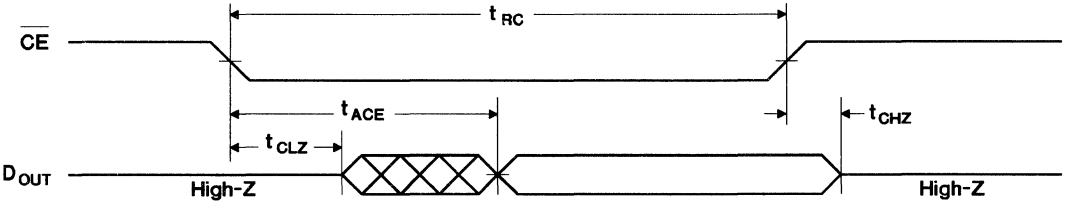
Symbol	Parameter	-35		-45		Unit	Conditions
		Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	35	-	45	-	ns	
t_{AA}	Address access time	-	35	-	45	ns	Output load A
t_{ACE}	Chip enable access time	-	35	-	45	ns	Output load A
t_{OE}	Output enable to output valid	-	12	-	15	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	0	-	0	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	22	0	25	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	12	0	15	ns	Output load B
t_{OH}	Output hold from address change	5	-	5	-	ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



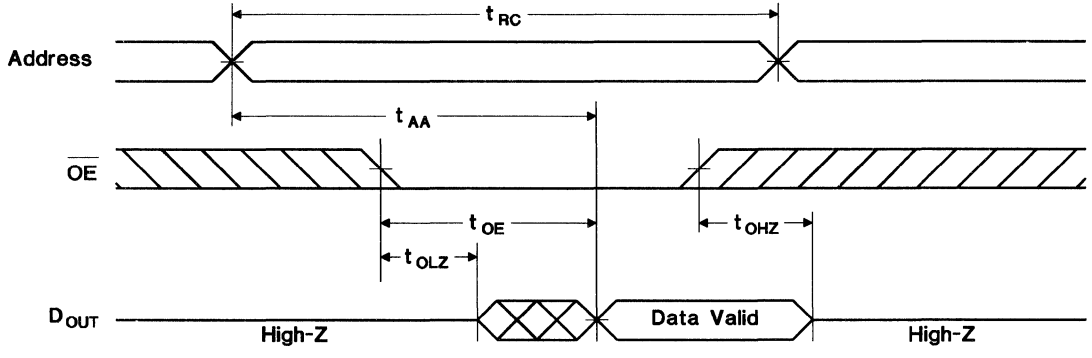
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



RC-3

Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

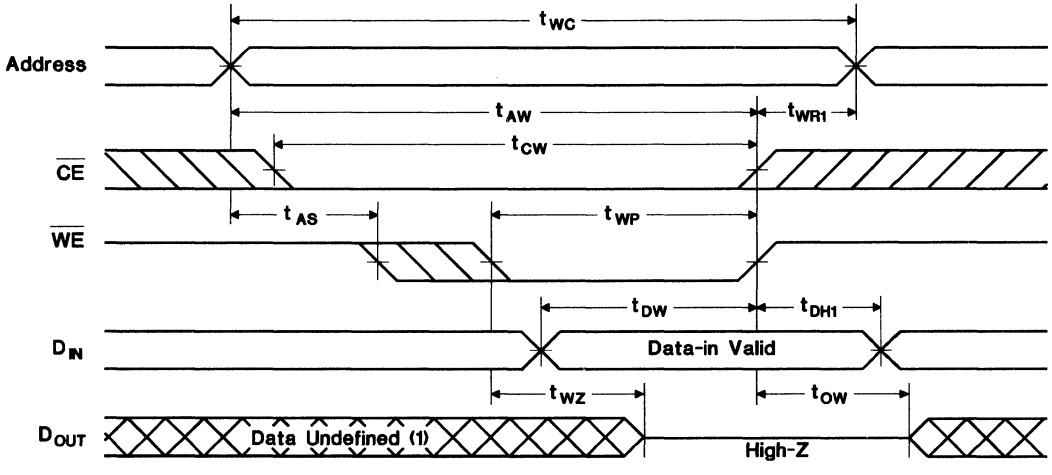
Write Cycle (TA = 0 to 70°C, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	-35		-45		Units	Notes
		Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	35	-	45	-	ns	
t_{CW}	Chip enable to end of write	30	-	40	-	ns	(1)
t_{AW}	Address valid to end of write	20	-	30	-	ns	(1)
t_{AS}	Address setup time	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	25	-	30	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	0	-	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	10	-	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	12	-	15	-	ns	Measured from first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high-Z	0	15	0	15	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	5	-	5	-	ns	I/O pins are in output state. (5)

Notes:

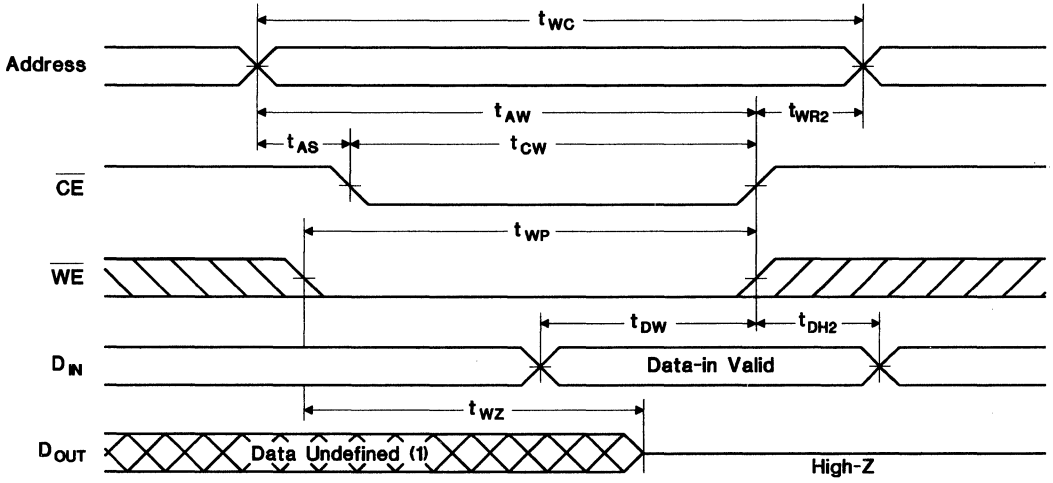
1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



WC-3

Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



WC-4

Notes:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

Power-Down/Power-Up Cycle (T_A = 0 to 70°C)

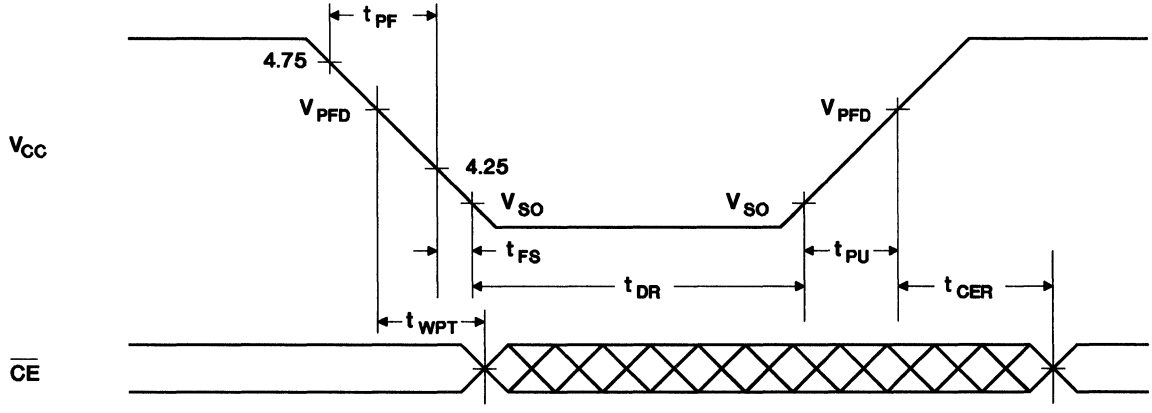
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{FPD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10	-	-	years	T_A = 25°C (2)
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Note: 1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

2. Battery is disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

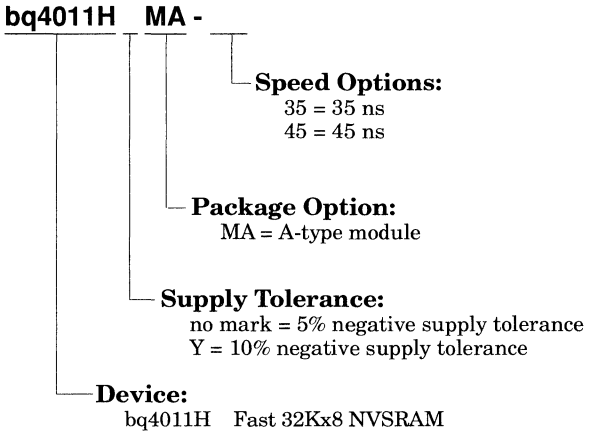
Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing



PD-B

Ordering Information



6

BENCHMARQ

bq4011H/bq4011HY

High-Speed 32Kx8 Nonvolatile SRAM

Features

- Access/cycle times of 20 and 25 ns
- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Industry-standard 28-pin 32K x 8 pinout
- Conventional SRAM operation; unlimited write cycles
- 10-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

The CMOS bq4011H is a nonvolatile 262,144-bit fast static RAM organized as 32,768 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM. Access times as fast as 20 ns are available.

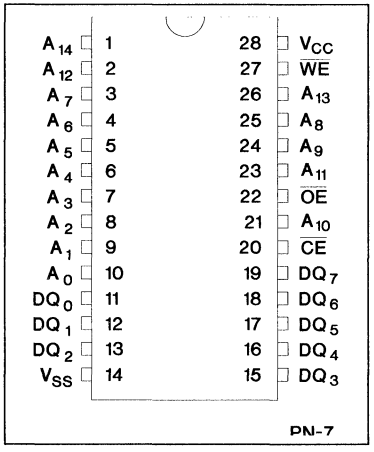
The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4011H uses an extremely low standby current CMOS SRAM, coupled with a small lithium coin cell to provide nonvolatility without long write cycle times and the write cycle limitations associated with EEPROM.

The bq4011H requires no external circuitry and is socket-compatible with industry-standard SRAMs.

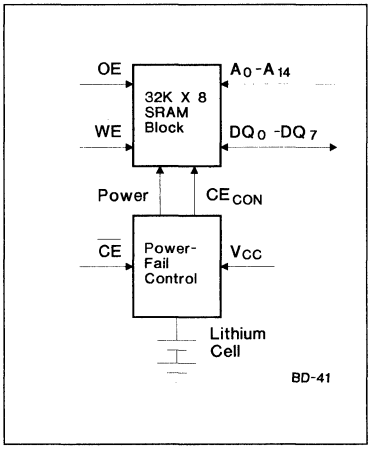
Pin Connections



Pin Names

$A_0 - A_{14}$	Address inputs
$DQ_0 - DQ_7$	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
V_{CC}	+5 volt supply input
V_{SS}	Ground

Block Diagram



Selection Guide

Part Number	Minimum Access Time (ns)	Negative Supply Tolerance	Part Number	Minimum Access Time (ns)	Negative Supply Tolerance
bq4011H -20	20	-5%	bq4011HY -20	20	-10%
bq4011H -25	25	-5%	bq4011HY -25	25	-10%

bq4013/bq4013Y

128Kx8 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Industry-standard 32-pin 128K x 8 pinout
- Conventional SRAM operation; unlimited write cycles
- 10-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

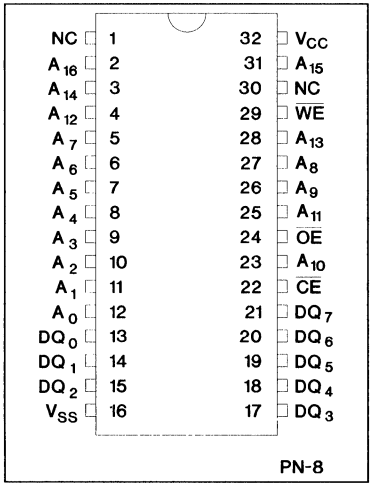
The CMOS bq4013 is a nonvolatile 1,048,576-bit static RAM organized as 131,072 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation. At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4013 uses an extremely low standby current CMOS SRAM, coupled with a small lithium coin cell to provide nonvolatility without long write cycle times and the write cycle limitations associated with EEPROM.

The bq4013 requires no external circuitry and is socket-compatible with industry-standard SRAMs and most EPROMs and EEPROMs.

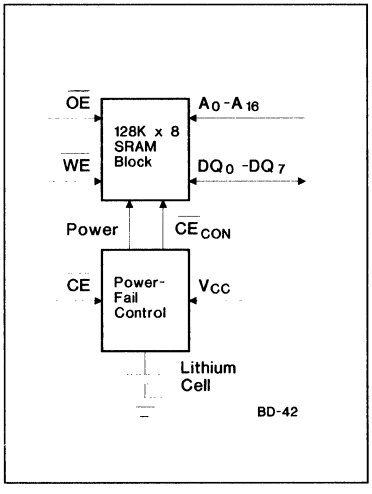
Pin Connections



Pin Names

A_0–A_{16}	Address inputs
DQ_0–DQ_7	Data input/output
$\overline{CE}$	Chip-enable input
$\overline{OE}$	Output-enable input
$\overline{WE}$	Write-enable input
NC	No connect
V_{CC}	+5 volt supply input
V_{SS}	Ground

Block Diagram



Selection Guide

Part Number	Minimum Access Time (ns)	Negative Supply Tolerance	Part Number	Minimum Access Time (ns)	Negative Supply Tolerance
bq4013 -85	85	-5%	bq4013Y -85	85	-10%
bq4013 -120	120	-5%	bq4013Y -120	120	-10%

Functional Description

When power is valid, the bq4013 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4013 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4013 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4013Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120 ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cell used by the bq4013 has an extremely long shelf life and provides data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cell is electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup cell provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4013Y
		4.75	5.0	5.5	V	bq4013
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = 0 to 70°C, $V_{CCmin} \geq V_{CC} \geq V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current	-	4	7	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current	-	2.5	4	mA	$\overline{CE} \geq V_{CC}$ - 0.2V, $0V \leq V_{IN} \leq$ 0.2V, or $V_{IN} \geq V_{CC}$ - 0.2V
I_{CC}	Operating supply current	-	75	105	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4013
		4.30	4.37	4.50	V	bq4013Y
V_{SO}	Supply switch-over voltage	-	3	-	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC} = 3V.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	10	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	10	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

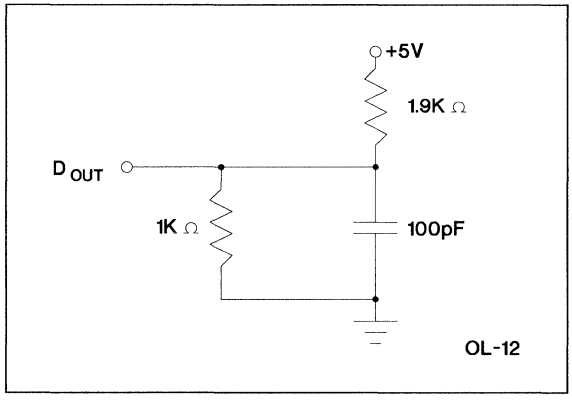


Figure 1. Output Load A

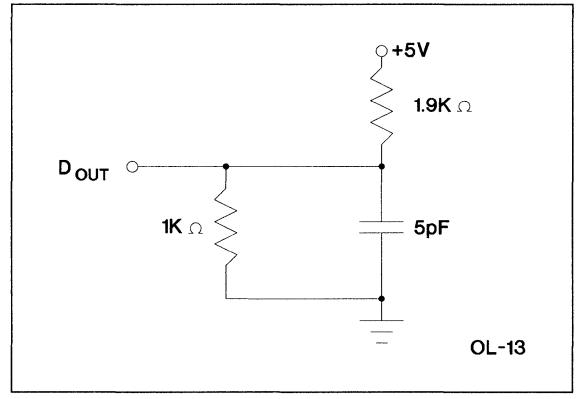
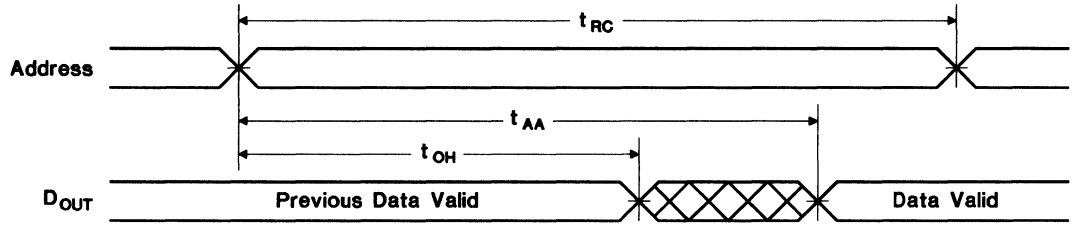


Figure 2. Output Load B

Read Cycle (T_A = 0 to 70°C, $V_{CCmin} \geq V_{CC} \geq V_{CCmax}$)

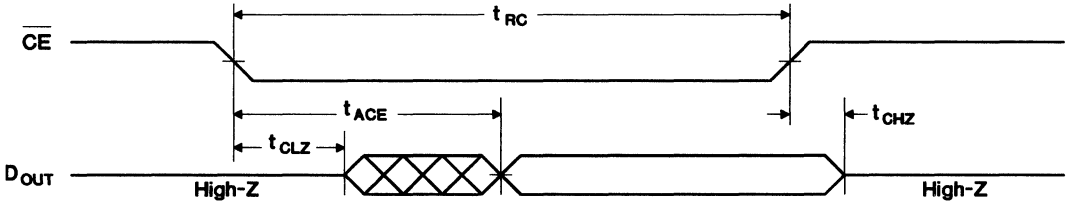
Symbol	Parameter	-85		-120		Unit	Conditions
		Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	85	-	120	-	ns	
t_{AA}	Address access time	-	85	-	120	ns	Output load A
t_{ACE}	Chip enable access time	-	85	-	120	ns	Output load A
t_{OE}	Output enable to output valid	-	45	-	60	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	0	-	0	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	35	0	45	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	0	35	ns	Output load B
t_{OH}	Output hold from address change	10	-	10	-	ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



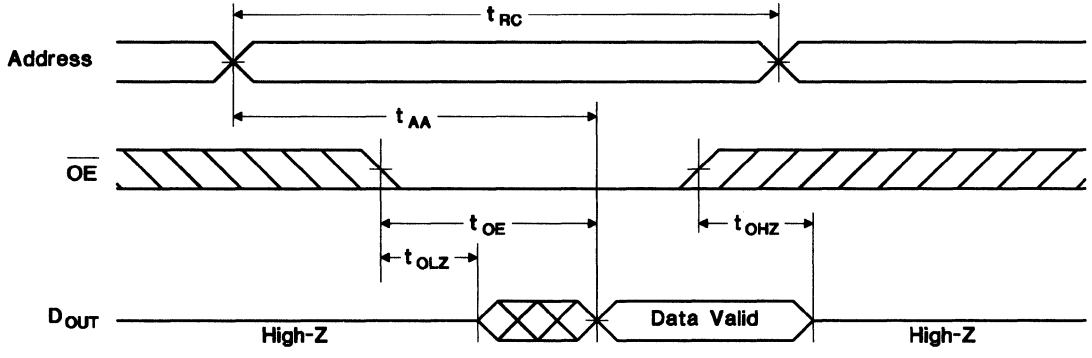
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



RC-3

Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

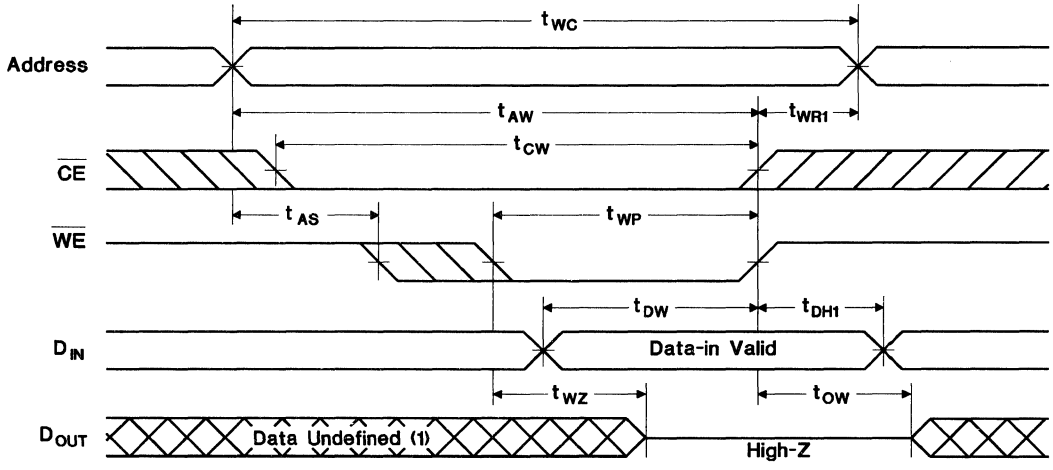
Write Cycle (TA = 0 to 70°C, VCCmin ≥ VCC ≥ VCCmax)

Symbol	Parameter	-85		-120		Units	Conditions/ Notes
		Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	85	-	120	-	ns	
t_{CW}	Chip enable to end of write	75	-	100	-	ns	(1)
t_{AW}	Address valid to end of write	75	-	100	-	ns	(1)
t_{AS}	Address setup time	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	65	-	85	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	35	-	45	-	ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	30	0	40	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	0	-	0	-	ns	I/O pins are in output state. (5)

Notes:

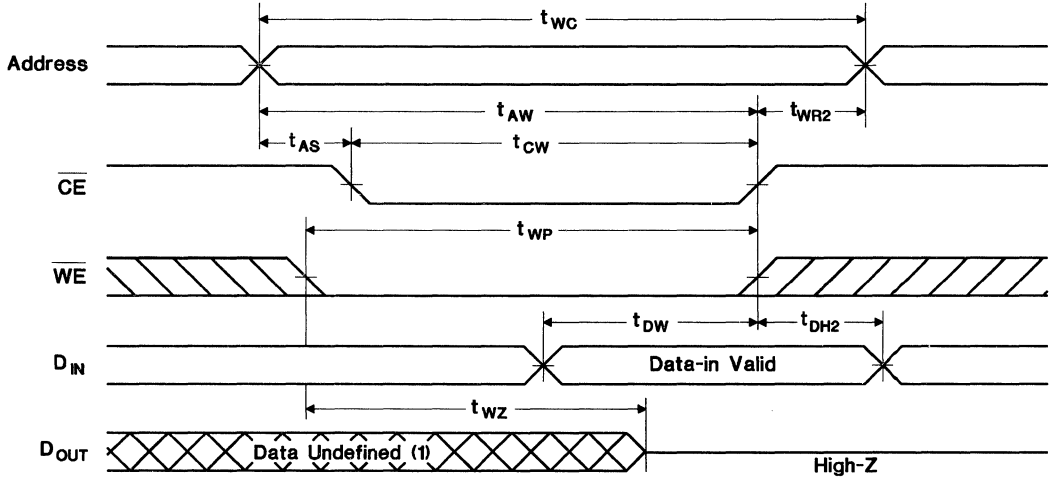
1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



WC-3

Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



WC-4

Notes:
1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

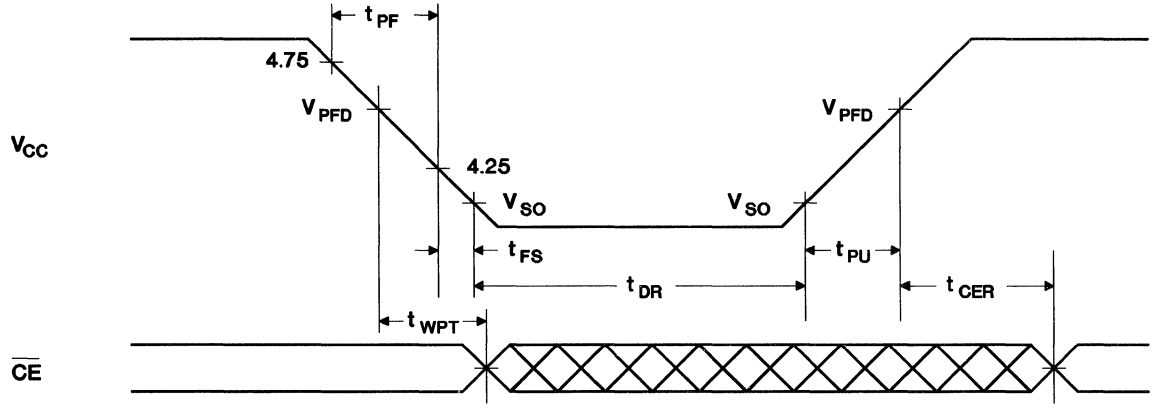
Power-Down/Power-Up Cycle (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{FPD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10	-	-	years	T_A = 25°C (2)
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Note:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Battery is disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

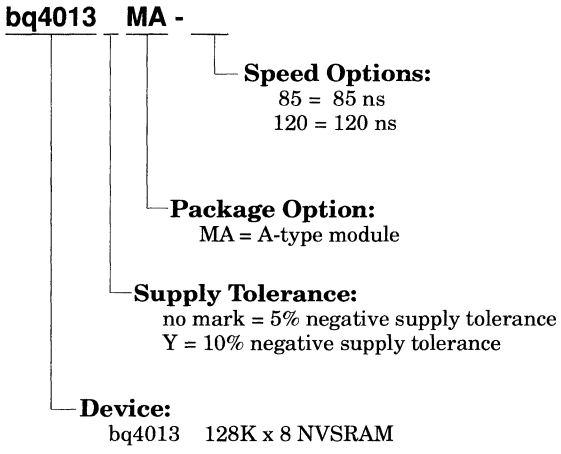
Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing



PD-B

Ordering Information



6

Notes

BENCHMARQ

Preliminary

bq4014/bq4014Y

256Kx8 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Industry-standard 32-pin 256K x 8 pinout
- Conventional SRAM operation; unlimited write cycles
- 10-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

The CMOS bq4014 is a nonvolatile 2,097,152-bit static RAM organized as 262,144 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

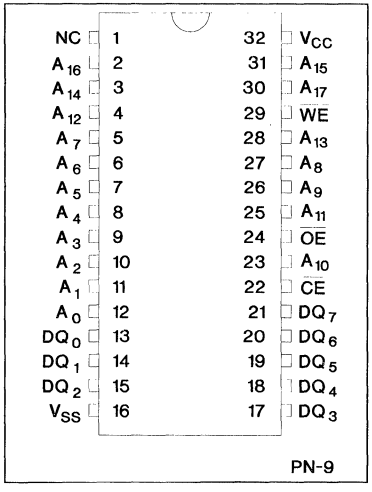
The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4014 uses extremely low standby current CMOS SRAMs, coupled with small lithium coin cells to provide nonvolatility without long write cycle times and the write cycle limitations associated with EEPROM.

The bq4014 requires no external circuitry and is compatible with the industry-standard 2Mb SRAM pinout.

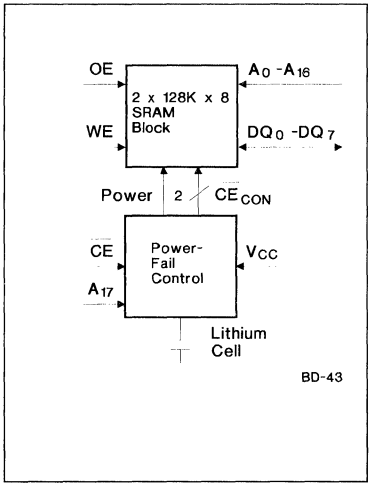
Pin Connections



Pin Names

A_0–A_{17}	Address inputs
DQ_0–DQ_7	Data input/output
$\overline{CE}$	Chip-enable input
$\overline{OE}$	Output-enable input
$\overline{WE}$	Write-enable input
NC	No connect
V_{CC}	+5 volt supply input
V_{SS}	Ground

Block Diagram



Selection Guide

Part Number	Minimum Access Time (ns)	Negative Supply Tolerance	Part Number	Minimum Access Time (ns)	Negative Supply Tolerance
bq4014 -85	85	-5%	bq4014Y -85	85	-10%
bq4014 -120	120	-5%	bq4014Y -120	120	-10%

Functional Description

When power is valid, the bq4014 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4014 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4014 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4014Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120 ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cells used by the bq4014 have an extremely long shelf life and provides data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cells are electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operatio should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4014Y
		4.75	5.0	5.5	V	bq4014
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = 0 to 70°C, $V_{CCmin} \geq V_{CC} \geq V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 2	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 2	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current	-	5	12	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current	-	2.5	4	mA	$\overline{CE} \geq V_{CC}$ - 0.2V, $0V \leq V_{IN} \leq 0.2V$, or $V_{IN} \geq V_{CC}$ - 0.2V
I_{CC}	Operating supply current	-	75	110	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4014
		4.30	4.37	4.50	V	bq4014Y
V_{SO}	Supply switch-over voltage	-	3	-	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC} = 3V.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	20	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	20	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

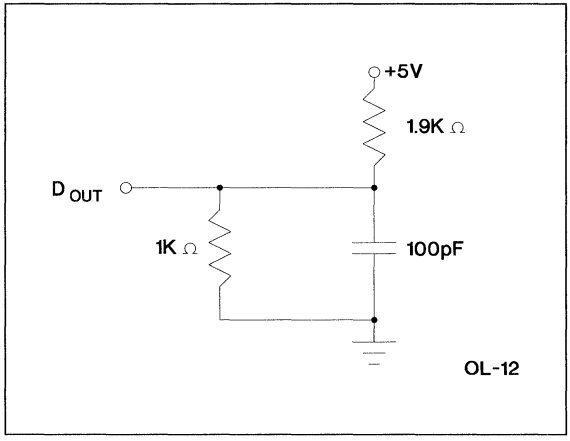


Figure 1. Output Load A

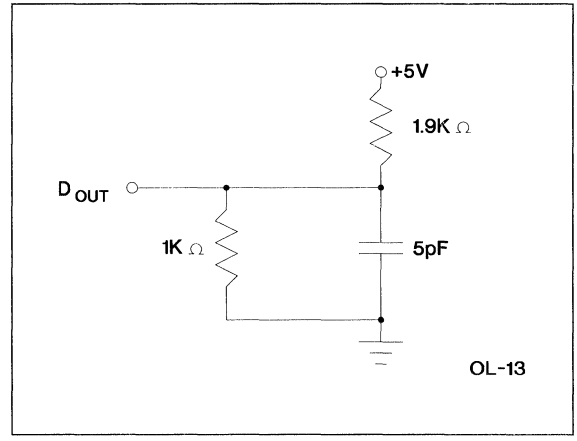
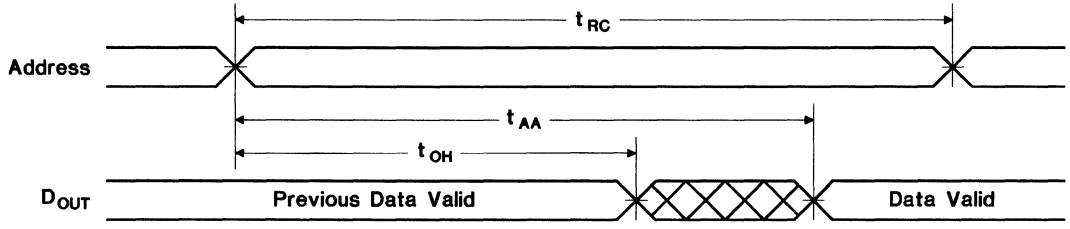


Figure 2. Output Load B

Read Cycle (T_A = 0 to 70°C, $V_{CCmin} \geq V_{CC} \geq V_{CCmax}$)

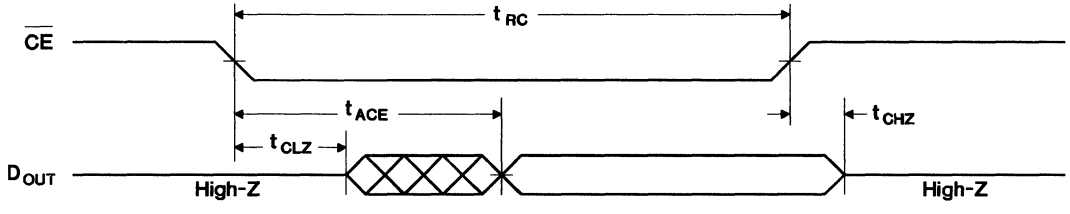
Symbol	Parameter	-85		-120		Unit	Conditions
		Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	85	-	120	-	ns	
t_{AA}	Address access time	-	85	-	120	ns	Output load A
t_{ACE}	Chip enable access time	-	85	-	120	ns	Output load A
t_{OE}	Output enable to output valid	-	45	-	60	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	0	-	0	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	35	0	45	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	0	35	ns	Output load B
t_{OH}	Output hold from address change	10	-	10	-	ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



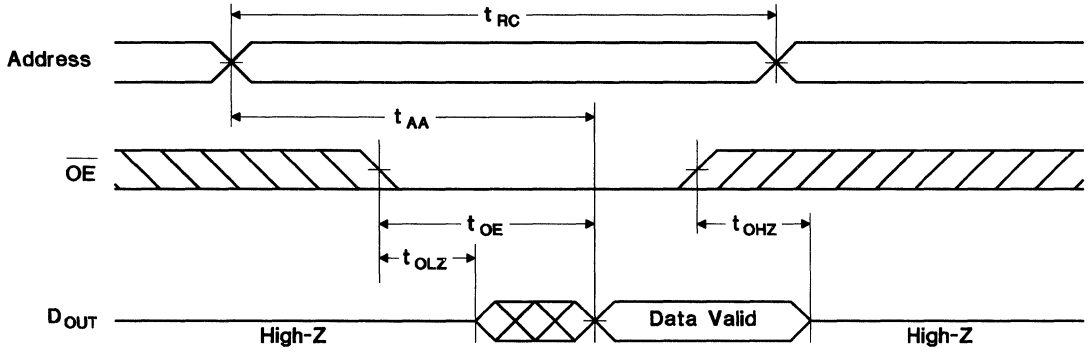
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



RC-3

Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE}$ = $\overline{OE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Device is continuously selected: $\overline{CE}$ = V_{IL}.

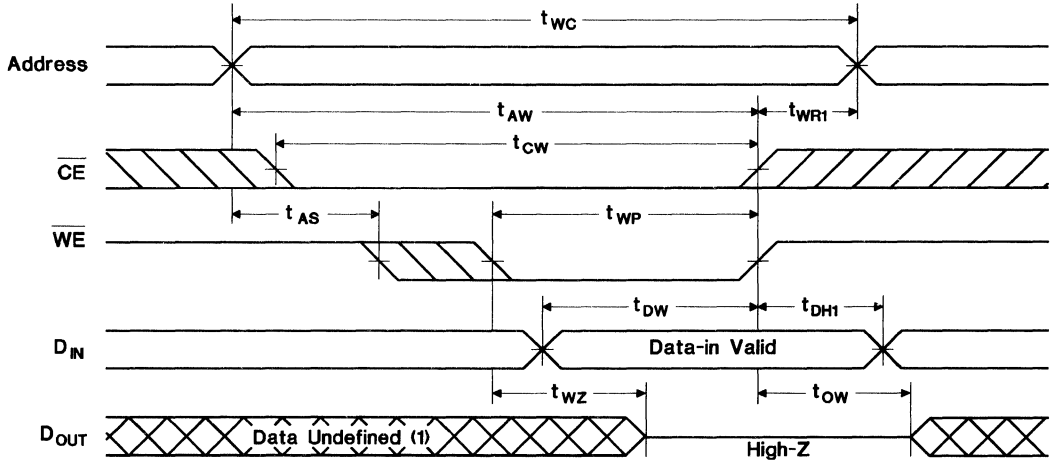
Write Cycle (T_A = 0 to 70°C, $V_{CCmin} \geq V_{CC} \geq V_{CCmax}$)

Symbol	Parameter	-85		-120		Units	Conditions/ Notes
		Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	85	-	120	-	ns	
t_{CW}	Chip enable to end of write	75	-	100	-	ns	(1)
t_{AW}	Address valid to end of write	75	-	100	-	ns	(1)
t_{AS}	Address setup time	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	65	-	85	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	35	-	45	-	ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	30	0	40	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	0	-	0	-	ns	I/O pins are in output state. (5)

Notes:

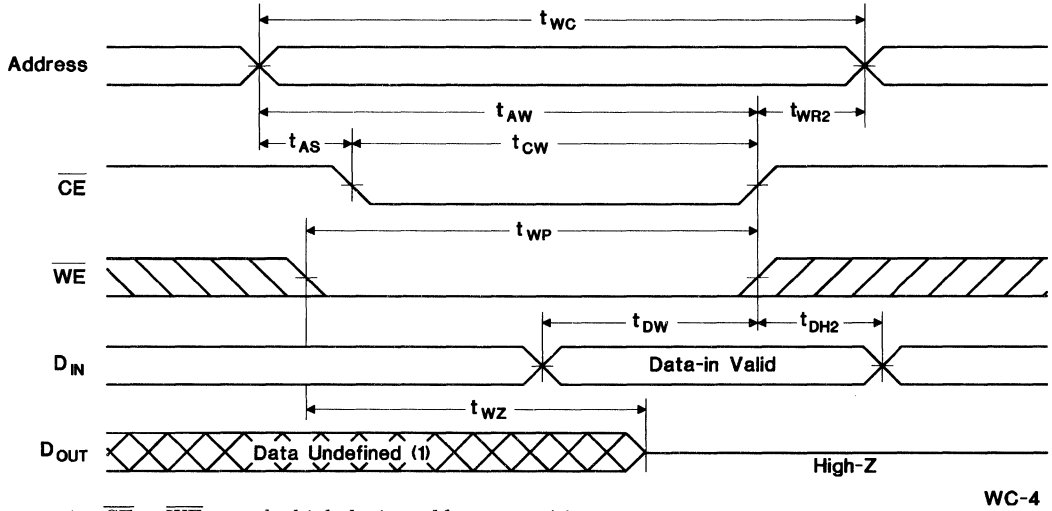
1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



WC-3

Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



WC-4

Notes:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

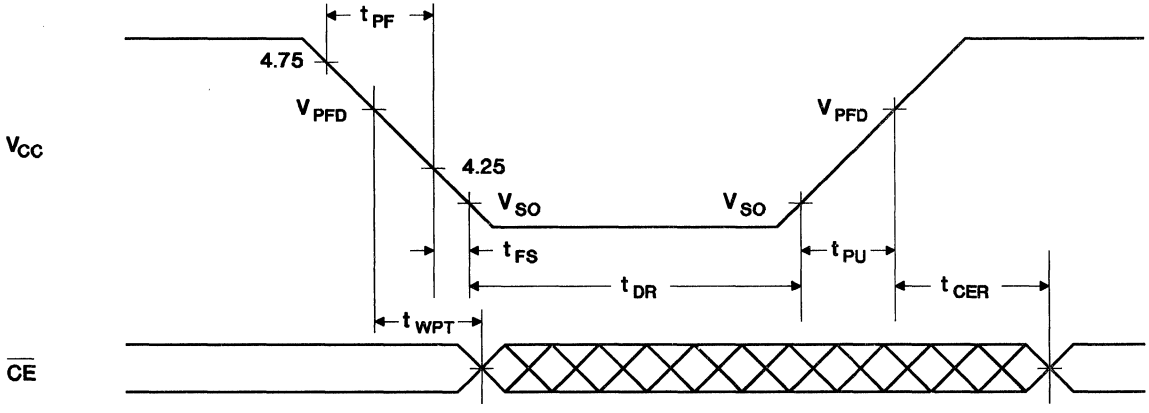
Power-Down/Power-Up Cycle (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{FPD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10	-	-	years	T_A = 25°C (2)
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Note: 1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Batteries are disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

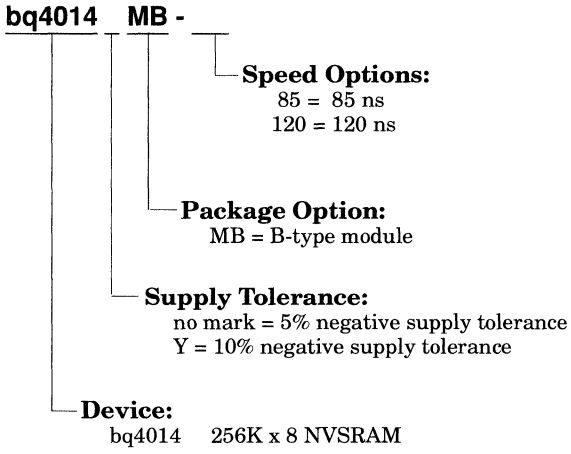
Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

Power-Down/Power-Up Timing



PD-B

Ordering Information



6

BENCHMARQ

Preliminary

bq4015/bq4015Y

512Kx8 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Industry-standard 32-pin 512K x 8 pinout
- Conventional SRAM operation; unlimited write cycles
- 5-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

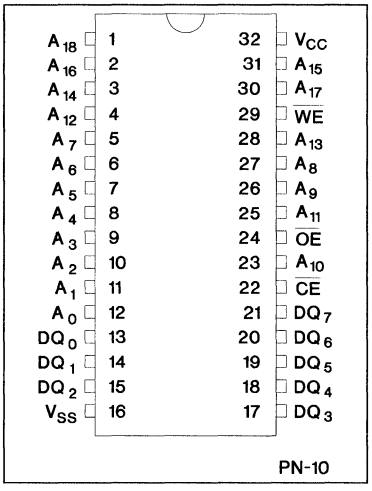
The CMOS bq4015 is a nonvolatile 4,194,304-bit static RAM organized as 524,288 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation. At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4015 uses extremely low standby current CMOS SRAMs, coupled with small lithium coin cells to provide nonvolatility without long write cycle times and the write cycle limitations associated with EEPROM.

The bq4015 requires no external circuitry and is compatible with the industry-standard 4Mb SRAM pinout.

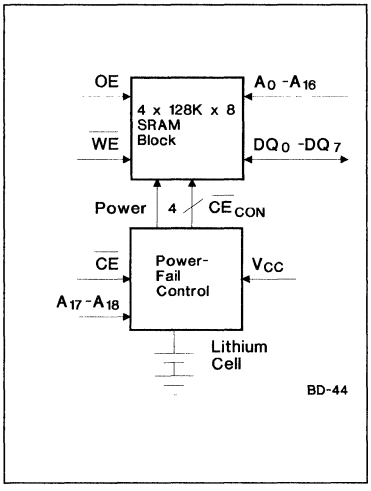
Pin Connections



Pin Names

A_0–A_{18}	Address inputs
DQ_0–DQ_7	Data input/output
$\overline{CE}$	Chip-enable input
$\overline{OE}$	Output-enable input
$\overline{WE}$	Write-enable input
V_{CC}	+5 volt supply input
V_{SS}	Ground

Block Diagram



Selection Guide

Part Number	Minimum Access Time (ns)	Negative Supply Tolerance	Part Number	Minimum Access Time (ns)	Negative Supply Tolerance
bq4015 -85	85	-5%	bq4015Y -85	85	-10%
bq4015 -120	120	-5%	bq4015Y -120	120	-10%

Functional Description

When power is valid, the bq4015 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4015 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4015 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4015Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120 ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cells used by the bq4015 have an extremely long shelf life and provides data retention for more than 5 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cells are electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4015Y
		4.75	5.0	5.5	V	bq4015
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = 0 to 70°C, $V_{CCmin} \geq V_{CC} \geq V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 4	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 4	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current	-	7	17	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current	-	2.5	5	mA	$\overline{CE} \geq V_{CC}$ - 0.2V, $0V \leq V_{IN} \leq 0.2V$, or $V_{IN} \geq V_{CC}$ - 0.2V
I_{CC}	Operating supply current	-	75	115	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4015
		4.30	4.37	4.50	V	bq4015Y
V_{SO}	Supply switch-over voltage	-	3	-	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC} = 3V.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	40	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	40	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

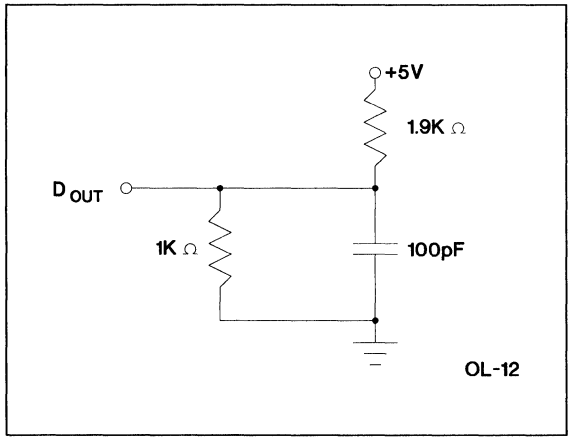


Figure 1. Output Load A

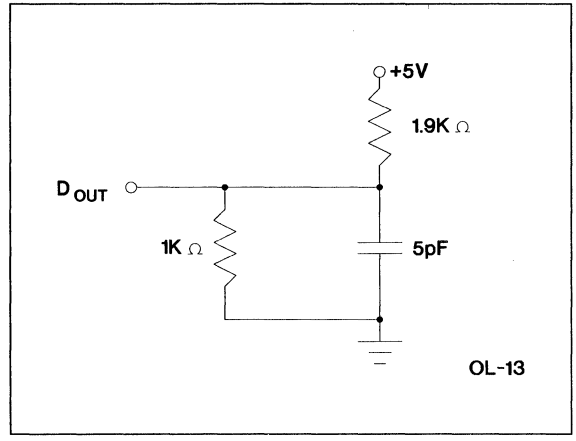
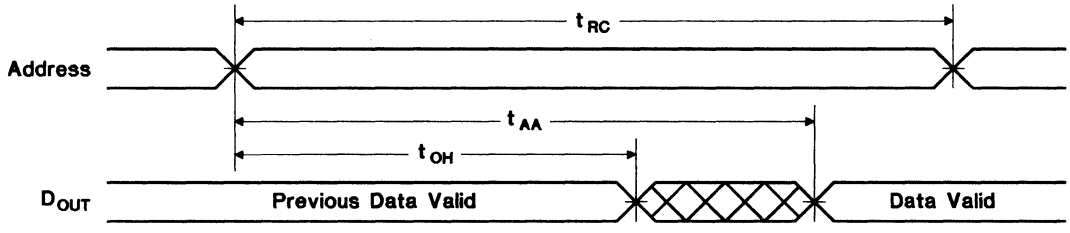


Figure 2. Output Load B

Read Cycle (TA = 0 to 70°C, VCCmin ≥ VCC ≥ VCCmax)

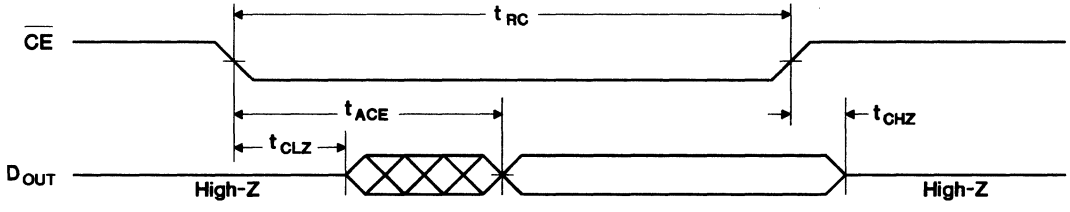
Symbol	Parameter	-85		-120		Unit	Conditions
		Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	85	-	120	-	ns	
t_{AA}	Address access time	-	85	-	120	ns	Output load A
t_{ACE}	Chip enable access time	-	85	-	120	ns	Output load A
t_{OE}	Output enable to output valid	-	45	-	60	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	0	-	0	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	35	0	45	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	0	35	ns	Output load B
t_{OH}	Output hold from address change	10	-	10	-	ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



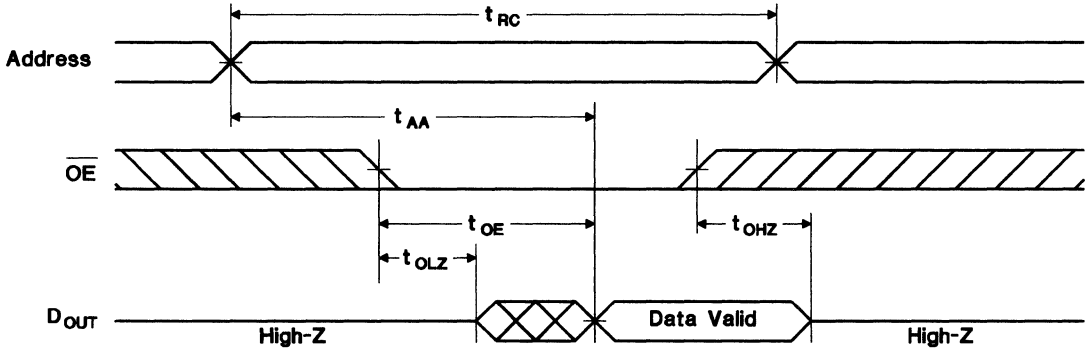
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



RC-3

Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

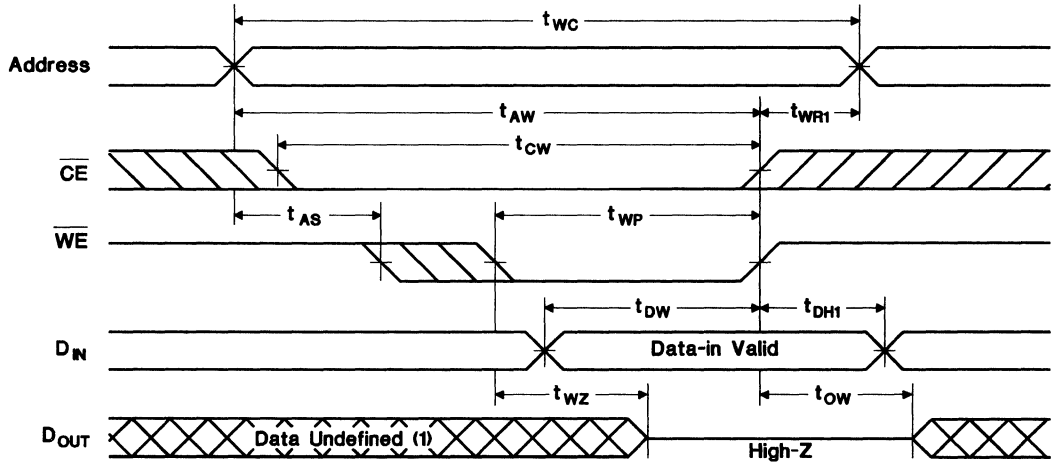
Write Cycle (TA = 0 to 70°C, VCCmin ≥ VCC ≥ VCCmax)

Symbol	Parameter	-85		-120		Units	Conditions/ Notes
		Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	85	-	120	-	ns	
t_{CW}	Chip enable to end of write	75	-	100	-	ns	(1)
t_{AW}	Address valid to end of write	75	-	100	-	ns	(1)
t_{AS}	Address setup time	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	65	-	85	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	35	-	45	-	ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	30	0	40	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	0	-	0	-	ns	I/O pins are in output state. (5)

Notes:

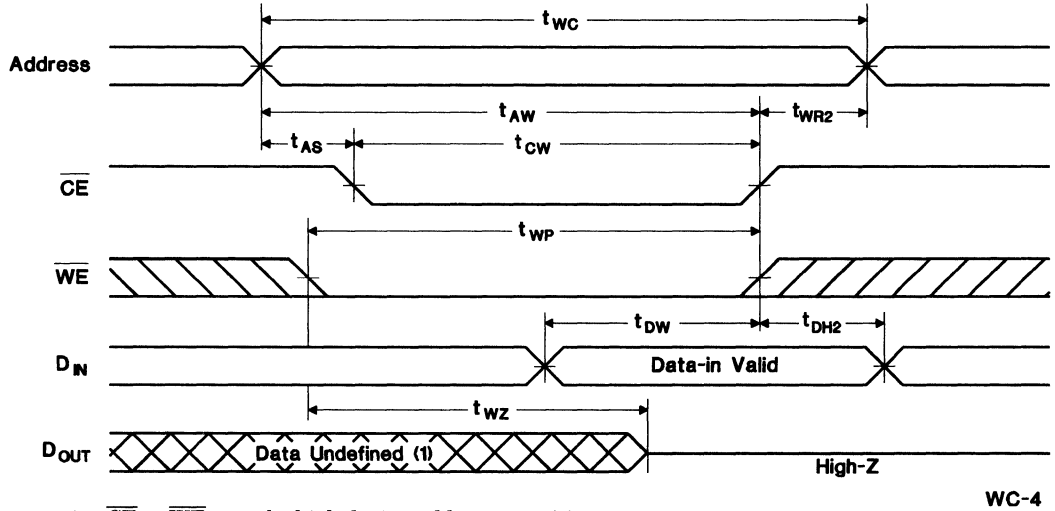
1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



WC-3

Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



WC-4

Notes:
1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

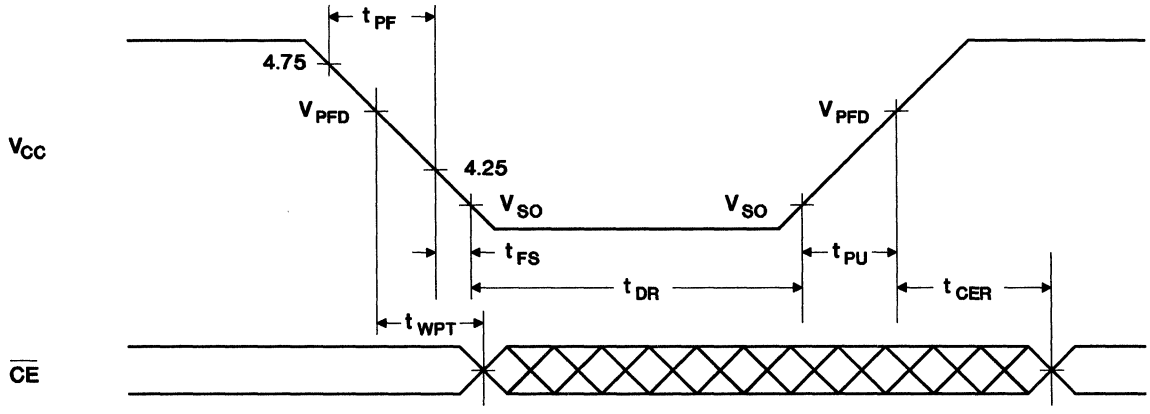
Power-Down/Power-Up Cycle (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{FPD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	5	-	-	years	T_A = 25°C (2)
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Note: 1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Batteries are disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

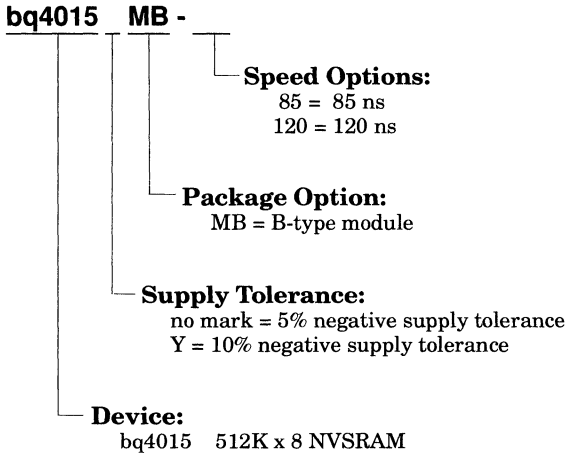
Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

Power-Down/Power-Up Timing



PD-B

Ordering Information



6

Notes

Preliminary

bq4024/bq4024Y

128Kx16 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Industry-standard 40-pin 128K x 16 pinout
- Conventional SRAM operation; unlimited write cycles
- 10-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

The CMOS bq4024 is a nonvolatile 2,097,152-bit static RAM organized as 131,072 words by 16 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

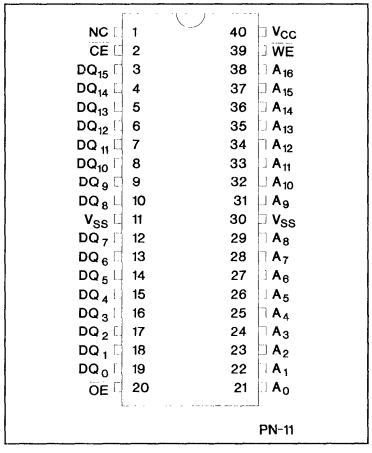
The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4024 uses extremely low standby current CMOS SRAMs, coupled with small lithium coin cells to provide nonvolatility without long write cycle times and the write cycle limitations associated with EEPROM.

The bq4024 requires no external circuitry and is compatible with the industry-standard 2Mb SRAM pinout.

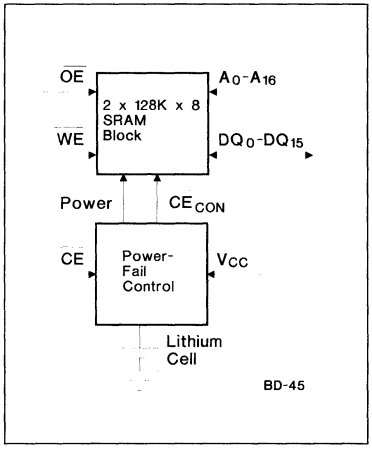
Pin Connections



Pin Names

A_0–A_{16}	Address inputs
DQ_0–DQ_{15}	Data input/output
$\overline{CE}$	Chip-enable input
$\overline{OE}$	Output-enable input
$\overline{WE}$	Write-enable input
NC	No connect
V_{CC}	+5 volt supply input
V_{SS}	Ground

Block Diagram



Selection Guide

Part Number	Minimum Access Time (ns)	Negative Supply Tolerance	Part Number	Minimum Access Time (ns)	Negative Supply Tolerance
bq4024 -85	85	-5%	bq4024Y -85	85	-10%
bq4024 -120	120	-5%	bq4024Y -120	120	-10%

Functional Description

When power is valid, the bq4024 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4024 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4024 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4024Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120 ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cells used by the bq4024 have an extremely long shelf life and provides data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cells are electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4024Y
		4.75	5.0	5.5	V	bq4024
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = 0 to 70°C, $V_{CC}min \geq V_{CC} \geq V_{CC}max$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 2	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current	-	5	11	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current	-	2.5	5	mA	$\overline{CE} \geq V_{CC}$ - 0.2V, $0V \leq V_{IN} \leq 0.2V$, or $V_{IN} \geq V_{CC}$ - 0.2V
I_{CC}	Operating supply current	-	95	200	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4024
		4.30	4.37	4.50	V	bq4024Y
V_{SO}	Supply switch-over voltage	-	3	-	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC} = 3V.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	10	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	20	pF	Input voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

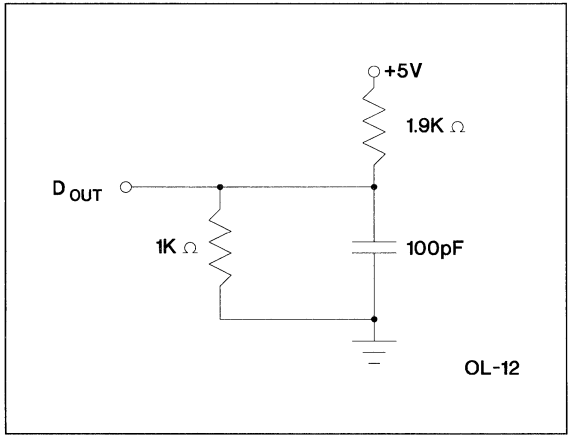


Figure 1. Output Load A

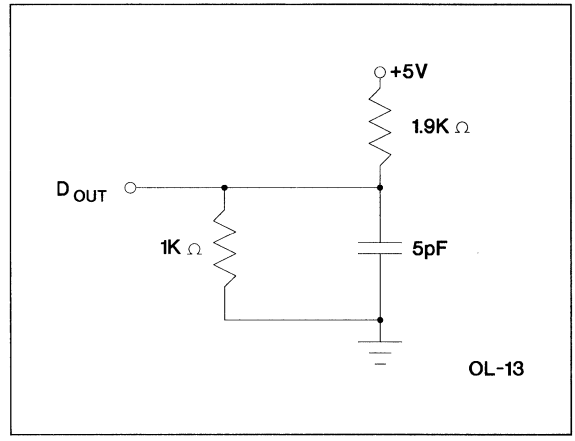
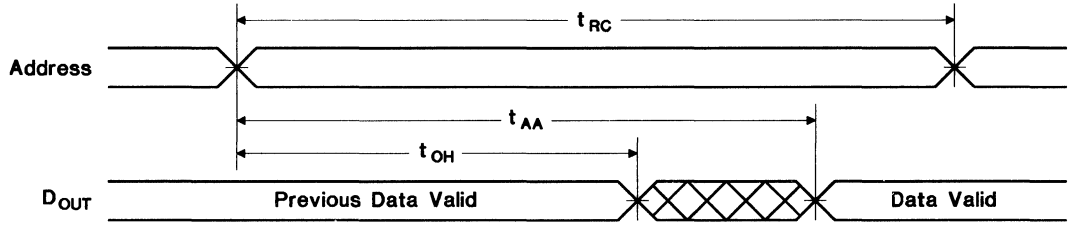


Figure 2. Output Load B

Read Cycle (T_A = 0 to 70°C, $V_{CCmin} \geq V_{CC} \geq V_{CCmax}$)

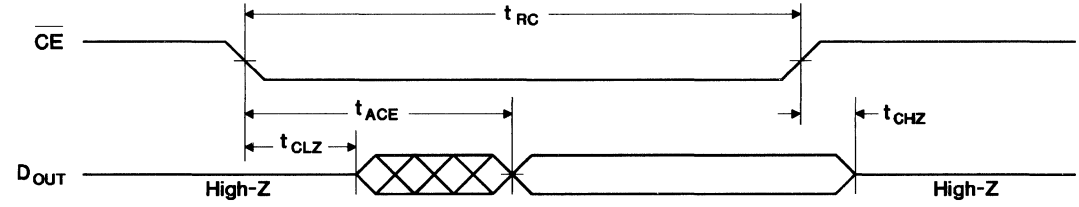
Symbol	Parameter	-85		-120		Unit	Conditions
		Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	85	-	120	-	ns	
t_{AA}	Address access time	-	85	-	120	ns	Output load A
t_{ACE}	Chip enable access time	-	85	-	120	ns	Output load A
t_{OE}	Output enable to output valid	-	45	-	60	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	0	-	0	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	35	0	45	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	0	35	ns	Output load B
t_{OH}	Output hold from address change	10	-	10	-	ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



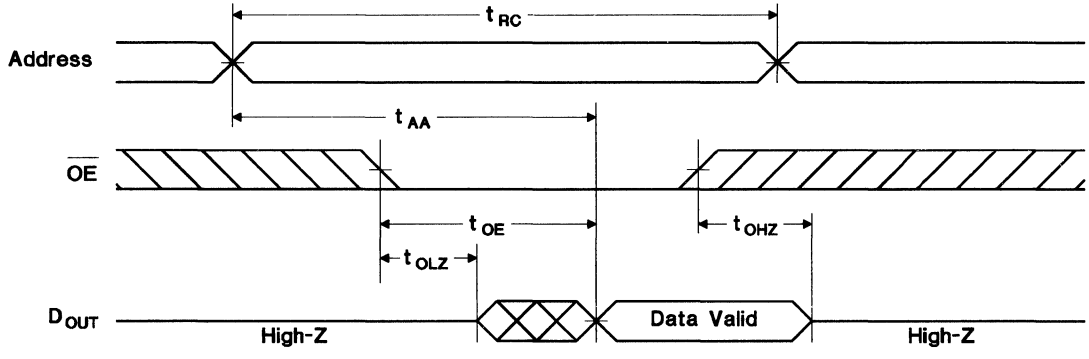
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



RC-3

Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

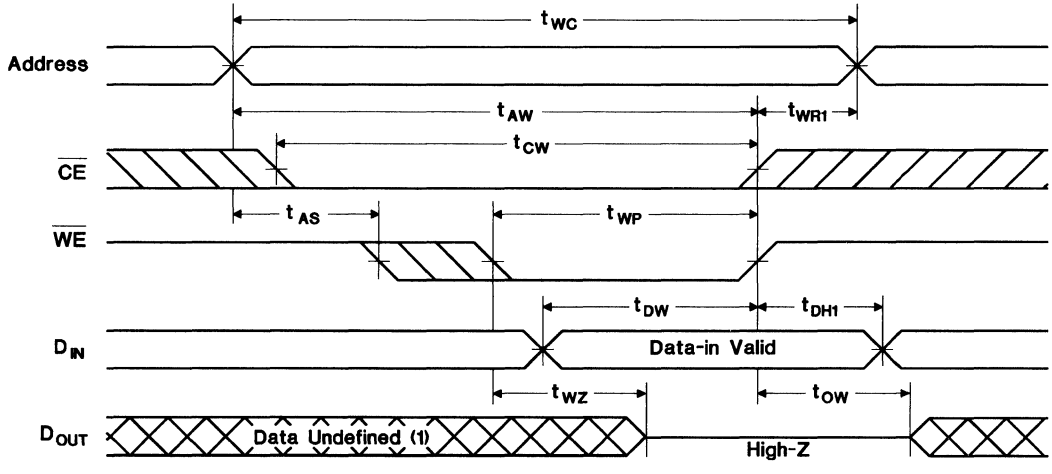
Write Cycle (T_A = 0 to 70°C, $V_{CCmin} \geq V_{CC} \geq V_{CCmax}$)

Symbol	Parameter	-85		-120		Units	Conditions/ Notes
		Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	85	-	120	-	ns	
t_{CW}	Chip enable to end of write	75	-	100	-	ns	(1)
t_{AW}	Address valid to end of write	75	-	100	-	ns	(1)
t_{AS}	Address setup time	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	65	-	85	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	35	-	45	-	ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle.(4)]
t_{DH2}	Data hold time (write cycle 2)	10	-	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high-Z	0	30	0	40	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	0	-	0	-	ns	I/O pins are in output state. (5)

Notes:

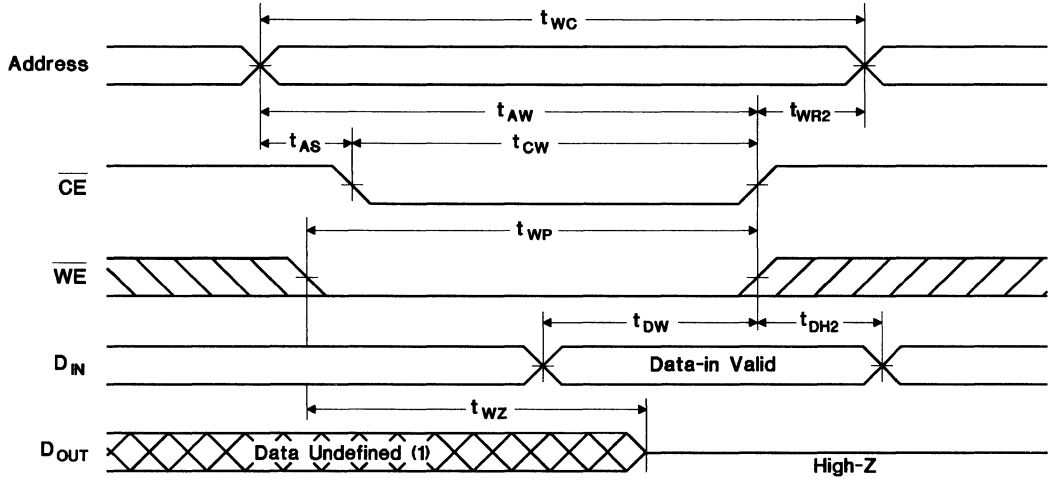
1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



WC-3

Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



WC-4

Notes:
1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

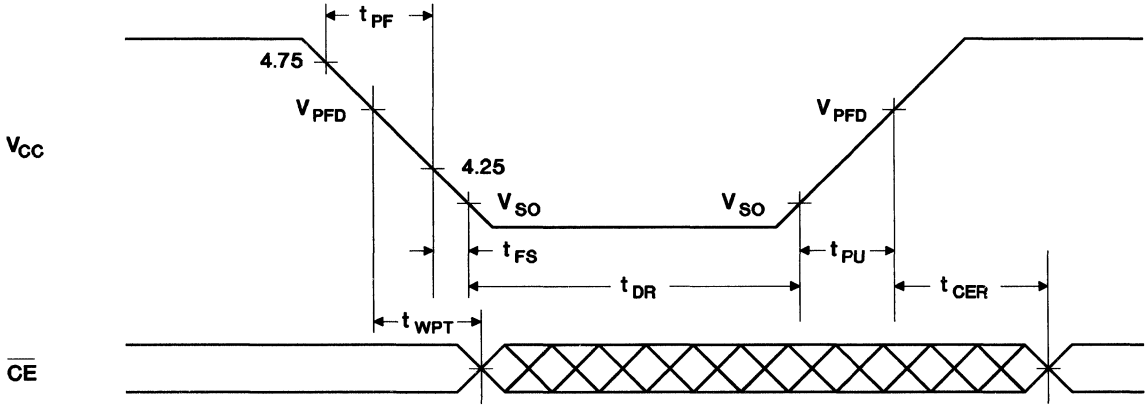
Power-Down/Power-Up Cycle (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10	-	-	years	T_A =25°C (2)
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Note: 1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Batteries are disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

Power-Down/Power-Up Timing



PD-B

Ordering Information

bq4024 MA -

Speed Options:
85 = 85 ns
120 = 120 ns

Package Option:
MA = A-type module

Supply Tolerance:
no mark = 5% negative supply tolerance
Y = 10% negative supply tolerance

Device:
bq4024 128K x 16 NVSRAM

6

Notes

BENCHMARQ

Preliminary **bq4025/bq4025Y**

256Kx16 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Industry-standard 40-pin 256K x 16 pinout
- Conventional SRAM operation; unlimited write cycles
- 5-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

The CMOS bq4025 is a nonvolatile 4,194,304-bit static RAM organized as 262,144 words by 16 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

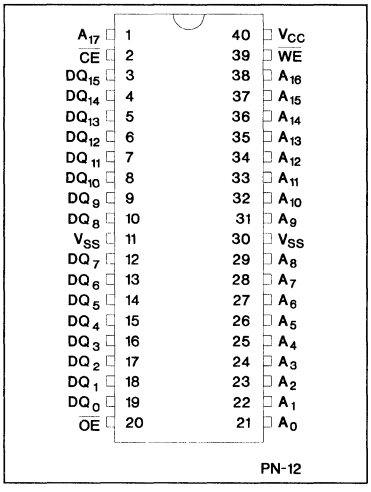
The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4025 uses extremely low standby current CMOS SRAMs, coupled with small lithium coin cells to provide nonvolatility without long write cycle times and the write cycle limitations associated with EEPROM.

The bq4025 requires no external circuitry and is compatible with the industry-standard 4Mb SRAM pinout.

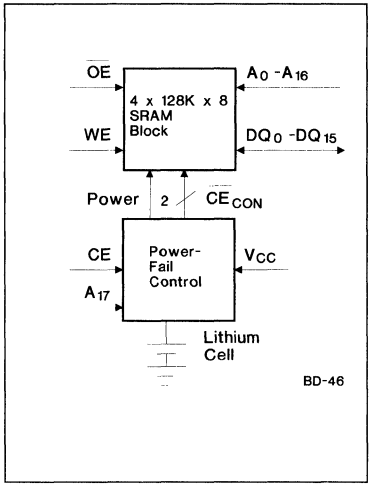
Pin Connections



Pin Names

A_0–A_{17}	Address inputs
DQ_0–DQ_{15}	Data input/output
$\overline{CE}$	Chip-enable input
$\overline{OE}$	Output-enable input
$\overline{WE}$	Write-enable input
V_{CC}	+5 volt supply input
V_{SS}	Ground

Block Diagram



Selection Guide

Part Number	Minimum Access Time (ns)	Negative Supply Tolerance	Part Number	Minimum Access Time (ns)	Negative Supply Tolerance
bq4025 -85	85	-5%	bq4025Y -85	85	-10%
bq4025 -120	120	-5%	bq4025Y -120	120	-10%

Functional Description

When power is valid, the bq4025 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4025 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4025 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4025Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120 ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cells used by the bq4025 have an extremely long shelf life and provides data retention for more than 5 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cells are electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4025Y
		4.75	5.0	5.5	V	bq4025
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C,

DC Electrical Characteristics (T_A = 0 to 70°C, $V_{CCmin} \geq V_{CC} \geq V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 4	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 2	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current	-	7	18	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current	-	2.5	5	mA	$\overline{CE} \geq V_{CC}$ - 0.2V, 0V ≤ $V_{IN} \leq$ 0.2V, or $V_{IN} \geq V_{CC}$ - 0.2V
I_{CC}	Operating supply current	-	95	200	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4025
		4.30	4.37	4.50	V	bq4025Y
V_{SO}	Supply switch-over voltage	-	3	-	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC} = 3V.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	20	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	40	pF	Input voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

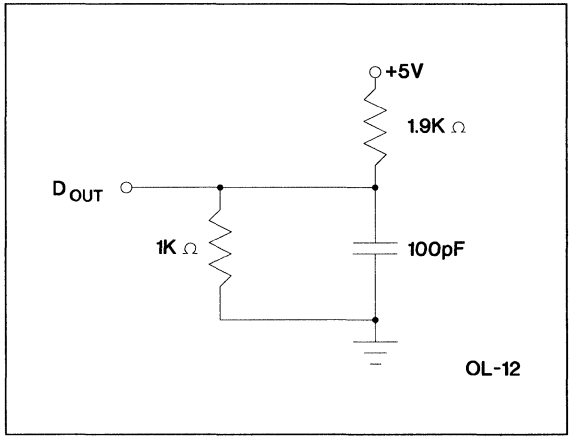


Figure 1. Output Load A

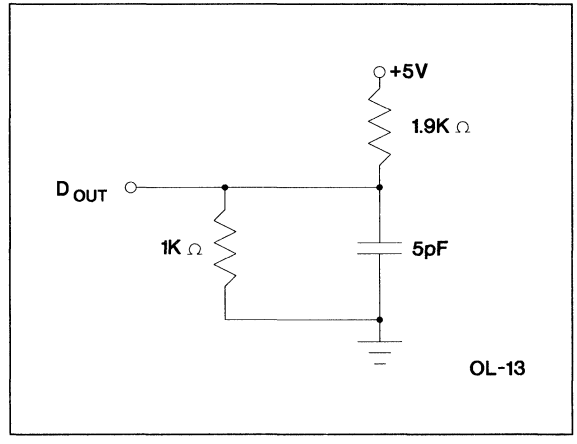
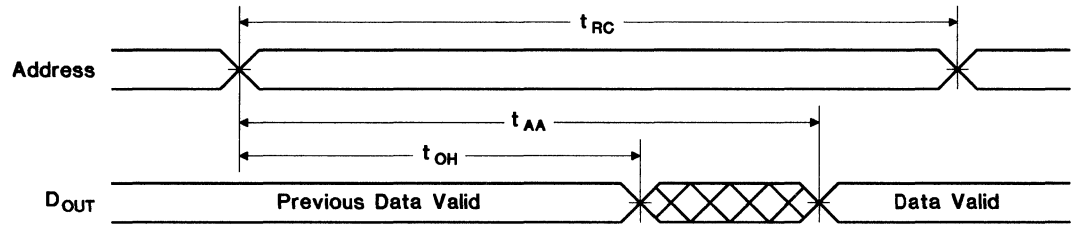


Figure 2. Output Load B

Read Cycle (T_A = 0 to 70°C, $V_{CCmin} \geq V_{CC} \geq V_{CCmax}$)

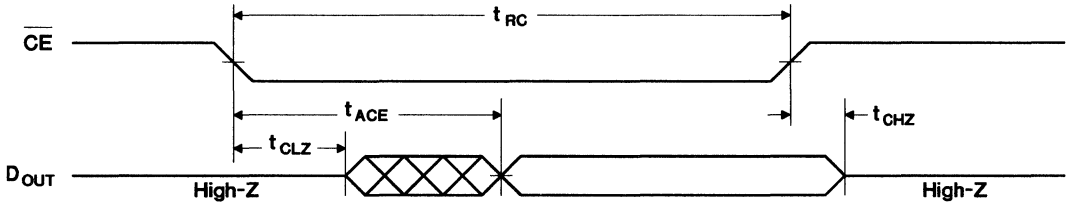
Symbol	Parameter	-85		-120		Unit	Conditions
		Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	85	-	120	-	ns	
t_{AA}	Address access time	-	85	-	120	ns	Output load A
t_{ACE}	Chip enable access time	-	85	-	120	ns	Output load A
t_{OE}	Output enable to output valid	-	45	-	60	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	0	-	0	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	35	0	45	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	0	35	ns	Output load B
t_{OH}	Output hold from address change	10	-	10	-	ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



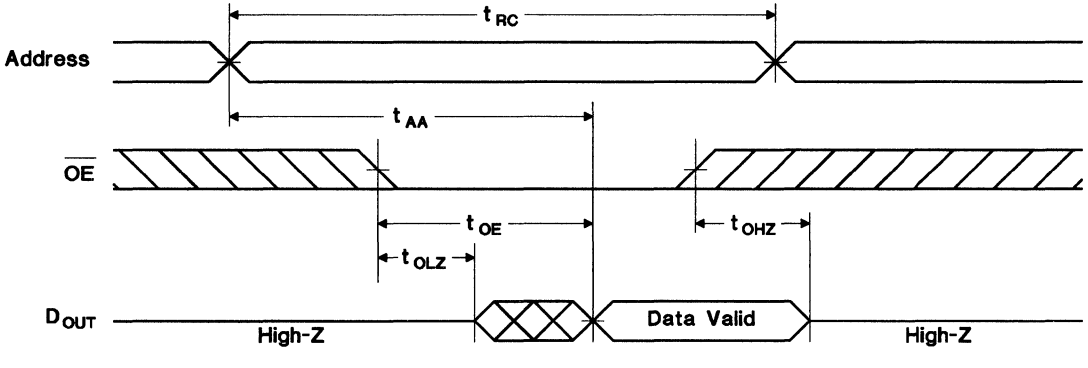
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



RC-3

Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

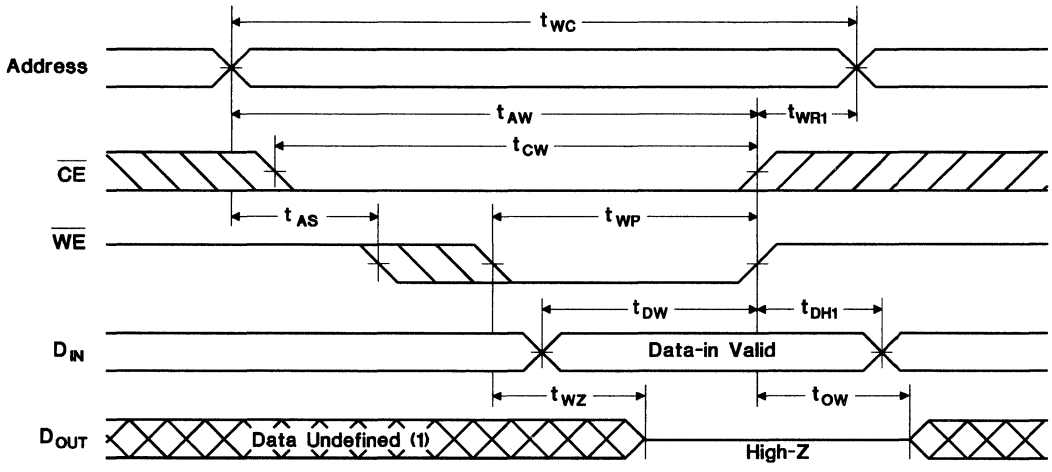
Write Cycle (T_A = 0 to 70°C, $V_{CCmin} \geq V_{CC} \geq V_{CCmax}$)

Symbol	Parameter	-85		-120		Units	Conditions/ Notes
		Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	85	-	120	-	ns	
t_{CW}	Chip enable to end of write	75	-	100	-	ns	(1)
t_{AW}	Address valid to end of write	75	-	100	-	ns	(1)
t_{AS}	Address setup time	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	65	-	85	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	35	-	45	-	ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high-Z	0	30	0	40	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	0	-	0	-	ns	I/O pins are in output state. (5)

Notes:

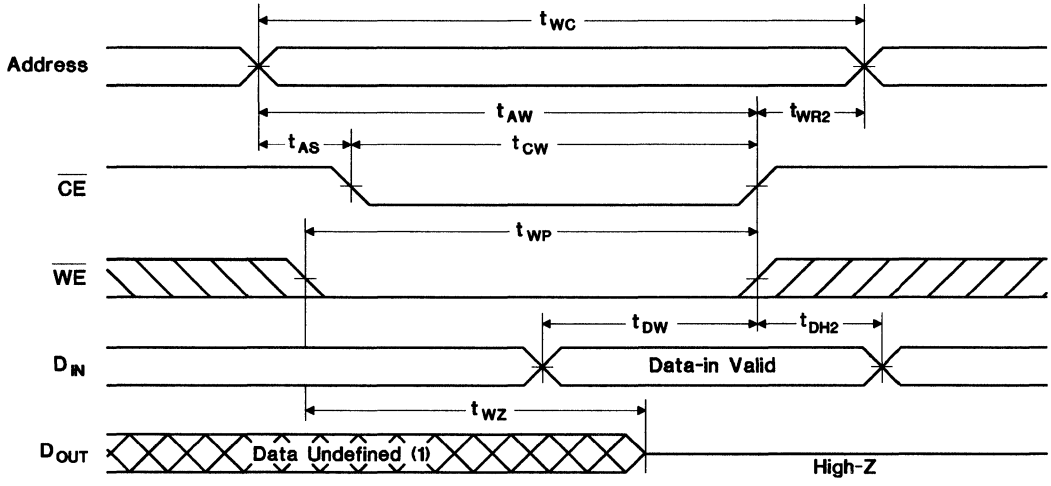
1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



WC-3

Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



WC-4

Notes:
1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

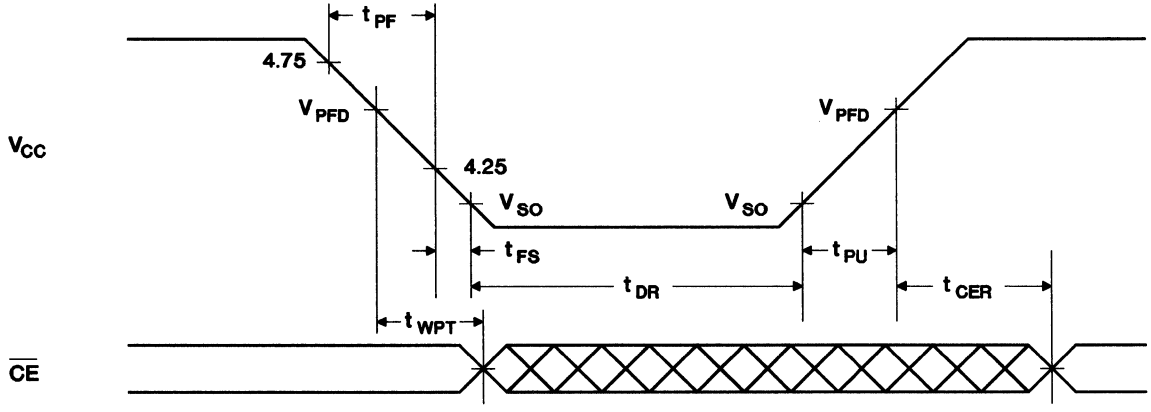
Power-Down/Power-Up Cycle (T_A = 0 to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	5			years	T_A = 25°C (2)
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Note: 1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Batteries are disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

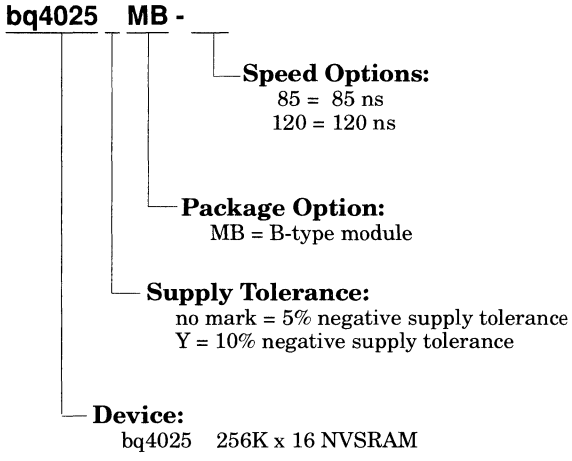
Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

Power-Down/Power-Up Timing



PD-B

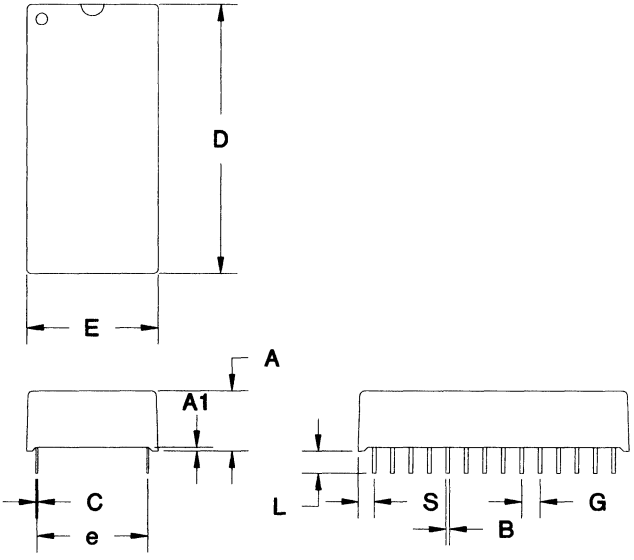
Ordering Information



6

Notes

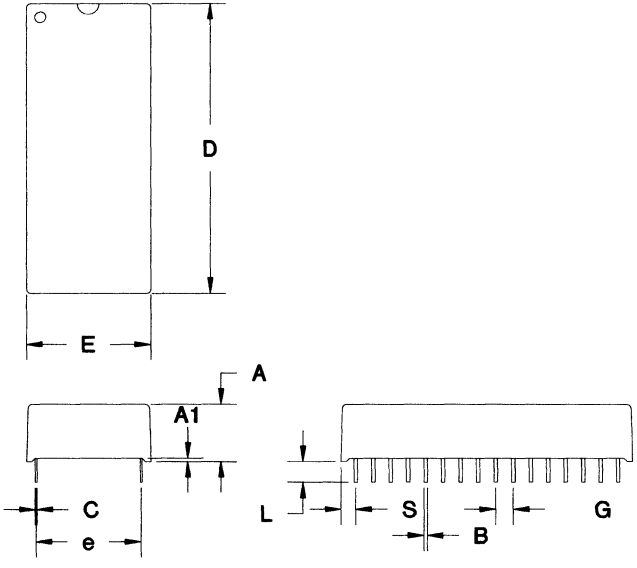
MA: 28-Pin A-Type Module



28-pin MA (A-type module)

Dimension	Minimum	Maximum	Units
A	0.365	0.375	inches
A1	0.015	-	inches
B	0.017	0.023	inches
C	0.008	0.013	inches
D	1.470	1.500	inches
E	0.710	0.740	inches
e	0.590	0.630	inches
G	0.090	0.110	inches
L	0.120	0.150	inches
S	0.075	0.110	inches

MA: 32-Pin A-Type Module

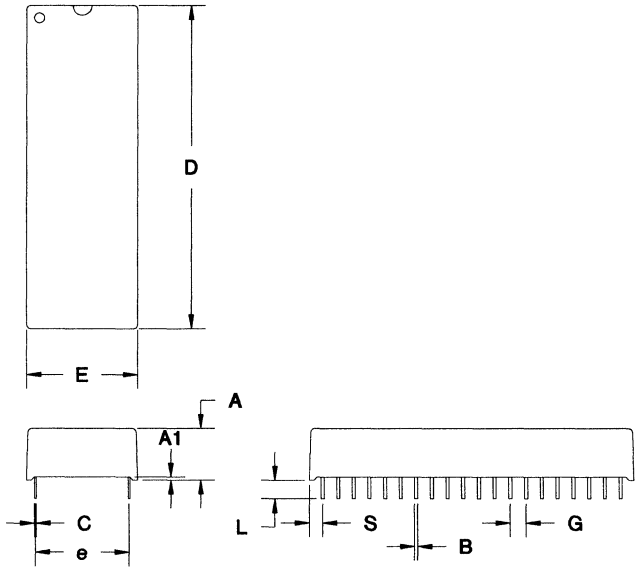


32-pin MA (A-type module)

Dimension	Minimum	Maximum	Units
A	0.365	0.375	inches
A1	0.015	-	inches
B	0.017	0.023	inches
C	0.008	0.013	inches
D	1.670	1.700	inches
E	0.710	0.740	inches
e	0.590	0.630	inches
G	0.090	0.110	inches
L	0.120	0.150	inches
S	0.075	0.110	inches

Package Drawings

MA: 40-Pin A-Type Module



40-pin MA (A-type module)

Dimension	Minimum	Maximum	Units
A	0.365	0.375	inches
A1	0.015	-	inches
B	0.017	0.023	inches
C	0.008	0.013	inches
D	2.070	2.100	inches
E	0.710	0.740	inches
e	0.590	0.630	inches
G	0.090	0.110	inches
L	0.120	0.150	inches
S	0.075	0.110	inches

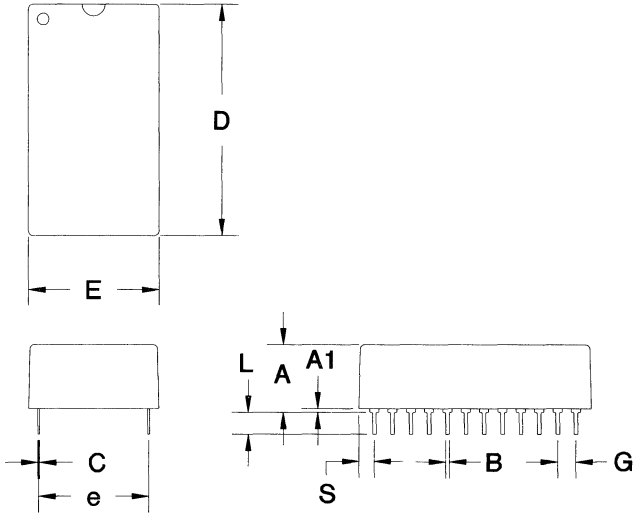
MB: 32-Pin B-Type Module

Package dimensions to be determined; contact sales office or factory.

MB: 40-Pin B-Type Module

Package dimensions to be determined; contact sales office or factory.

MT: 24-Pin T-Type Module

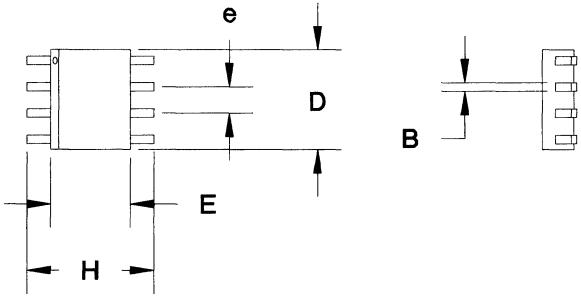


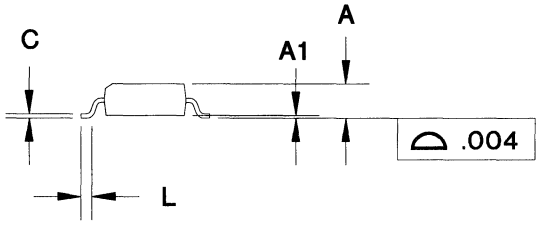
24-pin MT (T-type module)

Dimension	Minimum	Maximum	Units
A	0.360	0.375	inches
A1	0.015	-	inches
B	0.015	0.022	inches
C	0.008	0.013	inches
D	1.320	1.335	inches
E	0.685	0.700	inches
e	0.590	0.620	inches
G	0.090	0.110	inches
L	0.120	0.130	inches
S	0.100	0.120	inches

Package Drawings

SN: 8-Pin SOIC Narrow

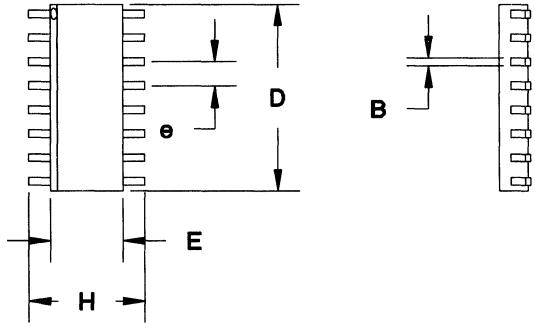


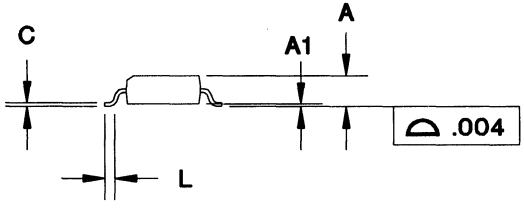


8-pin SOIC Narrow (SN)

Dimension	Minimum	Maximum	Units
A	0.060	0.070	inches
A1	0.004	0.010	inches
B	0.013	0.020	inches
C	0.007	0.010	inches
D	0.185	0.200	inches
E	0.150	0.160	inches
e	0.045	0.055	inches
H	0.225	0.245	inches
L	0.015	0.035	inches

SN: 16-Pin SOIC Narrow

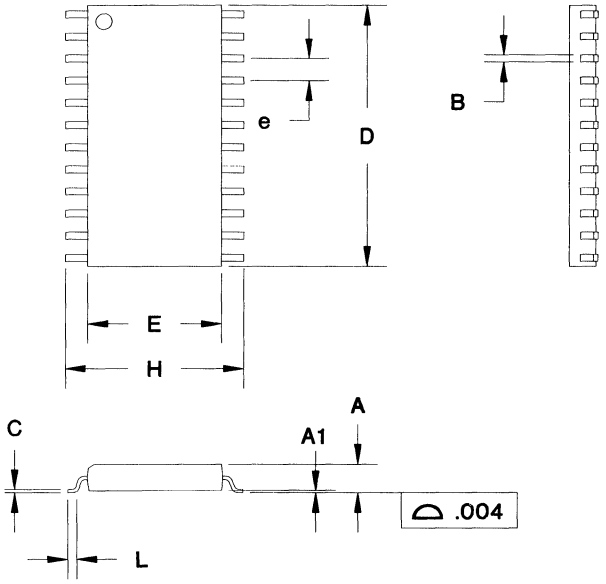




16-pin SOIC Narrow (SN)

Dimension	Minimum	Maximum	Units
A	0.060	0.070	inches
A1	0.004	0.010	inches
B	0.013	0.020	inches
C	0.007	0.010	inches
D	0.385	0.400	inches
E	0.150	0.160	inches
e	0.045	0.055	inches
H	0.225	0.245	inches
L	0.015	0.035	inches

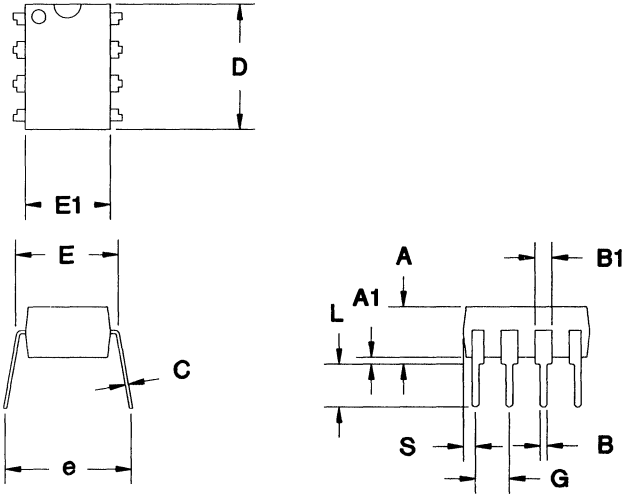
S: 24-Pin SOIC



24-pin SOIC (S)

Dimension	Minimum	Maximum	Units
A	0.095	0.105	inches
A1	0.004	0.012	inches
B	0.013	0.020	inches
C	0.008	0.013	inches
D	0.600	0.615	inches
E	0.290	0.305	inches
e	0.045	0.055	inches
H	0.395	0.415	inches
L	0.020	0.040	inches

PN: 8-Pin DIP Narrow

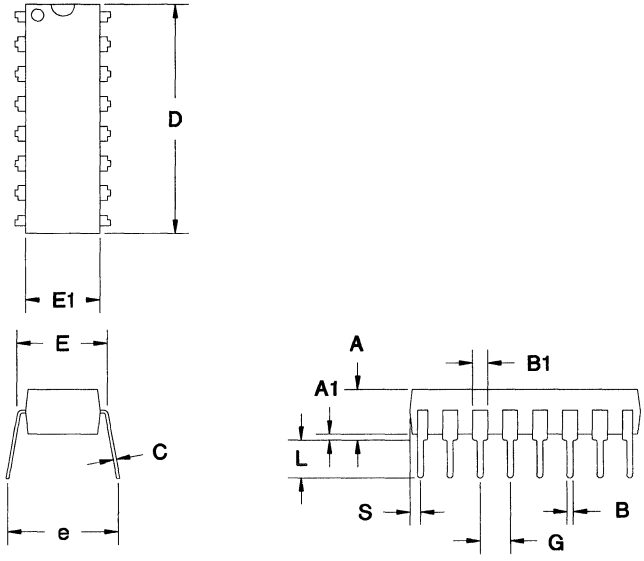


8-pin DIP Narrow (PN)

Dimension	Minimum	Maximum	Units
A	0.160	0.180	inches
A1	0.015	0.040	inches
B	0.015	0.022	inches
B1	0.055	0.065	inches
C	0.008	0.013	inches
D	0.350	0.380	inches
E	0.300	0.325	inches
E1	0.230	0.280	inches
e	0.300	0.370	inches
G	0.090	0.110	inches
L	0.115	0.150	inches
S	0.020	0.040	inches

Package Drawings

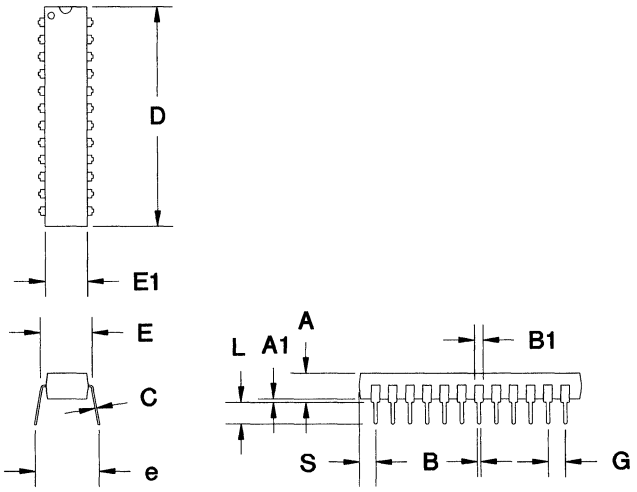
PN: 16-Pin DIP Narrow



16-pin DIP Narrow (PN)

Dimension	Minimum	Maximum	Units
A	0.160	0.180	inches
A1	0.015	0.040	inches
B	0.015	0.022	inches
B1	0.055	0.065	inches
C	0.008	0.013	inches
D	0.740	0.770	inches
E	0.300	0.325	inches
E1	0.230	0.280	inches
e	0.300	0.370	inches
G	0.090	0.110	inches
L	0.115	0.150	inches
S	0.020	0.040	inches

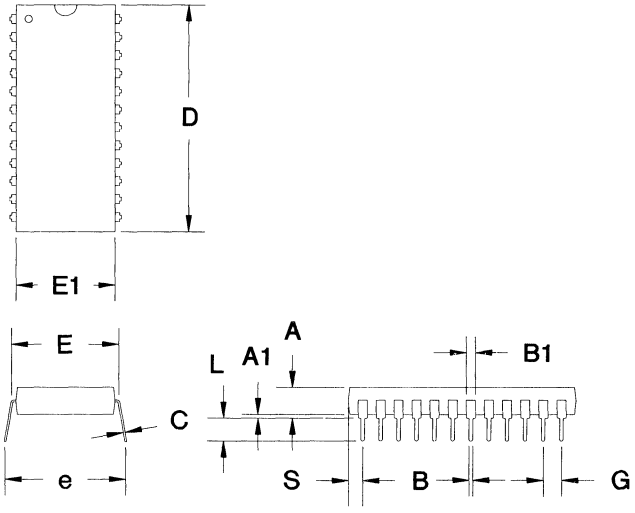
PN: 24-Pin DIP Narrow



24-pin DIP Narrow (PN)

Dimension	Minimum	Maximum	Units
A	0.160	0.190	inches
A1	0.015	0.040	inches
B	0.015	0.022	inches
B1	0.045	0.055	inches
C	0.008	0.013	inches
D	1.240	1.280	inches
E	0.300	0.325	inches
E1	0.250	0.300	inches
e	0.300	0.370	inches
G	0.090	0.110	inches
L	0.115	0.150	inches
S	0.070	0.090	inches

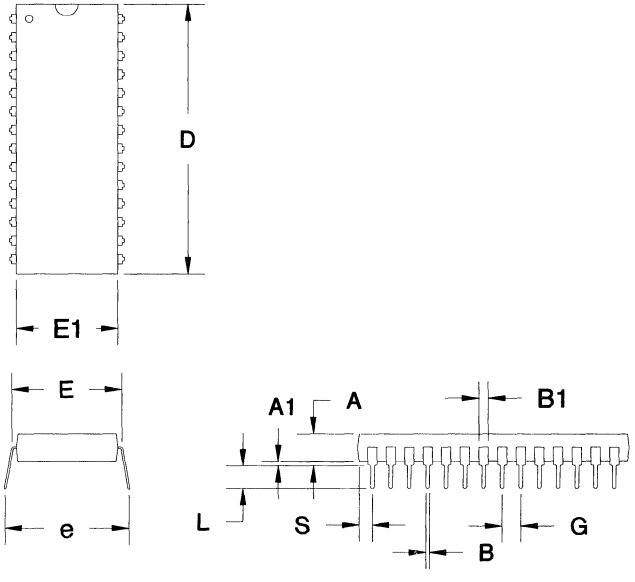
P: 24-Pin DIP



24-pin DIP (P)

Dimension	Minimum	Maximum	Units
A	0.160	0.190	inches
A1	0.015	0.040	inches
B	0.015	0.022	inches
B1	0.045	0.065	inches
C	0.008	0.013	inches
D	1.240	1.280	inches
E	0.600	0.625	inches
E1	0.530	0.570	inches
e	0.600	0.670	inches
G	0.090	0.110	inches
L	0.115	0.150	inches
S	0.070	0.090	inches

P: 28-Pin DIP

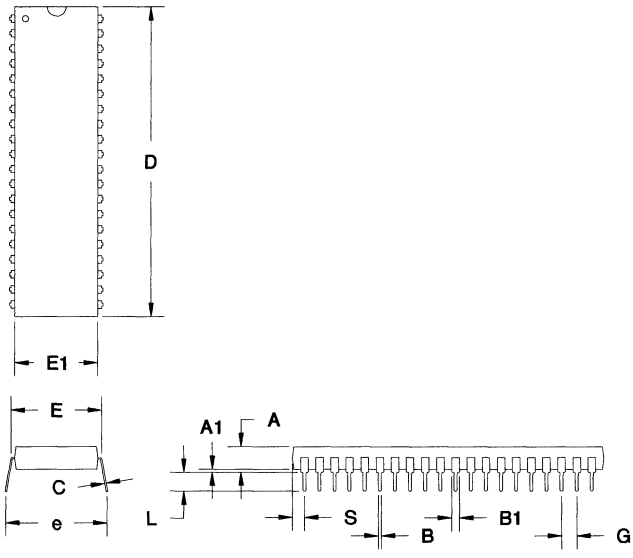


28-pin DIP (P)

Dimension	Minimum	Maximum	Units
A	0.160	0.190	inches
A1	0.015	0.040	inches
B	0.015	0.022	inches
B1	0.045	0.065	inches
C	0.008	0.013	inches
D	1.440	1.480	inches
E	0.600	0.625	inches
E1	0.530	0.570	inches
e	0.600	0.670	inches
G	0.090	0.110	inches
L	0.115	0.150	inches
S	0.070	0.090	inches

Package Drawings

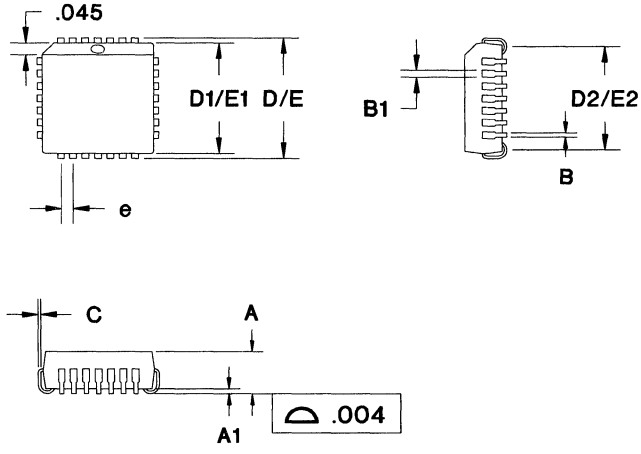
P: 40-Pin DIP



40-pin DIP (P)

Dimension	Minimum	Maximum	Units
A	0.160	0.190	inches
A1	0.015	0.040	inches
B	0.015	0.022	inches
B1	0.045	0.055	inches
C	0.008	0.013	inches
D	2.040	2.080	inches
E	0.600	0.625	inches
E1	0.530	0.570	inches
e	0.600	0.670	inches
G	0.090	0.110	inches
L	0.115	0.150	inches
S	0.070	0.090	inches

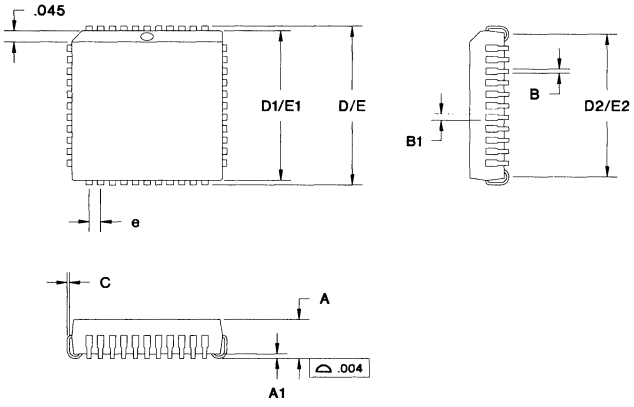
Q: 28-Pin Quad PLCC



28-pin Quad PLCC (Q)

Dimension	Minimum	Maximum	Units
A	0.165	0.180	inches
A1	0.020	-	inches
B	0.012	0.021	inches
B1	0.025	0.033	inches
C	0.008	0.012	inches
D	0.485	0.495	inches
D1	0.445	0.455	inches
D2	0.390	0.430	inches
E	0.485	0.495	inches
E1	0.445	0.455	inches
E2	0.390	0.430	inches
e	0.045	0.055	inches

Q: 44-Pin Quad PLCC



44-pin Quad PLCC (Q)

Dimension	Minimum	Maximum	Units
A	0.165	0.180	inches
A1	0.020	-	inches
B	0.012	0.021	inches
B1	0.025	0.033	inches
C	0.008	0.012	inches
D	0.685	0.695	inches
D1	0.645	0.655	inches
D2	0.590	0.630	inches
E	0.685	0.695	inches
E1	0.645	0.655	inches
E2	0.590	0.630	inches
e	0.045	0.055	inches

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