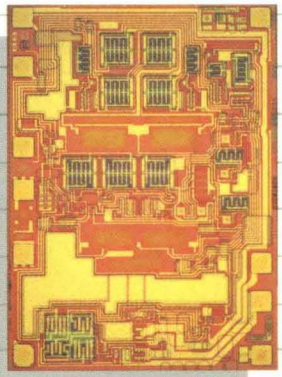
BURR-BROWN®

integrated circuits data book supplement vol. 33b



BURR-BROWN

integrated circuits data book supplement

volume 33b

BURR-BROWN®

Operational Amplifiers
Instrumentation Amplifiers
Isolation Amplifiers
Analog Circuit Functions
D/A Converters
A/D Converters
Voltage-to-Frequency Converters
Digital Signal Processing
DC/DC Converters

Model Index

Models with "S" page numbers are in this supplement. Other models are in Burr-Brown Integrated Circuits Data Book Volume 33.

Individual product data sheets for models not listed here are available from your local Burr-Brown salesperson or representative. See the listing on the inside back cover.

How To Use This Book

If you know the **MODEL NUMBER,**	Use the Model Index on the **INSIDE FRONT COVER.**
If you know the **PRODUCT TYPE,**	Use the **TABBED TABLE OF CONTENTS** on page *v*. Or, use the **SELECTION GUIDE TABLES** at the front of each tabbed section.
If you want **NEW MODELS,**	Use the Model Index on the **INSIDE FRONT COVER** or the **SELECTION GUIDE TABLES** at the front of each tabbed section. New models contained in this supplement are shown in boldface; for other models see *Burr-Brown Integrated Circuits Data Book Volume 33*. Contact your local Burr-Brown salesperson or representative for information on new models.
If you want a **PRICE,**	If you are in the USA, see the **USA PRICE LIST,** Section 16. If you are outside the USA, contact your local Burr-Brown salesperson or representative.
If you want **MILITARY** components,	Contact your local Burr-Brown salesperson or representative. See **INSIDE BACK COVER.**
If you want **DIE,**	Contact your local Burr-Brown salesperson or representative. See **INSIDE BACK COVER.**

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Burr-Brown Integrated Circuits Data Book Supplement

Volume 33b

BURR-BROWN®

About Burr-Brown

Burr-Brown Corporation is a leading designer and manufacturer of precision microcircuits and microelectronic-based systems for use in data acquisition, signal conditioning, measurement, and control.

We make our products for customers who pursue business success in the same way we do — through worldwide competition based on high performance, high quality, and high value. Our customers include OEMs, sophisticated end-users, systems integrators, and VARs who demand an extra measure of performance for their products and operations.

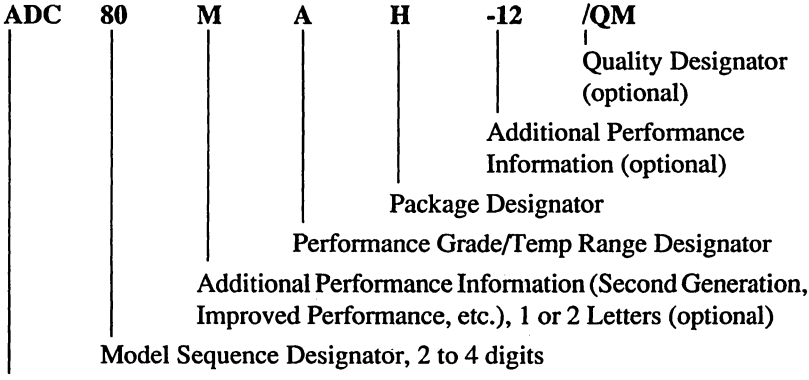
COMPANY FACTS

- ✔ Founded in 1956.
- ✔ Corporate headquarters: Tucson, Arizona, USA.
- ✔ 1450 employees.
- ✔ Manufacturing and technical facilities: Tucson; Livingston, Scotland; Atsugi, Japan.
- ✔ Sales and distribution subsidiaries in Austria, Belgium, England, France, Germany, Italy, Japan, the Netherlands, Sweden, and Switzerland; 19 international sales representative organizations worldwide.
- ✔ Superior customer service from more than 300 sales and service staff worldwide.
- ✔ 800+ high-performance products.

** See Burr-Brown Integrated Circuit Data Book Volume 33*

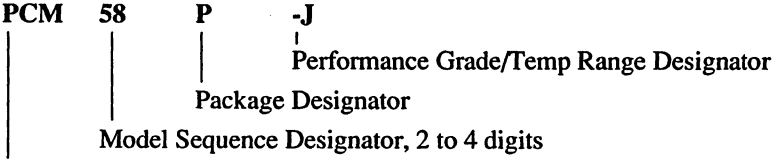
Understanding Component Model Numbers

Most Burr-Brown component products in this book have model numbers in the following form:



Exceptions: Second-source products are marked as similarly to the original vendor's part number as possible.

Some products designed for digital audio and signal processing applications have model numbers as follows:



Product Type Prefixes

Product Type	Prefix	Description
Amplifiers	OPA	Operational Amplifier
	INA	Instrumentation Amplifier
	PGA	Programmable Gain Amplifier
	ISO	Isolation Amplifier
Analog Circuit Functions	MFC	Multifunction Converter
	MPY	Multiplier
	DIV	Divider
	LOG	Logarithmic Amplifier
Frequency Products	VFC	Voltage-to-Frequency Converter
	UAF	Universal Active Filter
Conversion Products	ADC	A/D Converter
	ADS	A/D Converter with Sample/Hold
	DAC	D/A Converter
	DSP	Products Tailored Especially for Digital Signal Processing
	MPC	Multiplexer
	PCM	A/D and D/A Converters for Audio and Digital Signal Processing
	SDM	System Data Modules
	SHC	Sample/Hold
Miscellaneous	PWS	Power Supply
	PWR	Power Supply
	REF	Reference
	XTR	Transmitter
	RCV	Receiver

Performance Grade and Temperature Range Designators

	Temperature Range		
	0°C to 70°C (Commercial)	–25°C to +85°C [1] (Industrial)	–55°C to +125°C (Military)
Increasing Parametric Performance ↓	H	A	R
	J	B	S
	K	C (best)	T (best)
	L (best)		

NOTE: (1) For some industrial products this may be –40°C to 85°C.

Package Designators

M	Metal (hermetic)
P	Plastic DIP (nonhermetic)
G	Ceramic (hermetic or nonhermetic)
U	SOIC
N	PLCC
L	Ceramic Leadless Chip Carrier
D	Die
H	Ceramic hermetic

Quality Designators

Q	Burr-Brown's Q program
QM or /QM	Burr-Brown's Q program with Military Visual Criteria
BI or B	Burn-in

Where To Go From Here: Burr-Brown Sales & Service

The *Burr-Brown Integrated Circuits Data Book Supplement Vol. 33b* contains an extensive variety of new precision microcircuits. These have been introduced since the January 1989 publication of the 1300-page *Burr-Brown Integrated Circuits Data Book Vol. 33*, which is available free upon request from your local salesperson or by calling **1-800-548-6132** (USA only). With both books, you will have an up-to-date collection of product data sheets on all commercial Burr-Brown IC parts.

ABOUT THIS BOOK

All Burr-Brown models are listed in Selection Guide tables at the beginning of each tabbed section. With these tables you can quickly compare specs among different models and choose the best part for your design. Complete product data sheets for items in **bold** are in this book, starting on the referenced page. Items not in bold are in the larger IC Data Book.

Data sheets are arranged alphanumerically, so if you know the name of the part you can find it quickly. Or, use the Model Index on the **inside front cover.** There you'll find models in this book in **bold** and arranged alphanumerically, along with models indexed from the larger IC Data Book. Throughout this book the prefix 'S' designates page numbers for the Data Book Supplement.

SUPERIOR CUSTOMER SERVICE

Burr-Brown gives you the best customer service in the industry — whether you need additional technical literature, technical assistance from factory-trained applications engineers, to place an order, or to return products. For immediate assistance with any of the following, contact your local Burr-Brown salesperson or representative. See the **inside back cover.** Or, in the USA call our Customer Service Center at **1-800-548-6132.**

Technical Literature — In addition to individual data sheets, Burr-Brown has an extensive library of other useful publications. A brief summary: *IC Data Book, Vol. 33* (1/89); *Power Sources Handbook, Vol. 2* (8/90); reliability reports, application notes and handbook, *UPDATE, Design Update*, our applications engineering newsletter. We also offer a comprehensive product selection guide on a PC diskette. The same information is available via our Electronic Bulletin Board Service (see below).

Other Technical Information — Application engineers are available during working hours to help you with product selection, design advice, troubleshooting, documentation, etc. Call customer service at **1-800-548-6132** (USA only).

Electronic Bulletin Board Service — Computer-based information system offers up-to-date product announcements, application notes/suggestions, software/utilities (for example, pSPICE models), tech support message center, and E-mail. Available 24 hours per day at no charge, except for toll call. Use these settings: 300/1200/2400 8-N-1; XMODEM file transfer. BBS number is (602) 741-3978.

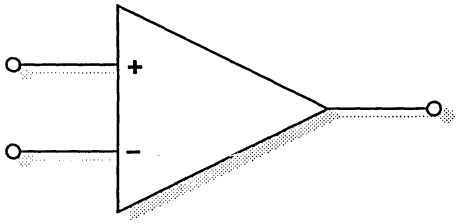
Placing Orders — You can place orders via telephone, FAX, mail, TWX, or Telex with any authorized Burr-Brown field sales office, sales representative, or our Tucson headquarters. A complete list of sales offices is on the inside back cover of this book. For more information about placing an order, contact your local Burr-Brown salesperson or representative. See the **inside back cover.** Or, call customer service at **1-800-548-6132** (USA only).

If the products you want are readily available off the shelf, you can pay for them with your **VISA** or **MasterCard.** For more information, call customer service at **1-800-548-6132.**

Prices and Quotations — Prices in this book (USA only) are USA OEM prices and are subject to change. Price quotations made by Burr-Brown or its authorized field sales representatives are valid for 30 days. Delivery quotations are subject to reconfirmation at the time of order placement. For more information about pricing, contact your local Burr-Brown salesperson or representative. Or, call customer service at **1-800-548-6132** (USA only).

Returns and Warranty Service — When returning products for any reason, contact Burr-Brown prior to shipping for authorization and shipping instructions. For complete instructions, contact your local Burr-Brown sales office or representative. In the USA, call our Customer Service Center at **1-800-548-6132.**

Please ship returned units prepaid and supply the original purchase order number and date, along with an explanation of the malfunction. Upon receipt of the returned unit and your RMA number, Burr-Brown will verify the malfunction and inform you of the warranty status, cost to repair or replace, credits, and status of replacement units where applicable.



OPERATIONAL AMPLIFIERS

2

APPLICATION GROUPS

Burr-Brown operational amplifiers are listed in eight applications groups described below. This helps you determine and select the best operational amplifier available for a design. Instrumentation amplifiers and isolation amplifiers are described in Sections 3 and 4 respectively.

LOW DRIFT

Low drift operational amplifiers are best suited for applications where accuracy must be preserved over a substantial temperature range. These amplifiers are optimized to minimize the initial input offset voltage and input offset voltage change with temperature. Input offset drifts from 0.1μV/°C to 5μV/°C are available within this group.

LOW BIAS CURRENT

Low bias current operational amplifiers consist of FET input designs. This group includes amplifiers with input bias currents from 0.01pA to 50pA. Applications with large feedback resistances or large source resistances (long time constants, integrators, current sources, etc.) and buffer applications will benefit by the use of low bias current amplifiers.

LOW NOISE

This group contains low noise bipolar and FET input operational amplifiers. Burr-Brown units offer guaranteed noise spectral density, 100% tested. In applications such as low noise signal conditioning, light measurements, radiation measurements, photodiode circuits or low noise data acquisition, the fully characterized and tested voltage noise performance of these units allows the designer to truly bound noise errors.

WIDEBAND

Wideband operational amplifiers have bandwidths greater than 5MHz. This group also contains fast settling and high slew rate amplifiers. These amplifiers reduce phase errors at high frequencies and accurately reproduce complex waveforms. These amplifiers are well suited for pulse, video, fast settling, and multiplexing applications.

HIGH VOLTAGE

Amplifiers in this group are designed to provide large output voltage swings and to operate on wide ranges of supply voltage. Output voltages from ±10V and ±145V (up to 290V, single supply) are available in this applications group. These amplifiers provide good frequency response and performance in other parameters. Most models have electrically isolated packages and automatic thermal sensing and shutdown. All units have FET inputs to minimize bias current errors when the amplifier is used with the large resistances usually found with high-voltage amplifiers.

HIGH CURRENT

These amplifiers provide output currents from ±1A to ±10A. They are used with small load resistances, coax cable driving, and with power booster applications. Many units have self-contained thermal sensing and shutdown to automatically protect the amplifiers from overheating and damage. All of these units have electrically isolated packages.

UNITY-GAIN BUFFER (POWER BOOSTER)

Unity-gain buffer amplifiers have a wide variety of applications. They are used to boost the output current capability of another amplifier, buffer an impedance that might load a critical circuit or to be an input impedance converter from an input that must not be loaded. These amplifiers may also be used inside the feedback loop of another operational amplifier to form a current-boosted composite amplifier.

SPECIAL PURPOSE

Special purpose op amps provide features or performance that don't fit conventional categories. These include op amps specified for very wide temperature range and devices with switchable inputs.

OPERATIONAL AMPLIFIERS SELECTION GUIDES

The following Selection Guides show parameters for the high grade. Refer to the Product Data Sheet for a full selection of grades. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book.*

LOW DRIFT

Low offset voltage drift vs temperature performance in both FET and bipolar input types is obtained by our sophisticated drift compensation techniques. First, the drift is measured and then special laser trim techniques are used to minimize the drift and the initial offset voltage at 25°C. Finally, "max drift" performance is retested for conformance with specifications.

LOW DRIFT OPERATIONAL AMPLIFIERS (≤5µV/°C) — **Boldface = NEW**

Description	Model	Offset Voltage, max: At 25°C, (±mV)	Offset Voltage, max: Temp Drift, (±µV/°C)	Bias Current (25°C), max (nA)	Open Loop Gain, min (dB)	Frequency Response: Unity Gain (MHz)	Frequency Response: Slew Rate (V/µs)	Rated Output, min: (±V)	Rated Output, min: (±mA)	Temp Range[1]	Pkg	Page No.
FET	**OPA627M**	**0.1**	**1**	**20**	**110**	**16**	**45**	**11.5**	**30**	**Ind**	**TO-99**	**S2-74**
	OPA627P	**0.25**	**2**	**50**	**104**	**16**	**40**	**11.5**	**30**	**Ind**	**DIP**	**S2-74**
	OPA637M	**0.1**	**1**	**20**	**110**	**50**	**100**	**11.5**	**30**	**Ind**	**TO-99**	**S2-74**
	OPA637P	**0.25**	**2**	**50**	**104**	**50**	**100**	**11.5**	**30**	**Ind**	**DIP**	**S2-74**
	OPA111M	0.25	1	±0.001	120	2	2	11	5	Ind	TO-99	2-55
Wideband	OPA156M	2	5	0.05	94	6	14	10	5	Mil	TO-99	2-80
	OPA356M	2	5	0.05	94	6	14	10	5	Com	TO-99	2-80
	OPA602M	0.25	2	±.001	92	6.5	28	10	15	Ind	TO-99	2-145
	OPA602P, U	0.5	5	±.002	88	6.5	24	10	15	Ind	DIP, SOIC	2-145
	OPA606M	0.5	5	±0.01	100	13	35	12	5	Com	TO-99	2-158
Dual FET	OPA2111M	0.5	2.8	±0.004	114	2	2	11	5	Ind	TO-99	2-195
	OPA2107P	**0.5**	**5**	**0.006**	**80**	**5**	**15**	**11**	**10**	**Ind**	**DIP, SOIC**	**S2-114**
Low Power (Dual) Single Supply Operation	**OPA1013**	**0.15**	**2**	**20**	**123**	**0.8**	**0.4**	**13**	**5**	**Com**	**DIP, TO-99**	**S2-104**
Bipolar	**OPA177Z, P**	**0.01**	**0.1**	**1.5**	**134**	**0.6**	**0.3**	**12**	**10**	**Ind**	**DIP**	**S2-13**
	OPA177S	**0.06**	**1.2**	**2.8**	**126**	**0.6**	**0.3**	**12**	**10**	**Ind**	**SOIC**	**S2-13**
	OPA77Z, P	**0.025**	**0.3**	**2.0**	**134**	**0.6**	**0.3**	**12**	**10**	**Ind**	**DIP**	**S2-13**
	OPA27J, Z	0.025	0.6	±40	120	8	1.9[3]	12	16.6	Mil	TO-99, DIP	2-27, 2-27
	OPA37J, Z	0.025	0.6	±40	120	63[2]	11.9[3]	12	16.6	Mil	TO-99, DIP	2-27, 2-27
	OPA27P, U	0.100	1.8	±80	117	8	1.9[3]	12	16.6	Com	DIP, SOIC	2-27
	OPA37P, U	0.100	1.8	±80	117	63[2]	11.9[3]	12	16.6	Com	DIP, SOIC	2-27

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) Gain-bandwidth product for OPA37. A_V = 5 min. (3) Typical.

LOW BIAS CURRENT

Our many years of experience in designing, manufacturing and testing FET amplifiers give us unique abilities in providing low and ultra-low bias current op amps. These amplifiers offer bias currents as low as 75fA (75 x 10^{-15}A) and voltage drift as low as 1µV/°C. With offset voltage laser-trimmed to as low as 250µV, the need for expensive trim pot adjustments is eliminated.

LOW BIAS CURRENT OPERATIONAL AMPLIFIERS (≤50pA) — **Boldface = NEW**

Description	Model	Offset Voltage, max: At 25°C, (±mV)	Offset Voltage, max: Temp Drift, (±µV/°C)	Bias Current (25°C), max (pA)	Open Loop Gain, min (dB)	Frequency Response: Unity Gain (MHz)	Frequency Response: Slew Rate (V/µs)	Rated Output, min: (±V)	Rated Output, min: (±mA)	Temp Range[1]	Pkg	Page No.
FET	OPA111M	0.25	1	±1	120	2	2	11	5	Ind	TO-99	2-55
	OPA627M	**0.1**	**1**	**20**	**110**	**16**	**45**	**12**	**30**	**Ind**	**TO-99**	**S2-74**
	OPA627P	**0.25**	**2**	**50**	**104**	**16**	**40**	**12**	**30**	**Ind**	**DIP**	**S2-74**
	OPA637M	**0.1**	**1**	**20**	**110**	**50**	**100**	**11.5**	**30**	**Ind**	**TO-99**	**S2-74**
	OPA637P	**0.25**	**2**	**50**	**104**	**50**	**100**	**11.5**	**30**	**Ind**	**DIP**	**S2-74**
Low Noise	OPA101M	0.25	5	–10	94	10	6.5	12	12	Ind	TO-99	2-43
	OPA102M	0.25	5	–10	94	40	14	12	12	Ind	TO-99	2-43
Ultra-Low Bias Current	OPA128M	0.5	5	±0.075	110	1	3	10	5	Com	TO-99	2-72
	AD515H	1	25	0.075	88	0.35	1	10	5	Com	TO-99	2-13
Dual FET	OPA2111M	0.5	2.8	±4	114	2	2	11	5	Ind	TO-99	2-195
	OPA2111P	2	15	±15	106	2	2	11	5	Com	DIP	2-195
	OPA2107P	**0.5**	**5**	**6**	**80**	**5**	**15**	**11**	**10**	**Ind**	**DIP, SOIC**	**S2-114 S2-114**
Quad FET	OPA404G	0.75	3[2]	±4	92	6.4	35	12	5	Ind	DIP	2-94
	OPA404P, U	2.5	5[2]	±12	88	6.4	35	11.5	5	Com	DIP, SOIC	2-94
Low Cost	OPA121M	2	10	±5	110	2	2	11	5	Com	TO-99	2-66
	OPA121P, U	3	10	±10	106	2	2	11	5	Com	DIP, SOIC	2-66
	OPA602M	0.25	2	1	92	6.5	28	10	15	Ind	TO-99	2-145
	OPA602P	0.5	5	2	88	6.5	24	10	15	Ind	DIP, SOIC	2-145
Wideband	OPA606M	0.5	5	±10	100	13	35	12	5	Com	TO-99	2-158
	OPA606P	3	10[2]	±25	90	12	30	11	5	Com	DIP	2-158

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) Typical.

LOW NOISE

Now both FET and bipolar input op amps are offered with guaranteed low noise specifications. Until now the designer had to rely on "typical" specs for his demanding low noise designs. These fully characterized parts allow a truly complete error budget calculation.

LOW NOISE OPERATIONAL AMPLIFIERS (Very Low e_N) — **Boldface = NEW**

Description	Model	Noise Voltage at 10kHz, max (nV/√Hz)	Bias Current (25°C), max (pA)	Offset Voltage, max: at 25°C (±mV)	Offset Voltage, max: Temp Drift (±µV/°C)	Open Loop Gain, min (dB)	Frequency Response: Gain BW (MHz)	Frequency Response: Slew Rate, min (V/µs)	Rated Output, min: (±V)	Rated Output, min: (±mA)	Temp Range[1]	Pkg	Page No.
Bipolar	OPA27J, Z	3.8	±40nA	0.025	0.6	120	8	1.9[2]	12	16.6	Mil	TO-99, DIP	2-27
	OPA37J, Z	3.8	±40nA	0.025	0.6	120	63	11.9[2]	12	16.6	Mil	TO-99, DIP	2-27
	OPA177Z, P	**10**	**1.5**	**0.01**	**0.1**	**134**	**0.6**	**0.3**	**12**	**10**	**Ind**	**DIP**	**S2-13**
	OPA177S	**10**	**2.8**	**0.06**	**1.2**	**126**	**0.6**	**0.3**	**12**	**10**	**Ind**	**SOIC**	**S2-13**
	OPA77Z, P	**11**	**2.0**	**0.025**	**0.3**	**134**	**0.6**	**0.3**	**12**	**10**	**Ind**	**DIP**	**S2-13**

(Continued on next page)

LOW NOISE OPERATIONAL AMPLIFIERS (Very Low e_N) (Continued) **Boldface = NEW**

Description	Model	Noise Voltage at 10kHz, max (nV/√Hz)	Bias Current (25°C), max (pA)	Offset Voltage, max at 25°C (±mV)	Offset Voltage, max Temp Drift (±µV/°C)	Open Loop Gain, min (dB)	Frequency Response Gain BW (MHz)	Frequency Response Slew Rate, min (V/µs)	Rated Output, min (±V)	Rated Output, min (±mA)	Temp Range[1]	Pkg	Page No.
Wide Bandwidth	OPA101M	8	–10	0.25	5	94	20	5	12	12	Ind	TO-99	2-43
	OPA102M	8	–10	0.25	5	94	40	10	12	12	Ind	TO-99	2-43
FET	OPA111M	8	±1	0.25	1	120	2	1	11	5	Ind	TO-99	2-55
	OPA602M	12[2]	1	0.25	2	92	6.5	28	10	15	Ind	TO-9	2-145
	OPA627M	**5.4**	**20**	**1**	**0.8**	**110**	**16**	**45**	**11.5**	**30**	**Ind**	**TO-99**	**S2-74**
	OPA627P	**6.2**	**50**	**0.25**	**2**	**104**	**16**	**40**	**11.5**	**30**	**Ind**	**DIP**	**S2-74**
	OPA637M	**5.4**	**20**	**1**	**0.8**	**110**	**50**	**100**	**11.5**	**30**	**Ind**	**TO-99**	**S2-74**
	OPA637P	**6.2**	**50**	**0.25**	**2**	**104**	**50**	**100**	**11.5**	**30**	**Ind**	**DIP**	**S2-74**
Low Cost	OPA27P, U	4.5	±80nA	0.100	1.8	117	8	1.9[2]	10	16.6	Com	DIP, SOIC	2-27
	OPA37P, U	4.5	±80nA	0.100	1.8	117	63	11.9[2]	10	16.6	Com	DIP, SOIC	2-27
Dual FET	OPA2111M	8	±4	0.5	2.8	114	2	1	11	5	Ind	TO-99	2-195
	OPA2111P	6[2]	±15	2	15	106	2	1	11	5	Com	DIP	2-195
Dual Audio Op Amp	**OPA2604**	**10**	**100**	**2**	**5**	**100**	**10**	**15**	**12**	**20**	**Ind**	**DIP, SOIC**	**S2-122 S2-122**

NOTES: (1) Ind = –25°C to +85°C, Mil = –55°C to +125°C, Com = 0°C to +70°C. (2) Typical.

UNITY-GAIN BUFFER (POWER BOOSTER)

These versatile amplifiers boost the ouput current capability of another amplifier; buffer an impedance that might load a critical circuit; and may be used inside the feedback loop of another op amp to form a current-boosted, composite amplifier. Currents as high as ±200mA are available with speeds of 2000V/µs.

UNITY-GAIN BUFFER OPERATIONAL AMPLIFIERS **Boldface = NEW**

Description	Model	Rated Output, min (±V)	Rated Output, min (±mA)	Frequency Responses –3dB (MHz)	Frequency Responses Full Power (MHz)	Frequency Responses Slew Rate (V/µs)	Gain (V/V)	Input Impedance (Ω)	Temp Range[1]	Pkg	Page No.
High Performance	3553AM	10	200	300	32	2000	≈1	10^{11}	Ind	TO-3	2-225
Low Cost	OPA633H, P	11	80	275	65	2500	≈1	1.5×10^6	Ind	TO-8, DIP	2-176
Transconductance Amp and Buffer	**OPA660**	**4**	**8**	**700**	**550**	**2000**	**≈1**	**10^6**	**Ind**	**DIP, SOIC**	**S2-88**

NOTE: (1) Ind = –25°C to +85°C.

WIDE BANDWIDTH

Design expertise in wideband circuits combines with our fully developed technology to create cost-effective wideband op amps. Burr-Brown high-speed amplifiers also offer outstanding DC performance specifications.

WIDE BANDWIDTH OPERATIONAL AMPLIFIERS (≥5MHz) — **Boldface = NEW**

		Frequency Response				Rated Output, min		Offset Voltage, max		Open Loop Gain, min			
Description	Model	Gain BW (MHz)	Slew Rate min (V/µs)	t_s ±0.1% (ns)	Comp	(±V)	(±mA)	At 25°C (±mV)	Temp Drift (±µV/°C)	(dB)	Temp Range[1]	Pkg	Page No.
FET	OPA156M	6	10	1.5µs	int	10	5	2	5	94	Mil	TO-99	2-80
	OPA356M	6	10	1.5µs	int	10	5	2	5	94	Com	TO-99	2-80
	OPA602M	6.5	28	600	int	10	15	0.25	2	92	Ind	TO-99	2-145
	OPA602P, U	6.5	24	600	int	10	15	0.5	5	88	Ind	DIP, SOIC	2-145
Dual	**OPA2107**	**5**	**15**	**1µs**	**int**	**11**	**10**	**0.5**	**5**	**82**	**Ind, Mil**	**DIP, TO-99, SOIC**	**S2-114, S2-114, S2-114**
Dual Audio	**OPA2604**	**10**	**25**	**2**	**int**	**10**	**20**	**1**	**5 typ**	**82**	**Ind**	**DIP, TO-99**	**S2-122, S2-122**
Op Amp	OPA605M	200, A=1000	300[3]	300	ext	10	30	0.5	5	96[3]	Ind	DIP	2-152
	OPA606M	13	25	1µs	int	12	5	0.5	5[2]	100	Com	TO-99	2-158
	OPA606P	12	20	1µs	int	11	5	3	10[2]	90	Com	TO-99	2-158
	OPA627M	**16**	**45**	**400**	**int**	**11.5**	**30**	**0.1**	**1**	**110**	**Ind**	**TO-99**	**S2-74**
	OPA627P	**16**	**40**	**400**	**int**	**11.5**	**30**	**0.25**	**2**	**104**	**Ind**	**DIP**	**S2-74**
	OPA637M	**50**	**100**	**300**	**G>5**	**11.5**	**30**	**0.1**	**1**	**110**	**Ind**	**TO-99**	**S2-74**
	OPA637P	**50**	**100**	**300**	**G>5**	**11.5**	**30**	**0.25**	**2**	**104**	**Ind**	**DIP**	**S2-74**
	3554M	1700, A=1000	1000	120	ext	10	100	1	15	100	Ind	TO-3	2-229
	3551	50, A=10	250	400	ext	10	10	1	50[2]	88	Com	TO-99	2-221
	3550	20, A=1	100	400	int	10	10	1	50[2]	88	Com	TO-99	2-217
Bipolar	3507	20, A=10	80	200	ext	10	10	10	30[2]	83	Com	TO-99	2-213
Current-Feedback	**OPA603P**	**50 (G=1 to 50)**	**1000**	**50**	**NA**	**10**	**75**	**5**	**8 typ**	**NA**	**Ind**	**DIP**	**S2-30**
Transconductance Amp and Buffer	**OPA660**	**700**	**2000**	**25**	**NA**	**4.0**	**20**	**20**	**50**	**NA**	**Ind**	**DIP, SOIC**	**S2-88**
Quad FET	OPA404G	6.4	28	600	int	11.5	5	0.75	3[2]	92	Ind	DIP	2-94
	OPA404P, U	6.4	24	600	int	11.5	5	2.5	5[2]	88	Com	DIP, SOIC	2-94
Low Noise Bipolar	OPA27	8,A=1	1.9[2]	—	int[3]	12	16.6	0.025	0.6	120	Mil	TO-99, DIP	2-27
	OPA37	63,A=5	11.9[2]	—	int[3]	12	16.6	0.025	0.6	120	Mil	TO-99, DIP	2-27
Low Noise FET	OPA101M	20, A=100	5	2.5µs	int	12	12	0.25	5	94	Ind	TO-99	2-43
	OPA102M	40, A=100	10	1.5µs	int	12	12	0.25	5	94	Ind	TO-99	2-43
Fast Settling	OPA600M	5000, A=1000	500	80	ext	9	180	4	40	86	Ind	DIP	2-137

(Continued on next page)

WIDE BANDWIDTH OPERATIONAL AMPLIFIERS (≥5MHz) (Continued) **Boldface = NEW**

Description	Model	Frequency Response: Gain BW (MHz)	Slew Rate min (V/µs)	t_s ±0.1% (ns)	Comp	Rated Output, min (±V)	Rated Output, min (±mA)	Offset Voltage, max: At 25°C (±mV)	Offset Voltage, max: Temp Drift (±µV/°C)	Open Loop Gain, min (dB)	Temp Range[1]	Pkg	Page No.
Very Fast	**OPA620**	**200**	**175[2]**	**10**	**int**	**3**	**150[2]**	**0.5**	**8[2]**	**55**	**Com, Mil**	**DIP, SOIC**	**S2-42 S2-42**
Settling Precision	**OPA621**	**500, A=10**	**350[2]**	**15**	**int**	**3**	**150[2]**	**0.5**	**12[2]**	**55**	**Com, Mil**	**DIP, SOIC**	**S2-48 S2-48**
Very Fast Settling	**OPA675G**	**3000, A=16**	**240**	**15**	**ext**	**2.1**	**30[2]**	**1**	**5**	**65**	**Com, Mil**	**DIP**	**S2-90**
Switched Input	**OPA676G**	**3000, A=16**	**240**	**15**	**ext**	**2.1**	**30[2]**	**1**	**5**	**65**	**Com, Mil**	**DIP**	**S2-90**
Low Cost	OPA27P, U	8,A=1	1.9[2]	—	int	12	16.6	0.100	1.8	117	Com	DIP, SOIC	2-27
	OPA37P, U	63, A=5	11.9[2]	—	int[3]	12	16.6	0.100	1.8	117	Com	DIP, SOIC	2-27

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) Typical. (3) G = 5 min for OPA37.

HIGH VOLTAGE, HIGH CURRENT OPERATIONAL AMPLIFIERS **Boldface = NEW**

Description	Model	Rated Output, min (±V)	Rated Output, min (±mA)	Offset Voltage, max: At 25°C (±mV)	Offset Voltage, max: Temp Drift (±µV/°C)	Bias Current (25°C), max (pA)	Frequency Response: Unity Gain (MHz)	Frequency Response: Slew Rate (V/µs)	Open Loop Gain (dB)	Temp Range[1]	Pkg	Page No.
High Power	OPA501M	26	10A	5	40	20nA	1	1.35	98	Ind	TO-3	2-109
	OPA511M	22	5A	10	65	40	1	1	91	Ind	TO-3	2-117
	OPA512BM	35	10A	6	65	30	4	2.5	110	Ind	TO-3	2-122
	OPA512SM	35	15A	3	40	20	4	2.5	110	Mil	TO-3	2-122
	OPA541M	**35**	**5A**	**1**	**30**	**50**	**1.6**	**6**	**90**	**Ind**	**TO-3**	**S2-22**
	OPA541AP	**30**	**5A**	**10**	**40**	**50**	**1.6**	**6**	**90**	**Ind**	**Power Plastic**	**S2-22**
(Dual)	OPA2541M	35	5A	1	30	50	1.6	8	90	Ind	TO-3	2-205
	3573M	20	2A[4]	10	65	40nA	1	2.6	94	Ind	TO-3	2-243
Wideband	3554M	10	100	1	15	50	1700[2]	1200	100	Ind	TO-3	2-229
High Voltage	3584M	145	15	3	25	20	20[2]	150	126	Com	TO-3	2-255
	3583M	140	75	3	25	20	5	30	118	Ind	TO-3	2-251
	3582	145	15	3	25	20	5	20	118	Com	TO-3	2-247
	3581	70	30	3	25	20	5	20	112	Com	TO-3	2-247
	3580	30	60	10	30	50	5	15	106	Com	TO-3	2-247
	OPA445BM	35	15	3	10	50	2	10	100	Ind	TO-99	2-104
Buffer	3553M	10	200	50	300[5]	200	300	2000	NA	Ind	TO-3	2-225
	OPA633	11	80	15	33[5]	35µA	275[5]	2500	NA	Ind	DIP	2-176

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) Gain-bandwidth product. (3) 2A peak. (4) 5A peak. (5) Typical.

SPECIAL PURPOSE

These op amps offer specialized performance or function, including devices with wide temperature range, low quiescent current, and switched inputs.

SPECIAL PURPOSE OPERATIONAL AMPLIFIERS — **Boldface = NEW**

Description	Model	Offset Voltage, max: At 25°C, (±mV)	Offset Voltage, max: Temp Drift, (±µV/°C)	Bias Current (25°C), max (nA)	Open Loop Gain, min (dB)	Frequency Response: Unity Gain (MHz)	Frequency Response: Slew Rate (V/µs)	Rated Output, min: (±V)	Rated Output, min: (±mA)	Temp Range[1]	Pkg	Page No.
Very Fast Settling	**OPA675G**	**1**	**5**	**35µA**	**65**	**185[2]**	**350**	**2.1**	**30**	**Com, Mil**	**DIP**	**S2-90**
	OPA676G	**1**	**5**	**35µA**	**65**	**185[2]**	**350**	**2.1**	**30**	**Com, Mil**	**DIP**	**S2-90**

NOTES: (1) Com = 0°C to +70°C, Mil = –55°C to +125°C. (2) –3dB BW at Gain of +10V/V.

Models STILL available but not featured in this book

Model	Description	Recommended Newer Model	Equivalency[1]
3329/03	Hybrid Power Booster	OPA633	F/E
3500	Low Bias Current Op Amp	OPA27	F/E
3501	Low Bias Current Op Amp	OPA111	P/P
3510	Low Drift Op Amp	OPA27	F/E
3521	Low Drift Op Amp	OPA111	P/P
3522	Low Drift Op Amp	OPA111	P/P
3523	Low Bias Current Op Amp	OPA128	P/P
3527	Low Drift FET Op Amp	OPA111	P/P
3528	Low Bias Current Op Amp	OPA128	P/P
3542	FET Input Op Amp	OPA121[2]	P/P
OPA37HT	Wide Temp Op Amp	OPA11HT	P/P
OPA103	Low Bias Current Op Amp	OPA128	P/P
OPA104	Low Bias Current Op Amp	OPA128	P/P
DEM102	Demo Kit for ISO102		
DEM106	Demo Kit for ISO106		

NOTES: (1) P/P = Pin for Pin. A true second source. F/E = Functional Equivalent. Very similar function, very similar performance, but not pin for pin. C/P = Closest Part. Similar function, similar performance, but significant differences exist. (2) Supply Range for OPA121 is ±5V to ±18V (instead of ±5V to ±20V).

OPERATIONAL AMPLIFIERS GLOSSARY

COMMON-MODE INPUT IMPEDANCE

Effective impedance (resistance in parallel with capacitance) between either input of an amplifier and its common, or ground terminal.

COMMON-MODE REJECTION (CMR)

When both inputs of a differential amplifier experience the same common-mode voltage (CMV), the output should, ideally, be unaffected. CMR is the ratio of the common-mode input voltage change to the differential input voltage (error voltage) which produces the same output change.

$$\text{CMR (in dB)} = 20 \log_{10} \text{CMV/Error Voltage}$$

Thus a CMR of 80dB means that 1V of common-mode voltage will cause an error of 100μV (referred to input).

COMMON-MODE VOLTAGE (CMV)

That portion of an input signal common to both inputs of a differential amplifier. Mathematically it is defined as the average of the signals at the two inputs:

$$\text{CMV} = (e_1 + e_2)/2$$

COMMON-MODE VOLTAGE GAIN

Ratio of the output signal voltage (ideally zero) to the common-mode input signal voltage.

COMMON-MODE VOLTAGE RANGE

Range of input voltage for linear, nonsaturated operation.

DIFFERENTIAL INPUT IMPEDANCE

Apparent impedance, resistance in parallel with capacitance, between the two input terminals.

FULL POWER FREQUENCY RESPONSE

Maximum frequency at which a device can supply its peak-to-peak rated output voltage and current, without introducing significant distortion.

GAIN-BANDWIDTH PRODUCT

Product of small signal, open-loop gain and frequency at that gain.

INPUT BIAS CURRENT

DC input current required at each input of an amplifier to provide zero output voltage when the input signal and input offset voltage are zero. The specified maximum is for each input.

INPUT BIAS CURRENT vs SUPPLY VOLTAGE

Sensitivity of input bias current to power supply voltages.

INPUT BIAS CURRENT vs TEMPERATURE

Sensitivity of input bias current to temperature.

INPUT CURRENT NOISE

Input current that would produce, at the output of a noiseless amplifier, the same output as that produced by the inherent noise generated internally in the amplifier when the source resistances are large.

INPUT OFFSET CURRENT

Difference of the two input bias currents of a differential amplifier.

INPUT OFFSET VOLTAGE

DC input voltage required to provide zero voltage at the output of an amplifier when the input signal and input bias currents are zero.

INPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE (PSR)

Sensitivity of input offset voltage to the power supply voltages. Both power supply voltages are changed in the same direction and magnitude over the operating voltage range.

INPUT OFFSET VOLTAGE vs TEMPERATURE (DRIFT)

Rate of change of input offset voltage with temperature. At Burr-Brown, this is the change in input offset voltage from +25°C to the maximum specification temperature, plus the change in input offset voltage from +25°C to the minimum specification temperature, this quantity is divided by the specified temperature range.

INPUT OFFSET VOLTAGE vs TIME

The sensitivity of input offset voltage to time.

INPUT VOLTAGE NOISE

Differential input voltage that would produce, at the output of a noiseless amplifier, the same output as that produced by the inherent noise generated internally in the amplifier when the source resistances are small.

MAXIMUM SAFE INPUT VOLTAGE

Maximum voltage that may be applied at, or between, the inputs without damage.

OPEN-LOOP GAIN

Ratio of the output signal voltage to the differential input signal voltage.

OPERATING TEMPERATURE RANGE

Temperature range over which the amplifier may be safely operated.

OUTPUT RESISTANCE

Open-loop output source resistance with respect to ground.

POWER SUPPLY RATED VOLTAGE

Normal value of power supply voltage at which the amplifier is designed to operate.

POWER SUPPLY VOLTAGE RANGE

Range of power supply voltage over which the amplifier may be safely operated.

QUIESCENT CURRENT

Current required from the power supply to operate the amplifier with no load and with the output at zero volts.

RATED OUTPUT

Peak output voltage and current that can be continuously, simultaneously supplied.

SETTLING TIME

Time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value.

SLEW RATE

Maximum rate of change of the output voltage when supplying rated output current.

SPECIFICATION TEMPERATURE RANGE

Temperature range over which "versus temperature" specifications are specified.

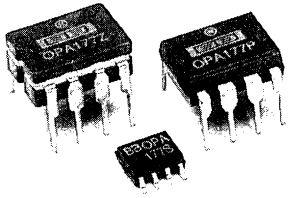
STORAGE TEMPERATURE RANGE

Temperature range over which the amplifier may be safely stored, unpowered.

UNITY-GAIN FREQUENCY RESPONSE

Frequency at which the open-loop gain becomes unity.

BURR-BROWN®



OPA177
OPA77

Precision
OPERATIONAL AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 10μV max
- LOW DRIFT: 0.1μV/°C
- HIGH OPEN-LOOP GAIN: 130dB min
- LOW QUIESCENT CURRENT: 1.5mA typ
- REPLACES INDUSTRY-STANDARD OP AMPS: OP-07, OP-77, OP-177, AD707, ETC.

APPLICATIONS

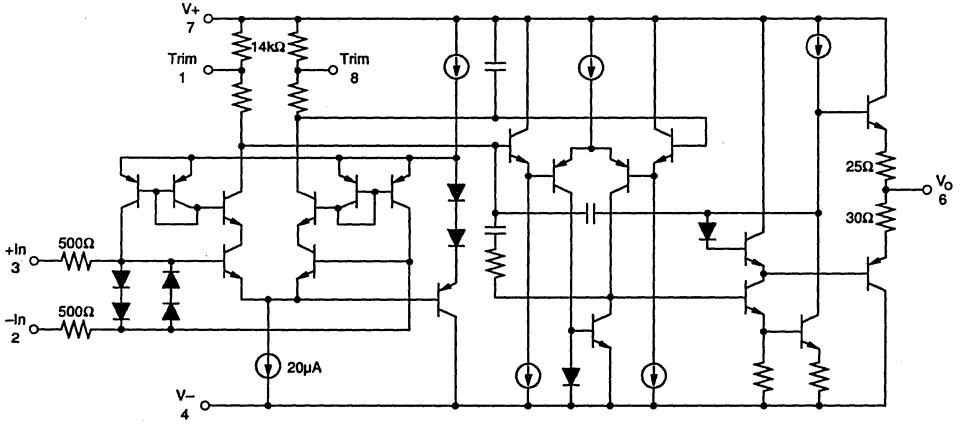
- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER

DESCRIPTION

The OPA177 and OPA77 precision bipolar op amps feature very low offset voltage and drift. Laser-trimmed offset, drift and input bias current virtually eliminate the need for costly external trimming. Their high performance and low cost make them ideally suited to a wide range of precision instrumentation.

The low quiescent current of the OPA177 and OPA77 dramatically reduce warm-up drift and errors due to thermoelectric effects in input interconnections. They provide an effective alternative to chopper-stabilized amplifiers. The low noise of the OPA177 and OPA77 maintains accuracy.

OPA177 and OPA77 performance gradeouts are available. Packaging options include 8-pin plastic DIP, 8-pin ceramic DIP, and SO-8 surface-mount packages.



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PDS-1081

OPA177 SPECIFICATIONS

ELECTRICAL

At V_S = ±15V, T_A = +25°C unless otherwise noted.

PARAMETER	CONDITION	OPA177E			OPA177F			OPA177G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE											
Input Offset Voltage			4	10		10	25		20	60	µV
Long-Term Input Offset[1]			0.2			0.3			0.4		µV/Mo
Voltage Stability											
Offset Adjustment Range	R_P = 20kΩ		±3			*			*		mV
Power Supply Rejection Ratio	V_S = ±3V to ±18V	120	125		115	*		110	120		dB
INPUT BIAS CURRENT											
Input Offset Current			0.3	1		*	1.5		*	2.8	nA
Input Bias Current			0.5	±1.5		*	±2		*	±2.8	nA
NOISE											
Input Noise Voltage	1Hz to 100Hz[2]		85	150		*	*		*	*	nVrms
Input Noise Current	1Hz to 100Hz		4.5			*			*		pArms
INPUT IMPEDANCE											
Input Resistance	Differential Mode[3]	26	45		*	*		18.5	*		MΩ
	Common Mode		200			*			*		GΩ
INPUT VOLTAGE RANGE											
Common-Mode Input Range[4]		±13	±14		*	*		*	*		V
Common-Mode Rejection	V_{CM} = ±13V	130	140		*	*		115	*		dB
OPEN-LOOP GAIN	R_L ≥ 2kΩ										
Large-Signal Voltage Gain	V_O = ±10V[5]	5000	12000		*	*		2000	6000		V/mV
OUTPUT											
Output Voltage Swing	R_L ≥ 10kΩ	±13.5	±14		*	*		*	*		V
	R_L ≥ 2kΩ	±12.5	±13		*	*		*	*		V
	R_L ≥ 1kΩ	±12	±12.5		*	*		*	*		V
Open-Loop Output Resistance			60			*			*		Ω
FREQUENCY RESPONSE											
Slew Rate	R_L ≥ 2kΩ	0.1	0.3		*	*		*	*		V/µs
Closed-Loop Bandwidth	G = +1	0.4	0.6		*	*		*	*		MHz
POWER SUPPLY											
Power Consumption	V_S = ±15V, No Load		40	60		*	*		*	*	mW
	V_S = ±3V, No Load		3.5	4.5		*	*		*	*	mW
Supply Current	V_S = ±15V, No Load		1.3	2		*	*		*	*	mA

ELECTRICAL

At V_S = ±15V, −40°C ≤ T_A ≤ +85°C, unless otherwise noted.

OFFSET VOLTAGE											
Input Offset Voltage			10	20		15	40		20	100	µV
Average Input Offset			0.03	0.1		0.1	0.3		0.7	1.2	µV/°C
Voltage Drift[6]											
Power Supply Rejection Ratio	V_S = ±3V to ±18V	120	125		110	120		106	115		dB
INPUT BIAS CURRENT											
Input Offset Current			0.5	1.5		*	2.2		*	4.5	nA
Average Input Offset Current			1.5	25		*	40		*	85	pA/°C
Drift[7]											
Input Bias Current			0.5	±4		*	*		*	±6	nA
Average Input Bias Current			8	25		*	40		15	60	pA/°C
Drift[7]											
INPUT VOLTAGE RANGE											
Common-Mode Input Range		±13	±13.5		*	*		*	*		V
Common-Mode Rejection	V_{CM} = ±13V		120	140		*	*		110	*	dB
OPEN-LOOP GAIN											
Large-Signal Voltage Gain	R_L ≥ 2kΩ, V_O = ±10V	2000	6000		*	*		1000	4000		V/mV
OUTPUT											
Output Voltage Swing	R_L ≥ 2kΩ	±12	±13		*	*		*	*		V
POWER SUPPLY											
Power Consumption	V_S = ±15V, No Load		60	75		*	*		*	*	mW
Supply Current	V_S = ±15V, No Load		2	2.5		*	*		*	*	mA

* Same as specifcation for product to left.

NOTES: (1) Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically less than 2µV. (2) Sample tested. (3) Guaranteed by design. (4) Guaranteed by CMRR test condition. (5) To insure high open-loop gain throughout the ±10V output range, A_{OL} is tested at −10V ≤ V_O ≤ 0V, 0V ≤ V_O ≤ +10V, and −10V ≤ V_O ≤ +10V. (6) OP177EZ and OP177FZ: TCV_{OS} is 100% tested. (7) Guaranteed by end-point limits.

OPA77 SPECIFICATIONS

ELECTRICAL

At V_S = ±15V, T_A = +25°C unless otherwise noted.

PARAMETER	CONDITION	OPA77E			OPA77F			OPA77G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE											
Input Offset Voltage			10	25		20	60		50	100	µV
Long-Term Input Offset Voltage Stability[1]			0.3			0.4			*		µV/Mo
Offset Adjustment Range	R_{TRIM} = 20kΩ		±3			*			*		mV
Power Supply Rejection Ratio	V_S = ±3V to ±18V		0.7	3		*	*		*	*	µV/V
INPUT BIAS CURRENT											
Input Offset Current			0.3	1.5		*	2.8		*	*	nA
Input Bias Current			1.2	±2		*	±2.8		*	*	nA
NOISE											
Input Noise Voltage	0.1Hz to 10Hz[2]		0.35	0.6		0.38	0.65		*	*	µVp-p
Input Noise Voltage Density	f = 10Hz[2]		8.5	18		*	20		*	*	nV/√Hz
	f = 100Hz[2]		7.5	13		*	13.5		*	*	nV/√Hz
	f = 1000Hz[2]		7.5	11		*	11.5		*	*	nV/√Hz
Input Noise Current	0.1Hz to 10Hz		35			*			*		pAp-p
Input Noise Current Density	f = 10Hz		0.73			*			*		pA/√Hz
	f = 100Hz		0.26			*			*		pA/√Hz
	f = 1000Hz		0.22			*			*		pA/√Hz
INPUT RESISTANCE											
Differential Input Resistance[3]		26	45		18.5	*		*	*		MΩ
Common-mode Input Resistance			200			*			*		GΩ
INPUT VOLTAGE RANGE											
Common Mode Input Range		±13	±14		*	*		*	*		V
Common-Mode Rejection	V_{CM} = ±13V		0.1	1		*	1.6		*	*	µV/V
OPEN-LOOP GAIN											
Large-Signal Voltage Gain	R_L ≥ 2kΩ, V_O = ±10V	5000	12000		2000	6000		*	*		V/mV
OUTPUT											
Output Voltage Swing	R_L ≥ 10kΩ	±13.5	±14		*	*		*	*		V
	R_L ≥ 2kΩ	±12.5	±13		*	*		*	*		V
	R_L ≥ 1kΩ	±12	±12.5		*	*		*	*		V
Open-Loop Output Resistance			60			*			*		Ω
FREQUENCY RESPONSE											
Slew Rate	R_L ≥ 2kΩ	0.1	0.3		*	*		*	*		V/µs
Closed-Loop Bandwidth	AVCL = +1	0.4	0.6		*	*		*	*		MHz
POWER SUPPLY											
Power Consumption	V_S = ±15V, No Load		50	60		*	*		*	*	mW
	V_S = ±3V, No Load		3.5	4.5		*	*		*	*	mW

ELECTRICAL

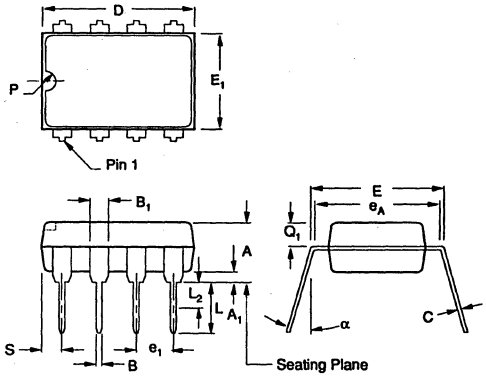
At V_S = ±15V, –25°C ≤ T_A ≤ +85°C for OPA77EZ and OPA77FZ, 0°C ≤ T_A ≤ +70°C for OPA77FP and OPA77GP, unless otherwise noted.

OFFSET VOLTAGE											
Input Offset Voltage	Z Package		10	45		20	100		*	*	µV
	P Package		10	55		20	100		80	150	µV
Average Input Offset[4]	Z Package		0.1	0.3		0.2	0.6		*	*	µV/°C
Voltage Drift	P Package		0.3	0.6		0.4	1		0.7	1.2	µV/°C
Power Supply Rejection Ratio	V_S = ±3V to ±18V		1	3		*	5		*	*	µV/V
INPUT BIAS CURRENT											
Input Offset Current			0.5	2.2		*	4.5		*	*	nA
Avg Input Offset Current Drift[5]			1.5	40		*	85		*	*	pA/°C
Input Bias Current			2.4	±4		*	±6		*	*	nA
Avg Input Bias Current Drift[5]			8	40		15	60		*	*	pA/°C
INPUT VOLTAGE RANGE											
Common Mode Input Range		±13	±13.5		*	*		*	*		V
Common-Mode Rejection	V_{CM} = ±13V		0.1	1		*	3		*	*	µV/V
OPEN-LOOP GAIN											
Large-Signal Voltage Gain	R_L ≥ 2kΩ, V_O = ±10V	2000	6000		1000	4000		*	*		V/mV
OUTPUT											
Output Voltage Swing	R_L ≥ 2kΩ	±12	±13		*	*		*	*		V
POWER SUPPLY											
Power Consumption	V_S = ±15V, No Load		60	75		*	*		*	*	mW

* Same as specification for product to left. NOTES: (1) Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs time over extended period after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5µV. (2) Sample tested. (3) Guaranteed by design. (4) OPA77E: TCV_{OS} is 100% tested on Z package. (5) Guaranteed by end-point limits.

MECHANICAL

P Package — 8-Pin Plastic DIP

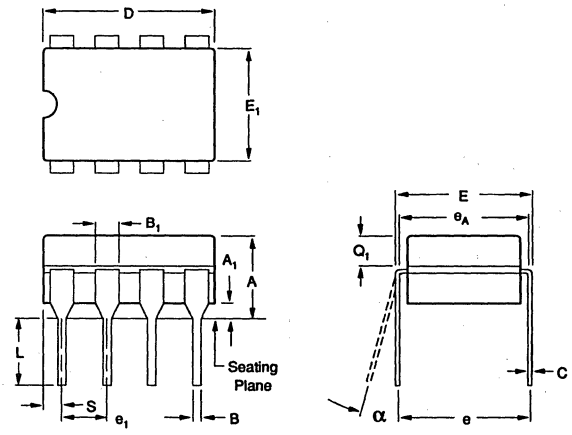


	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.155	.200	3.94	5.08
A_1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B_1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D (1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E_1	.240	.260	6.10	6.60
e_1	.100 BASIC		2.54 BASIC	
e_A	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
L_2 (2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q_1	.040	.075	1.02	1.91
S (1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e_1 and e_A apply in zone L_2 when unit installed.
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

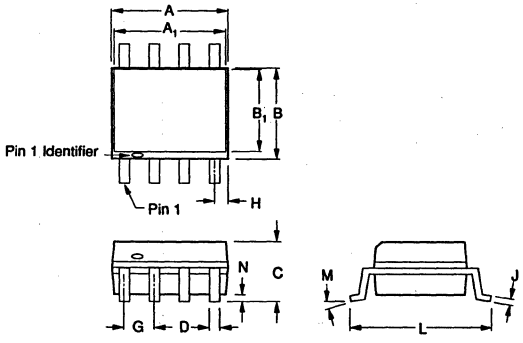
Z Package — 8-Pin SSI Ceramic DIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.160	.214	4.07	5.44
A_1	.009	.060	0.23	1.52
B	.015	.021	.38	.54
B_1	.045	.060	1.14	1.52
C	.008	.012	0.20	0.30
D	.365	.395	9.27	10.03
E	.290	.320	7.37	8.13
E_1	.245	.255	6.22	6.48
e_1	.100 BASIC		2.54 BASIC	
e_A	.268	.288	6.81	7.31
L	.125	.175	3.18	4.45
α	0°	15°	0°	15°
Q_1	.180	.220	4.57	5.59
S	—	.098	—	2.49
e	.290	.320	7.37	8.13

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

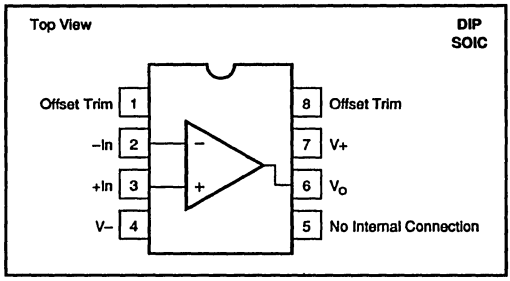
S Package — 8-Pin SOIC



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.185	.201	4.70	5.11
A_1	.178	.201	4.52	5.11
B	.146	.162	3.71	4.11
B_1	.130	.149	3.30	3.78
C	.054	.145	1.37	3.69
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.018	.026	0.46	0.66
J	.008	.012	0.20	0.30
L	.220	.252	5.59	6.40
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±22V
Differential Input Voltage	±30V
Input Voltage	$\pm V_S$ ±1V
Output Short Circuit	Continuous
Operating Temperature:	
Ceramic DIP (Z)	–55°C to +125°C
Plastic DIP (P), SO-8 (S)	–40°C to +85°C
Storage Temperature:	
Ceramic DIP (Z)	–65°C to +150°C
Plastic DIP (P), SO-8 (S)	–65°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMP. RANGE
OPA177FP	8-Pin Plastic DIP	–40°C to +85°C
OPA177GP	8-Pin Plastic DIP	–40°C to +85°C
OPA177GS	SO-8 Surface-Mount	–40°C to +85°C
OPA177EZ	8-Pin Ceramic DIP	–40°C to +85°C
OPA177FZ	8-Pin Ceramic DIP	–40°C to +85°C
OPA177GZ	8-Pin Ceramic DIP	–40°C to +85°C
OPA77FP	8-Pin Plastic DIP	0°C to +70°C
OPA77GP	8-Pin Plastic DIP	0°C to +70°C
OPA77EZ	8-Pin Ceramic DIP	–25°C to +85°C
OPA77FZ	8-Pin Ceramic DIP	–25°C to +85°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. ESD can cause damage ranging from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

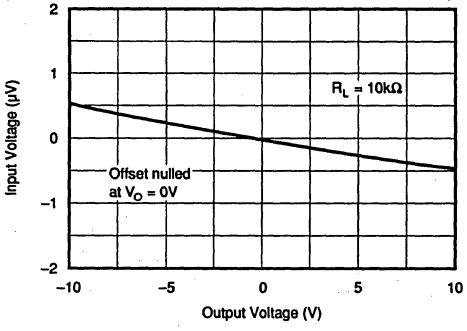
Burr-Brown's standard ESD test method consists of five 1000V positive and negative discharges (100pF in series with 1.5kΩ) applied to each pin.

Failure to observe proper handling procedures could result in small changes to the OPA177's input bias current.

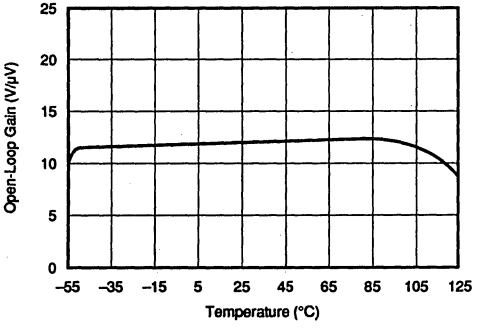
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

GAIN LINEARITY
(NORMALIZED INPUT VOLTAGE vs OUTPUT VOLTAGE)



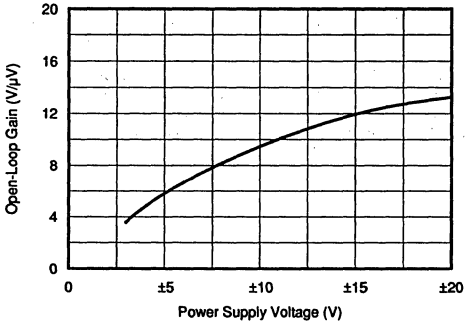
OPEN-LOOP GAIN vs TEMPERATURE



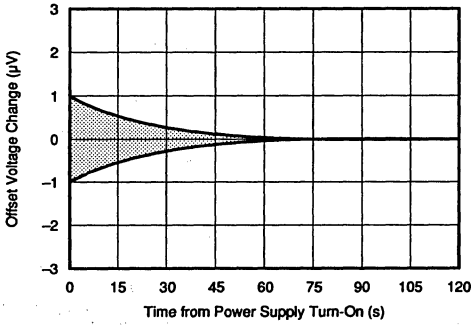
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

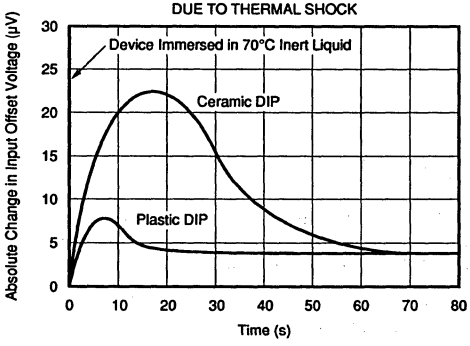
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



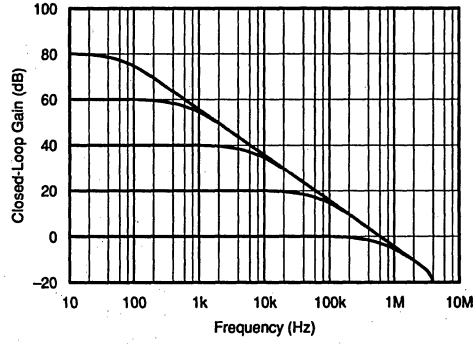
WARM-UP OFFSET VOLTAGE DRIFT



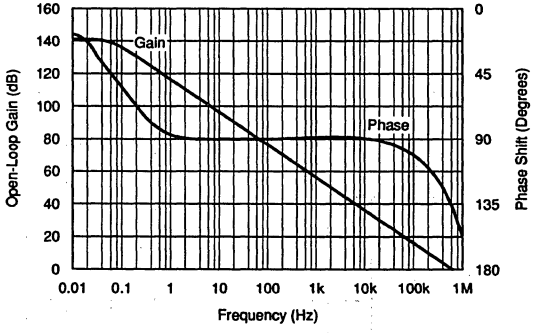
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



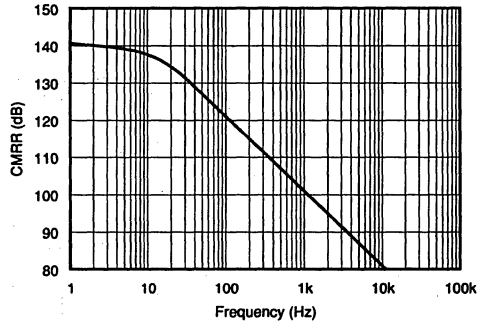
CLOSED-LOOP RESPONSE vs FREQUENCY



OPEN-LOOP GAIN/PHASE vs FREQUENCY



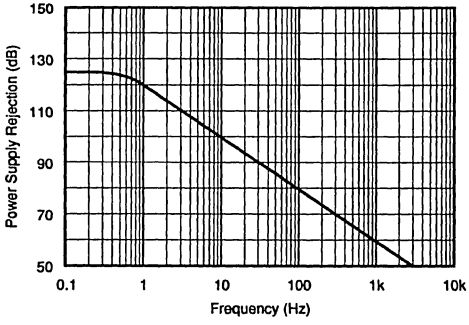
CMRR vs FREQUENCY



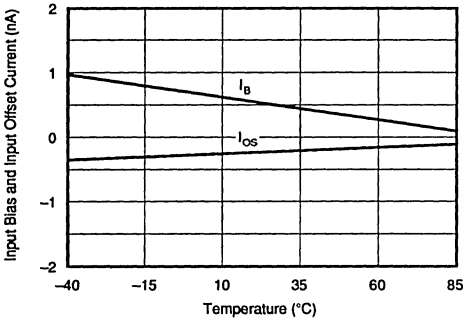
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

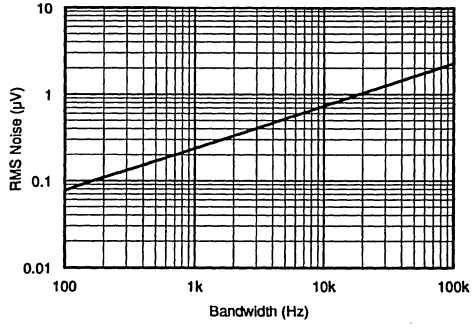
POWER SUPPLY REJECTION vs FREQUENCY



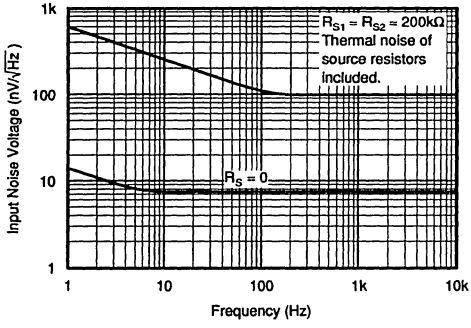
INPUT BIAS AND INPUT OFFSET CURRENT vs TEMPERATURE



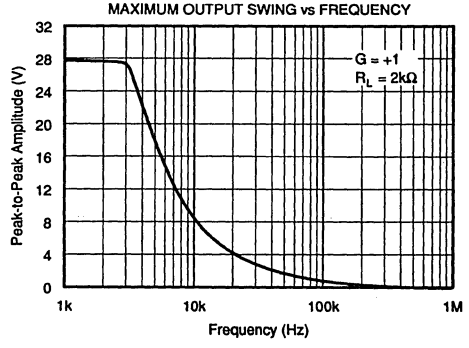
TOTAL NOISE vs BANDWIDTH (0.1Hz to Frequency Indicated)



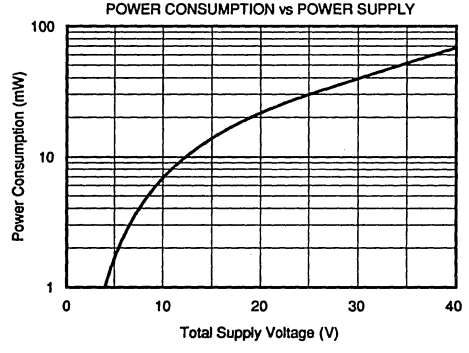
INPUT NOISE VOLTAGE DENSITY vs FREQUENCY



MAXIMUM OUTPUT SWING vs FREQUENCY

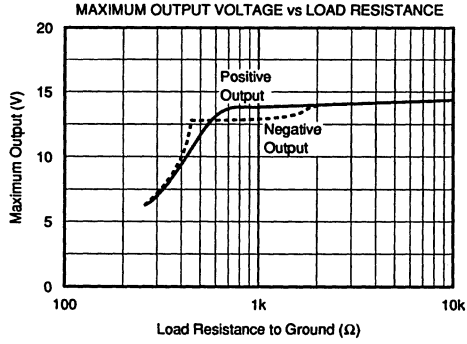


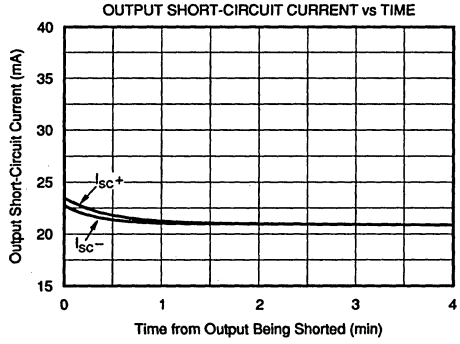
POWER CONSUMPTION vs POWER SUPPLY



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.





APPLICATIONS INFORMATION

The OPA177 is unity-gain stable, making it easy to use and free from oscillations in the widest range of circuitry. Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins. In most cases 0.1µF ceramic capacitors are adequate.

The OPA177 has very low offset voltage and drift. To achieve highest performance, circuit layout and mechanical conditions must be optimized. Offset voltage and drift can be degraded by small thermoelectric potentials at the op amp inputs. Connections of dissimilar metals will generate thermal potential which can mask the ultimate performance of the OPA177. These thermal potentials can be made to cancel by assuring that they are equal in both input terminals.

1. Keep connections made to the two input terminals close together.
2. Locate heat sources as far as possible from the critical input circuitry.
3. Shield the op amp and input circuitry from air currents such as cooling fans.

OFFSET VOLTAGE ADJUSTMENT

The OPA177 and OPA77 have been laser-trimmed for low offset voltage and drift so most circuits will not require external adjustment. Figure 1 shows the optional connection of an external potentiometer to adjust offset voltage. This adjustment should not be used to compensate for offsets created elsewhere in a system since this can introduce excessive temperature drift.

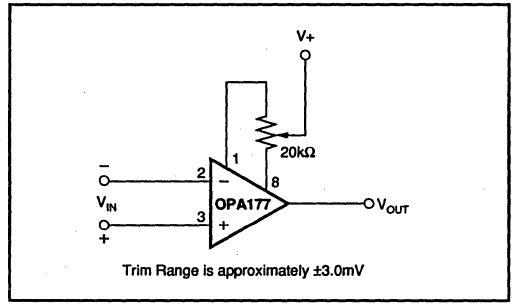


FIGURE 1. Optional Offset Nulling Circuit.

INPUT PROTECTION

The inputs of the OPA177 and OPA77 are protected with 500Ω series input resistors and diode clamps as shown in the simplified circuit diagram. The inputs can withstand ±30V differential inputs without damage. The protection diodes will, of course, conduct current when the inputs are overdriven. This may disturb the slewing behavior of unity-gain follower applications, but will not damage the op amp.

NOISE PERFORMANCE

The noise performance of the OPA177 and OPA77 is optimized for circuit impedances in the range of 2kΩ to 50kΩ. Total noise in an application is a combination of the op amp's input voltage noise and input bias current noise reacting with circuit impedances. For applications with higher source impedance, the OPA627 FET-input op amp will generally provide lower noise. For very low impedance applications, the OPA27 will provide lower noise.

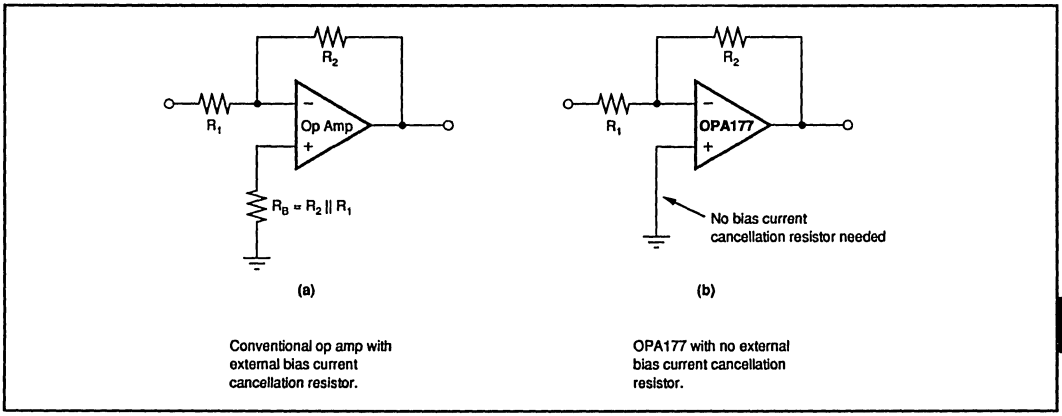


FIGURE 2. Input Bias Current Cancellation.

INPUT BIAS CURRENT CANCELLATION

The input stage base current of the OPA177 is internally compensated with an equal and opposite cancellation current. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

When the bias current is cancelled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, it is not necessary to balance the DC resistance seen at the two input terminals (Figure 2). A resistor added to balance the input resistances may actually increase offset and noise.

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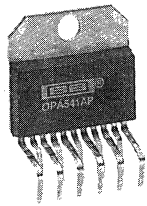


OPA541

High Power Monolithic OPERATIONAL AMPLIFIER

FEATURES

- POWER SUPPLIES TO ±40V
- OUTPUT CURRENT TO 10A PEAK
- PROGRAMMABLE CURRENT LIMIT
- INDUSTRY-STANDARD PINOUT
- FET INPUT
- TO-3 AND LOW-COST POWER PLASTIC PACKAGES

APPLICATIONS

- MOTOR DRIVER
- SERVO AMPLIFIER
- SYNCHRO EXCITATION
- AUDIO AMPLIFIER
- PROGRAMMABLE POWER SUPPLY

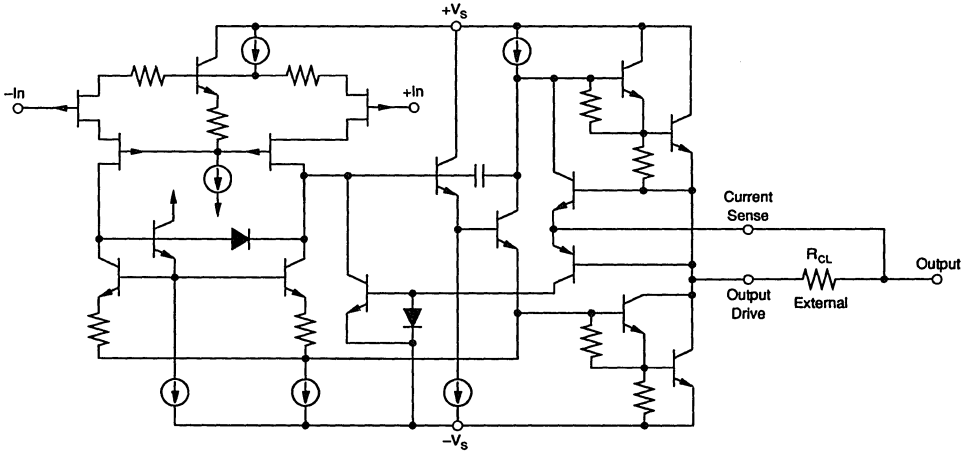
DESCRIPTION

The OPA541 is a power operational amplifier capable of operation from power supplies up to ±40V and continuous output currents up to 5A. Internal current limit circuity can be user-programmed with a single external resistor, protecting the amplifier and load from fault conditions. The OPA541 is fabricated using a proprietary bipolar/FET process.

Pinout is compatible with popular hybrid power amplifiers such as the OPA511, OPA512 and the 3573.

The OPA541 uses a single current-limit resistor to set both the positive and negative current limits. Applications currently using hybrid power amplifiers requiring two current-limit resistors need not be modified.

The OPA541 is available in an 11-pin power plastic package and an industry-standard 8-pin TO-3 hermetic package. The power plastic package has a copper-lead frame to maximize heat transfer. On the TO-3 package, the case is isolated from all circuitry, allowing it to be mounted directly to a heat sink without special insulators.



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PDS-737D

SPECIFICATIONS

ELECTRICAL

At T_C = +25°C and V_S = ±35VDC unless otherwise noted.

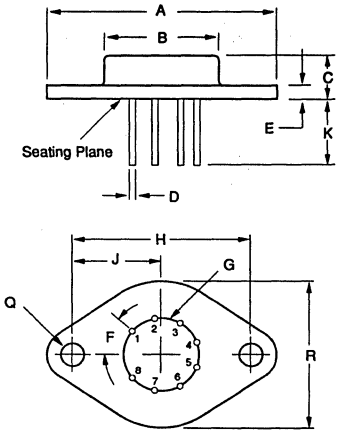
PARAMETER	CONDITIONS	OPA541AM/AP MIN	OPA541AM/AP TYP	OPA541AM/AP MAX	OPA541BM/SM MIN	OPA541BM/SM TYP	OPA541BM/SM MAX	UNITS
INPUT OFFSET VOLTAGE								
Vos			±2	±10		±0.1	±1	mV
vs Temperature	Specified Temperature Range		±20	±40		±15	±30	µV/°C
vs Supply Voltage	V_S = ±10V to $±V_{MAX}$		±2.5	±10		•	•	µV/V
vs Power			±20	±60		•	•	µV/W
INPUT BIAS CURRENT								
I_B			4	50		•	•	pA
INPUT OFFSET CURRENT								
I_{OS}			±1	±30		•	•	pA
	Specified Temperature Range			5		•		nA
INPUT CHARACTERISTICS								
Common-Mode Voltage Range	Specified Temperature Range	±(|V_S| – 6)	±(|V_S| – 3)		•	•		V
Common-Mode Rejection	V_{CM} = (|±V_S| – 6V)	95	113		•	•		dB
Input Capacitance			5			•		pF
Input Impedance, DC			1			•		TΩ
GAIN CHARACTERISTICS								
Open Loop Gain at 10Hz	R_L = 6Ω	90	97		•	•		dB
Gain-Bandwidth Product			1.6			•		MHz
OUTPUT								
Voltage Swing	I_O = 5A, Continuous	±(|V_S| – 5.5)	±(|V_S| – 4.5)		•	•		V
	I_O = 2A	±(|V_S| – 4.5)	±(|V_S| – 3.6)		•	•		V
	I_O = 0.5A	±(|V_S| – 4)	±(|V_S| – 3.2)		•	•		V
Current, Peak		9	10		•	•		A
AC PERFORMANCE								
Slew Rate		6	10		•	•		V/µs
Power Bandwidth	R_L = 8Ω, V_O = 20Vrms	45	55		•	•		kHz
Settling Time to 0.1%	2V Step		2			•		µs
Capacitive Load	Specified Temperature Range, G = 1	3.3					•	nF
	Specified Temperature Range, G >10			SOA[1]			•	
Phase Margin	Specified Temperature Range, R_L = 8Ω		40			•		Degrees
POWER SUPPLY								
Power Supply Voltage, $±V_S$	Specified Temperature Range	±10	±30	±35	•	±35	±40	V
Current, Quiescent			20	25		•	•	mA
THERMAL RESISTANCE								
OPA541AP:								
θ_{JC} (Junction-to-Case)	AC Output f > 60Hz		2.5					°C/W
θ_{JC}	DC Output		3					°C/W
θ_{JA} (Junction-to-Ambient)	No Heat Sink		40					°C/W
OPA541AM/BM/SM:								
θ_{JC} (Junction-to-Case)	AC Output f > 60Hz		1.25	1.5		•	•	°C/W
θ_{JC}	DC Output		1.4	1.9		•	•	°C/W
θ_{JA} (Junction-to-Ambient)	No Heat Sink		30			•		°C/W
TEMPERATURE RANGE								
T_{CASE}	AM, BM, AP	–25		+85	•		•	°C
	SM				–55		+125	°C

* Specification same as OPA541AM/AP.

NOTE: (1) SOA is the Safe Operating Area shown in Figure 1.

MECHANICAL

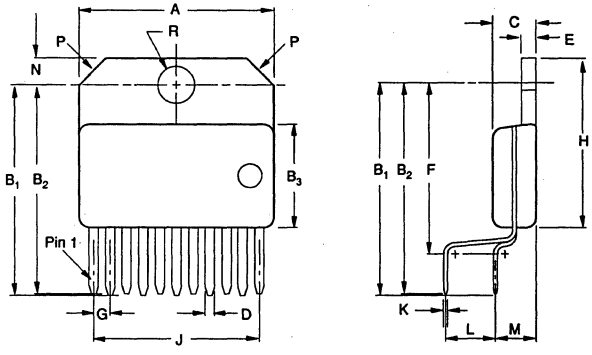
M Package — TO-3



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.260	.340	6.60	8.64
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.70 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

P Package — 11-Pin Plastic

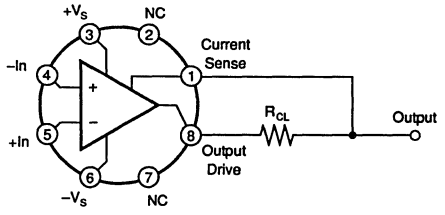


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.778	.798	19.76	20.27
B_1	.846	.886	21.49	22.50
B_2	.840	.880	21.34	22.35
B_3	.421 BASIC		10.69 BASIC	
C	.177 BASIC		4.50 BASIC	
D	.038 TYP		0.97 TYP	
E	.059	.063	1.50	1.60
F	.690	.710	17.53	18.03
G	.067 TYP		1.70 TYP	
H	.689 BASIC		17.50 BASIC	
J	.670 BASIC		17.02 BASIC	
K	.014	.018	0.36	0.46
L	.190	.210	4.83	5.33
M	.159	.179	4.04	4.55
N	.110		2.79	
P	45° x .120		45° x 3.05	
R	.148 D	.152 D	3.76 D	3.86 D

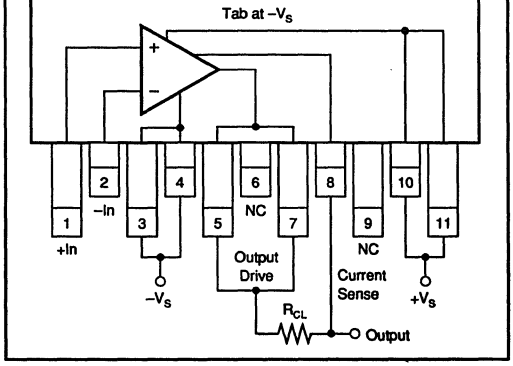
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

CONNECTION DIAGRAM

M Package — Top View



P Package — Top View



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$	80V
Output Current	see SOA
Power Dissipation, Internal[1]	125W
Input Voltage: Differential	$\pm V_S$
Common-mode	$\pm V_S$
Temperature: Pin solder, 10s	+300°C
Junction[1]	+150°C
Temperature Range:	
AM, BM SM	
Storage	–65°C to +150°C
Operating (case)	–55°C to +125°C
AP	
Storage	–40°C to +85°C
Operating (case)	–25°C to +85°C

NOTE: (1) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

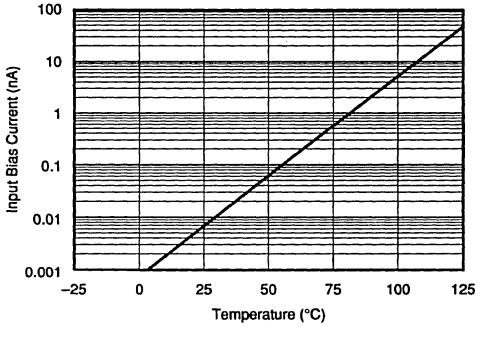
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	CONTINUOUS CURRENT
OPA541AP	Power Plastic	–25°C to +85°C	5A at 25°C
OPA541AM	TO-3	–25°C to +85°C	5A at 25°C
OPA541BM	TO-3	–25°C to +85°C	5A at 25°C
OPA541SM	TO-3	–55°C to +125°C	5A at 25°C

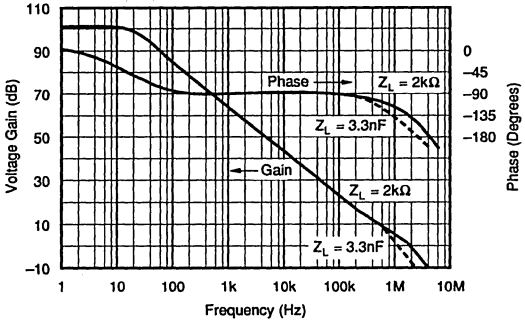
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±35VDC unless otherwise noted.

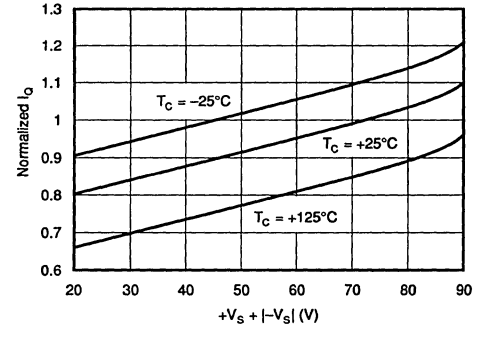
INPUT BIAS CURRENT vs TEMPERATURE



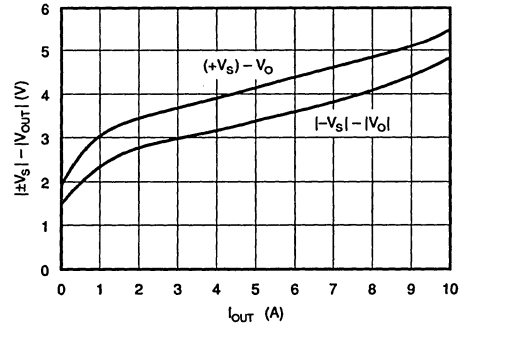
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



NORMALIZED QUIESCENT CURRENT vs TOTAL POWER SUPPLY VOLTAGE



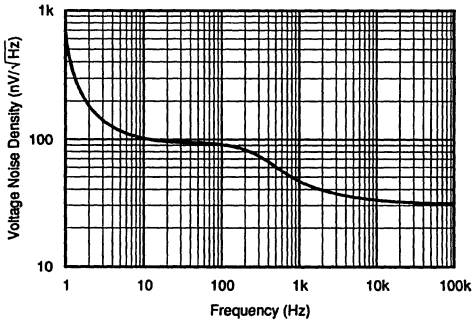
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



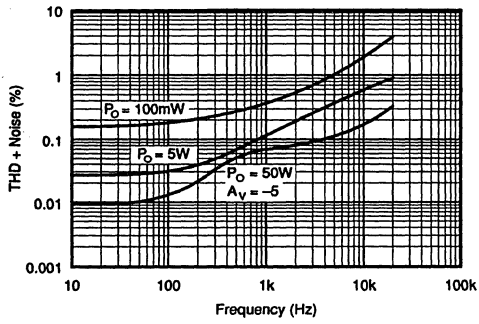
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±35VDC unless otherwise noted.

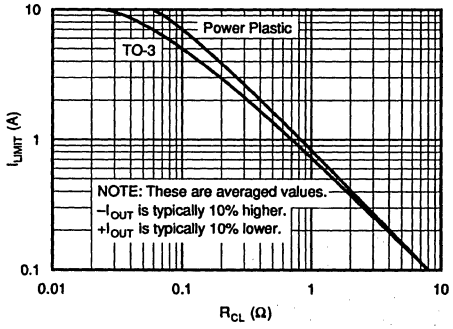
VOLTAGE NOISE DENSITY vs FREQUENCY



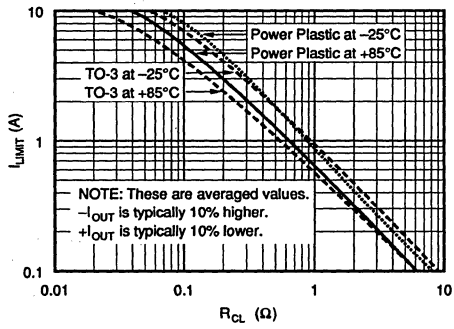
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



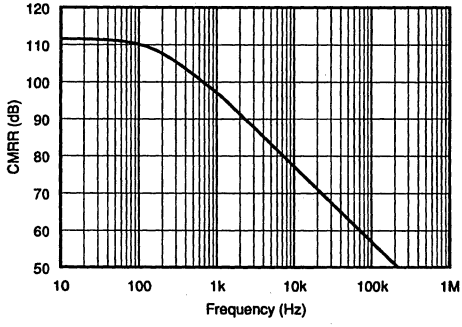
CURRENT LIMIT vs RESISTANCE LIMIT



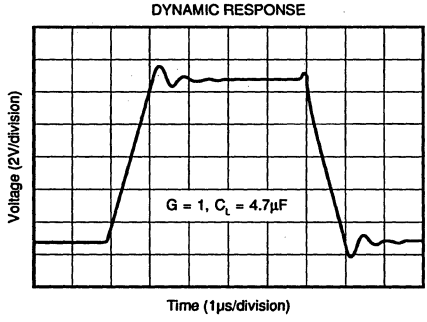
CURRENT LIMIT vs RESISTANCE LIMIT vs TEMPERATURE



COMMON-MODE REJECTION vs FREQUENCY



DYNAMIC RESPONSE



INSTALLATION INSTRUCTIONS

POWER SUPPLIES

The OPA541 is specified for operation from power supplies up to ±40V. It can also be operated from unbalanced or single power supplies as long as the total power supply voltage does not exceed 80V. The power supplies should be bypassed with low series impedance capacitors such as ceramic or tantalum. These should be located as near as practical to the amplifier's power supply pins. Good power amplifier circuit layout is, in general, like good high frequency layout. Consider the path of large power supply and output currents. Avoid routing these connections near low-level input circuitry to avoid waveform distortion and oscillations.

CURRENT LIMIT

Internal current limit circuitry is controlled by a single external resistor, R_{CL}. Output load current flows through this external resistor. The current limit is activated when the voltage across this resistor is approximately a base-emitter turn-on voltage. The value of the current limit resistor is approximately:

$$\text{AM, BM SM} \quad R_{CL} = \frac{0.809}{|I_{LIM}|} - 0.057$$

$$\text{AP} \quad R_{CL} = \frac{0.813}{|I_{LIM}|} - 0.02$$

Because of the internal structure of the OPA541, the actual current limit depends on whether current is positive or negative. The above R_{CL} gives an average value. For a given R_{CL}, $+I_{OUT}$ will actually be limited at about 10% below the expected level, while $-I_{OUT}$ will be limited about 10% above the expected level.

The current limit value decreases with increasing temperature due to the temperature coefficient of a base-emitter junction voltage. Similarly, the current limit value increases at low temperatures. Current limit versus resistor value and temperature effects are shown in the Typical Performance Curves. Approximate values for R_{CL} at other temperatures may be calculated by adjusting R_{CL} as follows:

$$\Delta R_{CL} = \frac{-2mV}{|I_{LIM}|} \times (T - 25)$$

The adjustable current limit can be set to provide protection from short circuits. The safe short-circuit current depends on power supply voltage. See the discussion on Safe Operating Area to determine the proper current limit value.

Since the full load current flows through R_{CL}, it must be selected for sufficient power dissipation. For a 5A current limit on the TO-3 package, the formula yields an R_{CL} of 0.105Ω (0.143Ω on the power plastic package due to different internal resistances). A continuous 5A through 0.105Ω would require an R_{CL} that can dissipate 2.625W.

Sinusoidal outputs create dissipation according to rms load current. For the same R_{CL}, AC peaks would still be limited to 5A, but rms current would be 3.5A, and a current limiting resistor with a lower power rating could be used. Some applications (such as voice amplification) are assured of signals with much lower duty cycles, allowing a current resistor with a low power rating. Wire-wound resistors may be used for R_{CL}. Some wire-wound resistors, however, have excessive inductance and may cause loop-stability problems. Be sure to evaluate circuit performance with resistor type planned for production to assure proper circuit operation.

HEAT SINKING

Power amplifiers are rated by case temperature, not ambient temperature as with signal op amps. The maximum allowable power dissipation is a function of the case temperature as shown on the power derating curve. All points on the power derating slope produce a maximum internal junction temperature of +150°C. Sufficient heat sinking must be provided to keep the case temperature within safe bounds for the maximum ambient temperature power dissipation. The thermal resistance of the heat sink required may be calculated by:

$$\theta_{HS} = \frac{T_{CASE} - T_{AMBIENT}}{P_D \text{ (max)}}$$

Commercially available heat sinks often specify their thermal resistance. These ratings are often suspect, however, since they depend greatly on the mounting environment and air flow conditions. Actual thermal performance should be verified by measurement of case temperature under the required load and environmental conditions.

No insulating hardware is required when using the TO-3 package. Since mica and other similar insulators typically add approximately 0.7°C/W thermal resistance, their elimination significantly improves thermal performance. See Burr-Brown Application Note AN-83 for further details on heat sinking. On the power plastic package, the metal tab is connected to $-V_S$, and appropriate actions should be taken when mounting on a heat sink or chassis.

SAFE OPERATING AREA

The safe operating area (SOA) plot provides comprehensive information on the power handling abilities of the OPA541. It shows the allowable output current as a function of the voltage across the conducting output transistor (see Figure 1). This voltage is equal to the power supply voltage minus the output voltage. For example, as the amplifier output swings near the positive power supply voltage, the voltage across the output transistor decreases and the device can safely provide large output currents demanded by the load.

Short circuit protection requires evaluation of SOA. When the amplifier output is shorted to ground, the full power supply voltage is impressed across the conducting output transistor. The current limit must be set to a value which is safe for the power supply voltage used. For instance, with V_S ±35V, a short to ground would force 35V across the conducting power transistor. A current limit of 1.8A would be safe.

Reactive, or EMF-generating, loads such as DC motors can present difficult SOA requirements. With a purely reactive

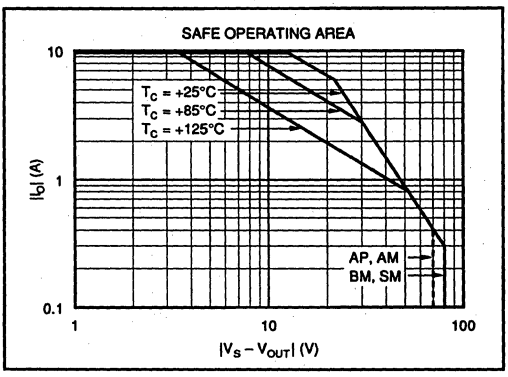


FIGURE 1. Safe Operating Area.

load, output voltage and load current are 90° out of phase. Thus, peak output current occurs when the output voltage is zero and the voltage across the conducting transistor is equal to the full power supply voltage. See Burr-Brown Application Note AN-123 for further information on evaluating SOA.

REPLACING HYBRID POWER AMPLIFIERS

The OPA541 can be used in applications currently using various hybrid power amplifiers, including the OPA501, OPA511, OPA512, and 3573. Of course, the application must be evaluated to assure that the output capability and other performance attributes of the OPA541 meet the necessary requirement. These hybrid power amplifiers use two current limit resistors to independently set the positive and negative current limit value. Since the OPA541 uses only one current limit resistor to set both the positive and negative current limit, only one resistor (see Figure 4) need be installed. If installed, the resistor connected to pin 2 (TO-3 package) is superfluous, but it does no harm.

Because one resistor carries the current previously carried by two, the resistor may require a higher power rating. Minor adjustments may be required in the resistor value to achieve the same current limit value. Often, however, the change in current limit value when changing models is small compared to its variation over temperature. Many applications can use the same current limit resistor.

APPLICATIONS CIRCUITS

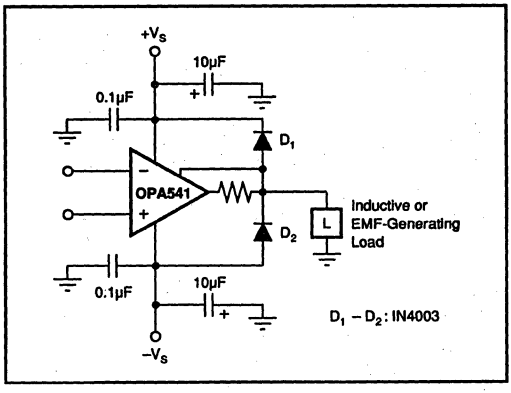


FIGURE 2. Clamping Output for EMF-Generating Loads.

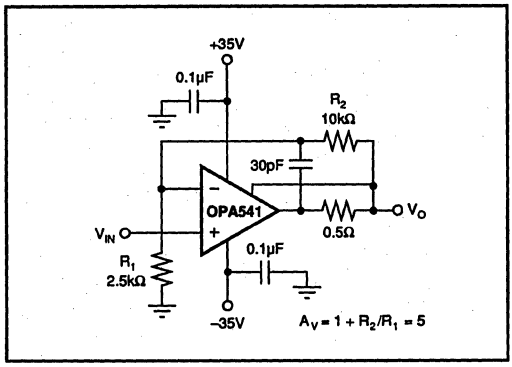


FIGURE 3. Isolating Capacitive Loads.

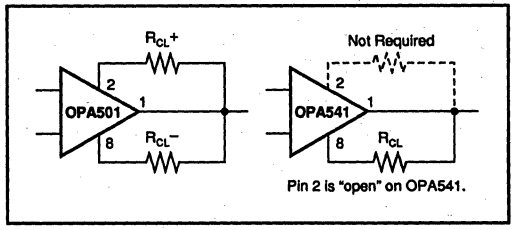


FIGURE 4. Replacing OPA501 with OPA541.

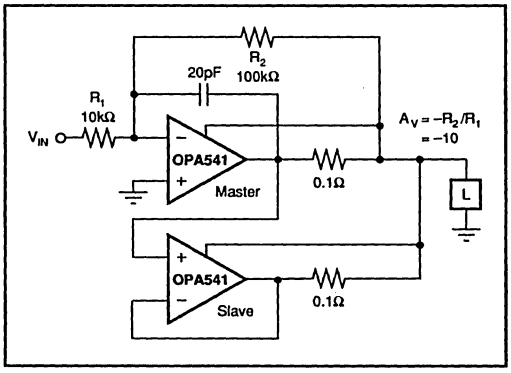


FIGURE 5. Paralleled Operation, Extended SOA.

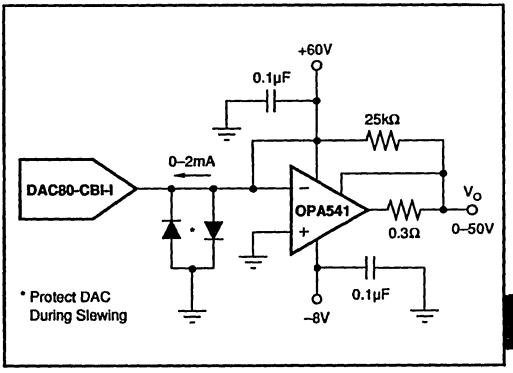


FIGURE 6. Programmable Voltage Source.

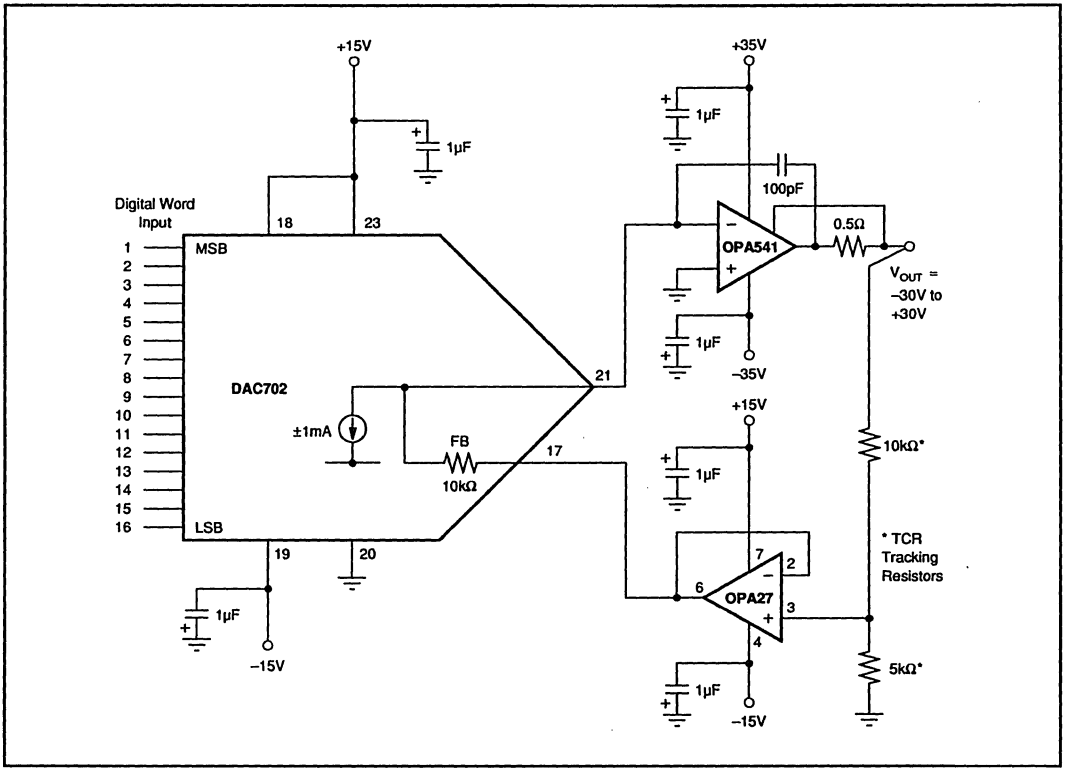


FIGURE 7. 16-Bit Programmable Voltage Source.

BURR-BROWN®

OPA603

High Speed, Current-Feedback OPERATIONAL AMPLIFIER

FEATURES

- BANDWIDTH: 100MHz, G = 1 to 10
- SLEW RATE: 1000V/µs
- FAST SETTLING TIME: 50ns to 0.1%
- WIDE SUPPLY RANGE: ±4.5 to ±18V
- HIGH OUTPUT CURRENT: ±150mA peak
- 8-PIN PLASTIC MINI-DIP PACKAGE

APPLICATIONS

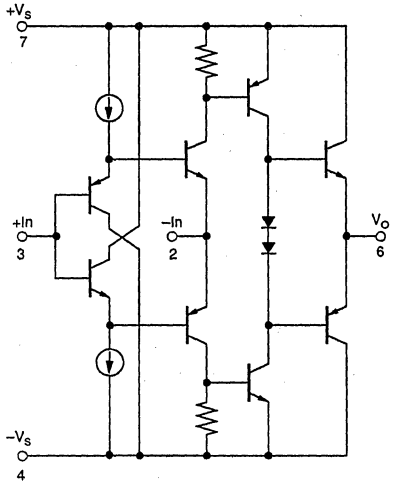
- ATE PIN DRIVERS
- LINE DRIVERS
- VIDEO AMPLIFIERS
- FAST DATA ACQUISITION
- SONAR, ULTRASOUND CIRCUITRY
- WAVEFORM GENERATORS

DESCRIPTION

The OPA603 is a high-speed current-feedback op amp with guaranteed specifications at both ±5V and ±15V power supplies. It can deliver full ±10V signals into 150Ω loads with up to 1000V/µs slew rate. This allows it to drive terminated 75Ω cables. With 150mA peak output current capability it is suitable for driving load capacitance or long lines at high speed.

In contrast with conventional op amps, the current-feedback approach provides nearly constant bandwidth and settling time over a wide range of closed-loop voltage gains.

The OPA603 is available in a plastic 8-pin dual-in-line package and is specified for the industrial temperature range.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1026A

SPECIFICATIONS, $V_S = \pm 15V$

ELECTRICAL

T_A = +25°C, R_L = 150Ω unless otherwise noted.

PARAMETER	CONDITIONS	OPA603AP MIN	OPA603AP TYP	OPA603AP MAX	UNITS
INPUT OFFSET VOLTAGE					
Initial				5	mV
vs Temperature			8		µV/°C
vs Common-Mode Voltage	V_{CM} = ±10V	50	60		dB
vs Supply (tracking) Voltage	V_S = ±12V to ±18V	80	85		dB
vs Supply (non-tracking)[1]	$\|V_S\|$ = 12V to 18V	55	60		dB
+INPUT BIAS CURRENT					
Initial				5	µA
vs Temperature			30		nA/°C
vs Common-Mode	V_{CM} = ±10V		200	500	nA/V
vs Supply (tracking)	V_S = ±12V to ±18V		50	100	nA/V
vs Supply (non-tracking)[1]	$\|V_S\|$ = 12V to 18V		150	300	nA/V
–INPUT BIAS CURRENT					
Initial				25	µA
vs Temperature			300		nA/°C
vs Common-Mode	V_{CM} = ±10V		200	600	nA/V
vs Supply (tracking)	V_S = ±12V to ±18V		300	500	nA/V
vs Supply (non-tracking)[1]	$\|V_S\|$ = 12V to 18V		1500	2000	nA/V
INPUT IMPEDANCE					
+Input			5 || 2		MΩ || pF
–Input			30 || 2		Ω || pF
OPEN LOOP CHARACTERISTICS					
Transresistance	V_O = ±10V	300	440		kΩ
Transcapacitance			1.8		pF
OUTPUT CHARACTERISTICS					
Voltage	R_L = 150Ω	±10	±12		V
Peak Current			150		mA
Short-Circuit Current[2]	V_O = 0V		170	200	mA
Output Resistance, Open-Loop			70		Ω
FREQUENCY RESPONSE	G = +2				
Small-Signal Bandwidth[3]		70	160		MHz
Gain Flatness, ±0.5dB		35	75		MHz
Full-Power Bandwidth	V_O = 20Vp-p		10		MHz
Differential Gain	f = 4.43MHz, V_O = 1V		0.03		%
Differential Phase	f = 4.43MHz, V_O = 1V		0.025		Degrees
TIME DOMAIN RESPONSE	G = +2				
Propagation Delay			10		ns
Rise and Fall Time			10		ns
Settling Time to 0.10%	10V Step		50		ns
Slew Rate			1000		V/µs
DISTORTION	G = +2, R_L = 100Ω, f = 10MHz				
2nd Harmonic Distortion	V_O = 0.2Vp-p	–60	–65		dBc
3rd Harmonic Distortion	V_O = 0.2Vp-p	–70	–90		dBc
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±4.5		±18	V
Current			±21	±25	mA
TEMPERATURE RANGE					
Specification		–25		+85	°C
Storage		–40		+150	°C
THERMAL RESISTANCE, $\theta_{JUNCTION\text{-}AMBIENT}$	Soldered to Printed Circuit		90		°C/W

NOTES: (1) One power supply fixed at 15V; the other supply varied from 12V to 18V. (2) Observe power derating curve. (3) See bandwidth versus gain curves, Figure 5.

SPECIFICATIONS, $V_S = \pm 5V$

ELECTRICAL

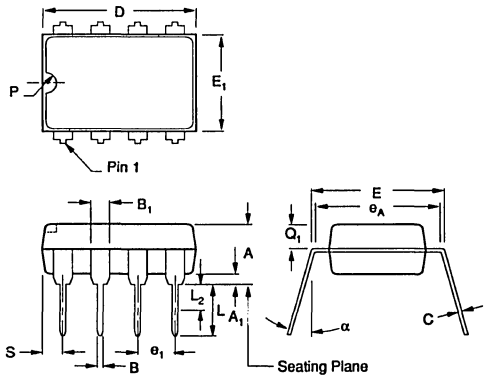
T_A = +25°C, R_L = 75Ω unless otherwise noted.

PARAMETER	CONDITIONS	OPA603AP MIN	OPA603AP TYP	OPA603AP MAX	UNITS
INPUT OFFSET VOLTAGE					
Initial				6	mV
vs Temperature			8		µV/°C
vs Common-Mode	V_{CM} = ±3V	50	55		dB
vs Supply (tracking)	V_S = ±4V to ±6V	75	80		dB
vs Supply (non-tracking)(1)	$\|V_S\|$ = 4V to 6V	55	60		dB
+INPUT BIAS CURRENT					
Initial				5	µA
vs Temperature			30		nA/°C
vs Common-Mode	V_{CM} = ±3V		350	600	nA/V
vs Supply (tracking)	V_S = ±4V to ±6V		100	200	nA/V
vs Supply (non-tracking)(1)	$\|V_S\|$ = 4V to 6V		200	300	nA/V
–INPUT BIAS CURRENT					
Initial				25	µA
vs Temperature			300		nA/°C
vs Common-Mode	V_{CM} = ±3V		300	600	nA/V
vs Supply (tracking)	V_S = ±4V to ±6V		500	700	nA/V
vs Supply (non-tracking)(1)	$\|V_S\|$ = 4V to 6V		2500	3000	nA/V
INPUT IMPEDANCE					
+Input			3.3 || 2		MΩ || pF
–Input			30 || 2		Ω || pF
OPEN LOOP CHARACTERISTICS					
Transresistance	V_O = ±2V	225	330		kΩ
Transcapacitance			2.4		pF
OUTPUT CHARACTERISTICS					
Voltage		±2	±2.75		V
Peak Current			150		mA
Short-Circuit Current(2)	V_O = 0V		170	200	mA
Output Resistance, Open-Loop			80		Ω
FREQUENCY RESPONSE	G = +2				
Small-Signal Bandwidth(3)			140		MHz
Gain Flatness, ±0.5dB			65		MHz
Full-Power Bandwidth			20		MHz
Differential Gain	f = 4.43MHz, V_O = 1V, R_L = 150Ω		0.03		%
Differential Phase	f = 4.43MHz, V_O = 1V, R_L = 150Ω		0.025		Degrees
TIME DOMAIN RESPONSE	G = +2, R_L = 100Ω				
Propagation Delay			15		ns
Rise and Fall Time			20		ns
Settling Time to 0.10%			60		ns
Slew Rate			750		V/µs
DISTORTION	G = +2, R_L = 100Ω, f = 10MHz				
2nd Harmonic Distortion	V_O = 0.2Vp-p		–67		dBc
3rd Harmonic Distortion	V_O = 0.2Vp-p		–78		dBc
POWER SUPPLY					
Specified Operating Voltage			±5		V
Operating Voltage Range		±4.5		±18	V
Current			±21	±25	mA
TEMPERATURE RANGE					
Specification		–25		+85	°C
Storage		–40		+150	°C
THERMAL RESISTANCE, $\theta_{JUNCTION\text{-}AMBIENT}$	Soldered to Printed Circuit		90		°C/W

NOTES: (1) One power supply fixed at 5V; the other supply varied from 4V to 6V. (2) Observe power derating curve. (3) See bandwidth versus gain curves, Figure 5.

MECHANICAL

P Package — 8-Pin Plastic DIP



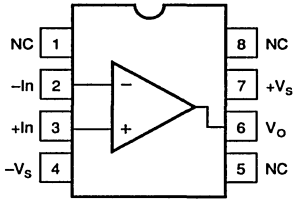
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D (1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2(2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q1	.040	.075	1.02	1.91
S (1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e_1 and e_A apply in zone L_2 when unit installed.
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

PIN CONFIGURATION

Top View — DIP



NC: No Internal Connection.
Solder to ground plane for improved heat dissipation.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	±V_S
Differential Input Voltage	±6V
Power Dissipation	See derating curve
Operating Temperature	+100°C
Storage Temperature	+150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

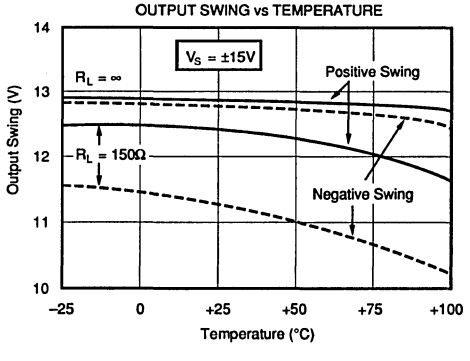
ORDERING INFORMATION

MODEL	PACKAGE	SPECIFIED TEMP. RANGE
OPA603AP	Plastic DIP	–25°C to +85°C

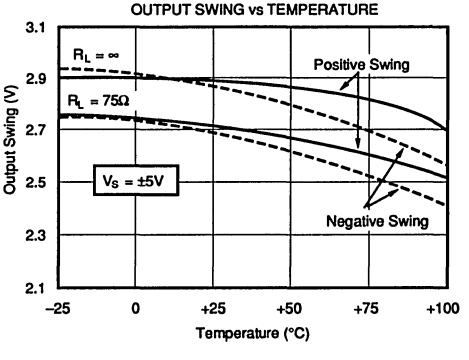
TYPICAL PERFORMANCE CURVES

T_A = +25°C unless otherwise noted.

OUTPUT SWING vs TEMPERATURE



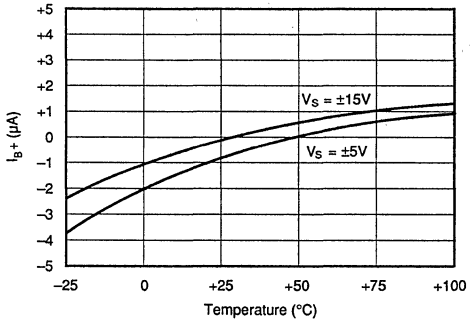
OUTPUT SWING vs TEMPERATURE



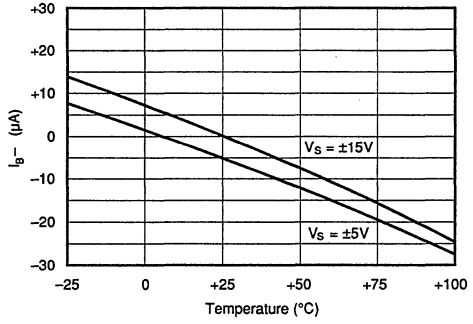
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C unless otherwise noted.

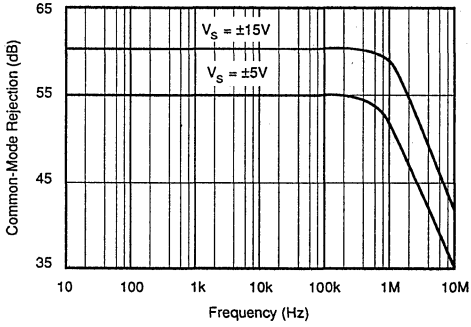
NONINVERTING INPUT BIAS CURRENT vs TEMPERATURE



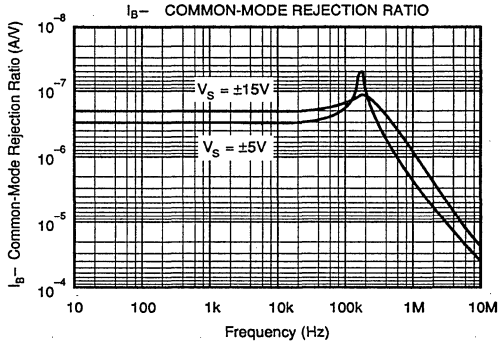
INVERTING INPUT BIAS CURRENT vs TEMPERATURE



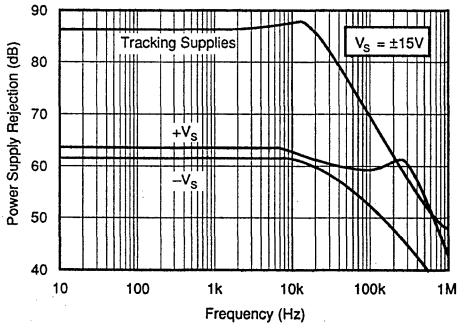
COMMON-MODE REJECTION vs FREQUENCY



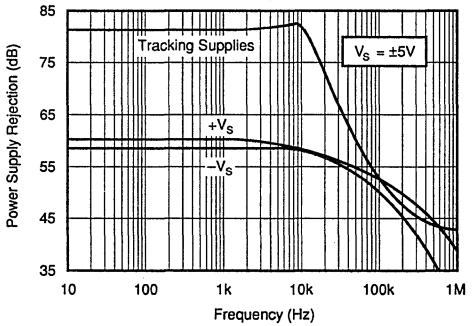
I_B– COMMON-MODE REJECTION RATIO



POWER SUPPLY REJECTION vs FREQUENCY

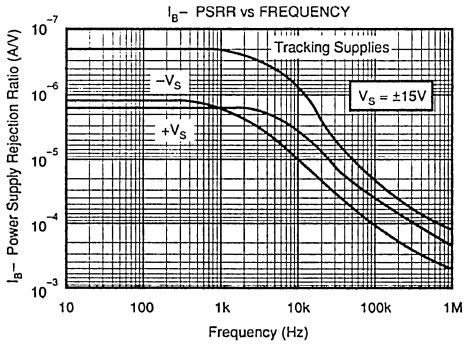


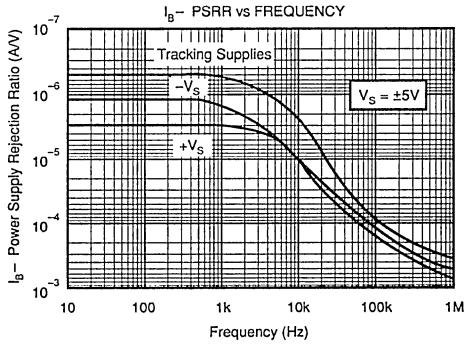
POWER SUPPLY REJECTION vs FREQUENCY

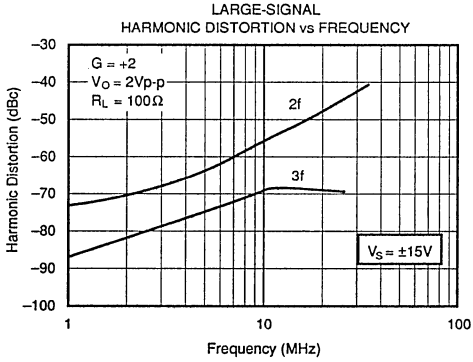


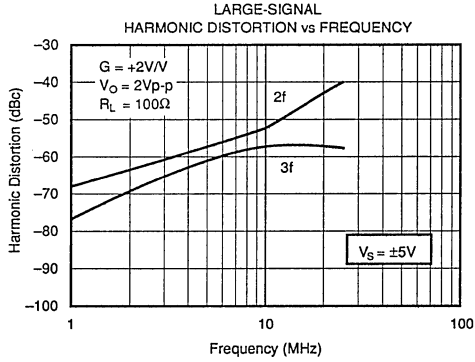
TYPICAL PERFORMANCE CURVES (CONT)

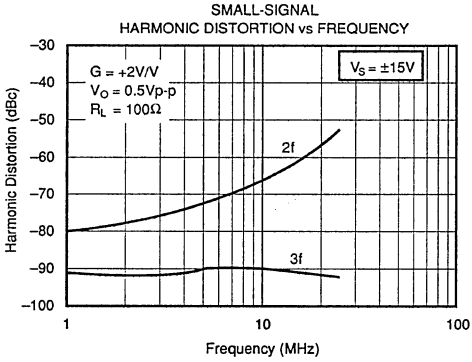
T_A = +25°C unless otherwise noted.

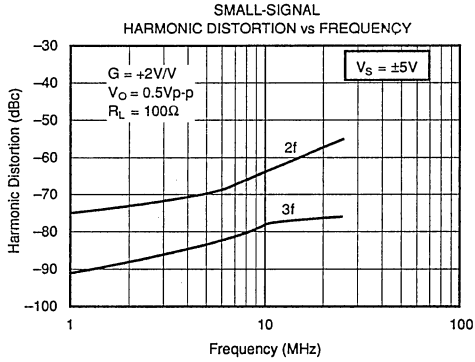








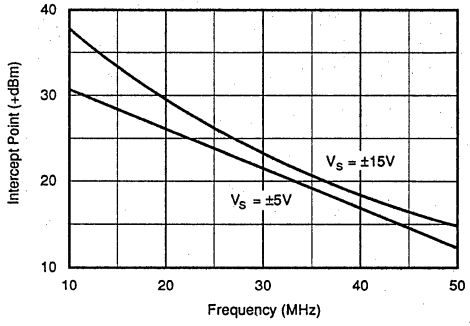




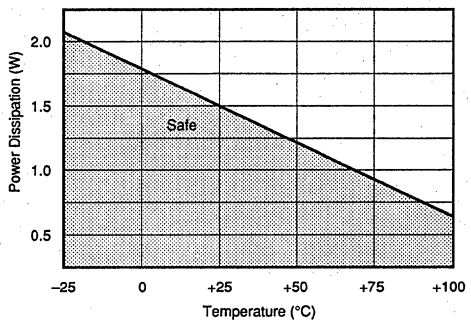
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C unless otherwise noted.

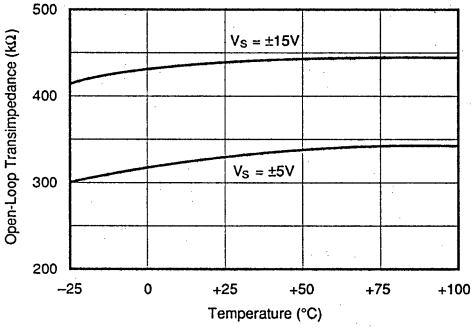
2-TONE, 3rd ORDER INTERMODULATION INTERCEPT



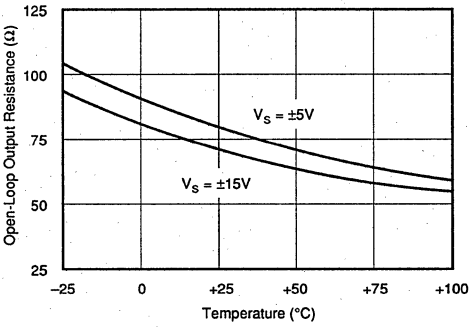
MAXIMUM POWER DISSIPATION vs TEMPERATURE



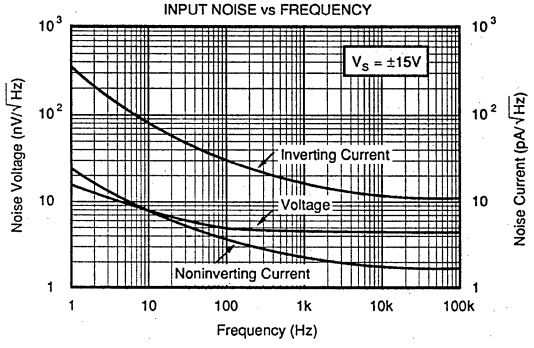
OPEN-LOOP TRANSIMPEDANCE vs TEMPERATURE



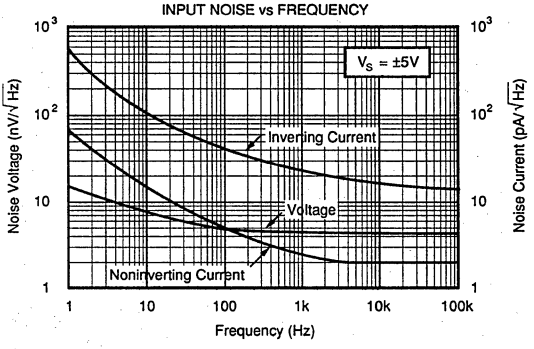
OPEN-LOOP OUTPUT RESISTANCE vs TEMPERATURE



INPUT NOISE vs FREQUENCY



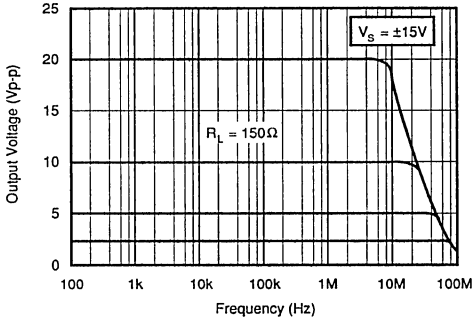
INPUT NOISE vs FREQUENCY



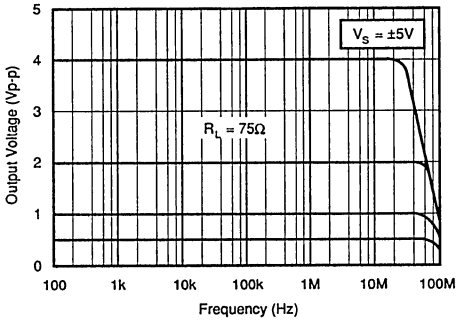
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C unless otherwise noted.

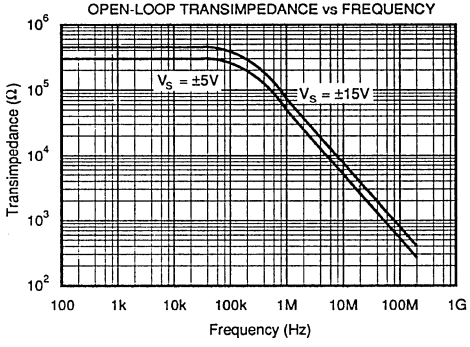
LARGE-SIGNAL OUTPUT vs FREQUENCY



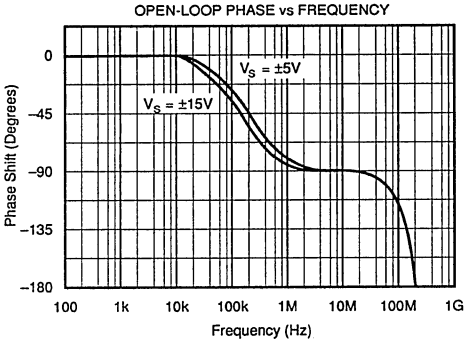
LARGE-SIGNAL OUTPUT vs FREQUENCY



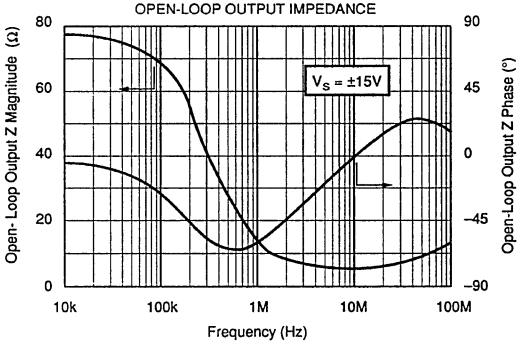
OPEN-LOOP TRANSIMPEDANCE vs FREQUENCY



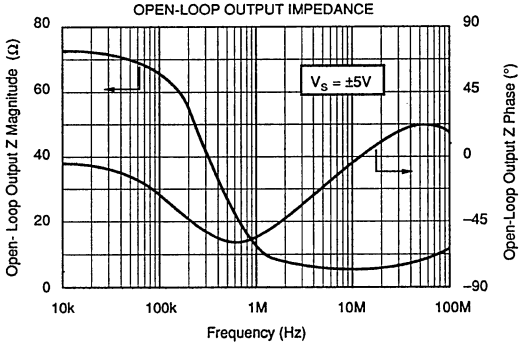
OPEN-LOOP PHASE vs FREQUENCY



OPEN-LOOP OUTPUT IMPEDANCE



OPEN-LOOP OUTPUT IMPEDANCE



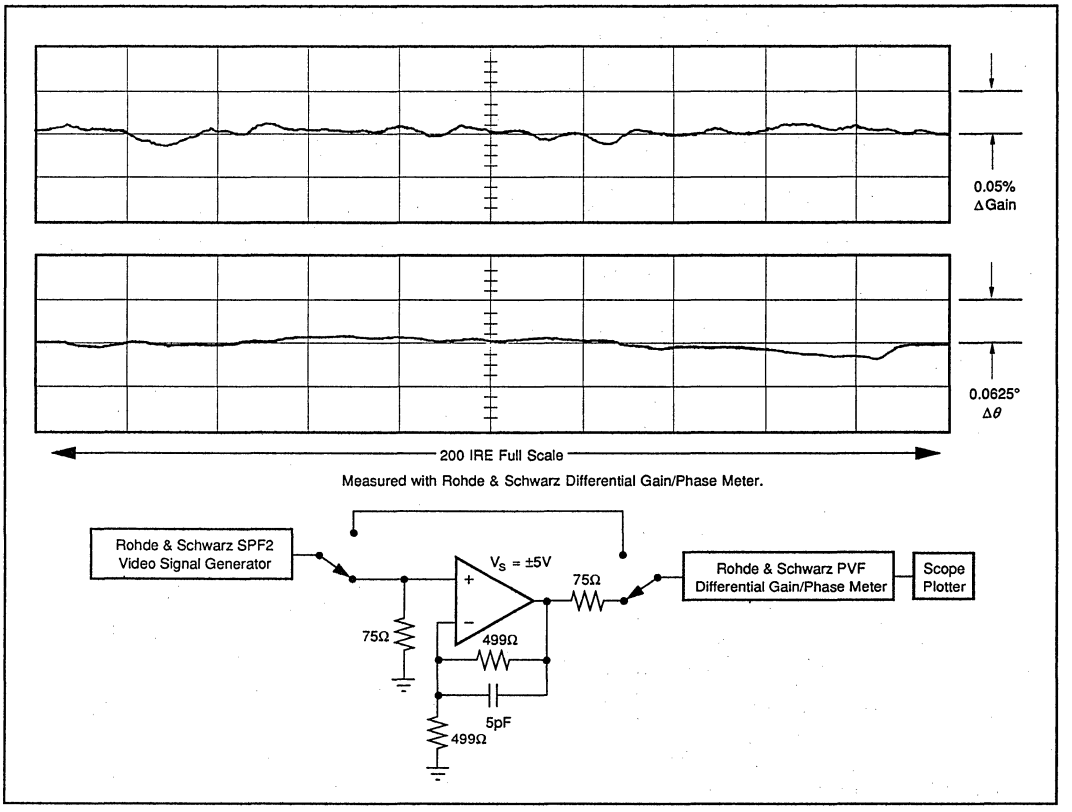


FIGURE 1. Video Differential Gain/Phase Performance.

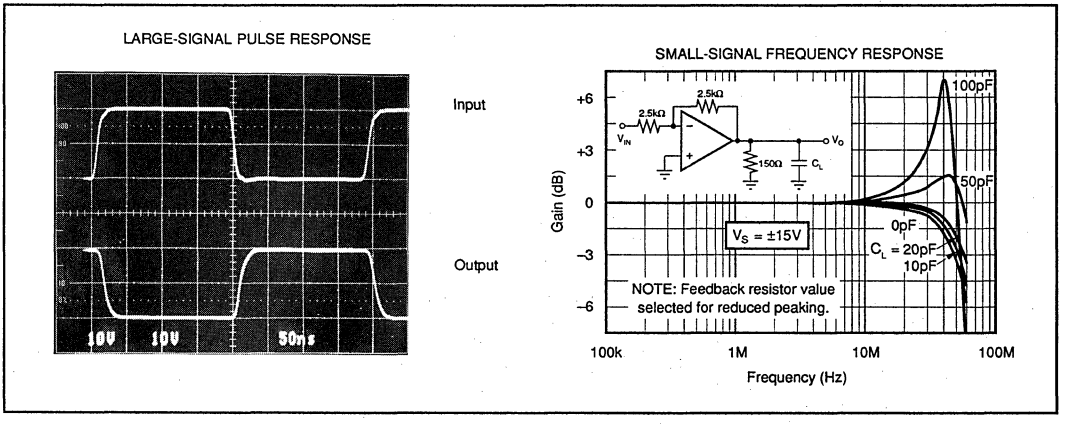


FIGURE 2. Dynamic Response— Inverting Unity-Gain.

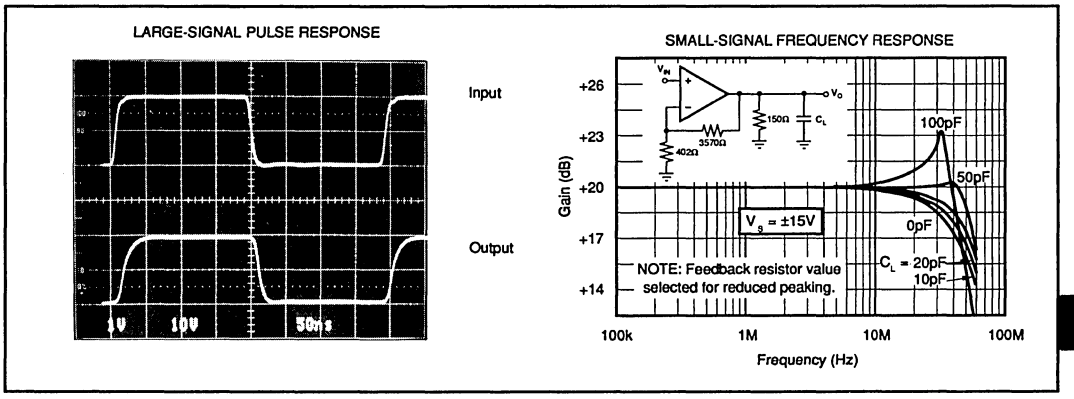


FIGURE 3. Dynamic Response, Gain = +10.

APPLICATIONS INFORMATION

For most circuit configurations, the OPA603 current-feedback op amp can be treated like a conventional op amp. As with a conventional op amp, the feedback network connected to the inverting input controls the closed-loop gain. But with a current-feedback op amp, the impedance of the feedback network also controls the open-loop gain and frequency response.

Feedback resistor values can be selected to provide a nearly constant closed-loop bandwidth over a very wide range of gain. This is in contrast to a conventional op amp where circuit bandwidth is inversely proportional to the closed-loop gain, sharply limiting bandwidth at high gain.

Figures 4a and 4b show appropriate feedback resistor values versus closed-loop gain for maximum bandwidth with minimal peaking. The dual vertical axes of these curves also show the resulting bandwidth. Note that the bandwidth remains nearly constant as gain is increased.

With control of the open-loop characteristics of the op amp, dynamic behavior can be tailored to an application's requirements. Lower feedback resistance gives wider bandwidth, more frequency-response peaking and more pulse response overshoot. The higher open-loop gain resulting from lower feedback network resistors also yields lower distortion. Higher feedback network resistance gives an over-damped response with little or no peaking and overshoot. This may be beneficial when driving capacitive loads. Feedback network impedance can also be varied to optimize dynamic performance. To achieve wider bandwidth, use a feedback resistor value somewhat lower than indicated in Figure 4.

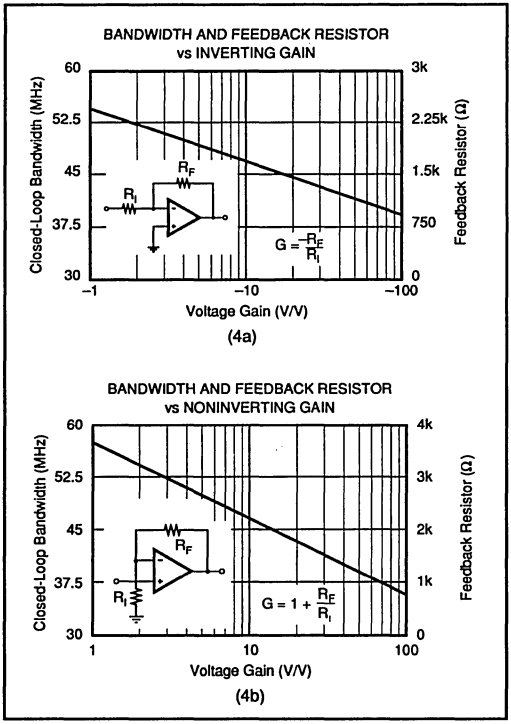


FIGURE 4. Feedback Resistor Selection Curves.

EXTENDING BANDWIDTH

For gains less than approximately 20, bandwidth can be extended by adding a capacitor, C_F, in parallel with a lower value for R_F. The optimum gain-setting resistor value in this case is far lower than those shown in Figure 1. For ±15V operation, select R_F with the following equation:

$$R_F\ (\Omega) = 30 \bullet (30 - G) \quad \text{for } V_S = \pm 15V$$

For example, for a gain of 10, use R_F = 600Ω. Optimum values differ slightly for ±5V operation:

$$R_F\ (\Omega) = 30 \bullet (23 - G) \quad \text{for } V_S = \pm 5V$$

C_F will range from 1pF to 10pF depending on the selected gain, load, and circuit layout. Adjust C_F to optimize bandwidth and minimize peaking. Figure 5 shows bandwidth which can be acheived using this technique.

Typical values for this capacitor range from 1pF to 10pF depending on closed-loop gain and load characteristics. Too large a value of C_F can cause instability.

UNITY-GAIN OPERATION

As Figure 4b indicates, the OPA603 can be operated in unity gain. A feedback resistor (approximately 2.8kΩ) sets the appropriate open-loop characteristics and resistor R_I is omitted. Just as with gains greater than one, the value of the feedback resistor (and capacitor if used) can be optimized for the desired dynamic response and load characteristics.

Care should be exercised not to exceed the maximum differential input voltage rating of ±6V. Large input voltage steps which exceed the device's slew rate of 1000V/µs can apply excessive differential input voltage.

CIRCUIT LAYOUT

With any high-speed, wide-bandwidth circuitry, careful circuit layout will ensure best performance. Make short, direct circuit interconnections and avoid stray wiring capacitance—especially at the inverting input pin. A component-side ground plane will help ensure low ground impedance. Do not place the ground plane under or near the inputs and feedback network.

Power supplies should be bypassed with good high-frequency capacitors positioned close to the op amp pins. In most cases, a 0.01µF ceramic capacitor in parallel with a 2.2µF solid tantalum capacitor at each power supply pin is adequate. The OPA603 can deliver high load current—up to 150mA peak. Applications with low impedance or capacitive loads demand large current transients from the power supplies. It is the power supply bypass capacitors which must supply these current transients. Larger bypass capacitors such as 10µF solid tantalum capacitors may improve performance in these applications.

POWER DISSIPATION

High output current causes increased internal power dissipation in the OPA603. Copper leadframe construction maximizes heat dissipation compared to conventional plastic packages. To achieve best heat dissipation, solder the device directly to the circuit board and use wide circuit board traces. Solder the unused pins, (1, 5 and 8) to a top-side ground plane for improved power dissipation. Limit the load and signal conditions depending on maximum ambient temperature to assure operation within the power derating curve.

The OPA603 may be operated at reduced power supply voltage to minimize power dissipation. Detailed specifications are provided for both ±15V and ±5V operation.

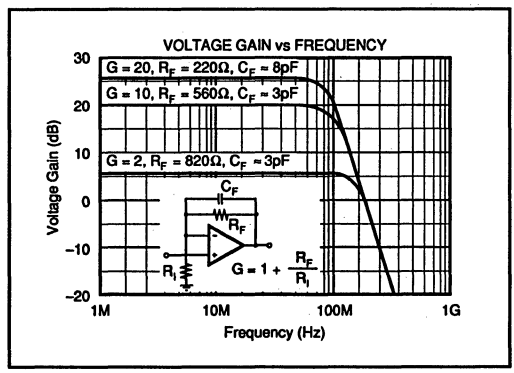


FIGURE 5. Bandwidth Results with Added Capacitor C_F.

APPLICATIONS CIRCUITS

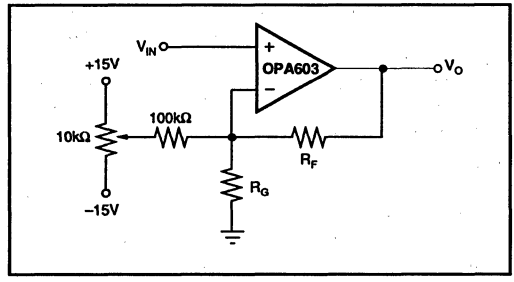


FIGURE 6. Offset Voltage Adjustment.

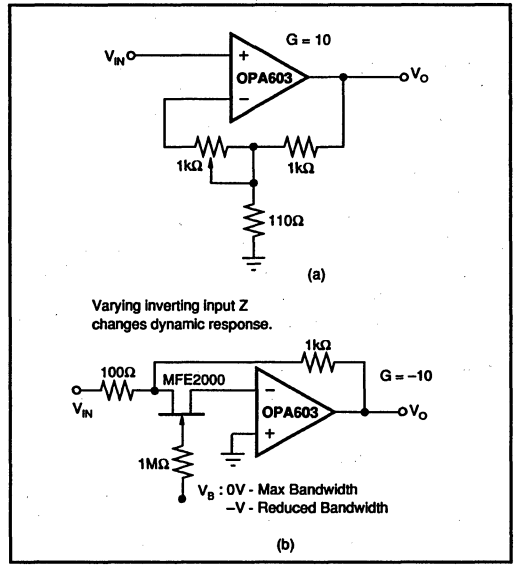


FIGURE 7. Controlling Dynamic Performance.

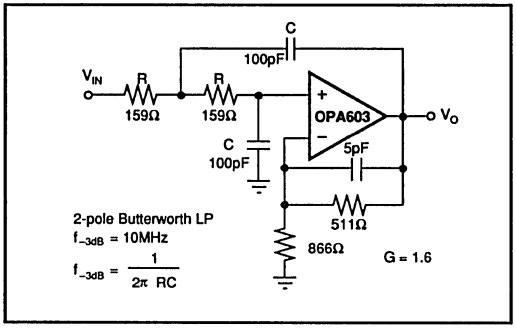


FIGURE 8. Low-Pass Filter — 10MHz.

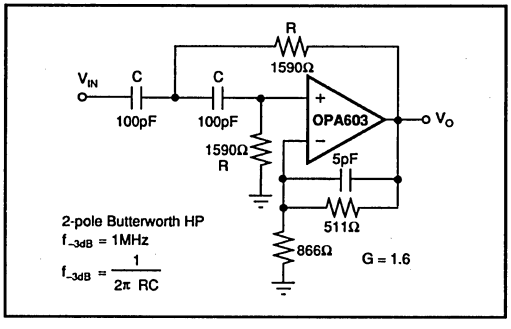


FIGURE 9. High-Pass Filter — 1MHz.

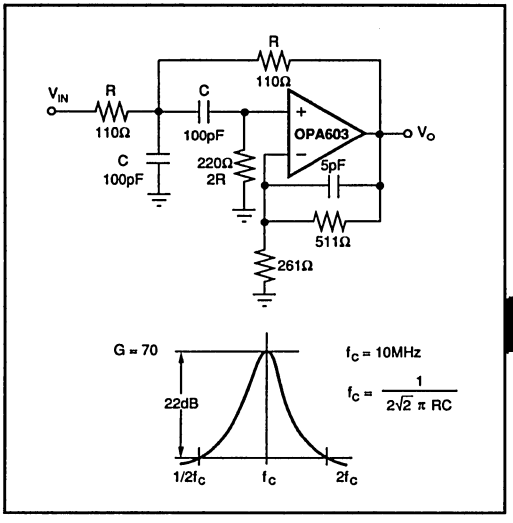
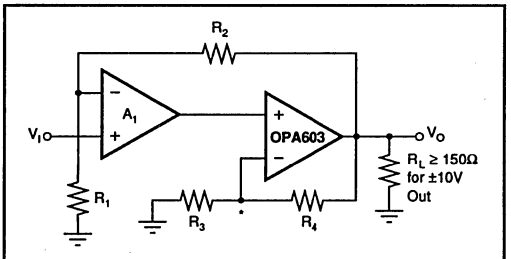


FIGURE 10. Bandpass Filter — 10MHz.



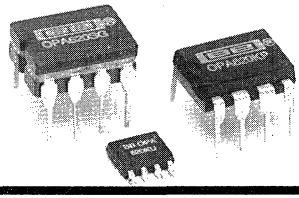
This composite amplifier uses the OPA603 current-feedback op amp to provide extended bandwidth and slew rate at high closed-loop gain. The feedback loop is closed around the composite amp, preserving the precision input characteristics of the OPA627/637. Use separate power supply bypass capacitors for each op amp.

* Minimize capacitance at this node.

GAIN (V/V)	A_1 OP AMP	R_1 (Ω)	R_2 (kΩ)	R_3 (Ω)	R_4 (kΩ)	–3dB (MHz)	SLEW RATE (V/μs)
100	OPA627	50.5(1)	4.99	20	1	15	700
1000	OPA637	49.9	4.99	12	1	11	500
NOTE: (1) Closest 1/2% value.							

FIGURE 11. Precision-Input Composite Amplifier.

BURR-BROWN®



OPA620

Wideband Precision OPERATIONAL AMPLIFIER

FEATURES

- LOW DISTORTION
- FAST SETTLING: 25ns (0.01%)
- GAIN-BANDWIDTH: 200MHz
- UNITY-GAIN STABLE
- LOW OFFSET VOLTAGE: ±100μV
- SLEW RATE: 250V/μs
- LOW DIFFERENTIAL GAIN/PHASE ERROR
- 8-PIN DIP AND SOIC PACKAGES AND DIE

APPLICATIONS

- HIGH-SPEED SIGNAL PROCESSING
- ADC/DAC BUFFER
- ULTRASOUND
- PULSE/RF AMPLIFIERS
- HIGH-RESOLUTION VIDEO
- ACTIVE FILTERS

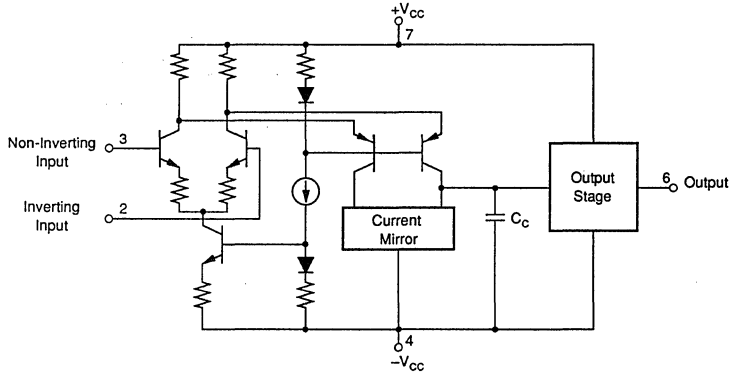
DESCRIPTION

The OPA620 is a precision wideband monolithic operational amplifier featuring very fast settling time, low differential gain and phase error, and high output current drive capability.

The OPA620 is internally compensated for unity-gain stability. This amplifier has a very low offset, fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA620 may be used in all op amp applications requiring high speed and precision.

Low noise and distortion, wide bandwidth, and high linearity make this amplifier suitable for RF and video applications. Short-circuit protection is provided by an internal current-limiting circuit.

The OPA620 is available in plastic, ceramic, SOIC packages, and die form. Two temperature ranges are offered: 0°C to +70°C and –55°C to +125°C.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510

PDS-872C

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA620KP/KU			OPA620KG/SG			OPA620LG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE											
Voltage: f_O = 100Hz	R_S = 0Ω		10			*			*		nV/√Hz
f_O = 1kHz			5.5			*			*		nV/√Hz
f_O = 10kHz			3.3			*			*		nV/√Hz
f_O = 100kHz			2.5			*			*		nV/√Hz
f_O = 1MHz to 100MHz			2.3			*			*		nV/√Hz
f_B = 100Hz to 10MHz			8.0			*			*		µV, rms
Current: f_O = 10kHz to 100MHz			2.3			*			*		pA/√Hz
OFFSET VOLTAGE[1]											
Input Offset Voltage	V_{CM} = 0VDC		±200	±1mV		*	*		±100	±500	µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±8			*			*		µV/°C
Supply Rejection	$\pm V_{CC}$ = 4.5V to 5.5V	50	60		*	*		55	*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		15	30		*	*		*	25	µA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		0.2	2		*	*		*	*	µA
INPUT IMPEDANCE											
Differential	Open-Loop		15 || 1			*			*		kΩ || pF
Common-Mode			1 || 1			*			*		MΩ || pF
INPUT VOLTAGE RANGE											
Common-Mode Input Range		±3.0	±3.5		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±2.5VDC, V_O = 0VDC	65	75		*	*		70	*		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L = 100Ω	50	60		*	*		55	*		dB
	R_L = 50Ω	48	58		*	*		53	*		dB
FREQUENCY RESPONSE											
Closed-Loop Bandwidth	Gain = +1V/V		300			*			*		MHz
(–3dB)	Gain = +2V/V		100			*			*		MHz
	Gain = +5V/V		40			*			*		MHz
	Gain = +10V/V		20			*			*		MHz
Gain-Bandwidth	Gain = +10V/V		200			*			*		MHz
Differential Gain	3.58MHz, G = +1V/V		0.05			*			*		%
Differential Phase	3.58MHz, G = +1V/V		0.05			*			*		Degrees
Harmonic Distortion[2]	G = +2V/V, f = 10MHz, V_O = 2Vp-p										
	Second Harmonic		–61	–50		*	*		*	*	dBc[3]
	Third Harmonic		–65	–55		*	*		*	*	dBc
Full Power Response[2]	V_O = 5Vp-p, Gain = +1V/V	11	16		*	*		*	*		MHz
	V_O = 2Vp-p, Gain = +1V/V	27	40		*	*		*	*		MHz
Slew Rate[2]	2V Step, Gain = –1V/V	175	250		*	*		*	*		V/µs
Overshoot	2V Step, Gain = –1V/V		10			*			*		%
Settling Time: 0.1%	2V Step, Gain = –1V/V		13			*			*		ns
0.01%			25			*			*		ns
Phase Margin	Gain = +1V/V		60			*			*		Degrees
Rise Time	Gain = +1V/V, 10% to 90%								*		
	V_O = 100mVp-p; Small Signal		2			*			*		ns
	V_O = 6Vp-p; Large Signal		22			*			*		ns
RATED OUTPUT											
Voltage Output	R_L = 100Ω	±2.8	±3.0		*	*		*	*		V
	R_L = 50Ω	±2.5	±3.0		*	*		*	*		V
Output Resistance	1MHz, Gain = +1V/V		0.015			*			*		Ω
Load Capacitance Stability	Gain = +1V/V		20			*			*		pF
Short Circuit Current	Continuous		±150			*			*		mA
POWER SUPPLY											
Rated Voltage	$\pm V_{CC}$		5			*			*		VDC
Derated Performance	$\pm V_{CC}$	4.0		6.0	*		*	*		*	VDC
Current, Quiescent	I_O = 0mADC		21	23		*	*		*	*	mA
TEMPERATURE RANGE											
Specification: KP, KU, KG, LG	Ambient Temperature	0		+70	*		*	*		*	°C
SG					–55		+125				°C
Operating: KG, LG, SG	Ambient Temperature				–55		+125	–55		+125	°C
KP, KU		–25		+85							°C
θ_{JA}											
KG, LG, SG						125			125		°C/W
KP			90								°C/W
KU			100								°C/W

* Same specifications as for KP/KU.

SPECIFICATIONS (cont)

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA620KP/KU			OPA620KG/SG			OPA620LG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification: KP, KU, KG, LG	Ambient Temperature	0		+70	*		*	*		*	°C
SG					–55		+125				°C
OFFSET VOLTAGE[1]											
Average Drift	T_A = T_{MIN} to T_{MAX}		±8			*			*		µV/°C
Supply Rejection	±V_{CC} = 4.5V to 5.5V	45	60		*	*		50	*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		15	40		*	*		*	35	µA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		0.2	5		*	*		*	*	µA
INPUT VOLTAGE RANGE											
Common-Mode Input Range		±2.5	±3.0		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±2.5VDC, V_O = 0VDC	60	75		*	*		65	*		dB
OPEN LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L = 100Ω	46	60		*	*		52	*		dB
	R_L = 50Ω	44	58		*	*		50	*		dB
RATED OUTPUT											
Voltage Output	R_L = 100Ω	±2.6	±3.0		*	*		*	*		V
	R_L = 50Ω	±2.5	±3.0		*	*		*	*		V
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		21	25		*	*		*	*	mA

* Same specifications as for KP/KU.

NOTES: (1) Offset Voltage specifications are also guaranteed with units fully warmed up. (2) Parameter is sample tested. (3) dBc = dB refered to carrier-input signal.

ORDERING INFORMATION

OPA620 ( ) ( )

- Basic Model Number
- Performance Grade Code
  - K, L = 0°C to +70°C
  - S = –55°C to +125°C
- Package Code
  - G = 8-pin Ceramic DIP
  - P = 8-pin Plastic DIP
  - U = 8-pin Plastic SOIC

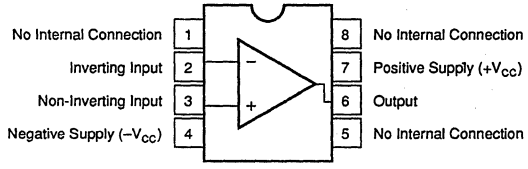
ABSOLUTE MAXIMUM RATINGS

Supply	±7VDC
Internal Power Dissipation[4]	See Applications Information
Differential Input Voltage	Total V_{CC}
Input Voltage Range	See Applications Information
Storage Temperature Range: KG, LG, SG	–65°C to +150°C
KP,KU	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Output Short Circuit to Ground (+25°C)	Continuous to Ground
Junction Temperature (T_J)	+175°C

NOTE: (4) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

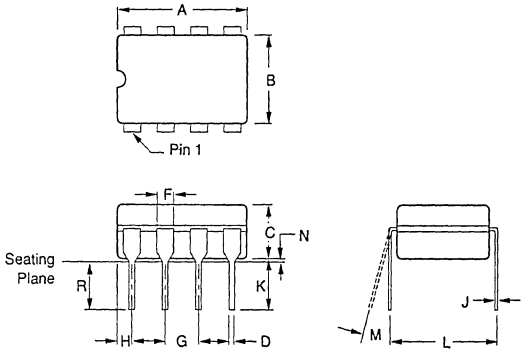
PIN CONFIGURATION (8-PIN DIP)

Top View



MECHANICAL

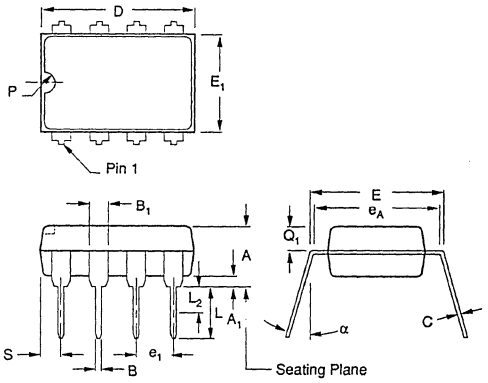
G Package — 8-Pin Ceramic



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.375	.405	9.53	10.28
B	.245	.251	6.22	6.38
C	.140	.170	3.56	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	—	.098	—	2.49
J	.008	.012	0.20	0.30
K	.150	—	3.80	—
L	.290	.320	7.37	8.13
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.125	.175	3.18	4.45

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

P Package — 8-Pin Plastic DIP

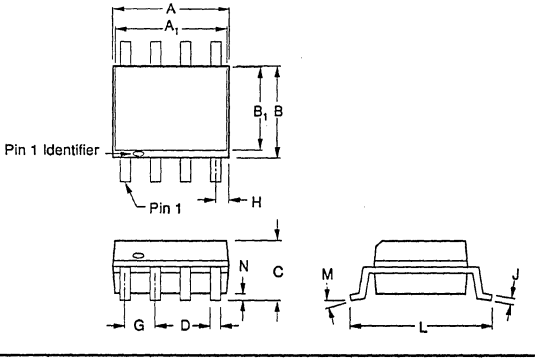


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D (1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2 (2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q1	.040	.075	1.02	1.91
S (1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e_1 and e_A applies in zone L_2 when unit installed.
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

U Package — 8-Pin SOIC



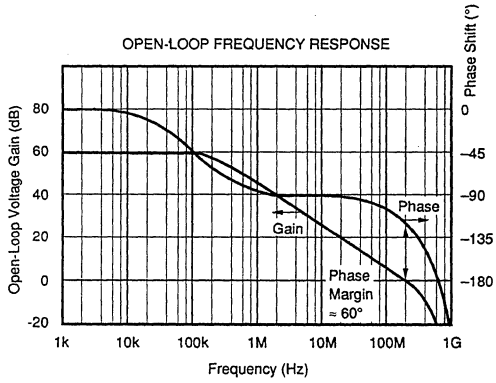
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.201	4.70	5.11
A1	.178	.201	4.52	5.11
B	.146	.162	3.71	4.11
B1	.130	.149	3.30	3.78
C	.054	.145	1.37	3.69
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.018	.026	0.46	0.66
J	.008	.012	0.20	0.30
L	.220	.252	5.59	6.40
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

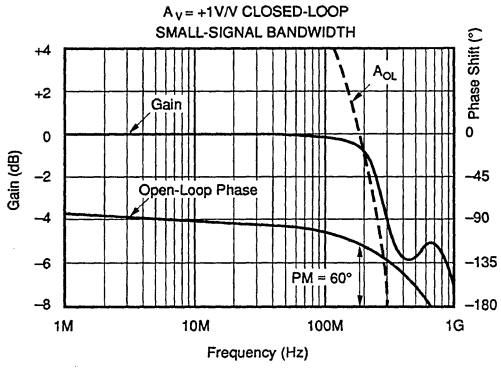
TYPICAL PERFORMANCE CURVES

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

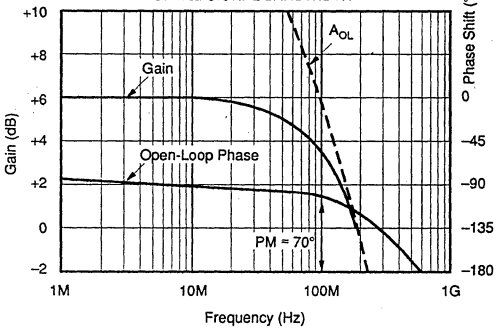
OPEN-LOOP FREQUENCY RESPONSE



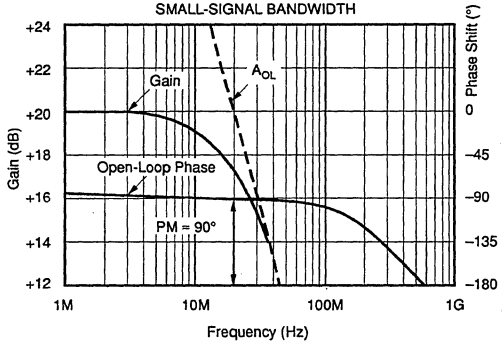
A_V = +1V/V CLOSED-LOOP SMALL-SIGNAL BANDWIDTH



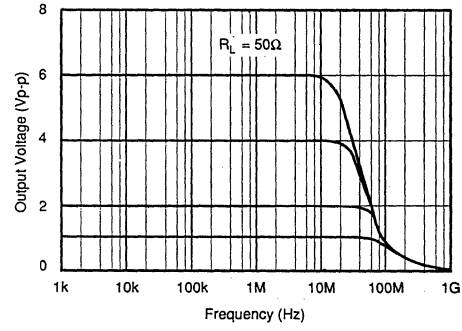
A_V = +2V/V CLOSED-LOOP SMALL-SIGNAL BANDWIDTH



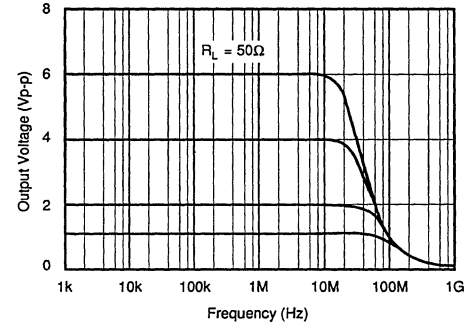
A_V = +10V/V CLOSED-LOOP SMALL-SIGNAL BANDWIDTH



A_V = +1V/V CLOSED-LOOP BANDWIDTH vs OUTPUT VOLTAGE SWING



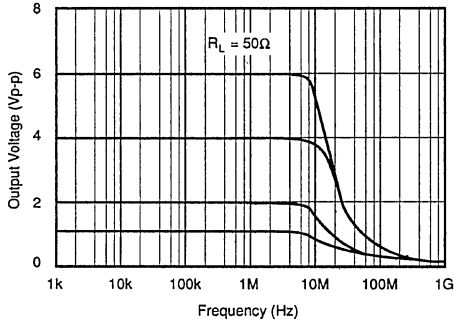
A_V = +2V/V CLOSED-LOOP BANDWIDTH vs OUTPUT VOLTAGE SWING



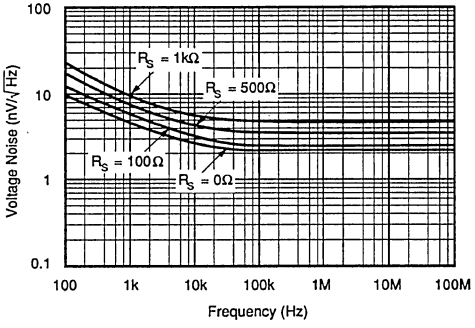
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

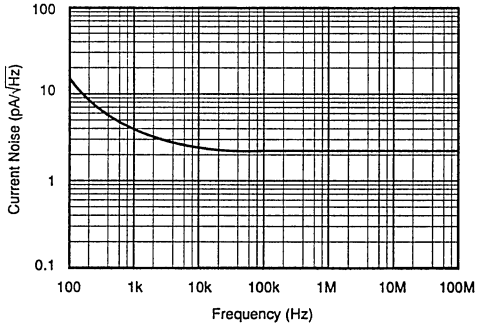
A_V = +10V/V CLOSED-LOOP BANDWIDTH vs OUTPUT VOLTAGE SWING



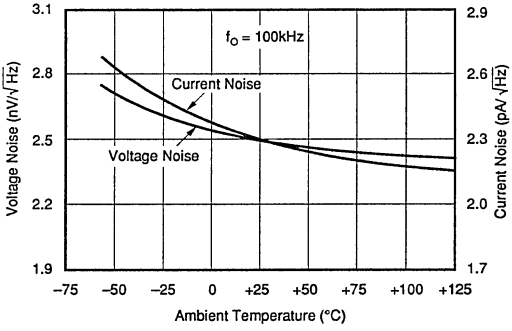
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY vs SOURCE RESISTANCE



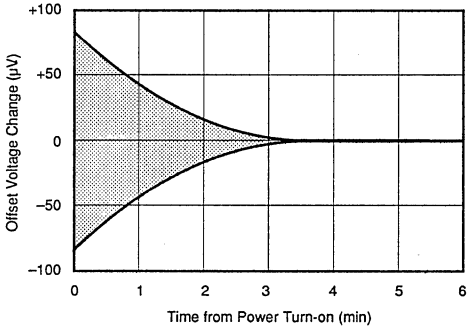
INPUT CURRENT NOISE SPECTRAL DENSITY



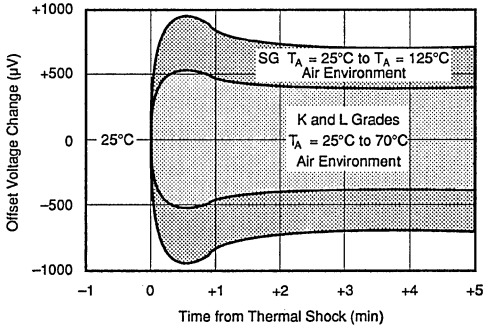
VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs TEMPERATURE



INPUT OFFSET VOLTAGE WARM-UP DRIFT



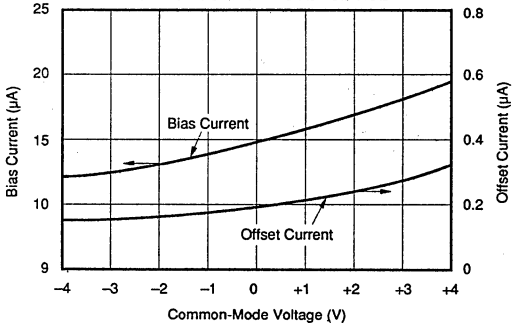
INPUT OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



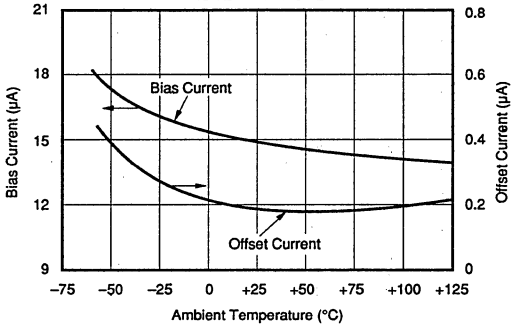
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

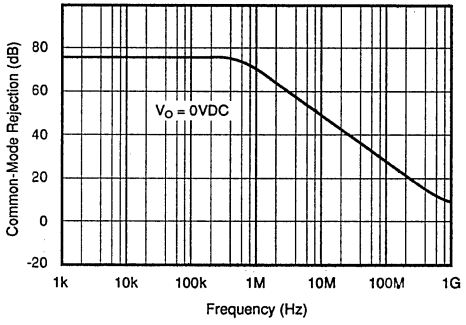
BIAS AND OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



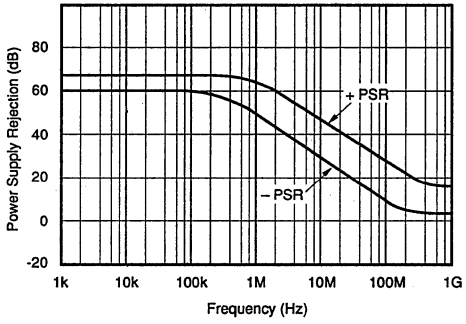
BIAS AND OFFSET CURRENT vs TEMPERATURE



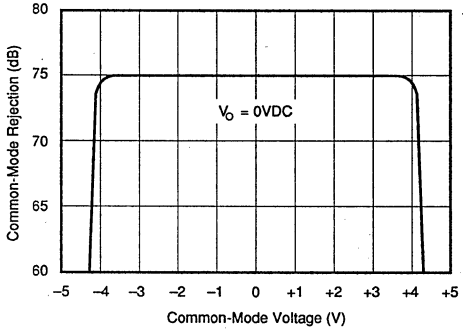
COMMON-MODE REJECTION vs FREQUENCY



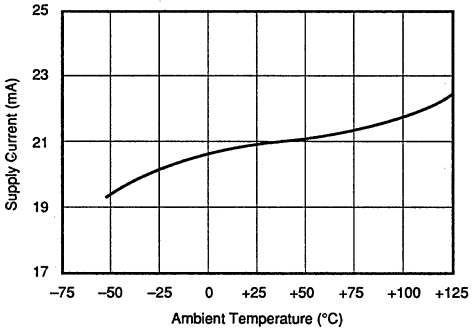
POWER SUPPLY REJECTION vs FREQUENCY



COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



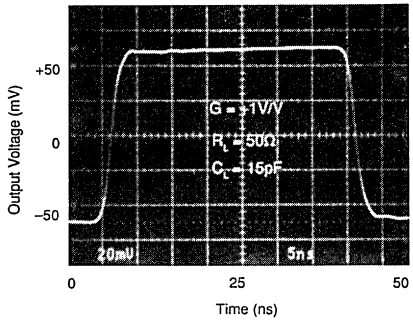
SUPPLY CURRENT vs TEMPERATURE



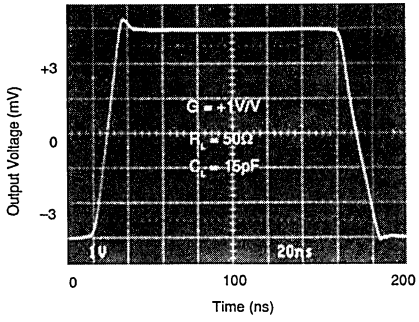
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

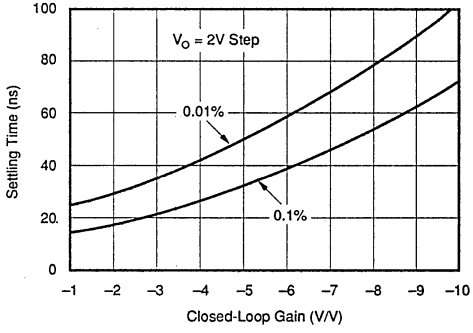
SMALL-SIGNAL TRANSIENT RESPONSE



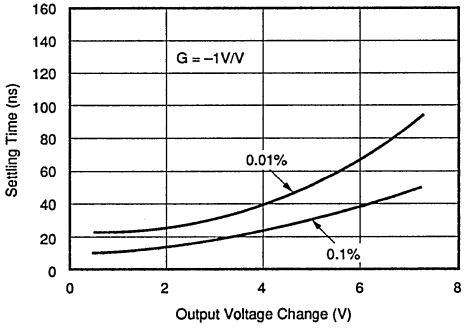
LARGE-SIGNAL TRANSIENT RESPONSE



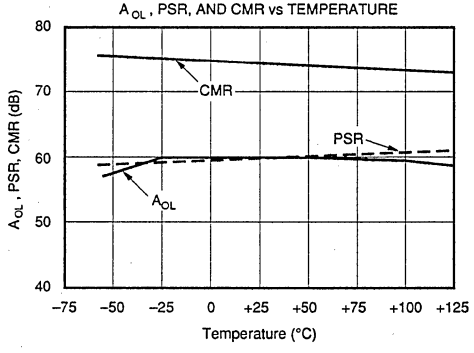
SETTLING TIME vs CLOSED-LOOP GAIN



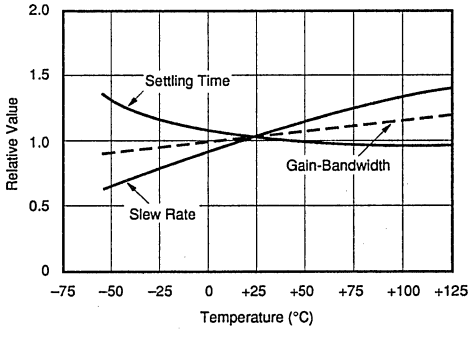
SETTLING TIME vs OUTPUT VOLTAGE CHANGE



A_{OL}, PSR, AND CMR vs TEMPERATURE



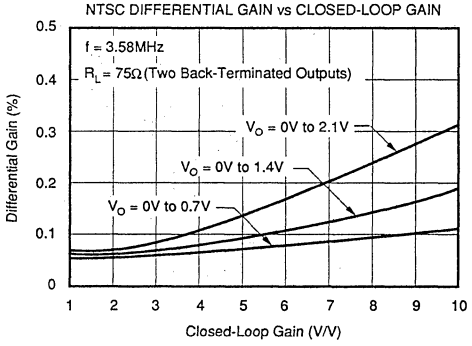
FREQUENCY CHARACTERISTICS vs TEMPERATURE



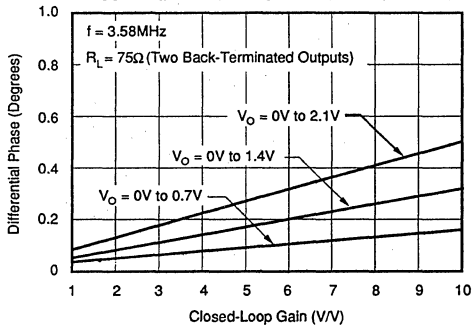
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

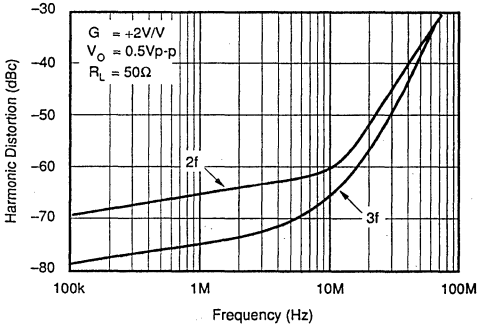
NTSC DIFFERENTIAL GAIN vs CLOSED-LOOP GAIN



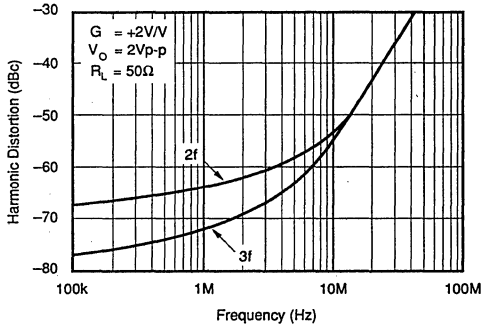
NTSC DIFFERENTIAL PHASE vs CLOSED-LOOP GAIN



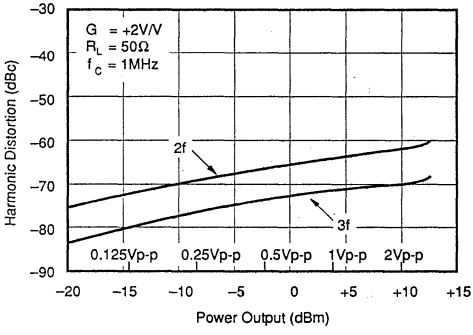
SMALL-SIGNAL
HARMONIC DISTORTION vs FREQUENCY



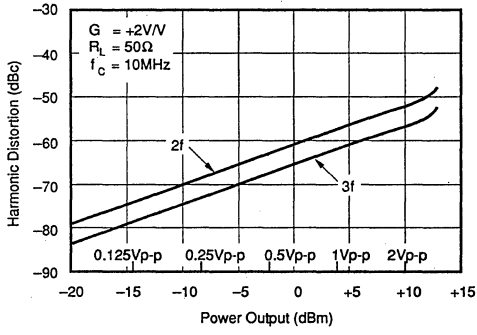
LARGE-SIGNAL
HARMONIC DISTORTION vs FREQUENCY



1MHz HARMONIC DISTORTION
vs POWER OUTPUT



10MHz HARMONIC DISTORTION
vs POWER OUTPUT



APPLICATIONS INFORMATION

DISCUSSION OF PERFORMANCE

The OPA620 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA620's design uses a "Classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer many disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e. one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Bias current cancellation through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 *microseconds* even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA620's "Classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA620. The use of low-drift thin-film resistors allows internal operating currents to be laser-trimmed at wafer-level to optimize AC performance such as bandwidth and settling time, as well as DC parameters such as input offset voltage and drift. The result is a wideband, high-frequency monolithic operational amplifier with a gain-bandwitdth product of 200MHz, a 0.01% settling time of 25ns, and an input offset voltage of 100µV.

WIRING PRECAUTIONS

Maximizing the OPA620's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA620, as it is with all high-frequency circuits. Oscillations at frequencies of 200MHz and above can easily occur if good grounding techniques are not used. A heavy ground plane (2oz copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (1µF to 10µF) with very short leads are recommended. Although not required, a parallel 0.01µF ceramic may be added if desired. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

2) Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

3) Whenever possible, solder the OPA620 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations. If sockets must be used, consider using zero-profile solderless sockets such as Augat part number 8134-HC-5P2. Alternately, Teflon® standoffs located close to the amplifier's pins can be used to mount feedback components.

4) Resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1kΩ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely *unacceptable* in high-frequency circuits.

5) Surface mount components (chip resistors, capacitors, etc) have low lead inductance and are therefore strongly recommended. Circuits using all surface mount components

Teflon® E. I. Du Pont de Nemours & Co.

with the OPA620KU (SOIC package) will offer the best AC performance. The parasitic package inductance and capacitance for the SOIC is lower than the both the Cerdip and 8-lead Plastic DIP.

6) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

7) Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, use of ±15V supplies will destroy the part.

8) Standard commercial test equipment has not been designed to test devices in the OPA620's speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

9) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

10) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

OFFSET VOLTAGE ADJUSTMENT

The OPA620's input offset voltage is laser-trimmed and will require no further adjustment for most applications. However, if additional adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3. This will reduce input bias current errors to the amplifier's offset current, which is typically only 0.2µA.

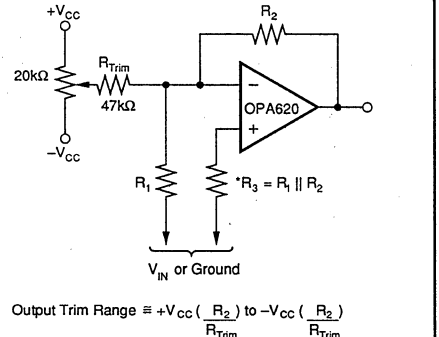


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA620 incorporates on-chip ESD protection diodes as shown in Figure 2. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

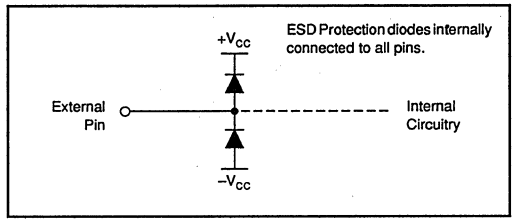


FIGURE 2. Internal ESD Protection.

All pins on the OPA620 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

The internal protection diodes are designed to withstand 2.5kV (using Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA620.

OUTPUT DRIVE CAPABILITY

The OPA620's design uses large output devices and has been optimized to drive 50Ω and 75Ω resistive loads. The device can easily drive 6Vp-p into a 50Ω load. This high-output drive capability makes the OPA620 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Internal current-limiting circuitry limits output current to about 150mA at 25°C. This prevents destruction from accidental shorts to common and eliminates the need for external current-limiting circuitry. Although the device can withstand momentary shorts to either power supply, it is not recommended.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the

OPA620 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

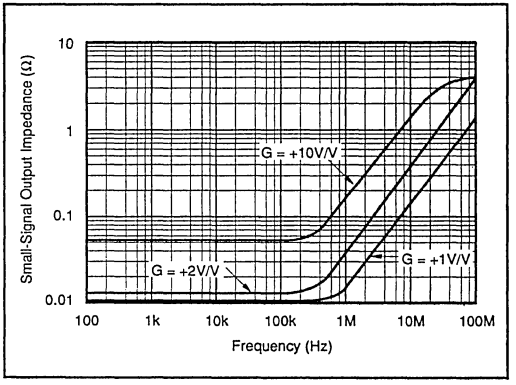


FIGURE 3. Small-Signal Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA620 does not require a heat sink for operation in most environments. The use of a heat sink, however, will reduce the internal thermal rise and will result in cooler, more relaible operation. At extreme temperatures and under full load conditions a heat sink is necessary. See "Maximum Power Dissipation" curve, Figure 4.

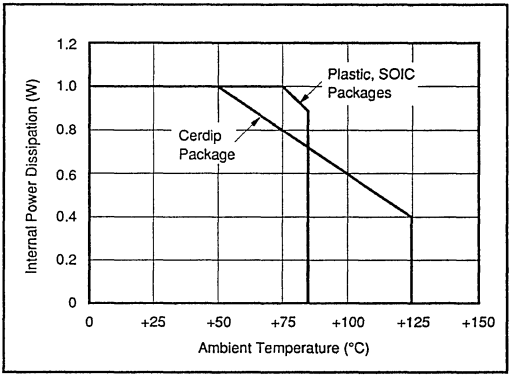


FIGURE 4. Maximum Power Dissipation.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 23mA = 230mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC}/2$, and is equal to P_{DL}, max = $(\pm V_{CC})^2/4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

When the output is shorted to common $P_{DL} = 5V \times 150mA = 750mW$. Thus, $P_D = 230mW + 750mW \approx 1W$. Note that the short-circuit condition represents the maximum amount of internal power dissipation that can be generated. Thus, the "Maximum Power Dissipation" curve starts at 1W and is derated based on a 175°C maximum junction temperature and the junction-to-ambient thermal resistance, θ_{JA}, of each package. The variation of short-circuit current with temperature is shown in Figure 5.

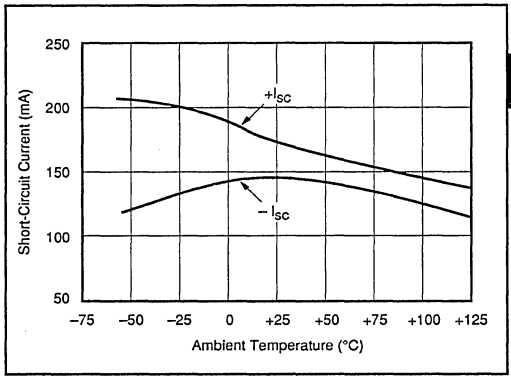


FIGURE 5. Short-Circuit Current vs Temperature.

CAPACITIVE LOADS

The OPA620's output stage has been optimized to drive resistive loads as low as 50Ω. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 20pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 6. This is particularly important when driving high capacitance loads such as flash A/D converters.

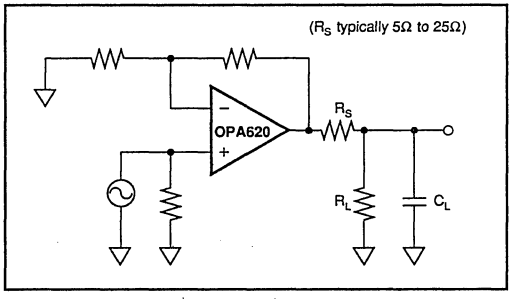


FIGURE 6. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA620 is internally compensated and is stable in unity gain with a phase margin of approximately 60°. However, the unity gain buffer is the most demanding circuit configuration for loop stability and oscillations are most likely to occur in this gain. If possible, use the device in a noise gain of two or greater to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of –1V/V is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA620 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of ±200µV centered around the final value of 2V.

Settling time, specified in an inverting gain of one, occurs in only 25ns to 0.01% for a 2V step, making the OPA620 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Wiring Precautions." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 30ns.

In practice, settling time measurements on the OPA620 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

Figure 7 shows the test circuit used to measure settling time for the OPA620. This approach uses a 16-bit sampling oscilloscope to monitor the input and output pulses. These waveforms are captured by the sampling scope, averaged, and then subtracted from each other in software to produce the error signal. This technique eliminates the need for the traditional "false-summing junction," which adds extra parasitic capacitance. Note that instead of an additional flat-top generator, this technique uses the scope's built-in calibration source as the input signal.

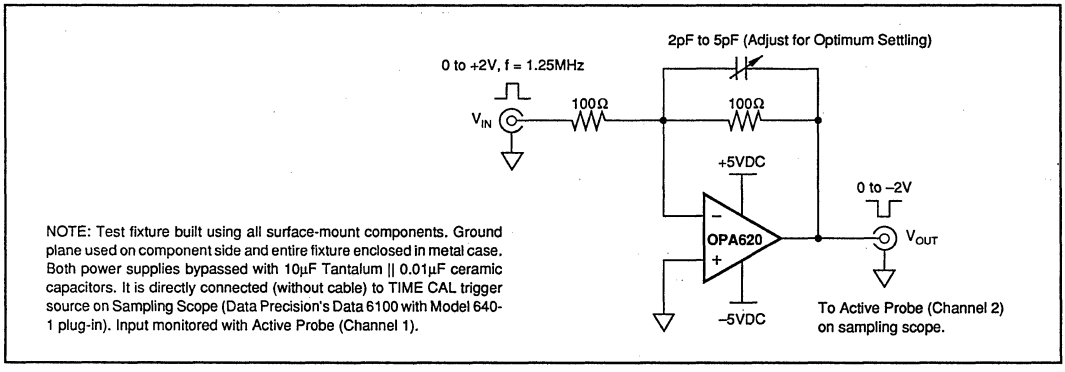


FIGURE 7. Settling Time Test Circuit.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase with closed-loop gain and output voltage transition as shown in the Typical Performance Curves. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

DISTORTION

The OPA620's Harmonic Distortion characteristics into a 50Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 8. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

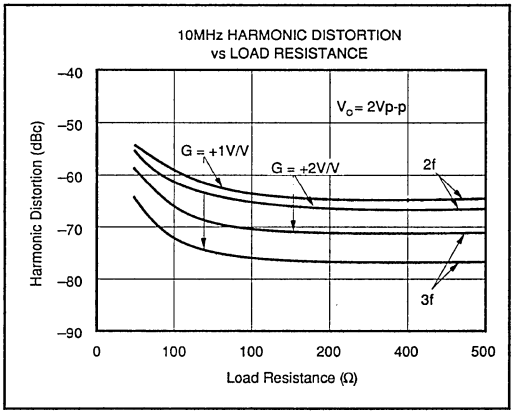


FIGURE 8. 10MHz Harmonic Distortion vs Load Resistance.

Two-tone, third-order intermodulation distortion (IM) is an important parameter for many RF amplifier applications. Figure 9 shows the OPA620's two-tone, third-order IM intercept vs frequency. For these measurements, tones were spaced 1MHz apart. This curve is particularly useful for determining the magnitude of the third-order IM products as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA620 to operate in a gain of +2V/V and drive 2Vp-p into 50Ω at a frequency of 10MHz. Referring to Figure 9 we find that the intercept point is +40dBm. The magnitude of the third-order IM products can now be easily calculated from the expression:

$$\text{Third IMD} = 2(\text{OPI}^3\text{P} - P_O)$$

where OPI^3P = third-order output intercept, dBm
P_O = output level/tone, dBm/tone
Third IMD = third-order intermodulation ratio below each output tone, dB

For this case OPI^3P = 40dBm, P_O = 10dBm, and the third-order IMD = 2(40 – 10) = 60dB below either 10dBm tone. The OPA620's low IMD makes the device an excellent choice for a variety of RF signal processing applications.

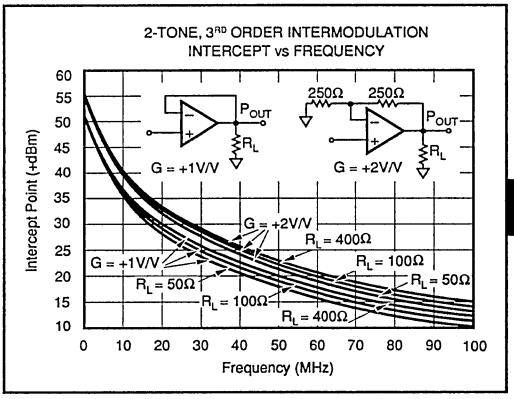


FIGURE 9. 2-Tone, 3rd Order Intermodulation Intercept vs Frequency.

NOISE FIGURE

The OPA620's voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA620's Noise Figure vs Source Resistance is shown in Figure 10.

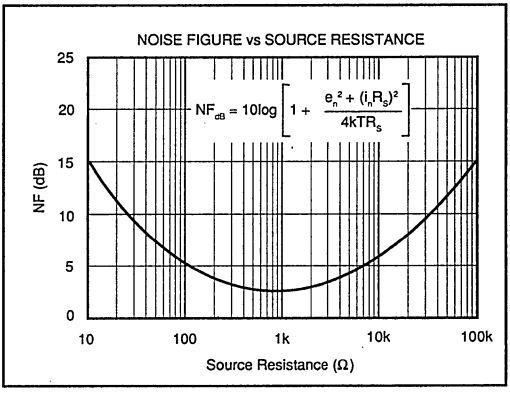


FIGURE 10. Noise Figure vs Source Resistance.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models using MicroSim Corporation's PSpice are available for the OPA620. Request Burr-Brown Application Note AN-167.

RELIABILITY DATA

Extensive reliability testing has been performed on the OPA620. Accelerated life testing (2000 hours) at maximum operating temperature was used to calculate MTTF at an ambient temperature of 25°C. These test results yield MTTF of: Cerdip package = 1.31E+9 Hours, Plastic DIP = 5.02E+7 Hours, and SOIC = 2.94E+7 Hours. Additional tests such as PCT have also been performed. Reliability reports are available upon request for each of the package options offered.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Request DEM1135 for 8-Pin DIP, and DEM1136 for SOIC package.

APPLICATIONS

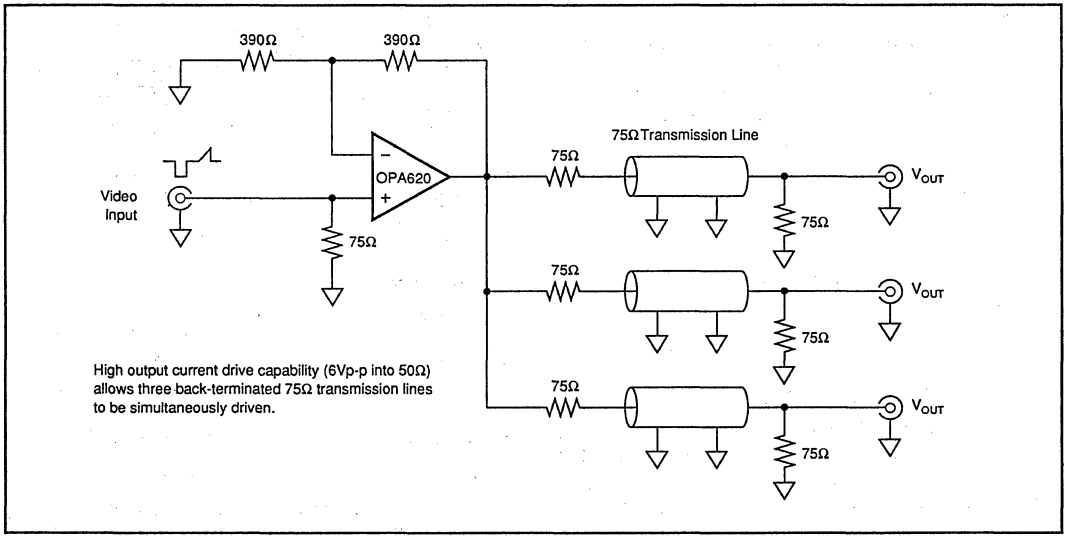


FIGURE 11. Video Distribution Amplifier.

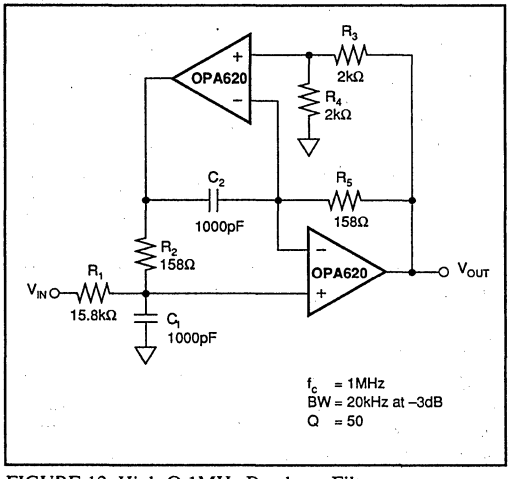


FIGURE 12. High-Q 1MHz Bandpass Filter.

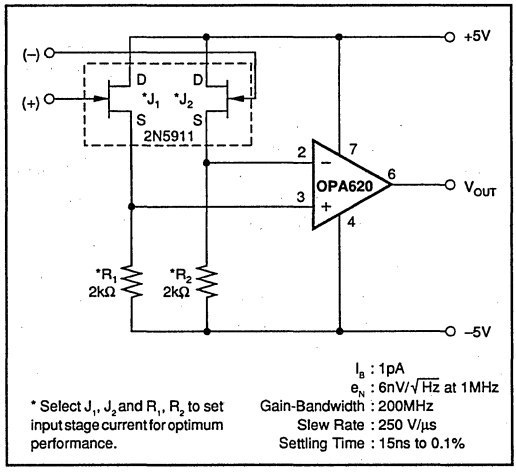


FIGURE 13. Low Noise, Wideband FET Input Op Amp.

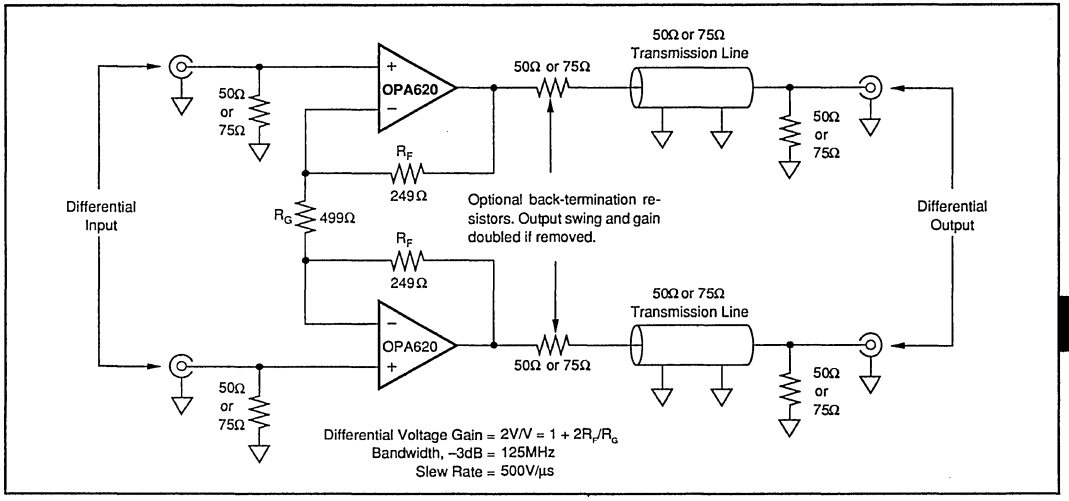


FIGURE 14. Differential Line Driver for 50Ω or 75Ω Systems.

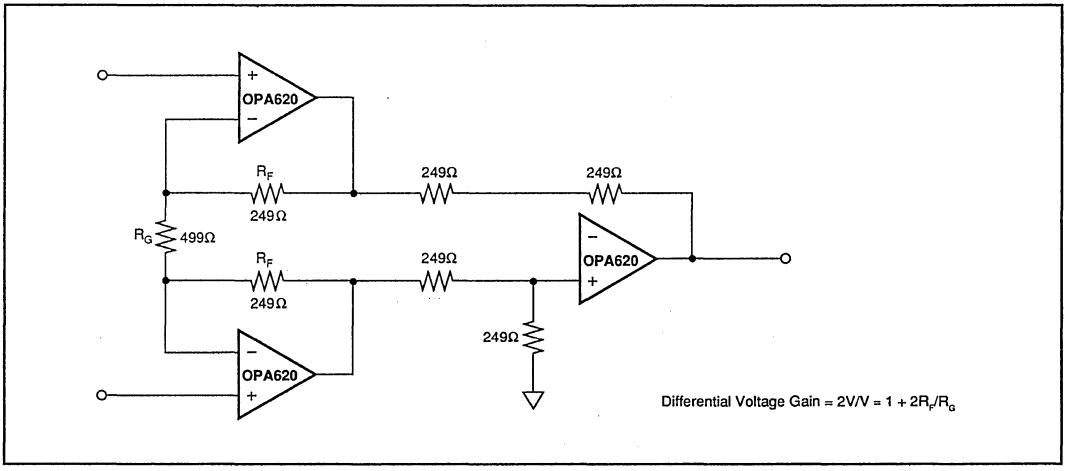


FIGURE 15. Wideband, Fast-Settling Instrumentation Amplifier.

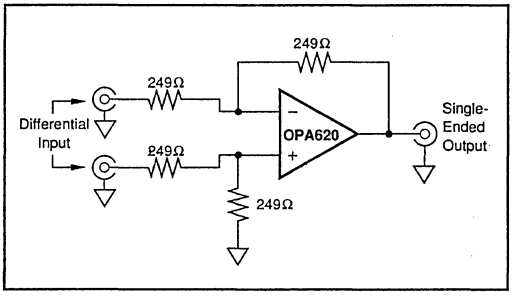


FIGURE 16. Unity Gain Difference Amplifier.

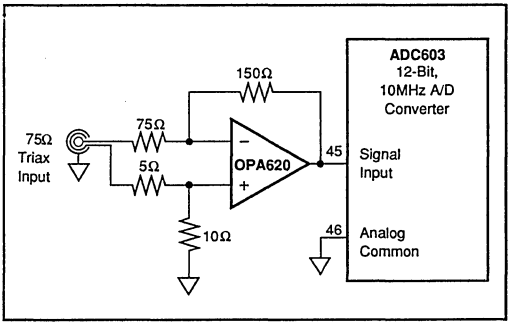
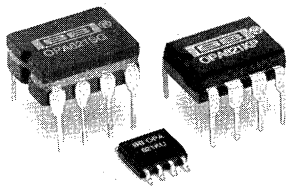


FIGURE 17. Differential Input Buffer Amplifier (G=–2V/V).

BURR-BROWN®



OPA621

Wideband Precision OPERATIONAL AMPLIFIER

FEATURES

- VERY LOW DISTORTION
- FAST SETTLING: 25ns (0.01%)
- GAIN-BANDWIDTH: 500MHz
- STABLE IN GAINS: ≥ ±2V/V
- LOW OFFSET VOLTAGE: ±100µV
- SLEW RATE: 500V/µs
- LOW DIFFERENTIAL GAIN/PHASE ERROR
- 8-PIN DIP, SOIC PACKAGES AND DIE

APPLICATIONS

- HIGH-SPEED SIGNAL PROCESSING
- ADC/DAC BUFFER
- ULTRASOUND
- PULSE/RF AMPLIFIERS
- HIGH-RESOLUTION VIDEO
- ACTIVE FILTERS

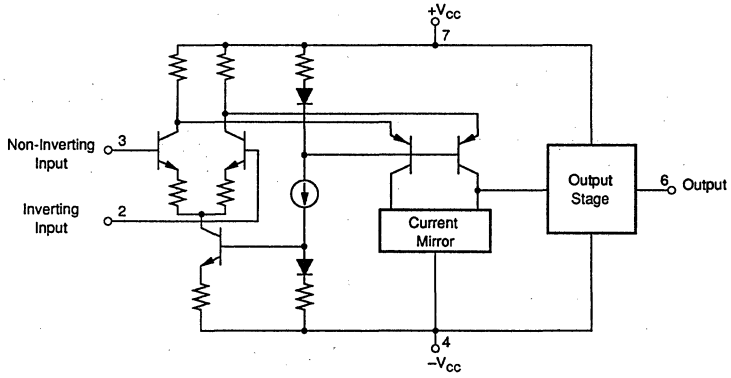
DESCRIPTION

The OPA621 is a precision wideband monolithic operational amplifier featuring very fast settling time, low differential gain and phase error, and high output current drive capability.

The OPA621 is stable in gains of ±2V/V or higher. This amplifier has a very low offset, fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA621 may be used in all op amp applications requiring high speed and precision.

Low noise and distortion, wide bandwidth, and high linearity make this amplifier suitable for RF and video applications. Short circuit protection is provided by an internal current-limiting circuit.

The OPA621 is available in plastic, ceramic, SOIC packages, and die form. Two temperature ranges are offered: 0°C to +70°C and –55°C to +125°C.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-939C

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA621KP/KU MIN	OPA621KP/KU TYP	OPA621KP/KU MAX	OPA621KG/SG MIN	OPA621KG/SG TYP	OPA621KG/SG MAX	OPA621LG MIN	OPA621LG TYP	OPA621LG MAX	UNITS
INPUT NOISE											
Voltage: f_O= 100Hz	R_S = 0Ω		10			*			*		nV/√Hz
f_O= 1kHz			5.5			*			*		nV/√Hz
f_O= 10kHz			3.3			*			*		nV/√Hz
f_O= 100kHz			2.5			*			*		nV/√Hz
f_O= 1MHz to 100MHz			2.3			*			*		nV/√Hz
f_B= 100Hz to 10MHz			8.0			*			*		µV, rms
Current: f_O= 10kHz to 100MHz			2.3			*			*		pA/√Hz
OFFSET VOLTAGE[1]											
Input Offset Voltage	V_{CM} = 0VDC		±200	±1mV		*	*		±100	±500	µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±12			*			*		µV/°C
Supply Rejection	$\pm V_{CC}$ = 4.5V to 5.5V	50	60		*	*		55	*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		18	30		*	*		*	25	µA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		0.2	2		*	*		*	*	µA
INPUT IMPEDANCE											
Differential	Open-Loop		15 || 1			*			*		kΩ || pF
Common-Mode			1 || 1			*			*		MΩ || pF
INPUT VOLTAGE RANGE											
Common-Mode Input Range		±3.0	±3.5		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±2.5VDC, V_O = 0VDC	65	75		*	*		70	*		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L = 100Ω	50	60		*	*		55	*		dB
	R_L = 50Ω	48	58		*	*		53	*		dB
FREQUENCY RESPONSE											
Closed-Loop Bandwidth											
(–3dB)	Gain = +2V/V		500			*			*		MHz
	Gain = +5V/V		100			*			*		MHz
	Gain = +10V/V		50			*			*		MHz
Gain-Bandwidth	Gain = +10V/V		500			*			*		MHz
Differential Gain	3.58MHz, G = +2V/V		0.05			*			*		%
Differential Phase	3.58MHz, G = +2V/V		0.05			*			*		Degrees
Harmonic Distortion[2]	G = +2V/V, f = 10MHz, V_O = 2Vp-p										
	f = 10MHz, Second Harmonic		–62	–50		*	*		*	*	dBc[3]
	Third Harmonic		–80	–70		*	*		*	*	dBc
Full Power Response[2]	V_O = 5Vp-p, Gain = +2V/V	22	32		*	*		*	*		MHz
	V_O = 2Vp-p, Gain = +2V/V	55	80		*	*		*	*		MHz
Slew Rate[2]	2V Step, Gain = –2V/V	350	500		*	*		*	*		V/µs
Overshoot	2V Step, Gain = –2V/V		15			*			*		%
Settling Time: 0.1%	2V Step, Gain = –2V/V		15			*			*		ns
0.01%			25			*			*		ns
Phase Margin	Gain = +2V/V		50			*			*		Degrees
Rise Time	Gain = +2V/V, 10% to 90%								*		
	V_O = 100mVp-p; Small Signal		1.8			*			*		ns
	V_O = 6Vp-p; Large Signal		8			*			*		ns
RATED OUTPUT											
Voltage Output	R_L = 100Ω	±2.8	±3.0		*	*		*	*		V
	R_L = 50Ω	±2.5	±3.0		*	*		*	*		V
Output Resistance	1MHz, Gain = +2V/V		0.015			*			*		Ω
Load Capacitance Stability	Gain = +2V/V		15			*			*		pF
Short Circuit Current	Continuous		±150			*			*		mA
POWER SUPPLY											
Rated Voltage	$\pm V_{CC}$		5			*			*		VDC
Derated Performance	$\pm V_{CC}$	4.0		6.0	*		*	*		*	VDC
Current, Quiescent	I_O = 0mADC		26	28		*	*		*	*	mA
TEMPERATURE RANGE											
Specification: KP, KU, KG, LG	Ambient Temperature	0		+70	*		*	*		*	°C
SG					–55		+125				°C
Operating: KG, LG, SG	Ambient Temperature				–55		+125	–55		+125	°C
KP, KU		–25		+85							°C
θ_{JA}											
KG, LG, SG						125			125		°C/W
KP			90								°C/W
KU			100								°C/W

* Same Specifications as for KP/KU.

SPECIFICATIONS (cont)

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA621KP/KU			OPA621KG/SG			OPA621LG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification: KP, KU, KG, LG	Ambient Temperature	0		+70	*		*	*		*	°C
SG					–55		+125				°C
OFFSET VOLTAGE[1]											
Average Drift	T_A = T_{MIN} to T_{MAX}		±12			*			*		µV/°C
Supply Rejection	±V_{CC} = 4.5V to 5.5V	45	60		*	*		50	*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		18	40		*	*		*	35	µA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		0.2	5		*	*		*	*	µA
INPUT VOLTAGE RANGE											
Common-Mode Input Range		±2.5	±3.0		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±2.5VDC, V_O = 0VDC	60	75		*	*		65	*		dB
OPEN LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L = 100Ω	46	60		*	*		52	*		dB
	R_L = 50Ω	44	58		*	*		50	*		dB
RATED OUTPUT											
Voltage Output	R_L = 100Ω	±2.6	±3.0		*	*		*	*		V
	R_L = 50Ω	±2.5	±3.0		*	*		*	*		V
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		26	30		*	*		*	*	mA

* Same specifications as for KP/KU.

NOTES: (1) Offset Voltage specifications are also guaranteed with units fully warmed up. (2) Parameter is sample tested. (3) dBc = dB refered to carrier-input signal.

ORDERING INFORMATION

OPA621 ( ) ( )

- Basic Model Number
- Performance Grade Code
  - K, L = 0°C to +70°C
  - S = –55°C to +125°C
- Package Code
  - G = 8-pin Ceramic DIP
  - P = 8-pin Plastic DIP
  - U = 8-pin Plastic SOIC

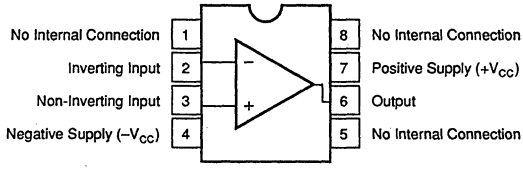
ABSOLUTE MAXIMUM RATINGS

Supply	±7VDC
Internal Power Dissipation[4]	See Applications Information
Differential Input Voltage	Total V_{CC}
Input Voltage Range	See Applications Information
Storage Temperature Range KG, LG, SG:	–65°C to +150°C
KP, KU:	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Output Short Circuit to Ground (+25°C)	Continuous to Ground
Junction Temperature (T_J)	+175°C

NOTE: (4) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

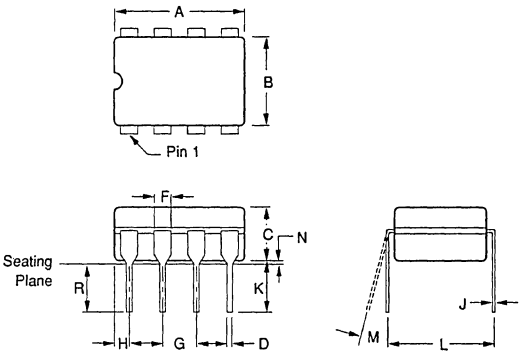
PIN CONFIGURATION (8-PIN DIP)

Top View



MECHANICAL

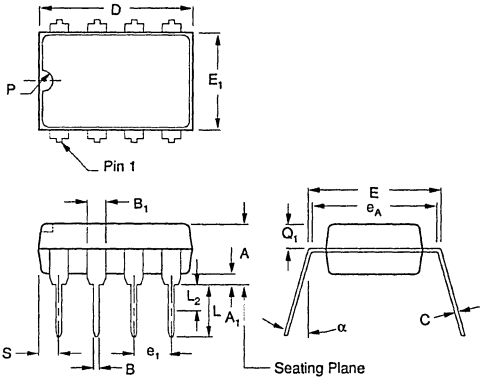
G Package — 8-Pin Ceramic



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.375	.405	9.53	10.28
B	.245	.251	6.22	6.38
C	.140	.170	3.56	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	—	.098	—	2.49
J	.008	.012	0.20	0.30
K	.150	—	3.80	—
L	.290	.320	7.37	8.13
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.125	.175	3.18	4.45

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

P Package — 8-Pin Plastic DIP

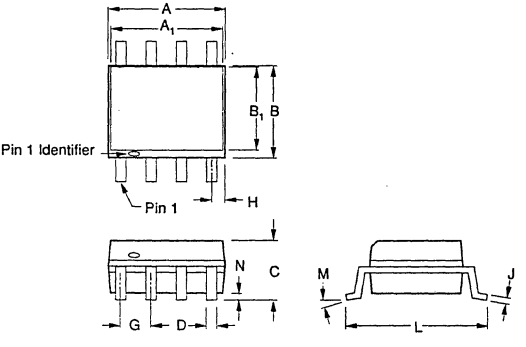


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D(1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2(2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q1	.040	.075	1.02	1.91
S(1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e_1 and e_A applies in zone L_2 when unit installed.
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

U Package — 8-Pin SOIC



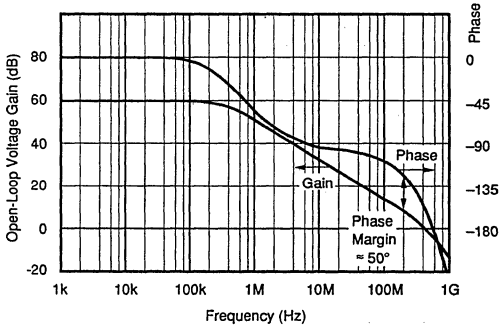
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.201	4.70	5.11
A1	.178	.201	4.52	5.11
B	.146	.162	3.71	4.11
B1	.130	.149	3.30	3.78
C	.054	.145	1.37	3.69
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.018	.026	0.46	0.66
J	.008	.012	0.20	0.30
L	.220	.252	5.59	6.40
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

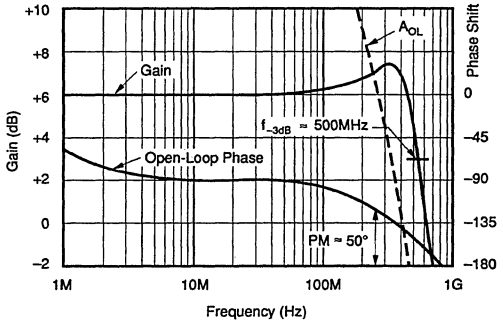
TYPICAL PERFORMANCE CURVES

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

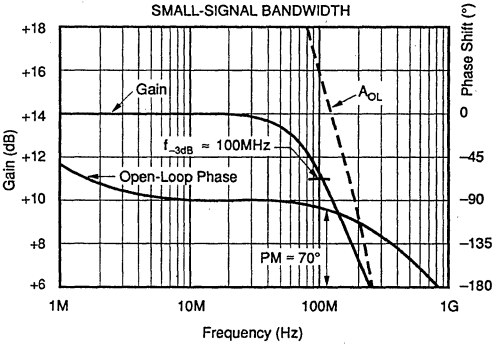
OPEN-LOOP FREQUENCY RESPONSE



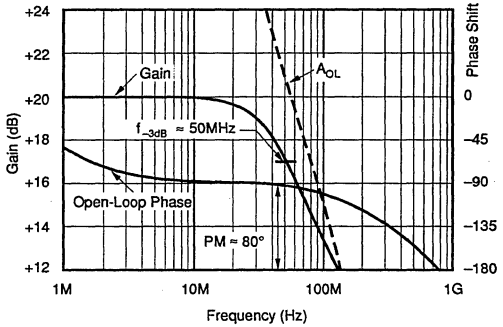
A_V = +2V/V CLOSED-LOOP SMALL-SIGNAL BANDWIDTH



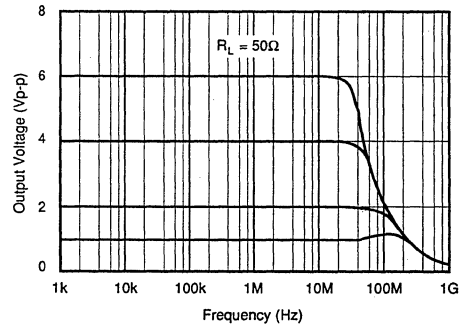
A_V = +5V/V CLOSED-LOOP SMALL-SIGNAL BANDWIDTH



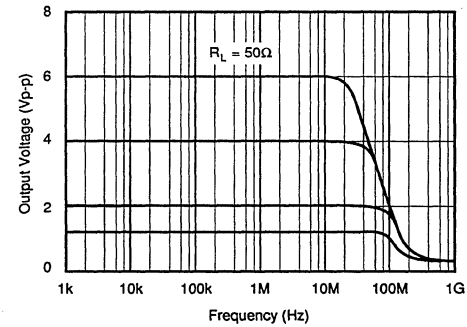
A_V = +10V/V CLOSED-LOOP SMALL-SIGNAL BANDWIDTH



A_V = +2V/V CLOSED-LOOP BANDWIDTH vs OUTPUT VOLTAGE SWING



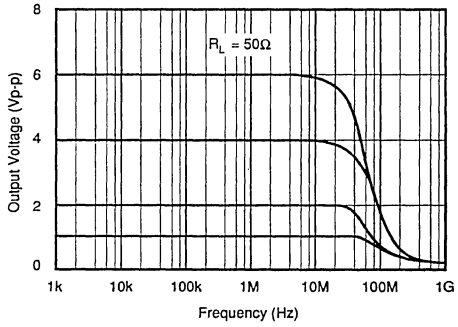
A_V = +5V/V CLOSED-LOOP BANDWIDTH vs OUTPUT VOLTAGE SWING



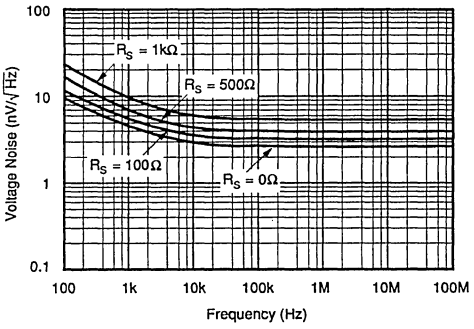
TYPICAL PERFORMANCE CURVES (CONT)

At V_{cc} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

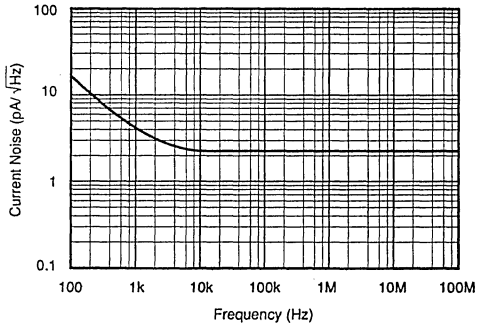
A_V = +10V/V CLOSED-LOOP BANDWIDTH vs OUTPUT VOLTAGE SWING



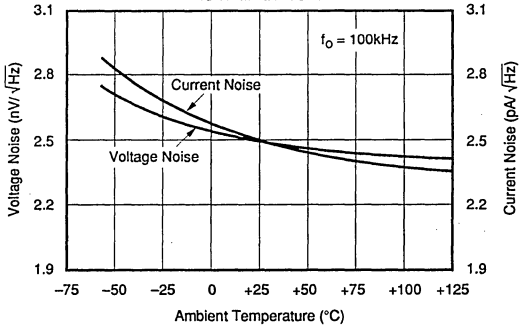
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY vs SOURCE RESISTANCE



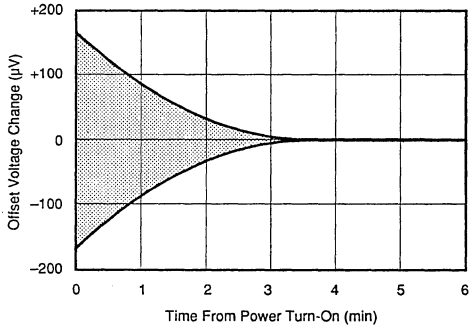
INPUT CURRENT NOISE SPECTRAL DENSITY



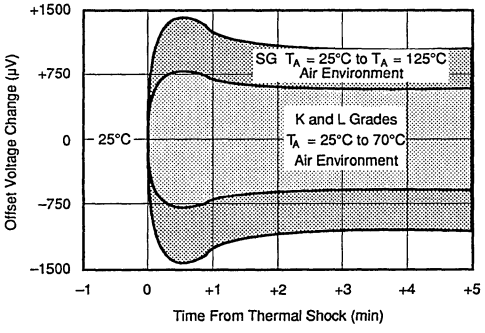
VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs TEMPERATURE



INPUT OFFSET VOLTAGE WARM-UP DRIFT



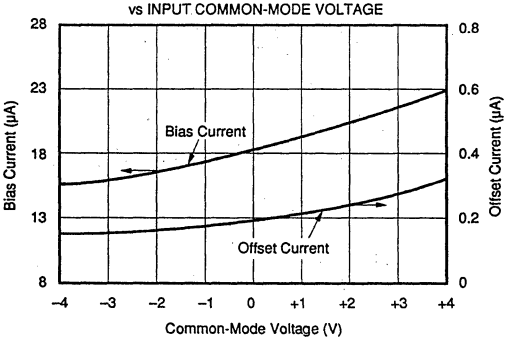
INPUT OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



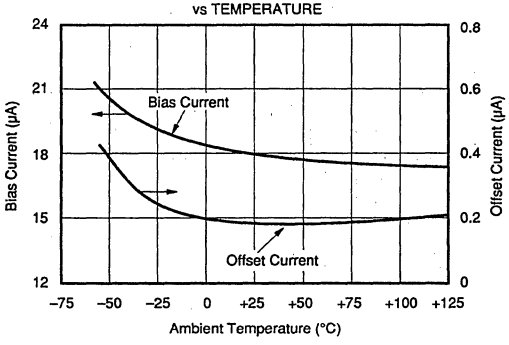
TYPICAL PERFORMANCE CURVES (CONT)

At V_{cc} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

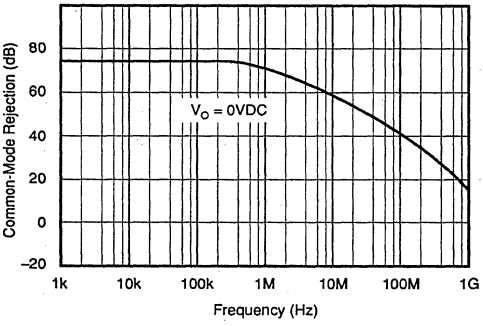
BIAS AND OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



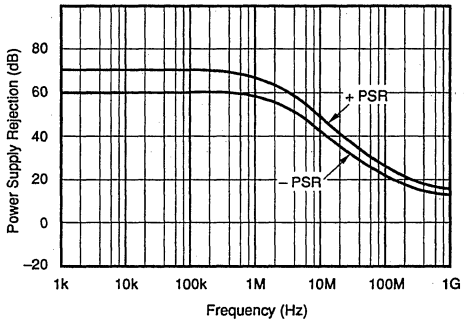
BIAS AND OFFSET CURRENT vs TEMPERATURE



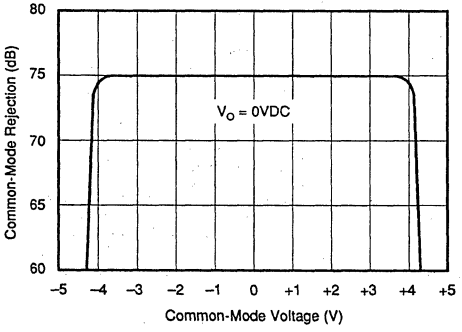
COMMON-MODE REJECTION vs FREQUENCY



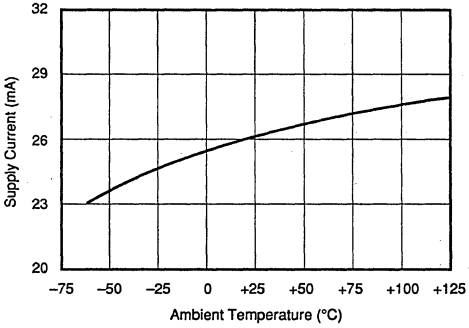
POWER SUPPLY REJECTION vs FREQUENCY



COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



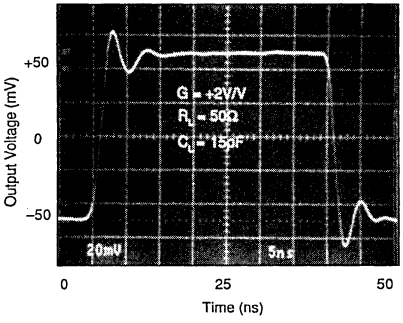
SUPPLY CURRENT vs TEMPERATURE



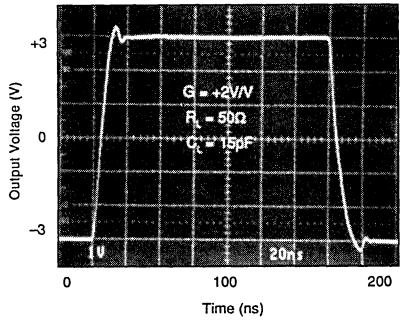
TYPICAL PERFORMANCE CURVES (CONT)

At V_{cc} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

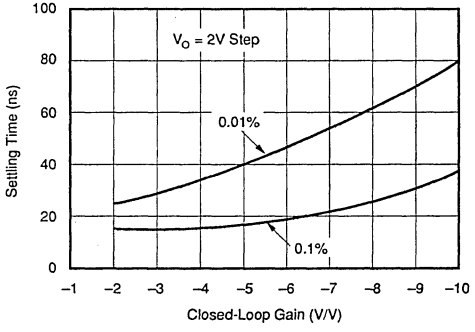
SMALL-SIGNAL TRANSIENT RESPONSE



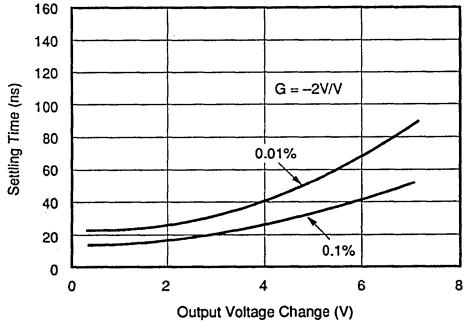
LARGE-SIGNAL TRANSIENT RESPONSE



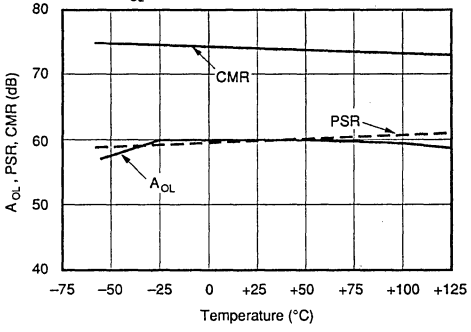
SETTLING TIME vs CLOSED-LOOP GAIN



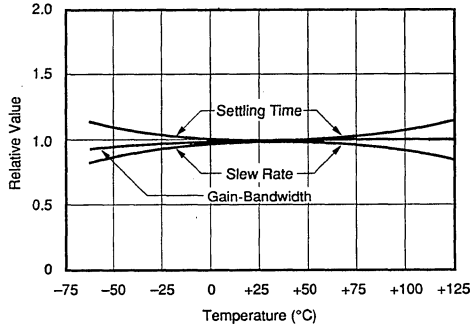
SETTLING TIME vs OUTPUT VOLTAGE CHANGE



A_{OL}, PSR, AND CMR vs TEMPERATURE



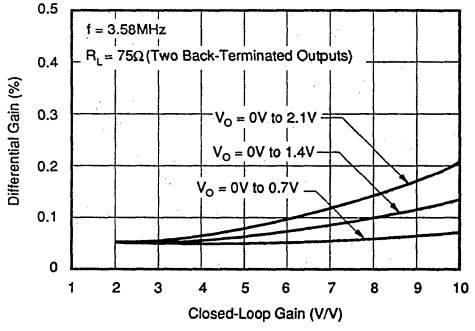
FREQUENCY CHARACTERISTICS vs TEMPERATURE



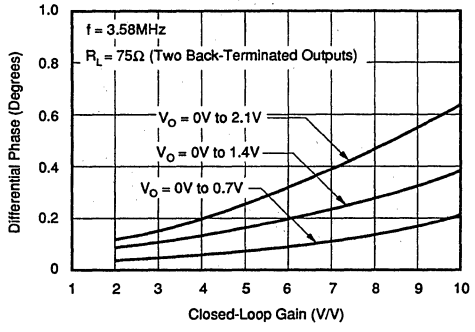
TYPICAL PERFORMANCE CURVES (CONT)

At V_{cc} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

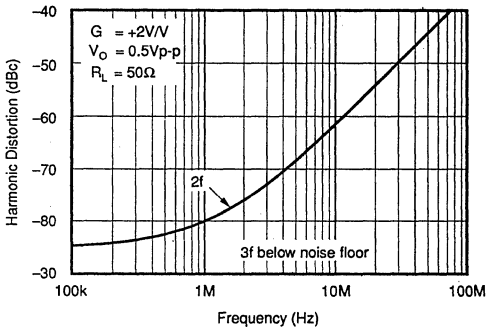
NTSC DIFFERENTIAL GAIN vs CLOSED-LOOP GAIN



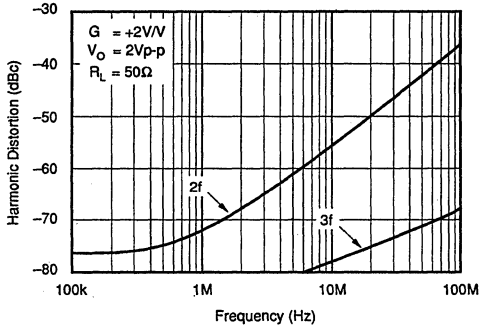
NTSC DIFFERENTIAL PHASE vs CLOSED-LOOP GAIN



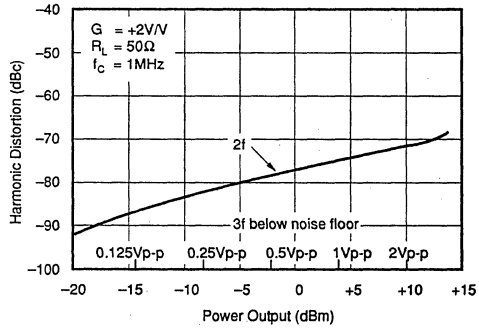
SMALL-SIGNAL
HARMONIC DISTORTION vs FREQUENCY



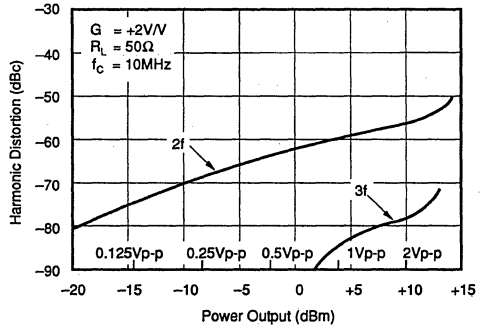
LARGE-SIGNAL
HARMONIC DISTORTION vs FREQUENCY



1MHz HARMONIC DISTORTION
vs POWER OUTPUT



10MHz HARMONIC DISTORTION
vs POWER OUTPUT



APPLICATIONS INFORMATION

DISCUSSION OF PERFORMANCE

The OPA621 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA621's design uses a "Classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer many disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e. one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Bias current cancellation through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 microseconds even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA621's "Classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA621. The use of low-drift thin-film resistors allows internal operating currents to be laser-trimmed at wafer-level to optimize AC performance such as bandwidth and settling time, as well as DC parameters such as input offset voltage and drift. The result is a wideband, high-frequency monolithic operational amplifier with a gain-bandwidth product of 500MHz, a 0.01% settling time of 25ns, and an input offset voltage of 100µV.

WIRING PRECAUTIONS

Maximizing the OPA621's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA621, as it is with all high-frequency circuits. Oscillations at frequencies of 500MHz and above can easily occur if good grounding techniques are not used. A heavy ground plane (2oz copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must always be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (1µF to 10µF) with very short leads are recommended. Although not required, a parallel 0.01µF ceramic may be added if desired. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

2) Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

3) Whenever possible, solder the OPA621 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations. If sockets must be used, consider using zero-profile solderless sockets such as Augat part number 8134-HC-5P2. Alternately, Teflon® standoffs located close to the amplifier's pins can be used to mount feedback components.

4) Resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1kΩ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely unacceptable in high-frequency circuits.

5) Surface mount components (chip resistors, capacitors, etc) have low lead inductance and are therefore strongly recommended. Circuits using all surface mount components with the OPA621KU (SOIC package) will offer the best AC performance. The parasitic package inductance and capaci-

Teflon® E. I. Du Pont de Nemours & Co.

tance for the SOIC is lower than the both the Cerdip and 8-lead Plastic DIP.

6) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

7) Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, use of ±15V supplies will destroy the part.

8) Standard commercial test equipment has not been designed to test devices in the OPA621's speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

9) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

10) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

OFFSET VOLTAGE ADJUSTMENT

The OPA621's input offset voltage is laser-trimmed and will require no further adjustment for most applications. However, if additional adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R3. This will reduce input bias current errors to the amplifier's offset current, which is typically only 0.2µA.

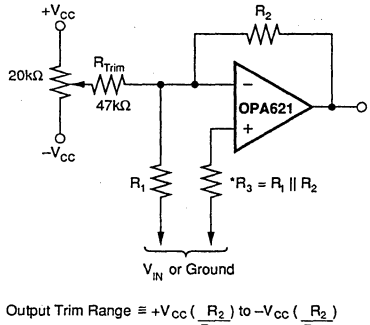


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA621 incorporates on-chip ESD protection diodes as shown in Figure 2. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

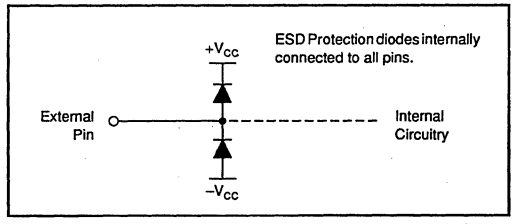


FIGURE 2. Internal ESD Protection.

All pins on the OPA621 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

The internal protection diodes are designed to withstand 2.5kV (using Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA621.

OUTPUT DRIVE CAPABILITY

The OPA621's design uses large output devices and has been optimized to drive 50Ω and 75Ω resistive loads. The device can easily drive 6Vp-p into a 50Ω load. This high-output drive capability makes the OPA621 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Internal current-limiting circuitry limits output current to about 150mA at 25°C. This prevents destruction from accidental shorts to common and eliminates the need for external current-limiting circuitry. Although the device can withstand momentary shorts to either power supply, it is not recommended.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the

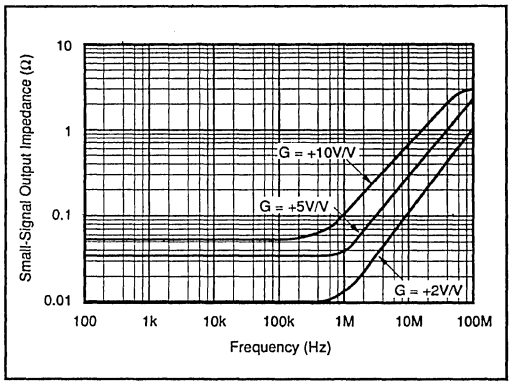


FIGURE 3. Small-Signal Output Impedance vs Frequency.

OPA621 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

THERMAL CONSIDERATIONS

The OPA621 does not require a heat sink for operation in most environments. The use of a heat sink, however, will

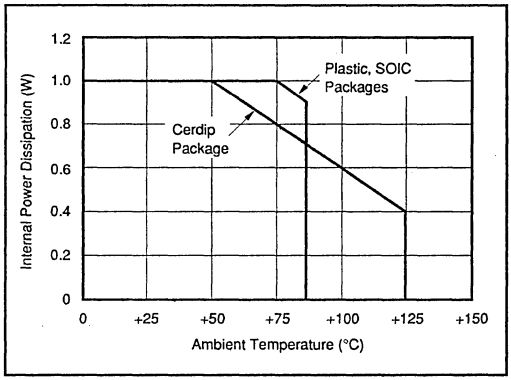


FIGURE 4. Maximum Power Dissipation.

reduce the internal thermal rise and will result in cooler, more reliable operation. At extreme temperatures and under full load conditions a heat sink is necessary. See "Maximum Power Dissipation" curve, Figure 4.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 28mA = 280mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC}/2$, and is equal to P_{DL}, max = $(\pm V_{CC})^2/4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

When the output is shorted to common $P_{DL} = 5V \times 150mA = 750mW$. Thus, $P_D = 280mW + 750mW \cong 1W$. Note that the short-circuit condition represents the maximum amount of internal power dissipation that can be generated. Thus, the "Maximum Power Dissipation" curve starts at 1W and is derated based on a 175°C maximum junction temperature

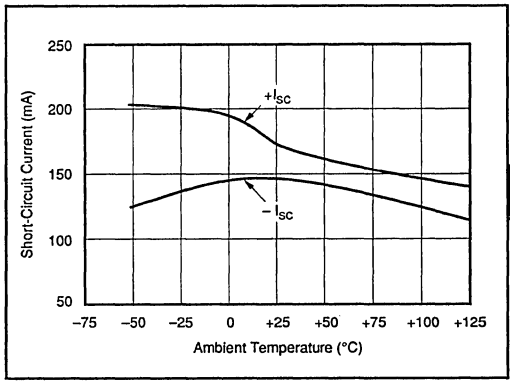


FIGURE 5. Short-Circuit Current vs Temperature.

and the junction-to-ambient thermal resistance, θ_{JA}, of each package. The variation of short-circuit current with temperature is shown in Figure 5.

CAPACITIVE LOADS

The OPA621's output stage has been optimized to drive resistive loads as low as 50Ω. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 15pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 6. This is particularly important when driving high capacitance loads such as flash A/D converters.

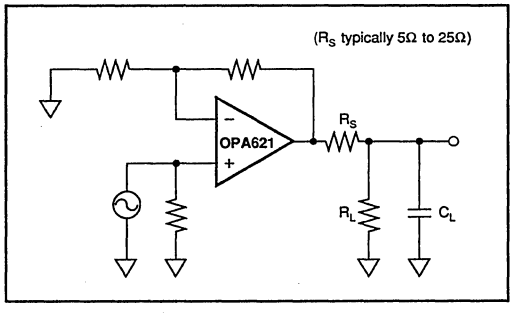


FIGURE 6. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA621 is stable in inverting gains of ≥–2V/V and in non-inverting gains ≥+2V/V. Phase margin for both configurations is approximately 50°. Inverting and non-inverting gains of unity should be avoided. The minimum stable gains of +2V/V and –2V/V are the most demanding circuit configurations for loop stability and oscillations are most likely to occur in these gains. If possible, use the device in a noise gain greater than three to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of –2V/V is equivalent to a noise gain of 3.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA621 in a good layout is flat with frequency for higher-gain circuits. However, low-gain circuits and configurations where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of ±200µV centered around the final value of 2V.

Settling time, specified in an inverting gain of two, occurs in only 25ns to 0.01% for a 2V step, making the OPA621 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Wiring Precautions." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 30ns.

In practice, settling time measurements on the OPA621 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

Figure 7 shows the test circuit used to measure settling time for the OPA621. This approach uses a 16-bit sampling oscilloscope to monitor the input and output pulses. These waveforms are captured by the sampling scope, averaged, and then subtracted from each other in software to produce the error signal. This technique eliminates the need for the traditional "false-summing junction," which adds extra parasitic capacitance. Note that instead of an additional flat-top generator, this technique uses the scope's built-in calibration source as the input signal.

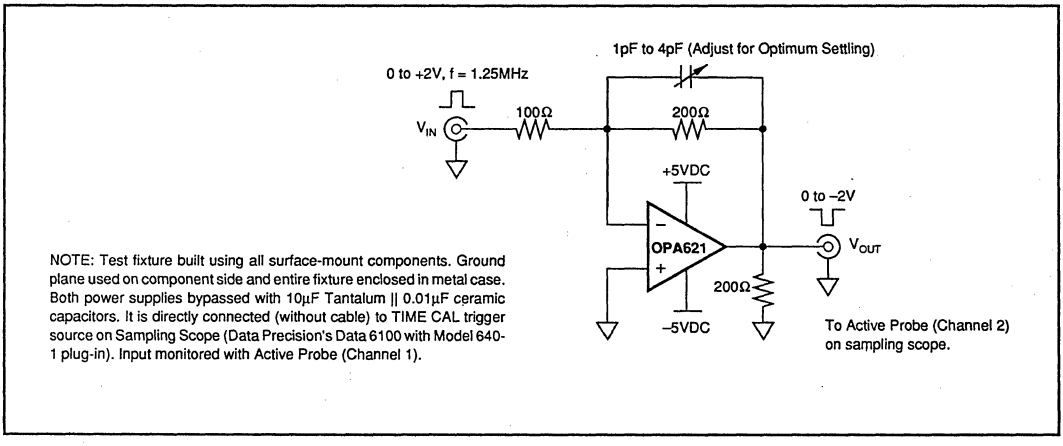


FIGURE 7. Settling Time Test Circuit.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase with closed-loop gain and output voltage transition as shown in the Typical Performance Curves. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

DISTORTION

The OPA621's Harmonic Distortion characteristics into a 50Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 8. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

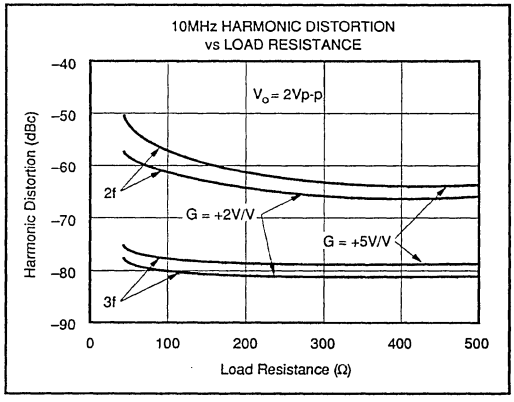


FIGURE 8. 10MHz Harmonic Distortion vs Load Resistance.

Two-tone, third-order intermodulation distortion (IM) is an important parameter for many RF amplifier applications. Figure 9 shows the OPA621's two-tone, third-order IM intercept vs frequency. For these measurements, tones were spaced 1MHz apart. This curve is particularly useful for determining the magnitude of the third-order IM products as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA621 to operate in a gain of +2V/V and drive 2Vp-p into 50Ω at a frequency of 10MHz. Referring to Figure 9 we find that the intercept point is +47dBm. The magnitude of the third-order IM products can now be easily calculated from the expression:

$$\text{Third IMD} = 2(\text{OPI}^3\text{P} - P_O)$$

where OPI^3P = third-order output intercept, dBm
P_O = output level/tone, dBm/tone
Third IMD = third-order intermodulation ratio below each output tone, dB

For this case OPI^3P = 47dBm, P_O = 10dBm, and the third-order IMD = 2(47 – 10) = 74dB below either 10dBm tone. The OPA621's low IMD makes the device an excellent choice for a variety of RF signal processing applications.

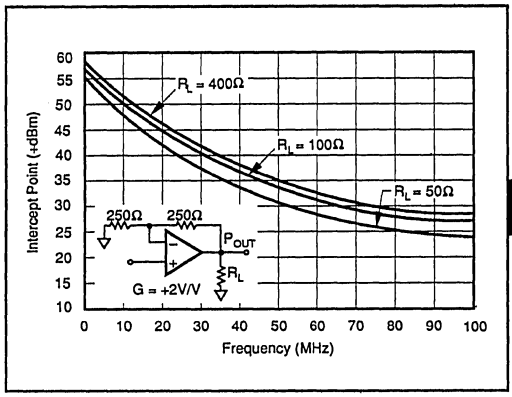


FIGURE 9. 2-Tone, 3rd Order Intermodulation Intercept vs Frequency.

NOISE FIGURE

The OPA621's voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA621's Noise Figure vs Source Resistance is shown in Figure 10.

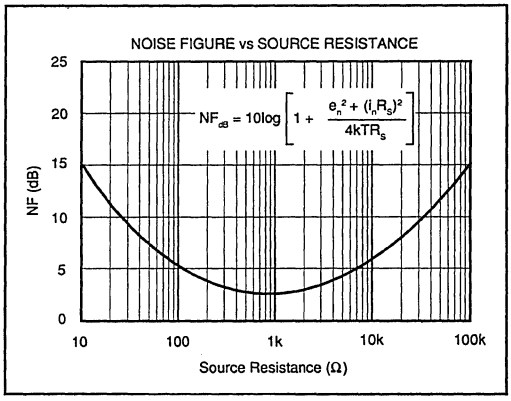


FIGURE 10. Noise Figure vs Source Resistance.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models using MicroSim Corporation's PSpice are available for the OPA621. Request Burr-Brown Application Note AN-167.

RELIABILITY DATA

Extensive reliability testing has been performed on the OPA621. Accelerated life testing (2000 hours) at maximum operating temperature was used to calculate MTTF at an ambient temperature of 25°C. These test results yield MTTF of: Cerdip package = 1.31E+9 Hours, Plastic DIP = 5.02E+7 Hours, and SOIC = 2.94E+7 Hours. Additional tests such as PCT have also been performed. Reliability reports are available upon request for each of the package options offered.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Request DEM1135 for 8-Pin DIP, and DEM1136 for SOIC package.

APPLICATIONS

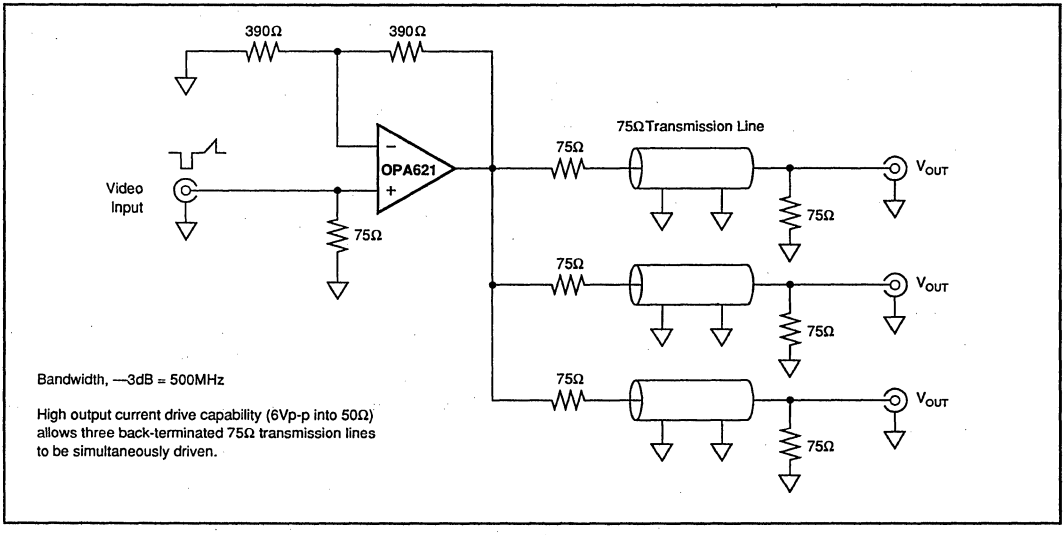


FIGURE 11. Video Distribution Amplifier.

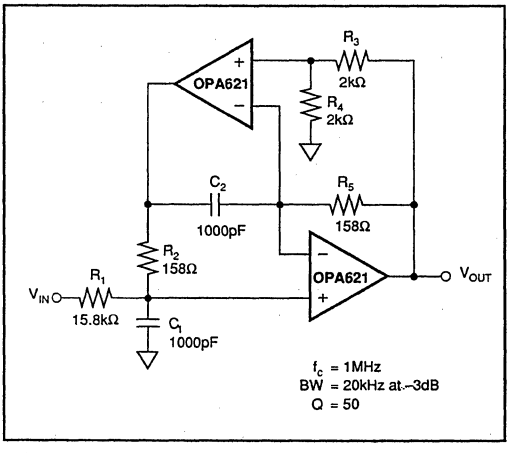


FIGURE 12. High-Q 1MHz Bandpass Filter

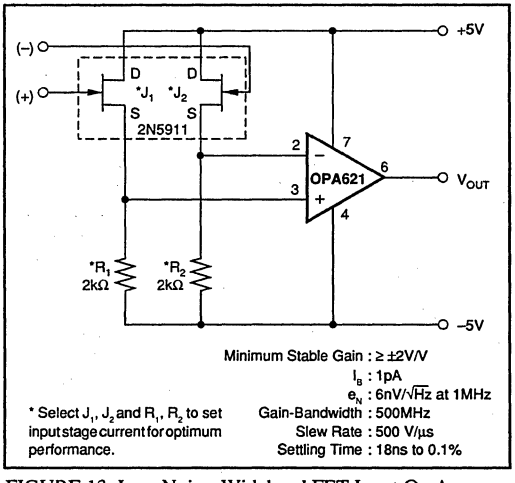


FIGURE 13. Low Noise, Wideband FET Input Op Amp.

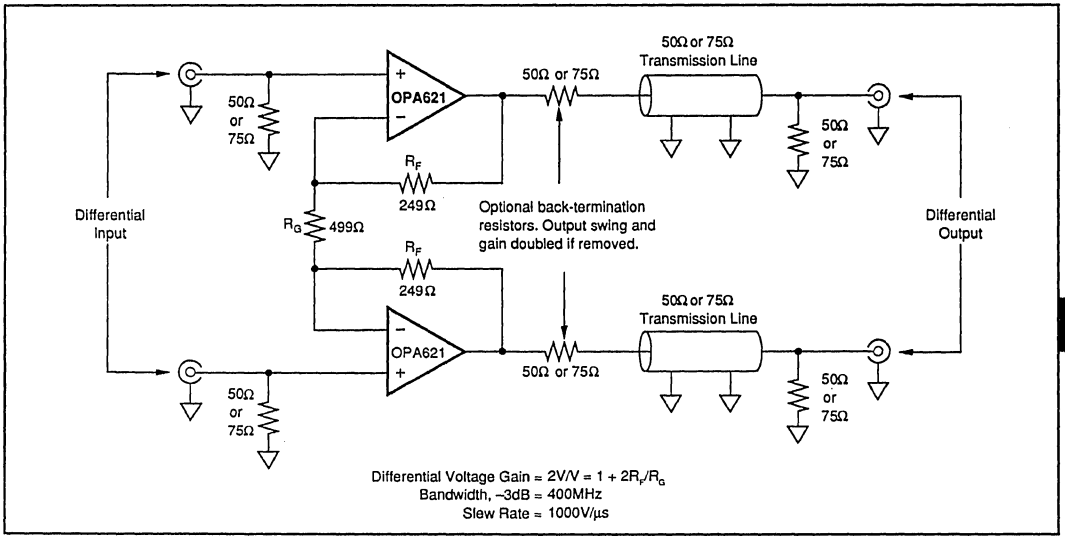


FIGURE 14. Differential Line Driver for 50Ω or 75Ω Systems.

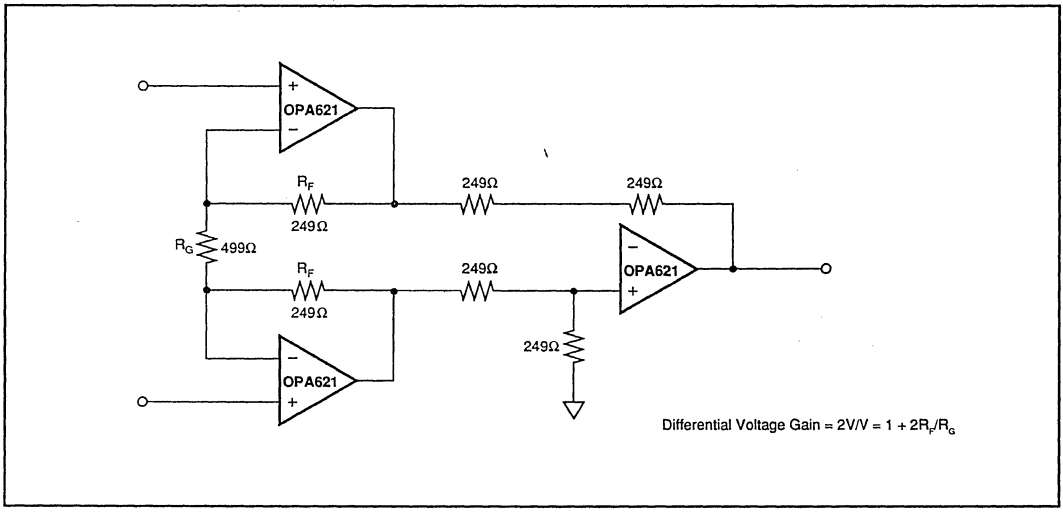


FIGURE 15. Wideband, Fast-Settling Instrumentation Amplifier.

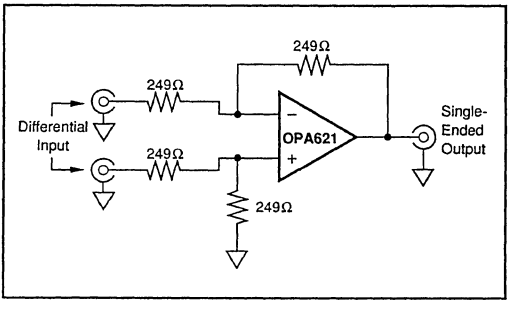


FIGURE 16. Unity Gain Difference Amplifier.

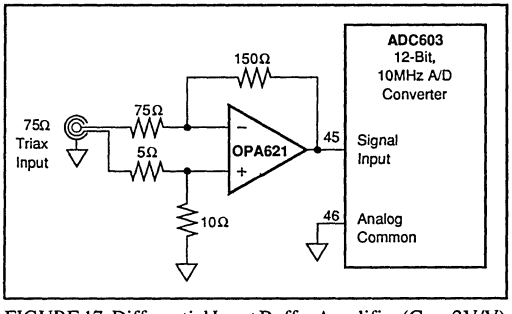


FIGURE 17. Differential Input Buffer Amplifier (G = –2V/V).

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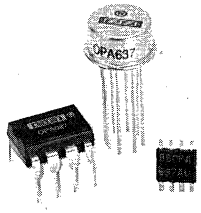


OPA627
OPA637

Precision High-Speed *Difet*® OPERATIONAL AMPLIFIERS

FEATURES

- VERY LOW NOISE: 4.5nV/√Hz at 10kHz
- FAST SETTLING TIME:
  OPA627—550ns to 0.01%
  OPA637—450ns to 0.01%
- LOW V_{OS}: 100μV max
- LOW DRIFT: 0.8μV/°C max
- LOW I_B: 5pA max
- OPA627: Unity-Gain Stable
- OPA637: STABLE IN GAIN ≥5

APPLICATIONS

- PRECISION INSTRUMENTATION
- FAST DATA ACQUISITION
- DAC OUTPUT AMPLIFIER
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- HIGH-IMPEDANCE SENSOR AMPS
- HIGH-PERFORMANCE AUDIO CIRCUITRY
- ACTIVE FILTERS

DESCRIPTION

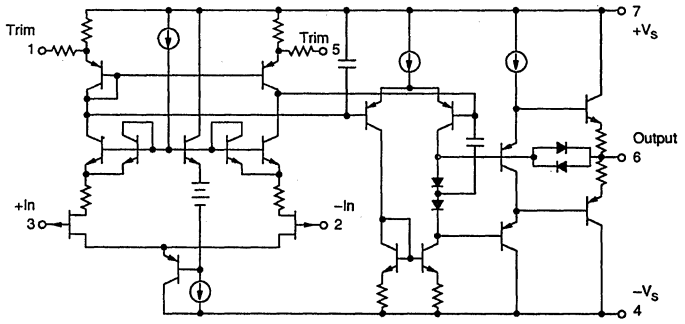
The OPA627 and OPA637 ***Difet*** operational amplifiers provide a new level of performance in a precision FET op amp. When compared to the popular OPA111 op amp, the OPA627/637 has lower noise, lower offset voltage, and much higher speed. It is useful in a broad range of precision and high speed analog circuitry.

The OPA627/637 is fabricated on a high-speed, dielectrically-isolated complementary NPN/PNP process. It operates over a wide range of power supply voltage—±4.5V to ±18V. Laser-trimmed ***Difet*** input circuitry provides high accuracy and low-noise performance comparable with the best bipolar-input op amps.

High frequency complementary transistors allow increased circuit bandwidth, attaining dynamic performance not possible with previous precision FET op amps. The OPA627 is unity-gain stable. The OPA637 is stable in gains equal to or greater than five.

Difet fabrication achieves extremely low input bias currents without compromising input voltage noise performance. Low input bias current is maintained over a wide input common-mode voltage range with unique cascode circuitry.

The OPA627/637 is available in plastic DIP, SOIC and metal TO-99 packages. Industrial and military temperature range models are available.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-998B

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_S = ±15V unless otherwise noted.

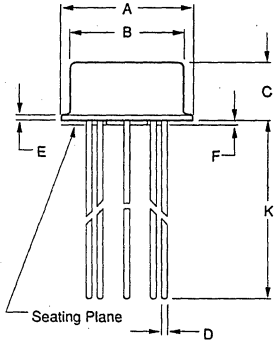
PARAMETER	CONDITIONS	OPA627BM/BP/SM OPA637BM/BP/SM			OPA627AM/AP/AU OPA637AM/AP/AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE [1]								
Input Offset Voltage			40	100		130	250	µV
AP, BP, AU Grades			100	250		280	500	µV
Average Drift			0.4	0.8		1.2	2	µV/°C
AP, BP, AU Grades			0.8	2		2.5		µV/°C
Power Supply Rejection	V_S = ±4.5 to ±18V	106	120		100	116		dB
INPUT BIAS CURRENT [2]								
Input Bias Current	V_{CM} = 0V		1	5		2	10	pA
Over Specified Temperature	V_{CM} = 0V			1			2	nA
SM Grade	V_{CM} = 0V			50				nA
Over Common-Mode Voltage	V_{CM} = ±10V		1			2		pA
Input Offset Current	V_{CM} = 0V		0.5	5		1	10	pA
Over Specified Temperature	V_{CM} = 0V			1			2	nA
SM Grade				50				nA
NOISE								
Input Voltage Noise								
Noise Density: f = 10Hz			15	40		20		nV/√Hz
f = 100Hz			8	20		10		nV/√Hz
f = 1kHz			5.2	8		5.6		nV/√Hz
f = 10kHz			4.5	6		4.8		nV/√Hz
Voltage Noise, BW = 0.1 to 10Hz			0.6	1.6		0.8		µVp-p
Input Bias Current Noise								
Noise Density, f = 1kHz			1.6	2.5		2.5		fA/√Hz
Current Noise, BW = 0.1 to 10Hz			30	60		48		fAp-p
INPUT IMPEDANCE								
Differential			10^{13} || 8			*		Ω || pF
Common-Mode			10^{13} || 7			*		Ω || pF
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±11	±11.5		*	*		V
Over Specified Temperature		±10.5	±11		*	*		V
Common-Mode Rejection	V_{CM} = ±10.5V	106	116		100	110		dB
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = ±10V, R_L = 1kΩ	112	120		106	116		dB
Over Specified Temperature	V_O = ±10V, R_L = 1kΩ	106	117		100	110		dB
SM Grade	V_O = ±10V, R_L - 1kΩ	100	114					dB
FREQUENCY RESPONSE								
Slew Rate: OPA627	G = –1, 10V Step	40	55		*	*		V/µs
OPA637	G = –4, 10V Step	100	135		*	*		V/µs
Settling Time: OPA627 0.01%	G = –1, 10V Step		550			*		ns
0.1%	G = –1, 10V Step		450			*		ns
OPA637 0.01%	G = –4, 10V Step		450			*		ns
0.1%	G = –4, 10V Step		300			*		ns
Gain-Bandwidth Product: OPA627	G = 1		16			*		MHz
OPA637	G = 10		80			*		MHz
Total Harmonic Distortion + Noise	G = +1, f = 1kHz		0.00003			*		%
POWER SUPPLY								
Specified Operating Voltage			±15			*		V
Operating Voltage Range		±4.5		±18	*		*	V
Current			±7	±7.5		*	*	mA
OUTPUT								
Voltage Output	R_L = 1kΩ	±11.5	±12.3		*	*		
Over Specified Temperature		±11	±11.5		*	*		V
Current Output	V_O = ±10V		±45			*		mA
Short Circuit Current		±35	+70/–55	±100	*	*	*	mA
Output Impedance, Open-Loop	1MHz		55			*		Ω
TEMPERATURE RANGE								
Specification: AP, BP, AM, BM, AU		–25		+85	*		*	°C
SM		–55		+125				°C
Storage: AM, BM, SM		–60		+150	*		*	°C
AP, BP, AU		–40		+125	*		*	°C
θ_{J-A}: AM, BM, SM			200			*		°C/W
AP, BP, AU			100			*		°C/W

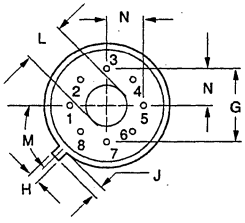
* Specifications same as OPA627B grade.

NOTES: (1) Offset voltage measured fully warmed-up. (2) High-speed test at T_J = 25°C. See Typical Performance Curves for warmed-up performance.

MECHANICAL

M Package — Metal TO-99

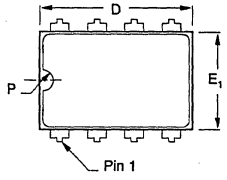


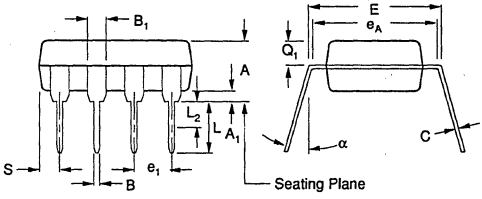


	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

P Package — 8-Pin Plastic DIP





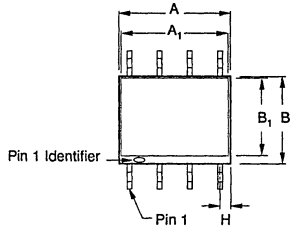
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.155	.200	3.94	5.08
A1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D(1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

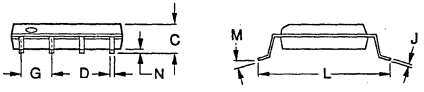
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
L2(2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q1	.040	.075	1.02	1.91
S(1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e1 and e_A applies in zone L_2 when unit installed.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

U Package — 8-Pin SOIC

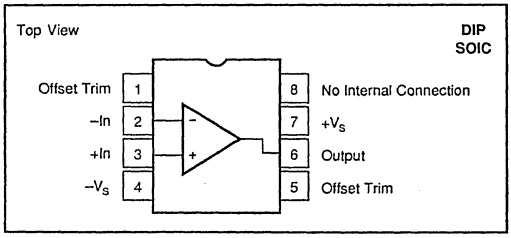


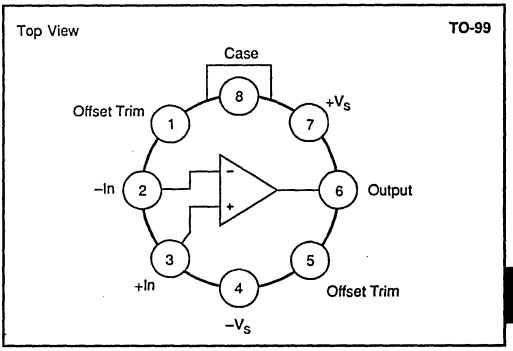


	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.185	.201	4.70	5.11
A1	.178	.201	4.52	5.11
B	.146	.162	3.71	4.11
B1	.130	.149	3.30	3.78
C	.054	.145	1.37	3.69
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.018	.026	0.46	0.66
J	.008	.012	0.20	0.30
L	.220	.252	5.59	6.40
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

PIN CONFIGURATIONS





ORDERING INFORMATION

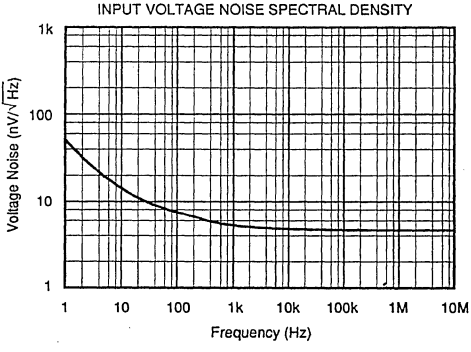
MODEL	PACKAGE	TEMPERATURE RANGE
OPA627AP	Plastic DIP	–25°C to +85°C
OPA627BP	Plastic DIP	–25°C to +85°C
OPA627AU	SOIC	–25°C to +85°C
OPA627AM	TO-99 Metal	–25°C to +85°C
OPA627BM	TO-99 Metal	–25°C to +85°C
OPA627SM	TO-99 Metal	–55°C to +125°C
OPA637AP	Plastic DIP	–25°C to +85°C
OPA637BP	Plastic DIP	–25°C to +85°C
OPA637AU	SOIC	–25°C to +85°C
OPA637AM	TO-99 Metal	–25°C to +85°C
OPA637BM	TO-99 Metal	–25°C to +85°C
OPA637SM	TO-99 Metal	–55°C to +125°C

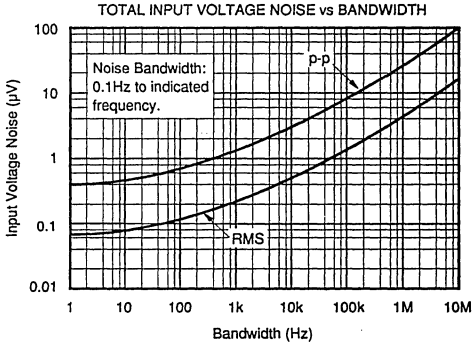
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	$+V_S$ + 2V to $-V_S$ – 2V
Differential Input Range	Total V_S + 4V
Power Dissipation	1000mW
Operating Temperature	
M Package	–65°C to +150°C
P, U Package	–40°C to +125°C
Storage Temperature	
M Package	–65°C to +150°C
P, U Package	–40°C to +125°C
Junction Temperature	
M Package	+175°C
P, U Package	+125°C
Lead Temperature (soldering, 10s)	+300°C

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

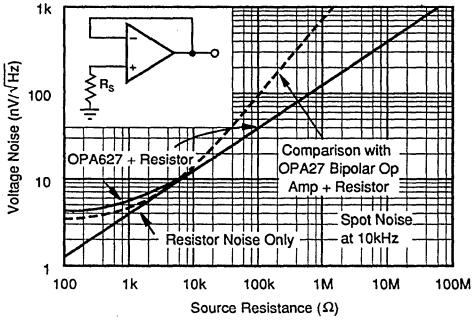




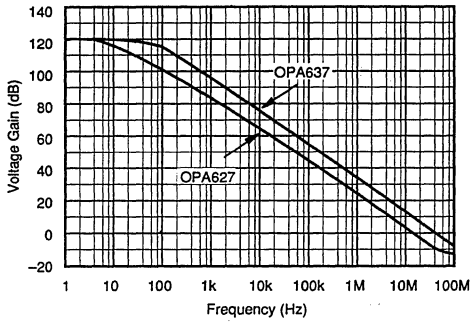
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

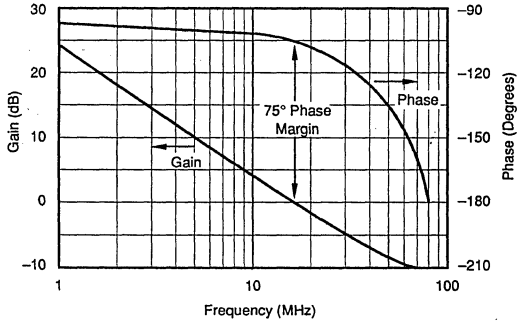
VOLTAGE NOISE vs SOURCE RESISTANCE



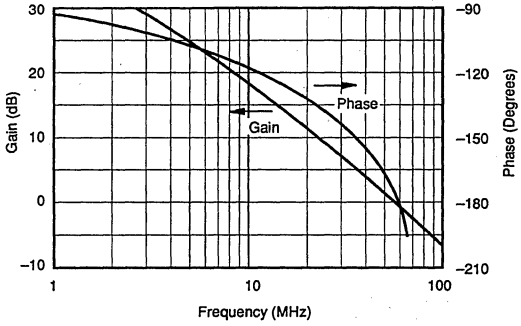
OPEN LOOP GAIN vs FREQUENCY



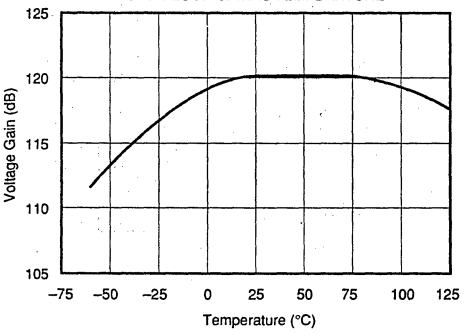
OPA627 GAIN/PHASE vs FREQUENCY



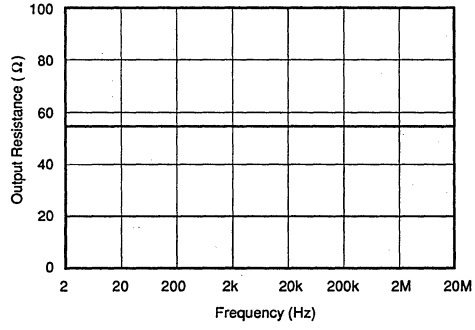
OPA637 GAIN/PHASE vs FREQUENCY



OPEN-LOOP GAIN vs TEMPERATURE



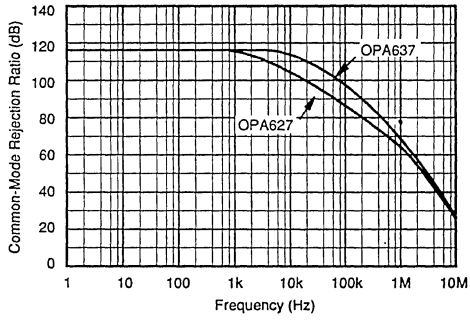
OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY



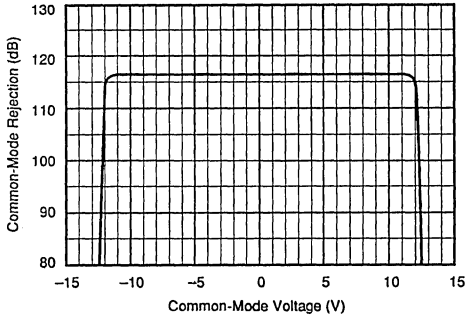
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

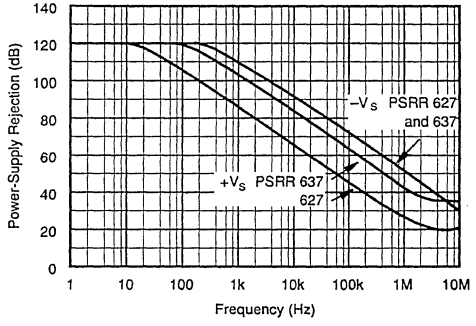
COMMON-MODE REJECTION vs FREQUENCY



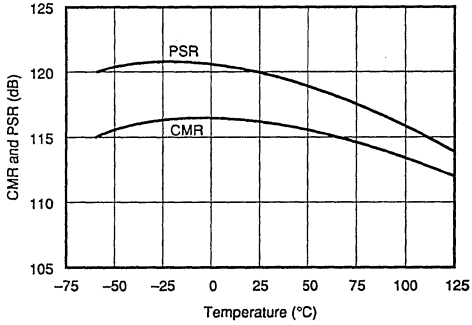
COMMON-MODE REJECTION vs INPUT COMMON MODE VOLTAGE



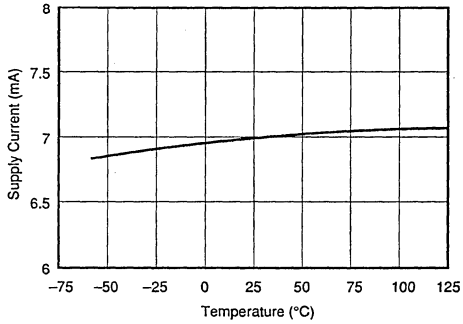
POWER-SUPPLY REJECTION vs FREQUENCY



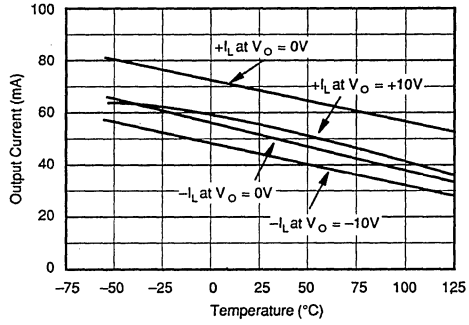
POWER-SUPPLY REJECTION AND COMMON-MODE REJECTION vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE



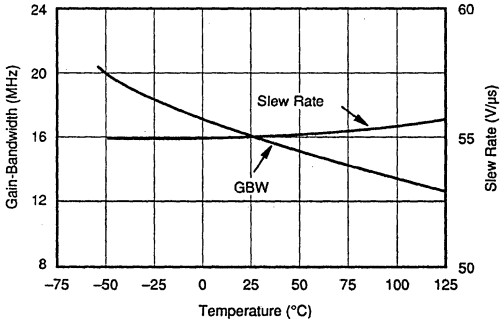
OUTPUT CURRENT LIMIT vs TEMPERATURE



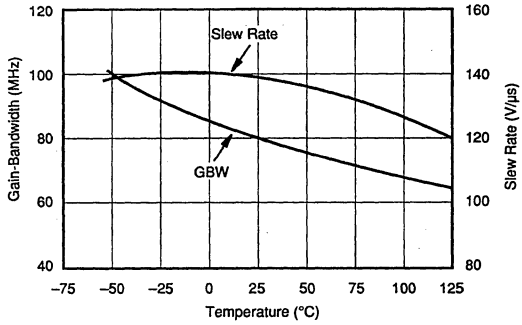
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

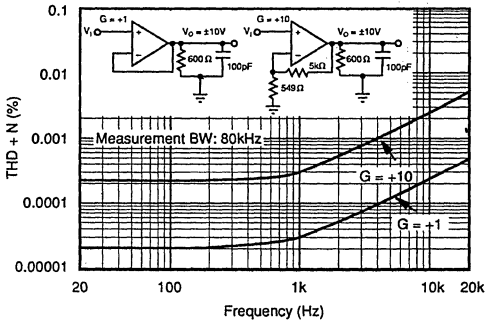
OPA627 GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



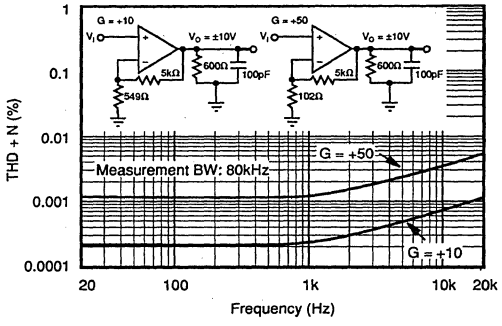
OPA637 GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



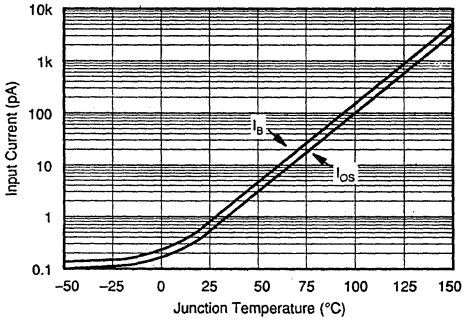
OPA627 TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



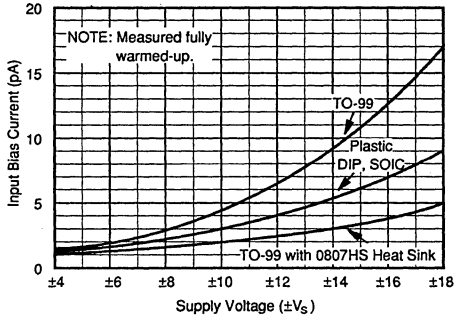
OPA637 TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



INPUT BIAS AND OFFSET CURRENT vs JUNCTION TEMPERATURE



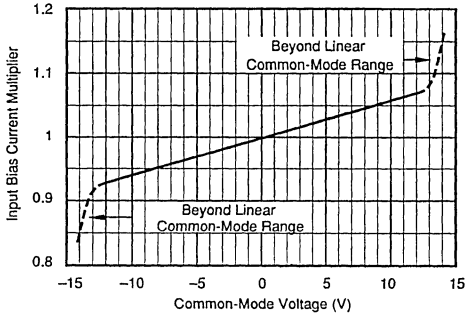
INPUT BIAS CURRENT vs POWER SUPPLY VOLTAGE



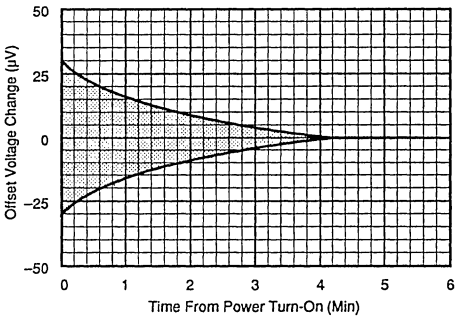
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

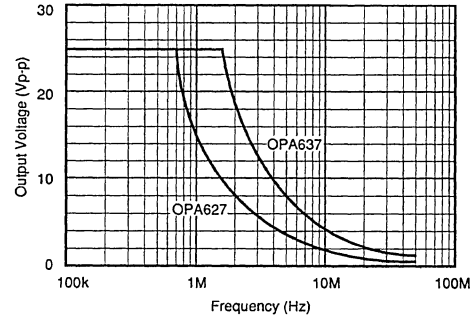
INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



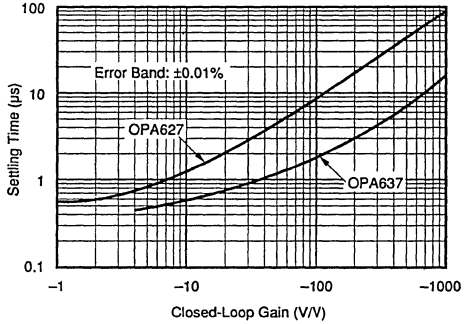
INPUT OFFSET VOLTAGE WARM-UP vs TIME



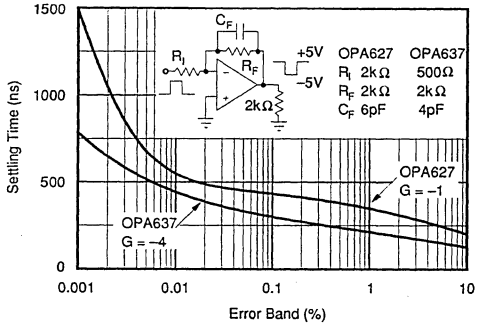
MAX OUTPUT VOLTAGE vs FREQUENCY



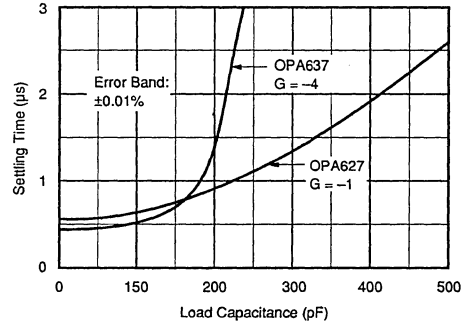
SETTLING TIME vs CLOSED-LOOP GAIN



SETTLING TIME vs ERROR BAND



SETTLING TIME vs LOAD CAPACITANCE



APPLICATIONS INFORMATION

The OPA627 is unity-gain stable. The OPA637 may be used to achieve higher speed and bandwidth in circuits with noise gain greater than five. Noise gain refers to the closed-loop gain of a circuit as if the non-inverting op amp input were being driven. For example, the OPA637 may be used in a non-inverting amplifier with gain greater than five, or an inverting amplifier of gain greater than four.

When choosing between the OPA627 or OPA637, it is important to consider the high frequency noise gain of your circuit configuration. Circuits with a feedback capacitor (Figure 1) place the op amp in unity noise-gain at high frequency. These applications must use the OPA627 for proper stability. An exception is the circuit in Figure 2, where a small feedback capacitance is used to compensate for the input capacitance at the op amp's inverting input. In this case, the closed-loop noise gain remains constant with frequency, so if the closed-loop gain is equal to five or greater, the OPA637 may be used.

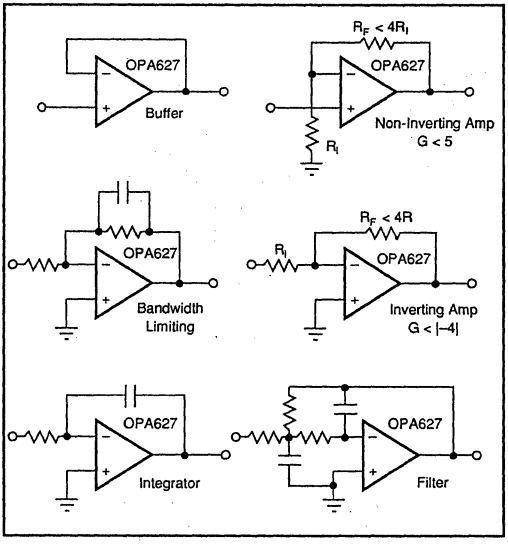


FIGURE 1. Circuits with Noise Gain Less than Five Require the OPA627 for Proper Stability.

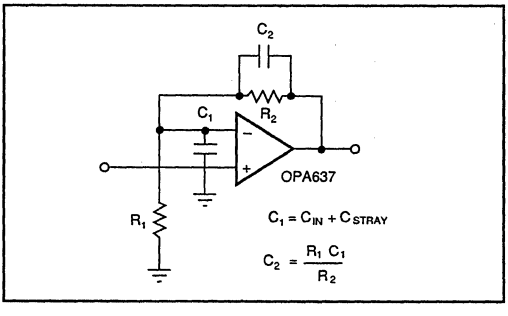


FIGURE 2. Circuits with Noise Gain Equal to or Greater than Five May Use the OPA637.

OFFSET VOLTAGE ADJUSTMENT

The OPA627/637 is laser-trimmed for low offset voltage and drift, so many circuits will not require external adjustment. Figure 3 shows the optional connection of an external potentiometer to adjust offset voltage. This adjustment should not be used to compensate for offsets created elsewhere in a system (such as in later amplification stages or in an A/D converter) because this could introduce excessive temperature drift.

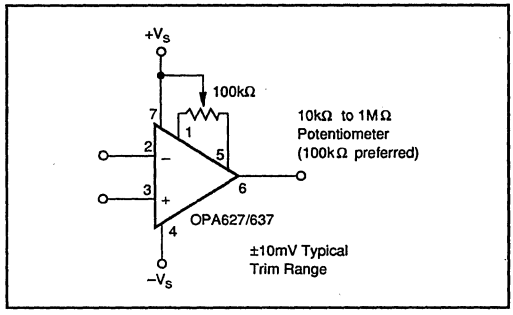


FIGURE 3. Optional Offset Voltage Trim Circuit.

NOISE PERFORMANCE

Some bipolar op amps may provide lower voltage noise performance, but both voltage noise and bias current noise contribute to the total noise of a system. The OPA627/637 is unique in providing very low voltage noise and very low current noise. This provides optimum noise performance over a wide range of sources, including reactive source impedances. This can be seen in the performance curve showing the noise of a source resistor combined with the noise of an OPA627. Above a 2kΩ source resistance, the op amp contributes little additional noise. Below 1kΩ, op amp noise dominates over the resistor noise, but compares favorably with precision bipolar op amps.

CIRCUIT LAYOUT

As with any high speed, wide bandwidth circuit, careful layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance—especially at the input pins and feedback circuitry.

The case connection (pin 8 of TO-99 metal package only) should be connected to an AC ground for lowest possible pickup of external fields. While DC ground would be the most likely choice, pin 8 could also be connected to either power supply. (The case is not internally connected to the negative power supply as it is with most common op amps.) For lowest possible input bias current, the case may be driven as a guard—see Input Bias Current section. Pin 8 of the plastic DIP and SOIC versions has no internal connection.

Power supply connections should be bypassed with good high frequency capacitors positioned close to the op amp pins. In most cases 0.1µF ceramic capacitors are adequate. The OPA627/637 is capable of high output current (in

excess of 45mA). Applications with low impedance loads or capacitive loads with fast transient signals demand large currents from the power supplies. Larger bypass capacitors such as 1µF solid tantalum capacitors may improve dynamic performance in these applications.

INPUT BIAS CURRENT

Difet fabrication of the OPA627/637 provides very low input bias current. Since the gate current of a FET doubles approximately every 10°C, to achieve lowest input bias current, the die temperature should be kept as low as possible. The high speed and therefore higher quiescent current of the OPA627/637 can lead to higher chip temperature. A simple press-on heat sink such as the Burr-Brown model 807HS (TO-99 metal package) can reduce chip temperature by approximately 15°C, lowering the I_B to one-third its warmed-up value. The 807HS heat sink can also reduce low-frequency voltage noise caused by air currents and thermoelectric effects. See the data sheet on the 807HS for details.

Temperature rise in the plastic DIP and SOIC packages can be minimized by soldering the device to the circuit board. Wide copper traces will also help dissipate heat.

The OPA627/637 may also be operated at reduced power supply voltage to minimize power dissipation and temperature rise. Using ±5V power supplies reduces power dissipation to one-third of that at ±15V. This reduces the I_B of TO-99 metal package devices to approximately one-fourth the value at ±15V.

Leakage currents between printed circuit board traces can easily exceed the input bias current of the OPA627/637. A circuit board "guard" pattern (Figure 4) reduces leakage effects. By surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential, leakage current will flow harmlessly to the low-impedance node. The case connection (TO-99 metal package only) may also be driven at guard potential to minimize any leakage which might occur from the input pins to the case. The case is not internally connected to $-V_S$.

Input bias current may also be degraded by improper handling or cleaning. Contamination from handling parts and circuit boards may be removed with cleaning solvents and deionized water. Each rinsing operation should be followed by a 30-minute bake at 85°C.

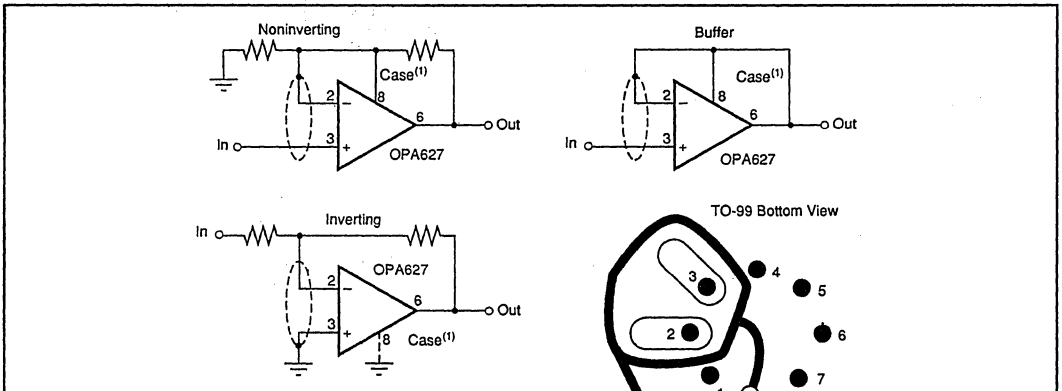
Many FET-input op amps exhibit large changes in input bias current with changes in input voltage. Input stage cascode circuitry makes the input bias current of the OPA627/637 virtually constant with wide common-mode voltage changes. This is ideal for accurate high input-impedance buffer applications.

PHASE-REVERSAL PROTECTION

The OPA627/637 has internal phase-reversal protection. Many FET-input op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This is most often encountered in non-inverting circuits when the input is driven below –12V, causing the output to reverse into the positive rail. The input circuitry of the OPA627/637 does not induce phase reversal with excessive common-mode voltage, so the output limits into the appropriate rail.

OUTPUT OVERLOAD

When the inputs to the OPA627/637 are overdriven, the output voltage of the OPA627/637 smoothly limits at approximately 2.5V from the positive and negative power supplies. If driven to the negative swing limit, recovery takes approximately 500ns. When the output is driven into the positive limit, recovery takes approximately 6µs. Output recovery of the OPA627 can be improved using the output clamp circuit shown in Figure 5. Diodes at the inverting input prevent degradation of input bias current.



Board Layout for Input Guarding:
Guard top and bottom of board.
Alternate—use Teflon® standoff for sensitive input pins.

Teflon® E.I. du Pont de Nemours & Co.

NOTE: (1) Case connected to pin 8 on TO-99 package only—see text.

FIGURE 4. Connection of Input Guard for Lowest I_B.

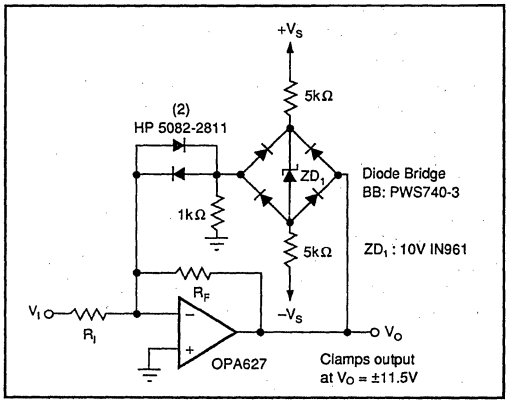


FIGURE 5. Clamp Circuit for Improved Overload Recovery.

CAPACITIVE LOADS

As with any high-speed op amp, best dynamic performance can be achieved by minimizing the capacitive load. Since a load capacitance presents a decreasing impedance at higher frequency, a load capacitance which is easily driven by a slow op amp can cause a high-speed op amp to perform poorly. See the typical curves showing settling times as a function of capacitive load. The lower bandwidth of the OPA627 makes it the better choice for driving large capacitive loads. Figure 6 shows a circuit for driving very large load capacitance. This circuit's two-pole response can also be used to sharply limit system bandwidth. This is often useful in reducing the noise of systems which do not require the full bandwidth of the OPA627.

INPUT PROTECTION

The inputs of the OPA627/637 are protected for voltages between $+V_S + 2V$ and $-V_S - 2V$. If the input voltage can exceed these limits, the amplifier should be protected. The diode clamps shown in Figure 7a will prevent the input voltage from exceeding one forward diode voltage drop beyond the power supplies—well within the safe limits. If

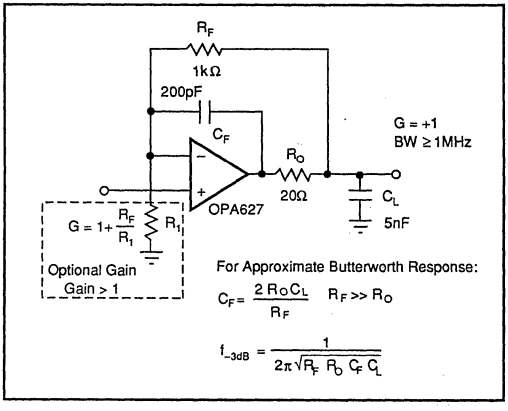


FIGURE 6. Driving Large Capacitive Loads.

the input source can deliver current in excess of the maximum forward current of the protection diodes, use a series resistor, R_S, to limit the current. Be aware that adding resistance to the input will increase noise. The $4nV/\sqrt{Hz}$ theoretical thermal noise of a 1kΩ resistor will add to the $4.5nV/\sqrt{Hz}$ noise of the OPA627/637 (by the square-root of the sum of the squares), producing a total noise of $6nV/\sqrt{Hz}$. Resistors below 100Ω add negligible noise.

Leakage current in the protection diodes can increase the total input bias current of the circuit. The specified maximum leakage current for commonly used diodes such as the 1N4148 is approximately 25nA—more than a thousand times larger than the input bias current of the OPA627/637. Leakage current of these diodes is typically much lower and may be adequate in many applications. Light falling on the junction of the protection diodes can dramatically increase leakage current, so common glass-packaged diodes should be shielded from ambient light. Very low leakage can be achieved by using a diode-connected FET as shown. The 2N4117A is specified at 1pA and its metal case shields the junction from light.

Sometimes input protection is required on I/V converters of inverting amplifiers (Figure 7b). Although in normal operation, the voltage at the summing junction will be near zero (equal to the offset voltage of the amplifier), large input transients may cause this node to exceed 2V beyond the power supplies. In this case, the summing junction should be protected with diode clamps connected to ground. Even with the the low voltage present at the summing junction, common signal diodes may have excessive leakage current. Since the reverse voltage on these diodes is clamped, a diode-connected signal transistor can be used as an inexpensive low leakage diode (Figure 7b).

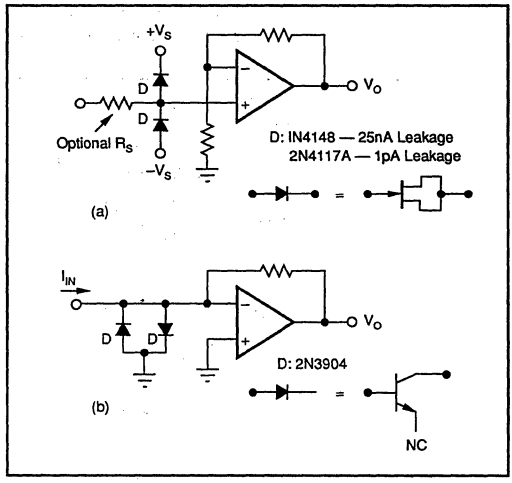


FIGURE 7. Input Protection Circuits.

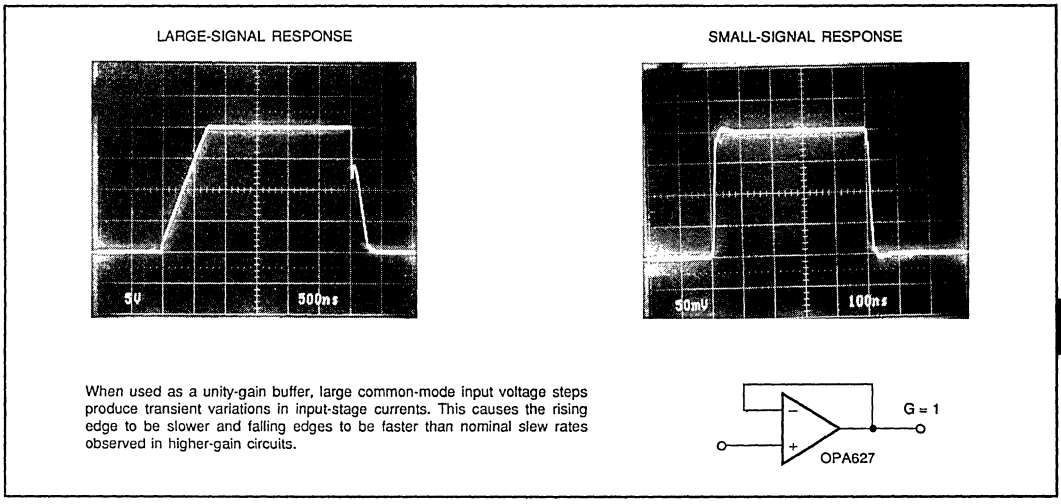


FIGURE 8. OPA627 Dynamic Performance, G = +1.

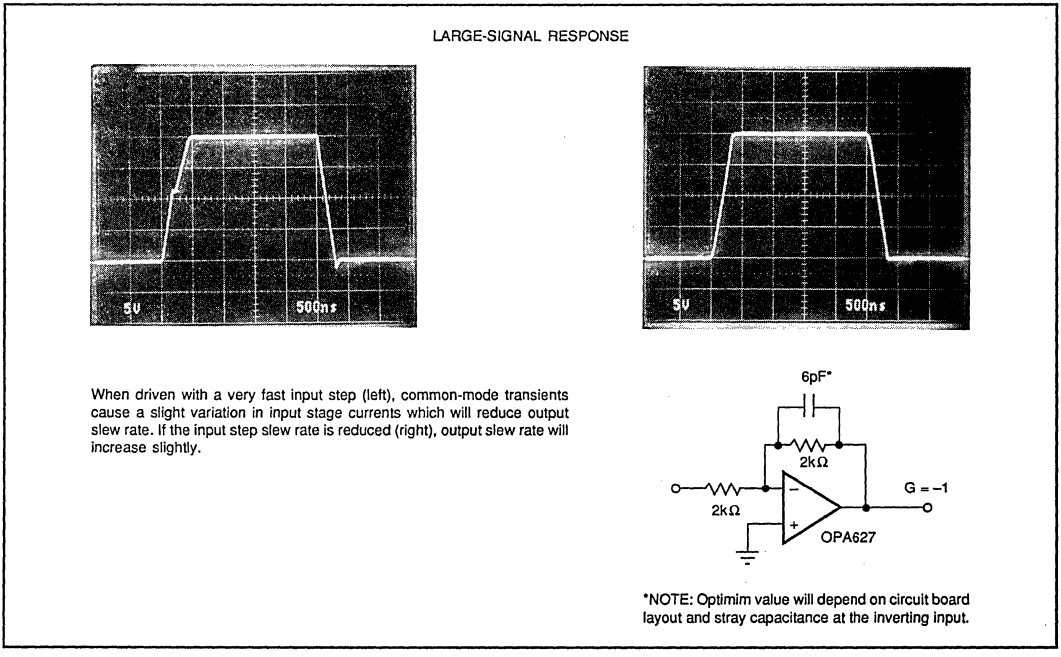


FIGURE 9. OPA627 Dynamic Performance, G = –1.

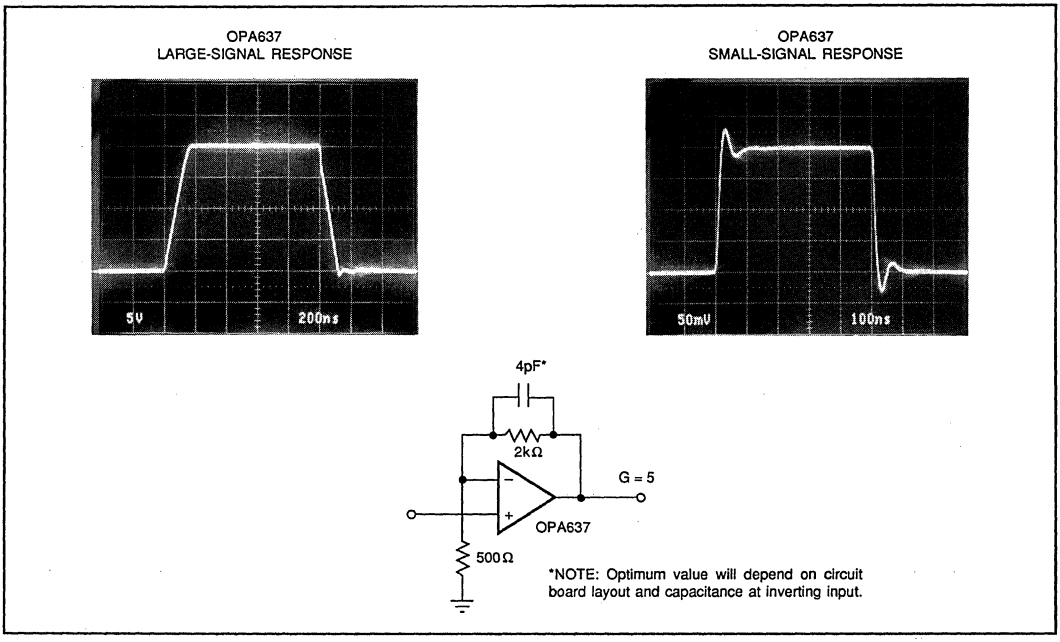
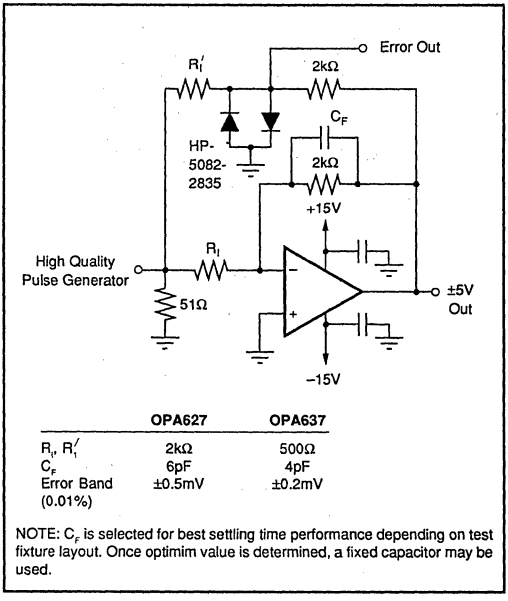


FIGURE 10. OPA637 Dynamic Response, G = 5.



	OPA627	OPA637
R_I, R_I'	2kΩ	500Ω
C_F	6pF	4pF
Error Band (0.01%)	±0.5mV	±0.2mV

NOTE: C_F is selected for best settling time performance depending on test fixture layout. Once optimim value is determined, a fixed capacitor may be used.

FIGURE 11. Settling Time and Slew Rate Test Circuit.

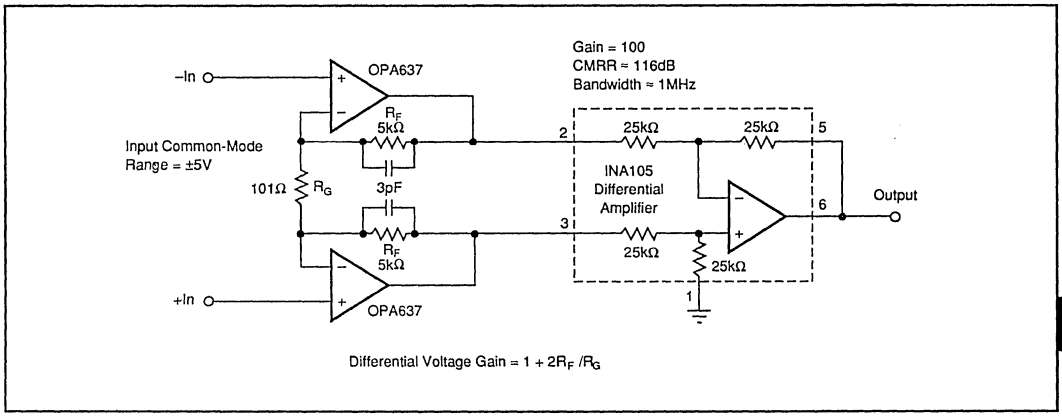


FIGURE 12. High Speed Instrumentation Amplifier, Gain = 100.

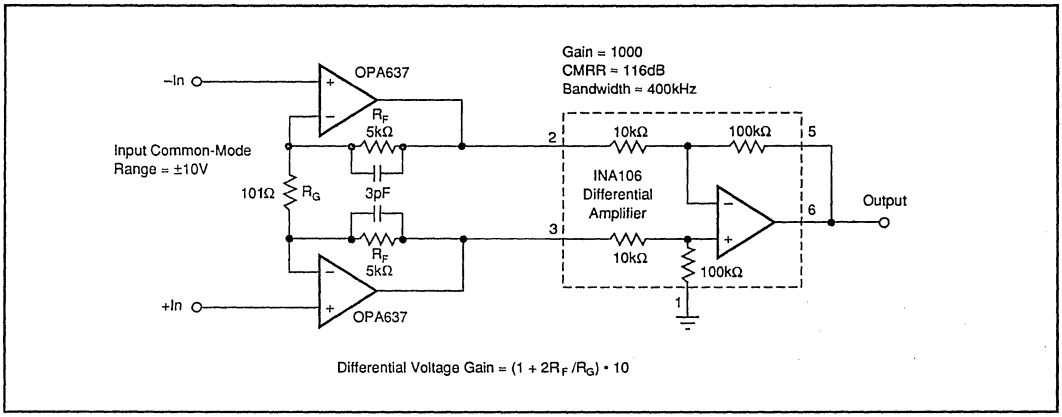
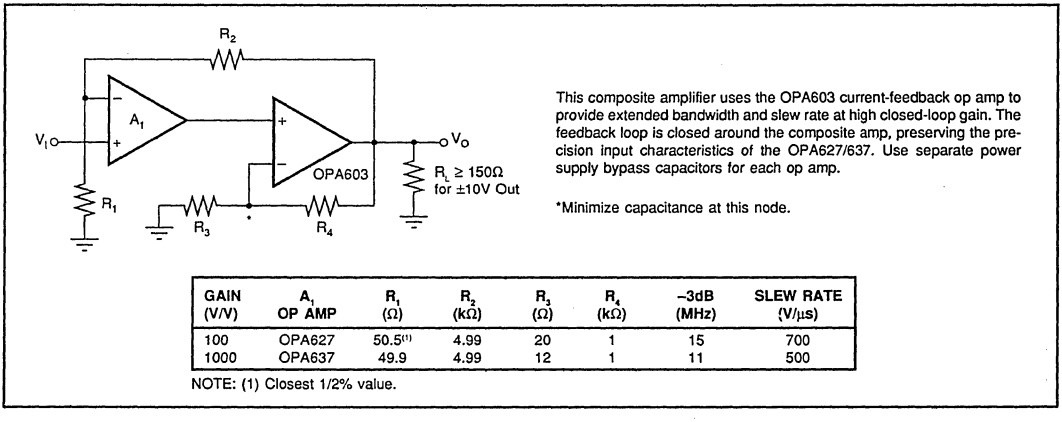


FIGURE 13. High Speed Instrumentation Amplifier, Gain = 1000.

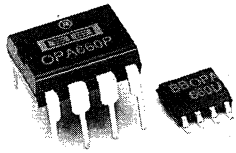


GAIN (V/V)	A_1 OP AMP	R_1 (Ω)	R_2 (kΩ)	R_3 (Ω)	R_4 (kΩ)	–3dB (MHz)	SLEW RATE (V/µs)
100	OPA627	50.5(1)	4.99	20	1	15	700
1000	OPA637	49.9	4.99	12	1	11	500

NOTE: (1) Closest 1/2% value.

FIGURE 14. Composite Amplifier for Wide Bandwidth.

BURR-BROWN®



OPA660

ADVANCE INFORMATION
SUBJECT TO CHANGE

Wide Bandwidth OPERATIONAL TRANSCONDUCTANCE AMPLIFIER AND BUFFER

FEATURES

- WIDE BANDWIDTH: 700MHz
- HIGH SLEW RATE: 2000V/µs
- LOW DIFFERENTIAL GAIN/PHASE DISTORTION
- VERSATILE CIRCUIT FUNCTION

APPLICATIONS

- VIDEO EQUIPMENT
- COMMUNICATIONS EQUIPMENT
- HIGH-SPEED DATA ACQUISITION

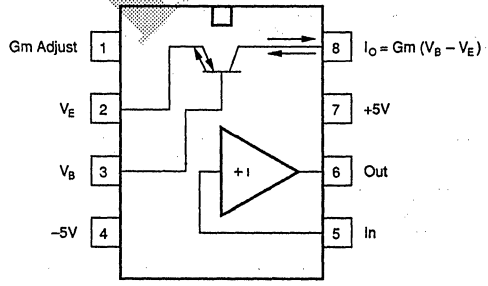
DESCRIPTION

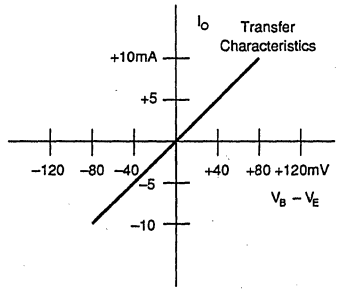
The OPA660 is a versatile building-block component designed for wide-bandwidth systems including high performance video, RF and IF circuitry. It includes an integrated voltage-controlled current source and voltage buffer in an 8-pin package.

The voltage-controlled current source or Operational Transconductance Amplifier (OTA) can be viewed as an "ideal transistor." Like a transistor, it has three terminals—a high-impedance input (base), a low-impedance input/output (emitter), and the current output (collector). The OTA, however, is self-biased and bipolar. The output current is zero for zero differential input voltage. AC inputs centered about zero produce an output current which is bipolar and centered about zero. The transconductance of the OTA can be adjusted with an external resistor, allowing bandwidth, quiescent current and gain tradeoffs to be optimized.

The buffer stage provides 700MHz bandwidth and 2000V/µs slew rate. When combined with the OTA section, the OPA660 can be interconnected as a current-feedback amplifier. Used as basic building blocks, the OPA660 can simplify the design of complex signal processing stages in video systems, communications equipment and high-speed data acquisition circuitry.

The OPA660 is packaged in SO-8 surface-mount, and 8-pin plastic DIP packages and is specified for the industrial temperature range.





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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1072

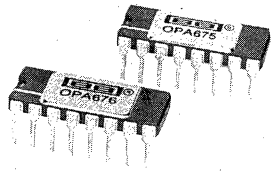
SPECIFICATIONS

ELECTRICAL

Typical at I_O = 20mA, V_S = ±5VDC, T_A = +25°C, R_L = 500Ω unless otherwise specified.

PARAMETER	CONDITIONS	OPA660AP, AU MIN	TYP	MAX	UNITS
OTA TRANSCONDUCTANCE					
Transconductance	V_O = 0V	75		200	mA/V
OPEN LOOP GAIN					
Open Loop Gain			60		dB
OTA INPUT OFFSET VOLTAGE					
Initial			±10	±20	mV
vs Temperature			50		µV/°C
vs Supply (tracking)	V_S = ±4.5V to ±5.5V	55	60		dB
vs Supply (non-tracking)	V+ = 4.5V to 5.5V	40	45		dB
vs Supply (non-tracking)	V– = –4.5V to –5.5V	40	48		dB
OTA NONINVERTING INPUT BIAS CURRENT					
Initial			±3	±5	µA
vs Temperature			5		nA/°C
vs Supply (tracking)	V_S = ±4.5V to ±5.5V			±750	nA/V
vs Supply (non-tracking)	V+ = 4.5V to 5.5V			±1500	nA/V
vs Supply (non-tracking)	V– = –4.5V to –5.5V			±500	nA/V
OTA OUTPUT BIAS CURRENT					
Output Bias Current	V_O = 0V		±10	±20	µA
vs Temperature			500		nA/°C
vs Supply (tracking)	V_S = ±4.5V to ±5.5V		±10	±25	µA/V
vs Supply (non-tracking)	V+ = 4.5V to 5.5V		±10	±25	µA/V
vs Supply (non-tracking)	V– = –4.5V to –5.5V		±10	±25	µA/V
OTA OUTPUT					
Current Output		±8	±15		mA
Output Voltage Compliance	I_O = ±1mA	±4.0	±4.4		V
Output Impedance			15k || 2.5	Ω || pF	
BUFFER OFFSET VOLTAGE					
Initial			±10	±20	mV
vs Temperature			50		µV/°C
vs Supply (tracking)	V_S = ±4.5V to ±5.5V	55	60		dB
vs Supply (non-tracking)	V+ = 4.5V to 5.5V	40	45		dB
vs Supply (non-tracking)	V– = –4.5V to –5.5V	40	48		dB
BUFFER INPUT BIAS CURRENT					
Initial			±3	±5	µA
vs Temperature			10		nA/°C
vs Supply (tracking)	V_S = ±4.5V to ±5.5V			±750	nA/V
vs Supply (non-tracking)	V+ = 4.5V to 5.5V			±1500	nA/V
vs Supply (non-tracking)	V– = –4.5V to –5.5V			±500	nA/V
BUFFER INPUT IMPEDANCE					
Input Impedance			1 || 1		MΩ || pF
BUFFER INPUT NOISE					
Voltage Noise			5		nV/√Hz
BUFFER DYNAMIC RESPONSE					
Small Signal Bandwidth			700		MHz
Full Power	V_O = ±2.5V		550		MHz
Differential Gain	3.58MHz, at 0.7V		0.1		%
Differential Phase	3.58MHz, at 0.7V		0.1		Degrees
Harmonic Distortion	2nd Harmonic		–65		dB
	3rd Harmonic		–90		dB
Slew Rate	5V Step		2000		V/µs
Settling Time 0.1%	2V Step		25		ns
Rise Time (10% to 90%)	V_O = 100mVp-p		1		ns
	5V Step		2		ns
BUFFER RATED OUTPUT					
Voltage Output		±4.00	±4.15		V
Current Output		8	15		mA
Gain		0.96	0.975		V/V
	R_L = 5kΩ		0.99		V/V
Output Impedance			8 || 2		Ω || pF
POWER SUPPLY					
Rated Voltage			±5		V
Derated Performance		±4.5		±5.5	V

BURR-BROWN®



OPA675
OPA676

Wideband Switched-Input OPERATIONAL AMPLIFIER

FEATURES

- FAST SETTLING: 9ns (1%)
- WIDE BANDWIDTH: 185MHz (A_V = 10)
- LOW OFFSET VOLTAGE: ±250µV
- TWO LOGIC SELECTABLE INPUTS
- FAST INPUT SWITCHING: 6ns (TTL)
- 16-PIN DIP PACKAGE

APPLICATIONS

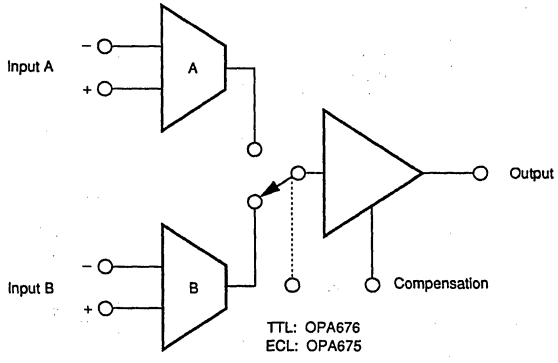
- PROGRAMMABLE-GAIN AMPLIFIER
- FAST 2-INPUT MULTIPLEXER
- SYNCHRONOUS DEMODULATOR
- PULSE/RF AMPLIFIERS
- VIDEO AMPLIFIERS
- ACTIVE FILTERS

DESCRIPTION

The OPA675 and OPA676 are wideband monolithic operational amplifiers with two independent differential inputs. Either input can be selected by an external logic signal. The OPA675 is compatible with ECL logic while the OPA676 is TTL compatible. Both amplifiers are externally compensated and feature very fast input selection speed: ECL = 4ns, TTL = 6ns. This amplifier features fully symmetrical differential inputs due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA675/676 may be used in all op amp applications requiring high speed and precision.

Low distortion and crosstalk make these amplifiers suitable for RF and video applications.

The OPA675 and OPA676 are available in KG (0°C to +70°C) and SG (–55°C to +125°C) grades. All grades are packaged in a 16-pin DIP.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
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PDS-864A

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 150Ω, and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	JG/SG MIN	JG/SG TYP	JG/SG MAX	KG MIN	KG TYP	KG MAX	UNITS
INPUT NOISE[1]								
Voltage: f_O = 10Hz	R_S = 0Ω		27			*		nV/√Hz
f_O = 100 Hz			10			*		nV/√Hz
f_O = 1kHz			3.8			*		nV/√Hz
f_O = 10kHz			2.6			*		nV/√Hz
f_O = 100kHz			2.4			*		nV/√Hz
f_B = 10Hz to 10MHz			7.9			*		µVrms
Current: f_O = 10Hz to 1MHz			2.7			*		pA/√Hz
OFFSET VOLTAGE[1]								
Input Offset Voltage	V_{CM} = 0VDC		±500	±2mV		±250	±1mV	µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±3	±10		±1	±5	µV/°C
Supply Rejection	$\pm V_{CC}$ = 4.5V to 5.5V	65	86		70	*		dB
BIAS CURRENT[1]								
Input Bias Current	V_{CM} = 0VDC		23	35		*	30	µA
OFFSET CURRENT[1]								
Input Offset Current	V_{CM} = 0VDC		0.8	5		*	*	µA
INPUT IMPEDANCE[1]								
Differential			4K||2			*		Ω||pF
Common-Mode			10^5||5			*		Ω||pF
INPUT VOLTAGE RANGE[1]								
Common-Mode Input Range			±2.5		*	*		V
Common-Mode Rejection	V_{IN} = ±0.5VDC, V_O = ±1.25V	75	100		85	*		dB
OPEN LOOP GAIN, DC[1]								
Open-Loop Voltage Gain		65	70		*	*		dB
FREQUENCY RESPONSE								
Closed-Loop Bandwidth	Gain = +2V/V		100			*		MHz
	Gain = +5V/V		145			*		MHz
	Gain = +10V/V		185			*		MHz
	Gain = +50V/V		60			*		MHz
Crosstalk	Gain = +10V/V, f = 100kHz		–100			*		dBC[2]
	f = 1MHz		–80			*		dBC
	f = 10MHz		–68			*		dBC
	f = 100MHz		–35			*		dBC
Harmonic Distortion: 10MHz	G = +10V/V, R_L = 50Ω, V_O = 0.5Vp-p							
	Second Harmonic		–61			*		dBC
	Third Harmonic		–73			*		dBC
Full Power Response	V_O = 2.5Vp-p, Gain = +10V/V	25	44		30	*		MHz
Slew Rate	Gain = +10V/V	200	350		240	*		V/µs
Settling Time: 1%			9			*		ns
0.1%	Gain = +10V/V		15			*		ns
0.01%	0.625V Output Step		25			*		ns
INPUT SELECTION[3]								
Transition Time	ECL: OPA675		4			*		ns
50% in to 50% Out	TTL: OPA676		6			*		ns
DIGITAL INPUT								
TTL Logic Levels: V_{IL}	Logic "LO"	0		+0.8	*		*	V
V_{IH}	Logic "HI"	+2.0		+5	*		*	V
I_{IL}	Logic "LO", V_{IL} = 0V		–0.05	–0.2		*	*	mA
I_{IH}	Logic "HI", V_{IH} = +2.7V		1	20		*	*	µA
ECL Logic Levels: V_{IL}	Logic "LO"	–1.81		–1.475	*		*	V
V_{IH}	Logic "HI"	–1.15		– 0.88	*		*	V
I_{IL}	Logic "LO", V_{IL} = –1.6V		–50	–100		*		µA
I_{IH}	Logic "HI", V_{IH} = –1.0V		–50	–100		*		µA
RATED OUTPUT								
Voltage Output	R_L = 150Ω	±2.1	±2.6		*	*		V
	R_L = 50Ω	+1.25	+1.8		*	*		V
		–0.95	–1.1		–1.0	*		V
Current Output			±30			*		mA
Output Resistance	1MHz, Open Loop, C_C = 5pF		5			*		Ω
Load Capacitance Stability	Gain = +2V/V		50			*		pF
Short Circuit Current	Continuous to Gnd		+45		*	*	*	mA
			–25		*	*	*	mA

* Same specifications as for JG.

SPECIFICATIONS (cont)

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 150Ω, and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	JG/SG MIN	JG/SG TYP	JG/SG MAX	KG MIN	KG TYP	KG MAX	UNITS
POWER SUPPLY								
Rated Voltage	$\pm V_{CC}$		5			*		VDC
Derated Performance	$\pm V_{CC}$	4.5		6.5	*		*	VDC
Current, Quiescent	I_O = 0mADC		22	30		*	*	mA
TEMPERATURE RANGE								
Specification	Ambient Temp JG, KG	0		+70	*		*	°C
	SG	−55		+125				°C
Operating:	Ambient Temp JG, KG, SG	−55		+125	*		*	°C
θ_{JA}			125			*		°C/W

* Same specifications as for JG.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±5VDC, R_L = 150Ω, and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

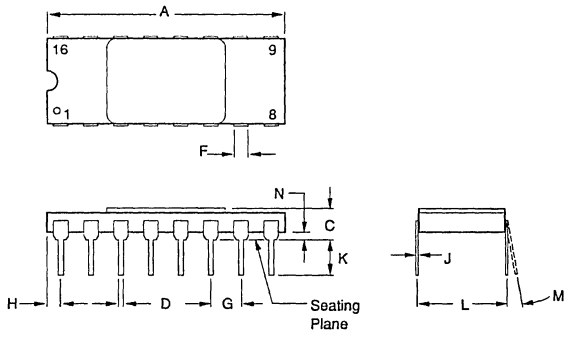
PARAMETER	CONDITIONS	JG/SG MIN	JG/SG TYP	JG/SG MAX	KG MIN	KG TYP	KG MAX	UNITS
TEMPERATURE RANGE								
Specification	Ambient Temp JG, KG	0		+70	*		*	°C
	SG	−55		+125				°C
OFFSET VOLTAGE								
Average Drift	T_A = T_{MIN} to T_{MAX}		±3	±10		±1	±5	µV/°C
Supply Rejection	$\pm V_{CC}$ = 4.5V to 5.5V	60	85		65	*		dB
BIAS CURRENT								
Input Bias Current	V_{CM} = 0VDC		29	50		*	*	µA
OFFSET CURRENT								
Input Offset Current	V_{CM} = 0VDC		0.8	10		*	*	µA
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±2.0	±2.3		*	*		V
Common-Mode Rejection	V_{IN} = ±0.5VDC, V_O = ±1.25V	60	80		65	*		dB
OPEN LOOP GAIN, DC								
Open-Loop Voltage Gain		60	68		63	69		dB
DIGITAL INPUT								
TTL Logic Levels: V_{IL}	Logic "LO"	0		+0.8	*		*	V
V_{IH}	Logic "HI"	+2.0		+5	*		*	V
I_{IL}	Logic "LO", V_{IL} = 0V		−0.08	−0.4		*	*	mA
I_{IH}	Logic "HI", V_{IH} = +2.7V		5	50		*	*	µA
ECL Logic Levels: V_{IL}	Logic "LO"	−1.81		−1.475	*		*	V
V_{IH}	Logic "HI"	−1.15		−0.88	*		*	V
I_{IL}	Logic "LO", V_{IL} = −1.6V		−50			*		µA
I_{IH}	Logic "HI", V_{IH} = −1.0V		−50			*		µA
RATED OUTPUT								
Voltage Output	R_L = 150Ω	±2.0	±2.5		*	*		V
	R_L = 50Ω	+1.25	+1.6		*	*		V
		−0.8	−1.0		−0.9	*		V
POWER SUPPLY								
Current, Quiescent	I_O = 0mADC		25	35		*	*	mA

* Same specifications as for JG.

NOTES: (1) Specifications are for both inputs (A and B). (2) dBC = Level referred to carrier-input signal. (3) Switching time from application of digital logic signal to input signal selection.

MECHANICAL

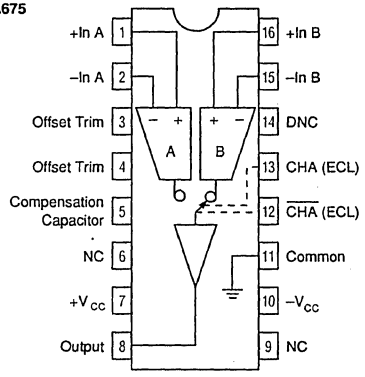
G Package — 16-Pin Hermetic DIP



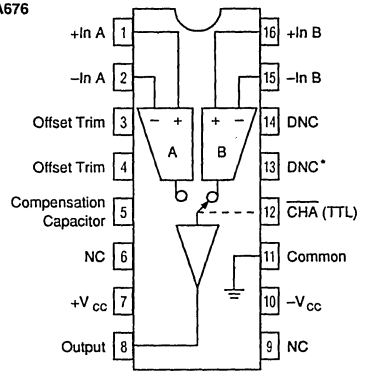
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

OPA675



OPA676



*Capacitance on this node slows channel select.

PIN ASSIGNMENTS: OPA675

1	+In A	16	+In B
2	–In A	15	–In B
3	Offset Trim	14	DNC
4	Offset Trim	13	CHA (ECL)
5	Compensation Capacitor	12	CHA (ECL)
6	NC	11	Common
7	$+V_{cc}$	10	$-V_{cc}$
8	Output	9	NC

DNC = Do Not Connect NC = No Internal Connection

PIN ASSIGNMENTS: OPA676

1	+In A	16	+In B
2	–In A	15	–In B
3	Offset Trim	14	DNC
4	Offset Trim	13	DNC
5	Compensation Capacitor	12	CHA (TTL)
6	NC	11	Common
7	$+V_{cc}$	10	$-V_{cc}$
8	Output	9	NC

DNC = Do Not Connect NC = No Internal Connection

ABSOLUTE MAXIMUM RATINGS

Supply	±7VDC
Differential Input Voltage	Total V_{cc}
Input Voltage Range (Analog and Digital)	$\pm V_{cc}$
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Ground (+25°C)	Continuous to ground
Junction Temperature	+175°C

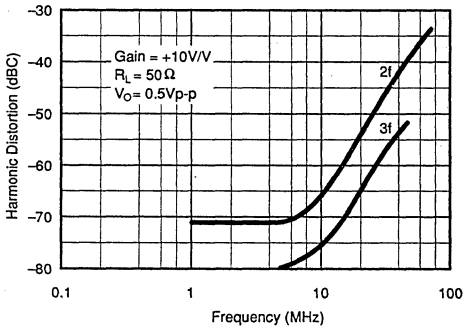
ORDERING INFORMATION

OPA675 ( )( )
OPA676 ( )( )

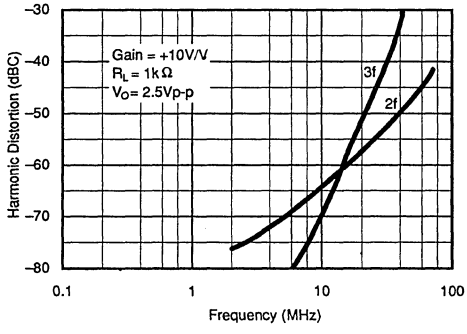
Basic Model Number
Performance Grade Code
J, K: 0°C to +70°C
S: –55°C to +125°C
Package Code
G: 16-pin Ceramic DIP

TYPICAL PERFORMANCE CURVES

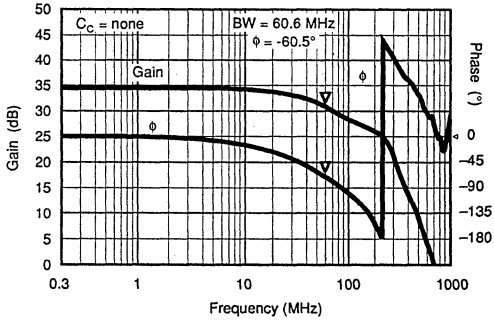
SMALL SIGNAL
HARMONIC DISTORTION vs FREQUENCY



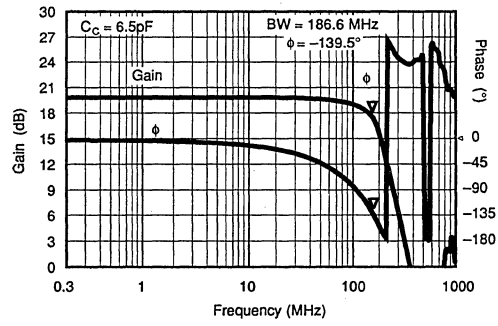
LARGE SIGNAL
HARMONIC DISTORTION vs FREQUENCY



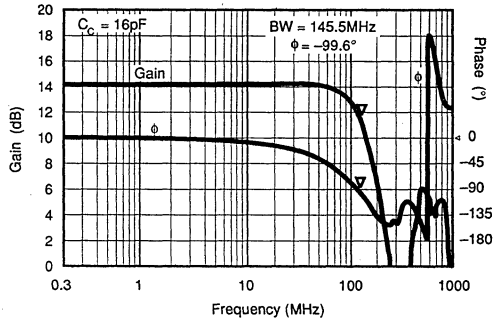
A_V = +50V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH



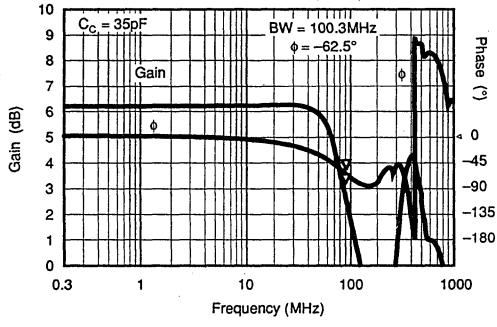
A_V = +10V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH



A_V = +5V/V CLOSED-LOOP
SMALL SIGNAL BAND WIDTH

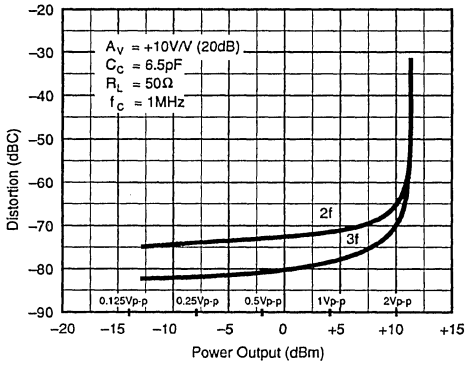


A_V = +2V/V CLOSED-LOOP
SMALL SIGNAL BAND WIDTH

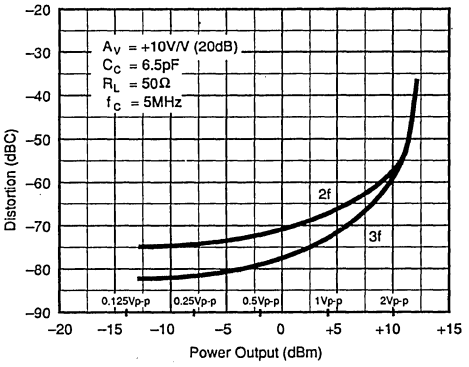


TYPICAL PERFORMANCE CURVES (cont)

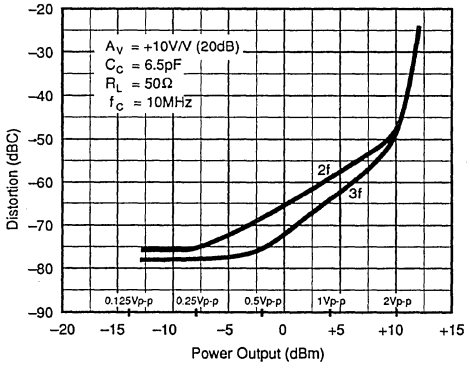
1MHz HARMONIC DISTORTION vs POWER OUTPUT



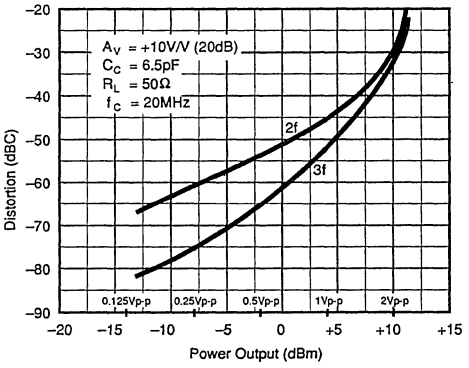
5MHz HARMONIC DISTORTION vs POWER OUTPUT



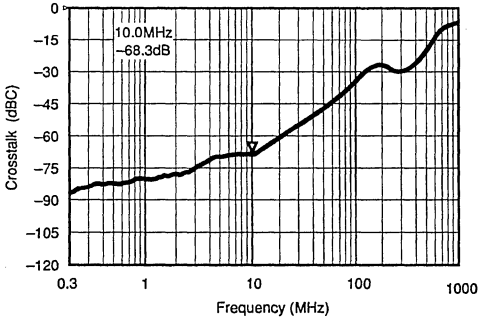
10MHz HARMONIC DISTORTION vs POWER OUTPUT



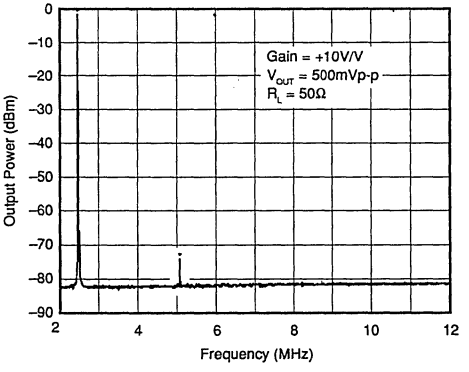
20MHz HARMONIC DISTORTION vs POWER OUTPUT



CHANNEL-TO-CHANNEL
CROSSTALK vs FREQUENCY

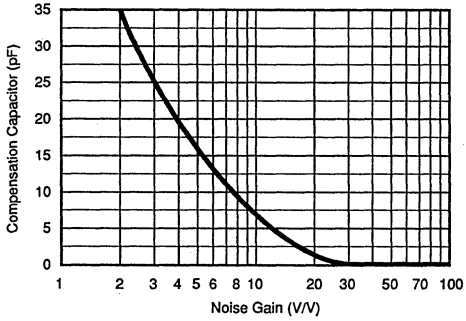


2.5MHz SMALL-SIGNAL
HARMONIC DISTORTION SPECTRUM

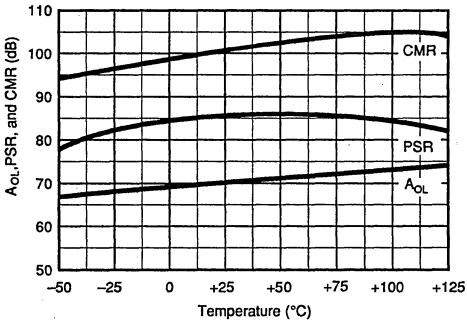


TYPICAL PERFORMANCE CURVES (cont)

NOMINAL FREQUENCY COMPENSATION vs NOISE GAIN



OPEN -LOOP GAIN, CMR AND PSR vs TEMPERATURE



THEORY OF OPERATION

An OPA675 simplified circuit is shown in Figure 1. It is a "classical" high-speed op-amp architecture with one important exception — the amplifier has two ECL logic selectable differential input stages. An appropriate differential ECL logic signal on A and $\overline{A}$ (labeled B Select) will turn on either Q5 or Q6, steering operating (tail) current to either differential input pair Q1 and Q2 or Q3 and Q4. The input pair receiving the tail current operates as a conventional op-amp input stage while the de-selected input pair receiving no tail current appears as an open circuit. The de-selected inputs have only a few pF parasitic capacitance and in the off condition exhibit only a very low leakage (bias) current of about 100pA. Two feedback networks can be connected to each input separately allowing a wide range of circuit applications. The feedback network connected to the selected input operates in a normal op amp fashion while the feedback network connected to the de-selected input is totally inactive, appearing only as an additional load to the amplifier's output stage.

The switched-input op amp (SWOP AMP) circuit of the OPA676 is basically the same as the OPA675 but a TTL compatible level shifter (Figure 2) has been added to its input selection logic circuit.

Standard TTL (OPA676) and ECL (OPA675) logic levels may be applied to each input selection circuit but only 350mV is typically required to switch between inputs. This logic input sensitivity allows simpler high-speed logic driver circuitry and it minimizes digital noise coupling into adjacent wideband analog circuitry and allows single ended ECL inputs to be used with V_{BB} applied to the other input.

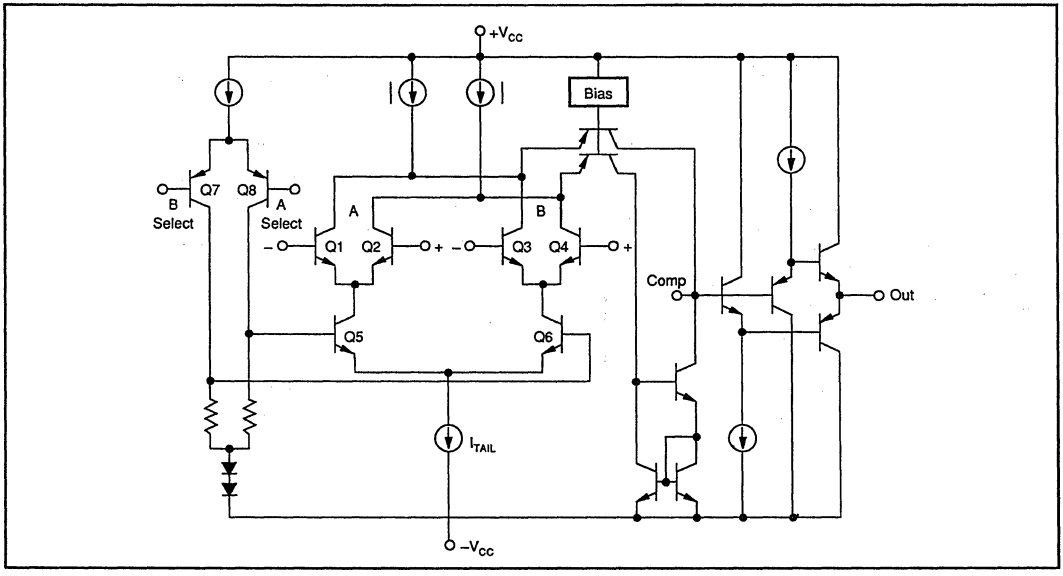


FIGURE 1. OPA675 Simplified Circuit Diagram.

The OPA675 and OPA676 are designed to be frequency compensated by a single capacitor connected from pin 5 to ground. Recommended compensation is shown in Typical Performance Curves. A small variable capacitor may be trimmed for best bandwidth, settling time, and gain peaking. This amplifier is designed for optimum performance in gains of 5V/V to 20 V/V but it can also be used over a far wider range of gains with excellent results. Closed-loop gain/phase (Bode) plots are shown in the Typical Performance Curves.

OFFSET TRIM

Input offset voltage is low enough for many video applications. If desired, offset voltage can be trimmed with a 1kΩ potentiometer connected to $+V_{CC}$. Trimming offset voltage in this manner will effect both input A and input B; independent control of input offset will require that trim adjust current be summed into one or both inputs. This technique is shown in a few applications circuits on the pages to follow.

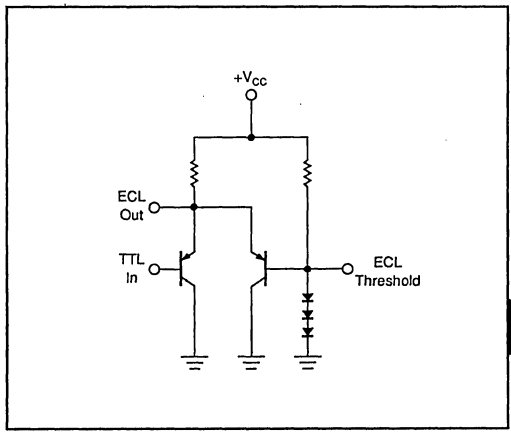


FIGURE 2. Internal OPA676 TTL Logic Level Shifter.

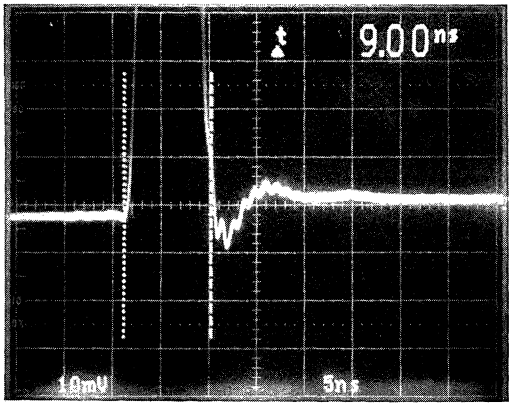


FIGURE 3. 1% Settling Time.

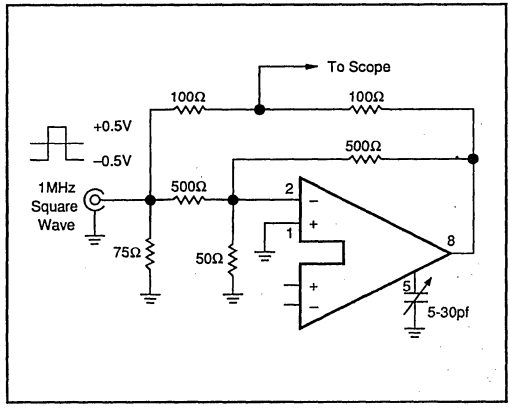


FIGURE 4. OPA675/676 Settling Time Test Circuit.

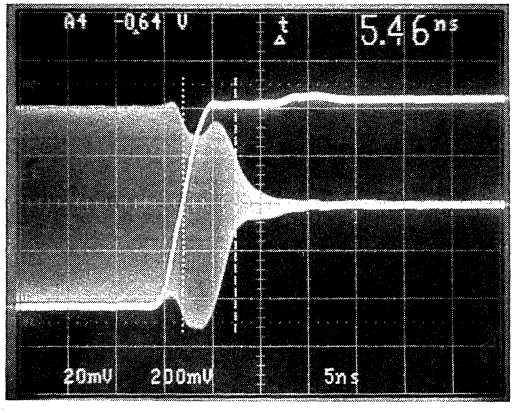


FIGURE 5. OPA676 Input Selection Time. Input A to B.

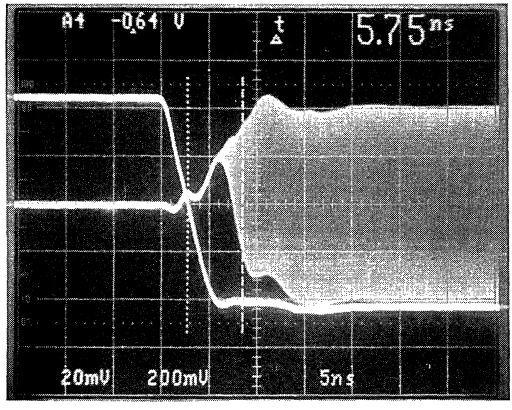


FIGURE 6. OPA676 Input Selection Time. Input B to A.

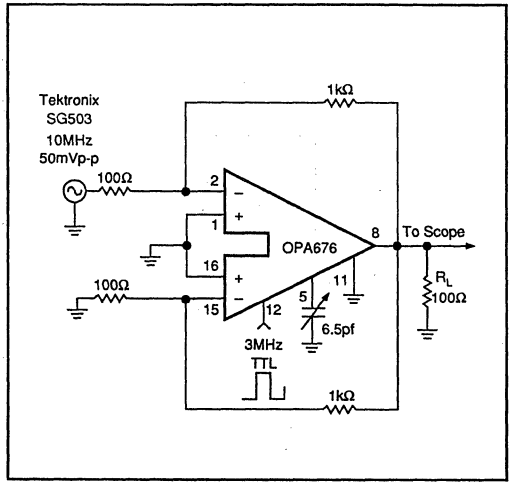


FIGURE 7. OPA676 Input Selection Transition Time Test Circuit.

APPLICATION TIPS

Wideband amplifier circuits require good layout techniques to be successful. The use of short, direct signal paths and heavy (2oz copper recommended) ground planes are absolutely necessary to achieve the performance level inherent in the OPA675/676. Oscillation, ringing, poor bandwith and settling, gain peaking, and instability are typical problems that plague all high-speed amplifiers when they are used in poor layouts. The OPA675 and OPA676 are no different in this respect — any amplifier with a gain bandwith product of a few GHz requires some care be taken in its application.

Points to remember:

1. Use a heavy copper ground plane on the component side of your PC board. This provides a low inductance ground and it also conducts heat from active circuit package pins into ambient air by convection.
2. Bypass power supply pins directly at the active device. The use of tantalum capacitors (1 to 10µF/10V) with very short leads is highly recommended. Supply pins should not be left unbypassed.

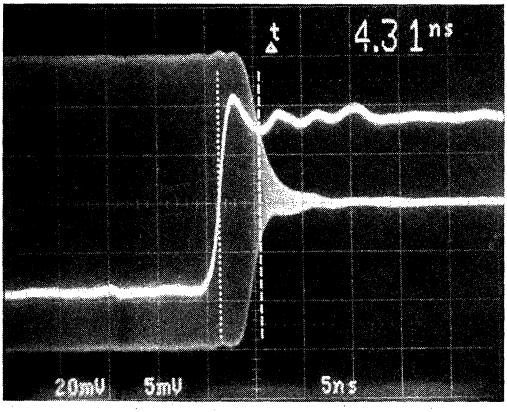


FIGURE 8. OPA675 Input Selection Time. Input A to B.

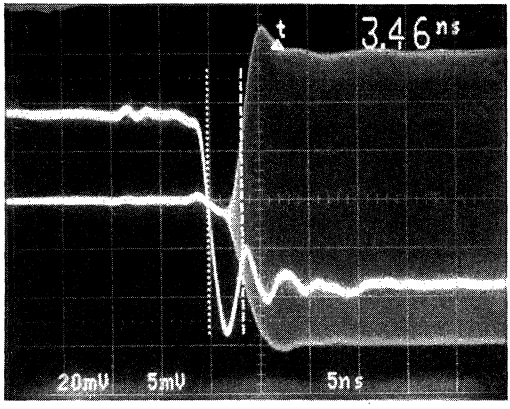


FIGURE 9. OPA675 Input Selection Time. Input B to A.

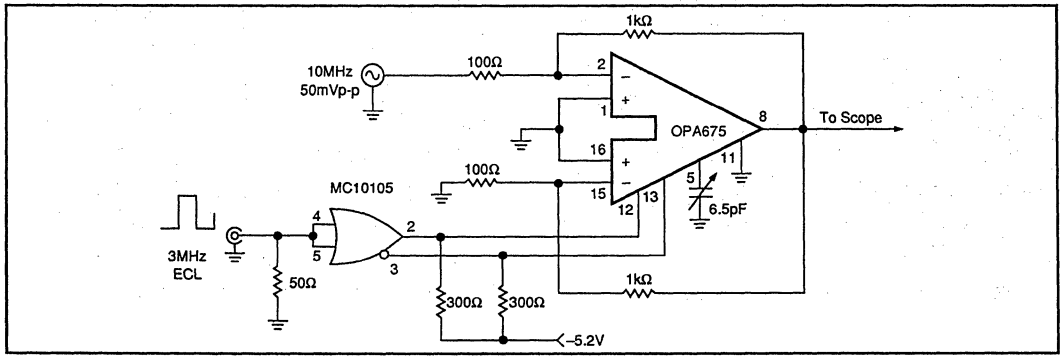


FIGURE 10. OPA675 Input Selection Transition Time Test Circuit.

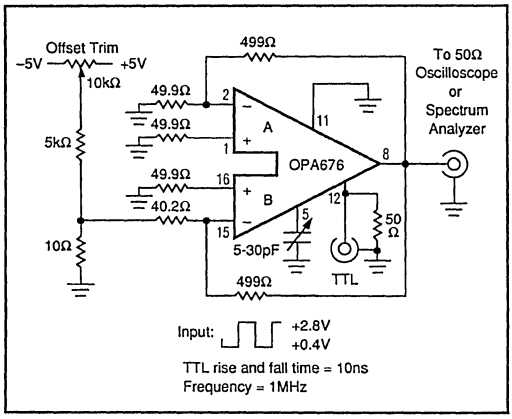


FIGURE 11. OPA676 Carrier Feedthrough and Switching Transient Test Circuit.

3. Signal paths should be short and direct. Feedback resistors, compensation capacitors, termination resistors, etc should have lead lengths no longer than 1/4 inch (6cm).
4. Surface mount components (chip resistors, capacitors, etc) have low inductance and are therefore recommended. Parasitic inductance and capacitance should be avoided if best performance is to be achieved.
5. Resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable range to about 1kΩ or on the high resistance end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon compensation resistors will be satisfactory.
6. Wirewound resistors (even "non-inductive" types) are absolutely unacceptable in high frequency circuits.
7. Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its "load." Lowest distortion is achieved with high impedance loads.
8. PC board traces for signal and power lines should be wide to reduce impedance or inductance.
9. Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, the use of ±15V supplies will result in destruction.
10. Standard commercial test equipment has not been designed to test devices in the OPA675/676 speed range. Benchtop op-amp testers and ATE systems will require a special test head to successfully test these amplifiers.
11. High-speed amplifiers can drive only a limited amount of capacitance. If the load exceeds 10 to 20pF consider using a fast buffer or a small resistor to isolate the capacitance from the amplifier's output. Capacitive loads will cause loop instability if not compensated for.
12. Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears as a purely resistive impedance.
13. For clean, fast input selection the logic input pins should be terminated with appropriate resistors. Resistors should be connected from input selection pins to ground plane with short leads. Failure to terminate long lines will result in ringing and poor high frequency switching.
14. Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is required; there is no shortcut.

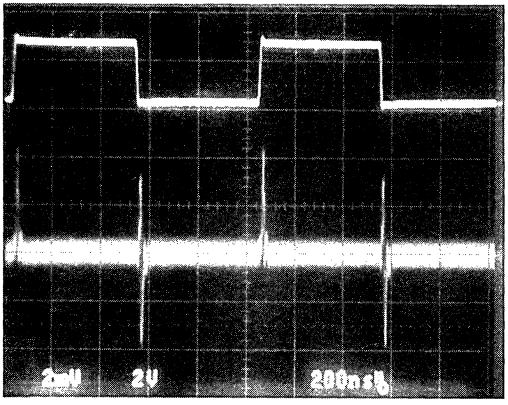


FIGURE 12. OPA676 Switching Transient. Top Trace: TTL Input (2V/cm). Bottom Trace: Amplifier Output (2mV/cm). Input B Offset Voltage has been Trimmed to Match Input A Offset Voltage.

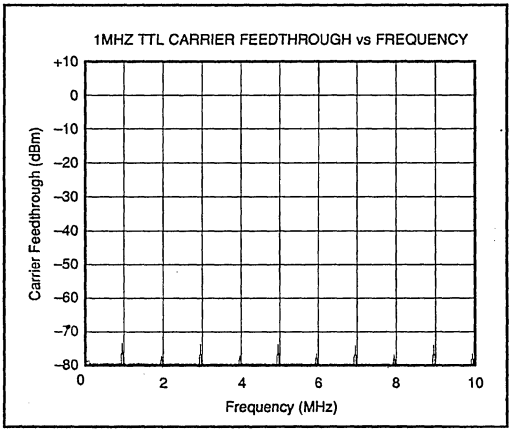


FIGURE 13. Carrier Feedthrough from 1MHz TTL Logic. Offset Trimmed for Maximum Carrier Rejection

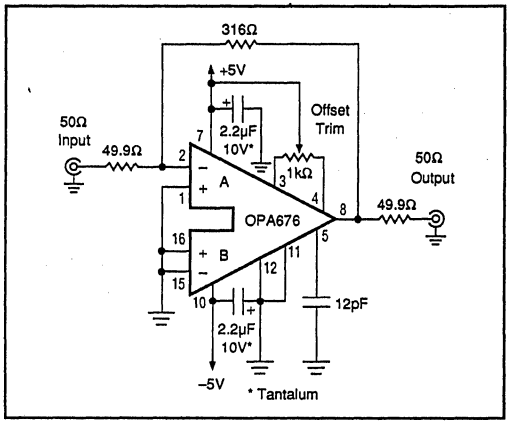


FIGURE 14. OPA676 Used As A Conventional Op-Amp: A 10dB Gain Wideband Video Amplifier with 50Ω Input/Output Impedance.

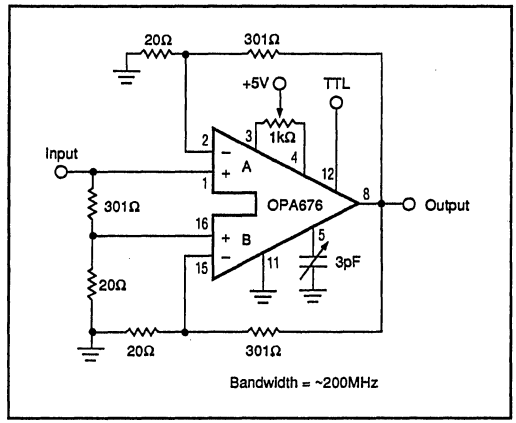


FIGURE 15. Very Fast Programmable Gain Amplifier with Voltage Gains of +1V/V and +16V/V (0dB and 24dB).

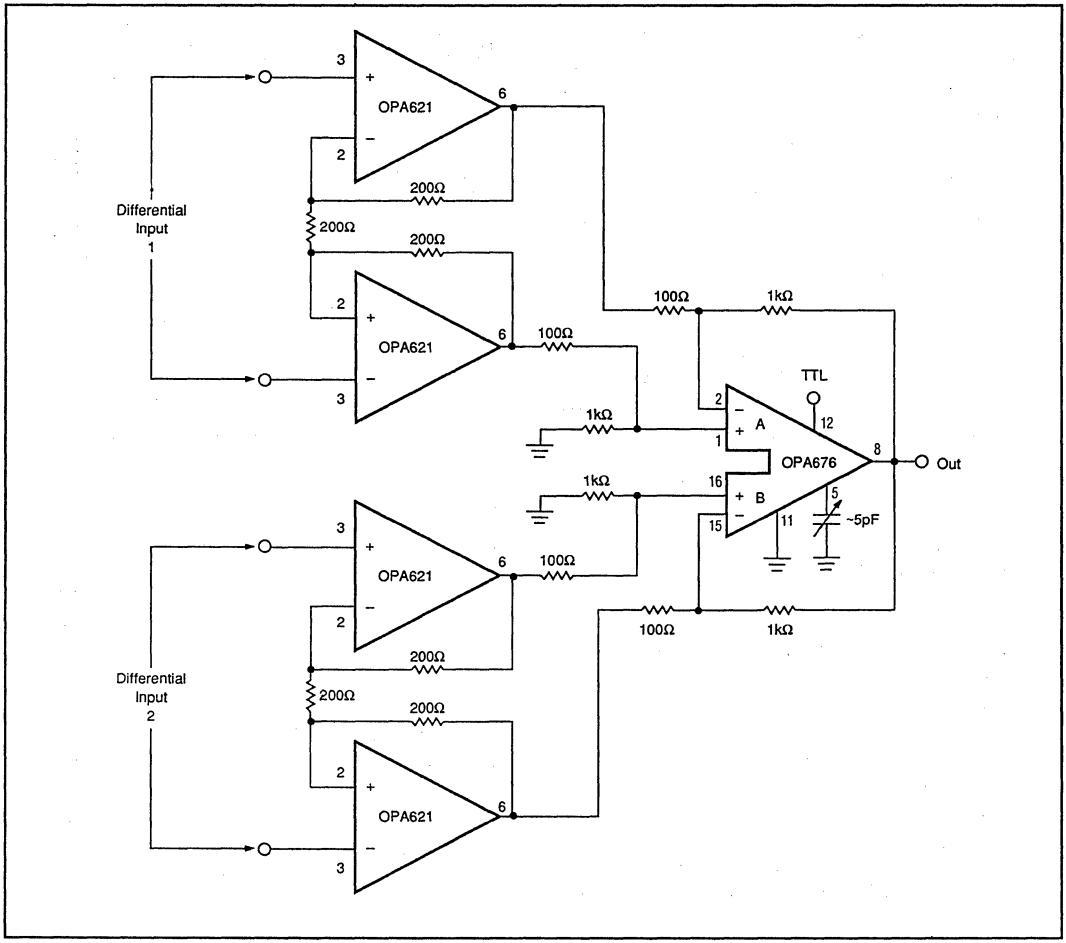


FIGURE 16. High Input Impedance Differential Input Multiplexer with Gain of 30V/V (30dB).

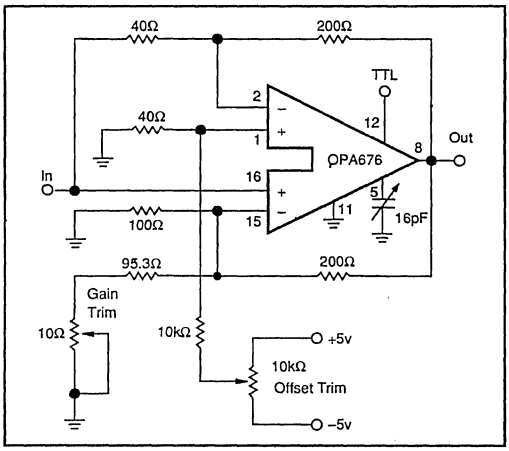


FIGURE 17. Synchronous Modulator/Demodulator with Carrier Balance Trim (Gain = ±5V/V).

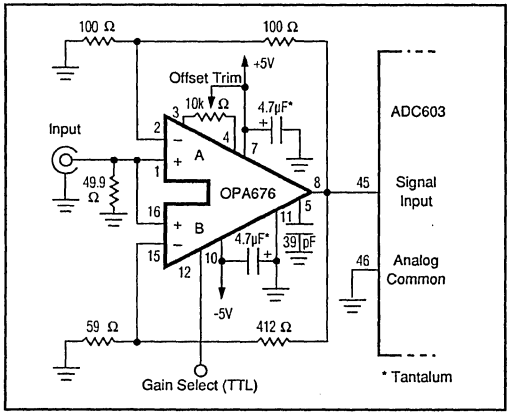


FIGURE 18. Programmable-Gain +2V/V (6dB) or +8V/V (18dB) Buffer Amplifier for Floating-Point Conversion.

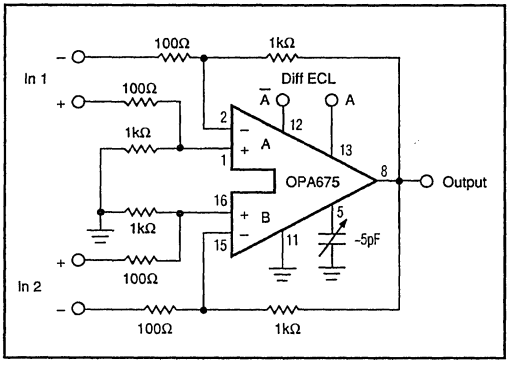


FIGURE 19. Differential Input Multiplexer with Gain of 10V/V (20dB).

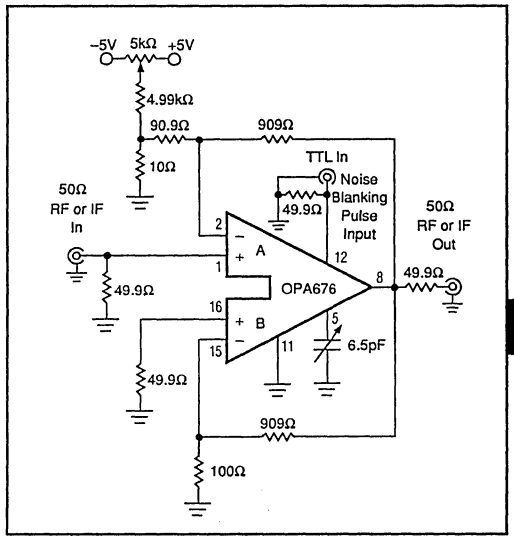


FIGURE 20. Receiver Noise Blanker: A Wideband Gated Video Amplifier.

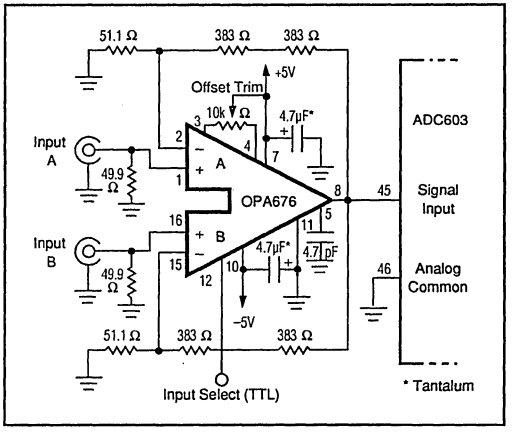


FIGURE 21. Multiplexed Input +16V/V Gain (24dB) Buffer Amplifier.

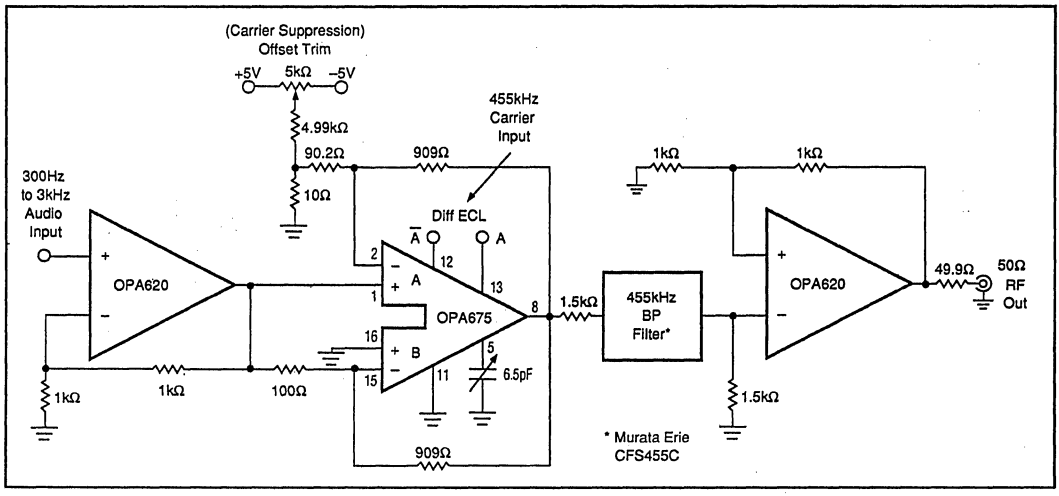
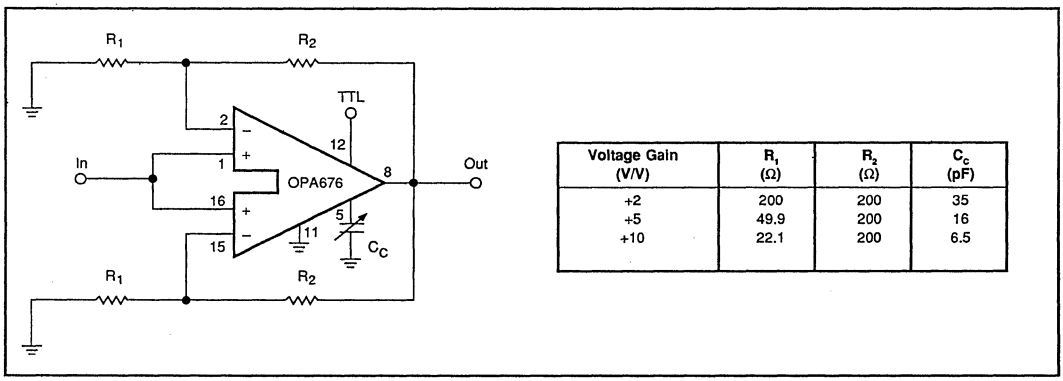
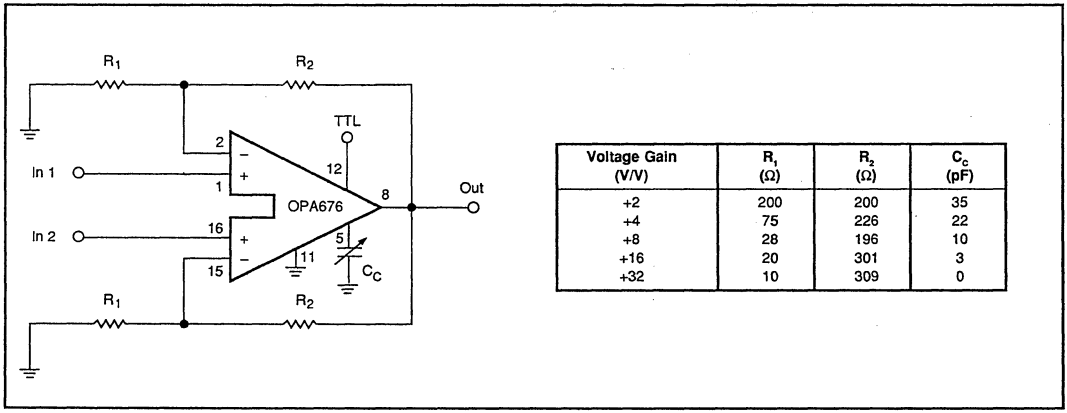


FIGURE 22. Single Sideband Supressed Carrier Generator.



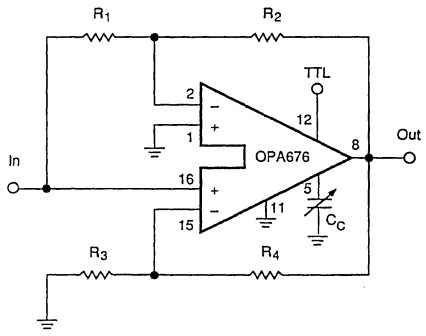
Voltage Gain (V/V)	R_1 (Ω)	R_2 (Ω)	C_c (pF)
+2	200	200	35
+5	49.9	200	16
+10	22.1	200	6.5

FIGURE 23. Programmable-Gain Amplifier.



Voltage Gain (V/V)	R_1 (Ω)	R_2 (Ω)	C_c (pF)
+2	200	200	35
+4	75	226	22
+8	28	196	10
+16	20	301	3
+32	10	309	0

FIGURE 24. Two-Input Multiplexer (with gain).



Voltage Gain (V/V)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)	C_C (pF)
±2	100	200	200	200	35
±5	40	200	50	200	16
±10	20	200	25	225	6.5

FIGURE 25. Synchronous Modulator/Demodulator (with gain).

BURR-BROWN®

OPA1013

Precision, Single-Supply DUAL OPERATIONAL AMPLIFIER

FEATURES

- SINGLE POWER SUPPLY OPERATION
- INPUT VOLTAGE RANGE TO GROUND
- OUTPUT SWINGS NEAR GROUND
- LOW QUIESCENT CURRENT: 500μA max
- LOW V_{OS}: 150μV max
- LOW DRIFT: 2μV/°C max
- LOW I_{OS}: 0.8nA max
- LOW NOISE: 0.55μVp-p, 0.1Hz to 10Hz

APPLICATIONS

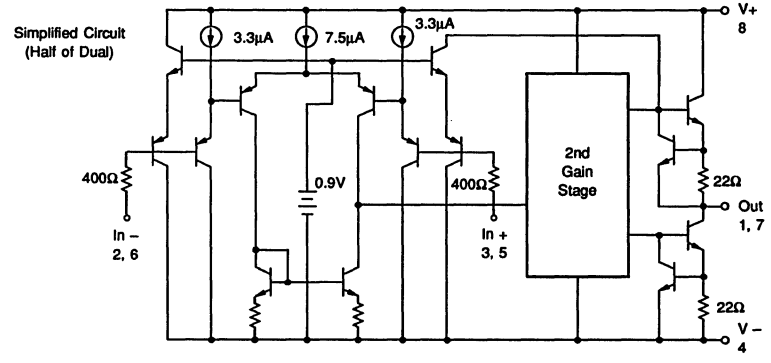
- PRECISION INSTRUMENTATION
- BATTERY-POWERED EQUIPMENT
- BRIDGE AMPLIFIERS
- 4-20mA CURRENT TRANSMITTERS
- VOLTAGE COMPARATOR

DESCRIPTION

The OPA1013 dual operational amplifier provides precision performance in single power supply and low power applications. It is laser trimmed for low offset voltage and drift, greatly reducing the large errors common with LM324-type op amps. Input offset current is also trimmed to reduce errors in high impedance applications.

The OPA1013 is characterized for operation at both +5V (single supply) and ±15V power supplies. When operated from a single supply, the input common-mode range includes ground and the output can swing to within 15mV of ground. Completely independent biasing networks eliminate interaction between the two amplifiers—even when one is used as a comparator.

The OPA1013 is available in 8-pin plastic DIP and metal TO-99 packages, specified for the 0°C to 70°C and –55°C to 125°C temperature ranges.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1059A

SPECIFICATIONS

ELECTRICAL

V_S = ±15V, V_{CM} = 0V, T_A = +25°C unless otherwise noted.

PARAMETER	CONDITION	OPA1013AM/AC			OPA1013M/C/DN8			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage			±15	±150		±50	±300	µV
	OPA1013DN8					±200	±800	µV
Time Stability			0.4			0.5		µV/Mo
Input Offset Current			±0.045	±0.8		±0.08	±1.5	nA
Input Bias Current			6	20		7	30	nA
Voltage Noise, BW = 0.1 to 10Hz			0.55			0.55		µVp-p
Noise Density, f = 10Hz			28			28		nV/√Hz
f = 1kHz			25			25		nV/√Hz
Current Noise Density, f = 10Hz			0.12			0.12		pA/√Hz
Input Resistance: Differential		100	400		70	300		MΩ
Input Resistance: Common-Mode			5			4		GΩ
Open-Loop Voltage Gain	V_O = ±10V, R_L = 2kΩ	1.5	3.1		1.2	2.9		V/µV
	V_O = ±10V, R_L = 600Ω	0.8	2.1		0.5	1.9		V/µV
Common-Mode Input Range		+13.5	+13.8		+13.5	+13.8		V
		−15	−15.3		−15	−15.3		V
Common-Mode Rejection	V_{CM} = +13.5 to −15V	100	117		97	114		dB
Power Supply Rejection	V_S = ±2 to ±18V	103	120		100	117		dB
Channel Separation	V_O = ±10V, R_L = 2kΩ	123	140		120	137		dB
Voltage Output	R_L = 2kΩ	±13	±14		±12.5	±14		V
Slew Rate		0.2	0.35		0.2	0.35		V/µs
Quiescent Current (per amplifier)			±0.35	±0.5		±0.35	±0.55	mA

V_S = +5V/0V, V_{CM} = 0V, V_O = +1.4V, T_A = +25°C unless otherwise noted.

PARAMETER	CONDITION	OPA1013AM/AC			OPA1013M/C/DN8			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage			±60	±250		±90	±450	µV
	OPA1013DN8					±250	±950	µV
Input Offset Current			±0.2	±1.3		±0.3	±2.0	nA
Input Bias Current			9	35		10	50	nA
Open-Loop Voltage Gain	V_O = 5mV to 4V		0.1			0.1		V/µV
	R_L = 500Ω							
Common-Mode Input Range		+3.5	+3.8		+3.5	+3.8		V
		0	−0.3		0	−0.3		V
Voltage Output Low	No Load		15	25		15	25	mV
Low	R_L = 600Ω to Ground		5	10		5	10	mV
Low	I_{SINK} = 1mA		200	350		200	350	mV
High	No Load	4	4.4		4	4.4		V
High	R_L = 600Ω to Ground	3.4	4		3.4	4		V
Quiescent Current (per amplifier)			0.31	0.45		0.33	0.5	mA

T_A = −55°C to +125°C, V_S = ±15V, V_{CM} = 0V unless otherwise noted.

PARAMETER	CONDITION	OPA1013AM			OPA1013M			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage			±80	±300		±110	±550	µV
	V_S = +5/0V, V_O = +1.4V							
	T_A = 100°C		±70	±450		±75	±750	µV
	V_{CM} = 0.1V, T_A = 125°C		±100	±450		±150	±750	µV
	V_{CM} = 0V, T_A = 125°C		±200	±900		±300	±1500	µV
Input Offset Voltage Drift			0.4	2.0		0.5	2.5	µV/°C
Input Offset Current			±0.3	±2.5		±0.4	±5.0	nA
	V_S = +5/0V, V_O = +1.4V		±0.6	±6		±0.9	±10	nA
Input Bias Current			7	30		9	45	nA
	V_S = +5/0V, V_O = +1.4V		11	80		15	120	nA
Open-Loop Voltage Gain	V_O = ±10V, R_L = 2kΩ	0.5	2.0		0.25	2.0		V/µV
Common-Mode Rejection	V_{CM} = +13 to −14.9V	97	114		94	113		dB
Power Supply Rejection	V_S = ±2 to ±18V	100	117		97	116		dB
Voltage Output	R_L = 2kΩ	±12	±13.8		±11.5	±13.8		V
V_O Low	V_S = +5/0V, R_L = 600Ω		6	15		6	18	mV
V_O High	V_S = +5/0V, R_L = 600Ω	3.2	3.8		3.1	3.8		V
Quiescent Current (per amplifier)			±0.38	±0.6		±0.38	±0.7	mA
	V_S = +5/0V, V_O = +1.4V		0.34	0.55		0.34	0.65	mA

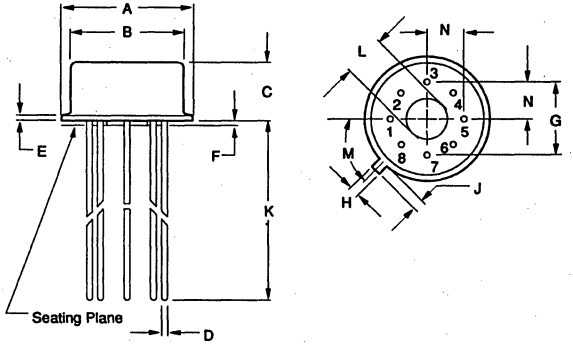
SPECIFICATIONS

T_A = 0°C to +70°C, V_S = ±15V, V_{CM} = 0V unless otherwise noted.

PARAMETER	CONDITION	OPA1013AC			OPA1013C/DN8			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage			±55	±240		±80	±400	µV
	OPA1013DN8					±230	±1000	µV
	V_S = +5/0V, V_O = +1.4V		±75	±350		±110	±570	µV
	OPA1013DN8					±280	±1200	µV
Input Offset Voltage Drift			0.3	2		0.4	2.5	µV/°C
	OPA1013DN8					0.7	5	µV/°C
Input Offset Current			±0.2	±1.5		±0.3	±2.8	nA
	V_S = +5/0V, V_O = +1.4V		±0.4	±3.5		±0.5	±6	nA
Input Bias Current			7	25		9	38	nA
	V_S = +5/0V, V_O = +1.4V		10	55		13	90	nA
Open-Loop Voltage Gain	V_O = ±10V, R_L = 2kΩ	1	2.5		0.7	2.2		V/µV
Common-Mode Rejection	V_{CM} = +13 to −15V	98	116		94	113		dB
Power Supply Rejection	V_S = ±2 to ±18V	101	119		97	116		dB
Voltage Output	R_L = 2kΩ	±12.5	±13.9		±12.0	±13.9		V
V_O Low	V_S = +5/0V, R_L = 600Ω		6	13		6	13	mV
V_O High	V_S = +5/0V, R_L = 600Ω	3.3	3.9		3.2	3.9		V
Quiescent Current (per amplifier)			±0.36	±0.55		±0.37	±0.6	mA
	V_S = +5/0V, V_O = +1.4V		0.32	0.50		0.34	0.55	mA

MECHANICAL

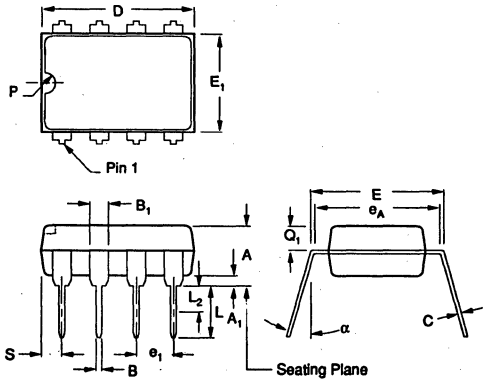
H Package — Metal TO-99



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

N8 Package — 8-Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D(1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

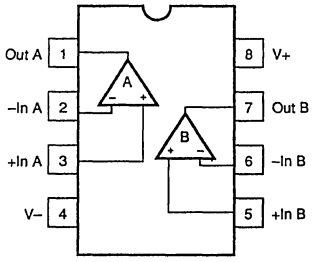
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2(2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q1	.040	.075	1.02	1.91
S(1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e1 and e_A applies in zone L_2 when unit installed.

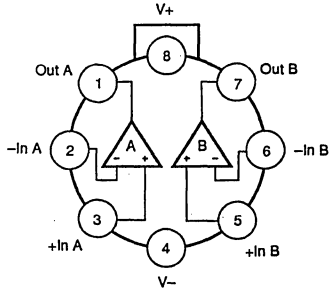
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

CONNECTION DIAGRAMS

N8 — Plastic Package — Top View



H — TO-99 Metal — Top View



ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA1013CN8	Plastic DIP	0°C to +70°C
OPA1013DN8	Plastic DIP	0°C to +70°C
OPA1013ACH	TO-99 Metal	0°C to +70°C
OPA1013CH	TO-99 Metal	0°C to +70°C
OPA1013AMH	TO-99 Metal	–55°C to +125°C
OPA1013MH	TO-99 Metal	–55°C to +125°C

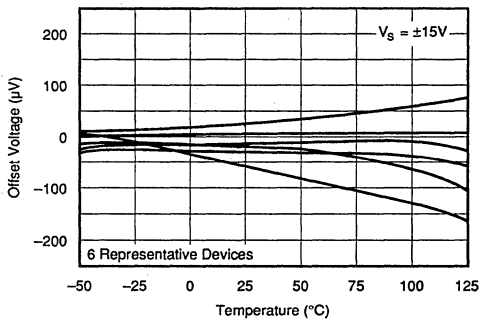
ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±22V
Differential Input Voltage	±30V
Input Voltage	V+ to (V–) –5V
Output Short Circuit (T_A = 25°C)	Continuous
Operating Temperature:	
OPA1013AM, OPA1013M	–55 to +125°C
OPA1013AC, OPA1013C, OPA1013D	0 to +70°C
Storage Temperature	–65 to +150°C
Lead Temperature (soldering, 10s)	+300°C

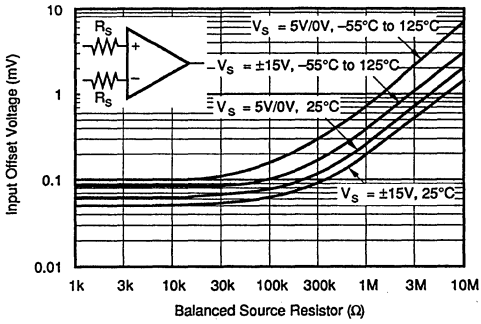
TYPICAL PERFORMANCE CURVES

T_A = +25°C unless otherwise noted.

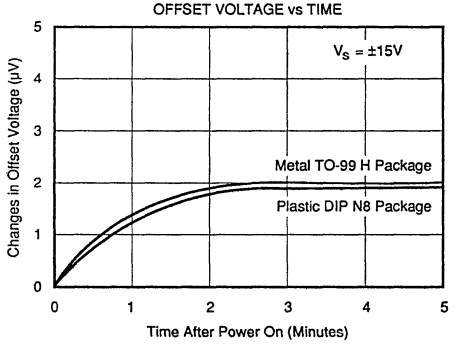
OFFSET VOLTAGE vs TEMPERATURE



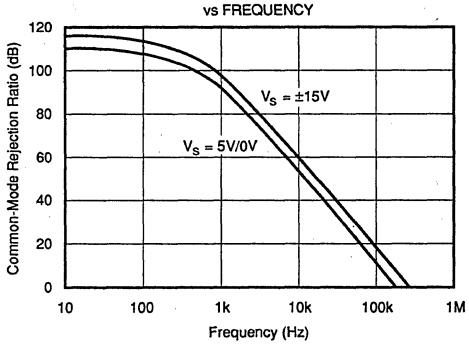
OFFSET VOLTAGE
vs BALANCED SOURCE RESISTANCE



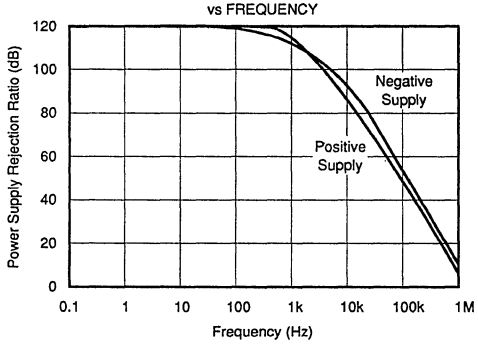
OFFSET VOLTAGE vs TIME



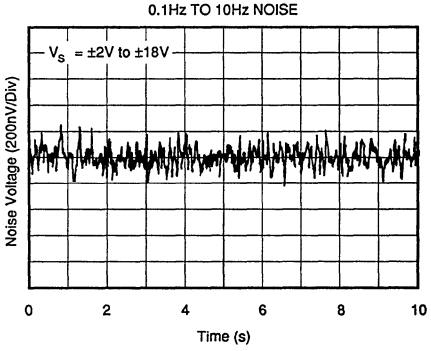
COMMON-MODE REJECTION RATIO
vs FREQUENCY



POWER SUPPLY REJECTION RATIO
vs FREQUENCY



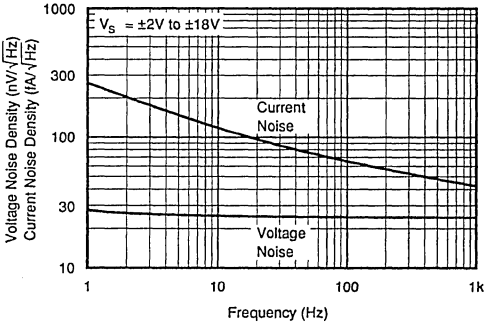
0.1Hz TO 10Hz NOISE



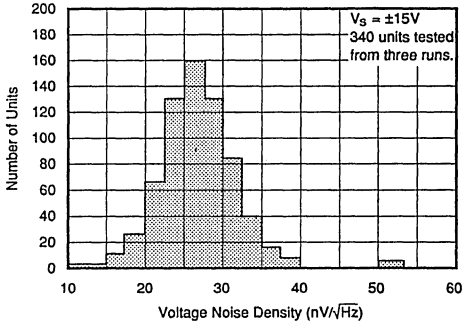
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C unless otherwise noted.

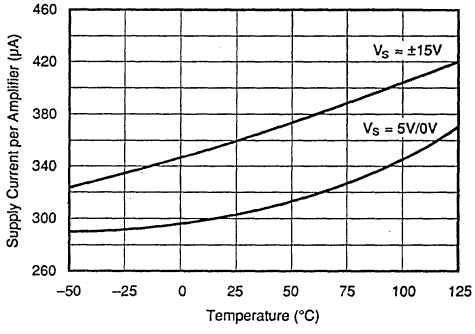
NOISE DENSITY vs FREQUENCY



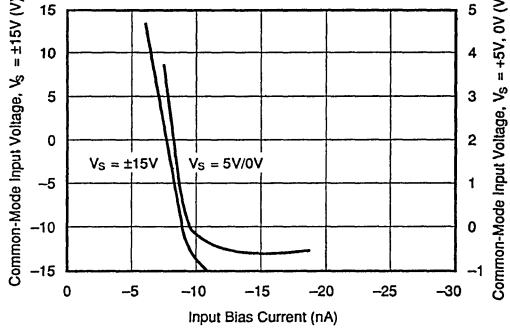
10Hz VOLTAGE NOISE DISTRIBUTION



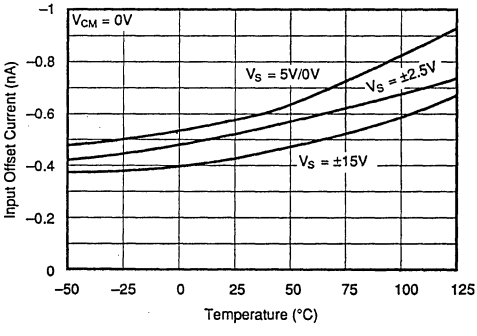
SUPPLY CURRENT vs TEMPERATURE



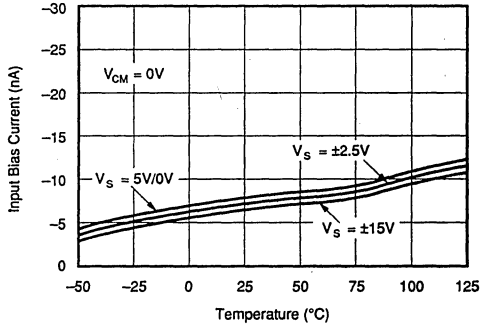
INPUT BIAS CURRENT
vs COMMON-MODE VOLTAGE



INPUT OFFSET CURRENT
vs TEMPERATURE



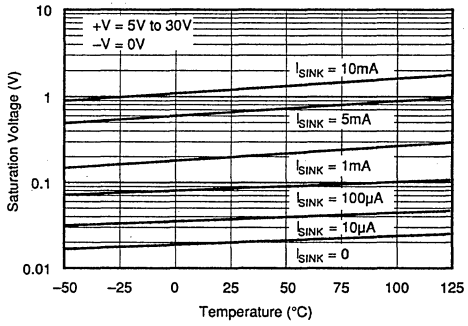
INPUT BIAS CURRENT
vs TEMPERATURE



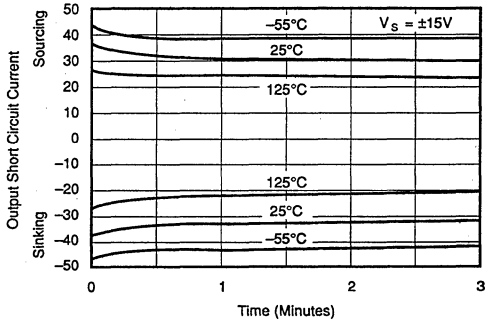
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C unless otherwise noted.

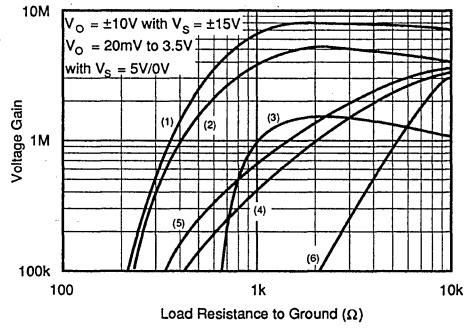
OUTPUT SATURATION AND SINK CURRENT vs TEMPERATURE



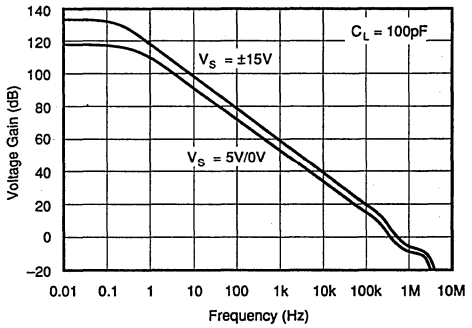
OUTPUT SHORT CIRCUIT CURRENT vs TIME



VOLTAGE GAIN vs LOAD RESISTANCE

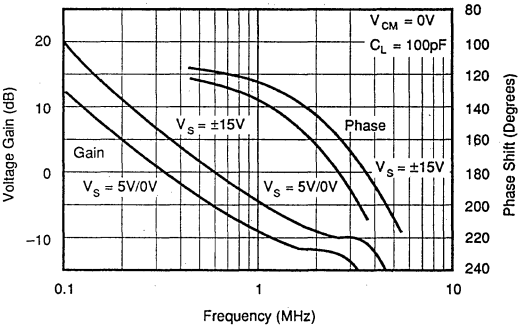


VOLTAGE GAIN vs FREQUENCY

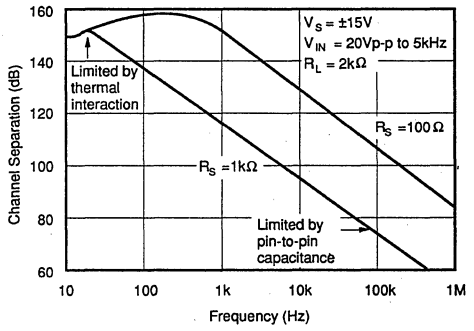


NOTES: (1) T_A = –55°C, V_S = ±15V. (2) T_A = +25°C, V_S = ±15V. (3) T_A = 125°C, V_S = ±15V. (4) T_A = +25°C, V_S = 5V/0V. (5) T_A = –55°C, V_S = 5V/0V. (6) T_A = 125°C, V_S = 5V/0V.

GAIN AND PHASE vs FREQUENCY

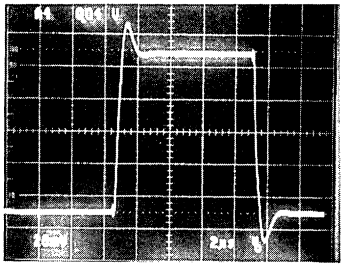


CHANNEL SEPARATION vs FREQUENCY

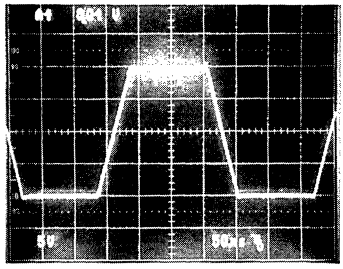


TYPICAL PERFORMANCE CURVES (CONT)

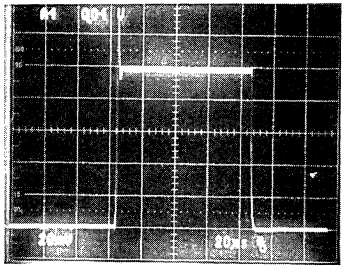
SMALL SIGNAL TRANSIENT RESPONSE
V_S = ±15V, G = +1



LARGE SIGNAL TRANSIENT RESPONSE
V_S = ±15V, G = +1

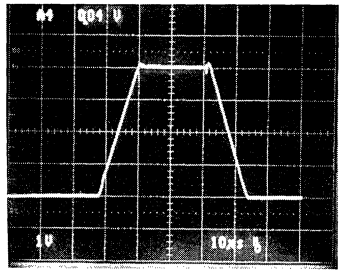


SMALL SIGNAL TRANSIENT RESPONSE
V_S = 5V/0V, G = +1, R_L = 600Ω to Ground



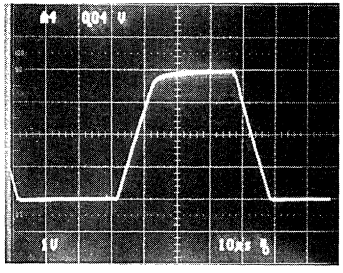
Input = 0V to 100mV Pulse

LARGE SIGNAL TRANSIENT RESPONSE
V_S = 5V/0V, G = +1, R_L = 4.7kV to 5V



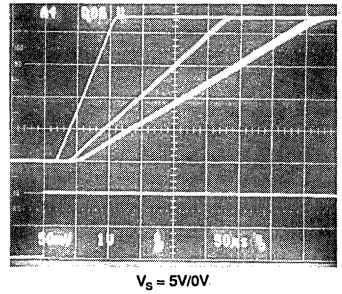
Input = 0V to 4V Pulse

LARGE SIGNAL TRANSIENT RESPONSE
V_S = 5V/0V, G = +1, No Load



Input = 0V to 4V Pulse

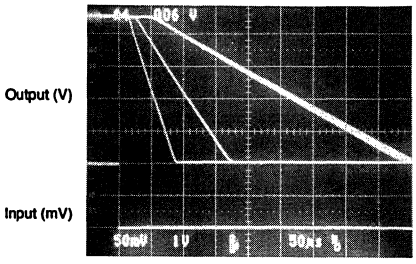
COMPARATOR RISE RESPONSE TIME
10mV, 5mV, 2mV Overdrives



V_S = 5V/0V

TYPICAL PERFORMANCE CURVES (CONT)

COMPARATOR FALL RESPONSE TIME
10mV, 5mV, 2mV Overdrives



V_S = 5V/0V

APPLICATIONS INFORMATION

The OPA1013 is unity-gain stable, making it easy to use and free from oscillations in the widest range of circuitry. Follow good design practice by bypassing the power supplies close to the op amp pins. In most cases 0.1µF ceramic capacitors are adequate.

SINGLE POWER SUPPLY OPERATION

The OPA1013 is specified for operation from a single power supply. This means that linear operation continues with the input terminals at (or even somewhat below) ground potential. When used in a non-inverting amplifier, 0V input must produce 0V output. In practice, the output swing is limited to approximately 15mV above ground with no load. Output swing near ground can be optimized when the output load is connected to ground. If the output must sink current, the ability to swing near ground will be diminished. The output swings to within approximately 200mV of ground when sinking 1mA.

INPUT PROTECTION

The circuitry of the OPA1013 is protected against overload for input voltages ranging from the positive supply voltage to 5V below the negative supply voltage (below ground in single supply operation). No external protection circuitry is required, as it is with other common single-supply op amps.

Furthermore, the OPA1013 is free from phase-reversal problems common with other single-supply op amps. When the inputs are driven below ground (or below the negative power supply), the output polarity remains correct.

COMPARATOR OPERATION

The OPA1013 functions well as a comparator, where high speed is not required. Sometimes, in fact, the low offset and docile characteristics of the OPA1013 may simplify the design of comparator circuitry. The two op amps in the OPA1013 use completely independent bias circuitry to avoid interaction when the inputs are over-driven. Driving one op amp into saturation will not affect the characteristics of the other amplifier. The outputs of the OPA1013 can drive one TTL load. Quiescent current remains stable when the inputs are overdriven.

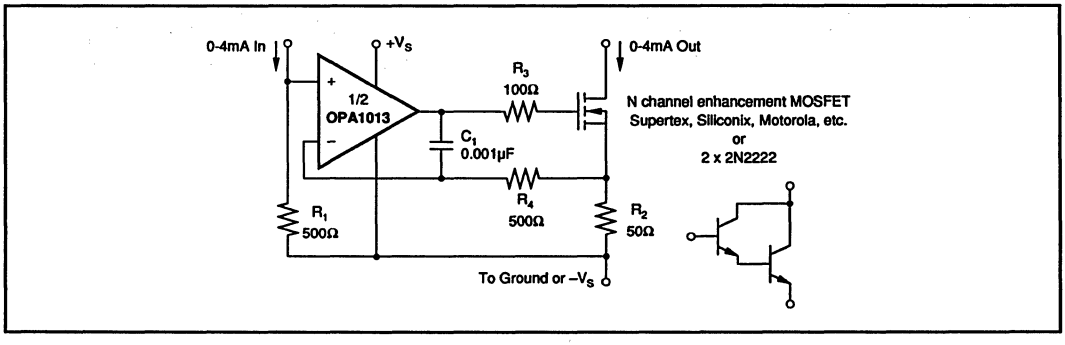


FIGURE 1. Precision Current Mirror.

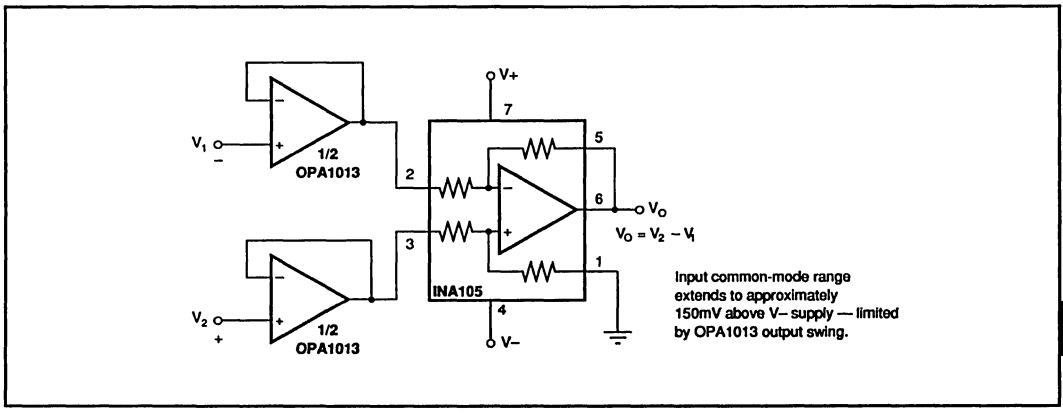


FIGURE 2. Instrumentation Amplifier.

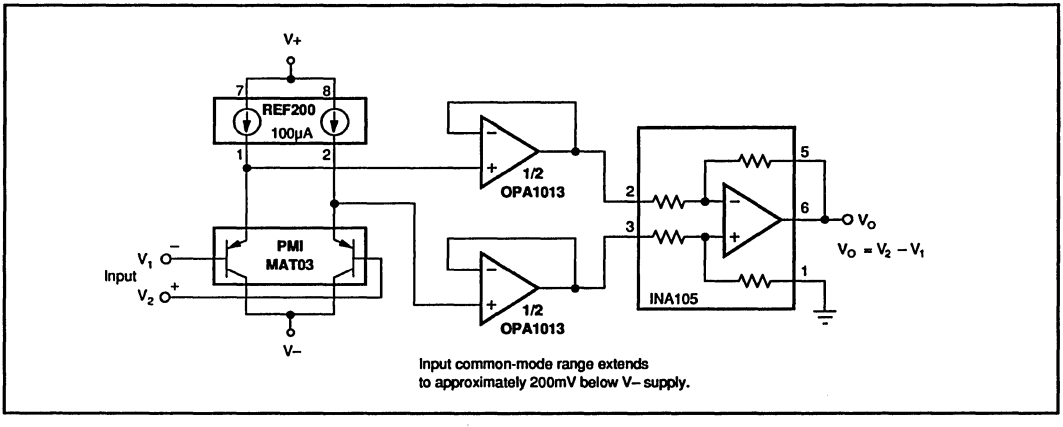


FIGURE 3. Instrumentation Amplifier.

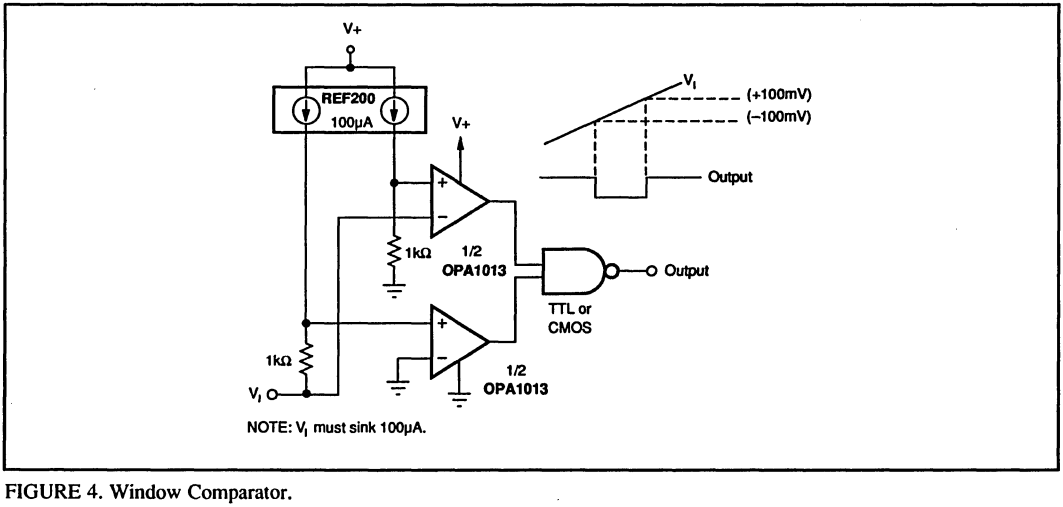
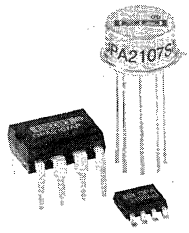


FIGURE 4. Window Comparator.

BURR-BROWN®



OPA2107

Precision Dual *Difet* ® OPERATIONAL AMPLIFIER

FEATURES

- VERY LOW NOISE: 8nV/$\sqrt{Hz}$ at 10kHz
- LOW V_{OS}: 500µV max
- LOW DRIFT: 5µV/°C max
- LOW I_B: 5pA max
- FAST SETTLING TIME: 2µs to 0.01%
- UNITY-GAIN STABLE

APPLICATIONS

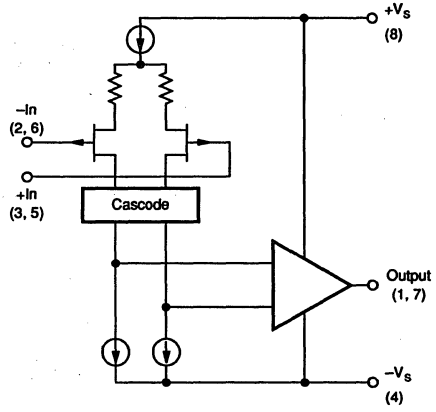
- DATA ACQUISITION
- DAC OUTPUT AMPLIFIER
- OPTOELECTRONICS
- HIGH-IMPEDANCE SENSOR AMPS
- HIGH-PERFORMANCE AUDIO CIRCUITRY
- MEDICAL EQUIPMENT, CT SCANNERS

DESCRIPTION

The OPA2107 dual operational amplifier provides precision ***Difet*** performance with the cost and space savings of a dual op amp. It is useful in a wide range of precision and low-noise analog circuitry and can be used to upgrade the performance of designs currently using BIFET® type amplifiers.

The OPA2107 is fabricated on a proprietary dielectrically isolated (***Difet***) process. This holds input bias currents to very low levels without sacrificing other important parameters, such as input offset voltage, drift and noise. Laser-trimmed input circuitry yields excellent DC performance. Superior dynamic performance is achieved, yet quiescent current is held to under 2.5mA per amplifier. The OPA2107 is unity-gain stable.

The OPA2107 is available in plastic DIP, metal TO-99, and SOIC packages. Industrial and Military temperature range versions are available.



Difet® Burr-Brown Corp.
BIFET® National Semiconductor

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-863A

SPECIFICATIONS

T_A = +25°C, V_S = ±15V unless otherwise noted.

PARAMETER	CONDITION	OPA2107AM, SM, AP, AU			OPA2107BM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE[1]								
Input Offset Voltage	V_{CM} = 0V		100	1mV		50	500	µV
Over Specified Temperature			0.5	2		0.2	1	mV
SM Grade			0.8	2.5				mV
Average Drift Over Specified Temperature			3	10		2	5	µV/°C
Power Supply Rejection	V_S = ±10 to ±18V	80	96		84	100		dB
INPUT BIAS CURRENT[1]								
Input Bias Current	V_{CM} = 0V		4	10		2	5	pA
Over Specified Temperature			0.25	1.5		0.15	1	nA
SM Grade			4	35				nA
Input Offset Current	V_{CM} = 0V		1	8		0.5	3	pA
Over Specified Temperature				1			0.5	nA
SM Grade			1	28				nA
INPUT NOISE								
Voltage: f = 10Hz	R_S = 0		30			*		nV/√Hz
f = 100Hz			12			*		nV/√Hz
f = 1kHz			9			*		nV/√Hz
f = 10kHz			8			*		nV/√Hz
BW = 0.1 to 10Hz			1.2			*		µVp-p
BW = 10 to 10kHz			0.85			*		µVrms
Current: f = 0.1Hz thru 20kHz			1.2			0.9		fA/√Hz
BW = 0.1Hz to 10Hz			23			17		fAp-p
INPUT IMPEDANCE								
Differential			10^{13} || 2			*		Ω || pF
Common-Mode			10^{14} || 4			*		Ω || pF
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±10.5	±11		*	*		V
Over Specified Temperature		±10.2	±10.5		*	*		V
SM Grade		±10	±10.3					V
Common-Mode Rejection	V_{CM} = ±10V	80	94		84	100		dB
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = ±10V, R_L = 2kΩ	82	96		84	100		dB
Over Specified Temperature		80	94		82	96		dB
SM Grade		80	92					dB
DYNAMIC RESPONSE								
Slew Rate	G = +1	13	18		*	*		V/µs
Settling Time: 0.1%	G = −1, 10V Step		1.5			*		µs
0.01%			2			*		µs
Gain-Bandwidth Product	G = 100		4.5			*		MHz
THD + Noise	G = +1, f = 1kHz		0.001			*		%
Channel Separation	f = 100Hz, R_L = 2kΩ		120			*		dB
POWER SUPPLY								
Specified Operating Voltage			±15			*		V
Operating Voltage Range		±4.5		±18	*		*	V
Current			±4.5	±5		*	*	mA
OUTPUT								
Voltage Output	R_L = 2kΩ	±11	±12		*	*		V
Over Specified Temperature		±10.5	±11.5		*	*		V
SM Grade		±10.2	±11.3					V
Short Circuit Current		±10	±40		*	*		mA
Output Resistance, Open-Loop	1MHz		70			*		Ω
Capacitive Load Stability	G = +1		1000			*		pF
TEMPERATURE RANGE								
Specification								
AP, AU, AM, BM		−25		+85	*		*	°C
SM		−55		+125				°C
Operating								
AP, AU		−25		+85				°C
AM, BM, SM		−55		+125	*		*	°C
Storage								
AP, AU		−40		+125				°C
AM, BM, SM		−65		+150	*		*	°C
Thermal Resistance (θ_{J-A})								
AP			90					°C/W
AU			175					°C/W
AM, BM, SM			200			*		°C/W

* Specifications same as OPA2107AM.

NOTE: (1) Specified with devices fully warmed up.

ORDERING INFORMATION

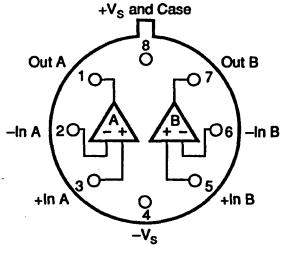
MODELS	PACKAGE	SPECIFICATION TEMPERATURE RANGE
OPA2107AP	Plastic DIP	–25 to +85°C
OPA2107AM	Metal TO-99	–25 to +85°C
OPA2107BM	Metal TO-99	–25 to +85°C
OPA2107SM	Metal TO-99	–55 to +125°C
OPA2107AU	SO-8 SOIC	–25 to +85°C

ABSOLUTE MAXIMUM RATINGS

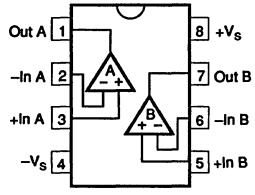
Supply Voltage ..... ±18V
Input Voltage Range ..... $\pm V_S$ ±2V
Differential Input Voltage ..... Total V_S ±4V
Operating Temperature
  M Package ..... –55°C to +125°C
  P and U Packages ..... –25°C to + 85°C
Storage Temperature
  M Package ..... –65°C to +150°C
  P and U Packages ..... –40°C to +125°C
Output Short Circuit to Ground (T_A = +25°C) ..... Continuous
Junction Temperature ..... +175°C
Lead Temperature
  M and P Packages (soldering, 10s) ..... +300°C
  U Package, SOIC (3s) ..... +260°C

PIN CONFIGURATIONS

Top View – M Package

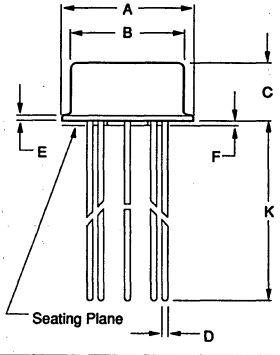


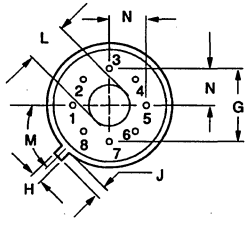
Top View – P & U Packages



MECHANICAL

M Package — Metal TO-99



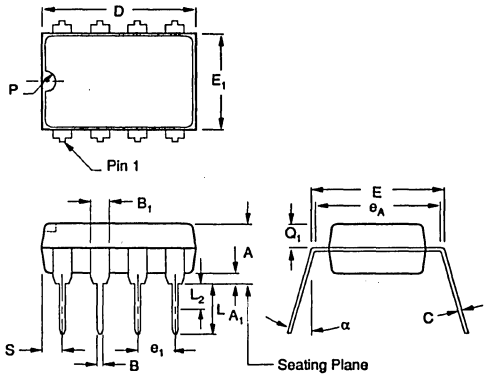


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

MECHANICAL (CONT)

P Package — 8-Pin Plastic DIP

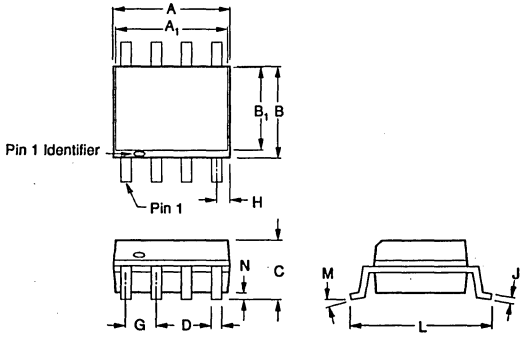


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D (1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2(2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q1	.040	.075	1.02	1.91
S (1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e_1 and e_A apply in zone L_2 when unit installed.
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

U Package — 8-Pin SOIC



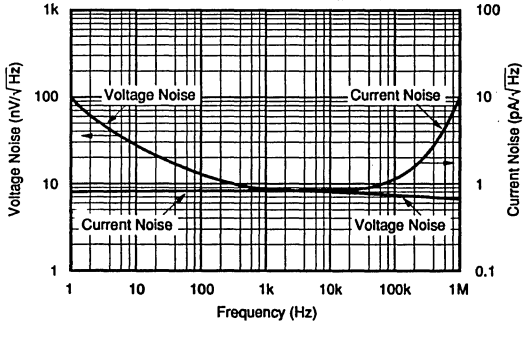
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.201	4.70	5.11
A1	.178	.201	4.52	5.11
B	.146	.162	3.71	4.11
B1	.130	.149	3.30	3.78
C	.054	.145	1.37	3.69
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.018	.026	0.46	0.66
J	.008	.012	0.20	0.30
L	.220	.252	5.59	6.40
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

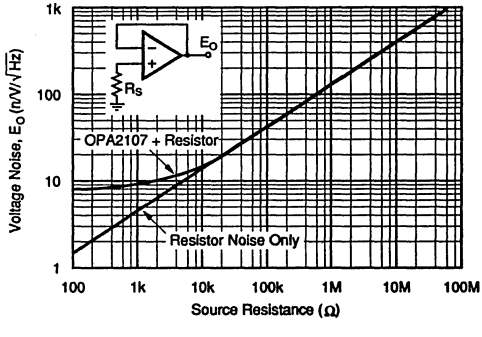
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



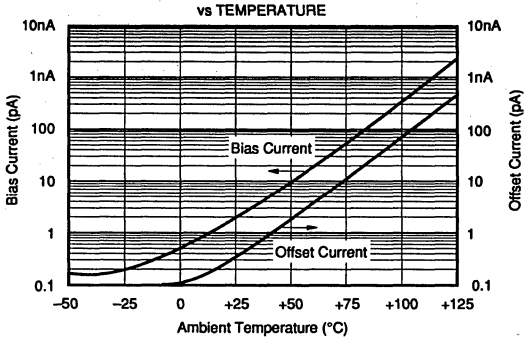
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY at 1kHz vs SOURCE RESISTANCE



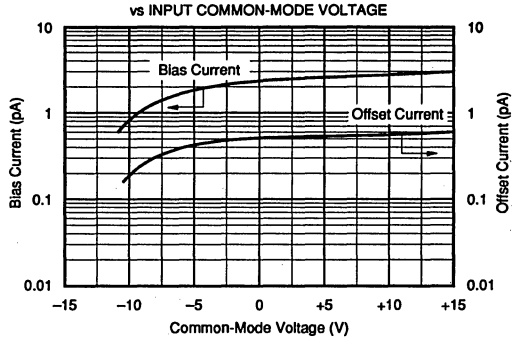
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

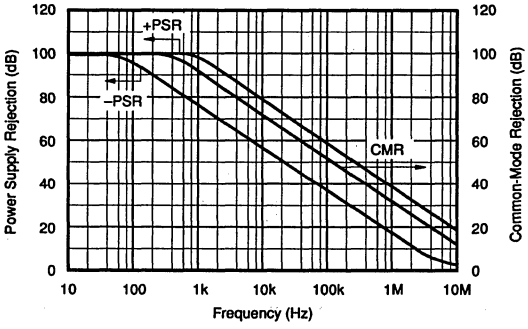
BIAS AND OFFSET CURRENT vs TEMPERATURE



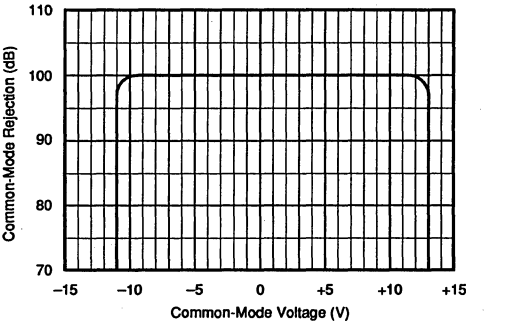
BIAS AND OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



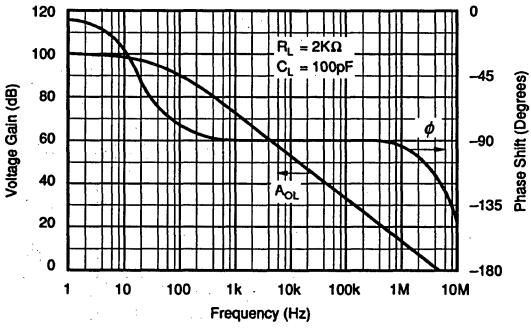
POWER SUPPLY AND COMMON-MODE REJECTION vs FREQUENCY



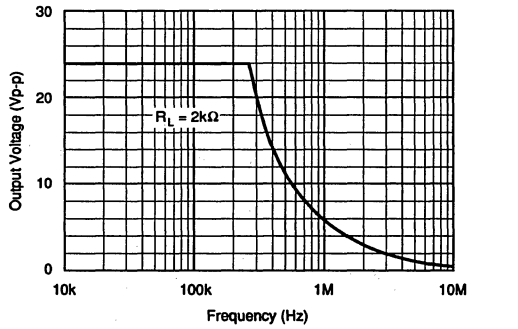
COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



OPEN-LOOP FREQUENCY RESPONSE



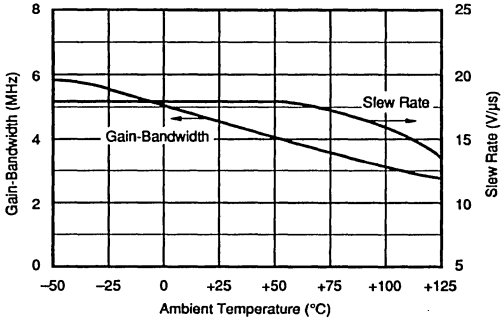
MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



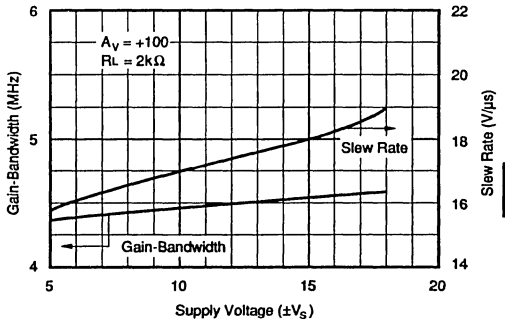
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

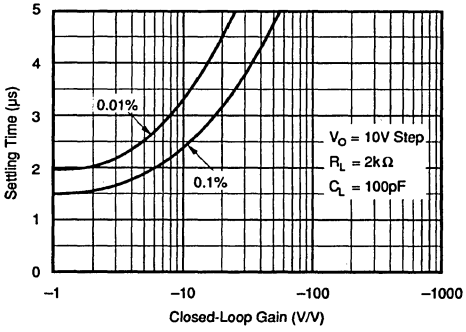
GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



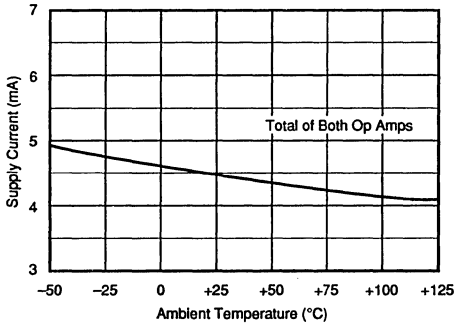
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



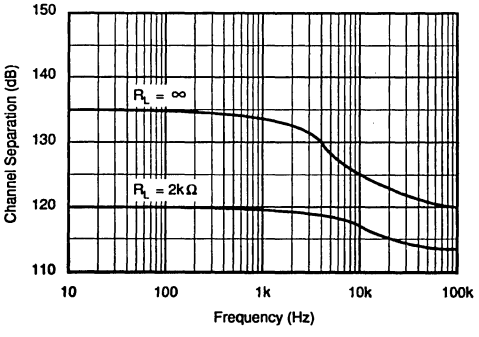
SETTLING TIME vs CLOSED-LOOP GAIN



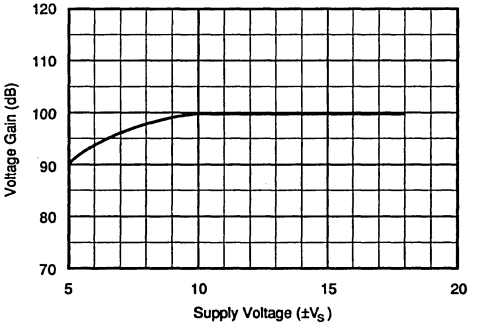
SUPPLY CURRENT vs TEMPERATURE



CHANNEL SEPARATION vs FREQUENCY



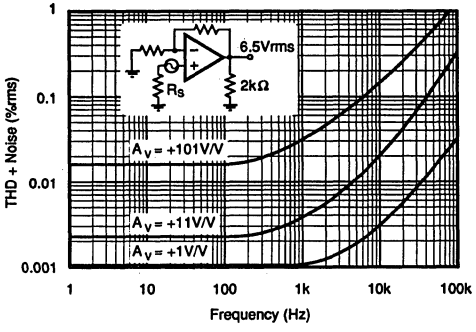
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



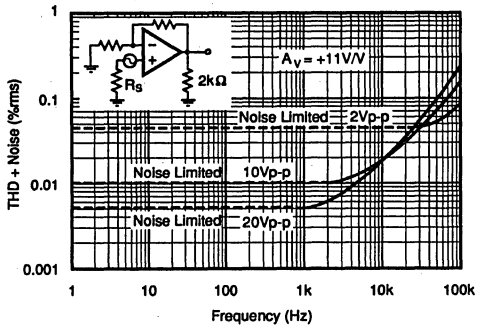
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

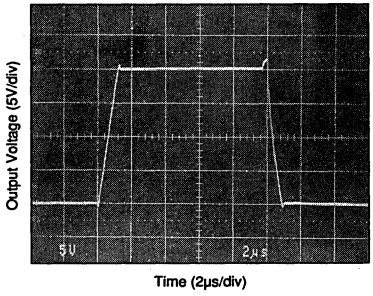
TOTAL HARMONIC DISTORTION vs FREQUENCY



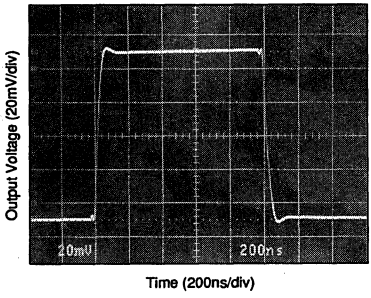
THD + NOISE vs FREQUENCY AND OUTPUT VOLTAGE



OPA2107 LARGE-SIGNAL RESPONSE



OPA2107 SMALL-SIGNAL RESPONSE



APPLICATIONS INFORMATION AND CIRCUITS

The OPA2107 is unity-gain stable and has excellent phase margin. This makes it easy to use in a wide variety of applications.

Power supply connections should be bypassed with capacitors positioned close to the amplifier pins. In most cases, 0.1µF ceramic capacitors are adequate. Applications with larger load currents and fast transient signals may need up to 1µF tantalum bypass capacitors.

INPUT BIAS CURRENT

The OPA2107's ***Difet*** input stages have very low input bias current—an order of magnitude lower than BIFET op amps. Circuit board leakage paths can significantly degrade performance. This is especially evident with the SO-8 surface-mount package where pin-to-pin dimensions are particularly small. Residual soldering flux, dirt, and oils, which conduct leakage current, can be removed by proper cleaning. In most instances a two-step cleaning process is adequate using a clean organic solvent rinse followed by de-ionized water. Each rinse should be followed by a 30-minute bake at 85°C.

A circuit board guard pattern effectively reduces errors due to circuit board leakage (Figure 1). By encircling critical high impedance nodes with a low impedance connection at the same circuit potential, any leakage currents will flow harmlessly to the low impedance node. Guard traces should be placed on all levels of a multiple-layer circuit board.

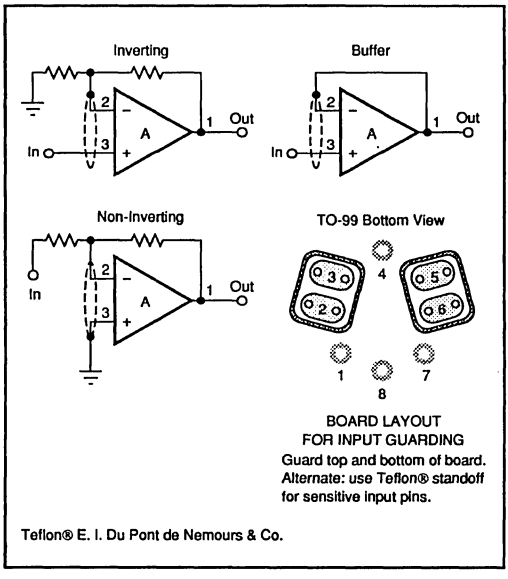


FIGURE 1. Connection of Input Guard.

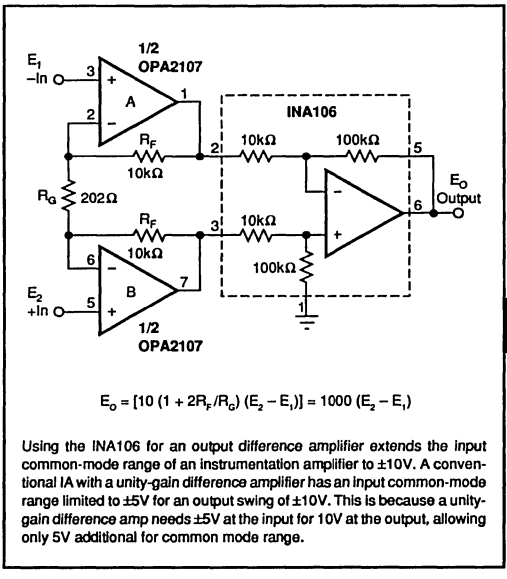


FIGURE 3. Precision Instrumentation Amplifier.

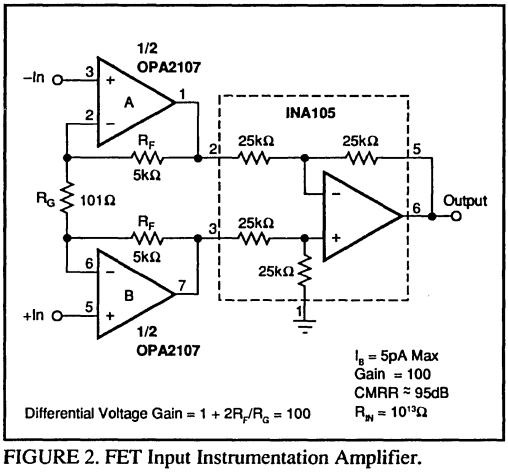
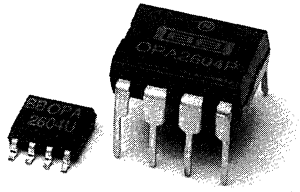


FIGURE 2. FET Input Instrumentation Amplifier.

BURR-BROWN®



OPA2604

ADVANCE INFORMATION
SUBJECT TO CHANGE

Dual FET-Input, Audio OPERATIONAL AMPLIFIER

FEATURES

- LOW DISTORTION: 0.0003% at 1kHz
- LOW NOISE: 10nV/√Hz
- HIGH SLEW RATE: 25V/µs
- WIDE GAIN-BANDWIDTH: 10MHz
- UNITY-GAIN STABLE
- WIDE POWER SUPPLY RANGE: V_S = ±4.5 to ±24V
- DRIVES 600Ω LOADS

APPLICATIONS

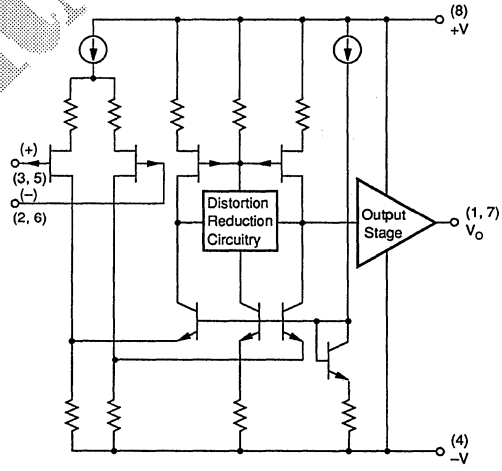
- PROFESSIONAL AUDIO EQUIPMENT
- PCM DAC I/V CONVERTER
- SPECTRAL ANALYSIS EQUIPMENT
- ACTIVE FILTERS
- TRANSDUCER AMPLIFIER
- DATA ACQUISITION

DESCRIPTION

The OPA2604 is a dual, FET-input operational amplifier designed for enhanced AC performance. Very low distortion, low noise and wide bandwidth provides superior performance in high performance audio and precision instrumentation.

New circuit techniques and special laser trimming of dynamic circuit performance yield very low harmonic distortion. The result is an op amp with exceptional sound quality. The low-noise FET input of the OPA2604 provides wide dynamic range, even with high source impedance. Offset voltage is laser-trimmed to provide excellent DC stability.

The OPA2604 is available in 8-pin plastic mini-DIP and SO-8 surface-mount packages, specified for the –25°C to +85°C temperature range.



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PDS-1069

SPECIFICATIONS

T_A = +25°C, V_S = ±15V unless otherwise noted.

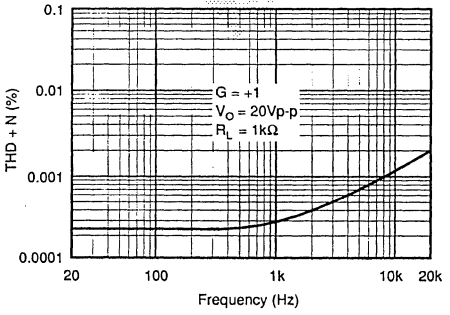
PARAMETER	CONDITION	OPA2604AP, AU MIN	OPA2604AP, AU TYP	OPA2604AP, AU MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage			±0.1	±2	mV
Average Drift			±5		µV/°C
Power Supply Rejection	V_S = ±5 to ±18V	80	92		dB
INPUT BIAS CURRENT[1]					
Input Bias Current	V_{CM} = 0V		25	100	pA
Input Offset Current	V_{CM} = 0V		±10		pA
NOISE					
Input Voltage Noise					
Noise Density: f = 10Hz			30		nV/$\sqrt{Hz}$
f = 100Hz			15		nV/$\sqrt{Hz}$
f = 1kHz			11		nV/$\sqrt{Hz}$
f = 10kHz			10		nV/$\sqrt{Hz}$
Voltage Noise, BW = 20Hz to 20kHz			1.5		µVp-p
Input Bias Current Noise					
Current Noise Density, f = 0.1Hz to 20kHz			3		fA/$\sqrt{Hz}$
INPUT VOLTAGE RANGE					
Common-mode Input Range		±12	±13		V
Common-mode Rejection	V_{CM} = ±12V	80	100		dB
Differential			10^{12} || 8		Ω || pF
Common-Mode			10^{12} || 10		Ω || pF
OPEN-LOOP GAIN					
Open-loop Voltage Gain	V_O = ±10V, R_L = 1kΩ	80	100		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product	G = 10		10		MHz
Slew Rate	20Vp-p, R_L = 1kΩ	15	25		V/µs
Settling Time 0.01%	G = –1, 10V Step		2		µs
0.1%	G = –1, 10V Step		1		µs
Total Harmonic Distortion + Noise (THD + N)	G = 1, f = 1kHz V_O = 20Vp-p, R_L = 1kΩ		0.0003		%
OUTPUT					
Voltage Output	R_L = 600Ω	±11	±12		V
Current Output	V_O = ±12V		±20		mA
Short Circuit Current			±50		mA
Output Resistance, Open-Loop			100		Ω
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±4.5		±24	V
Current, Total Both Amplifiers			±9.5	±11	mA
TEMPERATURE RANGE					
Specification		–25		+85	°C
Storage		–40		+125	°C
Thermal Resistance, θ_{J-A}			90		°C/W

NOTES: (1) High-speed test at T_J = 25°C.

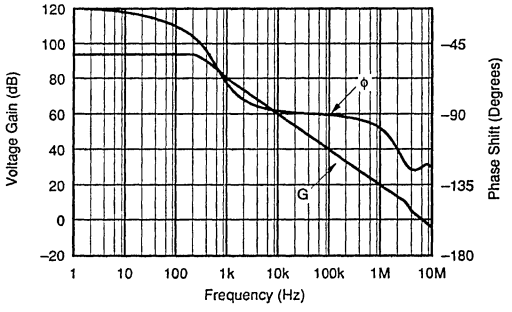
TYPICAL PERFORMANCE CURVES

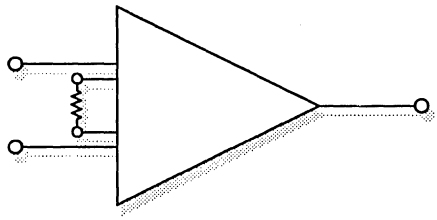
T_A = +25°C, V_S = ±15V unless otherwise noted.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



OPEN-LOOP GAIN/PHASE vs FREQUENCY





INSTRUMENTATION AMPLIFIERS

3

WHAT IS AN INSTRUMENTATION AMPLIFIER?

An instrumentation amplifier is a closed-loop, differential input, gain block. It is a committed circuit with the primary function of accurately amplifying the voltage applied to its inputs.

Ideally, the instrumentation amplifier responds only to the difference between the two input signals and exhibits extremely high impedance between the two input terminals, and from each terminal to ground. The output voltage is developed single-ended with respect to ground and is equal to the product of amplifier gain and the difference of the two input voltages. See Figure 1.

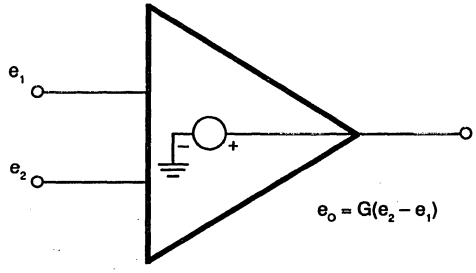


Figure 1. Idealized Model of an Instrumentation Amplifier.

Amplifier gain (G) is normally set by the user with a single external resistor. The properties of this model may be summarized as infinite input impedance, zero output impedance, the output voltage proportional to only the difference voltage ($e_2 - e_1$), a precisely known gain constant (G) (implying no nonlinearity), and unlimited bandwidth. This amplifier would completely

reject signal components common to both inputs (common-mode rejection) and would exhibit no DC offset voltage or drift.

CHARACTERISTICS OF INSTRUMENTATION AMPLIFIERS

It is desirable to achieve, as close as possible, the characteristics of the ideal instrumentation amplifier. The following paragraphs are a discussion of the other-than-ideal characteristics of instrumentation amplifiers.

INPUT IMPEDANCE

A simple model of a realistic instrumentation amplifier is shown in Figure 2. The impedance Z_{ID} represents the differential input impedance. The common-mode input impedance Z_{ICM} is represented as two equal components, $2Z_{ICM}$, from each input to ground. These finite resistances contribute an effective gain error due to loading of the source resistance. The instrumentation amplifier provides a load on the source of $Z_I = Z_{ID} \| Z_{ICM}$. If source impedance is $R_S = R_{S1} + R_{S2}$, the gain error caused by this loading is:

$$\text{Gain Error} = 1 - \frac{Z_I}{Z_I + R_S} = \frac{R_S}{Z_I + R_S} \cong \frac{R_S}{Z_I} \quad \text{if } Z_I >> R_S$$

If R_s is 10kΩ and Z_I is 10MΩ,

$$\text{Gain Error} \cong \frac{10 \times 10^3}{10 \times 10^6} = 0.1\%$$

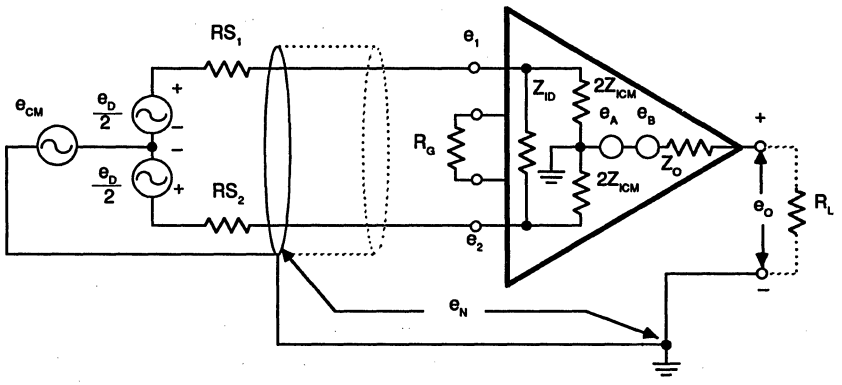


Figure 2. Simple Model of an Instrumentation Amplifier Shown in a Typical Application Configuration.

The DC common-mode input impedance Z_{ICM} will be independent of gain. The DC differential input impedance Z_{ID} may vary as a function of gain. Specifications give the worst-case value. The nonzero output impedance of the amplifier will also create a gain error, the value of which depends on the load resistance.

NONLINEARITY

The linearity of gain is possibly of more importance than the gain accuracy, since the value of the gain can be adjusted to compensate for simple gain errors. The nonlinearity is specified to be the peak deviation from a "best fit" straight line, expressed as a percent of peak-to-peak full scale output.

COMMON-MODE REJECTION

As illustrated in Figure 2, the output voltage has two components. One component is proportional to the differential input voltage $e_D = (e_2 - e_1)$. The second component is proportional to the common-mode input voltage. The common-mode voltage which appears at the amplifier's input terminals is defined as $e_{CM} = e_2 + e_1/2$. This may consist of some common-mode voltage in the source itself, e_{CM}, (such as bridge excitation) plus any noise voltage, e_N, between the source common and the amplifier common. As shown in Figure 2, the constant G represents the differential amplifier gain factor (fixed by the external gain-setting resistor). The constant (G/CMRR) represents the common-mode signal gain of the amplifier. The CMRR (common-mode rejection ratio) is the ratio of differential gain to common-mode gain. Thus CMRR is proportional to the differential gain and CMRR increases as the differential gain (G) increases. Hence, CMRR is usually specified for the maximum and the minimum values of gain of the amplifier. The common-mode rejection may be expressed in dB as CMRR (dB) = $20\log_{10}$ CMRR.

For an ideal instrumentation amplifier, the output voltage component due to common-mode voltage should be zero. For a realistic instrumentation amplifier, the CMRR — though very high — is still not infinite and so will cause an error voltage of e_{CM}/CMRR x G to appear at the output.

SOURCE IMPEDANCE UNBALANCE

If the source impedances are unbalanced, the source voltages ($e_{CM} + e_N$) are divided unequally upon the common-mode impedance, and a differential signal is developed at the amplifier's input. This error signal cannot be separated from the desired signal. In the circuit in Figure 2, if $R_{S2} = 0$, $R_{S1} = 1k\Omega$, $e_{CM} + e_N = 10V$, and $Z_{CM} = 100M\Omega$, then the effect of unbalance is to generate a voltage:

$$e_2 - e_1 = 10V - 10V\frac{10^8}{10^8 + 10^3} = 10V\frac{10^3}{10^8 + 10^3} \cong \frac{10V}{10^5} = 0.1mV$$

If e_D full scale is 10mV, then this error is

$$\text{Error} = \frac{0.1\,\text{mV}}{10\text{mV}} = 1\% \text{ of full scale}$$

OFFSET VOLTAGE AND DRIFT

Most instrumentation amplifiers are two-stage devices—they have a variable gain input stage and a fixed gain output stage. If V_I and V_O are the offset voltages of the input and output stages respectively, then the amplifier's total offset voltage referred to the input (RTI) = $V_I + V_O/G$, where G is the amplifier's gain. (Note that total E_{OS} (RTI) x G appears at the output.)

The initial offset voltage is usually adjustable to zero. Therefore voltage drift is the more significant term because it cannot be nulled. The offset voltage drift also has two components—one due to the input stage of the amplifier and the other due to the output stage. When the amplifier is operated at high gain, the drift of the input stage dominates. At low values of gain, the drift of the output stage will be the major component of drift. When the total output drift is referred to the input, the effective input voltage drift is largest for low values of gain. Output voltage drift will always be lowest at low gains. If $\Delta V_I/\Delta T = 2\mu V/°C$ and $\Delta V_O/\Delta T = 500\mu V/°C$ and the amplifier in a gain of 1000V/V is nulled at 25°C, then at 65°C the offset voltage will be

$$\begin{aligned} E_{OS}(\text{RTI})\ 65° &= 40°C[2\mu V/°C + (500\mu V/°C/1000V/V)] \\ &= 40°C(2.5\mu V/°C) = 100\mu V = 0.1\text{mV} \end{aligned}$$

If the full scale input is 10mV, then the error due to voltage drift is

$$\text{Error} = \frac{0.1\,\text{mV}}{10\text{mV}} = 1\% \text{ of full scale}$$

INPUT BIAS AND OFFSET CURRENTS

The input bias currents are the currents that flow out of (or into) either of the two inputs of the amplifier. They are the base currents for bipolar input stages and the leakage currents for JFET input stages. Offset current is the difference of the two bias currents.

The bias currents flowing into the source resistances will generate offset voltages of $E_{OS2} = I_{B2} \times R_{S2}$ and $E_{OS1} = I_{B1} \times R_{S1}$. If $R_{S1} = R_{S2} = R_S/2$, the offset voltage at the input is $E_{OS2} - E_{OS1} = I_{OS} \times R_S/2$. This input-referred offset error may be compared directly with the input voltage to compute percent error. (Note that the source must be returned to power supply common, or R_S will be infinite and the amplifier will saturate.)

APPLICATIONS OF INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are generally used in applications where extracting and accurately amplifying low level differential signals riding on high common-mode voltages (±10V) is very important. Such applications require high input impedance, high CMRR, low input noise, and excellent DC level stability (low offset voltage drift).

Instrumentation amplifiers are used as transducer amplifiers for various types of transducers such as strain gauge bridges, load cells, thermistor networks, thermocouples, current shunts, biological probes, weather gauges, and so forth. Other applications include recorder preamplifiers, multiplexer buffers, servo error amplifiers, current sensors, signal conditioners in process control and data acquisition systems, and in general measurements of small differential signals riding on common-mode voltages.

The small size, low cost, and high performance of these amplifiers offer an attractive approach for data acquisition applications: assigning a fixed-gain amplifier to each transducer and locating the amplifier physically near the transducer. This approach largely eliminates common-mode noise pickup problems since a high level signal (rather than a low level transducer signal) is then transmitted to the data gathering station. The result is a higher signal/noise ratio at the output. Using one amplifier per point may well be more economical, as well as offering better performance and flexibility, than the approach of using low level multiplexers.

INSTRUMENTATION AMPLIFIERS SELECTION GUIDES

The following Selection Guides show parameters for the high grade. Refer to the Product Data Sheet for a full selection of grades. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book.*

INSTRUMENTATION AMPLIFIERS — **Boldface = NEW**

Description	Model	Gain Range	Gain Accuracy, G=100 25°C, max(%)	Gain Drift, G=100 (ppm/°C)	Non-Linearity G=100 max(%)	Input Parameters CMR[6] min(dB)	Input Parameters Offset Voltage vs Temp max(µV/°C)	Dynamic Response, G=100 ±3dB BW (kHz)	Temp Range[1]	Pkg	Page No.
Very High Accuracy	**INA120**	**1, 10, 100, 1000**	**0.5**	**30**	**±0.01**	**96**	**±(0.25±10/G)**	**20**	**Ind**	**DIP**	**S3-50**
	INA104M	1-1000[2]	0.15	22[3]	±0.003	96	±(0.25±10/G)	25	Ind	DIP	3-34
	INA101G, M, L	1-1000[2]	0.03	22[3]	±0.003	96	±(0.25±10/G)	25	Ind, Mil	DIP	3-11
										TO-100,	3-11
										LCC	3-11
	INA101P, U	1-1000[2]	0.3	22[3]	±0.007	90	±(2±20/G) typ	25	Com	DIP	3-11
										SOIC	3-11
Low Quiescent Power	**INA102G[8], L[8]**	**1,10,100, 1000**	**0.15**	**15**	**±0.02**	**90**	**±(2±5/G)**	**3**	**Ind**	**DIP**	**S3-10**
										LCC	**S3-10**
	INA102P, U	**1,10,100, 1000**	**0.4**	**20**	**±0.05**	**80**	**±(5±10/G)**	**3**	**Com, Ind**	**DIP**	**S3-10**
										SOIC	**S3-10**
Low Noise, Low Distortion	**INA103G**	**1-1000[2]**	**0.1**	**25**	**±0.004**	**100**	**±(0.5+10/G) typ**	**800**	**Ind**	**DIP**	**S3-22**
	INA103P	**1-1000[2]**	**0.25**	**25**	**±0.010**	**90**	**±(0.5+20/G) typ**	**800**	**Com**	**DIP**	**S3-22**
Fast Settling FET Input	INA110G[8], L[8]	1,10,100, 200,500	0.1	20	±0.01	96	±(2±50/G)	470	Ind	DIP,	3-65
										LCC	3-65
	INA110P, U	1,10,100, 200, 500	0.2	6 typ	±0.02	87	±(2±20/G) typ	470	Com	DIP,	3-65
										SOIC	3-65
Buffer, Unity-Gain Difference	3627M	1V/V,fixed	0.01[3]	5	±0.001[3]	100	20	800[3]	Ind	TO-99	3-158
	INA105M[8], L[8]	1V/V,fixed	0.01[3]	5	±0.001[3]	86[5]	10	1000[3]	Ind	TO-99	3-45
	INA105P, U	1V/V,fixed	0.025[3]	5	±0.001[3]	72[5]	5 typ	1000[3]	Com	DIP,	3-45
										SOIC	3-45
Gain of 10 Difference	INA106M	10V/V,fixed	0.01[4]	10	±0.001[4]	100[5]	2	500[4]	Ind	TO-99	3-57
	INA106P	10V/V,fixed	0.025[4]	4 typ	±0.001[4]	86[5]	0.2 typ	500[4]	Com	DIP	3-57
High Com. Mode Volt. Difference (200VDC CMV)	**INA117G**	**1V/V,fixed**	**0.02[3]**	**10[3]**	**±0.001[3]**	**86[5]**	**20**	**200[3]**	**Ind**	**DIP**	**S3-36**
	INA117P	**1V/V,fixed**	**0.05[3]**	**10[3]**	**±0.001[3]**	**74[5]**	**40**	**200[3]**	**Com**	**DIP**	**S3-36**
4-20mA Loop Receiver	**RCV420BG**	**0.3125V/mA**	**0.05**	**25**	**±0.002**	**86**	**25[7]**	**150**	**Ind**	**DIP**	**S3-71**
	RCV420KP	**0.3125V/mA**	**0.1**	**50**	**±0.002**	**72**	**50[7]**	**150**	**Com**	**DIP**	**S3-71**

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) Set with external resistor. (3) Unity-gain. (4) Gain = 10. (5) No source imbalance. (6) DC to 60Hz, Gain = 10, 1kΩ unbalanced. (7) RTO. (8) BS 9000 Screening is available.

PROGRAMMABLE GAIN AMPLIFIERS

Description	Model	Gain Range	Gain Accuracy, G=100 25°C, max(%)	Gain Drift, G=100 (ppm/°C)	Non-Linearity G=100 max(%)	Input Parameters CMR[6] min (dB)	Input Parameters Offset Voltage vs Temp max (µV/°C)	Dynamic Response, G=100 ±3dB BW (kHz)	Temp Range[1]	Pkg	Page No.
Noninverting Input	PGA100G	Gain set word 1, 2, 4, 8...128	0.02	10	±0.005	NA	6 typ	5MHz	Ind	DIP	3-85
	PGA102G	Gain set	0.01	20	±0.01		3,G=100	250	Ind	DIP	3-93
	PGA102P	with 2-bit 100	0.02	50	±0.01		3,G=100	250	Com	DIP	3-93
Instr. Amplifier Input	PGA200G	Gain set word 1, 10, 100, 1000	0.02	10	±0.003	96	0.4,G=100	30	Ind	DIP	3-103
Fast Settling 2µs to 0.01%	**PGA202**	**Gain set word 1, 10, 100, 1000**	**0.15**	**5**	**±0.012**	**86**	**±(3+25/G)**	**1000**	**Ind, Com**	**DIP**	**S3-60**
Differential	**PGA203**	**Gain set word 1, 2, 4, 8**	**0.15**	**5**	**±0.012**	**86**	**±(3+25/G)**	**1000**	**Ind, Com**	**DIP**	**S3-60**
Differential	3606M	Gain set word 1, 2, 4, 8...1024	0.02	10	±0.004	90,G=1	±(1+20/G)	40	Ind	DIP	3-150

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C. (2) Set with external resistor. (3) Unity-gain. (4) Gain = 10 (5) No source imbalance. (6) DC to 60Hz, Gain = 10, 1kΩ unbalanced.

PRECISION TRANSMITTERS

Description	Model	Span: Untrimmed Error, max (%)	Span: Non-linearity, max (%)	Span: Temp Drift[1] (ppm/°C)	Input Parameters: Offset Voltage max	Input Parameters: Offset Voltage vs Temp max (µV/°C)	Input Parameters: CMR, DC, min (dB)	Output Parameters: Current Range (mA)	Output Parameters: Offset Current Error, max (µA)	Output Parameters: FS Output Current Error, max (µA)	Temp Range[2]	Pkg	Page No.
Two-Wire	XTR101G[5], L[5]	–5	0.01	±100	±30µV	±0.75	90	4-20	±6	±30	Ind	DIP	3-126
	XTR101P, U	–5	0.01	±100	±100µV	±1.5	90	4-20	±19	±60	Ind[3]	DIP, SOIC	3-126 3-126
Two-Wire RTD Linearity Compensation	**XTR103P**	**–1**	**0.01**	**±25**	**±50**	**±1**	**100**	**4-20**	**±10**	**25**	**Ind[3]**	**DIP**	**S3-83**
	XTR103U	**–1**	**0.01**	**±50**	**±100**	**±2**	**90**	**4-20**	**±20**	**±50**	**Ind[3]**	**SOIC**	**S3-83**
Two-Wire Hi-Z Strain Gage Linearity Compensation	**XTR104P**	**–1**	**0.01**	**±25**	**±50**	**±1**	**100**	**4-20**	**±10**	**±25**	**Ind[3]**	**DIP**	**S3-85**
	XTR104U	**–1**	**0.01**	**±50**	**±100**	**±2**	**90**	**4-20**	**±20**	**±50**	**Ind[3]**	**SOIC**	**S3-83**
Three-Wire and Current Source	XTR110G	0.2	0.005	30	—	—	—	4-20, 0-20, 5-25[4]	±16	±32	Ind	DIP	3-139
	XTR110P, U	0.6	0.025	50	—	—	—		±64	±96	Com	DIP, SOIC	3-139 3-139

NOTES: (1) With zero TC span resistor. (2) Com = 0°C to +70°C, Ind = –25°C to +85°C. (3) –40°C to +85°C. (4) Many more ranges with appropriate circuit. (5) BS 9000 screening is available.

INSTRUMENTATION AMPLIFIERS GLOSSARY

COMMON-MODE INPUT IMPEDANCE

Effective impedance (resistance in parallel with capacitance) between either input of an amplifier and its common, or ground, terminal.

COMMON-MODE REJECTION (CMR)

When both inputs of a differential amplifier experience the same common-mode voltage (CMV), the output should, ideally, be unaffected. CMR is the ratio of the common-mode input voltage change to the differential input voltage (error voltage) producing the same output change:

$$\text{CMR (in dB)} = 20\log_{10} \text{CMV/Error Voltage}$$

Thus a CMR of 80dB means that 1V of common-mode voltage will cause an error of 100μV (referred to input).

COMMON-MODE REJECTION RATIO (CMRR)

Ratio of the differential voltage gain of an amplifier to its common-mode voltage gain.

COMMON-MODE VOLTAGE (CMV)

That portion of an input signal common to both inputs of a differential amplifier. Mathematically it is defined as the average of the signals at the two inputs:

$$\text{CMV} = (e_1 + e_2) / 2$$

FEEDBACK

Return of a portion of the output signal from a device to the input of the device.

FULL POWER FREQUENCY RESPONSE

Maximum sinewave frequency at which a device can supply its peak-to-peak rated output voltage and current, without introducing significant distortion.

GAIN

Ratio of the output signal to the associated input signal of a device.

GAIN ERROR

Difference between the actual gain of an amplifier and the one predicted by the ideal gain expression.

INPUT BIAS CURRENT

DC input current required at each input of an amplifier to provide zero output voltage when the input signal and input offset voltage are zero. The specified maximum is for each input.

INPUT BIAS CURRENT DRIFT

Rate of change of input bias current with temperature or time.

INPUT GUARDING

Use of an input shield that is sometimes driven to follow the voltage level of the input signal and, thereby, remove leakage and loss-inducing voltage differences between the input signal path and surrounding stray conduction paths.

INPUT OFFSET CURRENT

Difference of the two input bias currents in a differential amplifier.

INPUT OFFSET VOLTAGE

DC input voltage required to provide zero voltage at the output of an amplifier when the input signal and input bias currents are zero.

INPUT PROTECTION

Means of protecting an input of a device from damage due to the application of excessive input voltage.

INSTRUMENTATION AMPLIFIER

Closed-loop, differential input, gain block exhibiting high input impedance and high common-mode rejection. Its primary function is to accurately amplify the voltage applied to its inputs.

NONLINEARITY

Peak deviation from a best-fit straight line (curve fitting on input/output graph) expressed as a percent of peak-to-peak full scale output.

OVERLOAD RECOVERY TIME

Time required for the output of an amplifier to return from saturation to linear operation, following the removal of an input overdrive signal.

SETTLING TIME

Time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value.

SLEW RATE

Maximum rate of change of an output voltage when supplying the rated output.

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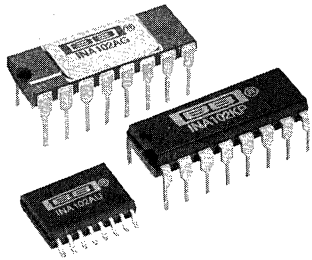


INA102

Low Power INSTRUMENTATION AMPLIFIER

FEATURES

- LOW QUIESCENT CURRENT: 750µA max
- INTERNAL GAINS: 1, 10, 100, 1000
- LOW GAIN DRIFT: 5ppm/°C max
- HIGH CMR: 90dB min
- LOW OFFSET VOLTAGE DRIFT: 2µV/°C max
- LOW OFFSET VOLTAGE: 100µV max
- LOW NONLINEARITY: 0.01% max
- HIGH INPUT IMPEDANCE: $10^{10}\Omega$

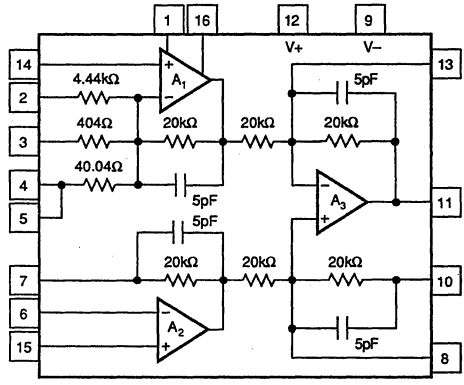
APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  Strain Gages (Weigh Scale Applications)
  Thermocouples
  Bridge Transducers
- REMOTE TRANSDUCER AMPLIFIER
- LOW-LEVEL SIGNAL AMPLIFIER
- MEDICAL INSTRUMENTATION
- MULTICHANNEL SYSTEMS
- BATTERY POWERED EQUIPMENT

DESCRIPTION

The INA102 is a high-accuracy monolithic instrumentation amplifier designed for signal conditioning applications where low quiescent power is desired. On-chip thin-film resistors provide excellent temperature and stability performance. State-of-the-art laser-trimming technology insures high gain accuracy and common-mode rejection while avoiding expensive external components. These features make the INA102 ideally suited for battery-powered and high-volume applications.

The INA102 is also convenient to use. A gain of 1, 10, 100, or 1000 may be selected by simply strapping the appropriate pins together. A gain drift of 5ppm/°C in low gains can then be achieved without external adjustment. When higher-than-specified CMR is required, CMR can be trimmed using the pins provided. In addition, balanced filtering can be accomplished in the output stage.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-523F

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C with ±15VDC power supply and in circuit of Figure 2 unless otherwise noted.

PARAMETER	CONDITIONS	INA102AG MIN	INA102AG TYP	INA102AG MAX	INA102CG MIN	INA102CG TYP	INA102CG MAX	INA102KP/INA102AU MIN	INA102KP/INA102AU TYP	INA102KP/INA102AU MAX	UNITS
GAIN											
Range of Gain		1		1000	•		•	•		•	V/V
Gain Equation, External, ±20%			G = 1 + (40k/R_G)[1]			•			•		V/V
Error, DC: G = 1	T_A = +25°C			0.1			0.05			0.15	%
G = 10	T_A = +25°C			0.1			0.05			0.35	%
G = 100	T_A = +25°C			0.25			0.15			0.4	%
G = 1000	T_A = +25°C			0.75			0.5			0.9	%
G = 1	T_A = T_{MIN} to T_{MAX}			0.16			0.08			0.21	%
G = 10	T_A = T_{MIN} to T_{MAX}			0.19			0.11			0.44	%
G = 100	T_A = T_{MIN} to T_{MAX}			0.37			0.21			0.52	%
G = 1000	T_A = T_{MIN} to T_{MAX}			0.93			0.62			1.08	%
Gain Temp. Coefficient											
G = 1				10			5			•	ppm/°C
G = 10				15			10			•	ppm/°C
G = 100				20			15			•	ppm/°C
G = 1000				30			20			•	ppm/°C
Nonlinearity, DC											
G = 1	T_A = +25°C			0.03			0.01			•	% of FS
G = 10	T_A = +25°C			0.03			0.01			•	% of FS
G = 100	T_A = +25°C			0.05			0.02			•	% of FS
G = 1000	T_A = +25°C			0.1			0.05			•	% of FS
G = 1	T_A = T_{MIN} to T_{MAX}			0.045			0.015			•	% of FS
G = 10	T_A = T_{MIN} to T_{MAX}			0.045			0.015			•	% of FS
G = 100	T_A = T_{MIN} to T_{MAX}			0.075			0.03			•	% of FS
G = 1000	T_A = T_{MIN} to T_{MAX}			0.15			0.1			•	% of FS
RATED OUTPUT											
Voltage	R_L = 10kΩ	±($\|V_{CC}\|$ – 2.5)			•			•			V
Current		±1			•			•			mA
Short-Circuit Current[2]			2			•			•		mA
Output Impedance, G = 1000			0.1			•			•		Ω
INPUT											
OFFSET VOLTAGE											
Initial Offset[3]	T_A = +25°C		±300	±300/G		±100	±200/G			•	µV
INA102AU										±500	±300/G µV
vs Temperature			±5	±10/G		±2	±5/G			•	µV/°C
vs Supply			±40	±50/G		±10	±20/G			•	µV/V
vs Time			±(20 + 30/G)			•			•		µV/mo
BIAS CURRENT											
Initial Bias Current											
(Each Input)	T_A = T_{MIN} to T_{MAX}		25	50		6	30		•	•	nA
vs Temperature			±0.1			•			•		nA/°C
vs Supply			±0.1			•			•		nA/V
Initial Offset Current	T_A = T_{MIN} to T_{MAX}		±2.5	±15		±2.5	±10		•	•	nA
vs Temperature			±0.1			•			•		nA/°C
IMPEDANCE											
Differential			10^{10} ‖ 2			•			•		Ω ‖ pF
Common-Mode			10^{10} ‖ 2			•			•		Ω ‖ pF
VOLTAGE RANGE											
Range, Linear Response	T_A = T_{MIN} to T_{MAX}	±($\|V_{CC}\|$ – 4.5)			•			•			V
CMR With 1kΩ Source Imbalance											
G = 1	DC to 60Hz	80	94		90	•		75	•		dB
G = 10	DC to 60Hz	80	100		90	•		•	•		dB
G = 10 to 1000	DC to 60Hz	80	100		90	•		•	•		dB
NOISE											
Input Voltage Noise											
f_B = 0.01Hz to 10Hz			1			•			•		µVp-p
Density, G = 1000: f_O = 10Hz			30			•			•		nV/√Hz
f_O = 100Hz			25			•			•		nV/√Hz
f_O = 1kHz			25			•			•		nV/√Hz
Input Current Noise											
f_B = 0.01Hz to 10Hz			25			•			•		pAp-p
Density: f_O = 10Hz			0.3			•			•		pA/√Hz
f_O = 100Hz			0.2			•			•		pA/√Hz
f_O = 1kHz			0.15			•			•		pA/√Hz

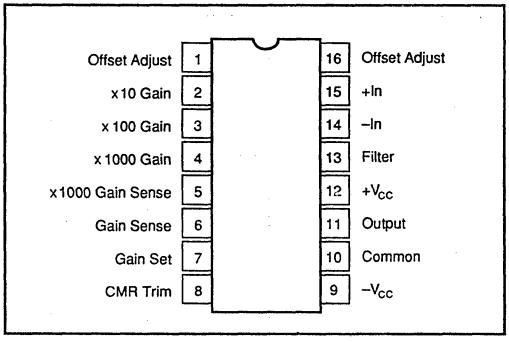
ELECTRICAL (CONT)

PARAMETER	CONDITIONS	INA102AG			INA102CG			INA102KP/INA102AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC RESPONSE											
Small Signal											
±3dB Flatness	V_{OUT} = 0.1Vrms										
G = 1			300			*			*		kHz
G = 10			30			*			*		kHz
G = 100			3			*			*		kHz
G = 1000			0.3			*			*		kHz
Small Signal,											
±1% Flatness	V_{OUT} = 0.1Vrms										
G = 1			30			*			*		kHz
G = 10			3			*			*		kHz
G = 100			0.3			*			*		kHz
G = 1000			0.03			*			*		kHz
Full Power, G = 1 to 100	V_{OUT} = 10V, R_L = 10kΩ	1.7	2.5		*	*		*	*		kHz
Slew Rate, G = 1 to 100	V_{OUT} = 10V, R_L = 10kΩ	0.1	0.15		*	*		*	*		V/µs
Settling Time	R_L = 10kΩ, C_L = 100pF										
0.1%: G = 1	10V Step		50			*			*		µs
G = 100			360			*			*		µs
G = 1000			3300			*			*		µs
0.01%: G = 1	10V Step		60			*			*		µs
G = 100			500			*			*		µs
G = 1000			4500			*			*		µs
POWER SUPPLY											
Rated Voltage			±15			*			*		V
Voltage Range		±3.5		±18	*		*	*		*	V
Quiescent Current	V_O = 0V,										
	$T_A = T_{MIN}$ to T_{MAX}		±500	±750		*	*		*	*	µA
TEMPERATURE RANGE											
Specification		–25		+85	*		*	0		+70	°C
INA102AU								**–25**		**+85**	°C
Operation	R_L > 50kΩ[2]	–25		+85	*		*	–25		+85	°C
Storage		–65		+150	*		*	–55		+125	°C

*Specification same as for INA102AG.

NOTES: (1) The internal gain set resistors have an absolute tolerance of ±20%; however, their tracking is 50ppm/°C. R_G will add to the gain error if gains other than 1, 10, 100 or 1000 are set externally. (2) At high temperature, output drive current is limited. An external buffer can be used if required. (3) Adjustable to zero.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

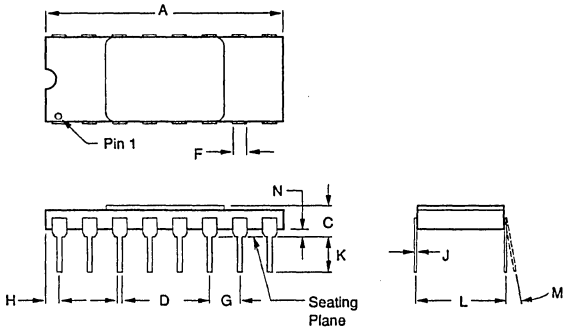
Supply	±18V
Input Voltage Range	$\pm V_{cc}$
Operating Temperature Range	–25°C to +85°C
Storage Temperature Range: Ceramic	–65°C to +150°C
Plastic, SOIC	–55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Output Short-Circuit Duration	Continuous to Ground

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA102AG	Ceramic DIP	–25°C to +85°C
INA102CG	Ceramic DIP	–25°C to +85°C
INA102KP	Plastic DIP	0°C to +70°C
INA102AU	Plastic SOIC	–25°C to +85°C

MECHANICAL

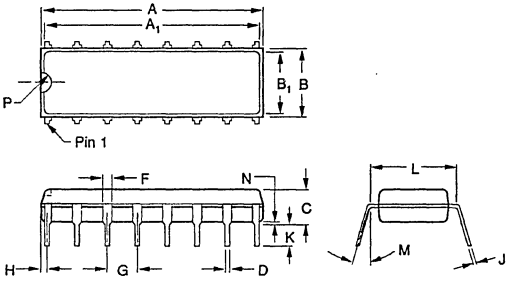
G Package — 16-Pin Ceramic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

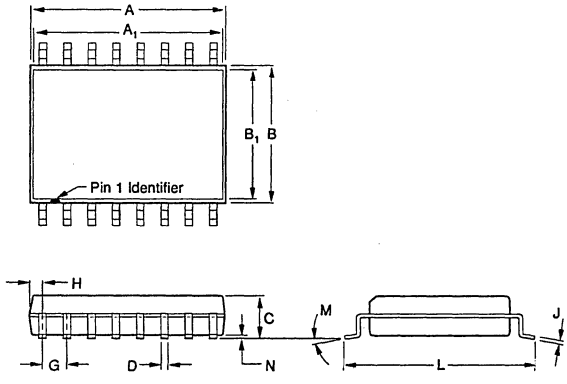
P Package — 16-Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.740	.800	18.80	20.32
A1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	0.20	.050	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

U Package — 16-Pin SOIC



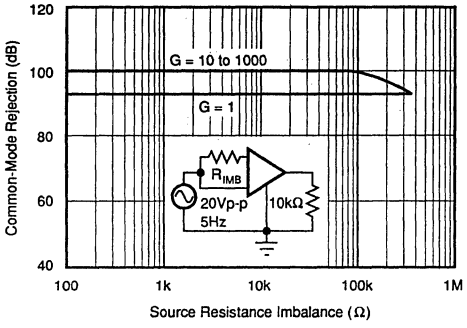
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.400	.416	10.16	10.57
A1	.388	.412	9.86	10.46
B	.286	.302	7.26	7.67
B1	.268	.286	6.81	7.26
C	.093	.109	2.36	2.77
D	.015	.020	0.38	0.51
G	.0.50 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.391	.421	9.93	10.69
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

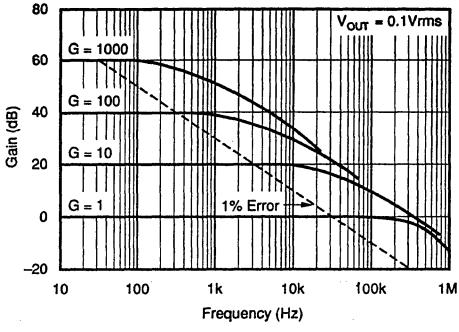
TYPICAL PERFORMANCE CURVES

At +25°C and in circuit of Figure 2 unless otherwise noted.

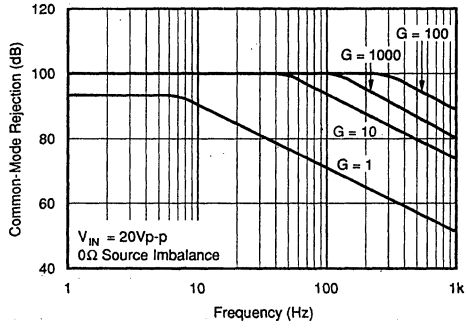
COMMON-MODE REJECTION vs SOURCE IMBALANCE



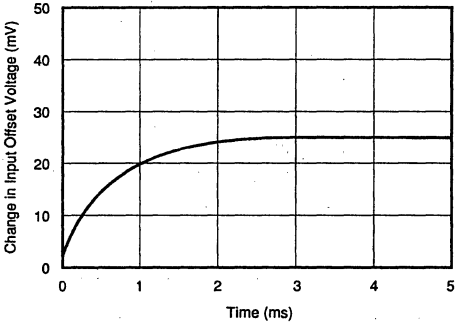
GAIN vs FREQUENCY



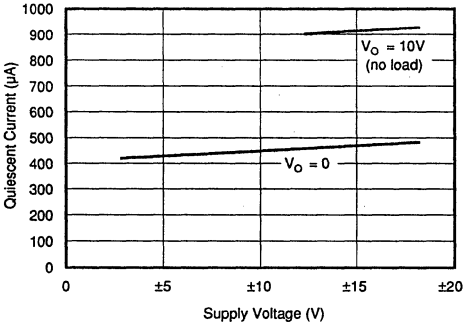
COMMON-MODE REJECTION vs FREQUENCY



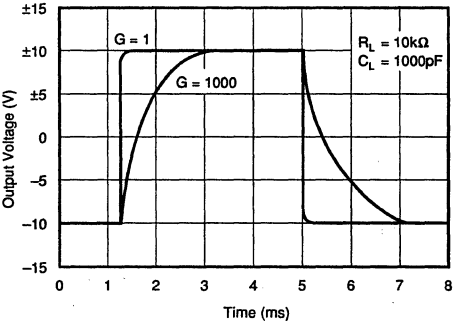
WARM-UP DRIFT vs TIME



QUIESCENT CURRENT vs SUPPLY

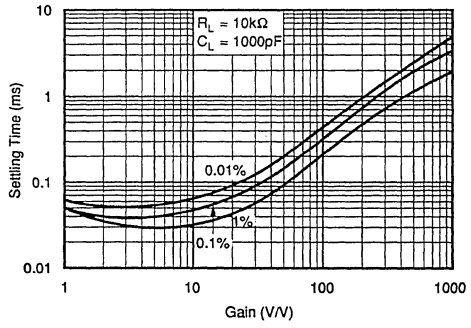


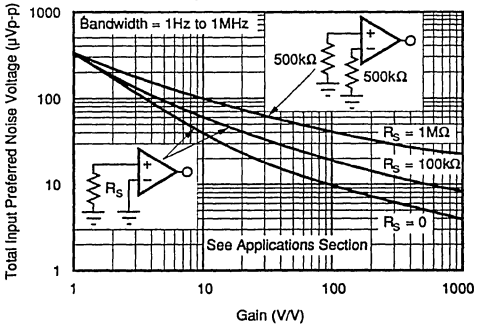
STEP RESPONSE

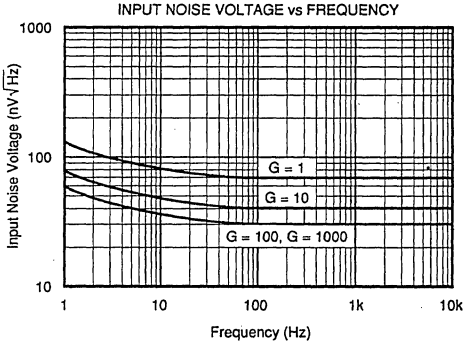


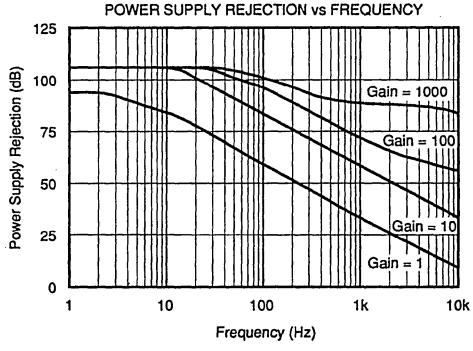
TYPICAL PERFORMANCE CURVES (CONT)

At +25°C and in circuit of Figure 2 unless otherwise noted.







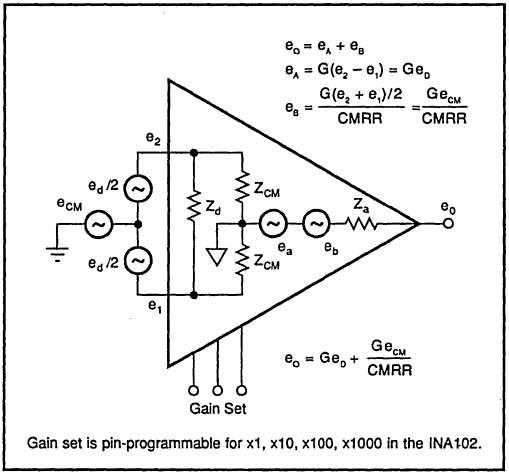


DISCUSSION OF PERFORMANCE

INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are differential-input closed-loop gain blocks whose committed circuit accurately amplifies the voltage applied to their inputs. They respond mainly to the difference between the two input signals and exhibit extremely high input impedance, both differentially and common-mode. The feedback network of this instrumentation amplifier is included on the monolithic chip. No external resistors are required for gains of 1, 10, 100, and 1000 in the INA102.

An operational amplifier, on the other hand, is an open-loop, uncommitted device that requires external networks to close the loop. While op amps can be used to achieve the same basic function as instrumentation amplifiers, it is very difficult to reach the same level of performance. Using op amps often leads to design tradeoffs when it is necessary to amplify low-level signals in the presence of common-mode voltages while maintaining high-input impedances. Figure 1 shows a simplified model of an instrumentation amplifier that eliminates most of the problems associated with op amps.



Gain set is pin-programmable for x1, x10, x100, x1000 in the INA102.

FIGURE 1. Model of an Instrumentation Amplifier.

THE INA102

A simplified schematic of the INA102 is shown on the first page. A three-amplifier configuration is used to provide the desirable characteristics of a premium performance instrumentation amplifier. In addition, INA102 has features not normally found in integrated circuit instrumentation amplifiers.

The input buffers (A_1 and A_2) incorporate high performance, low-drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide the high input impedance ($10^{10}\Omega$) desirable in instrumentation amplifier applications. The offset voltage, and offset voltage versus temperature, are low due to the monolithic design, and improved even further by state-of-the-art laser-trimming techniques.

The output stage (A_3) is connected in a unity-gain differential amplifier configuration. A critical part of this stage is the matching of the four 20kΩ resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to retain good common-mode rejection.

All of the internal resistors are made of thin-film nichrome on the integrated circuit. The critical resistors are laser-trimmed to provide the desired high gain accuracy and common-mode rejection. Nichrome ensures long-term stability and provides excellent TCR and TCR tracking. This provides gain accuracy and common-mode rejection when the INA102 is operated over wide temperature ranges.

USING THE INA102

Figure 2 shows the simplest configuration of the INA102. The output voltage is a function of the differential input voltage times the gain.

A gain of 1, 10, 100, or 1000 is selected by programming pins 2 through 7 (see Table I). Notice that for the gain of 1000, a special gain sense is provided to preserve accuracy. Although this is not always required, gain errors caused by external resistance in series with the low value 40.04Ω internal gain set resistor are thus eliminated.

Other gains between 1 and 10, 10 and 100, and 100 and 1000 can also be obtained by connecting an external resistor between pin 6 and either pin 2, 3, or 4, respectively (see Figure 6 for application).

$G = 1 + (40/R_G)$ where R_G is the total resistance between the two inverting inputs of the input op amps. At high gains, where the value of R_G becomes small, additional resistance (i.e., relays or sockets) in the R_G circuit will contribute to a gain error. Care should be taken to minimize this effect.

OPTIONAL OFFSET ADJUSTMENT PROCEDURE

It is sometimes desirable to null the input and/or output offset to achieve higher accuracy. The quality of the potentiometer will affect the results; therefore, choose one with good temperature and mechanical-resistance stability.

The optional offset null capabilities are shown in Figure 3. R_4 adjustment affects only the input stage component of the offset voltage. Note that the null condition will be disturbed when the gain is changed. Also, the input drift will be affected by approximately 0.31μV/°C per 100μV of input offset voltage that is trimmed. Therefore, care should be taken when considering use of the control for removal of other sources of offset. Output offset correction can be accomplished with A_1, R_1, R_2, and R_3, by applying a voltage to Common (pin 10) through a buffer amplifier. This buffer limits the resistance in series with pin 10 to minimize CMR error. Resistance above 0.1Ω will cause the common-mode rejection to fall below 100dB. Be certain to keep this resistance low.

It is important to not exceed the input amplifiers' dynamic range. The amplified differential input signal and its associated common-mode voltage should not cause the output of A_1 or A_2 to exceed approximately ±12V with ±15V supplies,

GAIN	CONNECT PINS
1	6 to 7
10	2 to 6 and 7
100	3 to 6 and 7
1000	4 to 7 and separately 5 to 6

TABLE I. Pin-Programmable Gain Connections.

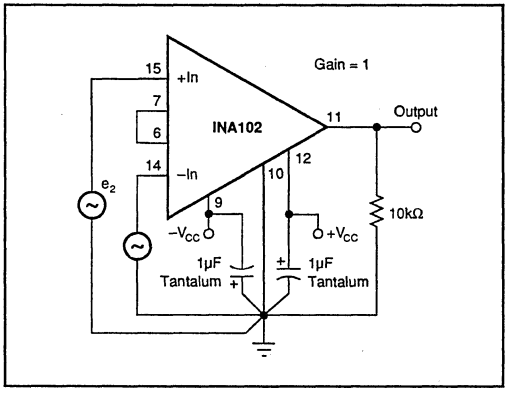


FIGURE 2. Basic Circuit Connection for the INA102.

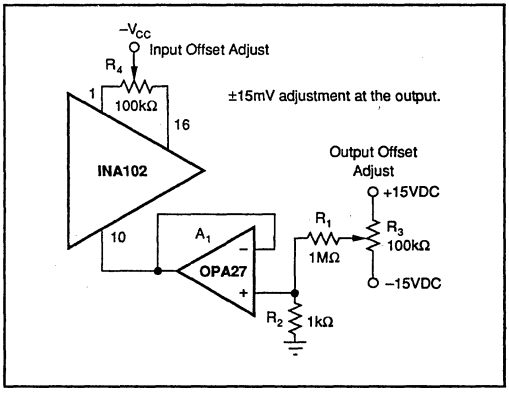


FIGURE 3. Optional Offset Nulling.

or nonlinear operation will result. To protect against moisture, especially in high gain, sealing compound may be used. Current injected into the offset pins should be minimized.

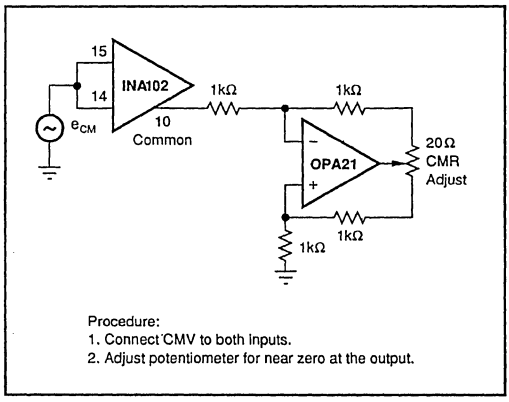


FIGURE 4. Optional Circuit for Externally Trimming CMR.

OPTIONAL FILTERING

The INA102 has provisions for accomplishing filtering with one external capacitor between pins 11 and 13. This single-pole filter can be used to reduce noise outside the signal bandwidth, but with some degradation to AC CMR.

When it is important to preserve CMR versus frequency (especially at 60Hz), two capacitors should be used. The additional capacitor is connected between pins 8 and 10. This will maintain a balance of impedances in the output stage. Either of these capacitors could also be trimmed slightly, to maximize CMR, if desired. Note that their ratio tracking will affect CMR over temperature.

OPTIONAL COMMON-MODE REJECTION TRIM

The INA102 is laser-adjusted during manufacturing to assure high CMR. However, if desired, a small resistance can be added in series with pin 10 to trim the CMR to an improved level. Depending upon the nature of the internal imbalances, either positive or negative resistance value could be required. The circuit shown in Figure 4 acts as a bipolar potentiometer and allows easy adjustment of CMR.

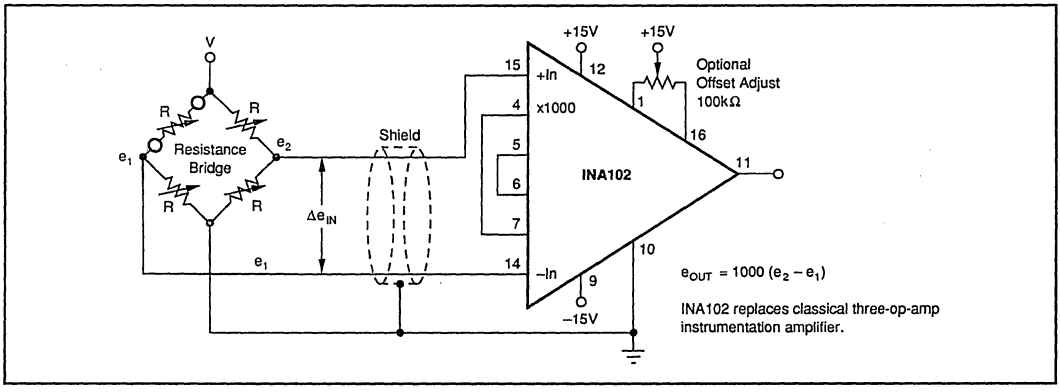


FIGURE 5. Amplification of a Differential Voltage from a Resistance Bridge.

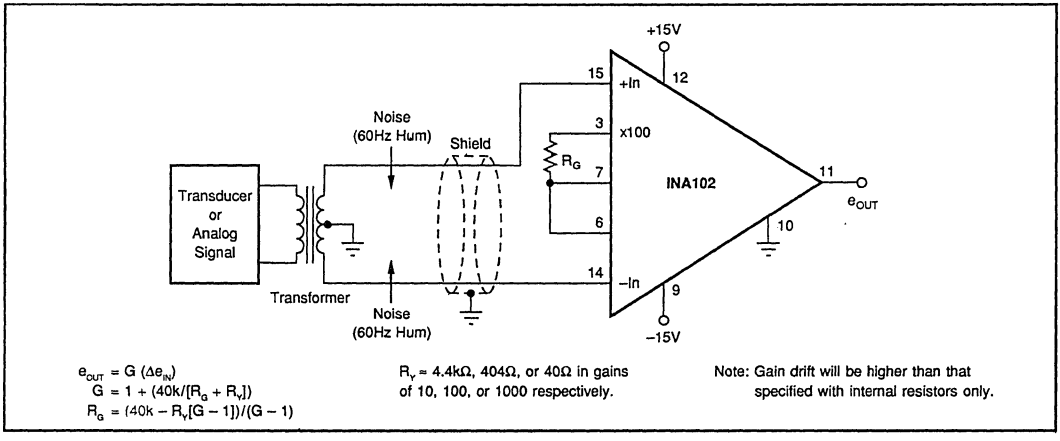


FIGURE 6. Amplification of a Transformer-Coupled Analog Signal Using External Gain Set.

TYPICAL APPLICATIONS

Many applications of instrumentation amplifiers involve the amplification of low-level differential signals from bridges and transducers such as strain gages, thermocouples, and RTDs. Some of the important parameters include common-mode rejection (differential cancellation of common-mode offset and noise, see Figure 1), input impedance, offset voltage and drift, gain accuracy, linearity, and noise. The INA102 accomplishes all of these with high precision at surprisingly low quiescent current. However, in higher gains (>100), the bias current can cause a large offset error at the output. This can saturate the output unless the source impedance is separated, e.g., two 500kΩ paths instead of one 1MΩ unbalanced input. Figures 5 through 16 show some typical applications circuits.

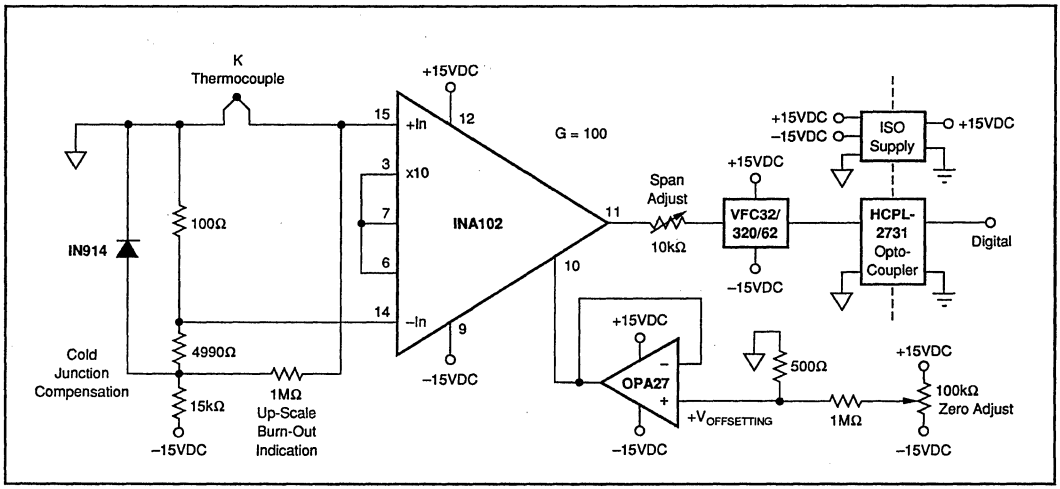


FIGURE 7. Isolated Thermocouple Amplifier with Cold Junction Compensation.

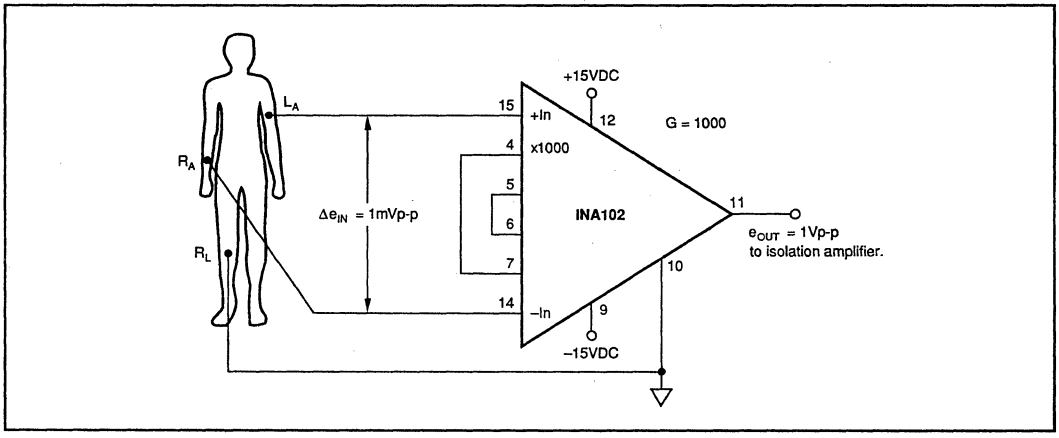


FIGURE 8. ECG Amplifier or Recorder Preamp for Biological Signals.

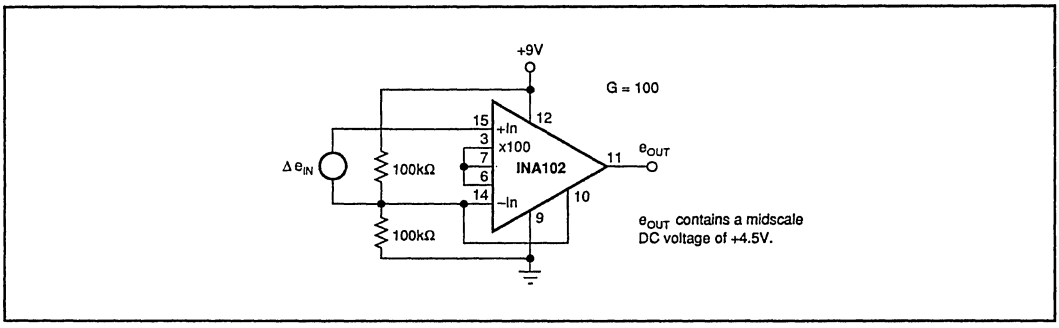


FIGURE 9. Single Supply Low Power Instrumentation Amplifier.

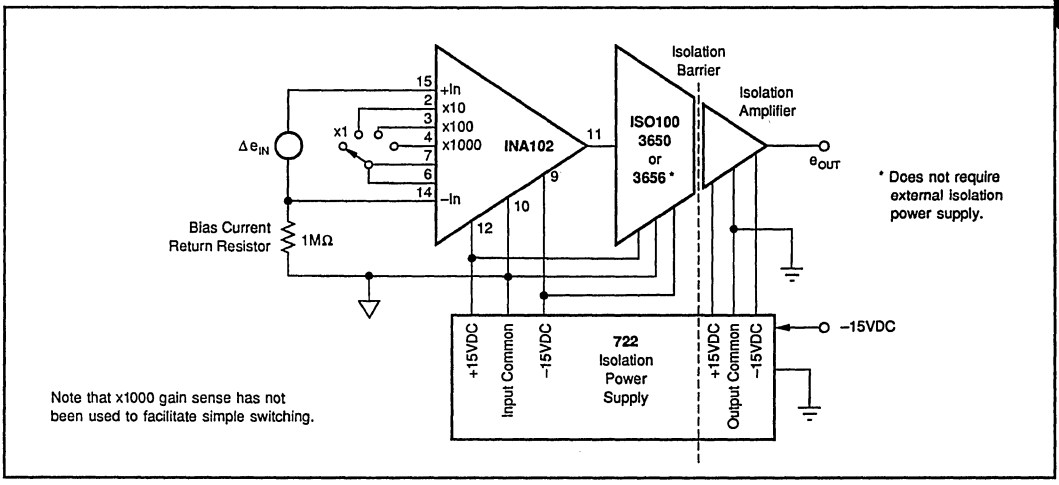


FIGURE 10. Precision Isolated Instrumentation Amplifier.

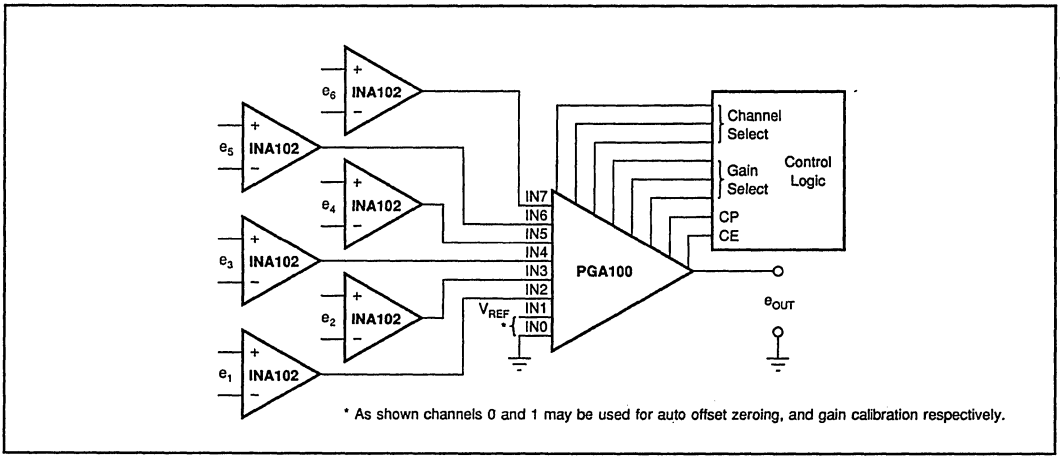


FIGURE 11. Multiple Channel Precision Instrumentation Amplifier with Programmable Gain.

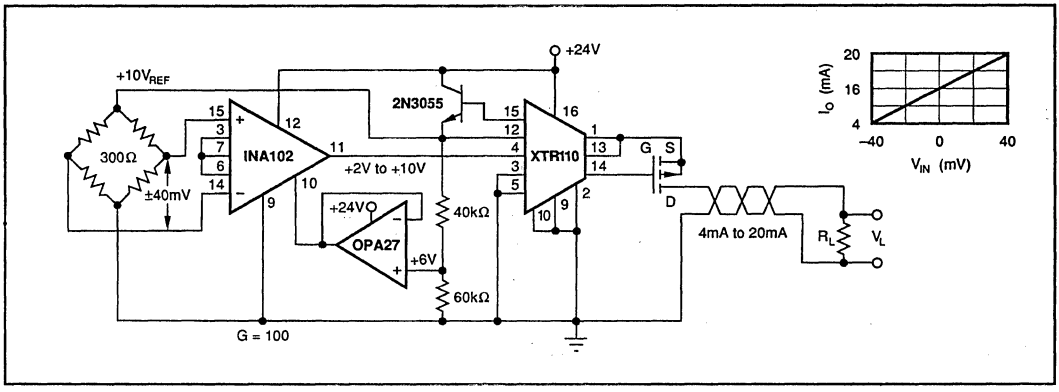


FIGURE 12. 4mA to 20mA Bridge Transmitter Using Single Supply Instrumentation Amplifier.

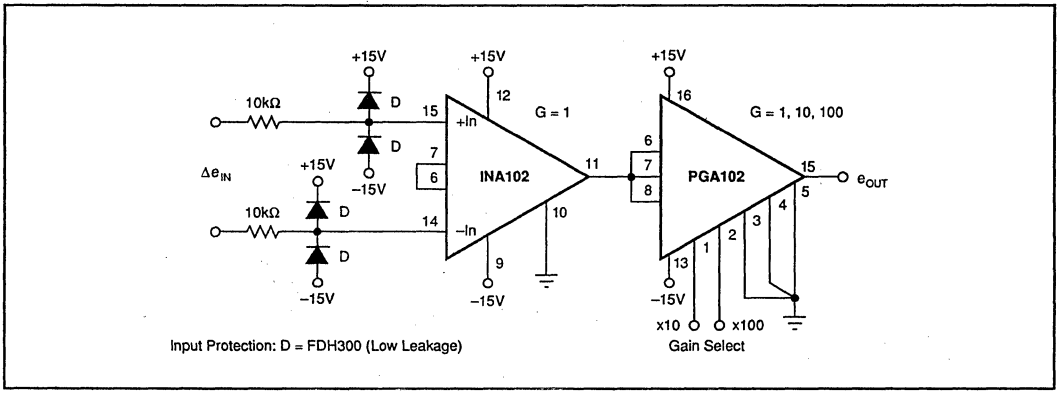


FIGURE 13. Programmable-Gain Instrumentation Amplifier Using the INA102 and PGA102.

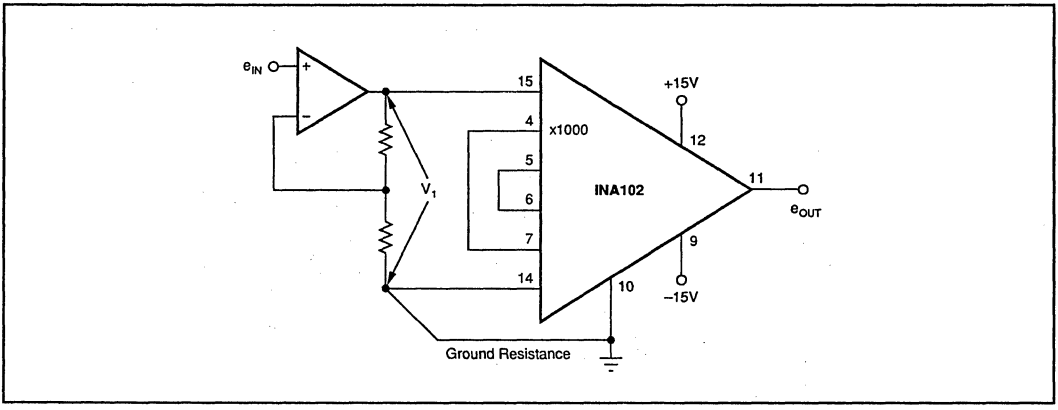


FIGURE 14. Ground Resistance Loop Eliminator (INA102 senses and amplifies V_1 accurately).

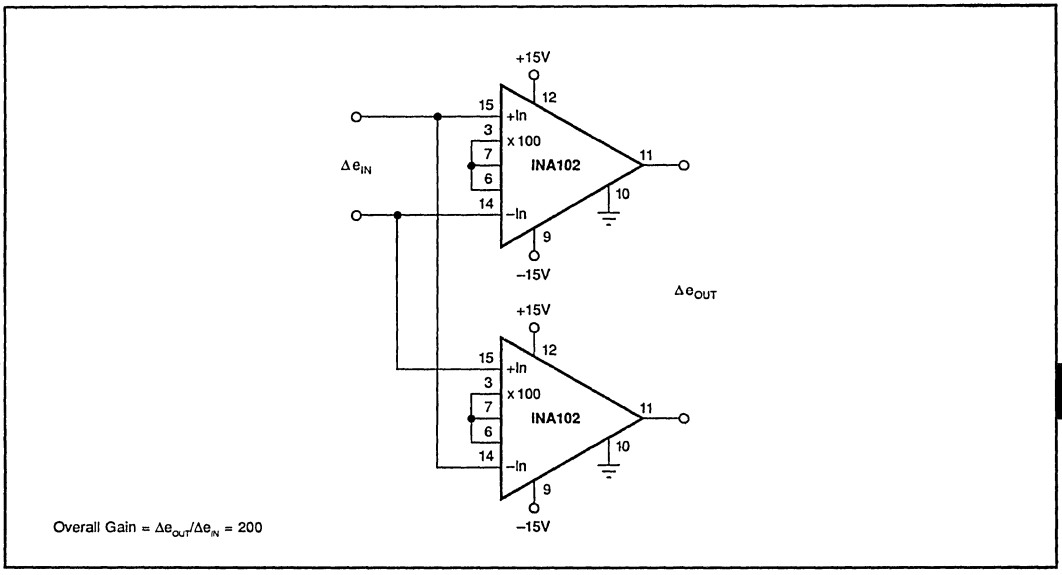
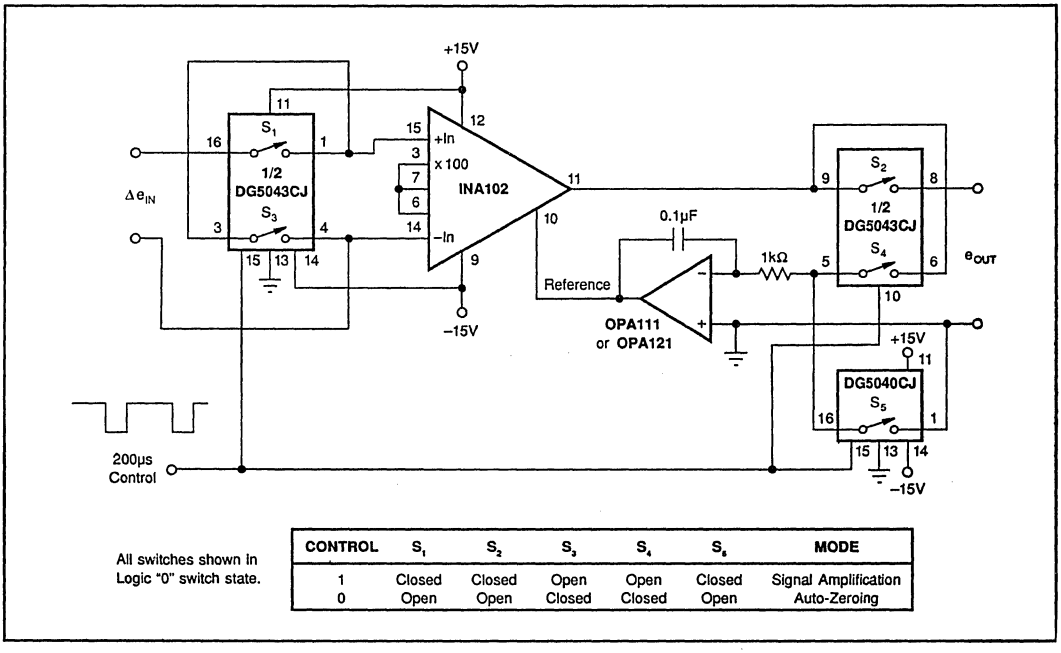


FIGURE 15. Differential Input/Differential Output Amplifier (twice the gain of one INA).

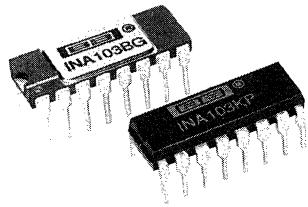


All switches shown in Logic "0" switch state.

CONTROL	S_1	S_2	S_3	S_4	S_5	MODE
1	Closed	Closed	Open	Open	Closed	Signal Amplification
0	Open	Open	Closed	Closed	Open	Auto-Zeroing

FIGURE 16. Auto-Zeroing Instrumentation Amplifier Circuit.

BURR-BROWN®



INA103

Low Noise, Low Distortion INSTRUMENTATION AMPLIFIER

FEATURES

- LOW NOISE : 1nV/√Hz
- LOW THD : <0.002% typ 20Hz-20kHz, G = 1 to 100
- HIGH GBW: 100MHz at G = 1000
- WIDE SUPPLY RANGE: ±9V to ±25V
- HIGH CMRR: >110dB
- BUILT-IN GAIN SETTING RESISTORS: G = 1, 100
- UPGRADES AD625

APPLICATIONS

- HIGH QUALITY MICROPHONE PREAMPS (REPLACES TRANSFORMERS)
- MOVING-COIL PREAMPLIFIERS
- DIFFERENTIAL RECEIVERS
- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  Strain Gages (Weigh Scale Applications)
  Thermocouples
  Bridge Transducers

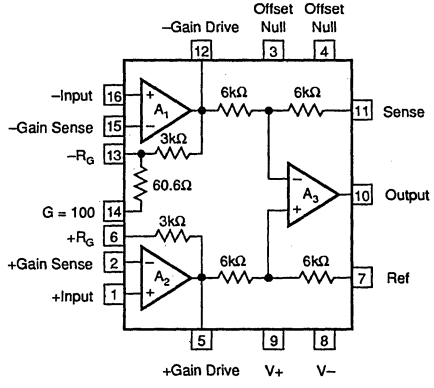
DESCRIPTION

The INA103 is an extremely low noise, low distortion monolithic instrumentation amplifier which is especially suitable for amplification of low level signals in audio systems. Input circuitry provides near-theoretical limit noise performance for 200Ω source impedances. A unique distortion-cancellation network in the input stage reduces THD to extremely low levels.

The INA103 is equally well-suited to preamplification and signal conditioning applications where low noise is required. In many cases, transformer coupling can be replaced by the INA103 to reduce cost and improve performance in signal conditioning systems.

The wide supply range (±9V to ±25V) of the INA103 increases its versatility. A copper lead frame in the plastic DIP package assures excellent thermal performance.

The INA103 pin configuration is compatible with the AD625. In many applications, the INA103 can replace the AD625 for improved performance. The INA103 is available in 16-pin DIP packages specified for the commercial (plastic DIP) and industrial (ceramic DIP) temperature ranges.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1016A

SPECIFICATIONS

ELECTRICAL

All specifications at T_A = +25°C, V_S = ±15V and R_L = 2kΩ, unless otherwise noted.

PARAMETER	CONDITIONS	INA103AG MIN	INA103AG TYP	INA103AG MAX	INA103BG MIN	INA103BG TYP	INA103BG MAX	INA103KP MIN	INA103KP TYP	INA103KP MAX	UNITS
GAIN											
Range of Gain		1		1000	*		*	*		*	V/V
Gain Equation [1]			G = 1 + 6kΩ/R_G			*			*		V/V
Gain Error, DC G = 1	±10V Output		0.005	0.05		0.003	0.01		*	*	%
G = 100			0.05	0.25		0.04	0.1		0.07	*	%
Eq.			0.5			0.1			*		%
Gain Temp. Co. G = 1	±10V Output		10			*			*		ppm/°C
G = 100			25			*			*		ppm/°C
Eq.			25			*			*		ppm/°C
Nonlinearity, DC G = 1	±10V Output		0.0003	0.01		0.0002	0.002		*	*	% of FS [2]
G = 100			0.0006	0.01		0.0006	0.004		*	*	% of FS
OUTPUT											
Voltage, R_L = 600Ω	T_A = T_{MIN} to T_{MAX}	±11.5	±12		*	*		*	*		V
R_L = 600Ω	V_S = ±25, T_A = 25°C	±20	±21		*	*		*	*		V
Current	T_A = T_{MIN} to T_{MAX}	±40			*			*			mA
Short Circuit Current			±70			*			*		mA
Capacitive Load Stability			10			*			*		nF
INPUT											
OFFSET VOLTAGE											
Initial Offset RTI [3]			(20 + 700/G)	(100 + 5000/G)		(20 + 320/G)	(50 + 2000/G)		(30 + 1200/G)	*	µV
vs Temp G = 1 to 1000	T_A = T_{MIN} to T_{MAX}		0.5 + 20/G			0.5 + 10/G			0.5 + 20/G		µV/°C
G = 1000	T_A = T_{MIN} to T_{MAX}		0.5			0.2			*		µV/°C
vs Supply	±9V to ±25V		0.2 + 8/G	4 + 60/G		*	2 + 30/G		*	*	µV/V
BIAS CURRENT											
Initial Bias Current			2.5	12		*	8		*	*	µA
vs Temp	T_A = T_{MIN} to T_{MAX}		15			*	40 [4]		*		nA/°C
Initial Offset Current			0.04	1		0.03	0.5		*	*	µA
vs Temp	T_A = T_{MIN} to T_{MAX}		0.5			*	2.5 [4]		*		nA/°C
IMPEDANCE											
Differential Mode			60 || 2			*			*		MΩ || pF
Common-Mode			60 || 5			*			*		MΩ || pF
VOLTAGE RANGE											
Range, Linear Response	Common Mode [5]	±11	±12		*	*		*	*		V
CMR											
G = 1	DC to 60Hz	72	86		80	91		*	*		dB
G = 100	DC to 60Hz	100	125		110	129		*	*		dB
NOISE											
INPUT											
Voltage [6]	R_S = 0Ω										
	10Hz		2			*			*		nV/√Hz
	100Hz		1.2			*			*		nV/√Hz
	1kHz		1			*	1.4 [4]		*		nV/√Hz
Current	1kHz		2			*			*		pA/√Hz
OUTPUT											
Voltage	1kHz		65			*			*		nV/√Hz
A Weighted, 20Hz-20kHz	20Hz-20kHz		–100			*			*		dBu
DYNAMIC RESPONSE											
–3dB Bandwidth: G = 1	Small Signal		6			*			*		MHz
G = 100	Small Signal		800			*			*		kHz
Full Power Bandwidth	G = 1										
	V_{OUT} = ±10V, R_L = 600Ω		240			*			*		kHz
Slew Rate	G = 1 to 500		15			*			*		V/µs
THD + Noise	G = 100, f = 1kHz		0.0009			*			*		%
Settling Time 0.1%											
G = 1	V_O = 20V Step		1.7			*			*		µs
G = 100			1.5			*			*		µs
Settling Time 0.01%											
G = 1	V_O = 20V Step		2			*			*		µs
G = 100			3.5			*			*		µs
Overload Recovery [7]	50% Overdrive		1			*			*		µs

*Same specification as INA103AG.

NOTES: (1) Gains other than 1 and 100 can be set by adding an external resistor, R_G between pins 2 and 15. Gain accuracy is a function of R_G. (2) FS = Full Scale. (3) Adjustable to zero. (4) Guaranteed but not tested. (5) V_O = 0V, see Typical Curves for V_{CM} vs V_O. (6) $V_{NOISE\ RTI} \approx \sqrt{V_{N\ INPUT} + (V_{N\ OUTPUT}/Gain)^2 + 4KTR_G}$. See Typical Curves. (7) Time required for output to return from saturation to linear operation following the removal of an input overdrive voltage.

SPECIFICATIONS (CONT)

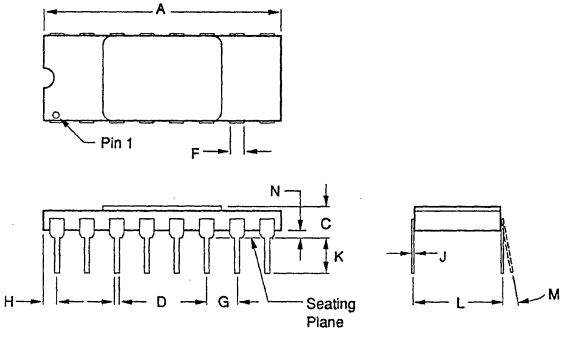
ELECTRICAL

All specifications at T_A = +25°C, V_S = ±15V and R_L = 2kΩ, unless otherwise noted.

PARAMETER	CONDITIONS	INA103AG			INA103BG			INA103KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY											
Rated Voltage			±15			*			*		V
Voltage Range		±9		±25	*		*	*		*	V
Quiescent Current			9	12.5		*	*		*	*	mA
TEMPERATURE RANGE											
Specification		–25		+85	*		*	0		+70	°C
Operation		–55		+125	*		*	–40		+85	°C
Storage		–65		+150	*		*	–40		+100	°C
Thermal Resistance, θ_{JA}			100			*			*		°C/W

MECHANICAL

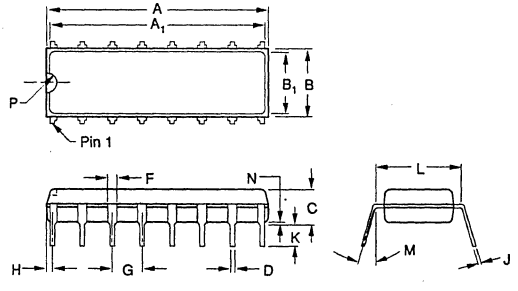
G Package — 16-Pin Hermetic DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

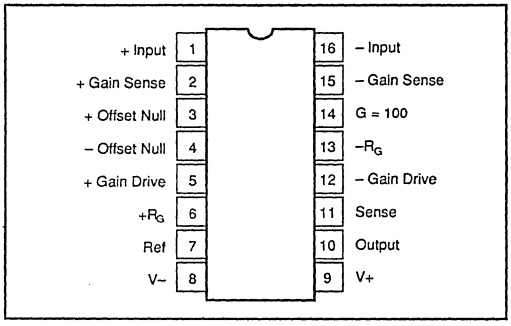
P Package — 16-Pin Plastic DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.740	.800	18.80	20.32
A1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	0.20	.050	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

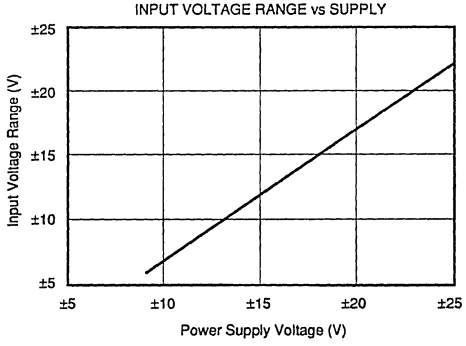
Supply	±25V
Input Voltage Range, Continuous	±V_S
Operating Temperature Range:	
P Package	–40°C to +85°C
G Package	–55°C to +125°C
Storage Temperature Range:	
P Package	–40°C to ±100°C
G Package	–65°C to ±150°C
Junction Temperature:	
P Package	+125°C
G Package	+150°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Common	Continuous

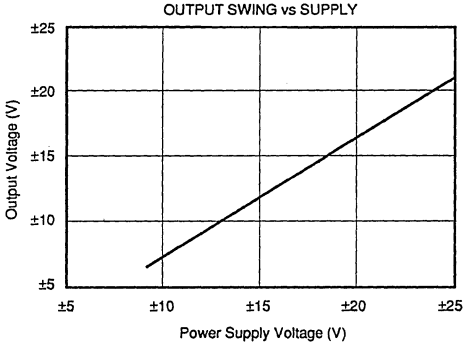
ORDERING INFORMATION

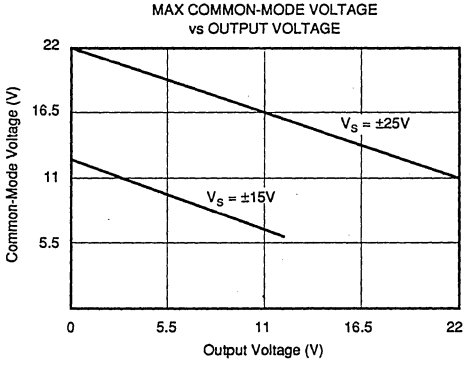
MODEL	PACKAGE	TEMP RANGE
INA103AG	Ceramic DIP	–25°C to +85°C
INA103BG	Ceramic DIP	–25°C to +85°C
INA103KP	Plastic DIP	0°C to +70°C

TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±15V unless otherwise noted.



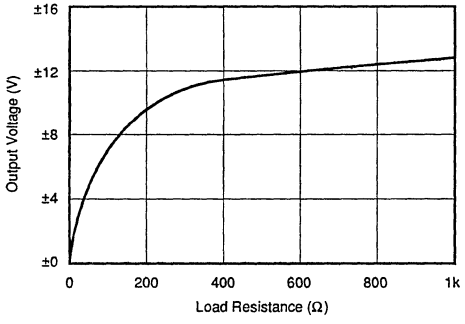




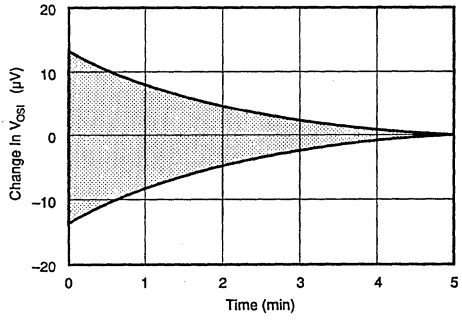
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V unless otherwise noted.

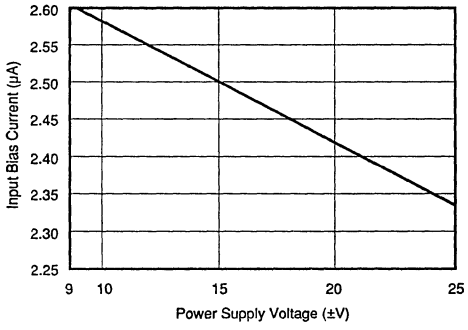
OUTPUT SWING vs LOAD RESISTANCE



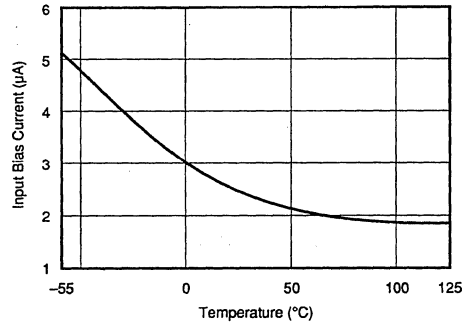
OFFSET VOLTAGE vs TIME FROM POWER UP
(G = 100)



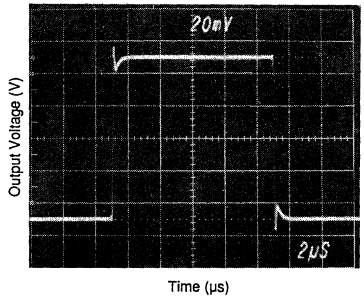
INPUT BIAS CURRENT vs SUPPLY



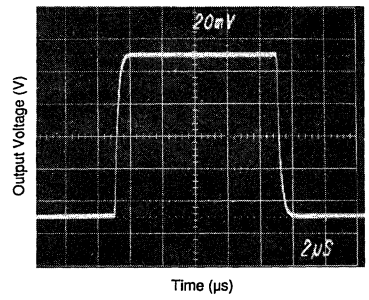
INPUT BIAS CURRENT vs TEMPERATURE



SMALL SIGNAL TRANSIENT RESPONSE
(G = 1)



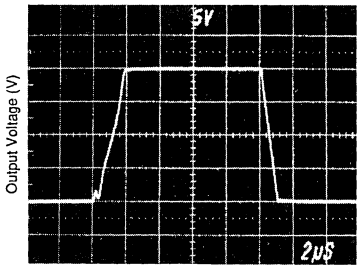
SMALL SIGNAL TRANSIENT RESPONSE
(G = 100)



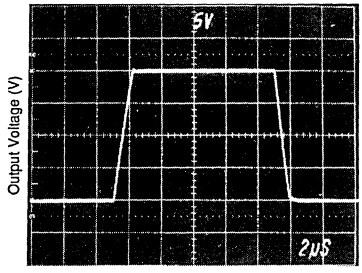
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V unless otherwise noted.

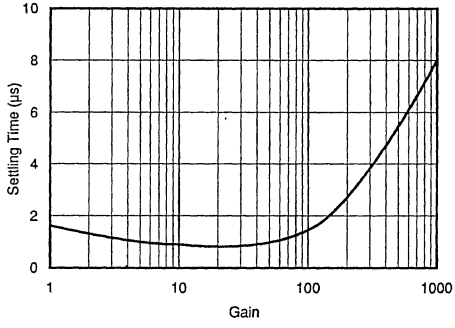
LARGE SIGNAL TRANSIENT RESPONSE
(G = 1)



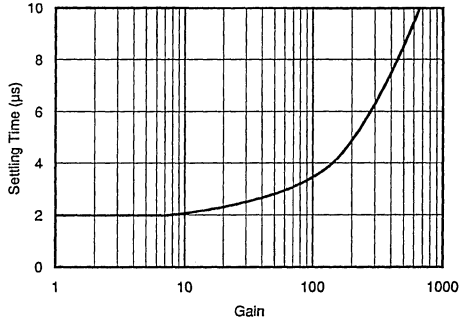
LARGE SIGNAL TRANSIENT RESPONSE
(G = 100)



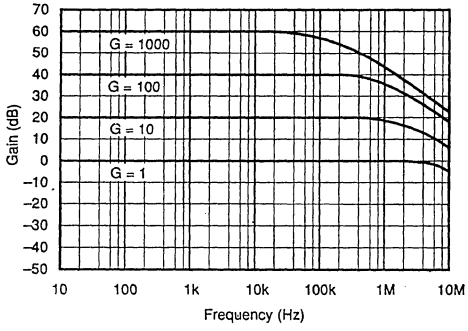
SETTLING TIME vs GAIN
(0.1%, 20V STEP)



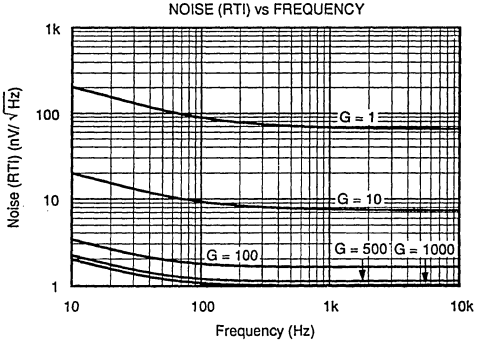
SETTLING TIME vs GAIN
(0.01%, 20V STEP)



SMALL-SIGNAL FREQUENCY RESPONSE



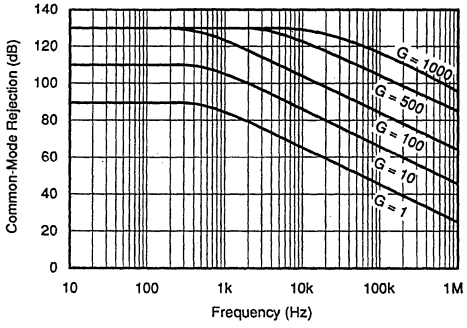
NOISE (RTI) vs FREQUENCY



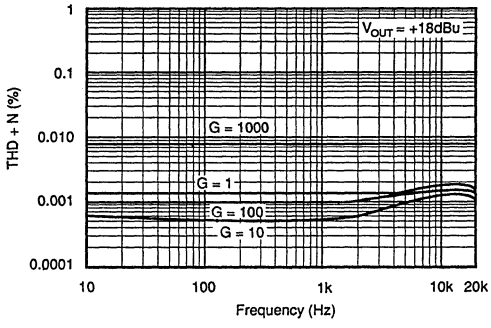
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V unless otherwise noted.

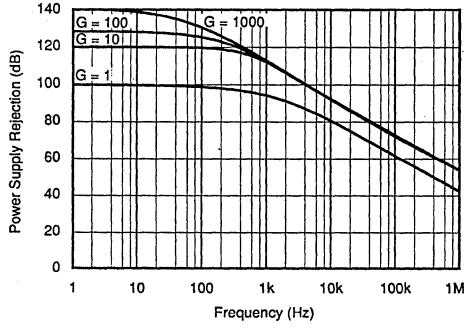
CMR vs FREQUENCY



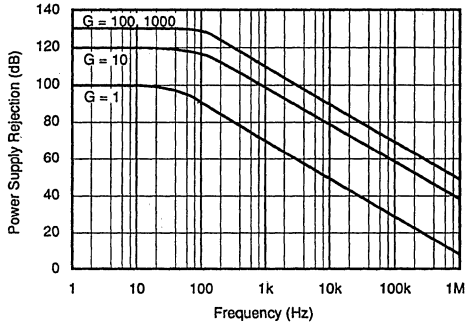
THD + N vs FREQUENCY



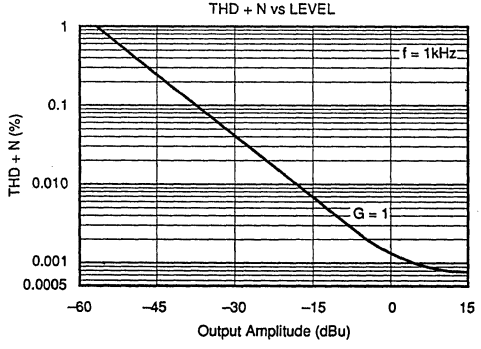
V+ POWER SUPPLY REJECTION vs FREQUENCY



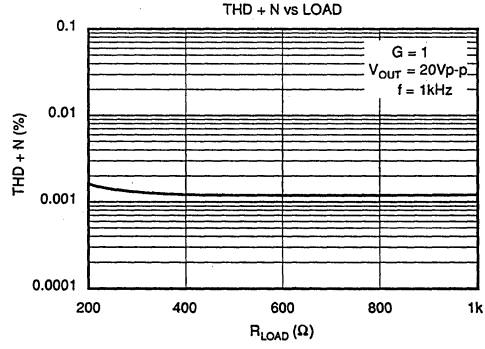
V– POWER SUPPLY REJECTION vs FREQUENCY



THD + N vs LEVEL



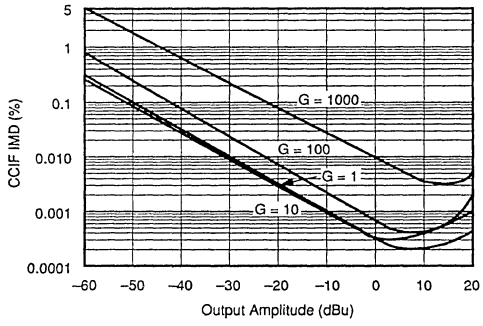
THD + N vs LOAD



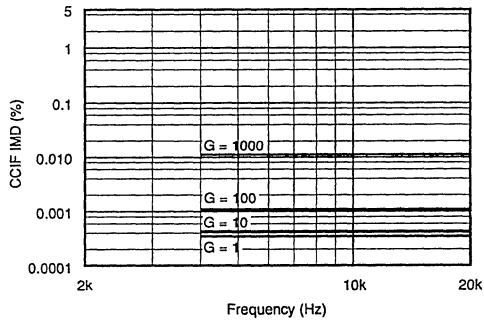
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V unless otherwise noted.

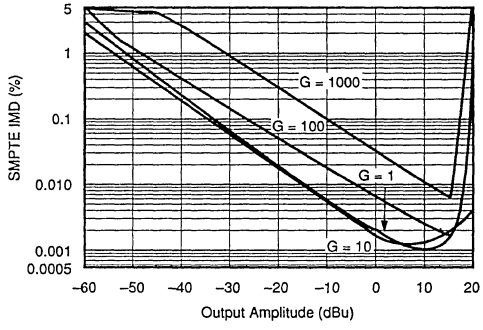
CCIF IMD vs AMPLITUDE



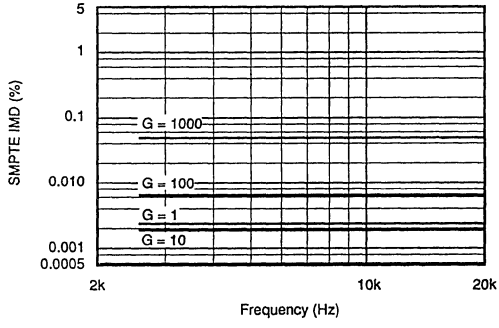
CCIF IMD vs FREQUENCY



SMPTE IMD vs AMPLITUDE



SMPTE IMD vs FREQUENCY



DISCUSSION OF PERFORMANCE

A simplified diagram of the INA103 is shown on the first page. The design uses a current feedback architecture which can be thought of as a classical three-op-amp instrumentation amplifier. The input stage (A_1 and A_2) incorporates wide-bandwidth, low noise, low drift amplifier circuitry. The unity-gain difference amp removes the common-mode signal from this input stage output signal, giving a single-ended output referred to the potential at the reference pin.

The Gain vs Frequency performance (shown in the Typical Performance Curves) illustrates the advantage of the circuit topology used in the INA103: bandwidth remains nearly constant over gain ranges from 1 to 100. This yields a gain-bandwidth product (GBW) of >100MHz at G = 1000. Gain-related errors are greatly reduced due to this high GBW. A distortion cancellation input stage and improved output stage reduce THD + N to less than 0.002% from 20Hz to 20kHz. The output can drive 200Ω loads with no crossover distortion (at 1kHz).

These performance advantages make the INA103 ideal for instrumentation amplifier applications which require low noise, excellent dynamic and spectral response, and wide bandwidth.

BASIC POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. Supplies should be decoupled with 1µF tantalum capacitors as close to the amplifier as possible. To avoid gain and CMR errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance. Resistance in series with the reference (pin 7) or the sense (pin 11) will degrade CMR. Also, to maintain stability, avoid capacitance from the output to the gain set, offset adjust, and input pins. A suggested PC board layout is shown in Figure 2.

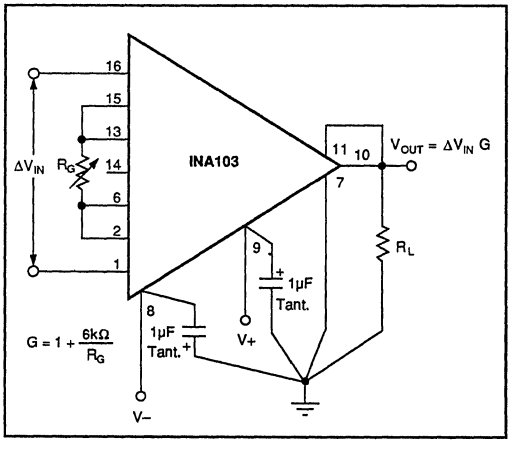


FIGURE 1. Basic Circuit Configuration.

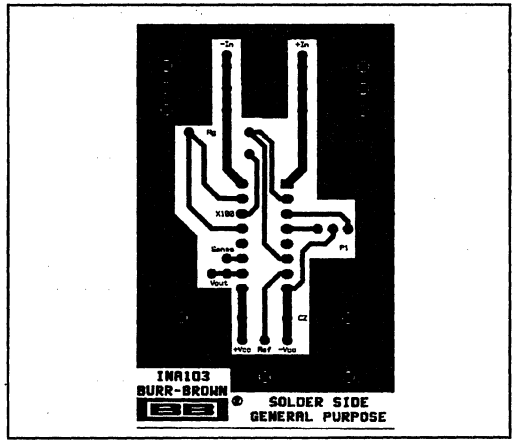


FIGURE 2. Suggested PC Board Layout for INA103. (Not Available from Burr-Brown).

OFFSET ADJUSTMENT

As with all instrumentation amplifiers, voltage offsets occur in both the input and output stages of the INA103. Input-referred voltage offsets are multiplied by the overall gain of the IA. Output-referred offsets are multiplied by the gain of the output stage (usually gain = 1). Input and output voltage offsets are actively laser-trimmed to near zero at the factory. Applications which require user voltage offset adjustment can employ one of the methods discussed below.

Output voltage offset can be adjusted using the null pins on the INA103, as shown in Figure 3. Although the null pins primarily adjust the output offset, they also have a small effect on the input offset. For 1mV of output offset change, the input offset will change approximately 1µV. Also, offset adjustment using the null pins will change the offset voltage drift of the INA103. For 1mV of offset change, the output offset drift changes by 3µV/°C. The change in input offset drift is negligible.

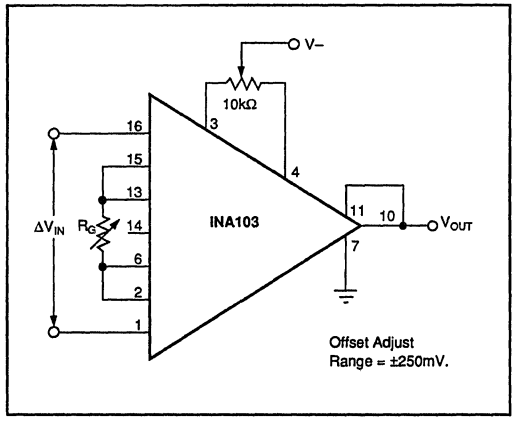


FIGURE 3. Offset Adjustment Circuit.

For output voltage offset adjustment with no effect on voltage offset drift or input voltage offset, use the circuit shown in Figure 4.

The INA103 has no trim pins for input offset adjustment. However, in AC coupled applications, input offset adjustment can be accomplished using the circuit shown in Figure 5.

The circuit shown in Figure 6 will provide automatic DC restoration for the Figure 5 circuit. The low frequency roll-off of this circuit is a function of the IA gain.

$$f_{-3dB} = \text{gain}/(12 \cdot \pi \cdot R \cdot C).$$

The circuit shown in Figure 7 can also be used for V_{OS} adjustment in floating source applications as long as the source impedance is greater than 10Ω. If the source impedance is less than 10Ω, the offset range may not be adequate to trim out the maximum input-referred V_{OS} of the INA103.

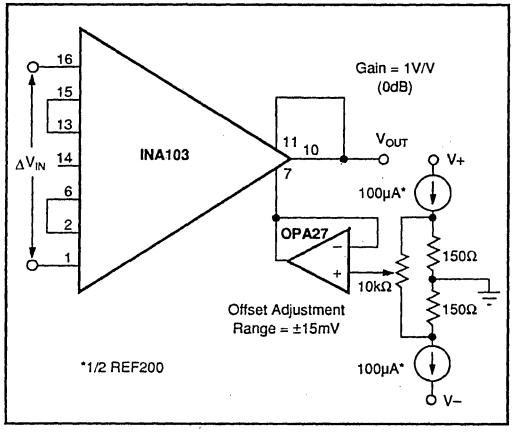


FIGURE 4. Output Offsetting.

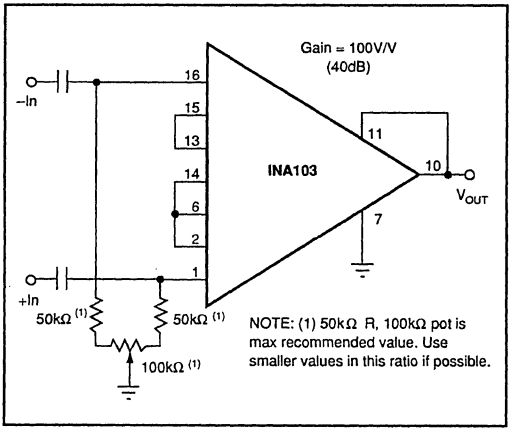


FIGURE 5. Input Offset Adjustment for AC-Coupled Inputs.

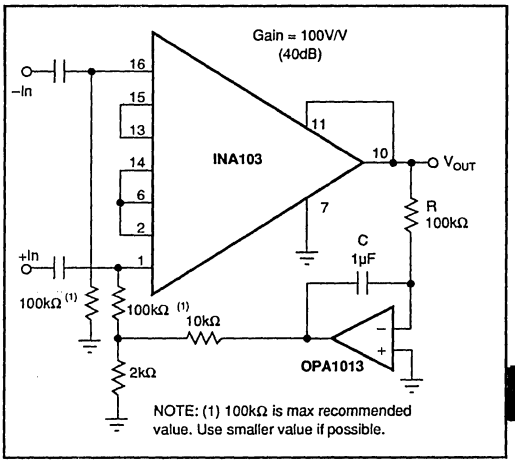


FIGURE 6. Automatic DC Restoration.

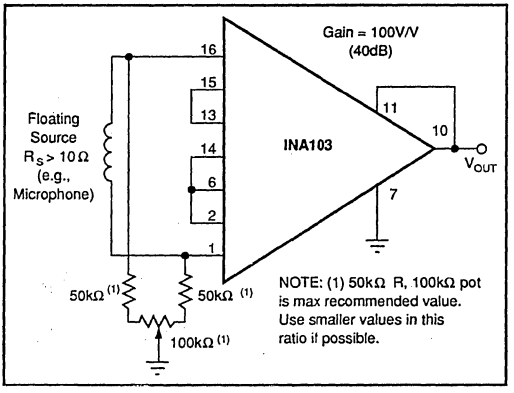


FIGURE 7. Input Offset Adjustment for Floating Source.

GAIN SELECTION

Gain selection is accomplished by strapping together the appropriate pins on the INA103. Table I shows possible gains from the internal resistors. To use the internal feedback resistors, connect pin 13 to pin 15, and pin 2 to pin 6. Keep the connections as short as possible to maintain accuracy.

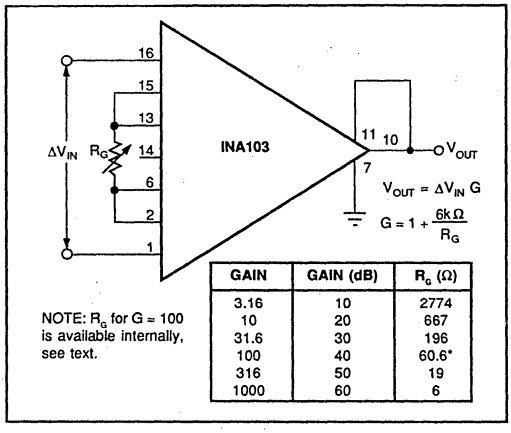
Gains other than 1 and 100 can be set by adding an external resistor, R_G, as shown in Figure 8. Gain accuracy is a function of resistor matching. For internal gains, accuracy is as shown in Table I. For external R_G, accuracy is a function of the external resistor accuracy, internal feedback resistor accuracy (typically 0.1%) and interconnection resistance (typically 0.1Ω). The equation for choosing R_G is shown below:

$$R_G = \frac{6k\Omega}{G-1}$$

where G is the gain value in V/V.

GAIN	CONNECT PIN 14 TO	GAIN ACCURACY (%)
1	None	0.01
100	Pin 2	0.1

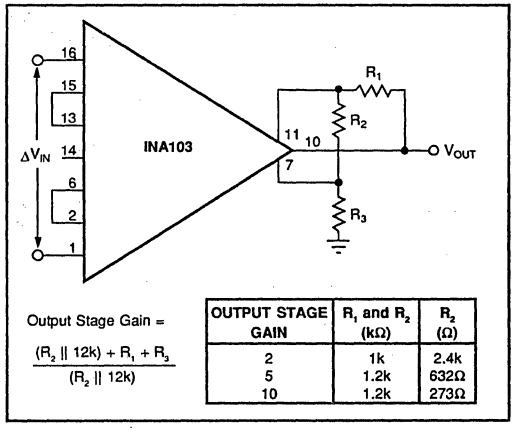
TABLE I. Internal Gain Connections.



NOTE: R_G for G = 100 is available internally, see text.

GAIN	GAIN (dB)	R_G (Ω)
3.16	10	2774
10	20	667
31.6	30	196
100	40	60.6*
316	50	19
1000	60	6

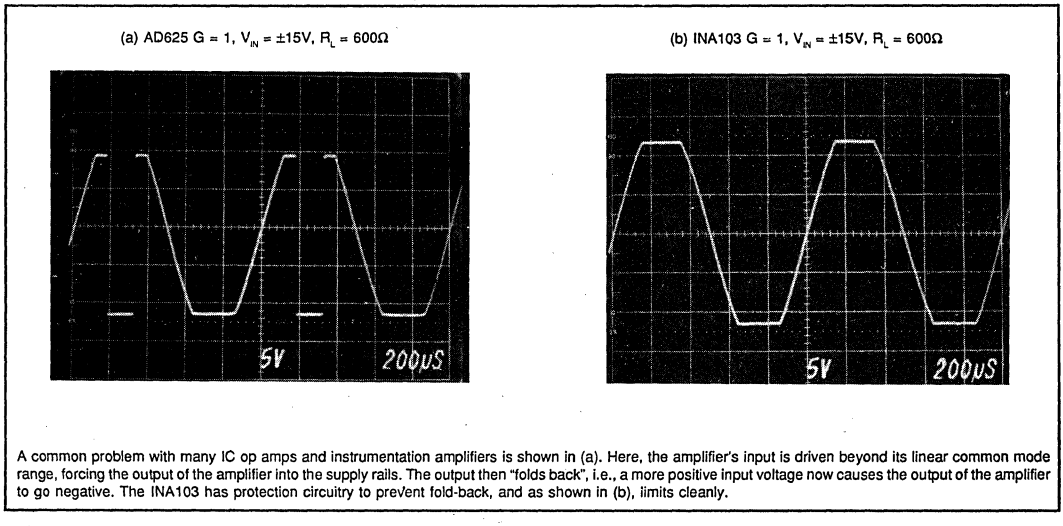
FIGURE 8. Gain Setting Using External Resistor.



Output Stage Gain = $\frac{(R_2 \parallel 12k) + R_1 + R_3}{(R_2 \parallel 12k)}$

OUTPUT STAGE GAIN	R_1 and R_2 (kΩ)	R_2 (Ω)
2	1k	2.4k
5	1.2k	632Ω
10	1.2k	273Ω

FIGURE 9. Gain Adjustment of Output Stage.



A common problem with many IC op amps and instrumentation amplifiers is shown in (a). Here, the amplifier's input is driven beyond its linear common mode range, forcing the output of the amplifier into the supply rails. The output then "folds back", i.e., a more positive input voltage now causes the output of the amplifier to go negative. The INA103 has protection circuitry to prevent fold-back, and as shown in (b), limits cleanly.

FIGURE 10. INA103 Overload Condition Performance.

COMMON-MODE INPUT RANGE

For low distortion, the differential input signal and its common-mode voltage must not cause the input amplifiers' outputs to exceed their linear output range (See Max Common-Mode Voltage vs Output Voltage curve). This can be avoided by reducing the input stage gain and increasing the output stage gain as shown in Figure 9. This is also useful for increasing total gain.

Unlike some instrumentation amplifiers, the INA103 will limit cleanly under overload conditions. See Figure 10.

OPTIONAL COMMON-MODE REJECTION TRIM

The INA103 is laser-adjusted during manufacturing to assure high CMR. However, if desired, the circuit shown in Figure 11 may be used to trim the CMR. Note that an approximate +0.2% gain error is induced.

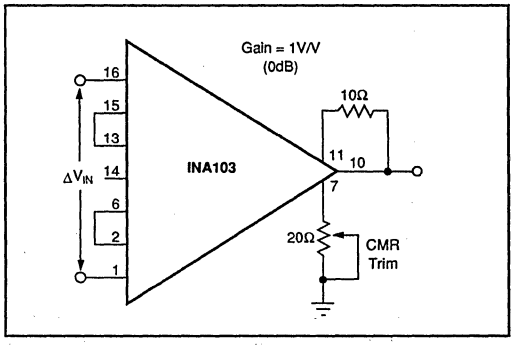


FIGURE 11. Optional Circuit for Externally Trimming CMR.

OUTPUT SENSE

An output-sense terminal allows greater accuracy in connecting the load. By attaching this feedback point at the load, IR drops due to load currents are eliminated since they are inside the feedback loop. Proper connection is shown in Figure 1. When more output current is needed, a power booster can be placed within the feedback loop as shown in Figure 12. Buffer errors are reduced by the loop gain of the output amplifier.

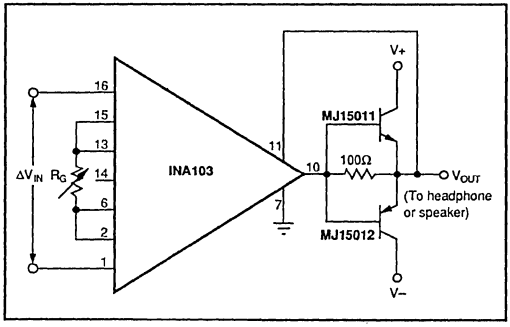


FIGURE 12. Current Boosting the Output.

INPUT IMPEDANCE AND PROTECTION CONSIDERATIONS

As with any low noise circuit, careful layout and power supply bypassing is necessary to prevent the coupling of noise sources into the INA103 through the power supply or from EMI radiation.

A return path for the input bias currents must always be provided. A resistor from the input to common will properly bias floating sources such as transformers, thermocouples, and AC-coupled inputs. This resistor should be high enough in value to prevent loading the source. The input bias currents flowing through these resistors will introduce a common-mode voltage to the amplifier, and caution should be exercised to assure that this common-mode voltage, in addition to the input signal, does not cause the input amplifiers to saturate. (See Common-Mode Input Range, above).

It is often necessary to decouple the input of the INA103 from the source (for example, in audio mixing systems where the INA103 may be placed on a buss). In this case, series resistors may be used to decouple the input. The source impedance presented to the INA103 should be as low as possible, to minimize DC errors and noise which may result due to the input bias current of the INA103. In addition, resistor values should be chosen to limit the input current to the INA103 to 10mA. While it is unlikely such currents would result from a signal input, should one power supply rail be lost due to a power supply failure or other system fault, it is possible for large currents to flow from the other power supply to ground through the input stage. Setting $R_{DECOUPLE} \geq 250\Omega$ should be adequate to provide this protection. Figure 13 shows a circuit with a decoupled and protected input. A graph is included to assist in choosing the best resistor values.

Inductive source impedances may cause the INA103 to oscillate. Placing a 470pF capacitor from each input to ground will prevent oscillation in such rare instances. Typical audio applications using twisted pair or coax generally do not require these capacitors.

APPLICATIONS

Many applications of instrumentation amplifiers involve the amplification of low-level differential signals from bridges and transducers such as strain gages, thermocouples, and RTDs. Some of the important parameters include common-mode rejection (differential cancellation of common-mode offset and noise), input impedance, offset voltage and drift, gain accuracy, linearity and noise. The INA103 accomplishes all of these with high precision.

In addition, the INA103 has been designed to provide extremely low noise and distortion for dynamic applications such as microphone preamplifiers in professional-quality mixing consoles.

Although the INA103 contains internal 3kΩ feedback resistors to set input stage gain, external feedback resistors can be used, as shown in Figure 14. For gains other than 1 or 100, it is possible to improve gain accuracy and gain temperature

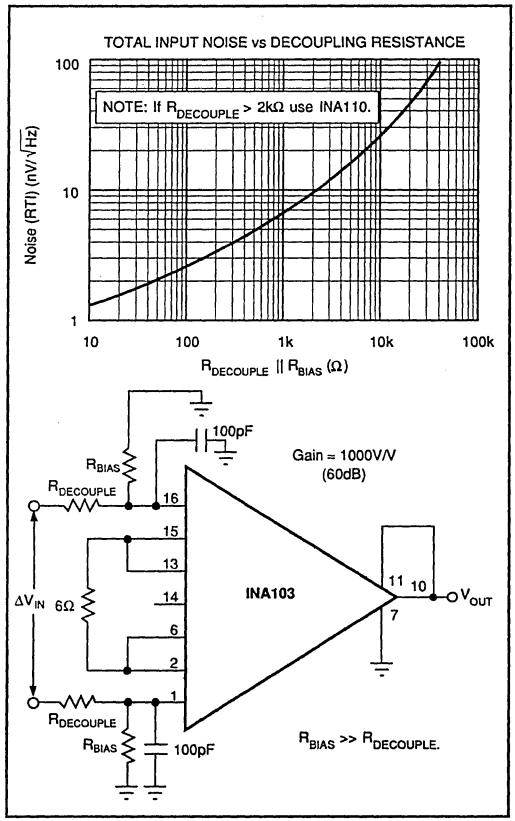


FIGURE 13. Input Decoupling and Protection.

coefficient by using matched external feedback and gain set resistors (the internal feedback resistors can have 50ppm/°C TCR). Other amplifiers, such as the AD625, have no internal feedback resistors. When using the INA103 to replace the AD625 in existing circuits, the external feedback resistors present in the existing circuit may be used (see Figure 14), or the circuit may be modified to take advantage of the INA103's internal resistors.

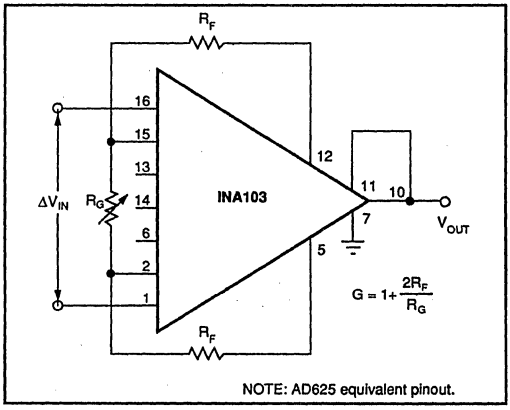


FIGURE 14. Use of External Resistors for Gain Set.

The INA103 input amplifiers are current feedback type. The value of the feedback resistors affects the dynamic performance and stability. Feedback resistors less than 2.5kΩ may result in instability. Feedback resistors larger than 3kΩ will result in reduced gain bandwidth and increased noise. For example, feedback resistors of 20kΩ will increase the gain-of-1000 input referred-noise of the INA103 from 1nV/√Hz to 1.5nV/√Hz.

Figure 15 is one way to make a microphone preamplifier with the INA103. This circuit is designed to allow the microphone to be phantom powered, and also allows for a 20dB pad on the input. The DC restoration circuit using the OPA627 has a low frequency cutoff of 1.59Hz, and automatically removes DC offsets from the amplified output signal.

Figures 16 through 19 show other applications circuits.

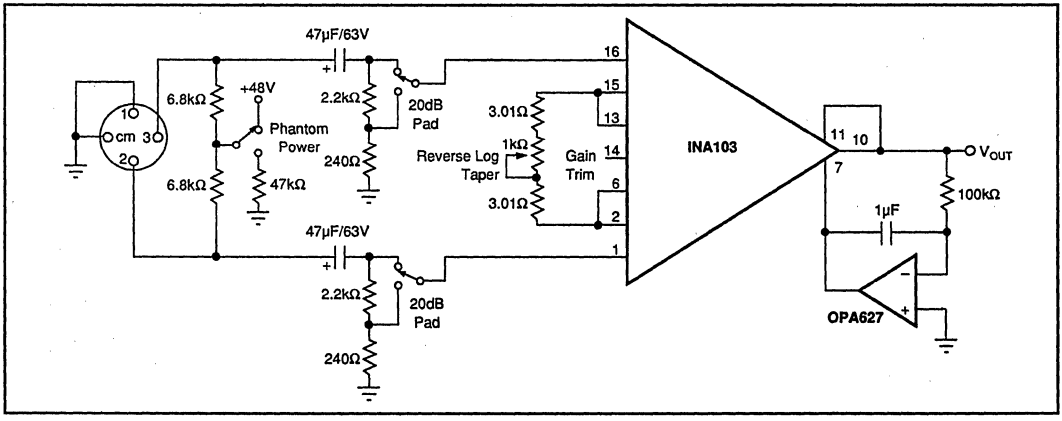


FIGURE 15.Microphone Preamplifier with Provision for Phantom Power Microphones.

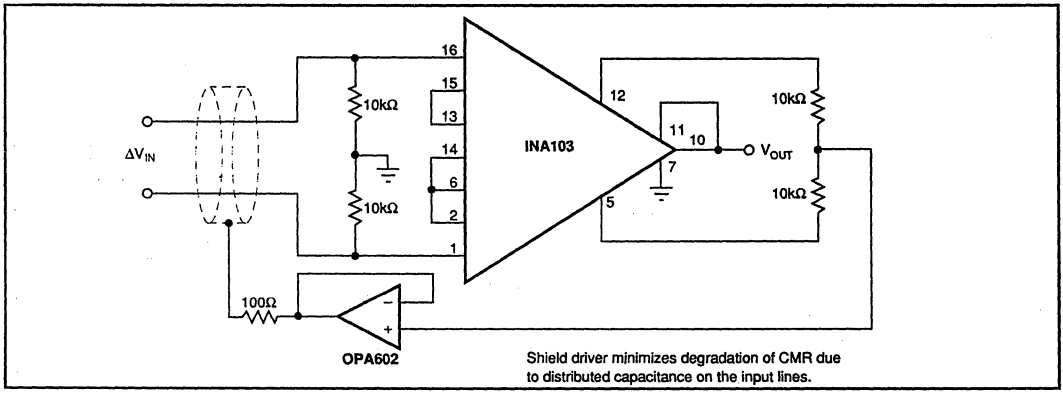


FIGURE 16. Instrumentation Amplifier with Shield Driver.

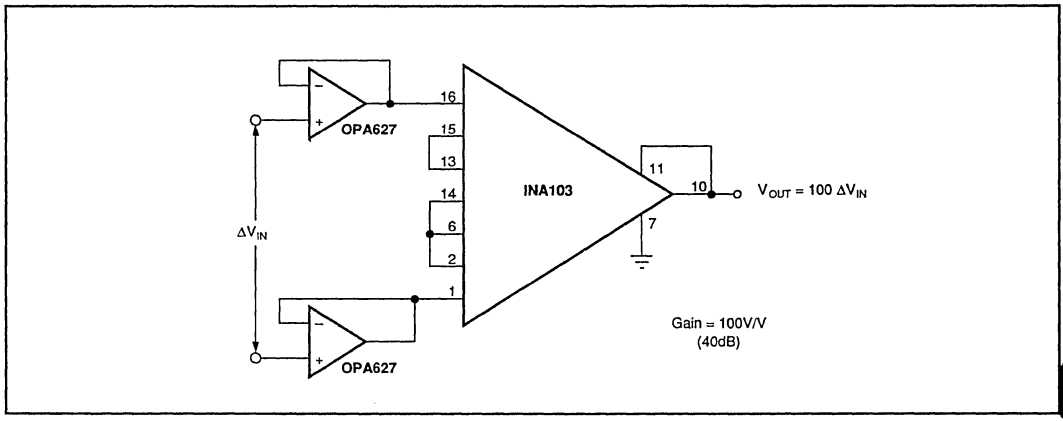


FIGURE 17. Gain-of-100 INA103 with FET Buffers.

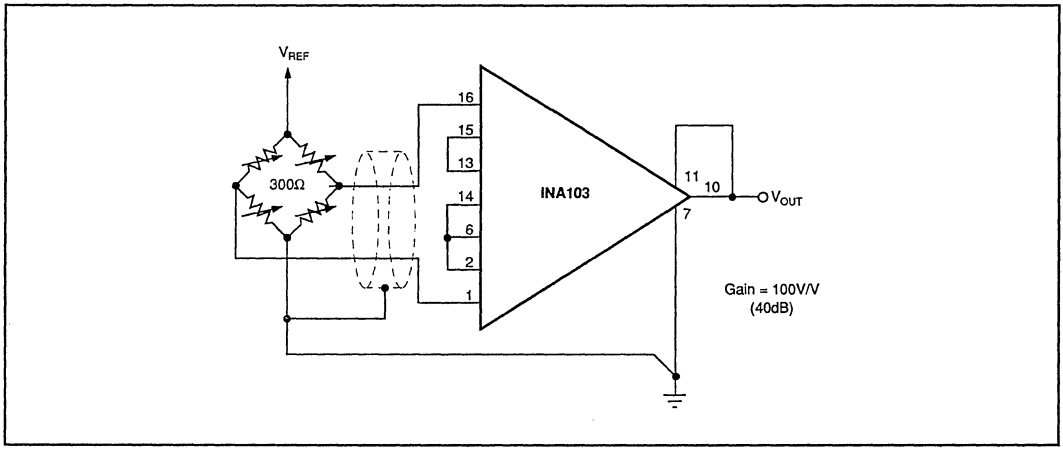


FIGURE 18. Bridge Amplifier.

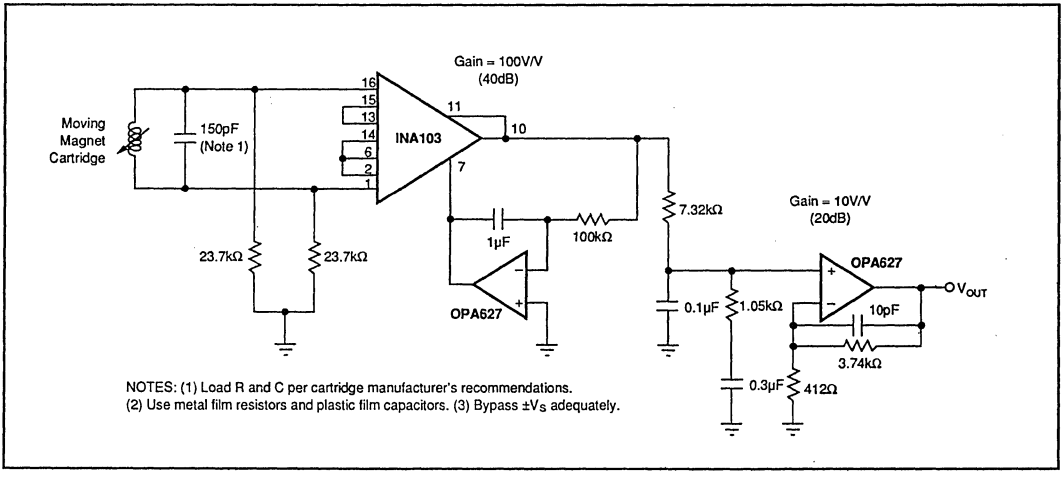
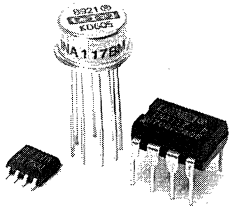


FIGURE 19. RIAA Phono Preamplifier.

BURR-BROWN®



INA117

High Common-Mode Voltage DIFFERENCE AMPLIFIER

FEATURES

- **COMMON-MODE INPUT RANGE: ±200V (V_S = ±15V)**
- **PROTECTED INPUTS: ±500V Common-Mode ±500V Differential**
- **UNITY GAIN: 0.02% Gain Error max**
- **NONLINEARITY: 0.001% max**
- **CMRR: 86dB min**

APPLICATIONS

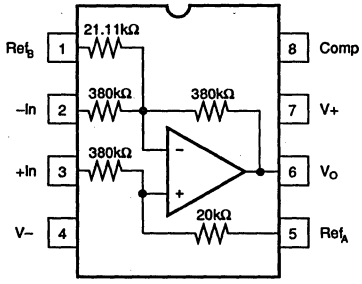
- **CURRENT MONITOR**
- **BATTERY CELL-VOLTAGE MONITOR**
- **GROUND BREAKER**
- **INPUT PROTECTION**
- **SIGNAL ACQUISITION IN NOISY ENVIRONMENTS**
- **FACTORY AUTOMATION**

DESCRIPTION

The INA117 is a precision unity-gain difference amplifier with very high common-mode input voltage range. It is a single monolithic IC consisting of a precision op amp and integrated thin-film resistor network. It can accurately measure small differential voltages in the presence of common-mode signals up to ±200V. The INA117 inputs are protected from momentary common-mode or differential overloads up to ±500V.

In many applications, where galvanic isolation is not essential, the INA117 can replace isolation amplifiers. This can eliminate costly isolated input-side power supplies and their associated ripple, noise and quiescent current. The INA117's 0.001% nonlinearity and 200kHz bandwidth are superior to those of conventional isolation amplifiers.

The INA117 is available in 8-pin plastic mini-DIP and SO-8 surface-mount packages, specified for the 0°C to +70°C temperature range. The metal TO-99 models are available specified for the –25°C to +85°C and –55°C to +125°C temperature range.



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PDS-748D

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_S = ±15V unless otherwise noted.

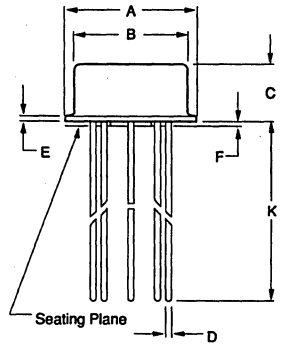
PARAMETER	CONDITIONS	INA117AM, SM			INA117BM			INA117P, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Initial [1]			1			•			•		V/V
Error			0.01	0.05		•	0.02		•	•	%
vs Temperature			2	10			•		•		ppm/°C
Nonlinearity [2]			0.0002	0.001		•	•		•	•	%
OUTPUT											
Rated Voltage	I_O = +20mA, –5mA	10	12		•	•		•	•		V
Rated Current	V_O = 10V	+20, –5			•			•			mA
Impedance			0.01			•			•		Ω
Current Limit	To Common		+49, –13			•			•		mA
Capacitive Load	Stable Operation		1000			•			•		pF
INPUT											
Impedance	Differential		800			•			•		kΩ
	Common-Mode		400			•			•		kΩ
Voltage Range	Differential	±10				•			•		V
	Common-Mode, Continuous	±200			•			•			V
Common-Mode Rejection [3]											
DC		70	80		86	94		•	•		dB
AC, 60Hz	V_{CM} = 400Vp-p	66	80		66	94		•	•		dB
vs Temperature, DC	$T_A = T_{MIN}$ to T_{MAX}										
AM, BM, P, KU		66	75		80	90			•		dB
SM		60	75								dB
OFFSET VOLTAGE	RTO [4]										
Initial			120	1000		•	1000		•	•	µV
KU Grade (SO-8 Package)									600	2000	µV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}		8.5	40		•	20		•		µV/°C
vs Supply	V_S = ±5V to ±18V	74	90		80	•		•	•		dB
vs Time			200			•			•		µV/mo
OUTPUT NOISE VOLTAGE	RTO [5]										
f_B = 0.01Hz to 10Hz			25			•			•		µVp-p
f_B = 10kHz			550			•			•		nV/√Hz
DYNAMIC RESPONSE											
Gain Bandwidth, –3dB			200			•			•		kHz
Full Power Bandwidth	V_O = 20Vp-p	30			•			•			kHz
Slew Rate		2	2.6		•	•		•	•		V/µs
Settling Time: 0.1%	V_O = 10V Step		6.5			•			•		µs
0.01%	V_O = 10V Step		10			•			•		µs
0.01%	V_{CM} = 10V Step, V_{DIFF} = 0V		4.5			•			•		µs
POWER SUPPLY											
Rated			±15			•			•		V
Voltage Range	Derated Performance	±5		±18	•		•	•		•	V
Quiescent Current	V_O = 0V		1.5	2		•	•		•	•	mA
TEMPERATURE RANGE											
Specification: AM, BM, P, KU		–25		+85	•		•	0		+70	°C
SM		–55		+125							°C
Operation		–55		+125	•		•	–25		+85	°C
Storage		–65		+150	•		•	–40		+85	°C

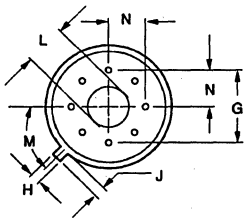
*Specification same as for INA117AM.

NOTES: (1) Connected as difference amplifier (see Figure 1). (2) Nonlinearity is the maximum peak deviation from the best-fit straight line as a percent of full-scale peak-to-peak output. (3) With zero source impedance (see discussion of common-mode rejection in Application Information section). (4) Includes effects of amplifier's input bias and offset currents. (5) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.

MECHANICAL

M Package — Metal TO-99

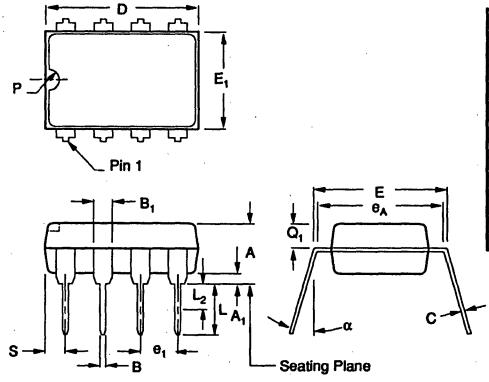




DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Tab is pin 8.

P Package — 8-Pin Plastic DIP

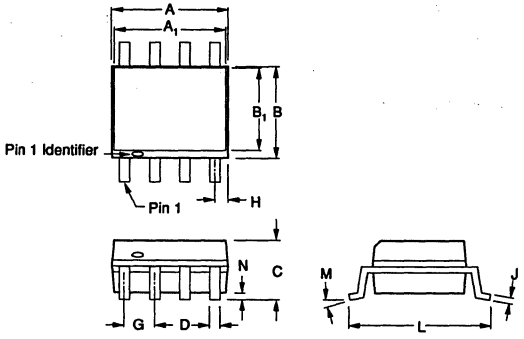


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D(1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2(2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q1	.040	.075	1.02	1.91
S(1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e_1 and e_A applies in zone L_2 when unit installed.
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

U Package — 8-Pin SOIC



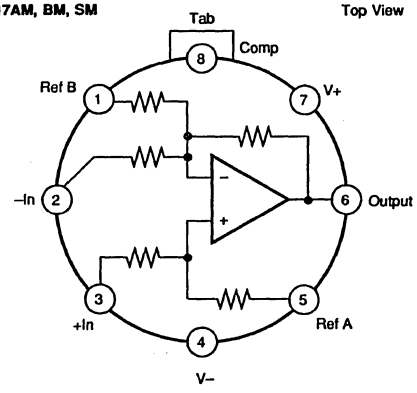
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.201	4.70	5.11
A1	.178	.201	4.52	5.11
B	.146	.162	3.71	4.11
B1	.130	.149	3.30	3.78
C	.054	.145	1.37	3.69
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.018	.026	0.46	0.66
J	.008	.012	0.20	0.30
L	.220	.252	5.59	6.40
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

PIN CONFIGURATION

Metal TO-99
INA117AM, BM, SM

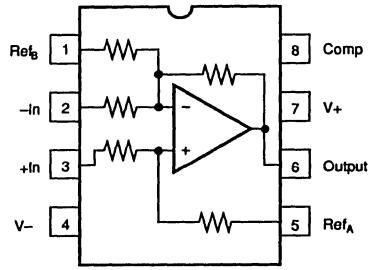
Top View



Case internally connected to V–. Make no connection.

Plastic DIP and SOIC
INA117P, KU

Top View



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Input Voltage Range, Continuous	±200V
Common-Mode and Differential, 10s	±500V
Operating Temperature	
M Metal TO-99 Package	–55 to +125°C
P Plastic DIP and U SO-8	–40 to +85°C
Storage Temperature	
M Package	–65 to +125°C
P Plastic DIP and U SO-8	–40 to +85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Common	Continuous

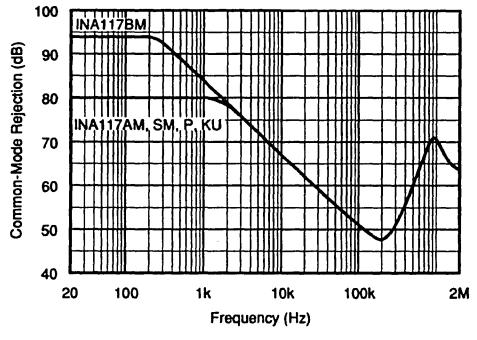
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA117P	Plastic DIP	0°C to +70°C
INA117KU	SO-8 Surface-Mount	0°C to +70°C
INA117AM	TO-99 Metal	–25°C to +85°C
INA117BM	TO-99 Metal	–25°C to +85°C
INA117SM	TO-99 Metal	–55°C to +125°C

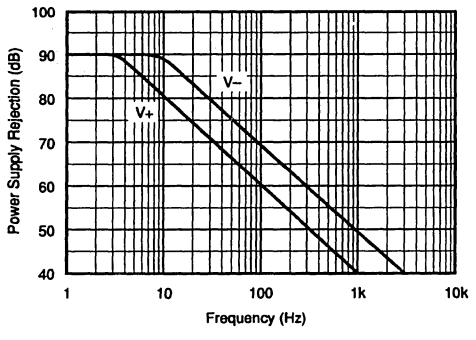
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

COMMON-MODE REJECTION vs FREQUENCY



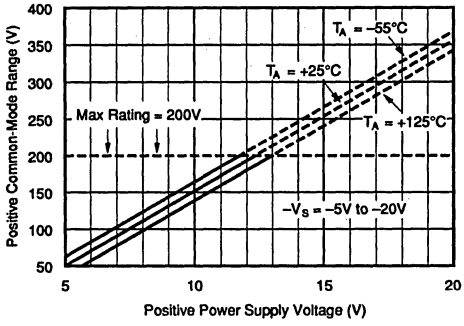
POWER SUPPLY REJECTION vs FREQUENCY



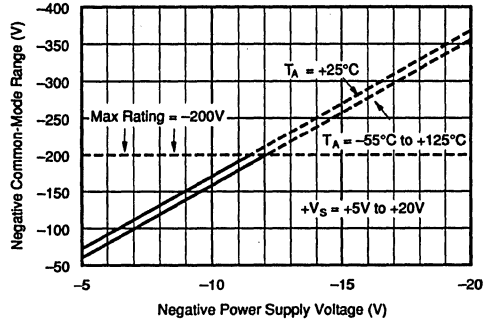
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

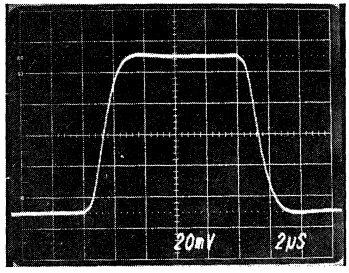
POSITIVE COMMON-MODE VOLTAGE RANGE
vs POSITIVE POWER SUPPLY VOLTAGE



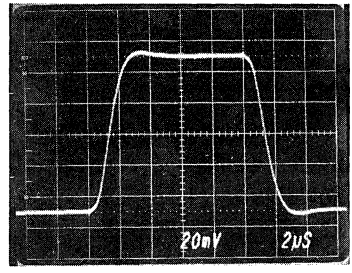
NEGATIVE COMMON-MODE VOLTAGE RANGE
vs NEGATIVE POWER SUPPLY VOLTAGE



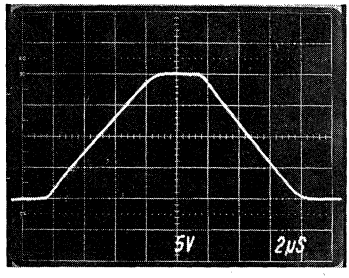
SMALL SIGNAL STEP RESPONSE
C_L = 0



SMALL SIGNAL STEP RESPONSE
C_L = 1000pF



LARGE SIGNAL STEP RESPONSE



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation.

Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins.

The output voltage is equal to the differential input voltage between pins 2 and 3. The common mode input voltage is rejected.

Internal circuitry connected to the compensation pin 8 cancels the parasitic distributed capacitance between the feedback resistor, R_2, and the IC substrate. For specified dynamic performance, pin 8 should be grounded or connected through a 0.1µF capacitor to an AC ground such as V+.

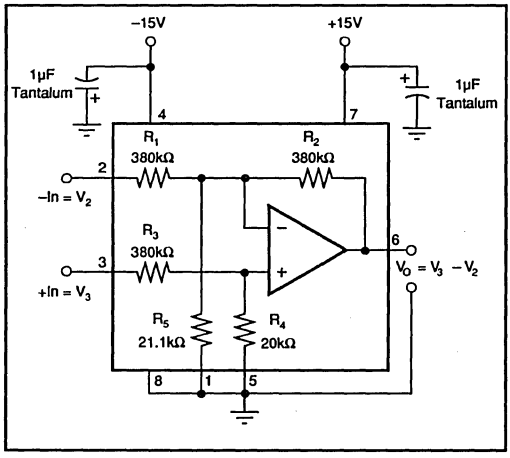


FIGURE 1. Basic Power and Signal Connections.

COMMON-MODE REJECTION

Common-mode rejection (CMR) of the INA117 is dependent on the input resistor network, which is laser-trimmed for accurate ratio matching. To maintain high CMR, it is important to have low source impedances driving the two inputs. A 75Ω resistance in series with pin 2 or 3 will decrease CMR from 86dB to 72dB.

Resistance in series with the reference pins will also degrade CMR. A 4Ω resistance in series with pin 1 or 5 will decrease CMRR from 86dB to 72dB.

Most applications do not require trimming. Figures 2 and 3 show optional circuits that may be used for trimming offset voltage and common-mode rejection.

TRANSFER FUNCTION

Most applications use the INA117 as a simple unity-gain difference amplifier. The transfer function is:

$$V_O = V_3 - V_2$$

V_3 and V_2 are the voltages at pins 3 and 2.

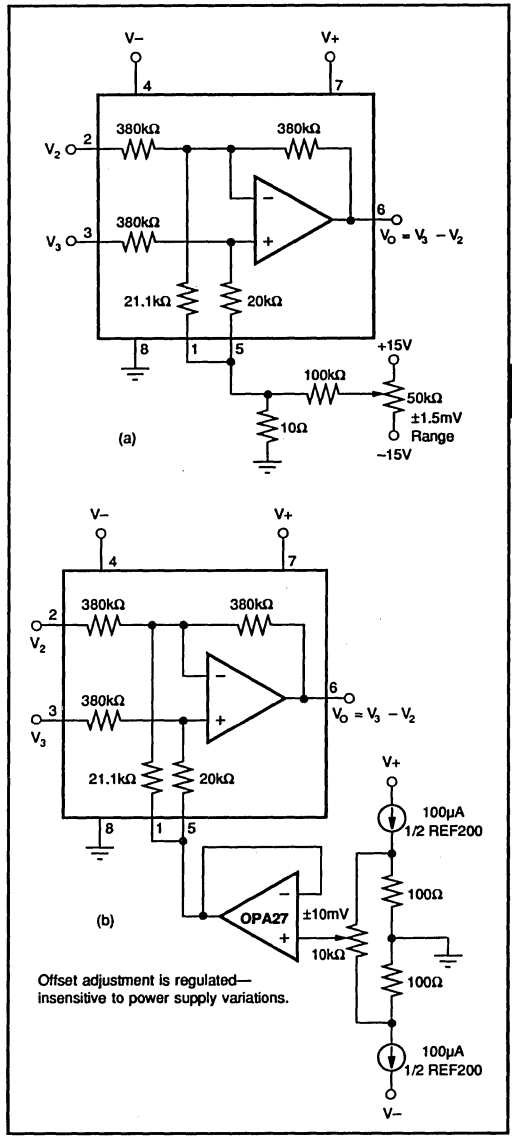


FIGURE 2. Offset Voltage Trim Circuits.

Some applications, however, apply voltages to the reference terminals (pins 1 and 5). A more complete transfer function is:

$$V_O = V_3 - V_2 + 19 \cdot V_5 - 18 \cdot V_1$$

V_5 and V_1 are the voltages at pins 5 and 1.

MEASURING CURRENT

The INA117 can be used to measure a current by sensing the voltage drop across a series resistor, R_S. Figure 4 shows the INA117 used to measure the supply currents of a device under test. The circuit in Figure 5 measures the output current of a power supply. If the power supply has a sense connection, it can be connected to the output side of R_S to eliminate the voltage-drop error. Another common application is current-to-voltage conversion as shown in Figure 6.

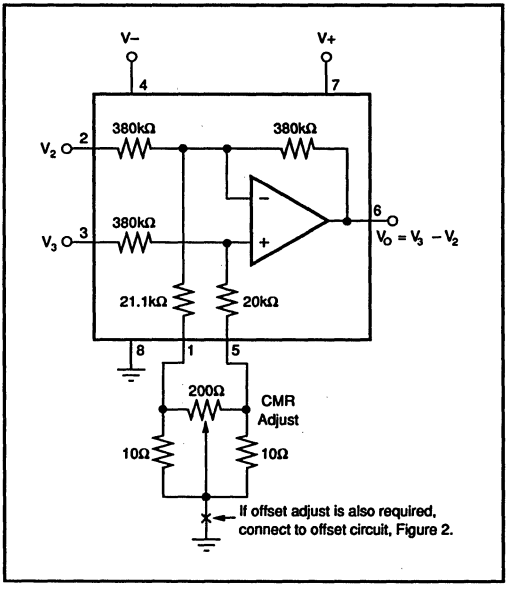


FIGURE 3. CMR Trim Circuit.

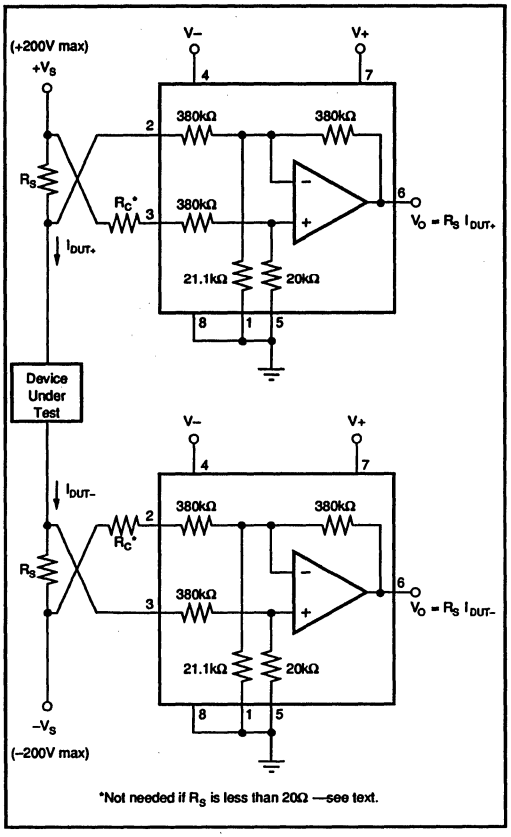


FIGURE 4. Measuring Supply Currents of Device Under Test.

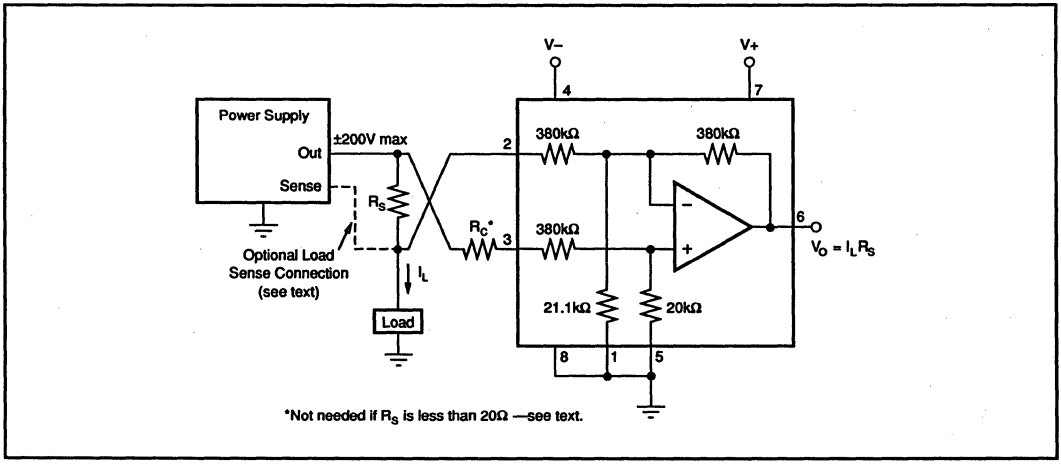


FIGURE 5. Measuring Power Supply Output Current.

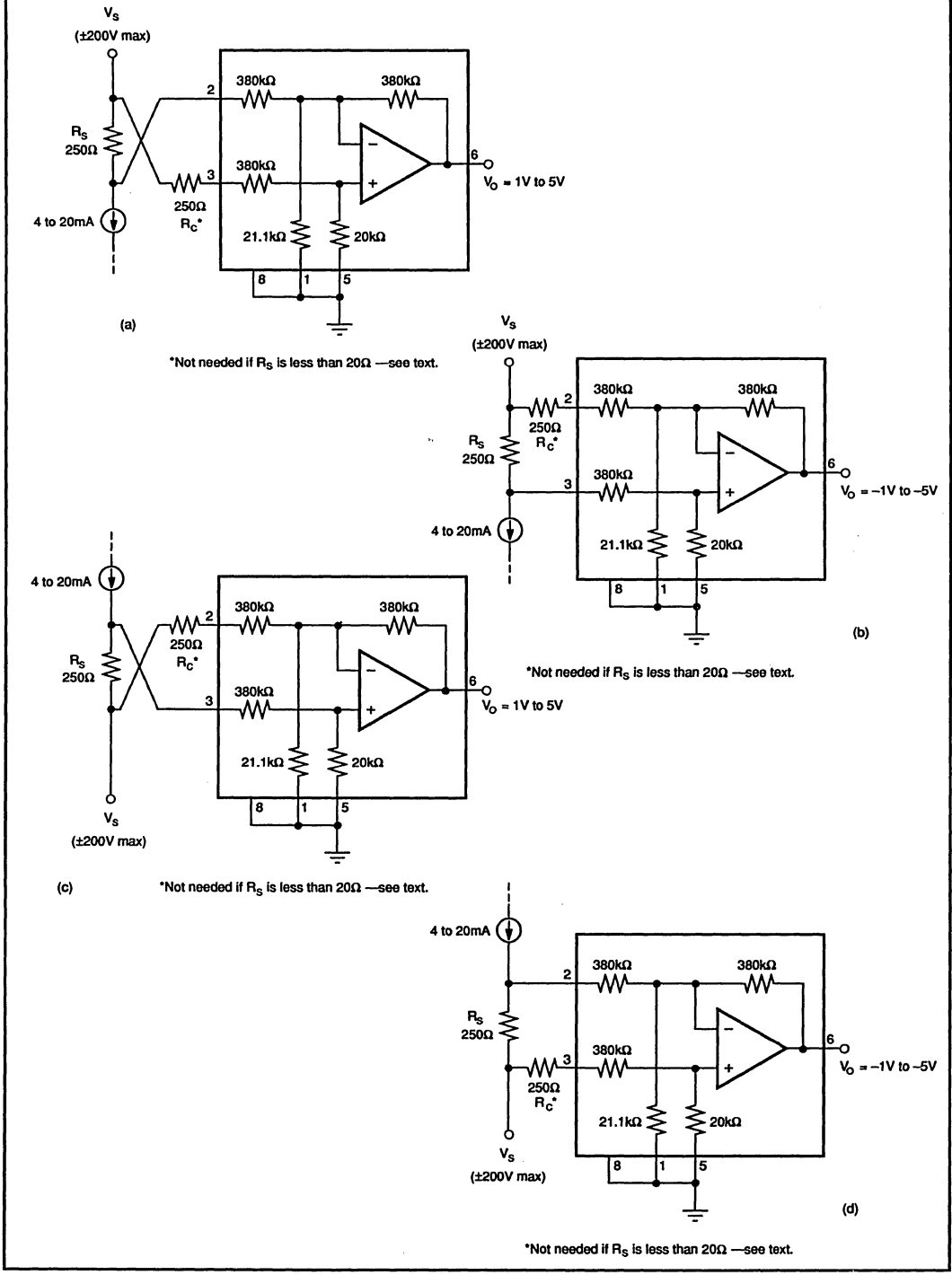


FIGURE 6. Current to Voltage Converter.

In all cases, the sense resistor imbalances the input resistor matching of the INA117, degrading its CMR. Also, the input impedance of the INA117 loads R_S, causing gain error in the voltage-to-current conversion. Both of these errors can be easily corrected.

The CMR error can be corrected with the addition of a compensation resistor, R_C, equal in value to R_S as shown in Figures 4, 5, and 6. If R_S is less than 20Ω, the degradation in CMR is negligible and R_C can be omitted. If R_S is larger than approximately 2kΩ, trimming R_C may be required to achieve greater than 86dB CMR. This is because the actual INA117 input impedances have 1% typical mismatch.

If R_S is more than approximately 100Ω, the gain error will be greater than the 0.02% specification of the INA117. This gain error can be corrected by slightly increasing the value of R_S. The corrected value, R_S', can be calculated by—

$$R_S' = \frac{R_S \cdot 380k\Omega}{380k\Omega - R_S}$$

Example: For a 1V/mA transfer function, the nominal, uncorrected value for R_S would be 1kΩ. A slightly larger value, $R_S' = 1002.6\Omega$, compensates for the gain error due to loading.

The 380kΩ term in the equation for R_S' has a tolerance of ±25%, so sense resistors above approximately 400Ω may require trimming to achieve gain accuracy better than 0.02%.

Of course, if a buffer amplifier is added as shown in Figure 7, both inputs see a low source impedance, and the sense resistor is not loaded. As a result, there is no gain error or CMR degradation. The buffer amplifier can operate as a unity gain buffer or as an amplifier with noninverting gain. Gain added ahead of the INA117 improves both CMR and signal-to-noise. Added gain also allows a lower voltage drop across the sense resistor. The OPA1013 is a good choice for the buffer amplifier since both its input and output can swing close to its negative power supply.

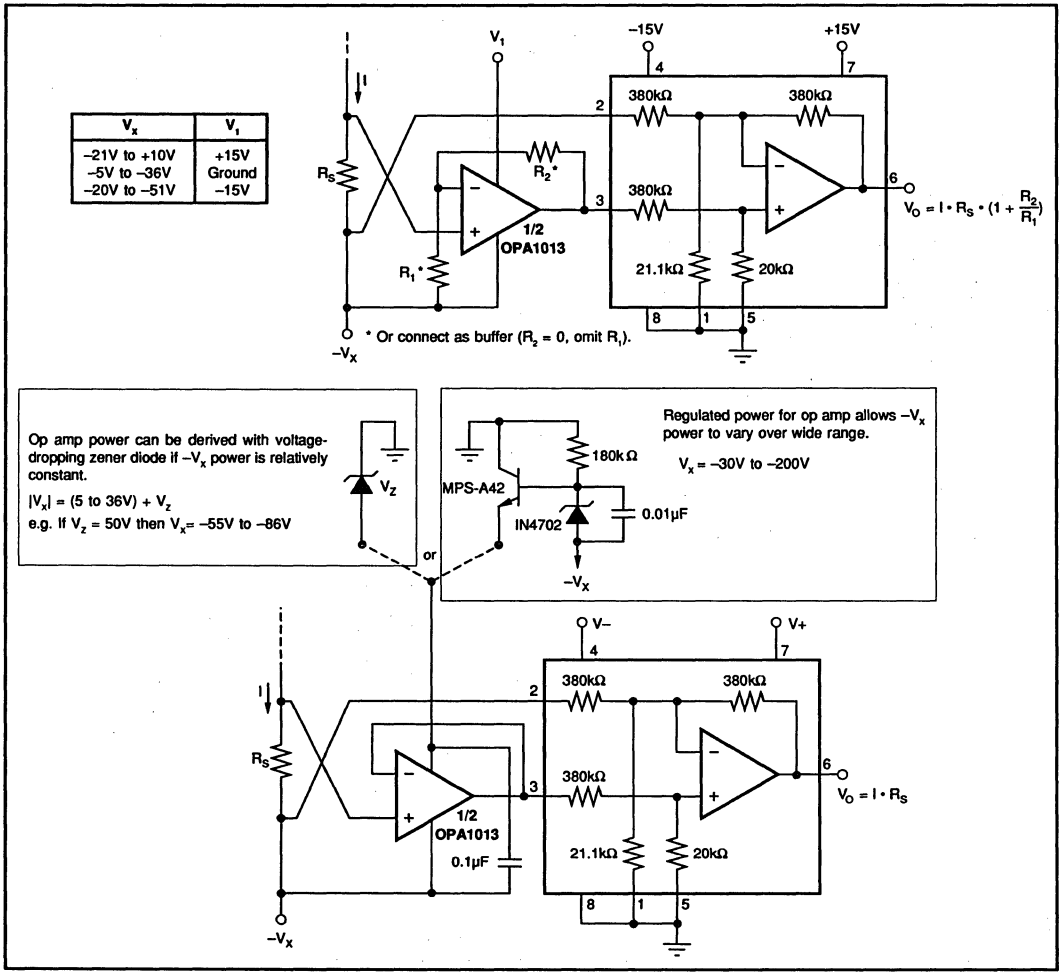


FIGURE 7. Current Sensing with Input Buffer.

Figure 8 shows very high input impedance buffer used to measure low leakage currents. Here, the buffer op amp is powered with an isolated, split-voltage power supply. Using an isolated power supply allows full ±200V common-mode input range.

NOISE PERFORMANCE

The noise performance of the INA117 is dominated by the internal resistor network. The thermal or Johnson noise of these resistors produces approximately 550nV/√Hz noise. The internal op amp contributes virtually no excess noise at frequencies above 100Hz.

Many applications may be satisfied with less than the full 200kHz bandwidth of the INA117. In these cases, the noise can be reduced with a low-pass filter on the output. The two-pole filter shown in Figure 9 limits bandwidth to 1kHz and reduces noise by more than 15:1. Since the INA117 has a 1/f noise corner frequency of approximately 100Hz, a cutoff frequency below 100Hz will not further reduce noise.

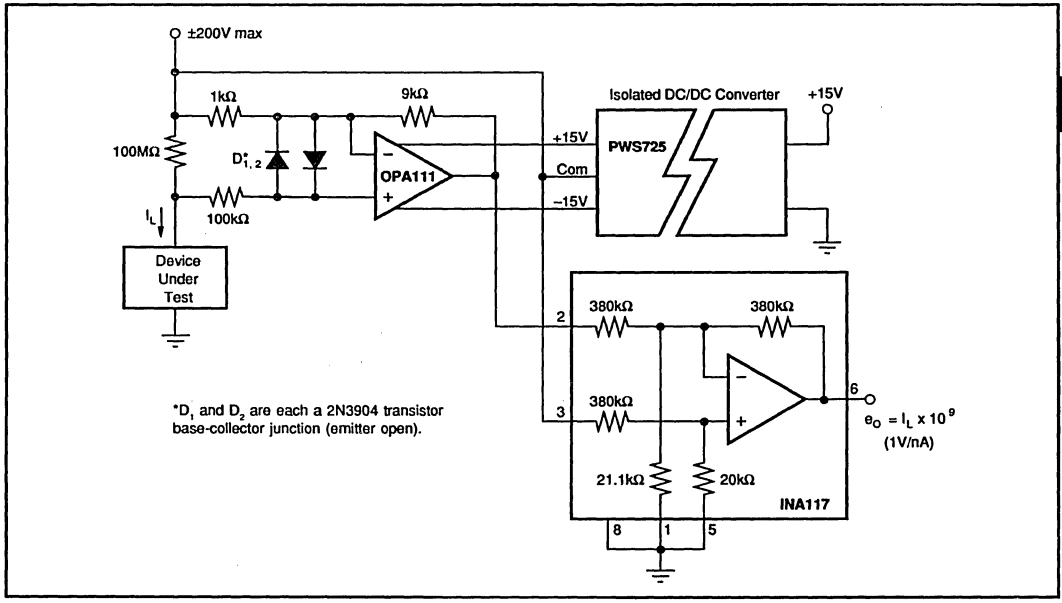
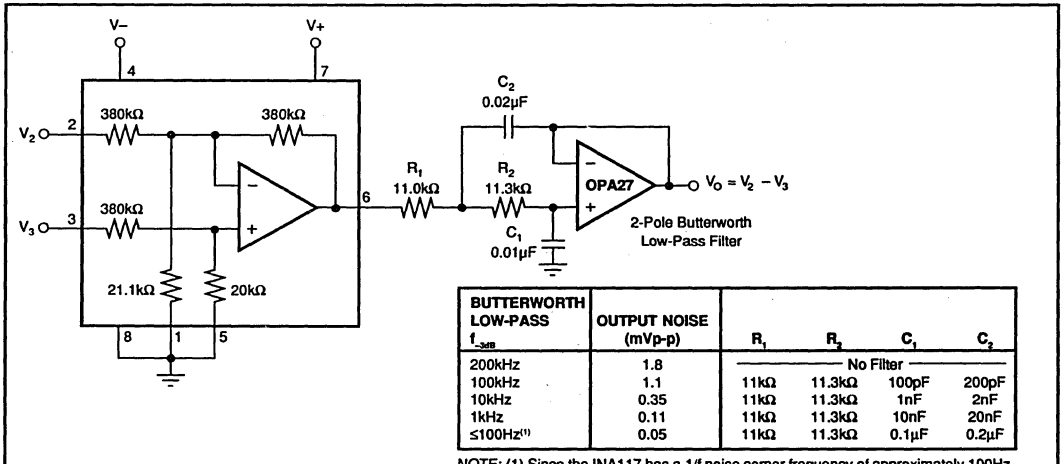


FIGURE 8. Leakage Current Measurement Circuit.

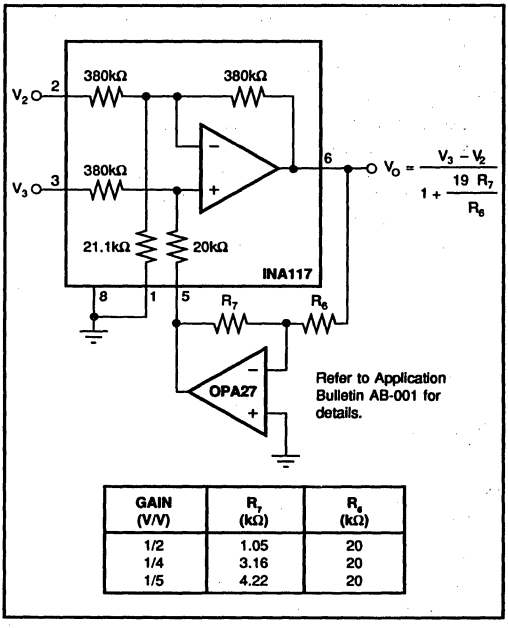


BUTTERWORTH LOW-PASS f_{-3dB}	OUTPUT NOISE (mVp-p)	R_1	R_2	C_1	C_2
200kHz	1.8	No Filter			
100kHz	1.1	11kΩ	11.3kΩ	100pF	200pF
10kHz	0.35	11kΩ	11.3kΩ	1nF	2nF
1kHz	0.11	11kΩ	11.3kΩ	10nF	20nF
≤100Hz(1)	0.05	11kΩ	11.3kΩ	0.1µF	0.2µF

NOTE: (1) Since the INA117 has a 1/f noise corner frequency of approximately 100Hz, bandwidth reduction below this frequency will not significantly reduce noise.

See Application Bulletin AB-017 for other filters.

FIGURE 9. Output Filter for Noise Reduction.



GAIN (V/V)	R_7 (kΩ)	R_6 (kΩ)
1/2	1.05	20
1/4	3.16	20
1/5	4.22	20

FIGURE 10. Reducing Differential Gain.

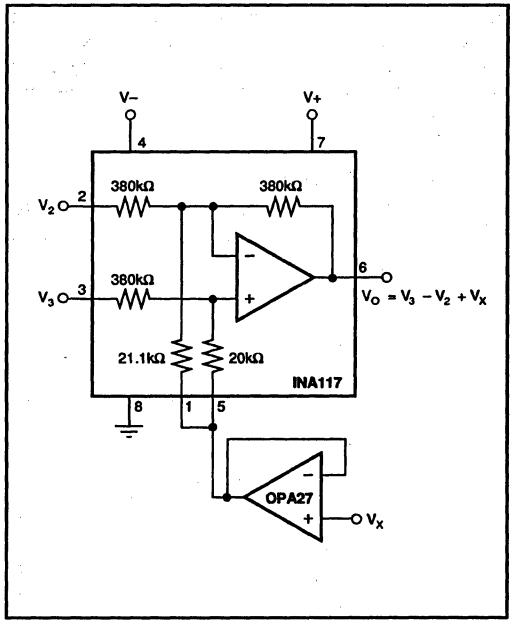


FIGURE 11. Summing V_X in Output.

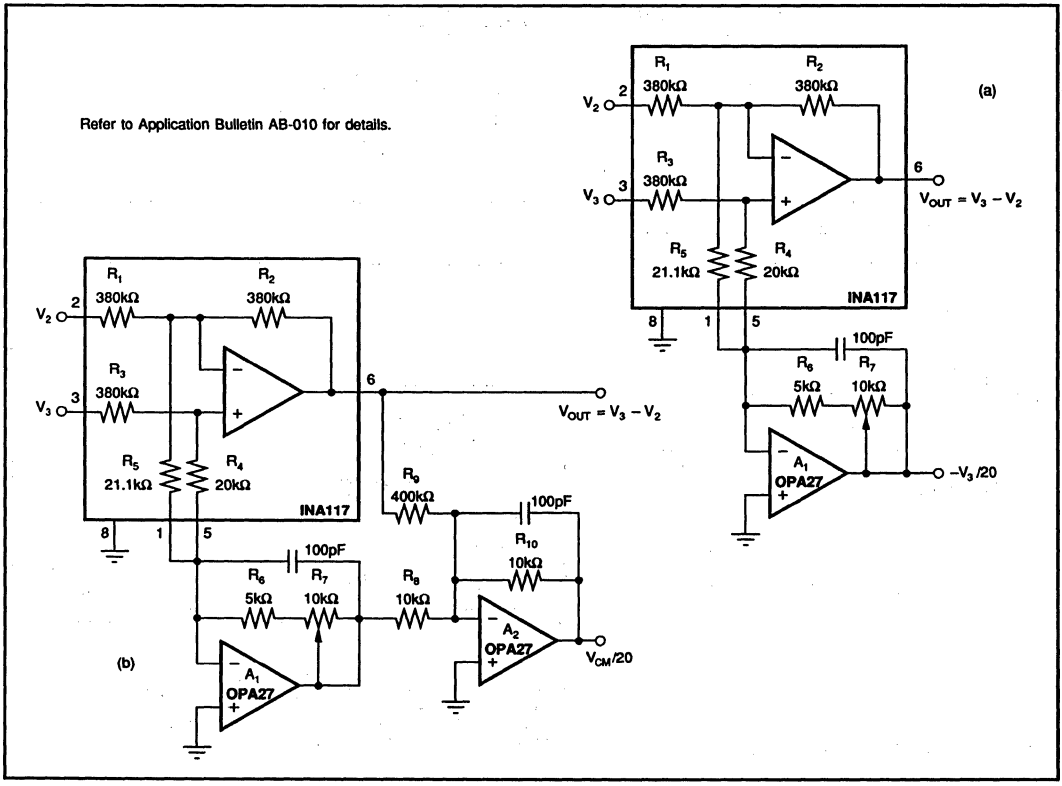


FIGURE 12. Common-Mode Voltage Monitoring.

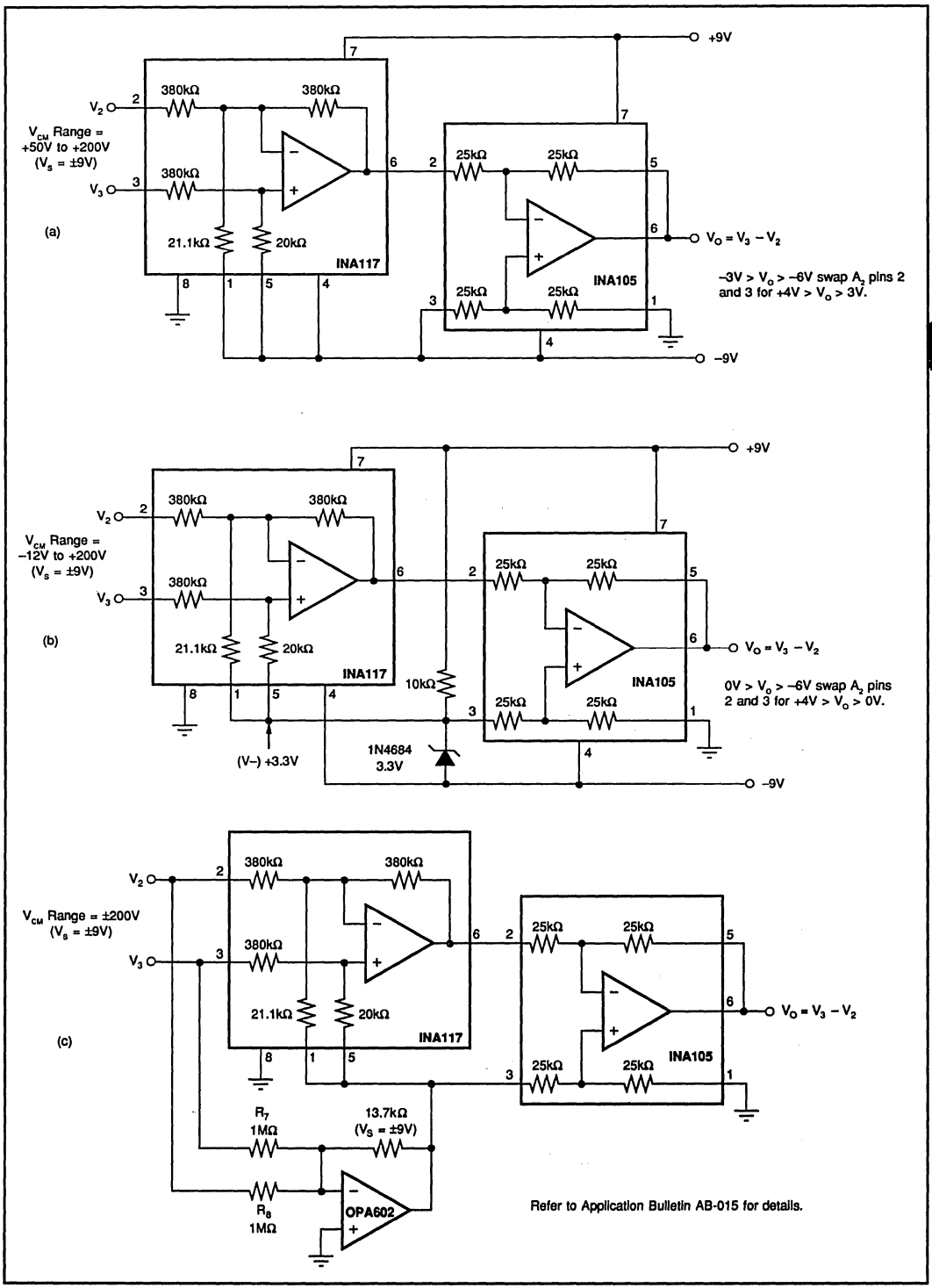


FIGURE 13. Offsetting or Boosting Common-Mode Voltage Range for Reduced Power Supply Voltage Operation.

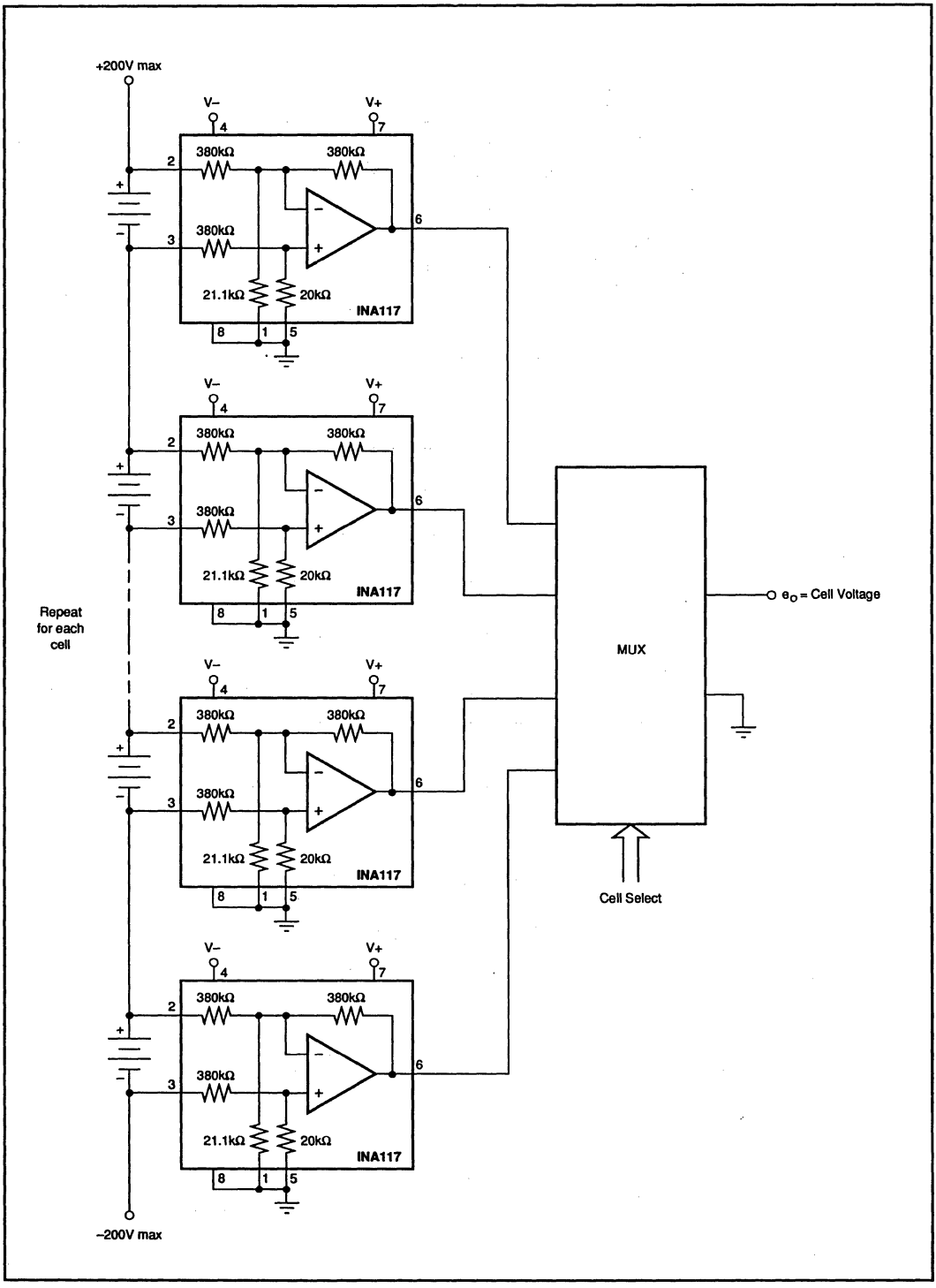


FIGURE 14. Battery Cell Voltage Monitor.

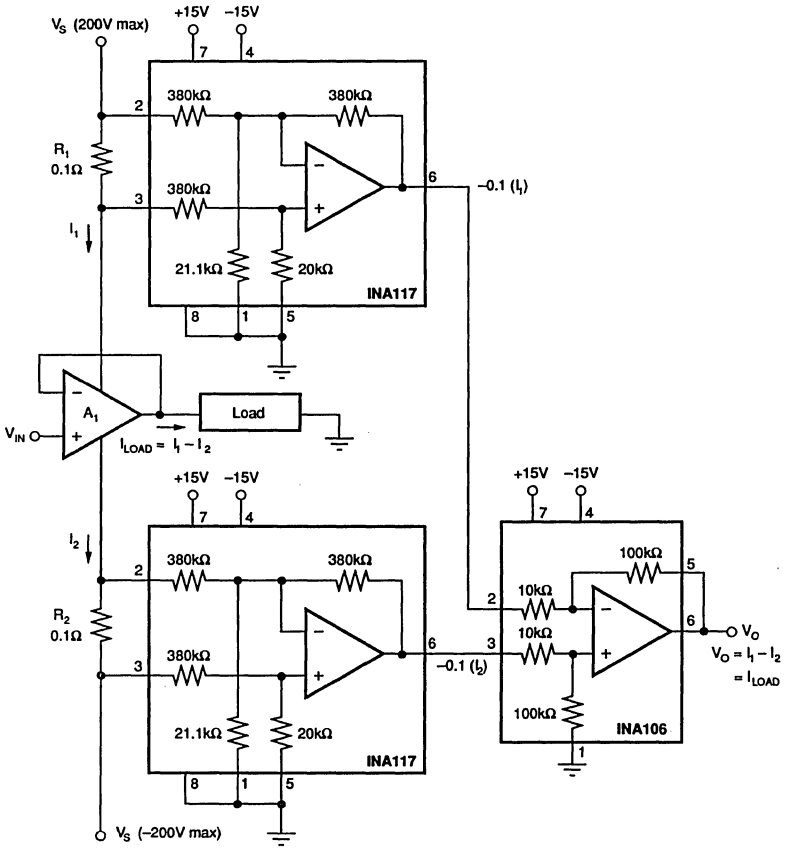


FIGURE 15. Measuring Amplifier Load Current.

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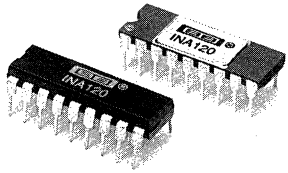


INA120

Precision INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 25μV max
- LOW OFFSET VOLTAGE DRIFT: 0.25μV/°C max
- PIN-STRAPPED GAINS: 1, 10, 100, 1000
- LOW GAIN DRIFT: 30ppm/°C max at G = 100
- HIGH COMMON-MODE REJECTION: 106dB at 60Hz, G = 100

APPLICATIONS

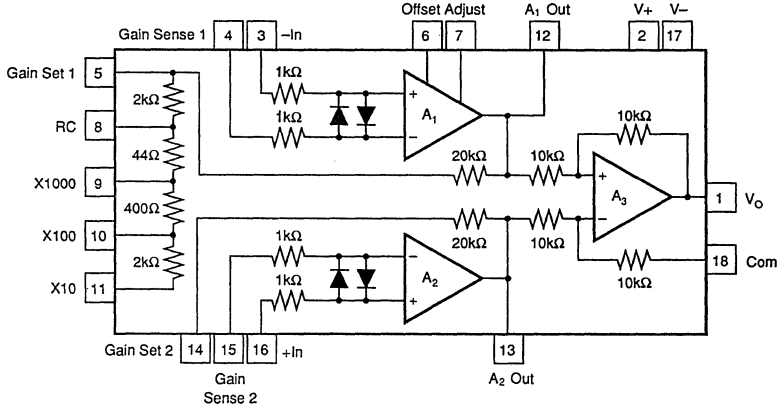
- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION SYSTEM
- SWITCHED-GAIN AMPLIFIER

DESCRIPTION

The INA120 is a precision instrumentation amplifier ideal for accurate signal acquisition. It combines precision, protected-input operational amplifiers, laser-trimmed gain-setting resistors, and a high common-mode rejection difference amplifier on a single chip.

Simple pin-strapped connections set precise gains of 1, 10, 100 or 1000. External resistors can be used to set any gain from one to 5000. Gains can be digitally selected with an external multiplexer. Gain-sense connections on the INA120 maintain accuracy when using multiplexer or gain-switching circuitry. Low power dissipation and careful on-chip thermal management reduce warm-up drift and assure excellent long-term stability.

The INA120 is available in both plastic and ceramic 18-pin DIP packages, specified for the industrial temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

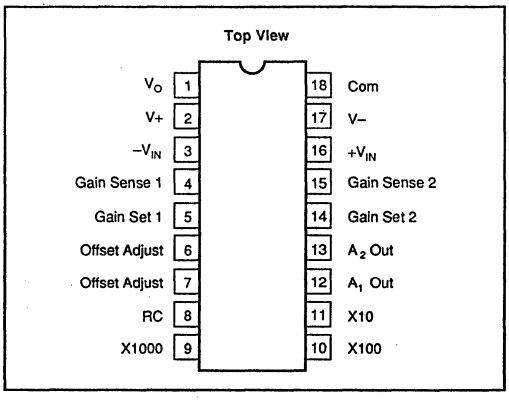
SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_S = ±15V unless otherwise specified.

PARAMETER	CONDITIONS	INA120CG MIN	INA120CG TYP	INA120CG MAX	INA120BG/BP MIN	INA120BG/BP TYP	INA120BG/BP MAX	INA120AP MIN	INA120AP TYP	INA120AP MAX	UNITS
GAIN											
Range of Gain		1		1000	1		1000	1		1000	V/V
Gain Equation			$1 + (2R_F/R_G)$			$1 + (2R_F/R_G)$			$1 + (2R_F/R_G)$		V/V
Gain Error	G = 1		0.01	0.05		0.01	0.05		0.02	0.1	%
	G = 10		0.05	0.1		0.05	0.2		0.1	0.2	%
	G = 100		0.1	0.2		0.1	0.3		0.2	0.5	%
	G = 1000		0.3	0.5		0.3	1		0.5	1	%
Gain Temp Coefficient	G = 1		4	10		4	20		6	20	ppm/°C
	G = 10		4	10		4	20		8	40	ppm/°C
	G = 100		6	30		6	40		10	60	ppm/°C
	G = 1000		22	50		22	50		40	100	ppm/°C
Nonlinearity	G = 1		0.001	0.005		0.001	0.01		0.001	0.01	% of FS
	G = 10		0.002	0.005		0.002	0.01		0.002	0.01	% of FS
	G = 100		0.004	0.01		0.004	0.02		0.004	0.02	% of FS
	G = 1000		0.008	0.05		0.008	0.1		0.008	0.1	% of FS
OFFSET VOLTAGE											
Initial Offset			(10+ 300/G)	(25+ 600/G)		(50+ 300/G)	(100+ 1000/G)		(50+ 600/G)	(200+ 2000/G)	µV
vs Temperature			(.25 + 10/G)			(1 + 20/G)			(2 + 20/G)		µV/°C
vs Power Supply	V_S = ±6V to ±18V		(1 + 20/G)	(10 + 150/G)		(1 + 20/G)	(20 + 250/G)		(1 + 20/G)	(40 + 300/G)	µV/V
INPUT BIAS CURRENT											
Initial Bias Current			±7	±20		±7	±20		±20	±50	nA
vs Temperature			±0.2			±0.2			±0.2		nA/°C
Initial Offset Current			±5	±10		±5	±20		±10	±50	nA
vs Temperature			±0.2			±0.2			±0.2		nA/°C
Impedance: Differential			10^{10} || 3			10^{10} ||·3			10^{10} || 3		Ω || pF
Common-Mode			10^{10} || 3			10^{10} || 3			10^{10} || 3		Ω || pF
INPUT VOLTAGE RANGE											
Range, Linear Response		±10	±12.5		±10	±12.5		±10	±12.5		V
CMRR (DC, 1kΩ Source Imbalance)	G = 1	80	90		74	90		70	85		dB
	G = 10	96	106		90	106		86	95		dB
	G = 100	106	110		106	110		100	105		dB
	G = 1000	106	110		106	110		100	105		dB
NOISE											
Input Voltage Noise											
f_B = 0.1Hz to 10Hz	G = 1000		0.7			0.7			0.7		µV p-p
Density; f = 10Hz	G = 1000		14			14			14		nV/√Hz
f = 100Hz			11			11			11		nV/√Hz
f = 1000Hz			10			10			10		nV/√Hz
Input Current Noise											
f_B = 0.1Hz to 10Hz			50			50			50		pAp-p
Density; f = 10Hz			1.8			1.8			1.8		pA/√Hz
f = 1kHz			0.4			0.4			0.4		pA/√Hz
Output Voltage Noise											
f_B = 0.1Hz to 10Hz			8			8			8		µVp-p
DYNAMIC RESPONSE											
Small Signal Bandwidth (–3dB)	G = 1		2			2			2		MHz
	G = 10		200			200			200		kHz
	G = 100		20			20			20		kHz
	G = 1000		2			2			2		kHz
Slew Rate		0.4	0.6		0.4	0.6		0.4	0.6		V/µs
Settling Time to 0.01%	G = 1		24			24			24		µs
	G = 10		30			30			30		µs
	G = 100		50			50			50		µs
	G = 1000		200			200			200		µs
Full Power Bandwidth, G < 200	V_O = ±10V, R_L = 2kΩ		9			9			9		kHz
Overload Recovery	50% Overdrive		2			2			2		µs
OUTPUT											
Voltage, R_L = 2kΩ	Over Temperature	±10.5	±12.8		±10.5	±12.8		±10.5	±12.8		V
Current	Over Temperature	5	15		5	15		5	15		mA
Short-Circuit Current			24			24			24		mA
Capacitive Load, Stable Operation			4000			4000			4000		pF
POWER SUPPLY											
Rated Voltage			±15			±15			±15		V
Voltage Range		±6		±18	±6		±18	±6		±18	V
Supply Current	V_O = 0V		±2.7	±4		±2.7	±4		±2.7	±4	mA
TEMPERATURE RANGE											
Specification		–25		+85	–25		+85	–25		+85	°C
Operation BP,AP					–40		+85	–40		+85	°C
Operation CG,BG		–55		+125	–55		+125				°C
Storage		See Absolute Maximum Table.									

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

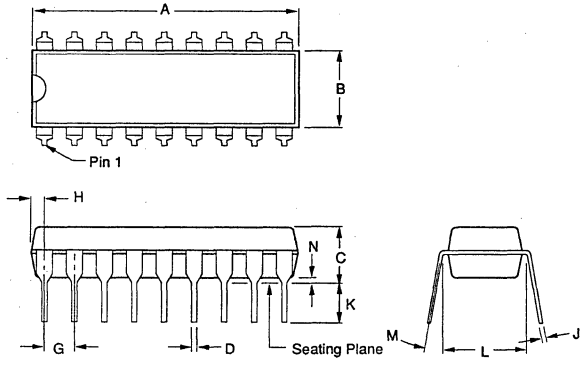
Supply Voltage	±18V
Input Voltage Range	(V+) +2 to (V–) –2V
Differential Input Voltage	Total V_s +4V
Operating Temperature	
Ceramic G Package	–65°C to +150°C
Plastic P Package	–40°C to +125°C
Storage Temperature	
Ceramic G Package	–65°C to +150°C
Plastic P Package	–40°C to +125°C
Junction Temperature	
Ceramic G Package	+175°C
Plastic P Package	+125°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA120AP	Plastic DIP	–25°C to +85°C
INA120BP	Plastic DIP	–25°C to +85°C
INA120BG	Ceramic DIP	–25°C to +85°C
INA120CG	Ceramic DIP	–25°C to +85°C

MECHANICAL

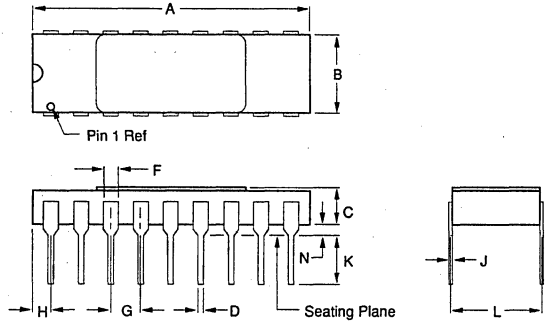
P Package — 18-Pin Plastic DIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.840	.940	21.34	23.88
B	.240	.280	6.10	7.11
C	—	.210	—	5.33
D	.014	.022	0.36	0.59
G	.100 BASIC		2.54 BASIC	
H	.040	.060	1.02	1.52
J	.008	.015	0.20	0.38
K	.115	.150	2.92	3.81
L	.280	.300	7.11	7.62
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

G Package — 18-Pin Ceramic DIP



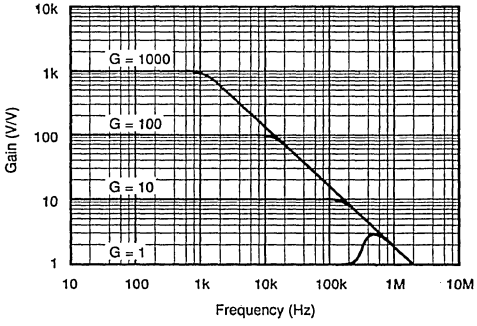
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	—	.960	—	24.38
B	.220	.310	5.59	7.87
C	—	.200	—	5.08
D	.014	.023	.36	.58
F	.030	.070	.76	1.78
G	.100 BASIC		2.54 BASIC	
H	—	.098	—	2.49
J	.008	.015	.20	.38
K	.125	.200	3.18	5.08
L	.290	.320	7.37	8.13
N	.015	.060	.38	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

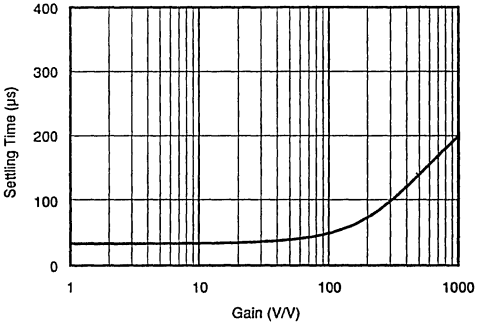
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

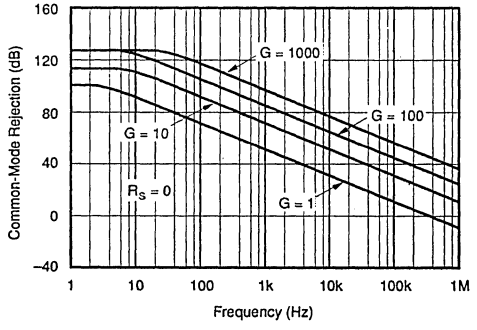
GAIN vs FREQUENCY



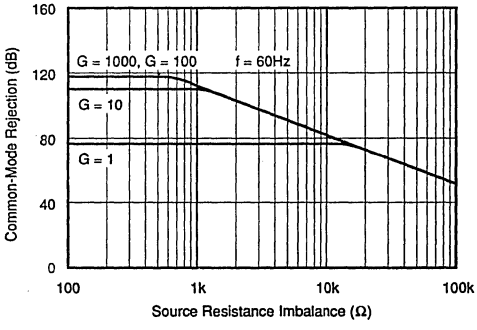
SETTLING TIME vs GAIN (0.1%)



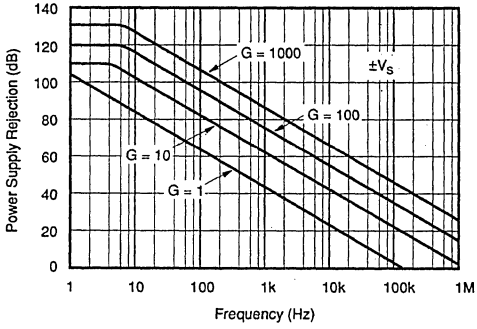
COMMON-MODE REJECTION vs FREQUENCY



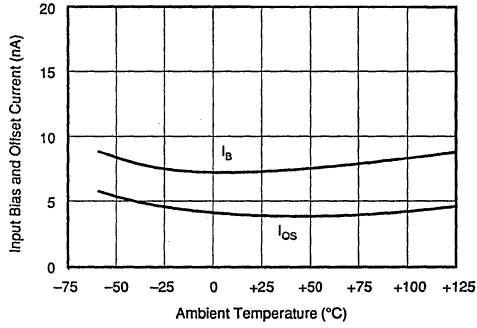
COMMON-MODE REJECTION vs SOURCE RESISTANCE IMBALANCE



POWER SUPPLY REJECTION vs FREQUENCY



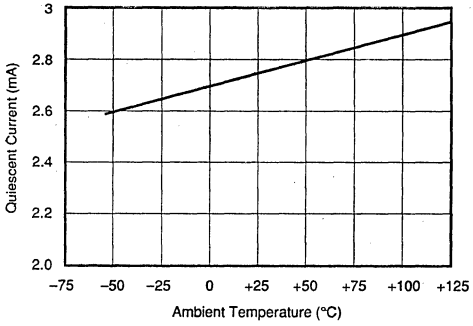
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



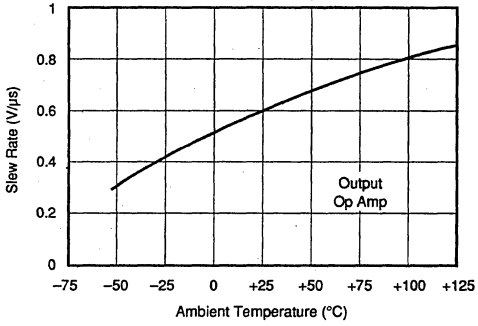
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

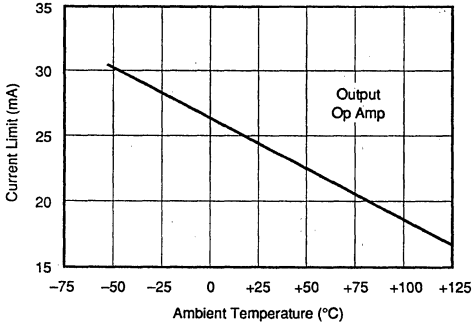
QUIESCENT CURRENT vs TEMPERATURE



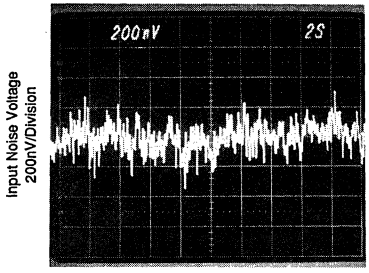
SLEW RATE vs TEMPERATURE



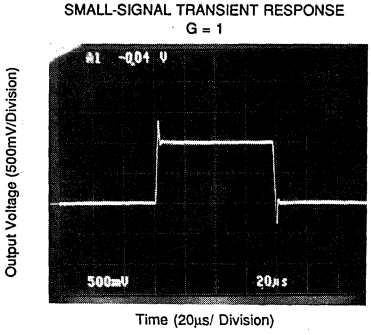
CURRENT LIMIT vs TEMPERATURE



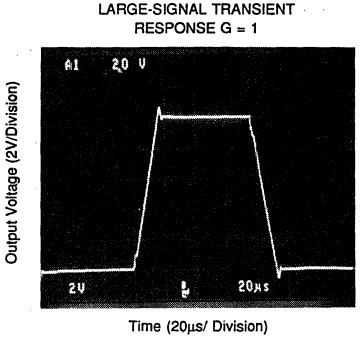
INPUT-REFERRED NOISE
G = 1000



SMALL-SIGNAL TRANSIENT RESPONSE
G = 1



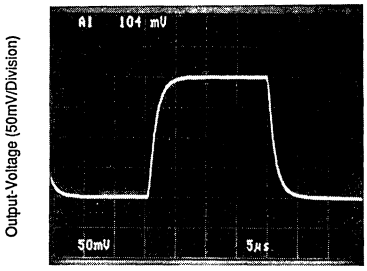
LARGE-SIGNAL TRANSIENT
RESPONSE G = 1



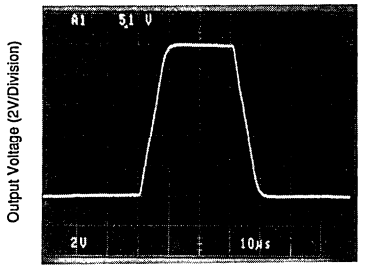
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

SMALL-SIGNAL TRANSIENT RESPONSE
G = 100



LARGE-SIGNAL TRANSIENT
RESPONSE G = 100



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA120. Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins as shown. The differential input voltage is applied to pins 16 and 3.

The output is referred to the output common reference terminal, pin 18. This terminal must have a low-impedance connection to ground. A resistance of 1Ω or greater in series with the common terminal could degrade common-mode rejection beyond the specified value.

SETTING THE GAIN

Gains of 1, 10, 100 or 1000 can be configured by interconnecting the gain-set pins as shown in the table of Figure 1. These pin-strapped gains provide best gain accuracy and drift because they are determined by the ratios of accurately trimmed and matched on-chip resistors.

Digital gain control can be achieved using an analog multiplexer as shown in Figure 2. Since the switches are in series with the high impedance gain-sense connections, pins 4 and 15, their series resistance does not significantly affect gain error or drift. Gain error at G = 1 is slightly higher than with direct pin connections shown in Figure 1. The gain is selected with a two-bit address, A_0 and A_1. The Multiplexer Enable control is directly connected to V+ since a logic "low" on this line would cause the input amplifiers to run open-loop.

Other gains may be set by connecting an external resistor, R_G, as shown in Figure 3a. Gain accuracy using an external gain-setting resistor is a function of R_G and the internal 20kΩ resistors. The internal resistors are typically within ±0.2% of nominal value and their drift under ±80ppm/°C. Inaccuracy and drift of R_G will contribute additional gain error and drift.

Figure 3b shows an external gain-setting resistor connected in parallel with internal resistors. By forming a portion of the effective R_G with internal resistors, gain accuracy and drift can be somewhat improved.

Connections available on the INA120 allow all input stage gain-setting resistors to be provided externally. A custom precision resistor network could be connected to provide the highest accuracy and lowest gain drift for non-standard gains. Impedance of this external network should be made close to that of the internal network for best performance.

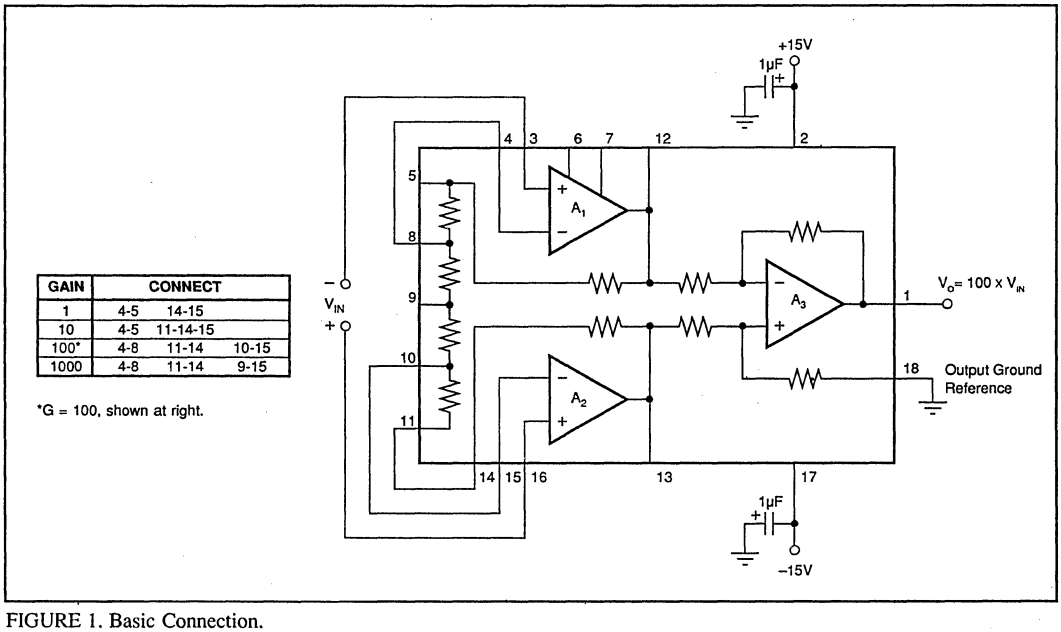
OFFSET TRIMMING

Many applications require no external offset voltage trimming. Figure 4 shows optional circuits for trimming offset voltage. Since the INA120 has two amplification stages, the offset voltage is comprised of two components—the input stage offset and output stage offset.

The input stage offset is equal to the combined offset of op amps A_1 and A_2. This input stage offset dominates at high gain. When used in gains of 100 to 1000, it is often sufficient to adjust the input stage offset with a potentiometer connected to pins 6 and 7 as shown. Connect both inputs to ground and adjust for 0V at the output, pin 1. Do not use pins 6 and 7 to trim offset voltage at G = 1 or to correct for offset in devices following the INA120 since this can cause excessive offset voltage drift.

At G = 1, offset is dominated by the output stage. Output stage offset can be trimmed by applying a correction voltage at the output reference terminal, pin 18. Low impedance must be maintained at this node to preserve the high CMR of the INA120. This is achieved by buffering the trim voltage with an op amp as shown.

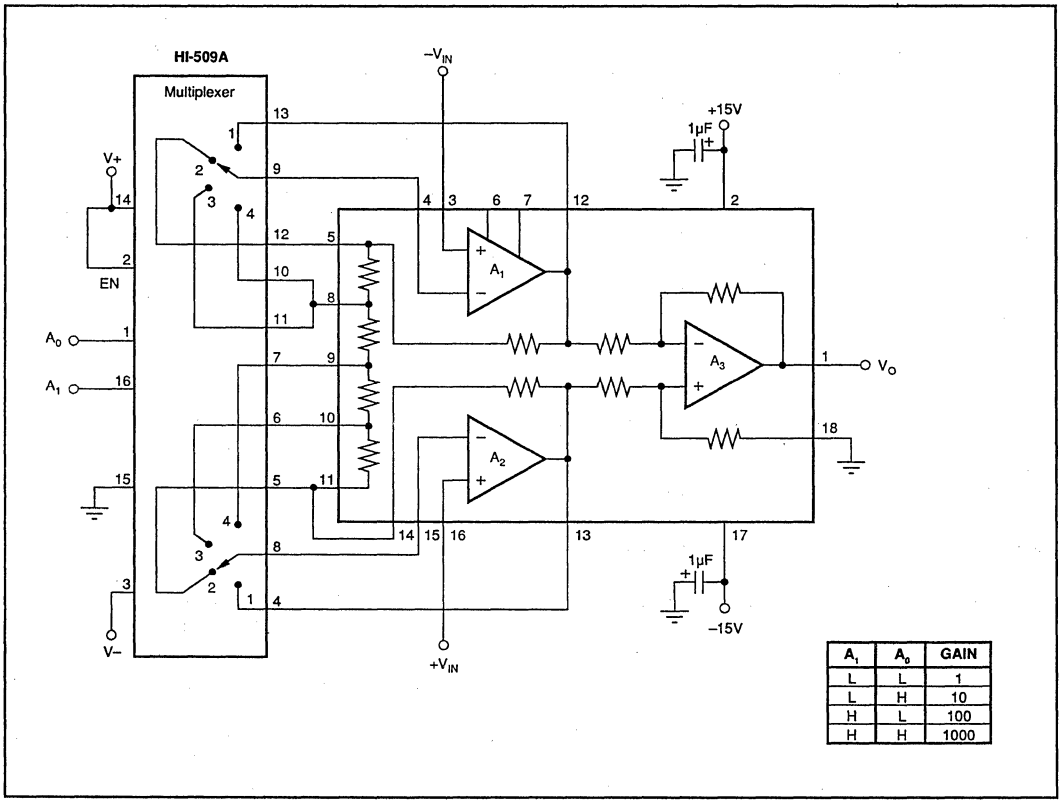
At intermediate gains it may be necessary to provide both input stage and output stage offset adjustments. Again, ground both inputs. Connect a jumper between pins 9 and 11 (temporarily connects the INA120 in high gain) and adjust R_1 for 0V at the output, pin 1. Then disconnect the jumper and adjust the output offset control for 0V output.



GAIN	CONNECT		
1	4-5	14-15	
10	4-5	11-14-15	
100*	4-8	11-14	10-15
1000	4-8	11-14	9-15

*G = 100, shown at right.

FIGURE 1. Basic Connection.



A_1	A_0	GAIN
L	L	1
L	H	10
H	L	100
H	H	1000

FIGURE 2. Digital Gain Control.

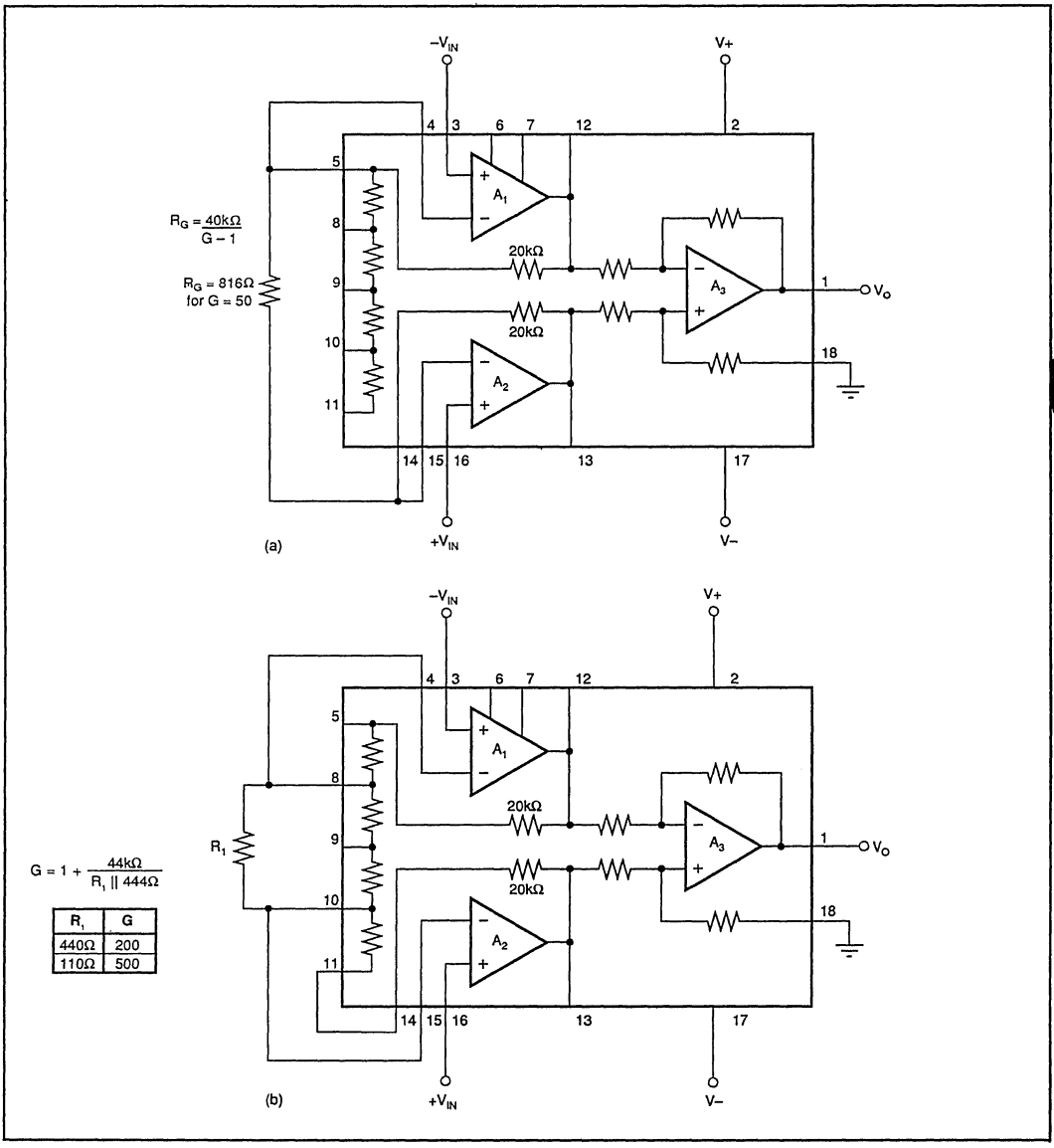


FIGURE 3. External Gain-Setting Resistors.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA120 is extremely high—approximately $10^{10}\Omega$. This does not mean, however, that no current flows in the input terminals. The input bias current of the INA120 is typically ±10nA (it can be either polarity). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA120 is to function. Figure 5 shows various provisions for an input bias current path. Without an appropriate current path, the inputs will float to a potential which exceeds the common-mode range of the INA120 and the input amplifiers will saturate.

INPUT PROTECTION

The inputs of the INA120 are protected for input voltages up to 2V beyond the power supply voltages. If the input can exceed these conditions, input clamp diodes should be provided as shown in Figure 6. R_S may not be required if the input cannot supply more than 100mA. If the input can supply larger currents, choose R_S according to the maximum source voltage, limiting current to under 100mA.

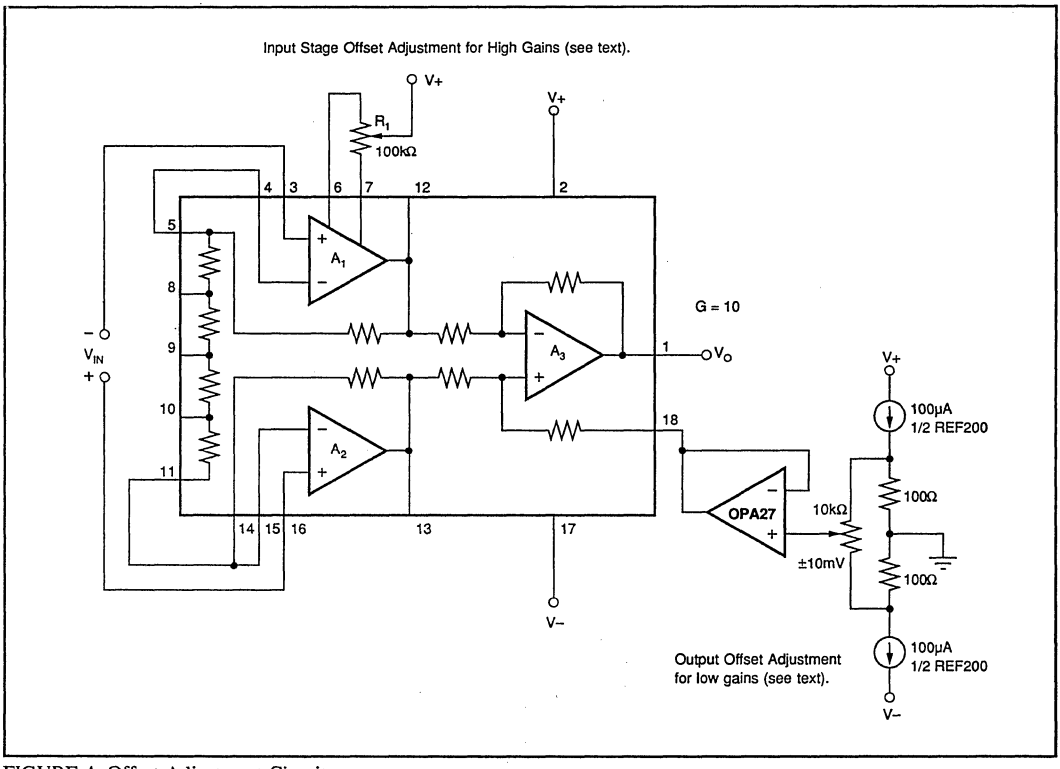


FIGURE 4. Offset Adjustment Circuits.

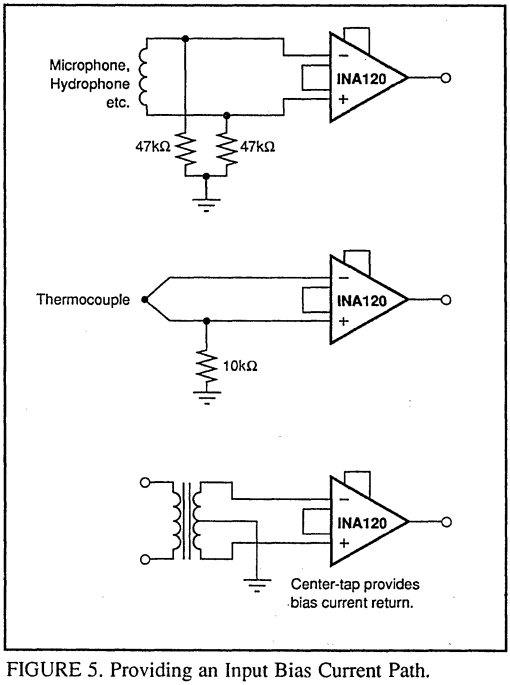


FIGURE 5. Providing an Input Bias Current Path.

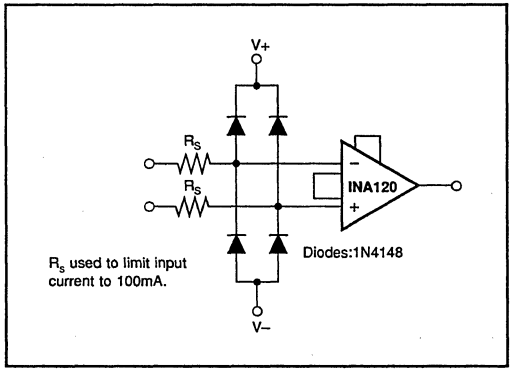
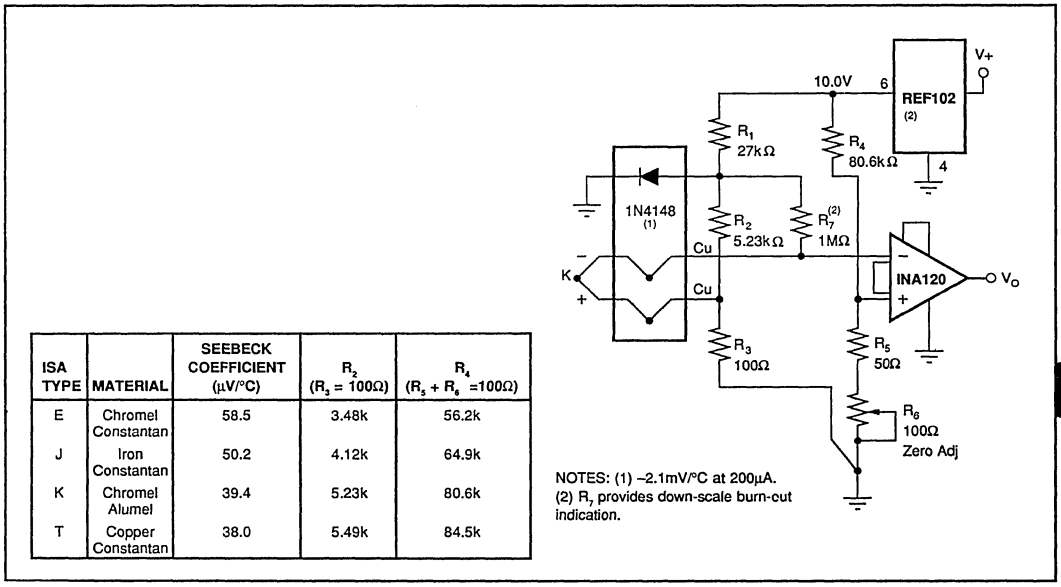


FIGURE 6. Input Protection Circuit.



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (μV/°C)	R_2 (R_3 = 100Ω)	R_4 (R_5 + R_6 =100Ω)
E	Chromel Constantan	58.5	3.48k	56.2k
J	Iron Constantan	50.2	4.12k	64.9k
K	Chromel Alumel	39.4	5.23k	80.6k
T	Copper Constantan	38.0	5.49k	84.5k

NOTES: (1) –2.1mV/°C at 200μA.
(2) R_7 provides down-scale burn-out indication.

FIGURE 7. Thermocouple Amplifier With Cold Junction Compensation.

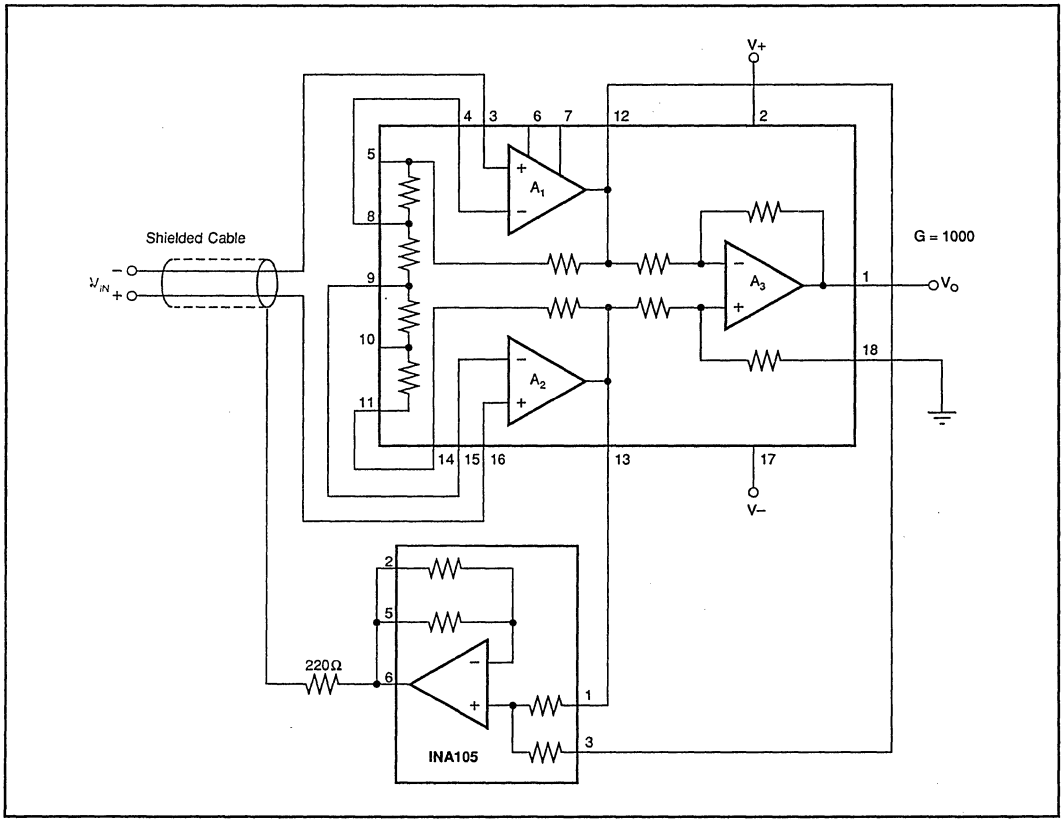
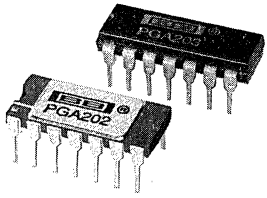


FIGURE 8. Guard Drive Circuit.

BURR-BROWN®



PGA202/203

Digitally-Controlled Programmable-Gain INSTRUMENTATION AMPLIFIER

FEATURES

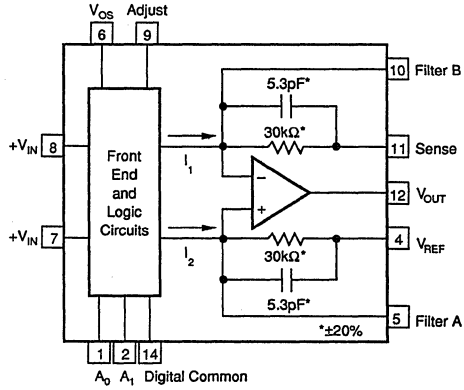
- DIGITALLY PROGRAMMABLE GAINS:
  DECADE MODEL—PGA202
  GAINS OF 1, 10, 100, 1000
  BINARY MODEL—PGA203
  GAINS OF 1, 2, 4, 8
- LOW BIAS CURRENT: 50pA max
- FAST SETTLING: 2µs to 0.01%
- LOW NON-LINEARITY: 0.012% max
- HIGH CMRR: 80dB min
- NEW TRANSCONDUCTANCE CIRCUITRY
- LOW COST

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- AUTO-RANGING CIRCUITS
- DYNAMIC RANGE EXPANSION
- REMOTE INSTRUMENTATION
- TEST EQUIPMENT

DESCRIPTION

The PGA202 is a monolithic instrumentation amplifier with digitally controlled gains of 1, 10, 100 and 1000. The PGA203 provides gains of 1, 2, 4, and 8. Both have TTL or CMOS-compatible inputs for easy microprocessor interface. Both have FET inputs and a new transconductance circuitry that keeps the bandwidth nearly constant with gain. Gain and offsets are laser trimmed to allow use without any external components. Both amplifiers are available in ceramic or plastic packages. The ceramic package is specified over the full industrial temperature range while the plastic package covers the commercial range.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1006A

SPECIFICATIONS

ELECTRICAL

At +25°C, V_{cc} = ±15V unless otherwise noted.

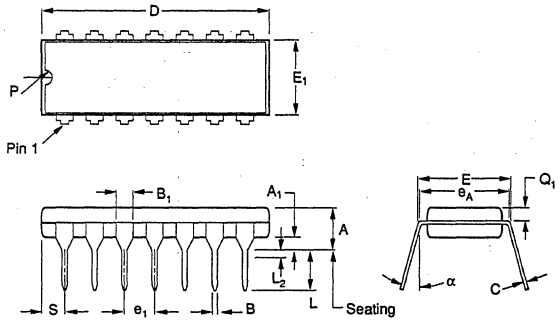
PARAMETER	CONDITION	PGA202/203AG [1] MIN	PGA202/203AG [1] TYP	PGA202/203AG [1] MAX	PGA202/203BG [1] MIN	PGA202/203BG [1] TYP	PGA202/203BG [1] MAX	PGA202/203KP [1] MIN	PGA202/203KP [1] TYP	PGA202/203KP [1] MAX	UNITS
GAIN											
Error [2]	G < 1000		0.05	0.25		0.05	0.15		*	*	%
	G = 1000		0.1	1		0.08	0.5		*	*	%
Nonlinearity	G < 1000		0.005	0.015		0.005	0.012		*	*	%
	G = 1000		0.01	0.05		0.01	0.025		*	*	%
Drift vs Temperature	G < 100		3	10		*	5		*		ppm/°C
	G = 100		10	100		*	50		*		ppm/°C
Stability vs Time	G = 1000		25	200		*	100		*		%/Month
RATED OUTPUT											
Voltage	$\|I_{OUT}\| \leq$ 5mA	±10	±12		*	*		*	*		V
Over Specified Temperature	See Typical Perf. Curve		±9			*			±10		V
Current	$\|V_{OUT}\| \leq$ 10V	±5	±10		*	*		*	*		mA
Impedance			0.5			*			*		Ω
ANALOG INPUTS											
Common-Mode Range		±10	±13		*	*		*	*		V
Abolute Max Voltage [3]	No Damage			±V_{cc}			*			*	V
Impedance, Differential			10 || 3			*			*		GΩ || pF
Common-Mode			10 || 1			*			*		GΩ || pF
OFFSET VOLTAGE (RTI)											
Initial Offset at 25°C [4]			±(0.3 + 3/G)	±(1 + 10/G)		*	±(0.5 + 5/G)		*	±(1 + 20/G)	mV
vs Temperature			±(2 + 10/G)	±(10 + 80/G)		*	±(5 + 40/G)		*		µV/°C
Offset vs Time			25			*			*		µV/Month
Offset vs Supply	10 ≤ V_{cc} ≤ 15		10 + 250/G	100 + 900/G		*	50 + 450/G		*	*	µV/V
INPUT BIAS CURRENT											
Initial Bias Current: at 25°C			10	50		*	*		*	*	pA
at 85°C			640	3200		*	*		*	*	pA
Initial Offset Current: at 25°C			5	25		*	*		*	*	pA
at 85°C			320	1600		*	*		*	*	pA
COMMON MODE REJECTION RATIO											
	G = 1	80	100		*	*		*	*		dB
	G = 10	86	110		*	*		*	*		dB
	G = 100	92	120		*	*		*	*		dB
	G = 1000	94	120		*	*		*	*		dB
INPUT NOISE											
Noise Voltage 0.1 to 10Hz			1.7			*			*		µVp-p
Noise Density at 10kHz [5]			12			*			*		nV/√Hz
OUTPUT NOISE											
Noise Voltage 0.1 to 10Hz			32			*			*		µVp-p
Density at 1kHz [5]			400			*			*		nV/√Hz
DYNAMIC RESPONSE											
Frequency Response	G < 1000		1000			*			*		kHz
	G = 1000		250			*			*		kHz
Full Power Bandwidth	G < 1000		400			*			*		kHz
	G = 1000		100			*			*		kHz
Slew Rate		10	20		15	*		*	*		V/µs
Settling Time (0.01%) [7]	G < 1000		2			*			*		µs
	G = 1000		10			*			*		µs
Overload Recovery Time [7]	G < 1000		5			*			*		µs
	G = 1000		10			*			*		µs
DIGITAL INPUTS											
Digital Common Range		–V_{cc}		V_{cc} – 8	*		*	*		*	V
Input Low Threshold [6]				0.8			*			*	V
Input Low Current				10			*			*	µA
Input High Voltage		2.4			*			*			V
Input High Current				10			*			*	µA
POWER SUPPLY											
Rated Voltage			±15			*			*		V
Voltage Range		±6		±18	*		*	*		*	V
Quiescent Current			6.5			*			*		mA
TEMPERATURE RANGE											
Specification		–25		85	*		*	0		70	°C
Operating		–55		125	*		*	–25		85	°C
Storage		–65		150	*		*	–40		100	°C
θ_{JA}			100			*			*		°C/W

* Same as the PGA202/203AG

NOTES: (1) All specifications apply to both the PGA202 and the PGA203. Values given for a gain of 10 are the same for a gain of 8 and other values may be interpolated. (2) Measured with a 10k load. (3) The analog inputs are internally diode clamped. (4) Adjustable to zero. (5) $V_{NOISE\ (RTI)} = \sqrt{(V_{N\ INPUT})^2 + (V_{N\ OUTPUT}/Gain)^2}$. (6) Threshold voltages are referenced to Digital Common. (7) From input change or gain change.

MECHANICAL

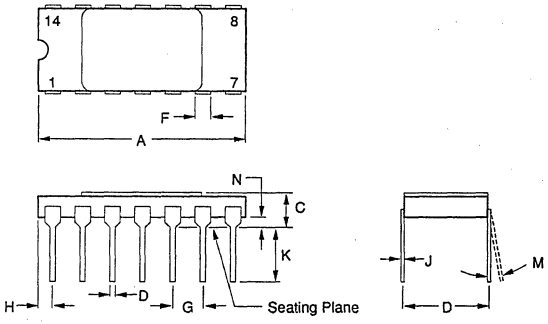
G Package — 14-Pin Plastic Package



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.120	.160	3.048	4.064
A_1	.015	.065	.381	1.651
B	.014	.020	.355	.508
B_1	.050	.065	1.270	1.651
C	.008	.012	.203	.304
D	.745	.770	18.923	19.558
E	.300	.325	7.620	8.255
E_1	.240	.260	6.096	6.604
e_1	.100 BASIC		2.540 BASIC	
e_A	.300 BASIC		7.620 BASIC	
L	.125	.150	3.175	3.810
L_2[1]	0	.030	0	.762
α	0°	15°	0°	15
P	—	.050	—	1.270
Q_1	.050	.085	1.270	2.159
S[2]	.065	.090	1.651	2.286

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.
(1) e_1 and e_A apply in zone L_2 when unit is installed.
(2) Not per JEDEC.

G Package — 14-Pin Hermetic DIP



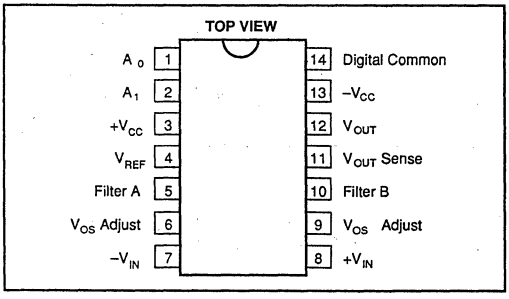
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.009	.060	0.23	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

ORDERING INFORMATION

MODEL	GAINS	PACKAGE	TEMPERATURE RANGE	OFFSET VOLTAGE MAX (mV)
PGA202KP	1, 10, 100, 1000	Plastic DIP	0°C to +70°C	±(1 + 20/G)
PGA202AG	1, 10, 100, 1000	Ceramic DIP	–25°C to +85°C	±(1 + 10/G)
PGA202BG	1, 10, 100, 1000	Ceramic DIP	–25°C to +85°C	±(0.5 + 5/G)
PGA203KP	1, 2, 4, 8	Plastic DIP	0°C to +70°C	±(1 + 20/G)
PGA203AG	1, 2, 4, 8	Ceramic DIP	–25°C to +85°C	±(1 + 10/G)
PGA203BG	1, 2, 4, 8	Ceramic DIP	–25°C to +85°C	±(0.5 + 5/G)

PIN CONFIGURATION



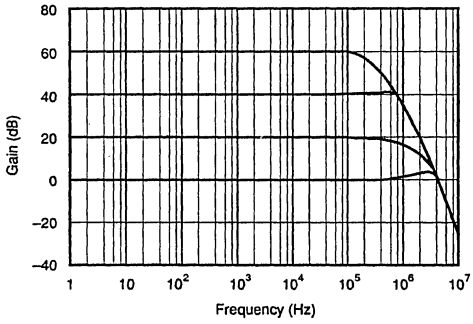
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation	750mW
Analog and Digital Inputs	±(V_{CC} + 0.5V)
Operating Temperature Range:	
G Package	–55°C to +125°C
P Package	–40°C to +100°C
Lead Temperature (soldering, 10s)	300°C
Output Short Circuit Duration	Continuous
Junction Temperature	175°C

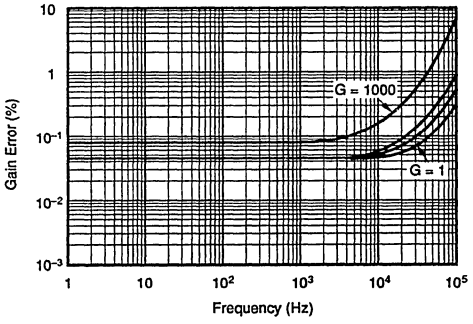
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

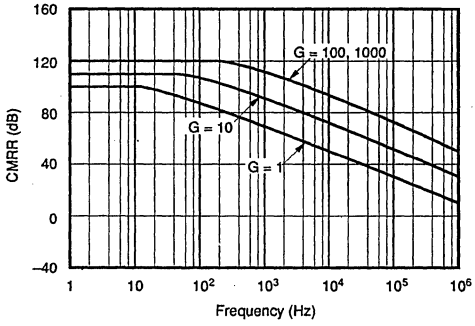
GAIN vs FREQUENCY



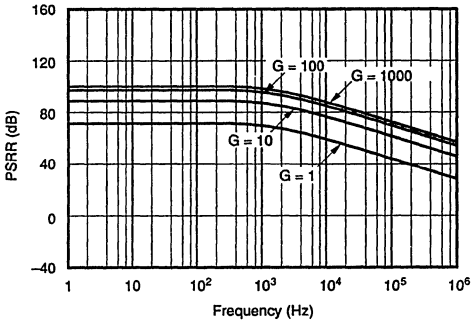
GAIN ERROR vs FREQUENCY



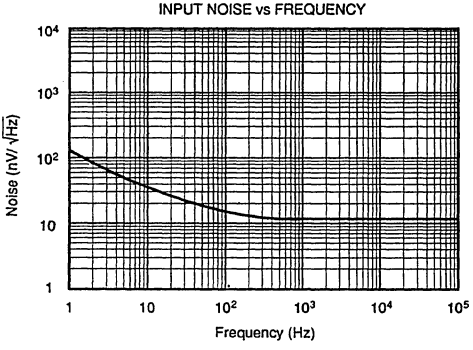
CMRR vs FREQUENCY



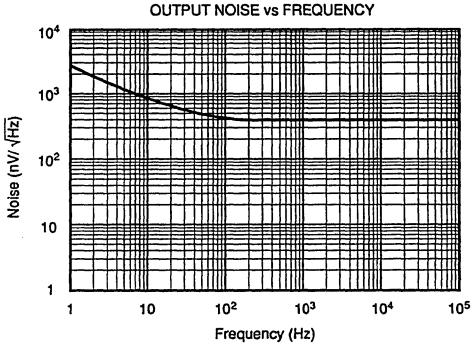
PSRR vs FREQUENCY



INPUT NOISE vs FREQUENCY



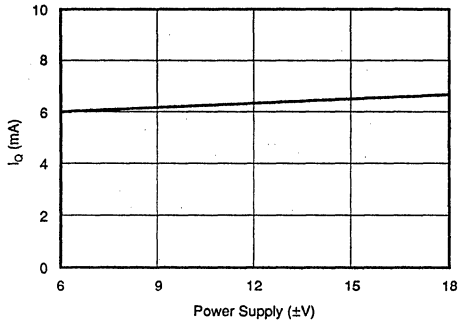
OUTPUT NOISE vs FREQUENCY



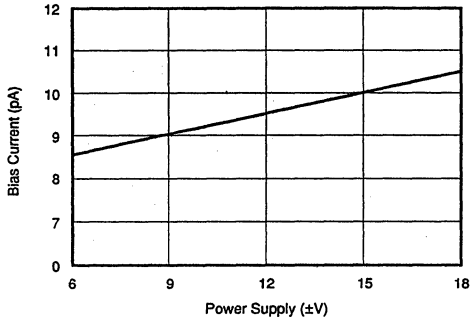
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

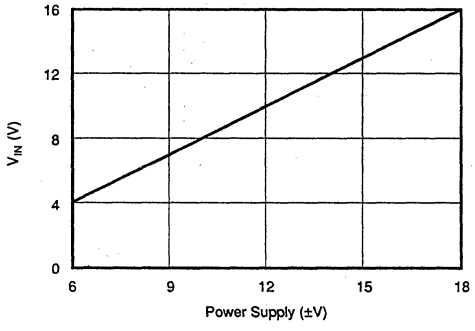
QUIESCENT CURRENT vs POWER SUPPLY



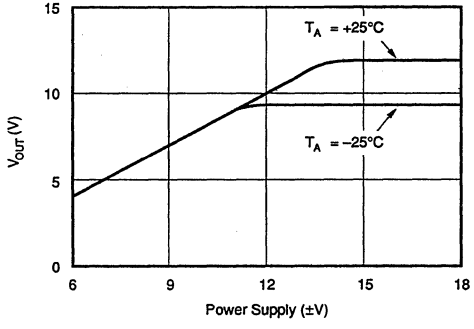
BIAS CURRENT vs POWER SUPPLY



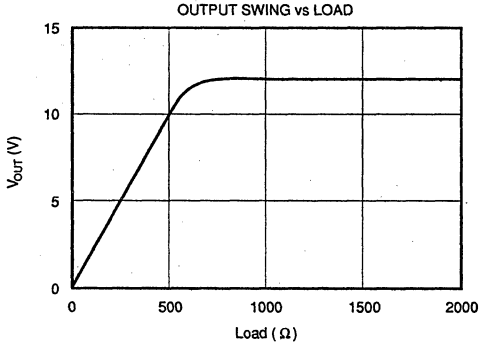
INPUT RANGE vs POWER SUPPLY



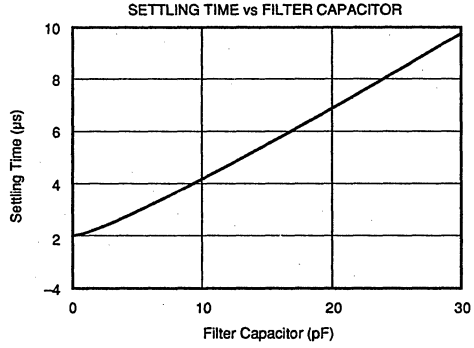
OUTPUT SWING vs POWER SUPPLY



OUTPUT SWING vs LOAD



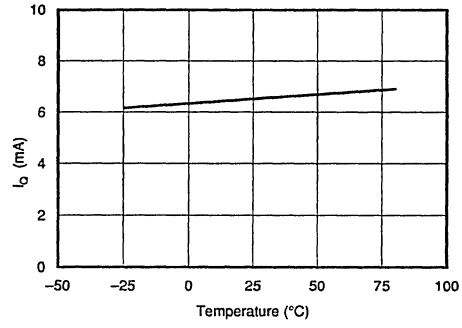
SETTLING TIME vs FILTER CAPACITOR



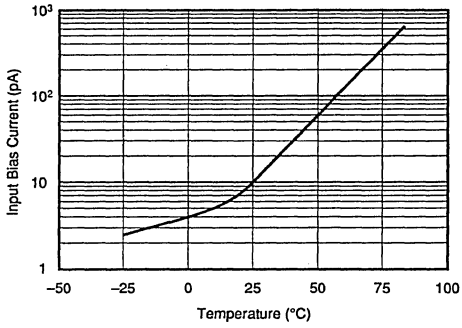
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

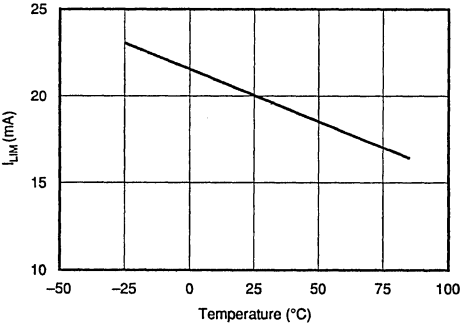
QUIESCENT CURRENT vs TEMPERATURE



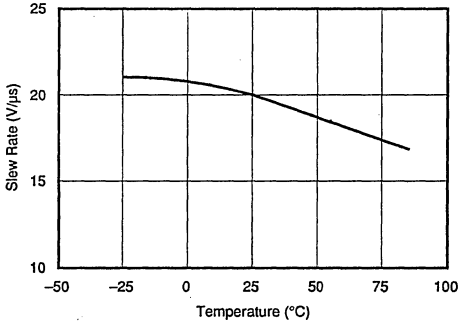
INPUT BIAS CURRENT vs TEMPERATURE



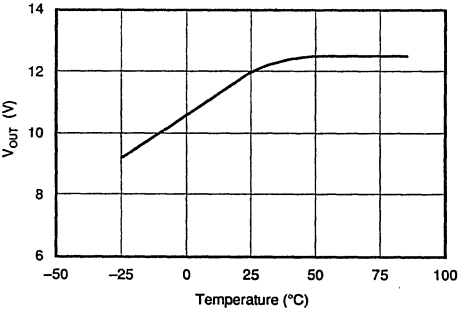
CURRENT LIMIT vs TEMPERATURE



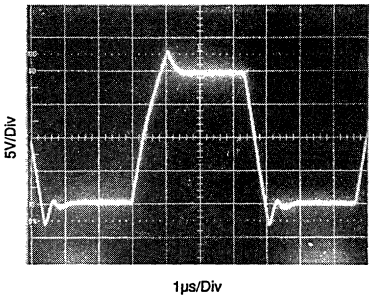
SLEW RATE vs TEMPERATURE



OUTPUT SWING vs TEMPERATURE



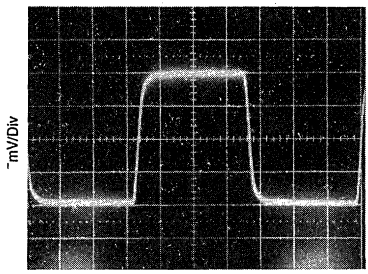
LARGE SIGNAL RESPONSE



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.

SMALL SIGNAL RESPONSE



DISCUSSION OF PERFORMANCE

A simplified diagram of the PGA202/203 is shown on the first page. The design consists of a digitally-controlled, differential transconductance front end stage using precision FET buffers and the classical transimpedance output stage. Gain switching is accomplished with a novel current steering technique that allows for fast settling when changing gains. The result is a high performance, programmable instrumentation amplifier with excellent speed and gain accuracy.

The input stage uses a new circuit topology that includes FET buffers to give extremely low input bias currents. The differential input voltage is converted into a differential output current with the transconductance gain selected by steering the input stage bias current between four identical input stages differing only in the value of the gain setting resistor. Each input stage is individually laser-trimmed for input offset, offset drift and gain.

The output stage is a differential transimpedance amplifier. Unlike the classical difference amplifier output stage, the common mode rejection is not limited by the resister matching. However, the output resistors are laser-trimmed to help minimize the output offset and drift.

BASIC CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. The power supplies should be decoupled with 1µF tantalum capacitors placed as close to the amplifier as possible for maximum performance. To avoid gain and CMR errors introduced by the external components, you should connect the grounds as indicated. Any resistance in the sense line (pin 11) or the V_{REF} line (pin 4) will lead to a gain error, so these lines should be kept as short as possible. Also to maintain stability, avoid capacitance from the output to the input or the offset adjust pins.

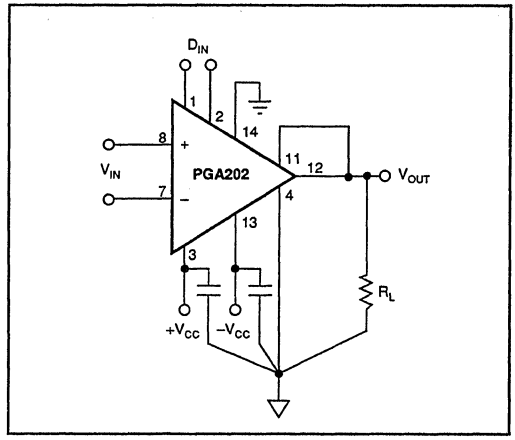


FIGURE 1. Basic Circuit Connections.

OFFSET ADJUSTMENT

Figure 2 shows the offset adjustment circuits for the PGA202/203. The input offset and the output offset are both separately adjustable. Notice that because the PGA202/203 change between four different input stages to change gain, the input offset voltage will change slightly with gain. For systems using computer autozeroing techniques, neither offset nor drift is a major concern, but it should be noted that since the input offset does change with gain, these systems should perform an autozero cycle after each gain change for optimum performance.

In the output offset adjustment circuit, the choice of the buffering op-amp is very important. The op-amp needs to have low output impedance and a wide bandwidth to maintain full accuracy over the entire frequency range of the PGA202/203. For these reasons we recommend the OPA602 as an excellent choice for this application.

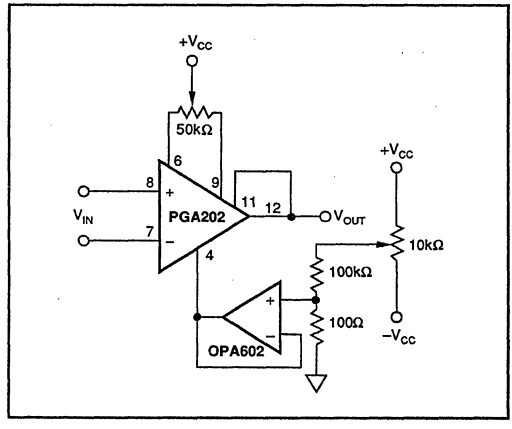


FIGURE 2. Offset Adjustment Circuits.

GAIN SELECTION

Gain selection is accomplished by the application of a 2-bit digital word to the gain select inputs. Table I shows the gains for the different possible values of the digital input word. The logic inputs are referred to their own separate digital common pin, which can be connected to any voltage between the minus supply and 8V below the positive supply. The gains are all internally trimmed to an initial accuracy of better than 0.1%, so no external gain adjustment is required. However, if necessary the gains can be increased by the use of an external attenuator around the output stage as shown in Figure 3. Recommended resistor values for certain selected output gains are given in Table II.

		PGA202		PGA203	
A_1	A_0	GAIN	ERROR	GAIN	ERROR
0	0	1	0.05%	1	0.05%
0	1	10	0.05%	2	0.05%
1	0	100	0.05%	4	0.05%
1	1	1000	0.10%	8	0.05%

TABLE I. Software Gain Selection.

OUTPUT GAIN	R_1	R_2
2	5kΩ	5kΩ
5	2kΩ	8kΩ
10	1kΩ	9kΩ

TABLE II. Output Stage Gain Control.

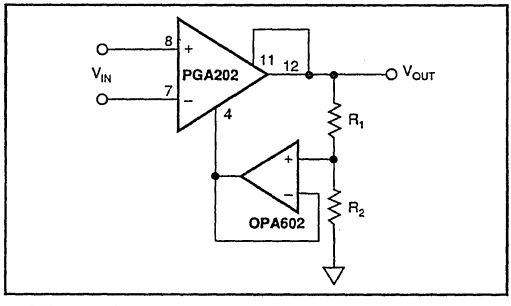


FIGURE 3. Gain Increase with Buffered Attenuator.

COMMON-MODE INPUT RANGE

Unlike the classical three op-amp type of circuit, the input common-mode range of the PGA202/203 does not depend on the differential input and the gain. In the standard three op-amp circuit, the input common-mode signal must be kept below the maximum output voltage of the input amplifier minus 1/2 the final output voltage. If, for example, these amplifiers can swing ±12V, then to get 12V at the output you must restrict the input common-mode voltage to only 6V. The circuitry of the PGA202/203 is such that the common-mode input range applies to either input pin regardless of the output voltage.

OUTPUT SENSE

An output sense has been provided to allow greater accuracy in connecting the load. By attaching this feedback point to the load at the load site, IR drops due to the load currents are eliminated since they are inside the feedback loop. Proper connection is shown in Figure 1. When more current is required, a power booster can be placed in the feedback loop as shown in Figure 4. Buffer errors are minimized by the loop gain of the output amplifier.

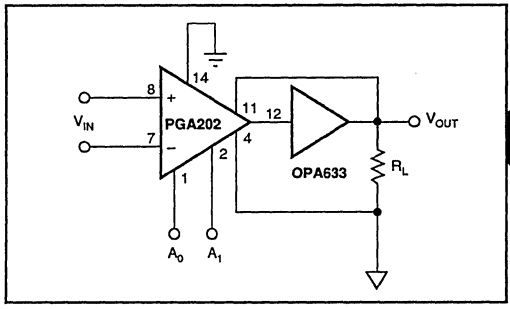


FIGURE 4. Current Boosting the Output.

OUTPUT FILTERING

The summing nodes of the output amplifier have also been made available to allow for output filtering. By placing matched capacitors in parallel with the existing internal capacitors as shown in Figure 5, you can lower the frequency response of the output amplifier. This will reduce the noise of the amplifier, at the cost of a slower response. The nominal frequency responses for some selected values of capacitor are shown in Table 3.

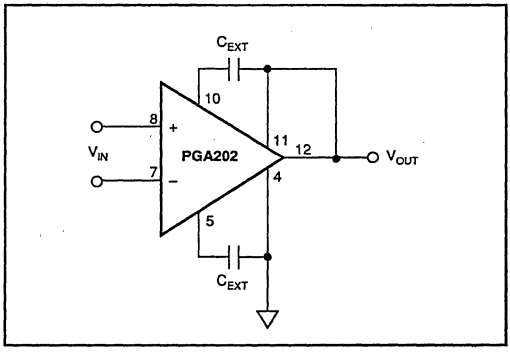


FIGURE 5. Output Filtering.

CUTOFF FREQUENCY	C_1 AND C_2
1MHz	None
100kHz	47pF
10kHz	525pF

TABLE 3. Output Frequency vs Filter Capacitors.

INPUT CHARACTERISTICS

Because the PGA202/203 have FET inputs, the bias currents drawn through input source resistors have a negligible effect on DC accuracy. The picoamp currents produce no more than microvolts through megohm sources. The inputs are also internally diode clamped to the supplies. Thus, input filtering and input series protection are easily achievable.

A return path for the input bias currents must always be provided to prevent the charging of any stray capacitance. Otherwise the amplifier could wander and saturate. A 1MΩ to 10MΩ resistor from the input to common will return floating sources such as thermocouples and AC-coupled inputs (see Applications Section, Figures 8 and 9.)

DYNAMIC PERFORMANCE

The PGA202 and the PGA203 are fast-settling FET input programmable gain instrumentation amplifiers. Careful attention to minimize stray capacitance is necessary to achieve specified performance. High source resistance will interact with the input capacitance to reduce speed and overall bandwidth. Also to maintain stability, avoid capacitance from the output to the input or the offset adjust pins.

Applications with balanced source impedance will provide the best performance. In some applications, mismatched source impedances may be required. If the impedance in the negative input exceeds that in the positive input, stray capacitance from the output will create a net negative feedback and improve the stability of the circuit. If, however, the impedance in the positive input is greater, then the feedback due to stray capacitance will be positive and instability may result. The degree of positive feedback will, of course, depend on the source impedance imbalance as well as the board layout and the operating gain. The addition of a small bypass capacitor of about 5 to 50pF directly across the input terminals of the PGIA will generally eliminate any instability arising from these stray capacitances. CMR errors due to the source imbalance will also be reduced by the addition of this capacitor.

The PGA202 and the PGA203 are designed for fast settling in response to changes in either the input voltage or the gain. The bandwidth and the settling times are mostly determined by the output stage and are therefore independent of gain, except at the highest gain of the PGA202 where other factors in the input stage begin to dominate.

APPLICATIONS

In addition to general purpose applications, the PGA202/203 are designed to handle two important and demanding classes of applications: inputs with high source impedances, and rapid scanning data acquisition systems requiring fast settling time. Because the user has access to output sense and output common pins, current sources can also be constructed with a minimum of external components. Some basic application circuits are shown in Figures 6 through 14.

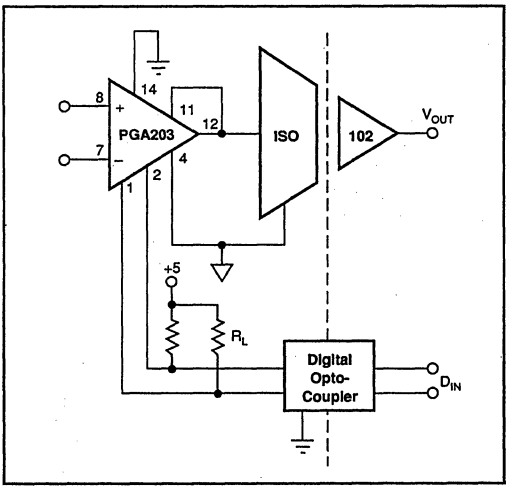


FIGURE 6. Isolated Programmable Gain Instrumentation Amplifier.

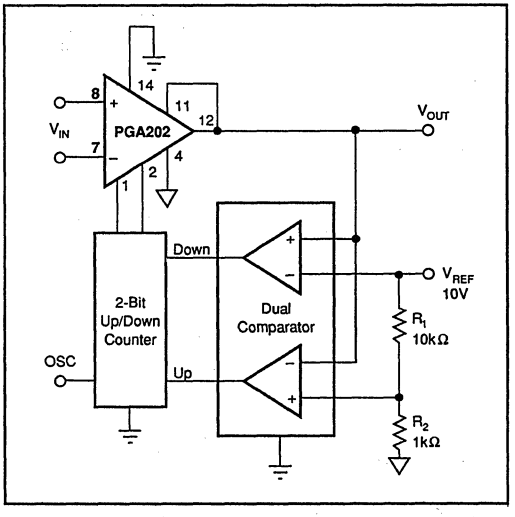


FIGURE 7. Auto Gain Ranging.

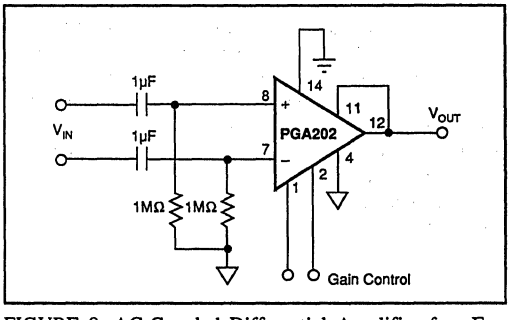


FIGURE 8. AC-Coupled Differential Amplifier for Frequencies above 0.16Hz.

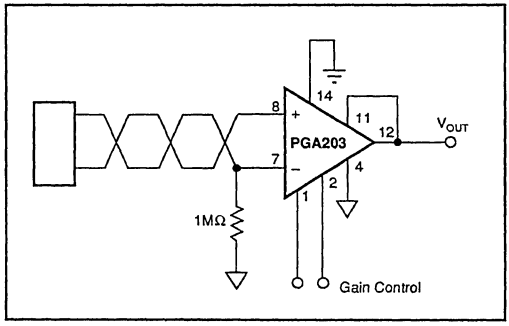


FIGURE 9. Floating Source Programmable Gain Instrumentation Amplifier.

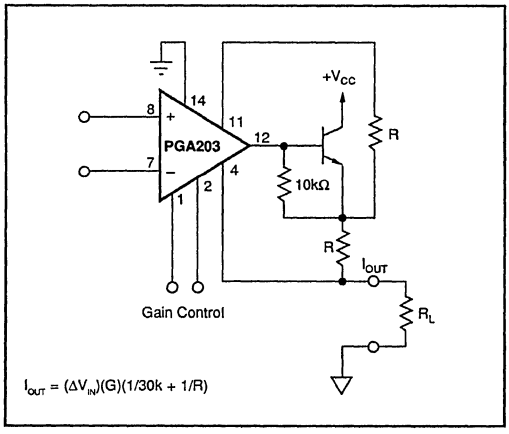


FIGURE 10. Programmable Current Source.

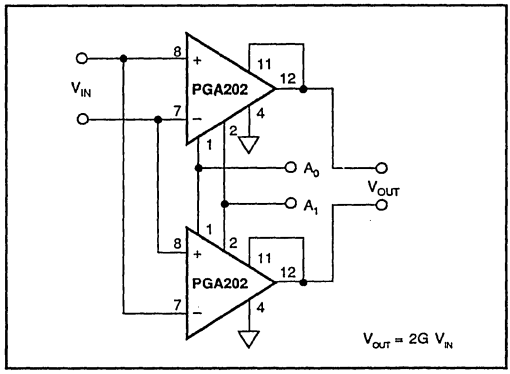


FIGURE 11. Programable Differential In/Differential Out Amplifier.

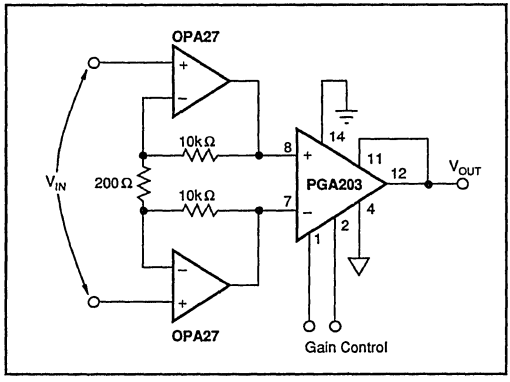
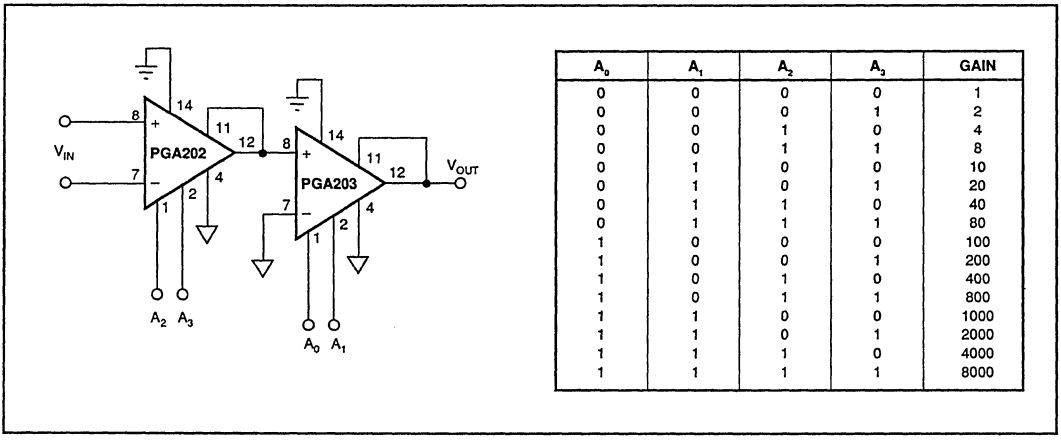


FIGURE 12. Low Noise Differential Amplifier with Gains of 100, 200, 400, 800.



A_0	A_1	A_2	A_3	GAIN
0	0	0	0	1
0	0	0	1	2
0	0	1	0	4
0	0	1	1	8
0	1	0	0	10
0	1	0	1	20
0	1	1	0	40
0	1	1	1	80
1	0	0	0	100
1	0	0	1	200
1	0	1	0	400
1	0	1	1	800
1	1	0	0	1000
1	1	0	1	2000
1	1	1	0	4000
1	1	1	1	8000

FIGURE 13. Cascaded Amplifiers.

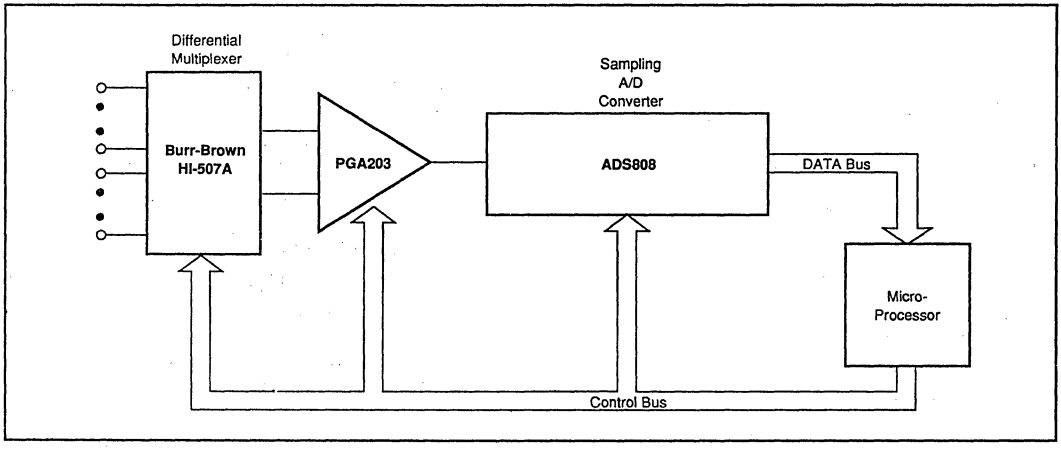
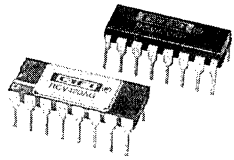


FIGURE 14. 8-Channel Differential Data Acquisition System.

BURR-BROWN®



RCV420

Precision 4mA to 20mA CURRENT LOOP RECEIVER

FEATURES

- COMPLETE 4-20mA TO 0-5V CONVERSION
- INTERNAL SENSE RESISTORS
- PRECISION 10V REFERENCE
- BUILT-IN LEVEL-SHIFTING
- ±40V COMMON-MODE INPUT RANGE
- 0.1% OVERALL CONVERSION ACCURACY
- HIGH NOISE IMMUNITY: 86dB CMR

APPLICATIONS

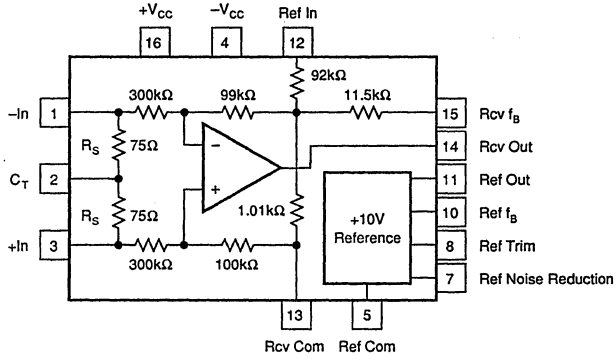
- PROCESS CONTROL
- INDUSTRIAL CONTROL
- FACTORY AUTOMATION
- DATA ACQUISITION
- SCADA
- RTUs
- ESD
- MACHINE MONITORING

DESCRIPTION

The RCV420 is a precision current-loop receiver designed to convert a 4–20mA input signal into a 0–5V output signal. As a monolithic circuit, it offers high reliability at low cost. The circuit consists of a premium grade operational amplifier, an on-chip precision resistor network, and a precision 10V reference. The RCV420 features 0.1% overall conversion accuracy, 86dB CMR, and ±40V common-mode input range.

The circuit introduces only a 1.5V drop at full scale, which is useful in loops containing extra instrument burdens or in intrinsically safe applications where transmitter compliance voltage is at a premium. The 10V reference provides a precise 10V output with a typical drift of 5ppm/°C.

The RCV420 is completely self-contained and offers a highly versatile function. No adjustments are needed for gain, offset, or CMR. This provides three important advantages over discrete, board-level designs: 1) lower initial design cost, 2) lower manufacturing cost, and 3) easy, cost-effective field repair of a precision circuit.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 741-4395 • Immediate Product Info: (800) 548-6132

PDS-837B

SPECIFICATIONS

ELECTRICAL

T = +25°C and $\pm V_{CC}$ = ±15V unless otherwise noted.

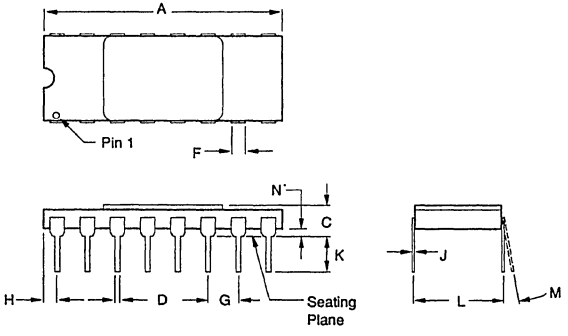
CHARACTERISTICS	RCV420AG			RCV420BG			RCV420KP			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN										
Initial		0.3125			*			*		V/mA
Error		0.025	0.1		*	0.05		0.05	0.15	% of span
vs Temp		15	50		*	25		*		ppm/°C
Nonlinearity[1]		0.0002	0.002		*	*		*	*	% of span
OUTPUT										
Rated Voltage (I_O = +10mA, –5mA)	10	12		*	*		*	*		V
Rated Current (E_O = 10V)	+10, –5			*			*			mA
Impedance (Differential)		0.01			*			*		Ω
Current Limit (To Common)		+49, –13			*			*		mA
Capacitive Load (Stable Operation)		1000			*			*		pF
INPUT										
Sense Resistance	74.25	75	75.75	*	*	*	*	*	*	Ω
Input Impedance (Common Mode)		200			*			*		kΩ
Common Mode Voltage			±40			*			*	V
CMR[2]	72	80		86	94		70	*		dB
vs Temp (DC) (T_A = T_{MIN} to T_{MAX})	66	76		80	90			*		dB
AC 60Hz		80			94			*		dB
OFFSET VOLTAGE (RTO) [3]										
Initial			1			*			*	mV
vs Temp		10	50		*	25		*		µV/°C
vs Supply (±11.4V to ±18V)	74	90		80	*		*	*		dB
vs Time		200			*			*		µV/mo
ZERO ERROR[4]										
Initial		0.01	0.05		*	0.025		0.025	0.075	% of span
vs Temp		10	50		*	25		*		ppm of span/°C
OUTPUT NOISE VOLTAGE										
f_B = 0.1Hz to 10Hz		50			*			*		µVp-p
f_O = 10kHz		800			*			*		nV/√Hz
DYNAMIC RESPONSE										
Gain Bandwidth		150			*			*		kHz
Full Power Bandwidth		30			*			*		kHz
Slew Rate		1.5			*			*		V/µs
Settling Time (0.01%)		10			*			*		µs
VOLTAGE REFERENCE										
Initial	9.995		10.005	*		*	9.99		10.01	V
Trim Range[5]		±4			*			*		%
vs Temp[6]		5	20		*	*		*		ppm/°C
vs Supply (±11.4V to ±18V)		0.0002			*			*		%/V
vs Output Current (I_O = 0 to +10mA)		0.0002			*			*		%/mA
vs Time		15			*			*		ppm/kHr
Noise (0.1Hz to 10Hz)		5			*			*		µVp-p
Output Current	+10, –2			*			*			mA
POWER SUPPLY										
Rated		±15			*			*		V
Voltage Range[7]	±11.4		±18	*		*	*		*	V
Quiescent Current (V_O = 0V)		3	4		*	*		*	*	mA
TEMPERATURE RANGE										
Specification	–25		+85	*		*	0		+70	°C
Operation	–55		+125	*		*	–25		+85	°C
Storage	–65		+150	*		*	–40		+85	°C

*Specification same as RCV420AG.

NOTES: (1) Nonlinearity is the max peak deviation from best fit straight line. (2) With 0 source impedance on Rcv Com pin. (3) Referred to output with all inputs grounded including Ref In. (4) With 4mA input signal and Voltage Reference connected (includes V_{OS}, Gain Error, and Voltage Reference Errors). (5) External trim slightly affects drift. (6) The "box method" is used to specify output voltage drift vs temperature. (7) I_O Ref = 5mA, I_O Rcv = 2mA.

MECHANICAL

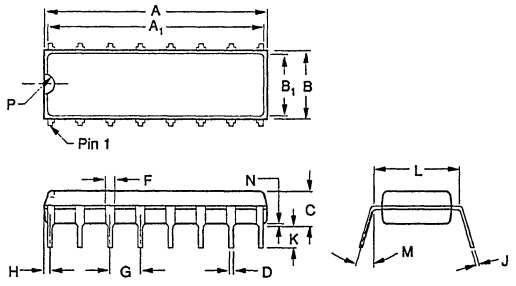
G Package — 16-Pin Hermetic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

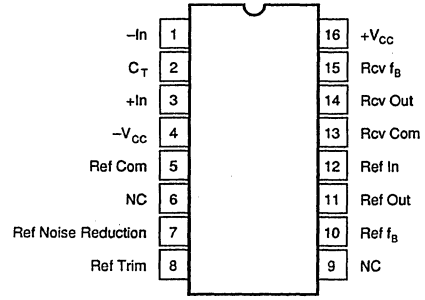
P Package — 16-Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.740	.800	18.80	20.32
A1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	0.20	.050	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply	±22V
Input Current, Continuous	40mA
Input Current Momentary, 0.1s	250mA, 1% Duty Cycle
Common Mode Input Voltage, Continuous	±40V
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Common (Rcv and Ref)	Continuous

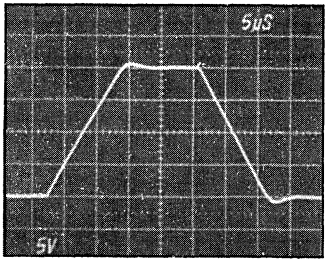
ORDERING INFORMATION

MODEL	PERFORMANCE GRADE	PACKAGE
RCV420AG	–25°C to +85°C	16-Pin Hermetic DIP
RCV420BG	–25°C to +85°C	16-Pin Hermetic DIP
RCV420KP	0°C to +70°C	16-Pin Plastic DIP

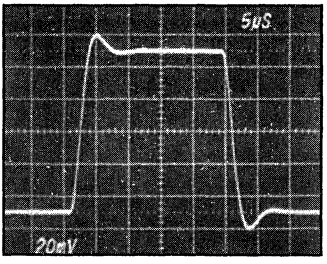
TYPICAL PERFORMANCE CURVES

T_A = +25°C, $\pm V_{CC}$ = 15V unless otherwise noted.

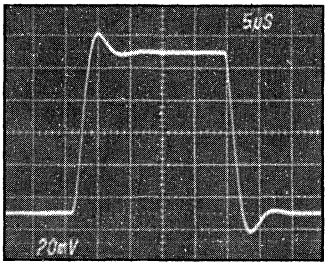
STEP RESPONSE
NO LOAD



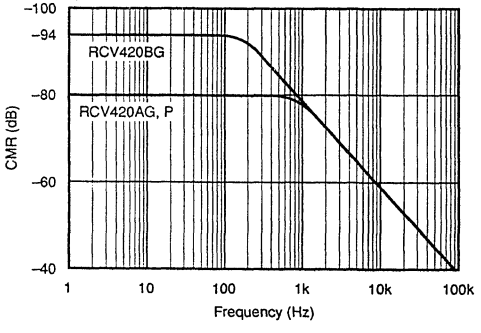
SMALL SIGNAL RESPONSE
NO LOAD



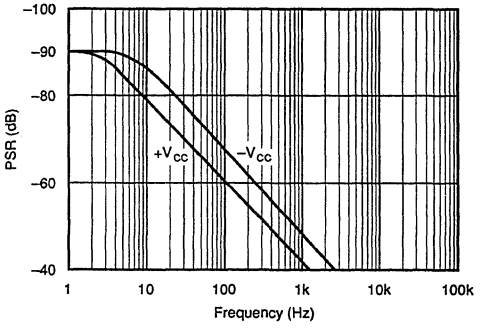
SMALL SIGNAL RESPONSE
R_L = ∞, C_L = 1000pF



COMMON-MODE REJECTION
vs FREQUENCY



POWER-SUPPLY REJECTION
vs FREQUENCY



THEORY OF OPERATION

Refer to the figure on the first page. For 0–5V output with 4–20mA input, the required transimpedance of the circuit is:

$$V_{OUT}/I_{IN} = 5V/16mA = 0.3125V/mA.$$

To achieve the desired output levels, 0V for 4mA and 5V for 20mA, the output of the amplifier must be offset by an amount:

$$V_{OS} = -(4mA)(0.3125V/mA) = -1.25V.$$

The input current signal is connected to either +In or –In, depending on the polarity of the signal, and returned to ground through the center tap, C_T. The balanced input—two matched 75Ω sense resistors, R_S—provides maximum rejection of common-mode voltage signals on C_T and true differential current-to-voltage conversion. The sense resistors convert the input current signal into a proportional voltage, which is amplified by the differential amplifier. The voltage gain of the amplifier is:

$$A_D = 5V/(16mA)(75\Omega) = 4.1667V/V.$$

The tee network in the feedback path of the amplifier provides a summing junction used to generate the required –1.25V offset voltage. The input resistor network provides high-input impedance and attenuates common-mode input voltages to levels suitable for the operational amplifier's common-mode signal capabilities.

BASIC POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. Both supplies should be decoupled with 1µF tantalum capacitors as close to the amplifier as possible. To avoid gain and CMR errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance. The input signal should be connected to either +In or –In, depending on its polarity, and returned to ground through the center tap, C_T. The output of the voltage reference, Ref Out, should be connected to Ref In for the necessary level shifting. If the Ref In pin is not used for level shifting, then it must be grounded to maintain high CMR.

GAIN AND OFFSET ADJUSTMENT

Figure 2 shows the circuit for adjusting the RCV420 gain. Increasing the gain of the RCV420 is accomplished by inserting a small resistor in the feedback path of the amplifier. Increasing the gain using this technique results in CMR degradation, and therefore, gain adjustments should be kept as small as possible. For example, a 1% increase in gain is typically realized with a 125Ω resistor, which degrades CMR by about 6dB.

A decrease in gain can be achieved by placing matched resistors in parallel with the sense resistors, also shown in Figure 2. The adjusted gain is given by the following expression

$$V_{OUT}/I_{IN} = 0.3125 \times R_X/(R_X + R_S).$$

A 1% decrease in gain can be achieved with a 7.5kΩ resistor. It is important to match the parallel resistance on each sense resistor to maintain high CMR. The TCR mismatch between the two external resistors will effect gain error drift and CMR drift.

There are two methods for nulling the RCV420 output offset voltage. The first method applies to applications using the internal 10V reference for level shifting. For these applica-

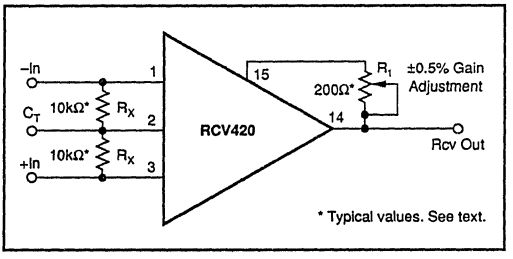


FIGURE 2. Optional Gain Adjustment.

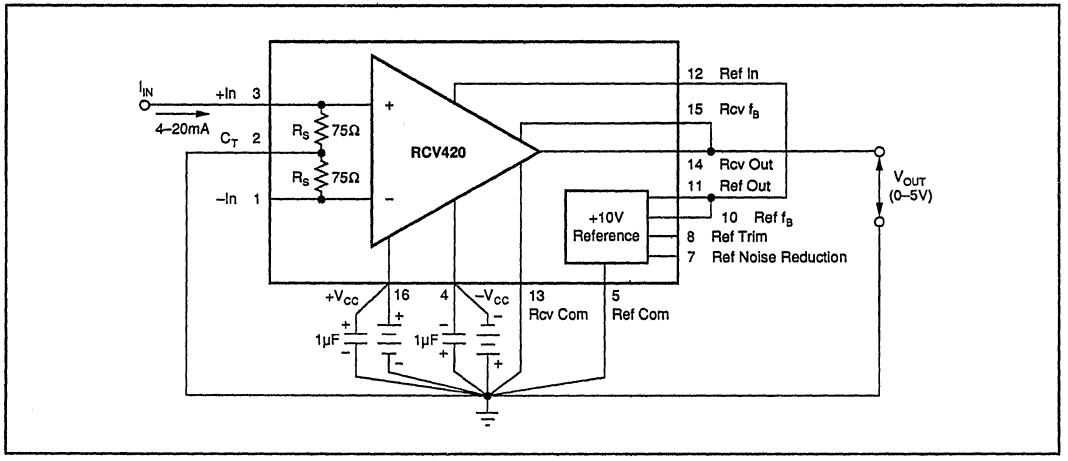


FIGURE 1. Basic Power Supply and Signal Connections.

tions, the voltage reference output trim procedure can be used to null offset errors at the output of the RCV420. The voltage reference trim circuit is discussed under "Voltage Reference."

When the voltage reference is not used for level shifting or when large offset adjustments are required, the circuit in Figure 3 can be used for offset adjustment. A low impedance on the Rcv Com pin is required to maintain high CMR.

ZERO ADJUSTMENT

Level shifting the RCV420 output voltage can be achieved using either the Ref In pin or the Rcv Com pin. The disadvantage of using the Ref In pin is that there is an 8:1 voltage attenuation from this pin to the output of the RCV420. Thus, use the Rcv Com pin for large offsets, because the voltage on this pin is seen directly at the output. Figure 4 shows the circuit used to level-shift the output of the RCV420 using the Rcv Com pin. It is important to use a low-output impedance amplifier to maintain high CMR. With this method of zero adjustment, the Ref In pin must be connected to the Rcv Com pin.

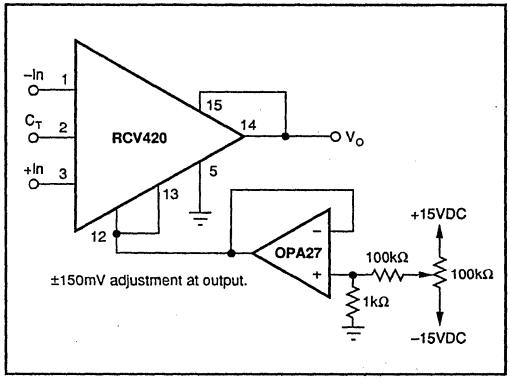


FIGURE 3. Optional Output Offset Nulling Using External Amplifier.

MAINTAINING COMMON-MODE REJECTION

Two factors are important in maintaining high CMR: (1) resistor matching and tracking (the internal resistor network does this) and (2) source impedance. CMR depends on the accurate matching of several resistor ratios. The high accuracies needed to maintain the specified CMR and CMR temperature coefficient are difficult and expensive to reliably achieve with discrete components. Any resistance imbalance introduced by external circuitry directly affects CMR. These imbalances can occur by: mismatching sense resistors when gain is decreased, adding resistance in the feedback path when gain is increased, and adding series resistance on the Rcv Com pin.

The two sense resistors are laser-trimmed to typically match within 0.01%; therefore, when adding parallel resistance to decrease gain, take care to match the parallel resistance on each sense resistor. To maintain high CMR when increasing the gain of the RCV420, keep the series resistance added to the feedback network as small as possible. Whether the Rcv Com pin is grounded or connected to a voltage reference for level shifting, keep the series resistance on this pin as low as possible. For example, a resistance of 20Ω on this pin degrades CMR from 86dB to approximately 80dB. For applications requiring better than 86dB CMR, the circuit shown in Figure 5 can be used to adjust CMR.

PROTECTING THE SENSE RESISTOR

The 75Ω sense resistors are designed for a maximum continuous current of 40mA, but can withstand as much as 250mA for up to 0.1s (see absolute maximum ratings). There are several ways to protect the sense resistor from overcur-

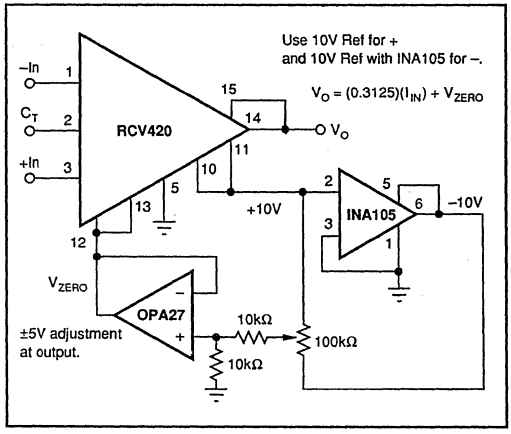


FIGURE 4. Optional Zero Adjust Circuit.

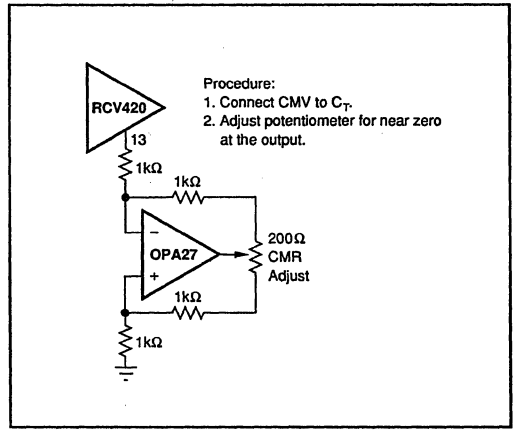


FIGURE 5. Optional Circuit for Externally Trimming CMR.

rent conditions exceeding these specifications. Refer to Figure 6. The simplest and least expensive method is a resistor as shown in Figure 6a. The value of the resistor is determined from the expression

$$R_X = V_{CC}/40mA - 75\Omega$$

and the full scale voltage drop is

$$V_{RX} = 20mA \times R_X$$

for a system operating off of a 32V supply $R_X = 725\Omega$ and $V_{RX} = 14.5V$. In applications that cannot tolerate such a large voltage drop, use circuits 6b or 6c. In circuit 6b a power JFET and source resistor are used as a current limit. The 200Ω potentiometer, R_X, is adjusted to provide a current limit of approximately 30mA. This circuit introduces a 1–4V drop at full scale. If only a very small series voltage drop at full scale can be tolerated, then a 0.032A series 217 fast-acting fuse should be used, as shown in Figure 6c.

RESISTOR NOISE IN THE RCV420

The output voltage noise of the RCV420 is dominated by the thermal noise generated in the resistor network. Figure 7 shows the model for calculating resistor noise in the RCV420. The expression for resistor noise is:

$$e_N(rms) = \sqrt{2\pi KTRB}$$

where: K = Boltzman's constant (J/°K)

T = Absolute temperature (°K)

R = Resistance (Ω)

B = Bandwidth (Hz)

At room temperature, this noise becomes:

$$e_N = 1.3 \times 10^{-10} \sqrt{R} \qquad (V/\sqrt{Hz})$$

The four noise sources in Figure 7 are:

$$e_{N1} = 1.3 \times 10^{-10} \sqrt{R_1}$$

$$e_{N2} = 1.3 \times 10^{-10} \sqrt{R_5}$$

$$e_{N3} = 1.3 \times 10^{-10} \sqrt{R_3}$$

$$e_{N4} = 1.3 \times 10^{-10} \sqrt{R_6}$$

Referred to output,

$$e_{NO1} = e_{N1}(A_D)$$

$$e_{NO2} = e_{N2}(A_D)$$

$$e_{NO3} = e_{N3}(R_4/R_3)$$

$$e_{NO4} = e_{N4}[(R_5 + R_6)/R_5](A_D)$$

where A_D is the differential voltage gain of amplifier. Adding as the root of the sums squared:

$$e_{NO} = \sqrt{(e_{NO1}^2 + e_{NO2}^2 + e_{NO3}^2 + e_{NO4}^2)}$$

e_{NO} at a 150kHz bandwidth

= 0.35mVrms

= 2.1mVp-p with a crest factor of 6 (statistically includes 99.7% of all noise peak occurrences).

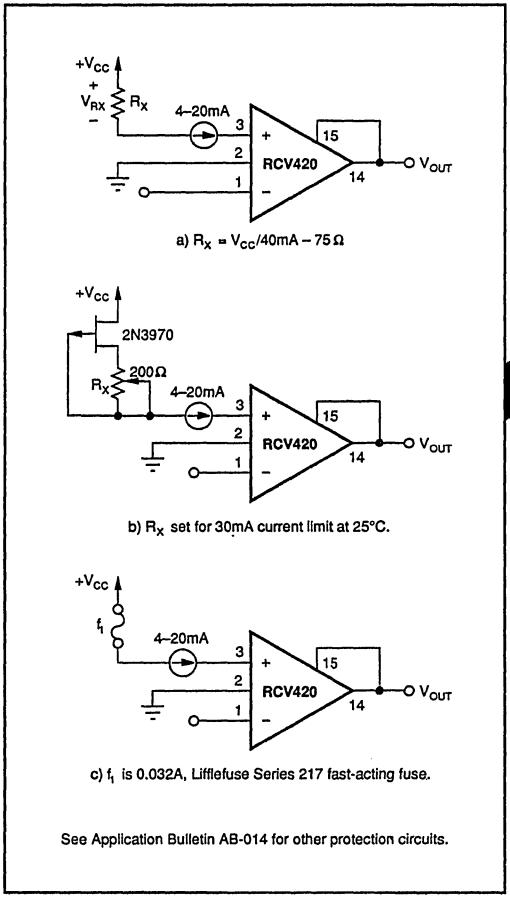


FIGURE 6. Protecting the Sense Resistors with a) Resistor, b) JFET, c) Fuse.

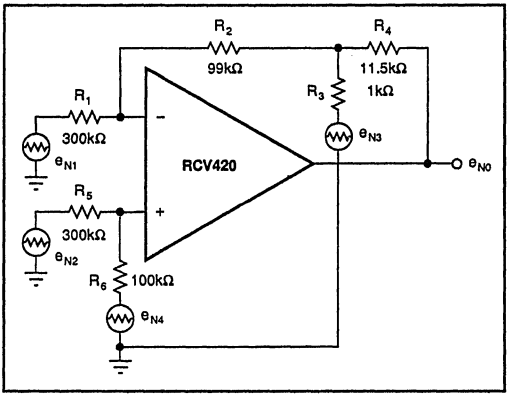


FIGURE 7. Resistor Noise Model.

VOLTAGE REFERENCE

The RCV420 contains a precision 10V reference. Figure 8 shows the circuit for output voltage adjustment. Trimming the output will change the voltage drift by approximately 0.007ppm/°C per mV of trimmed voltage. Any mismatch in TCR between the two sides of the potentiometer will also affect drift, but the effect is divided by approximately 5. The trim range of the voltage reference using this method is typically ±400mV. The voltage reference trim can be used to trim offset errors at the output of the RCV420. There is an 8:1 voltage attenuation from Ref In to RCV Out, and thus the trim range at the output of the receiver is typically ±50mV. The high-frequency noise (to 1MHz) of the voltage reference is typically 1mVp-p. When the voltage reference is used for level shifting, its noise contribution at the output of the receiver is typically 125µVp-p due to the 8:1 attenuation from Ref In to RCV Out. The reference noise can be reduced by connecting an external capacitor between the Noise Reduction pin and ground. For example, a 0.1µF capacitor reduces the high-frequency noise to about 200µVp-p at the output of the reference and about 25µVp-p at the output of the receiver.

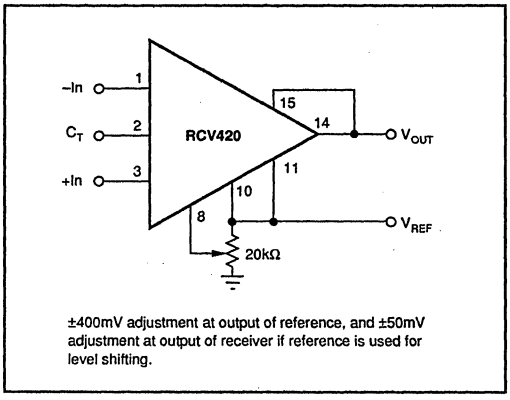


FIGURE 8. Optional Voltage Reference External Trim Circuit.

APPLICATIONS

The RCV420 is ideally suited for applications requiring precise current-to-voltage conversion and high CMR. The following figures show several typical application circuits.

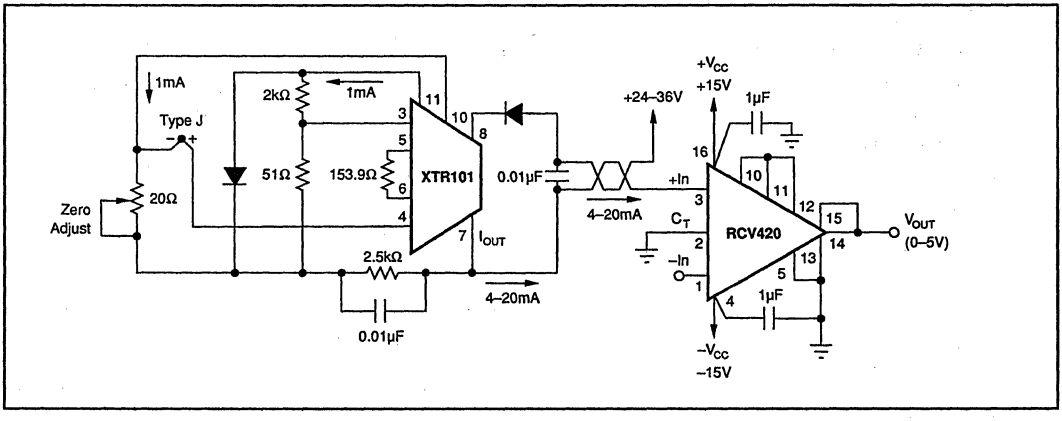


FIGURE 9. RCV420 Used in Conjunction with XTR101 to Form a Complete Solution for 4–20mA Loop.

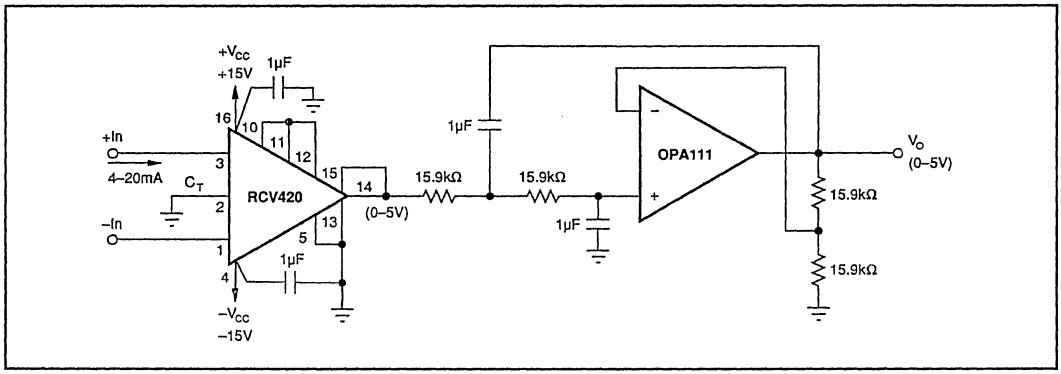


FIGURE 10. 4–20mA to 0-10V Conversion With Second-Order Active Low-Pass Filtering (f_{-3dB} = 10Hz).

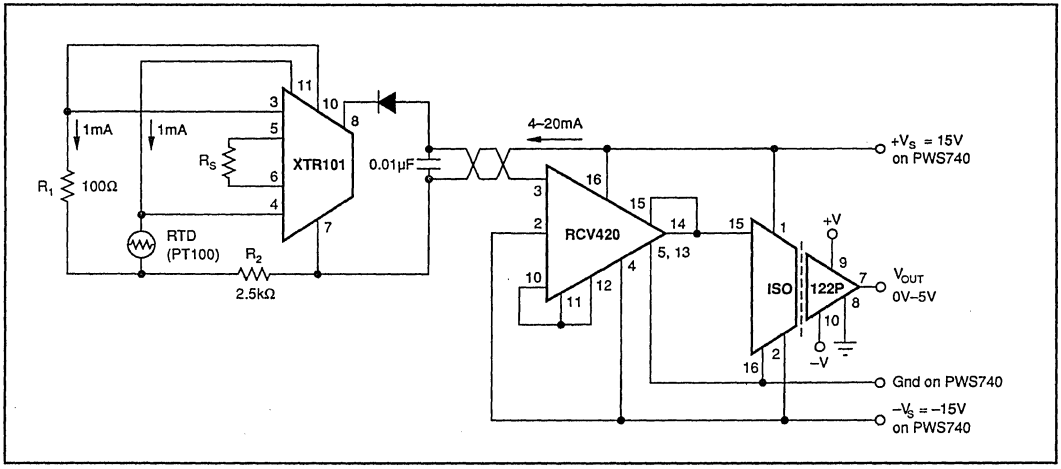
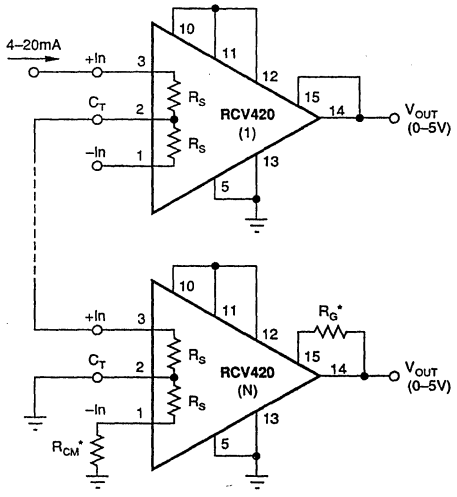


FIGURE 11. Isolated 4–20mA Instrument Loop (RTD shown).



*R_{CM} and R_G are used to provide a first order correction of CMR and Gain Error, respectively. Table 1 gives typical resistor values for R_{CM} and R_G when as many as three RCV420s are stacked. Table 2 gives typical CMR and Gain Error with no correction. Further improvement in CMR and Gain Error can be achieved using a 500kΩ potentiometer for R_{CM} and a 100Ω potentiometer for R_G.

RCV420	R_{CM} (kΩ)	R_G (Ω)
1	∞	0
2	200	7
3	67	23

TABLE 1. Typical Values for R_{CM} and R_G.

RCV420	CMR (dB)	GAIN ERROR %
1	94	0.025
2	68	0.075
3	62	0.200

TABLE 2. Typical CMR and Gain Error Without Correction.

FIGURE 12. Series 4–20mA Receivers.

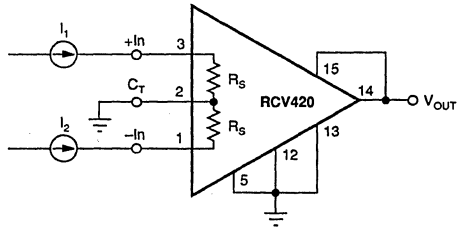


FIGURE 13. Differential Current-to-Voltage Converter.

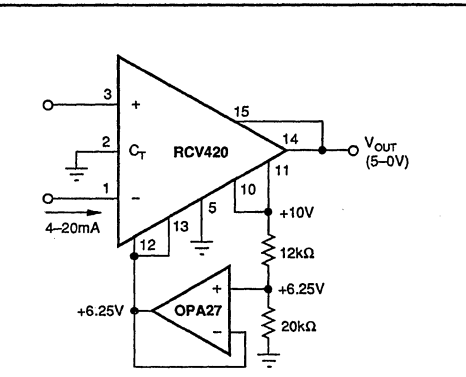


FIGURE 14. 4–20mA to 5–0V Conversion.

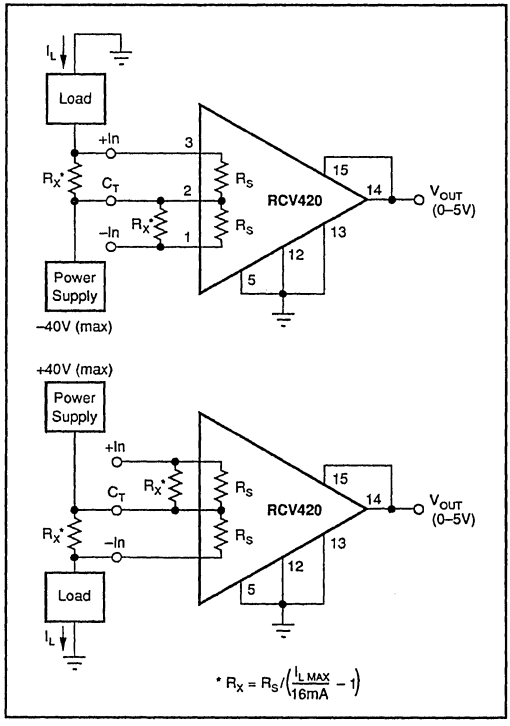


FIGURE 15. Power Supply Current Monitor Circuit.

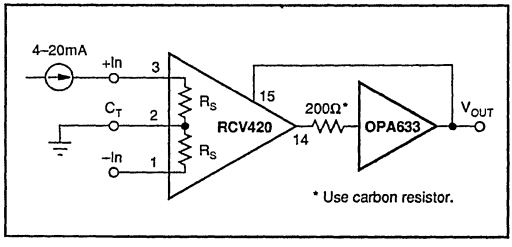


FIGURE 16. 4–20mA Receiver with Output Current Boosted to ±100mA.

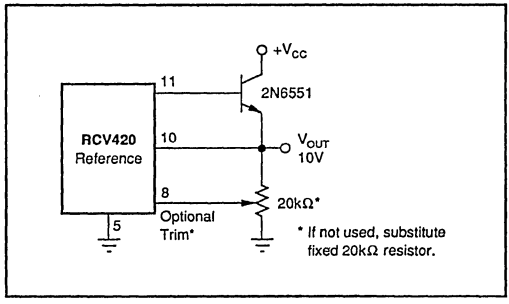


FIGURE 17. 10V with Output Current Boosted to 100mA max.

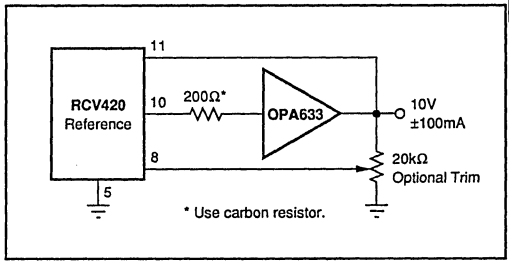


FIGURE 18. 10V with Output to Source/Sink 100mA.

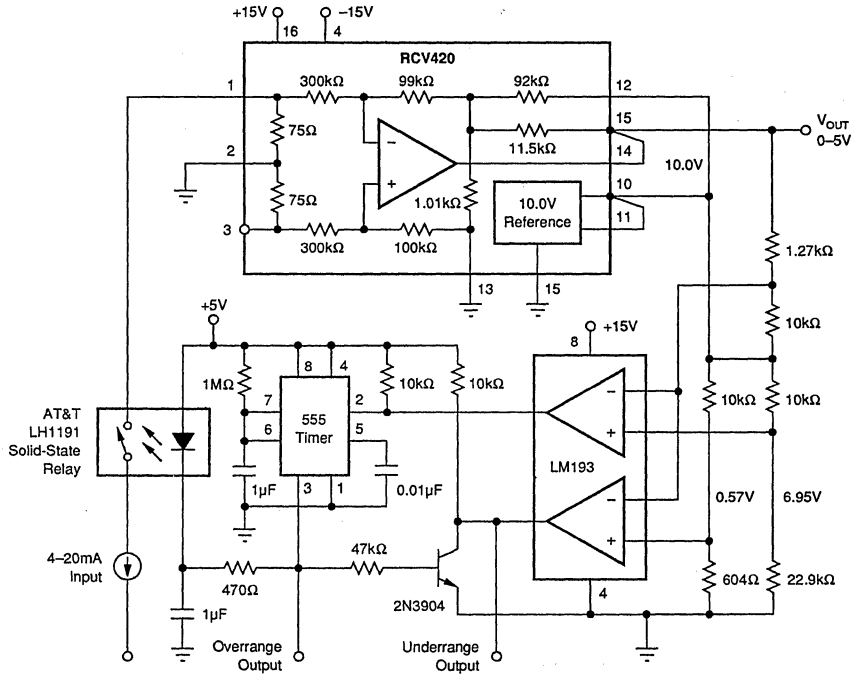


FIGURE 19. 4–20mA Current Loop Receiver with Open Line and Overrange Detection Logic Outputs.

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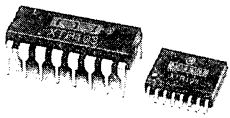


XTR103

ADVANCE INFORMATION
SUBJECT TO CHANGE

Precision 4mA to 20mA TWO-WIRE RTD TRANSMITTER

FEATURES

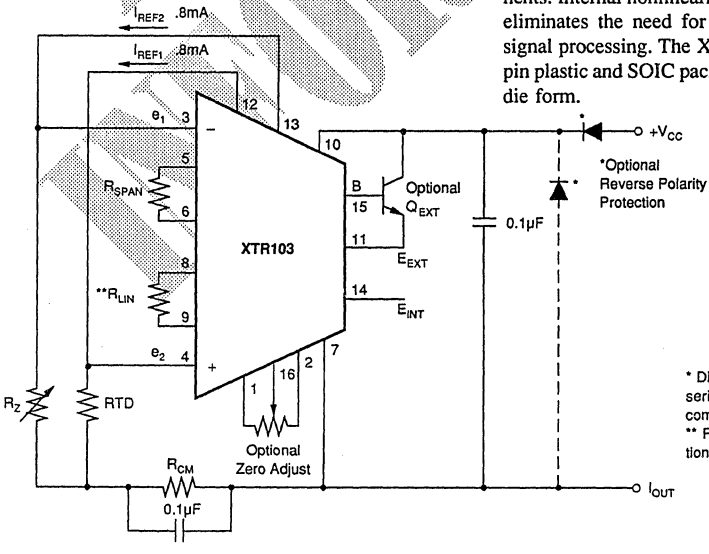
- INTEGRAL SENSOR EXCITATION AND LINEARIZATION
- LOW ZERO ERROR: 10µA
- LOW SPAN NONLINEARITY: 0.01%
- HIGH POWER SUPPLY REJECTION: 120dB
- HIGH COMMON-MODE REJECTION: 100dB
- WIDE SUPPLY RANGE: 9V to 40V
- –40°C to +85°C SPECIFIED TEMPERATURE RANGE

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- FACTORY AUTOMATION
- SCADA
- ENERGY MANAGEMENT SYSTEMS

DESCRIPTION

The XTR103 is a precision 4mA to 20mA, two wire transmitter. It provides a reliable, low-cost solution for Resistance Temperature Detection (RTD) signal conditioning. The circuit consists of a high accuracy instrumentation amplifier (IA), a voltage-controlled output current source, dual-matched precision current sources, and RTD linearization circuitry. Dielectric isolation and laser-trimmed thin film resistors guarantee a level of performance which is both difficult and expensive to reliably achieve with discrete components. Internal nonlinearity correction of RTD sensors eliminates the need for additional analog or digital signal processing. The XTR103 is housed in both 16-pin plastic and SOIC packages, and is also available in die form.



* Diode may be placed in either position; series connection increases minimum compliance voltage.
** R_{LIN} provides RTD nonlinearity correction.

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PDS-1065

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_{CC} = +24V, and 2N2222 external transistor.

PARAMETER	CONDITIONS	XTR103AP/U MIN	XTR103AP/U TYP	XTR103AP/U MAX	XTR103BP MIN	XTR103BP TYP	XTR103BP MAX	UNITS
OUTPUT								
Current	Linear Operation	4		20	*		*	mA
	Derated Performance	3.8		22	*		*	mA
Full Scale Output Current Error	Δe_{IN} = 1V, R_S = Infinite			50			25	µA
Current Limit			32	40		*	*	mA
Noise (to 1kHz)	R_S = 25Ω		6			*		µVp-p
Load Resistance[1]	At V_{CC} = 24V, I_O = 20mA			750			*	Ω
ZERO								
Initial Error[2]	e_{IN} = 0, R_S = Infinite			20			10	µA
vs Temperature				30			15	ppm/°C
vs Supply Voltage				20			10	ppm/V
vs Common-Mode Voltage				20			10	ppm/V
SPAN								
Output Current Equation	R_S in Ω, e_1 and e_2 in V	$I_O = 4mA + [0.016 + (40/R_S)] (e_2 - e_1)$						
Span Equation		$S = [0.016 + (40/R_S)]$						A/V
Untrimmed Error[3]		–1	–0.5	0	*	*	*	%
vs Temperature	Excluding TCR of R_S			50			25	ppm/°C
Nonlinearity: Ideal Input[4]				0.01			*	%
Sensor Input[5]				0.1			*	%
Hysteresis			0			*		%
Dead Band			0			*		%
INPUT								
Voltage Range				1			*	V
Impedance: Differential			3			*		GΩ
Common-mode			0.5			*		GΩ
Offset Voltage				50			25	µV
vs Temperature				1			0.5	µV/°C
vs Supply		110			120			dB
Bias Current				200			*	nA
vs Temperature				2			*	nA/°C
Offset Current				20			*	nA
vs Temperature				0.2			*	nA/°C
Common-Mode Range	e_1 and e_2 with respect to pin 7	2		4	*		*	V
Common-Mode Rejection	DC	90			100			dB
CURRENT SOURCES								
Magnitude			0.8			*		mA
Accuracy				0.5			0.25	%
vs Temperature				100			50	ppm/°C
vs Supply			50			*		ppm/V
vs Time			10			*		ppm/mo.
Compliance Voltage	with respect to pin 7			V_{CC} – 5			*	V
Match				0.1			*	%
vs Temperature				20			10	ppm/°C
vs V_{CC}			10			*		ppm/V
vs Time			1			*		ppm/mo.
Output Impedance			25			*		MΩ
POWER SUPPLY								
Voltage Range		9		40	*		*	V
TEMPERATURE RANGE								
Specification		–40		85	*		*	°C
Operating		–40		85	*		*	°C
Storage		–55		125	*		*	°C

NOTES: (1) The transmitter's maximum load resistance depends on V_{CC} and is determined by the equation: $R_{LMAX} = (V_{CC} - 9V) / I_{OMAX}$. (2) Zero Error includes current source errors. (3) Can be adjusted to zero. (4) Best fit span nonlinearity with an ideal voltage input. (5) Best fit, corrected span nonlinearity with a PT100 RTD input operated from –200°C to +850°C.

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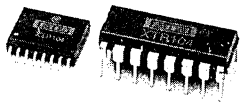


XTR104

ADVANCE INFORMATION
SUBJECT TO CHANGE

Precision 4mA to 20mA TWO-WIRE STRAIN GAUGE TRANSMITTER

FEATURES

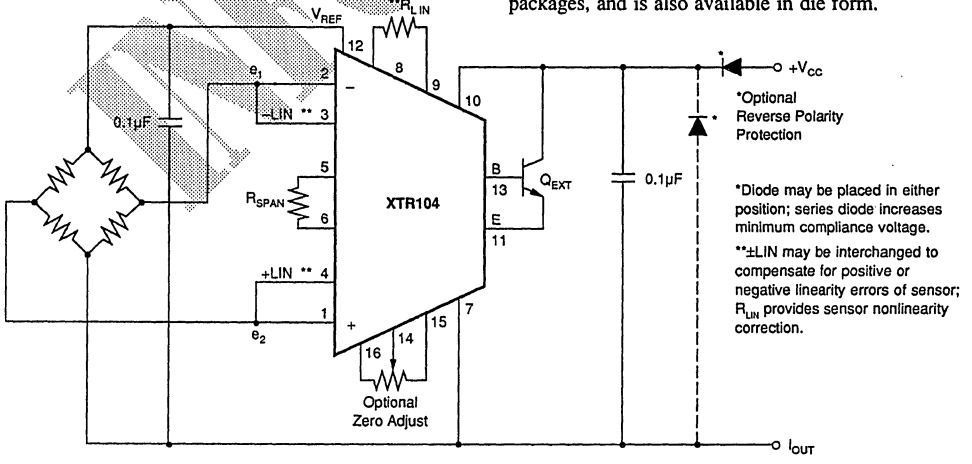
- INTEGRAL SENSOR EXCITATION AND LINEARIZATION
- LOW ZERO ERROR: 10µA
- LOW SPAN NONLINEARITY: 0.01%
- HIGH POWER SUPPLY REJECTION: 120dB
- HIGH COMMON-MODE REJECTION: 100dB
- WIDE SUPPLY RANGE: 9V to 40V
- –40°C to +85°C SPECIFIED TEMPERATURE RANGE

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- FACTORY AUTOMATION
- SCADA
- WEIGHTING SYSTEMS
- ACCELEROMETERS

DESCRIPTION

The XTR104 is a precision 4mA to 20mA, two wire transmitter. It provides a reliable, low-cost solution for high-impedance strain gauge bridge signal conditioning. The circuit consists of a high accuracy instrumentation amplifier (IA), a voltage-controlled output current source, a precision 5V reference, and bridge linearization circuitry. Dielectric isolation and laser-trimmed thin film resistors guarantee a level of performance which is both difficult and expensive to reliably achieve with discrete components. Internal nonlinearity correction of bridges eliminates the need for additional analog or digital signal processing. The XTR104 is housed in both 16-pin plastic and SOIC packages, and is also available in die form.



*Diode may be placed in either position; series diode increases minimum compliance voltage.

**±LIN may be interchanged to compensate for positive or negative linearity errors of sensor; R_{LIN} provides sensor nonlinearity correction.

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PDS-1066

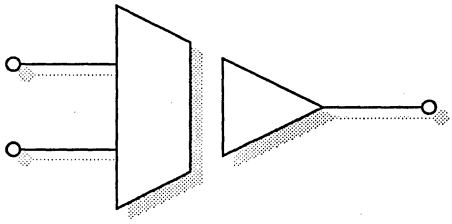
SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_{CC} = +24V, and 2N2222 external transistor.

PARAMETER	CONDITIONS	XTR104AP/U MIN	XTR104AP/U TYP	XTR104AP/U MAX	XTR104BP MIN	XTR104BP TYP	XTR104BP MAX	UNITS
OUTPUT								
Current	Linear Operation	4		20	*		*	mA
	Derated Performance	3.8		22	*		*	mA
Full Scale Output Current Error	Δe_{IN} = 1V, R_S= Infinite			50			25	µA
Current Limit			32	40		*	*	mA
Noise (to 1kHz)	R_S = 25Ω		6			*		µVp-p
Load Resistance[1]	At V_{CC} = 24V, I_O = 20mA			750			*	Ω
ZERO								
Initial Error[2]	e_{IN} = 0, R_S = Infinite			20			10	µA
vs Temperature				30			15	ppm/°C
vs Supply Voltage				20			10	ppm/V
vs Common-mode Voltage				20			10	ppm/V
SPAN								
Output Current Equation	R_S in Ω, e_1 and e_2 in V	I_O = 4mA + [0.016 + (40/R_S)] (e_2 – e_1)						
Span Equation		S = [0.016 + (40/R_S)]						A/V
Untrimmed Error[3]		–1	–0.5	0	*	*	*	%
vs Temperature	Excluding TCR of R_S			50			25	ppm/°C
Nonlinearity: Ideal Input[4]				01			*	%
Sensor Input[5]				0.1			*	%
Hysteresis			0			*		%
Dead Band			0			*		%
INPUT								
Voltage Range				1			*	V
Impedance: Differential			3			*		GΩ
Common-mode			0.5			*		GΩ
Offset Voltage				50			25	µV
vs Temperature				1			0.5	µV/°C
vs Supply		110			120			dB
Bias Current				200			*	nA
vs Temperature				2			*	nA/°C
Offset Current				20			*	nA
vs Temperature				0.2			*	nA/°C
Common-mode Range	e_1 and e_2 with respect to pin 7	2		3	*		*	V
Common-mode Rejection	DC	90			100			dB
VOLTAGE REFERENCE								
Magnitude			5			*		V
Accuracy				0.20			0.1	%
vs Temperature				50			25	ppm/°C
vs Supply			5			*		ppm/V
vs Load			50			*		ppm/mA
vs Time			10			*		ppm/mo.
Load Resistance		2500			*			Ω
POWER SUPPLY								
Voltage Range		9		40	*		*	V
TEMPERATURE RANGE								
Specification		–40		85	*		*	°C
Operating		–40		85	*		*	°C
Storage		–55		125	*		*	°C

NOTES: (1) The transmitter's maximum load resistance depends on V_{CC} and is determined by the equation: $R_{L\,MAX} = (V_{CC} - 9V) / I_{O\,MAX}$. (2) Zero Error includes voltage reference errors. (3) Can be adjusted to zero. (4) Best fit span nonlinearity with an ideal voltage input. (5) Best fit, corrected span nonlinearity with a 100mV full-scale input with a 2% endpoint nonlinearity.



ISOLATION PRODUCTS

4

WHAT IS AN ISOLATION AMPLIFIER?

An isolation amplifier is a device with the primary function of providing ohmic isolation (breaking the ohmic continuity of an electrical signal) between the input signal/circuitry and the output of the amplifier. It usually consists of an input operational amplifier or instrumentation amplifier followed by a unity-gain isolation stage. The sole purpose of the unity-gain isolation stage is to completely isolate the input from the output of the device. Ideally, the ohmic continuity of the input signal is broken (at the isolation barrier) yet accurate signal transfer without any attenuation is achieved across the unity-gain isolation stage. An important feature of an isolation amplifier is that it has a completely floating input which helps eliminate cumbersome connections to source ground.

Figures 1 and 2 show typical isolation amplifier applications. The isolation-mode voltage V_{ISO} is the voltage that exists across the isolation barrier. The contribution of the output-referred error caused by V_{ISO} is (V_{ISO}/IMRR) x Gain where IMRR is the Isolation Mode Rejection Ratio. V_{SIG} is the differential input signal and V_{CM} is the common-mode voltage. Leakage Current is the current that flows across the isolation barrier with some specified isolation voltage applied between the input and the output.

CHARACTERISTICS OF ISOLATION AMPLIFIERS

Following is a discussion of some characteristics and terms unique to isolation amplifiers.

COMMON-MODE VOLTAGE AND ISOLATION VOLTAGE

Some manufacturers (other than Burr-Brown) treat common-mode voltage and isolation voltages synonymously in describing the use and /or specifications of isolation amplifiers. It is important to understand the significance of these terms and the difference between them.

When the input common is grounded, the differential input signal V_D (see Figure 1) can be floated by the amount V_{CM} above the input ground. V_{CM} is the common-mode voltage (CMV) and is generally ±10V, limited by the CMV rating of the input stage amplifier. In applications involving higher systems common-mode voltages, the input common terminal is not grounded and the common-mode voltages are referenced across the isolation barrier to the output common terminal.

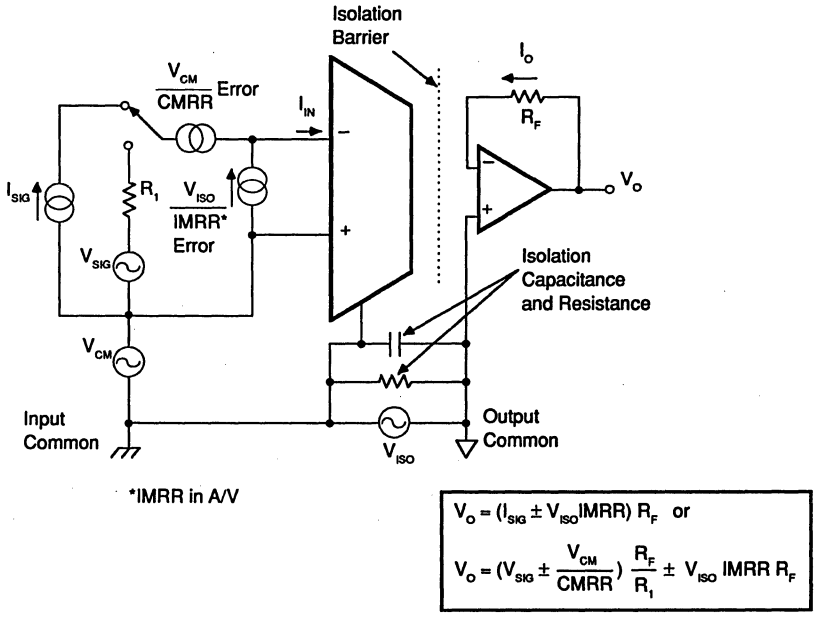


Figure 1. Typical Isolation Amplifier, Current (Input) Mode.

The isolation voltage V_{ISO} shown in Figure 1 is the potential difference between the input common and the output common terminals. The isolation voltage rating describes the amount of voltage that the isolation barrier can withstand without breakdown. This feature of the isolation amplifier allows two distinct ground connections to be made when necessary. It allows the isolation amplifier to be used in applications involving very high common-mode voltages and in applications of breaking ground loops.

Many applications involve a large "system common-mode voltage." In such applications, the isolation amplifier's input common terminal is not connected to any ground but the output common terminal is connected to the system ground. In such a case, the term V_{CM} shown in Figures 1 and 2 becomes negligible and V_{ISO} determines the safe limit for the system common-mode voltage. In this manner, the isolation amplifier can accommodate common-mode voltages of 2000V or more.

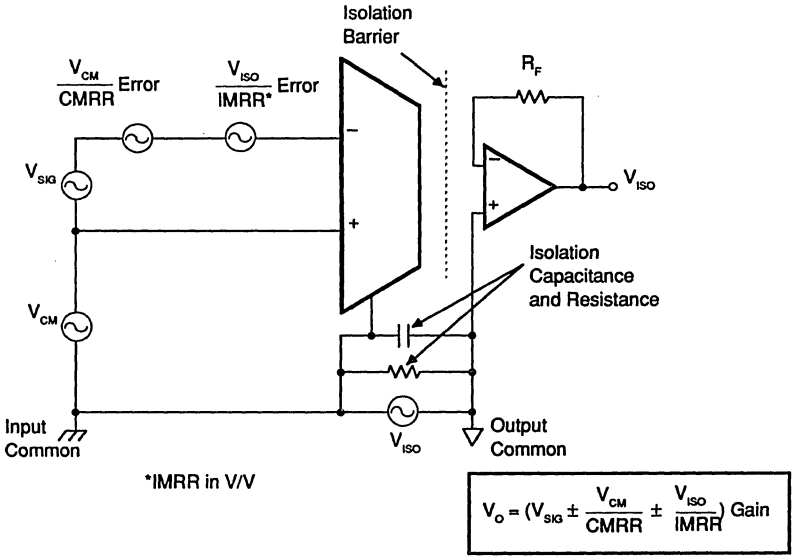


Figure 2. Typical Isolation Amplifier, Voltage (Input) Mode.

COMMON-MODE REJECTION AND ISOLATION REJECTION

Isolation-mode rejection (IMR) is another term that some other manufacturers refer to as common-mode rejection (CMR). The preceding discussion on the common-mode voltage and isolation voltage helps recognize the difference between CMR and IMR. The CMR is the measure of the input stage amplifier's ability to reject common-mode input signals (common-mode with reference to the output common) while transmitting the differential signal across the isolation barrier. The isolation-mode rejection ratio (IMRR) is defined by the equations shown in Figures 1 and 2. Thus, understanding the IMR capability of isolation amplifiers allows their meaningful use in applications requiring very high common-mode rejection ratios such as 100dB to 140dB.

ISOLATION VOLTAGE RATINGS, TEST VOLTAGE

It is important to understand the significance of the continuous derated isolation voltage specification and its relationship to the actual test voltage applied to the unit. Since a "continuous" test is impractical in a product manufacturing situation (implies infinite test duration) it is generally accepted practice to perform a production test at a higher voltage than the continuous rating for some shorter length of time.

The important consideration is then the relationship between actual test conditions and the continuous derated minimum specification." There are several rules of thumb used throughout the industry to establish this relationship. For most isolation amplifiers, Burr-Brown has chosen a very

conservative one: $V_{TEST} = (2 \times V_{CONTINOUS\ RATING}) + 1000V$. This relationship is appropriate for conditions where the system transient voltages are not well defined.* Where the real voltages are well defined or where the isolation voltage is not continuous, the user may choose to use a less conservative derating to establish a specification from the test voltage.

Beginning with the introduction of the ISO120 and ISO121, new introductions are being tested for partial discharge. To accommodate poorly defined transients, the part under test is exposed to a voltage 1.6 times the continuous rated voltage and must display a partial discharge level of ≤5pC in a 100% production test. This method is described in detail in the ISO120 data sheet.

APPLICATIONS OF ISOLATION AMPLIFIERS

When one or more of the following conditions/requirements are present in an application, an isolation amplifier would generally be the right choice as a signal conditioning device:

- When ohmic isolation between the signal source and the output is a requirement (isolation impedance between the input and the output is >10MΩ).
- When common-mode noise and voltage rejection requirements are >100dB.
- When is necessary to process signals in the presence of, or riding on, high common-mode voltages (CMV >> 10V).

In general, most applications can be broadly categorized into the following four types:

- Amplifying and measuring low level signals in the presence of high common-mode voltages.
- Breaking ground loops and/or eliminating source ground connections. The isolation amplifier provides full floating input, eliminating the need for connections to source ground, and thus allowing two-wire hook-up to the signal sources.
- Providing an interface between medical patient monitoring equipment and the transducer/devices that may be in physical contact with the patients. Such applications require high isolation voltage levels and very low leakage currents.
- Providing isolation protection to electronic instruments/equipment. Large common-mode voltages occasionally cause hazardous electronic faults. The low leakage currents and high isolation voltage capabilities of isolation amplifiers help protect instruments against damage caused by such faults.

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*Reference National Electrical Manufacturers Association (NEMA) Standards Parts ICS 1-109 and ICS 1-111.

Isolation amplifier performance requirements vary significantly, depending on the type of requirement. In applications where bandwidth and speed of response are more important than gain accuracy and linearity, the optically or capacitively coupled amplifiers will be the best choice. For applications where gain accuracy and linearity are key parameters, Burr-Brown's family of transformer or capacitively coupled amplifiers are the suitable choice.

ISOLATION AMPLIFIERS SELECTION GUIDES

The following Selection Guides show parameters for the high grade. Refer to the Product Data Sheet for a full selection of grades. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book.*

TRANSFORMER-COUPLED AMPLIFIERS **Boldface = NEW**

Descrip	Model	Isolation Voltage (V) Cont Peak	Isolation Voltage (V) Pulse Test, Peak	Isolation Mode Rejection, typ DC (dB)	Isolation Mode Rejection, typ 60Hz (dB)	Leakage Current at Test Voltage (μA)	Iso Impedance (Ω)	Iso Impedance (pF)	Gain Nonlinearity max (%)	Gain Nonlinearity typ (%)	Voltage Drift (±μV/°C) max	Bias Current max	±3dB Freq (kHz)	Ext Iso Power Req	Temp[1]	Page No.
High Isolation Voltage	3656G	±3500	±8000	160	125	0.5	10^{12}	6	±0.05	±0.03	5+ (1000/G_1)	100nA	30	No	Ind	4-108
Low Cost Self-Powered	**ISO212P**	**±1060**	**±1697**	**160**	**115**	**2**	**10^{10}**	**12**	**±0.025**	**±0.015**	**±30 (±30/G_1)**	**50nA**	**1**	**No**	**Com**	**S4-51**

NOTES: The package for the 3656G is a DIP, the package for the ISO212P is a SIP. (1) Ind = –25°C to +85°C Com = 0°C to +70°C.

OPTICALLY COUPLED AMPLIFIERS

Descrip	Model	Isolation Voltage (V) Cont Peak	Isolation Voltage (V) Pulse/ Test, Peak	Isolation Mode Rejection, typ DC (dB)	Isolation Mode Rejection, typ 60Hz (dB)	Leakage Current at Test Voltage (μA)	Iso Impedance (Ω)	Iso Impedance (pF)	Gain Nonlinearity max (%)	Gain Nonlinearity typ (%)	Voltage Drift (±μV/°C) max	Bias Current max	±3dB Freq (kHz)	Ext Iso Power Req	Temp[1]	Page No.
Balanced Current Input	3650G	±2000	±5000	140	120	0.25[2]	10^{12}	1.8	±0.05	±0.02	5	10nA	15	Yes[3]	Ind	4-100
Balanced	3652G	±2000	±5000	140	120	0.25[2]	10^{12}	1.8	±0.1	±0.05	25	50nA	15	Yes	Ind	4-100
Low Drift Wide BW	ISO100P	750	2500	146[3]	108[3]	0.3	10^{12}	2.5	0.07	0.02	4[3]	10nA	60	Yes	Ind	4-8

NOTES: All packages are DIPs. (1) Ind = –25°C to +85°C. (2) At 240V/60Hz. (3) R_{IN} = 10kΩ, Gain = 100.

CAPACITOR COUPLED, HERMETICALLY SEALED AMPLIFIERS **Boldface = NEW**

Descrip	Model	Isolation Voltage (V) Cont Peak	Isolation Voltage (V) Pulse/ Test, Peak	Isolation Mode Rejection, typ DC (dB)	Isolation Mode Rejection, typ 60Hz (dB)	Leakage Current at Test Voltage (μA)	Iso Impedance (Ω)	Iso Impedance (pF)	Gain Nonlinearity max (%)	Gain Nonlinearity typ (%)	Voltage Drift (±μV/°C) max	Bias Current max	±3dB Freq (kHz)	Ext Isol Power Req	Temp[1]	Page No.
1500VAC Isolation	ISO102B	±2121	±4000	160	120	1.0	10^{14}	6	±0.003	±0.002	±250	100μA	70	Yes	Ind	4-20
	ISO120B	±2121	±3535[2]	160	115	0.5	10^{14}	2	±0.02	±0.005	±150	50μA	60	Yes	Ind	4-44
	ISO122P	**±2121**	**±3394**	**160**	**140**	**0.5**	**10^{14}**	**2**	**±0.02**	**±0.008**	**±200**	**50μA**	**50**	**Yes**	**Com[3]**	**S4-40**
3500VAC Isolation	ISO106B	±4950	±8000	160	130	1.0	10^{14}	6	±0.025	±0.007	±250	100μA	70	Yes	Ind	4-20
	ISO121B	±4950	±5600[2]	160	115	0.5	10^{14}	2	±0.01	±0.005	±150	50μA	60	Yes	Ind	4-20

NOTES: All packages are DIPs. (1) Ind = –25°C to +85°C. Com = 0°C to +70°C. (2) Partial discharge voltage. (3) Not Hermetic.

ISOLATION POWER SUPPLIES[1] — **Boldface = NEW**

Description	Model	Isolation Voltage (V) Cont Peak	Isolation Voltage (V) Pulse/ Test Peak	Input Voltage (VDC) min	Input Voltage (VDC) max	Leakage Current 240VAC 60Hz (μA)	Isolation Impedance (Ω)	Isolation Impedance (pF)	Current, Balanced Loads On All Outputs (mA) Rated	Current, Balanced Loads On All Outputs (mA) Max[1]	Sensitivity To Input Change (V/V)	Temp[2]	Pkg	Page No.
Single ±15V Output	700	1500	4200	10	18	1	10^{10}	5	±3-30	±60	1.08	Ind	Mod	4-86
	700U	2000	5000	10	18	1	10^{10}	3	±3-30	±60	1.08	Ind	Mod	4-86
	PWS725A	2121	4000	7	18	1.2	10^{12}	9	±15	±40	1.15	Ind	DIP	4-65
	PWS726A	4950	8000	7	18	1.2	10^{12}	9	±15	±40	1.15	Ind	DIP	4-65
Dual ±15V Output	722	4950	8000	5	16	1	10^{10}	6	±3-40	±50	1.13	Ind	Mod	4-92
	PWS727	**1060**	**1700**	**10**	**18**	**1.5**	10^{12}	**8**	**±15**	**±30**	**1.15**	**Com**	**Mod**	**S4-62**
	PWS728	**1060**	**1700**	**4.5**	**5.5**	**1.5**	10^{12}	**8**	**±15**	**±30**	**3.2**	**Com**	**Mod**	**S4-62**
Quad ±15V Output	710	1000	3100	10	18	1	10^{10}	8	±9.5	±60	1.08	Ind	Mod	4-88
Quad ±8V Output	724	1000	3000	5	16	1	10^{10}	6	±3-16	±60	0.63	Ind	Mod	
Multiple Output (1-8)	PWS740	2121	4000	7	20	1.5	10^{12}	3	30[3]	60[3]	1.20	Ind	Sys[4]	4-96
	PWS745[8]	**1060**	**1700**	**4.5[5]**	**18[6]**	**1.5**	10^{12}	**8**	**±15**	**30**	[7]	**Ind**	**Comp**	**S4-69**
	PWS750	**1060**	**1700**	**4.5[5]**	**18[6]**	**1.5**	10^{12}	**8**	**±15**	**30**	[7]	**Ind**	**Comp**	**S4-71**

NOTES: (1) See complete Product Data Sheet for full specifications, especially regarding output current capabilities. (2) Ind = –25°C to +85°C. Com = 0°C to +70°C. (3) Per channel. (4) 1 TO-3 driver per 8 channels, plus 2 DIPs per channel. (5) 5V operation. (6) 15V operation. (7) 5V operation: 3.2; 15V operation: 1.15. (8) PWS745-1 driver may also be used with PWS740 and PWS750 components.

CAPACITOR-COUPLED ISOLATION AMPLIFIER, WITH POWER — **Boldface = NEW**

Description	Model	Isolation Voltage (V) Cont Peak	Isolation Voltage (V) Pulse/ Test, Peak	Isolation Mode Rejection, typ DC (dB)	Isolation Mode Rejection, typ 60Hz (dB)	Leakage Current at Test Voltage (μA)	Iso Impedance (Ω)	Iso Impedance (pF)	Gain Nonlinearity max (%)	Gain Nonlinearity typ (%)	Voltage Drift (±μV/°C) max	Bias Current max	±3dB Freq (kHz)	Temp[1]	Page No.
1500VAC Input Power	ISO103	2121	3394[2]	160	130	1.0	10^{12}	11	0.025	0.01	400[1]	50μA	20	Ind	S4-8
1500VAC Output Power	ISO113	2121	3394[2]	160	130	1.0	10^{12}	11	0.02	0.012	400[1]	50μA	20	Ind	S4-32
2500VAC Input Power	ISO107	3535	8000	160	100	1.2	10^{12}	13	0.025	0.01	400[1]	50μA	20	Ind	S4-16

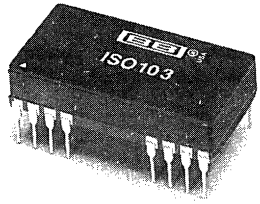
NOTES: All packages are DIPs. (1) Ind = –25°C to +85°C. (2) Partial discharge voltage.

CAPACITIVELY COUPLED VOLTAGE-TO-FREQUENCY CONVERTER — **Boldface = NEW**

Descrip	Model	Isolation Voltage (V) Cont Peak	Isolation Voltage (V) Pulse/ Test Peak	Leakage Current at Test Voltage (μA)	Isolation Impedance (Ω)	Isolation Impedance (pF)	Non-linearity at 1MHz (typ)	Bias Current max (μA)	Operating Freq max (MHz)	External Isolation Power Req	Temp[1]	Page No.
1500Vrms	ISO108	2121	3394[2]	0.3 typ	10^{12}	3	0.01	250	3	Yes	Ind	S4-24
3500Vrms	ISO109	4950	7918[2]	0.3 typ	10^{12}	3	0.01	250	3	Yes	Ind	S4-24

NOTES: Package is DIP. (1) Ind = –25°C to +85°C. (2) Partial discharge voltage.

BURR-BROWN®



ISO103

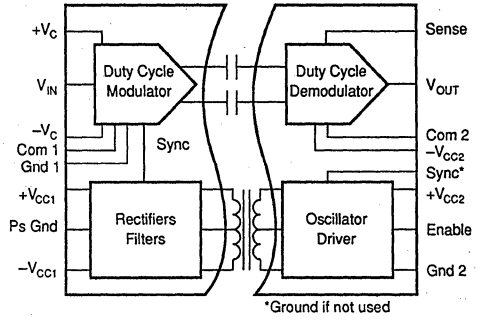
Low-Cost, Internally Powered ISOLATION AMPLIFIER

FEATURES

- SIGNAL AND POWER IN ONE DOUBLE-WIDE (0.6") SIDE-BRAZED PACKAGE
- 5600Vpk TEST VOLTAGE
- 1500Vrms CONTINUOUS AC BARRIER RATING
- WIDE INPUT SIGNAL RANGE: –10V to +10V
- WIDE BANDWIDTH: 20kHz Small Signal, 20kHz Full Power
- BUILT-IN ISOLATED POWER: ±10V to ±18V Input, ±50mA Output
- MULTICHANNEL SYNCHRONIZATION CAPABILITY (TTL)
- BOARD AREA ONLY 0.72in.² (4.6cm²)

APPLICATIONS

- MULTICHANNEL ISOLATED DATA ACQUISITION
- ISOLATED 4-20mA LOOP RECEIVER AND POWER
- POWER SUPPLY AND MOTOR CONTROL
- GROUND LOOP ELIMINATION



DESCRIPTION

The ISO103 isolation amplifier provides both signal and power across an isolation barrier. The ceramic non-hermetic hybrid package with side-brazed pins contains a transformer-coupled DC/DC converter and a capacitor-coupled signal channel.

Extra power is available on the isolated input side for external input conditioning circuitry. The converter is protected from shorts to ground with an internal current limit, and the soft-start feature limits the initial currents from the power source. Multiple-channel synchronization can be accomplished by applying a TTL clock signal to paralleled Sync pins. The Enable control is used to turn off transformer drive while keeping the signal channel demodulator active. This feature provides a convenient way to reduce quiescent current for low power applications.

The wide barrier pin spacing and internal insulation allow for the generous 1500Vrms continuous rating. Reliability is assured by 100% barrier breakdown testing that conforms to UL1244 test methods. Low barrier capacitance minimizes AC leakage currents.

These specifications and built-in features make the ISO103 easy to use, as well as providing for compact PC board layouts.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1004A

SPECIFICATIONS

ELECTRICAL

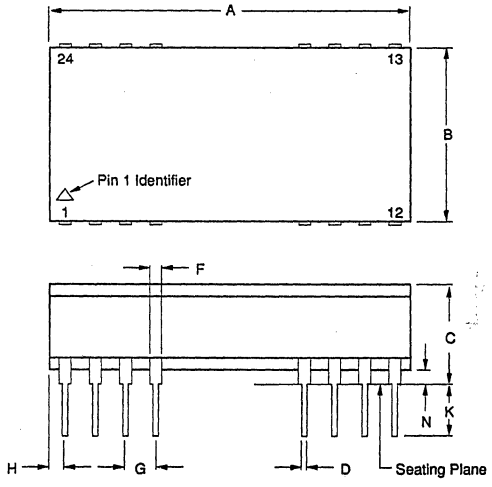
At T_A = +25°C and V_{CC2} = ±15V, ±15mA output current unless otherwise noted.

PARAMETER	CONDITIONS	ISO103 MIN	ISO103 TYP	ISO103 MAX	ISO103B MIN	ISO103B TYP	ISO103B MAX	UNITS
ISOLATION								
Rated Continuous Voltage[1]								
AC, 60Hz	T_{MIN} to T_{MAX}	1500			*			Vrms
DC	T_{MIN} to T_{MAX}	2121			*			VDC
Test Breakdown, 100% AC, 60Hz	10s	5657			*			Vpk
Isolation-Mode Rejection	1500Vrms, 60Hz		130			*		dB
	2121VDC		160			*		dB
Barrier Impedance			10^{12} || 9			*		Ω || pF
Leakage Current	240Vrms, 60Hz		1	2		*	*	µA
GAIN								
Nominal			1			*		V/V
Initial Error			±0.12	±0.3		±0.08	±0.15	% FSR
Gain vs Temperature			±60	±100		±20	±50	ppm/°C
Nonlinearity	V_O = –10V to 10V		±0.026	±0.05		±0.018	±0.025	% FSR
	V_O = –5V to 5V		±0.009			*		%FSR
INPUT OFFSET VOLTAGE								
Initial Offset			±20	±60		*	*	mV
vs Temperature			±300	±500		±100	±250	µV/°C
vs Power Supplies	V_{CC2} = ±10V to ±18V		0.9			*		mV/V
vs Output Supply Load	I_O = 0 to ±50mA		±0.3			*		mV/mA
SIGNAL INPUT								
Voltage Range	Output Voltage in Range	±10	±15		*	*		V
Resistance			200			*		kΩ
SIGNAL OUTPUT								
Voltage Range		±10	±12.5		*	*		V
Current Drive		±5	±20		*	*		mA
Ripple Voltage, 800kHz Carrier			25			*		mVp-p
400Ω/4.7nF (See Figure 4)			5			*		mVp-p
Capacitive Load Drive			1000			*		pF
Voltage Noise			4			*		µV/√Hz
FREQUENCY RESPONSE								
Small Signal Bandwidth			20			*		kHz
Slew Rate			1.5			*		V/µs
Settling Time	0.1%, –10/10V		75			*		µs
POWER SUPPLIES								
Rated Voltage, V_{CC2}			±15			*		V
Voltage Range		±10		±18	*		*	V
Input Current	I_O = ±15mA		+90/–4.5			*		mA
Ripple Current	No Filter		60			*		mAp-p
C_{IN} = 1µF			3			*		mAp-p
Rated Output Voltage		±14.25	±15	±15.75	*	*	*	V
Output Current	Balanced Load		±15	±50		*	*	mA
Single			30	100		*	*	mA
Load Regulation	Balanced Load		0.3			*		%/mA
Line Regulation			1.12			*		V/V
Output Voltage vs Temperature			2.5			*		mV/°C
Voltage Balance Error, ±V_{CC1}			0.05			*		%
Voltage Ripple (800kHz)	No External Capacitors		50			*		mVp-p
C_{EXT} = 1µF			5			*		mVp-p
Output Capacitive Load				1			*	µF
Sync Frequency	TTL, 50% Duty Cycle	1.25	1.6	2	*	*	*	MHz
TEMPERATURE RANGE								
Specification		–25		+85	*		*	°C
Operating		–25		+85	*		*	°C
Storage		–25		+125	*		*	°C

NOTE: (1) Conforms to UL1244 test methods. 100% tested at 1500Vrms for 1 minute.

MECHANICAL

G Package — 24-Pin Ceramic DIP



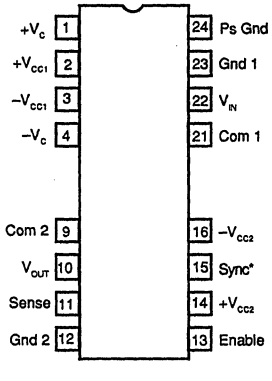
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.180	1.220	29.97	30.99
B	.580	.600	14.73	15.24
C	.310	.370	7.87	9.40
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.600	.620	15.24	15.75
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

ABSOLUTE MAXIMUM RATINGS

Supply Without Damage	±18V
V_{IN}, Sense Voltage	±50V
Com 1 to Gnd 1 or Com 2 to Gnd 2	±200mV
Enable, Sync	0V to $+V_{CC2}$
Continuous Isolation Voltage	1500Vrms
V_{ISO}, dv/dt	20kV/µs
Junction Temperature	150°C
Storage Temperature	–25°C to +125°C
Lead Temperature,10s	300°C
Output Short to Gnd 2 Duration	Continuous
$\pm V_{CC1}$ to Gnd 1 Duration	Continuous

PIN CONFIGURATION

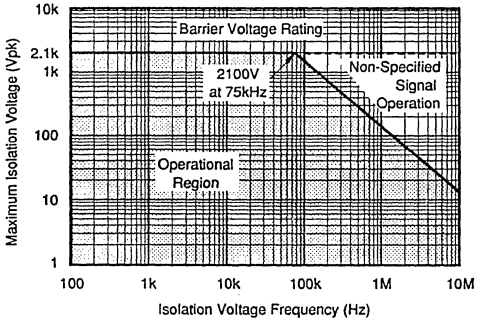


*Operation requires this pin be grounded or driven with TTL levels.

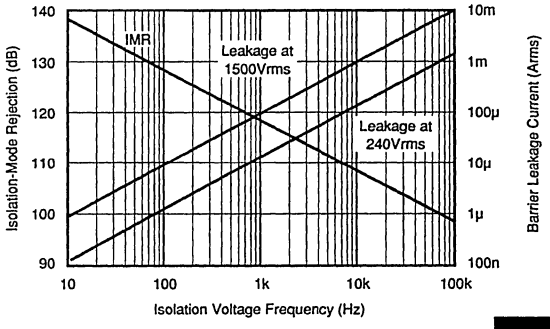
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC2} = ±15VDC, ±15mA output current unless otherwise noted.

RECOMMENDED RANGE OF ISOLATION VOLTAGE



IMR/LEAKAGE vs FREQUENCY



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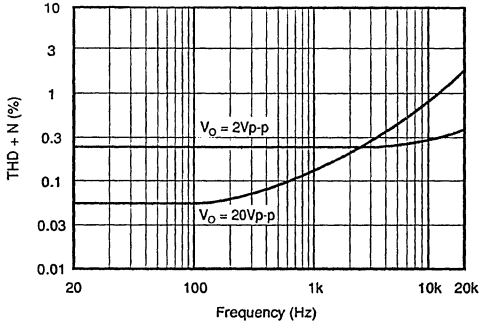
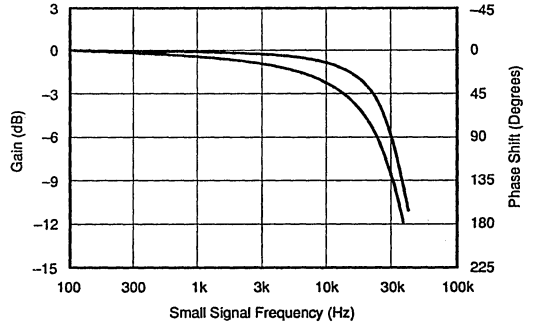
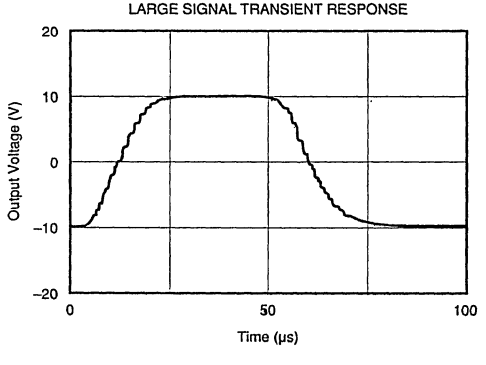
DISTORTION vs FREQUENCY



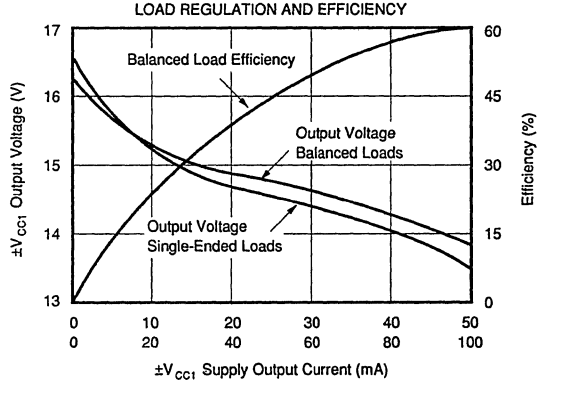
GAIN/PHASE vs FREQUENCY



LARGE SIGNAL TRANSIENT RESPONSE



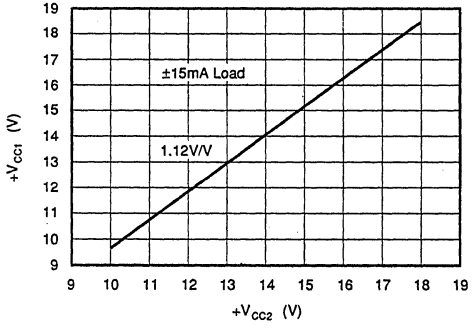
ISOLATED POWER SUPPLY
LOAD REGULATION AND EFFICIENCY



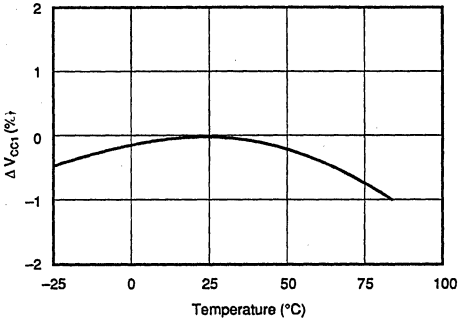
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC2} = ±15VDC, ±15mA output current unless otherwise noted.

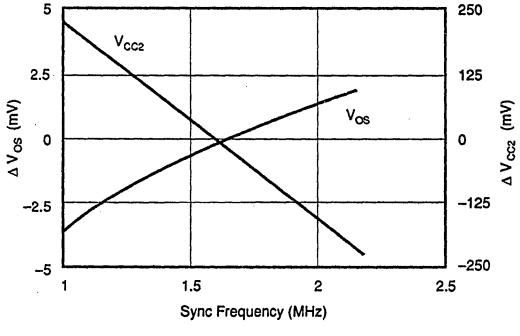
ISOLATED POWER SUPPLY LINE REGULATION



ISOLATION POWER SUPPLY VOLTAGE vs TEMPERATURE



ISOLATED SUPPLY VOLTAGE AND V_{OS} vs SYNC FREQUENCY



THEORY OF OPERATION

The block diagram on the front page shows the isolation amplifier's synchronized signal and power configuration, which eliminate beat frequency interference. A proprietary 800kHz oscillator chip, power MOSFET transformer drivers, patented square core wirebonded transformer, and single chip diode bridge provide power to the input side of the isolation amplifier as well as external loads. The signal channel capacitively couples a duty-cycle encoded signal across the ceramic high-voltage barrier built into the package. A proprietary transmitter-receiver pair of integrated circuits, laser trimmed at wafer level, and coupled through a pair of matched "fringe" capacitors, result in a simple, reliable design.

SIGNAL AND POWER CONNECTIONS

Figure 1 shows the proper power supply and signal connections. All power supply pins should be bypassed as shown with the π filter for $+V_{CC2}$, an option recommended if more than ±15mA are drawn from the isolated supply. Separate rectifier output pins ($\pm V_{CC1}$) and amplifier supply input pins ($\pm V_C$) allow additional ripple filtering and/or regulation. The separate input and output common pins and output sense are low current inputs tied to the signal source ground, output ground, and output load, respectively, to minimize errors due to IR drop in long conductors. Otherwise, connect Com 1 to Gnd 1, Com 2 to Gnd 2, and Sense to V_{OUT} at the ISO103 socket. The enable pin may be left open if the ISO103 is continuously operated. If not, a TTL low level will disable the internal DC/DC converter. The Sync input must be grounded for unsynchronized operation while a 1.25MHz to 2MHz TTL clock signal provides synchronization of multiple units.

OPTIONAL GAIN AND OFFSET ADJUSTMENTS

Rated gain accuracy and offset performance can be achieved with no external adjustments, but the circuit of Figure 2a may be used to provide a gain trim of ±0.5% for the values shown; greater range may be provided by increasing the size of R_1 and R_2. Every 2kΩ increase in R_1 will give an additional 1% adjustment range, with $R_2 \geq 2R_1$. If safety or convenience dictate location of the adjustment potentiometer on the other side of the barrier from the position shown in Figure 2a, the position of R_1 and R_2 may be reversed.

Gains greater than 1 may be obtained by using the circuit of Figure 2b. Note that the effect of input referred errors will be multiplied at the output in proportion to the increase in gain. Also, the small-signal bandwidth will be decreased in inverse proportion to the increase in gain. In most instances, a precision gain block at the input of the isolation amplifier will provide better overall performance.

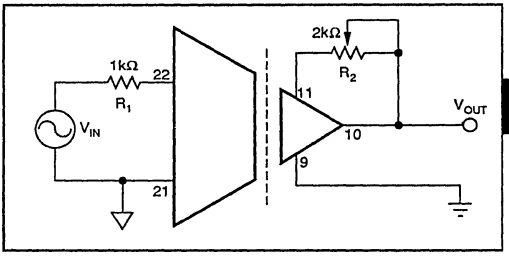


FIGURE 2a. Gain Adjust.

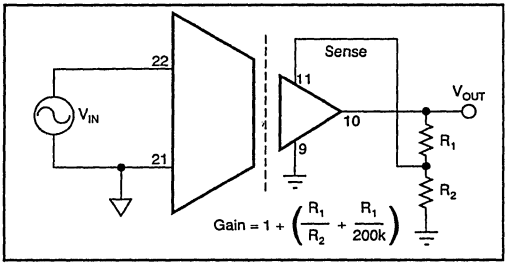


FIGURE 2b. Gain Setting.

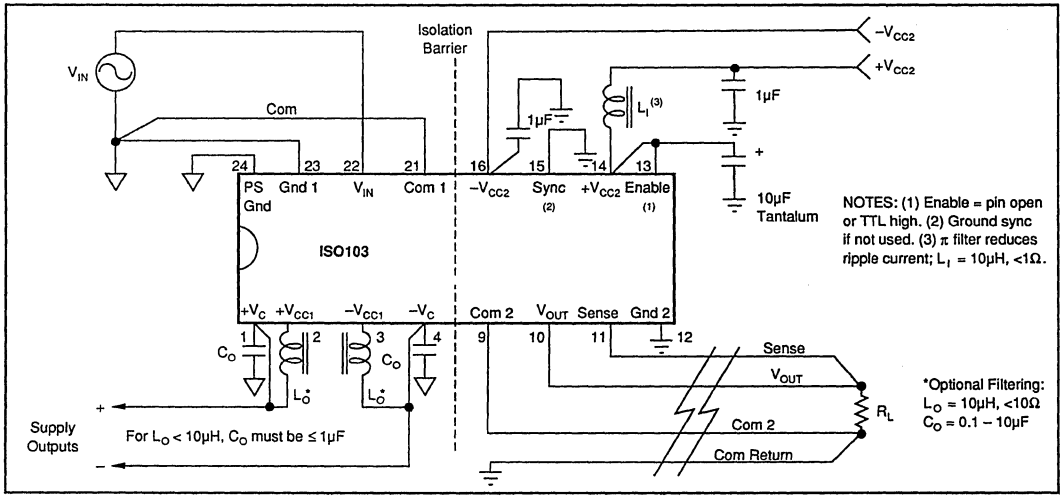


FIGURE 1. Signal and Power Connections.

Figure 3 shows a method for trimming V_{OS} of the ISO103. This circuit may be applied to either Signal Com (input or output) as desired for safety or convenience. With the values shown, ±15V supplies and unity gain, the circuit will provide ±150mV adjustment range and 0.25mV resolution with a typical trim potentiometer. The output will have some sensitivity to power supply variations. For a ±100mV trim, power supply sensitivity is 8mV/V at the output.

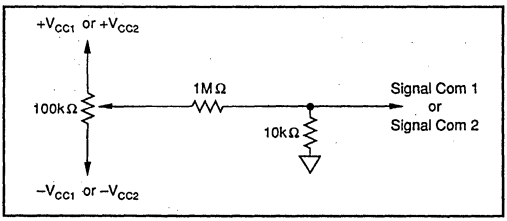


FIGURE 3. V_{OS} Adjust.

OPTIONAL OUTPUT FILTER

Figure 4 shows an optional output ripple filter that reduces the 800kHz ripple voltage to <5mVp-p without compromising DC performance. The small signal bandwidth is extended above 30kHz as a result of this compensation.

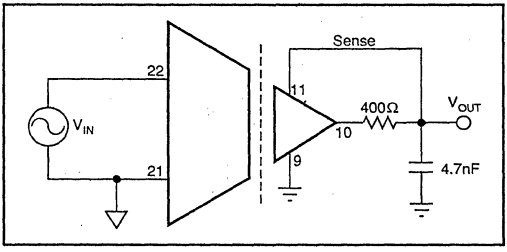


FIGURE 4. Ripple Reduction.

MULTICHANNEL SYNCHRONIZATION

Synchronization of multiple ISO103s can be accomplished by connecting pin 15 of each device to an external TTL level oscillator, as shown in Figure 7. The PWS750-1 oscillator is convenient because its nominal synchronizing output frequency is 1.6MHz, resulting in a 800kHz carrier in the ISO103 (its nominal unsynchronized value). The open collector output typically switches 7.5mA to a 0.2V low level so that the external pull-up resistor can be chosen for different pull-up voltages as shown in Figure 7. The number of channels synchronized by one PWS750-1 is determined by the total capacitance of the sync voltage conductors. They must be less than 1000pF to ensure TTL level switching at 800kHz. At higher frequencies the capacitance must be proportionally lower.

Customers can supply their own TTL level synchronization logic provided the frequency is between 1.25MHz and 2MHz, and the duty cycle is greater than 25%.

Multichannel synchronization with reduced power dissipation for applications requiring less than ±15mA from V_{CC1} is accomplished by driving both the Sync input pin (15) and Enable pin (13) with the TTL oscillator as shown in Figure 5.

ISOLATION BARRIER VOLTAGE

The typical performance of the ISO103 under conditions of barrier voltage stress is indicated in the first two performance curves—Recommended Range of Isolation Voltage and IMR/ Leakage vs Frequency. At low barrier modulation levels, errors can be determined by the IMRR characteristic. At higher barrier voltages, typical performance is obtained as long as the dv/dt across the barrier is below the shaded area in the first curve. Otherwise, the signal channel will be interrupted, causing the output to distort, and/or shift DC level. This condition is temporary, with normal operation resuming as soon as the transient subsides. Permanent damage to the integrated circuits occurs only if transients exceed 20kV/µs. Even in this extreme case, the barrier integrity is assured.

HIGH VOLTAGE TESTING

The ISO103 was designed to reliably operate with 1500Vrms continuous isolation barrier voltage. To confirm barrier integrity, a two-step breakdown test is performed on 100% of the units. First, a 5600V peak, 60Hz barrier potential is applied for 10s to verify that the dielectric strength of the insulation is above this level. Following this exposure, a 1500Vrms, 60Hz potential is applied for one minute to conform to UL1244. Life-test results show reliable operation under continuous rated voltage and maximum operating temperature conditions.

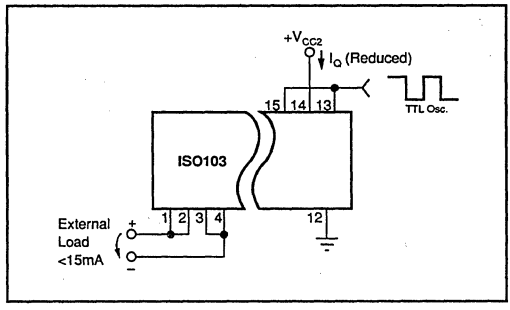


FIGURE 5. Reduced Power Dissipation.

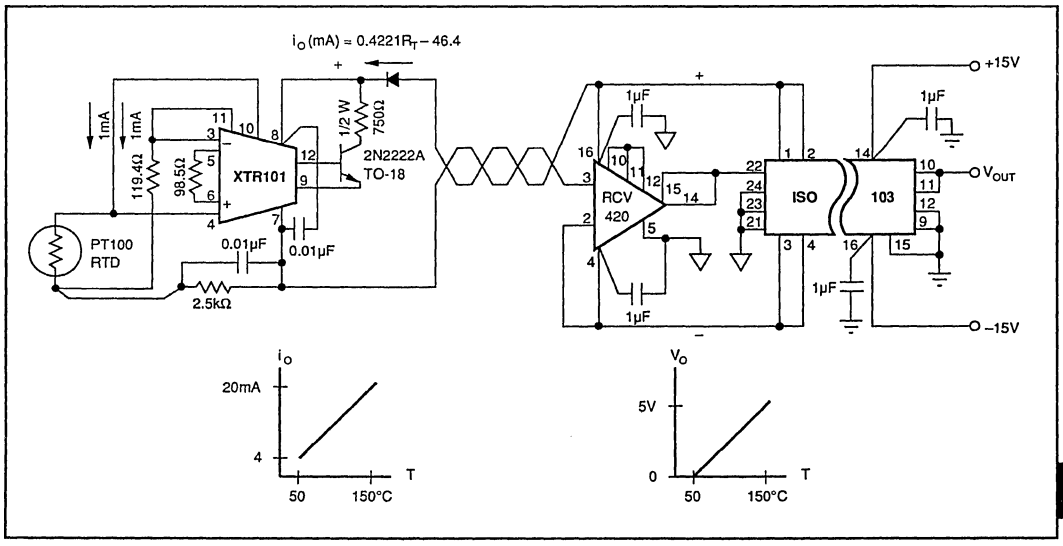


FIGURE 6. Isolated 4-20mA Instrument Loop.

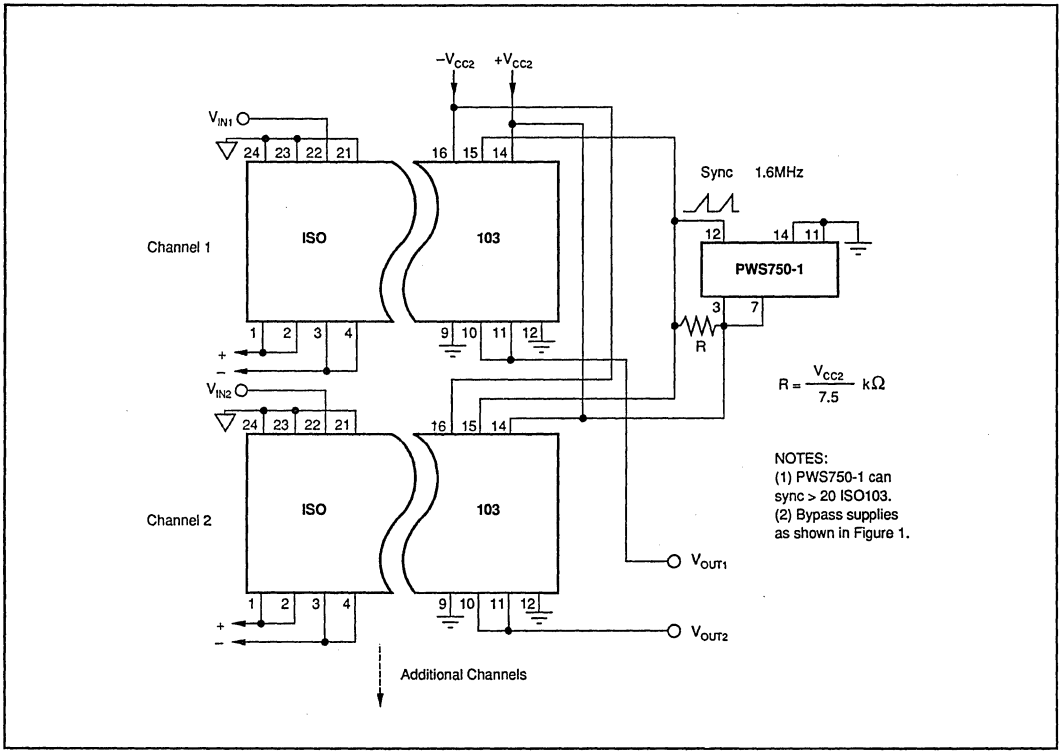
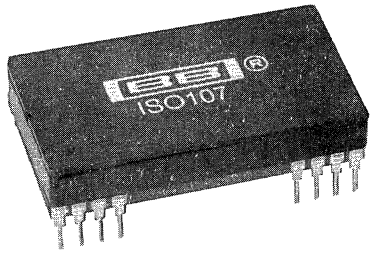


FIGURE 7. Synchronized-Multichannel Isolation.

BURR-BROWN®



ISO107

High-Voltage, Internally Powered ISOLATION AMPLIFIER

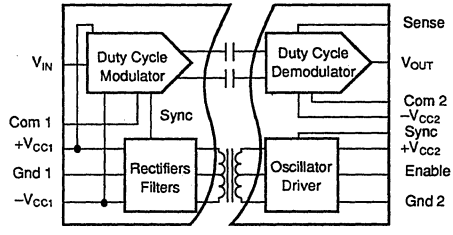
FEATURES

- SIGNAL AND POWER IN ONE TRIPLE-WIDE PACKAGE
- 8000Vpk TEST VOLTAGE
- 2500Vrms CONTINUOUS AC BARRIER RATING
- WIDE INPUT SIGNAL RANGE: –10V to +10V
- WIDE BANDWIDTH: 20kHz Small Signal, 20kHz Full Power
- BUILT-IN ISOLATED POWER: ±10V to ±18V Input, ±50mA Output
- MULTICHANNEL SYNCHRONIZATION CAPABILITY (TTL)

APPLICATIONS

- MULTICHANNEL ISOLATED DATA ACQUISITION
- BIOMEDICAL INSTRUMENTATION
- POWER SUPPLY AND MOTOR CONTROL
- GROUND LOOP ELIMINATION

ISO107 BLOCK DIAGRAM



DESCRIPTION

The ISO107 isolation amplifier provides both signal and power across an isolation barrier. The ceramic side-brazed hybrid package contains a transformer-coupled DC/DC converter and a capacitor-coupled signal channel.

Extra power is available on the isolated input side for external input conditioning circuitry. The converter is protected from shorts to ground with an internal current limit, and the soft-start feature limits the initial currents from the power source. Multiple-channel synchronization can be accomplished by applying a TTL clock signal to paralleled Sync pins. The Enable control is used to turn off transformer drive while keeping the signal channel demodulator active. This feature provides a convenient way to reduce quiescent current for low power applications.

The wide barrier pin spacing and internal insulation allow for the generous 2500Vrms continuous rating. Reliability is assured by 100% barrier breakdown testing that conforms to UL544 test methods. Low barrier capacitance minimizes AC leakage currents.

These specifications and built-in features make the ISO107 easy to use, as well as providing for compact PC board layouts.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-898B

SPECIFICATIONS

ELECTRICAL

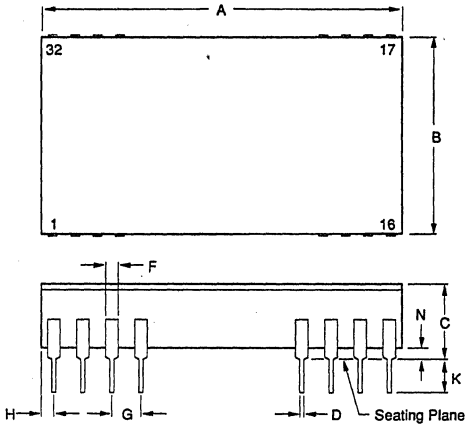
T_A = +25°C and V_{CC2} = ±15V, ±15mA output current unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
ISOLATION					
Rated Continuous Voltage [1]					
AC, 60Hz	T_{MIN} to T_{MAX}	2500			Vrms
DC	T_{MIN} to T_{MAX}	3500			VDC
Test Breakdown, AC, 60Hz	10s	8000			Vpk
Isolation-Mode Rejection	2500Vrms, 60Hz		100		dB
	2121VDC		160		dB
Barrier Impedance			10^{12} || 13		Ω || pF
Leakage Current	240Vrms, 60Hz		1.2	2	µA
GAIN					
Nominal			1		V/V
Initial Error			±0.1	±0.25	% FSR
Gain vs Temperature			±50	±120	ppm/°C
Nonlinearity			±0.01	±0.025	% FSR
INPUT OFFSET VOLTAGE					
Initial Offset			±20	±50	mV
vs Temperature			±150	±400	µV/°C
vs Power Supplies	V_{CC2} = ±10V to ±18V		±2		mV/V
INPUT					
Voltage Range	Output Voltage in Range	±10	±15		V
Resistance			200		kΩ
SIGNAL OUTPUT					
Voltage Range		±10	±12.5		V
Current Drive		±5	±20		mA
Ripple Voltage, 800kHz Carrier (See Figure 4)			20		mVp-p
Capacitive Load Drive			1000		pF
Voltage Noise			4		µV/√Hz
FREQUENCY RESPONSE					
Small Signal Bandwidth			20		kHz
Slew Rate			1.5		V/µs
Settling Time	0.1%, –10/10V		75		µs
POWER SUPPLIES					
Rated Voltage, V_{CC2}			±15		V
Voltage Range		±10		±18	V
Input Current	I_O = ±15mA		+75/–4.5		mA
Ripple Current	No Filter		10		mAp-p
	C_{IN} = 1µF		3		mAp-p
Rated Output Voltage		±14.25	±15	±15.75	V
Output Current	Balanced Load		±15	±50	mA
	Single		30	100	mA
Load Regulation	Balanced Load		0.5		%/mA
Line Regulation			1.18		V/V
Output Voltage vs Temperature			10		mV/°C
Voltage Balance Error, $\pm V_{CC1}$			0.05		%
Voltage Ripple	No External Capacitors		10		mVp-p
Output Capacitive Load (See Figure 1)				1	µF
Sync Frequency	TTL, 50% Duty Cycle	1.25	1.6	2	MHz
TEMPERATURE RANGE					
Specification		–25		+85	°C
Operating		–25		+85	°C
Storage		–25		+125	°C

NOTES: (1) Conforms to UL544 test methods. 100% tested at 2500Vrms for 1 minute.

MECHANICAL

P Package — 32-Pin Plastic DIP



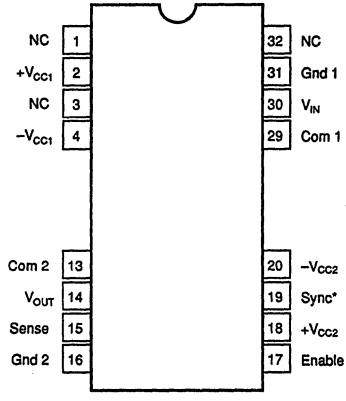
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.580	1.620	40.13	41.15
B	.880	.900	22.35	22.86
C	.310	.370	7.87	9.40
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.125	.180	3.18	4.57
L	.900	.920	22.86	23.37
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

ABSOLUTE MAXIMUM RATINGS

Supply Without Damage	±18V
V_{IN}, Sense Voltage	±50V
Com 1 to Gnd 1 or Com 2 to Gnd 2	±200mV
Enable, Sync	0V to $+V_{CC2}$
Continuous Isolation Voltage	2500Vrms
V_{ISO}, dv/dt	20kV/µs
Junction Temperature	150°C
Storage Temperature	–25°C to +125°C
Lead Temperature, 10s	300°C
Output Short to Gnd 2 Duration	Continuous
$\pm V_{CC1}$ to Gnd 1 Duration	Continuous

PIN CONFIGURATION



*Operation requires that this pin be grounded or driven with TTL levels.

TYPICAL PERFORMANCE CURVES

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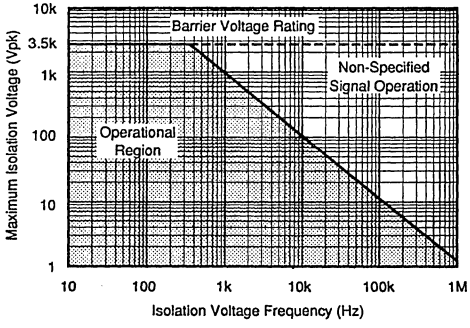
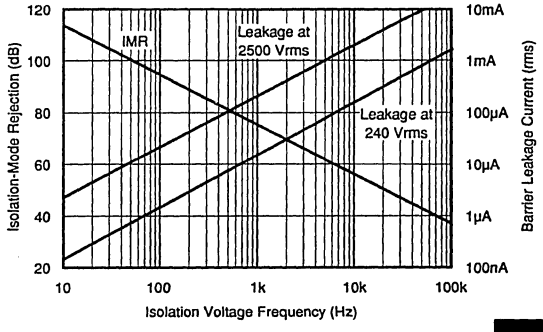
RECOMMENDED RANGE OF ISOLATION VOLTAGE

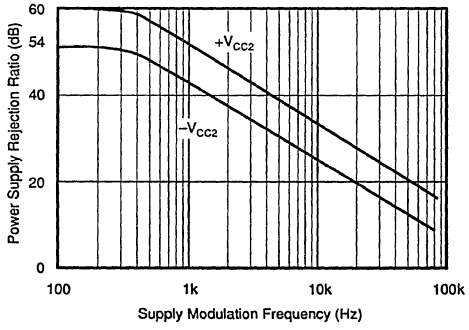


IMR/LEAKAGE vs FREQUENCY

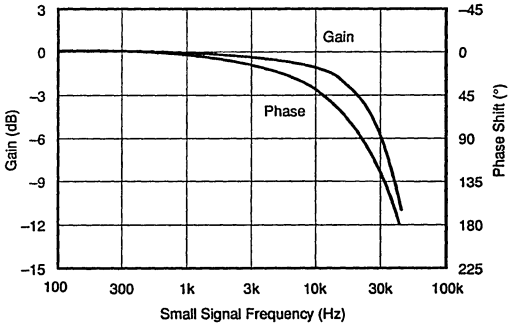


4

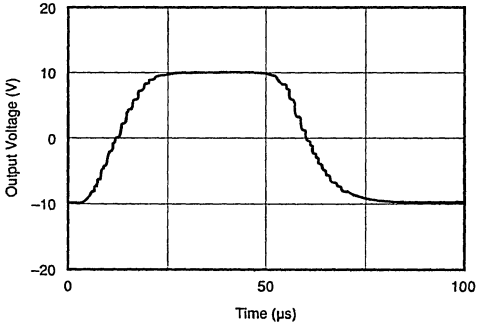
PSRR vs FREQUENCY



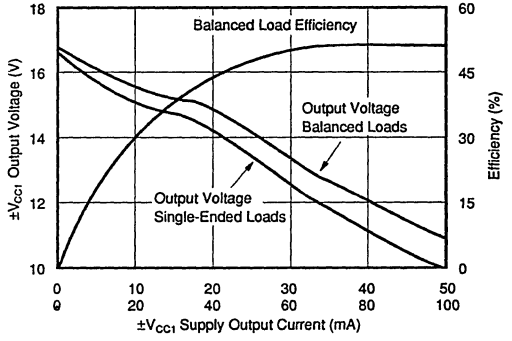
GAIN/PHASE vs FREQUENCY



LARGE SIGNAL TRANSIENT RESPONSE



ISOLATED POWER SUPPLY
LOAD REGULATION AND EFFICIENCY



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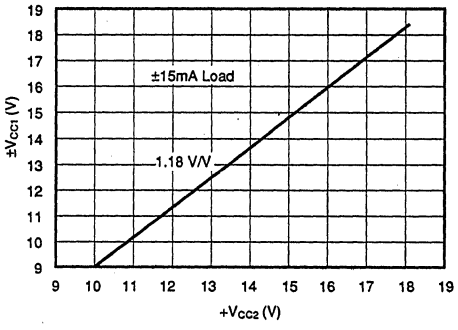
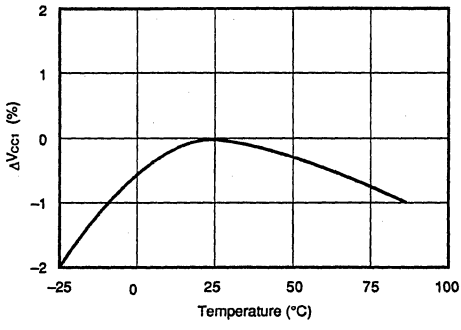


ISOLATED POWER SUPPLY VOLTAGE vs TEMPERATURE



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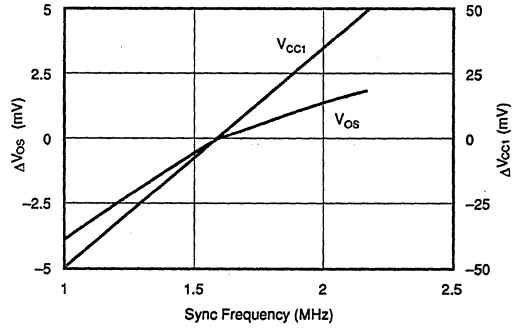

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Gains greater than 1 may be obtained by using the circuit of Figure 2b. Note that the effect of input offset errors will be multiplied at the output in proportion to the increase in gain. Also, the small-signal bandwidth will be decreased in in-

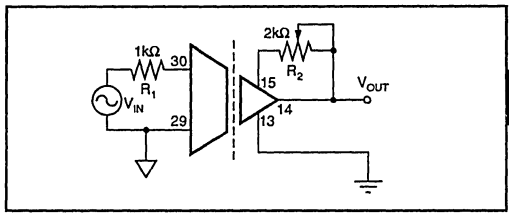


FIGURE 2a. Gain Adjust.

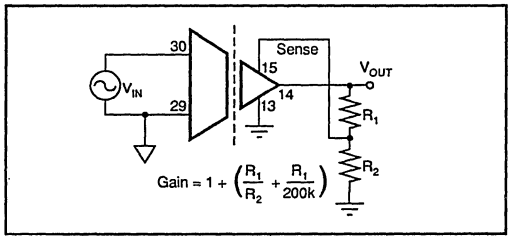


FIGURE 2b. Gain Setting.

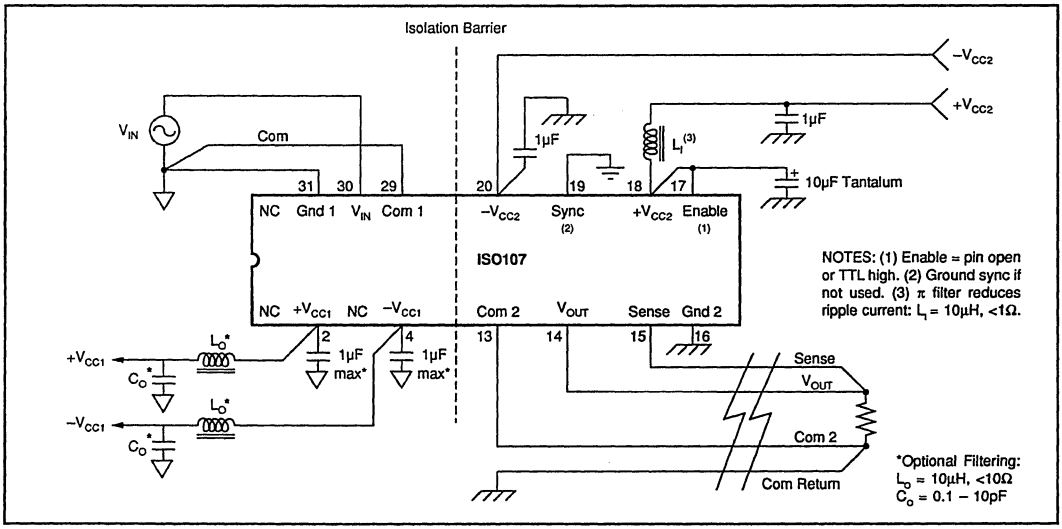


FIGURE 1. Signal and Power Connections.

verse proportion to the increase in gain. In most instances, a precision gain block at the input of the isolation amplifier will provide better overall performance.

Figure 3 shows a method for trimming V_{OS} of the ISO107. This circuit may be applied to either Signal Com (input or output) as desired for safety or convenience. With the values shown, ±15V supplies and unity gain, the circuit will provide ±150mV adjustment range and 0.25mV resolution with a typical trim potentiometer. The output will have some sensitivity to power supply variations. For a ±100mV trim, power supply sensitivity is 8mV/V at the output.

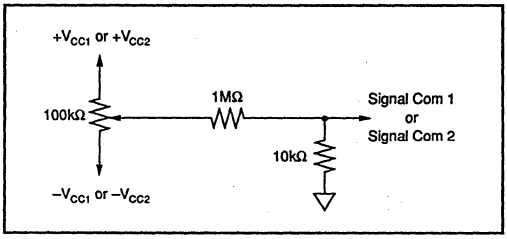


FIGURE 3. V_{OS} Adjust.

OPTIONAL OUTPUT FILTER

Figure 4 shows an optional output ripple filter that reduces the 800kHz ripple voltage to <3mVp-p without compromising DC performance. The small signal bandwidth is extended above 30kHz as a result of this compensation.

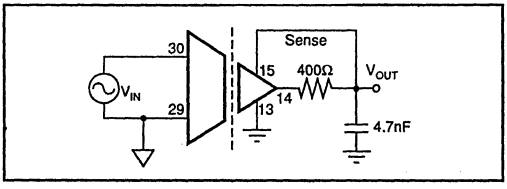


FIGURE 4. Ripple Reduction.

MULTICHANNEL SYNCHRONIZATION

Synchronization of multiple ISO107s can be accomplished by connecting pin 19 of each device to an external TTL level oscillator, as shown in Figure 6. The PWS750-1 oscillator is convenient because its nominal synchronizing output frequency is 1.6MHz, resulting in a 800kHz carrier in the ISO107 (its nominal unsynchronized value). The open collector output typically switches 7.5mA to a 0.2V low level so that the external pull-up resistor can be chosen for different pull-up voltages as shown in Figure 6. The number of channels synchronized by one PWS750-1 is determined by the total capacitance of the sync voltage conductors. They must be less than 1000pF to ensure TTL level switching at 800kHz. At higher frequencies the capacitance must be proportionally lower.

Customers can supply their own TTL level synchronization logic, provided the frequency is between 1.25MHz and 2MHz, and the duty cycle is greater than 25%.

ISOLATION BARRIER VOLTAGE

The typical performance of the ISO107 under conditions of barrier voltage stress is indicated in the first two performance curves—Recommended Range of Isolation Voltage and IMR/Leakage vs Frequency. At low barrier modulation levels, errors can be determined by the IMRR characteristic. At higher barrier voltages, typical performance is obtained as long as the dv/dt across the barrier is below the shaded area in the first curve. Otherwise, the signal channel will be interrupted, causing the output to distort, and/or shift DC level. This condition is temporary, with normal operation resuming as soon as the transient subsides. Permanent damage to the integrated circuits occurs only if transients exceed 20kV/µs. Even in this extreme case, the barrier integrity is assured.

HIGH VOLTAGE TESTING

The ISO107 was designed to reliably operate with 2500Vrms continuous isolation barrier voltage. To confirm barrier integrity, a two-step breakdown test is performed on 100% of the units. First, an 8000V peak, 60Hz barrier potential is applied for 10s to verify that the dielectric strength of the insulation is above this level. Following this exposure, a 2500Vrms, 60Hz potential is applied for one minute to conform to UL544. Life-test results show reliable operation under continuous rated voltage and maximum operating temperature conditions.

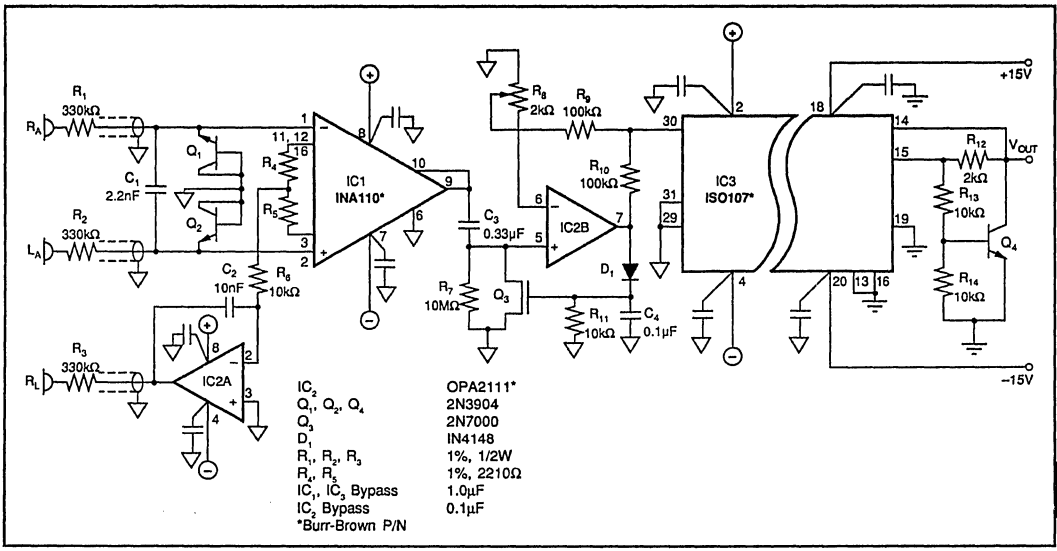


FIGURE 5. ECG Amplifier with Right Leg Drive, Defibrillator Protection, and E.S.U. Blanking.

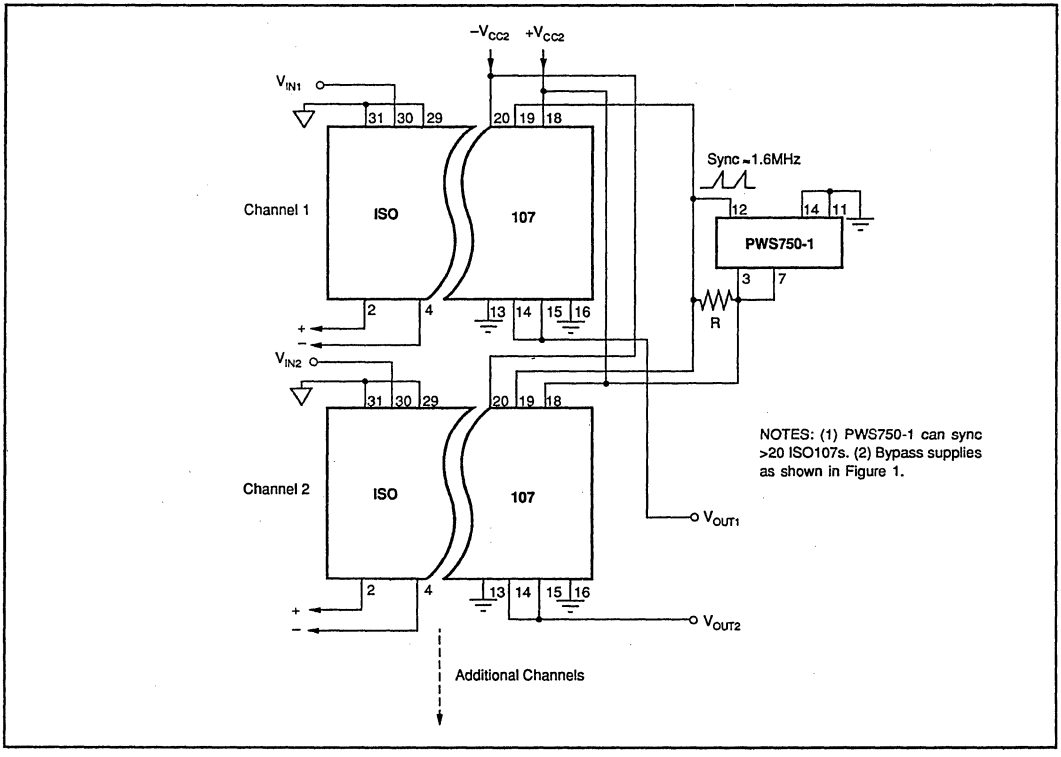
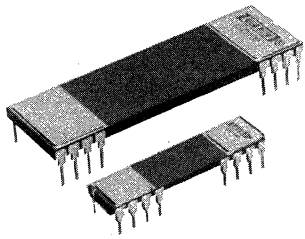


FIGURE 6. Synchronized-Multichannel Isolation.

BURR-BROWN®



ISO108
ISO109

Isolated
VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

- ISOLATED VFC IN HERMETIC DIP
- HIGH-VOLTAGE AC RATING:
  ISO108: 1500Vrms
  ISO109: 3500Vrms
- HIGH TRANSIENT IMMUNITY: 10kV/μs
- LOW BARRIER LEAKAGE CURRENT: 0.5μA
- TRUE INPUT INTEGRATING (NOISE REDUCTION)
- HIGH LINEARITY AT HIGH FREQUENCY: 0.01% at 1MHz
- LOW JITTER AT HIGH FREQUENCY: 200ppm (rms) at 1MHz
- VOLTAGE REFERENCE OUTPUT: 5VDC
- MULTIPLEXED OUTPUT CAPABILITY

APPLICATIONS

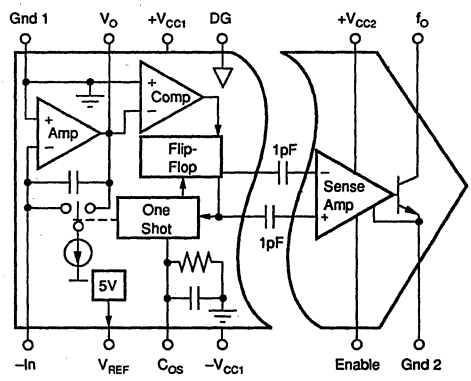
- ISOLATED A/D CONVERTER
- BIOMEDICAL DATA ACQUISITION
- PROCESS CONTROL
- INDUSTRIAL DATA ACQUISITION

DESCRIPTION

The ISO108 and ISO109 provide a high-speed VFC and isolated coupler in a hermetic DIP package. This represents a new function for diverse applications requiring both A/D conversion and galvanic isolation.

The input VFC transmits a differential digital signal across the isolation barrier through matched 1pF ceramic capacitors built into the 24-pin single-wide (ISO108) and 40-pin double-wide (ISO109) packages. Excellent transient immunity is provided by the barrier capacitor matching, patented sense amp design, and laser trimming.

Extra features include a voltage reference useful for offsetting and calibration, and a TTL-compatible enable input that provides for multiplexing multiple VFC outputs.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-841A

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC1}$ = ±15V, V_{CC2} = 5V unless otherwise noted.

PARAMETER	CONDITIONS	ISO108, 109 MIN	ISO108, 109 TYP	ISO108, 109 MAX	UNITS
ISOLATION					
Rated Continuous Voltage					
ISO108: AC, 60Hz	T_{MIN} to T_{MAX}	1500			Vrms
DC	T_{MIN} to T_{MAX}	2121			VDC
ISO109: AC, 60Hz	T_{MIN} to T_{MAX}	3500			Vrms
DC	T_{MIN} to T_{MAX}	4950			VDC
Partial Discharge Test[1]					
ISO108	2500Vrms			5	pC
ISO109	5600Vrms			5	pC
Transient Immunity w/o Signal Loss			10		kV/µs
Barrier Impedance			10^2 || 3		Ω || pF
Leakage Current, 60Hz	240Vrms		0.3	0.5	µA
Isolation Mode Rejection, 60Hz	2500Vrms		130		dB
TRANSFER FUNCTION					
Voltage-to-Frequency Mode	[2]				
Gain Error	FSR = 1MHz			5	%
Linearity Error	FSR = 1MHz		0.01	0.025	%
Gain Drift	FSR = 1MHz			100	ppm/°C
PSRR	V_{CC1} = ±8V to ±18V			0.1	%/V
Input Current Range[3]	0-FS Output	0		250	µA
INTEGRATOR OP AMP					
V_{OS}				3	mV
V_{OS} Drift			35	100	µV/°C
I_B			20	100	nA
V_{OUT} Range	R_L = 2kΩ	–0.2		$+V_{CC1} - 4$	V
Output Current Limit			20		mA
OPEN COLLECTOR OUTPUT					
V_{OL}	I_{OUT} = 10mA		0.25	0.4	V
I_{OH}	V_{OH} = 20V		0.1	1	µA
Fall Time	R_L = 470Ω, C_L = 500pF		50		ns
REFERENCE VOLTAGE					
Accuracy		4.97	5	5.03	V
Drift				50	ppm/°C
Output Current Limit		10	20	30	mA
PSRR	V_{CC1} = ±8V to ±18V		0.5		mV/V
Output Impedance	I_O = 0 to 10mA		0.4	1	Ω
POWER SUPPLY					
Voltage Range	$\pm V_{CC1}$	±8	±15	±18	V
	$+V_{CC2}$	4.5	5	20	V
Quiescent Current	$+V_{CC1}$ / $-V_{CC1}$		+14/–14	+17/–17	mA
	$+V_{CC2}$		+11	+17	mA
TEMPERATURE RANGE					
Specification		–25		+85	°C
Operating		–55		+125	°C
Storage		–55		+150	°C

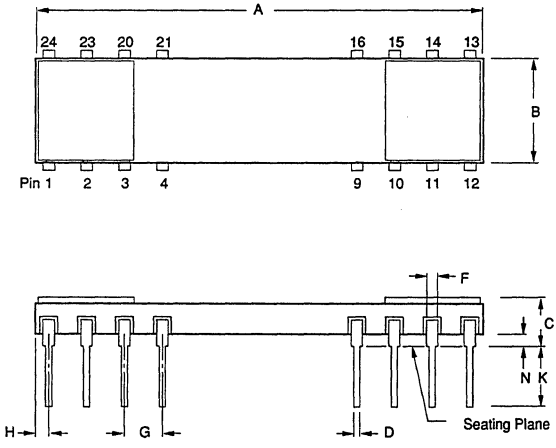
NOTES: (1) Conforms to VDE884 test methods. Tested at 1.6 x rated voltage: PD ≤ 5pC. (2) R_{IN} = 40kΩ, C_{OS} = 150pF. (3) $V_{IN} = I_{IN} \times R_{IN}$.

ABSOLUTE MAXIMUM RATINGS

Supply Without Damage	±20V
–In, C_{OS}	$\pm V_{CC1}$
Enable	Gnd 2/V_{CC2}
V_{REF}, V_O to Gnd 1	Continous
f_O Sink Current	50mA
Continuous Isolation Voltage:	
ISO108	1500Vrms
ISO109	3500Vrms
Barrier Transient, dV/dt	20kV/µs
Junction Temperature	+150°C
Storage Temperature	
ISO108, 109	–55°C to +150°C
Lead Temperature, 10s	+300°C

MECHANICAL

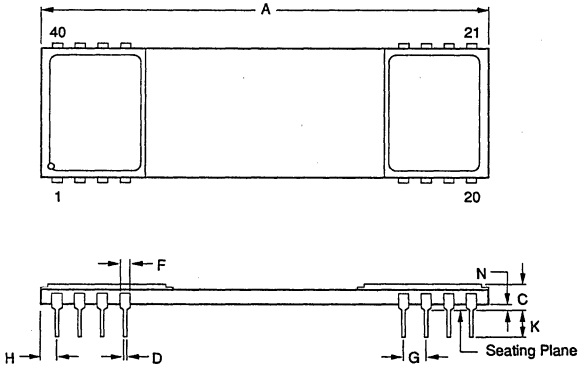
ISO108 — 24-Pin Single-Wide Hermetic Dip



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.190	1.210	30.23	30.73
B	.280	.300	7.11	7.62
C	.140	.185	3.56	4.70
D	.016	.020	0.41	0.51
F	.030	.050	0.76	1.27
G	.100 BASIC		2.54 BASIC	
H	.035	.065	0.89	1.65
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.300 BASIC		7.62 BASIC	
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

ISO109 — 40-Pin Double-Wide Hermetic DIP

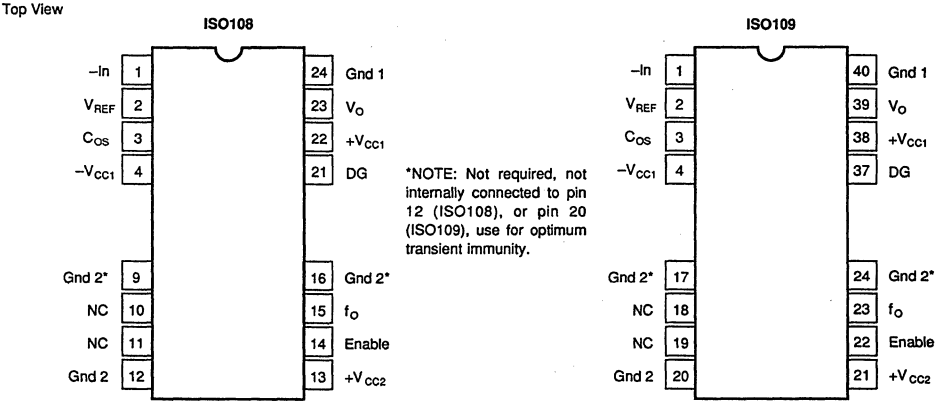


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.980	2.020	50.29	51.31
C	.115	.175	2.92	4.45
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

PIN CONFIGURATION

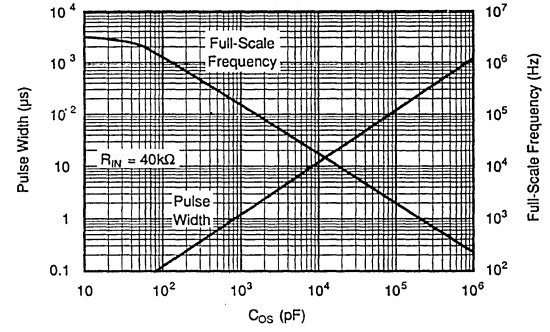
Top View



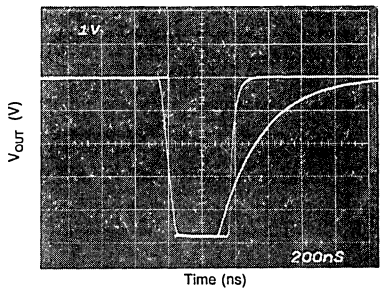
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

OUTPUT PULSE WIDTH AND FULL-SCALE FREQUENCY vs EXTERNAL ONE-SHOT CAPACITANCE

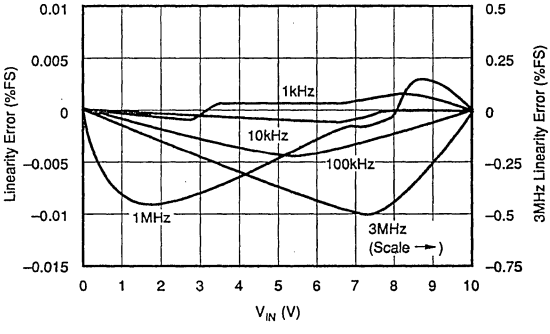


OUTPUT RESPONSE vs CAPACITIVE LOAD

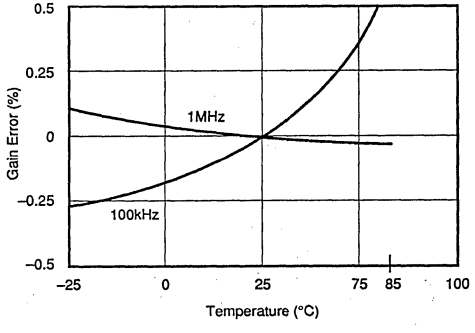


4

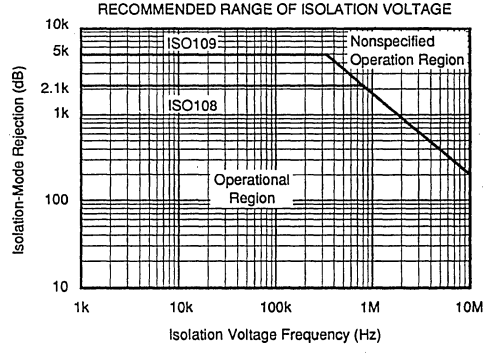
LINEARITY vs INPUT



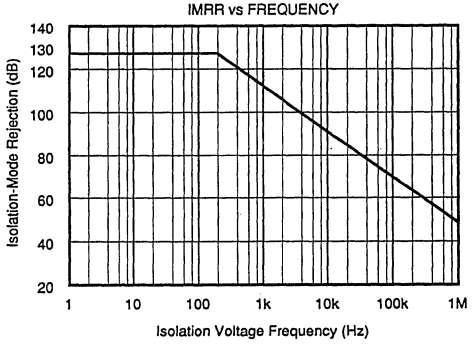
GAIN ERROR vs TEMPERATURE



RECOMMENDED RANGE OF ISOLATION VOLTAGE

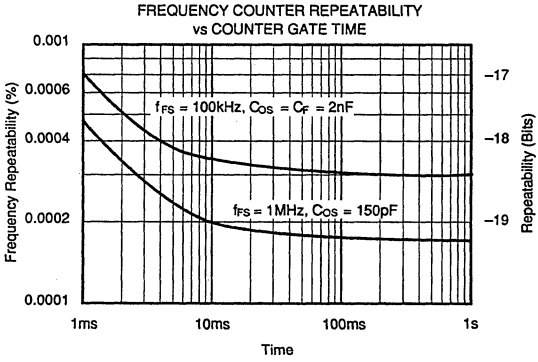


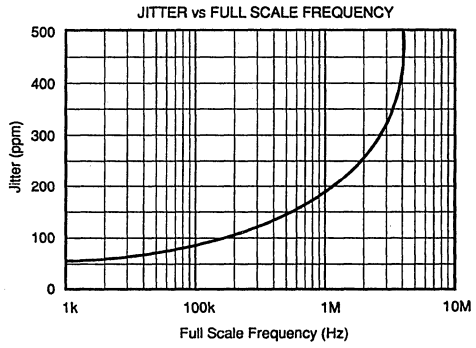
IMRR vs FREQUENCY



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.





THEORY OF OPERATION

A CHARGE BALANCE CONVERTER

The ISO108/109 uses a charge-balance technique to achieve high accuracy. The heart of this technique is an analog integrator formed by an operation amplifier, feedback capacitor, and input resistor. The integrator's output voltage is proportional to the charge stored in the capacitor. An input voltage develops an input current of V_{IN}/R_{IN}, which is forced to flow through the integrator capacitor. This current causes the integrator output voltage to ramp negatively.

When the output of the integrator ramps to 0V, the comparator trips, triggering the one-shot. This connects the reference current to the integrator input during the one-shot period, T_{OS}. This switched current causes the integrator output to ramp positively until the one-shot period ends. Then the cycle starts again.

The oscillation is regulated by the balance of the current (or charge) between the input current and the time-averaged reset current. The equation of current balance is:

$$I_{IN} = I_{REF} \cdot \text{Duty Cycle}$$

$$V_{IN}/R_{IN} = I_{REF} \cdot f_{OUT} \cdot T_{OS},$$

where T_{OS} is the one-shot period and f_{OUT} is the oscillation frequency.

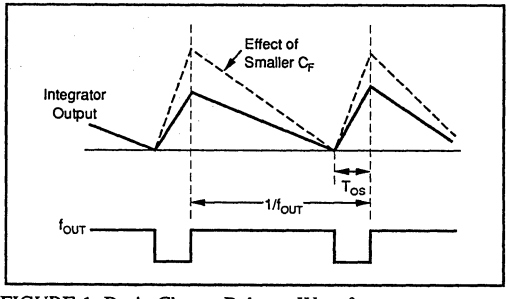


FIGURE 1. Basic Charge-Balance Waveforms.

CONNECTIONS AND BASIC OPERATION

External connections to the ISO108 and ISO109 are made as shown in Figure 2. The transfer function of the VFC is f_O [MHz] = (200pF)(40k)/(C_{OS} + 50pF)(R_{IN}). For a 10V full scale input, R_{IN} = 40kΩ for optimum performance; adjustment of C_{OS} then determines full-scale frequency as shown in performance curve Output Pulse Width and Full-Scale Frequency vs External One-Shot Capacitance. The fullscale frequency is typically 3MHz with C_{OS} =0pF.

Selection of the external resistor and capacitor type is important. Temperature drift of an external input resistor and one-shot capacitor will affect temperature stability of the output frequency. NPO ceramic capacitors will normally produce the best results. Silver-mica types will result in slightly higher drift, but may be adequate in many applications. A low-temperature coefficient film resistor should be used for R_{IN}.

The integrator capacitor serves as a "charge bucket," where charge is accumulated from the input, V_{IN}, and that charge is drained during the one-shot period. While the size of the bucket (capacitor value) is not critical, it must not leak. Capacitor leakage or dielectric absorption can affect the linearity and offset of the transfer function. High-quality ceramic capacitors can be used for values less than 0.01µF. Use caution with higher value ceramic capacitors. High-K ceramic capacitors may have voltage nonlinearities than can degrade overall linearity. Polystyrene, polycarbonate, or mylar film capacitors are superior for high values. External integrator capacitor C_F determines the integrator output voltage swing. It is recommended only for full-scale frequencies of 100kHz and below; in these cases, use $C_F = C_{OS}$. Decreasing the value of C_F will increase the peak-to-peak output swing, decrease jitter, but also decrease overrange capability.

The value of R_L depends on the pull-up voltage, output capacitance, and full scale frequency. The maximum output current is 10mA to assure a 0.4V maximum logic Low. Therefore, choosing R_L for 10mA output current results in the lowest rise-time for a given capacitive load. If a low full-scale frequency is used, a larger pull-up resistor will reduce

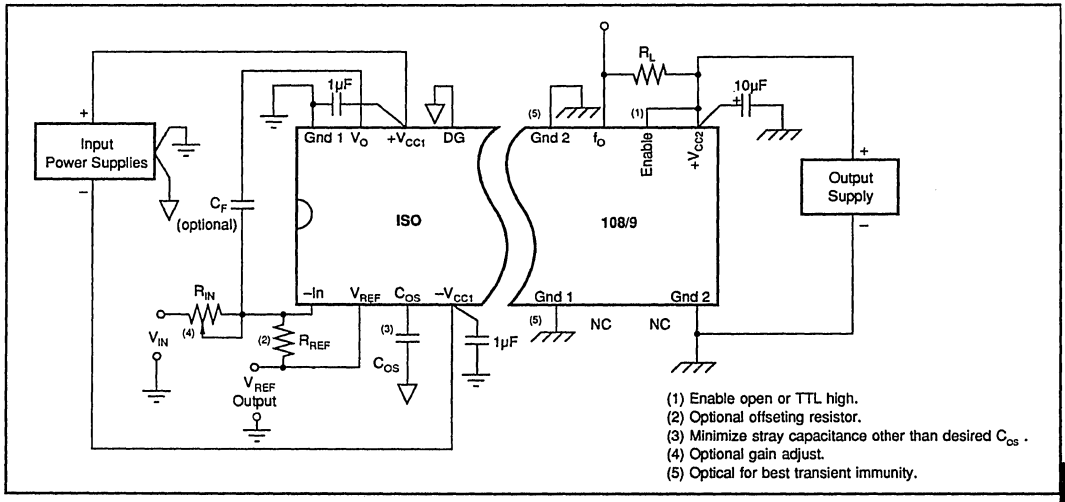


FIGURE 2. ISO108/109 Connection Diagram.

power dissipation without sacrificing performance. The effect of load capacitance (C_L) is shown in performance curve Output Response vs Capacitive Loads.

ENABLE PIN

The Enable pin can be left open or tied to a TTL high level for continuous output. A TTL low level applied to this pin will turn off the open collector output device. This feature allows multiple outputs to be tied together for one multiplexed output line. Individual ISOVFCs are selected one at a time with the Enable control. A multichannel ISOVFC system is shown in Figure 3. The 7442 BCD to 10 output decoder selects the active channel output. This is more accurate and convenient than switching sensitive input lines.

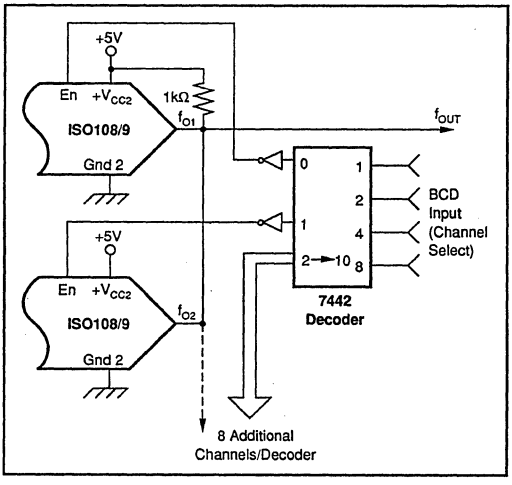


FIGURE 3. Multichannel Isolated Data Acquisition with Single Serial Output.

REFERENCE VOLTAGE

Figure 2, Note (2) shows a use of the reference voltage output to offset the input of the ISOVFC so that bipolar inputs can be accepted. Buried zener reference circuitry is used for low noise and excellent temperature drift. Output current is specified to 10mA and current-limited to approximately 20mA. Excessive or variable loads on V_{REF} can decrease frequency stability due to internal heating. Low level input signals should be amplified before the ISOVFC.

MEASURING OUTPUT FREQUENCY

To complete an integrating A/D conversion, the output frequency of the ISO108 and ISO109 must be counted. Simple frequency counting is accomplished by counting output pulses for a reference time (usually derived from a crystal oscillator). This can be implemented with counter/timer peripheral chips available for many popular microprocessor families. Many micro-controllers have counter inputs that can be programmed for frequency measurement.

Since f_{OUT} is an open-collector device, the negative-going edge provides the fastest logic transition. Clocking the counter on the falling edge will provide the best results in noisy environments. Alternately, a Schmidt trigger may be used on the rising edge.

Frequency can also be measured by accurately timing the period of one or more cycles of the VFC's output. Frequency must then be computed since it is inversely proportional to the measured period. This measurement technique can provide higher measurement resolution in short conversion times. It is the method used in most high-performance laboratory frequency counters. It is usually necessary to offset the transfer function so 0V input causes a finite frequency out. Otherwise the output period (and therefore the conversion time) approaches infinity. See Figure 4 and application note AN-130 for further details on counting techniques.

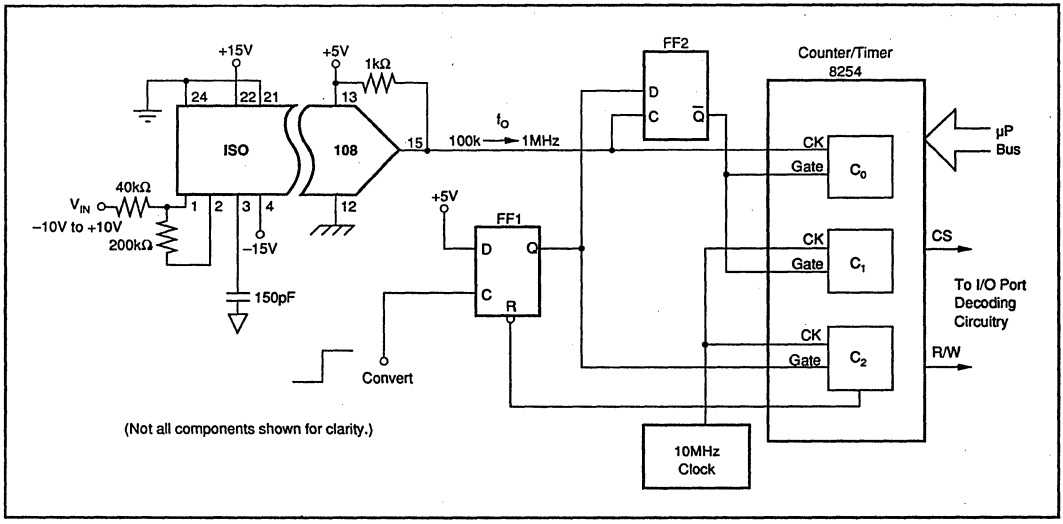


FIGURE 4. Isolated A/D Conversion System Using Ratiometric Counting and Microprocessor Interface.

FREQUENCY NOISE

Frequency noise (small random variation in the output frequency or "jitter") limits the useful resolution of fast frequency measurement techniques. Long measurement time averages the effect of frequency noise and achieves the maximum useful resolution. The ISO108 and ISO109 are designed to minimize frequency noise and allow improved useful resolution with short measurement times. The performance curve Frequency Count Repeatability vs Counter Gate Time shows the effect of noise as the counter gate time is varied. It shows the one standard deviation (1σ) count variation (as a percentage of FS counts) versus counter gate time.

ISOLATION BARRIER VOLTAGE

The performance of the ISO108 and ISO109 under conditions of isolation barrier voltage modulation is indicated in performance curve IMRR vs Frequency. An example is for a 1MHz full scale frequency and 1500Vrms, 60Hz barrier voltage; the output frequency is modulated –130dB R.T.I. = ±67Hz or ±67ppm. This linear modulation occurs up to the transient immunity limit of 10kV/μs as indicated on performance curve Recommended Range of Isolation Voltage. Above this level the output is interrupted and/or toggled by the barrier transients. Even under this condition, normal operation resumes as soon as the transient subsides. Over 20kV/μs can be tolerated in this mode without damage to the integrated circuits or to the ceramic high-voltage barrier.

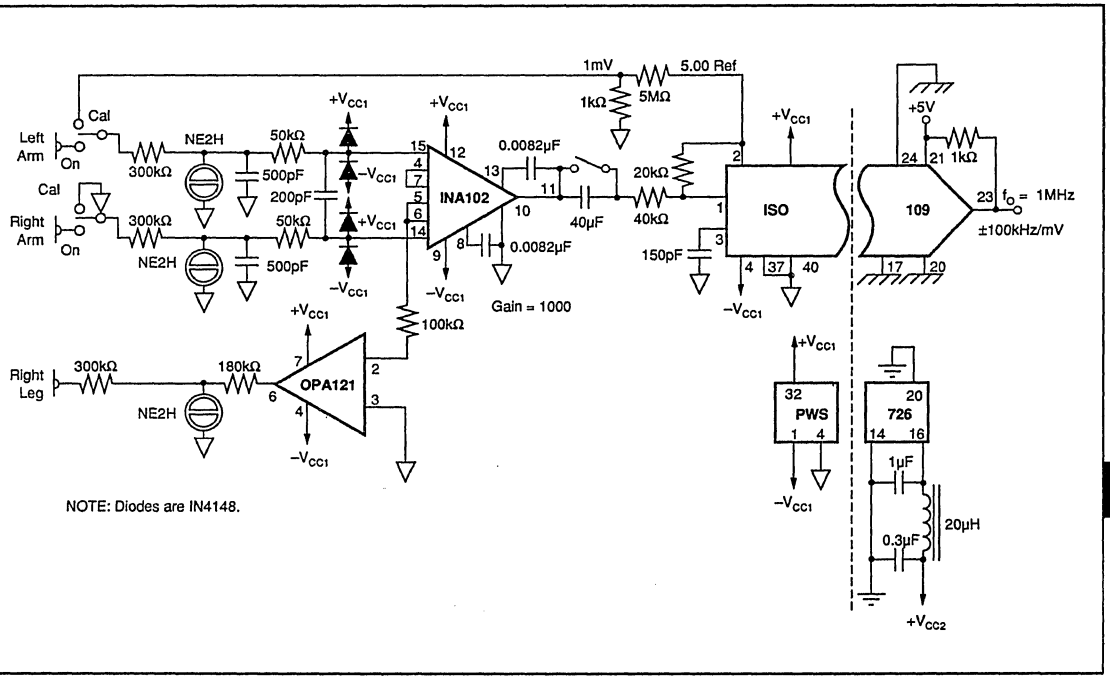
HIGH VOLTAGE TESTING

Burr-Brown Corporation has adopted a partial discharge test criterion that conforms to the German VDE0884 Optocoupler Standards. This method requires the measurement of minute current pulses (<5pC) while applying ≥2500Vrms (ISO108) or 5600Vrms (ISO109), 60Hz high-voltage stress across every device's isolation barrier. No partial discharge may be initiated to pass this test. This criterion confirms transient overvoltage ($1.6 \times V_{RATED}$) protection without damage to the ISOVFC. Life-test results verify the absence of failure under continuous rated voltage and maximum temperature.

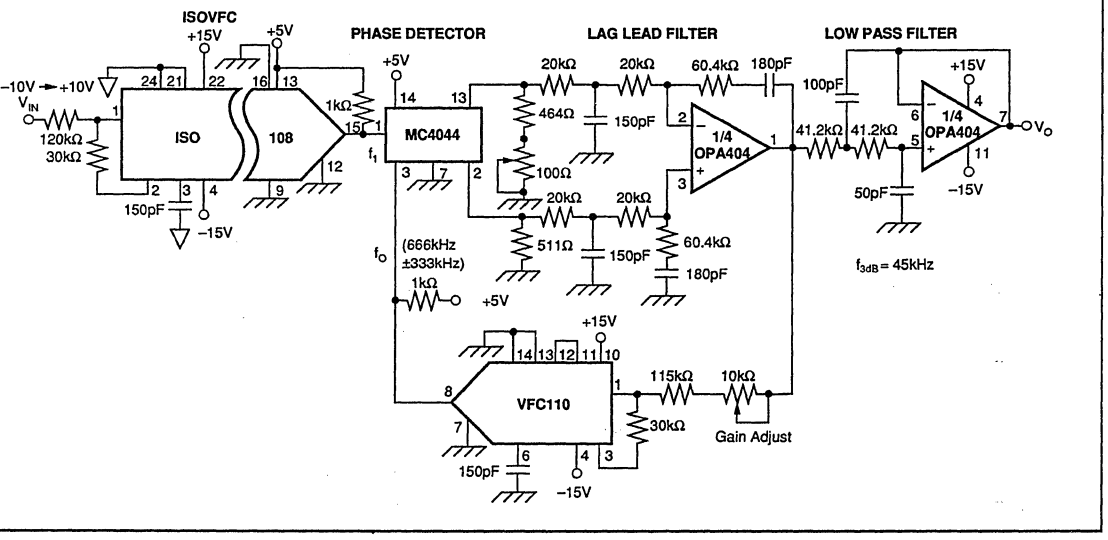
This new test method represents the "state of the art" for non-destructive high voltage reliability testing. It is based on the effects of non-uniform fields existing in heterogeneous dielectric material during barrier degradation. In the case of void non-uniformities, electric field stress begins to ionize the void region before bridging the entire high voltage barrier.

The transient conduction of charge during and after the ionization can be detected externally as a burst of 0.01μs-0.1μs current pulses that repeat on each AC voltage cycle. The minimum AC barrier voltage that initiates partial discharge is defined as the "inception voltage." Decreasing the barrier voltage to a lower level is required before partial discharge ceases and is defined as the "extinction voltage."

We have designed and characterized the package to yield an inception voltage in excess of 2500Vrms for the ISO108 and 5600Vrms for the ISO109 so that transient overvoltages below this level will not cause any damage. The extinction voltage is above 1500Vrms for the ISO108 and 3500Vrms for the ISO109, so that even overvoltage-induced partial discharge will cease once the barrier voltage is reduced to the rated level. Older high voltage test methods relied on applying a large enough overvoltage (above rating) to catastrophically break down marginal parts, but not so high as to damage good ones. Our new partial discharge testing gives us more confidence in barrier reliability than breakdown/no breakdown criteria.

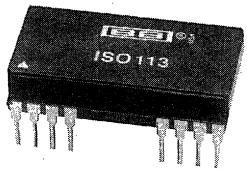


GURE 5. Serial TTL Output ECG Amplifier.



GURE 6. PLL Analog Isolator with High (10kV/µs) Transient Immunity.

BURR-BROWN®



ISO113

Low-Cost, High-Voltage, Internally Powered OUTPUT ISOLATION AMPLIFIER

FEATURES

- SELF-CONTAINED ISOLATED SIGNAL AND OUTPUT POWER
- SMALL PACKAGE SIZE: Double-Wide (0.6") Sidebraze DIP
- CONTINUOUS AC BARRIER RATING: 1500Vrms
- WIDE BANDWIDTH: 20kHz Small Signal, 20kHz Full Power
- BUILT-IN ISOLATED OUTPUT POWER: ±10V to ±18V Input, ±50mA Output
- MULTICHANNEL SYNCHRONIZATION CAPABILITY
- BOARD AREA ONLY 0.72in.² (4.6cm²)

APPLICATIONS

- 4mA TO 20mA V/I CONVERTERS
- MOTOR AND VALVE CONTROLLERS
- ISOLATED RECORDER OUTPUTS
- MEDICAL INSTRUMENTATION OUTPUTS
- GAS ANALYZERS

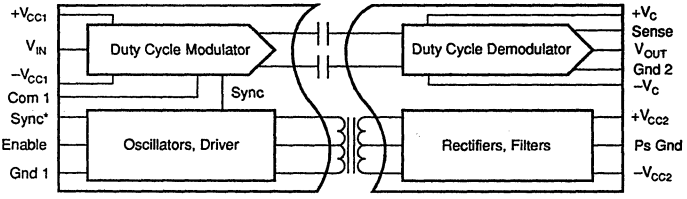
DESCRIPTION

The ISO113 output isolation amplifier provides both signal and output power across an isolation barrier in a small double-wide DIP package. The ceramic non-hermetic hybrid package with side-brazed pins contains a transformer-coupled DC/DC converter and a capacitor-coupled signal channel.

Extra power is available on the isolated output side for driving external loads. The converter is protected from shorts to ground with an internal current limit, and the soft-start feature limits the initial currents from the power source. Multiple-channel synchronization can be accomplished by applying a TTL clock signal to paralleled Sync pins. The Enable control is used to turn off transformer drive while keeping the signal channel modulator active. This feature provides a convenient way to reduce quiescent current for low power applications.

The wide barrier pin spacing and internal insulation allow for the generous 1500Vrms continuous rating. Reliability is assured by 100% barrier breakdown testing that conforms to UL1244 test methods. Low barrier capacitance minimizes AC leakage currents.

These specifications and built-in features make the ISO113 easy to use, and provides for compact PC board layout.



*Ground if not used

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PDS-844A

SPECIFICATIONS

ELECTRICAL

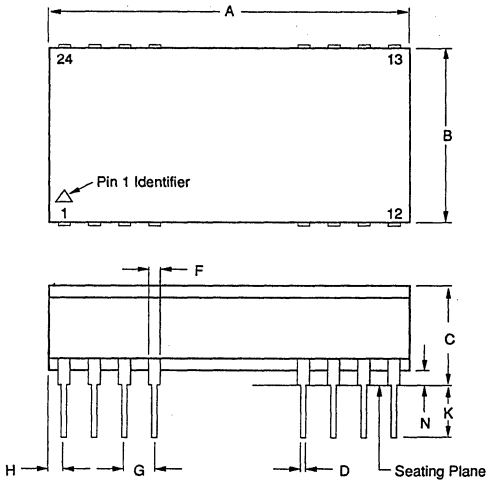
At T_A = +25°C and V_{CC1} = ±15V, ±15mA output current unless otherwise noted.

PARAMETER	CONDITIONS	ISO113 MIN	ISO113 TYP	ISO113 MAX	ISO113B MIN	ISO113B TYP	ISO113B MAX	UNITS
ISOLATION								
Rated Continuous Voltage								
AC, 60Hz	T_{MIN} to T_{MAX}	1500			*			Vrms
DC	T_{MIN} to T_{MAX}	2121			*			VDC
Test Breakdown, 100% AC, 60Hz	10s	5657			*			Vpk
Isolation-Mode Rejection	1500Vrms, 60Hz		130			*		dB
	2121VDC		160			*		dB
Barrier Impedance			10^{12} || 9			*		Ω || pF
Leakage Current	240Vrms, 60Hz		1	2		*	*	µA
GAIN								
Nominal			1			*		V/V
Initial Error			±0.3	±0.5		*	*	%FSR
Gain vs Temperature			±60	±100		±20	±50	ppm/°C
Nonlinearity	V_O = –10V to 10V		±0.05	±0.1		±0.03	±0.05	%FSR
	V_O = –5V to 5V		±0.02	±0.04		±0.012	±0.02	%FSR
INPUT OFFSET VOLTAGE								
Initial Offset			±20	±60		*	*	mV
vs Temperature			±300	±500		±100	±250	µV/°C
vs Power Supplies	V_{CC2} = ±10 to ±18V		0.9			*		mV/V
vs Output Supply Load	I_O = 0 to ±50mA		±0.3			*		mV/mA
SIGNAL INPUT								
Voltage Range	Output Voltage in Range	±10	±15		*	*		V
Resistance			200			*		kΩ
SIGNAL OUTPUT								
Voltage Range		±10	±12.5		*	*		V
Current Drive		±5	±20		*	*		mA
Ripple Voltage, 800kHz Carrier			25			*		mVp-p
	400Ω/4.7nF (See Figure 4)		5			*		mVp-p
Capacitive Load Drive			1000			*		pF
Voltage Noise			4			*		µV/√Hz
FREQUENCY RESPONSE								
Small Signal Bandwidth			20			*		kHz
Slew Rate			1.5			*		V/µs
Settling Time	0.1%, –10/10V		75			*		µs
POWER SUPPLIES								
Rated Voltage, V_{CC1}			±15			*		V
Voltage Range		±10		±18	*		*	V
Input Current	I_O = ±15mA		+90/–4.5			*		mA
Ripple Current	No Filter		60			*		mAp-p
	C_{IN} = 1µF		3			*		mAp-p
Rated Output Voltage		±14.25	±15	±15.75	*	*	*	V
Output Current	Balanced Load		±15	±50		*		mA
	Single		30	100		*		mA
Load Regulation	Balanced Load		0.3			*		%/mA
Line Regulation			1.12			*		V/V
Output Voltage vs Temperature			2.5			*		mV/°C
Voltage Balance, ±V_{CC2}			0.05			*		%
Voltage Ripple (800kHz)	No External Capacitors		50			*		mVp-p
	C_{EXT} = 1µF		5			*		mVp-p
Output Capacitive Load				1			*	µF
Sync Frequency	TTL, 50% Duty Cycle	1.25	1.6	2	*	*	*	MHz
TEMPERATURE RANGE								
Specification		–25		+85	*		*	°C
Operating		–25		+85	*		*	°C
Storage		–25		+125	*		*	°C

NOTE: (1) Conforms to UL1244 test methods. 100% tested at 1500Vrms for 1 minute.

MECHANICAL

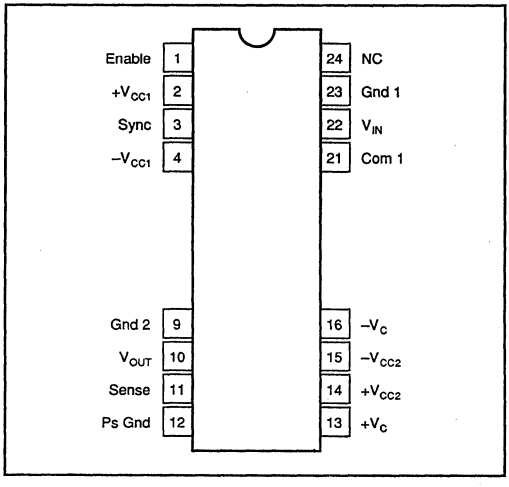
24-Pin Double-Wide DIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.180	1.220	29.97	30.99
B	.580	.600	14.73	15.24
C	.310	.370	7.87	9.40
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.600	.620	15.24	15.75
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

PIN CONFIGURATION



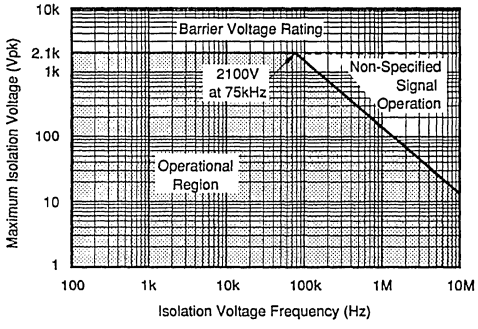
ABSOLUTE MAXIMUM RATINGS

Supply Without Damage	±18V
V_{IN}, Sense Voltage	±50V
Com to Gnd (either input or output)	±200mV
Enable, Sync	Gnd to $+V_{CC1}$
Continuous Isolation Voltage	1500Vrms
V_{ISO}, dv/dt	20kV/µs
Junction Temperature	+150°C
Storage Temperature	–25°C to +125°C
Lead Temperature,10s	+300°C
Output Short to Gnd Duration	Continuous
$\pm V_{CC2}$ to Gnd 2 Duration	Continuous

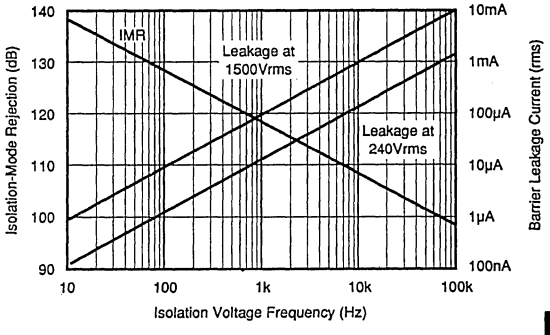
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC1} = ±15VDC, ±15mA output current unless otherwise noted.

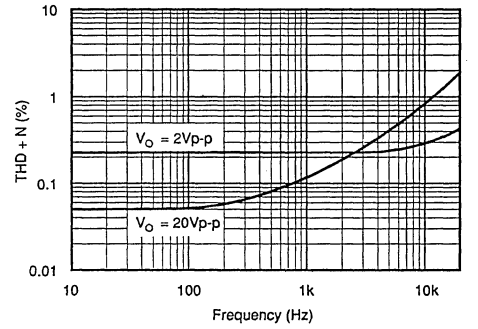
RECOMMENDED RANGE OF ISOLATION VOLTAGE



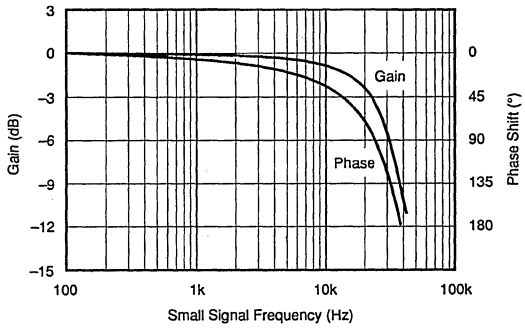
IMR/LEAKAGE vs FREQUENCY



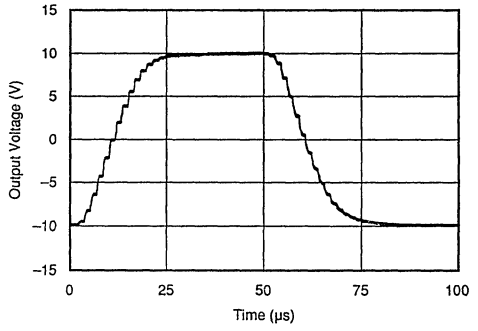
DISTORTION vs FREQUENCY



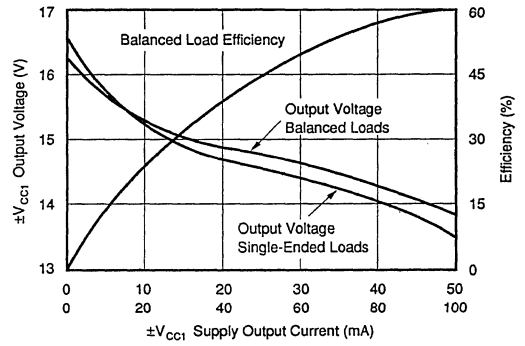
GAIN/PHASE vs FREQUENCY



LARGE SIGNAL TRANSIENT RESPONSE



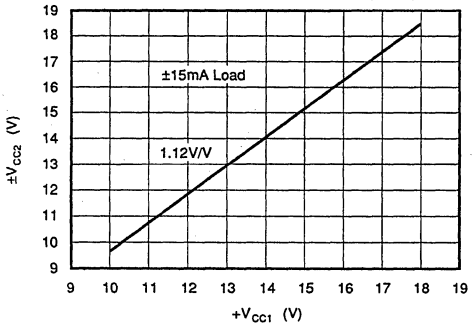
ISOLATED POWER SUPPLY
LOAD REGULATION AND EFFICIENCY



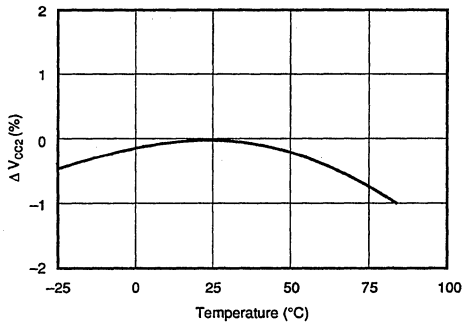
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC1} = ±15VDC, ±15mA output current unless otherwise noted.

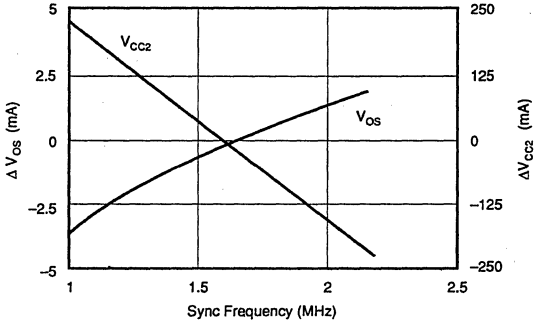
ISOLATED POWER SUPPLY LINE REGULATION

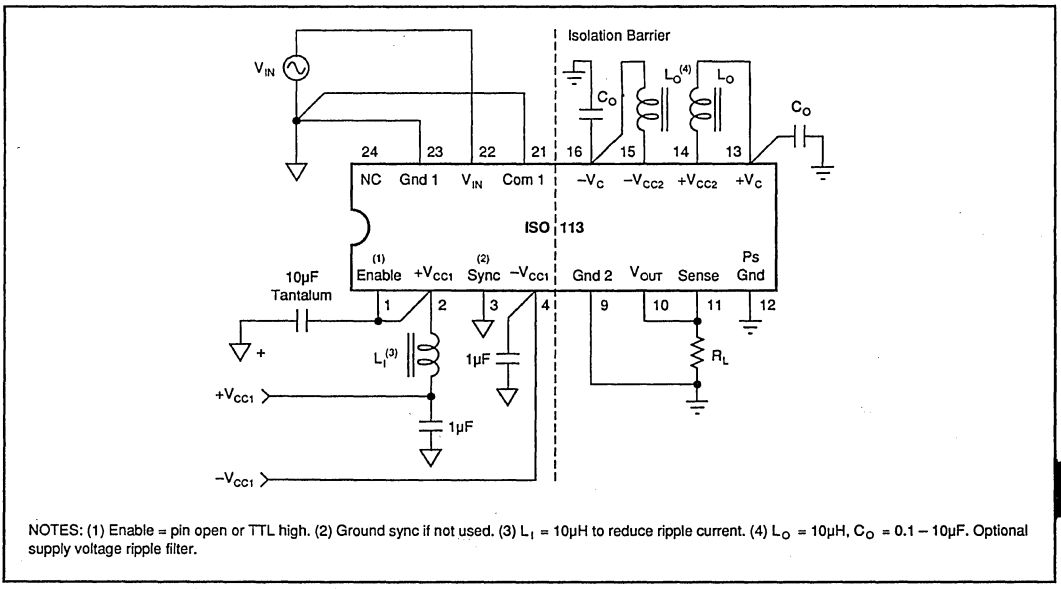


ISOLATION POWER SUPPLY VOLTAGE vs TEMPERATURE



ISOLATED SUPPLY VOLTAGE AND V_{OS} vs SYNC FREQUENCY





NOTES: (1) Enable = pin open or TTL high. (2) Ground sync if not used. (3) L_I = 10µH to reduce ripple current. (4) L_O = 10µH, C_O = 0.1 – 10µF. Optional supply voltage ripple filter.

FIGURE 1. Signal and Power Connections.

THEORY OF OPERATION

The block diagram on the front page shows the isolation amplifier's synchronized signal and power configuration, which eliminate beat frequency interference. A proprietary 800kHz oscillator chip, power MOSFET transformer drivers, patented square core wirebonded transformer, and single chip diode bridge provide power to the output side of the isolation amplifier as well as external loads. The signal channel capacitively couples a duty-cycle encoded signal across the ceramic high-voltage barrier built into the package. A proprietary transmitter-receiver pair of integrated circuits, laser trimmed at wafer level, and coupled through a pair of matched "fringe" capacitors, results in a simple, reliable design.

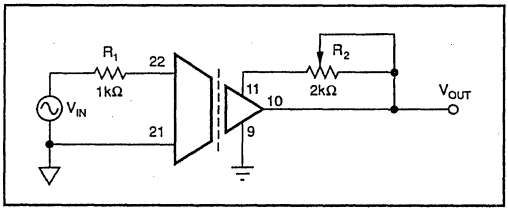


FIGURE 2a. Gain Adjust.

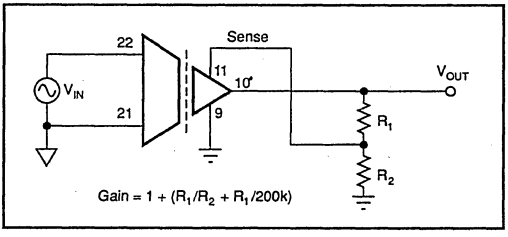


FIGURE 2b. Gain Setting.

SIGNAL AND POWER CONNECTIONS

Figure 1 shows the proper power supply and signal connections. All power supply pins should be bypassed as shown with the π filter for $+V_{CC1}$, an option recommended if more than ±15mA are drawn from the isolated supply. Separate rectifier output pins ($\pm V_{CC2}$) and amplifier supply input pins ($\pm V_C$) allow additional ripple filtering and/or regulation. The separate input common pin and output sense are low current inputs tied to the signal source ground, and output load, respectively, to minimize errors due to IR drop in long conductors. Otherwise, connect Com 1 to Gnd 1, and Sense to V_{OUT} at the ISO113 socket. The enable pin may be left open if the ISO113 is continuously operated. If not, a TTL low level will disable the internal DC/DC converter. The Sync input must be grounded for unsynchronized operation while a 1.25MHz to 2MHz TTL clock signal provides synchronization of multiple units.

OPTIONAL GAIN AND OFFSET ADJUSTMENTS

Rated gain accuracy and offset performance can be achieved with no external adjustments, but the circuit of Figure 2a may be used to provide a gain trim of ±0.5% for the values shown. Greater range may be provided by increasing the size of R_1 and R_2. Every 2kΩ increase in R_1 will give an additional 1% adjustment range, with $R_2 \geq 2R_1$. If safety or convenience dictate location of the adjustment potentiometer on the other side of the barrier from the position shown in Figure 2a, the position of R_1 and R_2 may be reversed.

Gains greater than 1 may be obtained by using the circuit of Figure 2b. Note that the effect of input referred errors will be multiplied at the output in proportion to the increase in gain. Also, the small-signal bandwidth will be decreased in inverse proportion to the increase in gain. In most instances, a precision gain block at the input of the isolation amplifier will provide better overall performance.

Figure 3 shows a method for trimming V_{OS} of the ISO113. This circuit may be applied to either Signal Com1 or Gnd2 as desired for safety or convenience. With the values shown, ±15V supplies and unity gain, the circuit will provide ±150mV adjustment range and 0.25mV resolution with a typical trim potentiometer. The output will have some sensitivity to power supply variations. For a ±100mV trim, power supply sensitivity is 8mV/V at the output.

OPTIONAL OUTPUT FILTER

Figure 4 shows an optional output ripple filter that reduces the 800kHz ripple voltage to <5mVp-p without compromising DC performance. The small signal bandwidth is extended above 30kHz as a result of this compensation.

MULTICHANNEL SYNCHRONIZATION

Synchronization of multiple ISO113s can be accomplished by connecting pin 3 of each device to an external TTL level oscillator, as shown in Figure 7. The PWS750-1 oscillator is convenient because its nominal synchronizing output frequency is 1.6MHz, resulting in a 800kHz carrier in the ISO113 (its nominal unsynchronized value). The open collector output typically switches 7.5mA to a 0.2V low level so that the external pull up resistor can be chosen for different pull-up voltages as shown in Figure 7. The number of channels synchronized by one PWS750-1 is determined by the total capacitance of the sync voltage conductors. They must be less than 1000pF to ensure TTL level switching at 800kHz. At higher frequencies the capacitance must be proportionally lower.

Customers can supply their own TTL level synchronization logic, provided the frequency is between 1.25MHz and 2MHz, and the duty cycle is greater than 25%.

Single or multichannel synchronization with reduced power dissipation for applications requiring less than ±15mA from V_{CC1} is accomplished by driving both the Sync input pin (3) and Enable pin (1) with the TTL oscillator as shown in Figure 5.

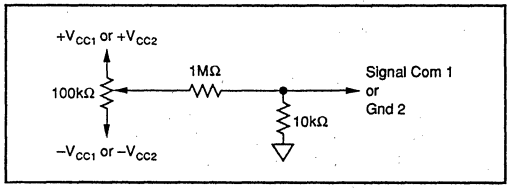


FIGURE 3. V_{OS} Adjust.

ISOLATION BARRIER VOLTAGE

The typical performance of the ISO113 under conditions of barrier voltage stress is indicated in the first two performance curves—Recommended Range of Isolation Voltage and IMR/ Leakage vs Frequency. At low barrier modulation levels, errors can be determined by the IMRR characteristic. At higher barrier voltages, typical performance is obtained as long as the dv/dt across the barrier is below the shaded area in the first curve. Otherwise, the signal channel will be interrupted, causing the output to distort, and/or shift DC level. This condition is temporary, with normal operation resuming as soon as the transient subsides. Permanent damage to the integrated circuits occurs only if transients exceed 20kV/µs. Even in this extreme case, the barrier integrity is assured.

HIGH VOLTAGE TESTING

The ISO113 was designed to reliably operate with 1500Vrms continuous isolation barrier voltage. To confirm barrier integrity, a two-step breakdown test is performed on 100% of the units. First, an 5657V peak, 60Hz barrier potential is applied for 10s to verify that the dielectric strength of the insulation is above this level. Following this exposure, a 1500Vrms, 60Hz potential is applied for one minute to conform to UL1244. Life-test results show reliable operation under continuous rated voltage and maximum operating temperature conditions.

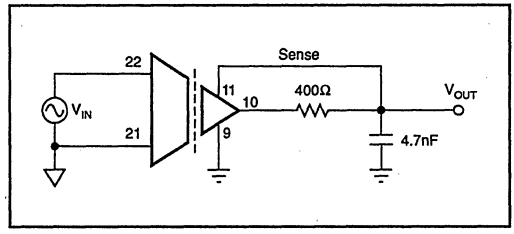


FIGURE 4. Ripple Reduction.

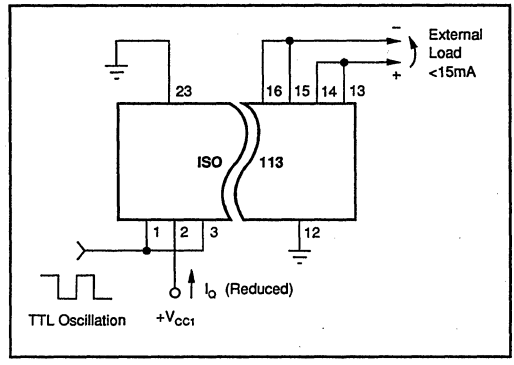


FIGURE 5. Reduced Power Dissipation.

APPLICATIONS

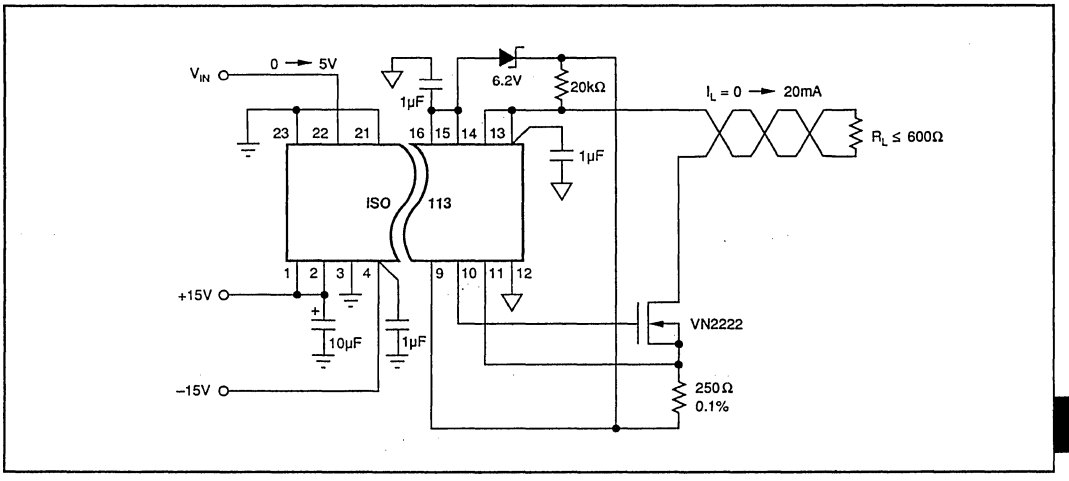


FIGURE 6. Isolated Current Loop Driver.

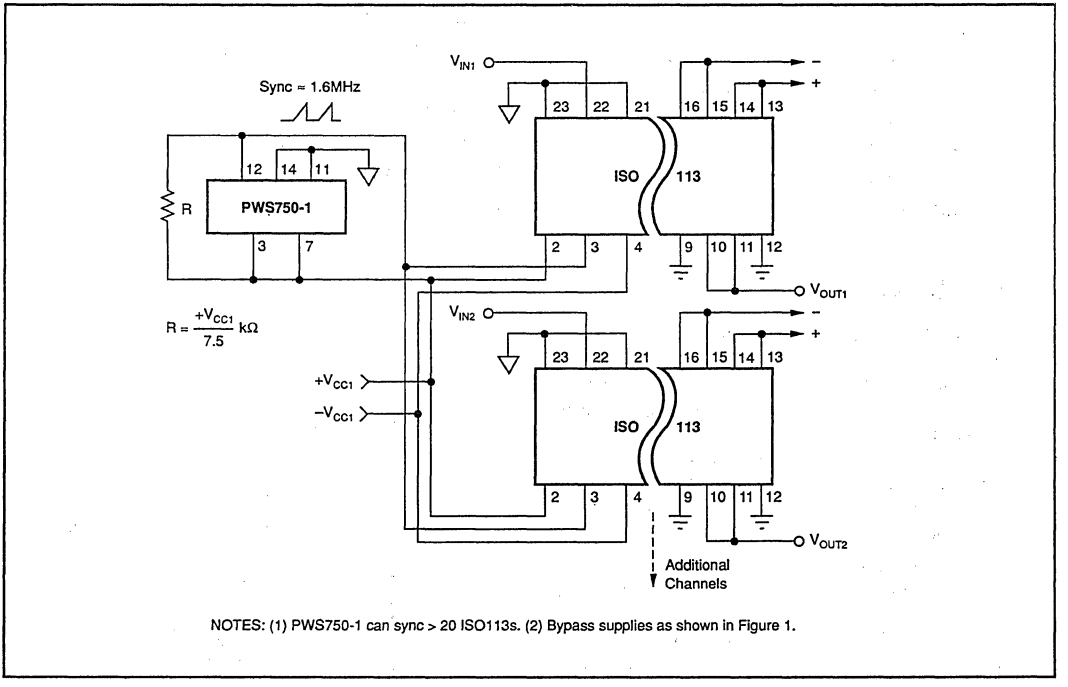


FIGURE 7. Synchronized-Multichannel Isolation.

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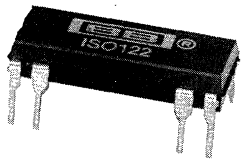


ISO122P

Precision Lowest Cost ISOLATION AMPLIFIER

FEATURES

- 100% TESTED FOR HIGH-VOLTAGE BREAKDOWN
- RATED 1500Vrms
- HIGH IMR: 140dB at 60Hz
- BIPOLAR OPERATION: $V_O = \pm 10V$
- SINGLE-WIDE 16-PIN PLASTIC DIP
- EASE OF USE: Fixed Unity Gain Configuration
- 0.020% max NONLINEARITY
- ±4.5V to ±18V SUPPLY RANGE

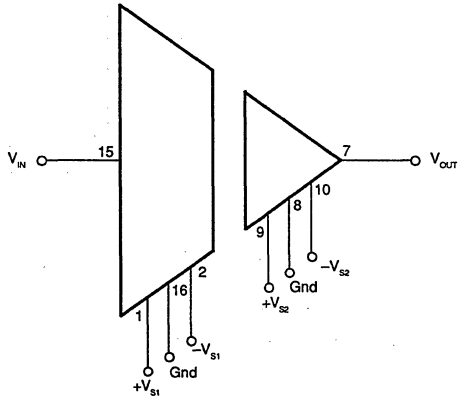
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL: Transducer Isolator, Isolator for Thermocouples, RTDs, Pressure Bridges, and Flow Meters, 4mA to 20mA Loop Isolation
- GROUND LOOP ELIMINATION
- MOTOR AND SCR CONTROL
- POWER MONITORING
- PC-BASED DATA ACQUISITION
- TEST EQUIPMENT
- VENDING MACHINES

DESCRIPTION

The ISO122P is a precision isolation amplifier incorporating a novel duty cycle modulation-demodulation technique. The signal is transmitted digitally across a 2pF differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity, resulting in excellent reliability and good high frequency transient immunity across the barrier. Both barrier capacitors are imbedded in the plastic body of the package.

The ISO122P is easy to use. No external components are required for operation. The key specifications are 0.020% max nonlinearity, 50kHz signal bandwidth, and 200µV/°C V_{OS} drift. A power supply range of ±4.5V to ±18V and quiescent currents of ±4.5mA on V_{S1} and ±5.0mA on V_{S2} make these amplifiers ideal for a wide range of applications.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-857C

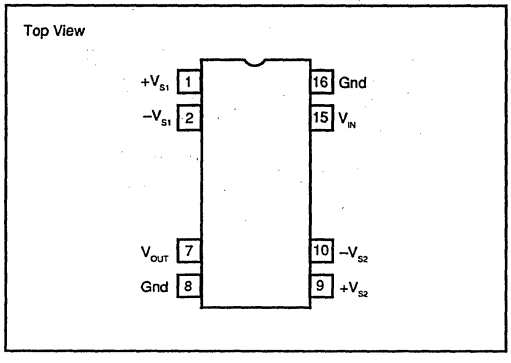
SPECIFICATIONS

At T_A = +25°C , V_{S1} = V_{S2} = ±15V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ISOLATION					
Voltage Rated Continuous AC 60Hz		1500			VAC
100% Test[1]	1s, 5pc PD	2400			VAC
Isolation Mode Rejection	60Hz		140		dB
Barrier Impedance			10^{14} || 2		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms		0.18	0.5	µArms
GAIN	V_O = ±10V				
Nominal Gain			1		V/V
Gain Error			±0.05	±0.50	%FSR
Gain vs Temperature			±10		ppm/°C
Nonlinearity			±0.008	±0.020	%FSR
INPUT OFFSET VOLTAGE					
Initial Offset			±5	±50	mV
vs Temperature			±200		µV/°C
vs Supply			±2		mV/V
Noise			4		µV/√Hz
INPUT					
Voltage Range[2]		±10	±12.5		V
Resistance			200		kΩ
OUTPUT					
Voltage Range		±10	±12.5		V
Current Drive		±5	±20		mA
Capacitive Load Drive			0.1		µF
Ripple Voltage[3]			20		mVp-p
FREQUENCY RESPONSE					
Small Signal Bandwidth			50		kHz
Slew Rate			2		V/µs
Settling Time	V_O = ±10V				
0.1%			50		µs
0.01%			350		µs
Overload Recover Time			150		µs
POWER SUPPLIES					
Rated Voltage			±15		V
Voltage Range		±4.5		±18	V
Quiescent Current: V_{S1}			±4.5	±7.0	mA
V_{S2}			±5.0	±7.0	mA
TEMPERATURE RANGE					
Specification		0		70	°C
Operating		–25		85	°C
Storage		–25		85	°C
θ_{JA}			100		°C/W

NOTES: (1) Tested at 1.6 X rated, fail on 5pC partial discharge. (2) Input Range is ±10V independent of input ±V_{S1}. (3) Ripple frequency is at carrier frequency (500kHz).

CONNECTION DIAGRAM

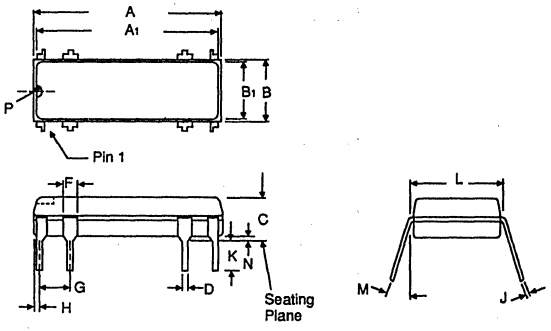


ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
V_{IN}	±100V
Continuous Isolation Voltage	1500Vrms
Junction Temperature	+150°C
Storage Temperature	+85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short to Common	Continuous

MECHANICAL

P Package — Single-Wide 16-Pin Plastic DIP



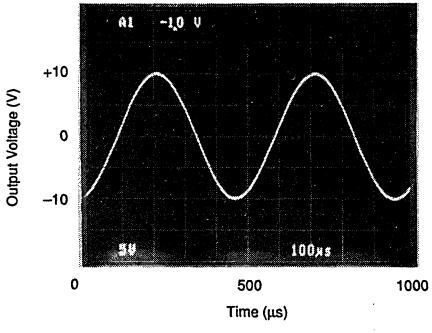
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.740	.800	18.80	20.32
A1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	0.20	.050	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

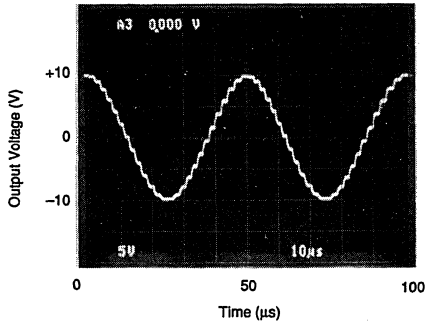
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

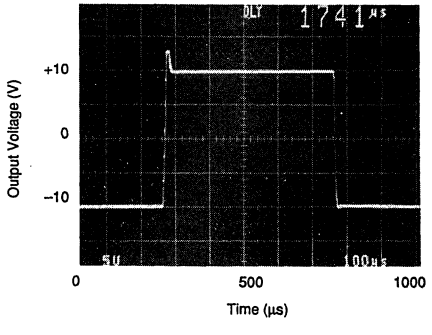
SINE RESPONSE
(f = 2kHz)



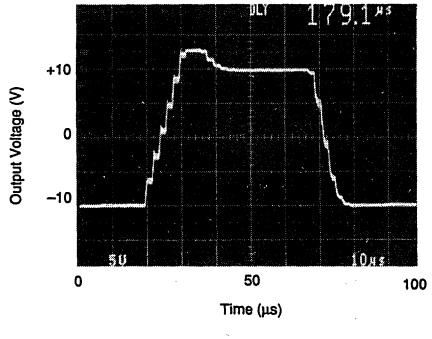
SINE RESPONSE
(f = 20kHz)



STEP RESPONSE



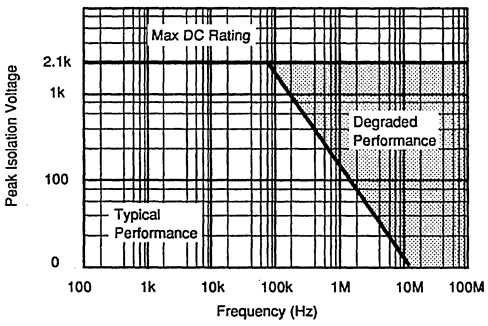
STEP RESPONSE



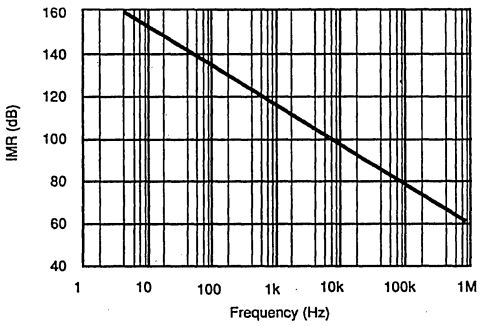
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

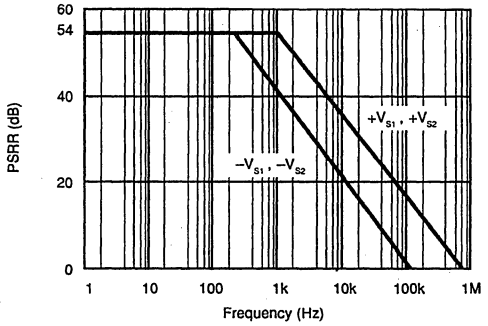
ISOLATION VOLTAGE vs FREQUENCY



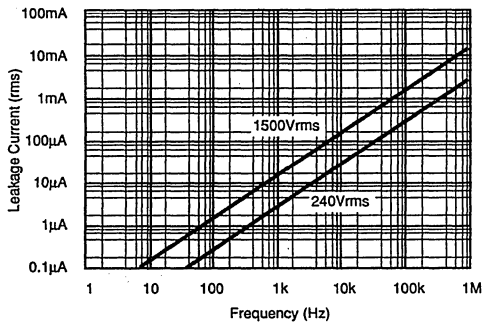
IMR vs FREQUENCY



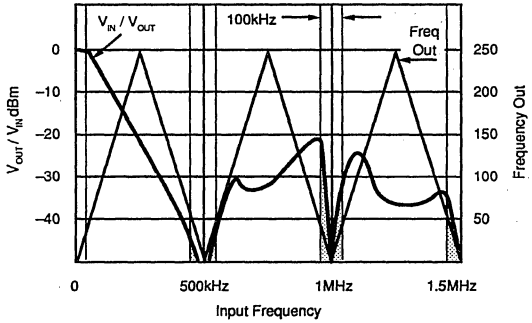
PSRR vs FREQUENCY



ISOLATION LEAKAGE CURRENT vs FREQUENCY



SIGNAL RESPONSE TO INPUTS GREATER THAN 250kHZ



(NOTE: Shaded area shows aliasing frequencies that cannot be removed by a low-pass filter at the output.)

THEORY OF OPERATION

The ISO122P isolation amplifier uses an input and an output section galvanically isolated by matched 1pF isolating capacitors built into the plastic package. The input is duty-cycle modulated and transmitted digitally across the barrier. The output section receives the modulated signal, converts it back to an analog voltage and removes the ripple component inherent in the demodulation. Input and output sections are fabricated, then laser trimmed for exceptional circuitry matching common to both input and output sections. The sections are then mounted on opposite ends of the package with the isolating capacitors mounted between the two sections.

MODULATOR

An input amplifier (A1, Figure 1) integrates the difference between the input current (V_{IN}/200kΩ) and a switched ±100µA current source. This current source is implemented by a switchable 200µA source and a fixed 100µA current sink. To understand the basic operation of the modulator, assume that V_{IN} = 0.0V. The integrator will ramp in one direction until the comparator threshold is exceeded. The comparator and sense amp will force the current source to switch; the resultant signal is a triangular waveform with a 50% duty cycle. The internal oscillator forces the current source to switch at 500kHz. The resultant capacitor drive is a complementary duty-cycle modulation square wave.

DEMODULATOR

The sense amplifier detects the signal transitions across the capacitive barrier and drives a switched current source into integrator A2. The output stage balances the duty-cycle modulated current against the feedback current through the 200kΩ feedback resistor, resulting in an average value at the V_{OUT} pin equal to V_{IN}. The sample and hold amplifiers in the output feedback loop serve to remove undesired ripple voltages inherent in the demodulation process.

BASIC OPERATION

SIGNAL AND SUPPLY CONNECTIONS

Each power supply pin should be bypassed with 1µF tantalum capacitors located as close to the amplifier as possible. The internal frequency of the modulator/demodulator is set at 500kHz by an internal oscillator. Therefore if it is desired to minimize any feedthrough noise (beat frequencies) from a DC/DC converter, use a π filter on the supplies (see Figure 4). ISO122P output has a 500kHz ripple of 20mV, which can be removed with a simple two pole low-pass filter with a 100kHz cutoff using a low cost op amp. See Figure 4.

The input to the modulator is a current (set by the 200kΩ integrator input resistor) that makes it possible to have an input voltage greater than the input supplies, as long as the output supply is at least ±15V. It is therefore possible when using an unregulated DC/DC converter to minimize PSR related output errors with ±5V voltage regulators on the isolated side and still get the full ±10V input and output swing. An example of this application is shown in Figure 10.

CARRIER FREQUENCY CONSIDERATIONS

The ISO122P amplifier transmits the signal across the isolation barrier by a 500kHz duty cycle modulation technique. For input signals having frequencies below 250kHz, this system works like any linear amplifier. But for frequencies above 250kHz, the behavior is similar to that of a sampling amplifier. The signal response to inputs greater than 250kHz performance curve shows this behavior graphically; at input

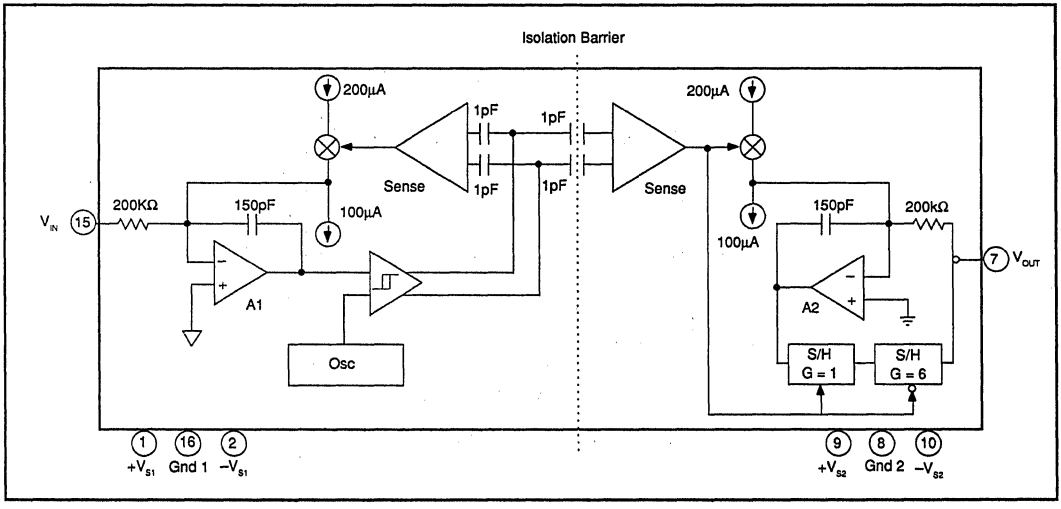


FIGURE 1. Block Diagram.

frequencies above 250kHz the device generates an output signal component of reduced magnitude at a frequency below 250kHz. This is the aliasing effect of sampling at frequencies less than 2 times the signal frequency (the Nyquist frequency). Note that at the carrier frequency and its harmonics, both the frequency and amplitude of the aliasing go to zero.

ISOLATION MODE VOLTAGE INDUCED ERRORS

IMV can induce errors at the output as indicated by the plots of IMV vs Frequency. It should be noted that if the IMV frequency exceeds 250kHz, the output also will display spurious outputs (aliasing), in a manner similar to that for V_{IN} > 250kHz and the amplifier response will be identical to that shown in the Signal Response to Inputs Greater Than 250kHz performance curve. This occurs because IMV-induced errors behave like input-referred error signals. To predict the total error, divide the isolation voltage by the IMR shown in the IMR vs Frequency curve and compute the amplifier response to this input-referred error signal from the data given in the Signal Response to Inputs Greater than 250kHz performance curve. For example if a 800kHz 1000Vrms IMR is present, then a total of [(–60dB) + (–30dB)] x (1000V) = 32mV error signal at 200kHz plus a 1V, 800kHz error signal will be present at the output.

HIGH IMV dV/dt ERRORS

As the IMV frequency increases and the dV/dt exceeds 1000V/µs, the sense amp may start to false trigger, and the output will display spurious errors. The common mode current being sent across the barrier by the high slew rate is the cause of the false triggering of the sense amplifier. Lowering the power supply voltages below ±15V may decrease the dV/dt to 500V/µs for typical performance.

HIGH VOLTAGE TESTING

Burr-Brown Corporation has adopted a partial discharge test criterion that conforms to the German VDE0884 Optocoupler Standards. This method requires the measurement of minute current pulses (<5pC) while applying 2400Vrms, 60Hz high voltage stress across every ISO122 isolation barrier. No partial discharge may be initiated to pass this test. This criterion confirms transient overvoltage (1.6 x 1500Vrms) protection without damage to the ISO122. Lifetest results verify the absence of failure under continuous rated voltage and maximum temperature.

This new test method represents the "state of the art" for non-destructive high voltage reliability testing. It is based on the effects of non-uniform fields that exist in heterogeneous dielectric material during barrier degradation. In the case of void non-uniformities, electric field stress begins to ionize the void region before bridging the entire high voltage barrier. The transient conduction of charge during and after the ionization can be detected externally as a burst of 0.01-0.1µs current pulses that repeat on each AC voltage cycle. The minimum AC barrier voltage that inititates partial discharge is defined as the "inception voltage." Decreasing the barrier voltage to a lower level is required before partial discharge ceases and is defined as the "extinction voltage." We have characterized and developed the package insulation processes to yield an inception voltage in excess of 2400Vrms so that transient overvoltages below this level will not damage the ISO122. The extinction voltage is above 1500Vrms so that even overvoltage induced partial discharge will cease once the barrier voltage is reduced to the 1500Vrms (rated) level. Older high voltage test methods relied on applying a large enough overvoltage (above rating) to break down marginal parts, but not so high as to damage good ones. Our new partial discharge testing gives us more confidence in barrier reliability than breakdown/no breakdown criteria.

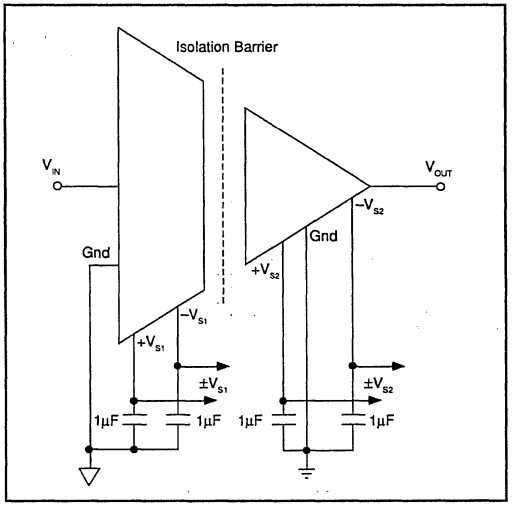


FIGURE 2. Basic Signal and Power Connections.

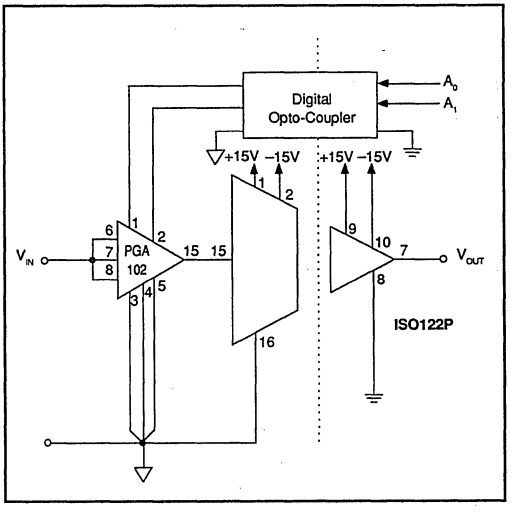


FIGURE 3. Programmable-Gain Isolation Channel with Gains of 1, 10, and 100.

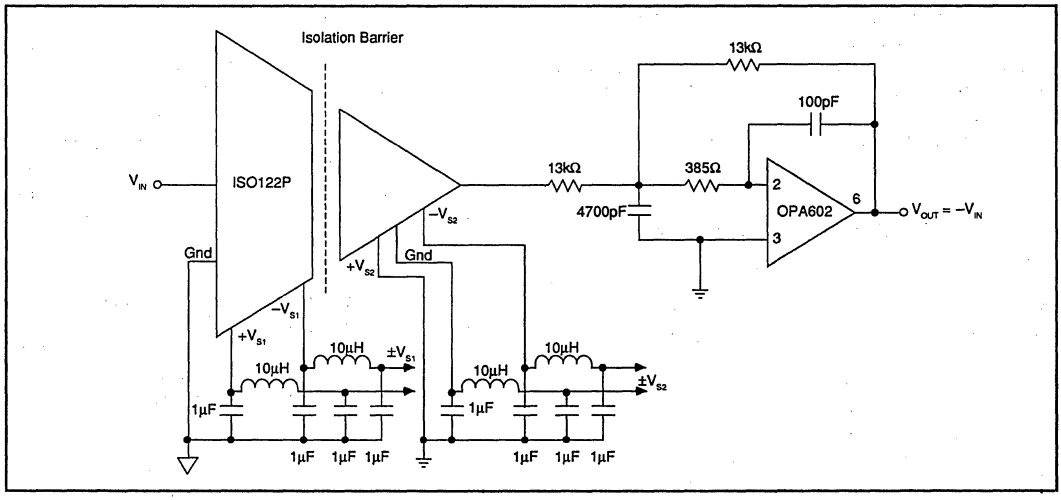


FIGURE 4. Optional π Filter to Minimize Power Supply Feedthrough Noise; Output Filter to Remove 500kHz Carrier Ripple.

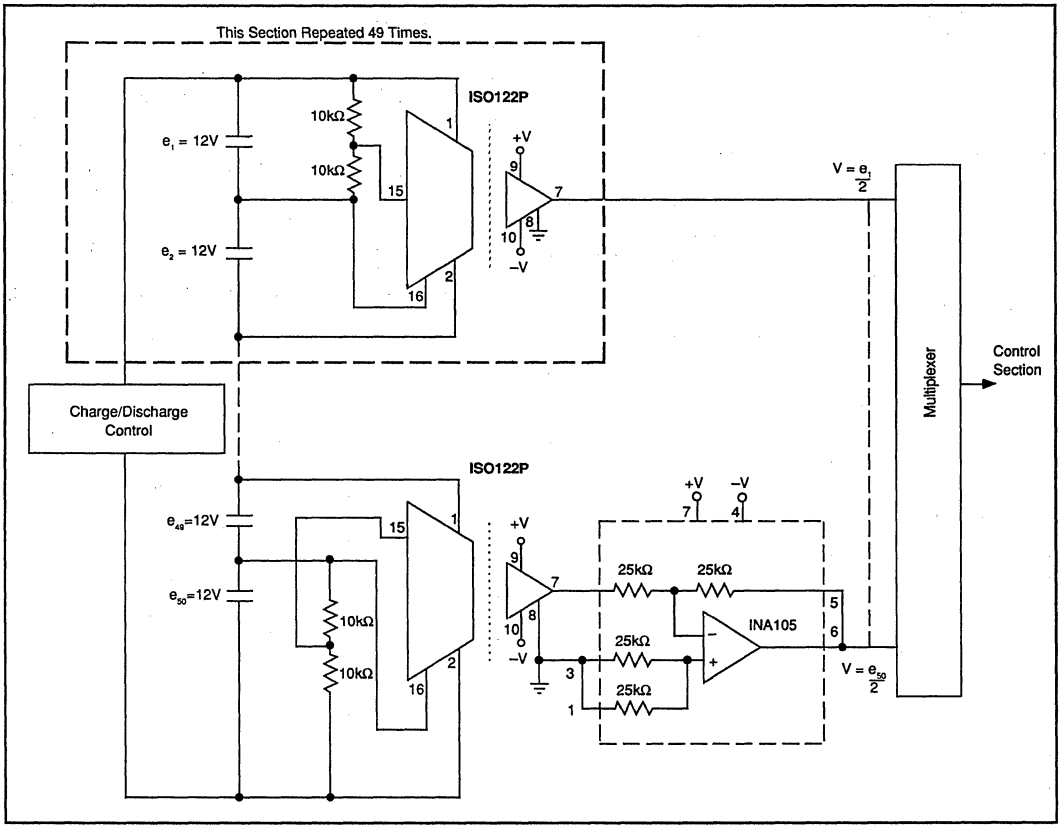
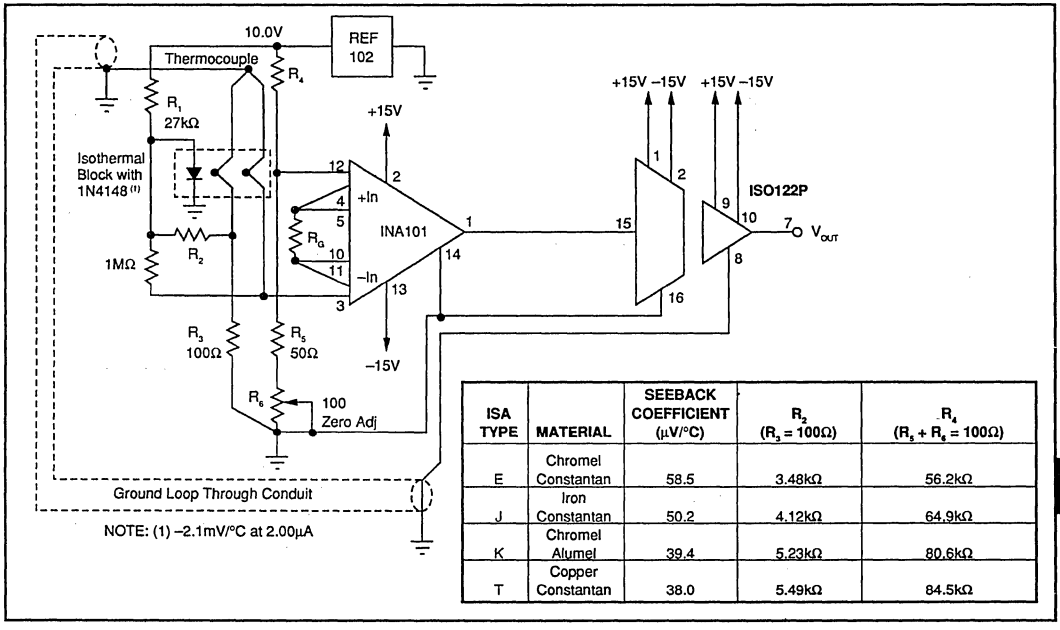


FIGURE 5. Battery Monitor for a 600V Battery Power System. (Derives Input Power from the Battery.)



ISA TYPE	MATERIAL	SEEBACK COEFFICIENT (µV/°C)	R_2 (R_3 = 100Ω)	R_4 (R_5 + R_6 = 100Ω)
E	Chromel Constantan	58.5	3.48kΩ	56.2kΩ
J	Iron Constantan	50.2	4.12kΩ	64.9kΩ
K	Chromel Alumel	39.4	5.23kΩ	80.6kΩ
T	Copper Constantan	38.0	5.49kΩ	84.5kΩ

FIGURE 6. Thermocouple Amplifier with Ground Loop Elimination, Cold Junction Compensation, and Up-scale Burn-out.

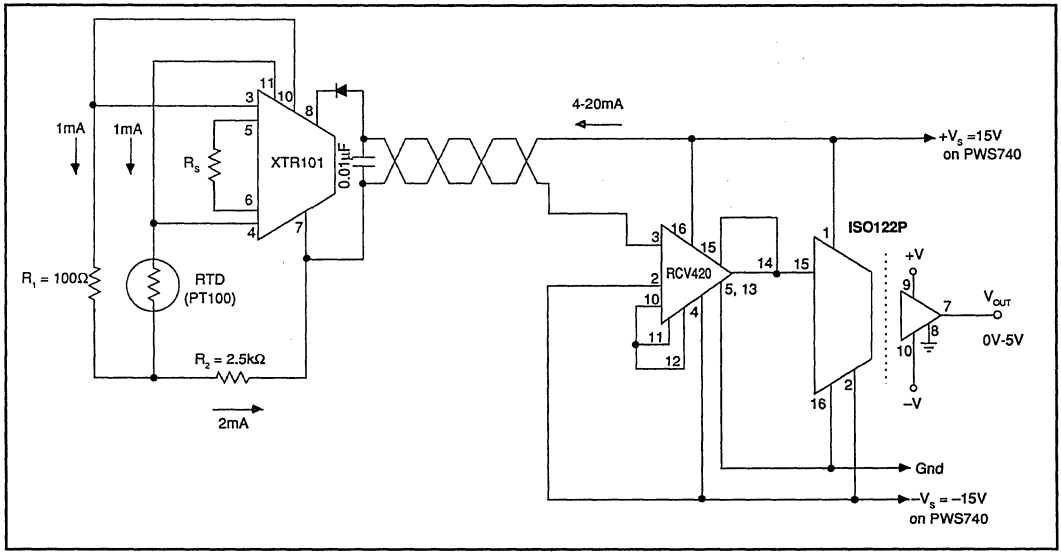


FIGURE 7. Isolated 4-20mA Instrument Loop. (RTD shown.)

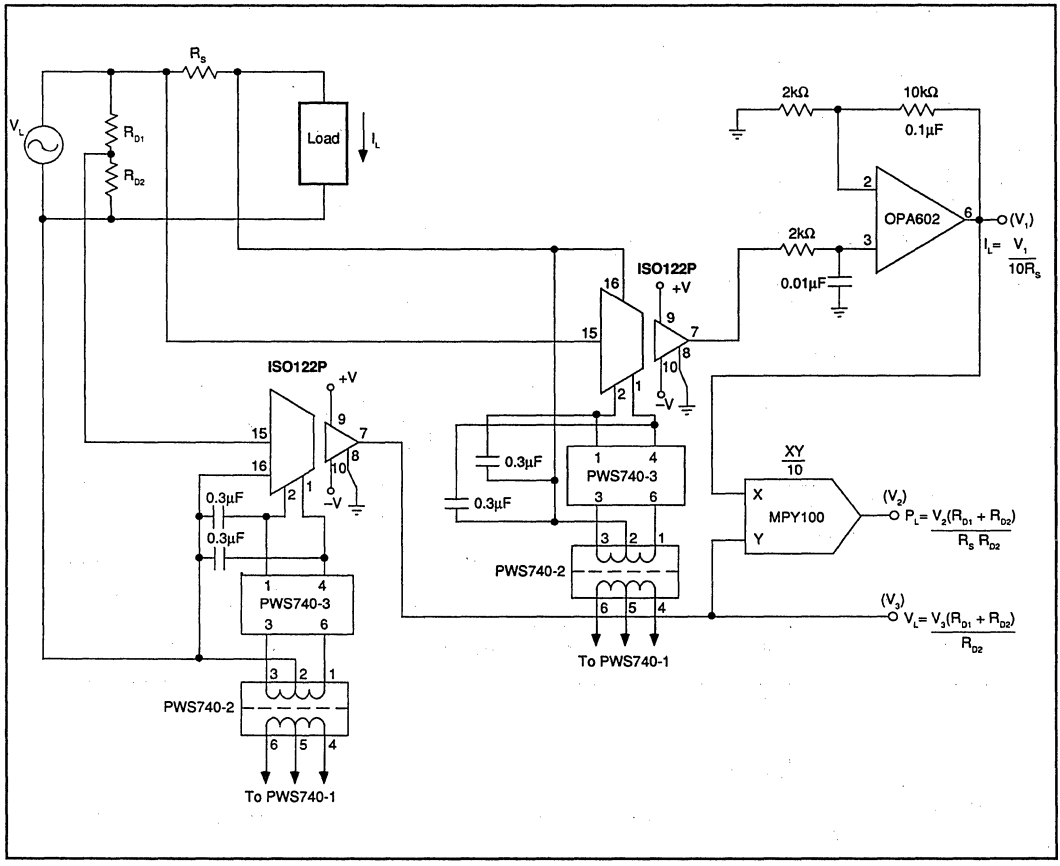


FIGURE 8. Isolated Power Line Monitor.

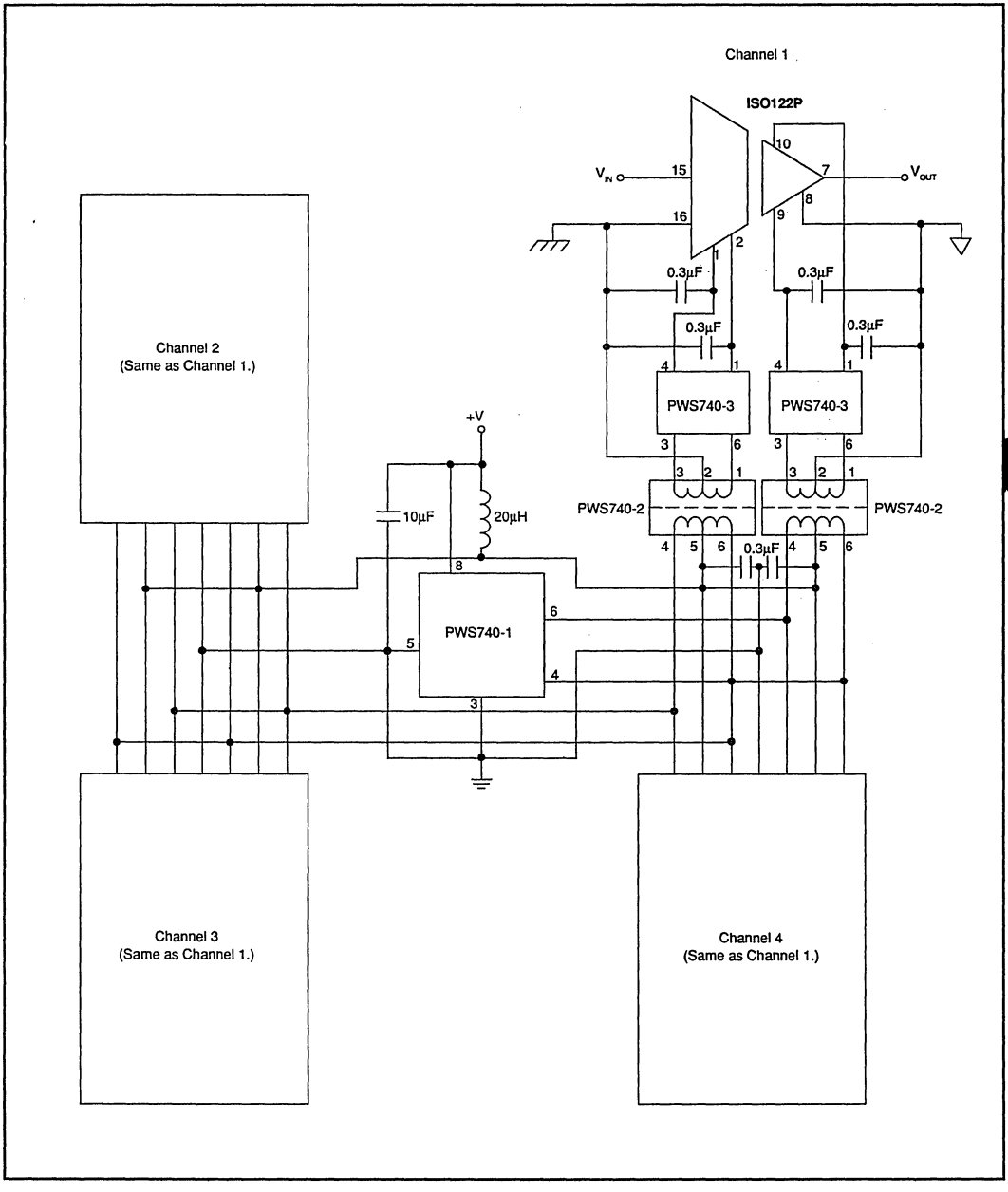


FIGURE 9. Three-Port, Low-Cost, Four-Channel Isolated, Data Acquisition System.

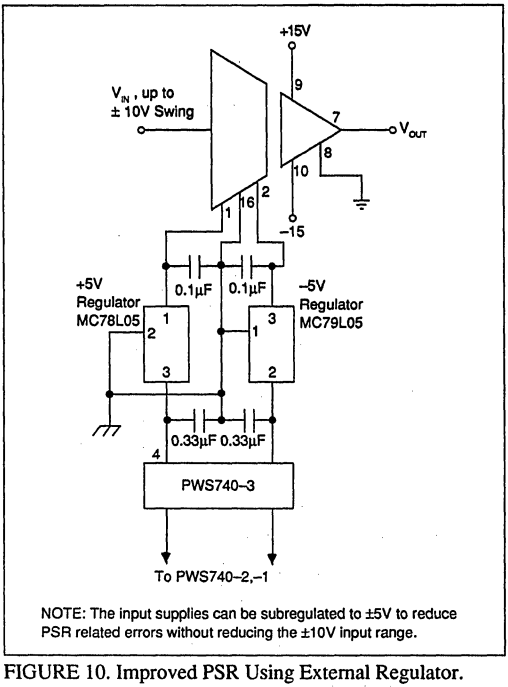


FIGURE 10. Improved PSR Using External Regulator.

BURR-BROWN®

ISO212P

Low Cost, Two-Port Isolated, Low Profile ISOLATION AMPLIFIER

FEATURES

- 12-BIT ACCURACY
- LOW PROFILE (LESS THAN 0.5" HIGH)
- SMALL FOOTPRINT
- EXTERNAL POWER CAPABILITY (±8V at 5mA)
- "MASTER/SLAVES" SYNCHRONIZATION CAPABILITY
- INPUT OFFSET ADJUSTMENT
- LOW POWER (75mW)
- SINGLE 12V OR 15V SUPPLY OPERATION

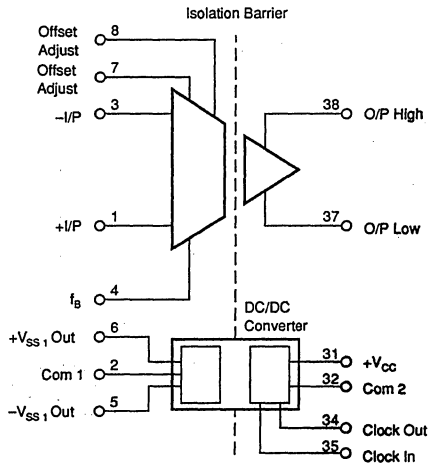
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL: Transducer Channel Isolator for Thermocouples, RTDs, Pressure Bridges, Flow Meters
- 4mA TO 20mA LOOP ISOLATION
- MOTOR AND SCR CONTROL
- GROUND LOOP ELIMINATION
- ANALYTICAL MEASUREMENTS
- POWER PLANT MONITORING
- DATA ACQUISITION/TEST EQUIPMENT ISOLATION
- MULTIPLEXED SYSTEMS WITH CHANNEL TO CHANNEL ISOLATION

DESCRIPTION

The ISO212P signal isolation amplifier is a member of a series of low-cost isolation products from Burr-Brown. The low-profile SIL plastic package allows PCB spacings of 0.5" to be achieved, and the small footprint results in efficient use of board space.

To provide isolation, the design uses high-efficiency, miniature toroidal transformers in both the signal and power paths. An uncommitted input amplifier and an isolated external bipolar supply ensure the majority of input interfacing or conditioning needs can be met. The ISO212P accepts an input voltage range of ±5V for single 15V supply operation or ±2.5V for single 12V supply operation.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-881B

SPECIFICATIONS

ELECTRICAL

At T = +25°C and V_{CC} = +15V unless otherwise noted.

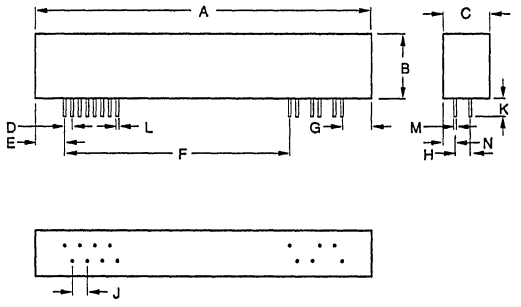
PARAMETER	CONDITIONS	ISO212JP			ISO212KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ISOLATION								
Voltage								
Rated Continuous								
AC, 60Hz	T_{MIN} to T_{MAX}	750			*			Vrms
DC	T_{MIN} to T_{MAX}	1060			*			VDC
100% Test (AC, 60Hz)	Partial Discharge 1s : <5pC	1200			*			Vrms
Isolation-Mode Rejection[1]	V_{ISO} = Rated Continuous 60Hz							
AC			115			*		dB
DC			160			*		dB
Barrier Resistance			10^{10}			*		Ω
Barrier Capacitance			12			*		pF
Leakage Current	V_{ISO} = 240Vrms, 60Hz		1	2		*	*	µArms
	V_{ISO} = 240Vrms, 50Hz			1.6			*	µArms
GAIN								
Initial Error			±1	±2		*	*	% FSR[2]
Gain vs Temperature			20	50		*	*	ppmFSR
Nonlinearity[3]	V_O = −5V to +5V		0.04	0.05		0.015	0.025	%FSR
INPUT OFFSET VOLTAGE								
Initial Offset	V_{IN} = 0V			±10 ±10/G			±7.5 ±7.5/G	mV
vs Temperature			±30 ±30/G			*		µV/°C
vs Power Supply[4]	V_{CC} = 14V to 16V		±1.5			*		mV/V
Adjustment Range		±20			*			mV
INPUT CURRENT								
Bias				50			*	nA
Offset				4			*	nA
INPUT								
Voltage Range [5]	Rated Operation G = 1	±5			*			V
OUTPUT								
Voltage Range	Out Hi to Out Lo Min Load = 1MΩ	±5			*			V
Ripple Voltage [6]	f = 0 to 100kHz		8			*		mVp-p
	f = 0 to 5kHz		0.4			*		mVrms
FREQUENCY RESPONSE								
Small Signal Bandwidth	I/P = 1Vp-p, −3dB G = 1		1			*		kHz
Full Signal Bandwidth	I/P = 10Vp-p, G = 1		200			*		Hz
ISOLATED POWER OUTPUTS								
Voltage Outputs ($\pm V_{SS\ 1}$) [7]	No Load	±7.5	±8		*	*		VDC
vs Temperature			−8			*		mV/°C
vs Load			90			*		mV/mA
Current Output [7]								
(Both Loaded)				5			*	mA
(One Loaded)				8			*	mA
POWER SUPPLIES								
Rated Voltage	Rated Performance		15			*		V
Voltage Range [5]		11.4		16	*		*	V
Quiescent Current	No Load		4.3	7		*	*	mA
TEMPERATURE RANGE								
Specification		0		+70	*		*	°C
Operating		−25		+85	*		*	°C

*Same as ISO212JP.

NOTES: (1) Isolation-mode rejection is the ratio of the change in output voltage to a change in isolation barrier voltage. It is a function of frequency. (2) FSR = Full Scale Range = 10V. (3) Nonlinearity is the peak deviation of the output voltage from the best-fit straight line. It is expressed as the ratio of deviation to FSR. (4) Power Supply Rejection is the change in V_{OS}/Supply Change. (5) At V_{CC} = +11.4V, input voltage range = ±2.5V min. (6) Ripple is the residual component of the barrier carrier frequency generated internally. (7) Derated at V_{CC} = +11.4V.

MECHANICAL

P Package —38-Pin Plastic SIP

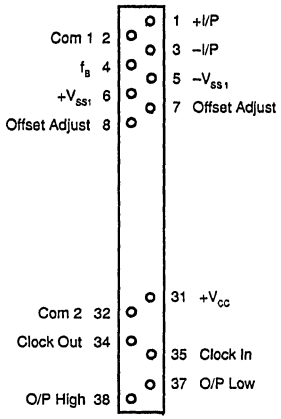


DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	56.39	57.05	2.220	2.246
B	10.54	11.76	0.415	0.463
C	7.49	8.26	0.295	0.325
D	1.27 TYP		0.050 TYP	
E	4.95 TYP		0.195 TYP	
F	38.10 TYP		1.500 TYP	
G	4.78 TYP		0.188 TYP	
H	2.54 TYP		0.100 TYP	
J	2.54 TYP		0.100 TYP	
K	3.18 TYP		0.125 TYP	
L	0.46 TYP		0.018 TYP	
M	0.25 TYP		0.010 TYP	
N	2.03	—	0.08	—

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

PIN CONFIGURATION

Bottom View



ABSOLUTE MAXIMUM RATINGS

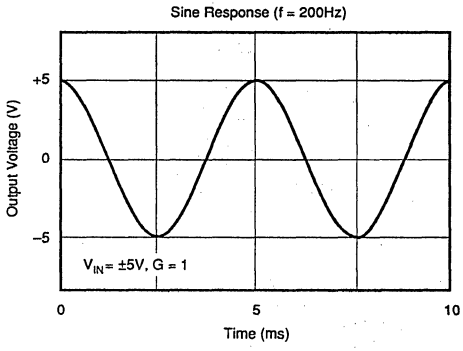
Supply Voltage Without Damage	18V
Continuous Isolation Voltage Across Barrier	750Vrms
Storage Temperature Range	−25°C to 100°C
Lead Temperature (soldering, 10s)	+300°C
Amplifier Output Short-Circuit Duration	Continuous to Common
Output Voltage Hi or Lo to Com 2	$\pm V_{CC}/2$

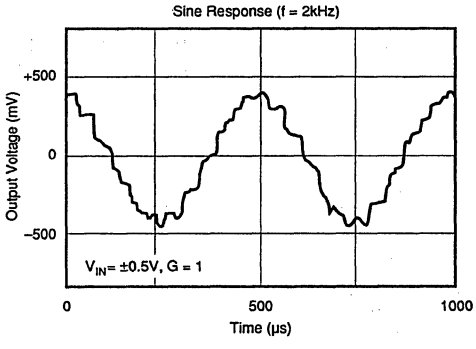
ORDERING INFORMATION

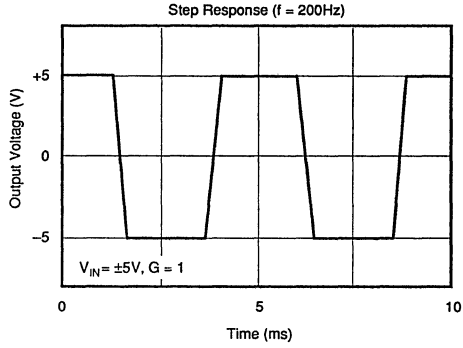
MODEL	PACKAGE	OPERATING TEMPERATURE RANGE
ISO212JP	Plastic SIP	−25°C to +85°C
ISO212KP	Plastic SIP	−25°C to +85°C

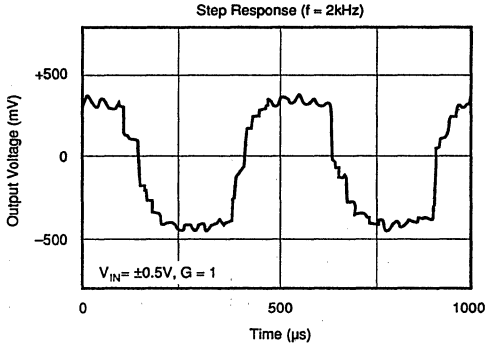
TYPICAL PERFORMANCE CURVES

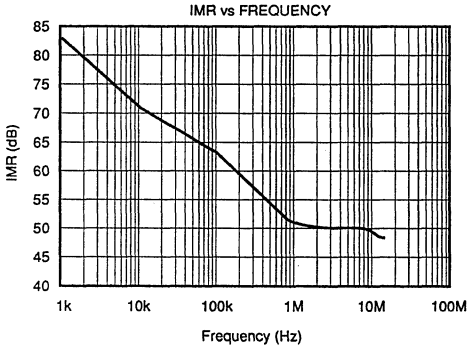
T_A = +25°C, V_S = ±15V unless otherwise noted.

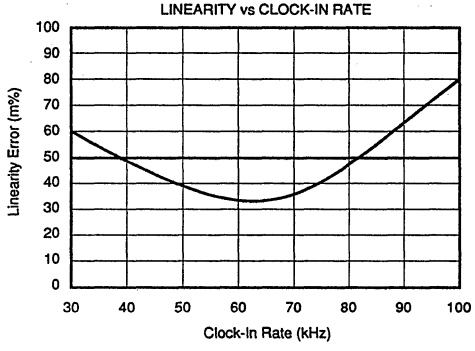






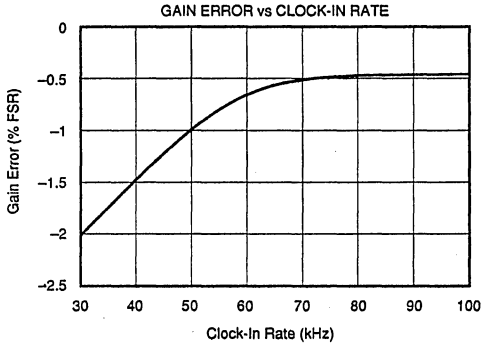






TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.



DISCUSSION OF SPECIFICATIONS

The ISO212P is intended for applications where isolation and input signal conditioning are required. Best signal-to-noise performance is obtained when the input amplifier gain setting is such that the f_B pin has a full scale range of ±5V. The bandwidth is internally limited to typically 1kHz, making the device ideal for use in conjunction with sensors that monitor slowly varying processes. To power external functions or networks, 5mA at ±8V typical is available at the isolated port.

LINEARITY PERFORMANCE

The ISO212P offers non-linearity performance compatible with 12-bit resolution systems (0.025%). Note that the specification is based on a best-fit straight line.

OPTIONAL OFFSET VOLTAGE ADJUSTMENT

In many applications, the untrimmed input offset voltage will be adequate. For situations where it is necessary to trim the offset, a potentiometer can be used. See Figure 1 for details. It is important to keep the traces to the offset adjust pins as short as practical, because noise can be injected into the input op amp via this route.

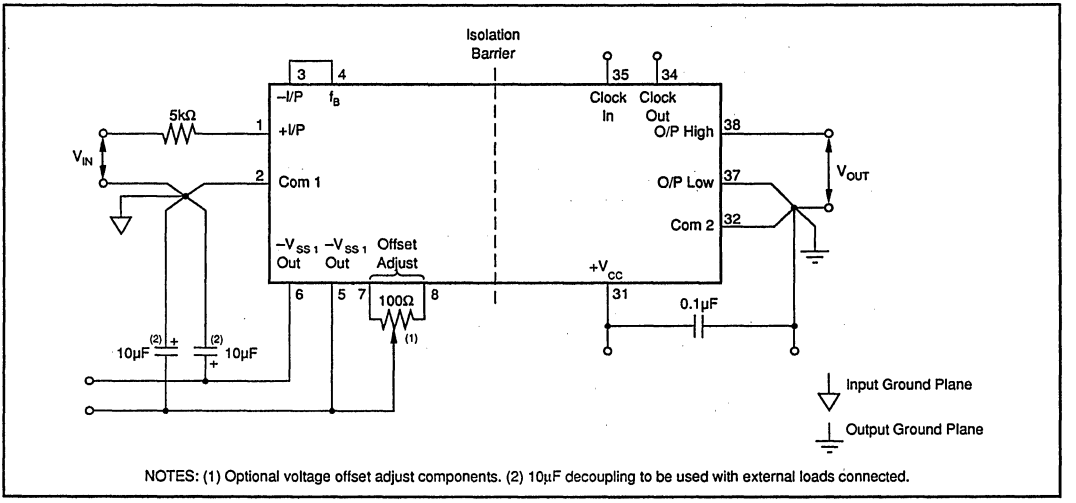
INPUT PROTECTION

If the ISO212P is used in systems where a transducer or sensor does not derive its power from the isolated power available from the device, then some input protection must be present to prevent damage to the input op amp when the ISO212P is not powered. A resistor of 5kΩ should be included to limit the output impedance of the signal source. Where the op amp is configured for an inverting gain, then R_{IN} of the gain setting network can be used. For non-inverting configurations, a separate resistor is required. Neglecting this point may also lead to problems when powering on the ISO212P.

USING ±V_{SS1} TO POWER EXTERNAL CIRCUITRY

The DC/DC converter in the ISO212P runs at a switching frequency of 25kHz. Internal rectification and filtering is sufficient for most applications at low frequencies or with no external networks connected.

The ripple on ±V_{SS1} will typically be 100mVp-p at 25kHz. Loading the supplies will increase the ripple unless extra filtering is added externally; a capacitor of 1µF is normally sufficient for most applications, although in some cases 10µF may be required. Noise introduced onto ±V_{SS1} should be decoupled to prevent degraded performance.



NOTES: (1) Optional voltage offset adjust components. (2) 10µF decoupling to be used with external loads connected.

FIGURE 1. Power Supply and Signal Connections Shown for Non-Inverting, Unity Gain Configuration.

THEORY OF OPERATION

The ISO212P has no galvanic connection between the input and output. The analog input signal referenced to the input common (Com 1) is multiplied by the gain of the input amplifier and accurately reproduced at the output. The output section uses a differential design so either the Hi or Lo pin may be referenced to the output common (Com 2). This allows simple input signal inversion while maintaining the high impedance input configuration. A simplified diagram of the ISO212P is shown in Figure 2. The design consists of a DC/DC converter, an uncommitted input operational amplifier, a modulator circuit and a demodulator circuit. Magnetic isolation is provided by separate transformers in the power and signal paths.

The DC/DC converter provides power and synchronization signals across the isolation barrier to operate the operational amplifier and modulator circuitry. It also has sufficient capacity to power external input signal conditioning networks. The uncommitted operational amplifier may be configured for signal buffering or amplification, depending on the application.

The modulator converts the input signal to an amplitude-modulated AC signal that is magnetically coupled to the demodulator by a miniature transformer providing the signal-path isolation. The demodulator recovers the input signal from the modulated signal using a synchronous technique to minimize noise and interference.

ABOUT THE BARRIER

For any isolation product, barrier integrity is of paramount importance in achieving high reliability. The ISO212P uses miniature toroidal transformers designed to give maximum isolation performance when encapsulated with a high-dielectric-strength material. The internal component layout is designed so that circuitry associated with each side of the barrier is positioned at opposite ends of the package. Areas where high electric fields can exist are positioned in the center of the package. The result is that the dielectric strength of the barrier typically exceeds 3kVrms.

ISOLATION VOLTAGE RATINGS

Because a long term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a high voltage for some shorter time. The relationship between actual test voltage and the continuous derated maximum specification is an important one. Historically, Burr-Brown has chosen a deliberately conservative one: V_{TEST} = (2 x ACrms continuous rating) + 1000V for ten seconds, followed by a test at rated ACrms voltage for one minute. This choice was appropriate for conditions where system transients were not well defined.

Recent improvements in high voltage stress testing have produced a more meaningful test for determining maximum permissible voltage ratings, and Burr-Brown has chosen to apply this new technology in the manufacture and testing of the ISO212P.

PARTIAL DISCHARGE

When an insulation defect such as a void occurs within an insulation system, the defect will display localized corona or ionization during exposure to high voltage stress. This ionization requires a higher applied voltage to start the discharge and a lower voltage to extinguish it once started. The higher start voltage is known as the inception voltage and the lower voltage is called the the extinction voltage. Just as the total insulation system has an inception voltage, so do the individual voids. A voltage will build up across a void until its inception voltage is reached. At this point, the void will ionize, effectively shorting itself out. This action redistributes electrical charge within the dielectric and is known as partial discharge. If the applied voltage gradient across the device continues to rise, another partial discharge cycle

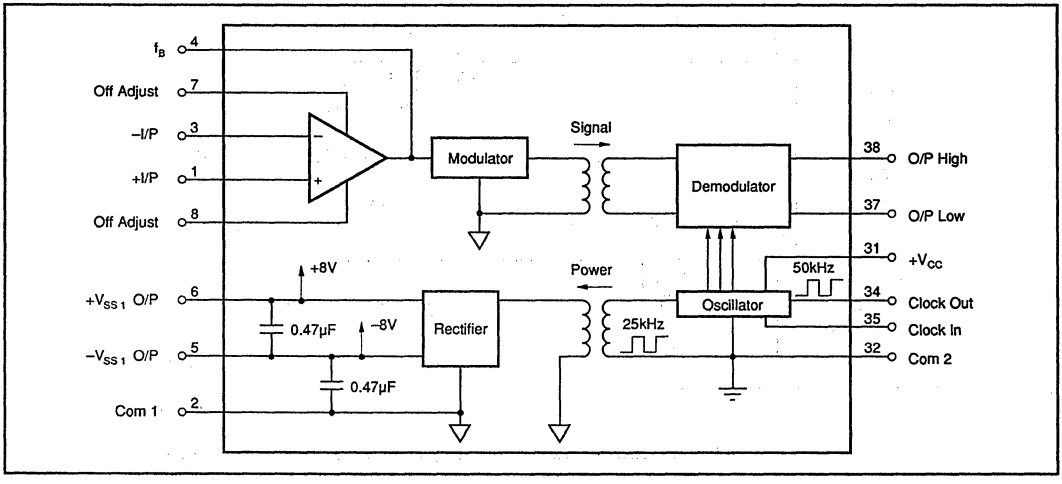


FIGURE 2. Simplified Diagram of Isolation Amplifier.

begins. The importance of this phenomenon is that if the discharge does not occur, the insulation system retains its integrity. If the discharge begins and is allowed to continue, the action of the ions and electrons within the defect will eventually degrade any organic insulation system in which they occur. The measurement of partial discharge is both useful in rating the devices and in providing quality control of the manufacturing process. The inception voltage of these voids tends to be constant, so that the measurement of total charge being re-distributed within the dielectric is a very good indicator of the size of the voids and their likelihood of becoming an incipient failure.

The bulk inception voltage, on the other hand, varies with the insulation system and the number of ionization defects. This directly establishes the absolute maximum voltage (transient) that can be applied across the test device before destructive partial discharge can begin.

Measuring the bulk extinction voltage provides a lower, more conservative, voltage from which to derive a safe continuous rating. In production, it's acceptable to measure at a level somewhat below the expected inception voltage and then de-rate by a factor related to expectations about the system transients. The isolation amplifier has been extensively evaluated under a combination of high temperatures and high voltage to confirm its performance in this respect. The ISO212P is free of partial discharges at rated voltages.

PARTIAL DISCHARGE TESTING IN PRODUCTION

Not only does this test method provide far more qualitative information about stress withstand levels than did previous stress tests, but it also provides quantitative measurements from which quality assurance and control measures can be based. Tests similar to this test have been used by some manufacturers such as those of high voltage power distribution equipment for some time, but they employed a simple measurement of RF noise to detect ionization. This method was not quantitative with regard to energy of the discharge and was not sensitive enough for small components such as isolation amplifiers. Now, however, manufacturers of HV test equipment have developed means to measure partial discharge, and VDE, the German standards group, has adopted use of this method for the testing of opto-couplers. To accommodate poorly defined transients, the part under test is exposed to a voltage that is 1.6 times the continuous rated voltage and must display <5pC partial discharge level in a 100% production test.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY AND SIGNAL CONNECTIONS

As with any mixed analog and digital signal component, correct decoupling and signal routing precautions must be used to optimize performance. Figure 1 shows the proper power supply and signal connections. V_{CC} should be bypassed to Com 2 with a 0.1µF ceramic capacitor as close to the device as possible. Short leads will minimize lead inductance. A ground plane will also reduce noise problems. If a low impedance ground plane is not used, signal common lines, and either O/P High or O/P Low pin should be tied directly to the ground at the supply and Com 2 returned via a separate trace to the supply ground.

To avoid gain and isolation mode (IMR) errors introduced by the external circuit, connect grounds as indicated in Figure 3. Layout practices associated with isolation amplifiers are very important. In particular, the capacitance associated with the barrier, and series resistance in the signal and reference leads, must be minimized. Any capacitance across the barrier will increase AC leakage and, in conjunction with ground line resistance, may degrade high frequency IMR.

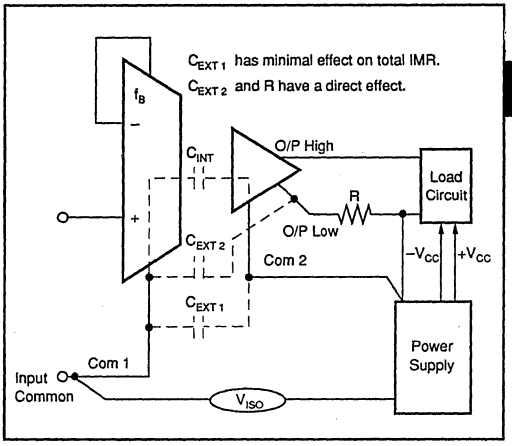


FIGURE 3. Technique for Connecting Com 1 and Com 2.

VOLTAGE GAIN MODIFICATIONS

The uncommitted operational amplifier at the input can be used to provide gain, signal inversion, active filtering or current to voltage conversion. The standard design approach for any op-amp stage can be used, provided that the full scale voltage appearing on f_B does not exceed ±5V.

If the input op-amp is overdriven, ripple at the output will result. To prevent this, the feedback resistor should have a minimum value of 10kΩ.

Also, it should be noted that the current required to drive the equivalent impedance of the feedback network is supplied by the internal DC/DC converter and must be taken into account when calculating the loading added to $\pm V_{SS\,1}$.

Since gain inversion can be incorporated in either the input or output stage of the ISO212P, it is possible to use the input amplifier in a non-inverting configuration and preserve the high impedance this configuration offers. Signal inversion at the output is easily accomplished by connecting O/P High to Com 2 instead of O/P Low.

ISOLATED POWER OUTPUT DRIVE CAPABILITY

On the input side of the ISO212P, there are two power supplies capable of delivering 5mA at ±8V to power external circuitry. When using these supplies with external loads, it is recommended that additional decoupling in the form of 10µF tantalum bead capacitors be added to improve the voltage regulation. Loss of linearity will result if additional filtering is not used with an output load. Again, power dissipated in the feedback loop around the input op amp must be subtracted from the available power output at $\pm V_{SS1}$.

If the ISO212P is to be used in multiple applications, care should be taken in the design of the power distribution network, especially when all ISO212Ps are synchronized. It is best to use a well decoupled distribution point and to take power to individual ISO212Ps from this point in a star arrangement as shown in Figure 4.

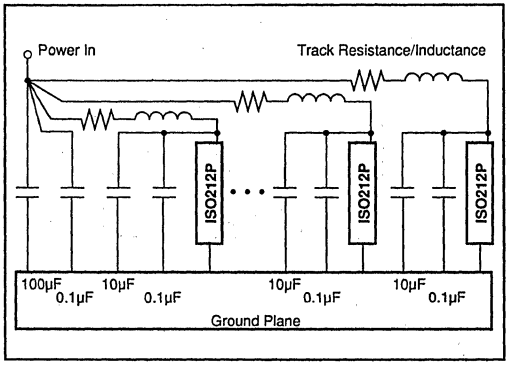


FIGURE 4. Recommended Decoupling and Power Distribution.

NOISE

Output noise is generated by residual components of the 25kHz carrier that have not been removed from the signal. This noise may be reduced by adding an output low pass filter (see Figure 8). The filter time constants should be set below the carrier frequency. The output from the ISO212P is a switched capacitor and requires a high impedance load to prevent degradation of linearity. Loads of less than 1MΩ will cause an increase in noise at the carrier frequency and will appear as ripple in the output waveform. Since the output signal power is generated from the input side of the barrier, decoupling of the $\pm V_{SS1}$ outputs will improve the signal to noise ratio.

SYNCHRONIZATION OF THE INTERNAL OSCILLATOR

The ISO212P has an internal oscillator and associated timing components, which can be synchronized, incorporated into the design. This alleviates the requirement for an external high-power clock driver. The typical frequency of oscillation is 50kHz. The internal clock will start when power is applied to the ISO212P and Clk In is not connected.

Because the frequencies of several ISO212Ps can be marginally different, "beat" frequencies ranging from a few Hz to a few kHz can exist in multiple amplifier applications. The design of the ISO212P accommodates "internal synchronous" noise, but a synchronous beat frequency noise will not be strongly attenuated, especially at very low frequencies if it is introduced via the power, signal, or potential grounding paths. To overcome this problem in systems where several ISO212Ps are used, the design allows synchroniztion of each oscillator in a system to one frequency. Do this by forcing the timing node on the internal oscillator with an external driver connected to Clk In. See Figure 5. The driver may be an external component with Series 4000 CMOS characteristics, or one of the ISO212Ps in the system can be used as the master clock for the system. See Figure 6 and 7 for connections in multiple ISO212P installations.

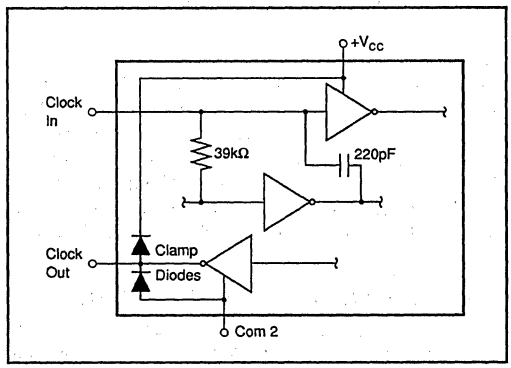


FIGURE 5. Equivalent Circuit, Clock Input/Output. Inverters are CMOS.

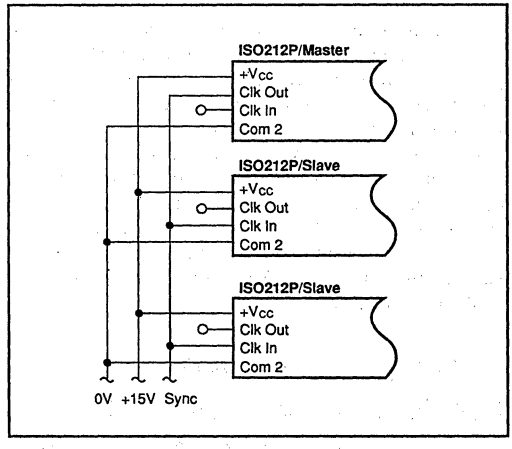


FIGURE 6. Oscillator Connections for Synchronous Operation in Multiple ISO212P Installations.

CHARGE ISOLATION

When more than one ISO212P is used in synchronous mode, the charge which is returned from the timing capacitor (220pF in Figure 5) on each transition of the clock becomes

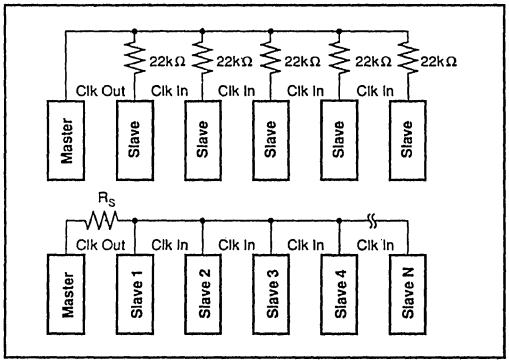


FIGURE 7. Isolating the Clk Out Node.

significant. Figure 7 illustrates a method of isolating the "Clk Out" clamp diodes (Figure 5) from this charge.

A 22kΩ resistor (recommended maximum to use) together with the 39kΩ internal oscillator timing resistor (Figure 5) forms a potential divider. The ratio of these resistors should be greater than 0.6 which ensures that the input voltage triggers the inverter connected to "Clk In". If using a single resistor, then account must be taken of the paralleled timing resistors. This means that the 22kΩ resistor must be halved to drive two ISO212Ps, or divided by 8 if driving 8 ISO212Ps to insure that the ratio of greater than 0.6 is maintained. The series resistors shown in Figure 7 reduce the high frequency content of the power supply current.

APPLICATIONS

The ISO212P isolation amplifier, together with a few low cost components, can isolate and accurately convert a 4-to-20mA input to a ±10V output with no external adjustment. Its low height (0.43" (11mm)) and small footprint (2.5" x 0.33" (57mm x 8mm)) make it the solution of choice in 0.5" board spacing systems and in all applications where board area savings are critical.

The ISO212P operates from a single +15V supply and offers low power consumption and 12-bit accuracy. On the input side, two isolated power supplies capable of supplying 5mA at ±8V are available to power external circuitry.

APPLICATIONS FLEXIBILITY

In Figure 8, the ISO212P's $+V_{ss\,1}$ isolated supply powers a REF200 to provide an accurate 100µA current source. This current is opposed by an equal but opposite current through the 75kΩ feedback resistor to establish an offset of –7.5V at I_{in} = 0mA. With I_{in} = 4-to-20mA, the output is –5 to +5V. The ratio of the 75kΩ and 3.12kΩ resistors assures the correct gain.

The polarity of the output can be reversed by simply reversing the O/P HI and O/P LO pins. This could be used in the Figure 8 circuit to change the –5V to +5V output to a +5V to –5V output range.

The primary function of the output circuitry is to add gain to produce a ±10V output and to reduce output impedance. The addition of a few resistors and capacitors provides a low pass filter with a cut-off frequency equal to the full signal bandwidth of the ISO212P, typically 200Hz. The filter response is flat to 1dB and rolls off from cut off at –12dB per octave.

The accuracy of the REF200 and external resistors eliminates the need for expensive trim pots and adjustments. The errors introduced by the external circuitry only add about 10% of the ISO212P's specified gain and offset voltage error.

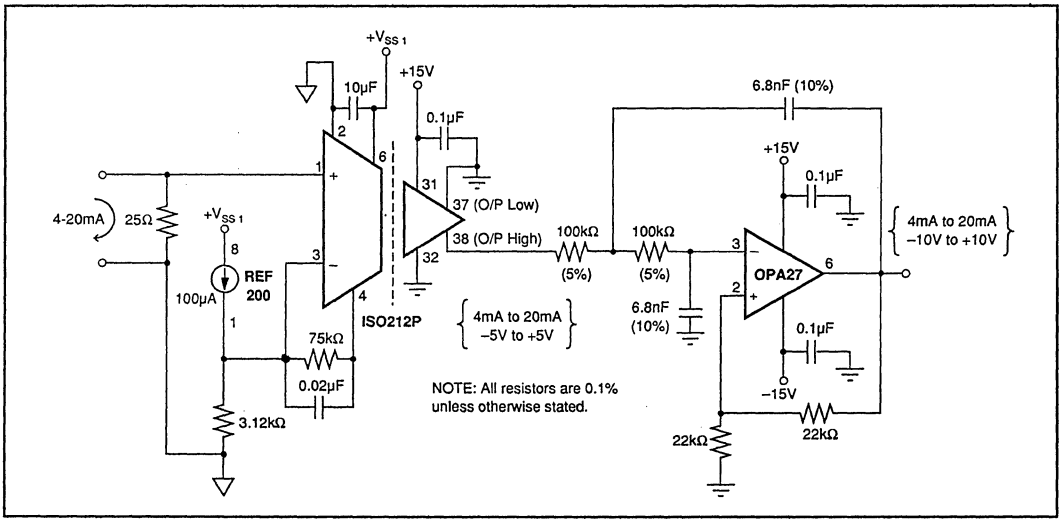


FIGURE 8. Isolated 4-20mA Current Receiver with Output Filter.

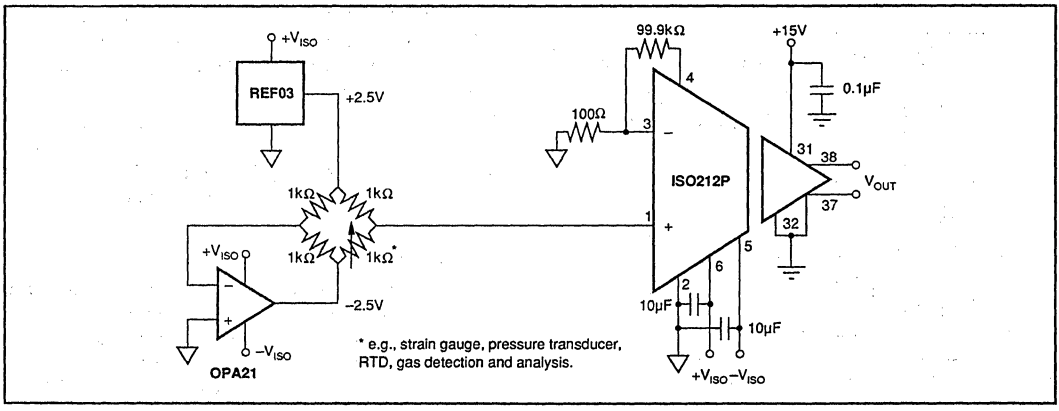


FIGURE 9. Instrument Bridge Isolation Amplifier.

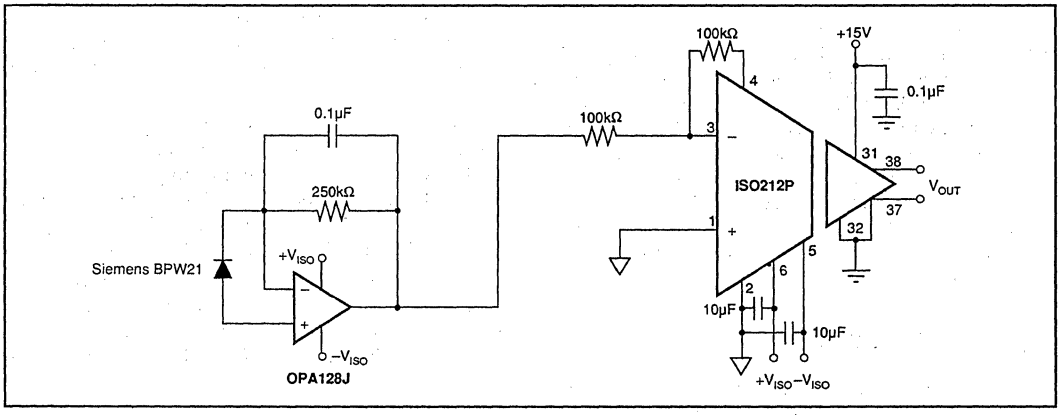


FIGURE 10. Photodiode Isolation Amplifier.

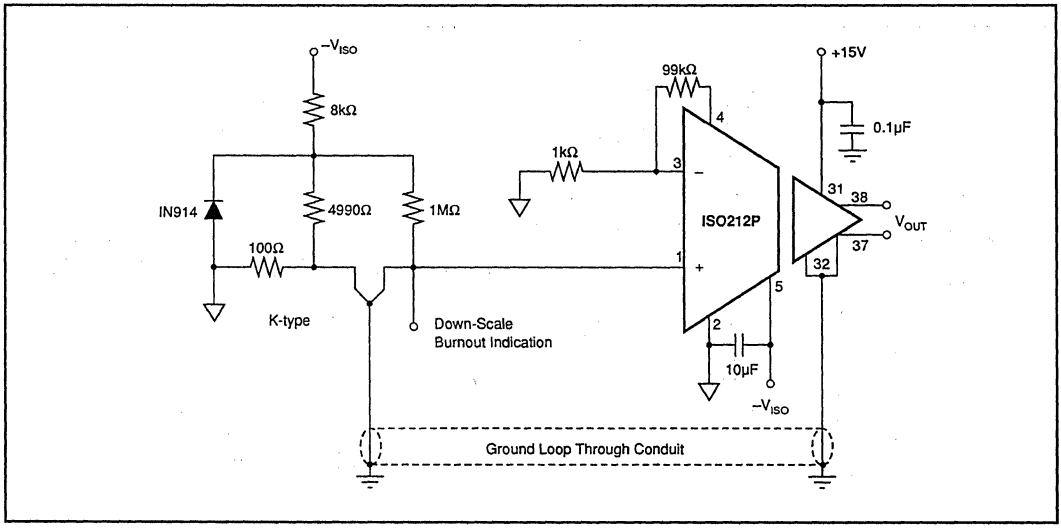


FIGURE 11. Thermocouple Amplifier with Ground Loop Elimination, Cold Junction Compensation and Down-Scale Burn-Out.

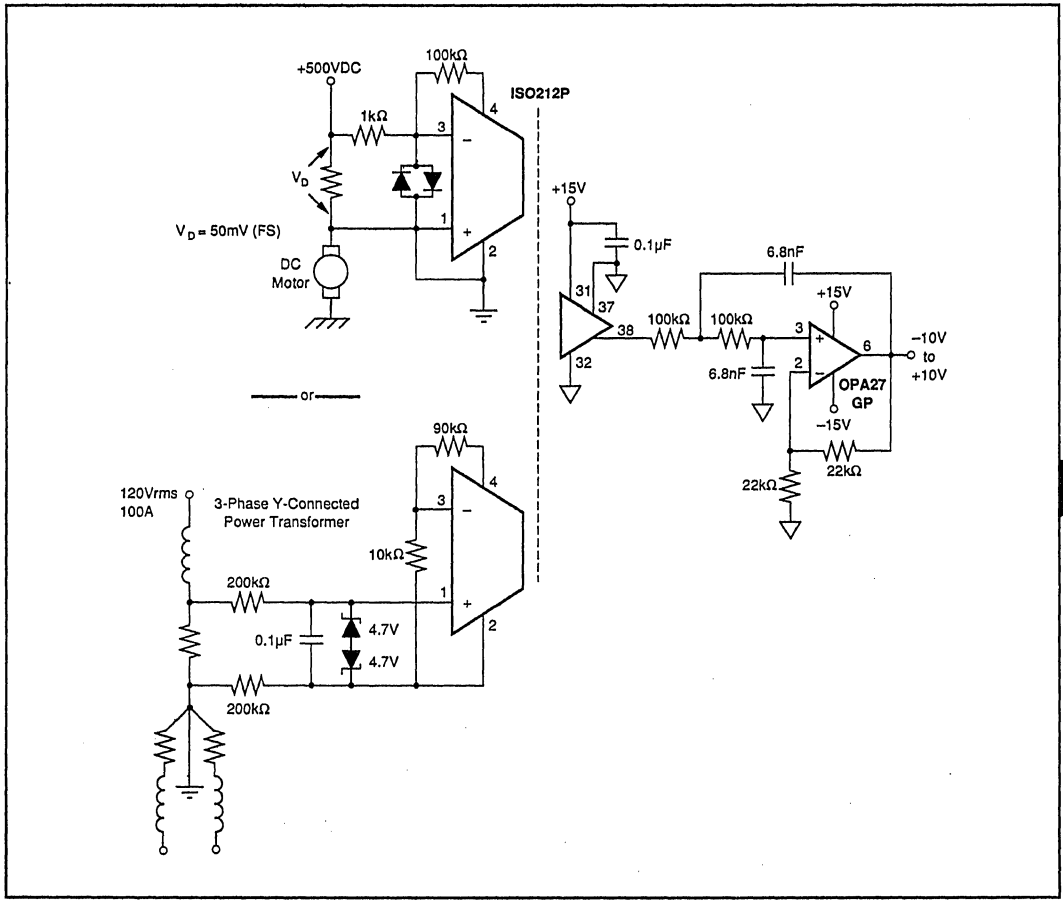


FIGURE 12. Isolated Current Monitoring Applications.

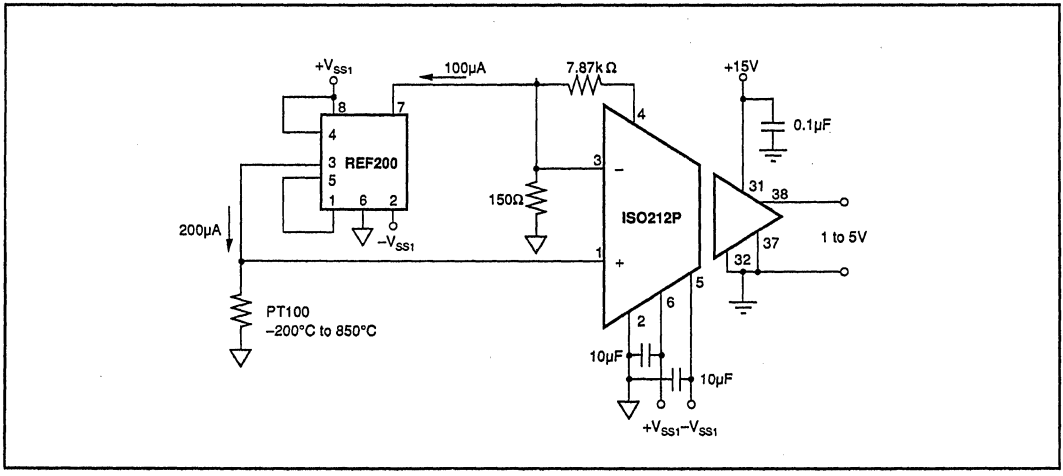


FIGURE 13. Isolated temperature Sensing and Amplification.

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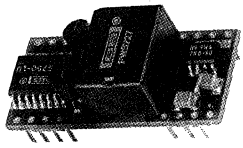


PWS727
PWS728

Isolated, Unregulated DC/DC CONVERTERS

FEATURES

- 100% TESTED FOR HIGH VOLTAGE BREAKDOWN
- COMPACT (28-pin DIP)
- 5V OR 15V INPUT OPTIONS
- SYNCHRONIZABLE (TTL)

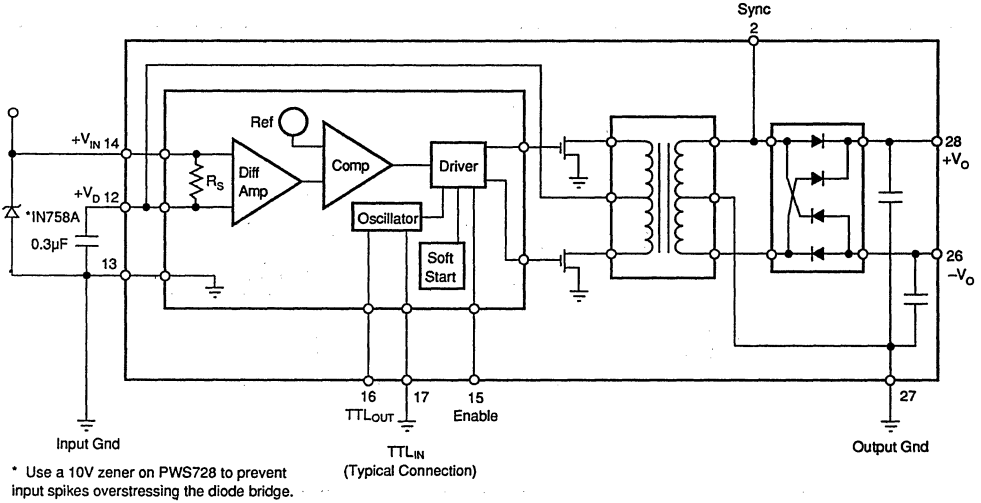
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- GROUND LOOP ELIMINATION
- POINT-OF-USE ANALOG POWER

DESCRIPTION

The PWS727 is a DC/DC converter which uses minimal PC board space and converts a single input 10 to 18VDC to bipolar voltages of the same value as the input. The PWS728 converts a 4.7 to 6VDC to bipolar voltages three times the value of the input. The converters are capable of providing ±15mA (PWS727) or ±12mA (PWS728) at rated voltage and up to ±30mA.

The PWS727 and PWS728 use a high-frequency (800kHz nominal) surface mount oscillator that makes it possible to minimize the transformer size. The transformer is composed of a split bobbin isolation transformer using a ferrite core and is encapsulated in a plastic package, allowing a higher isolation voltage rating. The design minimizes high frequency radiated noise on the output by using a ground plane directly under the high frequency components.



* Use a 10V zener on PWS728 to prevent input spikes overstressing the diode bridge.

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PDS-987

SPECIFICATIONS

ELECTRICAL

At V_{IN} =15VDC, Output Load = ±15mA (PWS727) and T_A = +25°C unless otherwise noted. Or V_{IN} = 5VDC, Output Load = ±12mA (PWS728) and T_A = +25°C unless otherwise noted

PARAMETER	CONDITIONS	PWS727 MIN	PWS727 TYP	PWS727 MAX	PWS728 MIN	PWS728 TYP	PWS728 MAX	UNITS
ISOLATION								
Voltage Rated Continuous AC 60Hz		750			•			Vrms
100% Test[1]	60Hz, 1s, <5pC PD	1200			•			Vrms
Barrier Impedance			10^{12} || 8			•		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms, 60Hz		1	1.5		•	•	µArms
INPUT								
Rated Voltage			15			5		V
Voltage Range		10		18	4.5		6	V
Current			55	65		110	130	mA
Current Ripple			2.5			7.5		mAp-p
Current Limit				250			•	mAp-p
TTL_{IN}, I_{IH}				10			•	nA
I_{IL}			–1			•		µA
V_{IH}		2.0			•			V
V_{IL}				.8			•	V
Frequency Range		1		2.5	•		•	MHz
TTL_{OUT}, I_{OL}				15			15	mA
OUTPUT								
Rated Output Voltage		14.25	15.0	15.75	•	•	•	VDC
Current			15	30		12	30	mA
Regulation								
(single ended load change)	$+I_O$ = 7.5 –15mA, $–I_O$ = 15mA		45			135		mV/mA
Sensitivity	V_{IN} = 10 to 18 V		1.13			3.8		V/V
Balance				15			25	mV
Ripple Voltage	At Switching Frequency		10			•		mVpp
Output Switching Noise	>800kHz		20			•		mVpp
Output Voltage Temp Coefficient			.05			•		V/°C
Sync	Loading			20 || 40			•	kΩ || pF
Sync Frequency[2]		725	800	875	•		•	kHz
TEMPERATURE RANGE								
Specification		0		70			•	°C
Operation		–40		85			•	°C
Storage		–40		85			•	°C

NOTE: (1) Tested at 1.6 x rated, fail on 5pC partial discharge leakage current on 5 successive pulses. (2) Nominal with pin 17 grounded.

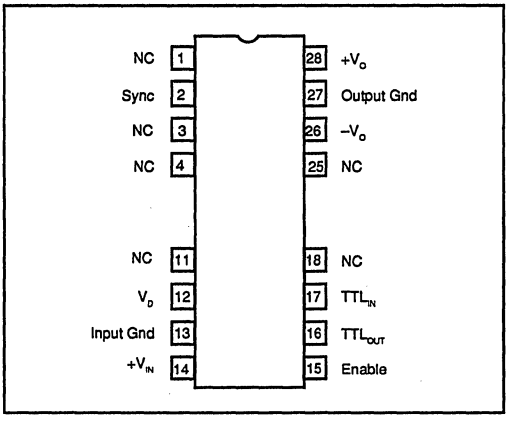
ORDERING INFORMATION

Basic Model Number	PWS727 PWS728

ABSOLUTE MAXIMUM RATINGS

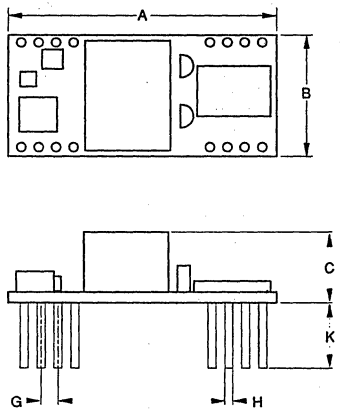
Supply Voltage	18V
Continuous Isolation Voltage	750Vrms
Junction Temperature	+150°C
Storage Temperature	85°C
Lead Temperature (Solder, 10s)	300°C
Output Short to Common	Continuous
Max Load, Sum of Both Outputs	60mA

PIN CONFIGURATION



MECHANICAL

28-Pin Double — Wide DIP



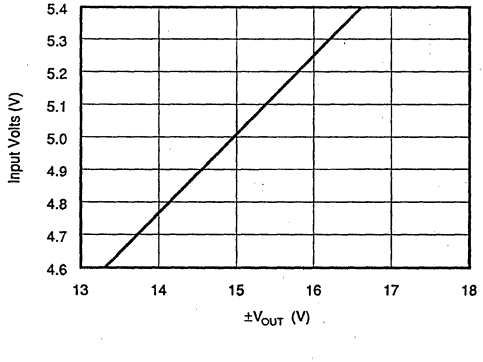
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.440	1.460	36.58	37.08
B	.690	.710	17.53	18.03
C	.390	.410	9.91	10.41
G	.100 BASIC		2.54 BASIC	
H	.020 BASIC		0.51 BASIC	
K	.190	.210	4.83	5.33
L	.600 BASIC		15.24 BASIC	

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

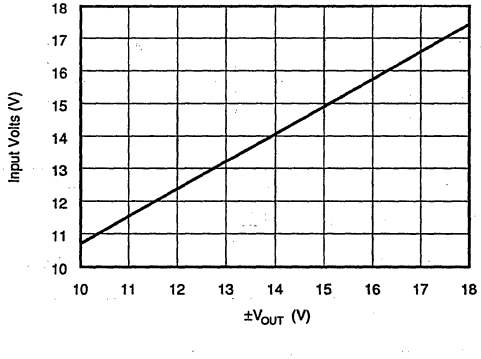
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{IN} = 15VDC, I_{LOAD} = ±15mA (PWS727), or V_{IN} = 5VDC, output load = ±12mA (PWS728) unless otherwise noted.

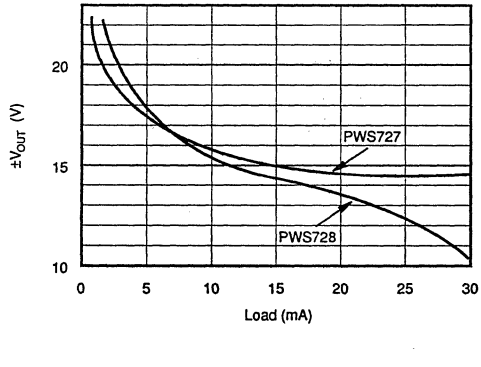
PWS728 LINE REGULATION



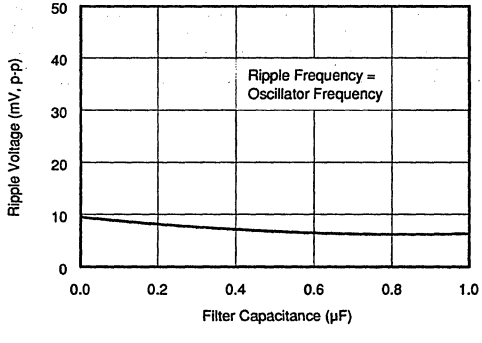
PWS727 LINE REGULATION



PWS727 AND PWS728 LOAD LINES

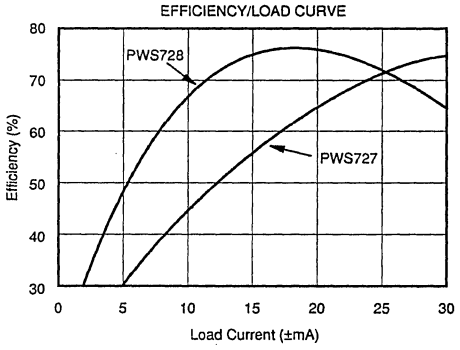


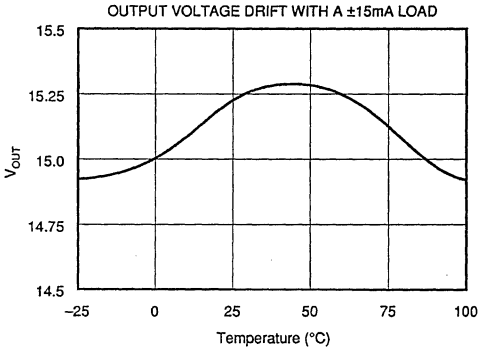
OUTPUT RIPPLE VOLTAGE

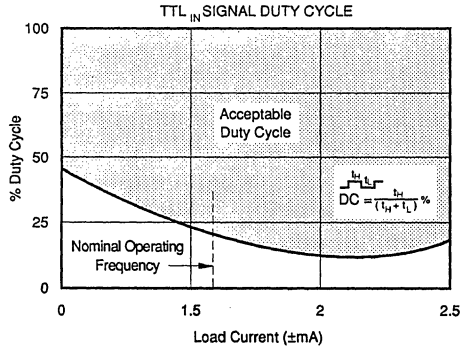


TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{IN} = 15VDC, I_{LOAD} = ±15mA (PWS727), or V_{IN} = 5VDC, output load = ±12mA (PWS728) unless otherwise noted.







THEORY OF OPERATION

The PWS727 and PWS728 are composed of the PWS750 building blocks which are assembled along with some standard components to build an isolated push pull DC/DC converter.

PWS727 AND PWS728 PIN FUNCTIONS

TTL_{IN} is used to optionally control the frequency of the oscillator with an external TTL level frequency source. The input frequency must be twice the desired driver frequency, since there is an internal divide by 2 circuit to produce a 50% duty cycle output. The input duty cycle can vary from 12% to 95%, (see the Typical Performance Curves). **When in the free running mode the TTL_{IN} pin must be tied to ground.**

TTL_{OUT} is used to synchronize the outputs of multiple PWS727s and/or PWS728s to minimize beat frequency problems if desired. A standard open collector output is provided, therefore a 330 to 3.3kΩ resistor will be necessary, depending on the amount of stray capacitance on the TTL_{IN} line. A maximum of 8 PWS727s or PWS728s can be connected without the use of an external TTL buffer. Connect the TTL_{OUT} of a master unit to the TTL_{IN} of the slave units.

An Enable pin is provided so that the driver can be shut down to minimize power use if required. A TTL low applied to the pin will shut down the driver within one cycle (1.25µs). A TTL high will enable driver outputs within one cycle. The TTL_{OUT} will still have an 800kHz signal when a master driver is disabled, so other synchronized drivers will not be shut down. The pin can be left open for normal operation.

The $+V_{IN}$ pin supplies power to the converter. The V_D pin connects the power to the transformer through the internal overcurrent sense resister. The other end of the overcurrent sense resister is tied to $+V_{IN}$. A 0.3µF bypass capacitor must be connected to the V_D pin to reduce the ripple current through the shunt resistor, otherwise false current limit conditions can occur due to ripple voltage peaks. During overload conditions the output drive shuts off for approximately 80µs, then turns back on for 20µs, resulting in a 25% power up duty cycle. If the overload condition still exists, then the output will shut off again. When the fault or the excessive load is removed, the converter resumes normal operation.

The Sync pin can be used to synchronize the internal oscillator of an ISO120 to the operating frequency of the converter. The Sync pin is connected directly to the secondary of the transformer, so an 800kHz square wave of twice the output magnitude is present. Minimum pc board trace length should be used to minimize loading the transformer. When making the connection to the ISO120, a simple frequency divider circuit (see Figure 3) is necessary to match the 400kHz nominal frequency required by the ISO120. If this function is not used, leave the pin disconnected.

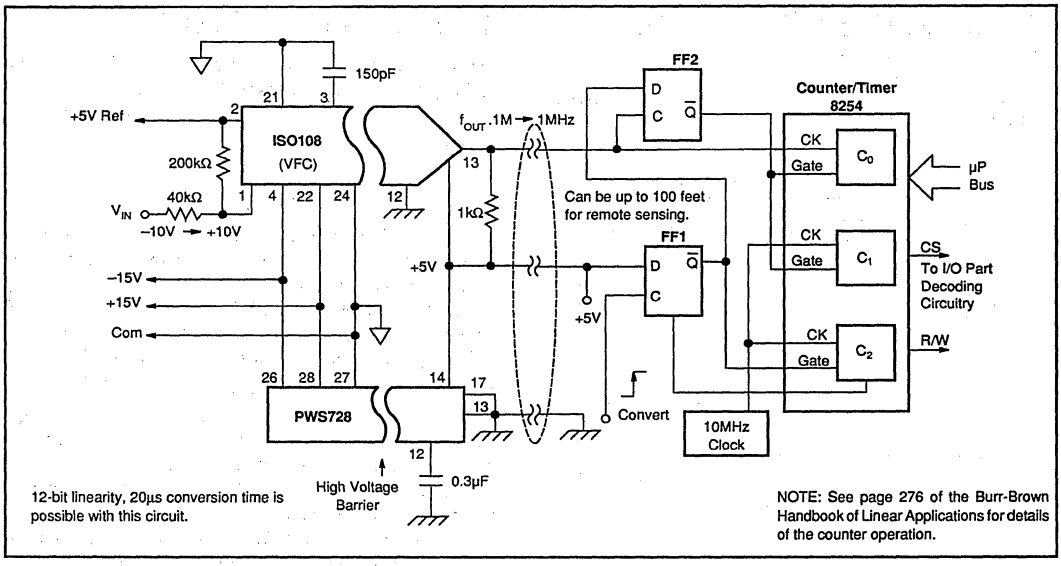


FIGURE 1. Isolated Integrated A/D Conversion System Using Ratiometric Counting and Microprocessor Interface, Operating from a Single 5V Supply.

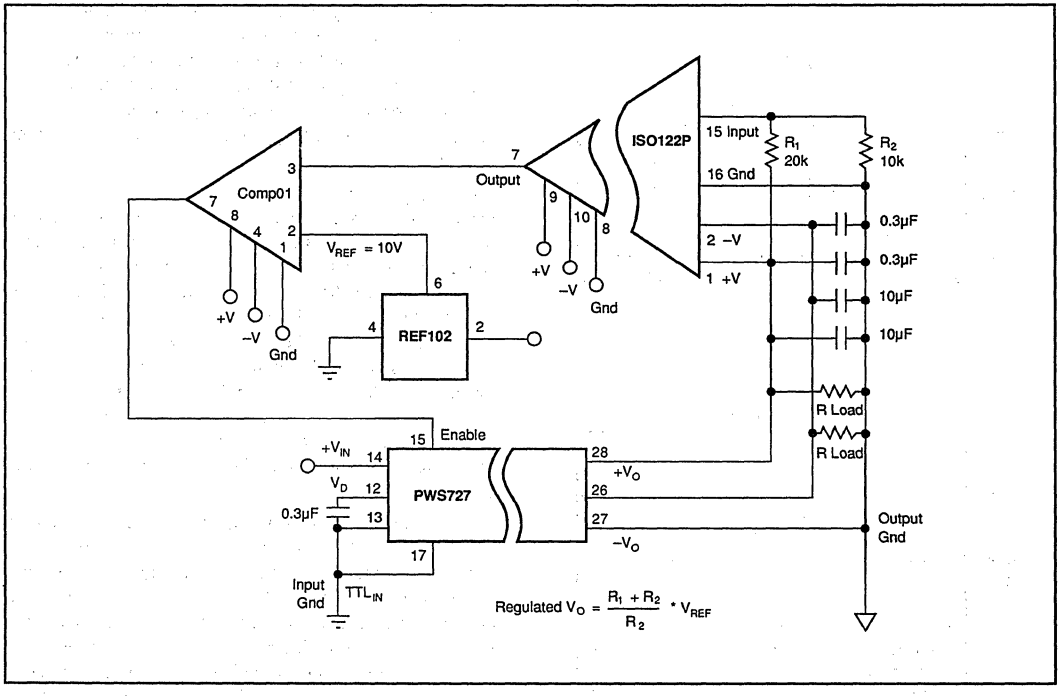


FIGURE 2. Regulated Output Using the Enable Pin to Cycle the Converter Output On and Off.

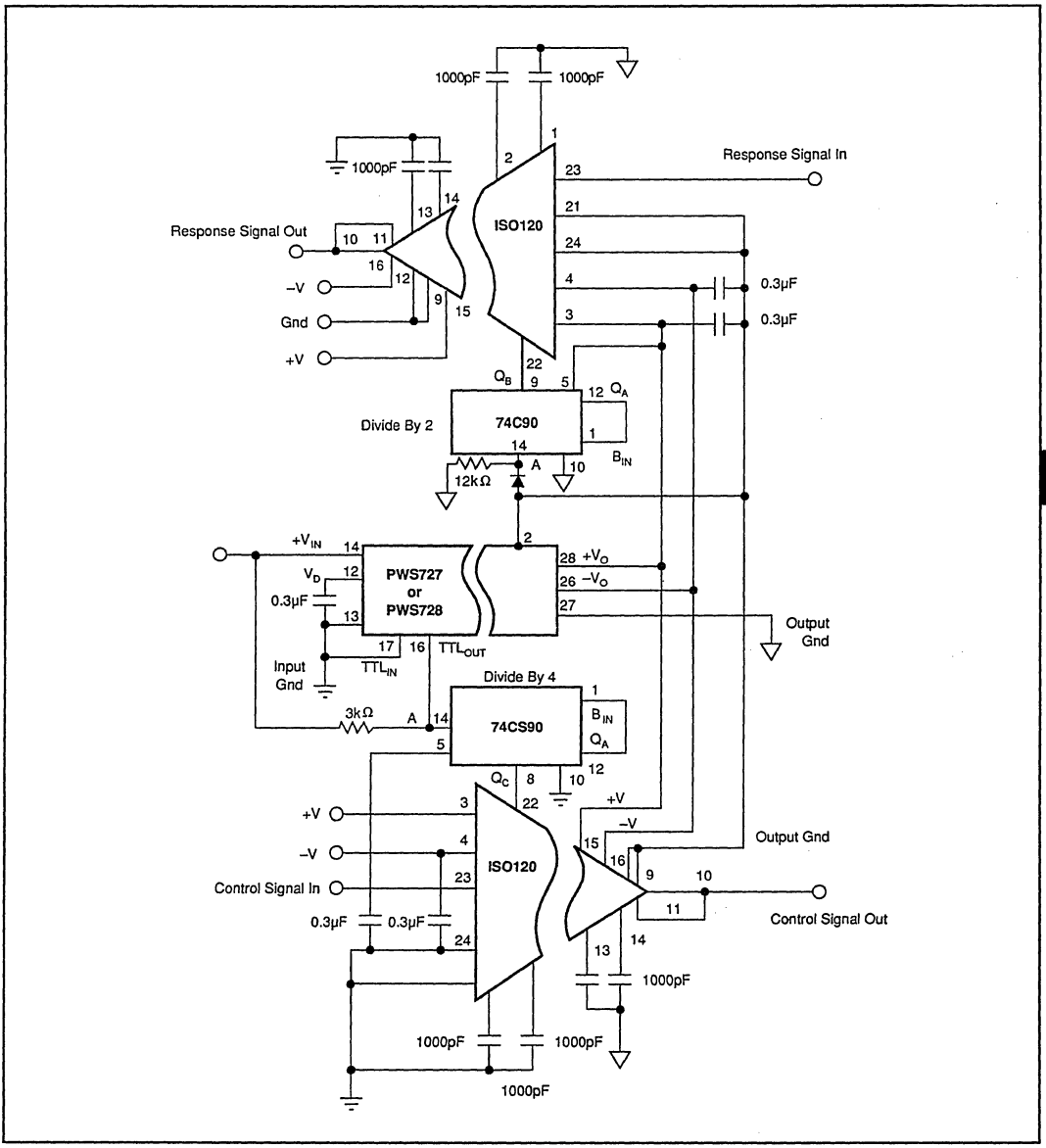


FIGURE 3. The PWS727 or PWS728 Can Be Used to Synchronize the ISO120. The Output Sync Must be Divided by 2 and the TTL_{OUT} Must Be Divided by 4.

BASIC OPERATION

PC BOARD LAYOUT CONSIDERATIONS

These converters have low output ripple so that standard layout methods are all that is necessary for good circuit performance. Bypass capacitors should be placed close to each device powered by the converters. To minimize the noise pickup by sensitive (12 bit resolution) circuits, a 10Ω resistor can be placed in series with the isolated power traces. The resistor in conjunction with the bypass capacitor acts as a low pass filter, to minimize isolation amplifier PSRR related ripple voltage feedthrough. A π filter can also be used at the input ($+V_{IN}$) to minimize input supply ripple current.

5V OPERATION

With 5V operation (PWS728) the transformer winding ratio is 3:1, therefore generating much greater currents in the primary. The input ripple will be larger, so an input π filter will be necessary to isolate the supply noise from the rest of the circuit. For example, when the output load is ± 15mA the input current will be approximately 120mA.

OUTPUT CURRENT RATING

The PWS727 and PWS728 contain soft start circuitry to protect the FETs from high inrush currents during turn on. The internal input current limit is 250mA peak to prevent thermal overload of the MOSFETs. The maximum output current rating is ±30mA. Total current, which can be drawn from each isolation channel, is the total of the of the power being drawn from both the +V and –V outputs. For example, if one output is not used, then maximum current can be drawn from the other output. In all cases the maximum current that can be drawn from any individual channel is:

$$(+I_{OUT}) + (-I_{OUT}) < 60mA$$

It should be noted that many analog circuit functions do not simultaneously draw equal current from both the positive and negative supplies.

HIGH VOLTAGE TESTING

Burr Brown Corporation has adopted a partial discharge test criterion that is similar to the German VDE0884 optocoupler standard. This method requires that less than 5pC partial discharge across the isolation barrier with 1200 Vrms 60Hz applied. This criterion confirms transient overvoltage (1.6 x 750 Vrms) protection without damage to the PWS727 or PWS728. Lifetest results verify the absence of high-voltage breakdown under continuous rated voltage and maximum temperature.

The minimum AC barrier voltage that initiates partial discharge above 5pC is defined as the "inception voltage". Decreasing the barrier voltage to a lower level is required before partial discharge ceases and is known as "extinction voltage". We have developed a package insulation system to yield an inception voltage greater than 1200 Vrms so that transient voltages below this level will not damage the isolation barrier. The extinction voltage is above 750 Vrms so that even overvoltage-induced partial discharge will cease once the barrier voltage is reduced to the rated value. Previous high voltage test methods relied on applying a large enough overvoltage (above rating) to break down marginal devices, but not so high as to damage good ones. Our partial discharge testing gives us more confidence in barrier reliability than breakdown/no breakdown criteria.

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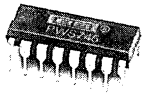


PWS745

ADVANCE INFORMATION
SUBJECT TO CHANGE

OSCILLATOR/DRIVER & TRANSFORMERS

FEATURES

- LOW POWER CONSUMPTION
- COMPACT SIZE
- EASE OF USE
- DRIVES UP TO 8 DC/DC CHANNELS
- 750VAC ISOLATION
- OPTIONAL 5V TO ±15V AND 15V TO ±15V TRANSFORMERS
- COMPATIBLE WITH PWS740 AND PWS750 COMPONENTS
- 0 to +85°C

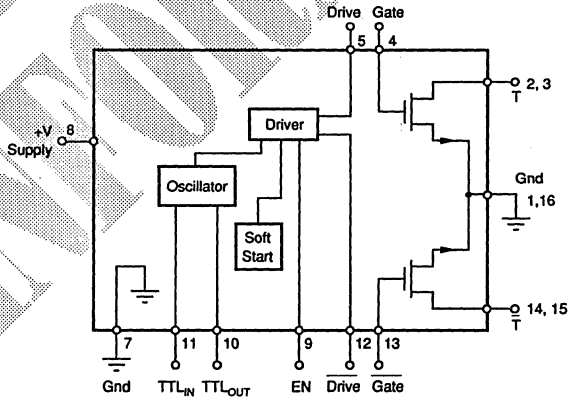
APPLICATIONS

- INDUSTRIAL CONTROL
- PROCESS CONTROL
- FACTORY AUTOMATION
- GROUND LOOP ELIMINATION

DESCRIPTION

The PWS745 provides driver and switching FETs in a 16-pin DIP package for use in multichannel DC/DC converter applications. The switching MOSFETs are built into the driver to allow simple low cost assembly of the multichannel converter. Additionally the PWS745-1 is capable of operating at 5V and can be easily synchronized with TTL level signals. The transformers are through-hole PC-board-mount versions of the popular PWS750 surface mount design. The PWS745-2 is a 15V to ±15V version, while the PWS745-4 is the 5V to ±15 version.

The small size is achieved by using the multiple chip transfer molding process that has been successfully used with the ISO122P. The power components are mounted directly on the copper lead frame, utilizing two pins for each die pad to maximize heat sink area. PWS745-1 may also be used in place of the PWS740-1 or PWS750-1 drivers, where through-hole technology is required at the driver location.



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PDS-1082

SPECIFICATIONS

ELECTRICAL

At V_{IN} =15 VDC, Output Load = ±15mA (PWS745-2) and T_A = +25°C unless otherwise noted.
Or V_{IN} = 5 VDC, Output Load = ±12mA (PWS745-4) and T_A = +25°C unless otherwise noted

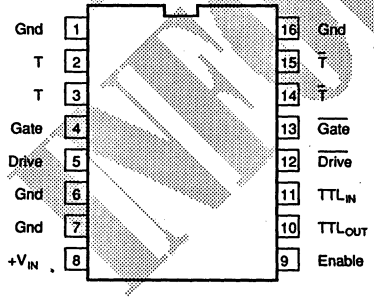
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PWS745-U OSCILLATOR/DRIVER					
Frequency: Internal Oscillator	TTI_{IN} = 0V	550	600	650	kHz
External Oscillator		800	1200	1600	kHz
Supply: 15V Operation		10	15	18	V
5V Operation		4.5	5	5.5	V
Current	No Load		10		mA
	Max Load		750		mA
Current Ripple	C_{BYPASS} = 1uF		2.5		mAp-p
TTL_{IN}, I_{IH}				10	nA
I_{IL}			−1		µA
V_{IH}		2			V
V_{IL}				0.8	V
Frequency		0.8		1.6	MHz
TTL_{OUT}, IOL				15	mA
Frequency		550	600	650	kHZ
PWS745-2					
Voltage Rated Continuous AC 60Hz		750			Vrms
100% Test (1)	60Hz, 1s, <5PC PD	1200			Vrms
Barrier Impedance			10^{12} || 8		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms, 60Hz			1.5	µArms
PWS745-4					
Voltage Rated Continuous AC 60Hz		750			Vrms
100% Test (1)	60Hz, 1s, <5PC PD	1200			Vrms
Barrier Impedance			10^{12} || 8		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms, 60Hz			1.5	µArms
TEMPERATURE RANGE					
Specification		−40		85	°C
Operation		−40		85	°C
Storage		−40		85	°C

NOTES: (1) Tested at 1.6 x rated, fail on 5PC partial discharge leakage current on 5 successive pulses.

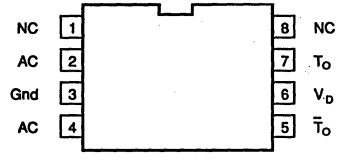
PIN CONFIGURATION

Top View Plastic 16-Pin DIP

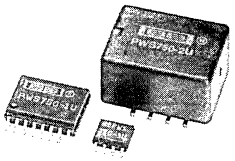
PWS745-1



PWS745-2
PWS745-4



BURR-BROWN®



PWS750

Isolated, Unregulated DC/DC CONVERTER COMPONENTS

FEATURES

- 100% TESTED FOR HIGH-VOLTAGE BREAKDOWN
- COMPACT-SURFACE MOUNT
- MULTICHANNEL OPERATION
- 5V OR 15V INPUT OPTIONS

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL EQUIPMENT
- GROUND-LOOP ELIMINATION
- PC-BASED DATA ACQUISITION
- VENDING MACHINES

DESCRIPTION

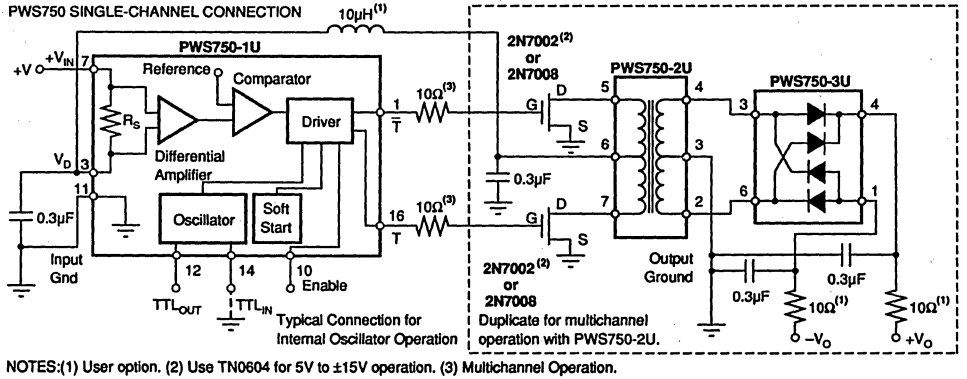
The PWS750 consists of three building blocks for building a low cost DC/DC converter. With them you can optimize DC/DC converter PC board layout or build a multichannel isolated DC/DC converter. All parts are surface mount, requiring minimal space to build the converter. The modular design minimizes the cost of isolated power.

The PWS750-1U is a high-frequency (800kHz nominal) driver that can drive N-channel MOSFETs up to the size of a 1.3A 2N7010. The recommended MOSFET for individual transformer drivers is the 2N7008. The PWS750-1U is supplied in a 16-pin double-wide SO package.

The PWS750-2U and PWS750-4U are split-bobbin wound isolation transformers using a ferrite core. They are encapsulated in plastic packages, allowing a high isolation voltage rating.

The PWS750-3U is a high-speed monolithic diode bridge in a plastic 8-pin SO package.

One PWS750-1U can be used to drive up to four channels (15V nominal operation). One PWS750-2U and PWS750-3U and two 2N7002 (surface mount) or 2N7008 (TO-92) MOSFETs made by Siliconix are used per isolated channel. When a PWS750-4U is used as the transformer (5V input), then two TN0604s made by Supertex must be used, due to the higher currents of the primary (lower RDS on) and the lower V_{GS} threshold. With 5V operation only one channel can be directly driven by the PWS750-1U (a simple FET booster circuit can be used for multichannel operation; see Figure 3).



NOTES:(1) User option. (2) Use TN0604 for 5V to ±15V operation. (3) Multichannel Operation.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-838C

SPECIFICATIONS

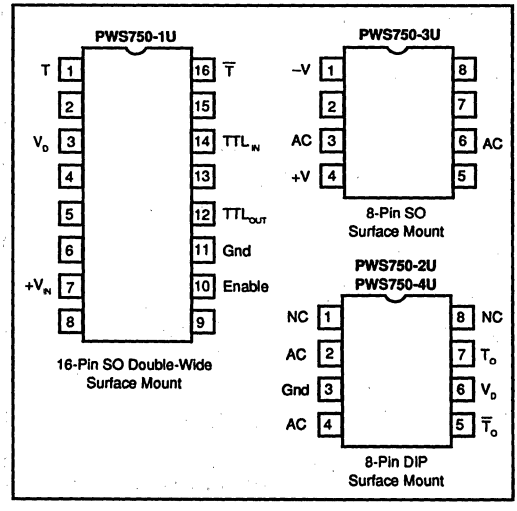
ELECTRICAL

At T_A = 25°C; $+V_{IN}$ = +15V; and I_{OUT} = ±15mA balanced loads unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PWS750-1U OSCILLATOR					
Frequency: Internal OSC	TTL_{IN} = 0V	725	800	875	kHz
External OSC		1		2.5	MHz
Supply: 15V Operation		10	15	18	V
5V Operation		4.5	5	5.5	V
T, $\overline{T}$ Drive Current				50	mApk
T, $\overline{T}$ Drive Voltage, High		3		7	V
Low				0.7	V
TTL_{IN}, I_{IH}			10		nA
I_{IL}			–1		µA
V_{IH}		2			V
V_{IL}				0.8	V
TTL_{OUT}, I_{OL}				15	mA
PWS750-2U $+V_{IN}$ TO $\pm V_{OUT}$ ISOLATION TRANSFORMER					
ISOLATION					
Voltage Rated Continuous AC 60Hz		750			Vrms
100% Test [1]	60Hz, 1s, <5pC PD	1200			Vrms
Barrier Impedance			10^{12} || 8		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms		1	1.5	µArms
Winding Ratio	Primary/Secondary		48/48		
PWS750-3U DIODE BRIDGE					
Reverse Recovery	$I_F = I_R$ = 50mA		40		ns
Reverse Breakdown	I_R = 100µA	55			V
Reverse Current	V_R = 40V			1.5	µA
Forward Voltage	I_F = 100mA			1.6	V
PWS750-4U $+5V_{IN}$ to $\pm 15V_{OUT}$ ISOLATION TRANSFORMER					
ISOLATION					
Voltage Rated Continuous AC 60Hz		750			Vrms
100% Test [1]	60Hz, 1s, <5pC PD	1200			Vrms
Barrier Impedance			10^{12} || 8		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms		1	1.5	µArms
Winding Ratio	Primary/Secondary		24/70		
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating	Derated performance	–40		+85	°C
Srorage		–40		+85	°C

NOTES: (1) Tested at 1.6 x rated, fail on 5pC partial discharge leakage current on five successive pulses at 60HZ.

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18V
Junction Temperature	150°C
Storage Temperature	–40°C to +85°C
Lead temperature (soldering, SOIC, 3s)	+260°C
Max Load, Sum of Both Outputs (PWS750-2U, 4U)	60mA

ORDERING INFORMATION

PWS750-XU

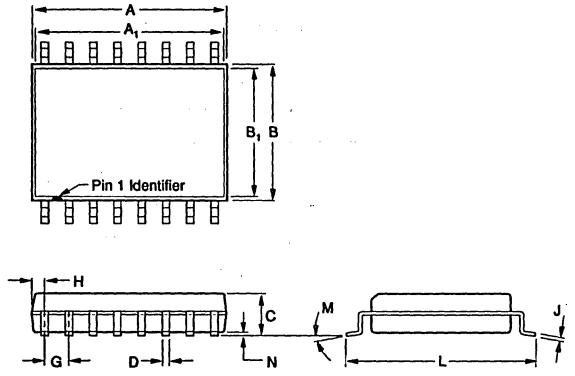
Basic Model Number

Components

1U : High-Frequency Driver
2U, 4U : Isolation Transformer
3U : High-Speed Monolithic Diode Bridge

MECHANICAL

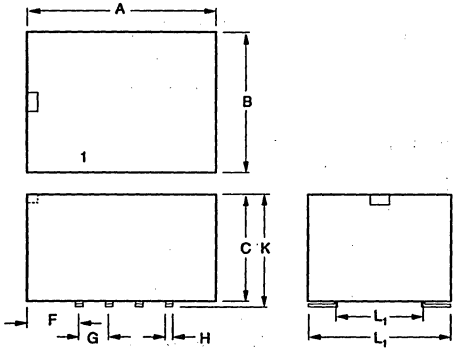
U Package — 16-Pin SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.400	.416	10.16	10.57
A1	.388	.412	9.86	10.46
B	.286	.302	7.26	7.67
B1	.268	.286	6.81	7.26
C	.093	.109	2.36	2.77
D	.015	.020	0.38	0.51
G	.0.50 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.391	.421	9.93	10.69
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

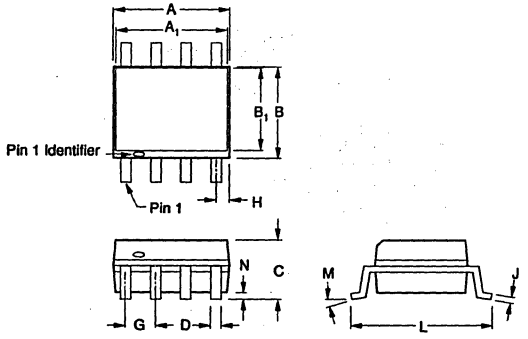
U Package — 8-Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.620	.640	15.78	16.26
B	.465	.485	11.81	12.32
C	.350	.370	8.89	9.40
F	.165	.185	4.19	4.70
G	.100 BASIC		2.54 BASIC	
H	.025 SQ		.635 SQ	
K	.370	.390	9.40	9.91
L1	.280	.300	7.11	7.62
L2	.465	.485	11.81	12.32

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

U Package — 8-Pin SOIC



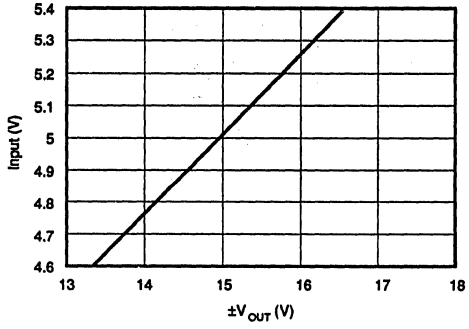
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.201	4.70	5.11
A1	.178	.201	4.52	5.11
B	.146	.162	3.71	4.11
B1	.130	.149	3.30	3.78
C	.054	.145	1.37	3.69
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.018	.026	0.46	0.66
J	.008	.012	0.20	0.30
L	.220	.252	5.59	6.40
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

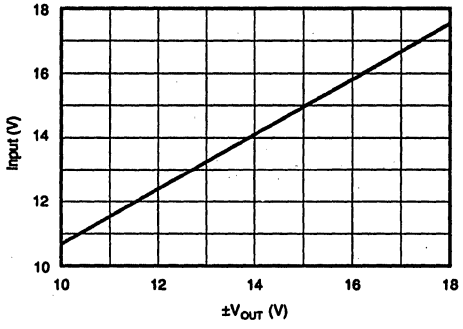
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{IN} = 15VDC, I_{LOAD} = ±15mA unless otherwise noted.

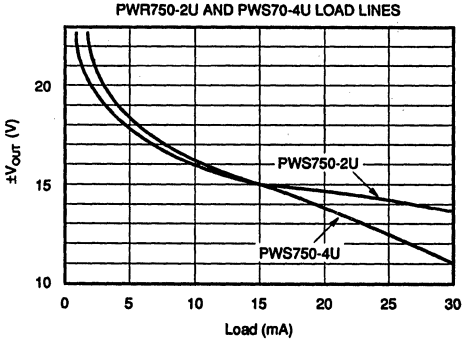
PWS750-4U LINE REGULATION



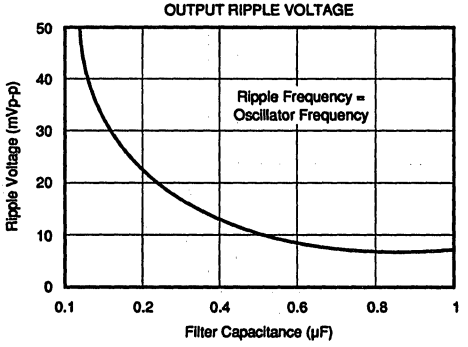
PWR750-2U LINE REGULATION



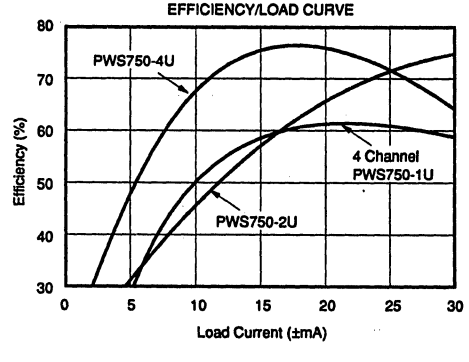
PWR750-2U AND PWS70-4U LOAD LINES



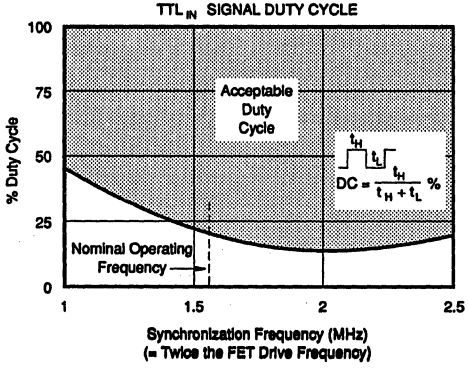
OUTPUT RIPPLE VOLTAGE



EFFICIENCY/LOAD CURVE

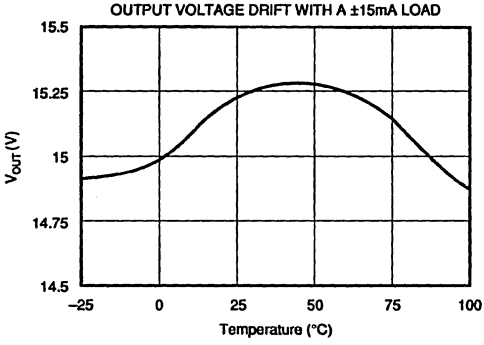


TTL$_{IN}$ SIGNAL DUTY CYCLE



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{IN} = 15VDC, I_{LOAD} = ±15mA unless otherwise noted.



MOSFET	MAX DRIVE CURRENT	PACKAGE	BREAKDOWN
TN0604	4A	TO-92	40V
2N7002	115mA	SO-T23	60V
2N7008	500mA	TO-92	60V
2N710	1.3A	TO-237	60V
2N7012	1.2A	4-Pin DIP	60V

TABLE 1. MOSFET Selector Guide.

THEORY OF OPERATION

The PWS750 components are basic building blocks to be used with other standard components to build an isolated push-pull DC/DC converter. The oscillator runs at 800kHz nominal, making it possible to reduce the size of the transformer and lower the output ripple voltage.

PWS750-1U OSCILLATOR PIN FUNCTIONS

TTL_{IN} is used to control the driver frequency with an external TTL level frequency source. The input frequency must be twice the desired driver frequency, since there is an internal divide-by-2 circuit to produce a 50% duty cycle output. The input duty cycle can vary from 12% to 95% (see Typical Performance Curves). When in the free running mode, the TTL_{IN} pin must be tied to ground.

TTL_{OUT} is used when it is desired to synchronize the outputs of multiple PWS750-1Us to minimize beat frequency problems. A standard open collector output is provided, therefore a 330Ω to 3.3kΩ pull-up resistor will be necessary depending on stray capacitance on the sync line. A maximum of eight PWS750-1Us can be connected without the use of an external TTL buffer.

An Enable pin is provided so that the driver (T, $\overline{T}$) can be shut down to minimize power use if required. A TTL low applied to the pin will shut down the driver within one cycle. A TTL high will enable the driver within one cycle. The TTL_{OUT} will still have an 800kHz signal when a master driver is disabled, so other synchronized drivers will not be shut down. The pin can be left open for normal operation.

The $+V_{IN}$ pin supplies power to the oscillator. The V_D pin connects the power to the transformer through the internal overcurrent sense resistor. The other end of the overcurrent sense resistor is tied to $+V_{IN}$. A 0.3µF bypass capacitor must be connected to the V_D pin to reduce the ripple current through the shunt resistor; otherwise false current limit conditions can occur due to ripple voltage peaks.

During overload conditions the output drive shuts off for approximately 80µs, then turns back on for 20µs, resulting in a 25% power up duty cycle. If the overload condition still exists, then the output will shut off again. When the fault or the excessive load is removed, the converter resumes normal operation.

The T and $\overline{T}$ pins are the complementary FET drive outputs and are tied directly to the corresponding FET gate. The connection must be as short as possible. For multiple channel operation they cannot be located above any ground or power planes, because capacitive loading will not allow fast enough charging of the FET gate.

PWS750-2U AND PWS750-4U TRANSFORMER PIN FUNCTIONS

On the primary side the V_D pin of the PWS750-2U is tied directly to the V_D pin of the PWS750-1U. Remember to place a 0.1µF capacitor as close to the PWS750-2U V_D pin as possible. The T_O and $\overline{T}_O$ pins are connected to the drains of the corresponding FETs, whose sources are connected to ground. On the secondary side of the transformer, the Gnd pin is tied directly to the isolated ground. AC pins are 800kHz square wave signals at twice the output voltage, and are connected directly to the corresponding pin on the PWS750-3U. Pins 2 and 4 can be interchanged for ease of hook up. The connection to the diode bridge must be as direct as possible to minimize radiated noise.

PWS750-3U HIGH SPEED DIODE BRIDGE PIN FUNCTIONS

The AC pins are tied directly to the AC pins of the PWS750-2U. The +V and –V pins are rectified output voltages. The filter capacitors must be located as close as possible to these pins to minimize series inductance and therefore noise. Bypass capacitors will be needed at each device in the circuit.

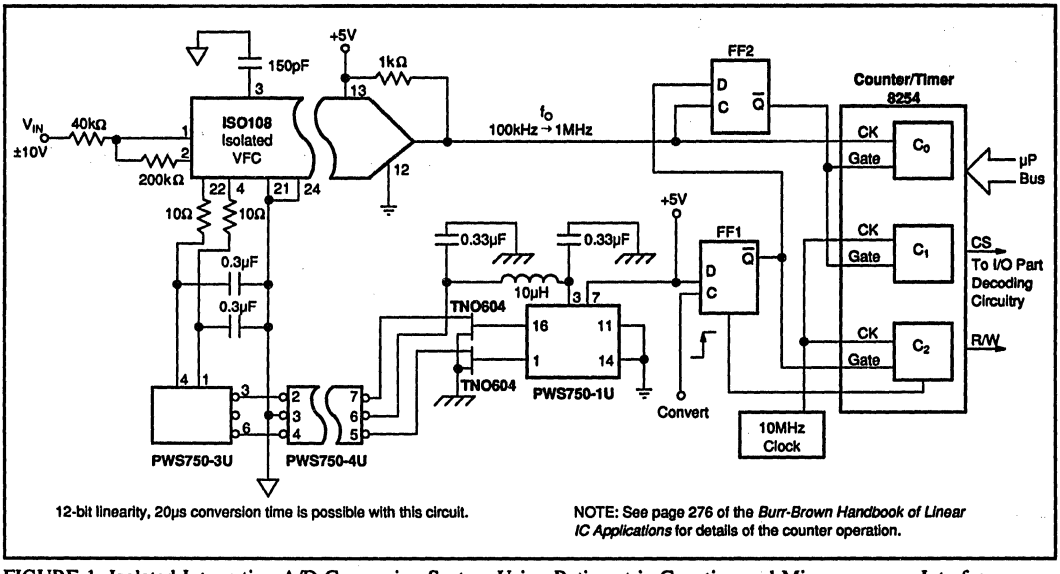


FIGURE 1. Isolated Integrating A/D Conversion System Using Ratiometric Counting and Microprocessor Interface.

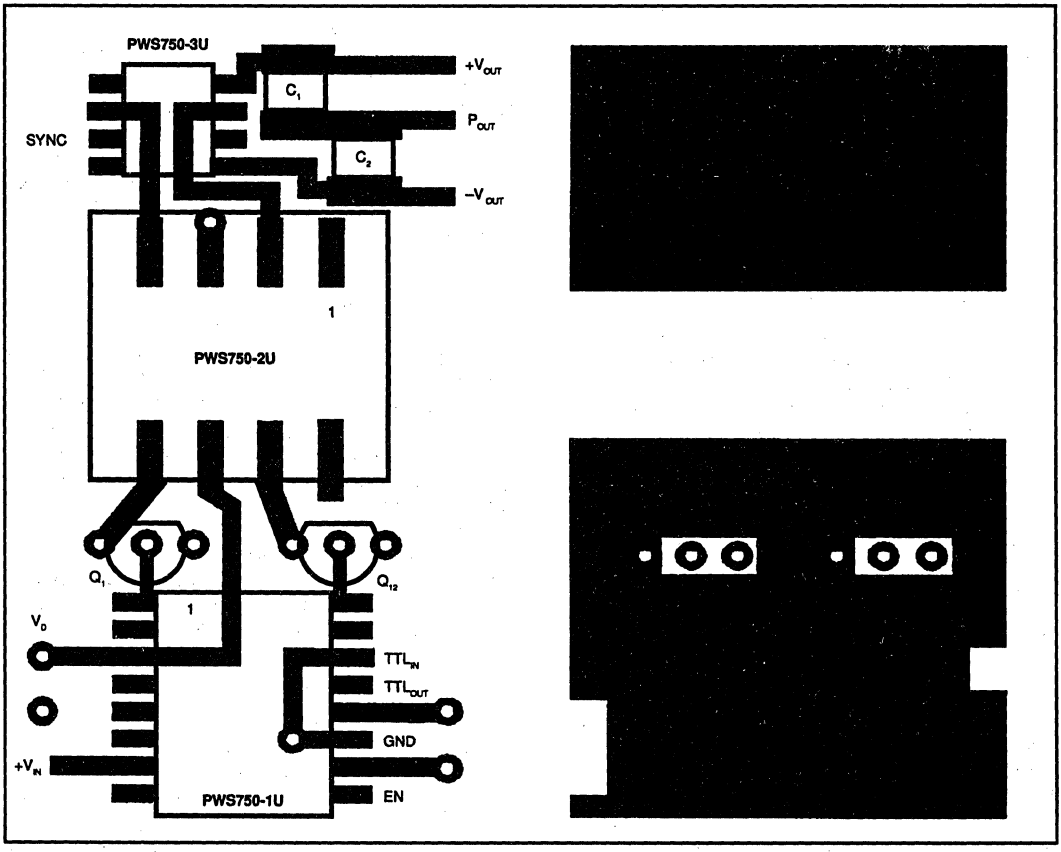


FIGURE 2. Sample PC Board Layout, 4:1.

BASIC OPERATION

SINGLE CHANNEL OPERATION, PC BOARD LAYOUT CONSIDERATIONS

A simple two-layer board can be used on single channel applications to create a DC/DC converter with low radiated noise. A ground plane should be located directly under both the input and the output components for optimum ground return paths. The surface mount components make it easy to design with a ground plane. The output filter capacitors should be located as close to the PWS750-3U as possible. A sample layout is shown in Figure 2.

For multiple channel applications, T and $\overline{T}$ traces must have minimum capacitive loading. Therefore, there should be no ground plane (or power plane) under these two traces. The driver signal is a 4-6V low current 800kHz signal, which will generate little radiated noise if the traces are kept short.

To minimize the noise pickup for sensitive 12-bit resolution circuits, place a 10Ω resistor in series with the isolated power traces. The resistor, in conjunction with the bypass capacitor, acts as a low pass filter to minimize isolation amplifier PSRR-related ripple voltage feedthrough. A pi filter with a 10µH inductor can also be used at the input ($+V_{IN}$) to minimize input supply ripple current; see Figure 1.

MULTIPLE CHANNEL OPERATION

The oscillator can drive up to four-channels (eight FETs) directly when operating at 10-18V. A 10Ω resistor must be placed in series with T and $\overline{T}$ to stabilize the FET gate charging. For more than four-channel operation, or 5V-multiple-channel operation, the driver circuit needs a FET booster circuit, as shown in Figure 3. Large gate drive surge currents (>100mA) are needed to turn on the gates.

If the total output current drawn by all the channels exceeds 250mA, then it will be necessary to circumvent the current limit circuit by leaving the V_D pin of the PWS750-1U open, and connect the V_D pin of the PWS750-2U directly to the supply.

5V OPERATION

With 5V operation, the transformer winding current ratio is 3:1, therefore generating much greater currents in the primary. The input ripple voltage will be larger, so an input pi filter will be necessary to isolate the converter noise from the rest of the circuit. For example, when the output is ±15mA the input current will be at least 120mA.

OUTPUT CURRENT RATING

The PWS750-1U oscillator contains soft start circuitry to protect the FETs from high inrush currents during turn on. The internal input current limit is 250mA peak to prevent thermal overload of the MOSFETs. The maximum output rating is ±30mA. Total current, which can be drawn from each isolation channel, is the total of the power being drawn from both the +V and –V outputs. For example, if one output is not used, then maximum current can be drawn from the other output. In all cases the maximum current that can be drawn from any individual channel is:

$$|+I_{OUT}| + |-I_{OUT}| < 60mA$$

It should be noted that many analog circuit functions do not simultaneously draw equal current from both the positive and negative supplies.

When multiple channel operation is used, the maximum current of all channels must be reduced to prevent the overcurrent limit to trip. Alternately, bypass the overcurrent by

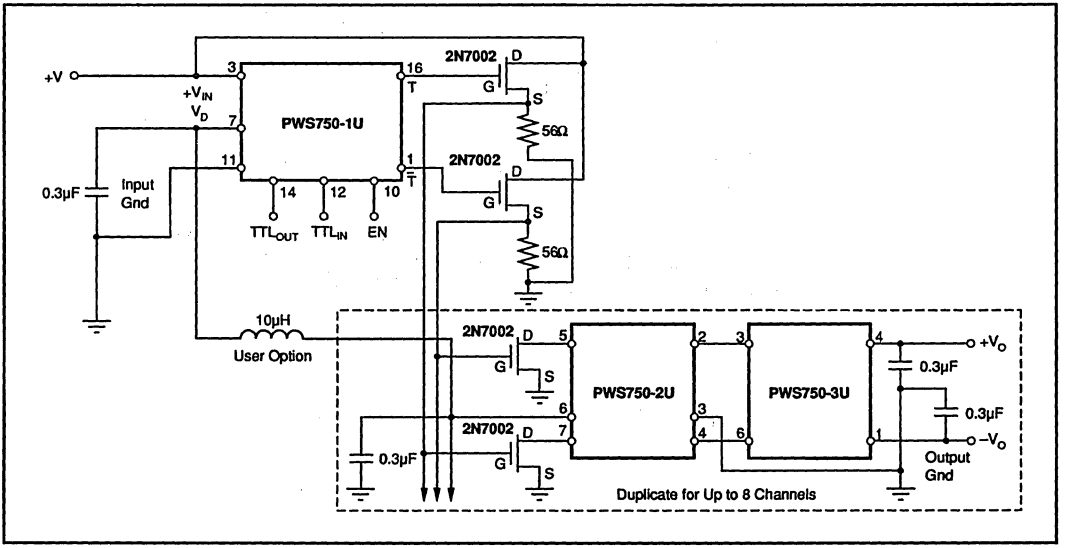


FIGURE 3. MOSFET Driver Booster Circuits.

leaving the V_D pin of the PWS750-1U open and connecting the V_D pin of the PWS750-2U directly to the supply.

HIGH VOLTAGE TESTING

Burr-Brown Corporation has adopted a partial discharge test criterion that conforms to the German VDE0884 optocoupler standard. This method requires that less than 5pC partial discharge crosses the isolation barrier with 1200Vrms 60Hz applied. This criterion confirms transient overvoltage (1.5 x 750Vrms) protection without damage to the PWS750-2U or PWS750-4U. Life test results verify the absence of high voltage breakdown under continuous rated voltage and maximum temperature.

The minimum AC barrier voltage that initiates partial discharge above 5pC is defined as the "inception voltage." Decreasing the barrier voltage to a lower level is required before partial discharge ceases; this is known as "extinction voltage." We have developed a package insulation system to yield an inception voltage greater than 1200Vrms so that transient voltages below this level will not damage the isolation barrier. The extinction voltage is above 750Vrms so that even overvoltage-induced partial discharge will cease once the barrier voltage is reduced to the rated value. Previous high voltage test methods relied on applying a large enough overvoltage (above rating) to break down marginal units, but not so high as to permanently damage good ones. Our partial discharge testing gives us more confidence in barrier reliability than breakdown/no breakdown criteria.

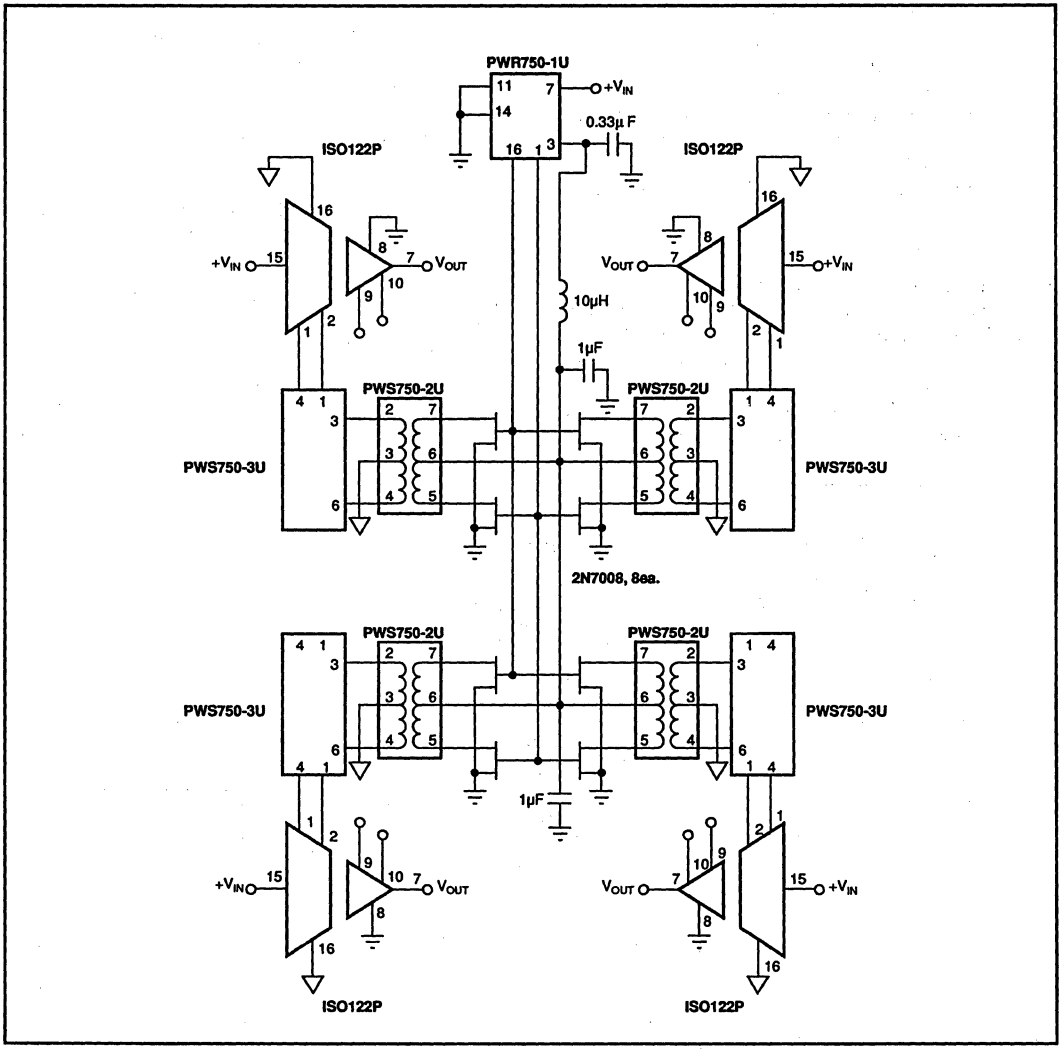


FIGURE 4. Four-Channels of ±10V Signal Isolation with Channel-to-Channel Isolation.

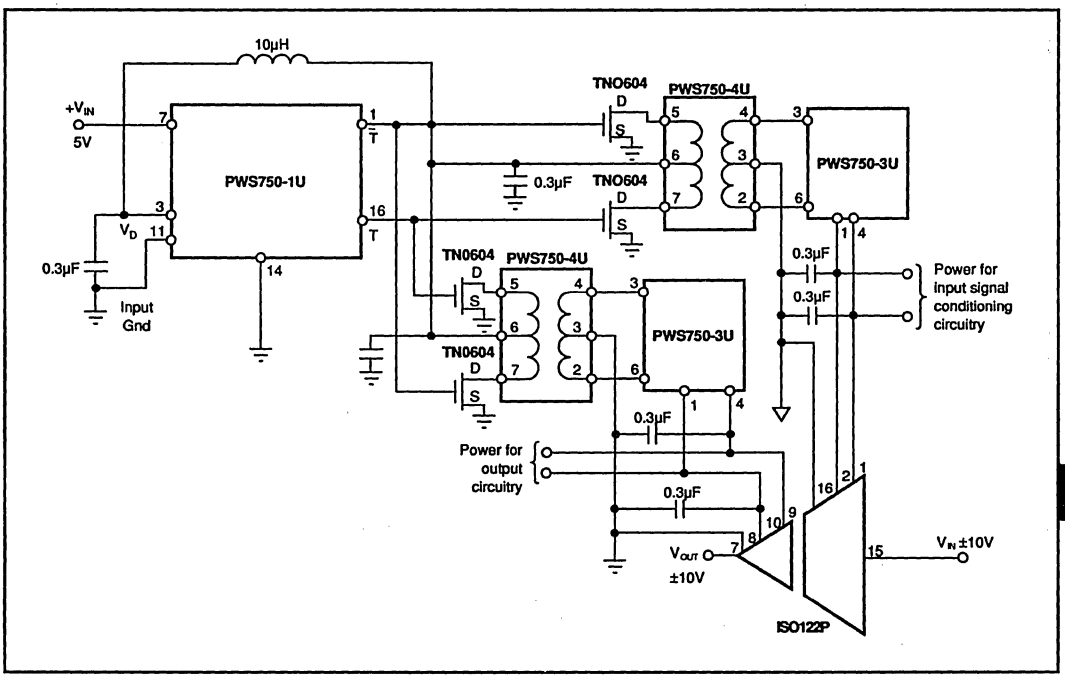


FIGURE 5. A Complete ±10V Signal Acquisition System Operating From a Single 5V Supply.

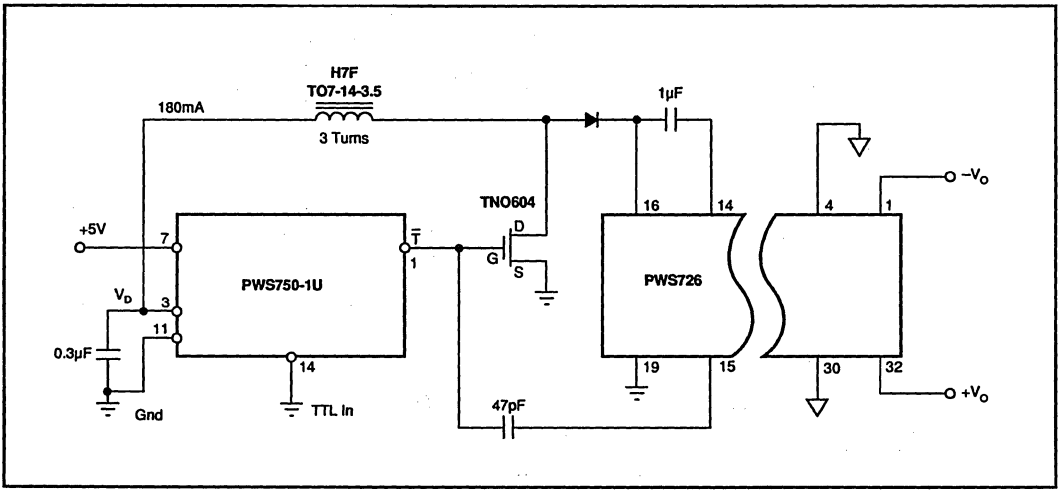


FIGURE 6. A PWS750 Driver Can Be Used to Boost the Input Voltage to 15V to Power a PWS726 From a 5V Supply.

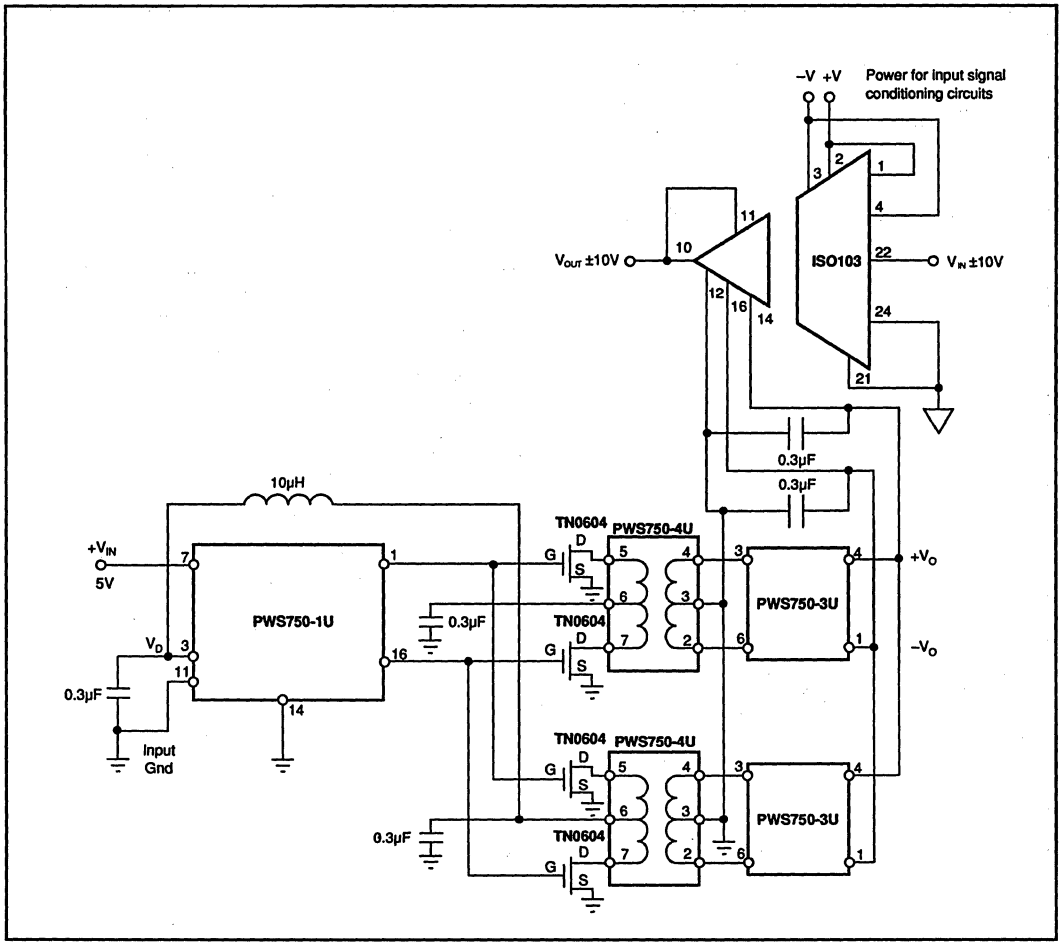


FIGURE 7. Powering the Internally Powered ISO103 Isolation Buffer From a Single 5V Supply. Two Power Channels Are Necessary to Provide the 80mA Nominal for the +V of the ISO103.

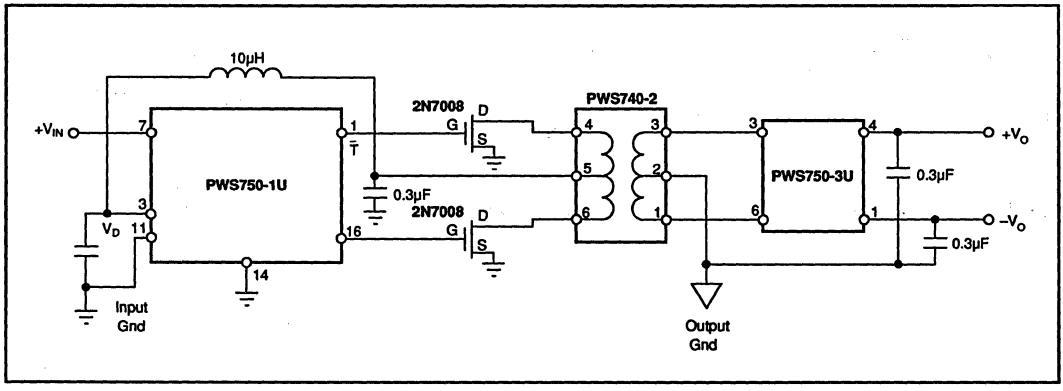


FIGURE 8. 1500VAC Isolation Using PWS740-2 Transformer.

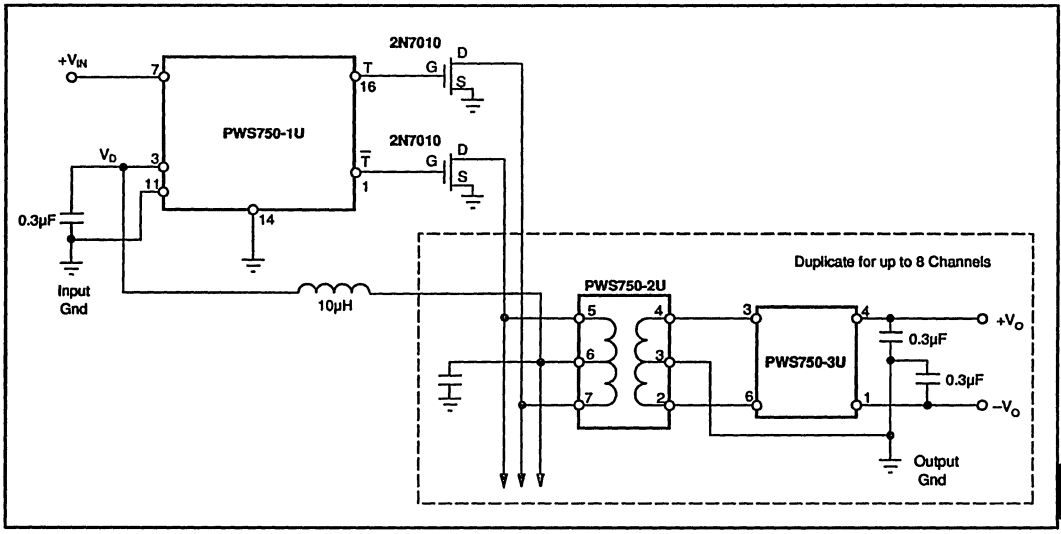
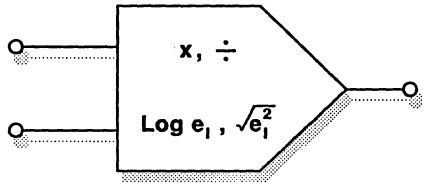


FIGURE 9. FET Pair Driving Up to Eight-Channels.



ANALOG CIRCUIT FUNCTIONS

5

Analog circuits act as building blocks with which to perform a variety of instrumentation, computation, and control functions. They provide a broad range of versatile, proven, and ready to use computational functions for the designer to use in developing simple or complex systems. The analog circuit functions include multipliers, dividers, multifunction converters, true rms-to-DC converters, logarithmic amplifiers, voltage and window comparators, peak detectors, precision oscillators, and filters. The multifunction converters also provide multiply, divide, square root, exponentiation, roots, sine, cosine, arctangent, vector magnitude rms-to-DC and logarithmic amplifier functions.

The availability of these relatively complex functions as precise, versatile, easy-to-use, low-cost building blocks has broadened the scope of practical analog circuit systems and greatly simplified analog circuit designs. The names of most analog circuit functions are self-explanatory and describe the main functions they perform.

The functions are used mostly for processing and/or conditioning of analog signals, and for simulation of algebraic and/or trigonometric analog computations. The variety of applications these functions are effectively used for is limited only by the designer's creative imagination. Some of the interesting applications for which analog circuit functions have found wide acceptance are listed in the table on the following page.

Types of Application	Recommended Analog Circuit Function
Analog simulation Algebraic and trigonometric computations Power series approximation, function fitting and linearizing Analog wave shaping	Multiplier, Divider, Multifunction Converter, Logarithmic Amplifier, Oscillator
VCO and AGC applications	Multiplier, Divider
Vector computation	Multifunction Converter, Multiplier
Power and energy measurements	Multiplier, rms-to-DC Converter
Modulation and demodulation	Multiplier, Divider
Signal compression	Logarithmic Amplifier
Log-antilog-log ratio computations	Logarithmic Amplifier
Light-related measurements	Logarithmic Amplifier
Analog signal conditioning	All circuit functions
Instrumentation and control systems	All circuit functions
Test equipment	All circuit functions
Transducer excitation	Oscillator
Signal reference	Oscillator
Alarm circuits	Voltage and Window Comparators
Bang-bang control applications	Voltage and Window Comparators
Control of limit stops	Voltage and Window Comparators
Analog memory and peak detection	Peak Detection

ANALOG CIRCUIT FUNCTIONS SELECTION GUIDES

The Selection Guides show parameters for the high grade. Refer to the Product Data Sheet for a full selection of grades. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book.*

MULTIPLIERS/DIVIDERS

You can select accuracy from 0.25% max and up from this complete line of integrated circuit multipliers. Most provide full four-quadrant multiplication. All are laser-trimmed for accuracy—no trim pots are needed to meet specified performance. These compact models bring the cost of high performance down to acceptable levels.

MULTIPLIERS/DIVIDERS **Boldface = NEW**

Model	Transfer Function	Error at +25°C max (%)	Temp Coeff (%/°C)	Feed-through (mV)	Offset Voltage (mV)	1% BW (kHz)	Temp Range[1]	Pkg	Page No.
MPY100	$[(X_1-X_2)(Y_1-Y_2)/10]+Z_2$	±0.5	0.008	30	7	70	Ind	TO-100	5-26
MPY534	$[(X_1-X_2)(Y_1-Y_2)/10]+Z_2$	±0.25	0.008	0.05%	2	3MHz	Com	TO-100	5-34
MPY600AP	**$[(X_1-X_2)(Y_1-Y_2)/2]+Z_2$**	**±0.25**	**0.02**	**2**	**5**	**10MHz**	**Ind**	**DIP**	**S5-25**
MPY634M	$[(X_1-X_2)(Y_1-Y_2)/10]+Z_2$	±0.5	0.015	0.15%	2	10MHz	Ind	TO-100	5-41
MPY634P, U	$[(X_1-X_2)(Y_1-Y_2)/10]+Z_2$	±2.0	0.03	0.3%	25	10MHz	Ind	DIP,SOIC	5-41
AD632	$[(X_1-X_2)(Y_1-Y_2)/10]+Z_2$	±0.5	0.01	0.15	15	50	Ind	TO-100	5-6

NOTE: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C.

SPECIAL FUNCTIONS

This group of models offers many different functions that are the quick, easy way to solve a wide variety of analog computational problems. Most are in integrated circuit packages and are laser-trimmed for excellent accuracy.

5

SPECIAL FUNCTIONS

Function	Model	Description	Comments	Temp Range[1]	Pkg	Page No.
Multifunction Converter	4302	$Y(Z/X)^m$ This function may be used to multiply, divide, raise to powers, take roots and form sine and cosine functions.	Plastic Package.	Ind	DIP	5-109
	LOG100	$K \text{ Log } (I_1/I_2)$	Optimized for log ratio of current inputs. Specified over six decades of input (1nA to 1mA), 55mV total error, 0.25% log conformity.	Com	DIP	5-18
Logarithmic Amplifier	4127G	$K \text{ Log } (I_1/I_{REF})$	A more versatile part that contains an internal reference and a current inverter. 1% and 0.5% accuracy.	Com	DIP	5-102
$\sqrt{\frac{1}{T}\int_0^T E_{IN}^2(t)dt}$	4341	True rms-to-DC conversion based on a log-antilog occupational approach. Pin compatible with 4340.	Some external trimming required. Lower cost in plastic package.	Ind	DIP	5-115
High Speed Window Comparator, ATE Pin Receiver	**CMP100**	**A dual comparator with high common-mode input range. Latched ECL outputs, ±5V supplies.**	**Propagation delay: 5ns, max for 100mV overdrive**	**Ind**	**DIP, SOIC**	**S5-14**
Switched Integrator	**ACF2101**	**This is a dual, integrating, transimpedance amplifier that converts an input current to an output voltage by integrating the current for a user determined period of time. Eliminates large feedback resistor of traditional I to V converters.**	**Includes HOLD and RESET switches and output multiplexer.** $V_{OUT} = -\frac{1}{C}\int i_{IN}\,dt$	**Ind**	**DIP**	**S5-6**

NOTE: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C.

DIVIDERS

Using a special log/antilog committed divider design overcomes the major problem encountered when trying to use a multiplier in a divider circuit. Outstanding accuracy is maintained even at very low denominator voltages.

DIVIDERS

Model	Transfer Function	Input Range	Accuracy D = 250mV max (%)	Temp Coeff (%/°C)	0.5% BW (kHz)	Rated Output, min	Temp Range[1]	Pkg	Page No.
DIV100P	10 x N/D	250mV to 10V	0.25	0.2	15	±10V, ±5mA	Ind	DIP	5-10

NOTE: (1) Ind = –25°C to +85°C.

FREQUENCY PRODUCTS

This group of products consists of precision oscillators and active filters for both signal generation and attenuation. Both fixed frequency and user-selected frequency units are available.

FREQUENCY PRODUCTS **Boldface = NEW**

Function	Model	Description	Comments	Temp Range[1]	Pkg	Page No.
Oscillator	4423	Very low cost in plastic package. Provides resistor-programmable quadrature outputs (sine and cosine wave outputs simultaneously available).	Frequency range: 0.002Hz to 20kHz. Frequency stability: 0.01%/°C. Quadrature phase error: ±0.1%.	Com	DIP	5-119
Universal Active Filter	**UAF42**	**These filters provide a complex pole pair. Based on state variable approach, low-pass, high-pass, and bandpass outputs are available.**	**Add only resistors to determine pole location (frequency and Q). Easily cascaded for complex filter responses.**	**Ind**	**DIP**	**S5-45**
	UAF41			Ind	DIP	5-82
	UAF21			Ind	DIP	5-74

NOTE: Com = 0°C to +70°C, Ind = –25°C to +85°C.

VOLTAGE REFERENCE

These products are precision voltage references that provide a +10V output. The output can be adjusted with minimal effect on drift or stability.

VOLTAGE REFERENCE — **Boldface = NEW**

Model	Output (V)	Min Output (mA)	Max Drift (ppm/°C)	Power Supply (V)	Power Supply (mA)	Temp Range[1]	Pkg	Page No.
REF10M	±10.00 ±0.005	10	1	+13.5/35	4.5	Com	TO-99	5-49
REF101M	±10.00 ±0.005	10	1	+13.5/35	4.5	Com	TO-99	5-55
REF102M	**±10.00 ±0.0025**	**10**	**2.5**	**+11.4/36**	**1.4**	**Ind, Mil**	**TO-99**	**S5-37**
REF102P, U	**±10.00 ±0.005**	**10**	**5**	**+11.4/36**	**1.4**	**Ind**	**DIP, SOIC**	**S5-37**

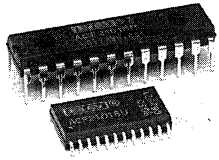
NOTE: (1) Com = 0°C to +70°C. Ind = –25°C to +85°C, Mil = –55°C to +125°C.

CURRENT REFERENCE — **Boldface = NEW**

Model	Output I (µA)	Max Drift Compliance	(ppm/°C)	Comments	Temp Range[1]	Pkg	Page No.
REF200M, P, U	Dual 100 ±0.5	2.5V to 40V	25	Includes 0.5% accurate current mirror	Ind	DIP, TO-99, SOIC	5-63 5-63 5-63

NOTE: (1) Ind = –25°C to +85°C.

BURR-BROWN®



ACF2101

ADVANCE INFORMATION
SUBJECT TO CHANGE

Low Noise, Dual SWITCHED INTEGRATOR

FEATURES

- INCLUDES INTEGRATION CAPACITOR, RESET AND HOLD SWITCHES, AND OUTPUT MULTIPLEXER
- LOW NOISE: 10μVrms
- LOW CHARGE TRANSFER: 0.1pC
- WIDE DYNAMIC RANGE: 120dB
- LOW DROOP: 2nV/μs

APPLICATIONS

- CURRENT TO VOLTAGE CONVERSION
- PHOTODETECTOR INTEGRATOR
- CURRENT INTEGRATOR
- CT SCANNER FRONT END
- PHOTOMETRIC MEASUREMENTS
- MEDICAL, SCIENTIFIC, AND INDUSTRIAL INSTRUMENTATION

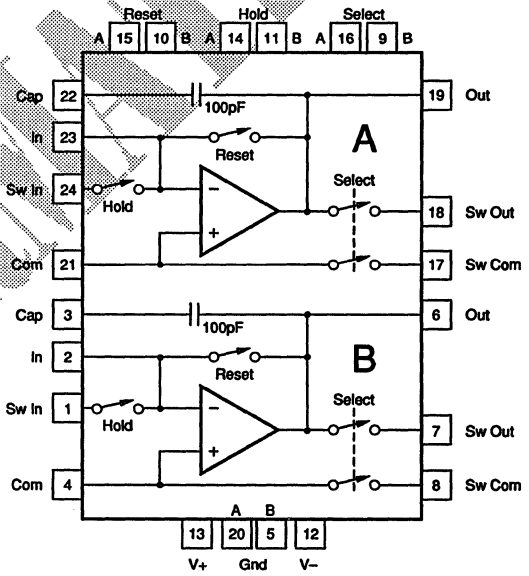
DESCRIPTION

The ACF2101 is a dual switched integrator for precision applications. Each channel can convert an input current to an output voltage by integration, using either an internal or external capacitor. Included on the chip are precision 100pF integration capacitors, hold and reset switches, and output multiplexers.

As a complete circuit on a single chip, the ACF2101 eliminates many of the problems commonly encountered in discrete designs, such as leakage current errors and noise pickup. The integrating approach can provide lower noise than conventional transimpedance amplifier designs and also eliminates the need for high performance, high value feedback resistors.

The extremely low bias current and low noise of the ACF2101's ***Difet***® amplifiers, along with active laser trimming of both offset and drift, assure precision current to voltage conversion.

Although designed for +5V, –15V supplies, the ACF2101 can be operated on supplies up to ±18VDC. It is available in both 24-pin plastic DIP and SOIC package.



Difet® Burr-Brown Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1078

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V+ = +5V, V– = –15V, Internal C = 100pF.

PARAMETER	CONDITIONS	ACF2101BP, BU MIN	TYP	MAX	UNITS
ANALOG INPUT					
INPUT RANGE					
Input Current Range					
Switched Input		0		+100	µA
Direct Input		0		+1	mA
INPUT IMPEDANCE					
Switched Input					
Hold Switch OFF			100		GΩ
Hold Switch ON			2		kΩ
Direct Input			Virtual Ground		
HOLD SWITCH VOLTAGE					
Hold Switch Withstand Voltage	Hold Switch OFF	0		±100	mV
OFFSET VOLTAGE					
Input Offset Voltage			±0.5	±2	mV
Average Drift			±1		µV/°C
DIGITAL INPUTS					
Logic Family	TTL Compatible				
V_{IH} (Logic 1 = Switch OFF)		2		5.5	V
V_{IL} (Logic 0 = Switch ON)		–0.5		0.8	V
I_{IH}	V_{IH} = +5V		2		µA
I_{IL}	V_{IL} = 0V		0		µA
Switching Speed					
Switch ON			100		ns
Switch OFF			100		ns
TRANSFER CHARACTERISTICS					
TRANSFER FUNCTION			$V_{OUT} = -1/C\int I_{IN}\,dt$		V
DYNAMIC CHARACTERISTICS					
Integrate Mode					
Slew Rate		1			V/µs
Reset Mode					
Slew Rate			5		V/µs
Settling Time to 0.01%FSR	10V Step		3		µs
Overload Recovery	Positive or Negative		1		µs
Output Multiplexer (Select Switches)					
Settling Time to 0.01%FSR	C_{LOAD} < 1000pF		5		µs
Settling Time to 0.01%FSR	C_{LOAD} < 100pF		1		µs
INTEGRATION CAPACITOR (C)					
Internal Capacitor					
Value			100		pF
Accuracy			0.5	2	%
Temperature Coefficient			20		ppm/°C
Memory			50		ppm of FSR[1]
RESET SWITCH					
Impedance					
Reset OFF			100		GΩ
Reset ON			2		kΩ
MODES OF OPERATION					
Switch	Hold / Reset				
Integrate Mode	ON / OFF				
Hold Mode	OFF / OFF				
Reset Mode	ON/OFF / ON				
(Logic 1 = OFF, Logic 0 = ON)					

ELECTRICAL (CONT)

T_A = +25°C, V+ = +5V, V– = –15V, Internal C = 100pF.

PARAMETER	CONDITIONS	ACF2101BP, BU MIN	TYP	MAX	UNITS
OUTPUT					
Voltage Output Range		+0.1		–10	V
Current Output, Direct Output			±5		mA
Short Circuit Current					
Direct Output			±25		mA
Switched Output			±5		mA
Output Impedance					
Direct Output			0.1		Ω
Switched Output					
Select Switch ON			250 || 5		Ω || pF
Select Switch OFF			100 || 5		GΩ || pF
Load Capacitance Stability					
Direct Output			500		pF
Switched Output			Any		pF
OUTPUT ACCURACY					
Nonlinearity				0.01	%FSR
Channel Separation	BW = 0.1Hz to 2kHz		–80		dB
Op Amp Bias Current			200		fA
Hold Mode Droop			2	10	nV/µs
Integrate Mode Droop			2	10	nV/µs
Voltage Offset					
Value			1		mV
Temperature Coefficient			1		µV/°C
Power Supply Rejection	V_S = +5V to +18V, –10V to –18V		100		dB
OUTPUT NOISE[2]					
Total Output Noise[3]	BW = 0.1Hz to 10Hz		2		µVrms
Integrate Mode[4]	BW = 0.1Hz to 250kHz		10(1 + C_{IN}/C)		µVrms
Hold Mode	BW = 0.1Hz to 250kHz		10		µVrms
Reset Mode	BW = 0.1Hz to 250kHz		10		µVrms
CHARGE TRANSFER ERRORS[5]					
Reset to Integrate Mode[6]					
Charge Transfer			0.1		pC
Charge Transfer TC			0.1		fC/°C
Charge Offset Error			1		mV
Charge Offset TC			1		µV/°C
Integrate to Hold Mode					
Charge Transfer			0.1		pC
Charge Transfer TC			0.1		fC/°C
Charge Offset Error			1		mV
Charge Offset TC			1		µV/°C
Hold to Integrate Mode					
Charge Transfer			0.1		pC
Charge Transfer TC			0.1		fC/°C
Charge Offset Error			1		mV
Charge Offset TC			1		µV/°C
POWER SUPPLY					
Specified Operating Voltage			+5, –15		V
Operating Voltage Range					
Positive Supply		+4.5		+18	V
Negative Supply		–10		–18	V
Current					
Positive Supply	For Dual		12	15	mA
Negative Supply	For Dual		3	4	mA
TEMPERATURE RANGE					
Specification		–40		+85	°C
Operation		–40		+125	°C
Storage		–40		+125	°C
Thermal Resistance	Junction to Ambient		40		°C/W

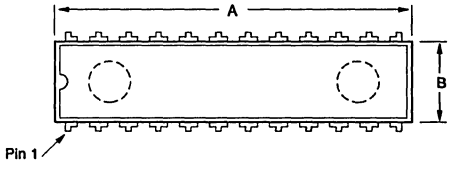
NOTES: (1) FSR is Full Scale Range = 10V (0 to –10V). (2) Total noise is rms total of noise for the modes of operation used. (3) Includes noise from all modes of operation. (4) C_{IN} = capacitance of sensor connected to ACF2101 input; C = integration capacitance. (5) Errors created when the internal switches are driven from one mode to another. (6) The charge transfer is 0.1pC; for an integration capacitance of 100pF, the resultant charge offset voltage error is 1mV.

ORDERING INFORMATION

MODEL	PACKAGE	SPECIFIED TEMP. RANGE
ACF2101BP	Plastic DIP	–40°C to +85°C
ACF2101BU	Plastic SOIC	–40°C to +85°C

MECHANICAL

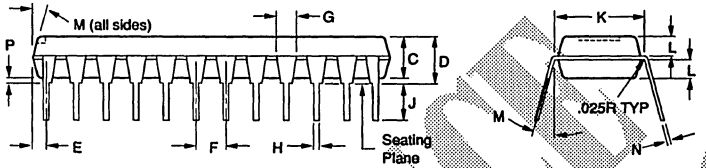
P Package — 24-Pin Single Wide Plastic DIP



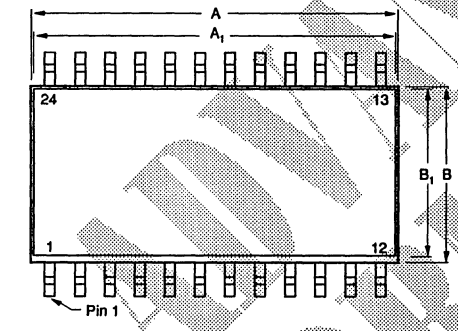
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.125	1.255	28.58	31.88
B	.250	.290	6.35	7.37
C	—	—	—	—
D	.150	.170	3.81	4.32
E	.010	.080	0.25	2.03
F	.100 BASIC		2.54 BASIC	
G	.050	.070	1.27	1.78

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
H	.016	.020	0.41	0.51
J	.125	N/A	3.18	N/A
K	.300 BASIC		7.62 BASIC	
L	—	—	—	—
M	0°	15°	0°	15°
N	.008	.015	0.20	0.38
P	.010	.030	0.25	0.76

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only.

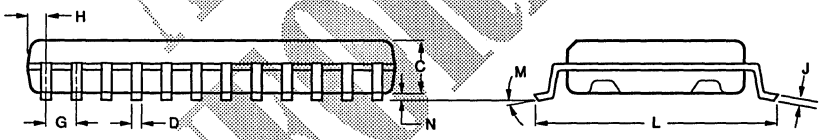


U Package — 24-Pin SOIC



	INCHES DIM	INCHES MIN	MILLIMETERS MAX	MILLIMETERS MIN
MAX				
A	.602	.618	15.29	15.70
A1	.595	.618	15.11	15.70
B	.286	.302	7.26	7.67
B1	.270	.285	6.86	7.24
C	.093	.108	2.36	2.74
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.026	.034	0.66	0.86
J	.008	.012	0.20	0.30
L	.390	.422	9.91	10.72
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

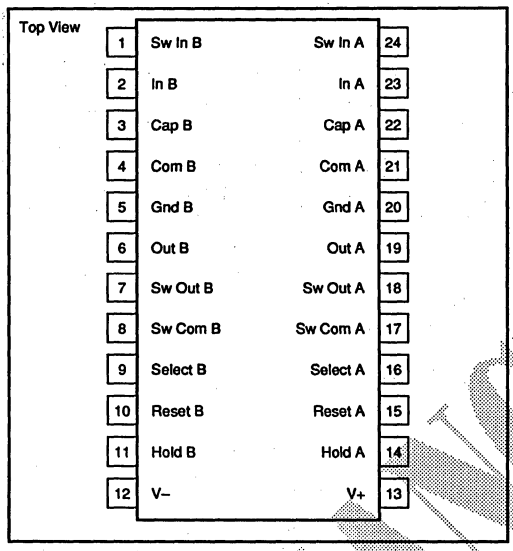
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.



ABSOLUTE MAXIMUM RATINGS

Supply	±18V
Input Current	±3mA
Output Short Circuit Duration	Continuous to Ground
Power Dissipation	500mW
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

PIN CONFIGURATION



APPLICATIONS INFORMATION

BASIC CIRCUIT CONNECTION

Basic Layout

As with any precision circuit, careful layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance—especially at the analog and digital input pins.

Figure 1a illustrates the basic connections needed for operation. Figure 1b illustrates the addition of external integration capacitors and input guards.

Leakage currents between printed circuit board traces can easily exceed the input bias current of the ACF2101. A circuit board "guard" pattern reduces leakage effects by surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential. Leakage will flow harmlessly to the low impedance node. Figure 3 shows a printed circuit pattern that can be used to guard critical pins. Note that traces leading to these pins should also be guarded.

Improper handling or cleaning may increase droop. Contamination from handling parts and circuit boards can be removed with cleaning solvents and de-ionized water.

Power Supplies

The ACF2101 can operate from supplies that range from +4.5V and –10V to ±18V. Since the output voltage integrates negatively from ground, a positive supply of +5V is sufficient to attain specified performance. Using +5V and –15V power supplies reduces power dissipation by one-half of that at ±15V.

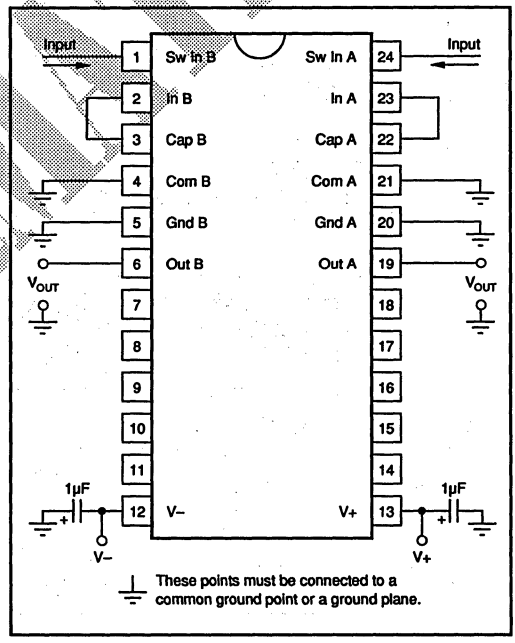


FIGURE 1a. Basic Circuit Connections.

Power supply connections should be bypassed with good high-frequency capacitors, such as 1µF solid tantalum capacitors, positioned close to the power supply pins.

MODES OF OPERATION

The three basic modes of operation of each integrator are controlled by the Hold and Reset switches. In Integrate mode, the output voltage integrates negatively toward –10V. In Hold mode, the output voltage remains at the present value, except for output droop. In Reset mode, the integration capacitor is discharged and the output voltage is driven to analog common. See Figure 4.

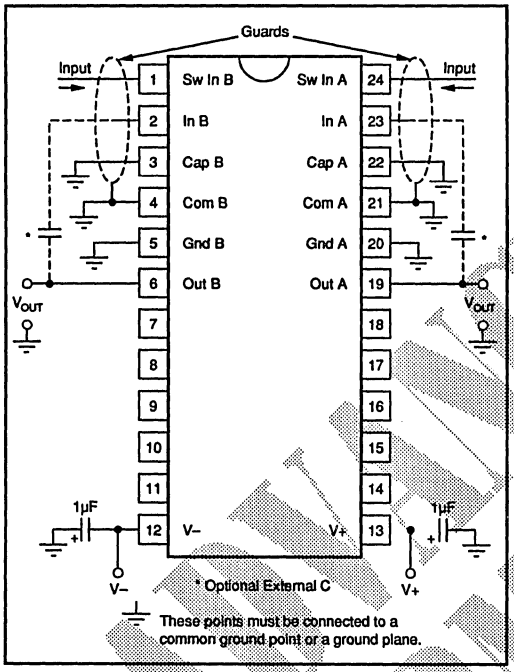


FIGURE 1b. Circuit Connections with External Capacitors and Guarding.

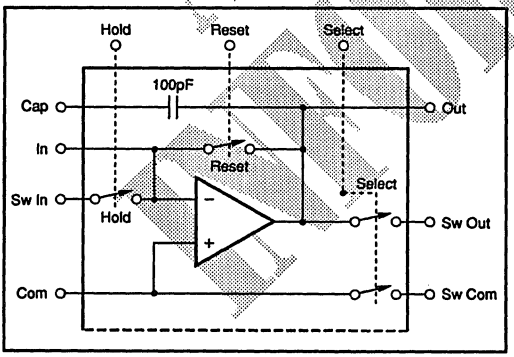


FIGURE 2. Switch Control Lines on One Channel of Two in ACF2101.

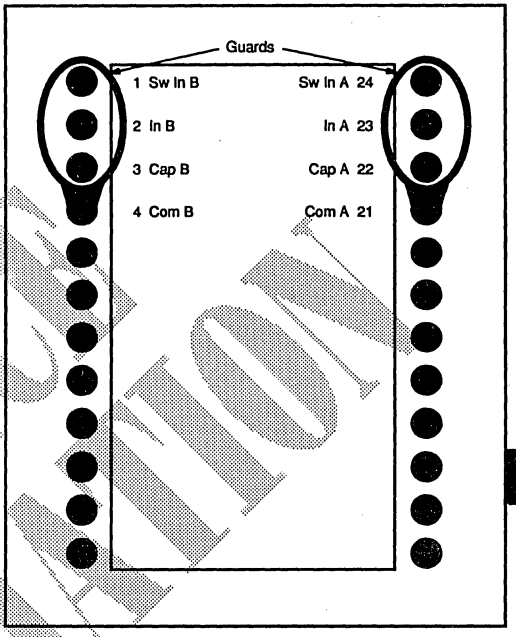
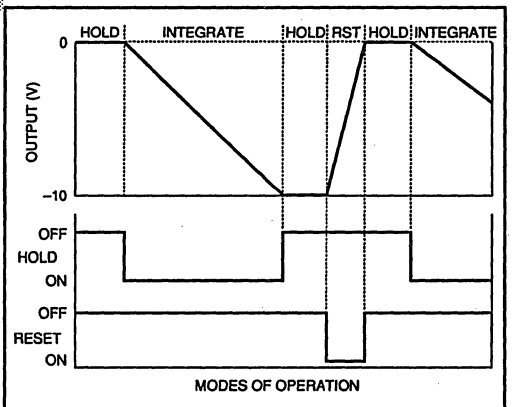


FIGURE 3. PC Board Layout Showing "Guard" Traces for Input. Both top and bottom of board should be guarded.



SWITCH	MODE OF OPERATION		
	Integrate	Hold	Reset
Hold Switch	ON	OFF	ON/OFF
Reset Switch	OFF	OFF	ON

ON: Switch shorted; Logic 0 input. OFF: Switch open; Logic 1 input.

FIGURE 4. Modes of Operation.

SWITCHES

Each integrator includes four switches: a Hold switch, a Reset switch, and two output Select switches. See Figure 2.

Hold and Reset Switches

The Hold switch is intended for low voltage applications, and care must be taken to insure that no more than 100mV are applied across the switch when it is in the off state. To use the Hold switch, connect the input current to the "Sw In" pin. The Hold switch disconnects the input current, and holds the output voltage at a fixed level. For direct input, connect the input current to the "In" pin that bypasses the Hold switch and connects directly to the input summing junction. If the Hold switch is not used, the switch should be in the off mode and the "Sw In" pin should be connected to analog common.

The Reset switch is used to discharge the integration capacitor before the start of a new integration period.

Select Switches

The two Select switches can be used to multiplex the outputs when multiple integrators are connected to a common bus. Figure 5 shows a number of ACF2101s multiplexed together into an A/D converter. The output settling time is determined by the Select switch "on" resistance of 250Ω and the total output capacitance. The total output capacitance includes the ACF2101 output capacitances plus the capacitance of the interconnections to the A/D converter.

OUTPUT VOLTAGE

The integrator output voltage range is from +0.1V to –10V. The output voltage (V_{OUT}) can be calculated as:

$$V_{OUT} = -\frac{i_{IN} \times \Delta t}{C}$$

V_{OUT} = the maximum output voltage (in volts)
C = the integration capacitance (in farads)
i_{IN} = the input current (in amperes)
Δt = the integration time (in seconds)

Examples of Component Values for –10V Output

I_{IN} (μA)	Δt (s)	C (pF)	V_{OUT} (V)
0.01	100m	100	–10
0.1	10m	100	–10
1	1m	100	–10
10	100μ	100	–10
100	10μ	100	–10
10	1m	1000	–10
100	100μ	1000	–10

OUTPUT OVERLOAD

When the output to the ACF2101 integrates to the negative limit, the output voltage smoothly limits at approximately 2.5V from the negative power supply, and reset time will increase by approximately 1μs for overload recovery. For fastest reset time avoid integrating to the negative limit.

EXTERNAL CAPACITOR

An external integration capacitor may be used instead of or in addition to the internal 100pF integration capacitor. Since the transfer function depends upon the characteristics of the integration capacitor, it must be carefully selected. An external integration capacitor should have low voltage coefficient, temperature coefficient, memory, and leakage current. The optimum selection depends upon the requirements of the specific application. Suitable types include NPO ceramic, polycarbonate, polystyrene, and silver mica. If the internal integration capacitor is not used, the CAP pin should be connected to common.

NOISE

The total output noise for a specific application of the ACF2101 is the rms total of the noise in the modes used: Integrate noise (e_{nI}), Hold noise (e_{nH}) and Reset noise (e_{nR}). The noise in both the Hold (e_{nH}) and Reset (e_{nR}) modes is 10μVrms. The noise in the Integrate mode (e_{nI}) is directly proportional to one plus the ratio of C_{IN} to C, where C_{IN} is the capacitance of the circuit at the input of the integrator and C is the integration capacitance:

Integrate output noise (e_{nI}) = (10μVrms) x (1 + C_{IN}/C)

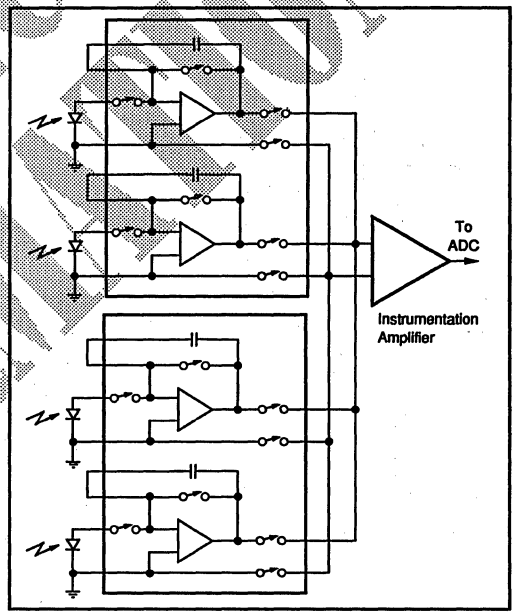


FIGURE 5. ACF2101s in Multiplexer Operation.

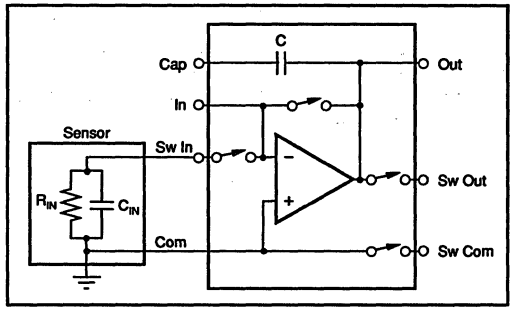


FIGURE 6. Capacitance of Circuit at Input of Integrator.

Therefore, for very low C_{IN}, the Integrate noise will approach 10μVrms. The total noise when in the Hold mode after proceeding through Reset and Integrate modes is calculated as shown below.

$$\text{Total Noise} = \sqrt{e_{nI}^2 + e_{nH}^2 + e_{nR}^2}$$

If only the Integrate and Reset modes are used, the total noise is the rms sum of the noise of the two modes as shown below.

$$\text{Total Noise} = \sqrt{e_{nI}^2 + e_{nR}^2}$$

DYNAMIC CHARACTERISTICS

Frequency Response

The ACF2101 switched integrator is a sampled system controlled by the sampling frequency (fs), which is usually dominated by the integration time. Input signals above the Nyquist frequency (fs/2) create errors by being aliased into the sampled frequency bandwidth. The sampled frequency bandwidth of the switched integrator has a –3dB characteristic at fs/2.25 and a null at fs and harmonics 2fs, 3fs, 4fs, etc. This characteristic is often used to eliminate known interference.

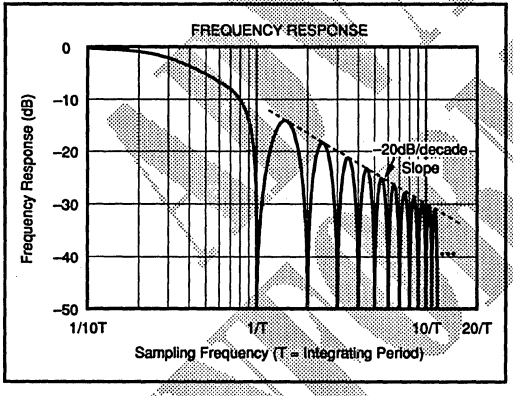


FIGURE 7. Frequency Response.

Charge Transfer

Charge transfer is the charge that is coupled from the logic control inputs through circuit capacitance to the integration capacitor when the Hold and Reset switches change mode. Careful printed circuit layout must be used to minimize external coupling from digital to analog circuitry and the resulting charge transfer. Charge transfer results in a DC charge offset error voltage. The ACF2101 switches are compensated to reduce charge transfer errors.

Since the ACF2101 switches contribute equal and opposite charge for positive and negative logic input transitions, the total error due to charge transfer is determined by the switching sequence. For each switch, a logic transition

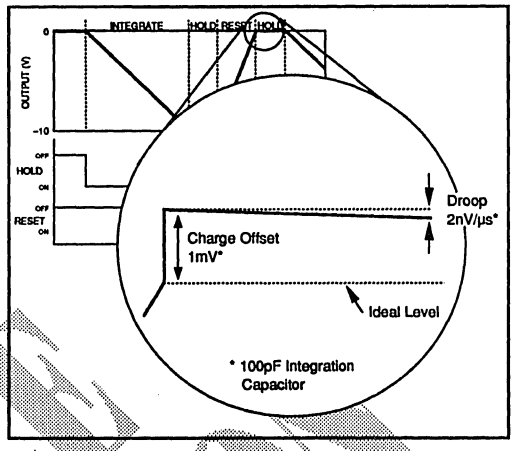


FIGURE 8. Droop and Charge Offset Effects.

results in a specific charge (and offset voltage) while an opposite going logic transition results in an opposite charge (and opposite offset voltage). Thus, if the Hold switch is turned on and off during one integration cycle, the total charge transfer at the end of the sequence due to the Hold switch is essentially zero.

The amount of charge transfer to the integration capacitor is constant for each switch. Therefore, the charge offset error voltage is lower for larger integration capacitors. The ACF2101's 0.1pC charge transfer results in a 1mV charge offset voltage when using the 100pF internal integration capacitor. The offset voltage will change linearly with the integration capacitance. That is, 50pF will result in a 2mV charge offset and 200pF in a 0.5mV charge offset.

Droop

Droop is the change in the output voltage over time as a result of the bias current of the amplifier, leakage of the integration capacitor and leakage of the Reset and Hold switches. Droop occurs in both the Integrate and Hold modes of operation. Careful printed circuit layout must be used to minimize external leakage currents as discussed previously.

The droop is calculated by the equation:

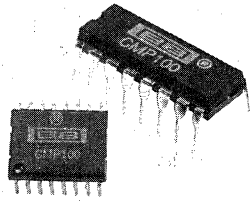
$$\text{Droop} = \frac{200\text{fA}}{C}$$

where C is the integration capacitance in farads and the result is in volts per second. For the internal integration capacitance of 100pF, the droop is calculated as:

$$\text{Droop} = \frac{200 \times 10^{-15}}{100 \times 10^{-12}} = 2\text{mV/s or } 2\text{nV/}\mu\text{s}$$

Droop increases by a factor of 2 for each 10°C increase above 25°C.

BURR-BROWN®

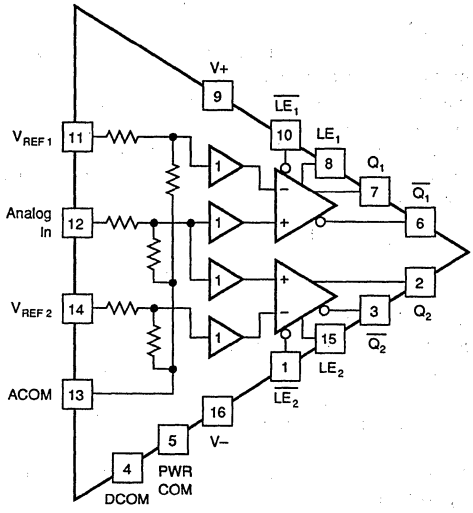


CMP100

HIGH-SPEED WINDOW COMPARATOR ATE PIN RECEIVER

FEATURES

- PROPAGATION DELAY: 5ns max, 100mV Overdrive
- COMMON MODE INPUT RANGE: ±12V
- INPUT IMPEDANCE: 120kΩ || 2pF
- OUTPUTS: Latchable, 10k ECL Compatible
- COMPLETE: No External Parts Required
- TEMPERATURE RANGE: –25°C to +85°C
- PACKAGES: 16-Pin Plastic DIP, 16-Lead Plastic SOIC



APPLICATIONS

- ATE PIN RECEIVER
- WINDOW COMPARATOR
- THRESHOLD DETECTOR

DESCRIPTION

CMP100 is a high-speed dual comparator designed for use as an automatic test system pin receiver. It is also useful in a wide variety of analog threshold detector and window comparator applications.

CMP100 has two reference inputs and one analog input which is common to both comparators. All inputs are attenuated by a voltage divider to provide high common mode voltage operation. The analog input attenuator is R-C tuned to optimize operation with high-speed input waveforms. The reference input attenuators are not R-C tuned. Each attenuator network is followed by a buffer amplifier ahead of the comparator circuits.

Complementary ECL output stages are capable of driving 50Ω terminated transmission lines to a –2V pull-down voltage. In addition, latch-enable inputs are provided for each comparator, allowing operation as a sampling comparator.

CMP100 is available as an industrial temperature range device, –25°C to +85°C, and is packaged in a 16-pin plastic DIP and in a 16-lead plastic SOIC.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1075

SPECIFICATIONS

ELECTRICAL

T_A = 25°C and at rated supplies: V+ = +5V, V– = –5.2V unless otherwise noted.

PARAMETER	CMP100AP, AU MIN	TYP	MAX	UNITS
ANALOG INPUTS				
Differential Input Voltage Range		24		V
Common Mode Voltage Range		±12		V
Resistance				
Reference Inputs: $V_{REF\,1}$, $V_{REF\,2}$	45	60	75	kΩ
Analog Input	90	120	150	kΩ
Capacitance, All Inputs		2		pF
TRANSFER CHARACTERISTICS				
ACCURACY				
Input Offset Voltage, V_{OS}[1]		10	20	mV
Common Mode Error			10	mV/V
Voltage Offset Drift		100	250	µV/°C
Power Supply Sensitivity of Offset: $\Delta V_{OS}/\Delta V+$			±10	µV/V
$\Delta V_{OS}/\Delta V-$			±10	µV/V
RESPONSE TIME				
Propagation Delay, t_{PD}[2, 3]				
100mV Overdrive, Latch Disabled		3.6	5	ns
DIGITAL SIGNALS[4] (Over Specification Temperature Range)				
Inputs (Latch Controls)				
Logic Levels: V_{IH}	–1.1			V
V_{IL}			–1.5	V
I_{IH} (V_I = –1.1V)			50	µA
I_{IL} (V_I = –1.5V)			5	µA
Outputs (Balanced)				
Logic Levels: V_{OL} (50Ω Load to –2V)			–1.5	V
V_{OH} (50Ω Load to –2V)	–1.1			V
POWER SUPPLY REQUIREMENTS				
Supply Voltage				
V+	+4.75	+5	+5.25	VDC
V–	–5.45	–5.2	–4.95	VDC
Supply Current[5]				
V+		+30	+40	mA
V–		–40	–50	mA
Power Dissipation[6]		360	460	mW
TEMPERATURE RANGE				
Specification	–25		+85	°C
Storage	–65		+150	°C

NOTES: (1) Defined as half the magnitude between low-to-high and high-to-low transition input voltages. (2) See section on "Measuring CMP100 Performance." (3) See "Discussion of Specifications" for exact conditions. (4) 10k ECL compatible. (5) Maximum supply current is specified at typical supply voltages. (6) Maximum Power Dissipation is calculated with typical supply voltages and maximum currents. Note that dissipation in the output transistors from driving 50Ω ECL loads will increase the total power dissipation by about 50mW.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common and Power Common ..... +6V
V– to Digital Common and Power Common ..... –6V
(V+) – (V–) 12V
Digital Inputs to Digital Common
Differential ..... ±4V
Common Mode ..... V– to V+
Differential Analog Input Voltage ..... ±25V
Package Power Dissipation 750mW
Storage Temperature ..... –60°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

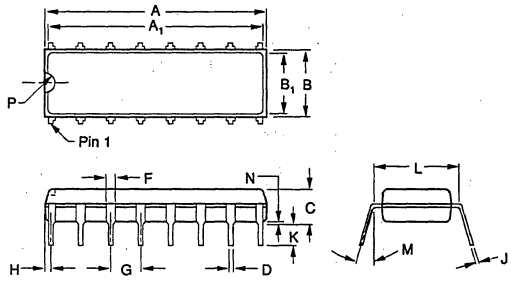
Stresses exceeding those listed above may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN DEFINITIONS

PIN	NAME	DESCRIPTION
1, 15	$\overline{LE2}$, $\overline{LE2}$	LATCH or UNLATCH comparator 1 outputs
2, 3	Q2, $\overline{Q2}$	ECL outputs of comparator 2
4	DCOM	Return for comparator circuits
5	PWRCOM	Return for ECL output transistor currents
6, 7	$\overline{Q1}$, Q1	ECL outputs of comparator 1
8, 10	$\overline{LE1}$, LE1	LATCH or UNLATCH comparator 2 outputs
9	V+	Positive Supply Voltage, +5V
11	$V_{REF\,1}$	Reference Voltage for comparator 1
12	Analog In	Analog Signal input
13	ACOM	Return for Analog In, $V_{REF\,1}$, $V_{REF\,2}$
14	$V_{REF\,2}$	Reference voltage for comparator 2
16	V–	Negative Supply Voltage: (ECL Supply, –5.2V)

MECHANICAL

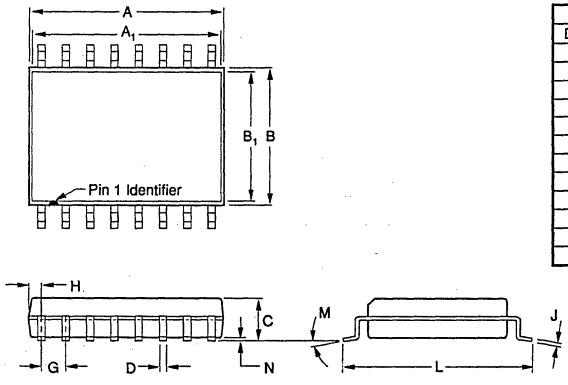
P Package — 16-Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.740	.800	18.80	20.32
A1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	0.20	.050	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

P Package — 16-Pin SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.400	.416	10.16	10.57
A1	.388	.412	9.86	10.46
B	.286	.302	7.26	7.67
B1	.268	.286	6.81	7.26
C	.093	.109	2.36	2.77
D	.015	.020	0.38	0.51
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.391	.421	9.93	10.69
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

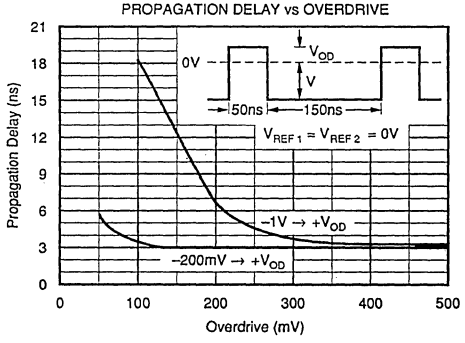
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

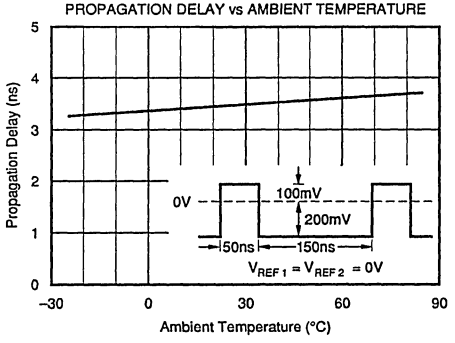
ORDERING INFORMATION

MODEL	PACKAGE
CMP100AP	16-Pin DIP
CMP100AU	16-Lead SOIC

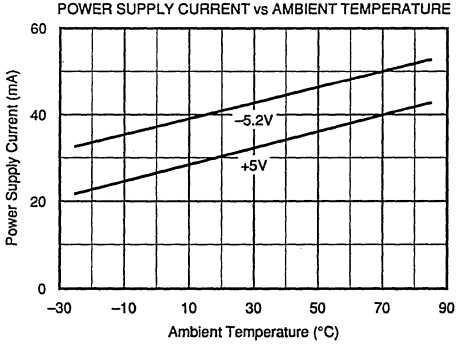
TYPICAL PERFORMANCE CURVES

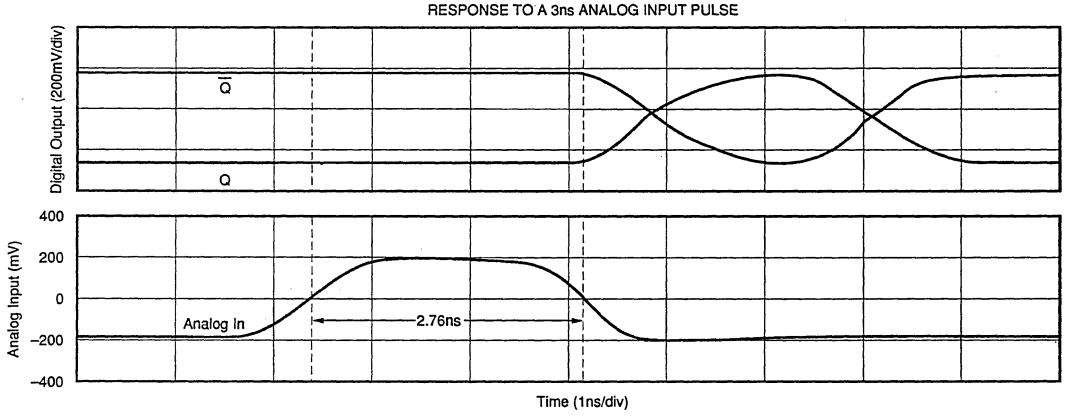
T_A = 25°C and at rated supplies: V+ = +5V, V– = –5.2V unless otherwise noted.





NOTE: Propagation Delay vs Overdrive is shown for two amplitudes of input pulse: from –200mV → +V_{OD} (0.2nV/ns slew rate) and –1V → +V_{OD} (1V/ns slew rate). For an inverse input waveform: from +1V → –V_{OD} and from +200mV → –V_{OD}, propagation delays identical to those above are produced.

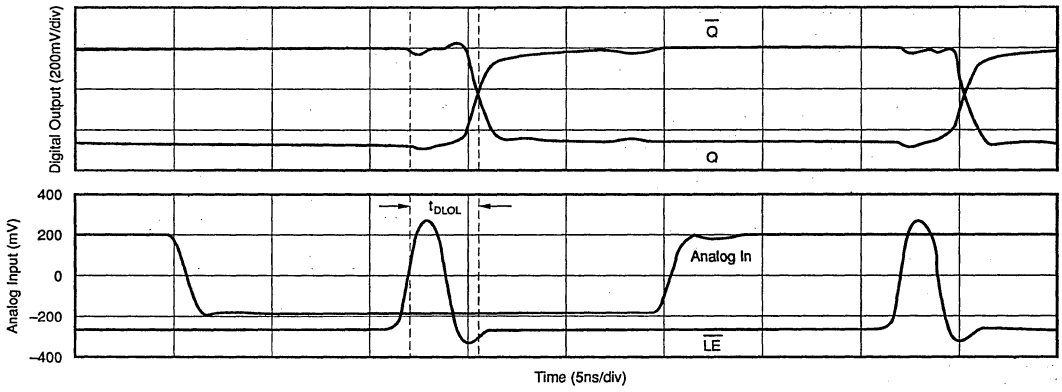




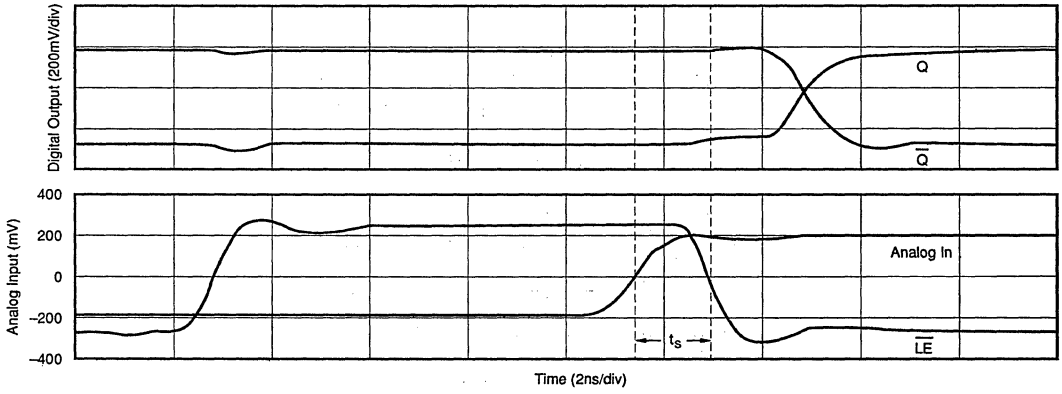
TYPICAL PERFORMANCE CURVES (CONT)

T_A = 25°C and at rated supplies: V+ = +5V, V– = –5.2V unless otherwise noted.

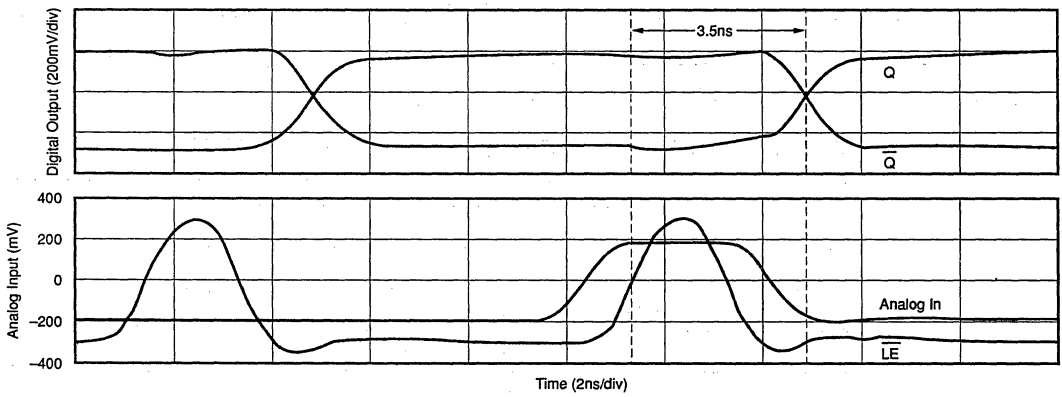
RESPONSE TO A 2ns LATCH ENABLE PULSE



SETUP TIME, t_S



CAPTURING A NARROW ANALOG PULSE



DISCUSSION OF SPECIFICATIONS

ANALOG INPUT

Offset Voltage, V_{OS}

The value of the the comparison threshold for V_{REF1} or V_{REF2} = 0V. V_{OS} and maximum drift vs temperature of V_{OS} are guaranteed.

Common Mode Error

As V_{REF} varies over its range, there is a small gain error which manifests itself as a change in the comparison level. Common mode error drifts typically –15µV/°C.

DYNAMIC PERFORMANCE

Figure 1 illustrates the following analog and logic performance definitions.

Input to Output High Propagation Delay, t_{PDH}

t_{PDH} is the propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output (Q output) Low-to-High transition. Output logic is not latched for this definition.

Input to Output Low Propagation Delay, t_{PDL}

t_{PDL} is the propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output (Q output) High-to-Low transition. Output logic is not latched for this definition.

The propagation delay of the CMP100 is virtually identical for negative going and positive going analog input edges.

Differential Propagation Delay (Skew), t_{DIFF}

t_{DIFF} is the difference in propagation delay from one comparator to another. The skew between each half of one CMP100 is no greater than 200ps.

Propagation Delay Dispersion

Propagation Delay Dispersion is the variation in propagation delay versus input overdrive. Note that propagation delay may also be a function of input slew rate and of the previous level.

The input waveform for the propagation delay specification is illustrated in the first typical performance curve, Propagation Delay vs Overdrive. The Propagation Delay listed in the Electrical Specifications table is specified using an input waveform with 100mV overdrive, a previous level of –200mV and a slew rate of 200V/µs. A typical propagation delay curve is also shown for a previous level of –1V. The outputs are not latched for this specification.

Overdrive

Overdrive is the voltage by which the input exceeds $V_{REF} \pm V_{OS}$.

Minimum Set-Up Time, t_S

t_S is the minimum time before the positive transition of the Latch Enable (LE) that an analog input signal change must be present in order to be acquired and held at the outputs.

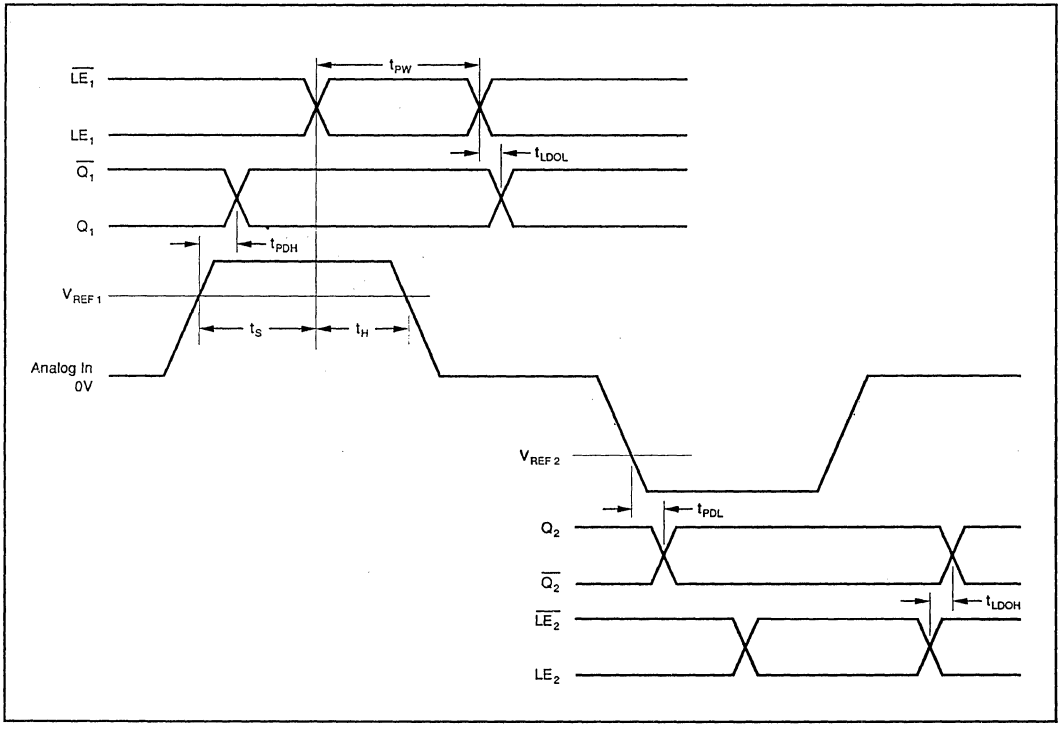


FIGURE 1. Analog and Logic Timing Definitions.

The t_S performance of CMP100 is illustrated in the Typical Performance Curves.

Minimum Hold Time, t_H

t_H is the minimum time after the positive transition of the Latch Enable (LE) that an analog input signal change must remain unchanged in order to be acquired and held at the outputs. t_H = 0 for CMP100.

LOGIC PERFORMANCE DEFINITIONS

Latch Enable to Output High Delay, t_{DLOH}

t_{DLOH} is the propagation delay of latch logic circuits measured from the 50% point of the Latch Enable signal (LE) High-to-Low transition to the 50% point of an output (Q) Low-to-High transition.

Latch Enable to Output Low Delay, t_{DLOL}

t_{DLOL} is the propagation delay of latch logic circuits measured from the 50% point of the Latch Enable signal High-to-Low transition to the 50% point of an output (Q) High-to-Low transition.

Minimum Latch Enable Pulse Width, t_{PW}

t_{PW} is the minimum time that the Latch Enable (LE) must be High in order to acquire and hold an input signal change.

The actual timing performance of CMP100 is illustrated in the Typical Performance Curves.

OPERATING CONSIDERATIONS

INPUT VOLTAGE

Input reference voltages $V_{REF\ 1}$ and $V_{REF\ 2}$ may vary from –12V to +12V. The frequency-compensated analog input network can also swing from –12V to +12V.

Care must be taken to be sure that the Maximum Differential Input Voltage is not exceeded. That is, the voltage between Analog In and $V_{REF\ 1}$ or between Analog In and $V_{REF\ 2}$ must not exceed ±25V. If this voltage is exceeded by 1 or 2 volts, even momentarily, emitter-base voltage breakdown of the input transistors will occur and cause a permanent shift of the offset voltage, V_{OS}, to an out-of-spec value. However, the CMP100 will continue to function and will not be destroyed.

Input voltages to the CMP100 of uncontrolled magnitude may occur during system power-up. Take care to assure that the Absolute Maximum Differential Input Voltage is not exceeded during power-up.

DRIVING SOURCE IMPEDANCE

An apparent slow response of the CMP100 may be due a combination of high source impedance and stray capacitance to ground at the analog input. An R-C combination of 1kΩ source resistance and 10pF to ground results in a 10ns time constant—more than double the typical response time of the CMP100.

THE LATCH FUNCTION

The latch function is used for sampling the state of the outputs and holding them until the output can be processed.

Figure 1 shows a timing diagram for differential input latch enable controls, LE and $\overline{LE}$. The latches of the CMP100 are transparent type latches. If LE is Low ($\overline{LE}$ is High), the Q outputs indicate the sign of the input difference voltage. When LE goes High ($\overline{LE}$ Low), the comparator outputs are held at the current state.

When the analog input signal passes through the reference level, the comparator output Q changes, after a time of t_{PDH} or t_{PDL}. However, if the output is to be latched, the input signal must have crossed the threshold for a time t_S (set-up time) before the rising edge of LE occurs in order to capture the correct output state. On the other hand, in order to capture a correct output state just before it changes, it is necessary to maintain that output state for t_H, (hold time) after the rising edge of LE. t_H = 0 for CMP100.

A minimum latch pulse width of t_{PW} is needed to capture the state of narrow pulses. See the Typical Performance Curves for an example of sampling a narrow pulse.

10k ECL LOGIC

If the latching function is not used, the Latch Enable inputs ($\overline{LE_1}$ and $\overline{LE_2}$) should be returned to an ECL High voltage (–0.8V) or to Digital Common (0V). LE_1 and LE_2 should be returned to an ECL Low level (–1.8V), to an ECL bias voltage (–1.3V) or to the –2V 50Ω load pull-down power supply. Connecting an ECL input to –5.2V may create a marginal transistor emitter-base breakdown situation over the ambient temperature range and is not recommended.

If a single (non-differential) ECL logic input is used, connect the complementary input to an ECL bias voltage (–1.3V).

100k ECL LOGIC

The negative power supply, V–, of the CMP100 can be operated at –4.5V. The common mode input range of the analog and reference inputs will be reduced to +12V to –7.5V. Output levels are not affected by changing the V– power supply voltage to –4.5V.

TTL INPUTS

The operating common mode range of a logic input is –2V to +2V. Thus one can bias the logic inputs to use them with TTL inputs if the High input level is maintained below +2V. In this case, the complementary logic input should be biased at the TTL threshold of +1.4V.

LEVEL SHIFTING ECL to TTL

The ECL outputs can be translated to TTL using a Motorola MC10125 Quad ECL-TTL translator. The logic delay t_{DLOH} and t_{DLOL} and the propagation delay t_{PDL} and t_{PDH} will be increased by the delay of the translator.

INSTALLATION

TERMINATING ECL OUTPUTS

The best performance will be achieved with the use of proper ECL terminations. Such a configuration is illustrated in Figure 3. The open-emitter outputs of the CMP100 are designed to be terminated through 50Ω resistors to –2V or any other equivalent termination. If high-speed ECL signals must be routed more than a few centimeters, MicroStrip or StripLine techniques may be required to insure proper transition times and prevent output ringing.

POWER SUPPLY SELECTION

Linear power supplies are preferred. Although switching power supply rms specifications may appear to indicate low noise output, voltage spikes generated by switchers may be hard to filter. Their high-frequency components may be extremely difficult to keep out of the power supply return system. If switchers must be used, their outputs must be carefully filtered and the power supply itself should be shielded and located as far away as possible from precision analog circuits.

PRINTED CIRCUIT LAYOUT CONSIDERATIONS

Power Supply Wiring

Use heavy power supply and power supply common (ground) wiring. A ground plane under the part is usually the best solution for preserving dynamic performance and reducing noise coupling into sensitive circuits.

When passing power through a connector, use every available spare pin for making power supply return connections, and use some of the pins as a Faraday shield to separate the Analog and Digital Common lines.

Power Supply Returns (ACOM, DCOM and PWRCOM)

For best performance, connect ACOM (pin 13) and DCOM (pin 4) to the ground plane under the comparator. PWRCOM (pin 5), which is connected to the collectors of the ECL outputs, can be returned by separate printed circuit trace but its inductance should be kept low to avoid ringing. Do not connect ACOM and DCOM together at the end of a long printed circuit trace and then run a single wire to the power supply. To use separate ACOM and DCOM return printed circuit traces, connect a 1µF to 47µF tantalum capacitor between DCOM and ACOM pins as close to the package as possible.

Power Supply Bypassing

Every power supply line leading into the comparator must be bypassed to the Common pins. The bypass capacitor should be located as close to the comparator package as possible and tied to a solid return, preferably to the ground plane under the device. If the capacitors are not close enough to the package, DC resistance and inductance may be above acceptable levels. Use tantalum capacitors with values of from 1µF to 10µF. Parallel them with smaller ceramic ca-

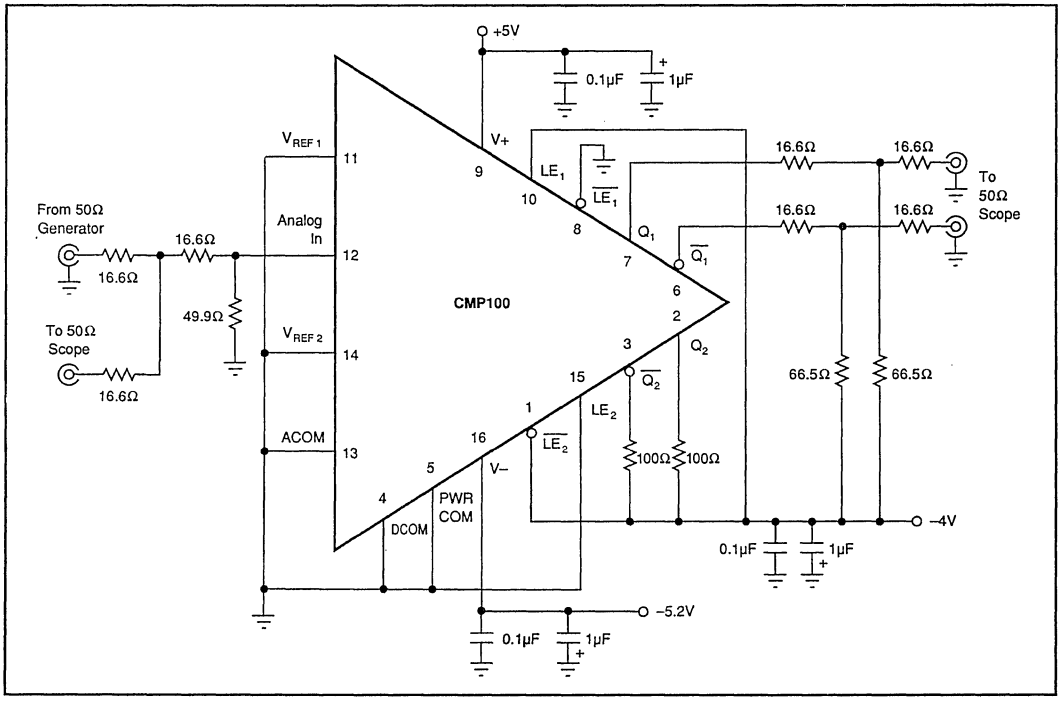


FIGURE 2. Circuit for Evaluating Analog Propagation Delay, t_{PDH}, t_{PDL}.

pacitors for high frequency filtering if necessary. Electrolytic capacitors are not recommended because their high frequency response is poor.

Separate the Analog and Digital Signals

Digital signal paths entering or leaving the layout should have minimum length to minimize crosstalk to analog wiring. Stray capacitive feedback from digital outputs to the analog input may cause the outputs to appear fuzzy well after the outputs have changed. Keep analog signals as far away as possible from digital signals. If they must cross, cross them at right angles. Coaxial cable may be necessary for analog inputs in some situations.

MEASURING CMP100 PERFORMANCE

USING AN OSCILLOSCOPE

Oscilloscope probes should be matched to the oscilloscope. Use an oscilloscope with at least 400MHz bandwidth.

Be sure the probe compensation is adjusted properly. Improper compensation will result in apparent overshoot and/or ringing if undercompensated, and an apparent slow edge if overcompensated. If the probe ground lead is too long, the output may appear distorted and oscillatory. Use probes with short (less than one inch) ground straps or use a coaxial cable connection instead of a probe. Do not use X1 or "straight" probes. Their bandwidth is 20MHz or less and capacitive loading is high. The best method is to use 50Ω matched terminations as shown in Figures 2 and 3.

MEASURING PROPAGATION DELAY

Figure 2 shows a circuit configuration used for evaluating propagation delay. It uses 50Ω matched terminations between the instruments and the CMP100 for best signal integrity. An HP8130A Pulse Generator is used for the analog input and for the latching signals. The oscilloscope is an HP54503A 500MHz Digitizing Oscilloscope. This setup was used to generate the dynamic performance waveforms in the Typical Performance Curves section.

MEASURING LOGIC TIMING

Figure 3 shows the circuit configuration used for evaluating logic propagation delay. The logic input LE1 has been added to the circuit of Figure 2.

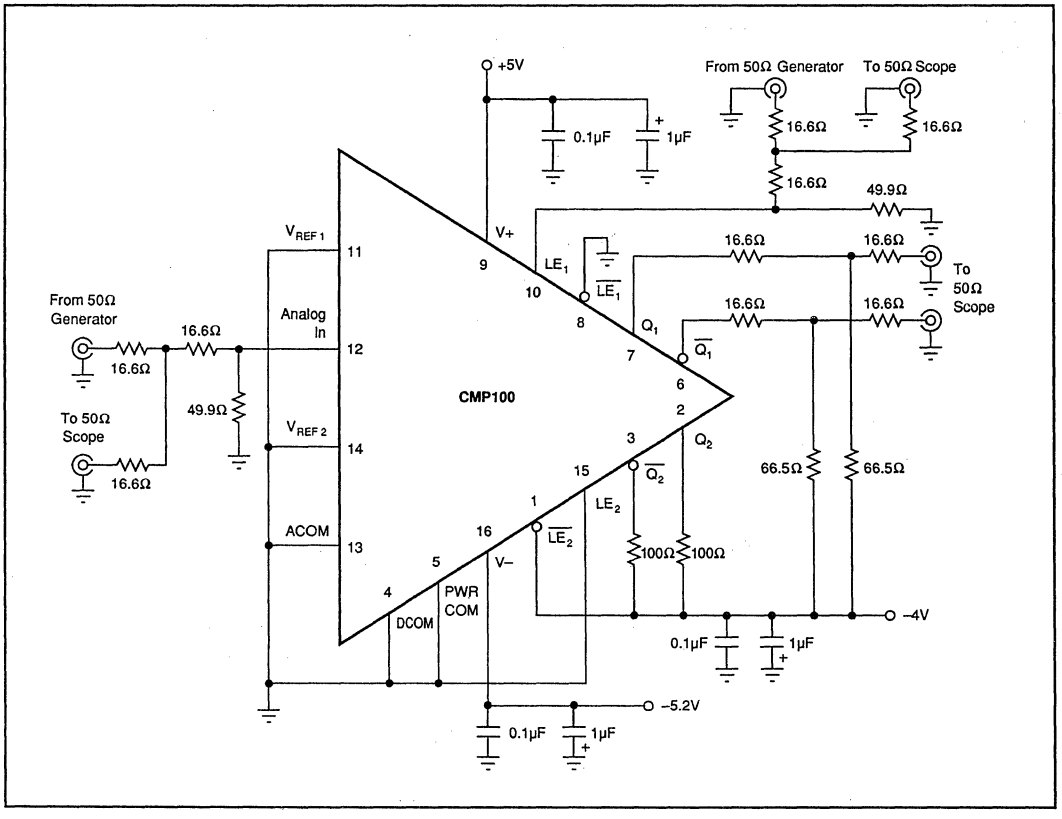


FIGURE 3. Circuit for Evaluating Logic Timing.

CMP100 APPLICATIONS

ATE PIN RECEIVER

A typical ATE pin receiver application using CMP100 is illustrated in Figure 4. The reference inputs, V_{REF1} and V_{REF2} are driven by D/A converters (Figure 5) while analog input is driven directly from the device under test (DUT).

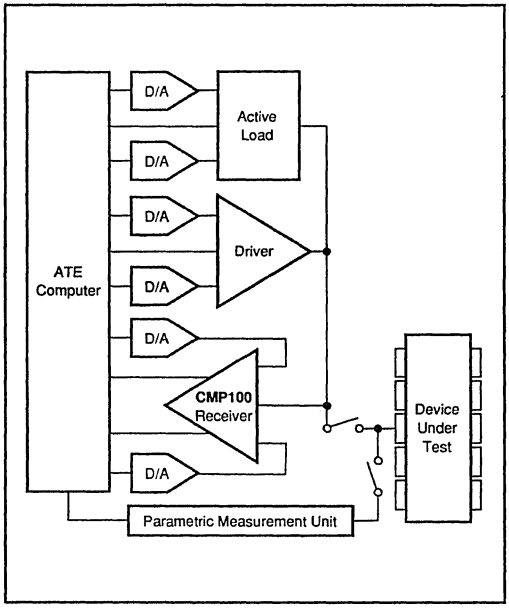


FIGURE 4. Typical ATE Pin Receiver Application.

WINDOW COMPARATOR

Because of its high speed, the CMP100 can be used to make timing measurements on modest-speed digital or high-speed analog waveforms. When the outputs of the CMP100 are combined with a NOR gate, a true window comparator function is implemented. Refer to gate G3 of Figure 6. The output pulse width generated by an input signal passing through the reference levels can be measured. This could be for a rise-time/fall-time measurement (setting the reference levels at 10% and 90% of the signal height) of a modest speed digital waveform, or for the width (and hence the value) of an analog ramp moving between two values from an integrating type signal detector.

PULSE RECOVERY

The window comparator function can also be used to reconstruct pulses that have been degraded. Positive and/or negative reference levels can be set up to detect both High and Low levels of the pulse.

A plot of the response of CMP100 to a narrow pulse with V_{REF1} = 0V is shown in the Typical Performance Curves section.

DETECTING TRANSIENTS

CMP100 can be connected to Detect and Hold transient occurrences above and below threshold voltages set by V_{REF1} and V_{REF2} as illustrated in Figure 6. The outputs of comparator 1 and comparator 2 are fed back to their LE inputs in order to self-latch their outputs. The Reset control is used to "unlock" the outputs after the transient occurrence has been read. The output NOR gate G3 combines CMP100 outputs into a single-output window comparator function.

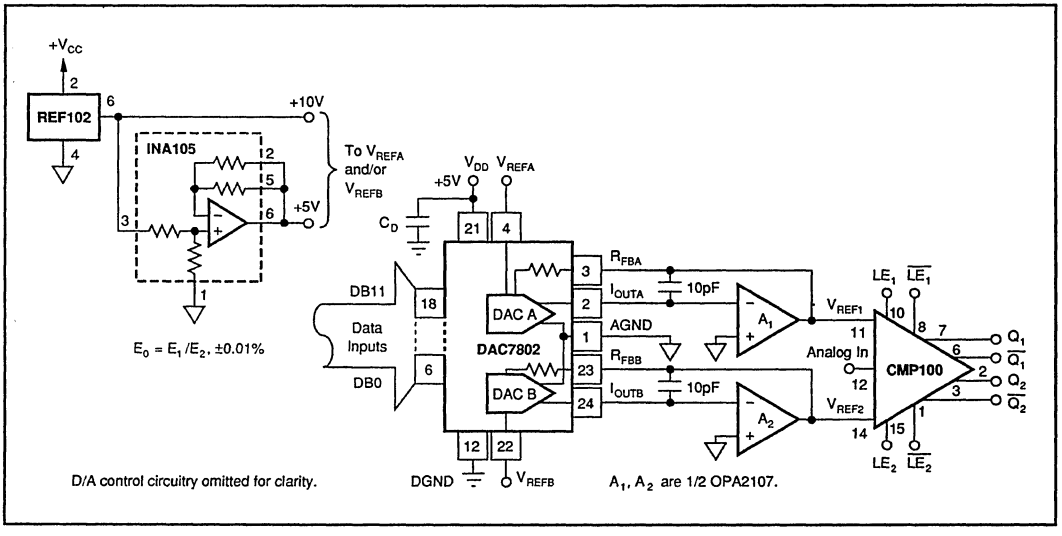


FIGURE 5. Dual DAC7802 (12-bit port), DAC7801 (8-bit port) or DAC7800 (serial port) D/A Converters Supply Reference Inputs to the CMP100. For higher resolution use DAC725, dual 16-bit D/A converter.

Note that the transient being detected must remain above $V_{REF\,1}$ (or below $V_{REF\,2}$) longer than the propagation delay of the CMP100 plus the propagation delay of gates G1 and G2.

In an application where only one polarity of transient needs to be captured, comparator 2 (not latched) can be used as the source of the Reset control signal to unlock comparator 1 based on a different threshold condition (defined by $V_{REF\,2}$) on the analog input signal. This connection will stretch the transient occurrence for the time the $V_{REF\,2}$ condition is present.

WIDE-BAND AMPLIFIERS FOR ANALOG INPUT SIGNAL CONDITIONING

In a component test application the analog input of the CMP100 is usually driven directly from the DUT output. Other applications may require a high-speed buffer or voltage gain ahead of the CMP100. Recommended wide-bandwidth amplifiers are Burr-Brown OPA603 for up to ±10V signals, or OPA620/OPA621 for very wide-band ±3V signals. A high speed instrumentation amplifier such as the Burr-Brown INA110 can be used for common mode rejection.

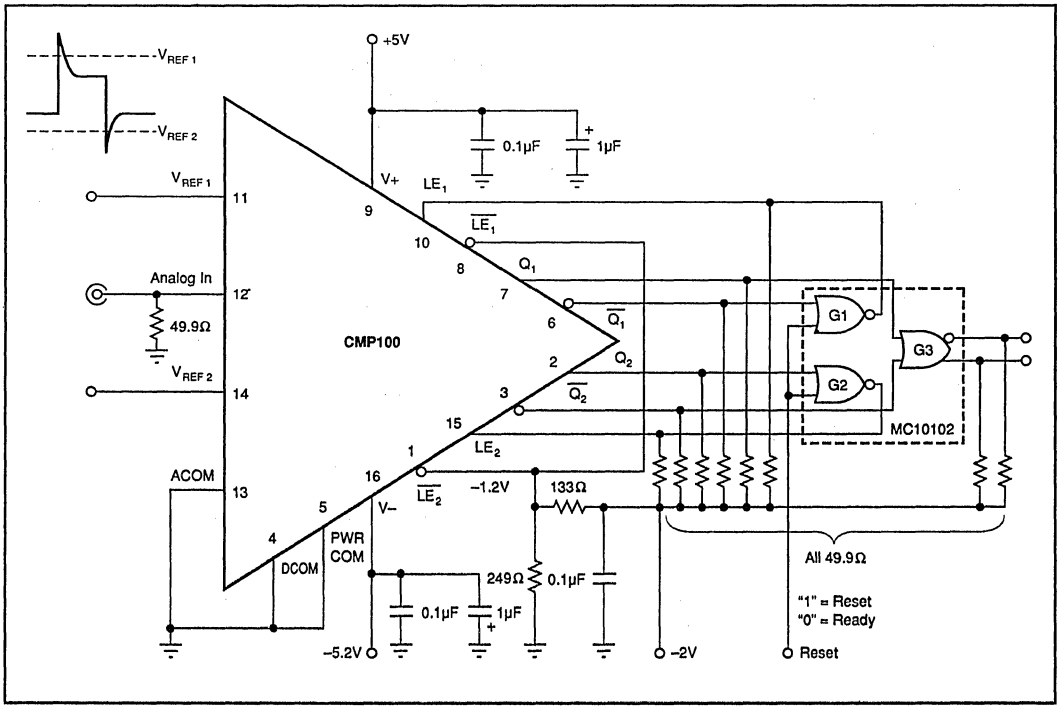
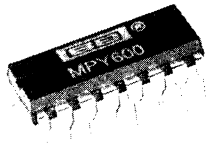


FIGURE 6. CMP100 Used to Detect and Hold Transient Occurrences on the Output Pulse of a Device Under Test, or Out-of-Limits Conditions in a Process-Variable Monitoring Application.

BURR-BROWN®



MPY600

Wide Bandwidth SIGNAL MULTIPLIER

FEATURES

- WIDE BANDWIDTH:
  75MHz — Current Output
  30MHz — Voltage Output
- LOW NOISE
- LOW FEEDTHROUGH: –60dB (5MHz)
- GROUND-REFERRED OUTPUT
- LOW OFFSET VOLTAGE

APPLICATIONS

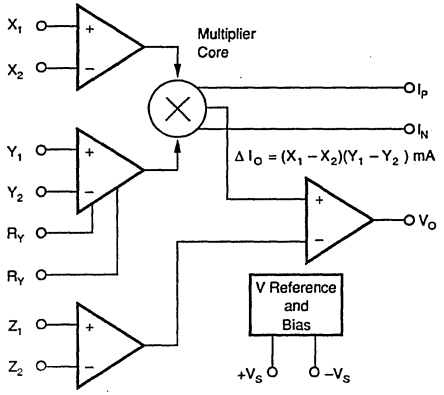
- MODULATOR/DEMODULATOR
- VIDEO SIGNAL PROCESSING
- CRT GEOMETRY CORRECTION
- CRT FOCUS CORRECTION
- VOLTAGE-CONTROLLED CIRCUITS

DESCRIPTION

The MPY600 is a wide-bandwidth four-quadrant signal multiplier. Its output voltage is equal to the algebraic product of the X and Y input voltages. For signals up to 30MHz, the on-board output op amp provides the complete multiplication function with a low-impedance voltage output. Differential current outputs extend multiplier bandwidth to 75MHz.

The MPY600 offers improved performance compared to common semiconductor modulator or multiplier circuits. It can be used for both two-quadrant (voltage-controlled amplifier) and four-quadrant (double-balanced) applications. While previous devices required cumbersome circuitry for trimming, balance and level-shifting, the MPY600 requires no external components. A single external resistor can be used to program the conversion gain for optimum spurious-free dynamic range. When used as a modulator, carrier feedthrough measures –60dB at 5MHz.

Differential X, Y and Z inputs can be connected in a variety of useful configurations, including squarer, divider, and square-rooter circuits. The MPY600 is available in 16-pin plastic DIP, specified for the industrial temperature range.



$$V_O = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{2V} + Z_2 - Z_1\right]$$

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

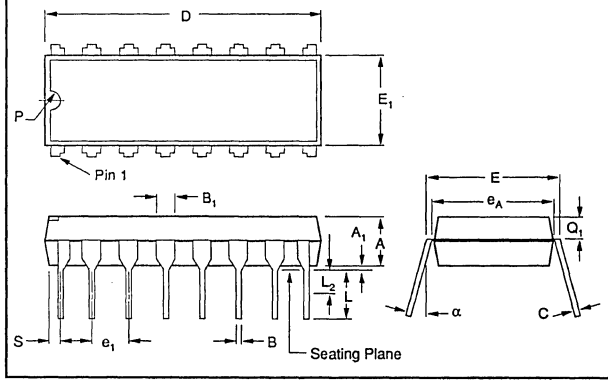
At V_S = ±5V, T_A = +25°C unless otherwise noted.

SPECIFICATION	CONDITIONS	MPY600AP MIN	MPY600AP TYP	MPY600AP MAX	UNITS
INPUTS (X, Y, Z)					
Full-Scale Differential Input					
X_1-X_2		±1			V
Y_1-Y_2		±2			V
Z_1-Z_2		±2			V
Input Voltage Range			±2.2		V
Differential Input Range			±2.5		V
Input Impedance			100 || 1.5		kΩ || pF
Input Offset Voltage			±0.5	±5	mV
Drift			25		µV/°C
CMRR	V_{CM} = ±2V		70		dB
PSRR			70		dB
Input Bias Current (X, Y)			+15		µA
Z Input			−15		µA
VOLTAGE OUTPUT					
Transfer Function			$V_O = \frac{(X_1-X_2)(Y_1-Y_2)}{2} + Z_2$		
Total Multiplier Error[1]	−1V ≤ X ≤ 1V, −2V ≤ Y ≤ 2V		±15	±25	mV
	−2V ≤ X ≤ 2V, −2V ≤ Y ≤ 2V		±25		mV
Gain Error			±1		%
Gain Temperature Drift			±200		ppm/°C
Power Supply Rejection	V_S = ±4 to ±6V		70		dB
Noise	f = 1kHz to 30MHz		120		nV/√Hz
Output Voltage Swing	R_L = 100Ω	±2.2	±3		V
Output Current		±22	±30		mA
Short-Circuit Limit			50		mA
Bandwidth	Small Signal		30		MHz
Slew Rate			150		V/µs
Settling Time to 0.1%	4V Step		150		ns
Differential Gain Error	3.58MHz, 0 to 0.7V		0.2		%
Differential Phase Error	3.58MHz, 0 to 0.7V		0.2		Degrees
Capacitive Load, Max	Stable Operation		100		pF
Feedthrough, X	X = 0dBm, f = 500kHz; Y Nulled		−65		dB
	X = 0dBm, f = 5MHz; Y Nulled		−60		dB
Feedthrough, Y	Y = 0dBm, f = 500kHz; X Nulled		−70		dB
	Y = 0dBm, f = 5MHz; X Nulled		−50		dB
Distortion, X	X = 0dBm, f = 500kHz, Y = 2V		−60		dB
	X = 0dBm, f = 5MHz, Y = 2V		−55		dB
Distortion, Y	Y = 0dBm, f = 500kHz, X = 2V		−65		dB
	Y = 0dBm, f = 5MHz, X = 2V		−55		dB
CURRENT OUTPUT					
Transfer Function			$\Delta I_O = (X_1 - X_2)(Y_1 - Y_2)$		mA
Total Multiplier Error[1]	−1V ≤ X ≤ 1V, −2V ≤ Y ≤ 2V		±20	±80	µA
	−2V ≤ X ≤ 2V, −2V ≤ Y ≤ 2V		±80		µA
Gain Error			±1		%
Gain Temperature Drift			±200		ppm/°C
Power Supply Rejection	V_S = ±4 to ±6V		50		dB
Noise, Output			100		pA/√Hz
Voltage Compliance Range			±2.5		V
Peak Output Current			5		mA
Noise, Input-Referred	f = 1kHz to 75MHz		50		nV/√Hz
Bandwidth, Small-Signal			75		MHz
Settling Time to 0.1%	4mA Step		150		ns
Feedthrough, X	X = 0dBm, f = 1MHz; Y Nulled		−65		dB
	X = 0dBm, f = 10MHz; Y Nulled		−45		dB
Feedthrough, Y	Y = 0dBm, f = 1MHz; X Nulled		−75		dB
	Y = 0dBm, f = 10MHz; X Nulled		−55		dB
Distortion, X	X = 0dBm, f = 1MHz, Y = 2V		−55		dB
	X = 0dBm, f = 10MHz, Y = 2V		−50		dB
Distortion, Y	Y = 0dBm, f = 1MHz, X = 2V		−65		dB
	Y = 0dBm, f = 10MHz, X = 2V		−50		dB
POWER SUPPLY					
Rated Performance			±5		V
Operating		±4.75		±8	V
Current			±30	±35	mA
TEMPERATURE RANGE					
Specified Temperature Range		−25		+85	°C
Storage Temperature Range		−40		+125	°C
Thermal Resistance, θ_{J-A}			50		°C/W

NOTES: (1) Deviation from ideal transfer function referred to full scale output. Includes gain, nonlinearity and offset errors.

MECHANICAL

P Package — 16-Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1(1)	.015	0.50	0.38	1.27
B	.014	.020	0.36	0.51
B1	.035	.065	0.89	1.65
C	.008	.012	0.20	0.30
D	.745	.785	19.00	19.94
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81
L2	.000	.030	0.00	0.76
a	0°	15°	0°	15°
P	.015	.050	0.38	1.27
Q1	.040	.075	1.02	1.91
S	.015	.060	0.38	1.52

(1) Not JEDEC Std.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

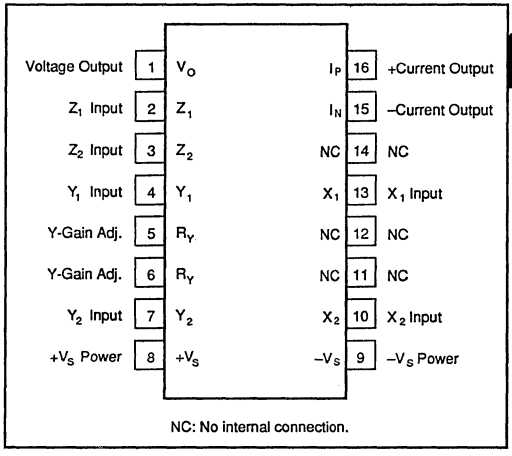
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	$\pm V_S$
Op Amp Output Current	100mA
Operating Temperature	+125°C
Storage Temperature	+150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

MODEL	PACKAGE	SPECIFIED TEMPERATURE RANGE
MPY600AP	Plastic DIP	–25°C to +85°C

PIN CONFIGURATION

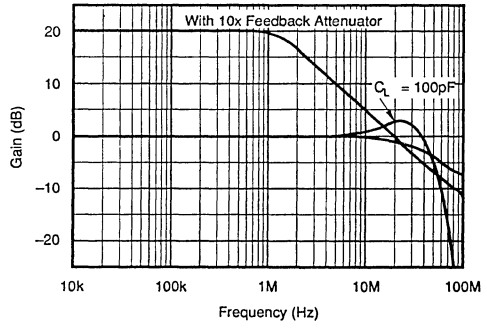


NC: No internal connection.

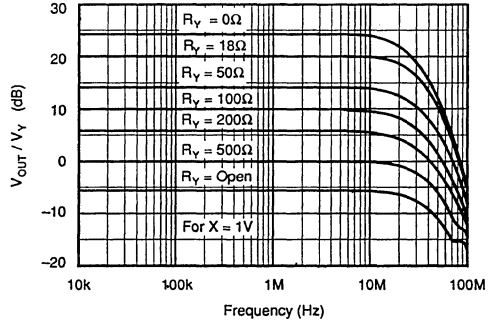
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±5V unless otherwise noted.

MULTIPLIER GAIN vs FREQUENCY



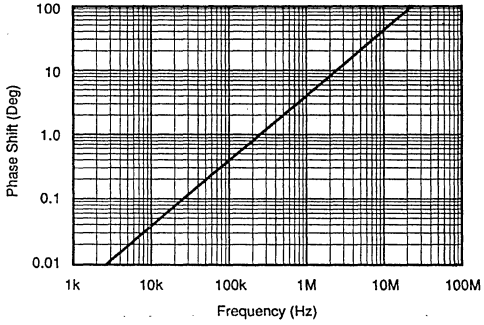
VOLTAGE OUTPUT FREQUENCY RESPONSE



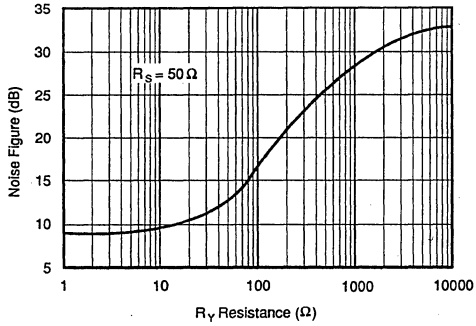
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±5V unless otherwise noted.

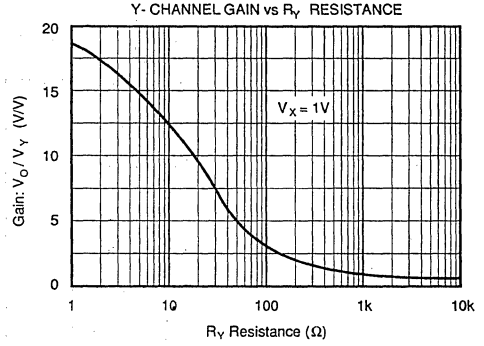
VOLTAGE OUTPUT PHASE SHIFT vs FREQUENCY



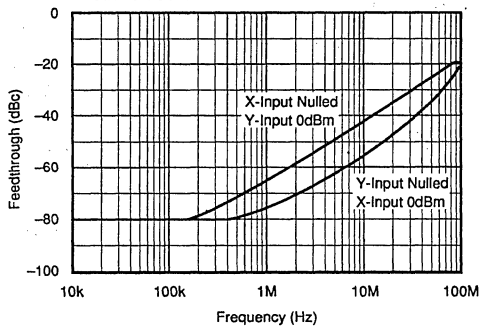
NOISE FIGURE vs R_Y RESTISTANCE



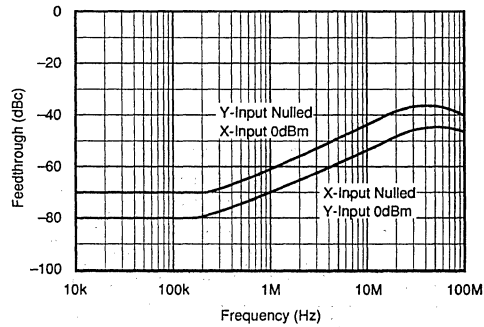
Y- CHANNEL GAIN vs R_Y RESISTANCE



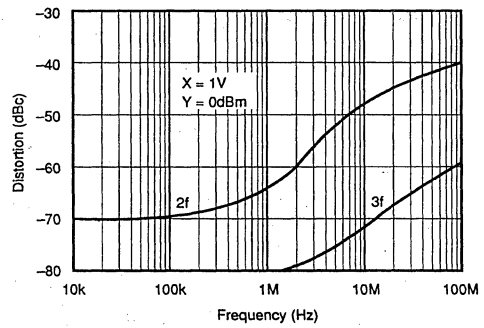
VOLTAGE OUTPUT FEEDTHROUGH vs FREQUENCY



CURRENT OUTPUT FEEDTHROUGH vs FREQUENCY



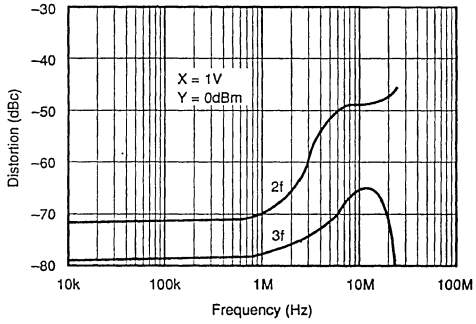
CURRENT OUTPUT HARMONIC DISTORTION vs FREQUENCY



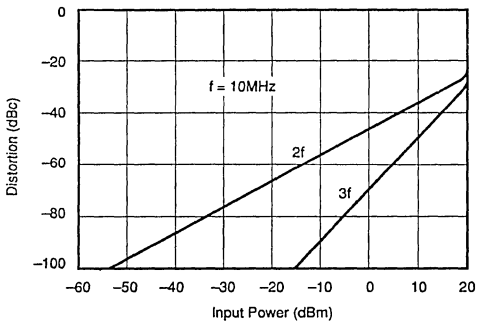
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±5V unless otherwise noted.

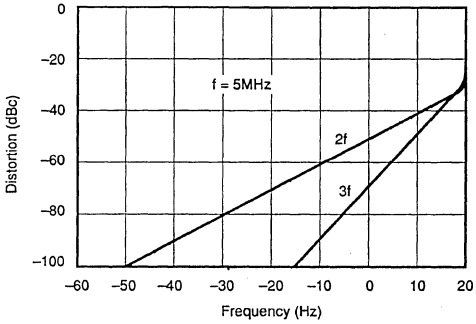
VOLTAGE OUTPUT HARMONIC DISTORTION vs FREQUENCY



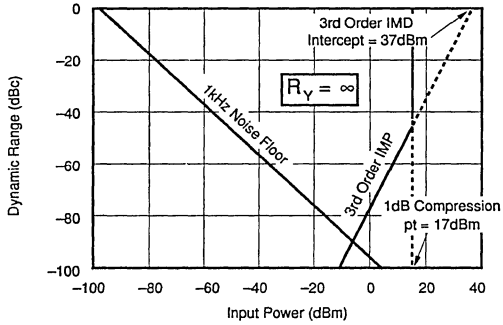
CURRENT OUTPUT HARMONIC DISTORTION vs INPUT POWER



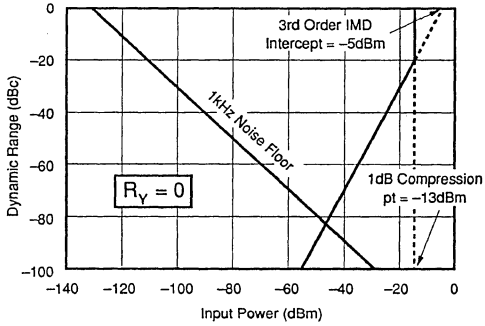
VOLTAGE OUTPUT HARMONIC DISTORTION vs INPUT POWER



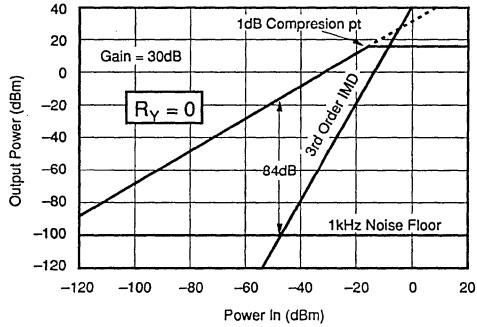
INPUT-REFERRED DYNAMIC RANGE vs INPUT POWER



INPUT-REFERRED DYNAMIC RANGE vs INPUT POWER



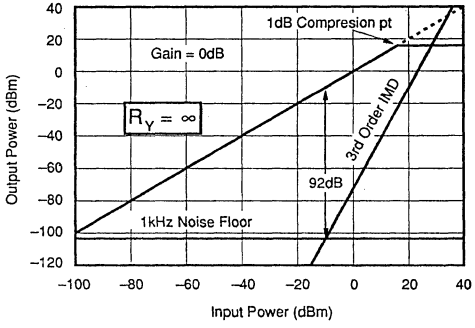
OUTPUT-REFERRED DYNAMIC RANGE vs INPUT POWER



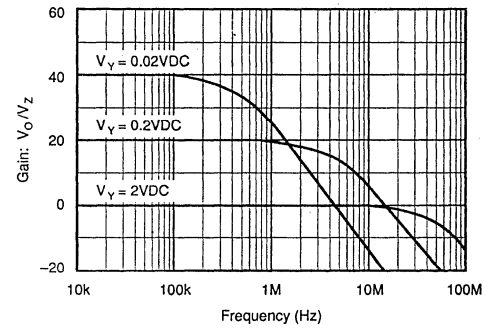
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±5V unless otherwise noted.

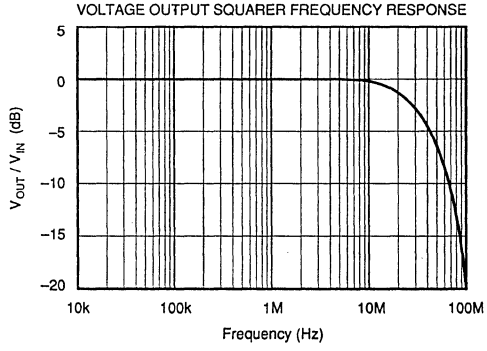
OUTPUT-REFERRED DYNAMIC RANGE vs INPUT POWER



DIVIDER RESPONSE vs FREQUENCY



VOLTAGE OUTPUT SQUARER FREQUENCY RESPONSE



POWER SUPPLIES

The MPY600 may be operated from power supplies from ±4.75V to ±8V. Operation from ±5V supplies is recommended. Since input and output levels are ±2V, larger supply voltage is not required for full output voltage swing. Furthermore, power dissipation can be minimized by using lower power supply voltage. Power supplies should be bypassed with good high-frequency capacitors such as ceramic or solid tantalum.

TRANSFER FUNCTION

The open-loop transfer function of the MPY600 is:

$$V_O = A\left[\frac{(X_1 - X_2) \bullet (Y_1 - Y_2)}{2V} - (Z_1 - Z_2)\right]$$

where A = open-loop gain of the output amplifier (typically 70dB).

X, Y, Z are differential input voltages— ±2V max.

An intuitive understanding of the transfer function can be gained by analogy to an op amp. Assuming that the open-loop gain is infinite, any output voltage can be created by an infinitesimally small quantity with the brackets. An applications circuit can be analyzed by assigning circuit voltages to the X, Y and Z inputs and setting the bracketed quantity equal to zero.

For example, in the basic multiplier connection (Figure 1), $Z_1 = V_O$ and $Z_2 = 0$. Setting this equal to zero:

$$\left[\frac{(X_1 - X_2) \bullet (Y_1 - Y_2)}{2V} - V_O\right] = 0$$

Solving for V_O yields the transfer function of the circuit.

The X input is specified for ±1V full-scale differential input. X inputs up to ±2V provide useful operation with somewhat reduced accuracy and distortion performance. The Y input is rated for ±2V full-scale input. The Y input gain (and therefore its full-scale range) can be varied with an external resistor connected to the R_Y terminals—see "Modulator/Demodulator." Full-scale inputs (X = ±1V, Y = ±2V) produce a ±1V output.

The differential inputs, X_1, X_2 and Y_1, Y_2, make it easy to trim offset voltage. The trim voltage is applied to the X_2 or Y_2 input, which is otherwise grounded (see X_2 input, Figure 5). Polarity of the input signals can be reversed by interchanging the inputs (reversing the connections X_1 and X_2, for instance). The unused current outputs (pins 15 and 16) must be grounded (or loaded—see discussion on current outputs).

The output amplifier is operated in unity gain. The output voltage can be increased (for small input signals) by placing the internal output op amp in higher gain (Figure 2). This reduces bandwidth and increases output offset voltage errors.

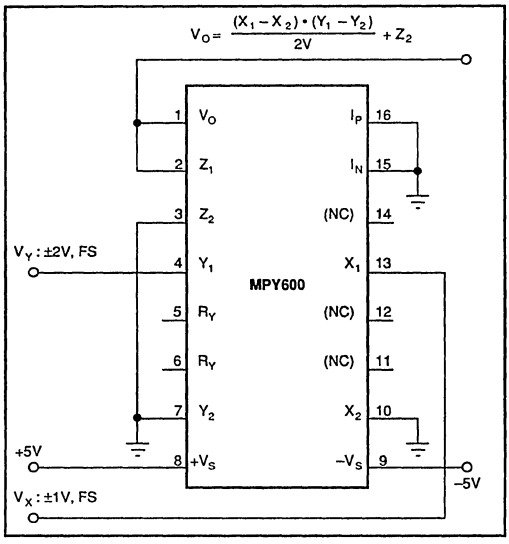


FIGURE 1. Basic Multiplier Connection.

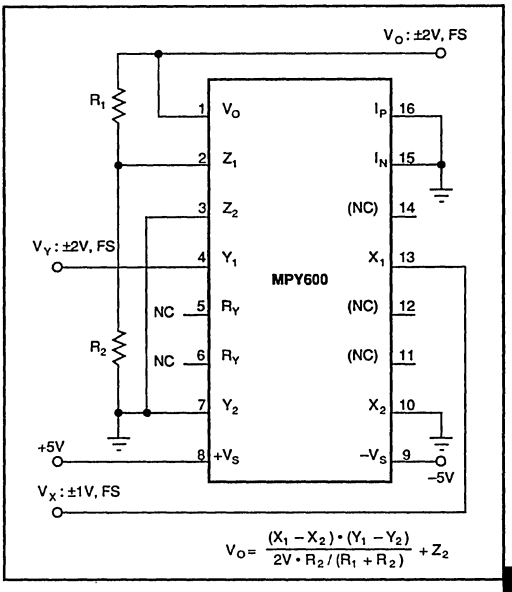


FIGURE 2. Adjusting the Scale Factor with Feedback.

CURRENT OUTPUT

The current output connections of the MPY600 can achieve wider bandwidth multiplier operation (Figure 3). The current output is determined by the X and Y inputs only, so applications which use the Z input to modify the transfer function (e.g., divider and square-root modes) cannot be used. A full-scale input of ±1V on the X and ±2V on the Y inputs produces a 2mA differential current at the current outputs. This consists of approximately 2.5mA quiescent current ±1mA signal current on each output. The current outputs may be used to drive any load impedance which maintains the voltage on the current outputs within their compliance range. This compliance limit is approximately 2.5V from the power supply voltages. The current outputs and voltage output may be used simultaneously, if desired.

Output capacitance and stray capacitance at the current output terminals will limit the multiplier bandwidth. This makes large output resistors (greater than approximately 1kΩ) impractical. The current outputs can be used to drive 50Ω or 75Ω loads directly.

The circuit shown in Figure 4 uses the current outputs to drive an external OPA621 op amp configured as a current-difference amplifier. It operates in a noise gain of 3.5. The OPA621 is stable in a noise gain of two or greater and has a 500MHz gain-bandwidth product. It achieves the full bandwidth performance of the MPY600. R_1 determines the transfer function gain. R_3 provides a proper load to optimize high-frequency effects. R_4 is made equal to the parallel combination of R_1 and R_3.

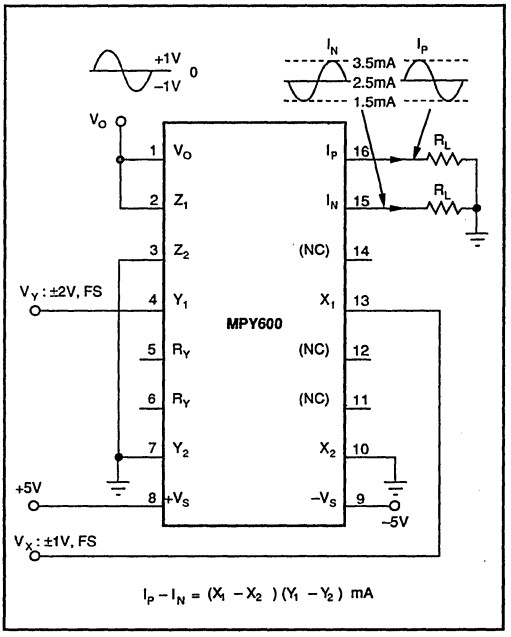


FIGURE 3. Current Output Connection.

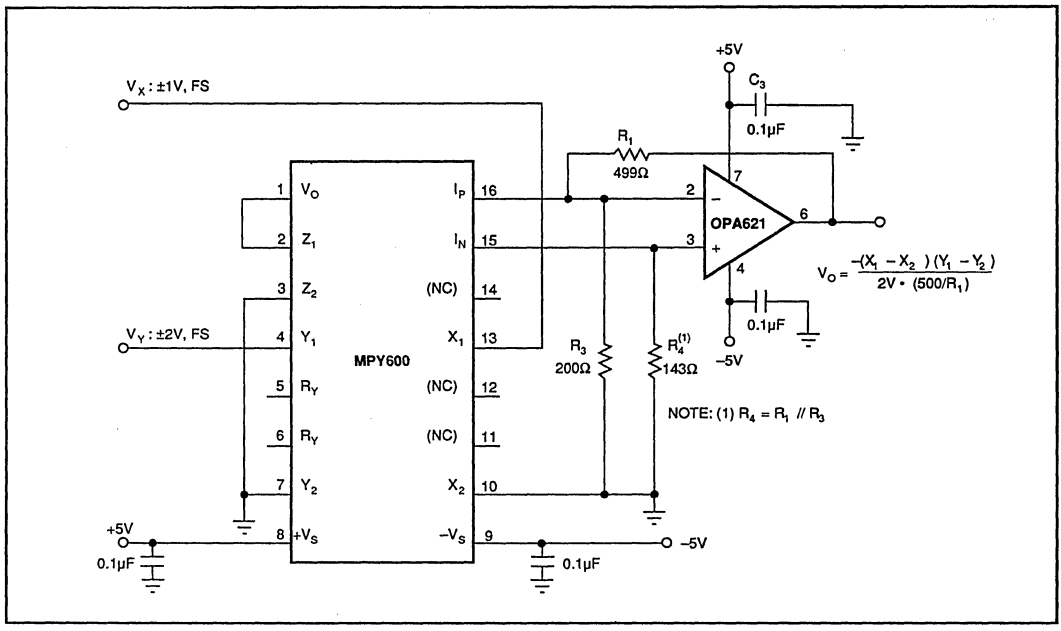


FIGURE 4. 75MHz DC-Coupled Multiplier.

MODULATOR/DEMODULATOR

The balanced modulator or demodulator shown in Figure 5 uses the basic multiplier configuration. It shows the offset of the X input trimmed to null carrier feedthrough. It also illustrates the use of R_Y to change the gain of the Y input. This can be used to optimize the spurious-free dynamic range for a given input level. The Y input is optimized for ±2V inputs. For lower input signals, the Y input can be programmed for higher gain by connecting an external resistor to the R_Y terminals. The conceptual diagram in Figure 6 reveals why varying the Y-channel gain can yield improved dynamic range. The R_Y selection curve in Figure 5 shows the optimum value of R_Y for a given Y-input signal level.

DIVIDER OPERATION

The MPY600 can be configured as a divider as shown in Figure 7. Numerator voltage is applied to the Z inputs; denominator voltage is applied to the X inputs. Since the feedback connection is made to a multiplying input, the effective gain of the output amplifier varies as a function of the denominator input. This causes the bandwidth to vary with denominator (see Typical Performance Curves for divider bandwidth performance). Accuracy in divider operation is approximately 3% for a 10:1 denominator range. Errors grow large and will eventually saturate the output as the denominator voltage approaches 0V.

SQUARE-ROOT CIRCUIT

The circuit in Figure 8 provides an output voltage proportional to the square-root of the input (for positive input voltages). Diode D_1 prevents latch-up if the input should go negative. The circuit can be configured for negative input and positive output by reversing the polarity of both the X and Y differential inputs. The output polarity can be inverted by reversing the X input polarity and the diode. Accuracy can be improved by trimming the offset at the Z input.

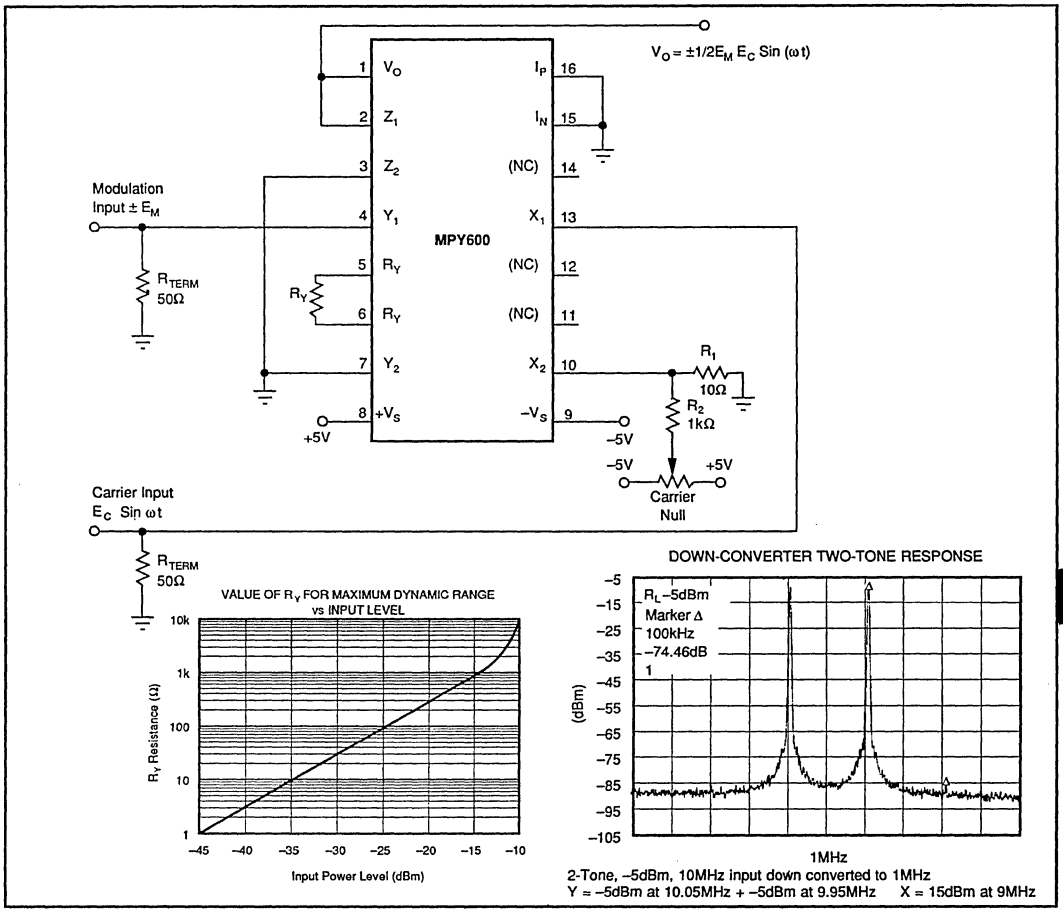


FIGURE 5. Balanced Modulator.

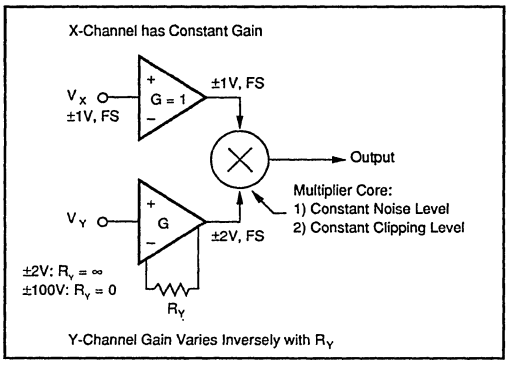


FIGURE 6. Variable Y-Channel Gain—Conceptual Model.

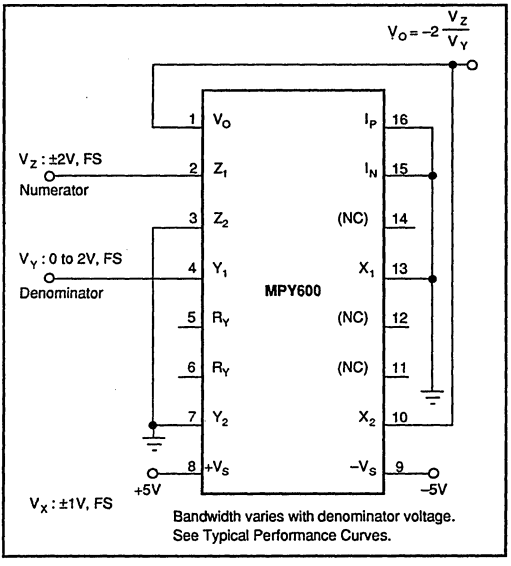


FIGURE 7. Divider Circuit.

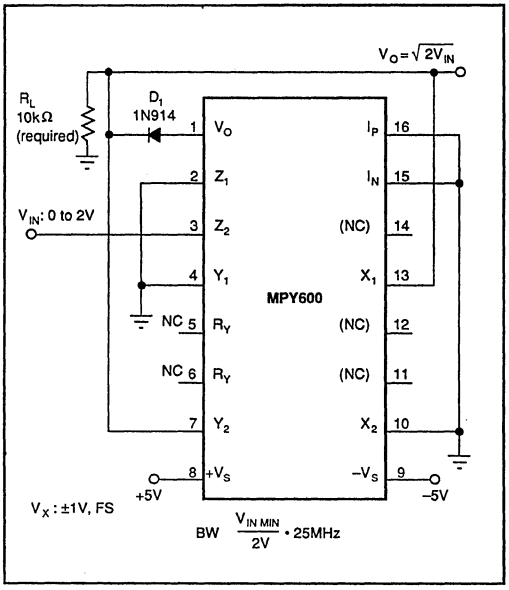


FIGURE 8. Square-Root Circuit.

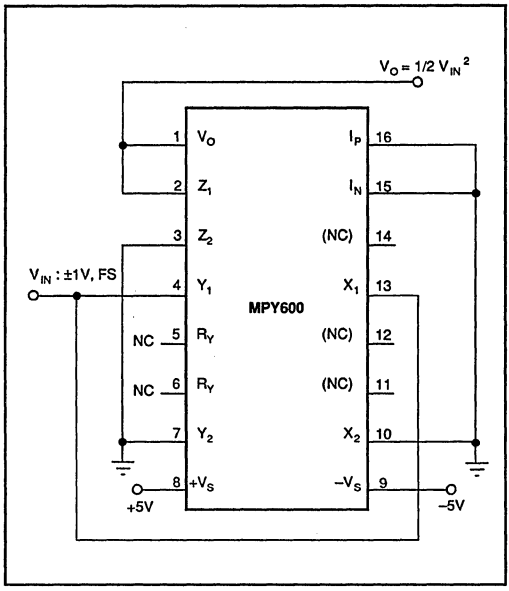


FIGURE 9. Squaring Circuit.

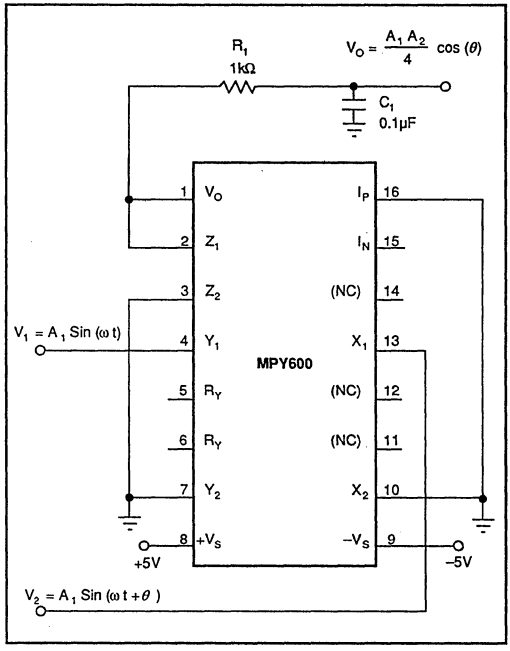


FIGURE 10. Phase Detector.

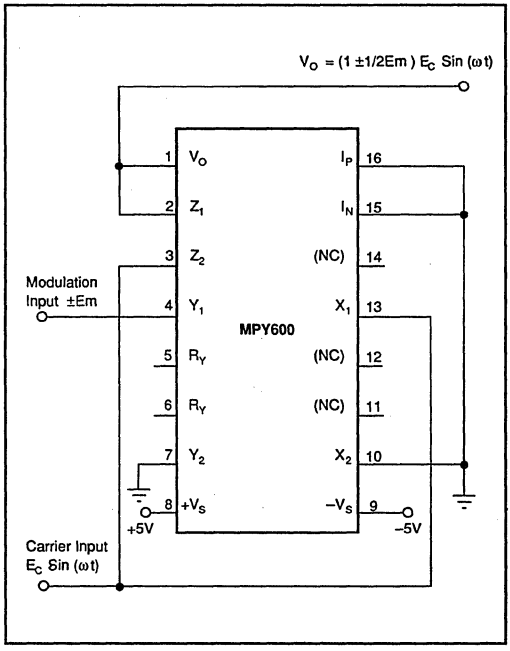


FIGURE 11. Linear AM Modulator.

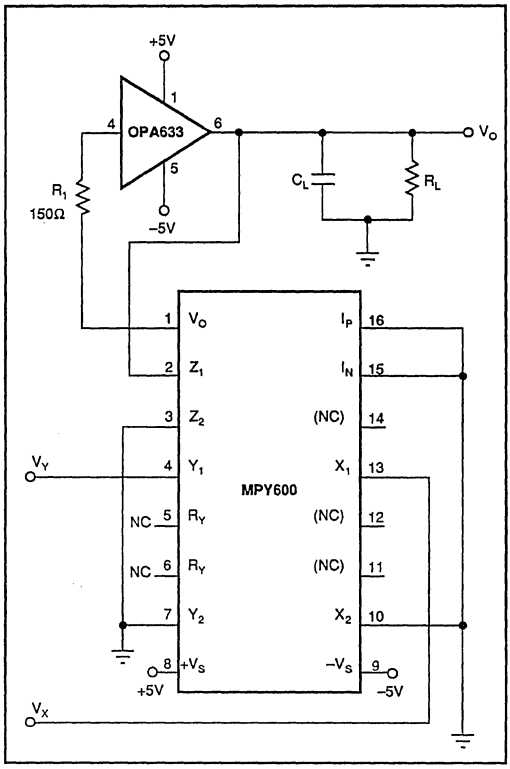


FIGURE 12. 25MHz Multiplier with Improved Load Driving Capability.

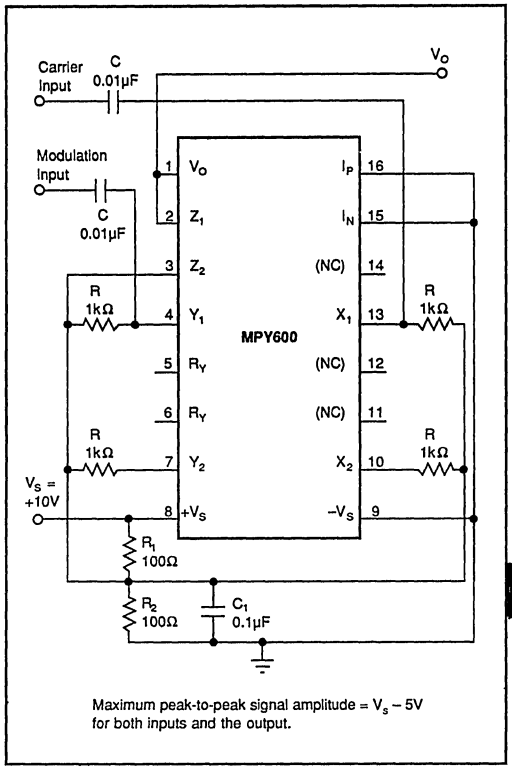


FIGURE 13. Single-Supply Balanced Modulator.

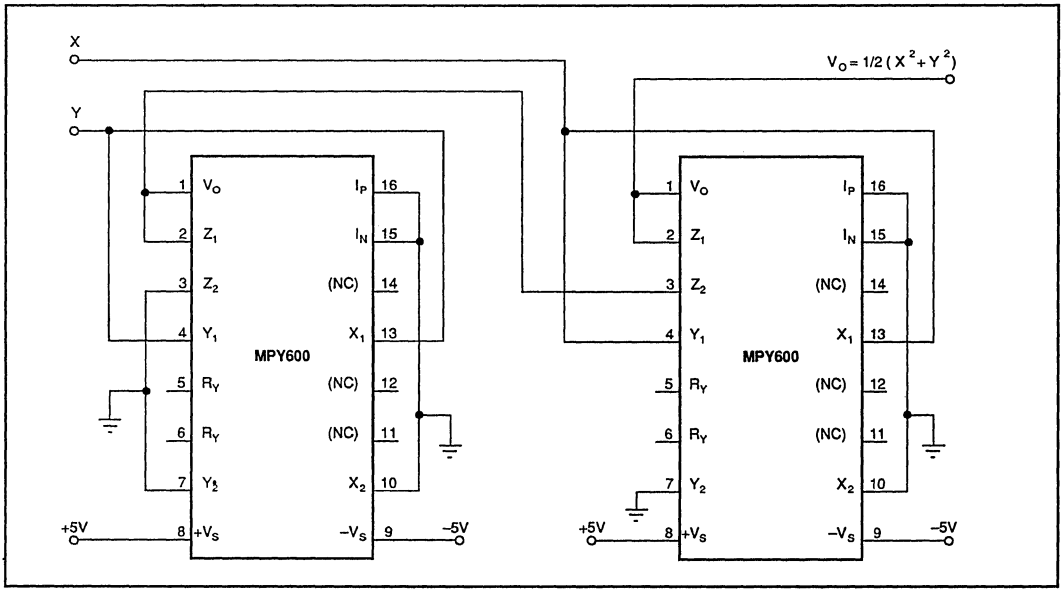


FIGURE 14. CRT Focus Correction.

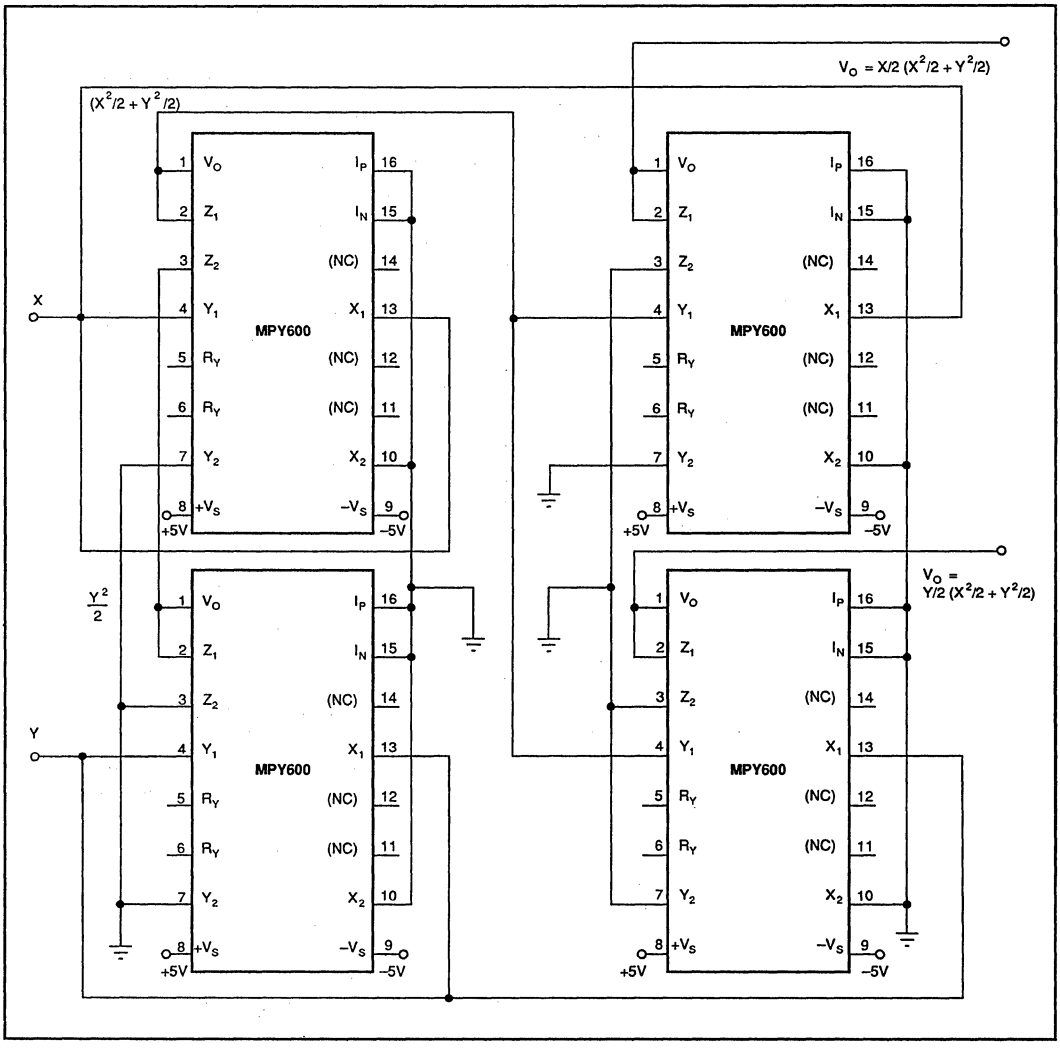


FIGURE 15. CRT Geometry Correction.

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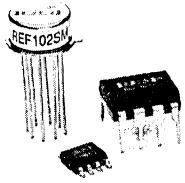


REF102

Precision VOLTAGE REFERENCE

FEATURES

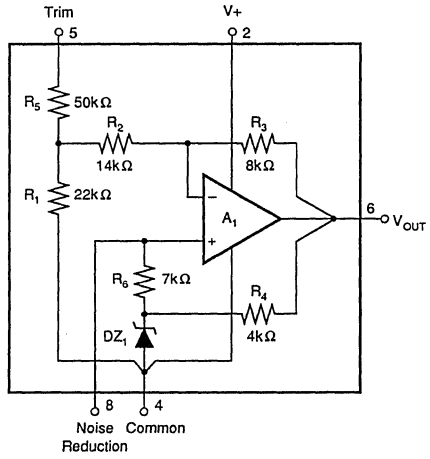
- +10V ±0.0025V OUTPUT
- VERY LOW DRIFT: 2.5ppm/°C max
- EXCELLENT STABILITY: 5ppm/1000hr typ
- EXCELLENT LINE REGULATION: 1ppm/V max
- EXCELLENT LOAD REGULATION: 10ppm/mA max
- LOW NOISE: 5μVp-p typ, 0.1Hz to 10Hz
- WIDE SUPPLY RANGE: 11.4VDC to 36VDC
- LOW QUIESCENT CURRENT: 1.4mA max
- PACKAGE OPTIONS: HERMETIC TO-99, PLASTIC DIP, SOIC, DIE

APPLICATIONS

- PRECISION-CALIBRATED VOLTAGE STANDARD
- D/A AND A/D CONVERTER REFERENCE
- PRECISION CURRENT REFERENCE
- ACCURATE COMPARATOR THRESHOLD REFERENCE
- DIGITAL VOLTMETERS
- TEST EQUIPMENT
- PC-BASED INSTRUMENTATION

DESCRIPTION

The REF102 is a precision 10V voltage reference. The drift is laser-trimmed to 2.5ppm/°C max (CM grade) over the industrial temperature range and 5ppm/°C max (SM grade) over the military temperature range. The REF102 achieves its precision without a heater. This results in low-power, fast warm-up, excellent stability, and low noise. The output voltage is extremely insensitive to both line and load variations and can be externally adjusted with minimal effect on drift and stability. Single supply operation from 11.4V to 36V and excellent overall specifications make the REF102 an ideal choice for demanding instrumentation and system reference applications. The REF102 is also available in die form.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_S = +15V power supply unless otherwise noted.

PARAMETER	CONDITIONS	REF102A/R			REF102B/S			REF102CM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT VOLTAGE											
Initial	T_A = 25°C	9.99		10.01	9.995		10.005	9.9975		10.0025	V
vs Temperature [1]				10			5			2.5	ppm/°C
vs Supply											
(Line Regulation)	V_S = 11.4V to 36V			2			1			1	ppm/V
vs Output Current											
(Load Regulation)	I_L = 0mA to +10mA			20			10			10	ppm/mA
	I_L = 0mA to –5mA			40			20			20	ppm/mA
vs Time	T_A = 25°										
M Package			5			•			•		ppm/1000hr
P, U Packages [2]			20			•					ppm/1000hr
Trim Range [3]		±3			•			•			%
NOISE	(0.1Hz to 10Hz)		5			•			•		µVp-p
OUTPUT CURRENT		+10, –5			•			•			mA
INPUT VOLTAGE RANGE		+11.4		+36	•		•	•		•	V
QUIESCENT CURRENT	(I_{OUT} = 0)			+1.4			•			•	mA
WARM-UP TIME [4]	(To 0.1%)		15			•			•		µs
TEMPERATURE RANGE											
Specification											
REF102A, B, C		–25		+85	•		•	•		•	°C
REF102R, S		–55		+125	•		•				°C

*Specifications same as REF102A/R.

NOTES: (1) The "box" method is used to specify output voltage drift vs temperature. See the Discussion of Performance section. (2) Typically 5ppm/1000hrs after 168hr powered stabilization. (3) Trimming the offset voltage affects drift slightly. See Installation and Operating Instructions for details. (4) With noise reduction pin floating. See Typical Performance Curves for details.

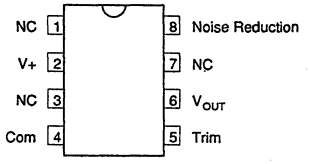
ORDERING INFORMATION

MODEL[1]	PACKAGE	TEMP RANGE	MAX INITIAL ERROR (mV)	MAX DRIFT (ppm/°C)
REF102AU	SOIC	–25 to +85°C	±10	±10
REF102AP	Plastic DIP	–25 to +85°C	±10	±10
REF102BP	Plastic DIP	–25 to +85°C	±5	±5
REF102AM	Metal TO-99	–25 to +85°C	±10	±10
REF102BM	Metal TO-99	–25 to +85°C	±5	±5
REF102CM	Metal TO-99	–25 to +85°C	±2.5	±2.5
REF102RM	Metal TO-99	–55 to +125°C	±10	±10
REF102SM	Metal TO-99	–55 to +125°C	±5	±5

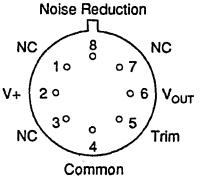
PIN CONFIGURATIONS

Top View

P, U Package



M Package

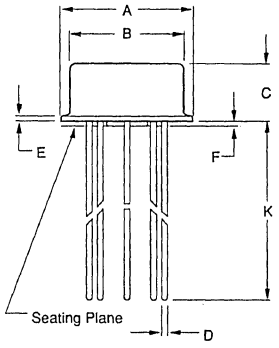


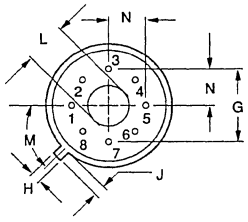
ABSOLUTE MAXIMUM RATINGS

Input Voltage	+40V
Operating Temperature	
P,U	–25°C to +85°C
M	–55°C to +125°C
Storage Temperature Range	
P,U	–40°C to +85°C
M	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
(SOIC 3s)	+260°C
Short-Circuit Protection to Common or V+	Continuous

MECHANICAL

M Package — Metal TO-99

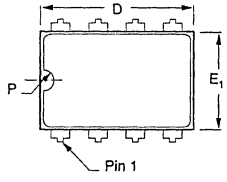


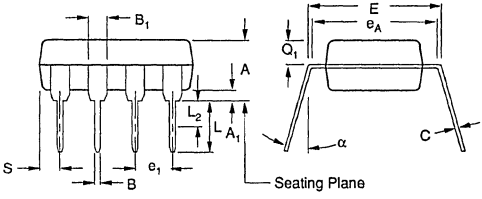


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

P Package — 8-Pin Plastic DIP





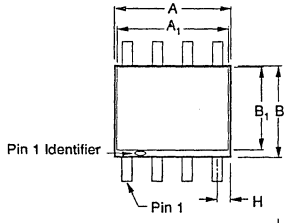
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.155	.200	3.94	5.08
A_1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B_1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D(1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E_1	.240	.260	6.10	6.60
e_1	.100 BASIC		2.54 BASIC	
e_A	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

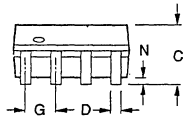
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
L_2(2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q_1	.040	.075	1.02	1.91
S(1)	.015	.050	0.38	1.27

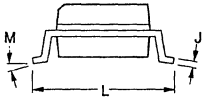
(1) Not JEDEC Std.
(2) e1 and e_A applies in zone L_2 when unit installed.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

U Package — 8-Pin SOIC







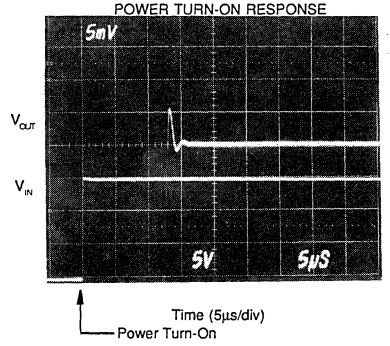
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.201	4.70	5.11
A_1	.178	.201	4.52	5.11
B	.146	.162	3.71	4.11
B_1	.130	.149	3.30	3.78
C	.054	.145	1.37	3.69
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.018	.026	0.46	0.66
J	.008	.012	0.20	0.30
L	.220	.252	5.59	6.40
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

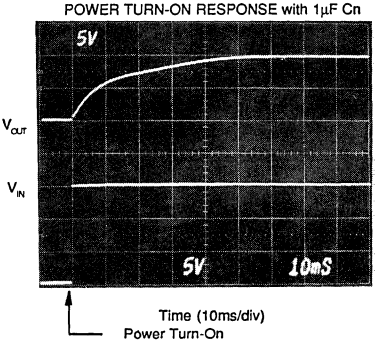
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = +15V unless otherwise noted.

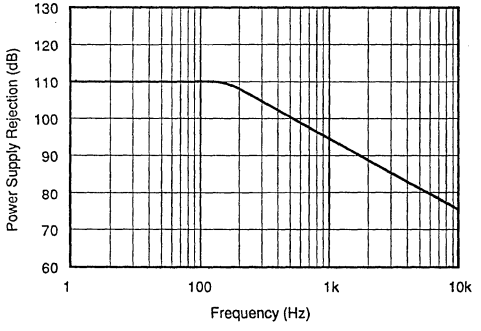
POWER TURN-ON RESPONSE



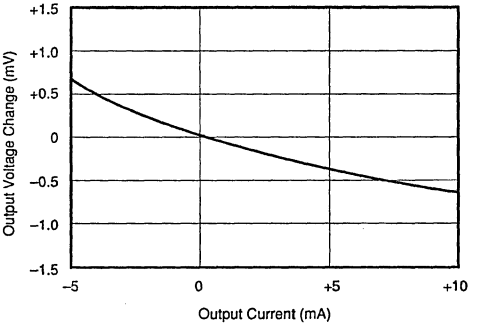
POWER TURN-ON RESPONSE with 1µF Cn



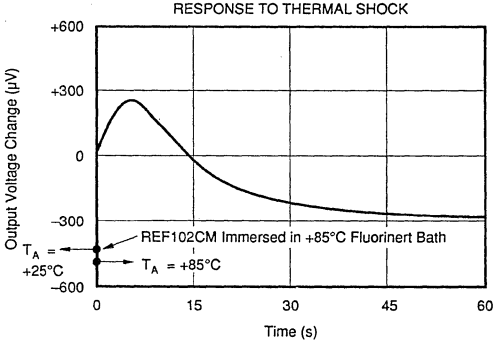
POWER SUPPLY REJECTION vs FREQUENCY



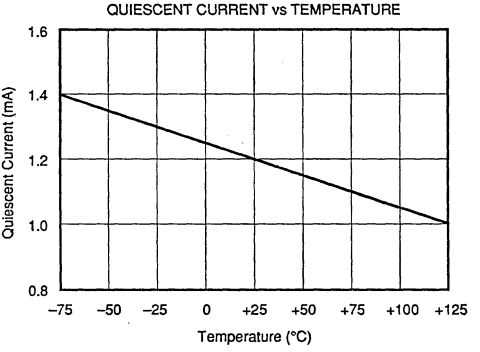
LOAD REGULATION



RESPONSE TO THERMAL SHOCK



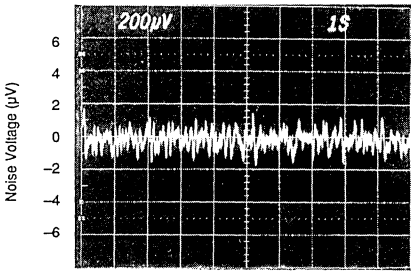
QUIESCENT CURRENT vs TEMPERATURE



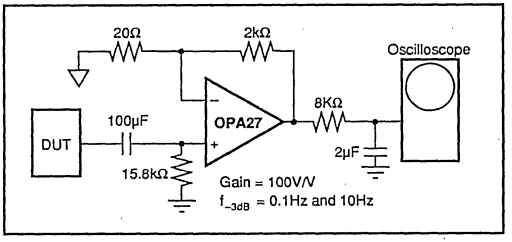
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = +15V unless otherwise noted.

TYPICAL REF102 REFERENCE NOISE



Low Frequency Noise (1s /div)
(See Noise Test Circuit)



Noise Test Circuit.

THEORY OF OPERATION

Refer to the diagram on the first page of this data sheet. The 10V output is derived from a compensated buried zener diode DZ_1, op amp A_1, and resistor network R_1–R_6.

Approximately 8.2V is applied to the non-inverting input of A_1 by DZ_1. R_1, R_2, and R_3 are laser-trimmed to produce an exact 10V output. The zener bias current is established from the regulated output voltage through R_4. R_5 allows user-trimming of the output voltage by providing for small external adjustment of the amplifier gain. Because the TCR of R_5 closely matches the TCR of R_1, R_2 and R_3, the voltage trim has minimal effect on the reference drift. The output voltage noise of the REF102 is dominated by the noise of the zener diode. A capacitor can be connected between the Noise Reduction pin and ground to form a low-pass filter with R_6 and roll off the high-frequency noise of the zener.

DISCUSSION OF PERFORMANCE

The REF102 is designed for applications requiring a precision voltage reference where both the initial value at room temperature and the drift over temperature are of importance to the user. Two basic methods of specifying voltage reference drift versus temperature are in common usage in the industry—the "butterfly method" and the "box method." The REF102 is specified with the more commonly used "box method." The "box" is formed by the high and low specification temperatures and a diagonal, the slope of which is equal to the maximum specified drift.

Since the shape of the actual drift curve is not known, the vertical position of the box is not exactly known either. It is, however, bounded by $V_{UPPER\ BOUND}$ and $V_{LOWER\ BOUND}$ (see Figure 1). Figure 1 uses the REF102CM as an example. It has a drift specification of 2.5ppm/°C maximum and a specification temperature range of –25°C to +85°C. The "box" height, V_1 to V_2, is 2.75mV.

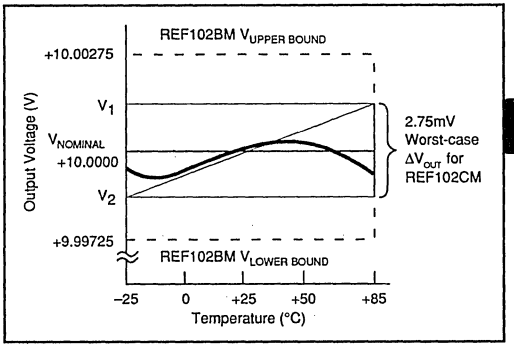


FIGURE 1. REF102CM Output Voltage Drift.

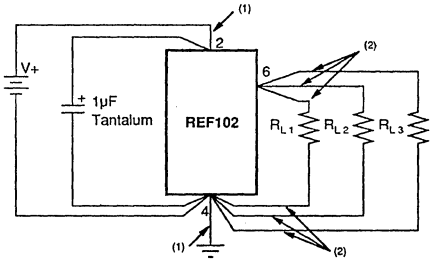
INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CIRCUIT CONNECTION

Figure 2 shows the proper connection of the REF102. To achieve the specified performance, pay careful attention to layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power-supply. Commons should be connected as indicated being sure to minimize interconnection resistances.

OPTIONAL OUTPUT VOLTAGE ADJUSTMENT

Optional output voltage adjustment circuits are shown in Figures 3 and 4. Trimming the output voltage will change the voltage drift by approximately 0.008ppm/°C per mV of trimmed voltage. In the circuit in Figure 3, any mismatch in TCR between the two sections of the potentiometer will also affect drift, but the effect of the ΔTCR is reduced by a factor of five by the internal resistor divider. A high quality potentiometer, with good mechanical stability, such as a cermet, should be used. The circuit in Figure 3 has a minimum trim range of ±300mV. The circuit in Figure 4 has less range but provides higher resolution. The mismatch in TCR between



NOTES: (1) Lead resistances here of up to a few ohms have negligible effect on performance. (2) A resistance of 0.1Ω in series with these leads will cause a 1mV error when the load current is at its maximum of 10mA. This results in a 0.01% error of 10V.

FIGURE 2. REF102 Installation.

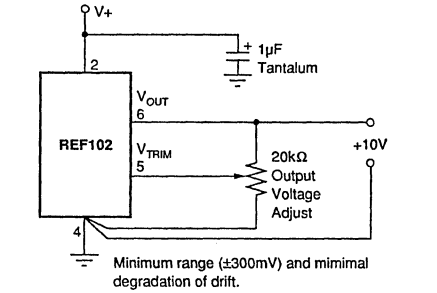


FIGURE 3. REF102 Optional Output Voltage Adjust.

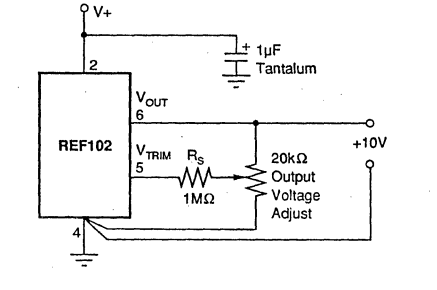


FIGURE 4. REF102 Optional Output Voltage Fine Adjust.

R_S and the internal resistors can introduce some slight drift. This effect is minimized if R_S is kept significantly larger than the 50kΩ internal resistor. A TCR of 100ppm/°C is normally sufficient.

OPTIONAL NOISE REDUCTION

The high-frequency noise of the REF102 is dominated by the zener diode noise. This noise can be greatly reduced by connecting a capacitor between the Noise Reduction pin and ground. The capacitor forms a low pass filter with R_6 (refer to the figure on the first page of the data sheet) and attenuates the high-frequency noise generated by the zener. Figure 5 shows the effect of a 1µF noise reduction capacitor on the high frequency noise of the REF102. R_6 is typically 7kΩ so the filter has a –3dB frequency of about 22Hz. The result is a reduction in noise from about 800µVp-p to under 200µ Vp-p. If further noise reduction is required, use the circuit in Figure 14.

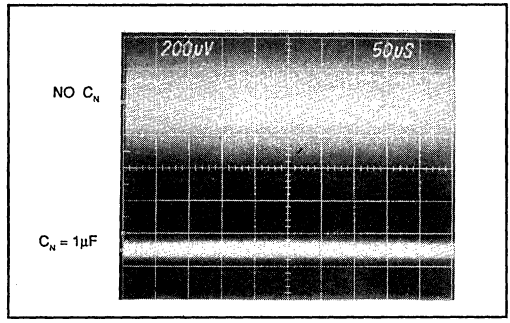


FIGURE 5. Effect of 1µF Noise Reduction Capacitor on Broadband Noise (f_{-3dB} = 1MHz).

APPLICATIONS INFORMATION

High accuracy, extremely low drift, outstanding stability, and low cost make the REF102 an ideal choice for all instrumentation and system reference applications. Figures 6 through 14 show a variety of useful application circuits.

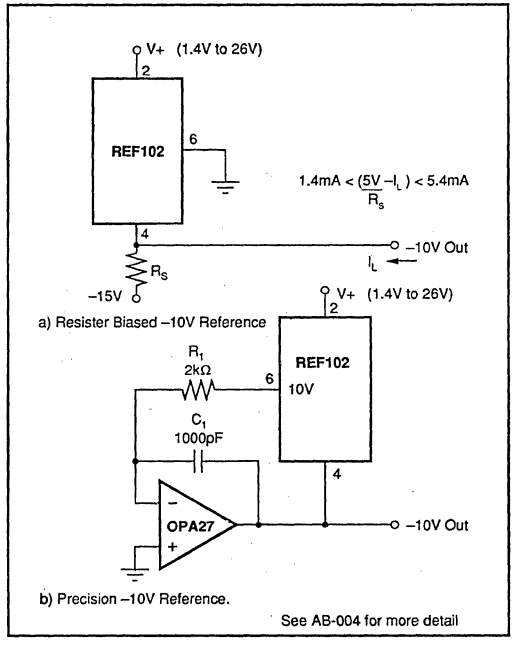


FIGURE 6. –10V Reference Using a) Resistor or b) OPA27.

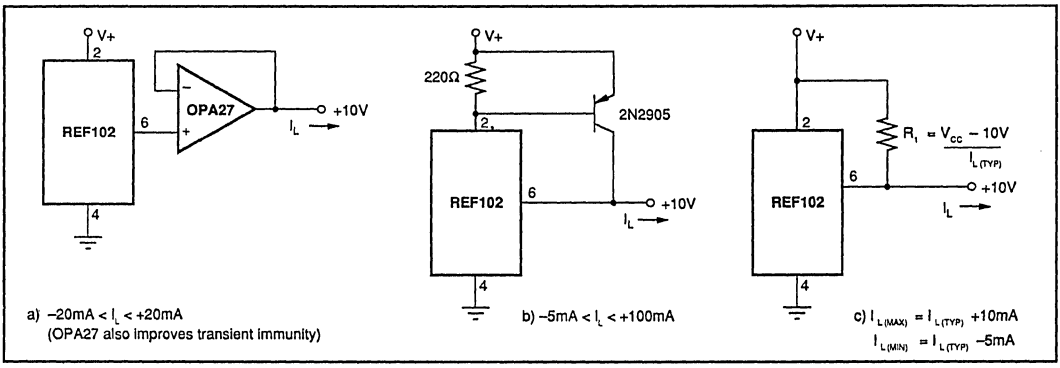


FIGURE 7. +10V Reference With Output Current Boosted to: a) ±20mA, b) +100mA, and c) $I_{L\,(TYP)}$ +10mA, −5A.

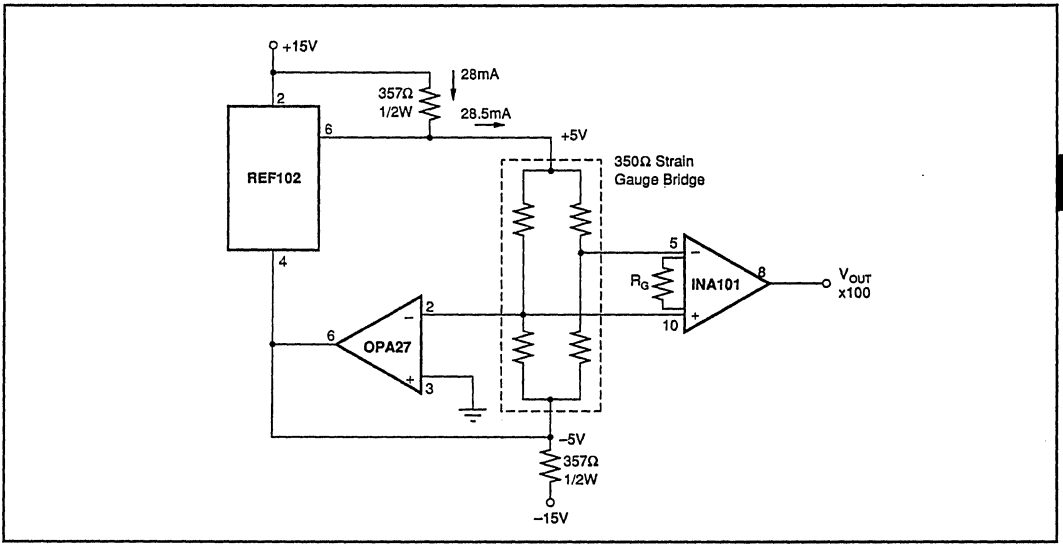


FIGURE 8. Strain Gauge Conditioner for 350Ω Bridge.

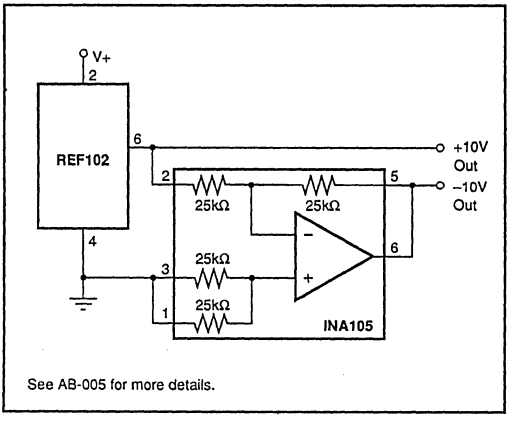


FIGURE 9. ±10V Reference.

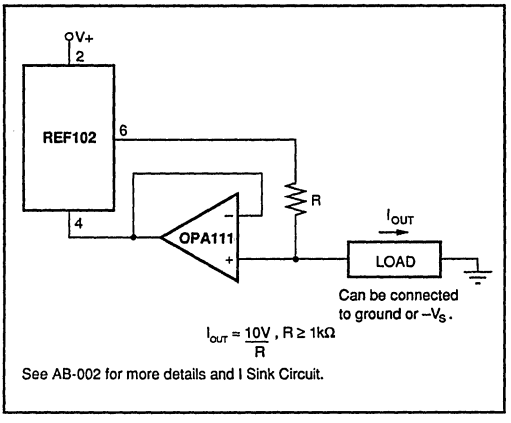
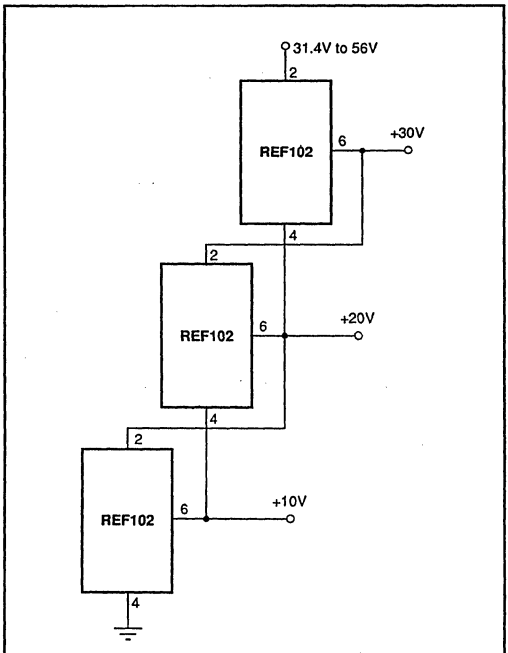


FIGURE 10. Positive Precision Current Source.



NOTES: (1) REF102s can be stacked to obtain voltages in multiples of 10V. (2) The supply voltage should be between 10n + 1.4 and 10n + 26 where n is the number of REF102s. (3) Output current of each REF102 must not exceed its rated output current of +10, –5mA. This includes the current delivered to the lower REF102.

FIGURE 11. Stacked References.

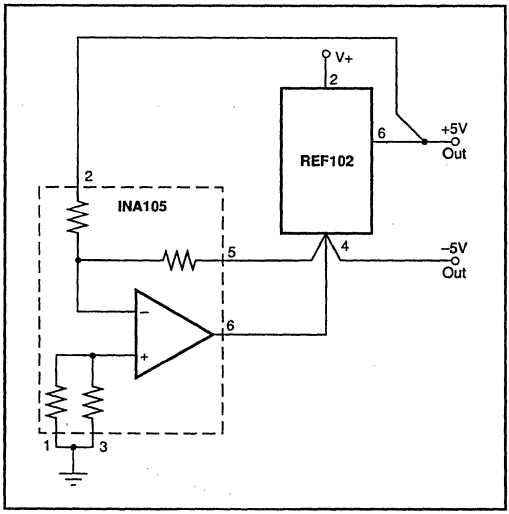


FIGURE 12. ±5V Reference.

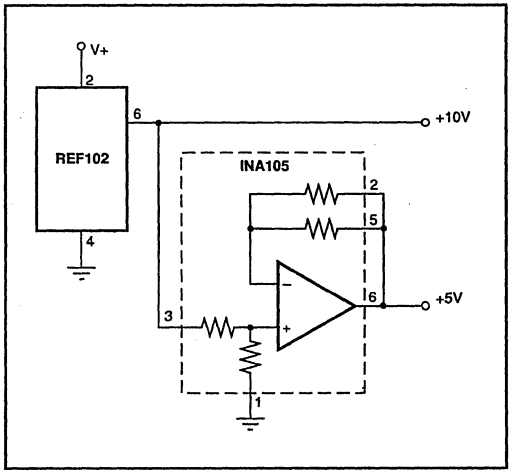


FIGURE 13. +5V and +10V Reference.

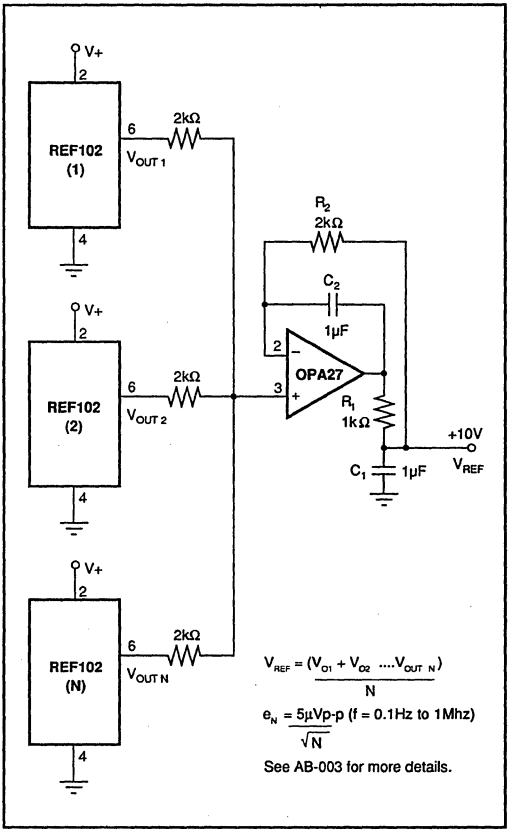
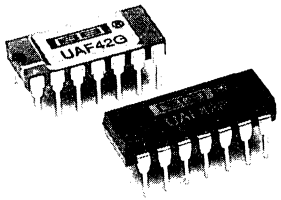


FIGURE 14. Precision Voltage Reference with Extremely Low Noise.

BURR-BROWN®



UAF42

ADVANCE INFORMATION
SUBJECT TO CHANGE

UNIVERSAL ACTIVE FILTER

FEATURES

- VERSATILE FUNCTION
  LOW-PASS, HIGH-PASS
  BAND-PASS, BAND-REJECT
- SIMPLE DESIGN PROCEDURE
- ACCURATE FREQUENCY AND Q
  INCLUDES ON-CHIP 1000pF ±0.5%
  CAPACITORS

APPLICATIONS

- TEST EQUIPMENT
- COMMUNICATIONS EQUIPMENT
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION SYSTEMS
- MONOLITHIC REPLACEMENT FOR UAF41

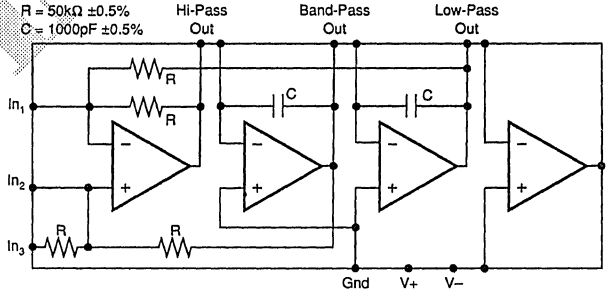
DESCRIPTION

The UAF42 is a universal active filter which can be configured for a wide range of low-pass, high-pass, and band-pass filters. It uses a classical state-variable analog architecture with an inverting amplifier and two integrators. The integrators include on-chip 1000pF capacitors trimmed to 0.5%. This solves one of the most difficult problems of active filter design—obtaining tight tolerance, low-loss capacitors.

Simple design procedures allow easy implementation of many filter types such as Butterworth, Bessel, Chebyshev and Gaussian. A fourth, uncommitted FET-input op amp (identical to the other three) can be used to form additional stages, or for special filter types such as band-reject and elliptic.

The classical topology of the UAF42 forms a continuous filter, free from the anomalies and switching noise associated with switched-capacitor filter types.

The UAF42 is available in a 14-pin plastic DIP and side-brazed ceramic packages, specified for the –25°C to +85°C temperature range.



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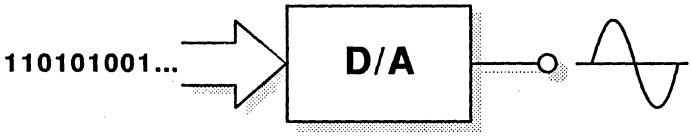
PDS-1070

SPECIFICATIONS

T_A = +25°C, V_S = ±15V unless otherwise noted.

PARAMETER	CONDITION	UAF42AP, AG MIN	UAF42AP, AG TYP	UAF42AP, AG MAX	UNITS
FILTER PERFORMANCE					
Frequency Range			0 to 100		kHz
Frequency Accuracy				1	%
vs Temperature			0.01		%/C
Maximum Q			500		—
Maximum (Q • Frequency) Product			500		kHz
Q vs Temperature	$(f_0 \cdot Q) < 10^4$		0.01		%/°C
	$(f_0 \cdot Q) < 10^5$		0.025		%/°C
Q Repeatability	$(f_0 \cdot Q) < 10^5$		10		%
Offset Voltage, Low-Pass Output				±5	mV
Resistor Accuracy			0.5		%
OFFSET VOLTAGE[1]					
Input Offset Voltage			±0.5	±5	mV
vs Temperature			±3		µV/°C
vs Power Supply	V_S = ±6 to ±18V	80	96		dB
INPUT BIAS CURRENT[1]					
Input Bias Current	V_{CM} = 0V		10	50	pA
Input Offset Current	V_{CM} = 0V		5		pA
NOISE[1]					
Input Voltage Noise					
Noise Density: f = 10Hz			50		nV/√Hz
f = 10kHz			18		nV/√Hz
Voltage Noise: BW = 0.1 to 10Hz			2		µVp-p
Input Bias Current Noise					
Noise Density: f = 10kHz			2		fA/√Hz
INPUT VOLTAGE RANGE[1]					
Common-Mode Input Range			±11.5		V
Common-Mode Rejection	V_{CM} = ±10V	80	96		dB
INPUT IMPEDANCE[1]					
Differential			10^{13} || 2		Ω || pF
Common-Mode			10^{13} || 6		Ω || pF
OPEN-LOOP GAIN[1]					
Open-loop Voltage Gain	V_O = ±10V, R_L = 2kΩ	90	120		dB
FREQUENCY RESPONSE[1]					
Slew Rate			10		V/µs
Gain-Bandwidth Product	G = +1		4		MHz
Total Harmonic Distortion	G = +1, f = 1kHz		0.0004		%
OUTPUT[1]					
Voltage Output	R_L = 2kΩ	±11	±11.5		V
Short Circuit Current			±25		mA
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±6		±18	V
Current			±6	±7	mA
TEMPERATURE RANGE					
Specification					
AP, AG		–25		+85	°C
Operating, AG		–55		+125	°C
Storage					
AP		–40		+125	°C
AG		–60		+150	°C
Thermal Resistance, θ_{J-A}			100		°C/W

NOTES: (1) Specifications apply to uncommitted op amp, A4. The three op amps forming the filter are identical to A4 and are tested as a complete filter.



DIGITAL-TO-ANALOG CONVERTERS

Burr-Brown offers a broad variety of Digital-to-Analog (D/A) converter products engineered to meet the most critical requirements for stability and reliability.

General purpose instrumentation D/As range in resolution from 12 to 18 bits. These models include industry standard products—many originated by Burr-Brown—as well as more complete, higher accuracy solutions. Burr-Brown's products are carefully designed and manufactured to minimize product variations, making them ideal for test equipment, process control, and other industrial and analytical applications.

PCM D/A converters are designed and tested to deliver excellent dynamic performance. The resolutions of these products are 16 and 18 bits. Typical applications are compact disc players, digital frequency synthesis, and telecommunications systems.

High-speed D/A converters offer very fast settling current output. Models are available with TTL or ECL logic inputs. These products are ideal for very high frequency synthesis and control systems.

DIGITAL-TO-ANALOG CONVERTERS SELECTION GUIDES

The Selection Guides show parameters for the high grade. Refer to the Product Data Sheet for a full selection of grades. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book*.

INSTRUMENTATION DIGITAL-TO-ANALOG CONVERTERS — **Boldface = NEW**

Description	Model	Resolution (Bits)	Linearity Error (%FSR)	Settling Time (µs)	Output Range	Temp Range[1]	Pkg[2]	Q, BI[3] Screen	Page No.
Very High Resolution	DAC729	18	±0.00075	5	±1mA, –2mA; +5V, +10V, ±5V, ±10V	Com	DDIP	BI	6.1-80
General Purpose	DAC700	16	±0.0015	1	–2mA	Com, Ind, Mil	DDIP	Q, BI	6.1-43
	DAC701	16	±0.0015	8	+10V	Com, Ind, Mil	DDIP	Q, BI	6.1-43
	DAC702	16	±0.0015	1	±1mA	Com, Ind, Mil	DDIP	Q, BI	6.1-43
	DAC703	16	±0.0015	8	±10V	Com, Ind, Mil	DDIP, SO	Q, BI	6.1-43
Low DLE Around Zero	DAC710	16	±0.0015	8 typ	±1mA	Com	DDIP	—	6.1-65
	DAC711	16	±0.0015	8 typ	±10V	Com	DDIP	—	6.1-65
Lowest Cost	DAC1600	16	±0.003	8 typ	±10V	Com	DDIP	—	6.1-108
Bus Interface:									
16-Bit Parallel	DAC707	16	±0.003	8	±10V	Com, Ind, Mil	DDIP	Q, BI	6.1-53
Serial/8-bit Parallel	DAC708	16	±0.003	1	±1mA, –2mA	Com, Ind, Mil	DDIP	Q, BI	6.1-53
Serial/8-bit Parallel	DAC709	16	±0.003	8	±5V, ±10V, +10V	Com, Ind, Mil	DDIP	Q, BI	6.1-53
Dual,Ser./8-bit Par.	DAC725	16	±0.003	8	±10V	Com, Ind	DDIP	BI	6.1-72
Industry Standard, General Purpose	DAC70BH	16	±0.003	1	±1mA, –2mA	Ind	DDIP	BI	6.1-5
	DAC71	16	±0.003	8	±1mA, –2mA; +10V, ±10V	Com	DDIP	BI	6.1-13
	DAC72BH	16	±0.003	1	"	Ind	DDIP	BI	6.1-5
Industry Standard	DAC7541A	12	±0.012	1	0 to 1mA	Com, Ind, Mil	DDIP, SO	Q, BI	6.1-112
Ind. Std. w/Latch	DAC7545	12	±0.012	2	0 to 1mA	Com, Ind, Mil	DDIP, SO	BI	6.1-120
Dual w/Bus Interface:									
Serial Input	**DAC7800**	**12**	**±0.012**	**0.8**	**0 to 1mA**	**Com**	**DIP, SO**	—	**S6.1-17**
8-bit Port Interface	**DAC7801**	**12**	**±0.012**	**0.8**	**0 to 1mA**	**Com**	**DIP, SO**	—	**S6.1-17**
12-bit Port Interface	**DAC7802**	**12**	**±0.012**	**0.8**	**0 to 1mA**	**Com**	**DIP, SO**	—	**S6.1-19**
Flexible Bus Interface:									
Industry Standard Pinout	**DAC667**	**12**	**±0.006**	**4**	**±2.5V, ±5V,±10V +5V, +10V**	**Com, Ind, Mil**	**DIP, SO**	—	**S6.1-5**
	DAC811	12	±0.006	4	±5V, ±10V, +10V	Com, Ind, Mil	DDIP, SO	BI	6.1-90
Small, Low Cost	**DAC813**	**12**	**±0.006**	**4**	**±5V, ±10V, +10V**	**Com, Ind, Mil**	**DIP, SO**	—	**S6.1-7**
Lowest Cost	DAC1201	12	±0.018	4 typ	±5V, ±10V, +10V	Com	DDIP	—	6.1-103
Industry Standard, General Purpose	DAC80	12	±0.012	0.3, 3 typ	±1mA, –2mA; +5V, +10V, ±5V, ±10V	Com	DDIP	BI	6.1-27
	DAC85H	12	±0.012	"	"	Ind	DDIP	Q, BI	6.1-35
	DAC87H	12	±0.012	"	"	Mil	DDIP	Q, BI	6.1-35

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ind = (–25°C to +85°C) or (–40°C to +85°C), Mil = –55°C to +125°C. (2) DIP = 0.3" wide DIP, DDIP = 0.6" wide DIP, SO = small outline surface mount. (3) Q indicates that optional reliability screening is available for the model. BI indicates that an optional 160 hour burn-in is available for the model.

AUDIO AND COMMUNICATIONS DIGITAL-TO-ANALOG CONVERTERS **Boldface = NEW**

Model	Resolution (Bits)	Max THD + N (V_{OUT} = FS)	Output Range	Input Format	Power Supply (V)	Package[1]	Power Dissipation (mW)	Page No.
PCM53	16	–88dB (JP) –92dB (KP)	±10V, ±1mA	Parallel	±15, +5	DDIP	600	6.2-152
PCM54	16	–82dB (HP) –88dB (JP) –92dB (KP)	±3V, ±1mA	Parallel	±5 to ±12	DDIP	300	6.2-164
PCM55	16	–82dB (HP) –88dB (JP)	±3V, ±1mA	Parallel	±5	SO	125	6.2-164
PCM56	16	–82dB (P) –88dB (P-J) –92dB (P-K)	±3V, ±1mA	Serial Latched	±5 to ±12	DIP	260	6.2-172
PCM60	**16**	**–82dB (P) –86dB (P-J)**	**2.8Vp-p, 2-Channel**	**Serial Latched**	**+5**	**SO**	**50**	**S6.2-27**
PCM66	**16**	**–82dB (P)**	**2.8Vp-p, 2-Channel**	**Serial Latched**	**+5**	**SO**	**50**	**S6.2-27**
PCM1700	**18**	**–82dB (P) –88dB (P-J) –92dB (P-K)**	**±3V, ±0.67mA**	**Serial Latched**	**±5**	**DDIP**	**380**	**S9.2-183**
PCM58	18	–92dB (P) –94dB (P-J) –96dB (P-K)	±1mA	Serial Latched	+5, –12	DDIP	400	6.2-180
PCM61	**18**	**–82dB (P) –88dB (P-J) –92dB (P-K)**	**±3V, ±1mA**	**Serial Latched**	**±5 to ±12**	**DDIP**	**200**	**S6.2-35**
PCM63	**20**	**–88dB (P) –92dB (P-J) –96dB (P-K)**	**±2mA**	**Latched**	**±5**	**DDIP**	**200**	**S6.2-39**
PCM64	18	–96dB	±1mA	Parallel	+5, –15	DIP	400	6.2-194

NOTES: (1) DIP = 0.3" wide DIP, DDIP = 0.6" wide DIP, SO = Small Outline Surface Mount.

DIGITAL SIGNAL PROCESSING DIGITAL-TO-ANALOG CONVERTERS **Boldface = NEW**

Model	Resolution (Bits)	Linearity Error (%FSR)	Settling Time (μs)	Output Range	Signal-to-Noise + Distortion Ratio (dB)	Total Harmonic Distortion (dB)	Temp Range[1]	Pkg[2]	Page No.
DSP-Compatible Digital Interface (Single—DSP201, Dual—DSP202):									
DSP201	**18**	**±0.006**	**—**	**±3V**	**86, f_{OUT} = 2kHz**	**–90**	**Ind**	**DDIP**	**S14-16**
DSP202	**18**	**±0.006**	**—**	**±3V**	**86, f_{OUT} = 2kHz**	**–90**	**Ind**	**DDIP**	**S14-16**
Ultra-Fast Settling, ECL Input:									
DAC65	12	±0.012	40ns	±1.2V, ±6.35mA	70, f_{OUT} = 1MHz	–68	Com	DDIP	6.2-143
DAC63	12	±0.012	50ns	±5mA, 0 to –10mA ±0.5V, 0 to +1.5V with internal resistor	—	—	Ind	DDIP	6.2-135
Ultra-Fast Settling, TTL Input:									
DAC812	12	±0.012	50ns	±5mA, 0 to –10mA ±0.5V, 0 to –1.5V with internal resistor	—	—	Ind	DDIP	6.2-146

NOTES: (1) Com = 0°C to +70°C, Ind = (–25°C to +85°C) or (–40°C to +85°C). (2) DDIP = 0.6" wide DIP.

MODELS STILL AVAILABLE BUT NOT FEATURED IN THIS BOOK

DAC10HT
DAC90BG
DAC90SG
DAC800P-CBI-V
DAC800P-CBI-I
DAC800-CBI-V
DAC800-CBI-I
DAC850-CBI-V
DAC850-CBI-I
DAC851-CBI-V
DAC851-CBI-I

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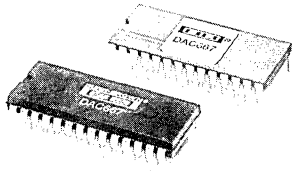


DAC667

ADVANCE INFORMATION
SUBJECT TO CHANGE

Microprocessor-Compatible 12-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- ±1/2LSB MAX NONLINEARITY OVER TEMP.
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- MICROCOMPUTER INTERFACE: DOUBLE-BUFFERED LATCH
- VOLTAGE OUTPUT: ±10V, ±5V, +10V WITH ±11.4V SUPPLIES
- GUARANTEED SPECS AT ±12V AND ±15V SUPPLIES, NO 5V SUPPLY REQUIRED
- LOW POWER DISSIPATION: 250mW Max
- TTL/5V CMOS-COMPATIBLE LOGIC INPUTS
- PIN COMPATIBLE WITH AD667
- 28-PIN 600 MIL WIDE CERAMIC OR PLASTIC DIP PACKAGE

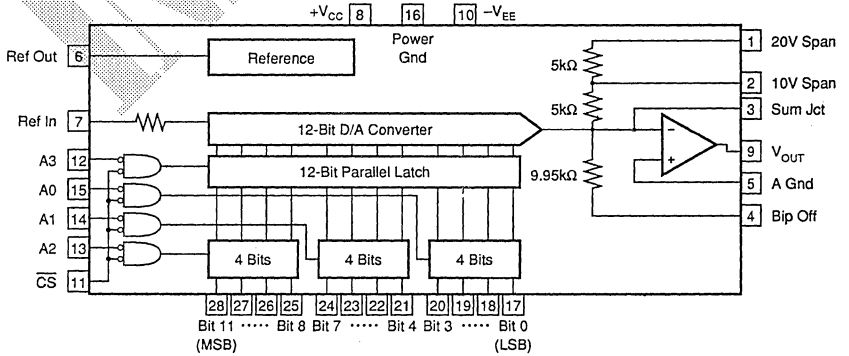
DESCRIPTION

The DAC667 is a complete monolithic integrated circuit microcomputer 12-bit digital-to-analog converter. It includes a precision voltage reference, microcomputer interface logic, double-buffered latch, and a 12-bit D/A converter with a voltage output amplifier. Fast current switches and a laser-trimmed thin-film resistor network provide a highly accurate and fast D/A converter.

A double-buffered latch facilitates microcomputer interfacing. The design of the input latch allows direct interface to 4-, 8-, 12-, or 16-bit data buses. The input buffer latches hold the 12-bit data until able to transfer to an internal 12-bit D/A converter latch, giving precise timing control over analog output change.

Input gating logic is designed so that loading of data can be accomplished simultaneously with the transfer of data (previously stored in adjacent latches) from input latches to the D/A latch. This feature avoids spurious analog output values while using an interface technique that saves computer instructions. The digital feedthrough of the DAC667 is minimized by the lack of high-impedance pins to pick up noise and by the use of separate digital supply and ground pins ($+V_D$ and DCOM).

The DAC667 is specified to ±1/4LSB maximum linearity error (B and K grades) at 25°C and ±1/2LSB maximum over the temperature range. All grades are guaranteed monotonic over the specification temperature range. The DAC667 is available in two performance grades and in plastic and ceramic package types.



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PDS-1080

SPECIFICATIONS

ELECTRICAL

T_A = +25°C. $+V_{CC}$, $-V_{EE}$ = ±12V or ± 15V and load on V_{OUT} = 5kΩ to ground unless otherwise noted.

PARAMETER	DAC667AH, JP MIN	DAC667AH, JP TYP	DAC667AH, JP MAX	DAC667BH, KP MIN	DAC667BH, KP TYP	DAC667BH, KP MAX	UNITS
DIGITAL INPUT							
Resolution			12			•	Bits
Logic Levels, TTL Compatible T_{MIN} to T_{MAX}							
V_{IH}	+2.0		+5.5	•		•	VDC
V_{IL}	+0		+0.8	•		•	VDC
I_{IH}, V_H = 5.5V		2	10			•	µA
I_{IL}, V_L = 0.8V		2	5			•	µA
ACCURACY ($+V_{CC}$, $-V_{EE}$ = ±12V or ± 15V)							
Linearity Error at 25°C		±1/4	±1/2		±1/8	±1/4	LSB
$T_A = T_{MIN}$ to T_{MAX}		±1/2	±3/4		±1/4	±1/2	LSB
Differential Linearity Error		±1/2	±3/4		±1/4	±1/2	LSB
$T_A = T_{MIN}$ to T_{MAX}		Monotonicity Guaranteed			Monotonicity Guaranteed		LSB
Gain Error[1]		±0.1	±0.2		•	•	%
Unipolar Offset Error[1]		±1	±2		•	•	LSB
Bipolar Offset Error[1]		±0.05	±0.1		•	•	% of FSR[2]
DRIFT (Over Specification Temperature Range)							
Differential Linearity		±2			•		ppm of FSR/°C
Gain (Full Scale), T_A = 25°C to T_{MIN} or T_{MAX}		±5	±30		±10	±15	ppm of FSR/°C
Unipolar Offset, T_A = 25°C to T_{MIN} or T_{MAX}		±1	±3		•	•	ppm of FSR/°C
Bipolar Zero, T_A = 25°C to T_{MIN} or T_{MAX}		±5	±10		•	•	ppm of FSR/°C
CONVERSION SPEED							
Settling Time (To Within ±0.01% of FSR for FSR Change; 2kΩ || 500pF Load)							
With 10kΩ Feedback		3	4		•	•	µs
With 5kΩ Feedback		2	3		•	•	µs
For 1LSB Change		2			•		µs
Slew Rate	10			•			V/µs
ANALOG OUTPUT							
Voltage Range, $+V_{CC}$, $-V_{EE}$ > ±11.4V		±2.5, ±5, ±10			•		V
		0 to +5, +10			•		V
Output Current	±5			•			mA
Output Impedance (at DC)		0.05			•		Ω
Short Circuit Current			40			•	mA
REFERENCE VOLTAGE							
Voltage	+9.9	+10.0	+10.1	•	•	•	V
External Current	+0.1	+1.0		•	•		mA
POWER SUPPLY SENSITIVITY							
$+V_{CC}$ = +11.4 to +16.5VDC		5	10		•	•	ppm of FS/%
$-V_{EE}$ = −11.4 to −16.5VDC		1	10		•	•	ppm of FS/%
POWER SUPPLY REQUIREMENTS							
Rated Voltages		±12, ±15			•		V
Ranges	±11.4		±16.5	•		•	V
Supply Current (No Load):							
+11.4 to +16.5VDC		10	15		•	•	mA
−11.4 to −16.5VDC		7.5	11		•	•	mA
TEMPERATURE RANGE							
Specification: J, K	0		+70	•		•	°C
A, B	−25		+85	•		•	°C
Storage: J, K	−65		+125	•		•	°C
A, B	−65		+150	•		•	°C

*Same as specification for DAC667AH, JP.

NOTES: (1) Adjustable to zero with external trim potentiometer. (2) FSR means Full Scale Range and is 20V for the ±10V range.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Power Ground	0 to +18V
$-V_{CC}$ to Power Ground	0 to -18V
Digital Inputs (pins 11-15, 17-28) to Power Ground	−1.0V to +7.0V
External Voltage Applied to BPO Span Resistor	±18V
Ref In to Reference Ground	±12V
Bipolar Offset to Reference Ground	±12V
10V Span Resistor to Reference Ground	±12V
20V Span Resistor to Reference Ground	±24V
Ref Out, V_{OUT} (Pins 6, 9)	Indefinite Short to Power Ground
Ref Out, V_{OUT} (Pins 6, 9)	Momentary Short to +V
Power Dissipation	1000mW
Lead Temperature (soldering 10s)	+300°C
Max Junction Temperature	165°C
Thermal Resistance, θ_{J-A}: Plastic DIP	130°C/W
Thermal Resistance, θ_{J-A}: Ceramic DIP	85°C/W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

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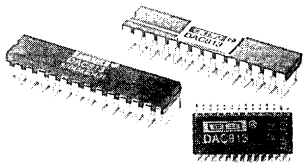


DAC813

ADVANCE INFORMATION
SUBJECT TO CHANGE

Microprocessor-Compatible 12-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- ±1/2LSB NONLINEARITY OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- LOW POWER: 270mW max
- DIGITAL INTERFACE DOUBLE BUFFERED: 12 AND 8 + 4 BITS
- SPECIFIED AT ±12V AND ±15V POWER SUPPLIES
- RESET FUNCTION TO BIPOLAR ZERO
- 0.3" WIDE DIP AND SO PACKAGES

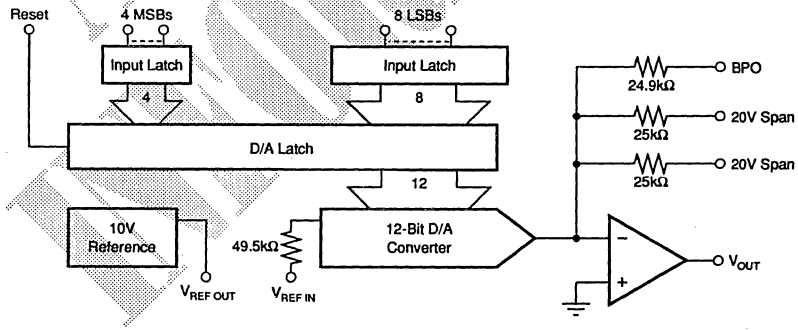
DESCRIPTION

The DAC813 is a complete monolithic 12-bit digital-to-analog converter with a flexible digital interface. It includes a precision +10V reference, interface control logic, double-buffered latch and a 12-bit D/A converter with voltage output operational amplifier. Fast current switches and laser-trimmed thin-film resistors provide a highly accurate, fast D/A converter.

Digital interfacing is facilitated by a double buffered latch. The input latch consists of one 8-bit byte and one 4-bit nibble to allow interfacing to 8-bit (right justified format) or 16-bit data buses. Input gating logic is designed so that the last nibble or byte to be loaded can be loaded simultaneously with the transfer of data to the D/A latch saving computer instructions.

A reset control allows the DAC813 D/A latch to asynchronously reset the D/A output to bipolar zero, a feature useful for power-up reset, recalibration, or for system re-initialization upon system failure.

The DAC813 is specified to ±1/2LSB maximum linearity error (J, A grades) and ±1/4LSB (K, B grades). It is packaged in a 28-pin 0.3" wide ceramic DIP (–25°C to +85°C specification temperature range), 28-pin 0.3" wide plastic DIP and 28-lead plastic SO (0°C to +70°C).



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PDS-1077

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, $\pm V_{CC}$ = ±12V or ±15V and load on V_{OUT} = 5kΩ to ground unless otherwise noted.

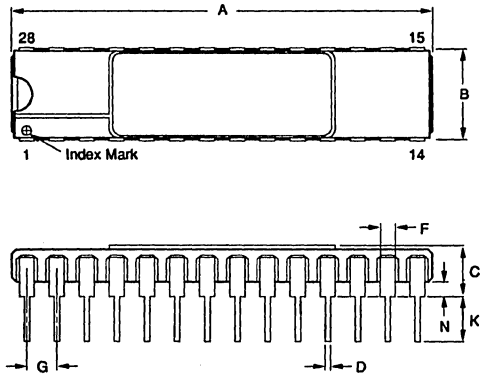
PARAMETER	CONDITIONS	DAC813AH, JP, JU			DAC813BH, KP, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUT								
Resolution				12			•	Bits
Codes[1]			USB, BOB			•		
Digital Inputs Over Temperature Range[2]								
V_{IH}		+2		+5.5	•		•	VDC
V_{IL}		0		+0.8	•		•	VDC
DATA Bits	I_{IH}, V_{IN} = +2.7V			±10			•	µA
	I_{IL}, V_{IN} = +0.4V			±10			•	µA
$\overline{WR}$, Reset, $\overline{LDAC}$, $\overline{LMSB}$, $\overline{LLSB}$	I_{IH}, V_{IN} = +2.7V			±10			•	µA
	I_{IL}, V_{IN} = +0.4V			±10			•	µA
ACCURACY								
Linearity Error			±1/4	±1/2		±1/8	±1/4	LSB
Differential Linearity Error			±1/2	±3/4		±1/4	±1/2	LSB
Gain Error[3]			±0.05	±0.2		•	•	%
Unipolar Offset Error[4]			±0.01	±0.02		•	•	% of FSR[6]
Bipolar Zero Error[5]			±0.02	±0.2		TBD	TBD	% of FSR
Monotonicity			Guaranteed			•		
Power Supply Sensitivity: $+V_{CC}$	20V Range		5	10		•	•	ppm of FSR/%
$-V_{CC}$			1	10			•	ppm of FSR/%
DRIFT	Over Specification							
Gain	Temperature Range		±5	±30		•	±15	ppm/°C
Unipolar Offset			±1	±3		•	±3	ppm of FSR/°C
Bipolar Zero			±3	±10		•	±5	ppm of FSR/°C
Linearity Error Over Temperature Range			±1/2	±3/4		±1/4	±1/2	LSB
Monotonicity Over Temperature Range			Guaranteed			•		
SETTLING TIME[7] (To Within ±0.01% of FSR of Final Value; 5kΩ || 500pF load)								
For Full Scale Range Change	20V Range		4	5		•	•	µs
	10V Range		3	4		•	•	µs
For 1LSB Change at Major Carry[8]			2			•		µs
Slew Rate			10			•		V/µs
ANALOG OUTPUT								
Voltage Range: Unipolar	$\pm V_{CC}$ > ±11.4V		0 to +10			•		V
Bipolar	$\pm V_{CC}$ > ±11.4V		±5, ±10			•		V
Output Current		±5			•			mA
Output Impedance	At DC		0.2			•		Ω
Short Circuit to Common Duration			Indefinite			•		
REFERENCE VOLTAGE								
Voltage		+9.95	+10	+10.05	•	•	•	V
Source Current Available for External Loads		5			•			mA
Impedance			2			•		Ω
Temperature Coefficient			±10	±40		•	±25	ppm/°C
Short Circuit to Common Duration			Indefinite			•		
POWER SUPPLY REQUIREMENTS								
Voltage: $+V_{CC}$		+11.4	+15	+16.5	•	•	•	VDC
$-V_{CC}$		−11.4	−15	−16.5	•	•	•	VDC
Current: $+V_{CC}$	No Load		10	13		•	•	mA
$-V_{CC}$	No Load		−5	−6		•	•	mA
Potential at DCOM with Respect to ACOM[9]		−3		+3	•		•	V
Power Dissipation			225	270		•	•	mW
TEMPERATURE RANGE								
Specification: J, K		0		+70	•		•	°C
A, B		−25		+85	•		•	°C
Storage: J, K		−60		+100	•		•	°C
A, B		−65		+150	•		•	°C

*Same as specification for DAC813AH, JP, JU.

NOTES: (1) USB = Unipolar Straight Binary; BOB = Bipolar Offset Binary. (2) TTL and 5V CMOS compatible. (3) Specified with 500Ω Pin 6 to 7. Adjustable to zero with external trim potentiometer. (4) Error at input code 000_{HEX} for unipolar mode, FSR = 10V. (5) Error at input code 800_{HEX} for bipolar range. Specified with 100Ω Pin 6 to 4 and with 500Ω pin 6 to 7. See page 9 for zero adjustment procedure. (6) FSR means Full Scale Range and is 20V for the ±10V range. (7) Maximum represents the 3σ limit. Not 100% tested for this parameter. (8) At the major carry, $7FF_{HEX}$ to 800_{HEX} and 800_{HEX} to $7FF_{HEX}$. (9) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

MECHANICAL

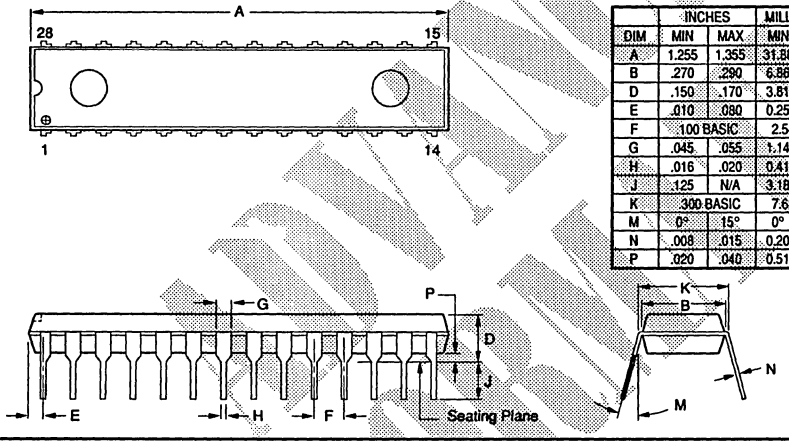
H Package — 0.3" 28-Pin Hermetic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.388	1.412	35.26	35.86
B	.300	.320	7.62	8.13
C	—	.160	—	4.06
D	.016	.020	0.41	0.51
F	.050 BASIC		1.27 BASIC	
G	.095	.105	2.41	2.67
J	.009	.012	0.23	0.30
K	.125	.180	3.18	4.57
L	.290	.310	7.37	7.87
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package. Metal lid connected to $-V_{CC}$.

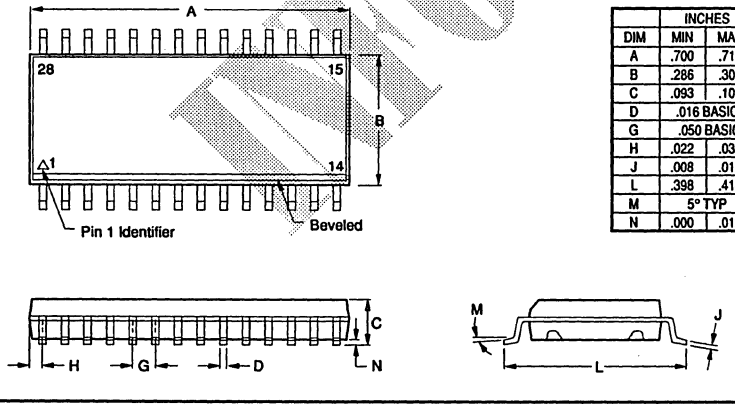
P Package — 0.3" 28-Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.255	1.355	31.88	34.42
B	.270	.290	6.86	7.37
D	.150	.170	3.81	4.32
E	.010	.080	0.25	2.03
F	.100 BASIC		2.54 BASIC	
G	.045	.055	1.14	1.40
H	.016	.020	0.41	0.51
J	.125	N/A	3.18	N/A
K	.300 BASIC		7.62 BASIC	
M	0°	15°	0°	15°
N	.008	.015	0.20	0.38
P	.020	.040	0.51	1.02

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

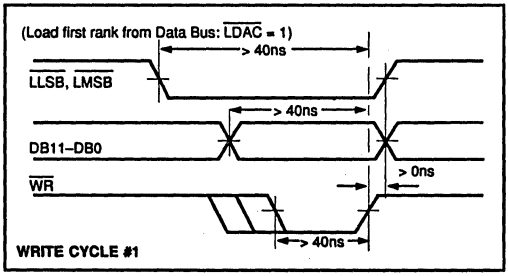
U Package — 28-Pin Plastic SOIC

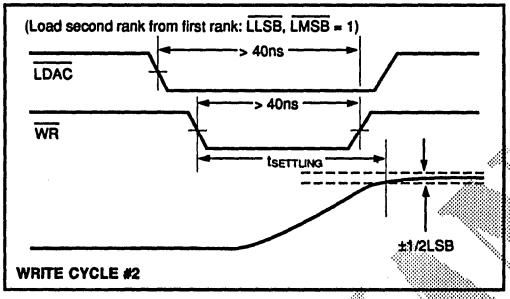


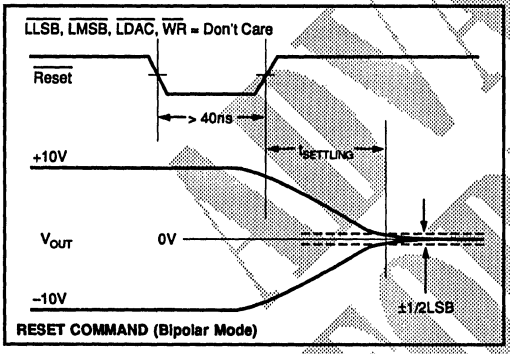
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.700	.716	17.78	18.19
B	.286	.302	7.26	7.67
C	.093	.109	2.36	2.77
D	.016 BASIC		0.41 BASIC	
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.398	.414	10.11	10.52
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

MINIMUM TIMING DIAGRAMS







PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	$+V_D$	This point is internally connected to $+V_s$ and is a decoupling point only. Separate bypass capacitors will minimize internal digital feedthrough to analog signals.
2, 3	20V Range	Connect Pin 2 or Pin 3 to Pin 9 (V_{OUT}) for a 20V FSR. Connect both to Pin 9 for a 10V FSR.
4	BPO	Bipolar offset. Connect to Pin 6 ($V_{REF\ OUT}$) through 100Ω resistor or 200Ω potentiometer for bipolar operation.
5	ACOM	Analog common, $\pm V_{CC}$ supply return.
6	$V_{REF\ OUT}$	+10V reference output.
7	$V_{REF\ IN}$	Connected to $V_{REF\ OUT}$ through a 1kΩ gain adjustment potentiometer or a 500Ω resistor.
8	$+V_{CC}$	Analog supply input, nominally +12V to +15V referred to ACOM.
9	V_{OUT}	D/A converter voltage output.
10	$-V_{CC}$	Analog supply input, nominally –12V or –15V referred to ACOM.
11	$\overline{WR}$	Master enable for $\overline{LDAC}$, $\overline{LLSB}$, and $\overline{LMSB}$. Must be low for data transfer to any latch.
12	$\overline{LDAC}$	Load DAC. Must be low with $\overline{WR}$ for data transfer to the D/A latch and simultaneous update of the D/A converter.
13	$\overline{Reset}$	When low, resets the D/A latch such that a Bipolar Zero output is produced. This control overrides all other data input operations.
14	$\overline{LMSB}$	Enable for 4-bit input latch of D8-D11 data inputs.
15	$\overline{LLSB}$	Enable for 8-bit input latch of D0-D7 data inputs.
16	DCOM	Digital common.
17	D0	Data Bit 1, LSB.
18	D1	Data Bit 2.
19	D2	Data Bit 3.
20	D3	Data Bit 4.
21	D4	Data Bit 5.
22	D5	Data Bit 6.
23	D6	Data Bit 7.
24	D7	Data Bit 8.
25	D8	Data Bit 9.
26	D9	Data Bit 10.
27	D10	Data Bit 11.
28	D11	Data Bit 12, MSB, positive true.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to ACOM	0 to +18V
$-V_{CC}$ to ACOM	0 to –18V
$+V_{CC}$ to $-V_{CC}$	0 to +36V
ACOM to DCOM	±18V
Digital Inputs (Pins 11–15, 17–28) to DCOM	±18V
External Voltage Applied to BPO Span Resistor	±18V
$V_{REF\ OUT}$	Indefinite Short to ACOM
V_{OUT}	Indefinite Short to ACOM

Power Dissipation	750mW
Lead Temperature (soldering, 10s)	+300°C
Max Junction Temperature	+165°C
Thermal Resistance, θ_{J-A}: Plastic DIP and SOIC	130°C/W
Ceramic DIP	85°C/W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

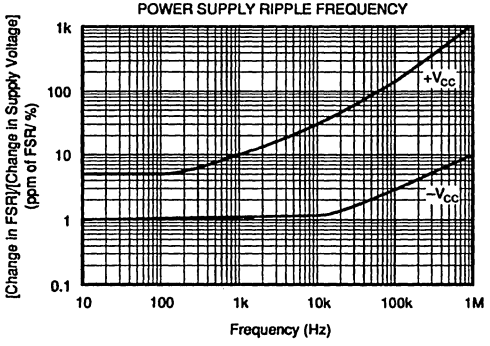
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	LINEARITY ERROR, MAX AT +25°C	GAIN DRIFT (ppm/°C)
DAC813JP	Plastic DIP	0°C to +70°C	±1/2LSB	30
DAC813JU	Plastic SOIC	0°C to +70°C	±1/2LSB	30
DAC813KP	Plastic DIP	0°C to +70°C	±1/4LSB	20
DAC813KU	Plastic SOIC	0°C to +70°C	±1/4LSB	20
DAC813AH	Ceramic DIP	–25°C to +85°C	±1/2LSB	30
DAC813BH	Ceramic DIP	–25°C to +85°C	±1/4LSB	20

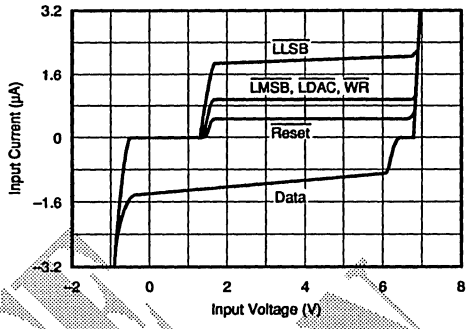
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.

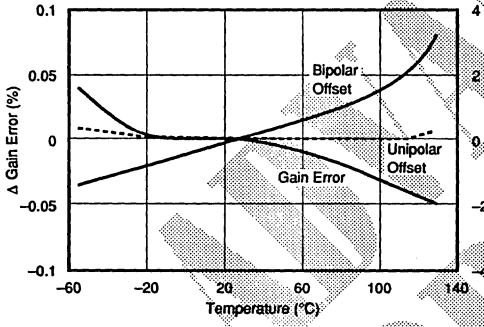
POWER SUPPLY REJECTION vs POWER SUPPLY RIPPLE FREQUENCY



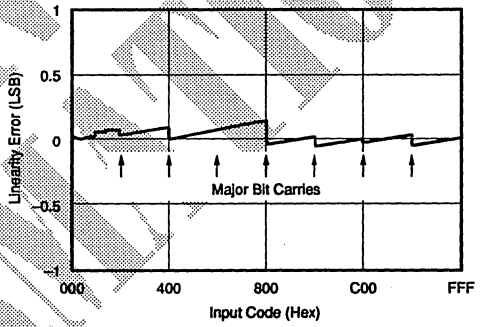
DIGITAL INPUT CURRENT vs INPUT VOLTAGE



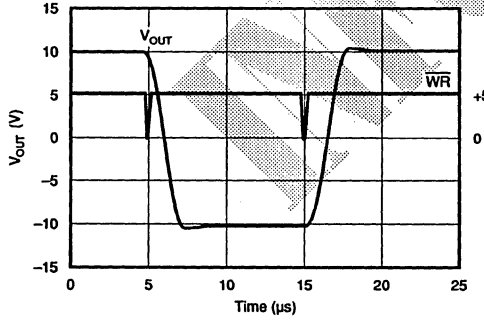
CHANGE OF GAIN AND OFFSET ERROR vs TEMPERATURE



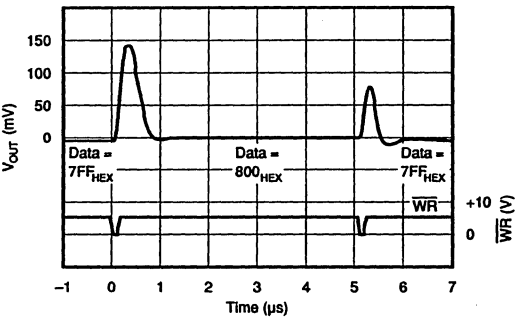
INTEGRAL LINEARITY ERROR



± FULL SCALE OUTPUT SWING

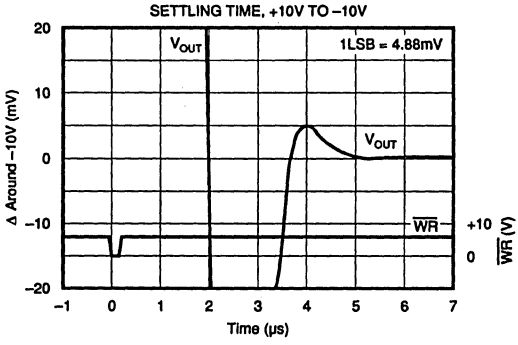


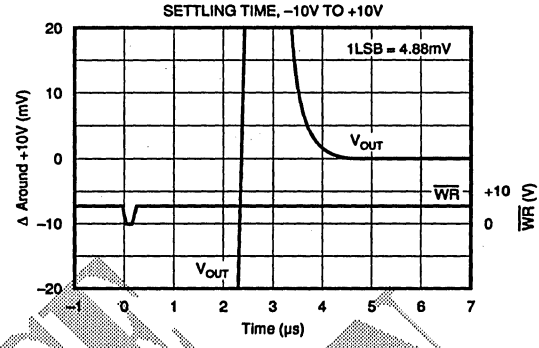
MAJOR CARRY GLITCH



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.





DISCUSSION OF SPECIFICATIONS

INPUT CODES

The DAC813 accepts positive-true binary input codes. DAC813 may be connected by the user for any one of the following codes: USB (Unipolar Straight Binary), BOB (Bipolar Offset Binary) or, using an external inverter on the MSB line, BTC (Binary Two's Complement). See Table I.

DIGITAL INPUT MSB to LSB	ANALOG OUTPUT USB Unipolar Straight Binary	BOB Bipolar Offset Binary	BTC* Binary Two's Complement
FFF_{HEX}	+ Full Scale	+ Full Scale	Zero – 1LSB
800_{HEX}	+ 1/2 Full Scale	Zero	– Full Scale
$7FF_{HEX}$	+ 1/2 Full Scale – 1LSB	Zero – 1LSB	+ Full Scale
000_{HEX}	Zero	– Full Scale	Zero

* Invert MSB of BOB code with external inverter to obtain BTC code.

TABLE I. Digital Input Codes.

LINEARITY ERROR

Linearity error as used in D/A converter specifications by Burr-Brown is the deviation of the analog output from a straight line drawn between the end points (inputs all "1s" and all "0s"). The DAC813 linearity error is specified at ±1/4LSB (max) at +25°C for B and K grades, and ±1/2LSB (max) for A and J grades.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of 1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the input changes from one state to the next. Monotonicity requires that DLE be less than 1LSB over the temperature range of interest.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital inputs. All grades of DAC813 are monotonic over their specification temperature range.

DRIFT

Drift specifications are determined by taking readings at high temperature, room temperature (25°C) and low temperature where high and low temperatures are the specification temperature range limits. Two drift numbers are calculated: the change from room to high temperature, divided by the temperature change, and the change from room to low temperature, divided by the temperature change. The largest drift number is used for determining the drift specifications.

Gain Drift is a measure of the change in the Full Scale Range (FSR) output over the specification temperature range. Gain Drift is expressed in parts per million per degree Celsius (ppm/°C).

Unipolar Offset Drift is measured with a data input of 000_{HEX}. The D/A is configured for unipolar output. Unipolar Offset Drift is expressed in parts per million of Full Scale Range per degree Celsius (ppm of FSR/°C).

Bipolar Zero Drift is measured with a data input of 800_{HEX}. The D/A is configured for bipolar output. Bipolar Zero Drift is expressed in parts per million of Full Scale Range per degree Celsius (ppm of FSR/°C).

SETTLING TIME

Settling Time is the total time (including slew time) for the output to settle within an error band around its final value after a change in input. Three settling times are specified to ±0.012% of Full Scale Range (FSR): two for maximum full scale range changes of 20V and 10V, and one for a 1LSB

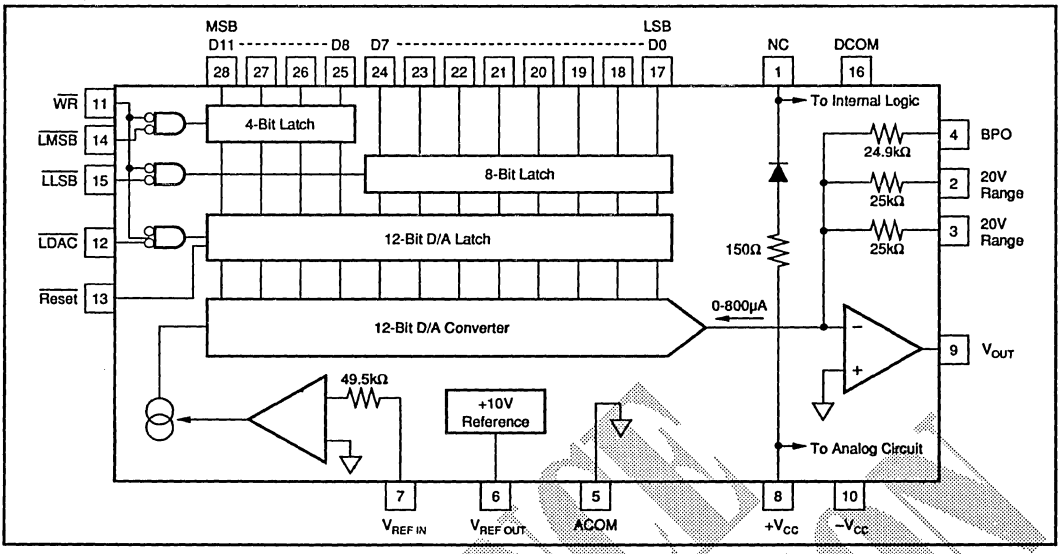


FIGURE 1. DAC813 Block Diagram.

change. The 1LSB change is measured at the major carry ($7FF_{HEX}$ to 800_{HEX} and 800_{HEX} to $7FF_{HEX}$), the input transition at which worst-case settling time occurs.

REFERENCE SUPPLY

DAC813 contains an on-chip +10V reference. This voltage (pin 6) has a tolerance of ±50mV. $V_{REF\ OUT}$ must be connected to $V_{REF\ IN}$ through a gain adjust resistor with a nominal value of 500Ω. The connection can be made through an optional 1kΩ trim resistor to provide adjustment to zero gain error. The reference output may be used to drive external loads, sourcing at least 5mA. This current should be constant, otherwise the gain of the converter may vary.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a ppm of FSR output change per percent of change in either $+V_{CC}$ or $-V_{CC}$ about the nominal voltages expressed in ppm of FSR/%. The first performance curve on page 5 shows typical power supply rejection versus power supply ripple frequency.

OPERATION

DAC813 is a complete single IC chip 12-bit D/A converter. The chip contains a 12-bit D/A converter, voltage reference, output amplifier, and microcomputer-compatible input logic as shown in Figure 1.

INTERFACE LOGIC

Input latches hold data temporarily while a complete 12-bit word is assembled before loading into the D/A latch. This double-buffered organization prevents the generation of spurious analog output values. Each latch is independently addressable.

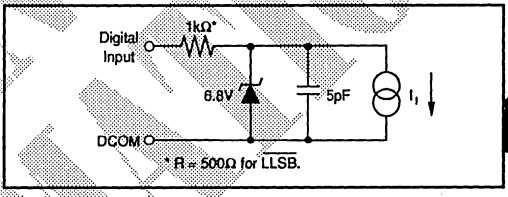


FIGURE 2. Equivalent Input Circuit for Digital Inputs.

WR	LLSB	LMSB	LDAC	RESET	OPERATION
1	X	X	X	1	No operation
X	X	X	X	0	D/A latch set to 800_{HEX}
0	1	0	1	1	Enables 4 MSBs input latch
0	0	1	1	1	Enables 8 LSBs input latch
0	1	1	0	1	Loads D/A latch from input latches
0	0	0	0	1	Makes all latches transparent

"X" = Don't Care

TABLE II. DAC813 Interface Logic Truth Table.

All latches are level-triggered. Data present when the control signals are logic "0" will enter the latch. When any one of the control signals returns to logic "1", the data is latched. A truth table for the control signals is presented in Table II.

LOGIC INPUT COMPATIBILITY

The DAC813 digital inputs are TTL, 5V CMOS compatible over the operating range of $+V_{CC}$. The input switching threshold remains at the TTL threshold over the supply range.

The logic input current over temperature is low enough to permit driving the DAC813 directly from the outputs of 5V CMOS devices.

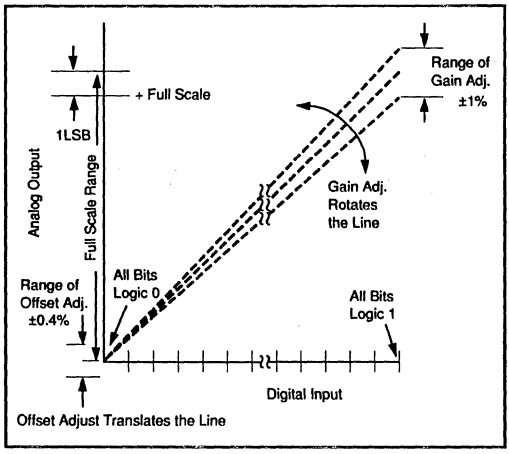


FIGURE 3. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

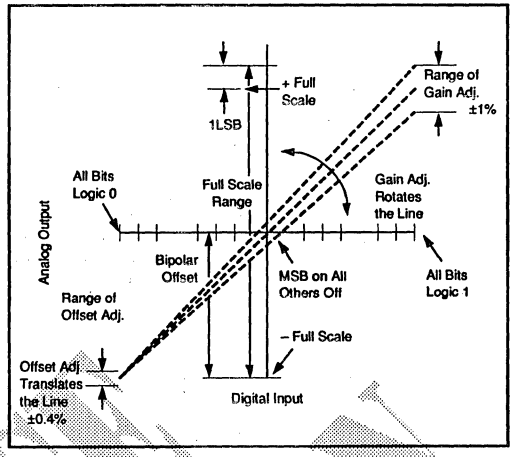


FIGURE 4. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

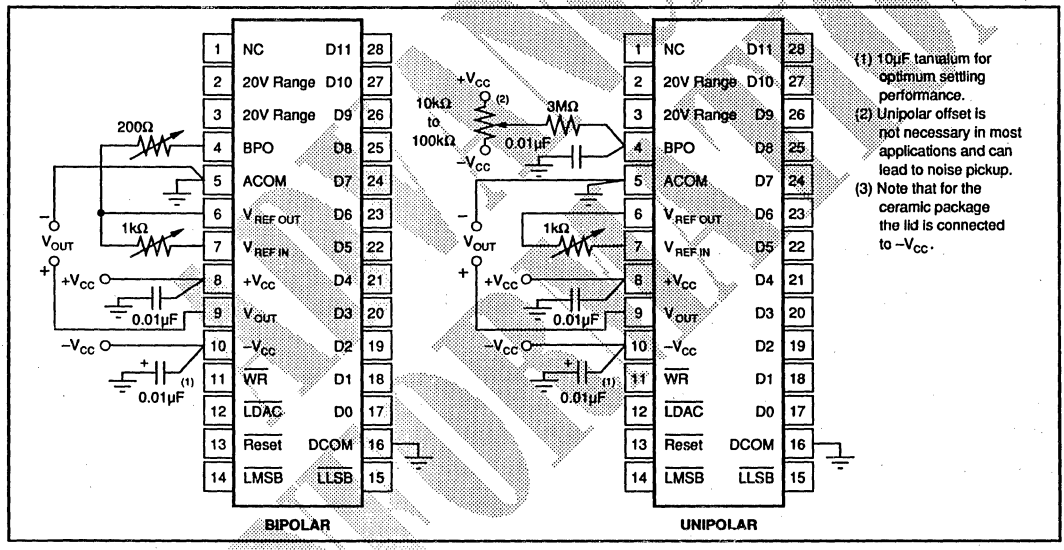


FIGURE 5. Power Supply, Gain, and Offset Connections.

RESET FUNCTION

When asserted low (<0.8V), $\overline{\text{Reset}}$ (Pin 13) forces the D/A latch to 800_{HEX} regardless of any other input logic condition. If the analog output is connected for bipolar operation (either ±10V or ±5V), the output will be reset to Bipolar Zero (0V). If the analog output is connected for unipolar operation (0 to +10V), the output will be reset to half-scale (+5V).

If $\overline{\text{Reset}}$ is not used, it should be connected to a voltage greater than +2V but not greater than +5.5V. If this voltage is not available $\overline{\text{Reset}}$ can be connected to $+V_{CC}$ through a 100kΩ to 1MΩ resistor to limit the input current.

DIGITAL INPUT	ANALOG OUTPUT		
MSB to LSB	0 to +10V	±5V	±10V
FFF_{HEX}	+9.9976V	+4.9976V	+9.9951V
800_{HEX}	+5.0000V	0.0000V	0.0000V
$7FF_{HEX}$	+4.9976V	–0.0024V	–0.0049V
000_{HEX}	0.0000V	–5.0000V	–10.0000V
1LSB	2.44mV	2.44mV	4.88mV

TABLE III. Digital Input/Analog Output.

GAIN AND OFFSET ADJUSTMENTS

Figures 3 and 4 illustrate the relationship of offset and gain adjustments to unipolar and bipolar D/A converter output.

OFFSET ADJUSTMENT

For unipolar (USB) configurations, apply the digital input code that should produce zero voltage output and adjust the offset potentiometer for zero output. For bipolar (BOB, BTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the offset potentiometer for minus full scale voltage. Example: If the full scale range is connected for 20V, the maximum negative output voltage is –10V. See Table III for corresponding codes.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the gain potentiometer for this positive full scale voltage. See Table III for positive full scale voltages.

INSTALLATION

POWER SUPPLY CONNECTIONS

Note that the lid of the ceramic packaged DAC813 is connected to $-V_{CC}$. Take care to avoid accidental short circuits in tightly spaced installations.

Power supply decoupling capacitors should be added as shown in Figure 5. Best performance occurs using a 1 to 10µF tantalum capacitor at $-V_{CC}$ and at least a 0.01µF ceramic capacitor at $+V_{CC}$. Applications with less critical settling time may be able to use 0.01µF at $-V_{CC}$ as well.

These capacitors should be located close to the DAC813.

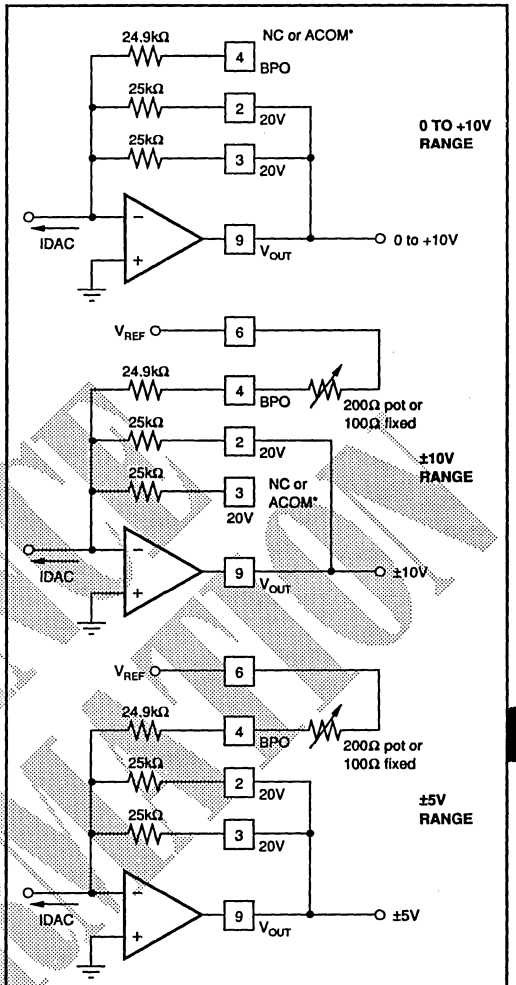
Pin 1 is connected to an internal logic supply and should not be used. A voltage about 1V lower than $+V_{CC}$ is present on the pin. In extreme digital noise environments, a decoupling capacitor of 0.01µF on pin 1 may help reduce D/A output noise.

DAC813 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. It is recommended that both Analog Common (ACOM, Pin 5) and Digital Common (DCOM, Pin 10) be connected directly to a ground plane under the package. If a ground plane is not used, connect the ACOM and DCOM pins together close to the package. Since the reference point for V_{OUT} and $V_{REF\,OUT}$ is the ACOM pin, it is also important to connect the load directly to the ACOM pin. Refer to Figure 5.

The change in current in the Analog Common pin (ACOM, Pin 5) due to an input data word change from 000_{HEX} to FFF_{HEX} is only 800µA.

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the DAC813 may be connected to produce bipolar output voltage ranges of ±10V and ±5V or unipolar output voltage range of 0 to +10V. Refer to Figure 6.



* Connecting unused resistors to ground will increase the wideband output noise by about 50%, while sharply reducing the possibility of digital noise pick-up by the sensitive summing mode.

FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

The internal feedback resistors (25kΩ) and the bipolar offset resistor (24.9kΩ) are trimmed to an absolute tolerance of less than ±2%. Therefore, one can change the range by adding a series resistor in various feedback circuit configurations. For example, a 600Ω resistor in series with the 20V range terminal can be used to obtain a 20.48V (±10.24V) range (5mV LSB). A 7.98kΩ resistor in series with the 10V range connection (20V ranges in parallel) gives a 16.384V (±8.192V) bipolar range (4mV LSB). Gain drift will be affected by the mismatch of the temperature coefficient of the external resistor with the internal D/A. Therefore the resistor should be used in the circuit arrangement that minimizes its contribution to gain drift.

APPLICATIONS

MICROCOMPUTER BUS INTERFACING

The DAC813 interface logic allows easy interface to microcomputer bus structures. The control signal is derived from external device select logic and the I/O Write or Memory Write (depending upon the system design) signals from the microcomputer.

The latch enable lines $\overline{LMSB}$, $\overline{LLSB}$, and $\overline{LDAC}$ determine which of the latches are selected. It is permissible to enable two or more latches simultaneously, as shown in some of the following examples.

The double-buffered latch permits data to be loaded into the input latches of several DAC813s and later strobed into the D/A latch of all D/As, simultaneously updating all analog outputs. All the interface schemes shown below use a base address decoder. If blocks of memory are used, the base address decoder can be simplified or eliminated altogether.

8-BIT INTERFACE

The control logic of DAC813 permits interfacing to right-justified data formats, illustrated in Figure 7. When a 12-bit D/A converter is loaded from an 8-bit bus, two bytes of data are required. Figure 8 illustrates an addressing scheme for right-justified data. The base address is decoded from the high-order address bits. A0 and A1 address the appropriate latches. Note that adjacent addresses are used. $X10_{HEX}$ loads the 8 LSBs and $X01_{HEX}$ loads the 4 MSBs and simultaneously transfers input latch data to the D/A latch. Addresses $X00_{HEX}$ and $X11_{HEX}$ are not used.

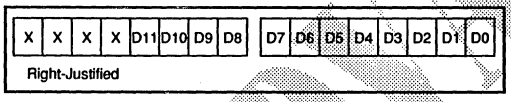


FIGURE 7. 12-Bit Data Format for 8-Bit Systems.

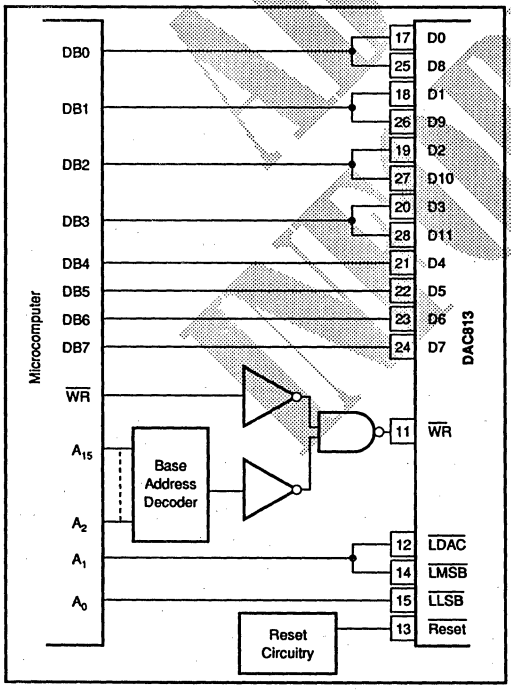


FIGURE 8. Right-Justified Data Bus Interface.

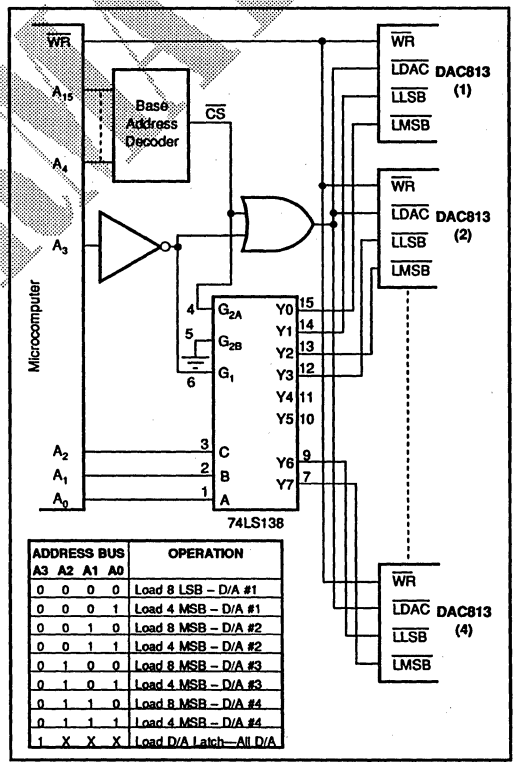
INTERFACING MULTIPLE DAC813s IN 8-BIT SYSTEMS

Many applications, such as automatic test systems, require that the outputs of several D/A converters be updated simultaneously. The interface shown in Figure 9 uses a 74LSB138 decoder to decode a set of eight adjacent addresses to load the input latches of four DAC813s. The example uses a right-justified data format.

A ninth address using A3 causes all DAC813s to be updated simultaneously. If a certain DAC813 is always loaded last (for instance, D/A #4), A3 is not needed, saving 8 address spaces for other uses. Incorporate A3 into the base address decoder, remove the inverter, connect the common $\overline{LDAC}$ line to $\overline{LLSB}$ of D/A #4, and connect D1 of the 74LS138 to +5V.

12- AND 16-BIT MICROCOMPUTER INTERFACE

For this application the input latch enable lines, $\overline{LMSB}$ and $\overline{LLSB}$, are tied low, causing the latches to be transparent. The D/A latch, and therefore DAC813, is selected by the address decoder and strobed by $\overline{WR}$.



ADDRESS BUS A3	A2	A1	A0	OPERATION
0	0	0	0	Load 8 LSB – D/A #1
0	0	0	1	Load 4 MSB – D/A #1
0	0	1	0	Load 8 MSB – D/A #2
0	0	1	1	Load 4 MSB – D/A #2
0	1	0	0	Load 8 MSB – D/A #3
0	1	0	1	Load 4 MSB – D/A #3
0	1	1	0	Load 8 MSB – D/A #4
0	1	1	1	Load 4 MSB – D/A #4
1	X	X	X	Load D/A Latch—All D/A

FIGURE 9. Interfacing Multiple DAC813s to an 8-Bit Bus.

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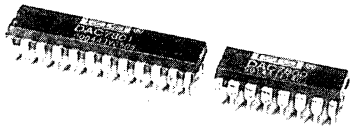


DAC7800
DAC7801

ADVANCE INFORMATION
SUBJECT TO CHANGE

Dual CMOS 12-Bit Multiplying DIGITAL-TO-ANALOG CONVERTERS

FEATURES

- SERIAL, 8-BIT (8+4)AND 12-BIT HIGH-SPEED INTERFACES
- SINGLE +5V SUPPLY
- GUARANTEED MONOTONIC OVER TEMPERATURE
- CHANNEL-TO-CHANNEL CROSSTALK: –94dB
- MULTIPLYING FEEDTHROUGH: –75dB
- 0.3IN. WIDE PLASTIC DIP PACKAGES

APPLICATIONS

- ATE PIN ELECTRONICS LEVEL SETTING
- PROGRAMMABLE FILTERS
- PROGRAMMABLE GAIN AMPLIFIERS
- PROCESS CONTROL OUTPUTS

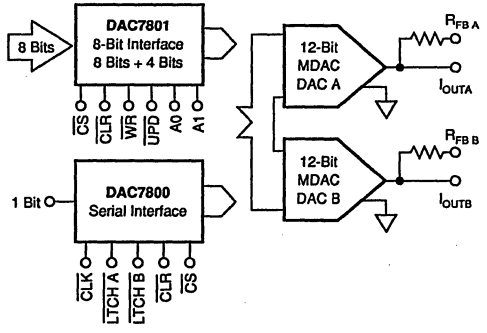
DESCRIPTION

The DAC7800 and DAC7801 are members of a new family of monolithic dual 12-bit CMOS multiplying digital-to-analog converters. DAC7802, with a 12-bit data port, is the other member of the family and has a complete data sheet, PDS-1038.

DAC7800 features a high-speed serial interface capable of clocking in data at a rate of 10MHz. Serial data is clocked MSB first into a 24-bit shift register and then strobed into each D/A separately or simultaneously as required. DAC7800 has an asynchronous CLEAR control useful for power-on-reset or system calibration conditions. It is packaged in a 16-pin 0.3in. wide plastic DIP.

DAC7801 has a 2-byte (8-bit + 4-bit) digital interface. Data is loaded into the interface logic in two steps for each D/A. Then both D/As are updated simultaneously. DAC7801 also features an asynchronous CLEAR control. DAC7801 is packaged in a 24-pin, 0.3in. wide plastic DIP.

These D/A converters have high speed digital interfaces, excellent AC multiplying performance and low power dissipation. High-stability thin film ladder resistors provide true 12-bit integral and differential linearity over the –40°C to +85°C temperature range.



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PDS-1079

SPECIFICATIONS

ELECTRICAL

At V_{DD} = +5VDC, V_{REFA} = V_{REFB} = 10V and T_A = –40°C to +85°C unless otherwise noted.

PARAMETER	CONDITIONS	DAC7800/7801KP MIN	DAC7800/7801KP TYP	DAC7800/7801KP MAX	DAC7800/7801LP MIN	DAC7800/7801LP TYP	DAC7800/7801LP MAX	UNITS
ACCURACY								
Resolution		12			*			Bits
Relative Accuracy				±1			±1/2	LSB
Differential Nonlinearity				±1			*	LSB
Gain Error	Measured Using R_{FBA} and R_{FBB}. All Registers Loaded with All 1s.			±3			±1	LSB
Gain Temperature Coefficient[1]			2	5		*	*	ppm/°C
Output Leakage Current	T_A = +25°C		0.005	10		*	*	nA
	T_A = –40°C to +85°C		3	150		*	*	nA
REFERENCE INPUT								
Input Resistance		6	10	14	*	*	*	kΩ
Input Resistance Match			0.5	3		*	2	%
DIGITAL INPUTS								
V_{IH} (Input High Voltage)		2			*			V
V_{IL} (Input Low Voltage)				0.8			*	V
I_{IN} (Input Current)	T_A = +25°C			±1			*	µA
	T_A = –40°C to +85°C			±10			*	µA
C_{IN} (Input Capacitance)			0.8	10		*	*	pF
POWER SUPPLY								
V_{DD}		4.5		5.5	*		*	V
I_{DD}			0.2	2		*	*	mA
Power Supply Rejection	V_{DD} from 4.5V to 5.5V			0.002			*	%/%

* Same specifications as for DAC7800/7801KP.

AC PERFORMANCE

OUTPUT OP AMP IS OPA602 UNLESS OTHERWISE STATED.

At V_{DD} = +5VDC, V_{REFA} = V_{REFB} = 10V and T_A = 25°C unless otherwise noted. These specifications are fully characterized but not subject to test.

PARAMETER	CONDITIONS	DAC7800/7801KP MIN	DAC7800/7801KP TYP	DAC7800/7801KP MAX	DAC7800/7801LP MIN	DAC7800/7801LP TYP	DAC7800/7801LP MAX	UNITS
OUTPUT CURRENT SETTLING TIME	To 0.01% of Full Scale R_L = 100Ω, C_L = 13pF		0.4	0.8		*	*	µs
DIGITAL-TO-ANALOG GLITCH IMPULSE	V_{REFA} = V_{REFB} = 0V R_L = 100Ω, C_L = 13pF		0.9			*		nV/s
AC FEEDTHROUGH	f_{VREF} = 10kHz		–75	–72		*	*	dB
OUTPUT CAPACITANCE	DAC Loaded with All 0s		30	50		*	*	pF
	DAC Loaded with All 1s		70	100		*	*	pF
CHANNEL-TO-CHANNEL ISOLATION								
V_{REFA} to I_{OUTB}	f_{VREFA} = 10kHz V_{REFB} = 0V, Both DACs Loaded with 1s	–90	–94		*	*		dB
V_{REFB} to I_{OUTA}	f_{VREFB} = 10kHz V_{REFA} = 0V, Both DACs Loaded with 1s	–90	–101		*	*		dB
DIGITAL CROSSTALK	Full Scale Transition R_L = 100Ω, C_L = 13pF		0.9			*		nV/s

NOTES: (1) Guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS

At T_A = +25°C unless otherwise noted.

V_{DD} to AGND	0V, +7V
V_{DD} to DGND	0V, +7V
AGND to DGND	–0.3, V_{DD}
Digital Input to DGND	–0.3, V_{DD} + 0.3
V_{REFA}, V_{REFB} to AGND	±25V
V_{REFA}, V_{REFB} to DGND	±25V
I_{OUTA}, I_{OUTB} to AGND	–0.3, V_{DD}
Storage Temperature Range	–55°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+175°C

BURR-BROWN®

DAC7802

Dual CMOS 12-Bit Multiplying DIGITAL-TO-ANALOG CONVERTER

FEATURES

- TWO DACS IN A 0.3" WIDE PACKAGE
- HIGH SPEED DIGITAL INTERFACE
- SINGLE +5V SUPPLY
- LOW CROSSTALK: –90DB MIN
- FULLY SPECIFIED OVER –40°C TO +85°C
- FOUR-QUADRANT MULTIPLICATION
- MONOTONICITY GUARANTEED

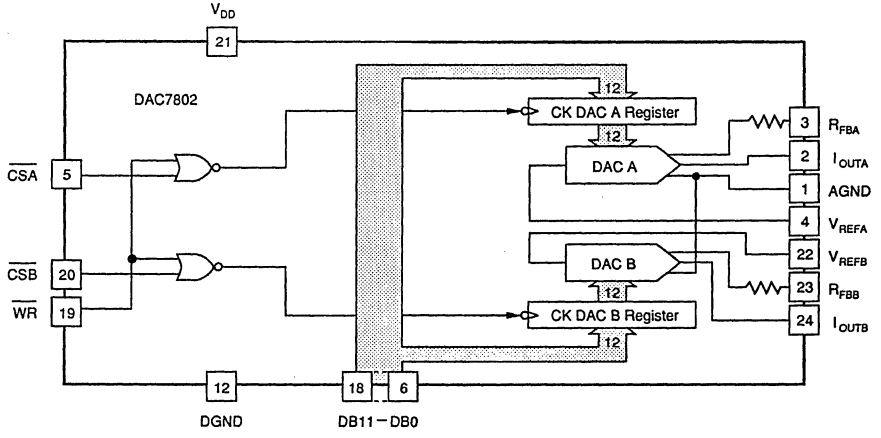
APPLICATIONS

- PROGRAMMABLE INSTRUMENTATION
- INDUSTRIAL AUTOMATION
- AUTOMATIC TEST EQUIPMENT
- PROCESS CONTROL
- PROGRAMMABLE FILTERS

DESCRIPTION

The DAC7802 is a dual CMOS, 12-bit four-quadrant multiplying digital-to-analog converter with high speed data latches. Data is loaded into the DAC as a 12-bit data word. The $\overline{CSA}$ and $\overline{CSB}$ lines control the selection of the data latches. The data is then latched on the rising edge of $\overline{WR}$. The high speed digital interface operates at 2–6 times the speed of similar CMOS DACs.

The digital interface speed and excellent AC multiplying performance is achieved by using an advanced CMOS process, optimized for analog and data conversion circuits. High stability resistors provide true 12-bit integral and differential linearity over the industrial temperature range.



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PDS-1038A

SPECIFICATIONS

ELECTRICAL

At V_{DD} = +5VDC, $V_{REFA} = V_{REFB}$ = 10V and T_A = –40°C to +85°C unless otherwise noted.

PARAMETER	CONDITIONS	DAC7802KP MIN	DAC7802KP TYP	DAC7802KP MAX	DAC7802LP MIN	DAC7802LP TYP	DAC7802LP MAX	UNITS
ACCURACY								
Resolution		12			*			Bits
Relative Accuracy				±1			±1/2	LSB
Differential Nonlinearity				±1			*	LSB
Gain Error	Measured Using R_{FBA} and R_{FBB}. All Registers Loaded with All 1s.			3			1	LSB
Gain Temperature Coefficient (1)			2	5		*	*	ppm/°C
Output Leakage Current	T_A = +25°C.		0.005	10		*	*	nA
	T_A = –40°C to +85°C.		3	150		*	*	nA
REFERENCE INPUT								
Input Resistance		6.0	10	14	*	*	*	kΩ
Input Resistance Match			0.5	3		*	2	%
DIGITAL INPUTS								
V_{IH} (Input High Voltage)		2.0			*			V
V_{IL} (Input Low Voltage)				0.8			*	V
I_{IN} (Input Current)	T_A = +25°C.			±1			*	µA
	T_A = –40°C to +85°C.			±10			*	µA
C_{IN} (Input Capacitance)			0.8	10		*	*	pF
POWER SUPPLY								
V_{DD}		4.5		5.5	*		*	V
I_{DD}			0.2	2		*	*	mA
Power Supply Rejection	V_{DD} from 4.5V to 5.5V.			0.002			*	%/%

* Same specifications as for DAC7802KP.

AC PERFORMANCE

OUTPUT OP-AMP IS OPA602 UNLESS OTHERWISE STATED.

At V_{DD} = +5VDC, $V_{REFA} = V_{REFB}$ = 10V and T_A = 25°C unless otherwise noted. These specifications are fully characterized but not subject to test.

PARAMETER	CONDITIONS	DAC7802KP MIN	DAC7802KP TYP	DAC7802KP MAX	DAC7802LP MIN	DAC7802LP TYP	DAC7802LP MAX	UNITS
OUTPUT CURRENT SETTLING TIME	To 0.01% of Full Scale. R_L = 100Ω, C_L = 13pF.		0.4	0.8		*	*	µs
DIGITAL-TO-ANALOG GLITCH IMPULSE	$V_{REFA} = V_{REFB}$ = 0V. R_L = 100Ω, C_L = 13pF.		0.9			*		nVs
AC FEEDTHROUGH	f_{VREF} = 10kHz.		–75	–72		*	*	dB
OUTPUT CAPACITANCE	DAC Loaded with All 0s.		30	50		*	*	pF
	DAC Loaded with All 1s.		70	100		*	*	pF
CHANNEL-TO-CHANNEL ISOLATION								
V_{REFA} to I_{OUTB}	f_{VREFA} = 10kHz. V_{REFB} = 0V, Both DACs Loaded with 1s.	–90	–94		*	*		dB
V_{REFB} to I_{OUTA}	f_{VREFB} = 10kHz. V_{REFA} = 0V, Both DACs Loaded with 1s.	–90	–101		*	*		dB
DIGITAL CROSSTALK	Full Scale Transition. R_L = 100Ω, C_L = 13pF.		0.9			*		nVs

NOTES: (1) Guaranteed but not tested.

ORDERING INFORMATION

MODEL	RELATIVE ACCURACY	GAIN ERROR
DAC7802KP	±1 LSB	3 LSB
DAC7802LP	±1/2 LSB	1 LSB

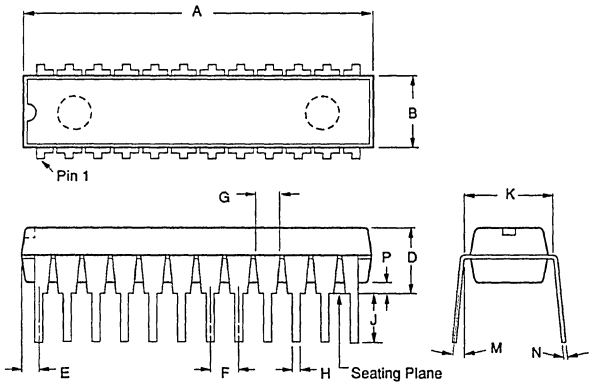
ABSOLUTE MAXIMUM RATINGS

At T_A = +25°C, unless otherwise noted.

V_{DD} to AGND	0V, +7V
V_{DD} to DGND	0V, +7V
AGND to DGND	–0.3, V_{DD}
Digital Input to DGND	–0.3, V_{DD} + 0.3
V_{REFA}, V_{REFB} to AGND	±25V
V_{REFA}, V_{REFB} to DGND	±25V
I_{OUTA}, I_{OUTB} to AGND	–0.3, V_{DD}
Storage Temperature Range	–55°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature, soldering 10s	+300°C
Junction Temperature	+175°C

MECHANICAL

P Package — 24-Pin Plastic DIP



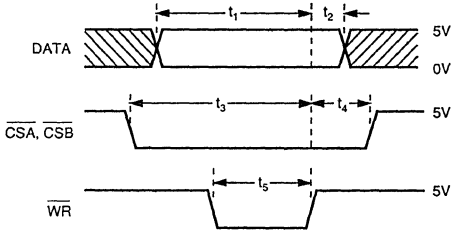
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.125	1.255	28.58	31.88
B	.250	.290	6.35	7.37
D	.150	.170	3.81	4.32
E	.010	.080	.25	2.03
F	.100 BASIC		2.54 BASIC	
G	.050	.070	1.27	1.78
H	.016	.025	0.41	0.64
J	.125		3.18	
K	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.008	.015	0.20	0.38
P	.010	.030	.25	.76

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

TIMING CHARACTERISTICS

At V_{DD} = +5V, and T_A = –40°C to +85°C.

PARAMETER	MINIMUM
t_1 - Data Setup Time	20ns
t_2 - Data Hold Time	15ns
t_3 - Chip Select to Write Setup Time	30ns
t_4 - Chip Select to Write Hold Time	0ns
t_5 - Write Pulse Width	30ns



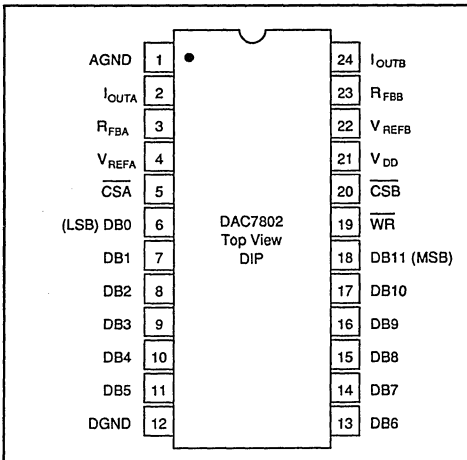
NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. $t_R = t_F$ = 5ns. (2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	FUNCTION
X	X	1	No Data Transfer
1	1	X	No Data Transfer
↓	↓	0	A Rising Edge on $\overline{CSA}$ or $\overline{CSB}$ Loads Data to the Respective DAC
0	1	↓	DAC A Register Loaded from Data Bus
1	0	↓	DAC B Register Loaded from Data Bus
0	0	↓	DAC A from DAC B Registers Loaded from Data Bus

X = Don't care. ↓ means rising edge triggered.

TABLE I. Logic Truth Table.

CONNECTION DIAGRAM



DATA INPUT	ANALOG OUTPUT
MSB ↓ ↓ LSB	
1111 1111 1111	$-V_{REF}$ (4095/4096)
1000 0000 0000	$-V_{REF}$ (2048/4096) = $-1/2V_{REF}$
0000 0000 0001	$-V_{REF}$ (1/4096)
0000 0000 0000	0 Volts

TABLE II. Unipolar Output Code.

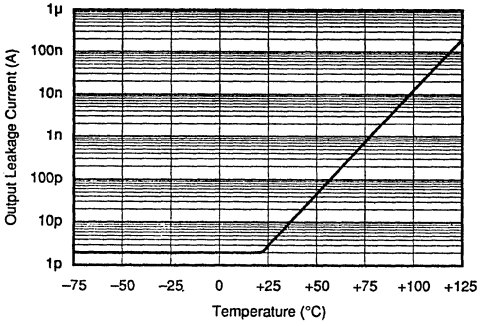
DATA INPUT	ANALOG OUTPUT
MSB ↓ ↓ LSB	
1111 1111 1111	$+V_{REF}$ (2047/2048)
1000 0000 0001	$+V_{REF}$ (1/2048)
1000 0000 0000	0 Volts
0111 1111 1111	$-V_{REF}$ (1/2048)
0000 0000 0000	$-V_{REF}$ (2048/2048)

TABLE III. Bipolar Output Code.

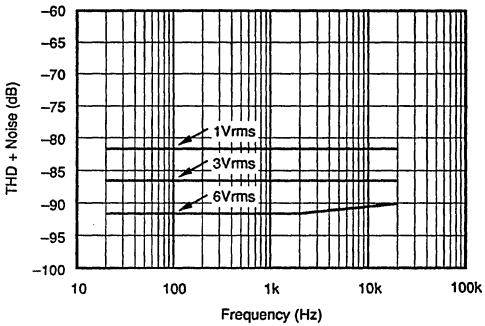
TYPICAL PERFORMANCE CURVES

OUTPUT OP-AMP IS OPA602 UNLESS OTHERWISE STATED.
T_A = +25°C, V_{DD} = +5V unless otherwise noted.

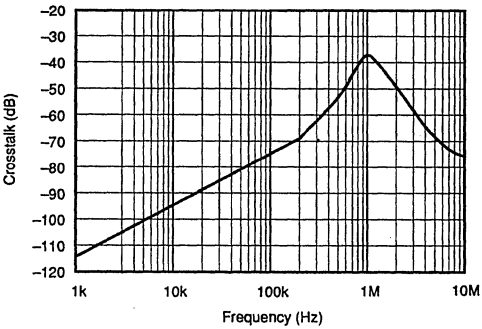
OUTPUT LEAKAGE CURRENT vs TEMPERATURE



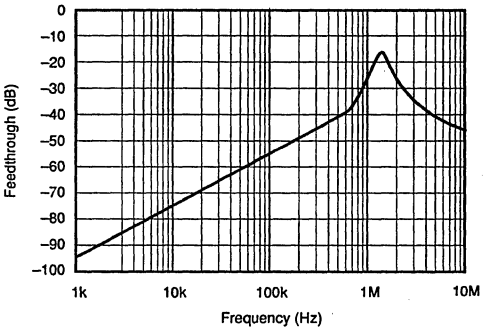
THD + NOISE vs FREQUENCY



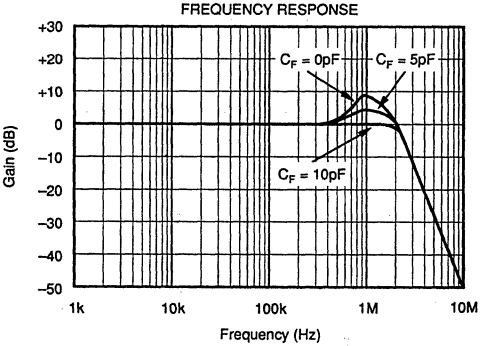
CHANNEL-TO-CHANNEL ISOLATION vs FREQUENCY



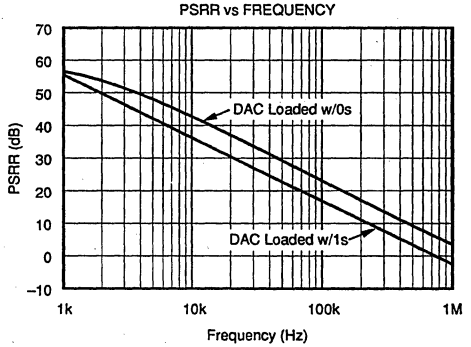
FEEDTHROUGH vs FREQUENCY



FREQUENCY RESPONSE



PSRR vs FREQUENCY



DISCUSSION OF SPECIFICATIONS

RELATIVE ACCURACY

This term, also known as end point linearity or integral linearity, describes the transfer function of analog output to digital input code. Relative accuracy describes the deviation from a straight line after zero and full scale errors have been removed.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1 LSB change in the output when the input code changes by 1 LSB. A differential nonlinearity specification of 1 LSB maximum guarantees monotonicity.

GAIN ERROR

Gain error is the difference between the full-scale DAC output and the ideal value. The ideal full scale output value for the DAC7802 is $-(4095/4096)V_{REF}$. Gain error may be adjusted to zero using external trims as shown in Figures 3 and 5.

OUTPUT LEAKAGE CURRENT

The current which appears at $I_{OUT\,A}$ ahd $I_{OUT\,B}$ with the DAC loaded with all zeros.

OUTPUT CAPACITANCE

This is the parasitic capacitance measured from $I_{OUT\,A}$ or $I_{OUT\,B}$ to AGND.

CHANNEL-TO-CHANNEL ISOLATION

The AC output error due to capacitive coupling from DACA to DACB or DACB to DACA.

MULTIPLYING FEEDTHROUGH ERROR

The AC output error due to capacitive coupling from V_{REF} to I_{OUT} with the DAC loaded with all zeros.

OUTPUT CURRENT SETTLING TIME

The time required for the output current to settle to within ±0.01% of final value for a full scale step.

DIGITAL-TO-ANALOG GLITCH ENERGY

The integrated area of the glitch pulse measured in nanovolt-seconds. The key contributor to digital-to-analog glitch is charge injected by digital logic switching transients.

DIGITAL CROSSTALK

Glitch impulse measured at the output of one DAC but caused by a full scale transition on the other DAC. The integrated area of the glitch pulse is measured in nanovolt-seconds.

CIRCUIT DESCRIPTION

Figure 1 shows a simplified schematic of one half of a DAC7802. The current from the $V_{REF\,A}$ pin is switched between $I_{OUT\,A}$ and AGND by the CMOS FET switch for that bit. This circuit architecture keeps the resistance at the $V_{REF\,A}$ pin constant so the reference could be provided by either a voltage or current, AC or DC, positive or negative polarity, and have a voltage range up to ±20V.

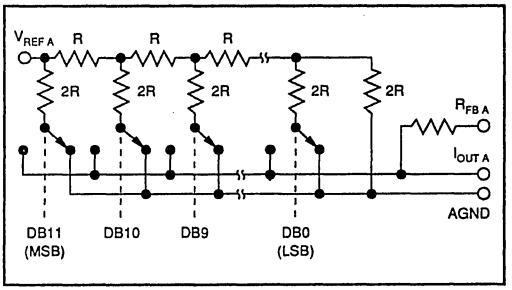


FIGURE 1. Simplified DAC Circuit.

APPLICATIONS

POWER SUPPLY CONNECTIONS

The DAC7802 is designed to operate on V_{DD} = +5V ±10%. For optimum performance and noise rejection, power supply decoupling capacitors C_D should be added as shown in the application circuits. These capacitors (1µF tantalum recommended) should be located close to the DAC7802. AGND and DGND should be connected together at one point only, preferably at the power supply ground point. Separate returns minimize current flow in low level signal paths if properly connected. Output op-amp analog ground should be tied as near to the AGND pin of the DAC7802 as possible.

WIRING PRECAUTIONS

To minimize the AC feedthrough when designing a PC board for the DAC7802, great care should be taken to minimize capacitive coupling between the V_{REF} lines and the I_{OUT} lines. Similarly, capacitive coupling between DACs may compromise the channel-to-channel isolation. Coupling from any of the digital control or data lines might degrade the glitch and digital crosstalk performance. Whenever possible, solder the DAC7802 directly into the PC board without a socket. Sockets add parasitic capacitance (which can degrade AC performance as described) and resistance (which may impact the DC accuracy).

AMPLIFIER OFFSET VOLTAGE

As with all precision CMOS MDACs, the output amplifier used with the DAC7802 should have low input offset voltage to preserve the transfer function linearity. The voltage output of the amplifier has an error component which is the offset voltage of the op-amp multiplied by the "noise gain" of the circuit. This "noise gain" is equal to $(R_F/R_O + 1)$ where R_O is the output impedance of the DAC I_{OUT} terminal and R_F is the feedback network impedance. The non-linearity arises from the output impedance of CMOS multiplying DACs varying with code. If the 0 code case is excluded (where R_O = infinity), the R_O will vary from R to 3R providing a "noise gain" variation between 4/3 to 2. In addition, the variation of R_O is non-linear with code, and the largest steps in R_O occur at major code transitions where the worst DAC differential non-linearity is also likely to be experienced. The non-linearity seen at the amplifier output is $2V_{OS} - 4V_{OS}/3 = 2V_{OS}/3$. Thus, to maintain good non-linearity the op-amp offset should be much less than 1/2LSB.

ESD PROTECTION

All digital inputs of the DAC7802 incorporate on-chip ESD protection circuitry. This protection is designed to withstand 2.5kV (using the Human Body Model; 100pF and 1500Ω). However, industry standard ESD protection methods should be used when handling or storing these components. When not in use, devices should be stored in conductive foam or rails. The foam or rails should be discharged to the destination socket potential before devices are removed.

RELIABILITY DATA

Extensive reliability testing has been performed on the DAC7802. Accelerated life testing (1008 hours) at 125°C was used to calculate MTTF at an ambient temperature of 25°C and 85°C. These test results yield MTTF of 2.5E+7 hours at 25°C and 2.6E+5 hours at 85°C. Additional tests such as PCT have also been performed. Reliability reports are available upon request.

UNIPOLAR CONFIGURATION

Figure 2 shows the DAC7802 in a typical unipolar (two-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table II. The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, or a dual amplifier such as the OPA2107. C1 and C2 provide phase compensation to minimize settling time and overshoot when using a high speed operational amplifier.

If an application requires the DAC to have zero gain error, the circuit shown in Figure 3 may be used. Resistors R2, and R4 induce a positive gain error greater than worst case initial negative gain error for a DAC7802KP. Trim resistors R1 and R3 provide a variable negative gain error and have sufficient trim range to correct for the worst case initial positive gain error plus the error produced by R2 and R4.

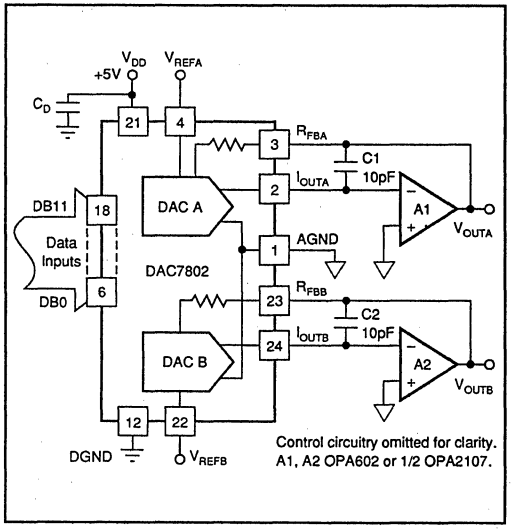


FIGURE 2. Unipolar Configuration.

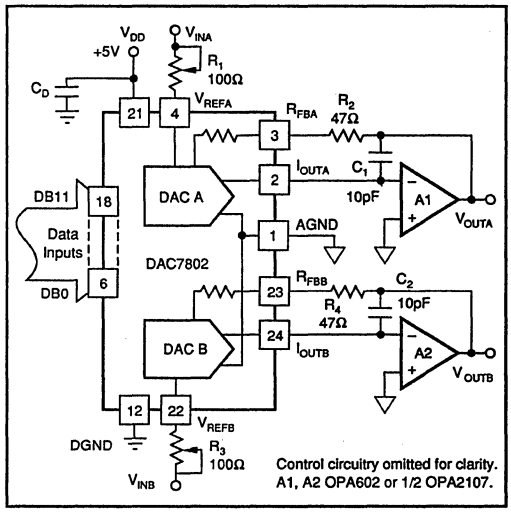


FIGURE 3. Unipolar Configuration with Gain Trim.

BIPOLAR CONFIGURATION

Figure 4 shows the DAC7802 in a typical bipolar (four-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table III.

The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, a dual amplifier such as the OPA2107, or a quad amplifier like the OPA404. C1 and C2 provide phase compensation to minimize settling time and overshoot when using a high speed operational amplifier. The bipolar offset resistors R5–R7 and R8–R10 should be ratio-matched to 0.01% to ensure the specified gain error performance.

If an application requires the DAC to have zero gain error, the circuit shown in Figure 5 may be used. Resistors R2 and R4 induce a positive gain error greater than worst case initial negative gain error for a DAC7802KP. Trim resistors R1 and R3 provide a variable negative gain error and have sufficient trim range to correct for the worst case initial positive gain error plus the error produced by R2 and R4.

12-BIT PLUS SIGN DACS

For a bipolar DAC with 13 bits of resolution, two solutions are possible. As shown in Figure 6, the addition of a precision difference amplifier and a high speed JFET switch provides a 12-bit plus sign voltage-output DAC. When the switch selects the op-amp output, the difference amplifier serves as a non-inverting output buffer. If the analog ground side of the switch is selected, the output of the difference amplifier is inverted.

Another option, shown in Figure 7, also produces a 12-bit plus sign output without the additional switch and digital control line.

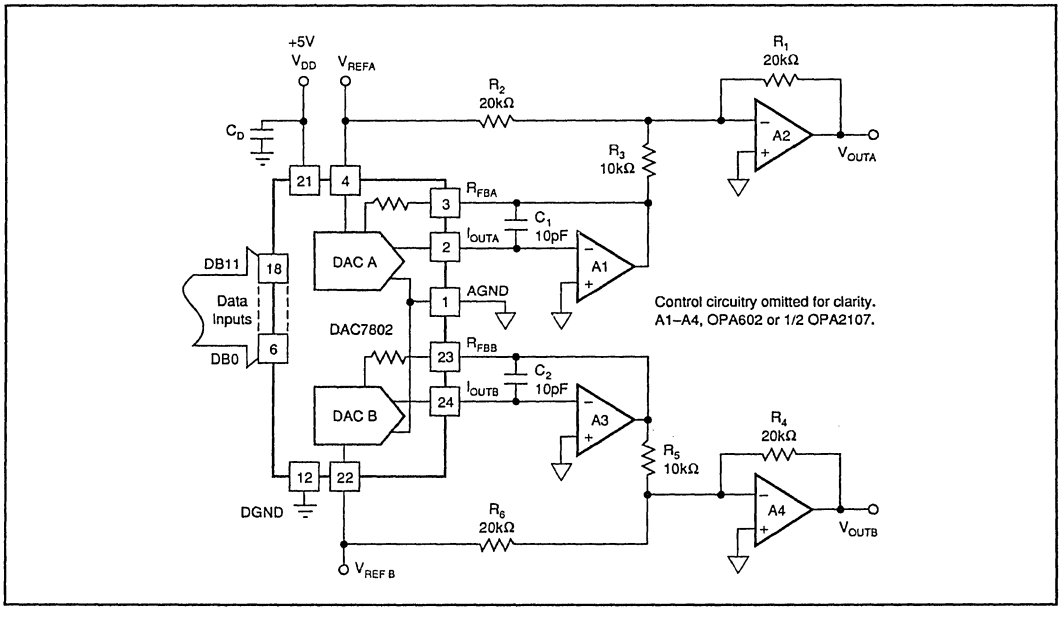


FIGURE 4. Bipolar Configuration.

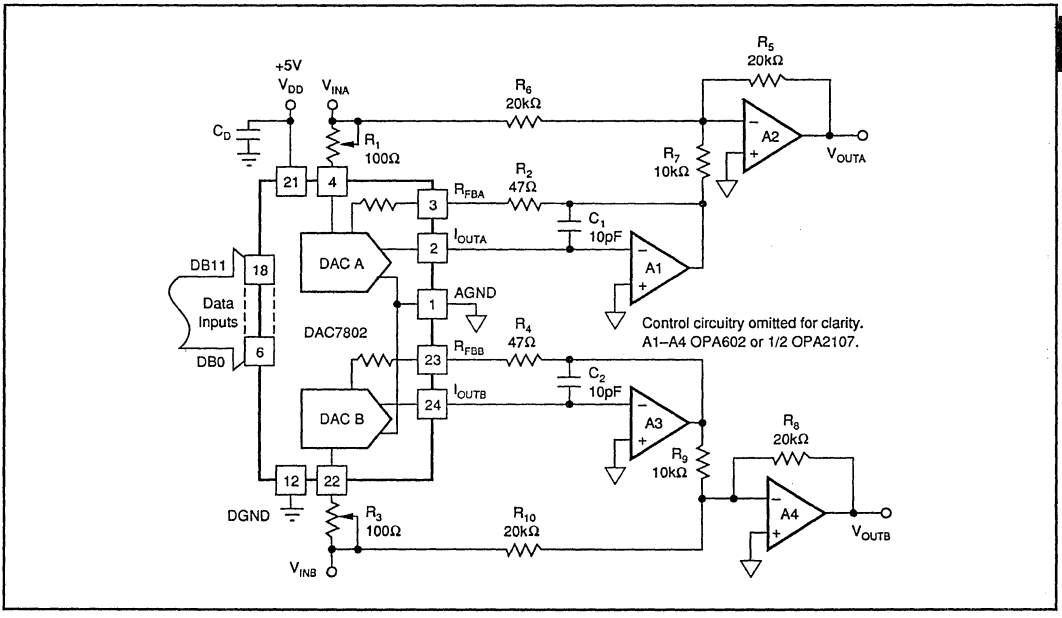


FIGURE 5. Bipolar Configuration with Gain Trim.

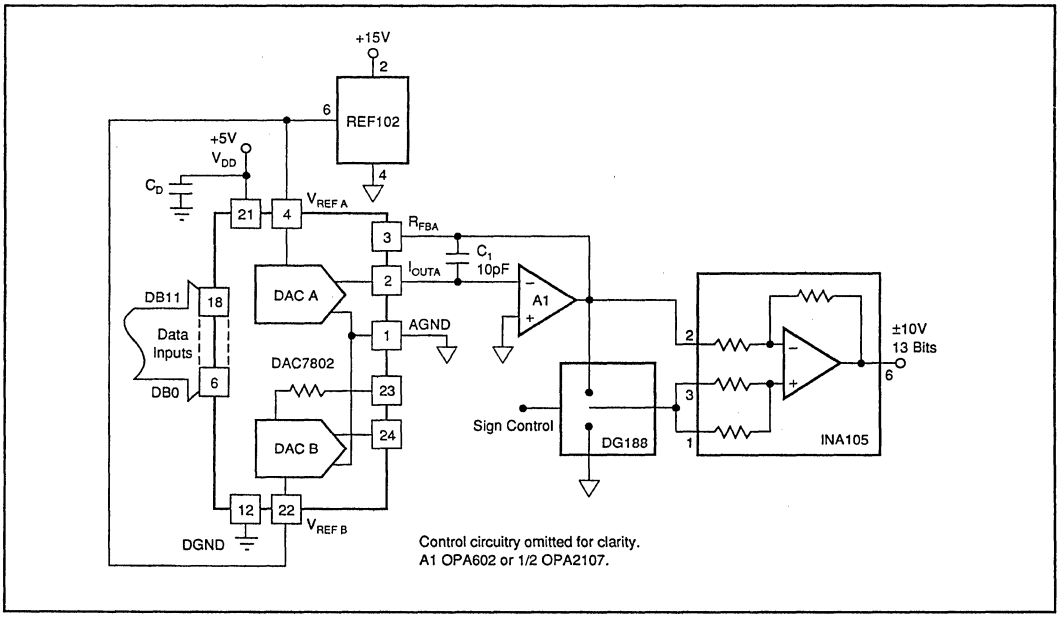


FIGURE 6. 12-Bit Plus Sign DAC.

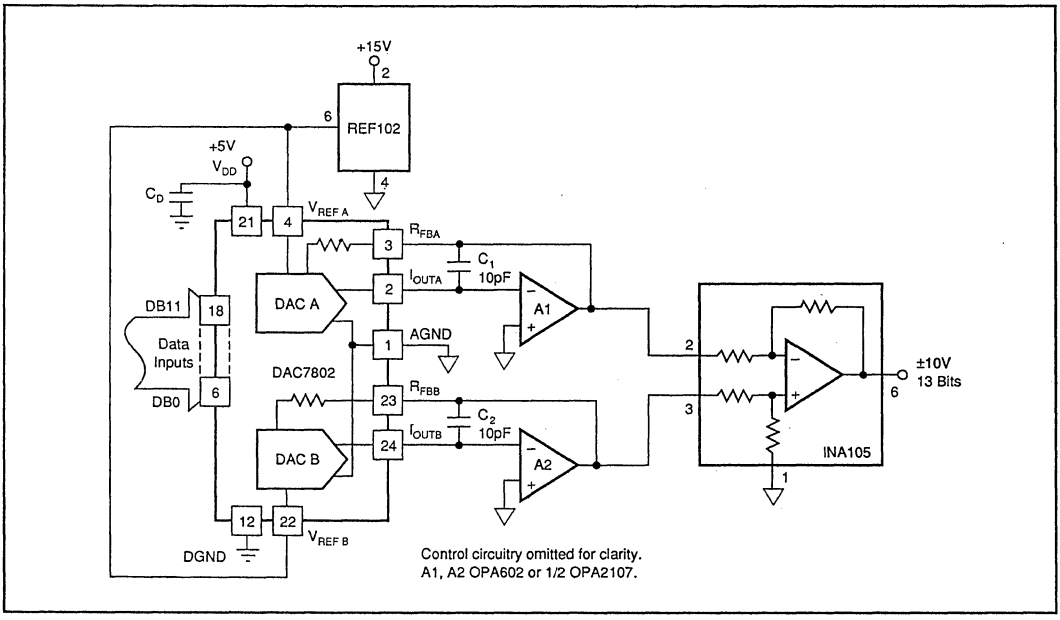
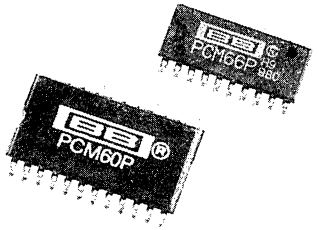


FIGURE 7. 13-Bit Bipolar DAC.

BURR-BROWN®



PCM60P
PCM66P

16-Bit CMOS Monolithic Audio DIGITAL-TO-ANALOG CONVERTER

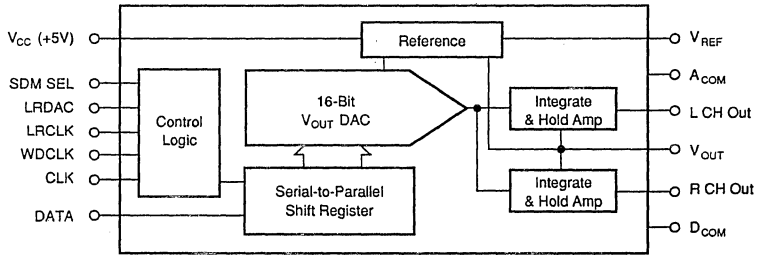
FEATURES

- LOW COST 16-BIT 2-CHANNEL CMOS MONOLITHIC D/A CONVERTER
- SINGLE SUPPLY +5V OPERATION
- 50mW POWER DISSIPATION
- GLITCH-FREE VOLTAGE OUTPUTS
- LOW DISTORTION: –86dB max THD + N
- COMPLETE WITH REFERENCE
- SERIAL INPUT FORMAT
- SINGLE OR DUAL DAC MODE OPERATION
- PLASTIC 20-PIN SOIC PACKAGE (PCM66P)
- PLASTIC 24-PIN SOIC PACKAGE (PCM60P)

DESCRIPTION

The PCM60P/66P is a low cost, dual output 16-bit CMOS digital-to-analog converter. The PCM60P/66P features true glitch-free voltage outputs and requires only a single +5V supply. The PCM60P/66P doesn't require an external reference. Total power dissipation is less than 50mW max. Low maximum Total Harmonic Distortion + Noise (–86dB max; PCM60P-J, PCM66P-J) is 100% tested. Either one or two channel output modes are fully user selectable.

The PCM60P/66P comes in a space-saving 24-pin plastic SOIC package. PCM60P/66P accepts a serial data input format and is compatible with other Burr-Brown PCM products such as the industry standard PCM56P.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1051A

SPECIFICATIONS

ELECTRICAL

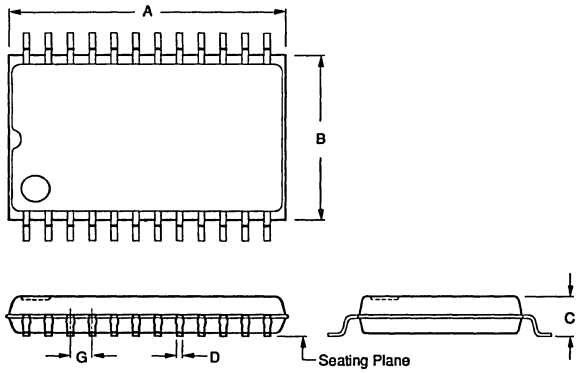
All specifications at 25°C, and $+V_{CC}$ = +5V unless otherwise noted.

PARAMETER	CONDITIONS	PCM60P/66P AND PCM60P-J/66P-J MIN	TYP	MAX	UNITS
RESOLUTION				16	Bits
DYNAMIC RANGE			96		dB
INPUT					
DIGITAL INPUT			TTL Compatible CMOS		
Logic Family					
Logic Level: V_{IH}	I_{IH} = +40µA max	+2.4		+5.25	V
V_{IL}	I_{IL} = –40µA max	0		0.8	V
Data Format			Serial BTC[1]		
Input Clock Frequency		8.5			MHz
DYNAMIC CHARACTERISTICS					
TOTAL HARMONIC DISTORTION + N[2]					
PCM60P/66P: f = 991Hz (0dB)[3]	f_S = 176.4kHz[4]		–88	–82	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–68		dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–28		dB
PCM60P-J/66P-J: f = 991Hz (0dB)	f_S = 176.4kHz		–92	–86	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–68		dB
f = 99lHz (–60db)	f_S = 176.4kHz		–28		dB
CHANNEL SEPARATION		+80	+85		dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error	V_{OUT} = 2.8Vp-p		±2	±10	%
Gain Mismatch	Channel to Channel		±1		%
Bipolar Zero Error[5]			±30		mV
Gain Drift	0°C to 70°C		100		ppm/°C
Warm-up Time		1			minute
IDLE CHANNEL SNR[6]	20-20kHz with A-weighted filter		±90		dB
OUTPUT					
ANALOG OUTPUT					
Output Range			2.8		Vp-p
Output Impedance			2		Ω
Short Circuit Duration	To Be Determined				
Settling Time	Suffieicnt to Meet 176.4kHz THD + N Specs				
Glitch Energy	Meets All THD + N Specs Without External Output Deglitching				
POWER SUPPLY REQUIREMENTS					
$+V_{CC}$ Supply Voltage		+4.75	+5	+5.25	V
Supply Current			+9.5		mA
Power Dissipation	V_{CC} = +5V			50	mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–30		+70	°C
Storage		–60		+100	°C

NOTE: 1) Binary Two's Complement coding. (2) Ratio of (Distortion$_{RMS}$ + Noise$_{RMS}$) / Signal$_{RMS}$. (3) D/A converter output frequency/signal level (on both left and right channels). (4) D/A converter sample frequency (4 x 44.1kHz; 4 times oversampling per channel). (5) Offset error at bipolar zero. (6) Ratio of output at BPZ (Bipolar Zero) to the full scale range using 20kHz low pass filter in addition to an A-weighted filter.

MECHANICAL

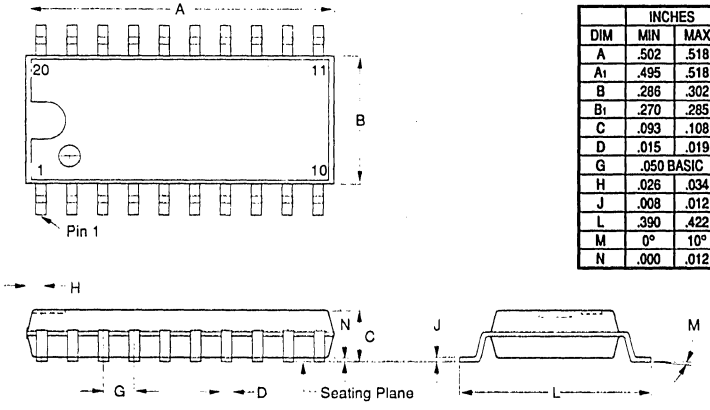
P Package — 24-Pin SOIC
PCM60P



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.614	.630	15.60	16.00
A1	.610	TYP	15.5	TYP
B	.328	.346	8.33	8.80
B1	.331	TYP	8.4	TYP
C	—	.098	—	2.50
D	.012	.020	0.30	0.50
G	.046	.054	1.17	1.37
H	.075	.115	1.91	2.92
J	.0039	.010	0.1	0.26
L	.453	.476	11.5	12.1
M	0°	TYP	0°	TYP
N	.0039		0.10	

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

P Package — 20-Pin Plastic SOIC
PCM66P



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.502	.518	12.75	13.16
A1	.495	.518	12.57	13.16
B	.286	.302	7.26	7.67
B1	.270	.285	6.86	7.24
C	.093	.108	2.36	2.74
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.026	.034	0.66	0.86
J	.008	.012	0.20	0.30
L	.390	.422	9.91	10.72
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	±10V
Input Voltage Range	–3V to +5.25V
Power Dissipation	50mW
Operating Temperature	–30°C to +70°C
Storage Temperature	–60°C to +100°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

PCM60P/PCM66P -X

Basic Model Number
P: Plastic
Performance Grade Code

PCM60P PIN ASSIGNMENTS

PIN	DESCRIPTION	MNEMONIC
1	Left/Right Clock	LRCLK
2	Word Clock	WDCLK
3	Clock Input	CLK
4	Data Input	DATA
5	No Connection	NC
6	No Connection	NC
7	Digital Common	D_{COM}
8	Analog Common	A_{COM}
9	No Connection	NC
10	Left Channel V_{OUT}	L CH Out
11	Output Common	V_{COM}
12	Right Channel V_{out}	R CH Out
13	$+V_{CC}$ Analog Supply	$+V_{CC}$
14	$+V_{CC}$ Analog Supply	$+V_{CC}$
15	Reference Decouple	C_{REF}
16	No Connection	NC
17	V_{REF} Sense	V_{REF} SENSE
18	Voltage Reference	V_{REF}
19	$+V_{CC}$ Analog Supply	$+V_{CC}$
20	$+V_{CC}$ Analog Supply	$+V_{CC}$
21	$+V_{CC}$ Digital Supply	$+V_{CC}$
22	No Connection	NC
23	Single DAC Mode	SDM SEL
24	Left/Right DAC Select	LRDAC

PCM66P PIN ASSIGNMENTS

PIN	DESCRIPTION	MNEMONIC
1	Left/Right Clock	LRCLK
2	Word Clock	WDCLK
3	Clock Input	CLK
4	Data Input	DATA
5	No Connection	NC
6	Digital Common	D_{COM}
7	Analog Common	A_{COM}
8	Left Channel V_{OUT}	L CH Out
9	Output Common	V_{COM}
10	Right Channel V_{OUT}	R CH Out
11	Analog Supply	$+V_{CC}$
12	Analog Supply	$+V_{CC}$
13	Reference Decouple	C_{REF}
14	Reference Sense	V_{REF} SENSE
15	Reference Output	V_{REF}
16	Analog Supply	$+V_{CC}$
17	Analog Supply	$+V_{CC}$
18	Digital Supply	$+V_{CC}$
19	Single DAC Mode	SDM SEL
20	Left/Right DAC Select	LRDAC

THEORY OF OPERATION

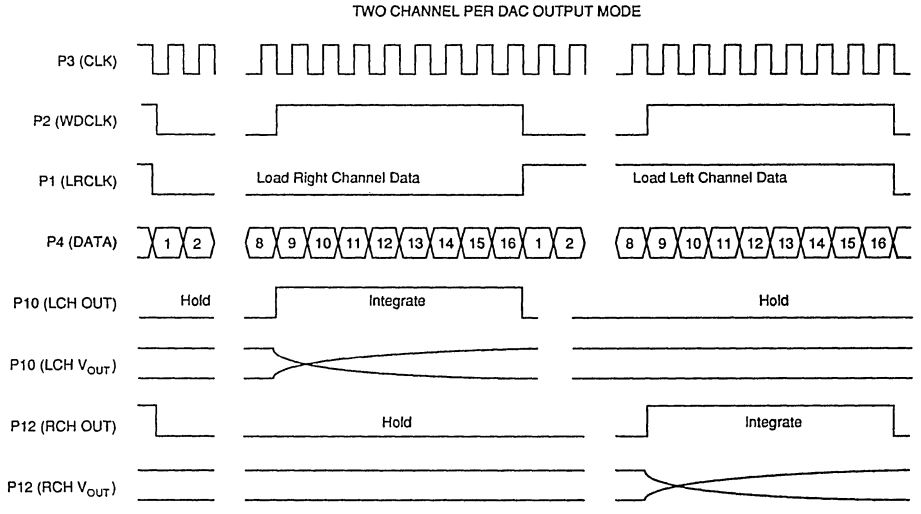
The PCM60P/66P is a dual output, 16-bit CMOS digital-to-analog audio converter. The PCM60P/66P, complete with internal reference, has two glitch-free voltage outputs and requires only a single +5V power supply. Output modes using either one or two channels per DAC are user selectable. The PCM60P/66P accepts a serial data input format that is compatible with other Burr-Brown PCM products such as the industry standard PCM56P.

ONE DAC TWO-CHANNEL OPERATION

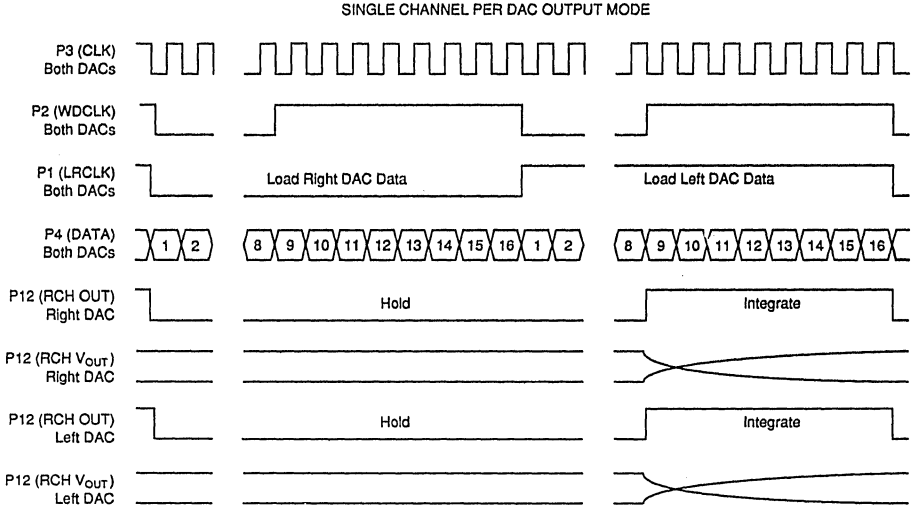
Normally, the PCM60P/66P is operated with a continuous clock input in a two-channel output mode. This mode is selected when SDM SEL is held low (single DAC mode select). Refer to the truth table shown by Table I for exact control logic relationships. Data for left and right channel output is loaded alternately into the PCM60P/66P while the control logic switches the left and right output amplifiers between the appropriate integrate and hold modes. Data word latching is controlled by WDCLK (word clock) and channel selection is made by LRCLK (left/right clock). Figure 1 shows the timing for the single DAC two-channel mode of operation. The block diagram in Figure 2 shows how a single DAC output provides switched output to both integrate and hold amplifiers. Output between left and right channels in this mode is not in phase. See Figure 3 for proper connection of the PCM60P/66P in the two-channel DAC mode.

PIN FUNCTIONS				SERIAL DATA WORD INPUT	LEFT CHANNEL OUTPUT	RIGHT CHANNEL OUTPUT
SDM SEL	LRDAC	LRCLCK	WDCLK			
0	X	0	0	Right	Hold	Hold
0	X	0	1	Right	Integrate	Hold
0	X	1	0	Left	Hold	Hold
0	X	1	1	Left	Hold	Integrate
1	0	0	0	Inhibited	V_{COM}	Hold
1	0	0	1	Inhibited	V_{COM}	Hold
1	0	1	0	Left	V_{COM}	Integrate
1	0	1	1	Left	V_{COM}	Integrate
1	1	0	0	Right	V_{COM}	Hold
1	1	0	1	Right	V_{COM}	Hold
1	1	1	0	Inhibited	V_{COM}	Integrate
1	1	1	1	Inhibited	V_{COM}	Integrate
NOTE: Positive edge of CLK (P3) latches LRCLK (P1), WDCLK (P2), and DATA (P4).						

TABLE I. PCM60P/66P Logic Truth Table.



NOTES: Single DAC Mode Select = 0; L/R DAC Select = X; WDCLK = 50% duty cycle; Serial Data is read in MSB first with BTC coding (MSB = Bit 1).



NOTES: Single DAC Mode Select = 1; L/R DAC Select = 0 (Left DAC) or 1 (Right DAC).

FIGURE 1. PCM60P/66P Timing Diagram.

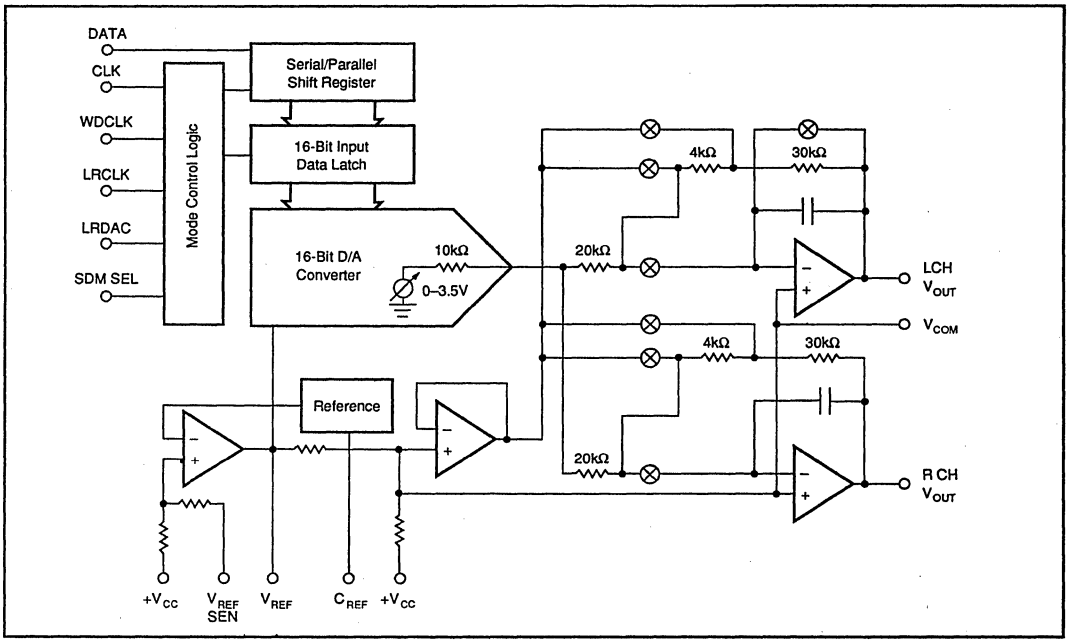


FIGURE 2. PCM60P/66P Block Diagram.

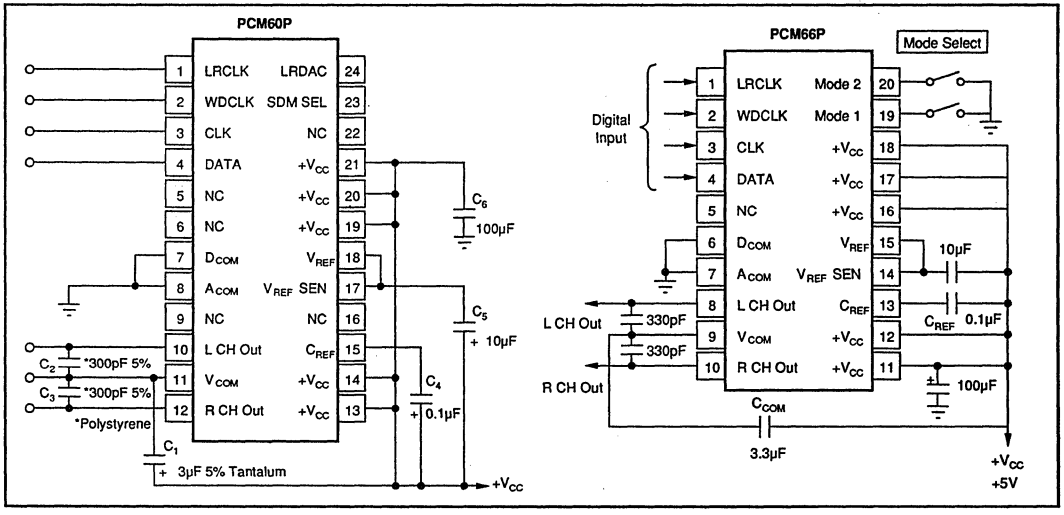


FIGURE 3. PCM60P/66P Connection Diagram.

TWO DAC TWO-CHANNEL OPERATION

In phase, two-channel output can be obtained by using two PCM60P/66Ps and choosing the single DAC mode (setting SDM SEL high). With the use of a high or low input level on LRDAC (P left/right DAC select), each DAC can have its right channel output dedicated to either left or right data input with no additional input signals being required to latch the appropriate data from an alternating L/R data word input stream. In the single DAC mode, the PCM60P/66P's left channel output is disabled and held at $+V_{COM}$. In this mode both DACs share common inputs for DATA, CLK, WDCLK, and LRCLK. Otherwise circuit connection is the same as the two-channel DAC mode, with the exception of LRDAC whose level selects whether the single DAC will output dedicated left or right channel data.

INTEGRATE AND HOLD OUTPUT AMPLIFIERS

The PCM60P/66P incorporates integrate and hold amplifiers on each output channel. This allows a single, very fast DAC to feed both amplifiers and reduce circuit complexity. It also serves to block the output glitch from the DAC to the individual channel outputs and effectively makes the PCM60P/66P outputs "glitch-free." The PCM60P/66P is a single +5V supply device with a voltage output swing of 2.8Vp-p. The outputs swing asymmetrically around V_{COM} ($+V_{CC} - 2.33V$). See Table II for exact input/output relationships. Since true CMOS amplifiers are used on the PCM60P/66P, the load resistance on the outputs should not be less than 100kΩ and the capacitive loads should not exceed 100pF. For maximum low-distortion performance, output buffer amplifiers should be considered.

DIGITAL INPUT	ANALOG OUTPUT	
Binary Two's Complement (Hex)	DAC Output (V)	Voltage (V) V_{OUT} Mode
7FFF	+FS	+3.5629443
0000	BPZ	+2.1629871
8000	–FS	+0.7630299
2E5B	V_{COM}	+2.6700000

TABLE II. PCM60P/66P Input/Output Relationships.

DISCUSSION OF SPECIFICATIONS

TOTAL HARMONIC DISTORTION + NOISE

The key specification for the PCM60P/66P is total harmonic distortion plus noise. Digital data words are read into the PCM60P/66P at four times the standard audio sampling frequency of 44.1kHz or 176.4kHz for each channel, such that a sine wave output of 991Hz is realized. For production testing, the output of the DAC goes to a programmable gain amplifier to provide gain at lower signal output test levels and then through a 20kHz low pass filter before being fed into an analog type distortion analyzer. Figure 4 shows a block diagram of the production THD + N test setup.

In terms of signal measurement, THD + N is the ratio of $Distortion_{RMS} + Noise_{RMS}/Signal_{RMS}$ expressed in dB. For the PCM60P/66P, THD + N is 100% tested at three different output levels using the test setup shown in Figure 4. It is significant to note that this circuit does not include any output deglitching circuitry. This means the PCM60P/66P meets even its –60dB THD + N specification without use of external deglitchers.

ABSOLUTE LINEARITY

Even though absolute integral and differential linearity specs are not given for the PCM60P/66P, the extremely low THD + N performance is typically indicative of 14-bit to 15-bit integral linearity in the DAC depending on the grade specified. The relationship between THD + N and linearity, however, is not such that an absolute linearity specification for every individual output code can be guaranteed.

IDLE CHANNEL SNR

Another appropriate spec for a digital audio converter is idle channel signal-to-noise ratio (idle channel SNR). This is the ratio of the noise on either DAC output at bipolar zero in relation to the full scale range of the DAC. The output of the DAC is band limited from 20Hz to 20kHz and an A-weighted filter is applied to make this measurement.

OFFSET, GAIN, AND TEMPERATURE DRIFT

The PCM60P/66P is specified for other important parameters such as channel separation and gain mismatch between output channels. And although the PCM60P/66P is primarily meant for use in dynamic applications, typical specs are also given for more traditional DC parameters such as gain error, bipolar zero offset error, and temperature gain drift.

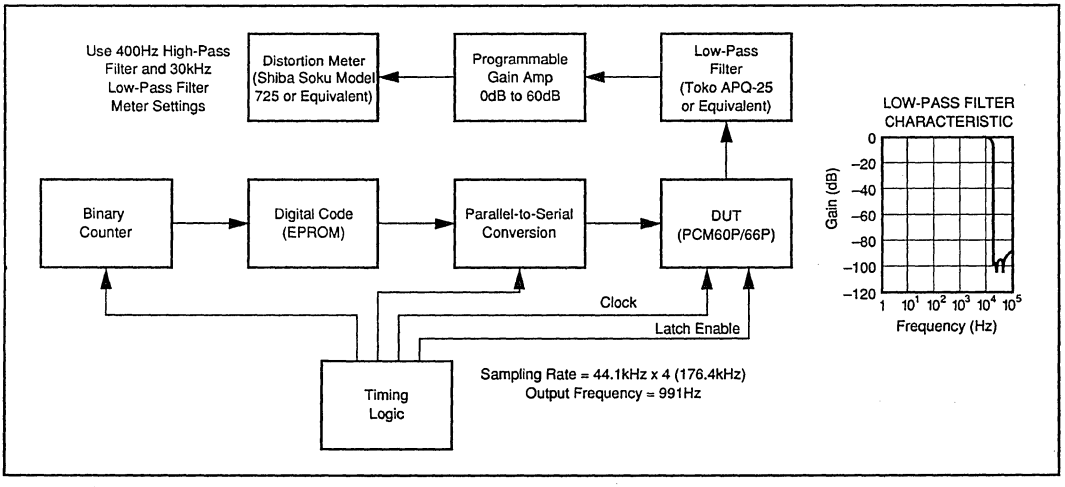


FIGURE 4. THD + N Test Setup Diagram.

TIMING CONSIDERATIONS

The data format of the PCM60P/66P is binary two's complement (BTC) with the most significant bit (MSB) being first in the serial input bit stream. Table II describes the exact input data to voltage output coding relationship. Any number of bits can precede the 16 bits to be loaded, as only the last 16 will be transferred to the parallel DAC register on the first positive edge of CLK (clock input) after WDCLK (word clock) has gone low. All inputs to the PCM60P/66P are TTL level compatible.

WDCLK DUTY CYCLE

WDCLK is the input signal that controls when data is loaded and how long each output is in the integrate mode. It is therefore recommended that a 50% (high) duty cycle be maintained on WDCLK. This will ensure that each output will have enough time to reach its final output value, and that the output level of each channel will be within the gain mismatch specification. Refer to Figure 1 for exact timing relationships of WDCLK to CLK and LRCLK and the outputs of the PCM60P/66P. The WDCLK can be high longer than 50%, as long as setup and hold times shown in Figure 5 are observed and the time high is roughly equivalent for both left and right channels.

SETUP AND HOLD TIMES

The individual serial data bit shifts, the serial to parallel data transfer, and left/right control are triggered on positive CLK edges. The setup time required for DATA, WDCLK, and LRCLK to be latched by the next positive going CLK is 15ns minimum. A minimum hold time of 15ns is also required after the positive going CLK edge for each data bit to be shifted into the serial input register. Refer to Figure 5 for the timing relationship of these signals.

MAXIMUM CLOCK RATE

The 100% tested maximum clock rate of 8.47MHz for the PCM60P/66P is derived by multiplying the standard audio sample rate of 44.1kHz times eight (4X oversampling times two channels) times the standard audio word bit length of 24 (44.1kHz X 4 X 2 X 24 = 8.47MHz). Note that this clock rate accommodates a 24-bit word length, even though only 16 bits are actually being used.

"STOPPED-CLOCK" OPERATION

The PCM60P/66P is normally operated with a continuous clock input signal. If the clock is to be stopped between input data words, the last 16 bits shifted in are not actually shifted from the serial register to the latched parallel DAC register until the first clock after the one used to input bit 16 (LSB). This means the data is not shifted into the DHC latch until the start of the next 16-bit data word input, unless at least one additional clock accompanies the 16 used to serially shift in data in the first place. In either case, the setup and hold times for DATA, WDCLK, and LRCLK must still be observed.

INSTALLATION

The PCM60P/66P only requires a single +5V supply. The +5V supply, however, is used in deriving the internal reference. It is therefore very important that this supply be as "clean" as possible to reduce coupling of supply noise to the outputs. If a good analog supply is available at greater than +5V, a zener diode can be used to obtain a stable +5V supply. A 100µF decoupling capacitor as shown in Figure 3 should be used regardless of how good the +5V supply is to maximize power supply rejection. All grounds should be connected to the analog ground plane as close to the PCM60P/66P as possible.

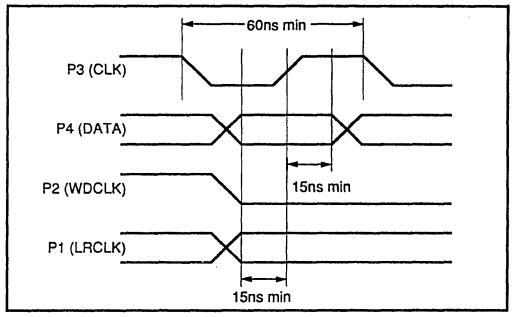


FIGURE 5. PCM60P/66P Setup and Hold Timing Diagram.

FILTER CAPACITOR REQUIREMENTS

As shown in Figure 3, C_{REF} and V_{REF} SENSE should have decoupling capacitors of 0.1µF (C_4) and 10µF (C_5) to $+V_{CC}$ respectively with no special tolerance being required. To maximize channel separation between left and right channels, 5% 300pF capacitors (C_2 and C_3) between V_{COM} and left and right channel outputs are required in addition to a 5% 3µF capacitor (C_1) between V_{COM} and +5V. The ratio of 10k to 1 is the important factor here for proper circuit operation. Placement of all capacitors should be as close to the appropriate pins of the PCM60P/66P as possible to reduce noise pickup from surrounding circuitry.

APPLICATIONS

Probably the most popular use of the PCM60P/66P is in applications requiring single power supply operation. For example, the PCM60P/66P is ideal for automotive compact disk (CD) and digital audio tape (DAT) playback units. To use a more complex bipolar DAC requiring ±5V supplies in the +12V application, for example, would require driving a stable "floating" ground and regulating the +12V to +10V. The single supply CMOS PCM60P/66P would only require a +5V zener diode to regulate its 50mW max supply. The outputs could be AC coupled to the rest of the circuit for perfectly acceptable high dynamic performance. The PCM60P/66P is ideal in any application requiring a minimum of additional circuitry as well as ultra-low-power CMOS performance.

Of course, the PCM60P/66P is the D/A converter of choice in any application requiring very low power dissipation. Portable battery powered test and measurement equipment requiring very low distortion digital to analog converters would be an ideal application for the CMOS PCM60P/66P with its 50mW max power dissipation.

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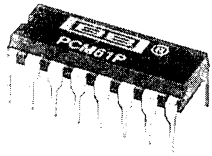


PCM61P

See Also PCM1700P
Dual 18-Bit D/A Converter
Pg. 9.2-183

Serial Input 18-Bit Monolithic Audio DIGITAL-TO-ANALOG CONVERTER

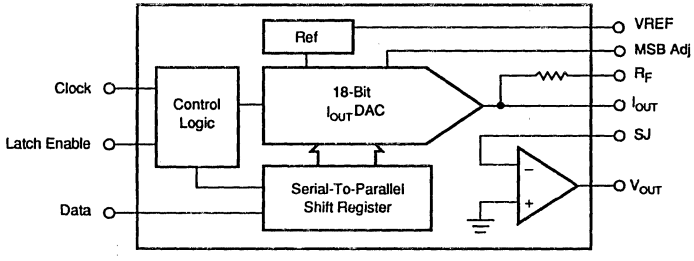
FEATURES

- 18-BIT MONOLITHIC AUDIO D/A CONVERTER
- LOW MAX THD + N: –92dB Without External Adjust
- 100% PIN COMPATIBLE WITH INDUSTRY STD 16-BIT PCM56P
- GLITCH FREE OUTPUT OF ±3V OR ±1mA
- CAPABLE OF 8X OVERSAMPLING RATE IN V_{OUT} MODE
- COMPLETE WITH INTERNAL REFERENCE AND OUTPUT OP-AMP
- RELIABLE PLASTIC 16-PIN DIP PACKAGE

DESCRIPTION

The PCM61P is an 18-bit totally pin compatible performance replacement for the popular 16-bit PCM56P. With the addition of two extra bits, lower max THD + N (–92dB; PCM61P-K) can be achieved in audio applications already using the PCM56P. The PCM61P is complete with internal reference and output op-amp and requires no external parts to function as an 18-bit DAC. The PCM61P is capable of an 8-times oversampling rate (single channel) and meets all of its specifications without an external output deglitcher.

The PCM61P comes in a small, reliable 16-pin plastic DIP package that has passed operating life tests under simultaneous high temperature, high humidity and high pressure testing.



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PDS-972A

SPECIFICATIONS

ELECTRICAL

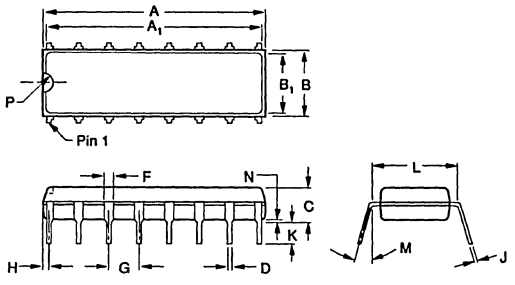
All Specifications at 25°C, and $+V_{CC}$ = +5V unless otherwise noted.

PARAMETER	CONDITIONS	PCM61P/P-J/P-K MIN	TYP	MAX	UNITS
RESOLUTION				18	bits
DYNAMIC RANGE			108		dB
INPUT					
DIGITAL INPUT					
Logic Family			TTL/CMOS Compatible		
Logic Level: V_{IH}		+2		$+V_{CC}$	V
V_{IL}		0		+0.8	V
I_{IH}	V_{IH} = +2.7V			+1	µA
I_{IL}	V_{IL} = +0.4V			–50	µA
Data Format		Serial BTC[1]			
Input Clock Frequency				16.9	MHz
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion + N[2]	Without MSB Adjustments				
PCM61P					
f = 991Hz (0dB)[3]	f_S = 176.4kHz[4]		–88	–82	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–74	–68	dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–34	–28	dB
PCM61P-J					
f = 991Hz (0dB)	f_S = 176.4kHz		–94	–88	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–76	–74	dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–36	–34	dB
PCM61P-K					
f = 991Hz (0dB)	f_S = 176.4kHz		–98	–92	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–80	–74	dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–40	–34	dB
IDLE CHANNEL SNR	20Hz to 20kHz at BPZ[5]		112		dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error			±2		%
Bipolar Zero Error			±30		mV
Differential Linearity Error			±0.001		%
Total Drift[6]	0°C to 70°C		±25		ppm of FSR/°C
Bipolar Zero Drift	0°C to 70°C		±4		ppm of FSR/°C
Warm-up Time		1			minute
MONOTONICITY			16		bits
ANALOG OUTPUT					
Voltage: Output Range			±3		V
Output Current		±8			mA
Output Impedance			0.1		Ω
Current: Output Range	±30%		±1		mA
Output Impedance	±30%		1.2		kΩ
SETTLING TIME	To ±0.006% of FSR				
Voltage: 6V Step			1.5		µs
1 LSB			1.		µs
Slew Rate			12		V/µs
Current: 1mA Step	10Ω to 100Ω load		250		ns
1mA Step	1kΩ load		350		ns
Glitch Energy	Meets all THD + N specs without external deglitching				
POWER SUPPLY REQUIREMENTS[7]					
$\pm V_{CC}$ Supply Voltage		±4.75	±5	±13.2	V
Supply Current: $+I_{CC}$	$+V_{CC}$ = +5V		+10	+17	mA
$+I_{CC}$	$+V_{CC}$ = +12V		+12		mA
$-I_{CC}$	$-V_{CC}$ = –5V		–25	–35	mA
$-I_{CC}$	$-V_{CC}$ = –12V		–27		mA
Power Dissipation	$\pm V_{CC}$ = ±5V		175	260	mW
	$\pm V_{CC}$ = ±12V		475		mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–30		+70	°C
Storage		–60		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$)/$Signal_{RMS}$. (3) D/A converter output frequency/signal level. (4) D/A converter sample frequency (4 x 44.1kHz; 4 times oversampling). (5) Bipolar zero, using A-weighted filter. (6) This is the combined drift error due to gain, offset, and linearity over temperature. (7) All positive and all negative supply pins must be tied together respectively.

MECHANICAL

P Package — 16-Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.740	.800	18.80	20.32
A1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	0.20	.050	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

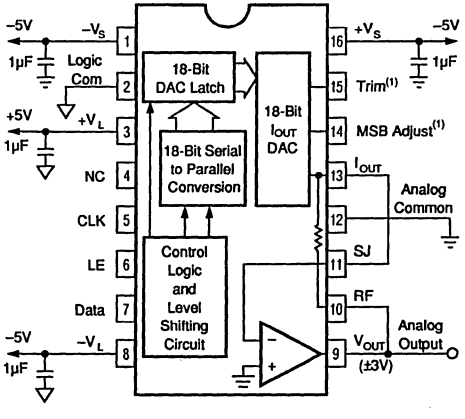
PIN ASSIGNMENTS

1	$-V_S$	Analog Negative Supply
2	LOG COM	Logic Common
3	$+V_L$	Logic Positive Supply
4	NC	No Connection
5	CLK	Clock Input
6	LE	Latch Enable Input
7	DATA	Serial Data Input
8	$-V_L$	Logic Negative Supply
9	V_{OUT}	Voltage Output
10	RF	Feedback Resistance
11	SJ	Summing Junction
12	ANA COM	Analog Common
13	I_{OUT}	Current Output
14	MSB ADJ	MSB Adjustment Terminal
15	TRIM	MSB Trim-pot Terminal
16	$+V_S$	Analog Positive Supply

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltages	±16VDC
Input Logic Voltage	–1V to V_S /$+V_L$
Power Dissipation	850mW
Operating Temperature Range	–25°C to +70°C
Storage Temperature Range	–60°C to +100°C
Lead Temperature (soldering, 10 seconds)	+300°C

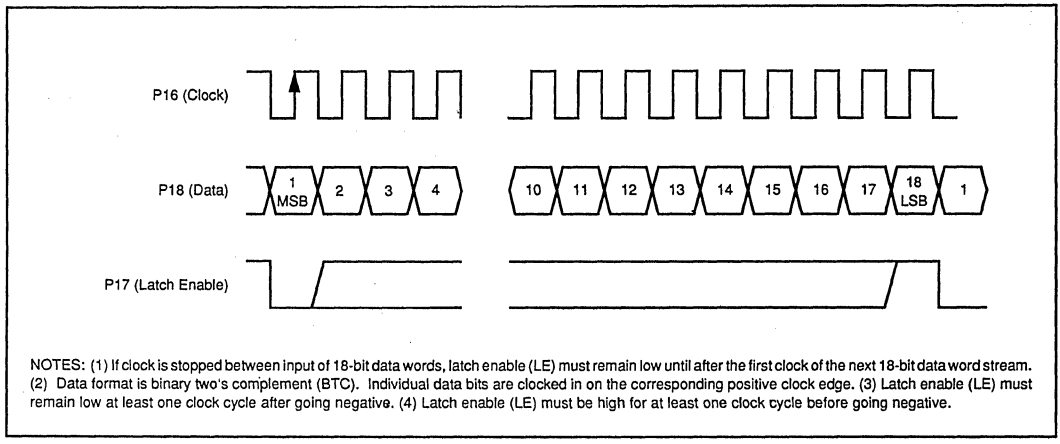
CONNECTION DIAGRAM



NOTE: (1) MSB error (Bipolar Zero differential linearity error) can be adjusted to zero using the external circuit shown in Figure 4.

TABLE I. PCM61P Input/Output Relationships.

DIGITAL INPUT	ANALOG OUTPUT		
Binary Two's Complement (BTC)	DAC Output	Voltage (V) V_{OUT} Mode	Current (mA) I_{OUT} Mode
1FFFF Hex	+FS	–0.99999237	+2.99997711
00000 Hex	BPZ	0.00000000	0.00000000
3FFFF Hex	BPZ – 1LSB	+0.00000763	–0.00002289
20000 Hex	–FS	+1.00000000	–3.00000000



NOTES: (1) If clock is stopped between input of 18-bit data words, latch enable (LE) must remain low until after the first clock of the next 18-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch enable (LE) must remain low at least one clock cycle after going negative. (4) Latch enable (LE) must be high for at least one clock cycle before going negative.

FIGURE 2. PCM61P Timing Diagram.

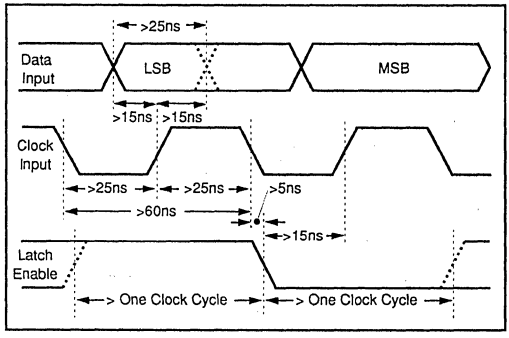


FIGURE 3. PCM61P Setup and Hold Timing Diagram.

MAXIMUM CLOCK RATE

The maximum clock rate of 16.9MHz for the PCM61P is derived by multiplying the standard audio sample rate of 44.1kHZ times sixteen (16X oversampling) times the standard audio word bit length of 24 (44.1kHz x 16 x 24 = 16.9MHz). Note that this clock rate accommodates a 24-bit word length, even though only 18 bits are actually being used.

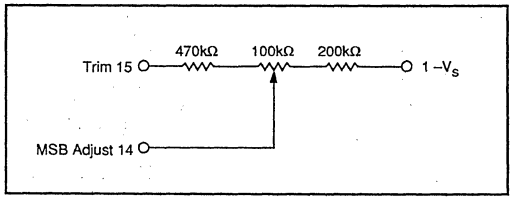


FIGURE 4. MSB Adjust Circuit.

MSB ERROR ADJUSTMENT PROCEDURE (OPTIONAL)

The MSB error of the PCM61P can be adjusted to make the differential linearity error (DLE) at BPZ essentially zero. This is important when the signal output levels are very low, because zero crossing noise (DLE at BPZ) becomes very significant when compared to the small code changes occurring in the LSB portion of the converter.

To statically adjust DLE at BPZ, refer to the circuit shown in Figure 4 or the PCM61P connection diagram.

Differential linearity error at bipolar zero and THD are guaranteed to meet data sheet specifications without any external adjustment. However, a provision has been made for an optional adjustment of the MSB linearity point, which makes it possible to eliminate DLE error at BPZ. Two procedures are given to allow either static or dynamic adjustment. The dynamic procedure is preferred because of the difficulty associated with the static method (accurately measuring 16-bit LSB steps).

After allowing ample warm-up time (5-10 minutes) to assure stable operation of the PCM61P, select input code 3FFFF hexadecimal (all bits on except the MSB). Measure the output voltage using a 6-1/2 digit voltmeter and record it. Change the digital input code to 00000 hexadecimal (all bits off except the MSB). Adjust the 100kΩ potentiometer to make the output read 22.9μV more than the voltage reading of the previous code (a 1LSB step = 22.9μV). A much simpler method is to dynamically adjust the DLE at BPZ. Assuming the device has been installed in a digital audio application circuit, send the appropriate digital input to produce a –60dB level sinusoidal output, then adjust the 100kΩ potentiometer until a minimum level of distortion is observed.

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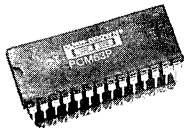


PCM63P

Colinear™ 20-Bit Monolithic Audio DIGITAL-TO-ANALOG CONVERTER

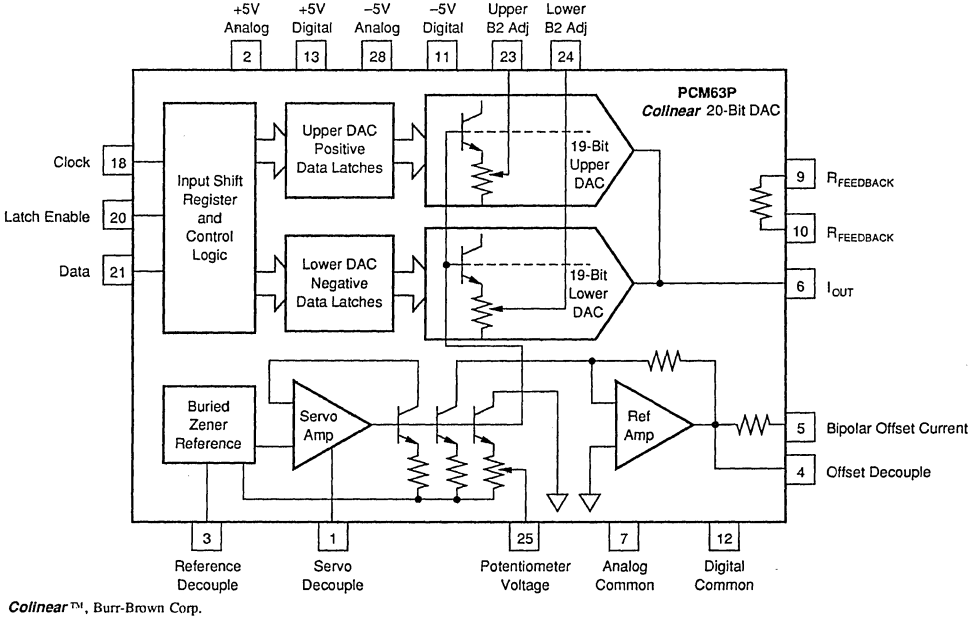
FEATURES

- *COLINEAR* 20-BIT AUDIO DAC
- NEAR-IDEAL LOW LEVEL OPERATION
- GLITCH-FREE OUTPUT
- ULTRA LOW –96dB max THD + N (Without External Adjustment)
- 116dB SNR min (A-Weight Method)
- INDUSTRY STD SERIAL INPUT FORMAT
- FAST (200ns) CURRENT OUTPUT (±2mA; ±2% max)
- CAPABLE OF 16x OVERSAMPLING
- COMPLETE WITH REFERENCE

DESCRIPTION

The PCM63P is a precision 20-bit digital-to-analog converter with ultra-low distortion (–96dB max with a full scale output; PCM63P-K). Incorporated into the PCM63P is a unique ***Colinear*** dual-DAC per channel architecture that eliminates unwanted glitches and other nonlinearities around bipolar zero. The PCM63P also features a very low noise (116dB max SNR; A-weighted method) and fast settling current output (200ns typ, 2mA step) which is capable of 16-times oversampling rates.

Applications include very low distortion frequency synthesis and high-end consumer and professional digital audio applications.



Colinear™, Burr-Brown Corp.

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1083

SPECIFICATIONS

ELECTRICAL

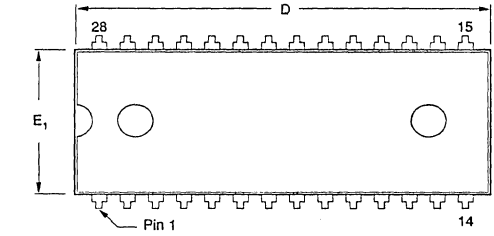
All specifications at 25°C and $\pm V_A$ and $\pm V_D$ = ±5V, unless otherwise noted.

PARAMETER	CONDITIONS	PCM63P, PCM63P-J, PCM63P-K MIN	TYP	MAX	UNITS
RESOLUTION		20			Bits
DYNAMIC RANGE, THD + N at –60dB Referred to Full Scale					
PCM63P		96	100		dB
PCM63P-J		100	104		dB
PCM63P-K		104	108		dB
DIGITAL INPUT					
Logic Family			TTL/CMOS Compatible		
Logic Level: V_{IH}		+2		$+V_D$	V
V_{IL}		0		0.8	V
I_{IH}	V_{IH} = +2.7V			+1	µA
I_{IL}	V_{IL} = +0.4V			–50	µA
Data Format			Serial, MSB First, BTC[1]		
Input Clock Frequency			30	25	MHz
TOTAL HARMONIC DISTORTION + N[2], Without Adjustments					
PCM63P					
f = 991Hz (0dB)[3]	f_S = 352.8kHz[4]		–92	–88	dB
f = 991Hz (–20dB)	f_S = 352.8kHz		–80	–74	dB
f = 991Hz (–60dB)	f_S = 352.8kHz		–40	–36	dB
PCM63P-J					
f = 991Hz (0dB)	f_S = 352.8kHz		–96	–92	dB
f = 991Hz (–20dB)	f_S = 352.8kHz		–82	–76	dB
f = 991Hz (–60dB)	f_S = 352.8kHz		–44	–40	dB
PCM63P-K					
f = 991Hz (0dB)	f_S = 352.8kHz		–100	–96	dB
f = 991Hz (–20dB)	f_S = 352.8kHz		–88	–82	dB
f = 991Hz (–60dB)	f_S = 352.8kHz		–48	–44	dB
ACCURACY					
Level Linearity	at –90dB Signal Level		±0.3	±1	dB
Gain Error			±1	±2	%
Bipolar Zero Error[5]			±10		mV
Gain Drift	0°C to 70°C		25		ppm/°C
Bipolar Zero Drift	0°C to 70°C		4		ppm of FSR/°C
Warm-up Time		1			Minute
IDLE CHANNEL SNR[6]	20Hz to 20kHz at BPZ[7]	+116	+120		dB
POWER SUPPLY REJECTION			+86		dB
ANALOG OUTPUT					
Output Range		±1.96	±2.00	±2.04	mA
Output Impedance			670		Ω
Internal $R_{FEEDBACK}$			1.5		kΩ
Settling Time	2mA Step		200		ns
Glitch Energy			No Glitch Around Zero		
POWER SUPPLY REQUIREMENTS					
$\pm V_A$, $\pm V_D$ Supply Voltage Range		±4.50	±5	±5.50	V
$+I_A$, $+I_D$ Combined Supply Current	$+V_A$, $+V_D$ = +5V		10	15	mA
$-I_A$, $-I_D$ Combined Supply Current	$-V_A$, $-V_D$ = –5V		–35	–45	mA
Power Dissipation	$\pm V_A$, $\pm V_D$ = ±5V		225	300	mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–40		+85	°C
Storage		–60		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$) / $Signal_{RMS}$. (3) D/A converter output frequency (signal level). (4) D/A converter sample frequency (8 x 44.1kHz; 8x oversampling). (5) Offset error at bipolar zero. (6) Measured using an OPA27 and 1.5kΩ feedback and an A-weighted filter. (7) Bipolar Zero.

MECHANICAL

P Package — 28-Pin Plastic DIP

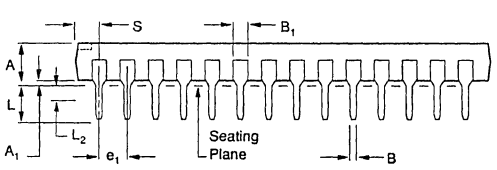


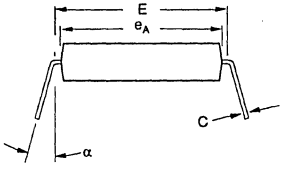
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A (1)	.169	.200	4.29	5.08
A1 (1)	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D (1)	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1 (1)	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
Q1	.020	.070	0.51	1.78
S1	.040	.080	1.02	2.03

(1) Not JEDEC Standard

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.





PIN ASSIGNMENTS

PIN	DESCRIPTION	MNEMONIC
P1	Servo Amp Decoupling Capacitor	CAP
P2	+5V Analog Supply Voltage	$+V_A$
P3	Reference Decoupling Capacitor	CAP
P4	Offset Decoupling Capacitor	CAP
P5	Bipolar Offset Current Output (+2mA)	BPO
P6	DAC Current Output (0 to –4mA)	I_{OUT}
P7	Analog Common Connection	ACOM
P8	No Connection	NC
P9	Feedback Resistor Connection (1.5kΩ)	RF_1
P10	Feedback Resistor Connection (1.5kΩ)	RF_2
P11	–5V Digital Supply Voltage	$-V_D$
P12	Digital Common Connection	DCOM
P13	+5V Digital Voltage Supply	$+V_D$
P14	No Connection	NC
P15	No Connection	NC
P16	No Connection	NC
P17	No Connection	NC
P18	DAC Data Clock Input	CLK
P19	No Connection	NC
P20	DAC Data Latch Enable	LE
P21	DAC Data Input	DATA
P22	No Connection	NC
P23	Optional Upper DAC Bit-2 Adjust (–4.29V)*	UB2 Adj
P24	Optional Lower DAC Bit-2 Adjust (–4.29V)*	LB2 Adj
P25	Bit Adjust Reference Voltage Tap (–3.52V)*	V_{POT}
P26	No Connection	NC
P27	No Connection	NC
P28	–5V Analog Supply Voltage	$-V_A$

*Nominal voltages at these nodes assuming $\pm V_A$; $\pm V_D$ = ±5V.

ABSOLUTE MAXIMUM RATINGS

$+V_A$, $+V_D$ to ACOM/DCOM	0V to +8V
$-V_A$, $-V_D$ to ACOM/DCOM	0V to –8V
$-V_A$, $-V_D$ to $+V_A$, $+V_D$	0V to +16V
ACOM to DCOM	±0.5V
Digital Inputs (pins 18, 20, 21) to DCOM	–1V to $+V_D$
Power Dissipation	500mW
Lead Temperature, (soldering, 10s)	+300°C
Max Junction Temperature	165°C
Thermal Resistance, θ_{JA}	70°C/W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

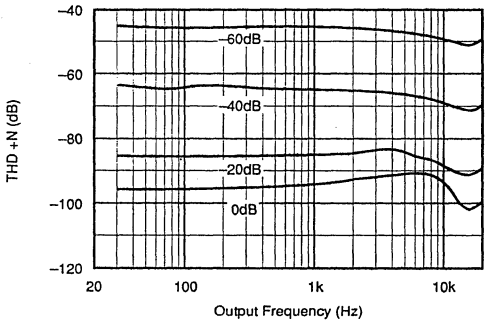
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	MAX THD + N, AT 0dB
PCM63P	Plastic DIP	0°C to +70°C	–88dB
PCM63P-J	Plastic DIP	0°C to +70°C	–92dB
PCM63P-K	Plastic DIP	0°C to +70°C	–96dB

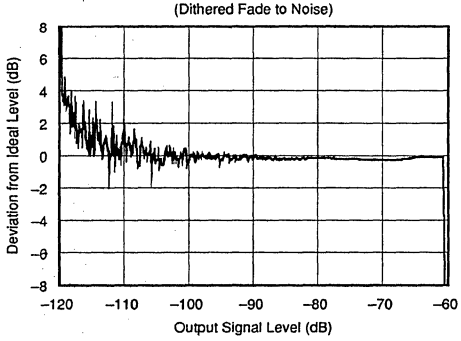
TYPICAL PERFORMANCE CURVES

All specifications at 25°C and $\pm V_A$ and $\pm V_D$ = ±5.0V, unless otherwise noted.

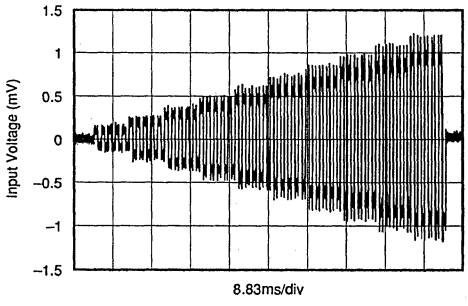
THD + N vs FREQUENCY



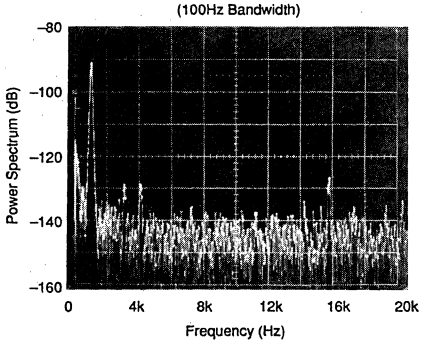
16-BIT LEVEL LINEARITY
(Dithered Fade to Noise)



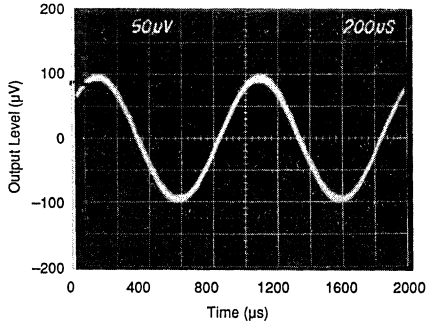
16-BIT MONOTONICITY



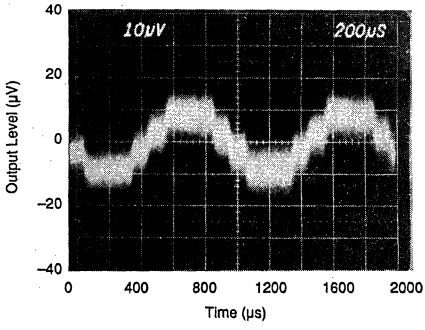
–90dB SIGNAL SPECTRUM
(100Hz Bandwidth)



–90dB SIGNAL
(10Hz to 20kHz Bandwidth)



–110dB SIGNAL
(10Hz to 20kHz Bandwidth)



THEORY OF OPERATION

DUAL-DAC *COLINEAR* ARCHITECTURE

Digital audio systems have traditionally used laser-trimmed, current-source DACs in order to achieve sufficient accuracy. However even the best of these suffer from potential low-level nonlinearity due to errors at the major carry bipolar zero transition. More recently, DACs employing a different architecture which utilizes noise shaping techniques and very high oversampling frequencies, have been introduced ("Bitstream", "MASH", or 1-bit DACs). These DACs overcome the low level linearity problem, but only at the expense of signal-to-noise performance, and often to the detriment of channel separation and intermodulation distortion if the succeeding circuitry is not carefully designed.

The PCM63 is a new solution to the problem. It combines all the advantages of a conventional DAC (excellent full scale performance, high signal-to-noise ratio and ease of use) with superior low-level performance. Two DACs are combined in a complementary arrangement to produce an extremely linear output. The two DACs share a common reference and a common R-2R ladder to ensure perfect tracking under all conditions. By interleaving the individual bits of each DAC and employing precise laser trimming of resistors, the highly accurate match required between DACs is achieved.

This new, complementary linear or dual-DAC ***Colinear*** approach, which steps away from zero with small steps in both directions, avoids any glitching or "large" linearity errors and provides an absolute current output. The low level performance of the PCM63P is such that real 20-bit resolution can be realized, especially around the critical bipolar zero point.

Table I shows the conversion made by the internal logic of the PCM63P from binary two's complement (BTC). Also, the resulting internal codes to the upper and lower DACs (see front page block diagram) are listed. Notice that only the LSB portions of either internal DAC are changing around bipolar zero. This accounts for the superlative performance of the PCM63P in this area of operation.

DISCUSSION OF SPECIFICATIONS

DYNAMIC SPECIFICATIONS

Total Harmonic Distortion + Noise

The key specification for the PCM63P is total harmonic distortion plus noise (THD + N). Digital data words are read into the PCM63P at eight times the standard compact disk audio sampling frequency of 44.1kHz (352.8kHz) so that a sine wave output of 991Hz is realized. For production testing, the output of the DAC goes to an I to V converter, then to a programmable gain amplifier to provide gain at lower signal output test levels, and then through a 40kHz low pass filter before being fed into an analog type distortion analyzer. Figure 1 shows a block diagram of the production THD + N test setup.

For the audio bandwidth, THD + N of the PCM63P is essentially flat for all frequencies. The typical performance curve, "THD + N vs Frequency", shows four different output signal levels: 0dB, –20dB, –40dB, and –60dB. The test signals are derived from a special compact test disk (the CBS CD-1). It is interesting to note that the –20dB signal falls only about 10dB below the full scale signal instead of the expected 20dB. This is primarily due to the superior low-level signal performance of the dual-DAC ***Colinear*** architecture of the PCM63P.

In terms of signal measurement, THD + N is the ratio of $Distortion_{RMS} + Noise_{RMS} / Signal_{RMS}$ expressed in dB. For the PCM63P, THD + N is 100% tested at all three specified output levels using the test setup shown in Figure 1. It is significant to note that this test setup does not include any output deglitching circuitry. All specifications are achieved without the use of external deglitchers.

Dynamic Range

Dynamic range in audio converters is specified as the measure of THD + N at an effective output signal level of –60dB referred to 0dB. Resolution is commonly used as a theoretical measure of dynamic range, but it does not take into account the effects of distortion and noise at low signal levels. The

ANALOG OUTPUT	INPUT CODE (20-bit Binary Two's Complement)	LOWER DAC CODE (19-bit Straight Binary)	UPPER DAC CODE (19-bit Straight Binary)
+Full Scale	011...111	111...111 + 1LSB*	111...111
+Full Scale – 1LSB	011...110	111...111 + 1LSB*	111...110
Bipolar Zero + 2LSB	000...010	111...111 + 1LSB*	000...010
Bipolar Zero + 1LSB	000...001	111...111 + 1LSB*	000...001
Bipolar Zero	000...000	111...111 + 1LSB*	000...000
Bipolar Zero – 1LSB	111...111	111...111	000...000
Bipolar Zero – 2LSB	111...110	111...110	000...000
–Full Scale + 1LSB	100...001	000...001	000...000
–Full Scale	100...000	000...000	000...000

*The extra weight of 1LSB is added at this point to make the transfer function symmetrical around bipolar zero.

TABLE I. Binary Two's Complement to ***Colinear*** Conversion Chart.

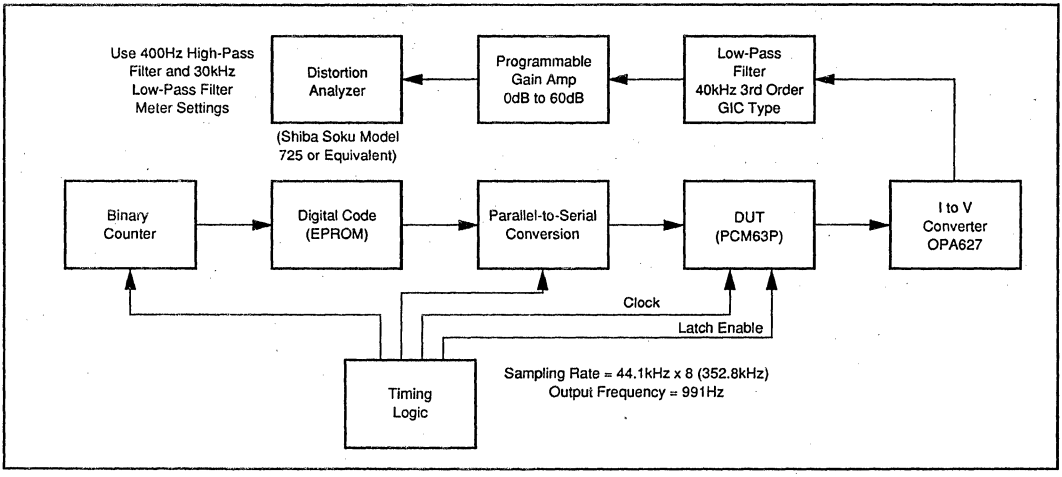


FIGURE 1. Production THD + N Test Setup.

Colinear architecture of the PCM63P, with its ideal performance around bipolar zero, provides a more usable dynamic range, even using the strict audio definition, than any previously available D/A converter.

Level Linearity

Deviation from ideal versus actual signal level is sometimes called "level linearity" in digital audio converter testing. See the "–90dB Signal Spectrum" plot in the Typical Performance Curves section for the power spectrum of a PCM63P at a –90dB output level. (The "–90dB Signal" plot shows the actual –90dB output of the DAC). The deviation from ideal for PCM63P at this signal level is typically less than ±0.3dB. For the "–110dB Signal" plot in the Typical Performance Curves section, true 20-bit digital code is used to generate a –110dB output signal. This type of performance is possible only with the low-noise, near-theoretical performance around bipolar zero of the PCM63P's ***Colinear*** DAC circuitry.

A commonly tested digital audio parameter is the amount of deviation from ideal of a 1kHz signal when its amplitude is decreased from –60dB to –120dB. A digitally dithered input signal is applied to reach effective output levels of –120dB using only the available 16-bit code from a special compact disk test input. See the "16-Bit Level Linearity" plot in the Typical Performance Curves section for the results of a PCM63P tested using this 16-bit dithered fade-to-noise signal. Note the very small deviation from ideal as the signal goes from –60dB to –100dB.

DC SPECIFICATIONS

Idle Channel SNR

Another appropriate specification for a digital audio converter is idle channel signal-to-noise ratio (idle channel SNR). This is the ratio of the noise on the DAC output at bipolar zero in relation to the full scale range of the DAC. To make this measurement, the digital input is continuously fed the code for bipolar zero while the output of the DAC is band-limited from 20Hz to 20kHz and an A-weighted filter is applied. The idle channel SNR for the PCM63P is typically greater than 120dB, making it ideal for low-noise applications.

Monotonicity

Because of the unique dual-DAC ***Colinear*** architecture of the PCM63P, increasing values of digital input will always result in increasing values of DAC output as the signal moves away from bipolar zero in one-LSB steps (in either direction). The "16-Bit Monotonicity" plot in the Typical Performance Curves section was generated using 16-bit digital code from a test compact disk. The test starts with 10 periods of bipolar zero. Next are 10 periods of alternating 1LSBs above and below zero, and then 10 periods of alternating 2LSBs above and below zero, and so on until 10LSBs above and below zero are reached. The signal pattern then begins again at bipolar zero.

With PCM63P, the low-noise steps are clearly defined and increase in near-perfect proportion. This performance is achieved without any external adjustments. By contrast, sigma-delta ("Bitstream", "MASH", or 1-bit DAC) architectures are too noisy to even see the first 3 or 4 bits change (at 16 bits), other than by a change in the noise level.

Absolute Linearity

Even though absolute integral and differential linearity specs are not given for the PCM63P, the extremely low THD + N performance is typically indicative of 16-bit to 17-bit integral linearity in the DAC, depending on the grade specified. The relationship between THD + N and linearity, however, is not such that an absolute linearity specification for every individual output code can be guaranteed.

Offset, Gain, And Temperature Drift

Although the PCM63P is primarily meant for use in dynamic applications, specifications are also given for more traditional DC parameters such as gain error, bipolar zero offset error, and temperature gain and offset drift.

DIGITAL INPUT

Timing Considerations

The PCM63P accepts TTL compatible logic input levels. Noise immunity is enhanced by the use of differential current mode logic input architectures on all input signal lines. The data format of the PCM63P is binary two's complement (BTC) with the most significant bit (MSB) being first in the serial input bit stream. Table II describes the exact relationship of input data to voltage output coding. Any number of bits can precede the 20 bits to be loaded, since only the last 20 will be transferred to the parallel DAC register after LE (P20, Latch Enable) has gone low.

All DAC serial input data (P21, DATA) bit transfers are triggered on positive clock (P18, CLK) edges. The serial-to-parallel data transfer to the DAC occurs on the falling edge of Latch Enable (P20, LE). The change in the output of the DAC coincides with the falling edge of Latch Enable (P20, LE). Refer to Figure 2 for graphical relationships of these signals.

Maximum Clock Rate

A typical clock rate of 16.9MHz for the PCM63P is derived by multiplying the standard audio sample rate of 44.1kHz by sixteen times (16X oversampling) the standard audio word bit length of 24 bits (44.1kHz X 16 X 24 = 16.9MHz). Note that this clock rate accommodates a 24-bit word length, even though only 20 bits are actually being used. The maximum clock rate of 25MHz is guaranteed, but is not 100% final tested. The setup and hold timing relationships are shown in Figure 3.

"Stopped Clock" Operation

The PCM63P is normally operated with a continuous clock input signal. If the clock is to be stopped between input data words, the last 20 bits shifted in are not actually shifted from the serial register to the latched parallel DAC register until Latch Enable (LE, P20) goes low. Latch Enable must remain low until after the first clock cycle of the next data word to insure proper DAC operation. In any case, the setup and hold times for Data and LE must be observed as shown in Figure 3.

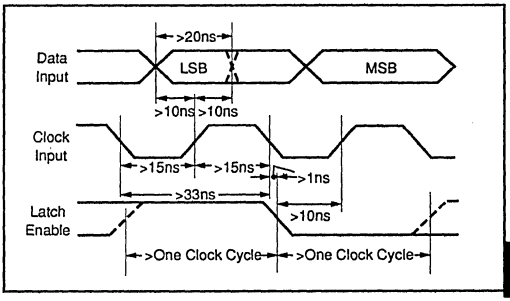
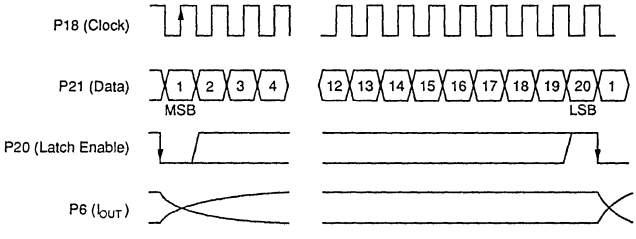


FIGURE 3. Setup and Hold Timing Diagram.

DIGITAL INPUT	ANALOG OUTPUT	CURRENT OUTPUT	VOLTAGE OUTPUT (With External Op Amp)
1,048,576LSBs	Full Scale Range	4.00000000mA	6.00000000V
1LSB	NA	3.81469727nA	5.72204590µV
$7FFFF_{HEX}$	+Full Scale	−1.99999619mA	+2.99999428V
00000_{HEX}	Bipolar Zero	0.00000000mA	0.00000000V
$FFFFF_{HEX}$	Bipolar Zero − 1LSB	+0.00000381mA	−0.00000572V
80000_{HEX}	−Full Scale	+2.00000000mA	−3.00000000V

TABLE II. Digital Input/Output Relationships.



NOTES: (1) If clock is stopped between input of 20-bit data words, Latch Enable (LE) must remain low until after the first clock cycle of the next 20-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch Enable (LE) must remain low at least one clock cycle after going negative. (4) Latch Enable (LE) must be high for at least one clock cycle before going negative. (5) I_{OUT} changes on negative going edge of Latch Enable (LE).

FIGURE 2. Timing Diagram.

INSTALLATION

POWER SUPPLIES

Refer to Figure 4 for proper connection of the PCM63P in the voltage-out mode using the internal feedback resistor. The feedback resistor connections (P9 and P10) should be left open if not used. The PCM63P only requires a ±5V supply. Both positive supplies should be tied together at a single point. Similarly, both negative supplies should be connected together. No real advantage is gained by using separate analog and digital supplies. It is more important that both these supplies be as "clean" as possible to reduce coupling of supply noise to the output. Power supply decoupling capacitors should be used at each supply pin to maximize power supply rejection, as shown in Figure 4, regardless of how good the supplies are. Both commons should be connected to an analog ground plane as close to the PCM63P as possible.

FILTER CAPACITOR REQUIREMENTS

As shown in Figure 4, various size decoupling capacitors can be used, with no special tolerances being required. The size of the offset decoupling capacitor is not critical either, with larger values (up to 100µF) giving slightly better SNR readings. All capacitors should be as close to the appropriate pins of the PCM63P as possible to reduce noise pickup from surrounding circuitry.

MSB ADJUSTMENT CIRCUITRY

Near optimum performance can be maintained at all signal levels without using the optional MSB adjust circuitry of the PCM63P shown in Figure 5. Adjustability is provided for those cases where slightly better full-scale THD + N is desired. Use of the MSB adjustments will only affect larger dynamic signals (between 0dB and –6dB). This improvement comes from bettering the gain match between the upper and lower DACs at these signal levels. The change is realized by small adjustments in the bit-2 weights of each DAC. Great care should be taken, however, as improper adjustment will easily result in degraded performance.

In theory, the adjustments would seem very simple to perform, but in practice they are actually quite complex. The first step in the theoretical procedure would involve making each bit-2 weight ideal in relation to its code minus one value (adjusting each potentiometer for zero differential nonlinearity error at the bit-2 major carries). This would be the starting point of each 100kΩ potentiometer for the next adjustment. Then, each potentiometer would be adjusted equally, in opposite directions, to achieve the lowest full-scale THD + N possible (reversing the direction of rotation

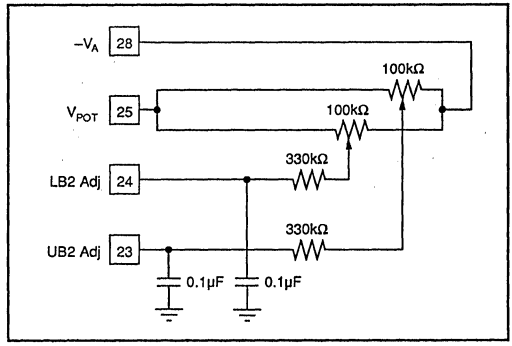


FIGURE 5. Optional Bit-2 Adjustment Circuitry.

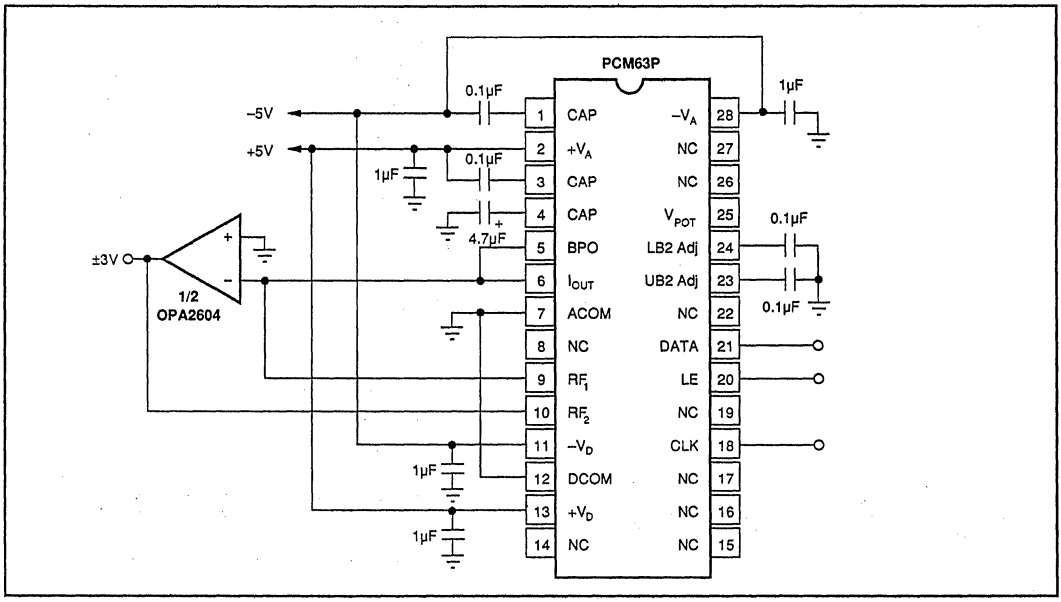


FIGURE 4. Connection Diagram.

for both if no immediate improvement were noted). This procedure would require the generation of the digital bit-2 major carry code to the input of the PCM63P and a DVM or oscilloscope capable of reading the output voltage for a one LSB step (5.72μV) in addition to a distortion analyzer.

A more practical approach would be to forego the minor correction for the bit-2 major carry adjustment and only adjust for upper and lower DAC gain matching. The problem is that just by connecting the MSB circuitry to the PCM63P, the odds are that the upper and lower bit-2 weights would be greatly changed from their unadjusted states and thereby adversely affect the desired gain adjustment. Just centering the 100kΩ potentiometers would not necessarily provide the correct starting point. To guarantee that each 100kΩ potentiometer would be set to the correct starting or null point (no current into or out of the MSB adjust pins), the voltage drop across each corresponding 330kΩ resistor would have to measure 0V. A voltage drop of ±1.25mV across either 330kΩ resistor would correspond to a ±1LSB change in the null point from its unadjusted state (1LSB in current or 3.81nA x 330kΩ = 1.26mV). Once these starting points for each potentiometer had been set, each potentiometer would then be adjusted equally, in opposite directions, to achieve the lowest full-scale THD + N possible. If no immediate improvement were noted, the direction of rotation for both potentiometers would be reversed. One direction of potentiometer counter-rotations would only make the gain mismatch and resulting THD + N worse, while the opposite would gradually improve and then worsen the THD + N after passing through a no mismatch point. The determination of the correct starting direction would be arbitrary. This procedure still requires a good DVM in addition to a distortion analyzer.

Each user will have to determine if a small improvement in full-scale THD + N for their application is worth the expense of performing a proper MSB adjustment.

APPLICATIONS

The most common application for the PCM63P is in high-performance and professional digital audio playback, such as in CD and DAT players. The circuit in Figure 6 shows the PCM63P in a typical combination with a digital interface format receiver chip (Yamaha YM3623), an 8X interpolating digital filter (Burr-Brown DF1700P), and two third-order low-pass anti-imaging filters (implemented using Burr-Brown OPA2604APs).

Using an 8X digital filter increases the number of samples to the DAC by a factor of 8, thereby reducing the need for a higher order reconstruction or anti-imaging analog filter on the DAC output. An analog filter can now be constructed using a simple phase-linear GIC (generalized immittance converter) architecture. Excellent sonic performance is achieved using a digital filter in the design, while reducing overall circuit complexity at the same time.

Because of its superior low-level performance, the PCM63P is also ideally suited for other high-performance applications such as direct digital synthesis (DDS).

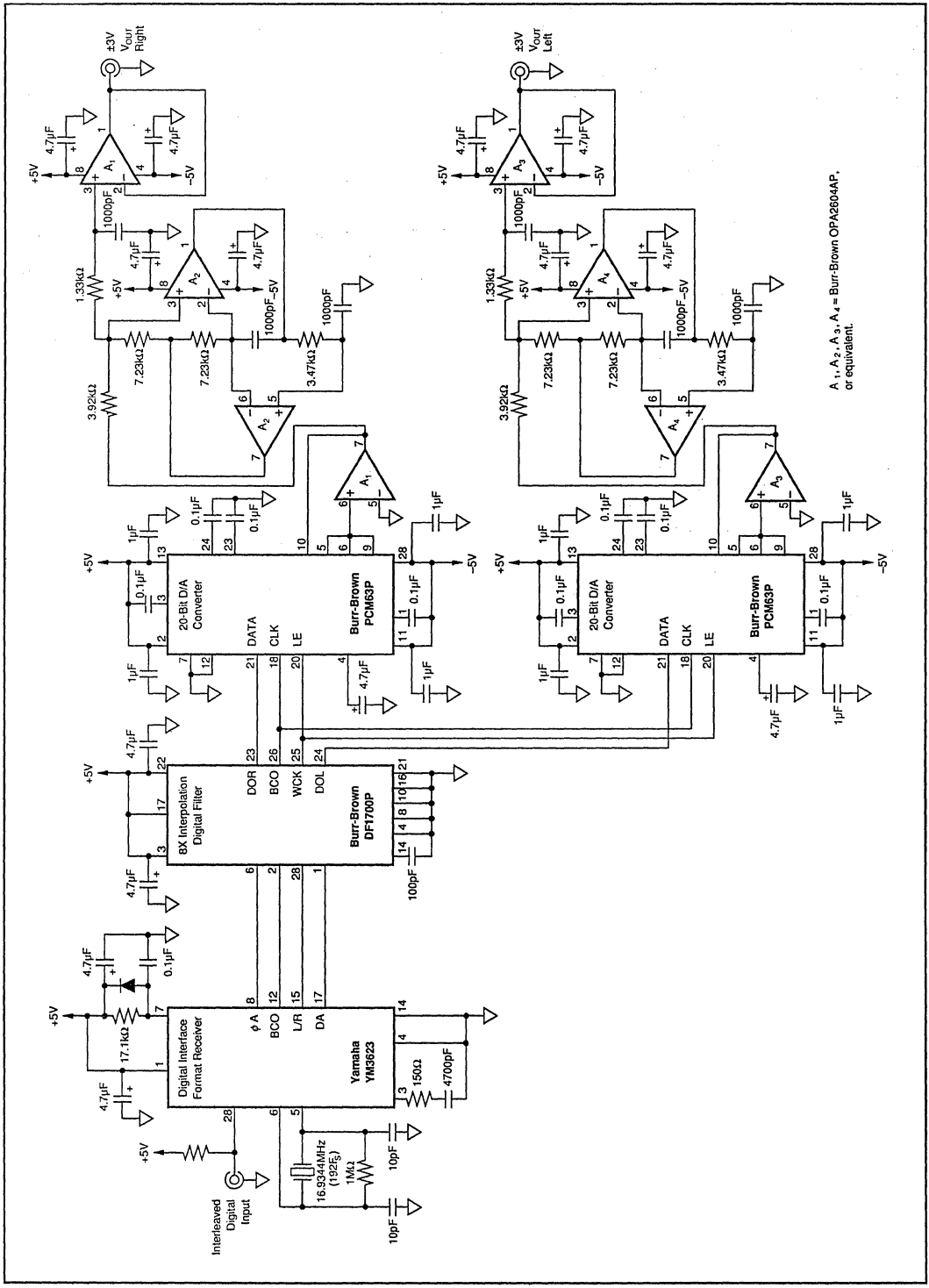
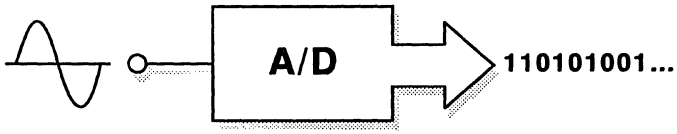


FIGURE 6. Stereo Audio Application.



ANALOG-TO-DIGITAL CONVERTERS

The Burr-Brown Analog-to-Digital (A/D) converter product line offers a broad selection of devices that enable you to choose the performance and price range ideally suited for your application. For example, the high-performance 12-bit ADC80, which converts to 12-bit accuracy in 25µs, was originated by Burr-Brown in 1975 and has become an industry standard. The recently introduced ADC603 is a 12-bit, 10MHz A/D converter that offers the industry's highest performance for RF signal processing applications. A high-resolution converter, the ADC76, converts 16 bits to ±0.003% absolute accuracy in only 15µs and is packaged in a 32-pin triple-wide dual-in-line package. Another performance category is total harmonic distortion for audio digital recording.

All devices are complete and fully specified, with a track record of high reliability proven both in the field as well as in internal qualification testing.

ANALOG-TO-DIGITAL CONVERTERS SELECTION GUIDES

The Selection Guide shows parameters for the high grade. Refer to the Product Data Sheet for a full selection of grades. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book.*

INSTRUMENTATION ANALOG-TO-DIGITAL CONVERTERS — **Boldface = NEW**

Description	Model	Resolution (Bits)	Linearity Error (%FSR)	Input Range (V)[1]	Conversion Time or Sampling Rate (µs)	NMC Resolution	Temp Range[2]	Pkg[3]	Q, BI[4] Screen	Page No.
Data-Bus Interface	**ADC700**	**16**	**±0.003**	**5, 10, 20 U/B**	**17**	**14**	**Mil, Ind, Com**	**TDIP**	**—**	**9.1-72**
Industry Std Pinouts	**ADC71**	**16**	**±0.003**	**5, 10, 20 U/B**	**50**	**14**	**Ind, Com**	**TDIP**	**—**	**S9.1-4**
	ADC76	**16**	**±0.003**	**5, 10, 20 U/B**	**17**	**14**	**Ind, Com**	**TDIP**	**—**	**S9.1-12**
Sampling 574 Type	**ADS574**	**12**	**±0.012**	**10, 20, U/B**	**40kHz**	**12**	**Ind**	**DIP, DDIP SO**	**—**	**S9.1-42**
Sampling 774 Type	**ADS774**	**12**	**±0.012**	**10, 20, U/B**	**100kHz**	**12**	**Ind**	**DIP, DDIP SO**	**—**	**S9.1-42**
Sampling, Interface	**ADS7800**	**12**	**±0.012**	**10, 20 B**	**333kHz**	**12**	**Com, Ind**	**DIP SO**	**—**	**S9.1-72**
High-Accuracy, 4-Channel, Auto-Calibration, Sampling	**ADS7802**	**12**	**±0.012**	**0 to +5**	**8.5**	**12**	**Ind**	**DDIP, PLCC**	**—**	**S9.1-153**
Industry Std Pinout and Interface	ADC574A	12	±0.012	10, 20 U/B	25	12	Mil,Ind,Com	DDIP	BI	9.1-52
	ADC674A	12	±0.012	10, 20 U/B	15	12	Mil,Ind,Com	DDIP	BI	9.1-62
	ADC774	12	±0.012	10, 20 U/B	8	12	Mil,Ind,Com	DDIP	BI	9.1-32
Sampling	**ADS807**	**12**	**±0.012**	**10, 20 U/B**	**100kHz**	**12**	**Mil,Ind,Com**	**DDIP**	**BI**	**S9.1-59**
Sampling	**ADS808**	**12**	**±0.012**	**10, 20 U/B**	**100kHz**	**12**	**Mil,Ind,Com**	**DDIP**	**BI**	**S9.1-59**
Medium Speed Monolithic	ADC80AG	12	±0.012	5, 10, 20 U/B	25	12	Ind	TDIP	BI	9.1-20
	ADC80MAH	12	±0.012	5, 10, 20 U/B	25	12	Ind	TDIP	BI	9.1-36
Medium Speed	ADC84KG	12	±0.012	5, 10, 20 U/B	10	12	Ind	TDIP	BI	9.1-44
	ADC85H	12	±0.012	5, 10, 20 U/B	10	12	Com	TDIP	Q, BI	9.1-44
Mil Temperature Range	ADC87H	12	±0.012	5, 10, 20 U/B	10	12	Mil	TDIP	Q	9.1-44
Serial Output	ADC804	12	±0.012	5,10,20 U/B	17	12	Mil,Ind,Com	DDIP	Q, BI	9.1-78

NOTES: (1) U/B indicates the input voltage range for the model: U = unipolar, B = Bipolar. (2) Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (3) DIP = 0.3" wide DIP, DDIP = 0.6" wide DIP, TDIP = 0.9" wide DIP, PLCC = Plastic Leaded Chip Carrier, SO = Small Outline Surface Mount. (4) Q indicates optional reliability screening is available for this model. BI indicates that an optional 160 hour burn-in is available for this model.

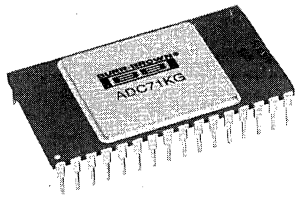
AUDIO, COMMUNICATIONS, DSP ANALOG-TO-DIGITAL CONVERTERS — **Boldface = NEW**

Description	Model	Resolution (Bits)	Linearity Error, max(%FSR)	Input Range (V)	Conversion Time or Sampling Rate (µs)	THD (dB, typ)	Temp Range[1]	Pkg[2]	Q[3] Screen	Page No.
High Accuracy, High Resolution	**ADC701**	16	±0.003	10V/20V	1.5	94w/SHC702	Com	TDIP	—	S9.2-137
Sampling, High-Resolution	**ADC614**	14	±0.003	±1.25	5MHz	76	Com	DIP	—	S9.2-134
	ADC603	12	±0.018	±1.25	10MHz	68	Com, Mil	DIP	—	S9.2-99
High Spurious-Free Range	**ADC604**	12	±0.024	±1.25	5MHz	83	Com	DIP	—	S9.2-119
	ADC803	12	±0.012	10V/20V	1.5	NA	Ind, Mil	TDIP	—	9.2-124
	ADC601	12	±0.012	10V/20V	1.0	70w/SHC802	Com	TDIP		S9.2-83
Sampling	**ADS602**	12	±0.03	10V/20V	1MHz	66	Com	TDIP	—	S9.1-51

Description	Model	Resolution (Bits)	Typical Linearity Error	Input Range (V)	Time or Sampling Rate (µs)	THD+N dB, max (V_{IN} = ±FS)	Output Format	Pkg[1]	Page No.[4]
High Performance	PCM75	16	15-Bit 14-Bit	±2.5, ±5 ±10V	17	–84 (J) –88 (K)	Parallel or Serial	TDIP	9.2-136
Low Cost	**PCM78**	16	14-Bit	±3	5	–88	Serial	DDIP	S9.2-165
Dual	**PCM1750**	18	14-Bit	±2.75	5	–90 (P)	Serial	DDIP	S9.2-187
Single Channel	**DSP101**	18	14-Bit	±2.75	5	–90	Serial	DDIP	S14-4
Dual Channel	**DSP102**	18	14-Bit	±2.75	5	–90	Serial	DDIP	S14-4

NOTES: (1) DIP = 0.3" wide DIP, DDIP = 0.6" wide DIP, TDIP = 0.9" wide DIP, PLCC = Plastic Leaded Chip Carrier, SO = Small Outline Surface Mount.

BURR-BROWN®



ADC71

NEW HERMETIC PACKAGE!

16-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

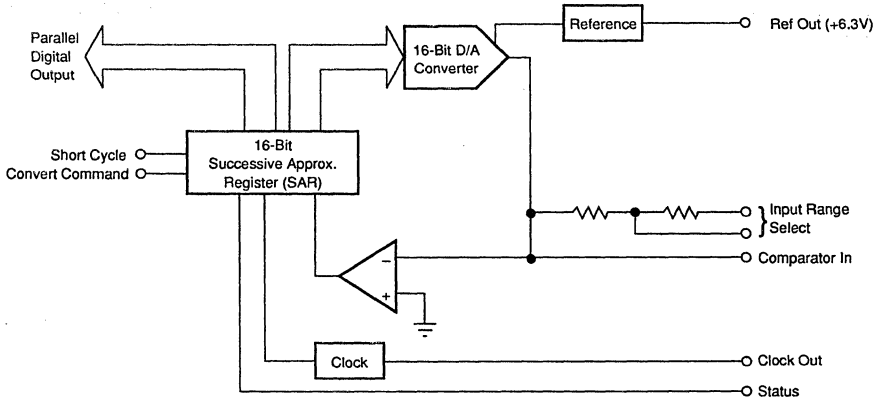
- **16-BIT RESOLUTION**
- **±0.003% MAXIMUM NONLINEARITY**
- **COMPACT DESIGN: 32-pin Hermetic Ceramic Package**
- **CONVERSION SPEED: 50µs max**
- **LOW COST**

DESCRIPTION

The ADC71 is a low cost, high quality, 16-bit successive approximation analog-to-digital converter. It uses laser-trimmed ICs and is packaged in a convenient 32-pin hermetic ceramic dual-in-line package. The converter is complete with internal reference, clock, comparator, and thin-film scaling resistors, which allow selection of analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V.

Data is available in parallel and serial form with corresponding clock and status output. All digital inputs and outputs are TTL-compatible.

Power supply voltages are ±15VDC and +5VDC.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1060

SPECIFICATIONS

ELECTRICAL

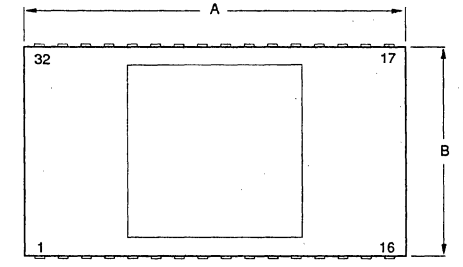
At +25°C and rated power supplies unless otherwise noted.

MODEL	ADC71J, K MIN	ADC71J, K TYP	ADC71J, K MAX	ADC71A, B MIN	ADC71A, B TYP	ADC71A, B MAX	UNITS
RESOLUTION			16			16	Bits
INPUTS							
ANALOG							
Voltage Ranges: Bipolar		±2.5, ±5, ±10			±2.5, ±5, ±10		V
Unipolar		0 to +5, 0 to +10, 0 to +20			0 to +5, 0 to +10, 0 to +20		V
Input Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			2.5		kΩ
0 to +10V, ±5.0V		5			5		kΩ
0 to +20V, ±10V		10			10		kΩ
DIGITAL[1]	Convert Command Positive pulse 50ns wide (min) trailing edge ("1" to "0" initiates conversion)						
Logic Loading			1				TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error[2]		±0.1	±0.2		±0.1	±0.2	%
Offset[2]: Unipolar		±0.05	±0.1		±0.05	±0.1	% of FSR[3]
Bipolar		±0.1	±0.2		±0.1	±0.2	% of FSR
Linearity Error: K, B			±0.003			±0.003	% of FSR
J, A			±0.006			±0.006	% of FSR
Inherent Quantization Error		±1/2			±1/2		LSB
Differential Linearity Error		±0.003			±0.003		% of FSR
POWER SUPPLY SENSITIVITY							
±15VDC		0.003			0.003		% of FSR/%V_S
+5VDC		0.001			0.001		% of FSR/%V_S
CONVERSION TIME[4]							
14 Bits			50			50	µs
WARM-UP TIME	5			•			min
DRIFT							
Gain		±10	±15		•	•	ppm/°C
Offset: Unipolar		±2	±4			±2	ppm of FSR/°C
Bipolar		±8	±10		±5	±10	ppm of FSR/°C
Linearity		±2	±3			±2	ppm of FSR/°C
No Missing Codes Temp Range							
J, A (13-Bits)	0		+70	–25		+85	°C
K, B (14-Bits)	0		+70	–25		+85	°C
OUTPUT							
DIGITAL DATA							
(All Codes Complementary)							
Parallel Output Codes[5]: Unipolar		CSB					
Bipolar		COB, CTC[6]					
Output Drive			2			•	TTL Loads
Serial Data Code (NRZ)		CSB, COB					
Output Drive			2			•	TTL Loads
Status		Logic "1" During Conversion					
Status Output Drive			2			2	TTL Loads
Clock Output Drive			2			2	TTL Loads
Frequency[7]		280			•		kHz
INTERNAL REFERENCE VOLTAGE	6.0	6.3	6.6	6.0	6.3	6.6	V
Max External Current with							
No Degradation of Specs			±200			±200	µA
Temp Coefficient			±10			•	ppm/°C
POWER SUPPLY REQUIREMENTS							
Power Consumption		655			655		mW
Rated Voltage, Analog	±11.4	±15	±16	•	•	•	VDC
Rated Voltage, Digital	+4.75	+5	+4.75	•	•	•	VDC
Supply Drain +15VDC		+10	+15		•	•	mA
Supply Drain –15VDC		–28	–35		•	•	mA
Supply Drain +5VDC		+17	+20		•	•	mA
TEMPERATURE RANGE							
Specification	0		+70	–25		+85	°C
Operating (Derated Specs)	–25		+85	–55		+125	°C
Storage	–55		+125	–55		+125	°C

NOTES: (1) CMOS/TTL compatible, i.e., Logic "0" = 0.8V, max Logic "1" = 2.0V, min for inputs. for digital outputs Logic "0" = +0.4V, max Logic "1" = 2.4V min. (2) Adjustable to zero. (3) FSR means Full Scale Range. for example, unit connected for ±10V range has 20V FSR. (4) Conversion time may be shortened with "Short Cycle" set for lower resolution, see "Additional Connections Required" section. (5) See Table I. CSB - Complementary Straight Binary. COB - Complementary Offset Binary. CTC - Complementary Two's Complement. (6) CTC coding obtained by inverting MSB (Pin 1).

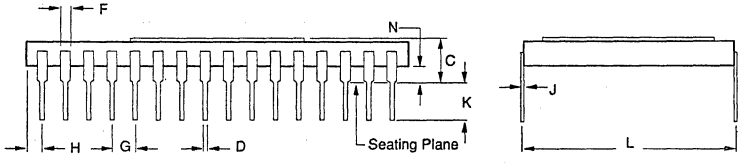
MECHANICAL

G Package — 32-Pin Hermetic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.580	1.620	40.13	41.15
B	.880	.900	22.35	22.86
C	.138	.186	3.51	4.72
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.900	.920	22.86	23.37
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.



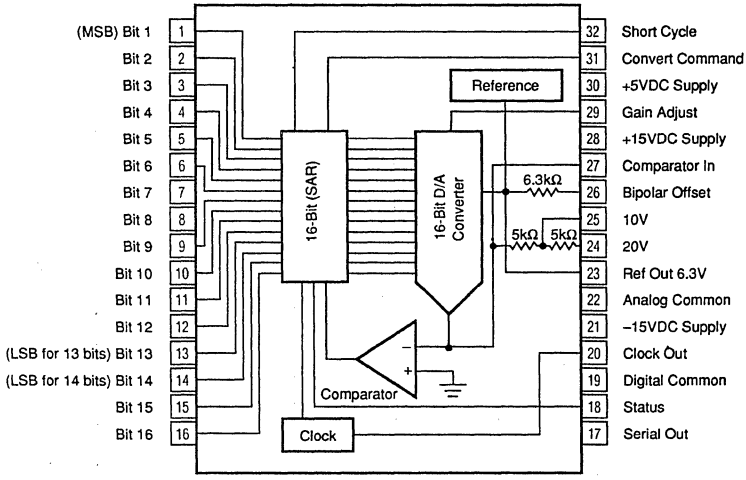
ABSOLUTE MAXIMUM SPECIFICATIONS

$+V_{CC}$ to Common	0 to +16.5V
$-V_{CC}$ to Common	0V to –16.5V
$+V_{DD}$ to Common	0V to +7V
Analog Common to Digital Common	±0.5V
Logic Inputs to Common	0V to V_{DD}
Maximum Power Dissipation	1000mW
Lead Temperature (10s)	300°C

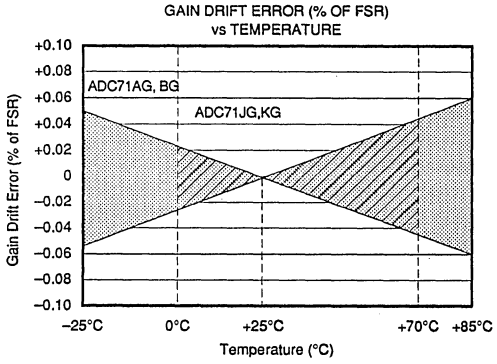
ORDERING INFORMATION

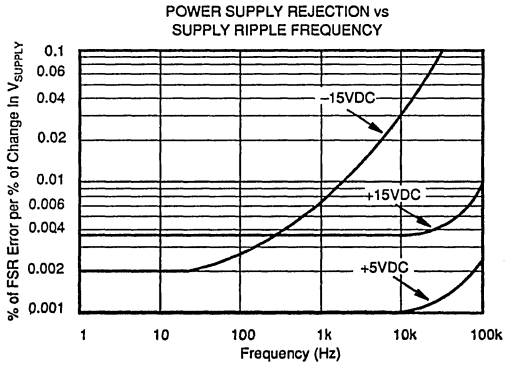
MODEL	TEMP RANGE	NONLINEARITY
ADC71JG	0°C to +70°C	±0.006% FSR
ADC71KG	0°C to +70°C	±0.003% FSR
ADC71AG	–25°C to +85°C	±0.006% FSR
ADC71BG	–25°C to +85°C	±0.003% FSR

PIN CONFIGURATION



TYPICAL PERFORMANCE CURVES





DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2 LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2 LSB means that the width of each bit step over the range of the A/D converter is 1 LSB, ±1/2 LSB.

The ADC71 is monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown guarantees that these converters will have no missing codes over a specified temperature range when short-cycled for 14-bit operation.

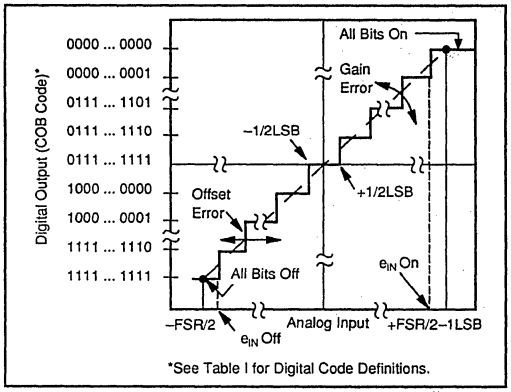


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

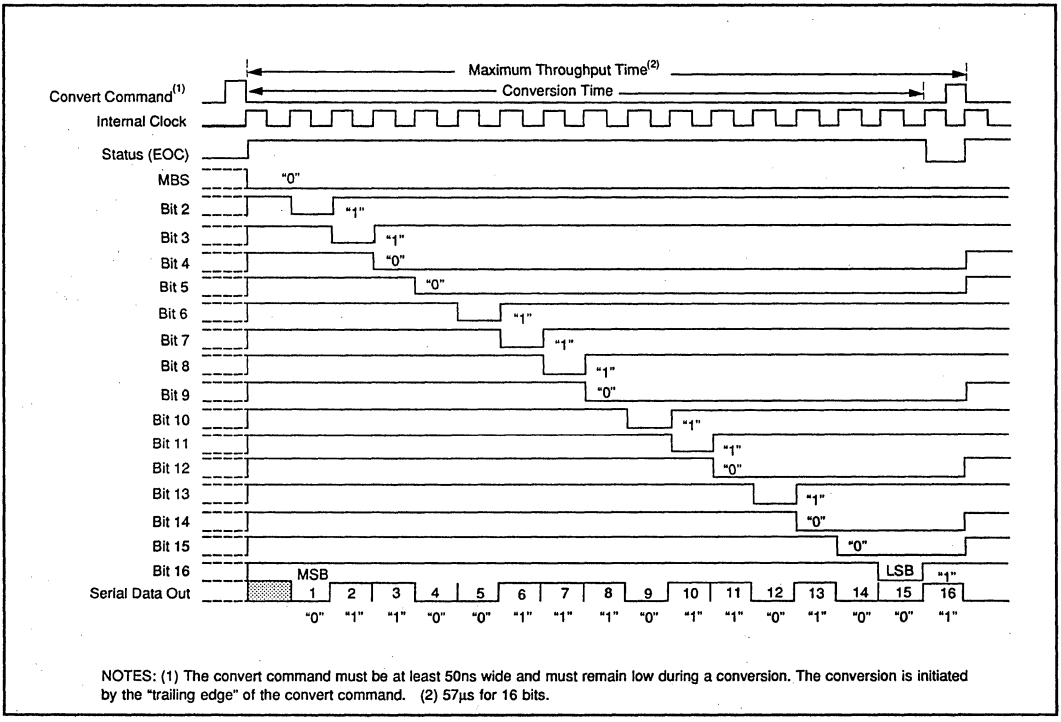
The timing diagram (Figure 2) assumes an analog input such that the positive true digital word 1001 1000 1001 0110 exists. The output will be complementary as shown in Figure 2 (0110 0111 0110 1001 is the digital output). Figures 3 and 4 are timing diagrams showing the relationship of serial data to clock and valid data to status.

DEFINITION OF DIGITAL CODES

PARALLEL DATA

Two binary codes are available on the ADC71 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary offset binary (COB) for bipolar input signal ranges. Complementary two's complement (CTC) may be obtained by inverting MSB (Pin 1).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 12-, 13- and 14-bit resolutions. Figure 5 shows the connections for 14-bit resolution, parallel data output, with ±10V input.



NOTES: (1) The convert command must be at least 50ns wide and must remain low during a conversion. The conversion is initiated by the "trailing edge" of the convert command. (2) 57µs for 16 bits.

FIGURE 2. ADC71 Timing Diagram.

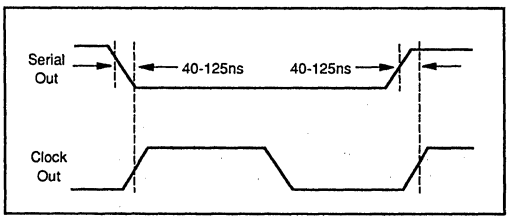


FIGURE 3. Timing Relationship of Serial Data to Clock.

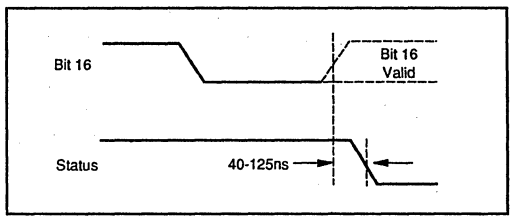


FIGURE 4. Timing Relationship of Valid Data to Status.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB(1) or CTC(2)	COB(1) or CTC(2)	COB(1) or CTC(2)	CSB(3)	CSB(3)	CSB(3)
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV	4.88mV
	n = 13	2.44mV	1.22mV	610µV	1.22mV	610µV	2.44mV
	n = 14	1.22mV	610µV	305µV	610µV	305µV	1.22mV
Transition Values MSB LSB							
000 ... 000(4)	+Full Scale	+10V–3/2LSB	+5V–3/2LSB	+2.5V–3/2LSB	+10V–3/2LSB	+5V–3/2LSB	+20V–3/2LSB
011 ... 111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111 ... 110	–Full Scale	–10V +1/2LSB	–5V +1/2LSB	–2.5V +1/2LSB	0 +1/2LSB	0 +1/2LSB	0 +1/2LSB

NOTES: (1) COB = Complementary Offset Binary. (2) Complementary Two's Complement—obtained by inverting the most significant bit MSB (pin 1). (3) CSB = Complementary Straight Binary. (4) Voltages given are the nominal value for transition to the code specified.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

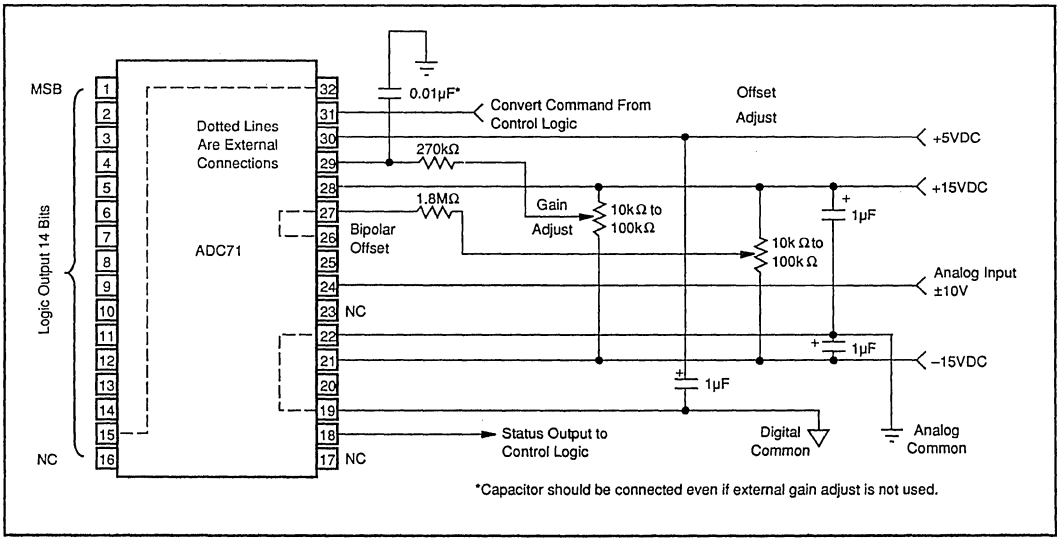


FIGURE 5. ADC71 Connections for: ±10V Analog Input, 14-Bit Resolution (Short-Cycled), Parallel Data Output.

SERIAL DATA

Two straight binary (complementary) codes are available on the serial output line: CSB and COB. The serial data is available only during conversion and appears with MSB occurring first. The serial data is synchronous with the internal clock as shown in the timing diagrams of Figures 2 and 3. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

DISCUSSION OF SPECIFICATIONS

The ADC71 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors. This ADC is factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to typically ±0.1% of FSR (typically ±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 6 and 7.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The power supply sensitivity is specified for ±0.003% of FSR/%ΔV_S for±15V supplies and ±0.001% of FSR/%Δ_S for +5 supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling and Figure 8.

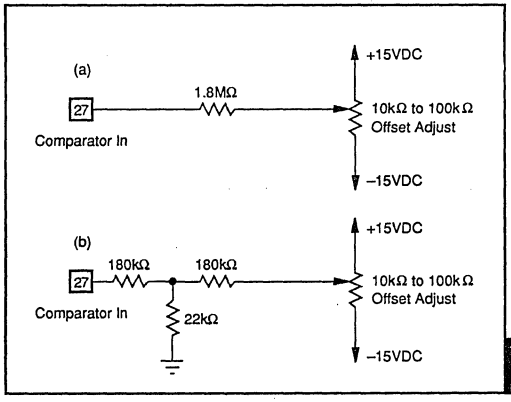


FIGURE 6. Two Methods of Connecting Optional Offset Adjust with a 0.4% of FSR of Adjustment.

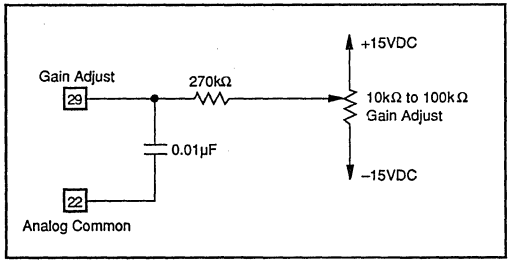


FIGURE 7. Connecting Optional Gain Adjust with a 0.2% Range of Adjustment.

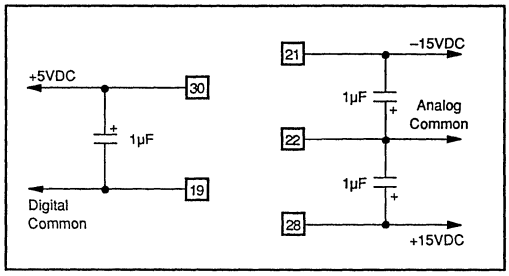


FIGURE 8. Recommended Power Supply Decoupling.

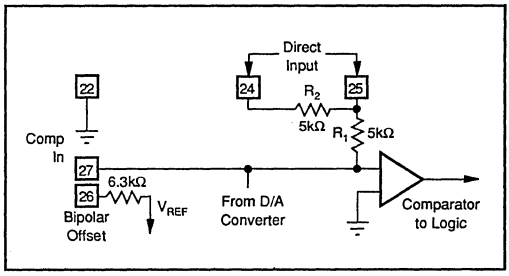


FIGURE 9. ADC71 Input Scaling Circuit.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital common are not connected internally in the ADC71 but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor patterns and a 0.01µF to 0.1µF non-polarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital commons returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The comparator input (Pin 27) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by Analog Common patterns.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum capacitors as shown in Figure 8 to obtain noise free operation. These capacitors should be located close to the ADC.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 9 for circuit details.

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Input Signal To Pin
±10V	COB or CTC*	27	Input Signal	24
±5V	COB or CTC*	27	Open	25
±2.5V	COB or CTC*	27	Pin 27	25
0 to +5V	CSB	22	Pin 27	25
0 to +10V	CSB	22	Open	25
0 to +20V	CSB	22	Input Signal	24

*Obtained by inverting MSB pin 1.

TABLE II. ADC71 Input Scaling Connections.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figure 6 and 7. Multiturn potentiometers with 100ppm/°C or better TCRs are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 29 (Gain Adjust) and Pin 27 (Offset Adjust) may be left open of no external adjustment is required.

ADJUSTMENT PROCEDURE

OFFSET — Connect the Offset potentiometer (make sure R_1 is as close to pin 27 as possible) as shown in Figure 6. Sweep the input through the end point transition voltage that should cause an output transition to all bits Off (E_{IN}).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}. The ideal transition voltage values of the input are given in Table I.

GAIN — Connect the Gain Adjust potentiometer as shown in Figure 7. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}.

Table I details the transition voltage levels required.

CONVERT COMMAND CONSIDERATIONS

Convert command resets the converter whenever taken high. This insures a valid conversion on the first conversion after power-up.

Convert command must stay low during a conversion unless it is desired to reset the converter during a conversion.

ADDITIONAL CONNECTIONS REQUIRED

The ADC71 may be operated at faster speeds by connecting the Short-Cycle Input, pin 32, as shown in Table III. Conversion speeds, linearity, and resolutions are shown for reference.

OUTPUT DRIVE

Normally all ADC71 logic outputs will drive two standard TTL loads; however, if long digital lines must be driver, external logic buffers are recommended.

HEAT DISSIPATION

The ADC71 dissipates approximately 0.6W (typical) and the packages have a case-to-ambient thermal resistance (θ_{CA}) of 25°C/W. For operation above 85°C, θ_{CA} should be lowered by a heat sink or by forced air over the surface of the package. See Figure 10 for θ_{CA} requirement above 85°C. If the converter is mounted on a PC card, improved thermal contact with the copper ground plane under the case can be achieved using a silicone heat sink compound. On a 0.062" thick PC card with a 16 square in (min) area, this techniques will allow operation to 85°C.

Resolution (Bits)	16	14	13	12
Connect Pin 32 to	Open	Pin 15	Pin 14	Pin 13
Maximum Conversion Speed (µs)[1]	57	50	46.5	43
Maximum Nonlinearity at 25°C (% of FSR)	0.003[2]	0.003[2]	0.006	0.006

NOTES: (1) Max conversion time to maintain specified nonlinearity error. (2) BH and KH models only.

TABLE III. Short-Cycle Connections and Specifications for 12- to 14-Bit Resolutions.

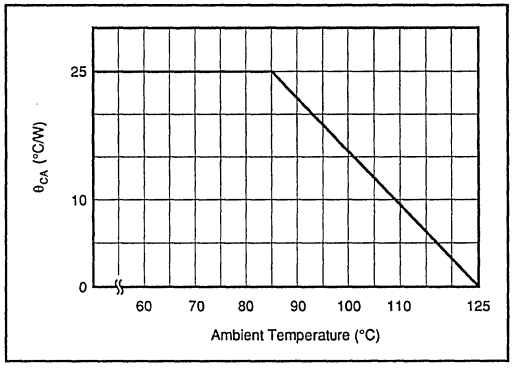


FIGURE 10. θ_{CA} Requirement Above 85°C.

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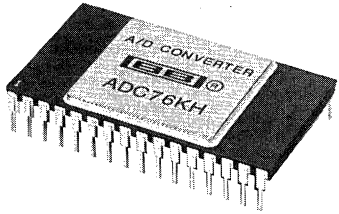


ADC76

NEW HERMETIC PACKAGE!

16-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **COMPACT DESIGN: 32-Pin Hermetic Side-Brazed Package**
- **16-BIT RESOLUTION**
- **LINEARITY ERROR ±0.003% max (KH, BH)**
- **NO MISSING CODES GUARANTEED FROM –25°C TO +85°C**
- **17µs CONVERSION TIME (16-Bit)**
- **SERIAL AND PARALLEL OUTPUTS**
- **LOW COST**

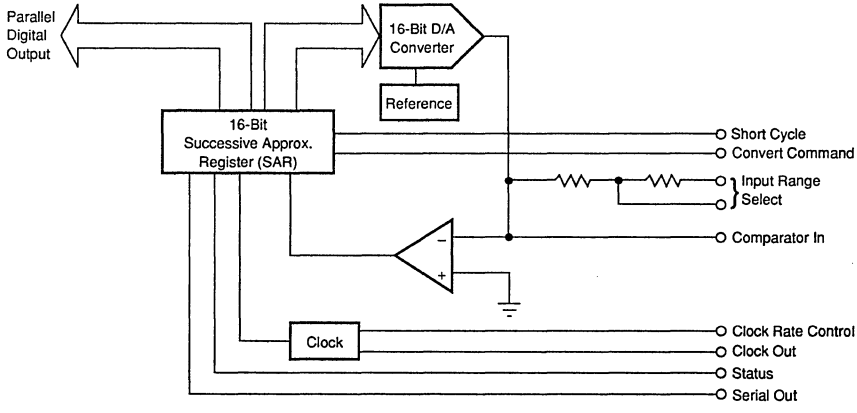
DESCRIPTION

The ADC76 is a low cost, high quality, 16-bit successive approximation analog-to-digital converter. The ADC76 uses state-of-the-art laser-trimmed IC thin-film resistors and is packaged in a hermetic 32-pin dual-in-line package. The converter is complete with internal reference, short cycling capabilities, serial output, and thin-film scaling resistors, which allow selection of analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V.

It is specified for operation over two temperature ranges: 0°C to +70°C (J, K) and –25°C to +85°C (A, B).

Data is available in parallel and serial form with corresponding clock and status output. All digital inputs and outputs are TTL-compatible.

Power supply voltages are ±15VDC and +5VDC.



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PDS-1063

SPECIFICATIONS

ELECTRICAL

At +25°C and rated power supplies unless otherwise noted.

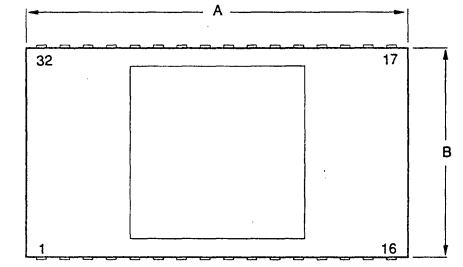
	ADC76J, K			ADC76A, B			
MODEL	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
RESOLUTION			16			*	Bits
ANALOG INPUTS							
Voltage Ranges: Bipolar		±2.5, ±5, ±10			*		V
Unipolar		0 to +5, 0 to +10			*		V
		0 to +20			*		
Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			*		kΩ
0 to +10V, ±5.0V		5			*		kΩ
0 to +20V, ±10V		10			*		kΩ
DIGITAL INPUTS[1]							
Convert Command		Positive pulse 50ns wide (min) trailing edge ("1" to "0" initiates conversion)					
Logic Loading			1			*	TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error[2]		±0.1	±0.2		*	*	%
Offset Error: Unipolar[2]		±0.05	±0.1		*	*	% of FSR[3]
Bipolar[2]		±0.1	±0.2		*	*	% of FSR
Linearity Error: K, B			±0.003			*	% of FSR
J, A			±0.006			*	% of FSR
Inherent Quantization Error		±1/2			*		LSB
Differential Linearity Error		±0.003			*		% of FSR
Noise (3σ, p-p)		±0.001	±0.003		*	*	% of FSR
POWER SUPPLY SENSITIVITY							
±15VDC		0.003			*		% of FSR/%V_s
+5VDC		0.001			*		% of FSR/%V_s
CONVERSION TIME[4]							
14 Bits			15			*	µs
15 Bits			16			*	µs
16 Bits			17			*	µs
WARM-UP TIME	5			*			Min
DRIFT							
Gain			±15			*	ppm/°C
Offset: Unipolar		±2	±4		*	*	ppm of FSR/°C
Bipolar			±10			*	ppm of FSR/°C
Linearity		±2	±3		*	*	ppm of FSR/°C
No Missing Codes Temp Range							
J, A (13-bit)	0		+70	–25		+85	°C
K, B (14-bit)	0		+70	–25		+85	°C
OUTPUT DIGITAL DATA							
(All codes complementary)							
Parallel							
Output Codes[5]: Unipolar		CSB			*		
Bipolar		COB, CTC[6]			*		
Output Drive			2			*	TTL Loads
Serial Data Code (NRZ)		CSB, COB			*		
Output Drive			2			*	TTL Loads
Status		Logic "1" during conversion			*		
Status Output Drive			2			*	TTL Loads
Internal Clock: Clock Output Drive			2			*	TTL Loads
Frequency[7]	933		1400	*		*	kHz
POWER SUPPLY REQUIREMENTS							
Power Consumption		0.655			*		W
Rated Voltage: Analog	±11.4	±15	±16	*	*	*	VDC
Digital	+4.75	+5	+5.25	*	*	*	VDC
Supply Drain: +15VDC		+10	+15		*	*	mA
–15VDC		–28	–35		*	*	mA
+5VDC		+17	+20		*	*	mA
TEMPERATURE RANGE							
Specification	0		+70	–25		+85	°C
Storage	–55		+125	*		*	°C

*Specification same as ADC76J, K.

NOTES: (1) CMOS/TTL compatible, i.e., Logic "0" = 0.8V, max, Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = 0.4V, max, Logic "1' = 2.4V, min. (2) Adjustable to zero. See "Optional External Gain and Offset Adjustment" section. (3) FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR. (4) Conversion time may be shortened with "Short Cycle" set for lower resolution and with use of Clock Rate Control. See "Optional Conversion Time Adjustment" section. The Clock Rate Control (pin 23) should be connected to Digital Common for specified conversion time. Short Cycle (pin 32) should be left open for 16-bit resolution or connected to the n + 1 digital output for n-bit resolution. For example, connect Short Cycle to Bit 15 (pin 15) for 14-bit resolution. For resolutions less than 16 bits, pin 32 should also be tied to +5V through a 2kΩ resistor. (5) See Table I. CSB—Complementary Straight Binary, COB—Complementary Offset Binary, CTC—Complementary Two's Complement. (6) CTC coding obtained by inverting MSB (pin 1). (7) Adjustable with Clock Rate Control from approximately 933kHz to 1.4MHz. See Figures 12 and 13 and Table III.

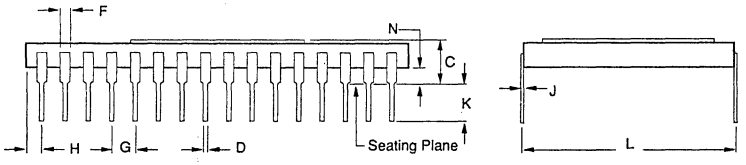
MECHANICAL

G Package — 32-Pin Hermetic DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.580	1.620	40.13	41.15
B	.880	.900	22.35	22.86
C	.138	.186	3.51	4.72
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.900	.920	22.86	23.37
N	.040	.060	1.02	1.52

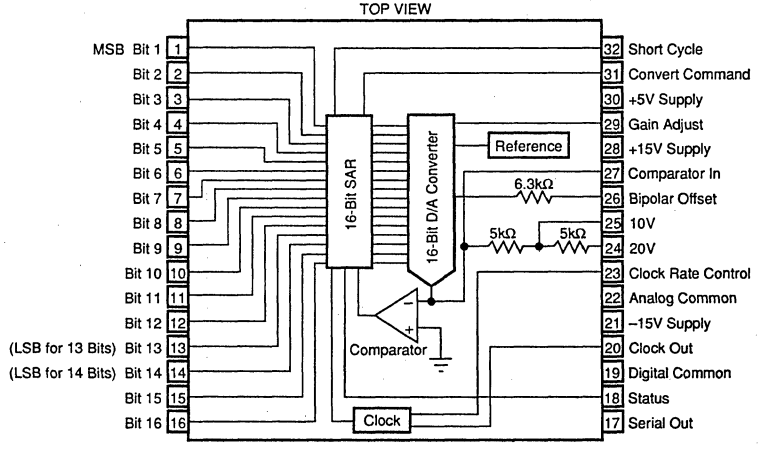
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.



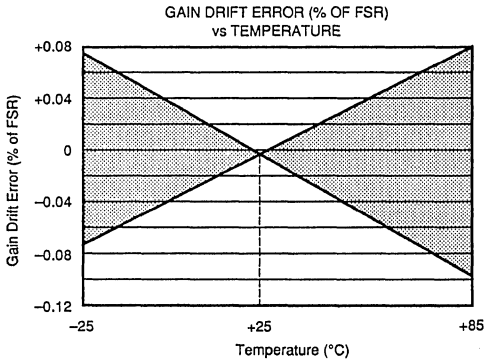
ABSOLUTE MAXIMUM SPECIFICATIONS

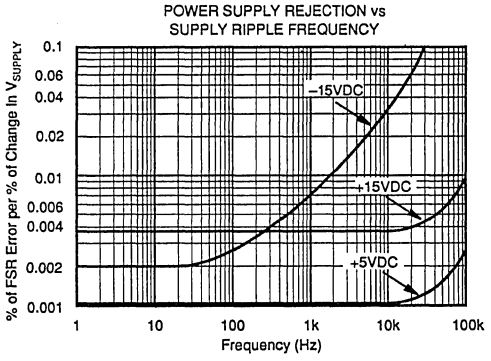
$+V_{CC}$ to Common	0 to +16.5V
$-V_{CC}$ to Common	0V to –16.5V
$+V_{DD}$ to Common	0V to +7V
Analog Common to Digital Common	±0.5V
Logic Inputs to Common	0V to V_{DD}
Maximum Power Dissipation	1000mW
Lead Temperature (10s)	300°C

PIN CONFIGURATION



TYPICAL PERFORMANCE CURVES





THEORY OF OPERATION

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent quantization error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure I) about the zero or minus full scale point (all bits Off) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A differential linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB, ±1/2LSB.

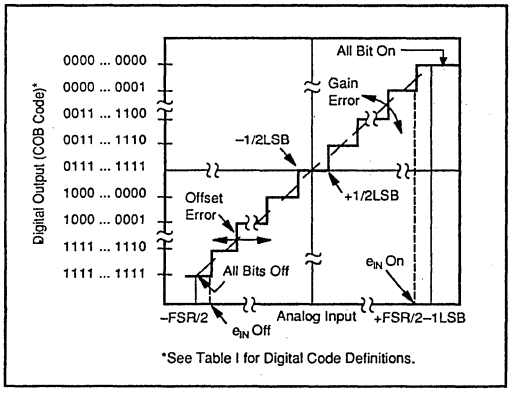


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

The ADC76 is also monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also guarantees that this converter will have no missing codes over a specified temperature range when short cycled for 14-bit operation

TIMING CONSIDERATIONS

The timing diagram in Figure 2 assumes an analog input such that the positive true digital word 1001 1000 1001 0110 exists. The output will be complementary as shown in Figure 2 (0110 0111 0110 1001 is the digital output). Figures 3 and 4 are timing diagrams showing the relationship of serial data to clock, and valid data to status.

DIGITAL CODES

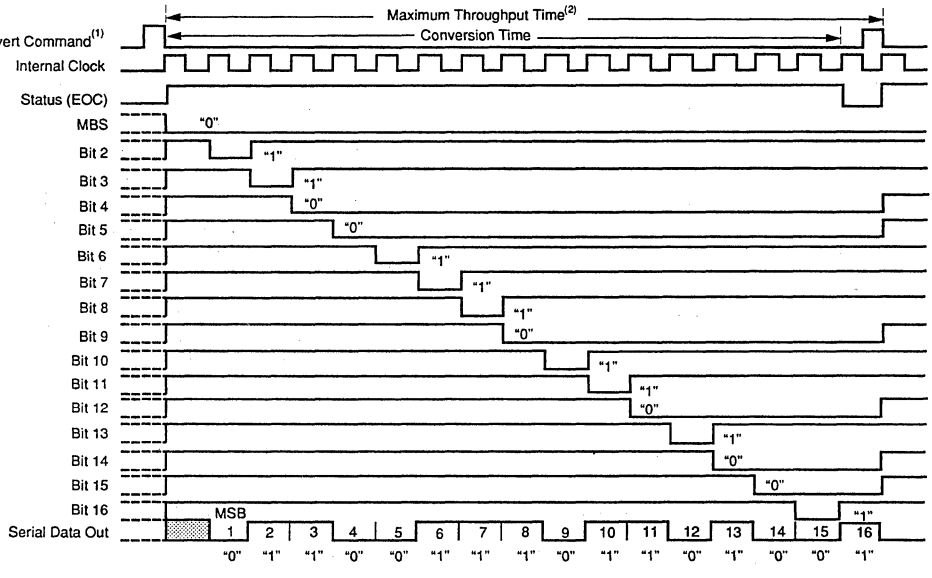
Parallel Data

Two binary codes are available on the ADC76 parallel output: they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges, and complementary offset binary (COB) for bipolar input signal ranges. Complementary two's complement (CTC) may be obtained by inverting the MSB (pin 1).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 12-, 13- and 14-bit resolutions. Figure 5 shows the connections for 14-bit resolution, parallel data output, with ±10V input.

Serial Data

Two straight binary (complementary) codes are available on the serial output line: CSB and COB. The serial data is available only during conversion and appears with MSB occurring first. The serial data is synchronous with the internal clock as shown in the timing diagrams of Figures 2 and 3. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.



NOTES: (1) The convert command must be at least 50ns wide and must remain low during a conversion. The conversion is initiated by the "trailing edge" of the convert command. (2) 17µs for 16 bits.

FIGURE 2. ADC76 Timing Diagram.

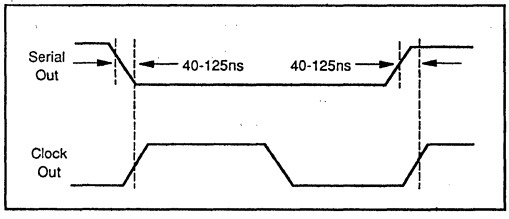


FIGURE 3. Timing Relationship of Serial Data to Clock.

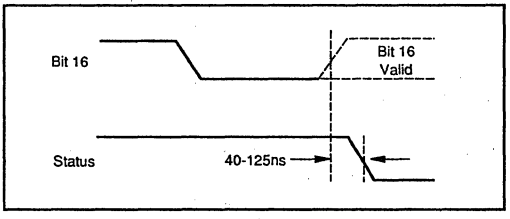


FIGURE 4. Timing Relationship of Valid Data to Status.

BINARY (BIN) OUTPUT	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +IOV	0 to +5V	0 to +20V
Code Designation		COB(1) or CTC(2)	COB(1) or CTC(2)	COB(1) or CTC(2)	CSB(3)	CSB(3)	CSB(3)
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV	4.88mV
	n = 13	2.44mV	1.22mV	610µV	1.22mV	610µV	2.44mV
	n = 14	1.22mV	610µV	305µV	610µV	305µV	1.22mV
Transition Values MSB LSB							
000 ... 000(4)	+Full Scale	+10V–3/2LSB	+5V–3/2LSB	+2.5V–3/2LSB	+10V–3/2LSB	+5V–3/2LSB	+20V–3/2LSB
011 ... 111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111 ... 110	–Full Scale	–10V +1/2LSB	–5V +1/2LSB	–2.5V +1/2LSB	0 +1/2LSB	0 +1/2LSB	0 +1/2LSB

NOTES: (1) COB = Complementary Offset Binary. (2) Complementary Two's Complement—obtained by inverting the most significant bit MSB (pin 1). (3) CSB = Complementary Straight Binary. (4) Voltages given are the nominal value for transition to the code specified.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

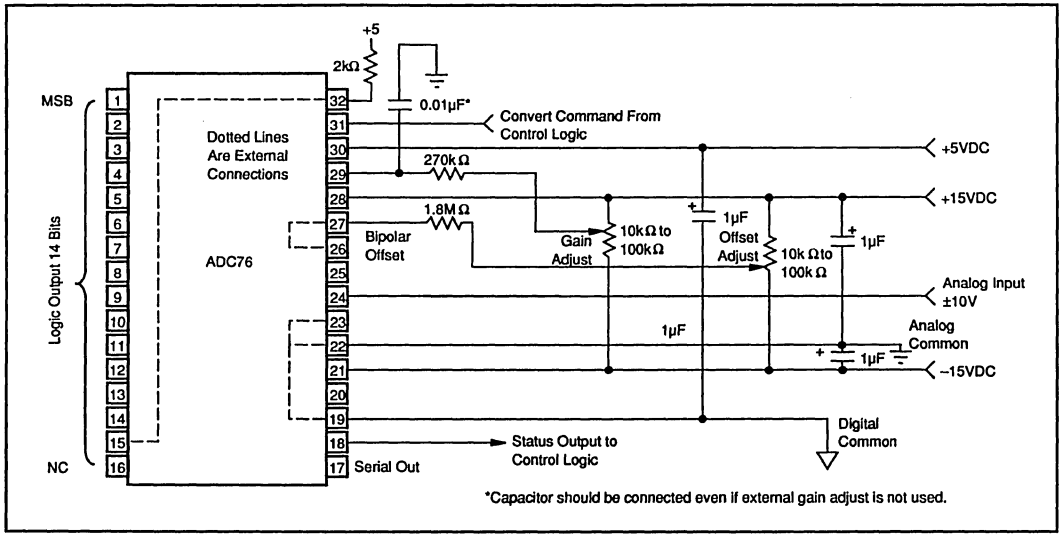


FIGURE 5. ADC76 Connections for: ±10V Analog Input, 14-Bit Resolution (Short-Cycled), Parallel Data Output.

DISCUSSION OF SPECIFICATIONS

The ADC76 is specified to meet critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion speed effects on accuracy. This ADC is factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to typically ±0.1% of FSR (±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 10 and 11.

POWER SUPPLY SENSITIVITY

Changes in the DC power supply voltages will affect accuracy. The ADC76 power supply sensitivity is specified at ±0.003% of FSR/%V_S for the ±15V supplies and ±0.0015% of FSR/%V_S for the +5V supply. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling, and Figure 7.

LINEARITY ERROR

Linearity error is not adjustable and is the most meaningful indicator of A/D converter accuracy. Linearity is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter.

DIFFERENTIAL LINEARITY ERROR

Differential linearity describes the step size between transition values. A differential linearity error of ±0.003% of FSR indicates that the size of any step may not vary from the ideal step size by more than 0.003% of Full Scale Range.

ACCURACY VERSUS SPEED

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC76 are shown in Figure 6.

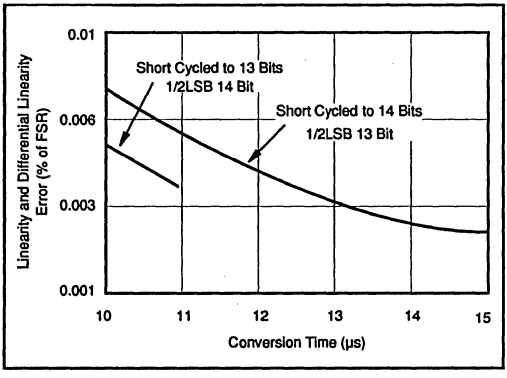


FIGURE 6. Linearity Versus Conversion Time.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital common are not connected internally in the ADC76, but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use a wide conductor pattern and a 0.01µF to 0.1µF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The comparator input (pin 27) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by Analog Common or ±15VDC supply patterns.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic capacitors as shown in Figure 7 to obtain noise free operation. These capacitors should be located close to the ADC.

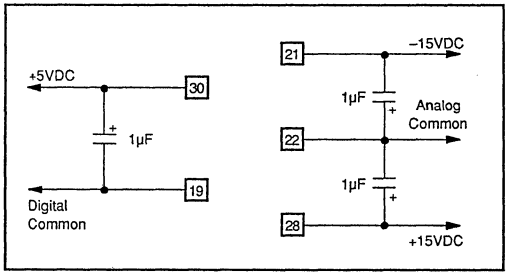


FIGURE 7. Recommended Power Supply Decoupling.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 8 for circuit details.

INPUT SIGNAL RANGE	OUTPUT CODE	CONNECT PIN 26 TO PIN	CONNECT PIN 24 TO	CONNECT INPUT SIGNAL TO PIN
±10V	COB or CTC*	27	Input Signal	24
±5V	COB or CTC*	27	Open	25
±2.5V	COB or CTC*	27	Pin 27	25
0 to +5V	CSB	22	Pin 27	25
0 to +10V	CSB	22	Open	25
0 to +20V	CSB	22	Input Signal	24

*Obtained by inverting MSB pin 1.

TABLE II. ADC76 Input Scaling Connections.

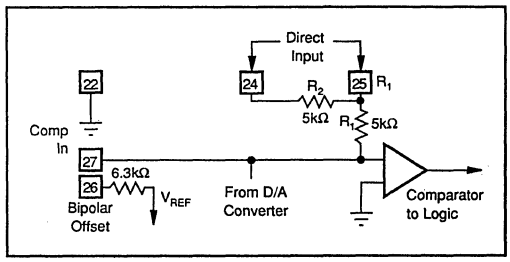


FIGURE 8. ADC76 Input Scaling Circuit.

OUTPUT DRIVE

Normally all ADC76 logic outputs will drive two standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

INPUT IMPEDANCE

The input signal to the ADC76 should be low impedance, such as the output of an op amp, to avoid any errors due to the relatively low input impedance of the ADC76.

If this impedance is not low, a buffer amplifier should be added between the input signal and the direct input to the ADC76 as shown in Figure 9.

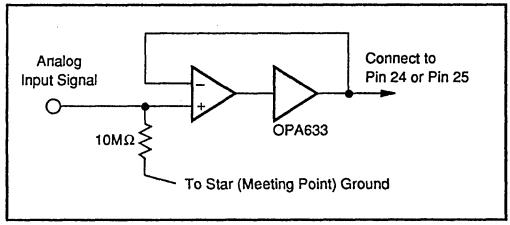


FIGURE 9. Source Impedance Buffering.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 10 and 11. Multiturn potentiometers with 100ppm/°C or better TCRs are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 29 (Gain Adjust) and pin 27 (Offset Adjust) may be left open if no external adjustment is required; however, pin 29 should always be bypassed with 0.01µF to Analog Common.

ADJUSTMENT PROCEDURE

Offset—Connect the Offset potentiometer (make sure R_1 is as close to pin 27 as possible) as shown in Figure 10.

Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN} Off), Figure 1.

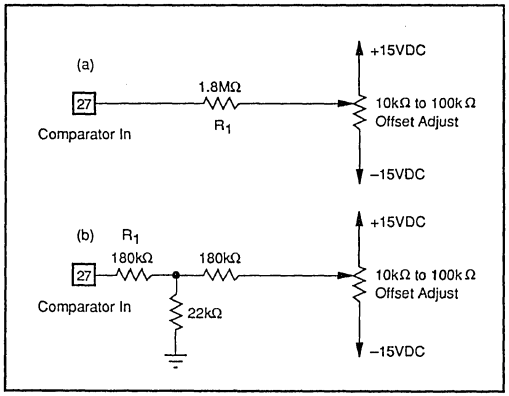


FIGURE 10. Two Methods of Connecting Optional Offset Adjust.

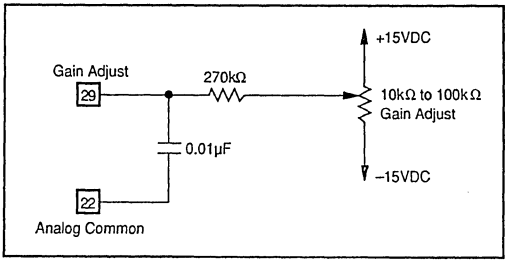


FIGURE 11. Connecting Optional Gain Adjust.

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN} Off. The ideal transition voltage values of the input are given in Table I.

Gain—Connect the Gain adjust potentiometer as shown in Figure 11. Sweep the input through the end point transition voltage; that should cause an output transition to all bits on E_{IN} On. Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN} On.

Table I details the transition voltage levels required.

CONVERT COMMAND CONSIDERATIONS

Convert command resets the converter whenever taken high. This insures a valid conversion on the first conversion after power-up.

Convert command must stay low during a conversion unless it is desired to reset the converter during a conversion.

OPTIONAL CONVERSION TIME ADJUSTMENT

The ADC76 may be operated with faster conversion times for resolutions less than 14 bits by connecting the Short Cycle (pin 32) as shown in Table III. Typical conversion times for the resolution and connections are indicated.

Resolution (Bits)	16	15	14	13	12
Connect Pin 32 to	Open	Pin 16	Pin 15	Pin 14	Pin 13
Typical Conversion Time	17µs	16µs	15µs	13µs	12µs

TABLE III. Short Cycle Connections for 12- to 16-Bit Resolutions.

Clock Rate Control may be connected to an external multi-turn trim potentiometer with a TCR of ±10ppm/°C or less as shown in Figure 12. The typical conversion time versus the Clock Rate Control voltage is shown in Figure 13. The effect of varying the conversion time and the resolution on Linearity Error and Differential Linearity Error is shown in Figure 6.

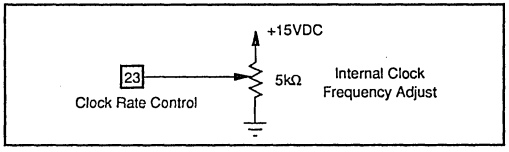


FIGURE 12. Clock Rate Control, Optional Fine Adjust.

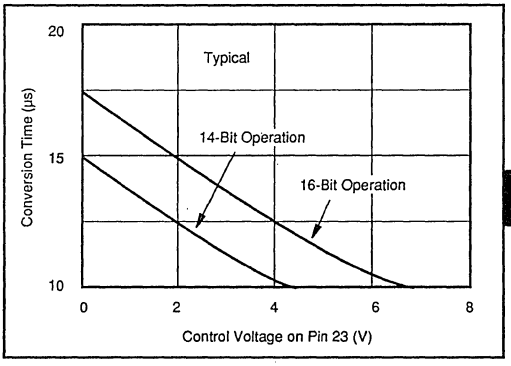


FIGURE 13. Conversion Time vs Clock Rate Control Voltage.

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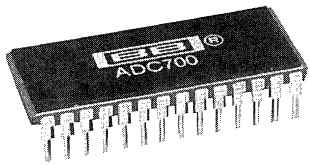


ADC700

16-Bit Resolution With Microprocessor Interface A/D CONVERTER

FEATURES

- COMPLETE WITH REFERENCE, CLOCK, 8-BIT PORT MICROPROCESSOR INTERFACE
- CONVERSION TIME: 17µs max
- LINEARITY ERROR: ±0.003% FSR max
- NO MISSING CODES TO 14 BITS OVER TEMPERATURE
- SPECIFIED AT ±12V AND ±15V SUPPLIES
- OUTPUT BUFFER LATCH FOR IMPROVED INTERFACE TIMING FLEXIBILITY
- PARALLEL AND SERIAL DATA OUTPUT
- SMALL PACKAGE: 28-Pin DIP

DESCRIPTION

The ADC700 is a complete 16-bit resolution successive approximation analog-to-digital converter.

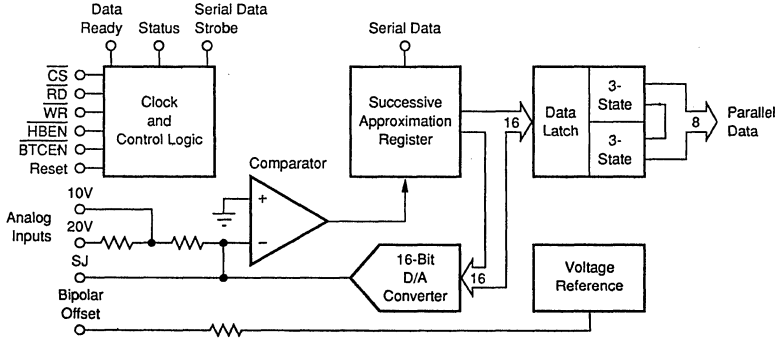
The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Gain and Zero errors may be externally trimmed to zero. Analog input ranges of 0V to +5V, 0V to +10V, 0V to +20V, ±2.5V, ±5V, and ±10V are available.

The conversion time is 17µs max for a 16-bit conversion over the three specification temperature ranges.

After a conversion, output data is stored in a latch separate from the successive approximation logic. This permits reading data during the next conversion, a feature that provides flexible interface timing, especially for interrupt-driven interfaces.

Data is available in two 8-bit bytes from TTL-compatible three-state output drivers. Output data is coded in Straight Binary for unipolar input signals and Bipolar Offset Binary or Twos complement for bipolar input signals. BOB or BTC is selected by a logic function available on one of the pins.

The ADC700 is available in commercial, industrial and military temperature ranges. It is packaged in a hermetic 28-pin side-braze ceramic DIP.



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PDS-856A

SPECIFICATIONS

ELECTRICAL

T_A = 25°C and at rated supplies: V_{DD} = +5V, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = −12V or −15V unless otherwise noted.

CHARACTERISTICS	ADC700JH/AH/RH MIN	ADC700JH/AH/RH TYP	ADC700JH/AH/RH MAX	ADC700KH/BH/SH MIN	ADC700KH/BH/SH TYP	ADC700KH/BH/SH MAX	UNITS
RESOLUTION			16			*	Bits
ANALOG INPUTS							
Voltage Ranges							
Bipolar		±2.5, ±5, ±10			*		V
Unipolar		0 to +5, 0 to +10, 0 to +20			*		V
Impedance (Direct Input)							
0V to +5V, ±2.5V		2.5 ±1%			*		kΩ
0V to +10V, ±5V		5 ±1%			*		kΩ
0V to +20V, ±10V		10 ±1%			*		kΩ
DIGITAL SIGNALS (Over Specification Temperature Range)							
Inputs							
Logic Levels[1]							
V_{IH}	+2.0		+5.5	*		*	V
V_{IL}	0		+0.8	*		*	V
I_{IH} (V_I = +2.7V)			±10			*	µA
I_{IL} (V_I = +0.4V)			±20			*	µA
Outputs							
Logic Levels							
V_{OL} (I_{OL} = −1.6mA)			+0.4			*	V
V_{OH} (I_{OH} = +20µA)	+2.4			*			V
$I_{LEAKAGE}$ Data Outputs Only, High Z		10			*		nA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error			±0.006			±0.003	% of FSR[2]
Differential Linearity Error			±0.012			±0.006	% of FSR
Gain Error[3]		±0.1	±0.2		*	*	%
Zero Error[3]							
Bipolar Zero		±0.1	±0.2		*	*	% of FSR
Unipolar Zero		±0.05	±0.1		*	*	% of FSR
Noise at Transitions (3σp-p)		±0.001	±0.003		*	*	% of FSR
Power Supply Sensitivity							
$+V_{CC}$		±0.0015			*		%FSR/%V_{CC}
$-V_{CC}$		±0.0015			*		%FSR/%V_{CC}
V_{DD}		±0.0005			*		%FSR/%V_{DD}
DRIFT (Over Specification Temperature Range)							
Gain Drift		±8	±15		*	*	ppm/°C
Zero Drift							
Bipolar Zero		±5	±10		*	*	ppm of FSR/°C
Unipolar Zero		±2	±4		*	*	ppm of FSR/°C
Linearity Drift		±1	±3		*	±2	ppm of FSR/°C
No Missing Codes Temperature Range							
JH (13-bit), KH (14-bit)	0		+70	*		*	°C
AH (13-bit), BH (14 bit)	−25		+85	*		*	°C
RH (13-bit), SH (14-bit)	−55		+125	*		*	°C
CONVERSION TIME 16 bits		15	17		*	*	µs
WARM-UP TIME	5			*			min
OUTPUT DATA CODES[4]							
Unipolar Parallel		USB			*		
Bipolar Parallel[5]		BTC, BOB			*		
Serial Output (NRZ)		USB, BOB			*		
POWER SUPPLY REQUIREMENTS							
Voltage Range							
$+V_{CC}$	+11.4	+15	+16	*	*	*	VDC
$-V_{CC}$	−11.4	−15	−16	*	*	*	VDC
V_{DD}	+4.75	+5	+5.25	*	*	*	VDC
Current[5]							
$+V_{CC}$		+10	+15		*	*	mA
$-V_{CC}$		−28	−35		*	*	mA
V_{DD}		+17	+20		*	*	mA
Power Dissipation		645	765		*	*	mW
TEMPERATURE RANGE							
Specification							
J, K Grades	0		+70	*		*	°C
A, B Grades	−25		+85	*		*	°C
R, S Grades	−55		+125	*		*	°C
Storage	−65		+150	*		*	°C

*Same specs as ADC700JH, AH, RH.

TIMING SPECIFICATIONS[6]

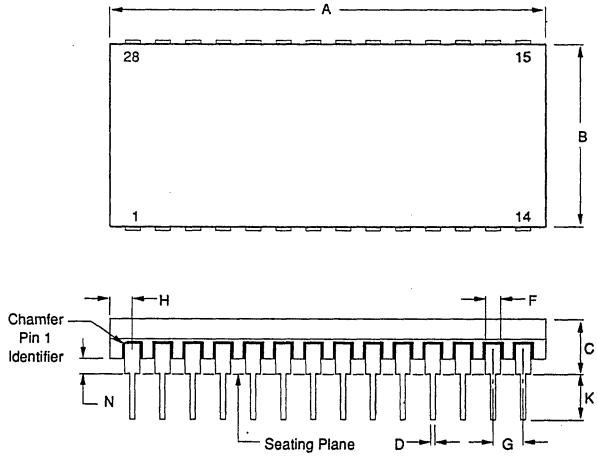
V_{DD} = +5V, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = −12V or −15V unless otherwise noted.

PARAMETER	LIMIT AT T_A = 25°C	LIMIT AT T_A = 0, +70°C −25°C, +85°C	LIMIT AT T_A = −55°C, +125°C	UNITS	DESCRIPTION
CONVERSION AND SERIAL DATA OUTPUT TIMING					
t_1	0	0	0	ns, min	$\overline{CS}$ to $\overline{WR}$ Setup time
t_2	110	130	145	ns, max	$\overline{WR}$ to Status delay
t_3	40	40	40	ns, min	$\overline{WR}$ pulse width
t_4	0	0	0	ns, min	$\overline{CS}$ to $\overline{WR}$ Hold time
t_5	15	17	17	µs, max	Conversion time
t_6	550	600	650	ns, max	Data Ready to Status time
t_7	1100	1150	1250	ns, max	$\overline{WR}$ to first Serial Data Strobe
t_8	250	210	200	ns, min	First Serial Data to first Serial Data Strobe
t_9	310	360	400	ns, max	Last Serial Data Strobe to Status
t_{10}	0	0	0	ns, min	Status to $\overline{WR}$ Setup time
PARALLEL DATA OUTPUT TIMING					
t_{11}	0	0	0	ns, min	$\overline{HBEN}$ to $\overline{RD}$ Setup time
t_{12}	0	0	0	ns, min	$\overline{CS}$ to $\overline{RD}$ Setup time
t_{13}[7]	50	58	66	ns, max	High Byte Data Valid after $\overline{RD}$ C_L = 20pF (High Byte bus access time)
	70	81	95	ns, max	High Byte Data Valid after $\overline{RD}$ C_L = 100pF (High Byte bus access time)
t_{14}	40	40	40	ns, min	$\overline{RD}$ pulse width
t_{15}	40	45	50	ns, max	Data Ready delay from $\overline{RD}$ ($\overline{HBEN}$ asserted)
t_{16}[8]	50	60	65	ns, max	Data Hold time after $\overline{RD}$ (bus relinquish time)
t_{17}	0	0	0	ns, min	$\overline{RD}$ to $\overline{CS}$ Hold time
t_{18}	0	0	0	ns, min	$\overline{RD}$ to $\overline{HBEN}$ Hold time
RESET TIMING					
t_{19}	60	70	80	ns, max	Data Ready low delay from $\overline{Reset}$
t_{20}	70	81	95	ns, max	Status low delay from $\overline{Reset}$

NOTES: (1) TTL, LSTTL, and 5V CMOS compatible. (2) FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR. (3) Externally adjustable to zero. (4) See Table I. USB – Unipolar Straight Binary; BTC – Binary Twos Complement; BOB – Bipolar Offset Binary; NRZ – Non Return to Zero. (5) Max supply current is specified at rated supply voltages. (6) All input control signals are specified with $t_{RISE} = t_{FALL}$ = 5ns (10% to 90% of 5V) and timed from a voltage level of 1.6V. (7) t_{13} is measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V. (8) t_{16} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

MECHANICAL

H Package — 28-Pin Ceramic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.435	1.465	36.45	37.21
B	.610 BASIC		15.49 BASIC	
C	.160	.205	4.06	5.21
D	.015	.019	.38	.48
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.055	.095	1.40	2.41
J	.009	.012	.23	.30
K	.125	.180	3.18	4.57
L	.600 BASIC		15.24 BASIC	
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

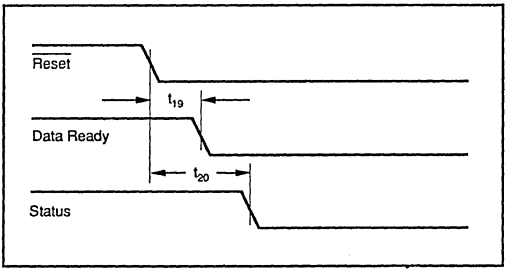
ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	LINEARITY ERROR (%FSR)
ADC700JH	0°C to 70°C	±0.006
ADC700KH	0°C to 70°C	±0.003
ADC700AH	–25°C to +85°C	±0.006
ADC700BH	–25°C to +85°C	±0.003
ADC700RH	–55°C to +125°C	±0.006
ADC700SH	–55°C to +125°C	±0.003

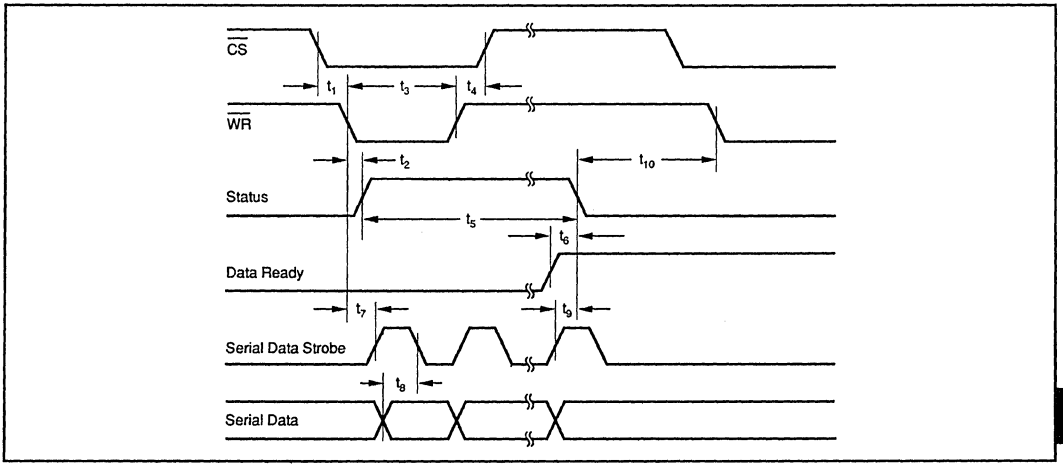
ABSOLUTE MAXIMUM RATINGS

$+V_{DD}$ to Digital Common	0V to +7V
$+V_{CC}$ to Analog Common	0V to +18V
$-V_{CC}$ to Analog Common	0V to –18V
Digital Common to Analog Common	–1V to +1V
Digital Inputs to Digital Common	–0.5V to V_{DD} + 0.5V
Analog Inputs	+16.5V
Power Dissipation	1000mW
Storage Temperature	–60°C to +150°C
Lead Temperature, (soldering, 10s)	+300°C

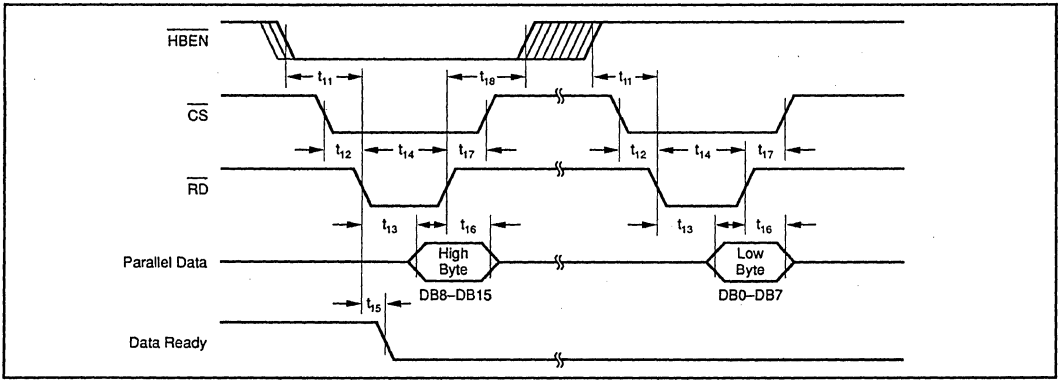
NOTES: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



ADC700 Reset Function Timing Diagram.

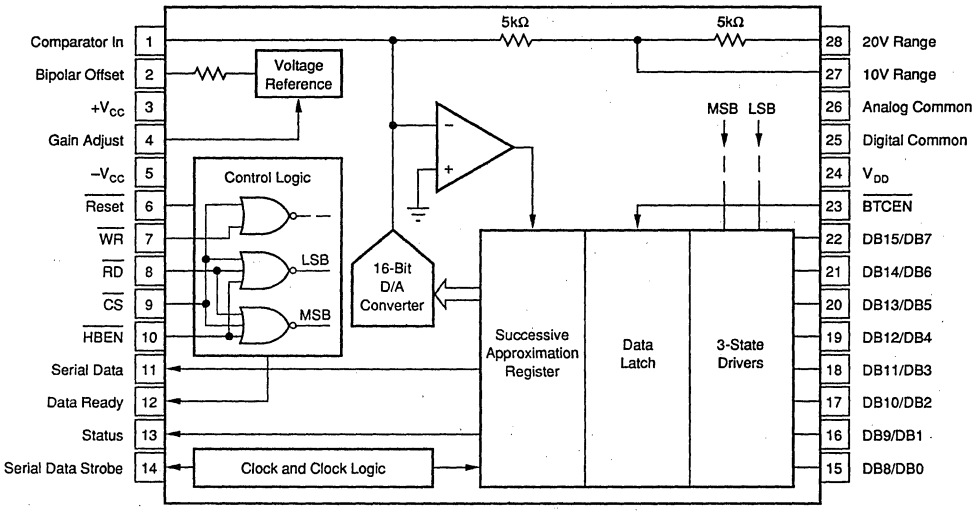


Start of Conversion and Serial Data Output Timing.



ADC700 Parallel Output Timing.

PIN CONFIGURATION



All internal control lines not shown. Refer to Figures 4 and 5 for Offset and Gain Adjust connections.

DESCRIPTION AND OPERATING FEATURES

The ADC700 is a 16-bit resolution successive approximation A/D converter. Parallel digital data as well as serial data is available. Several features have been included in the ADC700 making it easier to interface with microprocessors and/or serial data systems. Several analog input ranges are available.

Some of the key operating features are described here. More detail is given in later sections of the data sheet. Refer to the block diagram above.

RESET

The ADC700 has a $\overline{\text{Reset}}$ input that must be asserted upon power-up or after a power interruption. This initializes the SAR, the output buffer register and Data Ready flag. Since microprocessor systems already use a power-on reset circuit, the same system reset signal can be used to initialize the ADC700.

PARALLEL DATA

The parallel data output is available through an 8-bit port with 3-state output drivers. High byte and low byte are selected by $\overline{\text{HBEN}}$ (pin 10).

A buffer/latch is included between the successive approximation register (SAR) and the 3-state drivers. This feature permits more flexible interface timing than is possible from most successive approximation converters.

The "old" word can be read during the next conversion. A Data Ready flag (pin 12) is asserted when a "new" word is in the buffer register. The Data Ready flag goes low ("0") when the most significant byte (high byte) is read. If the "old" word is not read, or if only the least significant byte (low byte) is read, Data Ready is not reset. The next conversion output will overwrite the data latch when the conversion is complete. The Data Ready flag remains high. Refer to timing diagrams in the Specifications section.

SERIAL DATA

Sixteen-bit serial data output is available (pin 11) along with a serial output strobe (pin 14). This serial data strobe is not the internal SAR clock but is a special strobe for serial data consisting of 16 negative-going edges (during conversion) occurring about 200ns after each serial data bit is valid. This feature eases the interface to shift registers or through optocouplers for applications requiring galvanic isolation.

STATUS

The familiar Status (or Busy) flag, present in successive approximation A/D converters, is available (pin 13) and indicates that a conversion is in progress. Status is valid 110ns after assertion of the convert command ($\overline{\text{WR}}$ low). Status cannot be used as a sample-hold control because there is not enough time for the sample-hold to settle to the required error band before the ADC700 makes its first conversion decision.

CHIP SELECT

$\overline{\text{CS}}$ (pin 9) selects the ADC700. No other functions can be implemented unless $\overline{\text{CS}}$ is asserted. $\overline{\text{WR}}$ (pin 7) is the start-of-conversion strobe. $\overline{\text{RD}}$ strobes each output data byte, selected by $\overline{\text{HBEN}}$ (pin 10), to the 3-state drivers.

TWOS COMPLEMENT DATA CODE

$\overline{\text{BTCEN}}$ (pin 23) is a logic function that implements the Binary Twos Complement output code for bipolar (+ and –) analog input signal operation. This feature is compatible with twos complement arithmetic in microprocessor math algorithms.

INTERNAL CLOCK

The ADC700 has a self-contained clock to sequence the A/D logic. The clock is not available externally. An external 16-pulse strobe (pin 14) is brought out to clock serial data only. Use of ADC700 with external clock is not possible.

INTERNAL VOLTAGE REFERENCE

The ADC700 has an internal low-noise buried-zener voltage reference. The reference circuit has been drift compensated over the MIL temperature range using a laser trim algorithm. The reference voltage is not available externally.

DISCUSSION OF SPECIFICATIONS

BASIC DEFINITIONS

Refer to Figure 3 for an illustration of A/D converter terminology and to Table II in the Calibration section.

Full Scale Range, FSR

The nominal range of the A/D converter. For ADC700, the FSR is 20V for the 0V to +20V and the –10V to +10V input ranges or 10V for the 0V to +10V and –5V to +5V input ranges.

Least Significant Bit, LSB

The smallest analog input change resolved by the A/D converter. For an A/D converter with N bits output, the input value of the LSB is $FSR(2^{-N})$.

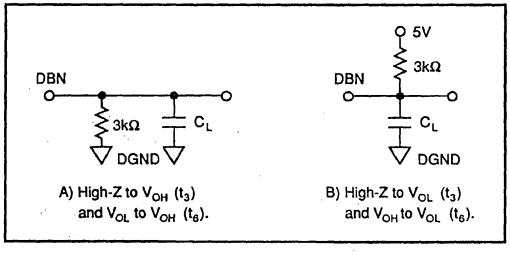


FIGURE 1. Load Circuits for Access Time.

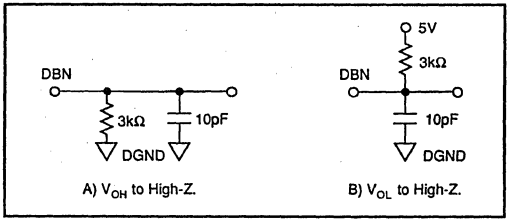


FIGURE 2. Load Circuits for Output Float Delay.

Most Significant Bit, MSB

That binary digit that has the greatest value or weight. The MSB weight is FSR/2.

Resolution

An N-bit binary-coded A/D converter resolves the analog input into 2^N values represented by the 2^N digital output codes.

ACCURACY

Linearity Error, Integral Linearity Error (ILE)

Linearity Error is defined as the deviation of actual analog input values from the ideal values about a straight line drawn through the code mid-points near positive full scale (at $+V_{FS}$ –1LSB) and at Zero input (at 1/2LSB below the first code transition, i.e. at Zero) or, in the case of bipolar operation, near minus full scale (at 1/2LSB below the first code transition, i.e. at $-V_{FS}$). Despite the definition, however, code transitions are easier to measure than code midpoints. Therefore linearity is measured as the deviation of the analog input values from a line drawn between the first and last code transitions. Linearity Error specifications are expressed in % of Full Scale Range (FSR). ADC700KH ILE is ±0.003% of FSR which is 1/2 LSB at 14-bits.

Differential Linearity Error (DLE), No Missing Codes

Differential Linearity Error is defined as the deviation in code width from the ideal value of 1LSB. If the DLE is greater than –1LSB anywhere along the range, the A/D will have at least one missing code. ADC700KH is specified to have a DLE of ±0.006% of FSR, which is ±1LSB at 14 bits. ADC700KH is specified to have *no missing codes* at the 14-bit level over specified temperature ranges.

Gain Error

The deviation from the ideal magnitude of the input span between the first code midpoint (at $-V_{FS}$ + 1/2LSB, for bipolar operation; at Zero for unipolar operation) to the last code midpoint (V_{FS} –1LSB). As with the linearity error

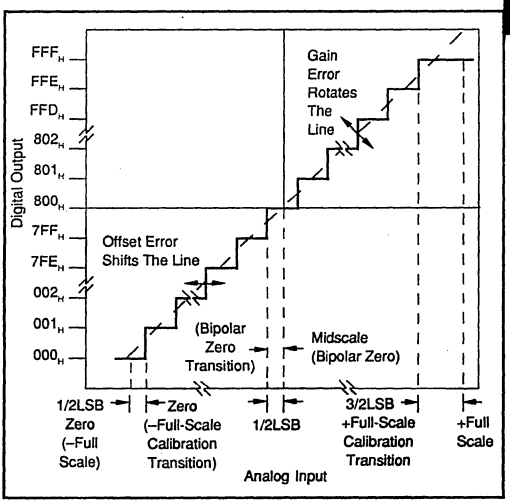


FIGURE 3. Transfer Characteristic Terminology.

measurements, code transition values are the locations actually measured for this spec. The ideal gain is V_{FSR} –2LSB. Gain Error is expressed in % (of reading). See Figure 3.

Gain Error of the ADC700 may be trimmed to zero using external trim potentiometers.

Offset Error

Unipolar Offset Error—The deviation of the actual code-midpoint value of the first code from the ideal value located at 1/2LSB below the ideal first transition value (i.e. at zero volts).

Bipolar Offset Error—The deviation of the actual code-midpoint of the first code from the ideal value located at 1/2LSB below the ideal first transition value located at $-V_{FS}$ +1/2LSB.

Again, transition values are the actual measured parameters. Offset and Zero errors of the ADC700 may be trimmed to zero using external trim potentiometers. Offset Error is expressed as a percentage of FSR.

Bipolar Zero Error—The deviation of the actual mid-scale-code midpoint value from zero. Transition values are the actual measured parameter and it is 1/2 LSB below zero volts. The error is comprised of Bipolar Offset Error, 1/2 the Gain Error, and the Linearity Error of bit 1. Bipolar Zero Error is expressed as a percentage of FSR.

Power Supply Sensitivity

Power Supply Sensitivity describes the maximum change in the full-scale transition value from the initial value for a change in each power supply voltage. PSR is specified in units of %FSR/% change in each supply voltage.

The major effect of power supply voltage deviations from the rated values will be a small change in the Gain (scale factor). Power Supply Sensitivity is also a function of ripple frequency. Figure 4 illustrates typical Power Supply Sensitivity performance of ADC700 versus ripple frequency.

INSTALLATION

POWER SUPPLY SELECTION

Linear power supplies are preferred. Switching power supply specifications may appear to indicate low noise output, but these specifications are rms specs. The spikes generated in switchers may be hard to filter. Their high-frequency components may be extremely difficult to keep out of the power supply return system. If switchers must be used, their outputs must be carefully filtered and the power supply itself should be shielded and located as far away as possible from precision analog circuits.

LAYOUT CONSIDERATIONS

Because of the high resolution and linearity of the ADC700, system design problems such as ground path resistance and contact resistance become very important. For a 16-bit resolution converter with a +10V Full-Scale Range, 1LSB is 153µV. Circuit situations that cause only second- or third-order errors in 8-, 10-, or 12-bit A/D converters can induce first-order errors in 16-bit resolution devices.

Power Supply Wiring

Use heavy power supply and power supply common (ground) wiring. A ground plane is usually the best solution for preserving dynamic performance and reducing noise coupling into sensitive converter circuits.

When passing converter power through a connector, use every available spare pin for making power supply return connections, and use some of the pins as a Faraday shield to separate the analog and digital common lines.

Power Supply Returns (Analog Common and Digital Common)

Connect Analog Common and Digital Common together right at the converter with the ground plane. This will usually give the best performance. However, it may cause problems for the system designer. Where it is absolutely necessary to separate analog and digital power supply returns, each should be separately returned to the power supply. Do not connect Analog Common and Digital Common together and then run a single wire to the power supply. Connect a 1 to 47µF tantalum capacitor between Digital Common and Analog Common pins as close to the package as possible.

Power Supply Bypassing

Every power-supply line leading into an A/D converter must be bypassed to its common pin. The bypass capacitor should be located as close to the converter package as possible and tied to a solid ground—connecting the capacitors to a noisy ground defeats the purpose of the bypass. Use tantalum capacitors with values of from 10µF to 100µF and parallel them with smaller ceramic capacitors for high frequency filtering if necessary.

Separate Analog and Digital Signals

Digital signals entering or leaving the layout should have minimum length to minimize crosstalk to analog wiring. Keep analog signals as far away as possible from digital signals. If they must cross, cross them at right angles. Coaxial cable may be necessary for analog inputs in some situations.

Shield Other Sensitive Points

The most critical of these is the comparator input (pin 1). If this pin is not used for offset adjustment, then it should be surrounded with ground plane or low-impedance power supply plane. If it is used for offset adjustment, the series

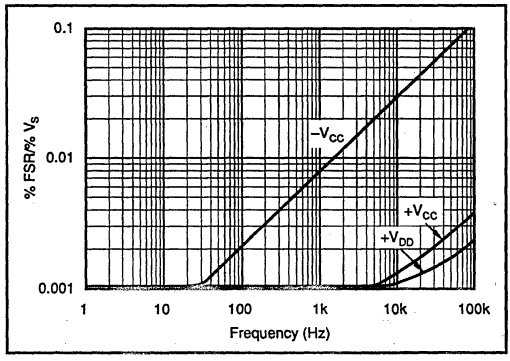


FIGURE 4. Power Supply Rejection Ripple vs Frequency.

resistor and potentiometer should be located as close to the converter as possible.

The Gain Adjust (pin 4) is an input that has a relatively high input impedance and is susceptible to noise pickup. The Gain Adjust pin should be bypassed with a 0.01µF to 0.1µF capacitor whether or not the gain adjust feature is used.

If the 20V Analog input range is used (pin 28), the 10V Range input (pin 27) may need to be shielded with ground plane to reduce noise pickup.

ANALOG SIGNAL SOURCE IMPEDANCE

The input impedance of the ADC700, typical of most successive approximation A/D converters, is relatively low (2.5kΩ to 10kΩ). The input current of a successive approximation A/D converter changes rapidly during the conversion algorithm as each bit current is compared to the analog input current. Since the output impedance of a closed-loop amplifier or a sample-hold amplifier increases with frequency and, in addition, the amplifier must settle to the required accuracy in time for the next comparison/decision after such a disturbance, care must be taken to select the proper driving amplifier.

Unfortunately, high-accuracy operational amplifiers tend to have low bandwidth, while wide-band amplifiers tend to have lower accuracy. One solution is to use a wide-band but perhaps less precise amplifier. Another solution is to add a wide-band buffer amplifier such as the Burr-Brown OPA633 inside the feedback loop of a slower (but precision) amplifier, Figure 5. This reduces the output impedance at high frequencies yet preserves the accuracy at low frequencies. When a sample/hold is needed, a high-linearity, high-speed sample/hold such as the Burr-Brown SHC76 should be used to drive the ADC700.

ANALOG INPUT RANGES

The analog input circuits of the ADC700 can be connected to accept unipolar or bipolar input signals. These ranges and connections are tabulated in Table I. Circuit connections are shown in Figures 6 and 7. Gain and offset adjustments are described in the calibration section.

To operate the ADC700 with a range that gives other convenient values for the LSB, the input resistor may be increased or decreased slightly without seriously affecting the Gain Drift of the converter. Since the input resistors of the ADC700 are within ±2% from unit to unit, this can be consistently done with a fixed series or parallel resistor. The ADC700 can then be calibrated using the Gain and Offset adjustments described in the calibration section. For example, using the ±10V input range, one can decrease the range slightly by paralleling the 10kΩ input resistor (pin 28 to pin 1) with a 610kΩ metal film resistor to achieve a 300µV LSB instead of the nominal standard 305.17578µV binary LSB.

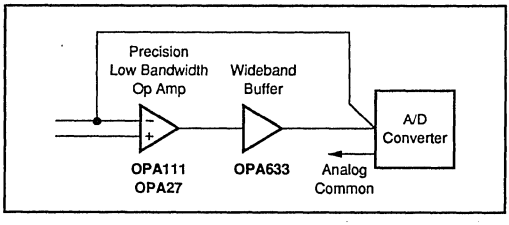


FIGURE 5. Wideband Buffer Reduces Output Impedance at High Frequencies.

OPTIONAL EXTERNAL GAIN AND OFFSET TRIM

Gain and Offset Error may be trimmed to zero using external Gain and Offset trim potentiometers connected to the ADC700 as shown in Figures 6 and Figure 7. A calibration procedure in described in the Operating Instructions section.

Multiturn potentiometers with 100ppm/°C or better TCR are recommended for minimum drift over temperature. These potentiometers may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 1 (Comparator In) and pin 4 (Gain Adjust) may be left open if no external adjustment is planned; however, pin 4 should always be bypassed with 0.01µF or larger to Analog Common.

OPERATING INSTRUCTIONS

CALIBRATION

Offset and Gain may be trimmed by external Offset and Gain potentiometers. Offset is adjusted first and then Gain. Calibration values are listed in Table II for all ADC700 input ranges. Offset and Gain calibration can be accomplished to a precision of about ±1/2LSB using a static adjustment procedure described below. By summing a small sine or triangular wave voltage with the accurate calibration voltage applied to the analog input, the output can be swept through each of the calibration codes to more accurately determine the transition points listed in Table II. NOTE: The transition points are not the same as the code midpoints used in the static calibration example.

OFFSET ADJUSTMENT, 14-BIT RESOLUTION EXAMPLE

Static Adjustment Procedure (At Code Midpoints)

0V to +10V Range—Set the analog input to $+1LSB_{14}$ = 0.00061V. Adjust the Offset potentiometer for a digital output of 0004_H. Set the analog input to +Full Scale $-2LSB_{14}$ = +9.9987V. Adjust the Gain potentiometer for a digital output of $FFFC_H$. For a half-scale calibration check, set the analog input to +5.0000V and read a digital output code of 8000_H.

INPUT SIGNAL RANGE	OUTPUT CODE		CONNECT PIN 2 TO PIN	CONNECT PIN 28 TO PIN	CONNECT SIGNAL TO PIN
	$\overline{BTCEN}$ = 1	$\overline{BTCEN}$ = 0			
±10V	BOB	BTC	1	Input Signal	28
±5V	BOB	BTC	1	Open	27
±2.5V	BOB	BTC	1	Pin 1	27
0V to +5V	USB	—	26	Pin 1	27
0V to +10V	USB	—	26	Open	27
0V to +20V	USB	—	26	Input Signal	28

TABLE I. ADC700 Input Range Connections.

ANALOG INPUT RANGE	VOLTAGE (V)					
	±10	±5	±2.5	0 TO +20	0 TO +10	0 TO +5
$+V_{FS}$	+10	+5	+2.5	+20	+10	+5
$-V_{FS}$	–10	–5	–2.5	0	0	0
FSR	20	10	5	20	10	5
TRANSITION CODES (Hexadecimal)	**TRANSITION VALUES (V)**					
For 16-bit Resolution (Reading all 16 bits)						
$FFFE_H$ to $FFFF_H$	+9.999542	+4.999771	+2.499886	+19.999542	+9.99971	+4.999886
$7FFF_H$ to 8000_H	–152.5µV	–38µV	–19µV	+9.999847	+4.999924	+2.499962
0000_H to 0001_H	–9.999847	–4.999924	–2.499962	+152µV	+76µV	+38µV
LSB (FSR/2^{16})	305µV	153µV	38µV	305µV	153µV	76µV
For 15-bit Resolution (Reading all 16 bits, Ignoring DB_0)						
$FFFD_H$ to $7FFE_H$	+9.999084	+4.999542	+2.499771	+19.999084	+9.999542	+4.999771
$7FFE_H$ to 8000_H	–305µV	–153µV	–76µV	+9.999625	+4.999847	+2.499924
0000_H to 0002_H	–9.999695	–4.999847	–2.499924	+305µV	+152µV	+76µV
LSB (FSR/2^{15})	610µV	305µV	153µV	610µV	305µV	153µV
For 14-bit Resolution (Reading all 16 bits, Ignoring DB_0 and DB_1)						
$FFFC_H$ to $FFFD_H$	+9.99817	+4.99908	+2.49954	+19.99817	+9.99908	+4.99954
$7FFD_H$ to 8000_H	–610µV	–305µV	–153µV	+9.99939	+4.999695	+2.499847
0000_H to 0004_H	–9.999390	–4.999694	–2.499847	+610µV	+305µV	+153µV
LSB (FSR/2^{14})	1221µV	610µV	305µV	1221µV	610µV	305µV

TABLE II. Transition Values for Calibration.

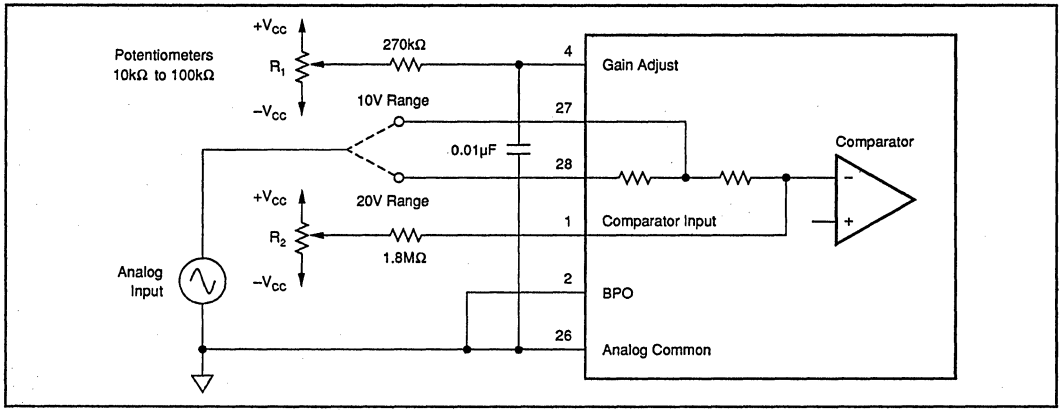


FIGURE 6. Unipolar Input Configuration with Gain and Offset Adjust Connections.

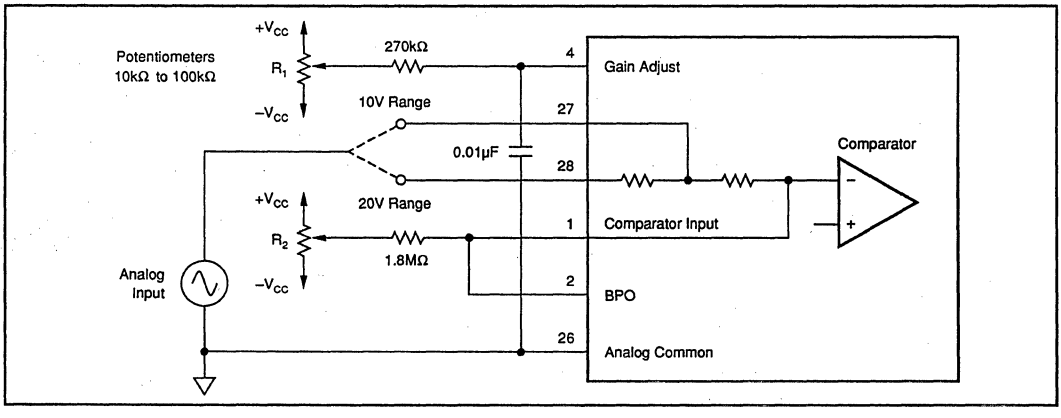


FIGURE 7. Bipolar Input Configuration with Gain and Offset Adjust Connections.

–10V to +10V Range—Set the analog input to –FS + $1LSB_{14}$ = –9.99878V. Adjust the Offset potentiometer for a digital output of 0004_H (8004_H if $\overline{BTCEN}$ is asserted). Set the analog input to +9.9976V. Adjust the Gain potentiometer for a digital output of $FFFC_H$ ($7FFC_H$ if $\overline{BTCEN}$ is assrted). For a half-scale calibration check, set the analog input to 0.0000V and read a digital output code of 8000_H (0000_H if $\overline{BTCEN}$ is asserted).

CONTROLLING AND INTERFACING THE ADC700

RESET

The ADC700 requires a Reset command upon power-up or after a power interruption to guarantee the condition of internal registers. If Status powers-up High, no conversion can be started. Reset initializes the SAR, the output buffer register, and the Data Ready flag and terminates a conversion in progress. Since microprocessor systems already use a power-on reset circuit, the same system reset signal can be used to initialize the ADC700. A power-up circuit is shown in Figure 8. Refer to Reset function timing diagram following the Timing Specifications Table.

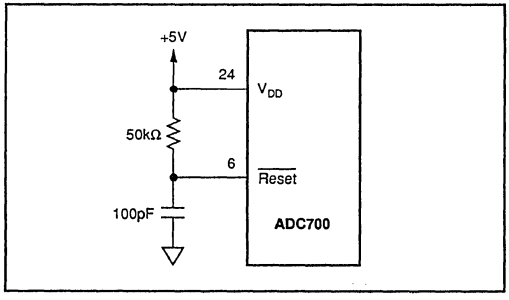


FIGURE 8. Power-Up Reset Circuit.

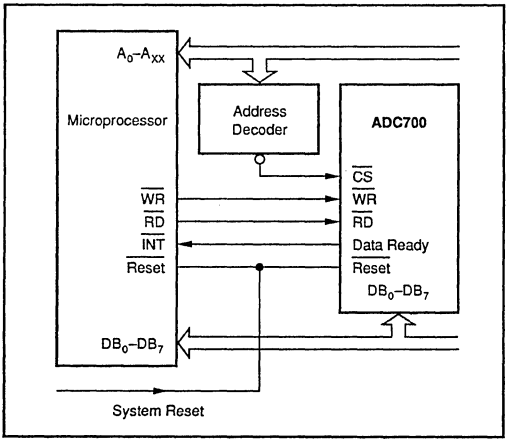


FIGURE 9. Parallel Data Bus Interface.

START OF CONVERSION

A conversion is started by asserting $\overline{CS}$ and $\overline{WR}$ Low. Status goes high about $t = t_1 + t_2 = 110ns$ later. The first successive approximation decision occurs about 900ns after $\overline{WR}$ is asserted. Status goes Low after the conversion is complete. Refer to Start of Conversion and Serial Data Output Timing following the Timing Specifications Table.

DATA READY FLAG

The data latch feature permits data to be read during the following conversion. The Data Ready flag indicates that the data from the most recent conversion is latched in the output data latch and that it hasn't been read. Data Ready remains High until the most significant data byte is read. If a subsequent conversion is initiated and completed, the new word will be stored in the output data latch regardless of the state of the Data Ready flag. The preceding word will be overwritten and lost.

READING PARALLEL DATA

Parallel data is latched in the output data latch at the end of a conversion. Data can be read any time, even during the subsequent conversion. The output data latch is not cleared by reading the data. Only the Data Ready flag is cleared by reading the MSB.

The output three-state drivers are enabled by asserting the $\overline{CS}$ and $\overline{RD}$ inputs Low. When $\overline{HBEN}$ is Low, the most significant eight bits are enabled and the Data Ready flag is cleared. When $\overline{HBEN}$ is High, the least significant eight bits are enabled. Refer to Parallel Data Output Timing information following the Timing Specifications Table.

To reduce noise interference to the absolute minimum, data should be read after the current conversion is complete. However, data can be read during the following conversion, with minimal interference, to maximize the sampling rate of the converter.

A typical parallel interface is illustrated in Figure 9.

READING SERIAL DATA

Serial data output of the ADC700 is facilitated by a Serial Data Strobe that provides 16 negative-going edges for strobing an external serial to parallel shift register located perhaps on the other side of an opto-coupler. Refer to the Serial Data Timing information following the Timing Specifications Table. An example of an isolation connection using the serial port feature is illustrated in Figure 10.

CONTINUOUS CONVERSION OPERATION

When $\overline{CS}$ is permanently connected to Digital Common and Status is connected to $\overline{WR}$, Figure 11, the ADC700 will continuously convert. The repetition time will not be precise and will vary slightly with the temperature for the ADC700 because the time will be determined by the internal clock frequency and control-circuit gate delays. If a precise repe-

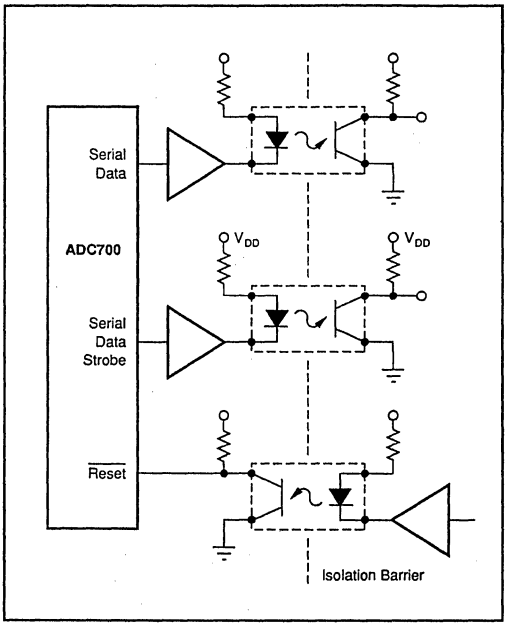


FIGURE 10. Serial Data Output Providing Convenient Isolation.

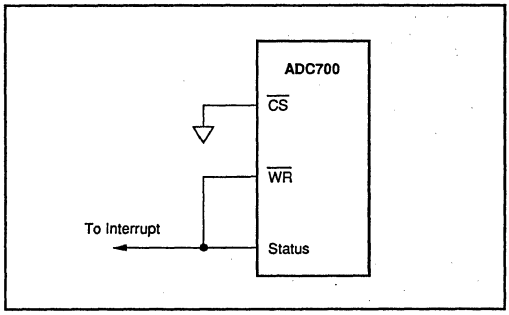


FIGURE 11. Continuous Conversion Circuit Connection.

PIN DESIGNATION	DEFINITION	FUNCTION
$\overline{CS}$ (Pin 9)	Chip Select	Must be Low to either initiate a conversion or read output data.
$\overline{WR}$ (Pin 7)	Write (Convert)	Conversion begins after the High-to-Low transition.
$\overline{RD}$ (Pin 8)	Read	Turns ON the three-state output drivers upon being asserted low.
$\overline{HBEN}$ (Pin 10)	High Byte Enable "1" = Low Byte "0" = High Byte	Selects the MSB or the LSB for readout. Data Ready is cleared when $\overline{HBEN}$ is Low and $\overline{RD}$ is asserted.
$\overline{Reset}$ (Pin 6)	Reset	Resets internal logic. Must be asserted after power-up or a power interruption clears Status and Data Ready to Low.
$\overline{BTCEN}$ (Pin 23)	BTC Enable	Sets the output code to Binary Twos Complement (BTC) when Low. Output code is Bipolar Offset Binary (BOB) when High.

TABLE III. Control Line Functions.

CONTROL LINE					
$\overline{RESET}$	$\overline{WR}$	$\overline{RD}$	$\overline{HBEN}$	$\overline{CS}$	OPERATION
0	X	X	X	X	Reset converter logic. Status and Data Ready set Low.
1	X	X	X	1	No operation.
1	0	X	X	0	Initiate conversion.
1	1	0	0	0	Places High Byte on output port. Clears Data Ready flag.
1	1	0	1	0	Placed Low Byte on output port. Does not clear Data Ready flag.
1	0	0	0	0	Initiates conversion and places High Byte or output port. Clears Data Ready.
1	0	0	1	0	Initiates conversion and places Low Byte on output port. Does not clear Data Ready flag.
NOTE: If a conversion command is asserted while a conversion is in progress, the command is ignored. If the conversion command remains asserted when a conversion is finished, a new conversion will begin.					

TABLE IV. Control Input Truth Table.

tition rate is needed, the continuous conversion connection should not be used.

Because the last data-word is stored in the data latch, it is possible to read it during the next A/D conversion. Assertion of $\overline{CS}$ and $\overline{HBEN}$ for reading parallel data should be timed from Status going low. The two-byte read operation must be complete before the conversion in process is complete or the Data Read is invalid.

Serial Data is available during continuous conversion with word synchronization available from STATUS.

USING A SAMPLE/HOLD WITH ADC700

Figure 12 illustrates using ADC700 with the Burr-Brown SHC76. The sample-to-hold settling time (to 14 bits, ±0.003%FSR) of the SHC76 is 1µs typ, 3µs max. The time from the Status going High to the first conversion decision is about 900ns. Therefore a time delay between the Sample-to-Hold command to the $\overline{WR}$ command to the ADC700 is required.

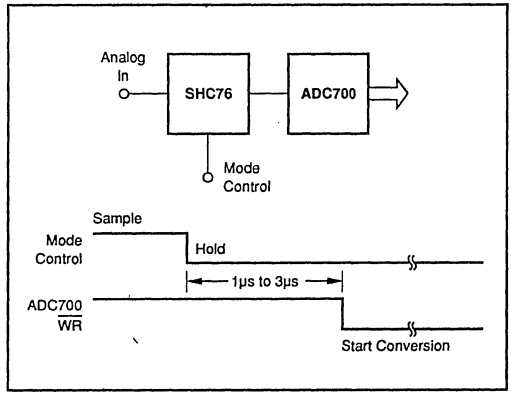
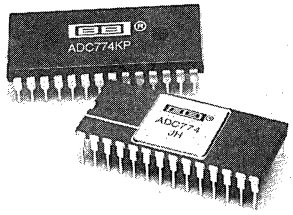


FIGURE 12. Using Sample/Hold with ADC700 Requires Time Delay Between Sample and Start-of-Conversion.

BURR-BROWN®



ADC774

Microprocessor-Compatible ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE, CLOCK, AND 8-, 12-, OR 16-BIT MICROPROCESSOR BUS INTERFACE**
- **ALTERNATE SOURCE FOR HI774 A/D CONVERTER: 8μs Conversion Time, 150ns Bus Access Time**
- **FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES**
- **NO MISSING CODES OVER TEMPERATURE:**
  0°C to +75°C: ADC774JH, KH, JP, KP
  –55°C to +125°C: ADC774SH, TH

DESCRIPTION

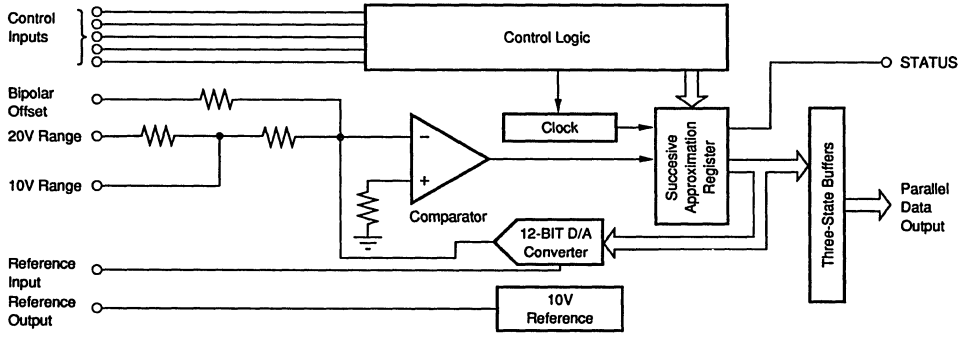
The ADC774 is a 12-bit successive approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom-designed for freedom from latch-up and for optimum AC performance. It is complete with a self-contained +10V reference, internal clock, digital interface for microprocessor control, and three-state outputs.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Full-scale and offset errors may be externally trimmed to zero. Internal scaling resistors are provided for the selection of analog input signal ranges of 0V to +10V, 0V to +20V, ±5V, and ±10V.

The converter may be externally programmed to provide 8- or 12-bit resolution. The conversion time for 12 bits is factory set for 8.5μs maximum.

Output data are available in a parallel format from TTL-compatible three-state output buffers. Output data are coded in straight binary for unipolar input signals and bipolar offset binary for bipolar input signals.

The ADC774, available in both industrial and military temperature ranges, requires supply voltages of +5V and ±12V or ±15V. It is packaged in a 28-pin plastic DIP and a hermetic side-brazed ceramic DIP.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-835B

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V, V_{LOGIC} = +5V unless otherwise specified.

PARAMETER	ADC774JP, ADC774JH, ADC774SH MIN	ADC774JP, ADC774JH, ADC774SH TYP	ADC774JP, ADC774JH, ADC774SH MAX	ADC774KP, ADC774KH, ADC774TH MIN	ADC774KP, ADC774KH, ADC774TH TYP	ADC774KP, ADC774KH, ADC774TH MAX	UNITS
RESOLUTION			12			•	Bits
INPUTS							
ANALOG							
Voltage Ranges: Unipolar		0 to +10, 0 to +20			•		V
Bipolar		±5, ±10			•		V
Impedance: 0 to +10V, ±5V	4.7	5	5.3	•	•	•	kΩ
±10V, 0V to +20V	9.4	10	10.6	•	•	•	kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$)							
Over Temperature Range							
Voltages: Logic 1	+2		+5.5	•		•	V
Logic 0	−0.5		+0.8	•		•	V
Current	−5	0.1	+5	•	•	•	µA
Capacitance		5			•		pF
TRANSFER CHARACTERISTICS							
ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (Adjustable to Zero)			±2			•	LSB
Bipolar Offset Error (Adjustable to Zero)			±10			±4	LSB
Full-Scale Calibration Error[1] (Adjustable to Zero)			±0.25			•	% of FS[2]
No Missing Codes Resolution (Diff. Linearity)	11			12			Bits
Inherent Quantization Error		±1/2			•		LSB
T_{MIN} to T_{MAX}							
Linearity Error: J, K Grades			±1			±1/2	LSB
S, T Grades			±1			±3/4	LSB
Full-Scale Calibration Error							
Without Initial Adjustment[1]: J, K Grades			±0.47			±0.37	% of FS
S, T Grades			±0.75			±0.5	% of FS
Adjusted to Zero at +25°C: J, K Grades			±0.22			±0.12	% of FS
S, T Grades			±0.5			±0.25	% of FS
No Missing Codes Resolution (Diff. Linearity)	11			12			Bits
TEMPERATURE COEFFICIENTS (T_{MIN} to T_{MAX})[3]							
Unipolar Offset: J, K Grades			±10			±5	ppm/°C
S, T Grades			±5			±2.5	ppm/°C
Max Change: All Grades			±2			±1	LSB
Bipolar Offset: All Grades			±10			±5	ppm/°C
Max Change: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration: J, K Grades			±45			±25	ppm/°C
S, T Grades			±50			±25	ppm/°C
Max Change: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration							
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V			±2			±1	LSB
−16.5V < V_{EE} < −13.5V or −12.6V < V_{EE} < −11.4V			±2			±1	LSB
+4.5V < V_{LOGIC} < +5.5V			±1/2			•	LSB
CONVERSION TIME[4][5]							
8-Bit Cycle		5	5.3		•	•	µs
12-Bit Cycle		7.5	8		•	•	µs
OUTPUTS							
DIGITAL (DB11–DB0, STATUS)							
(Over Temperature Range)							
Output Codes: Unipolar		Unipolar Straight Binary (USB)					
Bipolar		Bipolar Offset Binary (BOB)					
Logic Levels: Logic 0 (I_{SINK} = 1.6mA)			+0.4			•	V
Logic 1 (I_{SOURCE} = 500µA)	+2.4			•			V
Leakage, Data Bits Only, High-Z State	−5	0.1	+5	•	•	•	µA
Capacitance		5			•		pF
INTERNAL REFERENCE VOLTAGE							
Voltage	+9.9	+10	+10.1	•	•	•	V
Source Current Available for External Loads[6]	2			•			mA

SPECIFICATIONS

ELECTRICAL

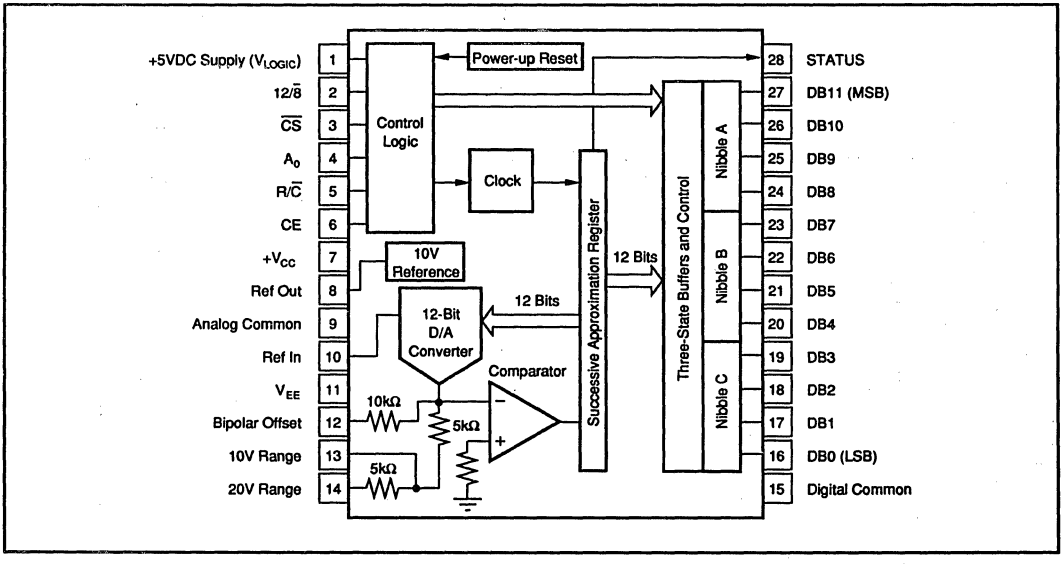
T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = –12V or –15V, V_{LOGIC} = +5V unless otherwise specified.

PARAMETER	ADC774JP, ADC774JH, ADC774SH			ADC774KP, ADC774KH, ADC774TH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS							
Voltage: V_{CC}	+11.4		+16.5	*		*	V
V_{EE}	–11.4		–16.5	*		*	V
V_{LOGIC}	+4.5		+5.5	*		*	V
Current: I_{CC}		3.5	5		*	*	mA
I_{EE}		15	20		*	*	mA
I_{LOGIC}		9	15		*	*	mA
Power Dissipation (±15V Supplies)		325	450		*	*	mW
TEMPERATURE RANGE (Ambient: T_{MIN}, T_{MAX})							
Specifications: J, K Grades	0		+75	*		*	°C
S, T Grades	–55		+125	*		*	°C
Storage	–65		+150	*		*	°C

*Same specification as ADC774JP, JH, SH.

NOTES: (1) With fixed 50Ω resistor from Ref Out to Ref In. This parameter is also adjustable to zero at +25°C. (2) FS in this specification table means Full Scale Range. That is, for a ±10V input range FS means 20V; for a 0V to +10V range, FS means 10V. The term Full Scale is used instead of Full-Scale Range to be consistent with other vendors' specifications tables. (3) Using internal reference. (4) See "Controlling the ADC774" section for detailed information concerning digital timing. (5) The Harris HI-774 uses a subranging/error correction technique that allows one to begin conversion before a preceding sample-hold or multiplexer has settled to ±1/2LSB. For 12-bit accurate conversions, the input transient to the ADC774 must settle to less than ±1/2LSB before conversion is started. The ADC774 is compatible with HI774 in all other respects. (6) External loading must be constant during conversion. The reference output requires no buffer amplifier with either ±12V or ±15V power supplies.

PIN CONFIGURATION

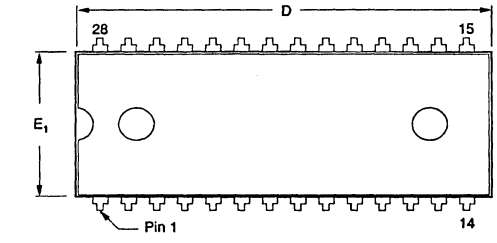


ORDERING INFORMATION

MODEL	PACKAGE (DIP)	TEMPERATURE RANGE	LINEARITY ERROR MAX (T_{MIN} TO T_{MAX})
ADC774JP	Plastic	0°C to 75°C	±1LSB
ADC774KP	Plastic	0°C to 75°C	±1/2LSB
ADC774JH	Ceramic	0°C to 75°C	±1LSB
ADC774KH	Ceramic	0°C to 75°C	±1/2LSB
ADC774SH	Ceramic	–55°C to 125°C	±1LSB
ADC774TH	Ceramic	–55°C to 125°C	±3/4LSB

MECHANICAL

P Package — 28-Pin Plastic DIP

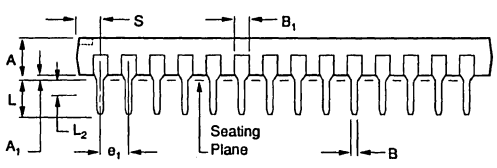


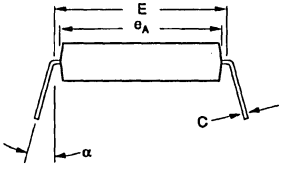
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A(1)	.169	.200	4.29	5.08
A1(1)	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D(1)	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1(1)	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
S(1)	.040	.080	1.02	2.03

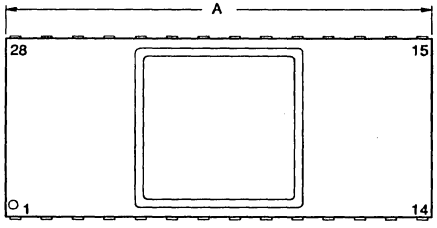
(1) Not JEDEC Standard

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.



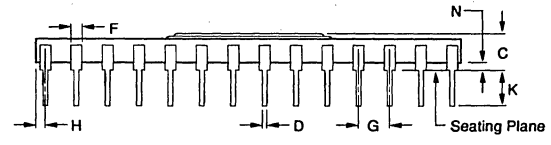


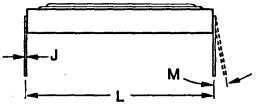
H Package — 0.6" Wide 28-Pin Hermatic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.386	1.414	35.20	35.92
C	.115	.175	2.92	4.45
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.036	.064	0.91	1.63
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.





ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common ..... 0V to +16.5V
V_{EE} to Digital Common ..... 0V to –16.5V
V_{LOGIC} to Digital Common ..... 0V to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$)
to Digital Common ..... –0.5V to V_{LOGIC} +0.5V
Analog Inputs (Ref In, Bipolar Offset, $10V_{IN}$)
to Analog Common ..... ±16.5V
$20V_{IN}$ to Analog Common ..... ±24V
Ref Out ..... Indefinite Short to Common, Momentary Short to V_{CC}
Max Junction Temperature ..... +165°C
Power Dissipation 1000mW
Lead Temperature (soldering, 10s) ..... +300°C
Thermal Resistance, θ_{J-A}: Ceramic ..... 50°C/W
Plastic ..... 100°C/W

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale. The zero value is located at an analog input value 1/2LSB before the first code transition (000_{HEX} to 001_{HEX}). The full-scale value is located at an analog value 3/2LSB beyond the last code transition (FFE_{HEX} to FFF_{HEX}) (see Figure 1).

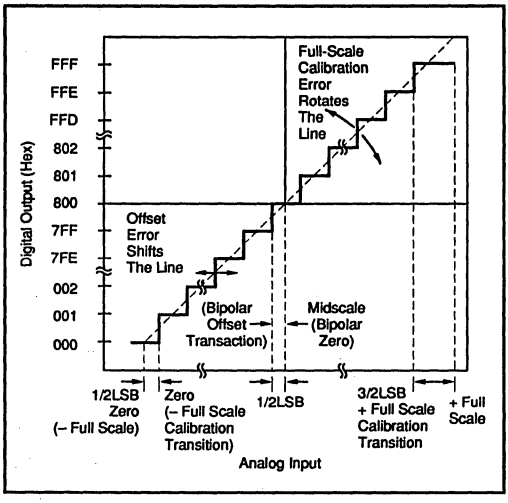


FIGURE 1. ADC774 Transfer Characteristics Terminology.

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V), the zero value of –10V is 2.44mV below the first code transition (000_{HEX} to 001_{HEX} at –9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (FFE_{HEX} at +9.99268) (see Table I).

NO MISSING CODES (DIFFERENTIAL LINEARITY ERROR)

A specification which guarantees no missing codes requires every code combination to appear in a monotonically increasing sequence as the analog input is increased throughout the range. Thus, every input code width (quantum) must have a finite width. If an input quantum has a value of zero (a differential linearity error of –1LSB), a missing code will occur.

ADC774KP, KH, and TH grades are guaranteed to have no missing codes to 12-bit resolution over their respective specification temperature ranges.

UNIPOLAR OFFSET ERROR

An ADC774 connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transaction should occur at an analog input value 1/2LSB above 0V. The unipolar offset temperature coefficient specifies the change of this transition value versus a change in ambient temperature.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset as the first transition value above the minus full-scale value. The ADC774 specifications, however, follow the terminology defined for the 574 converter several years ago. Thus, bipolar offset is located near the midscale value of 0V (bipolar zero) at the output code transition $7FF_{HEX}$ to 800_{HEX}.

Bipolar offset error for the ADC774 is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB below 0V. The bipolar offset temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

FULL SCALE CALIBRATION ERROR

The last output transition (FFE_{HEX} to FFF_{HEX}) occurs for an analog input value 3/2LSB below the nominal full-scale value. The full-scale calibration error is the deviation of the actual analog value at the last transition point from the ideal value. The full-scale calibration temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC774 assume the application of the rated power supply voltages of +5V and ±12V or ±15V. The major effect of power supply voltage deviations from the rated values will be a small change in the full-

BINARY (BIN) OUTPUT	INPUT VOLTAGE RANGE AND LSB VALUES				
Analog Input Voltage Range	**Defined as**	**±10V**	**±5V**	**0 to +10V**	**0 to +20V**
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{10V}{2^n}$	$\frac{20V}{2^n}$
	n = 8	78.13mV	39.06mV	39.06mV	78.13mV
	n =12	4.88mV	2.44mV	2.44mV	4.88mV
Output Transition Values					
FFE_{HEX} to FFF_{HEX}	+ Full-Scale Calibration	+10V – 3/2LSB	+5V – 3/2LSB	+10V – 3/2LSB	+10V – 3/2LSB
$7FF_{HEX}$ to 800_{HEX}	Midscale Calibration (Bipolar Offset)	0 – 1/2LSB	0 – 1/2LSB	+5V – 1/2LSB	±10V – 1/2LSB
000_{HEX} to 001_{HEX}	Zero Calibration (– Full-Scale Calibration)	–10V + 1/2LSB	–5V + 1/2LSB	0 to +1/2LSB	0 to +1/2LSB

TABLE I. Input Voltages, Transition Values, and LSB Values.

scale calibration value. This change, of course, results in a proportional change in all code transition values (i.e., a gain error). The specification describes the maximum change in the full-scale calibration value from the initial value for a change in each power supply voltage.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset and bipolar offset specify the maximum change from the +25°C value to the value at T_{MIN} or T_{MAX}.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/21LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

CODE WIDTH (QUANTUM)

Code width, or quantum, is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB.

INSTALLATION

LAYOUT PRECAUTIONS

Analog (Pin 9) and digital (Pin 15) commons are not connected together internally in the ADC774, but should be connected together as close to the unit as possible and to an analog common ground plane beneath the converter on the component side of the board. In addition, a wide conductor pattern should run directly from Pin 9 to the analog supply common, and a separate wide conductor pattern from Pin 15 to the digital supply common. Analog common (Pin 9) typically carries +8mA.

If the single-point system common cannot be established directly at the converter; a single wide conductor pattern then connects these two pins to the system common. In either case, the common return of the analog input signal should be referred to Pin 9 of the ADC. This prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

If the 20V analog input range is used (etiher bipolar or unipolar), the 10V range input (Pin 13) should be shielded with ground plane to reduce noise pickup. If the bipolar offset input (Pin 12) is not used to externally trim the unipolar offset as shown in Figure 2, connect it to Analog Common (Pin 9).

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC774 as possible. If no trim adjustments are used, the fixed resistors should likewise be as close as possible.

POWER SUPPLY DECOUPLING

Logic and analog power supplies should be bypassed with 10µF tantalum type capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC774 will be driving into a nominal DC input impedance of either 5kΩ or 10kΩ. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

RANGE CONNECTIONS

The ADC774 offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V, and ±10V. If a 10V input range is required, the analog input signal should be connected to Pin 13 of the converter. A signal requiring a 20V range is connected to Pin 14. In either case the other pin of the two is left unconnected. Full-scale and offset adjustmens are described below.

To operate the converter with a 10.24V (2.5mV LSB) or 20.48V (5mV LSB) input range, insert a 120Ω 1% metal-film resistor in series with Pin 13 for the 10.24V range, or a 240Ω 1% metal-film resistor in series with pin 14 for the 20.48V range. Offset adjustments are still perfomed as described below. A fixed metal-film resistor can be used because the input impedance of the ADC774 is trimmed to typically less than ±2% of the nominal value.

CALIBRATION

OPTIONAL EXTERNAL FULL-SCALE AND OFFSET ADJUSTMENTS

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADC774 as shown in Figures 2 and 3 for unipolar and bipolar operation.

CALIBRATION PROCEDURE— UNIPOLAR RANGES

If adjustment of unipolar offset and full scale is not required, replace R_2 with a 50Ω, 1% metal-film resistor and connect Pin 12 to Pin 9, omitting the adjustment network.

If adjustment is required, connect the converter as shown in Figure 2. Sweep the input through the end-point transition voltage (0V + 1/2LSB; +1.22mV for the 10V range, +2.44mV for the 10V range) that causes the output code to be DB0 ON

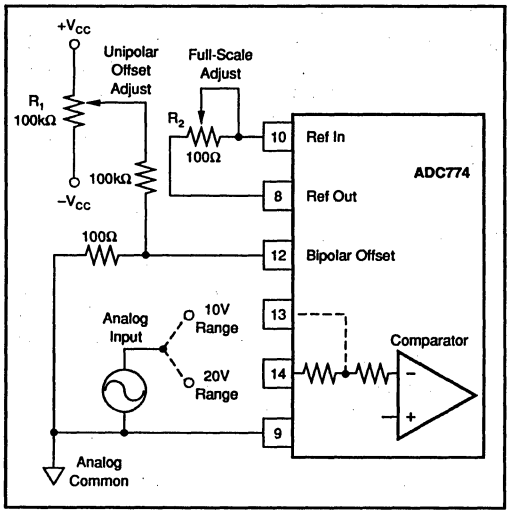


FIGURE 2. Unipolar Configuration.

(high). Adjust potentiometer R_1 until DB0 is alternately toggling ON and OFF with all other bits OFF. Then adjust full scale by applying an input voltage of nominal full-scale value minus 3/2LSB, the value which should cause all bits to be ON. This value is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust potentiometer R_2 until bits DB1-DB11 are ON and DB0 is toggling ON and OFF.

CALIBRATION PROCEDURE—BIPOLAR RANGES

If external adjustments of full-scale and bipolar offset are not required, the potentiometers may be replaced by 50Ω, 1% metal-film resistors.

If adjustments are required, connect the converter as shown in Figure 3. The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage which is

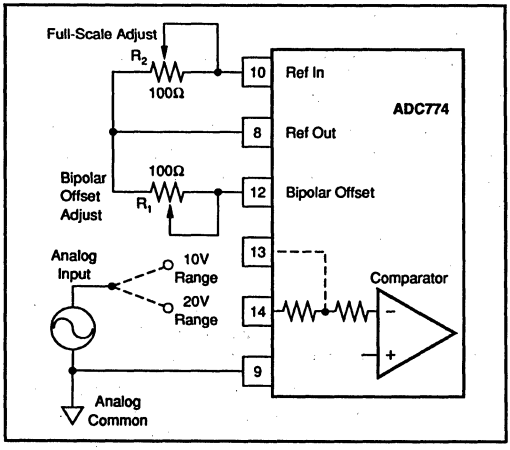


FIGURE 3. Bipolar Configuration.

1/2LSB above the minus full-scale value (–4.9988V for the ±5V range, –9.9976V for the ±10V range). Adjust R_1 for DB0 to toggle ON and OFF with all other bits OFF. To adjust full-scale, apply a DC input signal which is 3/2LSB below the nominal plus full-scale value (+4.9963V for ±5V range, +9.9927V for ±10V range) and adjust R_2 for DB0 to toggle ON and OFF with all other bits ON.

CONTROLLING THE ADC774

The Burr-Brown ADC774 can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready—choosing either 12 bits all at once, or 8 bits followed by 4 bits in a left-justified format. The five control inputs (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$, and CE) are all TTL/CMOS-compatible. The functions of the control inputs are described in Table II. The control function truth table is listed in Table III.

Read footnote 5 to the Electrical Specifications table if using ADC774 to replace the HI774.

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and A_0 are connected to digital common and CE and 12/$\overline{8}$ are connected to V_{LOGIC} (+5V). The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a high-to-low transition of R/$\overline{C}$. The three-state data output buffers are enable when R/$\overline{C}$ is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In either case the R/$\overline{C}$ pulse must remain low for a minimum for 50ns.

Figure 4 illustrates timing when conversion is initiated by and R/$\overline{C}$ pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enable for external access of the data after completion of the conversion. Figure 5 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode the output data from the previous conversion is enable during the positive portion of R/$\overline{C}$. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Timing specifications for stand-alone operation are listed in Table IV.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described below). If A_0 is latched high, the

PIN DESIGNATION	DEFINITION	FUNCTION
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8 or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in two 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSB's or LSB's as determined by the A_0 line.

TABLE II. ADC774 Control Line Functions.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

TABLE III. Control Input Truth Table.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STATUS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STATUS Delay After Data Valid		150	375	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

TABLE IV. Stand-Alone Mode Timing.

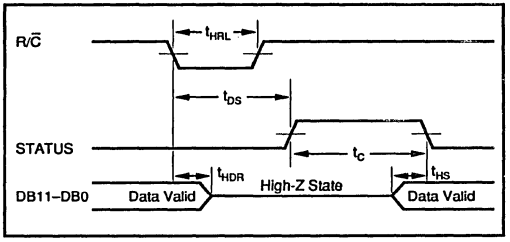


FIGURE 4. R/$\overline{C}$ Pulse Low—Outputs Enabled After Conversion.

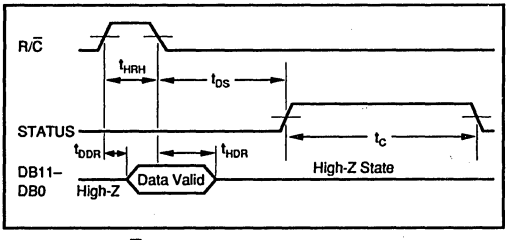


FIGURE 5. R/$\overline{C}$ Pulse High—Outputs Enabled Only While R/$\overline{C}$ Is High.

conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is low. If all 12 bits are read following an 8-bit conversion, the 3 LSBs (DB0–DB2) will be low (logic 0) and DB3 will be high (logic 1). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

CONVERSION START

The converter is commanded to initiate a conversion by a transition occurring on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$) as shown in Table III. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change state simultaneously, and the nominal delay time is the same regardless of which input actually starts conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Figure 6. The specifications for timing are contained in Table V.

The STATUS output shows the current state of the converter by being in a high state only during conversion. During this time the three-state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly causing an incorrect conversion length (8 bits versus 12 bits) for that conversion.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{DSC}	STS Delay from CE		60	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup time	50	20		ns
t_{HSC}	$\overline{CS}$ low during CE high	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE setup	50	0		ns
t_{HRC}	R/$\overline{C}$ low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0			ns
t_{HAC}	A_0 valid during CE high	50	20		ns
t_C	Conversion time				
	12-bit cycle at 25°C		7.5	8	µs
	0 to +75°C			8.5	µs
	–55°C to +125°C			9	µs
	8-bit cycle at 25°C		5	5.3	µs
	0 to +75°C			5.7	µs
	–55°C to +125°C			6	µs
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE setup	50	0		ns
t_{SAR}	R/$\overline{C}$ to CE setup	0			ns
t_{HSR}	$\overline{CS}$ valid after CE low	0			ns
t_{HRR}	R/$\overline{C}$ high after CE low	0			ns
t_{HAR}	A_0 valid after CE low	50			ns
t_{HS}	STS delay after data valid		150	375	ns

TABLE V. Timing Specifications.

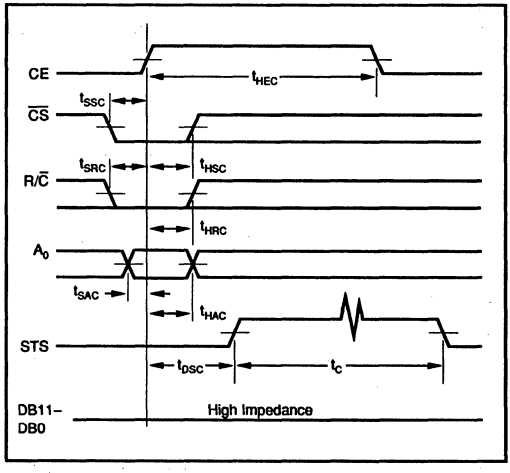


FIGURE 6. Conversion Cycle Timing.

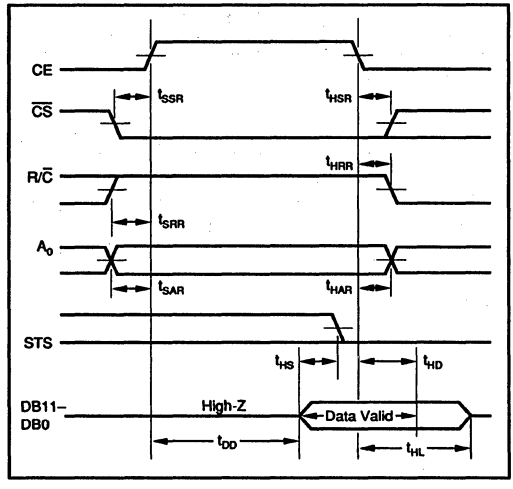


FIGURE 7. Read Cycle Timing.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. Upon satisfaction of these conditions, the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 7 and Table V for timing relationships and specifications.

In most applications the 12/$\overline{8}$ input will be hard-wired in either the high or low condition, although it is fully TTL- and CMOS-compatible and may be actively driven if desired. When 12/$\overline{8}$ is high, all 12 output lines (DB0–DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the A_0 state is ignored.

When $12/\overline{8}$ is low, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest accomplished by the state of A_0 during the read cycle. Connection of the ADC774 to an 8-bit bus for transfer of left-justified data is illustrated in Figure 9. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

When A_0 is low, the byte addressed contains the 8MSBs. When A_0 is high, the byte addressed contains the 4LSBs from the conversion followed by four logic zeros which have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 8. The design of the ADC774 guarantees that the A_0 input may be toggled at any time with no damage to the converter; the outputs which are tied together as illustrated in Figure 9 cannot be enabled at the same time.

In the majority of applications, the read operation will be attempted only after the conversion is complete and the STATUS output has gone low. In those situations requiring the earliest possible access to the data, the read may be started as much as (t_{DD} + t_{HS}) before STATUS goes low. Refer to Figure 7 for these timing relationships.

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 8. 12-Bit Data Format for 8-Bit Systems.

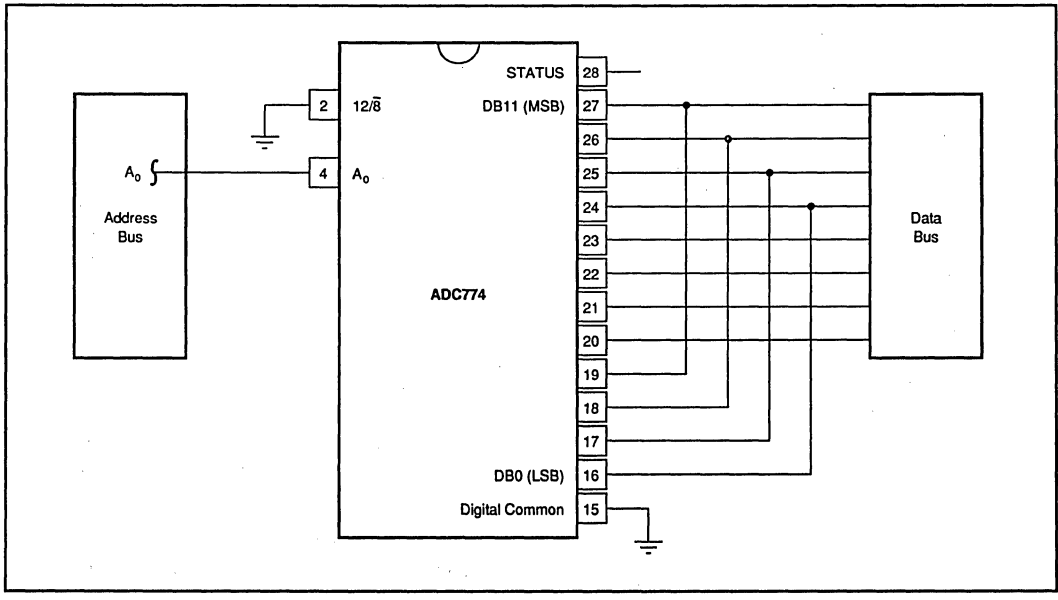


FIGURE 9. Connection to an 8-Bit Bus.

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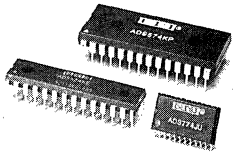


ADS574
ADS774

ADVANCE INFORMATION
SUBJECT TO CHANGE

Microprocessor-Compatible CMOS Sampling ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- **COMPATIBLE WITH ADC574A, ADC674A AND ADC774 SOCKETS**
- **COMPLETE SAMPLING A to D's WITH REFERENCE, CLOCK AND MICROPROCESSOR INTERFACE**
- **FAST ACQUISITION AND CONVERSION:**
  ADS774 at 8µs max
  ADS574 at 25µs max
- **ELIMINATE NEED FOR EXTERNAL SAMPLE/HOLD IN MOST APPLICATIONS**
- **GUARANTEED AC AND DC PERFORMANCE**
- **LOW POWER:**
  ADS574 at 100mW max
  ADS774 at 150mW max
- **PLASTIC OR HERMETIC DIPS (0.3" and 0.6" widths), SOIC, and DIE AVAILABLE**
- **CAN OPERATE FROM SINGLE +5V SUPPLY**

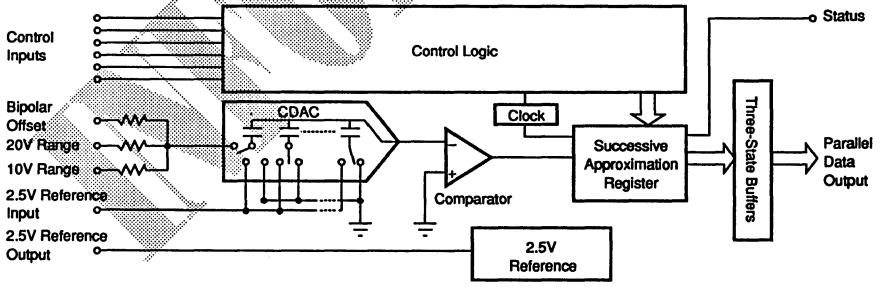
DESCRIPTION

The ADS574 and ADS774 are 12-bit successive approximation analog-to-digital converters using an innovative capacitor array (CDAC) that allows implementation in low-power CMOS technology, and provides inherent sampling. These are drop-in replacements for ADC574A, ADC674A and ADC774 models in most applications, with much lower power consumption, and with internal sampling.

The ADS574 and ADS774 are complete with internal clock, microprocessor interface, three-state outputs, and internal scaling resistors for input ranges of 0V to +10V, 0V to +20V, ±5V, or ±10V. The maximum conversion time for 12-bit conversions (including sample acquisition time) is factory set at 8µs maximum for the ADS774 and 25µs maximum for the ADS574.

User control over the inherent sampling function is provided for designers who want to eliminate the external sample/hold in existing designs.

The ADS574 and ADS774 are available in commercial (0°C to +70°C) and military (–55°C to +125°C) ranges, and require +5V, with –12V or –15V optional, depending on usage. No +15V supply is required. Both are available in 0.3" or 0.6" wide 28-pin plastic or hermetic DIPs, in 28-pin SOICs, and in die form.



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PDS-973A

SPECIFICATIONS

ELECTRICAL

$T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +5V, V_{EE} = −15V to +5V sampling frequency of 40kHz on ADS574 and 117kHz on ADS774; unless otherwise specified.

	ADS574JE/JP/JU/SF/SH ADS774JE/JP/JU/SE/SH			ADS574KE/KP/KU/TF/TH ADS774KE/KP/KU/TE/TH			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
RESOLUTION			12			•	Bits
INPUTS							
ANALOG							
Voltage Ranges: Unipolar		0 to +10, 0 to +20			•		V
Bipolar		±5, ±10			•		V
Impedance: ADS574:							
0 to +10V, ±5V	17.5	25	32.5	•	•	•	kΩ
±10V, 0V to +20V	70	110	150	•	•	•	kΩ
ADS774:							
0 to +10V, ±5V	8.75	12.5	16.25	•	•	•	kΩ
±10V, 0V to +20V	35	55	75	•	•	•	kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$) T_{MIN} to T_{MAX}							
Voltages: Logic 1	+2.0		+5.5	•		•	V
Logic 0	−0.5		+0.8	•		•	V
Current	−5	0.1	+5	•	•	•	µA
Capacitance		5			•		pF
TRANSFER CHARACTERISTICS							
DC ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (adjustable to zero)			±2			•	LSB
Bipolar Offset Error (adjustable to zero)			±10			±4	LSB
Full-Scale Calibration Error [1] (adjustable to zero)			±0.25			•	% of FS [2]
No Missing Codes Resolution (Diff. Linearity)	12			12			Bits
Inherent Quantization Error		±1/2			•		LSB
T_{MIN} to T_{MAX}							
Linearity Error: J, K Grades			±1			±1/2	LSB
S, T Grades			±1			±3/4	LSB
Full-Scale Calibration Error							
Without Initial Adjustment [1]: J, K Grades			±0.47			±0.37	% of FS
S, T Grades			±0.75			±0.5	% of FS
Adjusted to Zero at +25°C: J, K Grades			±0.22			±0.12	% of FS
S, T Grades			±0.5			±0.25	% of FS
No Missing Codes Resolution (Diff. Linearity)	12			12			Bits
AC ACCURACY [3] (F_{IN} = 10kHz for ADS574, F_{IN} = 20kHz for ADS774)							
Spurious Free Dynamic Range	73	78		76	•		dB
Total Harmonic Distortion		−77	−72		•	−75	dB
Signal-to-Noise Ratio	69	72		71	•		dB
Signal-to-(Noise +Distortion) Ratio	68	71		70	•		dB
Intermodulation Distortion		75			•		
ADS574 (F_{IN1} = 10kHz, F_{IN2} = 11.5kHz)							
ADS774 (F_{IN1} = 20kHz, F_{IN2} = 21.5kHz)							
TEMPERATURE COEFFICIENTS [4]							
Unipolar Offset			±5			±2.5	ppm/°C
Max Change			±2			±1	LSB
Bipolar Offset			±10			±5	ppm/°C
Max Change: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration			±45			±25	ppm/°C
Max Change: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration +4.75V < V_{DD} < +5.25V			±1/2			•	LSB

SPECIFICATIONS (CONT)

ELECTRICAL

$T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +5V, V_{EE} = −15V to +5V sampling frequency of 40kHz on ADS574 and 117kHz on ADS774; unless otherwise specified.

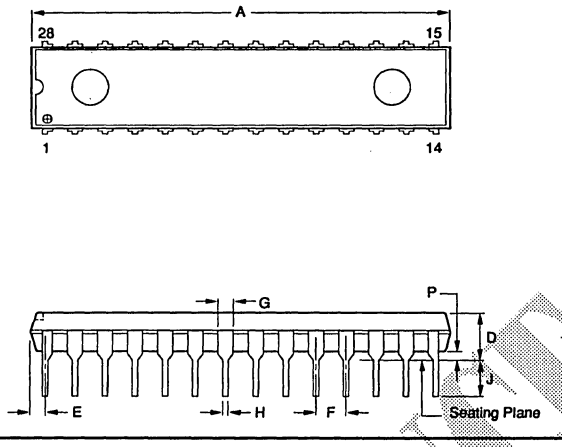
PARAMETER	ADS574JE/JP/JU/SF/SH ADS774JE/JP/JU/SE/SH MIN	TYP	MAX	ADS574KE/KP/KU/TF/TH ADS774KE/KP/KU/TF/TH MIN	TYP	MAX	UNITS
CONVERSION TIME (Including Acquisition Time)							
ADS574 $t_{AQ} + t_C$ at 25°C:							
8-Bit Cycle		16	18		•	•	µs
12-Bit Cycle		22	25		•	•	µs
12-Bit Cycle, T_{MIN} to T_{MAX}		22	25		•	•	µs
ADS574 $t_{AQ} + t_C$ at 25°C:							
8-Bit Cycle		5.5	5.9		•	•	µs
12-Bit Cycle		7.5	8		•	•	µs
12-Bit Cycle, T_{MIN} to T_{MAX}		8	8.5		•	•	µs
SAMPLING DYNAMICS							
Sampling Rate							
ADS574	40			•			kHz
ADS774 at 25°C	125			•			kHz
ADS774, T_{MIN} to T_{MAX}	117			•			kHz
Aperture Delay, t_{AP}							
With V_{EE} = +5V		20			•		ns
With V_{EE} = 0V to −15V							
ADS574		4.0			•		µs
ADS774		1.6			•		µs
Aperture Uncertainty (Jitter)							
With V_{EE} = +5V		300			•		ps, rms
With V_{EE} = 0V to −15V							
ADS574		30			•		ns, rms
ADS774		10			•		ns, rms
OUTPUTS							
DIGITAL (DB_{11} - DB_0, STATUS)							
(Over Temperature Range)							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (I_{SINK} = 1.6mA)					+0.4		V
Logic 1 (I_{SOURCE} = 500µA)	+2.4			•			V
Leakage, Data Bits Only, High-Z State	−5	0.1	+5	•	•	•	µA
Capacitance		5			•		pF
INTERNAL REFERENCE VOLTAGE							
Voltage	+2.4	+2.5	+2.6	•	•	•	V
Source Current Available for External Loads	0.5			•			mA
POWER SUPPLY REQUIREMENTS							
Voltage: V_{EE} (5)	−16.5		V_{DD}	•		•	V
V_{DD}	+4.5		+5.5	•		•	V
Current:							
ADS574: I_{EE} (5) (V_{EE} = −15V)		−1			•		mA
I_{DD}		+13	+20		•	•	mA
ADS774: I_{EE} (5) (V_{EE} = −15V)		−1			•		mA
I_{DD}		+15	+30		•	•	mA
Power Dissipation (T_{MIN} to T_{MAX})							
ADS574 (V_{EE} = 0V to +5V)		65	100		•	•	mW
ADS774 (V_{EE} = 0V to +5V)		75	150		•	•	mW
TEMPERATURE RANGE							
Specification: J, K Grades	0		+70	•		•	°C
S, T Grades	−55		+125	•		•	°C

*Same specification as ADS574JE/JP/JU/SF/SH or ADS774JE/JP/JU/SF/SH.

NOTES: (1) With fixed 50Ω resistor from REF OUT to REF IN. This parameter is also adjustable to zero at +25°C. (2) FS in this specification table means Full Scale Range. That is, for a ±10V input range, FS means 20V; for a 0 to +10V range, FS means 10V. (3) Based on using V_{EE} = +5V, which starts a conversion immediately upon a convert command. Using V_{EE} = 0V to −15V makes the ADS574/ADS774 emulate standard ADS574 operation. In this mode, the internal sample/hold acquires the input signal after receiving the convert command, and does not assume that the input level has been stable before the convert command arrives. (4) Using internal reference. (5) V_{EE} is optional, and is only used to set the mode for the internal sample/hold. When V_{EE} = −15V, I_{EE} = −1mA typ; when V_{EE} = 0V, I_{EE} = ±5µA typ; when V_{EE} = +5V, I_{EE} = +167µA typ.

MECHANICAL

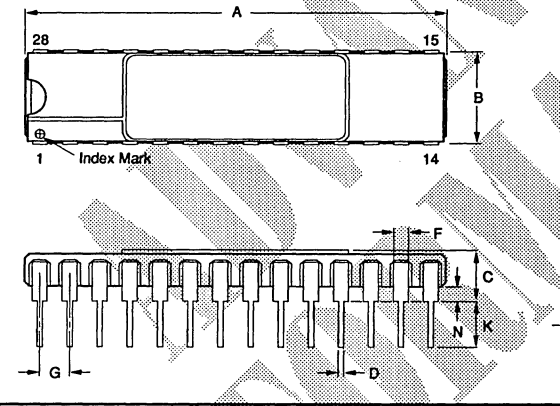
E Package — 0.3" Wide 28-Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.255	1.355	31.88	34.42
B	.270	.290	6.86	7.37
D	.150	.170	3.81	4.32
E	.010	.080	0.25	2.03
F	.100 BASIC		2.54 BASIC	
G	.045	.055	1.14	1.40
H	.016	.020	0.41	0.51
J	.125	N/A	3.18	N/A
K	.300 BASIC		7.62 BASIC	
M	0°	15°	0°	15°
N	.008	.015	0.20	0.38
P	.020	.040	0.51	1.02

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

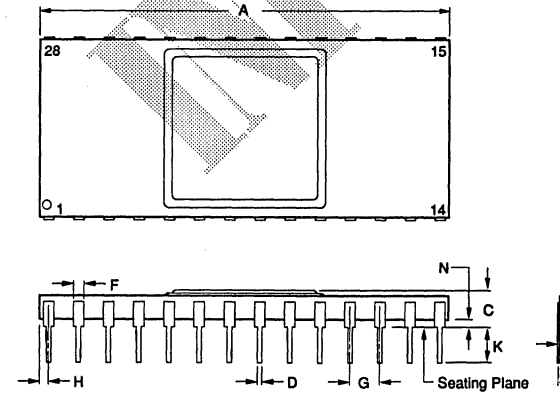
F Package — 0.3" Wide 28-Pin Hermetic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.388	1.412	35.26	35.86
B	.300	.320	7.62	8.13
C	—	.160	—	4.06
D	.016	.020	0.41	0.51
F	.050 BASIC		1.27 BASIC	
G	.095	.105	2.41	2.67
J	.009	.012	0.23	0.30
K	.125	.180	3.18	4.57
L	.290	.310	7.37	7.87
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

H Package — 0.6" Wide 28-Pin Hermetic DIP

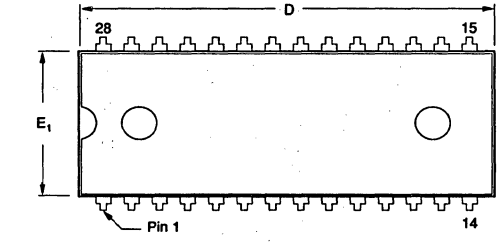


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.386	1.414	35.20	35.92
C	.115	.175	2.92	4.45
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.036	.064	0.91	1.63
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

MECHANICAL

P Package — 0.6" Wide 28-Pin Plastic DIP

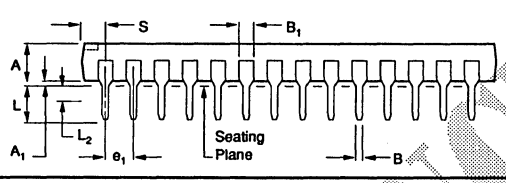


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A(1)	.169	.200	4.29	5.08
A1(1)	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D(1)	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1(1)	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

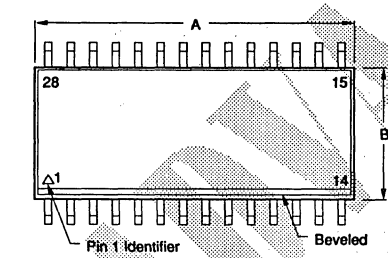
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
S(1)	.040	.080	1.02	2.03

(1) Not JEDEC Standard

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

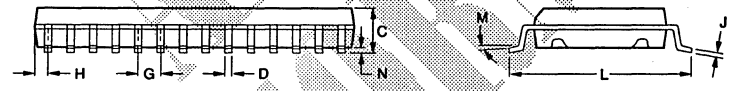


U Package — 28-Pin Plastic SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.700	.716	17.78	18.19
B	.288	.302	7.26	7.67
C	.093	.109	2.36	2.77
D	.016 BASIC		0.41 BASIC	
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.398	.414	10.11	10.52
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

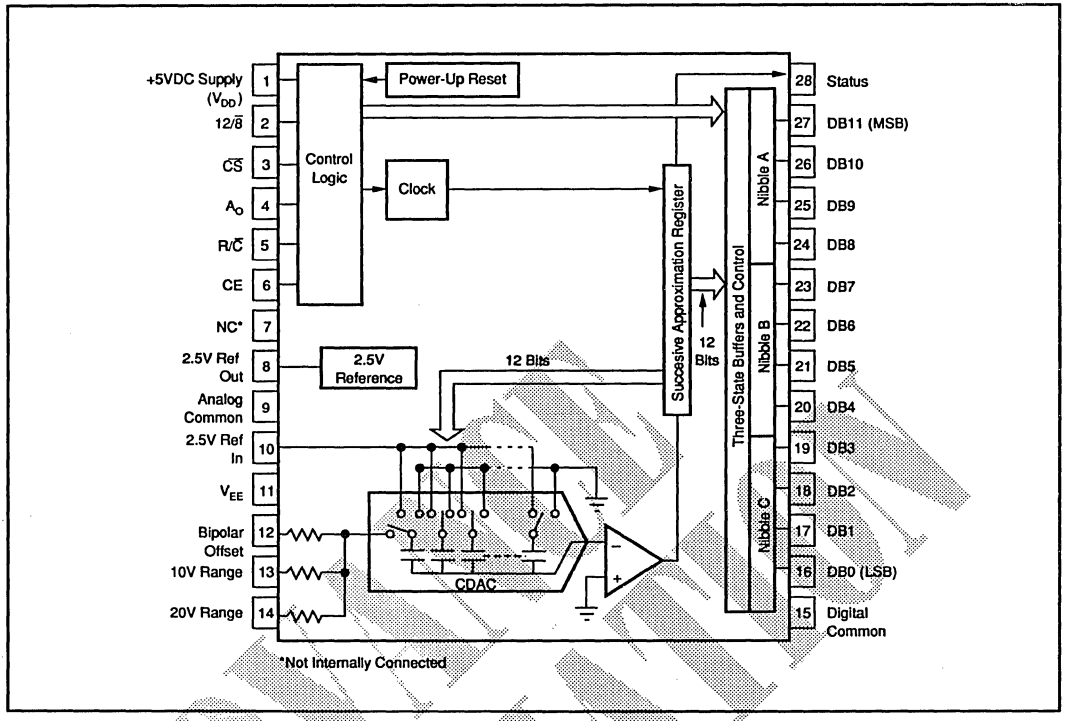
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.



ORDERING INFORMATION

MODEL	PACKAGE	CONVERSION TIME	TEMPERATURE RANGE	LINEARITY ERROR
ADS574JE	0.3" Plastic DIP	25µs	0°C to 70°C	±1LSB
ADS574KE	0.3"Plastic DIP	25µs	0°C to 70°C	±1/2LSB
ADS574JP	0.6" Plastic DIP	25µs	0°C to 70°C	±1LSB
ADS574KP	0.6"Plastic DIP	25µs	0°C to 70°C	±1/2LSB
ADS574JU	SOIC	25µs	0°C to 70°C	±1LSB
ADS574KU	SOIC	25µs	0°C to 70°C	±1/2LSB
ADS574SF	0.3" Ceramic DIP	25µs	–55°C to 125°C	±1LSB
ADS574TF	0.3" Ceramic DIP	25µs	–55°C to 125°C	±1/2LSB
ADS574SH	0.6" Ceramic DIP	25µs	–55°C to 125°C	±1LSB
ADS574TH	0.6" Ceramic DIP	25µs	–55°C to 125°C	±1/2LSB
ADS774JE	0.3" Plastic DIP	8µs	0°C to 70°C	±1LSB
ADS774KE	0.3" Plastic DIP	8µs	0°C to 70°C	±1/2LSB
ADS774JP	0.6" Plastic DIP	8µs	0°C to 70°C	±1LSB
ADS774KP	0.6" Plastic DIP	8µs	0°C to 70°C	±1/2LSB
ADS774JU	SOIC	8µs	0°C to 70°C	±1LSB
ADS774KU	SOIC	8µs	0°C to 70°C	±1/2LSB
ADS774SF	0.3" Ceramic DIP	8µs	–55°C to 125°C	±1LSB
ADS774TF	0.3" Ceramic DIP	8µs	–55°C to 125°C	±1/2LSB
ADS774SH	0.6" Plastic DIP	8µs	–55°C to 125°C	±1LSB
ADS774TH	0.6" Plastic DIP	8µs	–55°C to 125°C	±1/2LSB

CONNECTION DIAGRAM



Binary (BIN) Output		Input Voltage Range and LSB Values			
Analog Input Voltage Range	Defined As:	±10V	+5V	0V to +10V	0V to +20V
One Least Significant Bit (LSB)	FSR / 2^n n = 8 n = 12	20V / 2^n 78.13mV 4.88mV	10V / 2^n 39.06mV 2.44mV	10V / 2^n 39.06mV 2.44mV	20V / 2^n 78.13mV 4.88mV
Output Transition Values FFE_H to FFF_H $7FFF_H$ to 800_H 000_H to 001_H	+ Full-Scale Calibration Midscale Calibration (Bipolar Offset) Zero Calibration (– Full-Scale Calibration)	+10V – 3/2LSB 0 – 1/2LSB –10V + 1/2LSB	+5V – 3/2 LSB 0 – 1/2LSB –5V + 1/2LSB	+10V – 3/2LSB +5V – 1/2LSB 0 to +1/2LSB	+10V – 3/2LSB ±10V – 1/2LSB 0 to +1/2LSB

TABLE I. Input Voltages, Transition Values, and LSB Values.

DESIGNATION	DEFINITION	FUNCTION
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8- or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in two 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSBs or LSBs as determined by the A_0 line.

TABLE II. Control Line Functions.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeroes

TABLE III. Control Input Truth Table.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	25			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	100			ns
t_{DDR}	Data Access Time			150	ns

TABLE IV. Stand-Alone Mode Timing. ($T_A = T_{MIN}$ to T_{MAX}).

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{DSC}	STS delay from CE		60	200	ns
t_{HEC}	CE Pulse width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE setup	50	20		ns
t_{HSC}	$\overline{CS}$ low during CE high	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE setup	50	0		ns
t_{HRC}	R/$\overline{C}$ low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0			ns
t_{HAC}	A_0 valid during CE high	50	20		ns
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE setup	0			ns
t_{SAR}	A_0 to CE setup	50	25		ns
t_{HSR}	$\overline{CS}$ valid after CE low	0			ns
t_{HRR}	R/$\overline{C}$ high after CE low	0			ns
t_{HAR}	A_0 valid after CE low	50			ns

TABLE V. Timing Specifications, Fully Controlled Operation. ($T_A = T_{MIN}$ to T_{MAX}).

SYMBOL	PARAMETER	T_A	ADS574			ADS774			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$t_{AQ} + t_C$	12-bit Acquistion and Conversion	25°C		22	25		7.5	8	µs
		T_{MIN} to T_{MAX}			25			8.5	µs
	8-bit Acquistion and Conversion	25°C		16	18		5.5	5.9	µs
		T_{MIN} to T_{MAX}			18			6.3	µs
t_{HS}	STS Delay After Data Valid	T_{MIN} to T_{MAX}		400	1000		150	375	ns

TABLE VI. Conversion Timing.

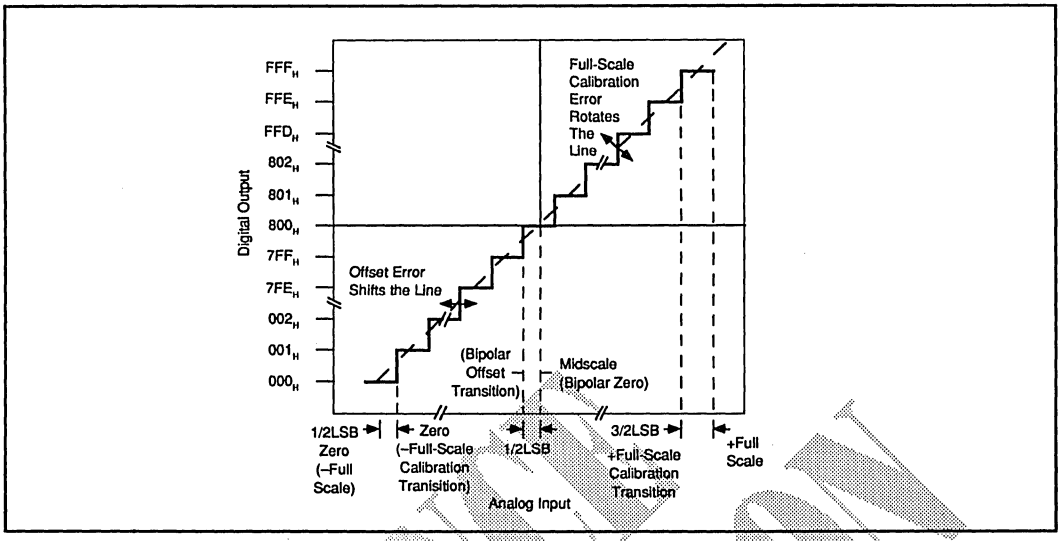


FIGURE 1. ADS574/ADS774 Transfer Characteristic Terminology.

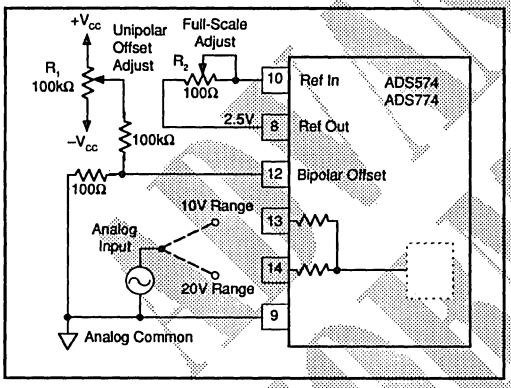


FIGURE 2. Unipolar Configuration.

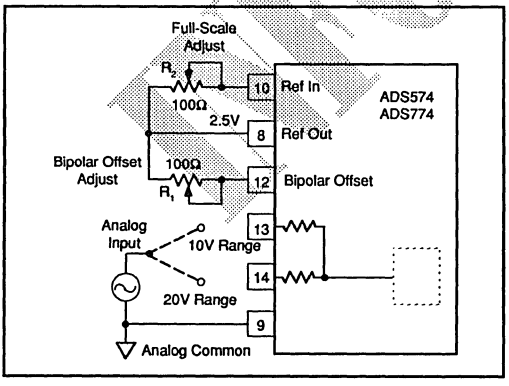


FIGURE 3. Bipolar Configuration.

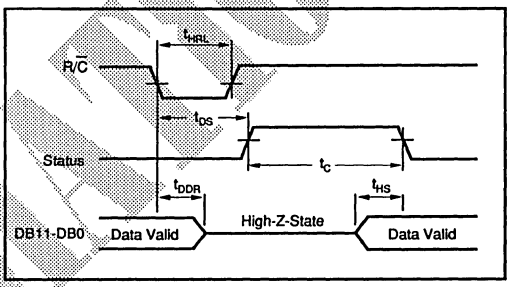


FIGURE 4. R/$\overline{C}$ Pulse Low—Outputs Enabled After Conversion.

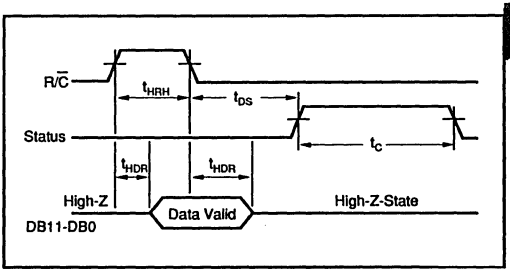


FIGURE 5. R/$\overline{C}$ Pulse High — Outputs Enabled Only While R/$\overline{C}$ Is High.

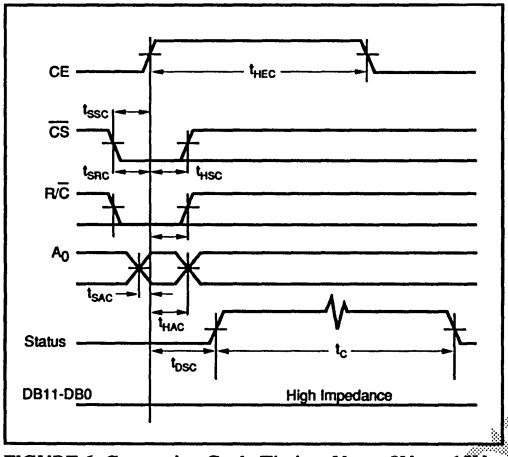


FIGURE 6. Conversion Cycle Timing, V_{EE} = 0V to –15V (ADC574/774 Emulation Mode).

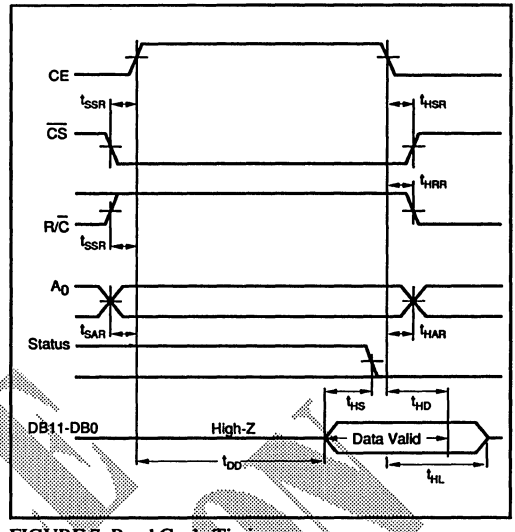


FIGURE 7. Read Cycle Timing.

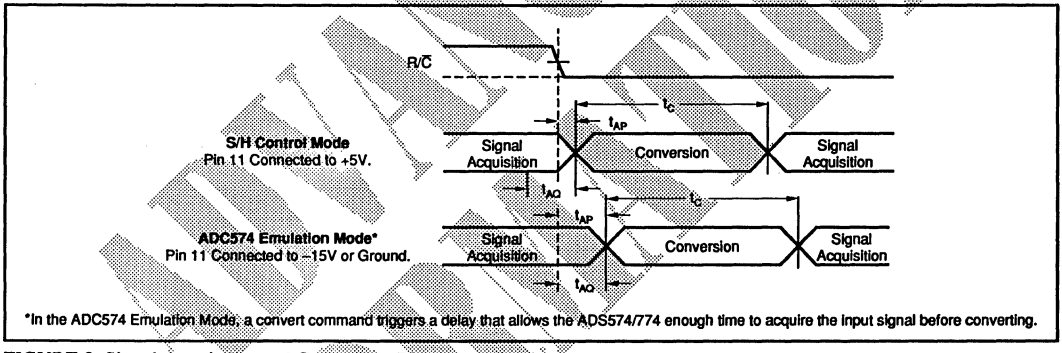


FIGURE 8. Signal Acquisition and Conversion Timing.

BURR-BROWN®

ADS602

12-Bit 1MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- LOW LINEARITY ERROR
- SAMPLE RATE: 1MHz
- INPUT RANGES: ±5V, 0V to +10V
- COMPLETE SUBSYSTEM: Contains Sample/Hold and Reference
- 32-PIN CERAMIC DIP PACKAGE

APPLICATIONS

- DIGITAL SIGNAL PROCESSING
- HIGH-SPEED DATA ACQUISITION SYSTEMS
- MEDICAL INSTRUMENTATION
- ANALYTICAL INSTRUMENTATION
- TEST AND IMAGING SYSTEMS
- WAVEFORM ANALYZERS

DESCRIPTION

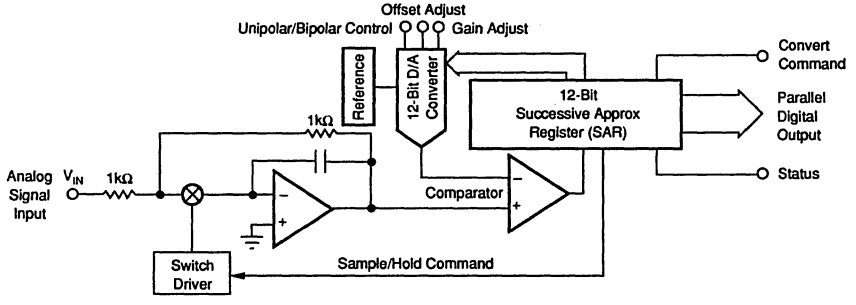
The ADS602 is a high-speed successive approximation analog-to-digital converter with internal sample/hold amplifier. This unique design utilizes a bipolar technology with on-chip thin film resistors to preserve analog accuracy and a high-speed CMOS chip to perform digital logic control. Outstanding linearity, noise, and dynamic range are achieved by this converter design. The ADS602 is thoroughly tested for dynamic performance.

The ADS602 is complete with internal reference, clock, and comparator and is packaged in a 32-pin ceramic DIP. Sample rate is set at the factory to 1MHz. Performance is guaranteed with no missing codes over the input voltage, power supply, and operating temperature range. The gain and offset errors are laser trimmed to specification. Optionally they may be externally adjusted to zero.

The user can switch between unipolar (0V to +10V) and bipolar (±5V) operation through one digital logic level input.

Output codes are available in complementary binary for unipolar inputs and complementary offset binary for bipolar inputs.

All digital input and output are TTL-compatible. Power supply requirements are ±15V and +5V.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1054

SPECIFICATIONS

ELECTRICAL

T_{CASE} = +25°C, 1MHz sampling rate, $\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, and 6-minute warm-up in a normal convection environment unless otherwise noted.

PARAMETER	CONDITIONS	ADS602JG MIN	ADS602JG TYP	ADS602JG MAX	ADS602KG MIN	ADS602KG TYP	ADS602KG MAX	UNITS
RESOLUTION				12			*	Bits
ANALOG CHARACTERISTICS								
INPUTS								
Voltage Ranges: Bipolar	Full Scale (FSR) [1, 2]	–5		+5	*		*	V
Unipolar	Full Scale (FSR) [1, 2]	0		+10	*		*	V
Input Resistance			1			*		kΩ
Input Capacitance			5	10		*	*	pF
TRANSFER CHARACTERISTICS								
STATIC ACCURACY								
Gain Error [3, 4]			±0.2	±0.3		±0.1	±0.2	% of FSR
Input Offset Error [3, 4]: Unipolar			±0.1	±0.8		*	±0.4	% of FSR
Bipolar			±0.1	±0.6		*	±0.4	% of FSR
Integral Linearity Error			1.2	1.5		0.9	1.25	LSB
Differential Linearity Error			1.2	1.5		0.9	1.25	LSB
No Missing Codes			Guaranteed			*		
Power Supply Rejection of Offset and Gain	$\Delta \pm V_{CC}$ = ±10%		±0.0036	0.5		*	*	%FSR/%V_{CC}
	$\Delta \pm V_{DD}$ = ±10%		±0.001	0.5		*	*	%FSR/%V_{DD}
CONVERSION CHARACTERISTICS								
Sample Rate	Without User Adjustment	DC		1M	*		*	samples/s
Power Supply Rejection of Conversion Time	$\Delta +V_{DD}$ = ±5%		±1			*		ns/%V_{DD}
DYNAMIC CHARACTERISTICS (The sampling frequency [f_S] = 1MHz and the input signal level = –0.5dB, unless otherwise stated.)								
Differential Linearity Error[5]	f_C = 480kHz, 68% of All Codes		0.35			0.25		LSB
	99% of All Codes		0.6			0.5		LSB
	100% of All Codes		1.2			0.9	1.25	LSB
Spurious Free Dynamic Range	f_C = 10kHz		–74			–86	–76	dB
	f_C = 480kHz		–68			–73	–70	dB
Total Harmonic Distortion[6]	f_C = 10kHz		–79			–83	–75	dBc
	f_C = 480kHz		–70			–72	–70	dBc
Two-Tone Intermodulation Distortion [6, 7]	f_C = 90kHz and 110kHz (–6.5dB)		–77			*		dBc
Signal-to-Noise and Distortion	f_C = 10kHz		71		70	72		dB
(SINAD) Ratio	f_C = 480kHz		63		64	67		dB
Signal-to-Noise Ratio (SNR)	f_C = 10kHz		71		70	73		dB
	f_C = 480kHz		67		67	69		dB
Analog Input Bandwidth (–3dB)								
Small Signal	–20dB Input		16			*		MHz
Full Power	0dB Input		4			*		MHz
DIGITAL CHARACTERISTICS								
INPUT								
Logic Family			TTL-Compatible CMOS		*	*	*	
Convert Command Logic Voltages	Logic Low	0		+0.8	*		*	V
	Logic High	+2		$+V_{DD}$	*		*	V
Convert Command Currents	Logic Low			–150			*	µA
Convert Command			High Level When Converting		*	*	*	
OUTPUT								
Logic Family			TTL-Compatible CMOS		*	*	*	
Bits 1 through 12, Status	Logic Low, I_{OL} = 3.2mA		+0.1	+0.4		*	*	V
	Logic High, I_{OH} = –1mA	+2.7	+4.9		*	*		V
Internal Clock Frequency			17			*		MHz
Status			Low Level When Data Valid		*	*	*	
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		–14.25	–15	–15.75	*	*	*	V
$+V_{DD}$		+4.75	+5	+5.25	*	*	*	mA
Supply Currents: $+I_{CC}$	Operating		26	30		*	*	mA
$-I_{CC}$			–110	–140		*	*	mA
$+I_{DD}$			60	80		*	*	mA
Power Consumption	Operating		2.3	2.8		*	*	W
Thermal Resistance, θ_{JC}[8]			8.7			*		°C/W

* Specification same as ADS602JG.

SPECIFICATIONS (CONT)

ELECTRICAL (FULL TEMPERATURE SPECIFICATIONS)

$\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, and 6-minute warm-up in a normal convection environment unless otherwise noted.

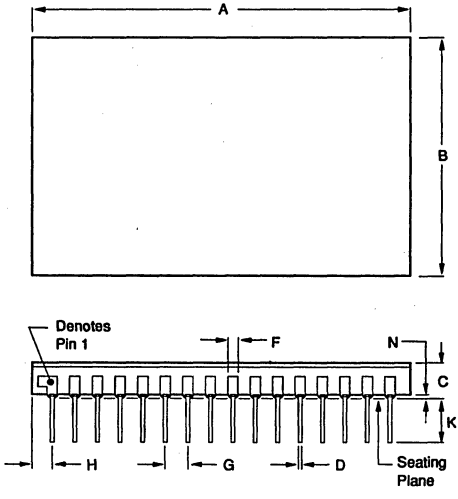
PARAMETER	CONDITIONS	ADS602JG MIN	ADS602JG TYP	ADS602JG MAX	ADS602KG MIN	ADS602KG TYP	ADS602KG MAX	UNITS
TEMPERATURE RANGE SPECIFICATION	T_{CASE}	0		+70	*		*	°C
TRANSFER CHARACTERISTICS								
STATIC ACCURACY								
Gain Error [4]			±0.2	±0.5		±0.1	±0.4	% of FSR
Input Offset Error [4]: Unipolar			±0.1	±0.8		*	±0.4	% of FSR
Bipolar			±0.1	±0.6		*	±0.4	% of FSR
Integral Linearity Error			1.25	1.5		1	1.25	LSB
Differential Linearity Error			1.25	1.5		1	1.25	LSB
No Missing Codes			Guaranteed			*		
Power Supply Rejection of Offset and Gain			±0.0036	0.5		*	*	%FSR/%V_{CC}
			±0.001	0.5		*	*	%FSR/%V_{DD}
CONVERSION CHARACTERISTICS								
Sample Rate	Without User Adjustment	DC		1M	*		*	samples/s
Power Supply Rejection of Conversion Time	Δ $+V_{DD}$ = ±5%		±1			*		ns/%V_{DD}
DYNAMIC CHARACTERISTICS (The sampling frequency [f_S] = 1MHz and the input signal level = –0.5dB, unless otherwise stated.)								
Differential Linearity Error	f_C = 480kHz, 68% of All Codes		0.35			0.25		LSB
	99% of All Codes		0.7			0.6		LSB
	100% of All Codes		1.3			1	1.25	LSB
Spurious Free Dynamic Range	f_C = 10kHz		73			85	71	dB
	f_C = 480kHz		62			65		dB
Total Harmonic Distortion	f_C = 10kHz		–81			–83	–70	dBc
	f_C = 480kHz		–63			–65		dBc
Two-Tone Intermodulation Distortion [7]	f_C = 90kHz and 110kHz (–6.5dB)		–77			–79		dBc
Signal-to-Noise and Distortion	f_C = 10kHz		71		68	70		dB
(SINAD) Ratio	f_C = 480kHz		63			64		dB
Signal-to-Noise Ratio (SNR)	f_C = 10kHz		71		70	73		dB
	f_C = 480kHz		67		67	69		dB
Analog Input Bandwidth (–3dB)								
Small Signal	–20dB Input		16			*		MHz
Full Power	0dB		4			*		MHz
DIGITAL CHARACTERISTICS								
INPUT								
Logic Family			TTL-Compatible CMOS		*	*	*	
Convert Command Logic Voltages	Logic Low	0		+0.8	*		*	V
	Logic High	+2		$+V_{DD}$	*		*	V
Convert Command Currents	Logic Low			–150			*	µA
Convert Command			High Level When Converting		*	*	*	
OUTPUT								
Logic Family			TTL-Compatible CMOS		*	*	*	
Bits 1 through 12, Status	Logic Low, I_{OL} = 3.2mA		+0.1	+0.4		*	*	V
	Logic High, I_{OH} = –1mA	+2.7	+4.9		*	*		V
Internal Clock Frequency			17			*		MHz
Status			Low Level When Data Valid		*	*	*	
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		–14.25	–15	–15.75	*	*	*	V
$+V_{DD}$		+4.75	+5	+5.25	*	*	*	mA
Supply Currents: $+I_{CC}$	Operating		26	30		*	*	mA
$-I_{CC}$			–110	–140		*	*	mA
$+I_{DD}$			60	80		*	*	mA
Power Consumption	Operating		2.3	2.8		*	*	W
Thermal Resistance, θ_{JC} [8]			8.7			*		°C/W

* Specification same as ADS602JG.

NOTES: (1) Over or under range on the analog input results in constant maximum or minimum digital output. (2) FSR = Full Scale Range. (3) Adjustable to zero. (4) If gain and offset adjust pins are not used, they should be grounded. (5) See Typical Performance Curves. (6) dBc = level referred to carrier input signal = –0.5dB of full scale; f_C = input frequency, f_S = sampling frequency. (7) IMD is referred to the large of the two input test signals. If referred to the peak envelope signal (=0dB), the intermodulation products will be 6dB lower. (8) Temperature ranges refer to case temperature. Thermal resistance was measured on a small (5" diameter) handwired circuit board, with the test device in a zero-insertion-force socket. Thermal resistance will be lower if the ADS602 is soldered into the PC board, a ground plane is used directly underneath the package, multiple PC board layers are used, or forced air cooling is employed. Use heat sinking if necessary to keep the case at specified and operating temperatures.

MECHANICAL

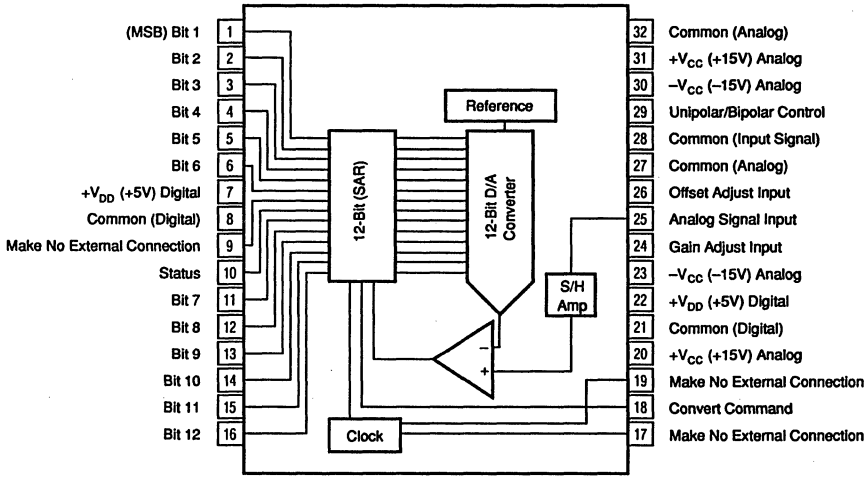
G Package — 32-Pin Ceramic Bottom-Braze



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.678	1.712	42.62	43.48
B	1.079	1.101	27.41	27.97
C	.180	.210	4.57	5.33
D	.016	.020	.41	.51
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.089	.106	2.26	2.69
J	.009	.012	.23	.30
K	.200	.210	5.08	5.33
L	.900 BASIC		22.86 BASIC	
N	.015	.035	.38	.89

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	±18V
$+V_{DD}$	+7V
Digital Inputs	+5.5V
Analog Inputs	$\pm V_{CC}$
Case Temperature	+125°C
Junction Temperature	+150°C
Storage Temperature	–65°C to +150°C

Stresses above these ratings may permanently damage the device.

ORDERING INFORMATION

ADS602 ( ) G

Basic Model Number

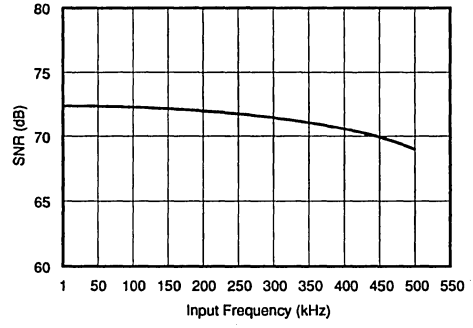
Performance Grade Code
J, K: 0°C to +70°C Case Temperature

Package Code
G: Ceramic Bottom Braze

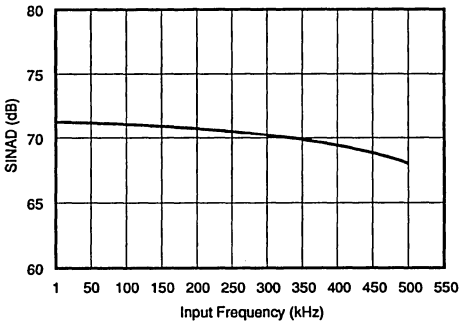
TYPICAL PERFORMANCE CURVES

$\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, 1MHz sampling rate, 6-minute warmup, and T_C = +25°C unless otherwise noted.

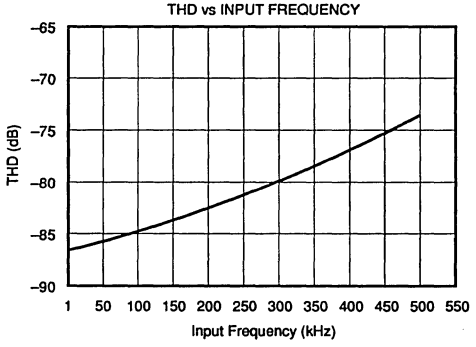
SNR vs INPUT FREQUENCY



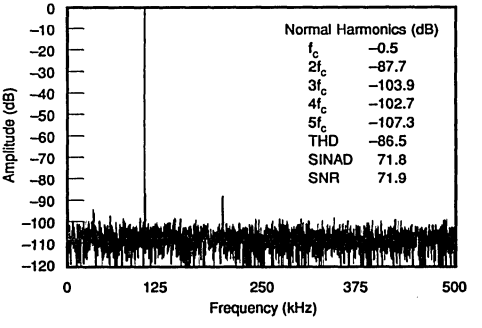
SINAD vs INPUT FREQUENCY



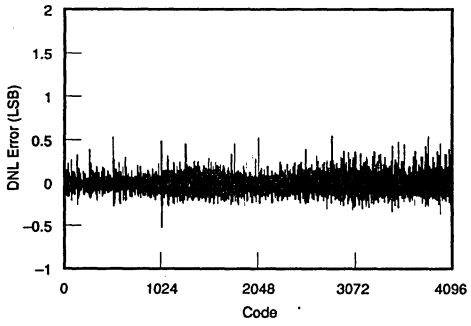
THD vs INPUT FREQUENCY



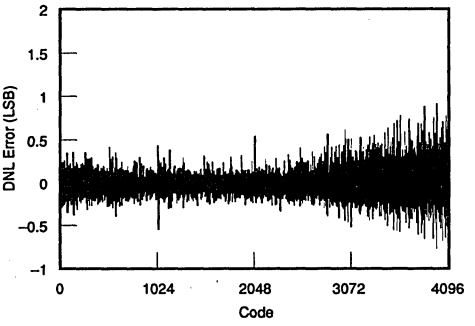
100kHz HARMONIC DISTORTION
(4096 Points)



100kHz DIFFERENTIAL NON-LINEARITY



480kHz DIFFERENTIAL NON-LINEARITY



PIN DEFINITIONS

PIN NUMBER	DESIGNATION	DESCRIPTION
1-6 and 11-16	Bit 1 to Bit 12	12-bit parallel output data.
10	Status	Conversion status strobe is high during data conversion, low when parallel data is valid.
18	Convert Command	High transition starts conversion, and should remain high during conversion. Low will reset clock and SAR logic. Rising edge may be used to latch data from previous conversion.
24	Gain Adjust Input	Allows gain error to be externally adjusted to zero. Ground this pin if it is not used.
25	Analog Signal Input	Signal input to internal S/H amplifier.
26	Offset Adjust Input	Allows offset error to be externally adjusted to zero. Ground this pin if it is not used.
29	Unipolar/Bipolar Control	Ground on this pin engages unipolar operation (0V to +10V). Leaving this pin open engages bipolar (±5V).

The ADS602 is a sampling A/D converter that employs a successive approximation architecture. The ideal transfer function for an ADS602 in the bipolar mode is described in Figure 1. Initial gain and offset errors may be adjusted to zero, gain drift over temperature rotates the transfer function about –full scale end point, and offset drift shifts the transfer function left or right over the operating temperature range. Integral linearity error is the deviation of an actual bit transition from the best fit straight line transfer function of the converter. A differential linearity error of 0.012% means that the width of each bit step over the range of the converter is 1LSB, ±0.5LSB. The ADS602 is guaranteed to have no missing codes over its temperature range.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CONNECTION

The basic connection for the ADS602 is shown in Figure 2. It is shown connected for ±5V bipolar operation. For unipolar operation, pin 29 should be grounded.

INTERFACING

The ADS602 has an impedance of approximately 1k; therefore, to maintain gain accuracy it must be driven from a low impedance source. The digital output lines should be buffered by a latch such as the 74AS574. These three-state drivers can then be connected directly to the data bus.

LAYOUT PRECAUTIONS

The ADS602 is a high-speed sampling analog-to-digital converter which requires more attention to circuit board layout than general purpose lower speed A/D converters.

The ADS602 has two pins for analog common, two pins for digital common, and two pins for each power supply input. Each pair of these pins must be connected together since they are not connected together internally. Connecting all commons to a ground plane close to the ADS602 is the best method to maximize performance. The ground plane minimizes noise and provides additional heat dissipation.

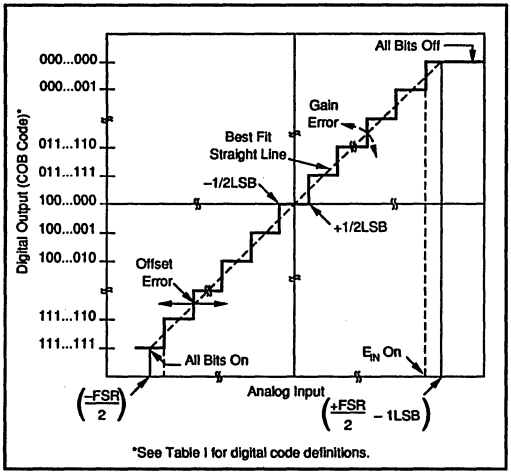


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

ANALOG INPUT VOLTAGE RANGE	±5V	0V TO +10V
Code Designation	COB (1)	CSB (2)
One Least Significant Bit (LSB)	2.44mV	2.44mV
Transition Values MSB LSB (3)		
111...111 / 111...110	–5V + 1/2LSB	0V + 1/2LSB
100...000 / 011...111	–1/2LSB	+5 – 1/2LSB
000...001 / 000...000	+5 – 3/2LSB	10V – 3/2LSB

NOTES: (1) COB = complementary offset binary. (2) CSB = complementary straight binary. (3) Voltages given are the nominal value for the transition from the next code.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

POWER SUPPLY DECOUPLING AND POWER SUPPLY SENSITIVITY

The +15V and +5V power supply pins should be bypassed with a 10µF tantalum capacitor as shown in Figure 2. Pin 30 requires bypassing with a 150µF tantalum capacitor. These capacitors should be located close to the ADS602 supply pins. Ceramic 0.01µF bypass capacitors have been provided internally for more effective bypassing and need not be added externally.

Changes in the DC power supply voltages will affect accuracy. Regulated power supplies with 1% or less ripple are recommended for use with the ADS602. Power supply decoupling helps to keep ripple low.

POWER DISSIPATION

The ADS602 dissipates approximately 2.3W. The package has a junction-to-case thermal resistance (θ_{JC}) of 8.7°C/W and a case-to-ambient thermal resistance (θ_{CA}) of 13.7°C/W in a normal convection environment.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and offset errors may be trimmed to zero using external trim potentiometers as shown in Figure 2. Multiturn potentiometers with 100ppm/°C temperature coefficient are recommended for minimum drift. If the gain adjust or offset adjust pins are not used, they must be grounded to meet the specified accuracy.

DYNAMIC PERFORMANCE TESTING

The ADS602 is a high performance sampling A/D converter and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a fast Fourier transform (FFT) to the ADC digital output will provide data on important dynamic performance parameters.

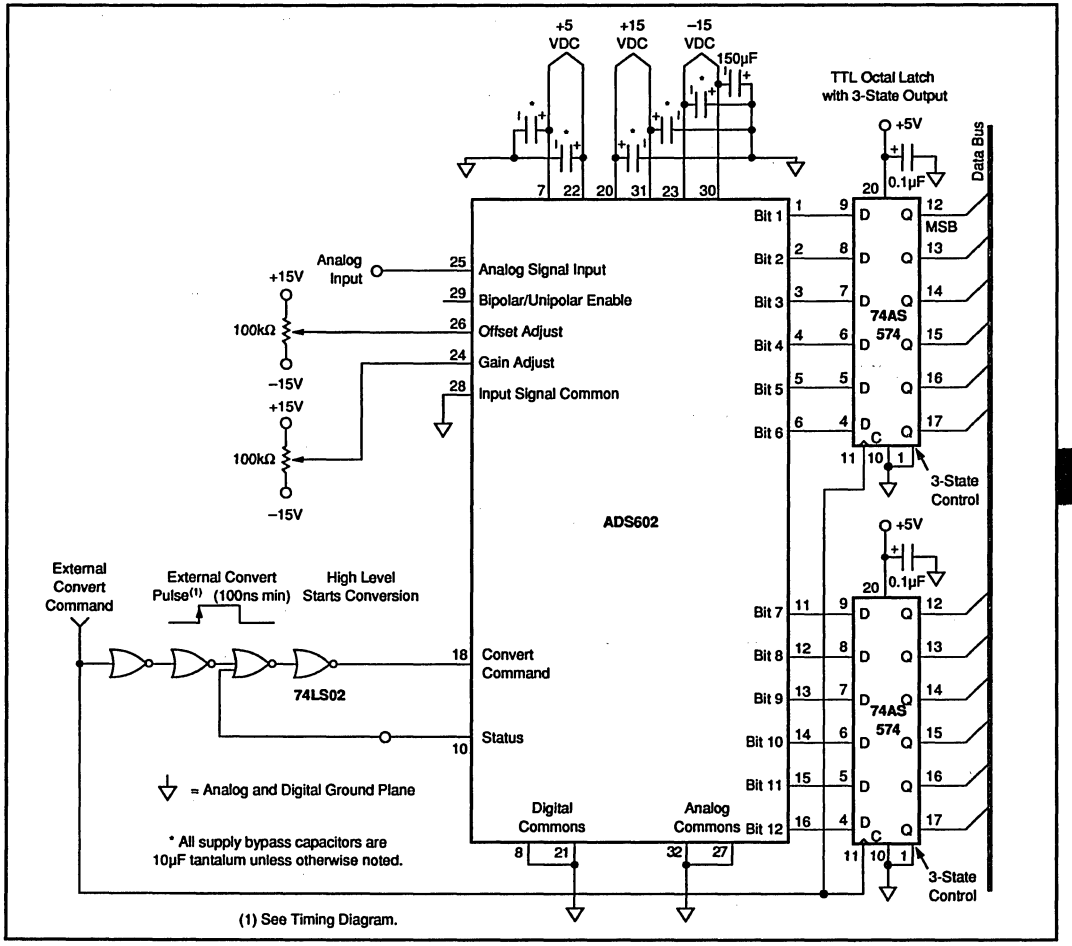


FIGURE 2. ADS602 Application Circuit.

Dynamic Performance Definitions

1. Signal-to-Noise-and-Distortion Ratio (SINAD):

$$10 \log \frac{\text{sinewave signal power}}{\text{noise + harmonic power (first 9 harmonics)}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{sinewave signal power}}{\text{noise power}}$$

3. Total Harmonic Distortion (THD):

$$10 \log \frac{\text{harmonic power (first 9 harmonics)}}{\text{sinewave signal power}}$$

4. Spurious Free Dynamic Range (SFDR):

$$10 \log \frac{\text{largest harmonic power}}{\text{sinewave signal power}}$$

5. Intermodulation Distortion (IMD):

$$10 \log \frac{\text{highest IMD product power (to 5th order)}}{\text{sinewave signal power}}$$

IMD is referred to the larger of the test signals f1 or f2. Five "bins" either side of peak are used for calculation of fundamental and harmonic power. The "0" frequency bin (DC) is not included in these calculations as it is of little importance in dynamic signal processing applications.

TIMING CONSIDERATIONS

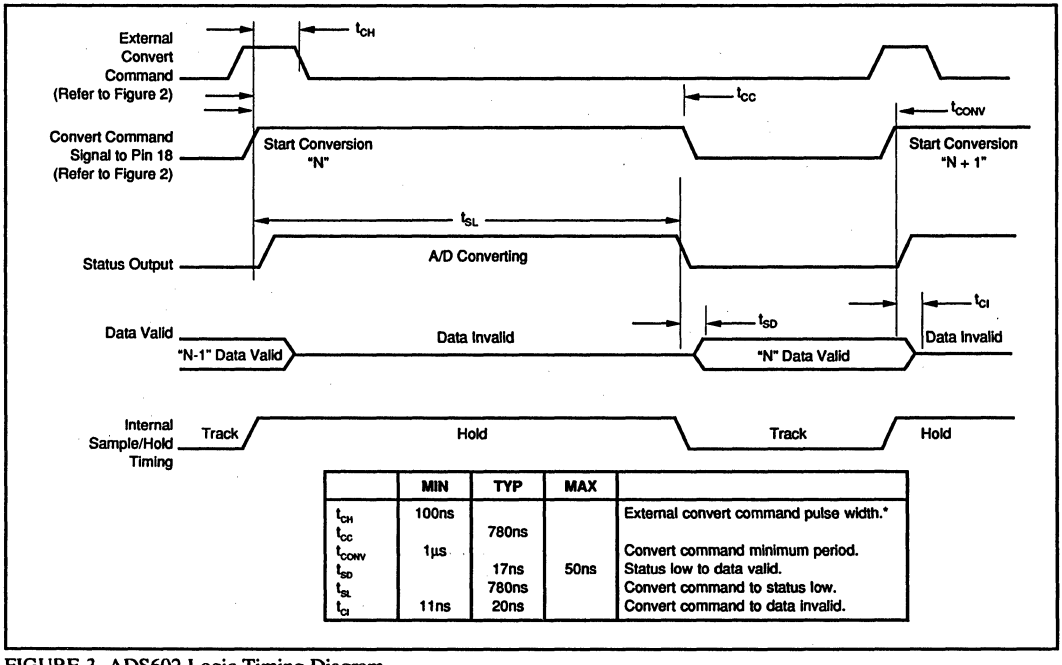
In addition to the timing details in Figure 3, the following list contains some important timing considerations for the ADS602:

1. When power is first applied, the convert command should be held low or below the +5V supply to prevent latch up.

2. The rising edge of the convert command pulse initiates a conversion. This convert command should remain high until the Status falls (i.e., the internal ADC is finished converting). A simple circuit that provides the correct convert command (pin 18) pulse length, is shown in Figure 2.

3. The ADS602 goes directly into the "hold" mode when a convert command signal is given. The Status falls approximately 780ns later, indicating that the conversion is complete. At this time, the sample-hold (internal to the ADS602) enters the track mode. The ADS602 will remain in the track mode until the next convert command is given.

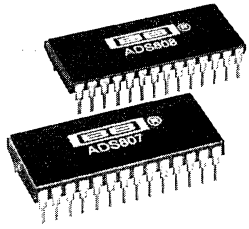
4. The data from conversion "N" can be latched directly by the convert command pulse "N + 1". This approach is illustrated in Figure 2. The falling edge of Status may be used to latch the data; however, Status must be delayed by t_{SD} (see Figure 3) plus the external latch (74AS574) setup time.



	MIN	TYP	MAX	
t_{CH}	100ns			External convert command pulse width.*
t_{CC}		780ns		
t_{CONV}	1µs			Convert command minimum period.
t_{SD}		17ns	50ns	Status low to data valid.
t_{SL}		780ns		Convert command to status low.
t_{CI}	11ns	20ns		Convert command to data invalid.

FIGURE 3. ADS602 Logic Timing Diagram.

BURR-BROWN®



ADS807
ADS808

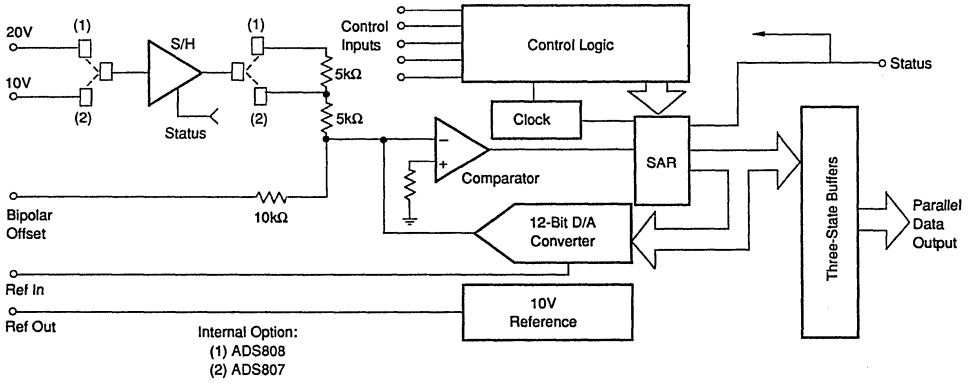
12-Bit Resolution Sampling A/D CONVERTER WITH MICROPROCESSOR INTERFACE

FEATURES

- 100ksps SAMPLING RATE
- DC SPECS:
  1/2LSB Integral Linearity Error
  1 LSB Differential Linearity Error
- AC SPECS:
  82dB Spurious-Free Dynamic Range
  72dB Signal-to-Noise Ratio
  80dB Total Harmonic Distortion
  75dB Two-Tone Intermodulation Distortion
- INTERNAL SAMPLE/HOLD, REFERENCE & CLOCK
- PIN COMPATIBLE WITH INDUSTRY STANDARD ADC574, ADC674, ADC774 A/D CONVERTERS
- POWER DISSIPATION: 660mW
- 28-PIN CERAMIC DIP

APPLICATIONS

- HIGH SPEED DATA ACQUISITION
- SPECTRUM ANALYSIS
- SPEECH SYNTHESIS AND RECOGNITION
- DSP PROCESS AND MOTION CONTROL



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PDS-855A

DESCRIPTION

ADS807 and ADS808 are complete 12-bit sampling A/D converters. Each contain a sample/hold and a successive approximation A/D converter with a buried zener reference, clock, and 574/674/774-type microprocessor interface. ADS807 analog input pins can be connected for 0V to +10V or ±5V analog input ranges. ADS808 has a ±10V analog input range.

The sample/hold has a 1.5µs max acquisition time to ±0.01% for a full scale input step change. Aperture Time is 25ns and Aperture Uncertainty is 300ps. The A/D converter alone converts in 8µs max.

DC performance is completely specified. 11-bit (J and S grades) and 12-bit (K and T grades) integral linearity grades are available.

AC performance is completely characterized: total harmonic distortion, intermodulation distortion, signal-to-noise ratio and spurious-free dynamic range at the rated 100ksps sampling rate.

ADS807/808s are packaged in a 28-pin side-braze, hermetic, double-wide ceramic DIP and are specified over 0°C to +70°C, and –55°C to +125°C temperature ranges.

ADS807/808s are excellent single-package replacements for A/D converters that use the industry standard 574A/674A/774 pinout along with a separate sample/hold.

SPECIFICATIONS

ELECTRICAL

T_A = +25°C. Sampling Frequency: f_s = 100kHz, $+V_{CC}$ = +15V, $-V_{CC}$ = –15V, V_{DD} = +5V.

	ADS807/808JH			ADS807/808KH			ADS807/808RH			ADS807/808SH			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
RESOLUTION			12			*			*			*	BITS
INPUT													
ANALOG INPUT													
Voltage Range [1]													
ADS807		0 to +10V, ±5V			*			*			*		V
ADS808		±10V			*			*			*		V
Impedance	100	150		*	*		*	*		*	*		MΩ
Bias Current			±400			*			*			*	nA
At T_{MIN} or T_{MAX}			±400			*			*			*	nA
DIGITAL INPUTS (Over Temperature Range)													
Logic Levels (TTL Compatible)													
V_{IL}	–1.0		+0.8	*		*	*		*	*		*	V
V_{IH}	+2.0		+5.5	*		*	*		*	*		*	V
I_{IL} (V_I = +0.4V)	–5			*			*			*			µA
I_{IH} (V_I = +2.7V)			+5			*			*			*	µA
DC ACCURACY													
Full Scale Error [2, 3]		±0.3			*			*			*		%
T_{MIN} to T_{MAX} [5]			±0.5			±0.4			±0.8			±0.6	%
Integral Linearity Error			±0.024			±0.012			±0.024			±0.012	% FSR (4)
T_{MIN} to T_{MAX}			±0.024			±0.012			±0.024			±0.012	% FSR
Differential Linearity Error			±0.024			±0.012			±0.024			±0.012	% FSR
No Missing Codes Resolution			11			12			11			12	Bits
T_{MIN} to T_{MAX}			11			12			11			12	Bits
Unipolar Zero (ADS807)			±3			±2			±3			±2	LSB
T_{MIN} to T_{MAX}			±2			±1			±3			±2	LSB
Bipolar Zero			±10			±5			±10			±5	LSB
T_{MIN} to T_{MAX}			±2			±1			±4			±2	LSB
Power Supply Sensitivity													
Change in Full-Scale Calibration													
$+14.5 < +V_{CC} < +16.5$			0.5			*			*			*	LSB
$-16.5 < -V_{CC} < -14.5$			1.0			*			*			*	LSB
$+4.5 < V_{DD} < +5.5$			0.5			*			*			*	LSB
AC CHARACTERISTICS [6]													
Spurious-free Dynamic Range (SFDR)													
f_{IN} = 10.7kHz (–0.5dB)		82			*			*			*		dB
Total Harmonic Distortion (THD)													
f_{IN} = 10.7kHz (–0.5dB)		80			*			*			*		dB
Two-tone Intermodulation Distortion (IMD) [7]													
f_{IN1} = 24.4kHz (–6.5dB)	f_{IN2} = 25.9kHz (–6.5dB)												
ADS807		75			*			*			*		dB
ADS808		72			*			*			*		dB

SPECIFICATIONS (CONT)

ELECTRICAL

T_A = +25°C. Sampling Frequency: f_S = 100kHz, $+V_{CC}$ = +15V, $-V_{CC}$ = −15V, V_{DD} = +5V.

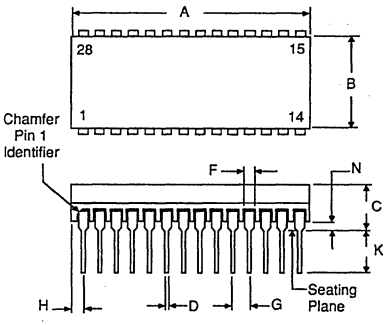
	ADS807/808JH			ADS807/808KH			ADS807/808RH			ADS807/808SH			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
AC CHARACTERISTICS (Cont.)													
Signal to Noise Ratio (SNR)													
f_{IN} = 10.7kHz (−0.5dB)		72			•			•			•		dB
Input Small Signal Bandwidth													
(2Vp-p sinewave)		2.5			•			•			•		MHz
SAMPLING DYMANICS													
Sampling Rate		100			•			•			•		kHz
Aperture Delay		25			•			•			•		ns
Aperture Uncertainty (Jitter)		300			•			•			•		ps, rms
Feedthrough (10Vp-p, 100kHz) [8]		0.02			•			•			•		%
Transient Response [9]		1.9			•			•			•		µs
Overvoltage Recovery [10]		11.4			•			•			•		µs
REFERENCE OUTPUT													
Voltage	9.9	10.0	10.1	•	•	•	•	•	•	•	•	•	V
Source Current Available for													
External Loads [11]	2			•			•			•			mA
DIGITAL OUTPUTS (Over Temperature)													
Format		Parallel			•			•			•		
Coding		Bipolar Offset Binary (BOB)				•			•			•	
Logic Levels (3-state output, TTI compatible)													
V_{OL} (I_{SINK} = 1.6mA)	0.0		+0.4	•		•	•		•	•		•	V
V_{OH} (I_{SOURCE} = 500µA)	+2.4		+5.0	•		•	•		•	•		•	V
$I_{LEAKAGE}$ (High-Z State)	−5	−0.1	+5	•	•	•	•	•	•	•	•	•	µA
POWER SUPPLIES													
Rated Voltage													
$+V_{CC}$	+14.5	+15	+16	•	•	•	•	•	•	•	•	•	V
$-V_{CC}$	−14.5	−15	−16	•	•	•	•	•	•	•	•	•	V
V_{DD}	+4.5	+5.0	+5.5	•	•	•	•	•	•	•	•	•	V
Current													
$+V_{CC}$		15	18		•	•		•	•		•	•	V
$-V_{CC}$		26	33		•	•		•	•		•	•	V
V_{DD}		9	15		•	•		•	•		•	•	V
Power Consumption		660	850		•	•		•	•		•	•	mW
TEMPERATURE RANGE													
Specification	0		+70	•		•	−55		+125	•		•	°C
Storage	−65		+150	•		•	•		•	•		•	°C

*Specification same as grade to the left.

NOTES: (1) ADS807: For input ranges −5V to +5V, 0 to +10V; ADS808: For input range ±10V (2) Adjustable to zero with external potentiometer. (3) Specifications assume a fixed 50Ω resistor between Ref Out (Pin 8) and Ref In (Pin 10). This specification measured at the FFE_{16} to FFF_{16} transition, includes offset. (4) FSR means Full Scale Range. For ADS807, FSR = 10V; for ADS808 FSR = 20V. (5) Change specifications for unipolar offset, bipolar zero and full-scale error correspond to the change from the initial value (at 25°C) to the value at T_{MIN} or T_{MAX}. (6) Refer to Discussion of Specifications section for definitions. (7) Intermodulation distortion is referred to the larger of the two input test signals. If referred to the peak envelope signal (approx. 0dB), the intermodulation products will be 6dB lower. (8) Sample/Hold Feedthrough: Feedthrough to the output of the A/D converter of a 100kHz sinewave signal when the Sample/Hold is in the HOLD mode. (9) For a 10V step input, 12-bit accuracy attained in specified time. (10) Recovers to specified performance in specified time after 2 x Full-Scale input overvoltage. (11) External load must be constant during conversion.

MECHANICAL

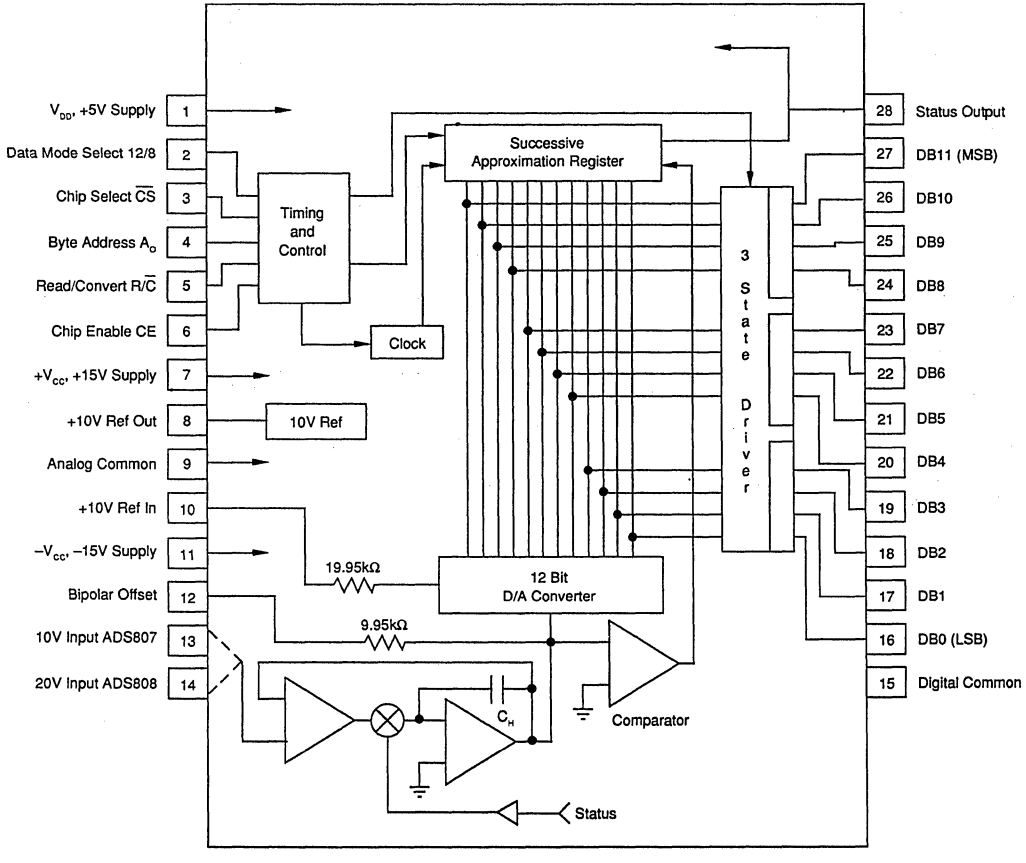
H Package — 28-Pin Ceramic DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	.610 BASIC		15.49 BASIC	
C	.160	.205	4.06	5.21
D	.015	.019	0.38	0.48
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.055	.095	1.40	2.41
J	.009	.012	0.23	0.30
K	.155	.195	3.94	4.95
L	.600 BASIC		15.24 BASIC	
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

PIN CONFIGURATION



NOTE: Pin 14 is a "No Connect" on the ADS807. Pin 13 is a "No Connect" on the ADS808.

ORDERING INFORMATION

Model	Input Range (V)	Linearity Error,%FSR	Specification Temperature Range
ADS807JH	–5 to +5	±0.024	0°C to +70°C
ADS807KH	or	±0.012	0°C to +70°C
ADS807RH	0 to +10	±0.024	–55°C to +125°C
ADS807SH		±0.012	–55°C to +125°C
ADS808JH	–5 to +5	±0.024	0°C to +70°C
ADS808KH	or	±0.012	0°C to +70°C
ADS808RH	–10 to +10	±0.024	–55°C to +125°C
ADS808SH		±0.012	–55°C to +125°C

BURN-IN SCREENING OPTION
See text for details.

Model	Burn-in Temperature	Specification Temperature Range
ADS807JH-BI	+125°C	0°C to +70°C
ADS807KH-BI	+125°C	0°C to +70°C
ADS807RH-BI	+125°C	–55°C to +125°C
ADS807SH-BI	+125°C	–55°C to +125°C
ADS808JH-BI	+125°C	0°C to +70°C
ADS808KH-BI	+125°C	0°C to +70°C
ADS808RH-BI	+125°C	–55°C to +125°C
ADS808SH-BI	+125°C	–55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Digital Common	+16.5V
$-V_{CC}$ to Digital Common	–16.5V
V_{DD} to Digital Common	+7V
Analog Common to Digital Common	±1V
Control Inputs to Digital Common	–0.5 to V_{DD} + 0.5V
Ref In, BIP Odd, to Analog Common	±16.5V
Analog Input Voltage	$+V_{CC}$ or $-V_{CC}$
Ref Out	Indefinite Short to Common Momentary Short to V_{CC}
Maximum Junction Temperature	160°C
Internal Power Dissipation	1000mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}	50°C/W

BURN-IN SCREENING

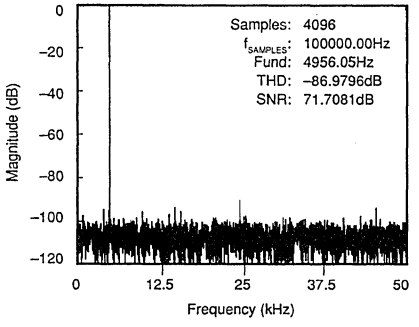
Burn-in screening is an option available for the ADS807/808. Burn-in duration is 160 hours at the temperatures listed below, or at an equivalent combination of time and temperature according to the Arrhenius equation using 1eV activation energy.

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number as shown in the table.

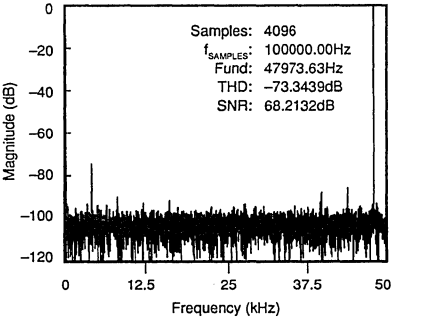
TYPICAL PERFORMANCE CURVES

T_A = +25°C, $+V_{CC}$ = +15V, $-V_{CC}$ = –15V, V_{DD} = +5V.

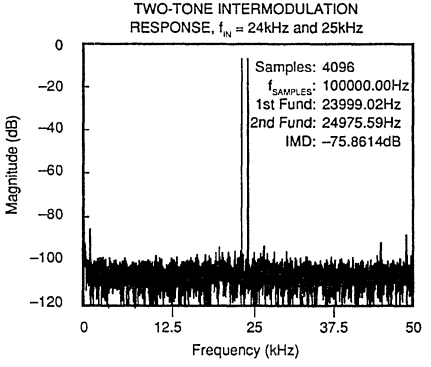
FULL-SCALE SINEWAVE RESPONSE, f_{IN} = 5kHz



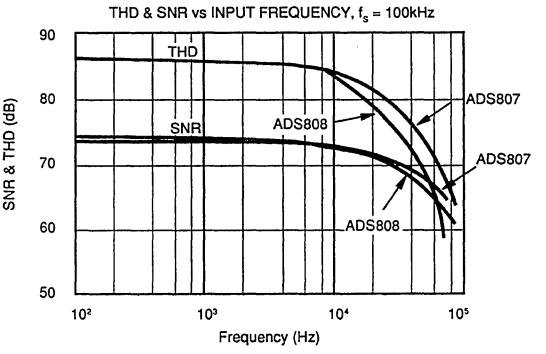
FULL-SCALE SINEWAVE RESPONSE, f_{IN} = 50kHz



TWO-TONE INTERMODULATION RESPONSE, f_{IN} = 24kHz and 25kHz

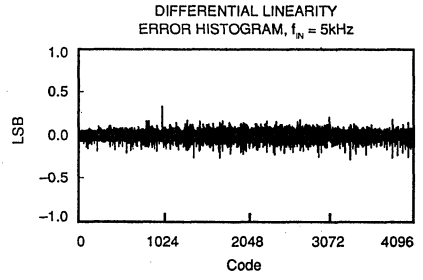


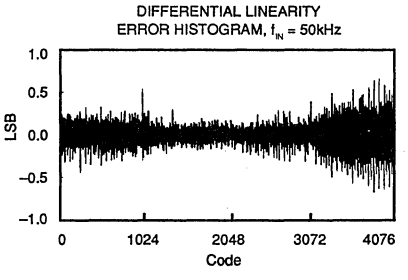
THD & SNR vs INPUT FREQUENCY, f_S = 100kHz



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, $+V_{CC}$ = +15V, $-V_{CC}$ = −15V, V_{DD} = +5V .





DISCUSSION OF SPECIFICATIONS

BASIC DEFINITIONS

Dynamic Range—The ratio of the maximum input signal to the smallest quantum the converter can produce. It is expressed in dB. For an ideal N-bit linear, binary-coded A/D converter, the Dynamic Range is:

$$\text{Dynamic Range} = 20 \log 2^N = 6.02N \text{ dB}$$

This ideal value is degraded by system noise, internal converter noise, and differential linearity error.

Full Scale Range, FSR—The nominal range of the A/D converter. ADS808 has a FSR of 20V for the −10V to +10V input range. ADS807 has a FSR of 10V for the 0V to +10V or −5V to +5V input ranges.

Least Significant Bit, LSB—The smallest analog input change that is resolved by the A/D converter. For an A/D converter with N bits output, the input value of the LSB is $FSR/2^N$.

Most Significant Bit, MSB—That binary digit that has the greatest value or weight. The MSB weight is FSR/2.

Resolution—An N-bit binary-coded A/D converter resolves the analog input into 2^N values represented by the 2^N digital output codes.

DC ACCURACY

Refer to Figure 1 for an illustration of A/D converter DC parameter terminology.

Linearity Error, Integral Linearity Error, (ILE)—Linearity error is defined as the deviation of actual analog input values from the ideal values about a straight line drawn through the code mid-points near full scale (at $+V_{FS}$ −1LSB) and at Zero input (at 1/2LSB below the first code transition, i.e. at zero) or, in the case of bipolar operation, near minus full scale (at 1/2LSB below the first code transition, i.e. at $-V_{FS}$).

Despite the definition, however, code transitions are easier to measure than code midpoints. Therefore linearity is measured as the deviation of the analog input values from a line drawn between the first and last code transitions. Linearity Error specifications are expressed in % of Full Scale Range (FSR). ADS807/808KH ILE is ±0.012% of FSR which is 1/2 LSB at 12-bits.

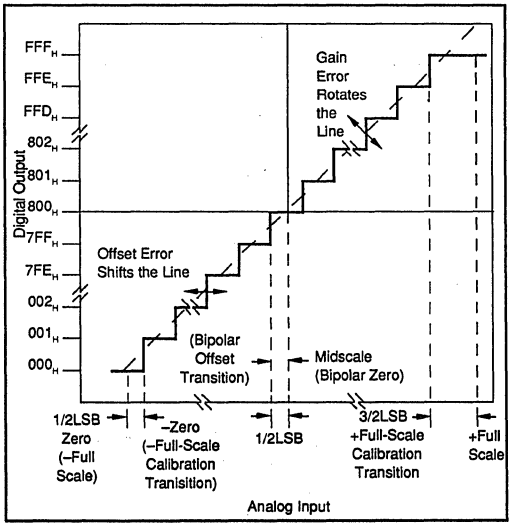


FIGURE 1. Transfer Characteristic Terminology.

Differential Linearity Error, (DLE); No Missing Codes—Differential Linearity Error is defined as the deviation in code width from the ideal value of 1LSB. If the DLE is greater than –1LSB anywhere along the range, the A/D will have at least one missing code. ADS807/808KH are specified to have a DLE of ±0.024% of FSR which is ±1LSB at 12 bits. ADS807/808s are specified to have No Missing Codes for 12-bit resolution over the specification temperature range.

Full Scale Error—The deviation from the ideal value of the input at the last code midpoint (V_{FS} – 1LSB). As with the linearity error measurements, code transition values are the locations actually measured for this spec. The ideal Full Scale transition value is FSR – 3/2LSB for unipolar input converters and FSR/2 – 3/2LSB for bipolar input A/D converters. Full Scale Error is expressed in % of FSR or in LSBs. Refer to Figure 1.

Full Scale Error of the ADS807/808 may be trimmed to zero using external trim potentiometers.

Offset Error

Unipolar Offset Error is defined as the deviation of the actual code-midpoint value of the first code from the ideal value located at 1/2LSB below the ideal first transition value (i.e. at zero volts).

Bipolar Offset Error is defined as the deviation of the actual code-midpoint of the first code from the ideal value located at 1/2LSB below the ideal first transition value located at $-V_{FS}$ +1/2LSB.

Again, transition values are the actual measured parameters. Offset and Zero errors of the ADS807/808 may be trimmed to zero using external trim potentiometers. Offset Error is expressed as a % of FSR.

Bipolar Zero Error is defined as the deviation of the actual mid-scale-code midpoint value of the input from the ideal mid-scale value (i.e. at ZERO volts). The transition value actually measured is 1/2LSB below zero input and has a value of FSR/2 – 1LSB. Refer to Figure 1. Bipolar Zero Error is the sum of the Bipolar Offset Error, 1/2 the Gain Error, and the Linearity Error. It is measured, rather than calculated to avoid tolerance buildup resulting from summing the tolerances of each spec.

Power Supply Sensitivity (Rejection) [PSS, PSR]—Power Supply Sensitivity describes the maximum change in the full-scale transition value from the initial value for a change in each power supply voltage. It is specified in units of LSB over the power supply range.

AC PERFORMANCE

Dynamic Differential Linearity Error—The deviation of the frequency of occurrence of output codes from the ideal when the A/D converter is operated with an input of specified frequency. If a particular code is wider than the ideal 1LSB width, then more counts than the theoretical will accumulate at that code. This characterization is done using a histogram method.

Signal-to-Noise Ratio (SNR)—The ratio of the signal power of a full-scale input sinewave to the RMS output noise power.

$$SNR_{dB} = 10 \log \left(\frac{\text{Sinewave Signal Power}}{\text{Output Noise Power}} \right)$$

For an ideal N-bit A/D converter (measured over an $f_S/2$ bandwidth) the SNR is:

$$SNR_{dB} = 6.02N + 1.76$$

This definition assumes that the output noise is described by what remains after all fundamental, harmonic, DC and outstanding spurious components have been removed. The noise power that is left is a "noise floor" that appears across all frequencies of the measured spectrum at some relatively flat level. SNR is expressed in dB.

Effective Bits—The effective number of bits is calculated using the rewritten formula above and the measured SNR.

$$N_{EFF} = \left(\frac{SNR_{MEAS} - 1.76}{6.02} \right)$$

Spurious-Free Dynamic Range (SFDR)—The power of the peak non-fundamental component (harmonic or spurious, in-band or out-of-band) in the output specturm to the input signal power. Some manufacurers data sheets label this spec as "Harmonics and Spurious Noise" or "AC Linearity Error". SFDR is expressed in dB at specified input frequencies and sampling rates.

$$SFDR_{dB} = 10 \log \left(\frac{\text{Power of Peak Spurious Component}}{\text{Sinewave Signal Power}} \right)$$

Total Harmonic Distortion (THD)—The ratio of power of the harmonic output to the sinewave input power. THD is expressed in dB at specified input frequencies and sampling rates.

$$THD_{dB} = 10 \log \left(\frac{\text{Harmonic Output Power (to 9 harmonics)}}{\text{Sinewave Signal Power}} \right)$$

Intermodulation Distortion (IMD)—The ratio of the power of the intermodulation products to the input power of the sum of two sinewaves of different frequency. IMD is expressed in dB at specified input frequencies and sampling rates.

$$IMD_{dB} = 10 \log \left(\frac{\text{IMD Product Power (to 5th order products)}}{\text{Sinewave Signal Power}} \right)$$

AC PERFORMANCE CHARACTERIZATION

SPECTRAL CHARACTERIZATION

ADS807/808 are characterized for AC performance using Fast Fourier Transform (FFT) techniques. Figure 2 shows a typical equipment configuration for single-tone testing of THD, SNR and SFDR. Figure 3 shows the setup for Two-tone IMD characterization.

Highly accurate phase-locked signal sources allow high resolution FFT measurements to be made without using window functions. By choosing appropriate signal frequencies and sample rates, an integral number of signal frequency periods can be sampled. [1] Since no spectral leakage results, no window function is needed. This "rectangular window" was used to generate the spectral performance curves shown in the Typical Performance Curves section of this data sheet. A 4096 point FFT was used for this 12-bit resolution converter to assure that the majority of codes were exercised. If phase-locked signal sources are not available, a windowing function must be applied to the time-domain samples. The four-sample Blackman-Harris window [2] is recommended for evaluating high-performance A/D converters.

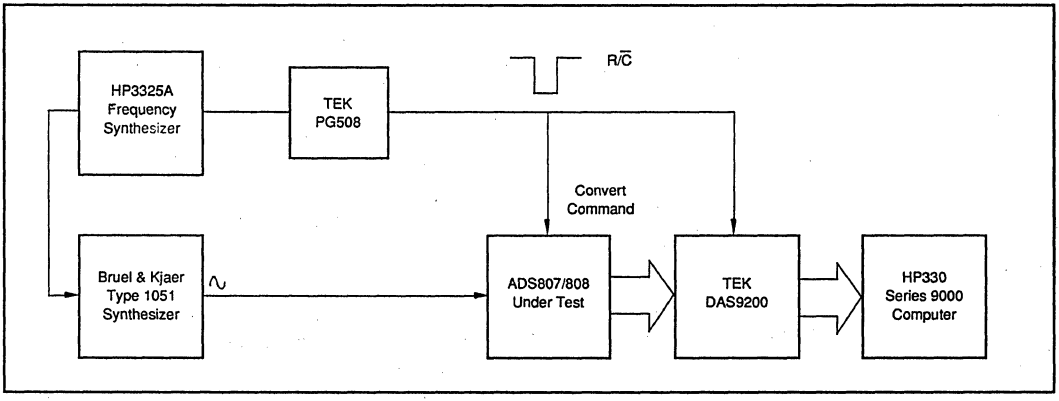


FIGURE 2. Equipment Configuration for Single-Tone Spectral Characterization.

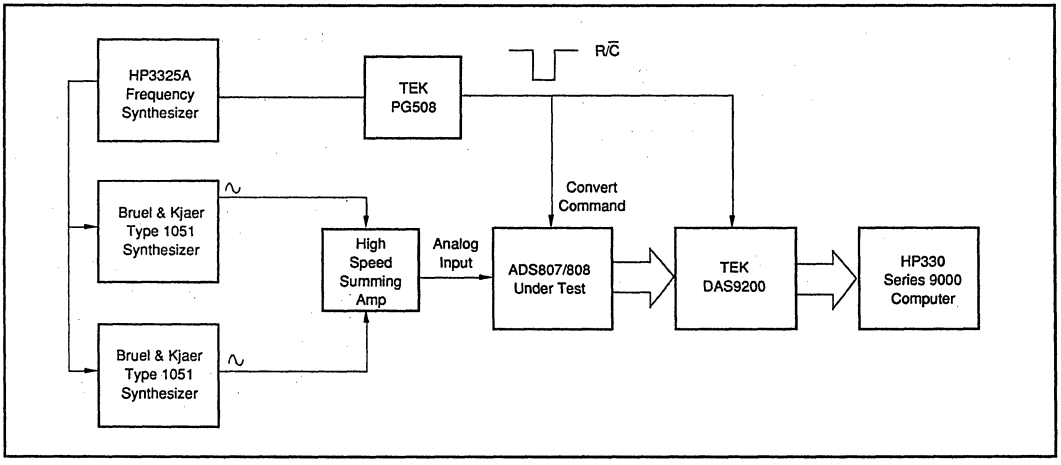


FIGURE 3. Equipment Configuration for Two-Tone Spectral Characterization.

DYNAMIC DLE CHARACTERIZATION

The FFT provides an excellent measure of harmonic and intermodulation distortion. Low-order spurious products are primarily caused by integral non-linearity of the sample/hold and A/D converter.

The influence of differential linearity errors is harder to distinguish in a plot of the output spectrum of an A/D converter — it may show up as high-order harmonics or as very minor variations in the overall appearance of the noise floor.

A more direct method of examining the differential linearity error under dynamic conditions is the histogram.[3] The equipment setup is the same as for the single-tone FFT. Two histograms of ADS808 performance are shown in the Typical Performance Curves section of this data sheet. Note the low DLE at low frequency and the minor degradation of the DLE at the Nyquist frequency.

References:

1. Brigham, E. Oran, *The Fast Fourier Transform*, Englewood Cliffs, N.J.: Prentice-Hall, 1974.

2. Harris, Fredric J., "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform," *Proceedings of the IEEE*, Vol. 66, No. 1, January 1987, pp 51-83.

3. "Dynamic Tests for A/D Converter Performance," Application Note AN-133, Burr-Brown Corporation, Tucson, AZ, 1985.

INSTALLATION

POWER SUPPLY SELECTION

Linear power supplies are preferred. Switching power supply specifications may appear to indicate low noise output, but these specifications are rms specs. The spikes generated in switchers may be hard to filter. Their high-frequency components may be extremely difficult to keep out the power supply return system. If switchers must be used, their outputs must be carefully filtered and the power supply itself should be shielded and located as far away as possible from precision analog circuits.

LAYOUT CONSIDERATIONS

Power Supply Wiring—Use heavy power supply and power supply common (ground) wiring. A ground plane is usually the best solution for preserving dynamic performance and reducing noise coupling into sensitive converter circuits.

When passing converter power through a connector, use every available spare pin for making power supply return connections, and use some of the pins as a Faraday shield to separate the Analog and Digital Common lines.

Power Supply Returns—(Analog Common & Digital Common) Connect Analog Common and Digital Common together right at the converter with the ground plane. They are not connected internally. This will usually give the best performance. However, it may cause problems for the system designer. Where it is absolutely necessary to separate analog and digital power supply returns, each should be separately returned to the power supply. Do not connect Analog Common and Digital Common together and then run a single wire to the power supply. When using separate returns, connect a 1µF to 47µF tantalum capacitor between Digital Common and Analog Common pins as close to the package as possible.

Power Supply Bypassing—Every power-supply line leading into an A/D converter must be bypassed to its Common pin. The bypass capacitor should be located as close to the converter package as possible and tied to a solid ground — connecting the capacitors to a noisy ground defeats the purpose of the bypass. Use tantalum capacitors with values of from 1µF to 47µF and parallel them with smaller ceramic capacitors for high frequency filtering if necessary.

Separate Analog and Digital Signals—Digital signals entering or leaving the layout should have minimum length to minimize crosstalk to analog wiring. Keep analog signals as far away as possible from digital signals. If they must cross, cross them at right angles. Coaxial cable may be necessary for analog inputs in some situations.

Wire-wrap construction is not recommended for best noise performance.

Shield Other Sensitive Points—If external gain and offset potentiometers are used, the potentiometers and associated series resistors should be located as close to the ADS807/808 as possible. If no trim adjusting is required and fixed resistors are used, they should also be located as close to the converter as possible.

ANALOG INPUT RANGES

Unipolar Connection (ADS807 only)

Analog input connections for the 0 to + 10V unipolar input range of ADS807 is shown in Figure 4.

When the 0V to +10V input range is used, apply the analog input to pin 13. If gain adjustment is not used, replace potentiometer R2 with a 50Ω ±1% metal film resistor to meet published specifications. If offset adjustment is not used, connect pin 12 (Bipolar Offset) directly to pin 9 (Analog Common).

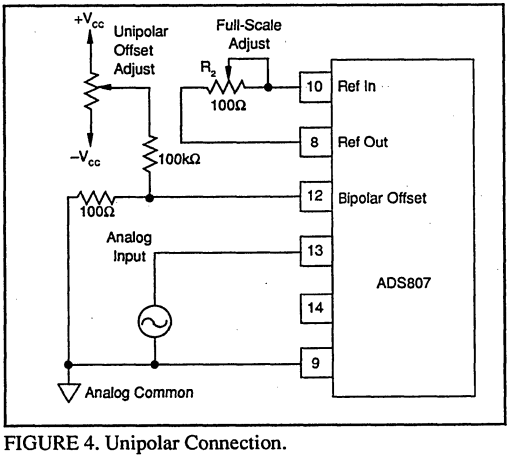


FIGURE 4. Unipolar Connection.

Bipolar Connection

Analog input connections for bipolar input ranges are shown in Figure 5.

Input pin 13 is used on the ADS807. Input pin 14 is used on the ADS808. If either bipolar offset or bipolar gain adjustments are not required, the trim potentiometer R_1 and R_2 are to be replaced with fixed 50Ω ±1% metal film resistors to meet published specifications.

CALIBRATION

UNIPOLAR RANGE (ADS807 only)

To adjust unipolar offset, sweep the input through the end-point transition voltage (0V +1/2LSB), +1.22mV for the ADS807, that causes the output code DB0 High. Adjust potentiometer R_1 until DB0 is alternately toggling High and Low with all other bits Low. Then adjust Full Scale by applying an input voltage of nominal full-scale minus 3/2LSB (V_{FS} –3/2LSB), the value which should cause all bits to be High. This value is +9.9963V. Adjust potentiometer R_2 until bits DB1-DB11 are High and DB0 is toggling High and Low.

BIPOLAR RANGES

The calibration procedure is similar to that decsribed above for unipolar operation, except that the offset adjustment is performed with an input voltage which is 1/2LSB above the minus full-scale value (–4.9988V for the ±5V range, ADS807; –9.9976V for the ±10V range, ADS808). Adjust R1 for DB0 to toggle High and Low with all other bits Low. To adjust full-scale, apply a DC input voltage which is 3/2LSB below the nominal plus full-scale value (+4.9963V for the ±5V range, ADS807; +9.9927V for the ±10V range, ADS808) and adjust R2 for DB0 to toggle High and Low with all other bits High.

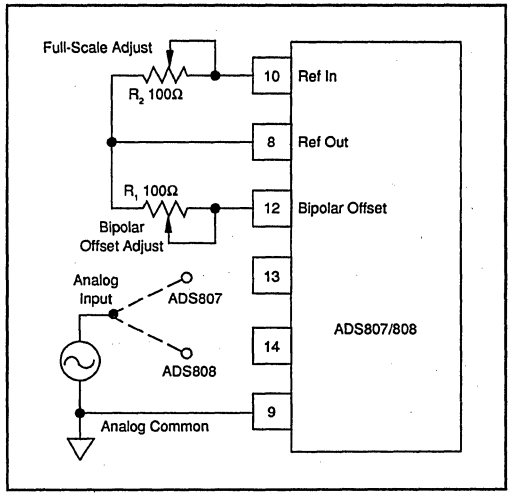


FIGURE 5. Bipolar Connection.

CONTROLLING THE ADS807/808

The Burr-Brown ADS807/808 can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready — choosing either 12 bits all at once, 8 bits followed by 4 bits in a left-justified format. The five control inputs (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$ and CE) all perform the same functions as the interface to the popular A/D converters ADC574A, ADC674A, and ADC774. They are TTL/5V-CMOS compatible. Table II contains a summary of the control line functions of the ADS807/808. The control function truth table is listed in Table III.

BINARY (BIN) OUTPUT	INPUT VOLTAGE RANGE AND LSB VALUES			
Input Voltage Range	Defined As:	±10V (ADS808)	0V to +10V (ADS807)	±5V (ADS807)
One Least Significant Bit (LSB)	FSR/2^n	20V/2^n	10V/2^n	10V/2^n
	n=8	78.13mV	39.06mV	39.06mV
	n=12	4.88mV	2.44mV	2.44mV
Output Transition Values				
FFE_H to FFF_H	+Full-scale	+10V-3/2LSB	+10V–3/2LSB	+5V–3/2LSB
$7FF_H$ to 800_H	Mid Scale, (BP Zero)	0V–1/2LSB	+5V–1/2LSB	0V–1/2LSB
000_H to 001_H	Zero, –Full Scale	–10V+1/2LSB	0V+1/2LSB	–5V+1/2LSB

TABLE I. Input Voltages, Transition Values, and LSB Values.

PIN DESIGNATION	DEFINITION	FUNCTION
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0->1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (Active Low)	Must be low ("0") to either initiate a conversion or read output data. 1->0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8- or 12- bit operation. 1->0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0->1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8- bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in 2 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing zeros (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSBs or LSBs as determined by the A_0 line.

TABLE II. ADS807/808 Control Line Functions.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
0->1	0	0	X	0	Hold & Initiate 12-bit conversion
0->1	0	0	X	1	Hold & Initiate 8-bit conversion
1	1->0	0	X	0	Hold & Initiate 12-bit conversion
1	1->0	0	X	1	Hold & Initiate 8-bit conversion
1	0	1->0	X	0	Hold & Initiate 12-bit conversion
1	0	1->0	X	1	Hold & Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

TABLE III. Control Input Truth Table. (X means Don't Care.)

STAND-ALONE (NO BUS INTERFACE) OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and A_0 are connected to digital common and CE and 12/$\overline{8}$ are connected to V_{DD} (+5V). The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a High-to-Low transition (Hold/Convert) of R/$\overline{C}$. This transition commands the sample/hold to Hold and the converter logic to start the conversion. The Sample-To-Hold settling time is so short that the sample/hold is fully settled to the required accuracy before the first successive approximation A/D decision occurs.

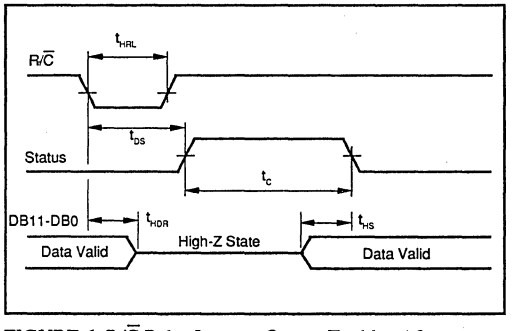


FIGURE 6. R/$\overline{C}$ Pulse Low — Output Enables After Conversion.

The three-state data output buffers are enabled when R/$\overline{C}$ is High and Status is Low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In either case the R/$\overline{C}$ pulse must remain low for a minimum of 50ns.

Figure 6 illustrates timing when the Hold/Convert command is initiated by an R/$\overline{C}$ pulse which goes Low and returns to the High state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion. Figure 7 illustrates the timing when Hold/Convert is initiated by a positive R/$\overline{C}$ pulse. In this mode the output data from the previous conversion is enabled during the positive portion of R/$\overline{C}$. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Timing specifications for stand-alone operation are listed in Table IV.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	115	150	375	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

TABLE IV. Stand-alone Mode Timing.

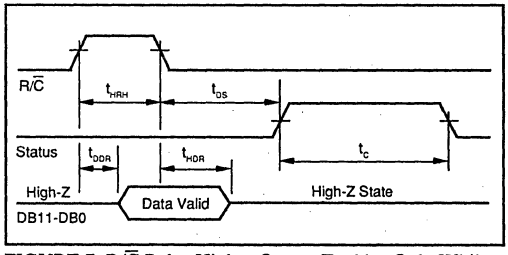


FIGURE 7. R/$\overline{C}$ Pulse High—Output Enables Only While R/$\overline{C}$ Is High.

Note that, unlike the R/$\overline{C}$ command input timing for non-sampling A/D converters such as the ADC574A/674A/774, a time period (Acquisition Time) must be allowed for the sample/hold amplifier to acquire the next sample. This time period, occurring immediately after the conversion is complete (Status goes Low), is 1µs typical (1.5µs maximum) for acquisition to ±0.01% of Full Scale Range for a 10V analog input change from the previous held value to the next.

FULLY CONTROLLED OPERATION

Throughput Period

The throughput period, reciprocal of the sampling rate, (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a Hold/Convert start transition (described below). If A_0 is latched High, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is Low. If all 12 bits are read following an 8-bit conversion, the 3LSBs (DB0-DB2) will be Low (logic 0) and DB3 will be High (logic 1). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

Conversion Start

The converter is commanded to initiate a Hold/Convert operation by a transition occurring on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$) as shown in Table III. Conversion is initiated by the last of the three logic inputs to reach the required state and thus all three may be dynamically controlled. If necessary all three may change state simultaneously, and the nominal delay time is the same regardless of which input actually starts the operation. If it is desired that a particular input establish the actual start of operation, the other two should be stable a minimum of 50ns prior to the transition of that input. Timing relationships for start of operation timing are illustrated in Figure 8. The specifications for timing are contained in Table V.

The Status output indicates the current state of the converter by being in a high state only during conversion. During this time the three-state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or re-started. However, if A_0 changes state after the beginning of operation, any additional Hold/Convert transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8-bits vs. 12-bits) for that conversion.

As with stand-alone operation described above, sample/hold Acquisition Time must be provided before the next Hold/Convert command.

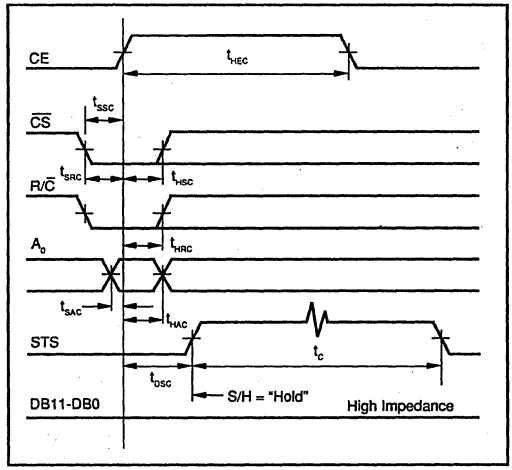


FIGURE 8. Conversion Cycle Timing.

READING OUTPUT DATA

After operation is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ High, Status Low, CE High and $\overline{CS}$ Low. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 11 and Table V for timing relationships and specifications.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Conversion Mode					
t_{DSC}	STS Delay from CE		60	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup time	50	20		ns
t_{HSC}	$\overline{CS}$ low during CE high	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE setup	50	0		ns
t_{HRC}	R/$\overline{C}$ low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0			ns
t_{HAC}	A_0 valid during CE high	50	20		ns
t_C	Conversion time plus				
	Acquisition time 12-bit cycle		9	10	µs
	8-bit cycle		6	6.5	µs
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE setup	50	0		ns
t_{SAR}	R/$\overline{C}$ to CE setup	0			ns
t_{HSR}	$\overline{CS}$ valid after CE low	0			ns
t_{HRR}	R/$\overline{C}$ high after CE low	0			ns
t_{HAR}	A_0 valid after CE low	50			ns
t_{HS}	STS delay after data valid	115	150	375	ns

NOTE: Specifications are at +25°C and measured at 50% level of transitions.

TABLE V. Timing Specifications.

In most applications the 12/$\overline{8}$ input will be hard-wired in either the High or Low condition, although it is fully TTL-and CMOS-compatible and may be actively driven if desired. When 12/$\overline{8}$ is High, all 12 output lines (DB0-DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the state of A_0 is ignored.

When 12/$\overline{8}$ is Low, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest accomplished by the state of A_0 during the Read cycle. Connection of the ADS807/808 to an 8-bit bus for transfer of left-justified data is illustrated in Figure 9. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

When A_0 is Low, the byte addressed contains the 8MSBs. When A_0 is High, the byte addressed contains the 4LSBs from the conversion followed by four logic zeros which have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 10. The design of the ADS807/808 guarantees that the A_0 input may be toggled at any time with no damage to the converter; the outputs which are tied together as illustrated in Figure 9 cannot be enabled at the same time.

In the majority of applications the Read operation will be attempted only after the conversion is complete and the Status output has gone Low. In those situations requiring the earliest possible access to the data, the Read operation may be started as much as (t_{DD} max + t_{HS} max) before Status goes Low. Of course, Acquisition Time must be allowed for the sample/hold before the next Hold/Convert operation is initiated. Refer to Figure 11 for these timing relationships.

Word 1							
Processor							
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter							
DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4
Word 2							
Processor							
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter							
DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 10. 12-Bit Data Format for 8-Bit Bus System.

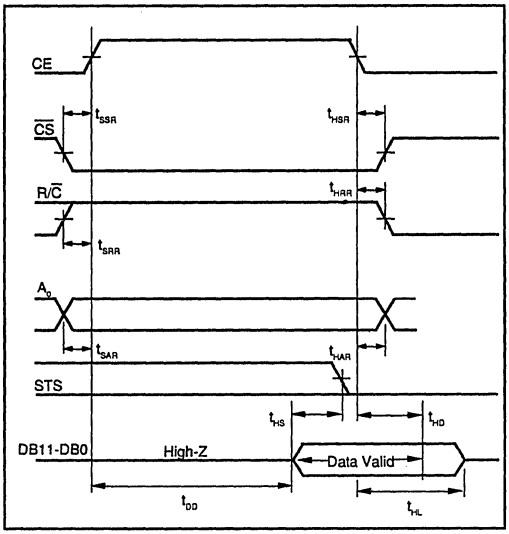


FIGURE 11. Read Cycle Timing.

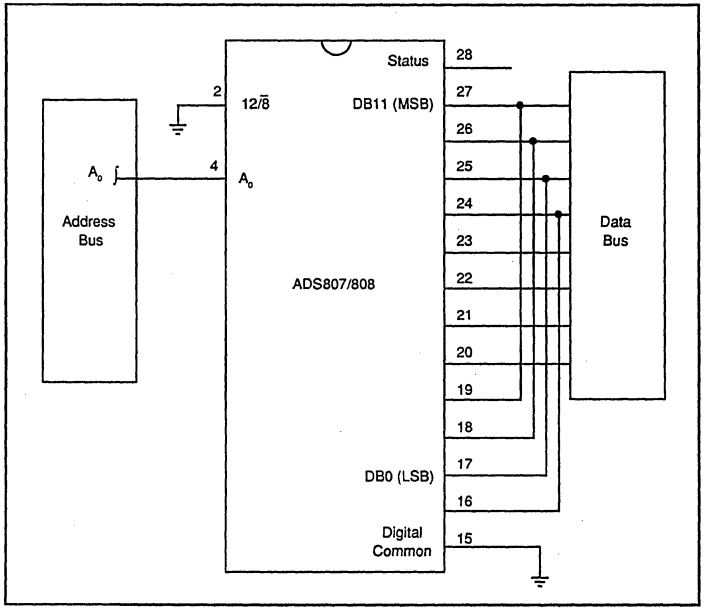


FIGURE 9. Connection to an 8-bit Bus.

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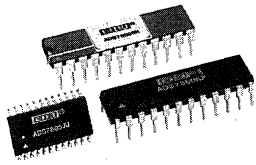


ADS7800

12-Bit 3µs Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **333k SAMPLES PER SECOND**
- **STANDARD ±10V AND ±5V INPUT RANGES**
- **DC PERFORMANCE OVER TEMP:**
  No Missing Codes
  1/2LSB Integral Linearity Error
  3/4LSB Differential Linearity Error
- **AC PERFORMANCE OVER TEMP:**
  72dB Signal-to-Noise Ratio
  80dB Spurious-free Dynamic Range
  –80dB Total Harmonic Distortion
- **INTERNAL SAMPLE/HOLD, REFERENCE, CLOCK, AND 3-STATE OUTPUTS**
- **POWER DISSIPATION: 215mW max**
- **PACKAGE: 24-Pin Single-wide DIP**
  24-Lead SOIC

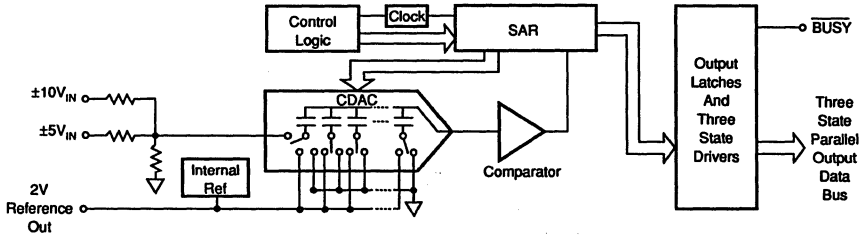
DESCRIPTION

The ADS7800 is a complete 12-bit sampling A/D converter using state-of-the-art CMOS structures. It contains a complete 12-bit successive approximation A/D converter with internal sample/hold, reference, clock, digital interface for microprocessor control, and three-state output drivers.

The ADS7800 is specified at a 333kHz sampling rate. Conversion time is factory set for 2.70µs max over temperature, and the high speed sampling input stage insures a total acquisition and conversion time of 3µs max over temperature. Precision, laser-trimmed scaling resistors provide industry-standard input ranges of ±5V or ±10V.

AC and DC performance are completely specified. Two grades based on linearity and dynamic performance are available to provide the optimum price/performance fit in a wide range of applications.

The 24-pin ADS7800 is available in plastic and side-braze hermetic 0.3" wide DIPs, and in an SOIC package. It operates from a +5V supply and either a –12V or –15V supply. The ADS7800 is available in grades specified over 0°C to +70°C and –40°C to +85°C temperature ranges.



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PDS-1018

SPECIFICATIONS

ELECTRICAL

$T_A = T_{MIN}$ to T_{MAX}, Sampling Frequency, f_S, = 333kHz, $-V_S = -15V$, $V_S = +5V$, unless otherwise specified.

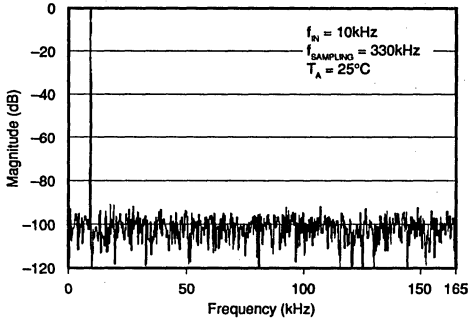
PARAMETER	CONDITIONS	ADS7800JP/JU/AH MIN	ADS7800JP/JU/AH TYP	ADS7800JP/JU/AH MAX	ADS7800KP/KU/BH MIN	ADS7800KP/KU/BH TYP	ADS7800KP/KU/BH MAX	UNITS
RESOLUTION				12			•	Bits
ANALOG INPUT								
Voltage Ranges			±10V/±5V			•		V
Impedance	±10V Range	4.4	6.3	8.1	•	•	•	kΩ
	±5V Range	2.9	4.2	5.4	•	•	•	kΩ
THROUGHPUT SPEED								
Conversion Time	Conversion Alone		2.5	2.7		•	•	µs
Complete Cycle	Acquisition + Conversion		2.6	3.0		•	•	µs
Throughput Rate		333	380		•	•		kHz
DC ACCURACY								
Full Scale Error [1]				±0.50			±0.35	%
Full Scale Error Drift			6			•		ppm/°C
Integral Linearity Error				±1			±1/2	LSB[2]
Differential Linearity Error				±1			±3/4	LSB
No Missing Codes			Guaranteed			Guaranteed		
Bipolar Zero [1]				±4			±2	LSB
Bipolar Zero Drift			1			•		ppm/°C
Power Supply Sensitivity								
	$-16.5V < -V_S < -13.5V$			±1/2			•	LSB
	$-12.6V < -V_S < -11.4V$			±1/2			•	LSB
	$+4.75V < V_S < +5.25V$			±1			±1/2	LSB
Transition Noise [3]			0.1			•		LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 47kHz	74	77		77	80		dB [4]
Total Harmonic Distortion	f_{IN} = 47kHz		–77	–74		–80	–77	dB
Two-tone Intermodulation Distortion	f_{IN1} = 24.4kHz (–6dB) f_{IN2} = 28.5kHz (–6dB)		–77	–74		–80	–77	dB
Signal to (Noise + Distortion) Ratio	f_{IN} = 47kHz	67	70		69	72		dB
Signal to Noise Ratio (SNR)	f_{IN} = 47kHz	68	71		70	73		dB
SAMPLING DYMNAMICS								
Aperture Delay			13			•		ns
Aperture Jitter			150			•		ps,rms
Transient Response [5]			130			•		ns
Overvoltage Recovery [6]			150			•		ns
INTERNAL REFERENCE VOLTAGE								
Voltage		1.9	2.0	2.1	•	•	•	V
Source Current Available for External Loads			10			•		µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	•		•	V
V_{IH}		+2.4		+5.3	•		•	V
I_{IL}		–5			•			µA
I_{IH}		+5			•			µA
DIGITAL OUTPUTS								
Data Format				Parallel, 12-bit or 8-bit/4-bit				
Data Coding				Binary Offset Binary				
V_{OL}	I_{SINK} = 1.6mA	0.0		+0.4	•		•	V
V_{OH}	I_{SOURCE} = 500µA	+2.4		+5.0	•		•	V
$I_{LEAKAGE}$ (High-Z State)			±0.1	±5		•	•	µA
POWER SUPPLIES								
Rated Voltage								
$-V_S$		–11.4	–15	–16.5	•	•	•	V
V_S (V_{SA} and V_{SD})		+4.75	+5.0	+5.25	•	•	•	V
Current								
$-I_S$			3.5	6		•	•	mA
I_S			18	25		•	•	mA
Power Consumption			135	215		•	•	mW
TEMPERATURE RANGE								
Specification	JP/JU/KP/KU	0		+70	•		•	°C
	AH/BH	–40		+85	•		•	°C
Storage		–65		+150	•		•	°C

* Same as specification for ADS7800JP/JU/AH. NOTES: (1) Adjustable to zero with external potentiometer. (2) LSB means Least Significant Bit. For ADS7800, 1LSB = 2.44mV for the ±5V range, 1LSB = 4.88mV for the ±10V range. (3) Noise was characterized over temperature near full scale, 0V, and negative full scale. 0.1LSB represents a typical rms level of noise at the worst case, which was near full scale input at +125°C. (4) All specifications in dB are referred to a full-scale input, either ±10V or ±5V. (5) For full-scale step input, 12-bit accuracy attained in specified time. (6) Recovers to specified performance in specified time after 2 x F_S input overvoltage.

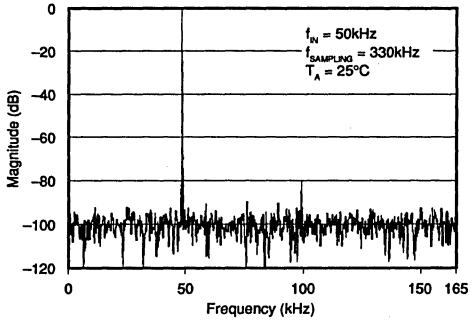
TYPICAL PERFORMANCE CURVES

$+V_S$ = +5V, $-V_S$ = −15V, and T_A = +25°C, unless otherwise noted. All plots use 1024 point FFTs.

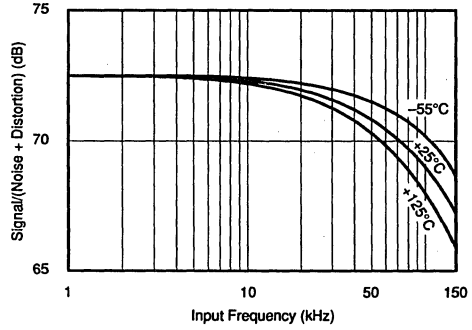
FREQUENCY SPECTRUM (10kHz f_{IN})



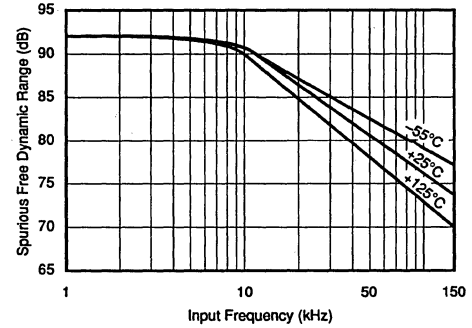
FREQUENCY SPECTRUM (50kHz f_{IN})



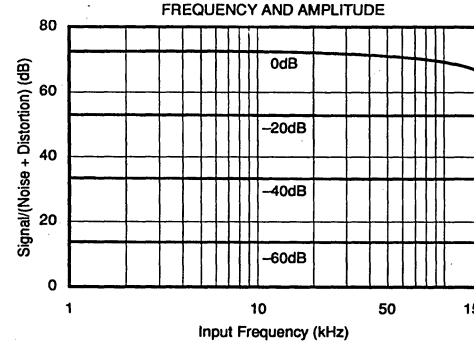
SIGNAL/(NOISE + DISTORTION) vs
INPUT FREQUENCY AND AMBIENT TEMPERATURE



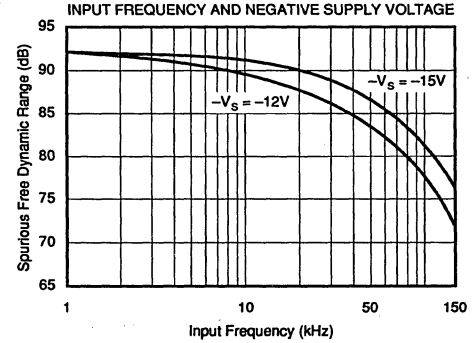
SPURIOUS FREE DYNAMIC RANGE vs
INPUT FREQUENCY AND AMBIENT TEMPERATURE



SIGNAL/(NOISE + DISTORTION) vs
FREQUENCY AND AMPLITUDE

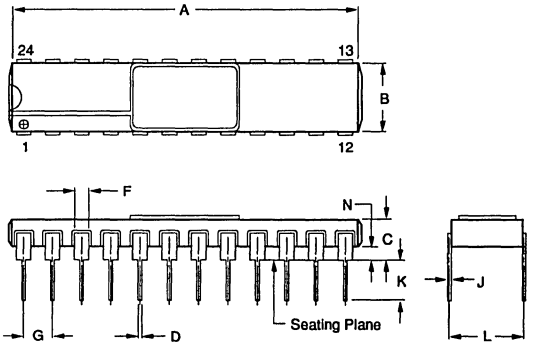


SPURIOUS FREE DYNAMIC RANGE vs
INPUT FREQUENCY AND NEGATIVE SUPPLY VOLTAGE



MECHANICAL

H Package — 24-Pin Side Braze Ceramic

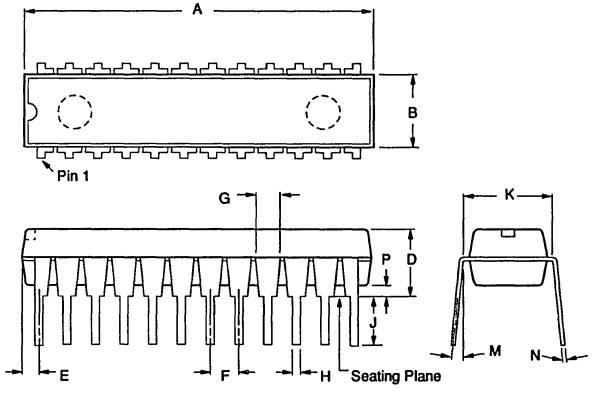


	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.188	1.212	30.18	30.78
B	.300	.320	7.62	8.13
C	—	.160	—	4.06
D	.016	.020	0.41	0.51
F	.050 TYP		1.27 TYP	
G	.095	.105	2.41	2.67
J	.009	.012	0.23	0.31
K	.170 BASIC		4.32 BASIC	
L	.290	.310	7.37	7.87
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

MECHANICAL

P Package — 24-Pin Plastic DIP

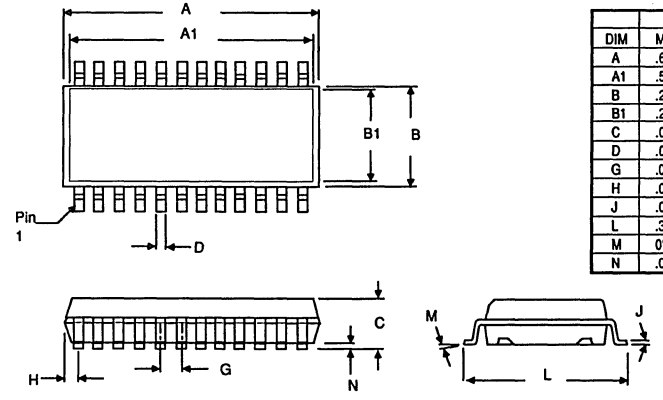


	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.125	1.255	28.58	31.88
B	.250	.290	6.35	7.37
D	.150	.170	3.81	4.32
E	.010	.080	.25	2.03
F	.100 BASIC		2.54 BASIC	
G	.050	.070	1.27	1.78
H	.016	.025	0.41	0.64
J	.125		3.18	
K	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.008	.015	0.20	0.38
P	.010	.030	.25	.76

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

MECHANICAL

U Package—24-Pin SOIC



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.602	.618	15.29	15.70
A1	.595	.618	15.11	15.70
B	.286	.302	7.26	7.67
B1	.270	.285	6.86	7.24
C	.093	.108	2.36	2.74
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.026	.034	0.66	0.86
J	.008	.012	0.20	0.30
L	.390	.422	9.91	10.72
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

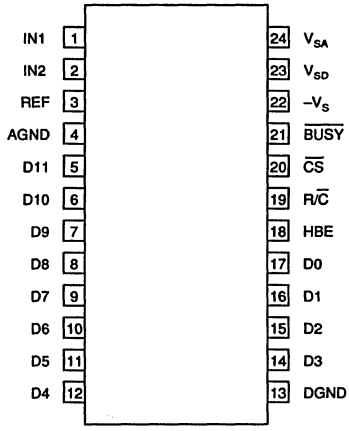
PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	IN1	±10V Analog Input. Connected to GND for ±5V range.
2	IN2	±5V Analog Input. Connected to GND for ±10V range.
3	REF	+2V Reference Output. Bypass to GND with 22µF to 47µF Tantalum. Buffer for external loads.
4	AGND	Analog Ground. Connect to pin 13.
5	D11	Data Bit 11. Most Significant Bit (MSB).
6	D10	Data Bit 10.
7	D9	Data Bit 9.
8	D8	Data Bit 8.
9	D7	Data Bit 7 if HBE is LOW; LOW if HBE is HIGH.
10	D6	Data Bit 6 if HBE is LOW; LOW if HBE is HIGH.
11	D5	Data Bit 5 if HBE is LOW; LOW if HBE is HIGH.
12	D4	Data Bit 4 if HBE is LOW; LOW if HBE is HIGH.
13	DGND	Digital Ground. Connect to pin 4.
14	D3	Data Bit 3 if HBE is LOW; Data Bit 11 if HBE is HIGH.
15	D2	Data Bit 2 if HBE is LOW; Data Bit 10 if HBE is HIGH.
16	D1	Data Bit 1 if HBE is LOW; Data Bit 9 if HBE is HIGH.
17	D0	Data Bit 0 if HBE is LOW. Least Significant Bit (LSB); Data Bit 8 if HBE is HIGH.
18	HBE	High Byte Enable. When held LOW, data output as 12-bits in parallel. When held HIGH, four MSBs presented on pins 14-17, pins 9-12 output LOWs. Must be LOW to initiate conversion.
19	R/$\overline{C}$	Read/Convert. Falling edge initiates conversion when $\overline{CS}$ is LOW, HBE is LOW, and $\overline{BUSY}$ is HIGH.
20	$\overline{CS}$	Chip Select. Outputs in Hi-Z state when HIGH. Must be LOW to initiate conversion or read data.
21	$\overline{BUSY}$	Busy. Output LOW during conversion. Data valid on rising edge in Convert Mode.
22	$-V_S$	Negative Power Supply. −12V or −15V. Bypass to GND.
23	V_{SD}	Positive Digital Power Supply. +5V. Connect to pin 24, and bypass to GND.
24	V_{SA}	Positive Analog Power Supply. +5V. Connect to pin 23, and bypass to GND.

ABSOLUTE MAXIMUM RATINGS

$-V_S$ to ANALOG COMMON	−16.5V
V_S to DIGITAL COMMON	+7V
Pin 23 (V_{SD}) to Pin 24 (V_{SA})	±0.3V
ANALOG COMMON to DIGITAL COMMON	±1V
Control Inputs to DIGITAL COMMON	−0.3 to V_S + 0.3V
Analog Input Voltage	±20V
Maximum Junction Temperature	160°C
Internal Power Dissipation	750mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}:	
Plastic DIP	100°C/W
SOIC	100°C/W
Ceramic	50°C/W

PIN CONFIGURATION



ORDERING INFORMATION:

Model	Integral Linearity Error (LSB)	Signal-to-(Noise+Distortion) Ratio (dB min)	Specification Temperature Range (°C)	Package
ADS7800JP	±1	67	0 to +70	Plastic DIP
ADS7800KP	±1/2	69	0 to +70	Plastic DIP
ADS7800JU	±1	67	0 to +70	Plastic SOIC
ADS7800KU	±1/2	69	0 to +70	Plastic SOIC
ADS7800AH	±1	67	−40 to +85	Ceramic DIP
ADS7800BH	±1/2	69	−40 to +85	Ceramic DIP

CAUTION

The ADS7800 is an ESD (electrostatic discharge) sensitive device. The digital control inputs have a special FET structure, which turns on when the input exceeds the supply by 18V, to minimize ESD damage. However, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. When not in use, devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

THEORY OF OPERATION

The ADS7800 combines the advantages of advanced CMOS technology (logic density, stable capacitors, and good analog switches) with Burr-Brown's proven skills in laser-trimmed thin-film resistors to provide a complete sampling analog-to-digital converter.

A basic charge-redistribution successive approximation architecture converts analog input voltages into digital words. Figure 1 shows the operation of a simplified three bit charge redistribution A-to-D. Precision laser-trimmed scaling resistors at the input divide standard input ranges (±10V or ±5V for the ADS7800) into levels compatible with the CMOS characteristics of the internal capacitor array.

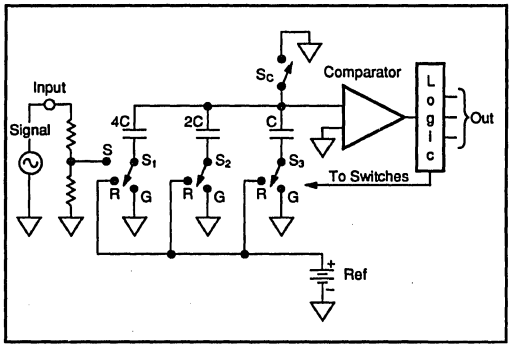


FIGURE 1. 3-Bit Charge Redistribution A-to-D.

While in the sampling mode, the capacitor array switch for the MSB capacitor (S_1) is in position "S", so that the charge on the MSB capacitor is proportional to the voltage level of the analog input signal, and the remaining array switches (S_2 and S_3) are set to position "R" to provide an accurate bipolar offset from the reference source REF. At the same time, switch S_C is also in the closed position to auto-zero any offset errors in the CMOS comparator.

When a convert command is received, switch S_1 is opened to trap a charge on the MSB capacitor proportional to the input level at the time of the sampling command, switches S_2 and S_3 are opened to trap an offset charge, and switch S_C is opened to float the comparator input. The charge trapped on the capacitor array can now be moved between the three capacitors in the array by connecting switches S_1, S_2 and S_3 to positions "R" (to connect to REF) or "G" (to connect to GND) successively, changing the voltage generated at the comparator input node.

The first approximation connects the MSB capacitor via switch S_1 to REF, while switches S_2 and S_3 are connected to GND. Depending on whether the comparator output is HIGH or LOW, the logic will then latch S_1 in position "R" or "G", and moves on to make the next approximation by connecting S_2 to REF and S_3 to GND. When the three successive approximation steps are made for this simple converter, the voltage level at the comparator will be within 1/2LSB of GND, and the data output word will be based on reading the positions of S_1, S_2 and S_3.

OPERATION

BASIC OPERATION

Figure 2 shows the simple hookup circuit required to operate the ADS7800 in a ±10V range in the Convert Mode. A convert command arriving on pin 19, R/$\overline{C}$, (a pulse taking pin 19 LOW for a minimum of 40ns) puts the ADS7800 in the hold mode, and a conversion is started. Pin 21, $\overline{BUSY}$, will be held LOW during the conversion, and rises only after the conversion is completed and the data has been transferred to the output latches. Thus, the rising edge of the signal on pin 21 can be used to read the data from the conversion. Also, during conversion, the $\overline{BUSY}$ signal puts the output data lines in Hi-Z states and inhibits input lines. This means that pulses on pin 19 are ignored, so that new

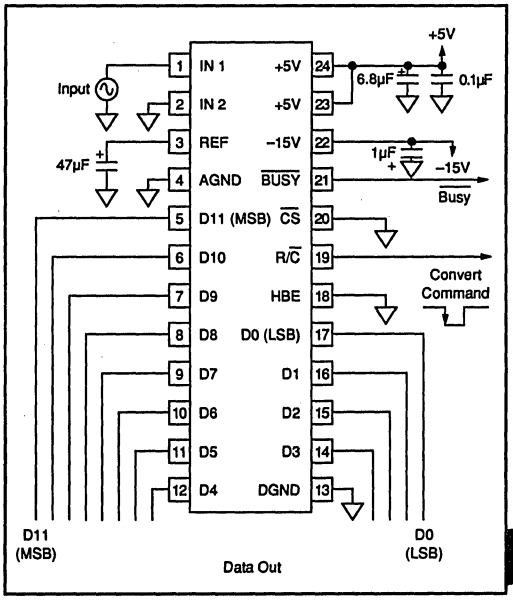


FIGURE 2. Basic ±10V Operation .

conversions cannot be initiated during a conversion, either as a result of spurious signals or to short-cycle the ADS7800.

In the Read Mode, the input to pin 19 is kept normally LOW, and a HIGH pulse is used to read data and initiate a conversion. In this mode, the rising edge of R/$\overline{C}$ on pin 19 will enable the output data pins, and the data from the previous conversion becomes valid. The falling edge then puts the ADS7800 in a hold mode, and initiates a new conversion.

The ADS7800 will begin acquiring a new sample as soon as the conversion is completed, even before the $\overline{BUSY}$ output rises on pin 21, and will track the input signal until the next conversion is started, whether in the Convert Mode or the Read Mode.

For use with an 8-bit bus, the data can be read out in two bytes under the control of pin 18, HBE. With a LOW input on pin 18, at the end of a conversion, the 8 LSBs of data are loaded into the latches on pins 9 through 12 and 14 through 17. Taking pin 18 HIGH then loads the 4 MSBs on pins 14 through 17, with pins 9 through 12 being forced LOW.

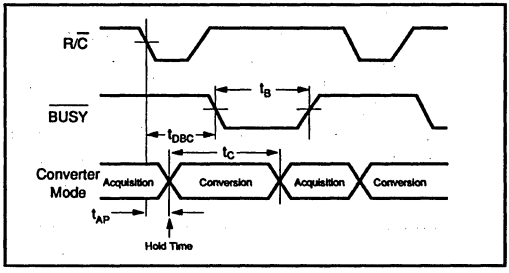


FIGURE 3. Acquisition and Conversion Timing.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{DBC}	BUSY delay from R/C		80	150	ns
t_B	BUSY Low		2.5	2.7	µs
t_{AP}	Aperture Delay		13		ns
Δt_{AP}	Aperture Jitter		150		ps, rms
t_C	Conversion Time		2.47	2.70	µs

TABLE I. Acquisition and Conversion Timing.

ANALOG INPUT RANGES

The ADS7800 offers two standard bipolar input ranges: ±10V and ±5V. If a ±10V range is required, the analog input signal should be connected to pin 1. A signal requiring a ±5V range should be connected to pin 2. In either case, the other pin of the two must be grounded or connected to the adjustment circuits described in the section on calibration. (See Figures 4 and 5, or 10 and 11.)

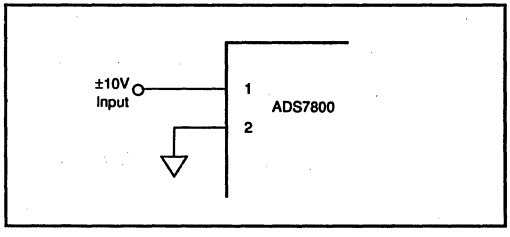


FIGURE 4. ±10V Range Without Trims.

CONTROLLING THE ADS7800

The ADS7800 can be easily interfaced to most microprocessor-based and other digital systems. The microprocessor may take full control of each conversion, or the ADS7800 may operate in a stand-alone mode, controlled only by the R/C input. Full control consists of initiating the conversion and reading the output data at user command, transmitting data either all 12-bits in one parallel word, or in two 8-bit bytes. The three control inputs (CS, R/C and HBE) are all TTL/CMOS compatible. The functions of the control lines are shown in Table II.

CS	R/C	HBE	BUSY	OPERATION
1	X	X	1	None - Outputs in Hi-Z State.
0	1↓0	0	1	Holds Signal and Initiates Conversion.
0	1	0	1	Output Three-State Buffers Enabled once Conversion has Finished.
0	1	1	1	Enable Hi-Byte in 8-bit Bus Mode.
0	1↓0	1	1	Inhibit Start of Conversion.
0	0	1	1	None - Outputs in Hi-Z State.
X	X	X	0	Conversion in Progress. Outputs Hi-Z State. New Conversion Inhibited until Present Conversion has Finished.

TABLE II. Control Line Functions.

For stand-alone operation, control of the ADS7800 is accomplished by a single control line connected to R/C. In this mode, CS and HBE are connected to GND. The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a HIGH-to-LOW transition on R/C. The three-state data output buffers are enabled when R/C is HIGH and BUSY is HIGH. Thus, there are two possible modes of operation: conversion can be initiated with either positive or negative pulses. In either case, the R/C pulse must remain LOW a minimum of 40ns.

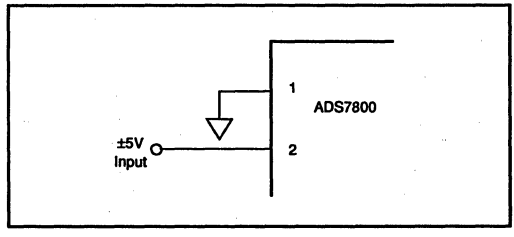


FIGURE 5. ±5V Range Without Trims.

Figure 6 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes LOW and returns HIGH during the conversion. In this case (Convert Mode), the three-state outputs go into the Hi-Z state in response to the falling edge of R/$\overline{C}$, and are enabled for external access of the data after completion of the conversion.

Figure 7 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode (Read Mode), the output data from the previous conversion is enabled during the HIGH portion of R/$\overline{C}$. A new conversion starts on the falling edge of R/$\overline{C}$, and the three-state outputs return to the Hi-Z state until the next occurrence of a HIGH on R/$\overline{C}$.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_W	R/$\overline{C}$ Pulse Width	40	10		ns
t_{DBC}	$\overline{BUSY}$ delay from R/$\overline{C}$		80	150	ns
t_B	$\overline{BUSY}$ LOW		2.5	2.7	µs
t_{AP}	Aperture Delay		13		ns
Δt_{AP}	Aperture Jitter		150		ps, rms
t_C	Conversion Time		2.47	2.70	µs
t_{DBE}	$\overline{BUSY}$ from End of Conversion		100		ns
t_{DB}	$\overline{BUSY}$ Delay after Data Valid	25	75	200	ns
t_A	Acquisition Time		130	300	ns
t_A+t_C	Throughput Time		2.6	3.0	µs
t_{HDR}	Valid Data Held After R/$\overline{C}$ LOW	20	50		ns
t_S	$\overline{CS}$ or HBE LOW before R/$\overline{C}$ Falls	25	5		ns
t_H	$\overline{CS}$ or HBE LOW after R/$\overline{C}$ Falls	25	0		ns
t_{DD}	Data Valid from $\overline{CS}$ LOW, R/$\overline{C}$ HIGH, and HBE in Desired State (Load = 100pF)		65	150	ns
t_{HDR}	Valid Data Held After R/$\overline{C}$ Low	20	50		ns
t_{HL}	Delay to Hi-Z State after R/$\overline{C}$ Falls or $\overline{CS}$ Rises (3kΩ Pullup or Pulldown)		50	150	ns

TABLE III. Timing Specifications (T_{MIN} to T_{MAX}).

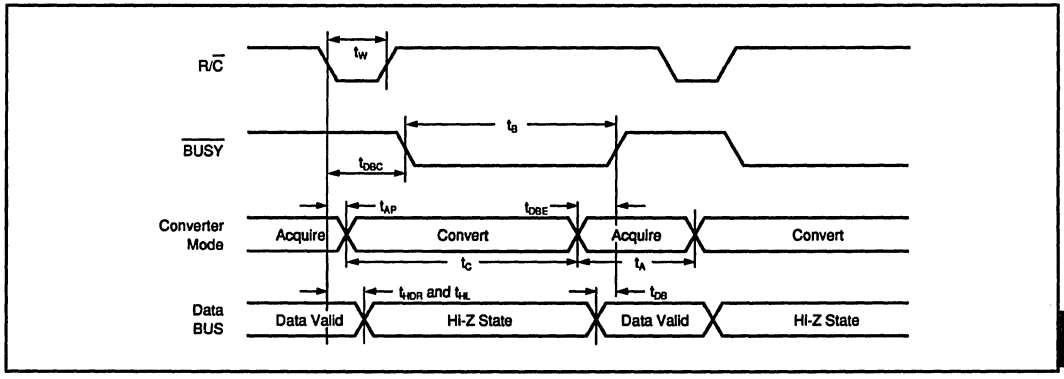


FIGURE 6. Convert Mode: R/$\overline{C}$ Pulse LOW — Outputs Enabled After Conversion.

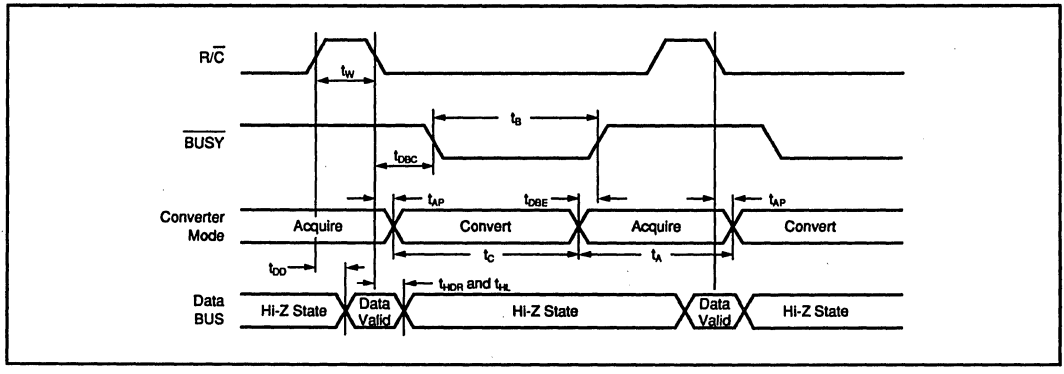


FIGURE 7. Read Mode: R/$\overline{C}$ Pulse HIGH— Outputs Enabled Only When R/$\overline{C}$ is High.

CONVERSION START

A conversion is initiated on the ADS7800 only by a negative transition occurring on R/$\overline{C}$, as shown in Table I. No other combination of states or transitions will initiate a conversion. Conversion is inhibited if either $\overline{CS}$ or HBE are HIGH, or if $\overline{BUSY}$ is LOW. $\overline{CS}$ and HBE should be stable a minimum of 25ns prior to the transition on R/$\overline{C}$.Timing relationships for start of conversion are illustrated in Figure 8.

The $\overline{BUSY}$ output indicates the current state of the converter by being LOW only during conversion. During this time the three-state output buffers remain in a Hi-Z state, and therefore data cannot be read during conversion. During this period, additional transitions on the three digital inputs ($\overline{CS}$, R/$\overline{C}$ and HBE) will be ignored, so that conversion cannot be prematurely terminated or restarted.

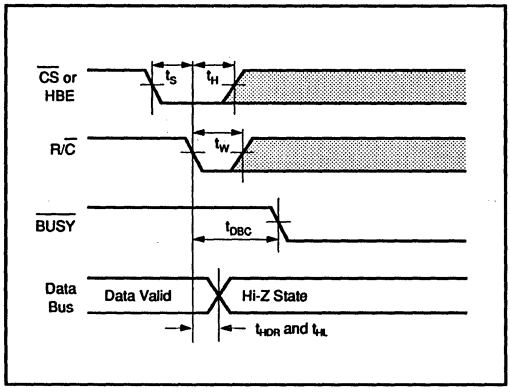


FIGURE 8. Conversion Start Timing.

INTERNAL CLOCK

The ADS7800 has an internal clock that is factory trimmed to achieve a typical conversion time of 2.47µs, and a maximum conversion time over the full operating temperature range of 2.7µs. No external adjustments are required, and with the guaranteed maximum acquisition time of 300ns, throughput performance is assured with convert pulses as close as 3µs.

READING DATA

After conversion is initiated, the output buffers remain in a Hi-Z state until the following three logic conditions are simultaneously met: R/$\overline{C}$ is HIGH, $\overline{BUSY}$ is HIGH and $\overline{CS}$ is LOW. Upon satisfaction of these conditions, the data lines are enabled according to the state of HBE. See Figure 9 and Table III for timing relationships and specifications.

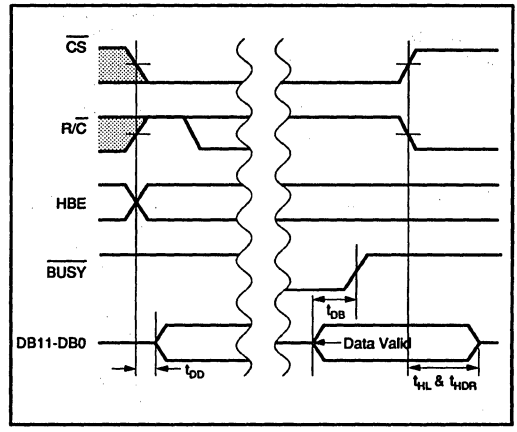


FIGURE 9. Read Cycle Timing.

CALIBRATION

OPTIONAL EXTERNAL GAIN AND OFFSET TRIM

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADS7800 as shown in Figures 10 and 11.

If adjustment of offset and full scale is not required, connections as shown in Figures 4 and 5 should be used.

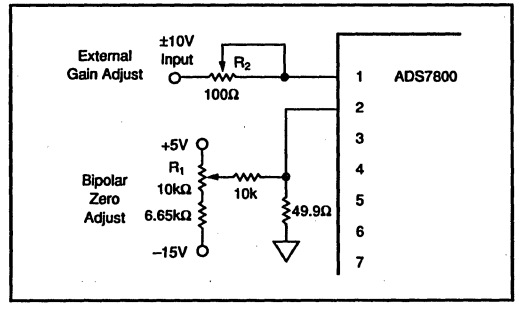


FIGURE 10. ±10V Range With External Trims.

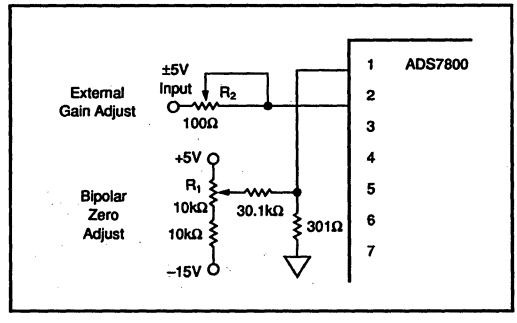


FIGURE 11. ±5V Range With External Trims.

INPUT VOLTAGE RANGE AND LSB VALUES			
Input Voltage Range Defined As:		±10V	±5V
Analog Input Connected to Pin		1	2
Pin Connected to GND		2	1
One Least Significant Bit (LSB)	FSR/2^{12}	20V/2^{12} 4.88mV	10V/2^{12} 2.44mV
OUTPUT TRANSITION VALUES			
FFEH to FFFH	+Full Scale	+10V–3/2LSB +9.9927V	+5V–3/2LSB +4.9963V
7FFH to 800H	Mid Scale (Bipolar Zero)	0V–1/2LSB –2.44mV	0V–1/2LSB –1.22mV
000H to 001H	–Full Scale	–10V+1/2LSB –9.9976V	–5V+1/2LSB –4.9988V

TABLE IV. Input Voltages, Transition Values, and LSB Values.

CALIBRATION PROCEDURE

First, trim offset, by applying at the input (pin 1 or 2) the mid-point transition voltage (–2.44mV for the ±10V range, –1.22mV for the ±5V range.) With the ADS7800 converting continually, adjust potentiometer R_1 until the MSB (D11 on pin 5) is toggling alternately HIGH and LOW.

Next adjust full scale, by applying at the input a DC input signal that is 3/2LSB below the nominal full scale voltage (+9.9927V for the ±10V range, +4.9963V for the ±5V range.) With the ADS7800 converting continually, adjust R2 until the LSB (D0 on pin 17) is toggling HIGH and LOW with all of the other bits HIGH.

LAYOUT CONSIDERATIONS

Because of the high resolution and linearity of the ADS7800, system design problems such as ground path resistance and contact resistance become very important.

ANALOG SIGNAL SOURCE IMPEDANCE

The input resistance of the ADS7800 is 6.3kΩ or 4.2kΩ (for the ±10V and ±5V ranges respectively.) To avoid introducing distortion, the source resistance must be very low, or constant with signal level. The output impedance provided by most op amps is ideal.

Pins 23 (V_{SD}) and 24 (V_{SA}) are not connected internally on the ADS7800, to maximize accuracy on the chip. They should be connected together as close as possible to the unit. Pin 24 may be slightly more sensitive than pin 23 to supply variations, but to maintain maximum system accuracy, both should be well isolated from digital supplies with wide load variations.

To limit the effects of digital switching elsewhere in a system on the analog performance of the system, it often makes sense to run a separate +5V supply conductor from the supply regulator to any analog components requiring +5V, including the ADS7800.

The V_S pins (23 and 24) should be connected together and bypassed with a parallel combination of a 6.8µF Tantalum capacitor and a 0.1µF ceramic capacitor located close to the converter to obtain noise-free operation. (See Figure 2.) The $-V_S$ pin 22 should be bypassed with a 1µF tantalum capacitor, again as close as possible to the ADS7800.

Noise on the power supply lines can degrade converter performance, especially noise and spikes from a switching power supply. Appropriate supplies or filters must be used.

The GND pins (4 and 13) are also separated internally, and should be directly connected to a ground plane under the converter if at all possible. A ground plane is usually the best solution for preserving dynamic performance and reducing noise coupling into sensitive converter circuits. Where any compromises must be made, the common return of the analog input signal should be referenced to pin 4, AGND, on the ADS7800, which prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and related resistors should be located as close to the ADS7800 as possible.

REFERENCE BYPASS

Pin 3 (REF) should be bypassed with a 22µF to 47µF tantalum capacitor. A rated working voltage of 2V or more is acceptable here. This pin is used to enhance the system accuracy of the internal reference circuit, and is not recommended for driving external signals. If there are important system reasons for using the ADS7800 reference externally, the output of pin 3 must be appropriately buffered.

"HOT SOCKET" PRECAUTION

Two separate +5V V_S pins, 23 and 24, are used to minimize noise caused by digital transients. If one pin is powered and the other is not, the ADS7800 may "Latch Up" and draw excessive current. In normal operation, this is not a problem because both pins will be soldered together. However, during evaluation, incoming inspection, repair, etc., where the potential of a "Hot Socket" exists, care should be taken to power the ADS7800 only after it has been socketed.

MINIMIZING "GLITCHES"

Coupling of external transients into an analog-to-digital converter can cause errors which are difficult to debug. In addition to the discussions earlier on layout considerations for supplies, bypassing and grounding, there are several other useful steps that can be taken to get the best analog performance out of a system using the ADS7800. These potential system problem sources are particularly important to consider when developing a new system, and looking for the causes of errors in breadboards.

First, care should be taken to avoid glitches during critical times in the sampling and conversion process. Since the ADS7800 has an internal sample/hold function, the signal that puts it into the hold state (R/$\overline{C}$ going LOW) is critical, as it would be on any sample/hold amplifier. The R/$\overline{C}$ falling edge should be sharp and have minimal ringing, especially during the 20ns after it falls.

Although not normally required, it is also good practice to avoid glitching the ADS7800 while bit decisions are being made. Since the above discussion calls for a fast, clean rise and fall on R/$\overline{C}$, it makes sense to keep the rising edge of the convert pulse outside the time when bit decisions are being made. In other words, the convert pulse should either be short (under 100ns so that it transitions before the MSB decision), or relatively long (over 2.75µs to transition after the LSB decision).

Next, although the data outputs are forced into a Hi-Z state during conversion, fast bus transients can still be capacitively coupled into the ADS7800. If the data bus experiences fast transients during conversion, these transients can be attenuated by adding a logic buffer to the data outputs. The $\overline{BUSY}$ output can be used to enable the buffer.

Naturally, transients on the analog input signal are to be avoided, especially at times within ±20ns of R/$\overline{C}$ going LOW, when they may be trapped as part of the charge on the capacitor array. This requires careful layout of the circuit in front of the ADS7800.

Finally, in multiplexed systems, the timing on when the multiplexer is switched may affect the analog performance of the system. In most applications, the multiplexer can be switched as soon as R/$\overline{C}$ goes LOW (with appropriate delays), but this may affect the conversion if the switched signal shows glitches or significant ringing at the ADS7800 input. Whenever possible, it is safer to wait until the conversion is completed before switching the multiplexer. The extremely fast acquisition time and conversion time of the ADS7800 make this practical in many applications.

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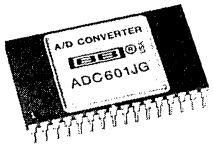


ADC601

12-Bit 900ns ANALOG-TO-DIGITAL CONVERTER

FEATURES

- FAST CONVERSION: 900ns
- CAN BE SHORT-CYCLED
- INPUT RANGES: ±5V, ±10V, 0 to –10V
- HIGH SIGNAL/NOISE RATIO: 68dB
- LOW IMD: 75dB
- PARALLEL AND SERIAL OUTPUT
- 32-PIN CERAMIC DIP PACKAGE

APPLICATIONS

- DIGITAL SIGNAL PROCESSING
- HIGH-SPEED DATA ACQUISITION SYSTEMS
- MEDICAL INSTRUMENTATION
- ANALYTICAL INSTRUMENTATION
- TEST AND IMAGING SYSTEMS
- WAVEFORM ANALYZERS

DESCRIPTION

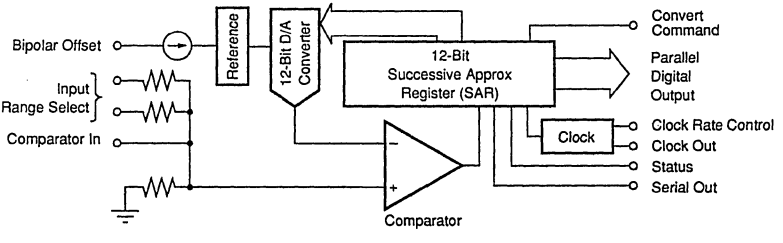
The ADC601 is a high-speed Duolithic™ (two chips) successive approximation analog-to-digital converter. This unique two-chip design utilizes a bipolar technology with on-chip thin film resistors to preserve analog accuracy and a high-speed CMOS chip to perform digital logic control. Outstanding linearity, noise, and dynamic range are achieved by this converter design. The ADC601 has been tested with several sample/hold amplifiers and distortion results are documented in this data sheet.

The ADC601 is complete with internal reference, clock, and comparator and is packaged in a 32-pin ceramic DIP. Conversion time is set at the factory to 900ns. Serial and parallel output performance is guaranteed with no missing codes over the full input voltage, power supply, and operating temperature range. The gain and offset errors are laser trimmed to specification. Optionally they may be externally adjusted to zero.

Internal scaling resistors are provided for the selection of analog signal input ranges of ±5V, ±10V and 0V to –10V. The ADC601's input is specifically designed to be easily driven with minimal disturbance to the driving amplifier.

Output codes are available in complementary binary for unipolar inputs and bipolar offset binary for bipolar inputs.

All digital inputs and outputs are TTL-compatible. Power supply requirements are ±15V and +5V.



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PDS-867B

SPECIFICATIONS

ELECTRICAL

T_{CASE} = +25°C, 900ns conversion time, $\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, and 6-minute warm-up in a normal convection environment unless otherwise noted.

PARAMETER	CONDITIONS	ADC601JG MIN	ADC601JG TYP	ADC601JG MAX	ADC601KG MIN	ADC601KG TYP	ADC601KG MAX	UNITS
RESOLUTION				12			*	Bits
ANALOG CHARACTERISTICS								
INPUTS								
Voltage Ranges: Bipolar	Full Scale(FSR)[1][2]		±5, ±10			*		V
Unipolar	Full Scale(FSR)[1][2]		0 to –10			*		V
Impedance: –10V to 0V, ±5V			1.4			*		kΩ
±10V			2.4			*		kΩ
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error[3]	990ns Conversion Time		±0.08	±0.55		*	±0.2	%
Input Offset Error[3]: Unipolar	990ns Conversion Time		±0.12	±1.2		*	±0.5	% of FSR
Bipolar	990ns Conversion Time		±0.08	±0.8		*	±0.25	% of FSR
Integral Linearity Error	990ns Conversion Time			±0.024			±0.012	% of FSR
Differential Linearity Error	990ns Conversion Time			±0.024			±0.012	% of FSR
No Missing Codes				Guaranteed				
Power Supply Rejection of Offset and Gain	$\Delta +V_{CC}$ = ±5%		±0.0036			*		$\%FSR/\%V_{CC}$
	$\Delta -V_{CC}$ = ±5%		±0.0005			*		$\%FSR/\%V_{CC}$
	$\Delta +V_{DD}$ = ±5%		±0.001				*	$\%FSR/\%V_{DD}$
DIGITAL CHARACTERISTICS								
INPUT								
Logic Family				TTL-Compatible CMOS				
Convert Command Logic Voltages	Logic Low	0		+0.8	*		*	V
	Logic High	+2		$+V_{DD}$	*		*	V
Convert Command Currents	Logic Low			–150				µA
	Logic High			–150				µA
Convert Command				High Level When Converting				
CONVERSION TIME								
Factory Set	Without User Adjustment		0.9	1		*	*	µs
Power Supply Rejection of Conversion Time	D $+V_{DD}$ = ±5%		±1			*		$ns/\%V_{DD}$
OUTPUT								
Logic Family				TTL-Compatible CMOS				
Bits 1 through 12, Serial, Status, Clock Out	Logic Low, I_{OL} = 3.2mA		+0.1	+0.4		*	*	V
	Logic High, I_{OH} = –1mA	+2.7	+4.9		*	*	*	V
Internal Clock Frequency			13			*		MHz
Status				Low Level When Data Valid				
DYNAMIC CHARACTERISTICS [4][5][6] Tested using Sample/Hold Amplifier SHC804 and ADC601 (See Typical Performance Curves)								
Differential Linearity Error	f_c = 10kHz: 68.3% of All Codes		0.5			0.4		LSB
	99.7% of All Codes		0.8			0.6		LSB
	100% of All Codes		1.0			0.7		LSB
Total Harmonic Distortion	f_c = 10kHz, f_s = 500kHz		–70			*		dBc
	f_c = 10kHz, f_s = 1MHz		–74			*		dBc
	f_c = 100kHz, f_s = 500kHz		–72			*		dBc
	f_c = 250kHz, f_s = 500kHz		–70			*		dBc
	f_c = 500kHz, f_s = 1MHz		–68			*		dBc
Two-Tone Intermodulation Distortion[7]	f_c = 11kHz and 15kHz, f_s = 500kHz		–79			*		dBc
	f_c = 50kHz and 55kHz, f_s = 500kHz		–78			*		dBc
	f_c = 90kHz and 110kHz, f_s = 500kHz		–77			*		dBc
Signal-to-Noise and Distortion (SINAD) Ratio	f_c = 100kHz, f_s = 500kHz		67			*		dB
	f_c = 250kHz, f_s = 500kHz		66			*		dB
	f_c = 500kHz, f_s = 1MHz		65			*		dB
Signal-to-Noise Ratio (SNR)	f_c = 100kHz, f_s = 500kHz		69			*		dB
	f_c = 250kHz, f_s = 500kHz		68			*		dB
	f_c = 500kHz, f_s = 1MHz		67			*		dB
PERFORMANCE OVER TEMPERATURE								
Gain	T_{MIN} to T_{MAX}		±10	±30		*	*	ppm of FSR/°C
Input Offset: Unipolar	T_{MIN} to T_{MAX}		±2	±7		*	*	ppm of FSR/°C
Bipolar	T_{MIN} to T_{MAX}		±3	±10		*	*	ppm of FSR/°C
Internal Linearity Error	0.9µs Conversion Time T_{MIN} to T_{MAX}		±0.02			±0.015		% of FSR
Differential Linearity Error	0.9µs Conversion Time T_{MIN} to T_{MAX}		±0.02			±0.015		% of FSR
No Missing Codes	0.9µs Conversion Time T_{MIN} to T_{MAX}			Guaranteed				
Conversion Drift			2			*		ns/°C

SPECIFICATIONS (cont)

ELECTRICAL

T_{CASE} = +25°C, 900ns conversion time, $\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, and 6-minute warm-up in a normal convection environment unless otherwise noted.

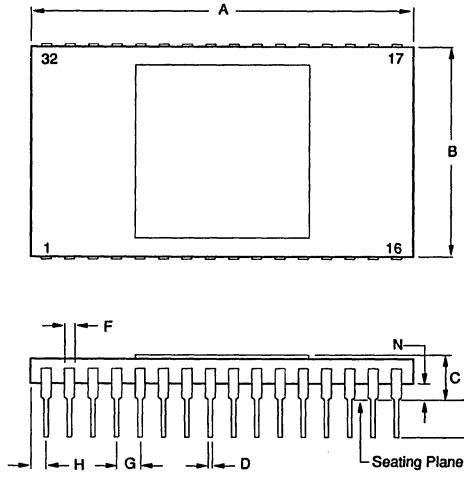
PARAMETER	CONDITIONS	ADC601JG MIN	ADC601JG TYP	ADC601JG MAX	ADC601KG MIN	ADC601KG TYP	ADC601KG MAX	UNITS
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$		+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		−14.25	−15	−15.75	*	*	*	V
$+V_{DD}$		+4.75	+5	+5.25	*	*	*	V
Supply Currents: $+I_{CC}$			5.4	7.0		*	*	mA
$-I_{CC}$			−65	−84.5		*	*	mA
$+I_{DD}$			53	68.9		*	*	mA
Power Consumption	Nominal $\pm V_{CC}$ and $+V_{DD}$		1.3	1.7		*	*	W
Thermal Resistance, θ_{JC}			25			*	*	°C/W
TEMPERATURE RANGE[8]								
Specification		0		+70	*		*	°C
Operating		−25		+85	*		*	°C

* Same specifications as for ADC601JG.

NOTES: (1) Over or under range on the analog input results in constant maximum or minimum digital output. (2) FSR = Full Scale Range. (3) Adjustable to zero. (4) Dynamic tests are performed using SHC804 with ADC601 unless otherwise specified. Performance may vary depending upon choice of sample/hold. (5) See Typical Performance Curves. (6) dBc = level referred to carrier input signal = 0dB; f_c = input frequency; f_s = sampling frequency. (7) IMD is referred to the larger of the two input test signals. If referred to the peak envelope signal (=0dB), the intermodulation products will be 6dB lower. For example, unit connected for ±10V has 20V FSR. (8) Temperature ranges refer to case temperature. Thermal resistance was measured on a small (5" diameter) handwired circuit board; with the test device in a (zero insertion force) socket. Thermal resistance will be lower if the ADC601 is soldered into the PC board, a ground plane is used directly underneath the package, multiple PC board layers are used, or forced air cooling is employed. Use heat sinking if necessary to keep the case at specified and operating temperatures.

MECHANICAL

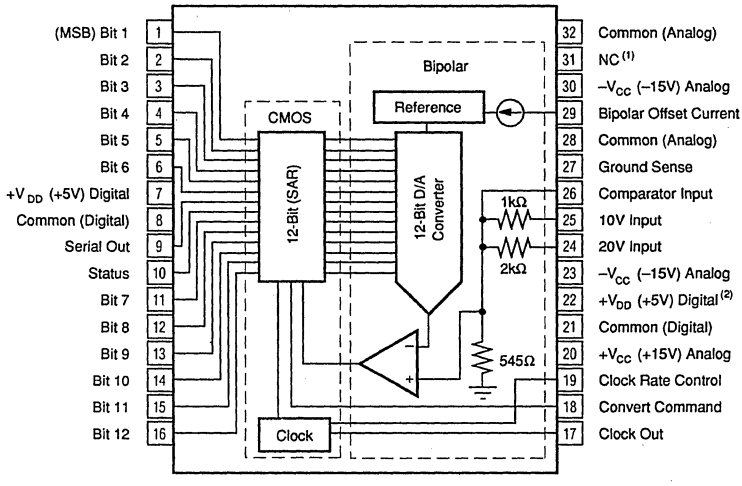
H Package — 32-Pin Hermetic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.580	1.620	40.13	41.15
B	.880	.900	22.35	22.86
C	.138	.186	3.51	4.72
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.900	.920	22.86	23.37
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

PIN CONFIGURATION



(1) NC = No internal connection. Any voltage may be connected to pin 31, however.
(2) Pin 22 must be very cleanly decoupled to keep digital noise out of the analog circuits.

PIN DEFINITIONS

PIN NUMBER	DESIGNATION	DESCRIPTION
1-6 and 11-16	Bit 1 to Bit 12	12-bit parallel output data capable of sinking 3.2mA.
9	Serial Out	12-bit serial data output synchronized with the negative edge of each appropriate clock cycle.
10	Status	Conversion status strobe is high during data conversion; low when parallel data is valid. Negative edge may be used to latch parallel data, however, appropriate latch set-up time must be provided. Refer to t_{BBL} in the ADC601 timing diagram.
17	Clock Out	Negative edge indicates when serial data is valid. After convert command goes high, fist cycle clocks bit 1 (MSB). The clock continues to run when convert command is high and resets low with convert command.
18	Convert Command	High transition starts conversion; and should remain high during conversion. Low will reset clock and SAR logic.
19	Clock Rate Control	May be used to increase clock speed, by increasing the positive portion of the clock. High is normal operation.
24	20V Input	20V input range allows ±10Vp-p analog input signal. Short to ground when not used.
25	10V Input	10V input range allows 0 to –10Vp-p or ±5Vp-p input range.
26	Comparator In	Only used in bipolar mode when it is connected to bipolar offset pin through short lead with low resistance.
27	Ground Sense	Ground Sense pin. (See text for use).
29	Bipolar Offset Current	Bipolar offset current short to comparator In through very short lead with very low resistance for bipolar operation. Short to ground for unipolar operation.

ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	±18V
$+V_{DD}$	+7V
Digital Inputs	+5.5V
Analog Inputs	$\pm V_{CC}$
Comparator Input	–3.7V to +0.7V
Case Temperature	+125°C
Junction Temperature	+165°C
Storage Temperature	–65°C to +150°C

Stresses above these ratings may permanently damage the device.

ORDERING INFORMATION

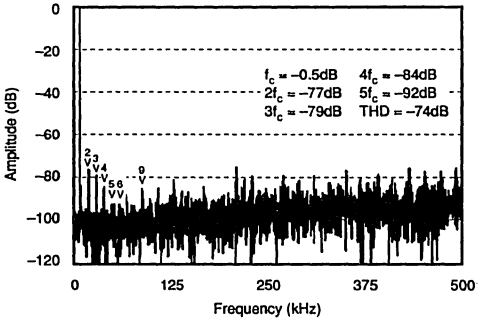
ADC601 ( ) G

Basic Model Number
Performance Grade Code
J, K: 0°C to +70°C Case Temperature
Package Code
G: Ceramic DIP

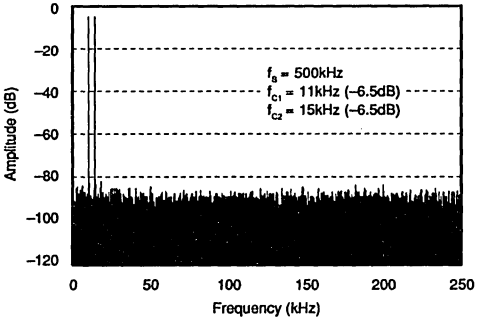
TYPICAL PERFORMANCE CURVES

$\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, 15-minute warmup, and T_C = +25°C, unless otherwise noted. All dynamic performance curves are 4096-point FFTs.

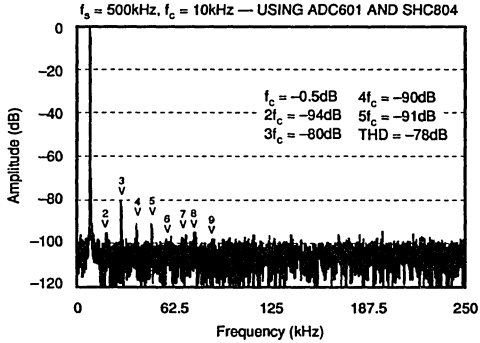
TOTAL HARMONIC DISTORTION
f_S = 1MHz, f_C = 10kHz — USING ADC601 AND SHC804



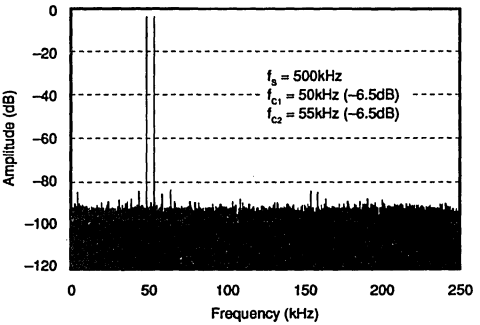
TWO-TONE INTERMODULATION
USING ADC601 AND SHC804



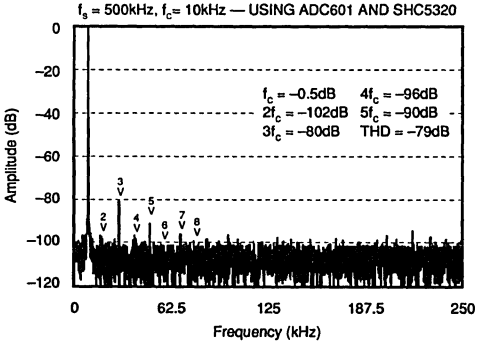
TOTAL HARMONIC DISTORTION
f_S = 500kHz, f_C = 10kHz — USING ADC601 AND SHC804



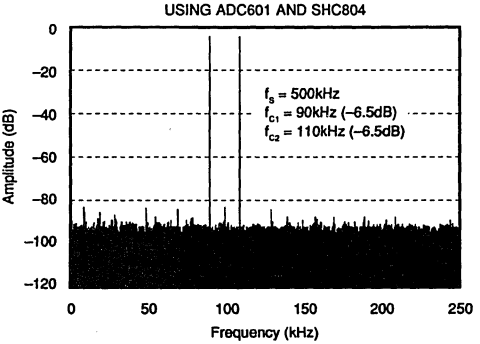
TWO-TONE INTERMODULATION
USING ADC601 AND SHC804



TOTAL HARMONIC DISTORTION
f_S = 500kHz, f_C = 10kHz — USING ADC601 AND SHC5320

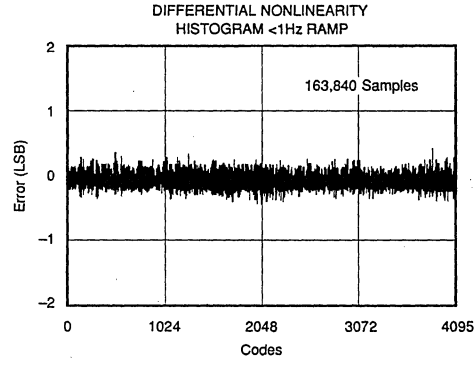


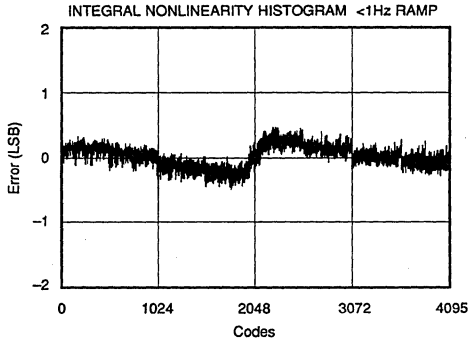
TWO-TONE INTERMODULATION
USING ADC601 AND SHC804

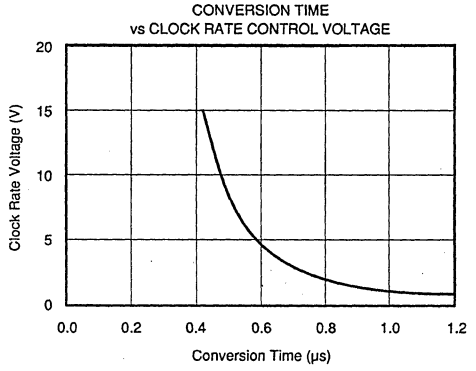


TYPICAL PERFORMANCE CURVES (cont)

$\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, R_S = 50Ω, 15-minute warmup, and T_C = +25°C, unless otherwise noted.







THEORY OF OPERATION

The ADC601 is a successive approximation analog-to-digital converter as shown on the front page of this product data sheet. A common problem with other successive approximation A/D converters is input current transients caused by the D/A converter's switching. This requires a fast-settling amplifier to drive the input and to provide a low source impedance at high frequency.

To minimize this problem, the ADC601's comparator is connected in a differential mode, greatly reducing the input transients. In addition, the input voltage scaling resistors reduce the voltage that is applied to the + input of the comparator. For best performance, a fast settling wideband sample/hold amplifier such as Burr-Brown's SHC804 is still recommended to drive the ADC601. The small signal settling time of this amplifier should be less than 100ns if sampling rates approach 1MHz.

The accuracy of a successive approximation analog-to-digital converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters

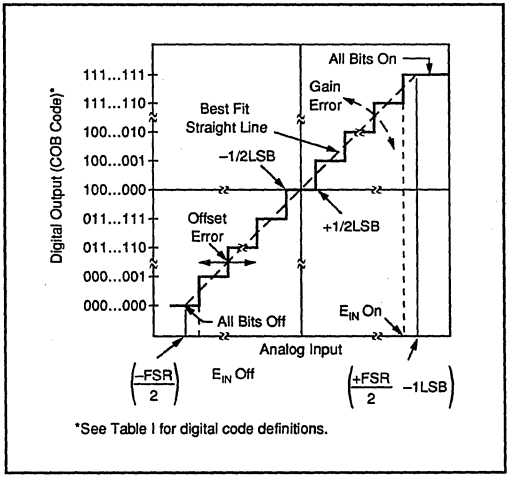


FIGURE 1. Input vs Ouput for an Ideal Bipolar A/D Converter.

have an inherent quantization error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry matching and tracking properties of the ladder and scaling networks, power supply rejection, reference errors and the dynamic errors of the DAC and comparator. Initial gain and offset errors may be adjusted to zero, gain drift over temperature rotates the transfer function (Figure 1) about the zero point, and offset drift shifts the transfer function left or right over the operating temperature range. Linearity error is not adjustable, but it is the most meaningful indicator of A/D converter accuracy. Integral linearity error is the deviation of an actual bit transition from the best fit straight line transfer function of the A/D converter. A differential linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB, ±1/2 LSB. The ADC601 is guaranteed to have no missing codes over its specified temperature range.

ACCURACY VS CONVERSION TIME

In successive approximation A/D converters, the conversion time affects integral and differential linearity error. Conversion time effects on linearity and differential linearity error for the ADC601 are shown in the Typical Performance Curves.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CONNECTION

The basic connection for the ADC601 is shown in Figure 2. It is shown connected for ±5V bipolar input operation. Refer to Table I for other connections.

INTERFACING

Because the ADC601 is a high-speed converter, it must be driven from an amplifier source that has low impedance at high frequency. The SHC803, SHC804, and SHC5320 are specifically designed to give accurate, stable results. At the ADC601 output, the digital lines should be buffered by a latch such as the 74LS574. These three-state drivers can then connect directly to the data bus.

LAYOUT PRECAUTIONS

The ADC601 is a high-speed analog-to-digital converter that requires more attention to circuit board layout than general purpose, lower speed A/D converters.

The wideband ADC601 comparator input (pin 26) is very sensitive to noise. Any connection to this point should be as short as possible and shielded by analog common or ±15VDC supply patterns. The clock output (pin 17) is sensitive to stray capacitance, and capacitance on this pin could alter the clock wave shape.

The ADC601 has two pins for analog common, two pins for digital common, and two pins for each power supply input. Each pair of these pins **must** be connected together externally. The connection between the digital supply pins and the connection between the digital common pins must be as short as possible. The analog and digital commons are not connected together internally in the ADC601.

Connecting all commons to a ground plane close to the ADC601 is the best method to minimize noise and dissipate heat as shown in Figure 3.

GROUND SENSE

A special analog ground called "ground sense" (shown in Figure 3) has been provided to eliminate the voltage drop that would otherwise be in the ground return of the internal R-2R ladder. Measuring the input signal with respect to the sense terminal (pin 27) makes the measurement independent of the connection impedance between the sense terminal and the analog common, pin 28. This sense pin must be connected to analog common as close to the input signal source as possible or connected to the ground plane. Low impedance analog and digital common returns are essential for low noise performance. To minimize coupling between analog and digital circuits on a layout, special attention should be taken to ensure that the clock noise on the +5V supply line does not couple into the analog inputs.

GROUND LOOPS

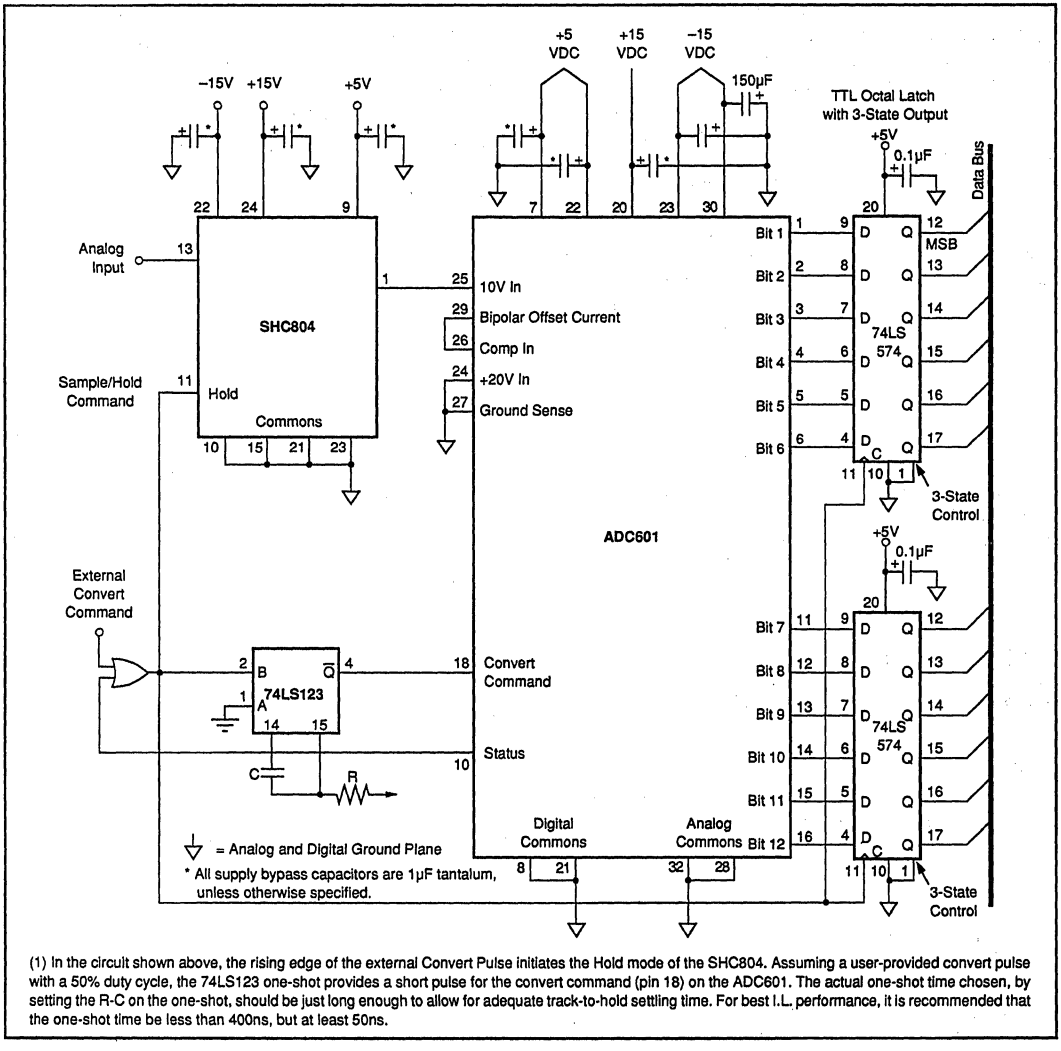
Figure 4 illustrates the interaction that occurs between the analog and digital grounds when an ADC is connected into a test circuit. This interaction is created by ground loops. The circuit shows how ground loops are created when the ADC tester combines digital and analog portions of the circuit together. In this case, the loop is between the analog test signal generator and the digital circuitry that detects the ADC code. Here the digital ground connection between the ADC and the tester is in parallel with the analog grounds. Some of the digital current is diverted into the analog signal return, which creates a code-dependent error signal due to the resistance in the analog signal return. This error distorts the linearity measurement and induces hysteresis. It can be substantially reduced if the analog and digital ground effects are isolated from each other in the ADC tester. The best method is to use a low resistance, low inductance ground plane.

POWER SUPPLY DECOUPLING

Each power supply pin should be bypassed with a 1µF or 150µF tantalum capacitor as shown in Figure 2. These capacitors should be located close to the ADC. Ceramic 0.01µF bypass capacitors have been provided internally for more effective bypassing and need not be added externally.

ADDITIONAL DECOUPLING

A 100pF capacitor may be placed on Clock Rate Adjust (pin 19) to ground in order to reduce noise on the clock. Up to 30pF may be placed on Comparator In (pin 26) without degrading conversion accuracy at Nyquist frequencies.



(1) In the circuit shown above, the rising edge of the external Convert Pulse initiates the Hold mode of the SHC804. Assuming a user-provided convert pulse with a 50% duty cycle, the 74LS123 one-shot provides a short pulse for the convert command (pin 18) on the ADC601. The actual one-shot time chosen, by setting the R-C on the one-shot, should be just long enough to allow for adequate track-to-hold settling time. For best I.L. performance, it is recommended that the one-shot time be less than 400ns, but at least 50ns.

FIGURE 2. Basic Connection Diagram in Bipolar Operation and Dynamic Test Circuit.

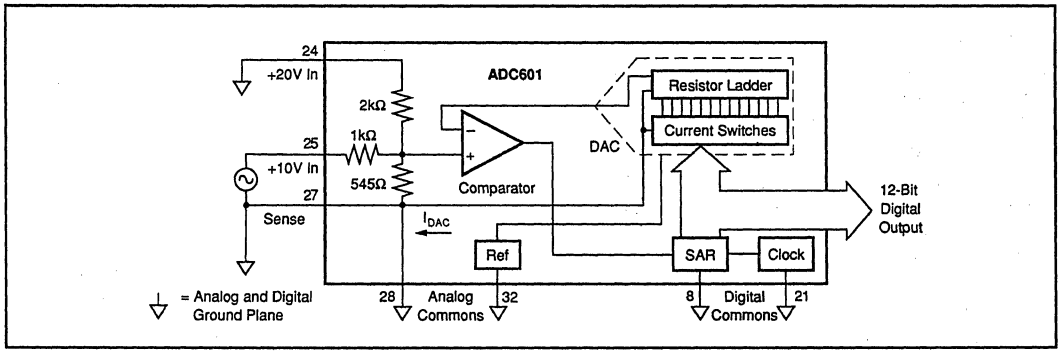


FIGURE 3. Analog and Digital Grounds, and Analog Input Sense.

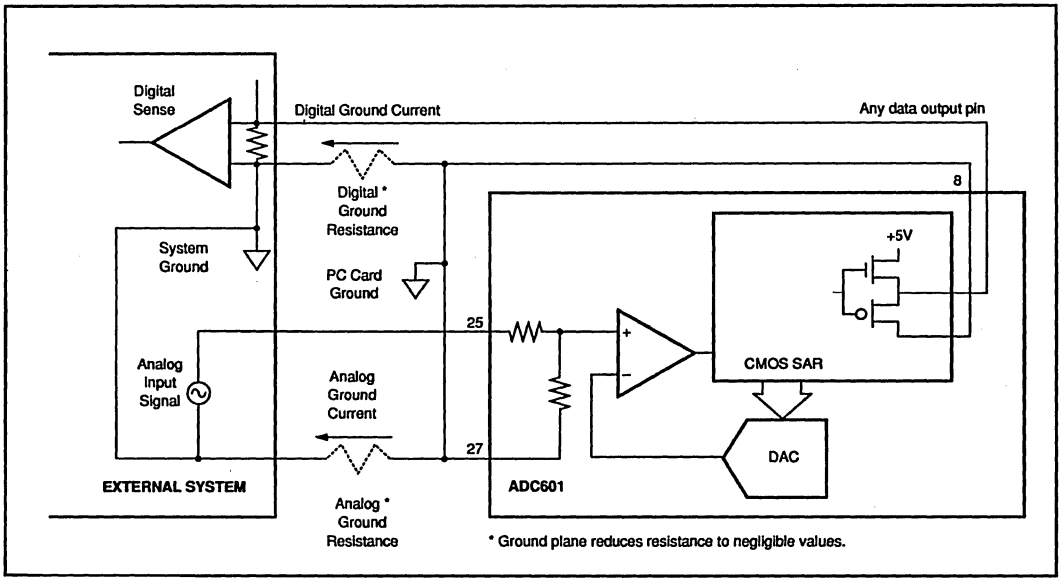


FIGURE 4. Ground Loop Interaction Between Analog and Digital Grounds when ADC Is Connected.

POWER SUPPLY SENSITIVITY

Changes in the DC power supply voltages will affect accuracy. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. Power supply decoupling, shown in Figure 2, helps to keep ripple low. Switching power supplies should be used with caution. EMI/RFI filters such as BNX002 made by Murata/Erie Company, Canada give good results with switching supplies.

INPUT RANGE SCALING

The analog input can be scaled to an appropriate input signal range by proper pin connections to the A/D converter. Connect input signals as shown in Table I.

Input Signal Range	Output Code	Connect Pin 29 To	Connect Gain Adjust	Connect Pin 24 To	Connect Pin 25 To
±10V	BOB or BTC*	26	Yes	40Ω resistor in series with input signal	Gain Adjust Potentiometer
			No	Input Signal	Analog Common
±5V	BOB or BTC*	26	Yes	Gain Adjust Potentiometer	10Ω resistor in series with input signal
			No	Analog Common	Input Signal
0 to −10V	CSB	Analog Common	Yes	Gain Adjust Potentiometer	10Ω resistor in series with input signal

* Obtained by inverting MSB (pin 1) externally.

TABLE I. ADC601 Input Scaling Connections.

INPUT IMPEDANCE

If external gain adjust is not used, the source impedance driving the ADC601 should be low (such as the output of an op amp) to avoid gain errors due to the relatively low input impedance of the ADC601.

If the source impedance is not low, a buffer amplifier can be added between the input signal and the ADC601 inputs.

BIPOLAR OFFSET CURRENT

The bipolar offset current provided in the ADC601 on pin 29 is for use only in bipolar operation where pins 26 and 29 are connected together. Pin 29 should be grounded for unipolar operation. To prevent noise interference, this output should not be used for any other purpose; make no other connection to pin 29.

OUTPUT DRIVE

All ADC601 data outputs will drive two standard TTL loads or 10 low-power Schottky TTL loads. If long digital lines must be driven, external logic buffers are required. The clock output is sensitive to capacitive loading and should be buffered if high capacitive loads are being driven.

PARALLEL AND SERIAL OUTPUT

Parallel and serial output may be used simultaneously, however proper buffering is essential. This will avoid excessive loading which can interfere with proper operation.

POWER DISSIPATION

The ADC601 dissipates approximately 1.3W. The package has a junction-to-case thermal resistance (θ_{JC}) of 25°C/W and a case-to-ambient thermal resistance (θ_{CA}) of 22°C/W in a normal convection environment. For operation above +85°C a heat sink is recommended. This should contact the bottom of the ADC601 for best results. See electrical specification table notes.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and offset errors may be trimmed to zero using external trim potentiometers as shown in Figures 5, 6, and 7. For sufficient adjustment range, a series resistor must be connected to the analog input pin as specified in Table I. Multiturn potentiometers with 100ppm/°C temperature coefficient are recommended for minimum drift. All fixed resistors should be ±1% metal film. If the Offset adjust is not used, pin 26 should be left open except for bipolar operation when it is connected to pin 29. If Gain adjust is not used, the unused input (pin 24 or 25) must be grounded to meet specified gain accuracy.

Adjustment Procedure

Refer to Table II for LSB voltages and transition values.

For unipolar offset, connect the offset potentiometer and resistors as shown in Figure 5. Sweep the input through the end point transition voltage, from 111...110 to 111...111. Adjust the offset potentiometer until the actual end point transition voltage occurs at –1/2LSB.

For bipolar offset, connect the offset potentiometer and resistors as shown in Figure 5. Sweep the input through zero and adjust the offset potentiometer until the transition from 0111 1111 111 to 1000 0000 0000 occurs at –1/2LSB.

For gain, connect the gain potentiometer as shown in Figure 6. Sweep the input through the end point transition voltage, which should cause an output transition from 000...000... to 000...001. Adjust the gain potentiometer until this transition occurs at the correct end point transition voltage as given in Table II.

OPTIONAL CLOCK RATE CONTROL

The clock is factory-set for a conversion time between 800ns and 900ns. By use of the optional clock rate control shown in Figure 7, the 12-bit conversion time can be typically adjusted down to 700ns. It can also be used, if desired, to get slightly higher speed or to assure maximum conversion time at elevated temperature. If the clock rate control is not used, Pin 19 should be left open or bypassed with 100pF capacitor. Conversion time versus clock rate control voltage is shown in the Typical Performance Curves.

More positive voltage on clock rate control increases speed of conversion. Voltage of less than 1V may cause the clock to stop.

Analog Input Voltage Range	±10V	±5V	0 to –10V
Code Designation	BOB[1] or BTC[2]	BOB or BTC	CSB[3]
One Least Significant Bit (LSB)	4.88mV	2.44mV	2.44mV
Transition Values MSB LSB[4]			
000...000	–10V + 1/2LSB	–5V + 1/2LSB	–10V + 3/2LSB
000...001			
011...111	–1/2LSB	–1/2LSB	–5V + 1/2LSB
100...000			
111...110	+10V – 3/2LSB	+5V – 3/2LSB	–1/2LSB
111...111			

NOTES: (1) BOB = Bipolar Offset Binary. (2) BTC = Binary Two's Complement (obtained by inverting the most significant bit (pin 1). (3) CSB = Complementary Straight Binary. (4) Voltages given are the nominal value for the transition from the next lower code.

TABLE II. Input Voltages, Transition Values, LSB Values, and Code Definitions.

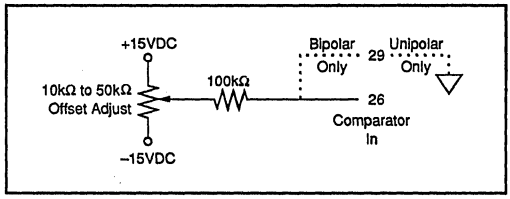


FIGURE 5. Optional Offset Adjust.

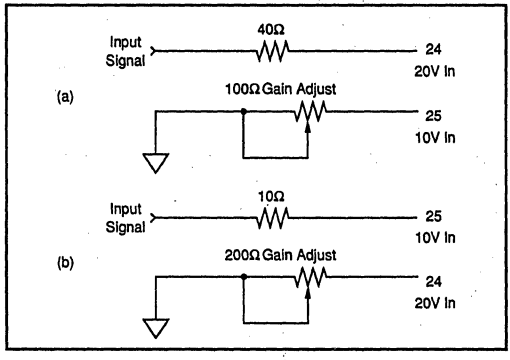


FIGURE 6. Optional Gain Adjust: (a) ±10VBipolar Operation, (b) ±15V Bipolar or 0 to –10V Unipolar Operation

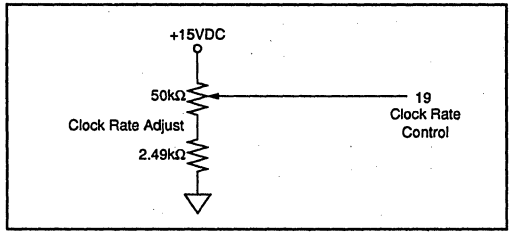


FIGURE 7. Optional Clock Rate Control.

EXTERNAL SHORT CYCLE

The ADC601 may be short-cycled for fewer bits of resolution at faster conversion speeds. The short cycle circuit (Figure 8) works by having the 74LS165 shift register count the clock pulses out of the ADC which correspond to the ADC bit becoming valid. The shift register will output a negative going pulse when the programmed 74LS165 input is shifted to the serial output Q-not. The negative pulse then resets the R-S flip/flop to a low and brings convert comand low, thus stopping the ADC conversion. At the time the ADC stops converting, status goes low which initiates a parallel load to the shift register, thus programming it for the next conversion. The R-S flip/flop made from the 74LS00 nand gates and the other 2 nand gates act as gating for the reset pulse from the shift register. For short-cycling from 9 to 11 bits, cascade two 74LS165s together.

The 74LS165 shift register is programmed on inputs A-G to short cycle the ADC601 on a given bit. For the circuit shown, input A will short cycle the ADC on bit 7, input B on bit 6, etc to input G short cycling on bit 1. All shift register inputs should be tied to GND except the input corresponding to the desired short-cycle bit, which should be tied high. To disable short cycling completely, tie all shift register inputs to ground.

TIMING CONSIDERATIONS

The timing diagram (Figure 9) shows the relationship between the convert command, clock and outputs. The digital output word uses positive logic for bipolar operation and complementary logic for unipolar operation.

The following are some important points to consider on the ADC601 timing. The times given are typical unless otherwise noted. Nominal maximum and minimum times are also given in Figure 9.

1. When power is first applied, the status of the ADC601 will be undetermined. A convert command must be applied to initialize the ADC601.
2. The convert command must be low at least 50ns prior to the rising edge that starts a conversion.
3. The clock runs continuously when the initial convert command goes high and whenever the convert command is high thereafter. It does not run when convert command is low.
4. The clock is started by a rising transition of the convert command.
5. Parallel Output Data: The successive approximation register (SAR) is reset after the leading edge of the first clock period in the conversion cycle. The MSB is set to logic "0" and all other bits are set to logic "1". The bits are determined in succession starting with the MSB, Bit 1, as shown in Figure 9. Each bit will be valid after its corresponding clock pulse.

   In most applications the rising edge of the Convert Command may be used to strobe parallel data out of the ADC601 directly. It is recommended that all outputs are buffered if large capacitive loads are being driven.
6. Status goes high after the rising edge of the first clock pulse and goes low after all 12 bits are valid.
7. Bit 12 will become valid before status goes low; a new conversion may be initiated anytime after the output data has been read.
8. The converter may be restarted during a conversion. If a convert command is held at zero for a minimum of 50ns, the SAR will be reset and a new conversion will start on the next rising transition regardless of the state of the converter prior to the convert commands being received.

Figures 10, 11, and 12 are digital oscilloscope displays of the actual pulse shapes and relationships.

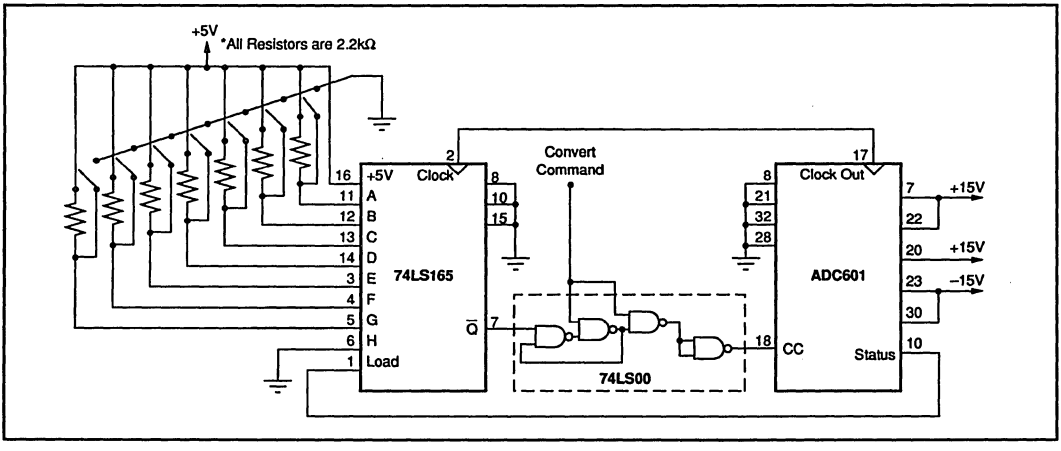
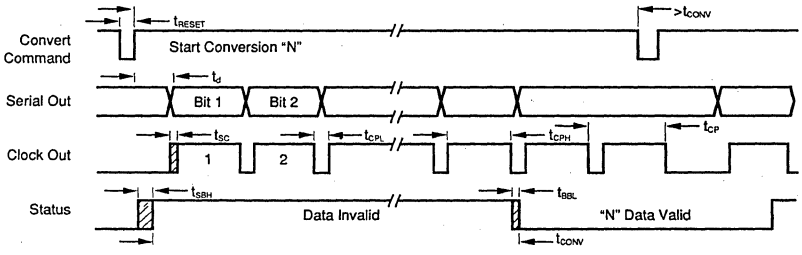


FIGURE 8. External Short Cycle Circuit.



SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS
t_{CP}	Clock Period		100		ns
t_{CPH}	Clock Pulse High		60		ns
t_{CPL}	Clock Pulse Low		40		ns
t_{CONV}	Conversion Time		850	1µs	ns
t_{SC}	Serial to Clock Out Delay	0		5.5	ns
t_{SBH}	Start to Status High Delay			13.0	ns
t_{BBL}	Data Valid to Status Low Delay	0		3.0	ns
t_{RESET}	Convert Command Low	50		400	ns
t_d	CC to First Clock Pulse			24	ns

NOTE: Logic timing limits: T_A = +25°C and +125°C, unless otherwise specified

FIGURE 9. ADC601 Logic Timing Diagram.

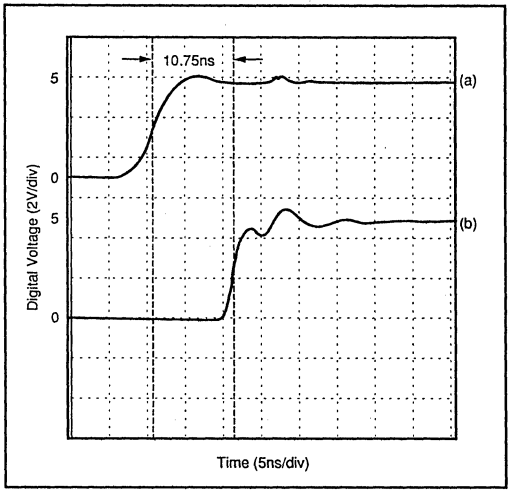
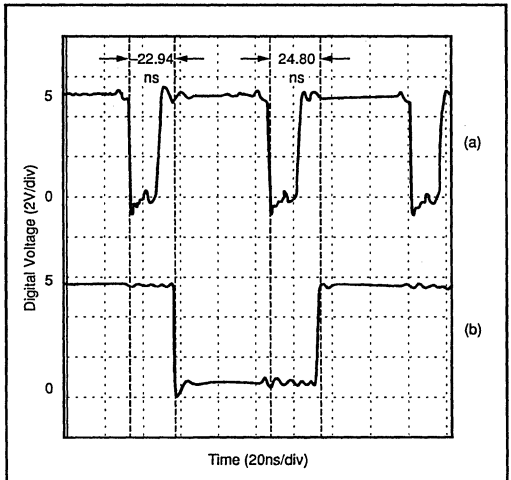


FIGURE 10. (a) Convert Command, (b) Status.



NOTE: The Serial Data Output is Synchronized with the Negative Edge of Each Appropriate Clock Cycle.

FIGURE 11. (a) Clock, (b) Serial Out.

DIGITAL CODES

Parallel Data

Two binary codes are available on the ADC601 parallel output; straight binary (logic "0" true) for unipolar input signal ranges and bipolar offset binary (logic "1" true) for bipolar input signal ranges. Binary two's complement may be obtained for bipolar input ranges by inverting the MSB. It should be noted that for unipolar input ranges –10V is full scale.

Table II shows the LSB, transition values, and code definitions for each possible analog signal range.

Serial Data (NRZ)

ADC601 serial data operation is guaranteed to match the parallel data. If an optoisolator is used to eliminate ground connections, buffer the output with an appropriate TTL line driver. It is recommended that all outputs be buffered if large capacitive loads are being driven.

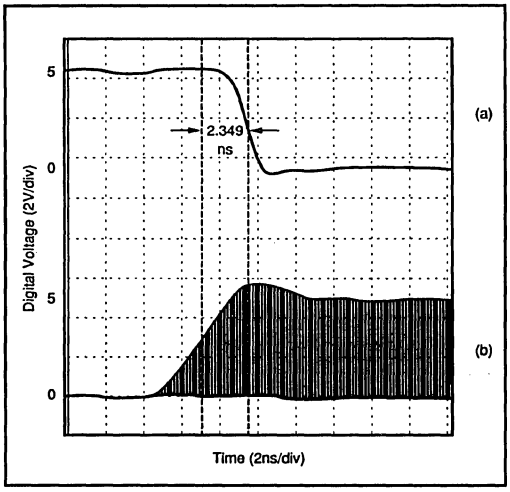


FIGURE 12. (a) Status, (b) Bit-12 Data.

TESTING OF THE ADC601

Careful test fixture design is required to accurately test the ADC601. Proper grounding, correct routing of analog and digital signals and power supply bypassing are crucial in achieving successful results. High-frequency layout techniques and copper ground planes are recommended.

ANALOG-TO-DIGITAL CONVERTER TEST TECHNIQUE

A very effective way of determining the DC performance of an ADC is by using the "servo loop method." A block diagram of this technique is shown in Figure 13. This measurement system automatically locates the analog voltage that causes the digital output to alternate between the desired code and the adjacent code. A computer is programmed to place the desired code on the I/O bus which is one input to the digital comparator. The other input to this comparator is the digital output of the ADC. Depending upon the results of this comparison, the integrator is directed to change its output until an equilibrium state is achieved, in where the comparator and the ADC digital words are equal. Once in equilibrium, the DVM measures the analog input to the ADC and transmits the information to the computer via an IEEE-488 bus. The test program checks all the desired code combinations, verifying the performance of the ADC. Test time will range from 10 seconds to several minutes depending on the speed of the test program, settling time of the DVM, and number of codes to be checked.

DYNAMIC PERFORMANCE TESTING

The ADC601 is a very high performance converter and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a fast Fourier transform (FFT) to the ADC digital output will provide data on all important dynamic performance parameters: total harmonic distortion (THD), signal-to-noise ratio (SNR) or the more severe signal-to-noise-and-distortion ratio (SINAD), and intermodulation Distortion (IMD).

A typical test setup for performing high-speed FFT testing of analog-to-digital converters is shown in Figure 14. Highly accurate phase-locked signal sources allow high resolution FFT measurements to be made without using window functions. By choosing appropriate signal frequences and sample rates, an integral number of signal frequency periods can be sampled. As no spectral leakage results, a "rectangular" window (no window function) can be used. This was used to generate the typical FFT performance curves shown in the Typical Performance Curves.

If generators cannot be phase-locked and set to extreme accuracy, a very low side-lobe window must be applied to the digital data before executing an FFT. A commonly used window such as the Hanning window is not appropriate for testing high performance converters; a minimum four-sample Blackman-Harris window is strongly recommended.[1] To assure that the majority of codes are exercised in the ADC601 (12 bits), a 4096-point FFT is taken. If the data storage RAM is limited, a smaller FFT may be taken if a sufficient number of samples are averaged (ie, a 10-sample average of 512-point FFTs).

IMD two-tone testing shown in Figure 15 is referenced[3] to the larger of the test signals f_1 or f_2. Five "bins" either side of peak are used for calculation of fundamental and harmonic power. The "0" frequency bin (DC) is not included in these calculations as it is of little importance in dynamic signal processing applications.

Dynamic Performance Definitions

1. Signal-to-Noise-and-Distortion[2] Ratio (SINAD):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (first nine harmonics)}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

3. Total Harmonic Distortion (THD):

$$10 \log \frac{\text{Harmonic Power (first nine harmonics)}}{\text{Sinewave Signal Power}}$$

4. Intermodulation Distortion (IMD):

$$10 \log \frac{\text{IMD Product Power (RMS sum; to fifth order)}}{\text{Sinewave Signal Power}}$$

5. Spurious-Free Dynamic Range (SFDR):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Largest Power Product}}$$

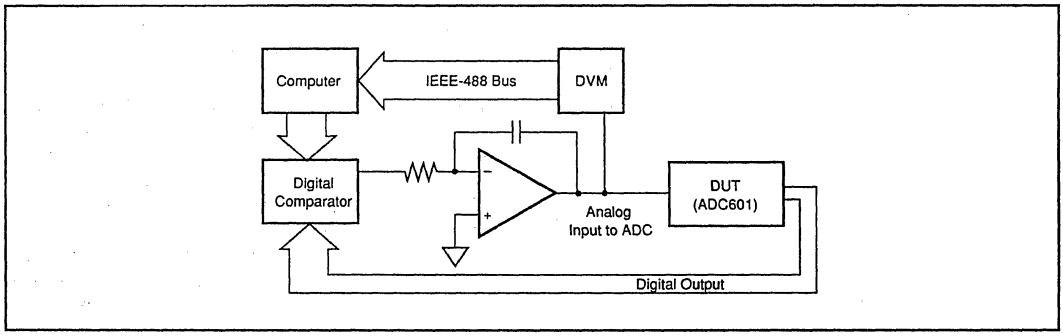


FIGURE 13. Servo Loop Analog-to-Digital Tester.

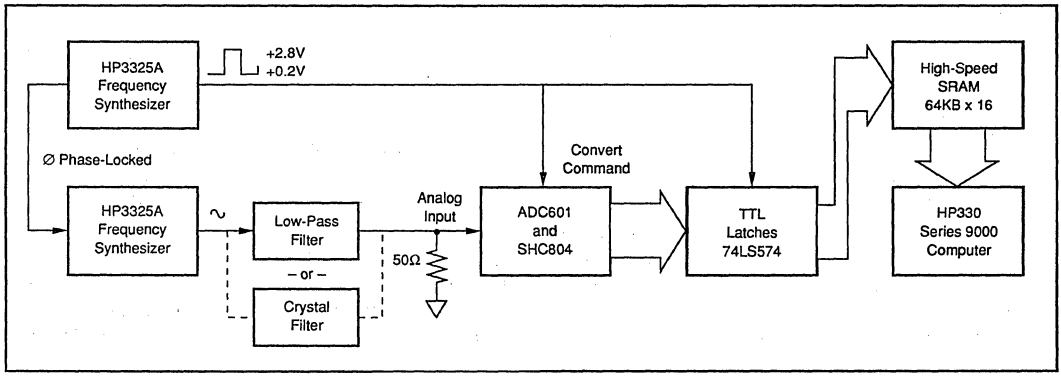


FIGURE 14. Block Diagram of FFT Test for THD, SNR, and SINAD.

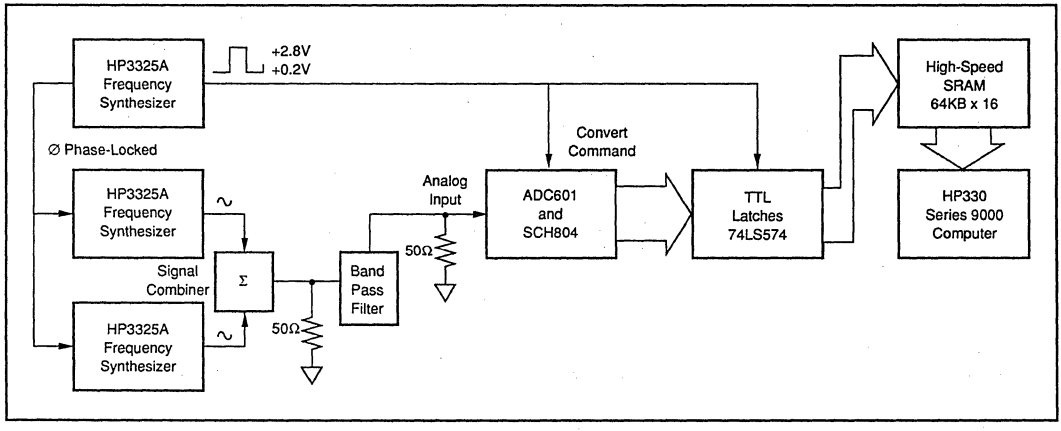


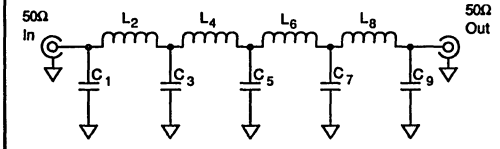
FIGURE 15. Block Diagram of FFT Test for Two-Tone IMD.

MAJOR POINTS TO CONSIDER

Attention to test set up details can prevent errors that contribute to poor test results. Important points to remember when testing high performance converters are:

1. The ADC analog input must not be overdriven. Using a signal amplitude slightly lower than FSR will allow a small amount of "headroom" so that noise or DC offset voltage will not overrange the ADC and "hard limit" on signal peaks. Overrange peaks will, however, just result in a constant full-scale digital output.
2. Two-tone tests can produce signal envelopes that exceed FSR. Set each test signal to slightly less than –6dB to prevent "hard limiting" on peaks.

3. Low-pass filtering (or bandpass filtering) of test signal generators is absolutely necessary for THD and IMD tests. An easily built LC low-pass filter (Figure 16) will eliminate harmonics from the test signal generator.
4. Test signal generators must have exceptional noise performance (better than –155dBc/Hz) to achieve accurate SNR measurements. Good generators together with fifth-order elliptical bandpass filters are recommended for SNR tests. Narrow bandwidth crystal filters can also be used to filter generator broadband noise but they should be carefully tested for operation at high levels.
5. The analog input of the ADC601 should be driven by a low output impedance S/H amplifier such as a SHC804. Short leads are necessary to prevent digital noise pickup.
6. A low-noise (jitter) clock signal (convert command) generator is required for good ADC dynamic performance. A poor generator can seriously impair good SNR performance. Short leads are necessary to preserve fast TTL rise times.
7. Two-tone testing will require isolation between test signal generators to prevent IMD generation in the test generator output circuits. An active summing amplifier using an OPA600 is shown in Figure 18. This circuit will provide excellent performance from DC to 5MHz with harmonic and intermodulation distortion products typically better than –70dBc. A passive (hybrid transformer) signal combiner can also be used (Figure 17) over a range of about 0.1MHz to 30MHz. This combiner's port-to-port isolation will be ≈45dB between signal generators and its input-output insertion loss will be ≈6dB. Distortion will be better than –85dBc for the powdered-iron core specified. Avoid ferrites. The circuits shown in Figures 17 and 18, have bandwidths beyond those required for the ADC601; therefore, they have even better performance at 500kHz. These combiners are always good additions to high-speed engineering labs.
8. A very low side-lobe window must be used for FFT calculations if generators cannot be phase-locked and set to exact frequencies. A minimum four-sample Blackman-Harris window function is recommended.(1)
9. Digital data may be latched into an external TTL 12-bit register by the status falling edge before the next convert command level. Latches should be mounted on PC boards in very close proximity to the ADC601. Avoid long leads.
10. Do not overload the data output logic. These outputs are designed to drive two TTL loads.
11. A well-designed, clean PC board layout will assure proper operation and clean spectral response. Proper grounding and bypassing, short lead lengths and separation of analog and digital signals and ground returns are particularly important for high frequency circuits. Multilayer PC boards are recommended for best performance, but a two-sided PC board with large, heavy (2oz-foil) ground planes can give excellent results, if carefully designed.
12. Prototyping "plug-boards" or wire-wrap boards will not be satisfactory. Request layout application notes from Burr-Brown.



9th Order 0.5dB Ripple
Tchebychev Low-Pass Filter

Attenuation at 2X cutoff frequency = 90dB.

Cutoff frequency = –3dB frequency; to convert cutoff frequency to –0.5dB frequency, multiply all LC values by 0.98997.

Cutoff Freq. (MHz)	C_1 (pF)	C_3 (pF)	C_5 (pF)	C_7 (pF)	C_9 (pF)	L_7 (H)	L_8 (H)	L_9 (H)	L_9 (H)
5.0	1134.6	1729.2	1765.6	1729.2	1134.6	2.056	2.216	2.216	2.056
2.5	2269	3458	3531	3458	2269	4.11	4.43	4.43	4.11
1.25	4538	6917	7062	6917	4538	8.23	8.86	8.86	8.23
0.625	9077	13,833	14,125	13,833	9077	16.45	17.73	17.73	16.45
0.50	11,346	17,292	17,656	17,292	11,346	20.56	22.16	22.16	20.56

FIGURE 16. Ninth-Order Harmonic Filter.

NOTES:

1. "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform," Fredric J. Harris. *Proceedings of the IEEE*, Vol. 66, No. 1, January 1978, pp 51-83.
2. SINAD test includes harmonics whereas SNR does not include these important spurious products.
3. If IMD is referenced to peak envelope power, distortion will be of 6dB better.

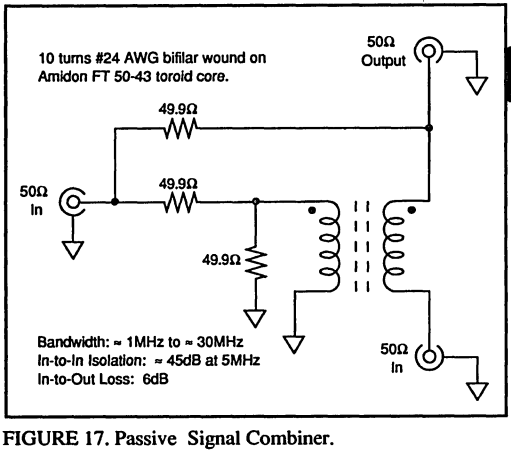


FIGURE 17. Passive Signal Combiner.

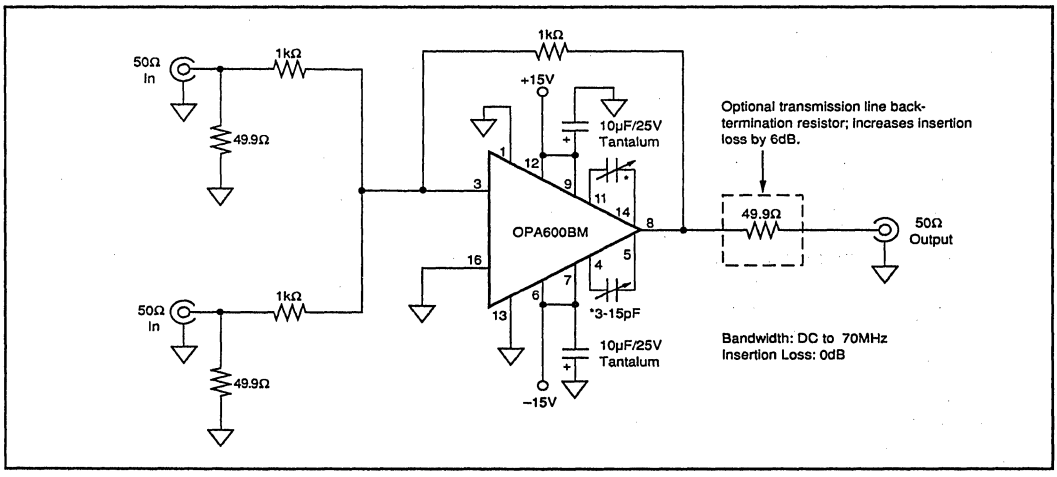


FIGURE 18. Active Signal Combiner.

BURR-BROWN®

ADC603

12-Bit 10MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- HIGH SPURIOUS-FREE DYNAMIC RANGE
- SAMPLE RATE: DC to 10MHz
- HIGH SIGNAL/NOISE RATIO: 68.2dB
- HIGH SINAD RATIO: 66dB
- LOW HARMONIC DISTORTION: –69.6dBc
- LOW INTERMOD. DISTORTION: –77.7dBc
- COMPLETE SUBSYSTEM: Contains Sample/Hold and Reference
- 46-PIN DIP PACKAGE
- 0°C TO +70°C AND –55°C TO +125°C

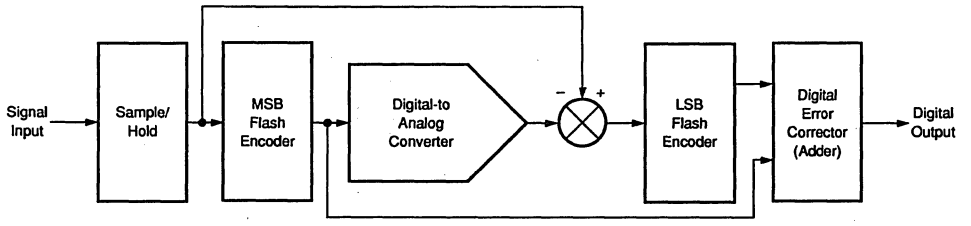
APPLICATIONS

- DIGITAL SIGNAL PROCESSING
- RADAR SIGNAL ANALYSIS
- TRANSIENT SIGNAL RECORDING
- FFT SPECTRUM ANALYSIS
- HIGH-SPEED DATA ACQUISITION
- IR IMAGING SYSTEMS
- DIGITAL RECEIVERS
- SIGINT, ECM, AND EW SYSTEMS
- DIGITAL OSCILLOSCOPES

DESCRIPTION

The ADC603 is an high performance analog-to-digital converter capable of digitizing signals at any rate from DC to 10 megasamples per second. Outstanding spurious-free dynamic range has been achieved by minimizing noise and distortion. Complete static and dynamic test results are furnished with each KH and SH grade unit at no additional cost.

The ADC603 is a two-step subranging ADC subsystem containing an ADC, sample/hold amplifier, voltage reference, timing, and error-correction circuitry in a 46-pin hybrid DIP package. Logic is TTL. Two temperature ranges are available: 0°C to +70°C (JH, KH) and –55°C to +125°C (RH, SH).



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-865B

SPECIFICATIONS

ELECTRICAL

T_C = +25°C, 10MHz sampling rate, R_S = 50Ω, $\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = –5.2V, and 15-minute warmup in convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	ADC603JH MIN	ADC603JH TYP	ADC603JH MAX	ADC603KH MIN	ADC603KH TYP	ADC603KH MAX	UNITS
RESOLUTION				12			12	Bits
INPUTS								
ANALOG								
Input Range	Full Scale	–1.25		+1.25	*		*	V
Input Impedance			1.5			*		MΩ
Input Capacitance			5			*		pF
DIGITAL								
Logic Family				TTL Compatible				
Convert Command	Start Conversion			Positive Edge				
Pulse Width	t = Conversion Period	10		t – 20	*		*	ns
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error	f = 200Hz		±0.2	1		±0.1	0.8	%FSR[1]
Input Offset	DC		±0.2	0.75		*	0.5	%FSR
Integral Linearity Error	f = 200Hz		0.75			0.5	1	LSB
Differential Linearity Error	f = 200Hz: 68.3% of all Codes		0.3			0.25	0.5	LSB
	99.7% of all Codes		0.4			0.3	0.65	LSB
	100% of all Codes		0.5	1		0.4	0.75	LSB
No Missing Codes			Guaranteed			Guaranteed		
Power Supply Rejection	$\Delta +V_{CC}$ = ±10%		±0.03			*	±0.07	%FSR/%
	$\Delta -V_{CC}$ = ±10%		±0.04			*	±0.07	%FSR/%
	$\Delta +V_{DD1}$ = ±10%		±0.004			*	±0.03	%FSR/%
	$\Delta -V_{DD2}$ = ±10%		±0.01			*	±0.03	%FSR/%
CONVERSION CHARACTERISTICS								
Sample Rate		DC		10M	DC		10M	Samples/s
Pipeline Delay	Logic Selectable		1, 2 or 3 Convert Command Periods					
DYNAMIC CHARACTERISTICS								
Differential Linearity Error	f = 4.9MHz: 68.3% of all Codes		0.3			*		LSB
	99.7% of all Codes		0.75			0.5		LSB
	100% of all Codes		1	1.25		0.6	0.9	LSB
Spurious Free Dynamic Range								
f = 5MHz (–0.5dB)	f_S = 9.99MHz		–72	–63		–74	–66	dB
Total Harmonic Distortion[2](THD)								
f = 5MHz (–0.5dB)	f_S = 9.99MHz		–68	–61		–69.6	–64	dBc[3]
f = 100kHz			–70	–65		–72.1	–68	dBc
Two-Tone Intermodulation Distortion[2][4]								
f = 2.2MHz (–6.5dB)	f_S = 8.006MHz		–75	–67		–77.7	–71	dBc
f = 2.5MHz (–6.5dB)								
Signal-to-Noise and Distortion (SINAD) Ratio								
f = 5MHz (–0.5dB)	f_S = 9.99MHz	60	65		62	66		dB
f = 100kHz (–0.5dB)		64	67		66	68.5		dB
Signal-to-Noise Ratio (SNR)								
f = 5MHz (–0.5dB)	f_S = 9.99MHz	63	67		66	68.2		dB
f = 100kHz (–0.5dB)		66	68		69	70.1		dB
Aperture Delay Time			–5			*	+9	ns
Aperture Jitter			9			*	20	ps rms
Analog Input Bandwidth (–3dB)								
Small Signal	–20dB Input		70		50	*		MHz
Full Power	0dB Input		40		30	*		MHz
Overload Recovery Time	2x Full-Scale Input		80			*	140	ns
OUTPUTS								
Logic Family				TTL Compatible				
Logic Coding	Logic Selectable		Two's Complement or Inverted Two's Complement					
Logic Levels	Logic LO, I_{OL} = –3.2mA	0	+0.3	+0.8	0	+0.3	+0.5	V
	Logic HI, I_{OH} = 160µA	+2.4	+3.5	+5	+2.4	+3.5	+5	V
EOC Delay Time	Data Out to DV	5	35		5	35		ns
Tri-State Enable/Disable Time	I_{OL} = –6.4mA, 50% In to 50% Out		37	100		37	100	ns
Data Valid Pulse Width		20	45	60	20	45	60	ns
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	+14.25	+15	+15.75	V
$-V_{CC}$		–14.25	–15	–15.75	–14.25	–15	–15.75	V
$+V_{DD1}$		+4.75	+5	+5.25	+4.75	+5	+5.25	V
$-V_{DD2}$		–4.95	–5.2	–5.46	–4.95	–5.2	–5.46	V
Supply Currents: $+I_{CC}$	Operating		+60			+60	+80	mA
$-I_{CC}$			–60			–60	–80	mA
$+I_{DD1}$			+280			+280	+330	mA
$-I_{DD2}$			–565			–565	–630	mA
Power Consumption	Operating		6.1			6.1		W

SPECIFICATIONS

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

$\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = –5.2V, R_S = 50Ω, 15-minute warmup, and $T_C = T_{MIN}$ to T_{MAX}, unless otherwise noted.

PARAMETER	CONDITIONS	ADC603JH MIN	ADC603JH TYP	ADC603JH MAX	ADC603KH MIN	ADC603KH TYP	ADC603KH MAX	UNITS
TEMPERATURE RANGE								
Specification	T_{CASE}	0		+70	*		*	°C
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error	f = 200Hz		±0.4	1.5		*	1	%FSR
Input Offset	DC		±0.4	1		*	0.5	%FSR
Integral Linear Error	f = 200Hz		0.75			0.6	1.25	LSB
Differential Linearity Error	f = 200Hz: 68.3% of all Codes		0.4			0.3	0.6	LSB
	99.7% of all Codes		0.5			0.4	0.75	LSB
	100% of all Codes		0.75			0.6	1	LSB
No Missing Codes			Guaranteed			Guaranteed		
Power Supply Rejection	$\Delta +V_{CC}$ = ±10%		±0.04			*	±0.08	%FSR/%
	$\Delta -V_{CC}$ = ±10%		±0.05			*	±0.08	%FSR/%
	$\Delta +V_{DD1}$ = ±10%		±0.004			*	±0.05	%FSR/%
	$\Delta -V_{DD2}$ = ±10%		±0.02			*	±0.05	%FSR/%
CONVERSION CHARACTERISTICS								
Sample Rate		DC		10M	DC		10M	Samples/s
DYNAMIC CHARACTERISTICS								
Differential Linearity Error	f = 4.9MHz: 68.3% of all Codes		0.5			0.4		LSB
	99.7% of all Codes		1			0.6		LSB
	100% of all Codes		1.25	1.5		0.7	1	LSB
Spurious Free Dynamic Range[5]	f = 5MHz (–0.5dB)		–65	–60		–72	–65	dB
Total Harmonic Distortion[2]								
f = 5MHz (–0.5dB)	f_S = 9.99MHz		–67	–58		–68.8	–62	dBc
f = 100kHz			–69	–62		–69.5	–67	dBc
Two-Tone Intermodulation Distortion								
f = 2.2MHz (–6.5dB)	f_S = 8.006MHz		–72	–64		–74.4	–68	dBc
f = 2.5MHz (–6.5dB)								
Signal-to-Noise and Distortion								
(SINAD) Ratio								
f = 5MHz (–0.5dB)	f_S = 9.99MHz	57	65		61	65.4		dB
f = 100kHz (–0.5dB)		62	66		64	66.5		dB
Signal-to-Noise Ratio (SNR)								
f = 5MHz (–0.5dB)	f_S = 9.99MHz	60	67		64	68		dB
f = 100kHz (–0.5dB)		64	68		68	69.5		dB
Aperture Delay Time			–6			*	+10	ns
Aperture Jitter			10			*	20	ps rms
Analog Input Bandwidth (–3dB)								
Small Signal	–20dB Input		70		50	*		MHz
Full Power	0dB Input		40		30	*		MHz
Overload Recovery Time	2x Full-Scale Input		80			*		ns
OUTPUTS								
Logic Levels	Logic LO, I_{OL} = –3.2mA	0	+0.3	+0.8	*	*	+0.5	V
	Logic HI, I_{OH} = 160µA	+2.4	+3.5	+5	*	*	*	V
EOC Delay Time	Data Out to DV	5	35		*	*		ns
Tri-State Enable/Disable Time	I_{OL} = –6.4mA, 50% In to 50% Out		42	100		*	*	ns
Data Valid Pulse Width		20	45	60	*	*	*	ns
POWER SUPPLY REQUIREMENTS								
Supply Currents: $+I_{CC}$	Operating		+65			*	+80	mA
$-I_{CC}$			–61			*	–80	mA
$+I_{DD1}$ [6]			+285			*	+333	mA
$-I_{DD2}$ [7]			–570			*	–630	mA
Power Consumption	Operating		6.1			*		W

* Same specifications as ADC603JH/RH.

NOTES: (1) FSR: Full-Scale Range = 2.5Vp-p. (2) Units with tested and guaranteed distortion specifications are available on special order—Inquire. (3) dBC = level referred to carrier-input signal = 0dB); F = input frequency; F_S = sampling frequency. (4) IMD is referred to the larger of the two input test signals. If referred to the peak envelope signal (=0dB), the intermodulation products will be 6dB lower. (5) SFDR tested at temperature for K grade only. (6) Pins 3 and 30 (analog) typically draw 80% of the total +5V current. Pin 21 (digital) typically draws 20%. (7) Pin 6 (analog) typically draws 45% of the total –5.2V current. Pin 31 (digital) typically draws 55%.

SPECIFICATIONS

ELECTRICAL

T_C = +25°C, 10MHz sampling rate, R_S = 50Ω, $\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = –5.2V, and 15-minute warmup in convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	ADC603RH MIN	ADC603RH TYP	ADC603RH MAX	ADC603SH MIN	ADC603SH TYP	ADC603SH MAX	UNITS
RESOLUTION				12			12	Bits
INPUTS								
ANALOG								
Input Range	Full scale	–1.25		+1.25	*		*	V
Input Impedance			1.5			*		MΩ
Input Capacitance			5			*		pF
DIGITAL								
Logic Family			TTL Compatible					
Convert Command	Start Conversion		Positive Edge					
Pulse Width	t = Conversion Period	10		t – 20	*		*	ns
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error	f = 200Hz		±0.2	±2		±0.1	±1	%FSR[1]
Input Offset	DC		±0.2	±2		*	±0.75	%FSR
Integral Linearity Error	f = 200Hz		0.75			0.5	1	LSB
Differential Linearity Error	f = 200Hz:68.3% of all codes		0.3			0.25	0.5	LSB
	99.7% of all codes		0.4			0.3	0.65	LSB
	100% of all codes		0.5			0.4	0.75	LSB
No Missing Codes			Guaranteed			Guaranteed		
Power Supply Rejection	$\Delta +V_{CC}$ = ±10%		±0.03			*	±0.125	%FSR/%
	$\Delta -V_{CC}$ = ±10%		±0.04			*	±0.125	%FSR/%
	$\Delta +V_{DD1}$ = ±10%		±0.004			*	±0.03	%FSR/%
	$\Delta -V_{DD2}$ = ±10%		±0.01			*	±0.03	%FSR/%
CONVERSION CHARACTERISTICS								
Sample Rate		DC		10M	DC		10M	Samples/s
Pipeline Delay	Logic Selectable		1, 2 or 3 Convert Command Periods					
DYNAMIC CHARACTERISTICS								
Differential Linearity Error	f = 4.9MHz: 68.3% of all codes		0.3			*	0.5	LSB
	99.7% of all codes		0.75			0.5	1	LSB
	100% of all codes		1			0.6	1.25	LSB
Total Harmonic Distortion[2](THD)								
f = 5MHz (–0.5dB)	f_S = 9.99MHz		–68			–69.6	–64	dBc[3]
f = 100kHz			–70			–72.1	–66	dBc
Two-Tone Intermodulation Distortion[2](IMD)								
f = 2.2MHz (–6.5dB)	f_S = 8.006MHz		–75			–77.7	–71	dBc
f = 2.5MHz (–6.5dB)								
Signal-to-Noise and Distortion (SINAD) Ratio								
f = 5MHz (–0.5dB)	f_S = 9.99MHz		65		62	66		dB
f = 100kHz (–0.5dB)			67		64	68.5		dB
Signal-to-Noise Ratio (SNR)								
f = 5MHz (–0.5dB)	f_S = 9.99MHz		67		64	68.2		dB
f = 100kHz (–0.5dB)			68		66	70.1		dB
Aperture Delay Time			–5			*	+9	ns
Aperture Jitter			9			*	20	ps rms
Analog Input Bandwidth (–3dB)								
Small Signal	–20dB input		70		50	*		MHz
Full Power	0dB input		40		30	*		MHz
Overload Recovery Time	2x Full-Scale input		80			*	140	ns
OUTPUTS								
Logic Family			TTL Compatible					
Logic Coding	Logic Selectable		Two's Complement or Inverted Two's Complement					
Logic Levels	Logic LO, I_{OL} = –3.2mA	0	+0.3	+0.8	0	+0.3	+0.5	V
	Logic HI, I_{OH} = 160µA	+2.4	+3.5	+5	+2.4	+3.5	+5	V
EOC Delay Time	Data Out to DV	5	35		5	35		ns
Tri-State Enable/Disable Time	I_{OL} = –6.4mA, 50% In to 50% Out		37	100		37	100	ns
Data Valid Pulse Width		20	45	60	20	45	60	ns
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	+14.25	+15	+15.75	V
$-V_{CC}$		–14.25	–15	–15.75	–14.25	–15	–15.75	V
$+V_{DD1}$		+4.75	+5	+5.25	+4.75	+5	+5.25	V
$-V_{DD2}$		–4.95	–5.2	–5.46	–4.95	–5.2	–5.46	V
Supply Currents: $+I_{CC}$	Operating		+60			+60	+80	mA
$-I_{CC}$			–60			–60	–80	mA
$+I_{DD1}$			+280			+280	+330	mA
$-I_{DD2}$			–565			–565	–630	mA
Power Consumption	Operating		6.1			6.1		W

* Same specifications as ADC603JH/RH

SPECIFICATIONS

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

$\pm V_{CC} = \pm 15V$, $+V_{DD1} = +5V$, $-V_{DD2} = -5.2V$, $R_S = 50\Omega$, 15-minute warmup, and $T_C = T_{MIN}$ to T_{MAX}, unless otherwise noted.

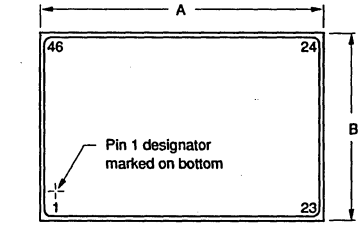
PARAMETER	CONDITIONS	ADC603RH MIN	ADC603RH TYP	ADC603RH MAX	ADC603SH MIN	ADC603SH TYP	ADC603SH MAX	UNITS
TEMPERATURE RANGE								
Specification	T_{CASE}	–55		+125	*		*	°C
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error	f = 200Hz		±0.4	±2		*	±1.5	%FSR
Input Offset	DC		±0.4	±2		*	±1	%FSR
Integral Linear Error	f = 200Hz		0.75			0.6	1.25	LSB
Differential Linearity Error	f = 200Hz: 68.3% of all codes		0.4			0.3	0.6	LSB
	99.7% of all codes		0.5			0.4	0.75	LSB
	100% of all codes		0.75			0.6	1	LSB
No Missing Codes			Guaranteed			Guaranteed		
Power Supply Rejection	$\Delta +V_{CC} = \pm 10\%$		±0.04			*	±0.08	%FSR/%
	$\Delta -V_{CC} = \pm 10\%$		±0.05			*	±0.08	%FSR/%
	$\Delta +V_{DD1} = \pm 10\%$		±0.004			*	±0.05	%FSR/%
	$\Delta -V_{DD2} = \pm 10\%$		±0.02			*	±0.05	%FSR/%
CONVERSION CHARACTERISTICS								
Sample Rate		DC		10M	DC		10M	Samples/s
DYNAMIC CHARACTERISTICS								
Differential Linearity Error	f = 4.9MHz: 68.3% of all codes		0.5			0.4	0.75	LSB
	99.7% of all codes		1			0.6	1.25	LSB
	100% of all codes		1.25			0.7	1.5	LSB
Total Harmonic Distortion[2]								
f = 5MHz (–0.5dB)	f_S = 9.99MHz		–67			–68.8	–62	dBc
f = 100kHz			–69			–69.5	–64	dBc
Two-Tone Intermodulation Distortion								
f = 2.2MHz (–6.5dB)	f_S = 8.006MHz		–72			–74.4	–68	dBc
f = 2.5MHz (–6.5dB)								
Signal-to-Noise and Distortion (SINAD) Ratio								
f = 5MHz (–0.5dB)	f_S = 9.99MHz		65		60	65.4		dB
f = 100kHz (–0.5dB)			66		62	66.5		dB
Signal-to-Noise Ratio (SNR)								
f = 5MHz (–0.5dB)	f_S = 9.99MHz		67		62	68		dB
f = 100kHz (–0.5dB)			68		64	69.5		dB
Aperture Delay Time			8			*	+10	ns
Aperture Jitter			10			*	20	ps rms
Analog Input Bandwidth (–3dB)								
Small Signal	–20dB Input		70		50	*		MHz
Full Power	0dB Input		40		30	*		MHz
Overload Recovery Time	2x Full-Scale Input		80			*		ns
OUTPUTS								
Logic Levels	Logic LO, I_{OL} = –3.2mA	0	+0.3	+0.8	*	*	+0.5	V
	Logic HI, I_{OH} = 160µA	+2.4	+3.5	+5	*	*	*	V
EOC Delay Time	Data Out to DV	5	35		*	*		ns
Tri-State Enable/Disable Time	I_{OL} = –6.4mA, 50% In to 50% Out		42	100		*	*	ns
Data Valid Pulse Width		20	45	60	*	*	*	ns
POWER SUPPLY REQUIREMENTS								
Supply Currents: $+I_{CC}$	Operating		+65			*	+80	mA
$-I_{CC}$			–61			*	–80	mA
$+I_{DD1}$			+285			*	+333	mA
$-I_{DD2}$			–570			*	–630	mA
Power Consumption	Operating		6.1			*		W

* Same specifications as ADC603JH/RH

NOTES: (1) FSR: Full-Scale Range = 2.5Vp-p. (2) Units with tested and guaranteed distortion specifications are available on special order—inquire. (3) dBC = level referred to carrier-input signal = 0dB); F = input frequency; F_S = sampling frequency. (4) IMD is referred to the larger of the two input test signals. If referred to the peak envelope signal (=0dB), the intermodulation products will be 6dB lower.

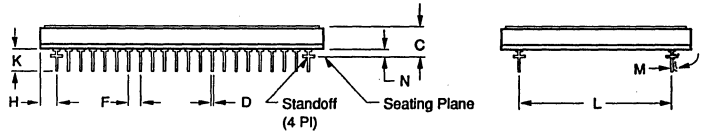
MECHANICAL

H Package — Metal and Ceramic



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	2.370	2.420	60.20	61.47
B	1.560	1.610	39.62	40.89
C	.200	.260	5.08	6.60
D	.018 Dia BASIC		0.46 Dia BASIC	
F	.100 BASIC		2.54 BASIC	
H	0.75	.115	1.91	2.92
K	.150	.190	3.81	4.83
L	1.300 BASIC		33.02 BASIC	
M	—	10°	—	10°
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.



PIN ASSIGNMENTS

1	Common (Case)	46	Common (Analog)
2	NC	45	Analog Signal In
3	$+V_{DD1}$ (+5V) Analog	44	$+V_{CC}$ (+15V) Analog
4	S/H Out	43	$-V_{CC}$ (–15V) Analog
5	A/D In	42	NC
6	$-V_{DD2}$ (–5.2V) Analog	41	NC
7	NC	40	NC
8	NC	39	DNC
9	Bit 1(MSB)	38	DNC
10	Bit 2	37	Gain Adjust
11	Bit 3	36	Offset Adjust
12	Bit 4	35	Common (Analog)
13	Bit 5	34	$+V_{CC}$ (+15V) Analog
14	Bit 6	33	$-V_{CC}$ (–15V) Analog
15	Bit 7	32	Common (Analog)
16	Bit 8	31	$-V_{DD2}$ (–5.2V) Digital
17	Bit 9	30	$+V_{DD1}$ (+5V) Analog
18	Bit 10	29	1 Pipeline Delay Select
19	Bit 11	28	0 Pipeline Delay Select
20	Bit 12 (LSB)	27	Output Logic Invert
21	$+V_{DD1}$ (+5V) Digital	26	Common (Digital)
22	Data Valid Output	25	Tri-State $\overline{\text{ENABLE}}$
23	Common (Digital)	24	Convert Command In

ORDERING INFORMATION

ADC603 ( ) H

Basic Model Number

Performance Grade Code
- J, K: 0°C to +70°C Case Temperature
- R, S: –55°C to +125°C Case Temperature

Package Code
- H: Metal and Ceramic

ABSOLUTE MAXIMUM RATINGS

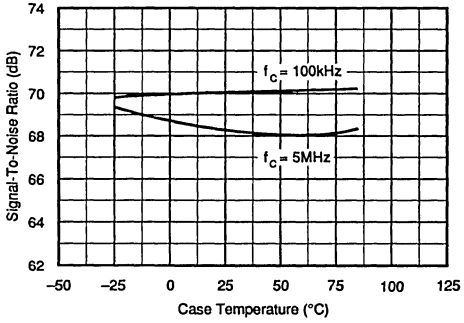
$\pm V_{CC}$	±16.5V
$+V_{DD1}$	+7V
$\pm V_{DD2}$	–7V
Analog Input	±5V
Logic Input	–0.5V to $+V_{DD1}$
Case Temperature	+125°C
Junction Temperature	+165°C
Storage Temperature	–65°C to +165°C

Stresses above these ratings may permanently damage the device.

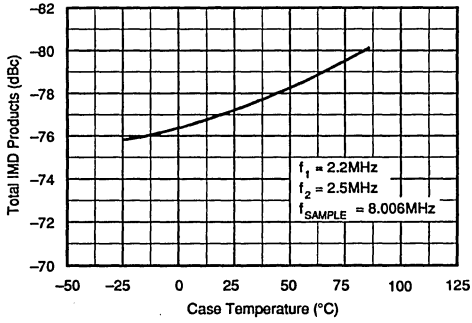
TYPICAL PERFORMANCE CURVES

$\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = –5.2V, R_S = 50Ω, 15-minute warmup, and T_C = +25°C, unless otherwise noted. All plots are 4096 point FFTs.

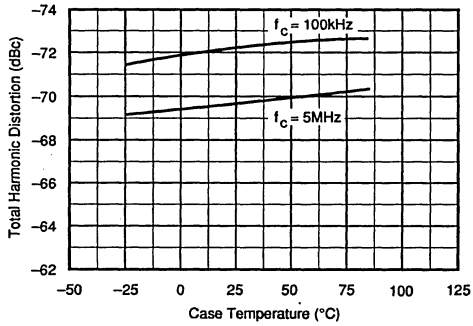
SIGNAL-TO-NOISE RATIO vs TEMPERATURE



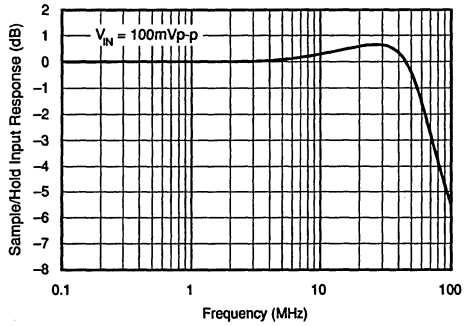
TWO-TONE IMD vs TEMPERATURE



TOTAL HARMONIC DISTORTION vs TEMPERATURE



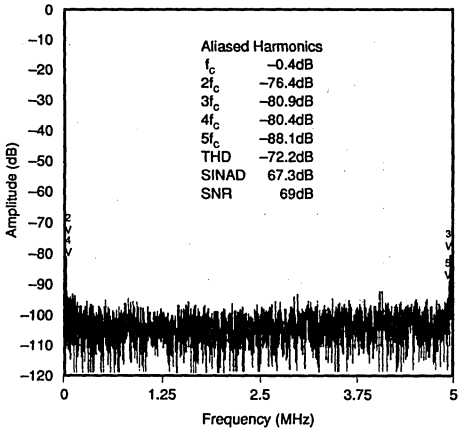
ANALOG INPUT BANDWIDTH



TYPICAL PERFORMANCE CURVES

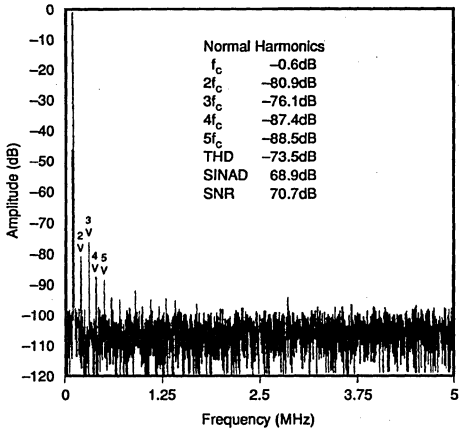
$\pm V_{CC} = \pm 15V$, $+V_{DD1} = +5V$, $-V_{DD2} = -5.2V$, $R_S = 50\Omega$, 10MHz sample rate, 15-minute warmup, and $T_C = +25°C$, unless otherwise noted. All plots are 4096-point FFTs.

5MHz HARMONIC DISTORTION



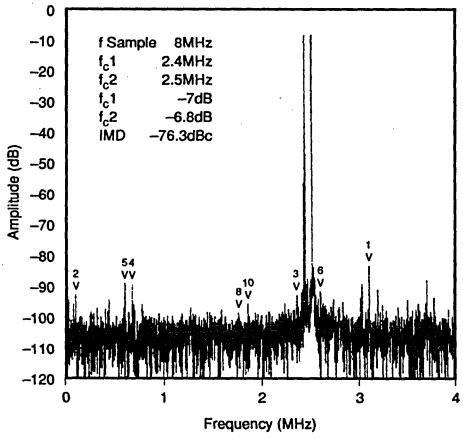
NOTE: Sample rate = 9.99 MHz; even harmonics folded to left edge and odd harmonics folded to right edge. Any non-harmonically related spurious products show clearly in the center.

100kHz HARMONIC DISTORTION



NOTE: Sample rate = 9.99 MHz; harmonics appear in normal order.

TWO-TONE INTERMODULATION DISTORTION



NOTE: Sample rate = 8MHz; highest IMD product is cursor number 1: f1 +f2. The second-order –76.3dBc product determines the wideband spurious-free dynamic range of this example. For RF applications third-order IMD products such as those at cursors 3 and 6 are the limiting spurs. Under these conditions spurious-free dynamic range is limited by 2f2+ f1 to 84.3dBc.

Sample rates of 10MHz show similar results.

TWO-TONE INTERMODULATION DISTORTION PRODUCTS

CURSOR	IMD	FREQUENCY	dB
1	2nd order : f1 + f2	3.086395621579MHz	–83.1
2	2nd order : f2 – f1	0.080140734949MHz	–91.4
3	3rd order : 2f1 – f2	2.339718530102MHz	–92.4
4	3rd order : 2f1 + f2	0.666536356529MHz	–88.4
5	3rd order : 2f2 – f1	0.586395621579MHz	–88.2
6	3rd order : 2f2 + f1	2.580140734949MHz	–91.1
7	4th order : 3f1 – f2	3.246677091478MHz	–109
8	4th order : 3f1 + f2	1.753322908522MHz	–100
9	4th order : 2f2 – 2f1	0.130281469898MHz	–114.8
10	4th order : 2f2 + 2f1	1.833463643471MHz	–95
11	4th order : 3f2 – f1	2.926114151681MHz	–115.4
12	4th order : 3f2 + f1	1.913604378421MHz	–98.2

NOTE: IMD products in this table are refered to full-scale (0dB). To refer IMD to carrier, subtract the larger of f_c1 or f_c2. In this example, IMD referred to carrier will be 6.8dB higher (worse) than the full-scale value shown.

THEORY OF OPERATION

The ADC603 is a two-step subranging analog-to-digital converter. This architecture is shown in Figure 1. The major system building blocks are: sample/hold amplifier, MSB flash encoder, DAC and error amplifier, LSB flash encoder, digital error corrector, and timing circuits. The ADC603 uses hybrid technology with laser-trimmed integrated circuits mounted in a multilayer ceramic package to integrate this complex circuit into a complete analog-to-digital converter subsystem with state-of-the-art performance.

Conceptually, the subranging technique is simple: sample and hold the input signal, convert to digital with a coarse ADC, convert back to analog with a coarse-resolution (but high-accuracy) DAC, subtract this voltage from the S/H output, amplify this "remainder," convert to digital with a second coarse ADC, and combine the digital output from the first ADC (MSB) with the digital output from the second ADC (LSB). In practice, however, achieving high conversion speed without sacrificing accuracy is a difficult task.

The analog input signal is sampled by a high-speed sample/hold amplifier with low distortion, fast acquisition time and very low aperture uncertainty (jitter). A diode bridge sampling switch is used to achieve an acceptable compromise between speed and accuracy. The diode bridge switching transients are buffered from the analog input by a high input impedance buffer amplifier. Since the hold capacitor does not appear in the feedback of the diode bridge output buffer, the capacitor can acquire the signal in 25ns. The low-bias-current output buffer is then required to settle to only the resolution (7 bits) of the first (MSB) flash encoder in 25ns, while an additional 60ns is allowed for settling to the resolution (12 bits) of the second (LSB) flash encoder. Sample/hold droop appears as only an offset error and does not effect linearity.

Both the MSB and the LSB flash encoder (ADC) function are performed by multiplexing one high-speed 7-bit resolution converter formed by parallel-connecting two 6-bit flash ADCs. The DAC voltage reference is also used to generate reference voltages for the MSB and LSB encoder to compensate drift errors. Buffering and scaling amplifiers are laser-trimmed to minimize voltage offset errors and optimize gain (input full-scale range) symmetry.

The subtraction DAC is an ECL 7-bit resolution monolithic DAC with 14-bit accuracy. Laser-trimmed thin-film nichrome resistors and high-speed bipolar circuitry allow the DAC output to settle to 14-bit accuracy in only 35ns.

A "remainder" or coarse conversion-error voltage is generated by resistively subtracting the DAC output from the output of the sample/hold amplifier. Before the second (LSB) conversion, the "remainder" is amplified by a wideband fast-settling two-input amplifier with a gain of 32V/V. To prevent overload on large amplitude transients, the active input is switched off to blank the amplifier input from the beginning of the S/H acquisition time to the end of the MSB encoder update time.

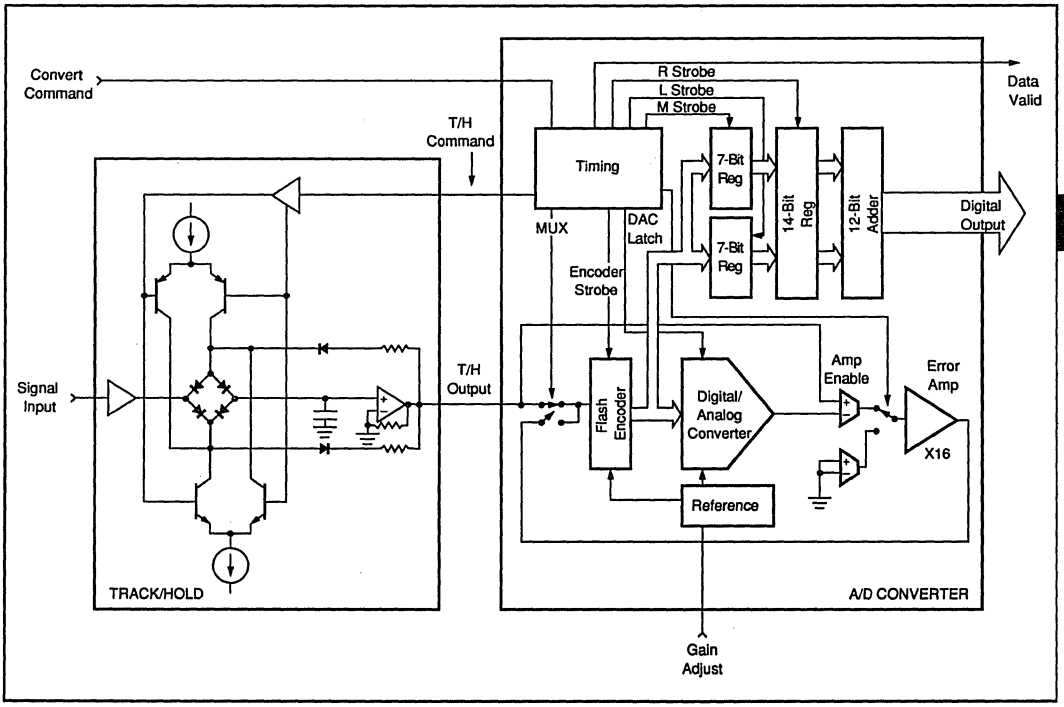


FIGURE 1. ADC603 Block Diagram—A Two-Step Subranging Architecture.

Internal timing circuits (ECL logic is used internally) supply all the critical timing signals necessary for proper operation of the ADC603. Some noncritical timing signals are also generated in the digital error correction circuitry. Timing signals are laser-trimmed for both pulse width and delay. ECL logic is used for its speed, low noise characteristics and timing delay stability over a wide range of temperatures and power supply voltages. Basic timing is derived from the output of a three-stage shift register driven by a synchronized 20MHz oscillator.

The convert command pulse is differentiated to allow triggering by pulses from as narrow as 10ns to as wide as 80% duty cycle.

The ADC603 timing technique generates a variable width S/H gate pulse which is determined by the conversion command pulse period minus a fixed 67ns ADC conversion time. ADC603 conversion rates are therefore possible somewhat above the 10MHz specification, but S/H acquisition time is sacrificed and accuracy is rapidly degraded. Converters with guaranteed operation at 10.24MHz sample rate are available on special order.

The output of the MSB and LSB encoders are read into separate 7-bit latches. The latched MSB data, along with the latched LSB data, is then read into a 14-bit latch after the leading edge of the LSB strobe and before being applied to the adder, where the actual error correction takes place. These latches eliminate any critical timing problems that could result when the converter is operated at the maximum conversion rate.

The function of the digital error correction circuitry is to assemble the 7-bit words from the two flash encoders into a 12-bit output word. A data valid (DV) pulse is also generated which is used to indicate when output data can be latched into an external register. This DV pulse is delayed 6ns after the output data has settled to allow sufficient set-up time for an external TTL data latch. A high-speed latch such as a 74F174 is recommended.

The 14-bit register output is then sent to a 12-bit adder where the final data output word is created. The MSB data forms the most significant seven bits of a 12-bit word, with the last five bits being assigned zeros. In a similar fashion, the LSB data from the least significant bits forms the other input to the adder, with the first five bits being assigned zeros. As two 12-bit words are being added, the output of the adder could exceed 12 bits in range; however, the final data output is only a 12-bit word, so a means of detecting an overrange is included to prevent reading erroneous data. The converter data output is forced to all ones for a full-scale input or overrange. The data output does not "roll-over" if the converter input exceeds its specified full-scale range of ±1.25V.

DISCUSSION OF PERFORMANCE

DYNAMIC PERFORMANCE TESTING

The ADC603 is a very high performance converter and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a fast Fourier transform (FFT) to the ADC digital output will provide data on all important dynamic performance parameters: total harmonic distortion (THD), signal-to-noise ratio (SNR) or the more severe signal-to-noise-and-distortion ratio (SINAD), and intermodulation distortion (IMD).

A typical test setup for performing high-speed FFT testing of analog-to-digital converters is shown in Figure 2. Highly accurate phase-locked signal sources allow high resolution FFT measurements to be made without using window functions. By choosing appropriate signal frequencies and sample rates, an integral number of signal frequency periods can be sampled. As no spectral leakage results, a "rectangular" window (no window function) can be used. This was used to generate the typical FFT performance curves shown on page 5.

If generators cannot be phase-locked and set to extreme accuracy, a very low side-lobe window must be applied to the digital data before executing an FFT. A commonly used window such as the Hanning window is not appropriate for testing high performance converters; a minimum four-sample Blackman-Harris window is strongly recommended.[1] To

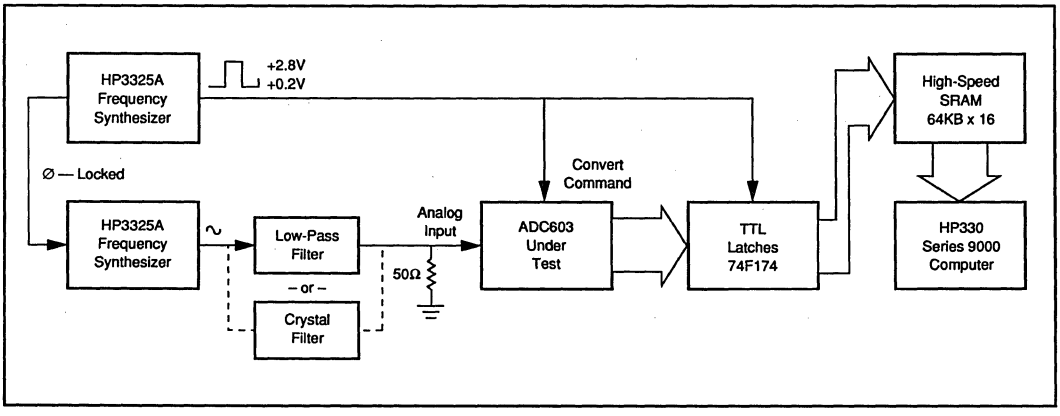


FIGURE 2. Block Diagram of FFT Test for THD, SNR, and SINAD.

assure that the majority of codes are exercised in the ADC603 (12 bits), a 4096-point FFT is taken. If the data storage RAM is limited, a smaller FFT may be taken if a sufficient number of samples are averaged (i.e., a 10-sample average of 512-point FFTs).

Dynamic Performance Definitions

1. Signal-to-Noise-and-Distortion[2] Ratio (SINAD):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (first 9 harmonics)}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

3. Total Harmonic Distortion (THD):

$$10 \log \frac{\text{Harmonic Power (first 9 harmonics)}}{\text{Sinewave Signal Power}}$$

4. Intermodulation Distortion (IMD):

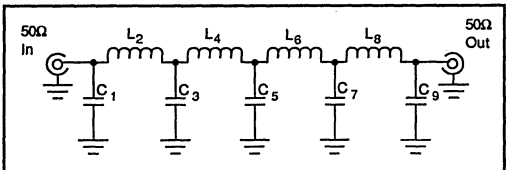
$$10 \log \frac{\text{Highest IMD Product Power (to 5th order)}}{\text{Sinewave Signal Power}}$$

IMD is referenced[3] to the larger of the test signals f_1 or f_2. Five "bins" either side of peak are used for calculation of fundamental and harmonic power. The "0" frequency bin (DC) is not included in these calculations as it is of little importance in dynamic signal processing applications.

APPLICATION TIPS

Attention to test set-up details can prevent errors that contribute to poor test results. Important points to remember when testing high performance converters are:

1. The ADC analog input must not be overdriven. Using a signal amplitude slightly lower than FSR will allow a small amount of "headroom" so that noise or DC offset voltage will not overrange the ADC and "hard limit" on signal peaks.
2. Two-tone tests can produce signal envelopes that exceed FSR. Set each test signal to slightly less than –6dB to prevent "hard limiting" on peaks.
3. Low-pass filtering (or bandpass filtering) of test signal generators is absolutely necessary for THD and IMD tests. An easily built LC low-pass filter (Figure 4) will eliminate harmonics from the test signal generator.
4. Test signal generators must have exceptional noise performance (better than –155dBC/Hz) to achieve accurate SNR measurements.[4] Good generators together with fifth-order elliptical bandpass filters are recommended for



9th Order 0.5dB Ripple
Tchebychev Low-Pass Filter

Attenuation at 2x cutoff frequency = 90dB.

Cutoff frequency = –3dB frequency; to convert cutoff frequency to –0.5dB frequency, multiply all LC values by 0.98997.

CUTOFF FREQ. (MHz)	C_1 (pF)	C_3 (pF)	C_5 (pF)	C_7 (pF)	C_9 (pF)	L_2 (µH)	L_4 (µH)	L_6 (µH)	L_8 (µH)
5	1134.6	1729.2	1765.6	1729.2	1134.6	2.056	2.216	2.216	2.056
2.5	2269	3458	3531	3458	2269	4.11	4.43	4.43	4.11
1.25	4538	6917	7062	6917	4538	8.23	8.86	8.86	8.23
0.625	9077	13,833	14,125	13,833	9077	16.45	17.73	17.73	16.45

FIGURE 4. Ninth-Order Harmonic Filter.

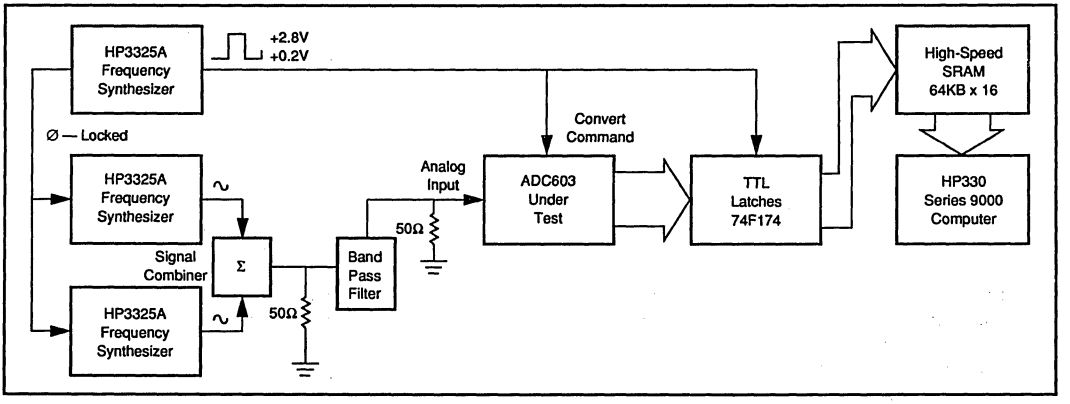


FIGURE 3. Block Diagram of FFT Test for Two-Tone IMD.

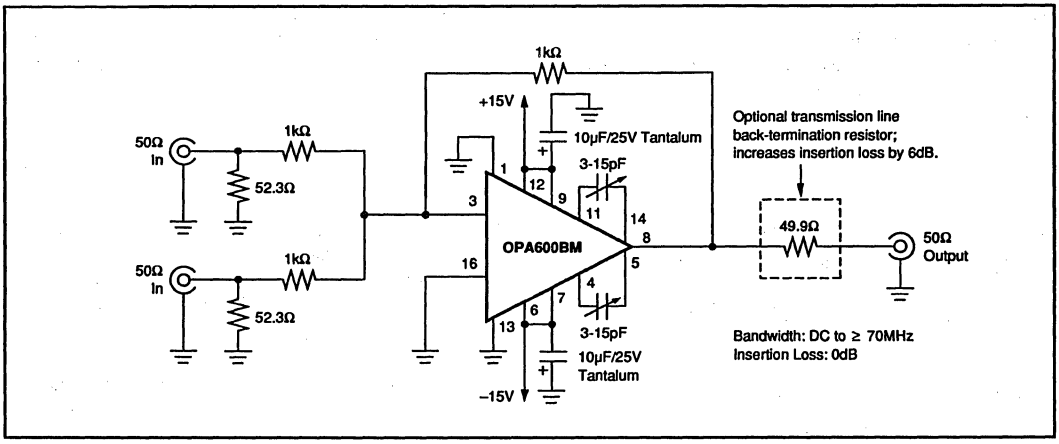


FIGURE 5. Active Signal Combiner.

SNR tests. Narrow-bandwidth crystal filters can also be used to filter generator broadband noise, but they should be carefully tested for operation at high levels.

5. The analog input of the ADC603 should be terminated directly at the input pin sockets with the correct filter terminating impedance (50Ω or 75Ω), or it should be driven by a low output impedance buffer such as an OPA675/676, OPA620/621, or OPA600. Short leads are necessary to prevent digital noise pickup.
6. A low-noise (jitter) clock signal (convert command) generator is required for good ADC dynamic performance. A poor generator can seriously impair good SNR performance. Short leads are necessary to preserve fast TTL rise times.
7. Two-tone testing will require isolation between test signal generators to prevent IMD generation in the test generator output circuits. An active summing amplifier using an OPA600 is shown in Figure 5. This circuit will provide excellent performance from DC to 5MHz with harmonic and intermodulation distortion products typically better than –70dBC. A passive (hybrid transformer) signal combiner can also be used (Figure 6) over a range of about 0.1MHz to 30MHz. This combiner's port-to-port isolation will be ≈45dB between signal generators and its input-output insertion loss will be ≈6dB. Distortion will be better than –85dBC for the powdered-iron core specified. Avoid ferrites.
8. A very low side-lobe window must be used for FFT calculations if generators cannot be phase-locked and set to exact frequencies. A minimum four-sample Blackman-Harris window function is recommended.[1]
9. Digital data must be latched into an external TTL 12-bit register by the Data Valid output pulse or by using the convert command pulse (Figures 11, 12, 13, and 14). Latches should be mounted on PC boards in very close proximity to the ADC603. Avoid long leads.
10. Do not overload the data output logic. These outputs are designed to drive 2 TTL loads. Do not connect ADC603 data output pins directly to a noisy digital bus; use external 3-state logic for noise immunity.

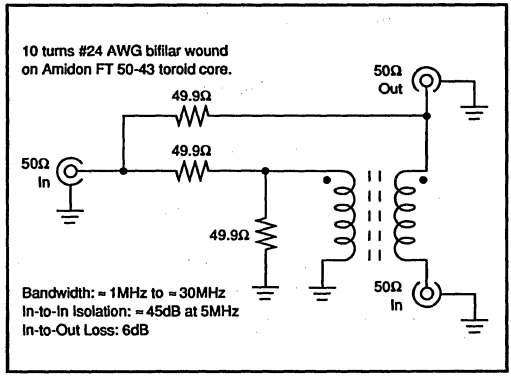


FIGURE 6. Passive Signal Combiner.

11. A well-designed, clean PC board layout will assure proper operation and clean spectral response.[5, 6] Proper grounding and bypassing, short lead lengths, separation of analog and digital signals, and the use of ground planes are particularly important for high frequency circuits. Multilayer PC boards are recommended for best performance, but a two-sided PC board with large, heavy (2oz-foil) ground planes can give excellent results, if carefully designed.
12. Prototyping "plug-boards" or wire-wrap boards will not be satisfactory.
13. Floating inputs can eliminate ground-loop noise. A simple common-mode choke (balun) shown in Figure 7 and 8, or a differential amplifier (Figure 9 and 10) can reduce analog input noise.
14. Connect analog and digital ground pins of the ADC603 directly to the ground plane. In our experience, connecting these pins to a common ground plane gives the best results. Analog and digital power supply commons

should be tied together at the ground plane. Adding power supply and ground-return filtering[7] is optional and may improve noise rejection.

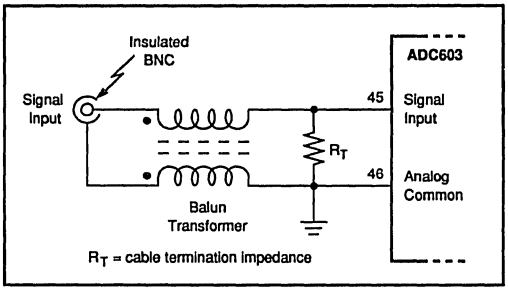


FIGURE 7. Floating-Input Balun Transformer.

NOTES:

1. "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform", Fredric J. Harris. *Proceedings of the IEEE*, Vol. 66, No. 1, January 1978, pp 51-83.
2. SINAD test includes harmonics whereas SNR does not include these important spurious products.
3. If IMD is referenced to peak envelope power, distortion will be of 6dB better.
4. "Test Report: FFT Characterization of Burr-Brown ADC600K", Signal Conversion Ltd., Swansea, Wales, U.K.
5. *MECL System Design Handbook*, 3rd Edition, Motorola Corp.
6. Motorola MECL, Motorola Corp.
7. Murata-Erie BNX002-01.

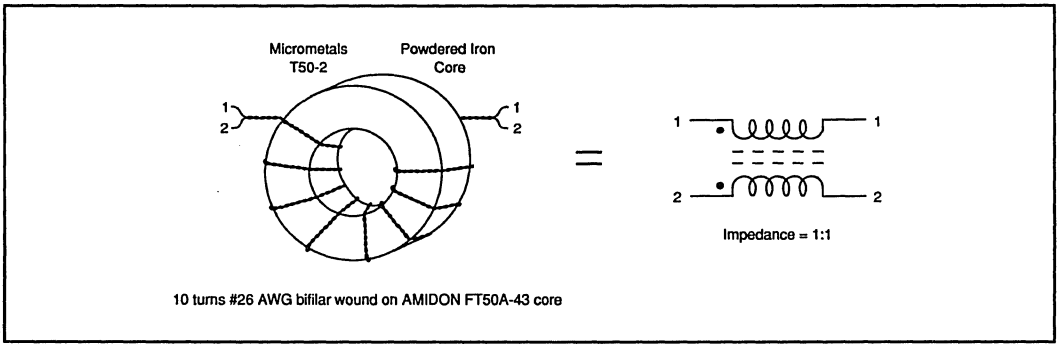


FIGURE 8. Balun Transformer Windings.

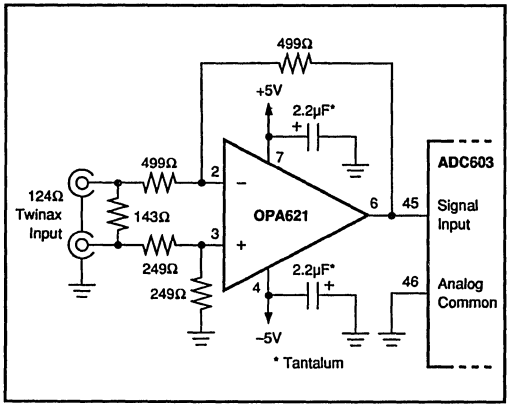


FIGURE 9. Differential Input Buffer Amplifier (Gain = –1V/V).

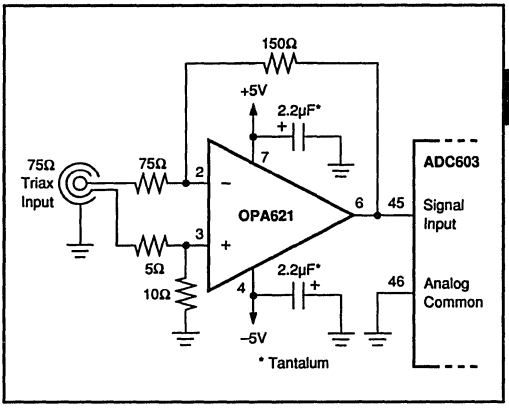


FIGURE 10. Differential Input Buffer Amplifier (Gain = –2V/V).

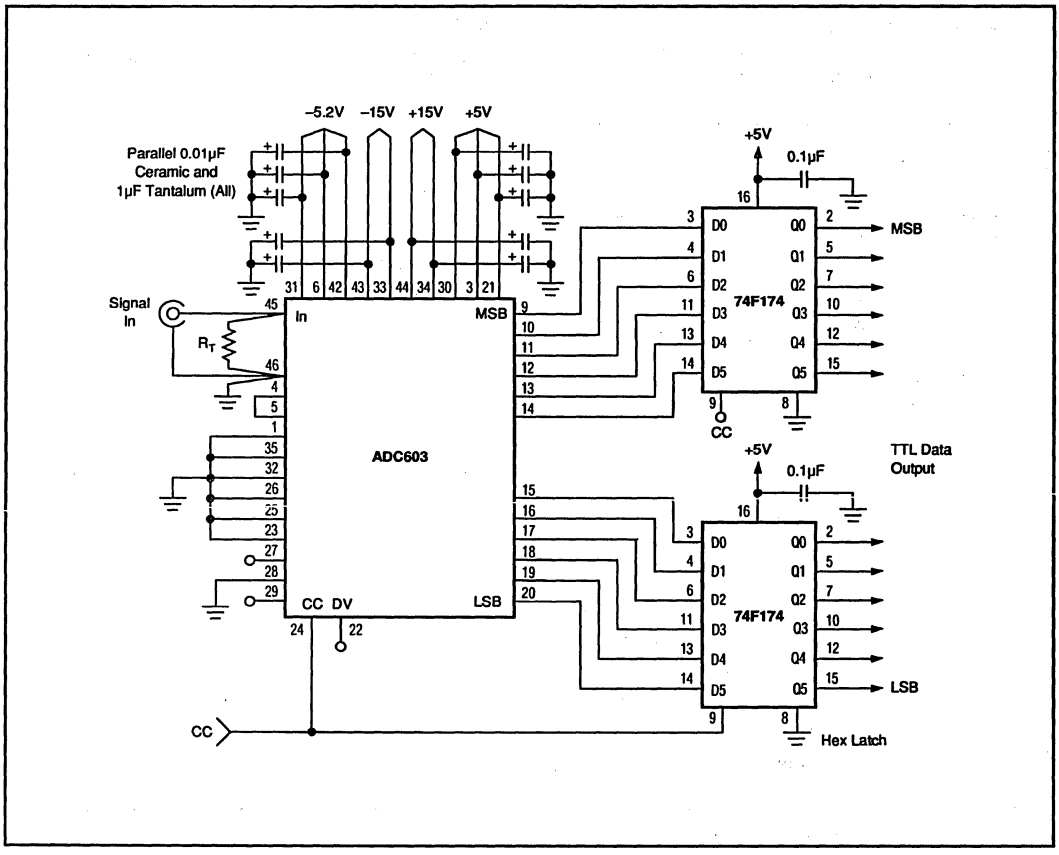


FIGURE 11. Interface Circuit—Digital Output Strobed by Convert Command. Supply connection shown: power supplies and grounds shared by analog and digital pins using common ground plane (recommended circuit).

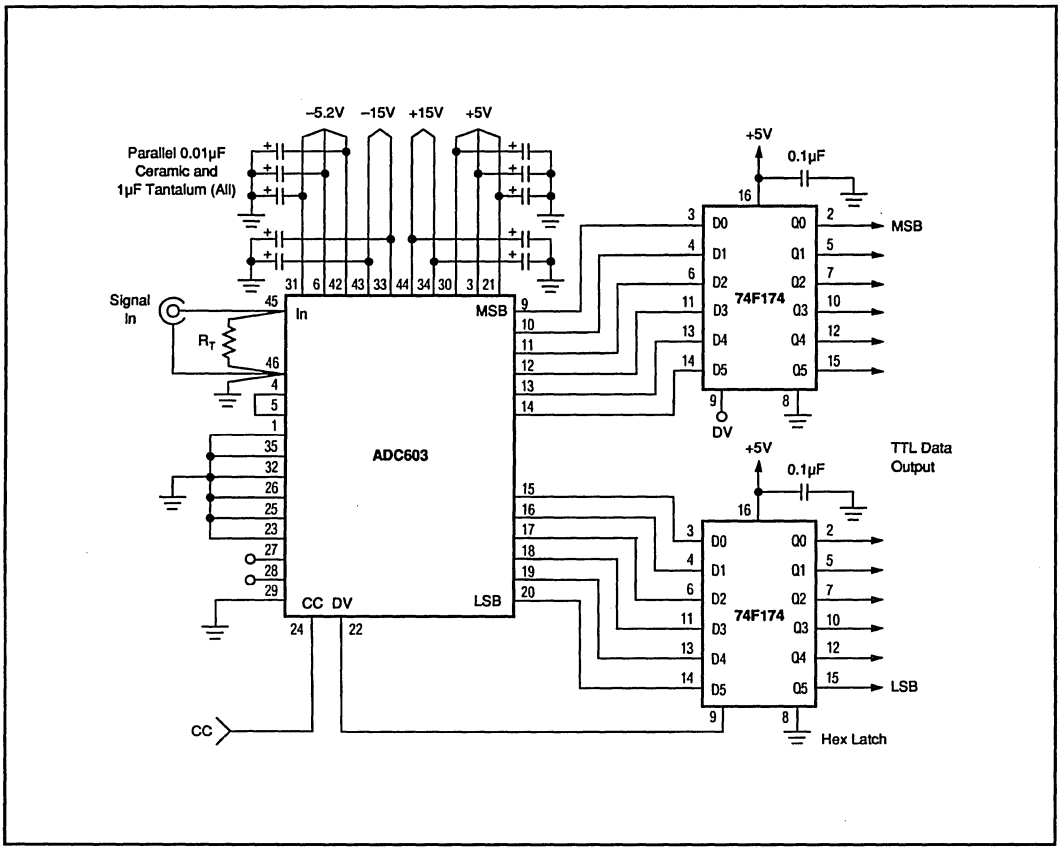
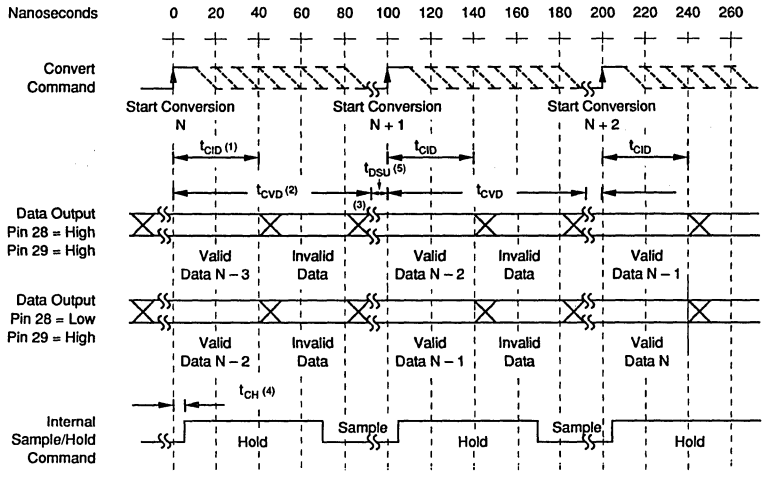


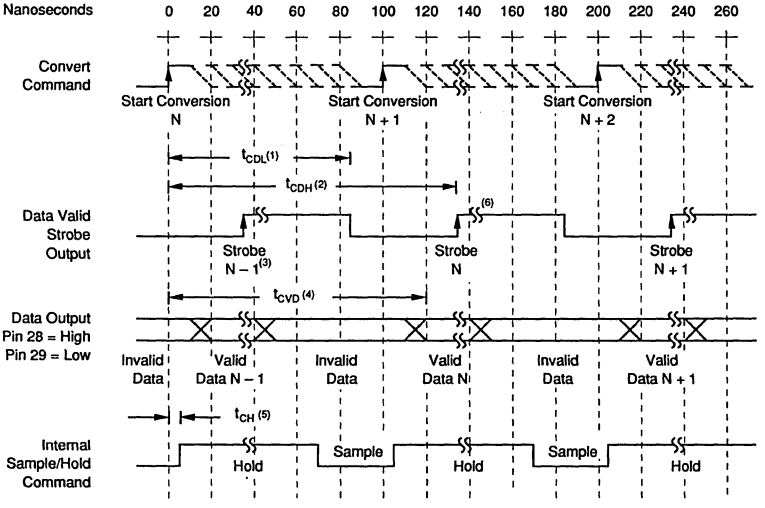
FIGURE 12. Interface Circuit—Digital Output Strobed by Data Valid Pulse. Supply connection shown: power supplies and grounds shared by analog and digital pins using common ground plane.



NOTES: (1) t_{CID} = Delay time from Convert Command to Invalid Data. Typical value = 40ns. Independent of conversion rate. (2) t_{CVD} = Delay time from Convert Command to Valid Data. Typical value = 93ns. Independent of conversion rate. (3) The ⟆ symbol indicates the portion of the waveform that will "stretch out" at lower conversion rates. (4) t_{CH} = Delay time from Convert Command to the internal hold. Typical value = 6ns. Independent of conversion rate. (5) t_{DSU} = data set-up time. This depends on conversion rate and may be calculated by:

$$t_{DSU} = \frac{1}{f_{SAMPLE}} - t_{CVD}$$

FIGURE 13. Convert Command Strobe Timing.



NOTES: (1) t_{CDL} = Delay time from Convert Command to the falling edge of Data Valid Strobe. Typical value = 85ns. Independent of conversion rate. (2) t_{CDH} = Delay time from Convert Command to the rising edge of Data Valid Strobe. Typical value = 135ns. Independent of conversion rate. (3) If Conversion "N" is the first conversion, then there is no Strobe N-1, and the Data Valid Strobe Signal will simply be high until t_{CDL} after the first Convert Command. (4) t_{CVD} = delay time from Convert Command to Valid Data. Typical value = 120ns. Independent of conversion rate. (5) t_{CH} = Delay time from Convert Command to Internal Hold Command. Typical value = 6ns. Independent of conversion rate. (6) The ⟆ symbol indicates the portion of the waveform that will "stretch out" at lower conversion rates.

FIGURE 14. Data Valid Strobe Timing.

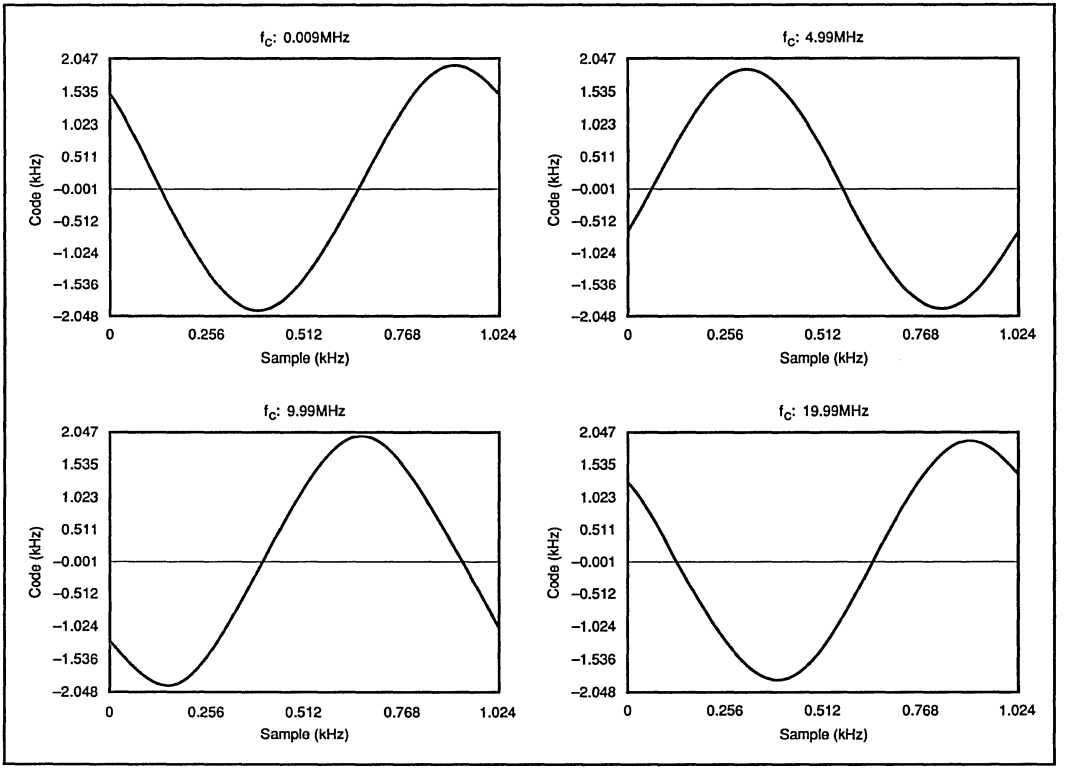


FIGURE 15. Digitized Sine Waves (f_S = 10MHz).

DIGITIZING INPUT WAVEFORMS

The response of the ADC603 is illustrated by the digitized waveforms of Figure 15. The 4.99MHz sine wave near the Nyquist limit is virtually identical to much lower frequency sine wave input. The under-sampled 19.999MHz sine wave illustrates the ADC603's excellent analog input full-power bandwidth.

HISTOGRAM TESTING

Histogram testing is used to test differential nonlinearity of the ADC603. This system's block diagram (the same for FFT testing and waveform digitizing) is shown in Figure 2 and histogram test results for a typical converter are shown in Figure 16. Note that low-frequency differential nonlinearity is 1/2LSB and it shows virtually no degradation near the Nyquist limit of 5MHz; there are no missing codes present and the peak nonlinearity does not exceed 1LSB. Histogram testing is a useful performance indicator as the width of all codes can be determined.

SPECTRUM ANALYZER TESTING

A beat-frequency technique (Figure 17) can be used to view digitized waveforms on an oscilloscope and, with care, this technique can also be used for testing high-speed ADC dynamic characteristics with an analog spectrum analyzer.

In this method a test signal is digitized by the ADC603 and the output digital data is latched into an external latch by the converter Data Valid output pulse driving a divide-by-N counter. The buffered ECL/TTL level translator latch drives a 12-bit video-speed DAC which reconstructs the digital signal back into an analog replica of the ADC603 input. This analog signal, including distortion products and noise resulting from digitization, can then be viewed on an ordinary analog RF spectrum analyzer.

It is important to realize that the distortion and noise measured by this technique include not only that from the ADC603, but also from the entire analog-to-analog test system. Nonlinearity of the reconstruction circuit must be very low to measure a high performance ADC, and this places severe requirements on the ADC, deglitcher, and buffer amplifiers.

Using a high-speed video DAC63 in the analog reconstruction circuit allows excellent test circuit linearity to be achieved. Clocking the DAC (demodulating) at f_C/N allows a longer DAC settling time and keeps linearity high in the digital-to-analog portion of the test circuit. Spectrum analyzer dynamic range can be a limiting factor in this method. To increase dynamic range, a sharp notch filter can be used to attenuate the high-level fundamental frequency. Attenuating

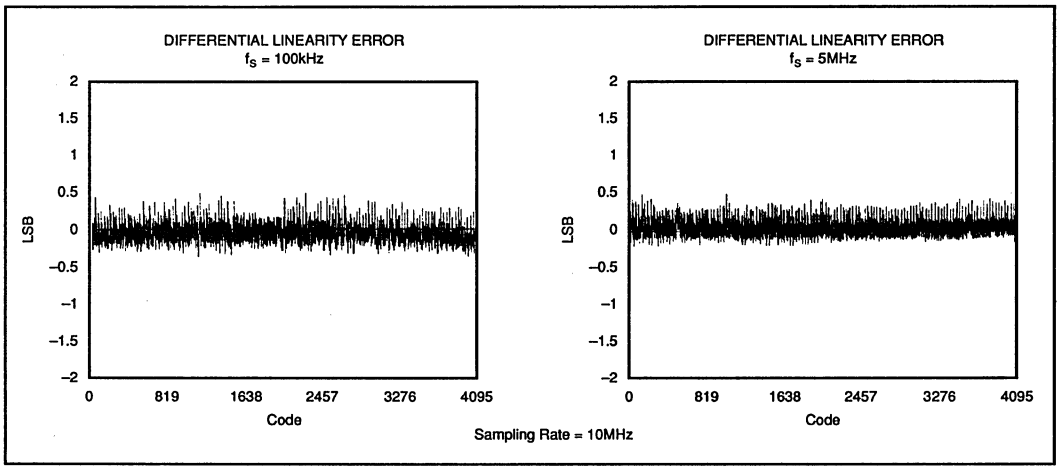


FIGURE 16. 100kHz and 5MHz Differential Linearity.

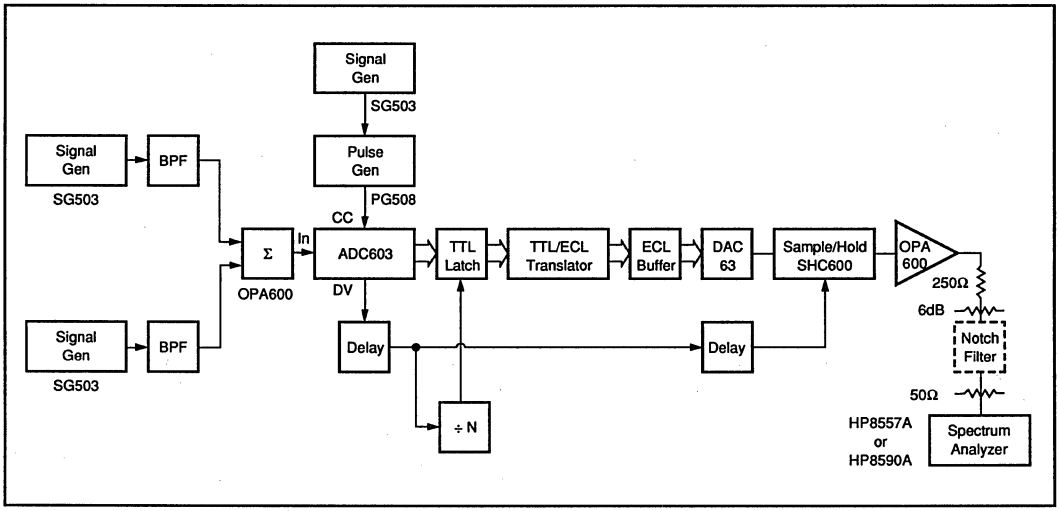


FIGURE 17. Analog-to-Analog Spectral Analysis by Beat-Frequency Techniques.

the high-level fundamental signal allows the analog spectrum analyzer to be used on a more sensitive range without generating distortion products within its front end.

Note that even though the signal is demodulated at a frequency of sample rate/N, the distortion products still maintain a correct frequency relationship to the fundamental. While this analog technique can give good performance, it cannot exclude some distortion products unavoidably generated within the analog reconstruction portion of the test system. For this reason, the digital FFT technique is capable of more accurate high-speed analog/digital converter dynamic performance measurements and is the preferred method of testing high-performance A/D converters.

TIMING

The ADC603 generates all necessary timing signals internally. There are two methods for reading output data, offering three selectable levels of data pipeline delay as described below.

Convert Command Timing Option (pin 29 = HI)

With this option, the Convert Command signal is used both for initiating a new conversion and for reading valid data from a previous conversion. This method is most useful in synchronous systems where data samples are taken continuously.

See Figure 13 for timing relationships.

Pin 28 is used to control the amount of pipeline delay. If pin 28 is held LO, then output data "N – 2" will be valid on the rising edge of Convert Command "N." If pin 28 is held HI, then output data "N – 3" will be valid on the rising edge of Convert Command "N." These timing relationships are valid at any conversion rate up to 10MHz. At rates approaching 10MHz, however, the data setup time before the rising Convert Command edge may become as short as 6ns. Therefore, the use of high-speed TTL latches such as the 74F174 hex flip-flop is recommended to capture the data. If slower latches must be used, then the setup time can effectively be improved by adding several nanoseconds of delay between the Convert Command and the latch clock signal.

Data Valid Timing Option (pin 29 = LO)

With this option, data from conversion "N" becomes valid after a fixed delay from the rising edge of Convert Command "N." The delay is approximately 135ns, at which time the Data Valid strobe signal will rise. This signal may be connected directly to the clock input of the user's data latch.

See Figure 18 for timing relationships. Pin 28 must be left HI at all times when using the Data Valid timing option.

The advantages of this method are that no subsequent conversions are required in order to read the data, and the data is available as soon as possible after the start of conversion. Therefore, the Data Valid option is most useful in systems where the ADC may be operated asynchronously, or where the very first data latch output after power-up must represent a valid conversion. Note that because the delay is fixed at approximately 135ns independent of conversion rate, the Data Valid pulse will overlap into the next conversion at rates above 7.4MHz. This does not preclude proper operation at any rate up to 10MHz.

DATA OUTPUT

Output logic inversion can be accomplished by programming pin 27. Binary Two's Complement or Inverted Binary Two's Complement output data formats are available (Table II).

The ADC603 output logic is TTL compatible. The tri-state output is controlled by $\overline{\text{ENABLE}}$ pin 25. For normal operation, pin 25 will be tied LO. A logic HI on pin 25 will switch the ouput data register to a high-impedance state (Figure 20). Output OFF leakage current I_{OZL} and I_{OZH} will be less than 50µA over the converter's specified operating temperature range. Tri-state output should be isolated from noisy digital bus lines, since the noise can couple back through the OFF data register and create noise in the ADC.

DIGITAL INPUTS

Logic inputs are TTL compatible. Open inputs will assume a HI logic state; unused inputs may be allowed to float or they may be tied to an appropriate TTL logic level.

	DATA LATCHED BY CONVERT COMMAND		DATA LATCHED BY DATA VALID STROBE
PIN NUMBER	N–3	N–2	N–1
28	HI	LO	HI
29	HI	HI	LO

TABLE I. Pipeline Delay Selection Logic.

NOTES:

1. *FAST™ Applications Handbook*, 1987. Fairchild Semiconductor Corp.
2. *Fairchild Advanced CMOS Technology*, Technology Seminar Notes, 1985.
3. "Impedance Matching Tweaks Advance CMOS IC Testing", Gerald C. Cox, *Electronic Design*, April, 1987.
4. "Grounding for Electromagnetic Compatibility", Jerry H. Boogar, *Design News*, 23 February, 1987.

OFFSET AND GAIN ADJUSTMENT

The ADC603 is carefully laser-trimmed to achieve its rated accuracy without external adjustments. If desired, both gain error and input offset voltage error may be trimmed to zero with external potentiometers (Figure 23). Trim range is typically 2%; large offsets and gain changes should be made elsewhere in the system. Using an input buffer amplifier allows a convenient point for injecting large offset voltages and making wide gain adjustments.

If offset and gain trim is not used, pins 36 and 37 should be left unconnected.

THERMAL REQUIREMENTS

The ADC603 is tested and specified over a temperature range of 0°C to +70°C (J, K grade) and –55°C to +125°C (R, S grade). The converters are tested in a forced-air environment with a 10 SCFM air flow. With a small heat sink (Figure 24) the ADC603 can be operated in a normal convection ambient-air environment if submodule case temperature does not exceed the upper limit of its specification.[1]

High junction temperature can be avoided by using forced-air cooling, but it is not required at moderate ambient

INPUT VOLTAGE (Exact Center of Code)	DIGITAL DATA OUTPUT LOGIC CODING	
	Binary Two's Complement (BTC) Pin 27 = LO	Inverted Binary Two's Complement (BTC) Pin 27 = HI
	MSB LSB	MSB LSB
+FS (+1.25V)	011111111111*	100000000000*
+FS – 1LSB (+1.2494V)	011111111111	100000000000
+FS – 2LSB (+1.2488V)	011111111110	100000000001
+3/4FS (+0.9375V)	011000000000	100111111111
+1/2FS (+0.625V)	010000000000	101111111111
+1/4FS (+0.3125V)	001000000000	110111111111
+1LSB (+610µV)	000000000001	111111111110
Bipolar Zero (0V)	000000000000	111111111111
–1LSB (–610µV)	111111111111	000000000000
–1/4FS (–0.3125V)	111000000000	000111111111
–1/2FS (+0.625V)	110000000000	001111111111
–3/4FS (–0.9375V)	101000000000	010111111111
–(FS – 1LSB) (–1.2494V)	100000000001	011111111110
–FS (–1.25V)	100000000000	011111111111

* Indicates overrange condition.

TABLE II. Digital Data Output Logic Coding.

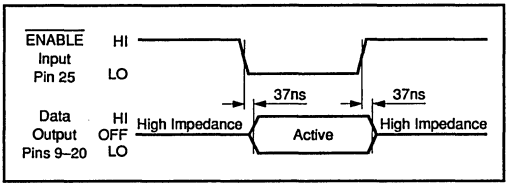


FIGURE 22. Digital Data Tri-State Output.

temperatures. Thermal resistance of the ADC603 package is: θ_{JC} = 4.8°C/W, measured to the underside of the case.

NOTES:

1. "Maximizing Heat Transfer from PCBs", *Machine Design*, March 26, 1987, Jeilong Chung.

ENVIRONMENTAL SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device —it cannot be improved by testing. However, environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels.

Burr-Brown offers environmentally screened versions of our standard military temperature range products, designed to provide enhanced reliability at moderate cost. The screening illustrated in Table III is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient way of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

SCREEN	MIL-STD-883 METHOD, CONDITION	SCREENING LEVEL
Internal Visual	2017	Visual requirements only (par 3.1 through 3.1.8)
Electrical Test	Burr-Brown Test Procedure	
High Temperature Storage (Stabilization Bake)	1008	24hr, +125°C
Temperature Cycling	1010	10 cycles, –55°C to –125°C
Constant Acceleration	2001, A	2000G; Y Axis Only
Burn-In	1015, D	160hr, +125°C T_J, No PDA
Hermeticity, Gross Leak	1014, C	Bubble Test Only, Preconditioning Omitted
Final Electrical	Burr-Brown Test Procedure	
External Visual	2009	

TABLE III. Optional Screening Flow.

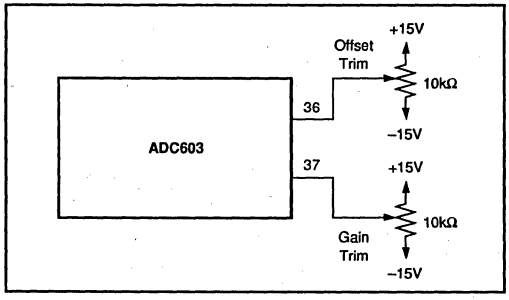


FIGURE 19. Optional Gain and Offset Trim.

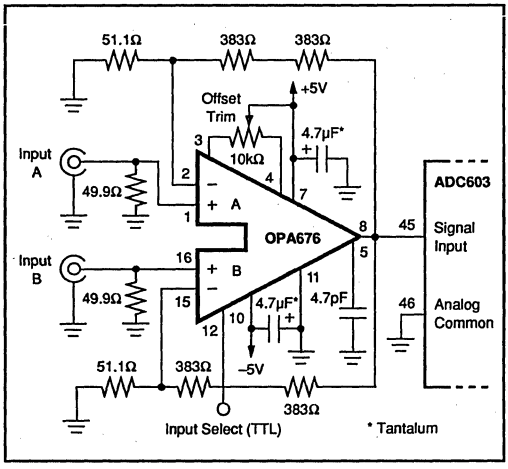


FIGURE 21. A Multiplexed-Input Buffer Amplifier (Gain = +16V/V).

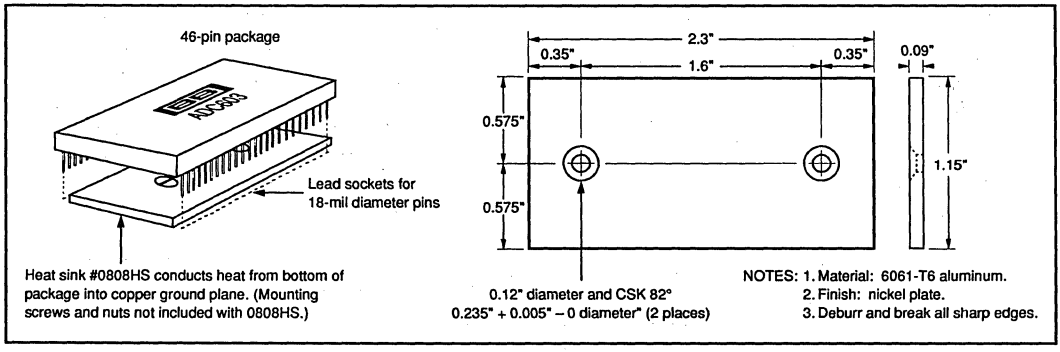
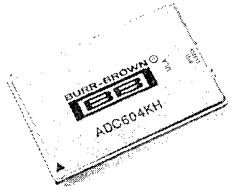


FIGURE 20. Heat Sink Transfers Heat from the DIP Package into a Copper Ground Plane.

BURR-BROWN®



ADC604

12-Bit 5MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 83dB SPURIOUS-FREE DYNAMIC RANGE
- SAMPLE RATE: DC to 5MHz
- HIGH SIGNAL/NOISE RATIO: 68.6dB
- LOW HARMONIC DISTORTION: –83dBc
- LOW INTERMOD. DISTORTION: –83dBc
- SWEPT-POWER FFT TESTED (KH)
- COMPLETE SUBSYSTEM: Contains Sample/Hold and Reference
- 46-PIN DIP PACKAGE
- 0°C TO +70°C

APPLICATIONS

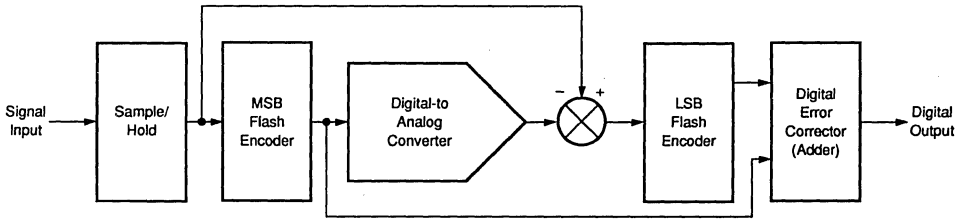
- DIGITAL RECEIVERS
- RADAR SIGNAL ANALYSIS
- FFT SPECTRUM ANALYSIS
- RF INSTRUMENTATION
- MAGNETIC RESONANCE IMAGING
- SIGINT, ECM, AND EW SYSTEMS

DESCRIPTION

The ADC604 is a high performance 12-bit analog-to-digital converter designed for spectrum analysis applications. Outstanding spurious-free dynamic range has been achieved by minimizing noise and distortion. Complete static and dynamic test results are furnished with each KH grade unit at no additional cost.

The ADC604 is a two-step subranging ADC sub-system containing an ADC, sample/hold amplifier, voltage reference, timing, and error-correction circuitry in a 46-pin hybrid DIP package. Logic is TTL.

This converter is pin-compatible with Burr-Brown's 12-bit 10MHz ADC603.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 66-6491 • FAX: (602) 889-1510

PDS-1052

SPECIFICATIONS

ELECTRICAL

T_C = +25°C, 5MHz sampling rate, R_S = 50Ω, $\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = −5.2V, and 15-minute warmup in convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	ADC604JH MIN	ADC604JH TYP	ADC604JH MAX	ADC604KH MIN	ADC604KH TYP	ADC604KH MAX	UNITS
RESOLUTION				12			12	Bits
INPUTS								
ANALOG								
Input Range	Full Scale	−1.25		+1.25	*		*	V
Input Impedance			1.5			*		MΩ
Input Capacitance			5			*		pF
DIGITAL								
Logic Family				TTL Compatible				
Convert Command	Start Conversion			Positive Edge				
Pulse Width	t = Conversion Period	10		t − 20	*		*	ns
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error	f = 8kHz		±0.2	±2		±0.1	±1	%FSR[1]
Input Offset	DC		±0.2	±2		*	±0.75	%FSR
Integral Linearity Error	f = 8kHz		0.75			0.5	1	LSB
Differential Linearity Error	f = 8kHz: 100% of all Codes		0.5	1.0		0.4	0.75	LSB
No Missing Codes			Guaranteed			Guaranteed		
Power Supply Rejection	$\Delta +V_{CC}$ = ±10%		±0.03	±0.1		*	*	%FSR/%
	$\Delta -V_{CC}$ = ±10%		±0.04	±0.1		*	*	%FSR/%
	$\Delta +V_{DD1}$ = ±10%		±0.004	±0.07		*	*	%FSR/%
	$\Delta -V_{DD2}$ = ±10%		±0.01	±0.07		*	*	%FSR/%
CONVERSION CHARACTERISTICS								
Sample Rate		DC		5M	*		*	Samples/s
Pipeline Delay	Logic Selectable		1, 2 or 3 Convert Command Periods					
DYNAMIC CHARACTERISTICS[2]								
Differential Linearity Error	f = 2MHz: 100% of all Codes		0.6	1.5		0.5	1.0	LSB
Harmonic Distortion (HD)								
f = 2.00MHz (−0.5dB)	f_S = 4.99MHz		−80	−75		−83	−80	dBc[3]
f = 8kHz (−0.5dB)			−83	−79		−86	−82	dBc
Two-Tone Intermodulation Distortion[4]								
f = 2.20MHz (−6.5dB)	f_S = 4.99MHz		−80	−75		−83	−80	dBc
f = 2.30MHz (−6.5dB)								
Spurious-Free Dynamic Range (SFDR)								
f = 2.00MHz (−0.5dB)	f_S = 4.99MHz	75	80		80	83		dB
f = 8kHz (−0.5dB)		79	83		82	86		dB
Signal-to-Noise Ratio (SNR)								
f = 2.00MHz (−0.5dB)	f_S = 4.99MHz	64	67		65	68.6		dB
f = 8kHz (−0.5dB)		65.5	70.5		66.5	71.5		dB
Aperture Delay Time		−20	−5	+20	*	*	*	ns
Aperture Jitter			9	20		*	*	ps rms
Analog Input Bandwidth (−3dB)								
Small Signal	−20dB Input	40	60		*	*		MHz
Full Power	0dB Input	20	30		*	*		MHz
Overload Recovery Time	2x Full-Scale Input		205	400		*	*	ns
OUTPUTS								
Logic Family				TTL Compatible				
Logic Coding	Logic Selectable		Two's Complement or Inverted Two's Complement					
Logic Levels	Logic "LO" I_{OL} = −3.2mA	0	+0.3	+0.8	*	*	+0.5	V
	Logic "HI" I_{OH} = 160µA	+2.4	+3.5	+5.0	*	*	*	V
EOC Delay Time	Data Out to DV		See Timing Diagram: Figure 15					
Tri-State Enable/Disable Time	I_{OL} = −6.4mA, 50% In to 50% Out		37	100		*	*	ns
Data Valid Pulse Width			See Timing Diagram: Figure 15					
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		−14.25	−15	−15.75	*	*	*	V
$+V_{DD1}$		+4.75	+5	+5.25	*	*	*	V
$-V_{DD2}$		−4.95	−5.2	−5.46	*	*	*	V
Supply Currents: $+I_{CC}$	Operating		+60			*	+80	mA
$-I_{CC}$			−60			*	−80	mA
$+I_{DD1}$			+280			*	+330	mA
$-I_{DD2}$			−565			*	−630	mA
Power Consumption	Operating		6.1	7.0		*	*	W

* Same specifications as ADC604JH.

SPECIFICATIONS (CONT)

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

$\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = –5.2V, R_S = 50Ω, 5MHz sampling rate, 15-minute warmup, and $T_C = T_{MIN}$ to T_{MAX}, unless otherwise noted.

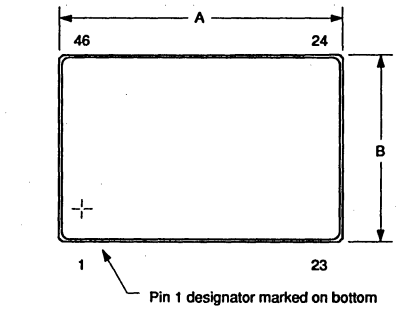
PARAMETER	CONDITIONS	ADC604JH MIN	ADC604JH TYP	ADC604JH MAX	ADC604KH MIN	ADC604KH TYP	ADC604KH MAX	UNITS
TEMPERATURE RANGE								
Specification	T_{CASE}	0		+70	*		*	°C
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error	f = 8kHz		±0.4	±2		*	±1.5	%FSR
Input Offset	DC		±0.4	±2		*	±1.5	%FSR
Integral Linear Error	f = 8kHz		0.75			0.6	1.25	LSB
Differential Linearity Error	f = 8kHz: 100% of all Codes		0.6	1.5		0.5	*	LSB
No Missing Codes			Guaranteed			Guaranteed		
Power Supply Rejection	$\Delta +V_{CC}$ = ±10%		±0.04	±0.2		*		%FSR/%
	$\Delta -V_{CC}$ = ±10%		±0.05	±0.2		*		%FSR/%
	$\Delta +V_{DD1}$ = ±10%		±0.004	±0.1		*		%FSR/%
	$\Delta -V_{DD2}$ = ±10%		±0.02	±0.1		*		%FSR/%
CONVERSION CHARACTERISTICS								
Sample Rate		DC		5M	*		*	Samples/s
DYNAMIC CHARACTERISTICS[2]								
Differential Linearity Error	f = 2MHz: 100% of all Codes		0.6	1.5		0.5	*	LSB
Harmonic Distortion (HD)								
f = 2.00MHz (–0.5dB)	f_S = 4.99MHz		–75	–73		–80	–77	dBc[3]
f = 8kHz			–80	–77		–83	–80	dBc
Two-Tone Intermodulation Distortion[4]								
f = 2.20MHz (–6.5dB)	f_S = 4.99MHz		–77	–72		–82	–80	dBc
f = 2.30MHz (–6.5dB)								
Spurious-Free Dynamic Range (SFDR)								
f = 2.00MHz (–0.5dB)	f_S = 4.99MHz	73	75		77	80		dB
f = 8kHz (–0.5dB)		77	80		80	83		dB
Signal-to-Noise Ratio (SNR)								
f = 2.00MHz (–0.5dB)	f_S = 4.99MHz	62	67		*	68		dB
f = 8kHz (–0.5dB)		65			*	70		dB
Aperture Delay Time		–25	–6	+25	*	*	*	ns
Aperture Jitter			10			*	20	ps rms
Analog Input Bandwidth (–3dB)								
Small Signal	–20dB Input		60			*		MHz
Full Power	0dB Input		30			*		MHz
Overload Recovery Time	2x Full-Scale Input		220			*		ns
OUTPUTS								
Logic Levels	Logic "LO", I_{OL} = –3.2mA	0	+0.3	+0.5	*	*	*	V
	Logic "HI", I_{OH} = 160µA	+2.4	+3.5	+5.0	*	*	*	V
EOC Delay Time	Data Out to DV	See Figure 15; Δ Timing Typically Within ±20% Over Temperature						
Tri-State Enable/Disable Time	I_{OL} = –6.4mA, 50% In to 50% Out		42	100		*	*	ns
Data Valid Pulse Width		See Figure 15; Δ Timing Typically Within ±20% Over Temperature						
POWER SUPPLY REQUIREMENTS								
Supply Currents: $+I_{CC}$	Operating		+65	+80		*	*	mA
$-I_{CC}$			–61	–80		*	*	mA
$+I_{DD1}$[5]			+285	+333		*	*	mA
$-I_{DD2}$[6]			–570	–630		*	*	mA
Power Consumption	Operating		6.1	7.0		*	*	W

* Same specifications as ADC604JH.

NOTES: (1) FSR: Full-Scale Range = 2.5Vp-p. (2) Units with lower distortion are available on special order; inquire. (3) dBc = level referred to carrier-input signal = 0dB); f = input frequency; f_S = sampling frequency. (4) IMD is referred to the larger of the two input test signals. If referred to the peak envelope signal (=0dB), the intermodulation products will be 6dB lower. (5) Pins 3 and 30 (analog) typically draw 80% of the total +5V current. Pin 21 (digital) typically draws 20%. (6) Pin 6 (analog) typically draws 45% of the total -5.2V current. Pin 31 (digital) typically draws 55%.

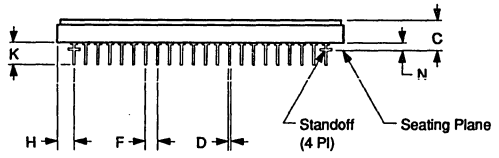
MECHANICAL

Package — Metal and Ceramic



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.370	2.420	60.20	61.47
B	1.560	1.610	39.62	40.89
C	.200	.260	5.08	6.60
D	.018 DIA. BASIC		0.46 DIA. BASIC	
F	.100 BASIC		2.54 BASIC	
H	.075	.115	1.91	2.92
K	.150	.190	3.81	4.83
L	1.300 BASIC		33.02 BASIC	
M	—	10°	—	10°
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)



PIN ASSIGNMENTS

1	Common (Case)	46	Common (Analog)
2	DNC	45	Analog Signal In
3	$+V_{DD1}$ (+5V) Analog	44	$+V_{CC}$ (+15V) Analog
4	S/H Out	43	$-V_{CC}$ (–15V) Analog
5	A/D In	42	NC
6	$-V_{DD2}$ (–5.2V) Analog	41	NC
7	NC	40	NC
8	NC	39	DNC
9	Bit 1 (MSB)	38	DNC
10	Bit 2	37	Gain Adjust
11	Bit 3	36	Offset Adjust
12	Bit 4	35	Common (Analog)
13	Bit 5	34	$+V_{CC}$ (+15V) Analog
14	Bit 6	33	$-V_{CC}$ (–15V) Analog
15	Bit 7	32	Common (Analog)
16	Bit 8	31	$-V_{DD2}$ (–5.2V) Digital
17	Bit 9	30	$+V_{DD1}$ (+5V) Analog
18	Bit 10	29	1 Pipeline Delay Select
19	Bit 11	28	0 Pipeline Delay Select
20	Bit 12 (LSB)	27	Output Logic Invert
21	$+V_{DD1}$ (+5V) Digital	26	Common (Digital)
22	Data Valid Output	25	Tri-State $\overline{\text{ENABLE}}$
23	Common (Digital)	24	Convert Command In

NOTE: NC = no connection, DNC = do not connect.

ORDERING INFORMATION

ADC604 ( ) H

Basic Model Number

Performance Grade Code
J, K: 0°C to +70°C Case Temperature

Package Code
H: Metal and Ceramic

ABSOLUTE MAXIMUM RATINGS

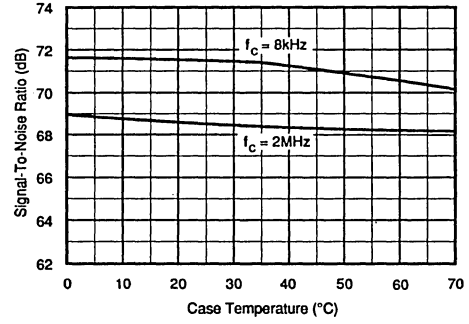
$\pm V_{CC}$	±16.5V
$+V_{DD1}$	+7.0V
$\pm V_{DD2}$	–7.0V
Analog Input	±5.0V
Logic Input	–0.5V to $+V_{DD1}$
Case Temperature (Operating)	+125°C
Junction Temperature	+165°C
Storage Temperature	–65°C to +165°C

Stresses above these ratings may permanently damage the device.

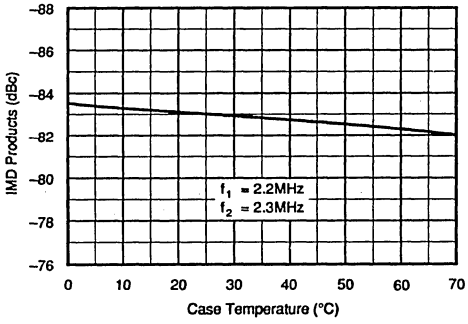
TYPICAL PERFORMANCE CURVES

$\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = −5.2V, R_s = 50Ω, 5MHz sampling rate, 15-minute warmup, and T_C = +25°C, unless otherwise noted.

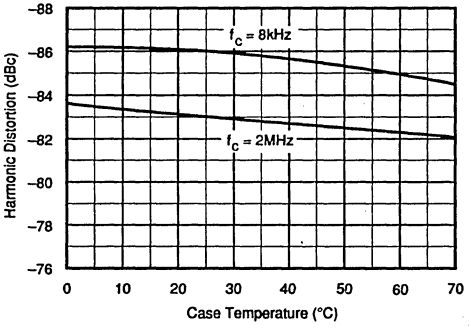
SIGNAL-TO-NOISE RATIO vs TEMPERATURE



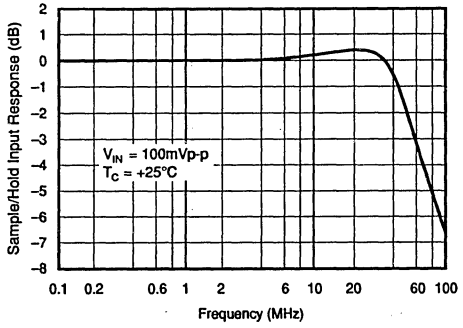
TWO-TONE IMD vs TEMPERATURE



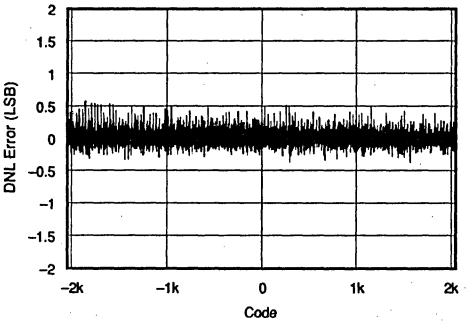
HARMONIC DISTORTION vs TEMPERATURE



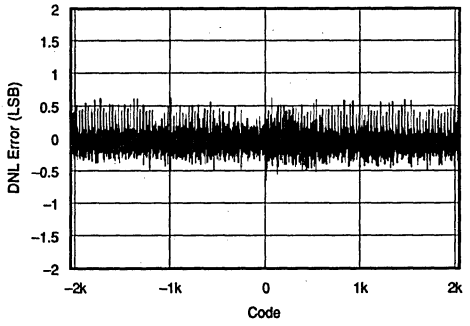
ANALOG INPUT BANDWIDTH



2MHz DIFFERENTIAL LINEARITY ERROR



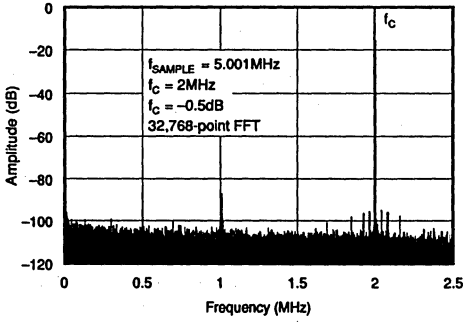
8kHz DIFFERENTIAL LINEARITY ERROR



TYPICAL PERFORMANCE CURVES

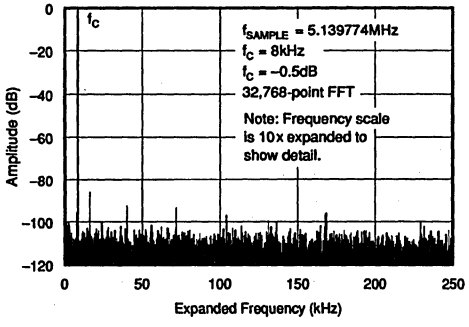
$\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = −5.2V, R_s = 50Ω, 5MHz sampling rate, 15-minute warmup, and T_c = +25°C, unless otherwise noted.

2MHz HARMONIC DISTORTION



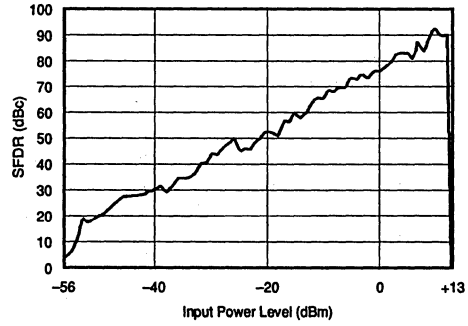
NOTE: All harmonics are aliased.

8kHz HARMONIC DISTORTION

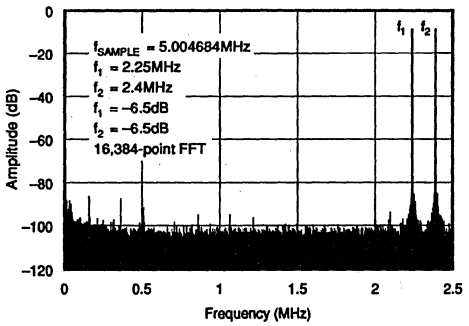


NOTE: Harmonics appear in normal order.

SPURIOUS-FREE DYNAMIC RANGE vs INPUT POWER LEVEL



TWO-TONE INTERMODULATION DISTORTION



THEORY OF OPERATION

ADC604 is a two-step subranging analog-to-digital converter. This architecture is shown in Figure 1. The major system building blocks are: sample/hold amplifier, MSB flash encoder, DAC and error amplifier, LSB flash encoder, digital error corrector, and timing circuits. ADC604 uses hybrid technology with laser-trimmed integrated circuits mounted in a multilayer ceramic package to integrate this complex circuit into a complete analog-to-digital converter subsystem with state-of-the-art performance.

Conceptually, the subranging technique is simple: sample and hold the input signal, convert to digital with a coarse ADC, convert back to analog with a coarse-resolution (but high-accuracy) DAC, subtract this voltage from the S/H output, amplify this "remainder," convert to digital with a second coarse ADC, and combine the digital output from the first ADC (MSB) with the digital output from the second ADC (LSB). In practice, however, achieving high conversion speed without sacrificing accuracy is a difficult task.

The analog input signal is sampled by a high-speed sample/hold amplifier with very low distortion, fast acquisition time and very low aperture uncertainty (jitter). A bootstrapped diode bridge sampling switch is used to achieve an excellent compromise between speed and accuracy. The diode bridge switching transients are buffered from the analog input by a high input impedance buffer amplifier. Since the hold capacitor does not appear in the feedback of the diode bridge output buffer, the capacitor can acquire the signal in 65ns. The low-bias-current output buffer is then required to settle to only the resolution (7 bits) of the first (MSB) flash encoder in 65ns while an additional 85ns is allowed for settling to the resolution (12 bits) of the second (LSB) flash encoder. Sample/hold droop appears as only an offset error and does not affect linearity.

Both the MSB and the LSB flash encoder (ADC) functions are performed by multiplexing one high-speed 7-bit resolution converter formed by parallel-connecting two 6-bit flash ADCs. The DAC voltage reference is also used to generate reference voltages for the MSB and LSB encoder to compensate drift errors. Buffering and scaling amplifiers are laser-trimmed to minimize voltage offset errors and optimize gain (input full-scale range) symmetry.

The subtraction DAC is an ECL 7-bit resolution monolithic DAC with 14-bit accuracy. Laser-trimmed thin-film nichrome resistors and high-speed bipolar circuitry allow the DAC output to settle to 14-bit accuracy in only 35ns.

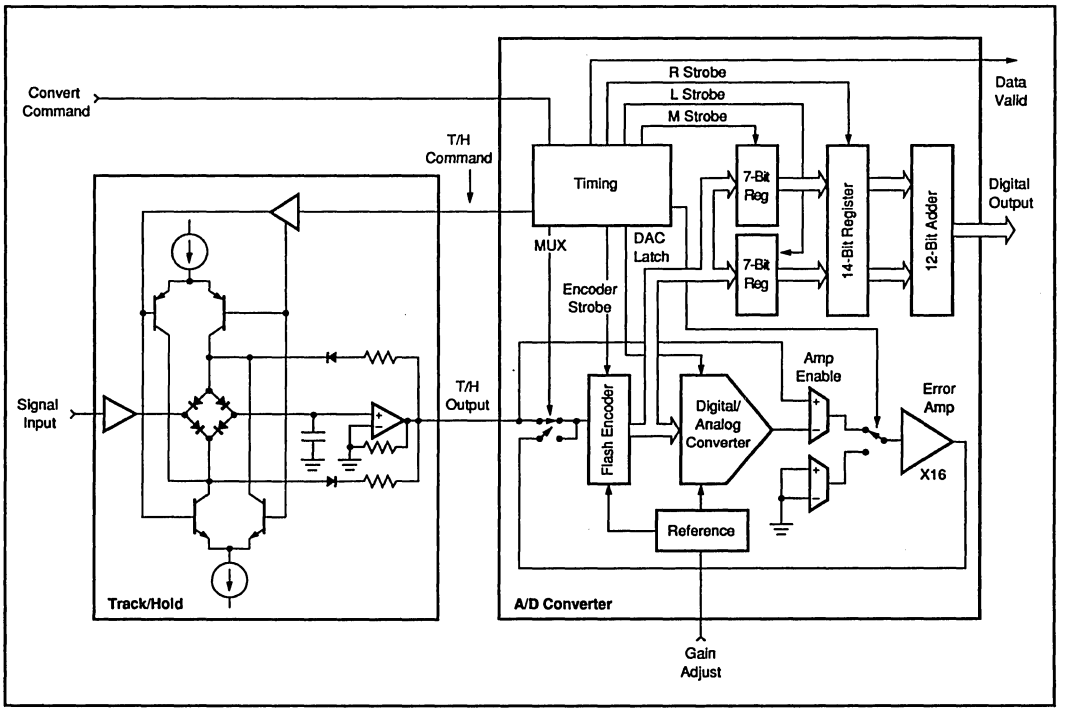


FIGURE 1. ADC604 Block Diagram—A Two-Step Subranging Architecture.

A "remainder" or coarse conversion-error voltage is generated by resistively subtracting the DAC output from the output of the sample/hold amplifier. Before the second (LSB) conversion, the "remainder" is amplified by a wideband fast-settling two-input amplifier with a gain of 32V/V. To prevent overload on large amplitude transients, the active input is switched off to blank the amplifier input from the beginning of the S/H acquisition time to the end of the MSB encoder update time.

Internal timing circuits (ECL logic is used internally) supply all the critical timing signals necessary for proper operation of the ADC604. Some noncritical timing signals are also generated in the digital error correction circuitry. Timing signals are laser-trimmed for both pulse width and delay. ECL logic is used for its speed, low noise characteristics and timing delay stability over a wide range of temperatures and power supply voltages. Basic timing is derived from the output of a three-stage shift register driven by a synchronized 20MHz oscillator.

The convert command pulse is differentiated to allow triggering by pulses from as narrow as 10ns to as wide as 80% duty cycle.

The ADC604 timing technique generates a variable width S/H gate pulse which is determined by the conversion command pulse period minus a fixed 135ns ADC conversion time. ADC604 conversion rates are therefore possible somewhat above the 5MHz specification but S/H acquisition time is sacrificed and accuracy is rapidly degraded. Converters with guaranteed operation at 5.12MHz sample rate are available on special order.

The output of the MSB and LSB encoders are read into separate 7-bit latches. The latched MSB data, along with the latched LSB data, is then read into a 14-bit latch after the leading edge of the LSB strobe and before being applied to the adder, where the actual error correction takes place. These latches eliminate any critical timing problems that could result when the converter is operated at the maximum conversion rate.

The function of the digital error correction circuitry is to assemble the 7-bit words from the two flash encoders into a 12-bit output word. A data valid (DV) pulse is also generated to indicate when output data can be latched into an external register. This DV pulse is delayed 6ns after the output data has settled to allow sufficient set-up time for an external TTL data latch. A high-speed latch such as a 74F174 is recommended.

The 14-bit register output is then sent to a 12-bit adder where the final data output word is created. The MSB data forms the most significant seven bits of a 12-bit word, with the last five bits being assigned zeros. In a similar fashion, the LSB data from the least significant bits form the other input to the adder with the first five bits being assigned zeros. As two 12-bit words are being added, the output of the adder could exceed 12 bits in range; however, the final data output is only a 12-bit word, so a means of detecting an overrange is included to prevent reading erroneous data. The converter

data output is forced to all ones for a full-scale input or over-range. The data output does not "roll-over" if the converter input exceeds its specified full-scale range of ±1.25V.

DISCUSSION OF PERFORMANCE

DYNAMIC PERFORMANCE TESTING

ADC604 is a very high dynamic range converter and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a fast Fourier transform (FFT) to the ADC digital output will provide data on all important dynamic performance parameters: harmonic distortion (HD), signal-to-noise ratio (SNR), spurious-free dynamic range (SFDR), swept power response, and inter-modulation distortion (IMD).

A typical test setup for performing high-speed FFT testing of analog-to-digital converters is shown in Figure 2. Highly accurate phase-locked signal sources allow high resolution FFT measurements to be made without using window functions. By choosing appropriate signal frequencies and sample rates, an integral number of signal frequency periods can be sampled. As no spectral leakage results, a "rectangular" window (no window function) can be used. This coherent sampling method was used to generate the typical FFT performance curves shown on page 6. The ratio of the sampling frequency to the signal frequency must be a non-rational number.

If generators cannot be phase-locked and set to extreme accuracy, a very low side-lobe window must be applied to the digital data before executing an FFT. A commonly used window such as the Hanning window is not appropriate for testing high performance converters; a minimum four-sample Blackman-Harris window is strongly recommended.[1] To assure that the majority of codes are exercised in the ADC604 (12 bits), a 4096-point FFT is taken. If the data storage RAM is limited, a smaller FFT may be taken if a sufficient number of samples are averaged (ie, a 10-sample average of 512 point FFTs).

DYNAMIC PERFORMANCE DEFINITIONS

1. Spurious-free dynamic range (SFDR):

$$10 \log \frac{\text{sinewave signal power}}{\text{highest harmonic or spurious signal power}}$$

2. Signal-to-noise ratio (SNR):

$$10 \log \frac{\text{sinewave signal power}}{\text{total noise power}}$$

3. Harmonic distortion (HD):

$$10 \log \frac{\text{highest harmonic power (to ninth harmonic)}}{\text{sinewave signal power}}$$

4. Intermodulation distortion (IMD):

$$10 \log \frac{\text{highest IMD product power (to fifth order)}}{\text{sinewave signal power}}$$

IMD is referenced to the larger of the test signals f_1 or f_2, not to full-scale range (FSR). The "0" frequency bin (DC) is not included in these calculations as it is of little importance in dynamic signal processing applications.

APPLICATION TIPS

Attention to test set-up details can prevent errors that contribute to poor test results. Important points to remember when testing high performance converters are:

1. The ADC analog input must not be overdriven. Using a signal amplitude slightly lower than FSR will allow a small amount of "headroom" so that noise or DC offset voltage will not overrange the ADC and "hard limit" on signal peaks.
2. Two-tone tests can produce signal envelopes that exceed FSR. Set each test signal to slightly less than –6dB to prevent "hard limiting" on peaks.
3. Low-pass filtering (or bandpass filtering) of test signal generators is absolutely necessary for accurate tests. An easily built LC low-pass filter (Figure 4) will eliminate harmonics from the test signal generator.
4. Test signal generators must have exceptional noise performance (better than –155dBc/Hz) to achieve accurate SNR measurements.[4] Good generators together with fifth-order elliptical bandpass filters are recommended for SNR tests. Narrow bandwidth crystal filters can also be used to filter signal generator broadband noise, but they should be carefully tested for low-distortion operation at high signal levels.
5. The analog input of the ADC604 should be terminated directly at the input pin sockets with the correct filter terminating impedance (50Ω or 75Ω) or it should be driven by a very low distortion buffer amplifier with low output impedance, such as an OPA621 or equivalent. Short leads (<1 inch) are necessary to prevent digital noise pickup.
6. A low phase noise (jitter) clock signal (convert command) generator is required for good ADC dynamic performance. A poor generator can seriously impair good SNR performance. Short leads are necessary to preserve fast TTL rise times.
7. Two-tone testing will require high isolation between test signal generators to prevent IMD generation in the test generator output circuits. A passive (hybrid transformer) signal combiner can be used (Figure 5) over a range of about 0.1MHz to 30MHz. This combiner's port-to-port isolation will be ≈45dB between signal generators and its input-output insertion loss will be ≈6dB. Distortion will be better than –85dBc for the powdered-iron core specified. Avoid ferrites.
8. A very low side-lobe window must be used for FFT tests if generators cannot be phase-locked and set to exact frequencies to perform coherent sampling measurements. A minimum four-sample Blackman-Harris window function is recommended.[1]
9. Digital data must be latched into an external TTL 12-bit register by the Data Valid output pulse or by using the Convert Command pulse (Figures 10 and 11). Latches

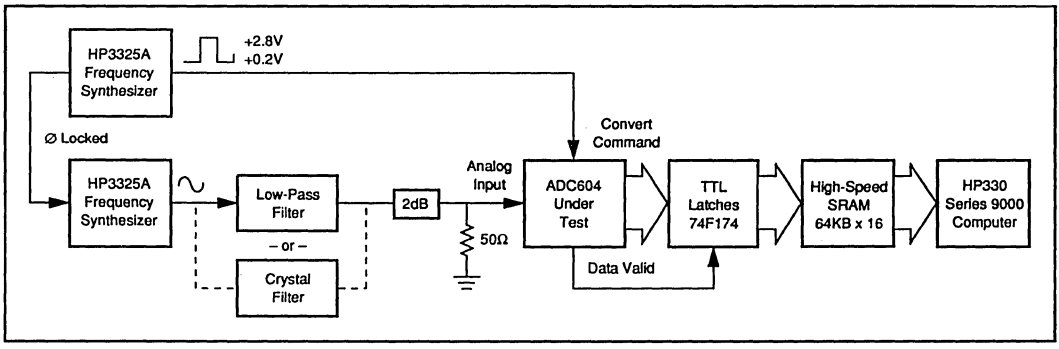


FIGURE 2. Block Diagram of FFT Test for HD, SNR, SFDR and Swept-Power Test.

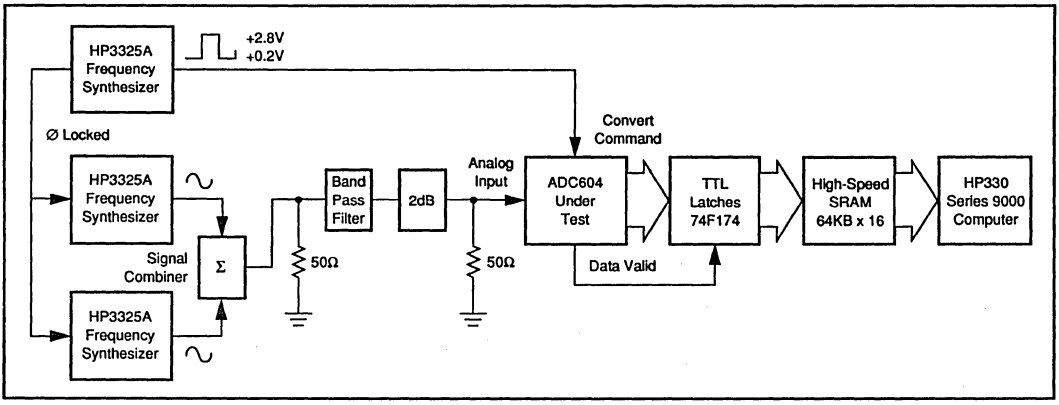
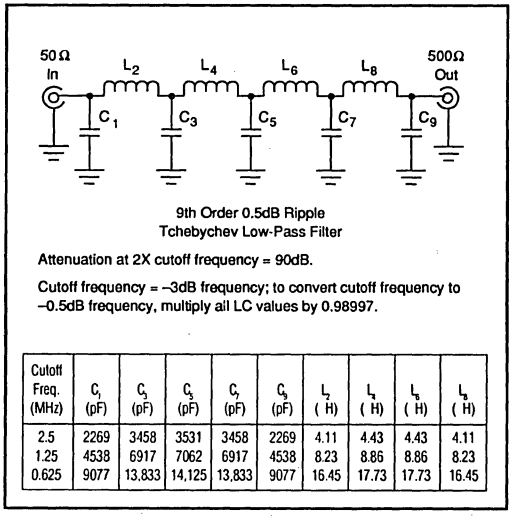


FIGURE 3. Block Diagram of FFT Test for Two-Tone IMD.



9th Order 0.5dB Ripple
Tchebychev Low-Pass Filter

Attenuation at 2X cutoff frequency = 90dB.

Cutoff frequency = –3dB frequency; to convert cutoff frequency to –0.5dB frequency, multiply all LC values by 0.98997.

Cutoff Freq. (MHz)	C_1 (pF)	C_3 (pF)	C_5 (pF)	C_7 (pF)	C_9 (pF)	L_2 (H)	L_4 (H)	L_6 (H)	L_8 (H)
2.5	2269	3458	3531	3458	2269	4.11	4.43	4.43	4.11
1.25	4538	6917	7062	6917	4538	8.23	8.86	8.86	8.23
0.625	9077	13,833	14,125	13,833	9077	16.45	17.73	17.73	16.45

FIGURE 4. Ninth-Order Harmonic Filter.

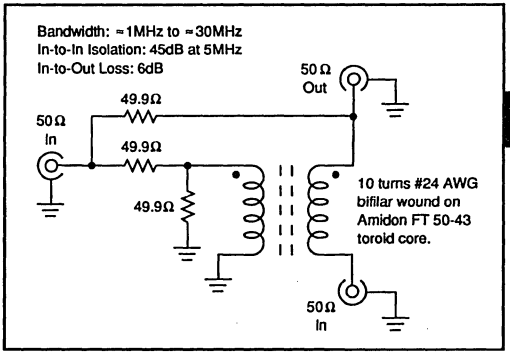


FIGURE 5. Passive Signal Combiner.

should be mounted on PC boards in very close proximity to the ADC604. Avoid long leads.

10. Do not overload the data output logic. These outputs are designed to drive two TTL loads but a lighter load will minimize the amplitude of digital switching transients. Do not connect ADC603 data output pins directly to a noisy digital bus; use external three-state logic for noise immunity.
11. A well-designed, clean PC board layout will assure proper operation and clean spectral response.[5][6] Proper grounding and bypassing, short lead lengths and separation of analog and digital signals, and the use of ground planes are particularly important for high frequency circuits. Multilayer PC boards are recommended for best performance, but a two-sided PC board with large, heavy (2oz-foil) ground planes can give acceptable results, if it is carefully designed.
12. Prototyping "plug-boards" or wire-wrap boards will NOT be satisfactory. There are no shortcuts.
13. Floating inputs can minimize ground-loop noise. A simple common-mode choke (balun) shown in Figure 6 and 7 or a differential amplifier (Figure 8 and 9) can reduce analog input noise.
14. Connect analog and digital ground pins of the ADC604 directly to the ground plane. In our experience, connecting these pins to a common ground plane gives the best results. Analog and digital power supply commons should be tied together at the ground plane. Adding power supply and ground-return filtering[7] is optional and may improve noise reduction.

NOTES:

1. "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform", Fredric J. Harris. *Proceedings of the IEEE*, Vol. 66, No. 1, January 1978, pp 51-83.
2. SFDR test includes harmonics and non-harmonic spurious products.
3. If IMD is referenced to peak envelope power, distortion will be of 6dB better.
4. "Test Report: FFT Characterization of Burr-Brown ADC600K", Signal Conversion Ltd., Swansea, Wales, U.K.
5. *MECL System Design Handbook*, 3rd Edition, Motorola Corp.
6. Motorola MECL. Motorola Corp.
7. Murata-Erie BNX002-01.

HISTOGRAM TESTING

Histograms are used to test differential nonlinearity of the ADC604. This system's block diagram (the same for FFT testing and waveform digitizing) is shown in Figure 2 and histogram test results for a typical converter are shown in the Typical Performance Curves. Note that low-frequency differential nonlinearity is under 1/2LSB and it shows virtually no degradation near the Nyquist limit of 2.5MHz; there are no missing codes present and the peak nonlinearity does not exceed 3/4LSB. Histogram testing is a useful performance indicator as the width of all codes can be determined.

SWEPT-POWER FFT TESTING

ADC604 converters are comprehensively tested to assure their conformance with Burr-Brown specifications. As this converter is designed for spectral-analysis applications, all important dynamic parameters are FFT tested, including a swept-power response measurement on KH-grade devices. A/D converter spurious signal levels typically show a variation with input signal power. To insure that these spurs remain at an acceptable level over the whole range of input signal amplitudes, a point-by-point measurement of worst-case spurious signal levels (harmonic or non-harmonic) is made as the input signal level is stepped by 1dB from an over-driven amplitude down to the ADC noise level. To minimize measurement error due to noise, eight FFTs are averaged to generate each data point.

Plotting these data points results in the curve labeled "Spurious-Free Dynamic Range vs Input Power Level" shown in the Typical Performance Curves on page 5. Each ADC604KH is supplied with FFT plots and a swept-power test plot. Units with guaranteed swept-power performance are available on special order.

TIMING

The ADC604 generates all necessary timing signals internally. There are two methods for reading output data, offering three selectable levels of data pipeline delay as described below:

(1) Convert Command timing option (pin 29 = HIGH) — With this option, the Convert Command signal is used both for initiating a new conversion and for reading valid data from a previous conversion. This method is most useful in synchronous systems where data samples are taken continuously.

See Figure 13 for timing relationships.

Pin 28 is used to control the amount of pipeline delay. If pin 28 is held LOW, then output data "N – 2" will be valid on the rising edge of Convert Command "N". If pin 28 is held HIGH, then output data "N – 3" will be valid on the rising edge of Convert Command "N". These timing relationships are valid at any conversion rate up to 5MHz. At a conversion rate of 5MHz, the data setup time before the rising Convert Command edge is about 50ns.

(2) Data Valid timing option (pin 29 = LOW) — With this option, data from conversion "N" becomes valid after a fixed delay from the rising edge of Convert Command "N". The delay is approximately 165ns. At about t = 185ns, the Data Valid strobe signal will rise. This strobe signal may be connected directly to the clock input of the external data latches, providing a data setup time of approximately 20ns.

See Figure 14 for timing relationships. Pin 28 must be left HIGH at all times when using the Data Valid timing option.

The advantages of this method are: (a) no subsequent conversions are required in order to read the data (ie, single-shot conversion capability), and (b) the data is available as soon as possible after the start of conversion. Therefore, the Data Valid option is most useful in systems where the ADC may be operated asynchronously, or where the very first data latch output after power-up must represent a valid conversion.

DATA OUTPUT

Output logic inversion can be accomplished by programming pin 27. Binary Two's Complement or Inverted Binary

Two's Complement output data format are available (Table II).

The ADC604 output logic is TTL compatible. The tri-state output is controlled by $\overline{\text{ENABLE}}$ pin 25. For normal operation, pin 25 will be tied LO. A logic HI on pin 25 will switch the ouput data register to a high-impedance state (Figure 16). Output OFF leakage current I_{OZL} and I_{OZH} will be less than 50µA over the converter's specified operating temperature range. Tri-state outputs must not be connected directly to a noisy digital bus, as this noise can be coupled into the converter's analog input.

DIGITAL INPUTS

Logic inputs are TTL compatible. Open inputs will assume a HI logic state; unused inputs may be allowed to float or they may be tied to an appropriate TTL logic level.

NOTES:

1. *FAST™ Applications Handbook*, 1987. Fairchild Semiconductor Corp.
2. *Fairchild Advanced CMOS Technology*, Technology Seminar Notes, 1985.
3. "Impedance Matching Tweaks Advance CMOS IC Testing", Gerald C. Cox, *Electronic Design*, April, 1987.

PIN NUMBER	DATA LATCHED BY CONVERT COMMAND		DATA LATCHED BY DATA VALID STROBE
	N-3	N-2	N-1
28	HI	LO	HI
29	HI	HI	LO

TABLE I. Pipeline Delay Selection Logic.

INPUT VOLTAGE	DIGITAL DATA OUTPUT LOGIC CODING	
	BINARY TWO'S COMPLEMENT (BTC) PIN 27 = LO	INVERTED BINARY TWO'S COMPLEMENT ($\overline{\text{BTC}}$) PIN 27 = HI
+FS (+1.25V)	011111111111	100000000000
+FS – 1LSB	011111111110	100000000001
+3/4 FS	000111111111	111000000000
+1/2 FS	001111111111	110000000000
+1 LSB	000000000000	111111111111
Bipolar Zero	111111111111	000000000000
–1 LSB	111111111110	000000000001
–1/2 FS	101111111111	010000000000
–3/4 FS	100111111111	011000000000
–FS – 1LSB	100000000001	011111111110
–FS (–1.25V)	100000000000	011111111111
	MSB LSB	MSB LSB

TABLE II. Digital Data Output Logic Coding.

3. "Grounding for Electromagnetic Compatibility", Jerry H. Boogar, *Design News*, February 23, 1987.

OFFSET AND GAIN ADJUSTMENT

The ADC604 is carefully laser-trimmed to achieve its rated accuracy without external adjustments. If desired, both gain error and input offset voltage error may be trimmed over a very small range with external potentiometers (Figure 17). Trim range is typically only 0.1%; larger offsets and gain changes should be made elsewhere in the system. Using an input buffer amplifier allows a convenient point for injecting large offset voltages and making wide gain adjustments.

If offset and gain trim is not used, pins 36 and 37 should be left unconnected.

THERMAL REQUIREMENTS

The ADC604 is tested and specified over a temperature range of 0°C to +70°C in a forced-air environment with 500 LFPM air flow. With a small heat sink (Figure 18), the ADC604 can be operated in a normal convection ambient-air environment if submodule case temperature does not exceed the upper limit of its specification.[1]

High junction temperature can be avoided by using forced-air cooling, but it is not required at moderate ambient temperatures. Thermal resistance of the ADC604 package is: θ_{JC} = 4.8°C/W measured to the underside of the case.

NOTES:

1. "Maximizing Heat Transfer from PCBs", *Machine Design*, March 26, 1987, Jeilong Chung.

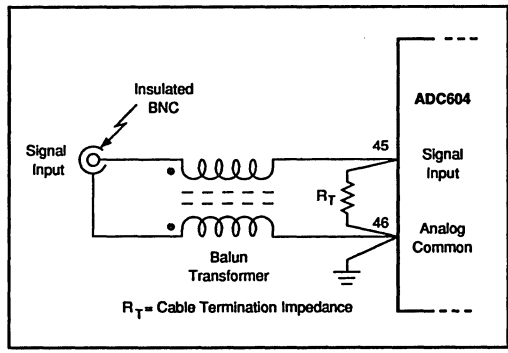


FIGURE 6. Floating-Input Balun Transformer.

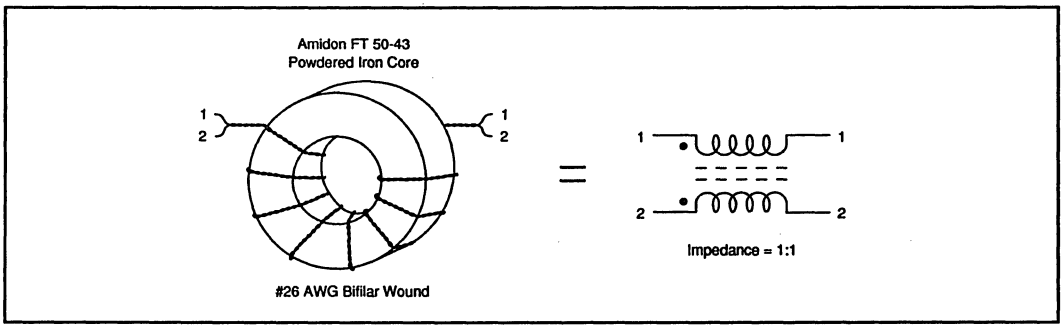


FIGURE 7. Balun Transformer Windings.

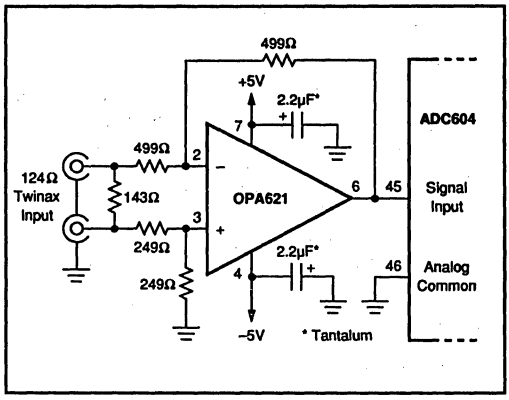


FIGURE 8. Differential Input Buffer Amplifier (Gain = -1V/V).

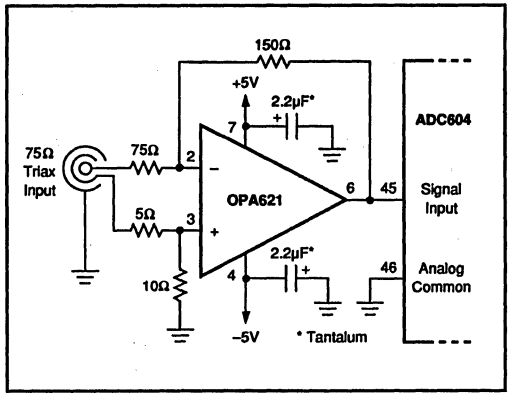


FIGURE 9. Differential Input Buffer Amplifier (Gain = -2V/V).

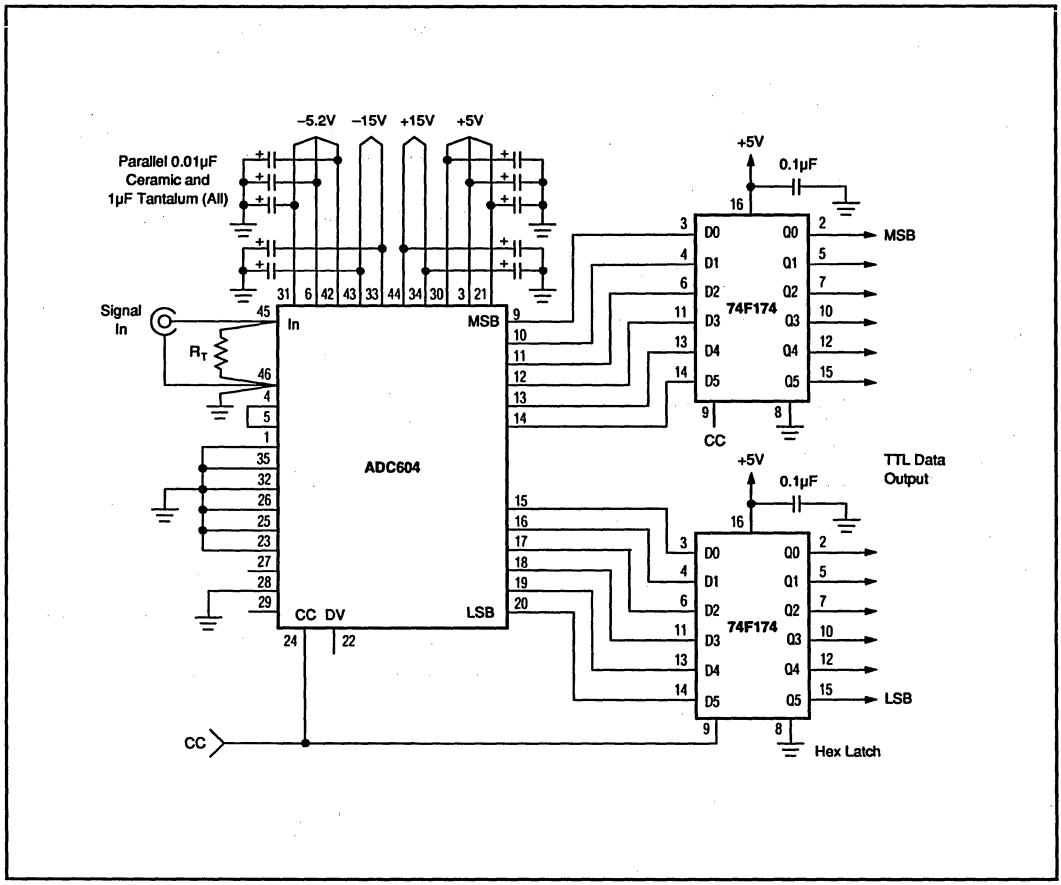


FIGURE 10. Interface Circuit—Digital Output Strobed by Convert Command. Supply connection shown: power supplies and grounds shared by analog and digital pins using common ground plane. (Recommended circuit)

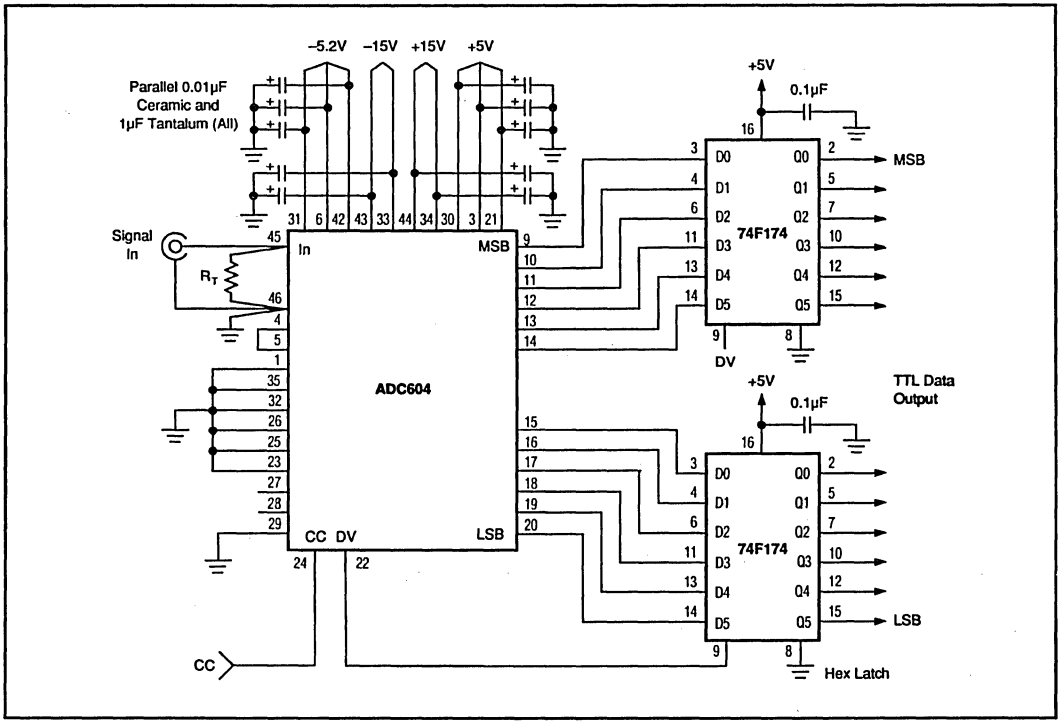


FIGURE 11. Interface Circuit—Digital Output Strobed by Data Valid Pulse. Supply connection shown: power supplies and grounds shared by analog and digital pins, using common ground plane.

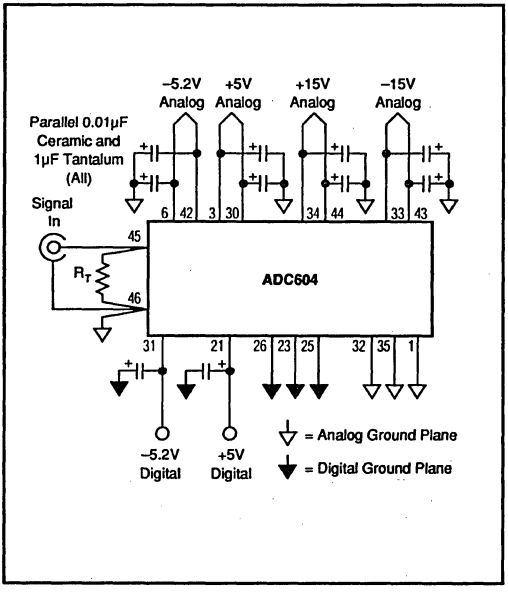


FIGURE 12. Power Supply Connections with Separate Analog and Digital Power Supplies and Ground Planes.

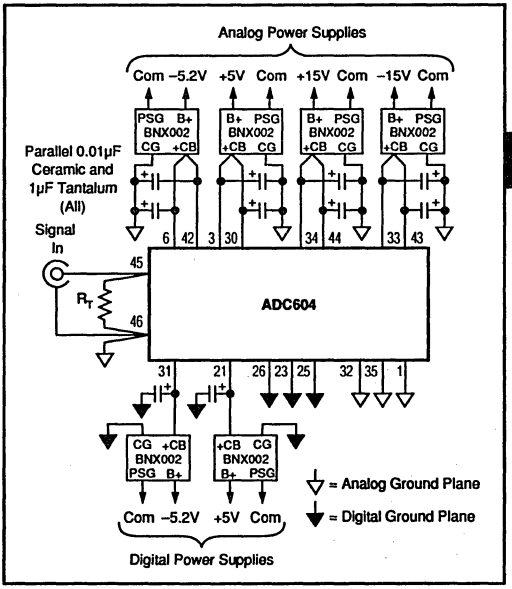
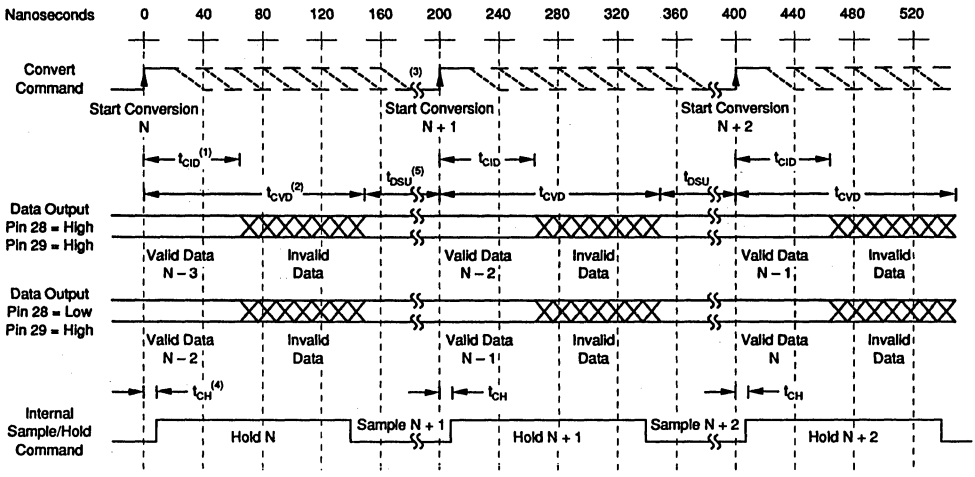
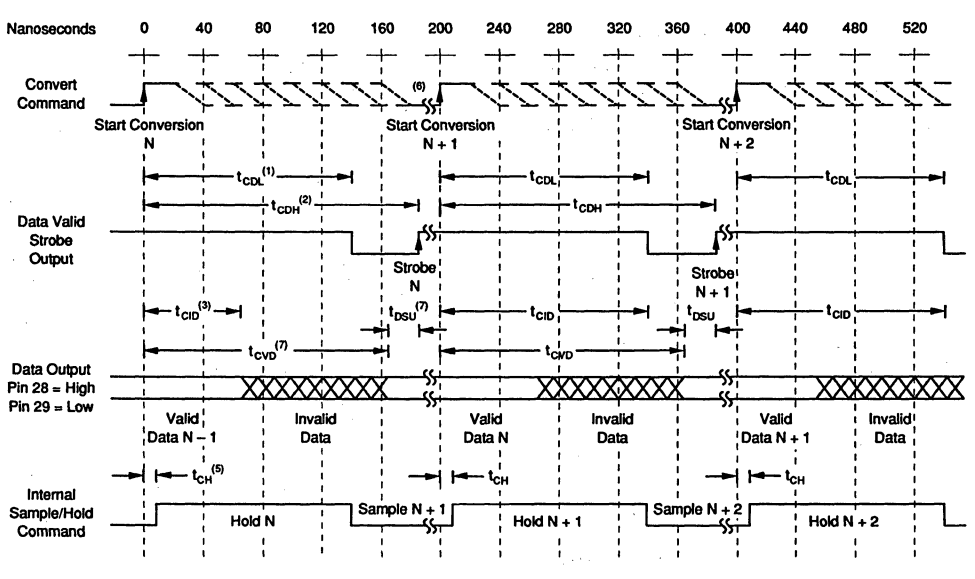


FIGURE 13. Power Supply Connections with Separate Analog and Digital Power Supplies and Ground Planes with Noise Filtering



NOTES: (1) t_{CID} = delay time from Convert Command to Invalid Data. Typical value = 65ns. Independent of conversion rate. (2) t_{CVD} = Delay time from Convert Command to Valid Data. Typical Value = 150ns. Independent of conversion rate. (3) The ⟆ symbol indicates the portion of the waveform that will "stretch out" at lower conversion rates. (4) t_{CH} = delay time from Convert Command to the internal hold command. Typical value = 6ns. Independent of conversion rate. (5) t_{DSU} = data set-up time. This depends on conversion rate and may be calculated by: $t_{DSU} = \frac{1}{f_{SAMPLE}} - t_{CVD}$

FIGURE 14. Convert Command Strobe Timing.



NOTES: (1) t_{CDL} = delay time from Convert Command to the falling edge of Data Valid strobe. Typical value = 140ns. Independent of conversion rate. (2) t_{CDH} = delay time from Convert Command to the rising edge of Data Valid strobe. Typical value = 185ns. Independent of conversion rate. (3) t_{CID} = delay time from Convert Command to Invalid Data. Typical value = 65ns. Independent of conversion rate. (4) t_{CVD} = delay time from Convert Command to Valid Data. Typical Value = 165ns. Independent of conversion rate. (5) t_{CH} = delay time from Convert Command to the internal hold command. Typical value = 6ns. Independent of conversion rate. (6) The ⟆ symbol indicates the portion of the waveform that will "stretch out" at lower conversion rates. (7) t_{DSU} = data setup time. Typical value = 20ns. Independent of conversion rate.

FIGURE 15. Data Valid Strobe Timing.

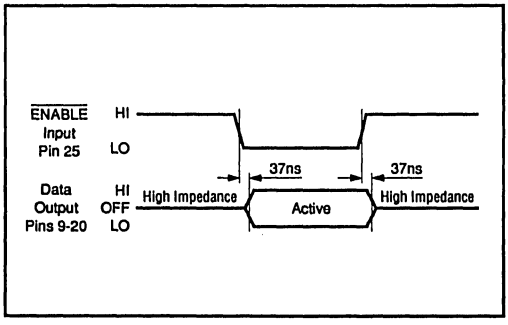


FIGURE 16. Digital Data Tri-State Output.

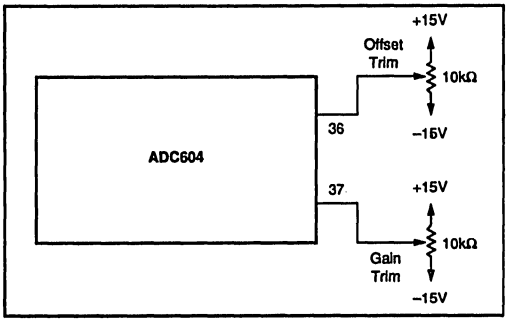


FIGURE 17. Optional Gain and Offset Trim.

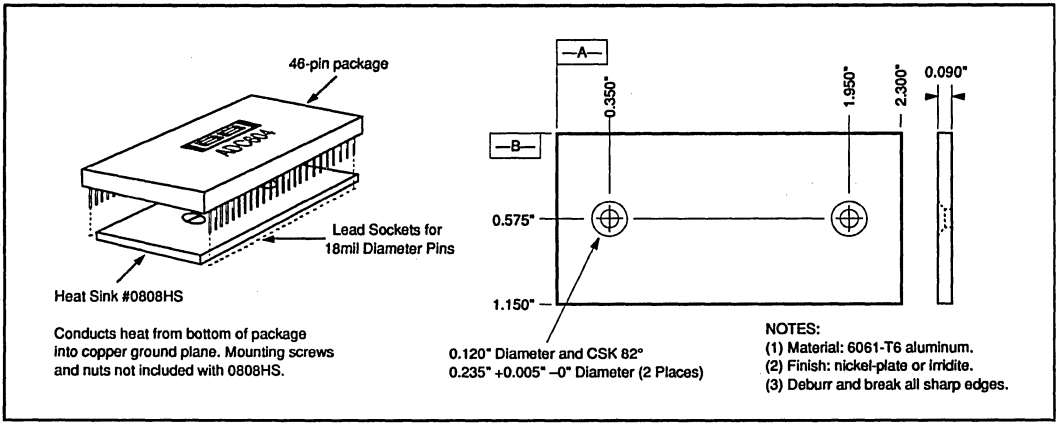


FIGURE 18. Heat Sink Transfers Heat from the DIP Package into a Copper Ground Plane.

BURR-BROWN®

ADC614

ADVANCE INFORMATION
SUBJECT TO CHANGE

14-Bit 5MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- SPURIOUS-FREE DYNAMIC RANGE: 85dB
- SAMPLE RATE: DC to 5MHz
- HIGH SIGNAL/NOISE RATIO: 78dB
- LOW HARMONIC DISTORTION: –85dBc
- LOW INTERMOD. DISTORTION: –85dBc
- COMPLETE SUBSYSTEM: Contains Sample/Hold and Reference
- DIP PACKAGE HYBRID
- 0°C TO +70°C

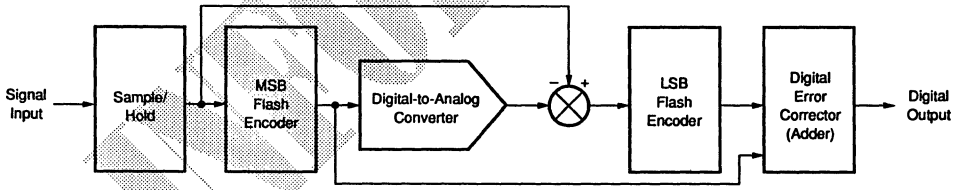
APPLICATIONS

- SIGINT SYSTEMS
- DIGITAL SIGNAL PROCESSING
- RADAR SIGNAL ANALYSIS
- TRANSIENT SIGNAL RECORDING
- FFT SPECTRUM ANALYSIS
- HIGH-SPEED DATA ACQUISITION
- IR IMAGING SYSTEMS
- DIGITAL RECEIVERS

DESCRIPTION

The ADC614 is a high performance analog-to-digital converter capable of digitizing signals at any rate from DC to 5 megasamples per second. Outstanding spurious-free dynamic range has been achieved by minimizing noise and distortion.

The ADC614 is a two-step subranging ADC subsystem containing an ADC, sample/hold amplifier, voltage reference, timing, and error-correction circuitry in a hybrid DIP package. Logic is TTL. Temperature range available: 0°C to +70°C.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1085

SPECIFICATIONS

ELECTRICAL

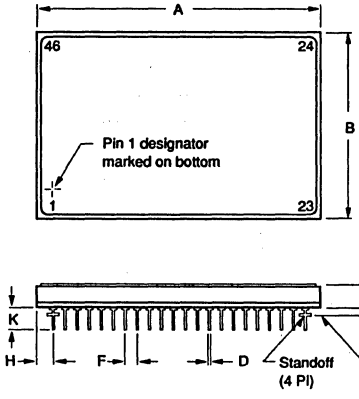
T_C = +25°C, 5MHz sampling rate, R_s = 50Ω, $\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = –5.2V, and 15-minute warmup in convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	ADC614 MIN	ADC614 TYP	ADC614 MAX	UNITS
RESOLUTION				14	Bits
INPUTS					
ANALOG					
Input Range	Full Scale	–1.25		+1.25	V
Input Impedance			1.5		MΩ
Input Capacitance			5		pF
DIGITAL					
Logic Family			TTL Compatible		
Convert Command	Start Conversion		Positive Edge		
Pulse Width	t = Conversion Period	10		t – 20	ns
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error	f = 200Hz		±0.2		%FSR[1]
Input Offset	DC		±0.2		%FSR
Integral Linearity Error	f = 200Hz		±0.5		LSB
Differential Linearity Error	f = 200Hz: 68.3% of All Codes		±0.3		LSB
	99.7% of All Codes		±0.4		LSB
	100% of All Codes		±0.5		LSB
Missing Codes			none		
Power Supply Rejection	$\Delta+V_{CC}$ = ±10%		TBD		%FSR/%
	$\Delta-V_{CC}$ = ±10%		TBD		%FSR/%
	$\Delta-V_{DD1}$ = ±10%		TBD		%FSR/%
	$\Delta-V_{DD2}$ = ±10%		TBD		%FSR/%
CONVERSION CHARACTERISTICS					
Sample Rate		DC		5M	Samples/s
Pipeline Delay			1,2 or 3 Convert Command Periods		
DYNAMIC CHARACTERISTICS					
Differential Linearity Error	f = 2.3MHz: 68.3% of All Codes		±0.4		LSB
	99.7% of All Codes		±0.5		LSB
	100% of All Codes		±0.6		LSB
Total Harmonic Distortion[2]					
f = 2.3MHz (–0.5dB)	f_s = 5MHz		–85		dBc[3]
f = 100kHz			–88		dBc
Two-Tone Intermodulation Distortion[2][4]					
f = 2.3MHz (–6.5dB)	f_s = 5MHz		–85		dBc
f = 2.2MHz (–6.5dB)					dBc
Signal-to-Noise and Distortion (SINAD) Ratio					
f = 2.3MHz (–0.5dB)	f_s = 5MHz		TBD		dB
f = 100kHz (–0.5dB)			TBD		dB
Signal-to-Noise Ratio (SNR)					
f = 2.3MHz (–0.5dB)	f_s = 5MHz		74		dB
f = 100kHz (–0.5dB)			78		dB
Aperture Delay Time			–5		ns
Aperture Jitter			2		ps rms
Analog Input Bandwidth (–3dB)					
Small Signal	–20dB Input		70		MHz
Full Power	0dB Input		40		MHz
Overload Recovery Time	2x Full-Scale Input		TBD		ns
OUTPUTS					
Logic Family			TTL Compatible		
Logic Coding	Logic Selectable		Two's Complement or Inverted Two's Complement		
Logic Levels		+0.8	TTL	+2.4	V
EOC Delay Time	Data Out to DV		TBD		ns
POWER SUPPLY REQUIREMENTS					
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	V
$-V_{CC}$		–14.25	–15	–15.75	V
$+V_{DD1}$		+4.75	+5	+5.25	V
$-V_{DD2}$		–4.95	–5.2	–5.46	V
Supply Currents: $+I_{CC}$	Operating		TBD		mA
$-I_{CC}$			TBD		mA
$+I_{DD1}$			TBD		mA
$-I_{DD2}$			TBD		mA
Power Consumption	Operating		6.5		W

NOTES: (1) FSR: Full-Scale Range = 2.5Vp-p. (2) Units with tested and guaranteed distortion specifications will be available. (3) dBc = level referred to carrier-input signal (= 0dB); F = input frequency; F_s = sampling frequency. (4) IMD is referred to the larger of the two input test signals. If referred to the peak envelope signal (= 0dB), the intermodulation products will be 6dB lower.

MECHANICAL

H Package — Metal and Ceramic



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	2.370	2.420	60.20	61.47
B	1.560	1.610	39.62	40.89
C	.200	.260	5.08	6.60
D	.018 Dia BASIC		0.46 Dia BASIC	
F	.100 BASIC		2.54 BASIC	
H	0.75	.115	1.91	2.92
K	.150	.190	3.81	4.83
L	1.300 BASIC		33.02 BASIC	
M	—	10°	—	10°
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

PIN ASSIGNMENTS

1	Common (Case)	46	Common (Analog)
2	DNC	45	Analog Signal In
3	$+V_{DD1}$ (+5V) Analog	44	$+V_{CC}$ (+15V) Analog
4	S/H Out	43	$-V_{CC}$ (–15V) Analog
5	A/D In	42	NC
6	$-V_{DD2}$ (–5.2V) Analog	41	NC
7	Bit 13	40	NC
8	Bit 14 (LSB)	39	DNC
9	Bit 1 (MSB)	38	DNC
10	Bit 2	37	Gain Adjust
11	Bit 3	36	Offset Adjust
12	Bit 4	35	Common (Analog)
13	Bit 5	34	$+V_{CC}$ (+15V) Analog
14	Bit 6	33	$-V_{CC}$ (–15V) Analog
15	Bit 7	32	Common (Analog)
16	Bit 8	31	$-V_{DD2}$ (–5.2V) Digital
17	Bit 9	30	$+V_{DD1}$ (+5V) Analog
18	Bit 10	29	1 Pipeline Delay Select
19	Bit 11	28	0 Pipeline Delay Select
20	Bit 12	27	Output Logic Invert
21	$+V_{DD1}$ (+5V) Digital	26	Common (Digital)
22	Data Valid Output	25	Tri-State Enable
23	Common (Digital)	24	Convert Command In

ORDERING INFORMATION

ADC614 ( ) H

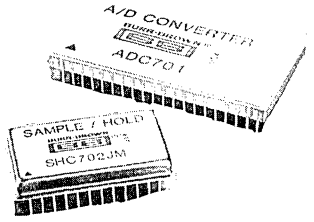
- Basic Model Number
- Performance Grade Code
  - J, K: 0°C to +70°C Case Temperature
- Package Code
  - H: Metal and Ceramic

ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	±16.5V
$+V_{DD1}$	+7V
$\pm V_{DD2}$	–7V
Analog Input	±5V
Logic Input	–0.5V to $+V_{DD1}$
Case Temperature	+125°C
Junction Temperature	+165°C
Storage Temperature	–65°C to +165°C

Stresses above these ratings may permanently damage the device.

BURR-BROWN®



ADC701
SHC702

IMPROVED SPECIFICATIONS
NEW FEATURES

16-Bit 512kHz SAMPLING A/D CONVERTER SYSTEM

FEATURES

- CONVERSION RATE: to 512kHz over temp
- NO MISSING CODES AT 16 BITS
- SPURIOUS-FREE DYNAMIC RANGE: 107dB
- LOW NONLINEARITY: ±0.0015%
- SELECTABLE INPUT RANGES: ±5V, ±10V, 0 to +10V, 0 to +5V, –10V to 0
- LOW POWER DISSIPATION: 2.8W Typical Including Sample/Hold
- METAL AND CERAMIC DIP PACKAGES

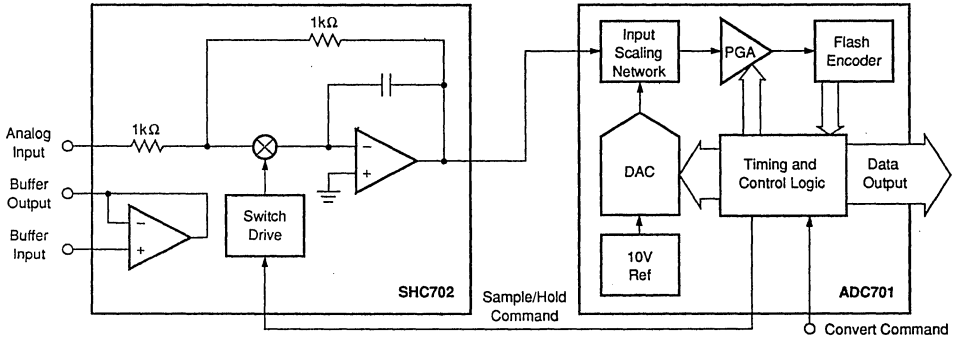
APPLICATIONS

- MEDICAL IMAGING
- SONAR
- PROFESSIONAL AUDIO RECORDING
- AUTOMATIC TEST EQUIPMENT
- HIGH PERFORMANCE FFT SPECTRUM ANALYSIS
- ULTRASOUND SIGNAL PROCESSING
- HIGH SPEED DATA ACQUISITION
- REPLACES DISCRETE MODULAR ADCs

DESCRIPTION

The ADC701 is a very high speed 16-bit analog-to-digital converter based on a three-step subranging architecture. Outstanding dynamic performance is achieved with the SHC702 companion sample/hold amplifier. Both devices use hybrid construction for applications where reliability, small size, and low power consumption are especially important.

Excellent linearity and stability are assured through use of a new ultra-precise monolithic D/A converter and a low-drift reference circuit. Custom monolithic op amps provide very high bandwidth and low noise in all sections of the analog signal path. Logic is CMOS/TTL compatible and is designed for maximum flexibility.



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PDS-877A

SPECIFICATIONS

ELECTRICAL (ADC701 ONLY)

T_A = +25°C, 500kHz sampling rate, $\pm V_{CC}$ = ±15V, $\pm V_{DD1}$ = ±5V, $+V_{DD2}$ = +5V, and five minute warmup in a convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	ADC701JH MIN	ADC701JH TYP	ADC701JH MAX	ADC701KH MIN	ADC701KH TYP	ADC701KH MAX	UNITS
RESOLUTION				16			*	Bits
INPUTS								
ANALOG								
Voltage Ranges	Unipolar			0 to +5, 0 to +10, −10 to 0				V
	Bipolar			±5, ±10				V
Resistance	0 to +5V Range	2.45	2.5	2.55	*	*	*	kΩ
	0 to +10V, −10 to 0, ±5V Ranges	4.9	5	5.1	*	*	*	kΩ
	±10V Range	9.8	10	10.2	*	*	*	kΩ
Capacitance	All Ranges		5			*		pF
DIGITAL								
Logic Family				TTL-Compatible CMOS				
Convert Command	Start Conversion			Rising Edge				
Pulse Width	t = Conversion Period	50		t − 50	*		*	ns
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error[1]	0 to +10V Range		±0.03	±0.1		*	*	%
	±10V Range		±0.03	±0.1		*	*	%
Power Supply Sensitivity of Gain	All Ranges, All Supplies		±0.005	±0.1		*	*	%/V
Input Offset Error[1]	0 to +10V Range		±1	±3		*	*	mV
	±10V Range		±5	±10		*	*	mV
Power Supply Sensitivity of Offset	All Ranges, All Supplies		±0.006	±0.1		*	*	%FSR/V
Integral Linearity Error[2]			±0.002	±0.003		±0.0012	*	%FSR[3]
Differential Linearity Error[2]			±0.0006	±0.0012		*	*	%FSR
No Missing Codes			Guaranteed			Guaranteed		
Noise	$R_{SOURCE} \leq 50\Omega$		0.6			*		LSB rms
CONVERSION CHARACTERISTICS								
Sample Rate	Unadjusted	DC		512	*		*	kHz
Conversion Time[4]	Unadjusted		1.45	1.5		*	*	µs
OUTPUTS								
DIGITAL								
Logic Family				TTL-Compatible CMOS				
Data Coding	Unipolar Ranges			Straight Binary				
	Bipolar Ranges			Offset Binary				
Logic "0" Levels (V_{OL})	$I_{OL} \leq 3.2$mA		0.1	0.4		*	*	V
Logic "1" Levels (V_{OH})	$I_{OH} \leq 80\mu$A	4	4.9		*	*		V
Data Valid Setup Time Before Strobe	Both Edges	28	37		*	*		ns
INTERNAL REFERENCE								
Voltage	$R_{LOAD} \geq 5k\Omega$	+9.995	+10.000	+10.005	*	*	*	V
Current Available to External Loads		2	5		*	*		mA
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		−14.25	−15	−15.75	*	*	*	V
$+V_{DD1}$		+4.75	+5	+5.25	*	*	*	V
$-V_{DD1}$		−4.25	−5	−6	*	*	*	V
$+V_{DD2}$		+4.25	+5	+5.25	*	*	*	V
Supply Currents: $+I_{CC}$	Operating		25	30		*	*	mA
$-I_{CC}$			33	45		*	*	mA
$+I_{DD1}$			45	55		*	*	mA
$-I_{DD1}$			37	50		*	*	mA
$+I_{DD2}$			133	150		*	*	mA
Power Dissipation	Nominal Voltages		1.95	2.3		*	*	W
PERFORMANCE OVER TEMPERATURE								
Specification Temperature Range	T_A Min to T_A Max	+15		+55	0		+70	°C
Gain Error	All Ranges		±10	±15		*	*	ppm/°C
Input Offset Error	All Unipolar Ranges		±1	±5		*	*	ppm FSR/°C
	All Bipolar Ranges		±1	±5		*	*	ppm FSR/°C
Integral Linearity Error[2]			±0.2			*	±0.5	ppm/°C
Differential Linearity Error[2]			±0.05			*	±0.3	ppm/°C
No Missing Codes			Typical			Guaranteed		
Reference Output Drift			±3			*		ppm/°C
Drift of Conversion Time	Unadjusted		+3	+4		*	*	ns/°C
Sample Rate	Unadjusted	DC		512	*		*	kHz

* Same specifications as ADC701JH.

SPECIFICATIONS

ELECTRICAL (SHC702 ONLY)

T_A = +25°C, 500kHz sampling rate, $\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, and five minute warmup in a convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	SHC702JM MIN	SHC702JM TYP	SHC702JM MAX	UNITS
INPUTS (Without Input Buffer)					
ANALOG					
Voltage Range		±10.25	±11		V
Resistance		0.98	1	1.02	kΩ
Capacitance			3		pF
DIGITAL					
Logic Family			LSTTL		
Input Loading			2		LSTTL Loads
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain	$R_{SOURCE} \approx 0\Omega$		−1		V/V
Gain Error	$R_{SOURCE} = 0\Omega$		±0.02	±0.1	%
Linearity Error	Sample Mode		±0.0003		%FSR
Offset Error	Sample Mode		±0.5	±3	mV
Charge Offset (Pedestal) Error	Sample/Hold Mode, $R_{SOURCE} \leq 50\Omega$		±0.5	±5	mV
Droop Rate	Hold Mode		±0.2	±2	µV/µs
Dynamic Nonlinearity	Sample/Hold Mode		±0.0005		%FSR
Power Supply Sensitivity	Offset Plus Charge Offset, All Supplies		±0.003		%FSR/V
DYNAMIC CHARACTERISTICS					
Acquisition Time	10V Step to ±150µV		600		ns
	5V Step to ±150µV		500		ns
Sample-to-Hold Settling Time[5]	to ±150µV		120		ns
Aperture Delay Time			20		ns
Aperture Uncertainty (Jitter)			10	25	ps rms
Slew Rate			150		V/µs
Small Signal Bandwidth	V_{IN} = ±1V		3.1		MHz
Full-Power Bandwidth	V_{IN} = ±10V		2		MHz
Feedthrough Rejection	Hold Mode, 10Vp-p Square Wave Input		0.001		%
OUTPUT					
Voltage Range	$R_{LOAD} \geq 1k\Omega$	±10.25	±11		V
Output Current		±40			mA
Short Circuit Protection	$R_{LOAD} = 0\Omega$		Indefinite		
Output Impedance	DC		0.01	0.1	Ω
INPUT BUFFER CHARACTERISTICS					
INPUT					
Impedance			10^{13} ||3		Ω||pF
Bias Current	V_{IN} = ±10V		±2	±15	pA
Offset Voltage	$R_{SOURCE} \leq 10k\Omega$		±0.3	±1.5	mV
Voltage Range		±10.25	±11		V
DYNAMIC CHARACTERISTICS					
Slew Rate		20	35		V/µs
Full-Power Bandwidth	V_{IN} = ±10V		570		kHz
Settling Time	10V Step to ±150µV		1.7		µs
OUTPUT					
Output Current		±15	±20		mA
Short Circuit Protection	$R_{LOAD} = 0\Omega$		Indefinite		
POWER SUPPLY REQUIREMENTS					
Voltage: $+V_{CC}$	Operating	+13.5	+15	+16.5	V
$-V_{CC}$		−13.5	−15	−16.5	V
$+V_{DD1}$		+4.75	+5	+5.25	V
Current: $+I_{CC}$	Operating		33	40	mA
$-I_{CC}$			18	25	mA
$+I_{DD1}$			5	10	mA
Power Dissipation	Nominal Voltages		790	950	mW
PERFORMANCE OVER TEMPERATURE					
Specification Temperature Range	T_A Min to T_A Max	0		+70	°C
Sample/Hold Gain Error	$R_{SOURCE} = 0\Omega$		±1	±5	ppm/°C
Sample/Hold Offset Error	$R_{SOURCE} \leq 50\Omega$		±10	±30	µV/°C
Sample/Hold Charge Offset Error	$R_{SOURCE} \leq 50\Omega$		±10	±80	µV/°C
Droop Rate				±50	µV/µs
Buffer Offset Error	$R_{SOURCE} \leq 10k\Omega$		±3	±15	µV/C

NOTES: (1) Adjustable to zero. Tested and guaranteed for 0 to +10V and ±10V ranges only. (2) Peak-to-peak based on 99.9% of all codes. (3) FSR means full-scale range and depends on the input range selected. (4) ADC conversion time is defined as the time that the Sample/Hold must remain in the Hold mode; i.e., the duration of the Sample/Hold command. This time must be added to the Sample/Hold acqusition time to obtain the total system throughput time. (5) Given for reference only — this time overlaps with the ADC701 conversion time and does not affect system throughput rate.

SPECIFICATIONS

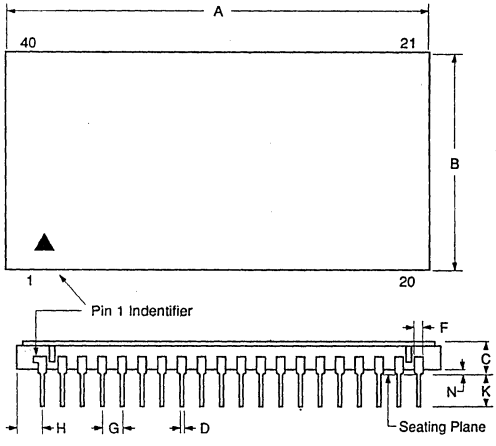
ELECTRICAL (COMBINED ADC701/SHC702)

T_A= +25°C, 500kHz sampling rate, $\pm V_{CC}$= ±15V, $\pm V_{DD1}$= ±5V, $+V_{DD2}$= +5V, and five minute warmup in a convection environment, ±5V input range unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Sample Rate	Unadjusted	DC		512	kHz
Dynamic Nonlinearity			±0.002		%FSR
Total Harmonic Distortion (THD)	f_{IN} = 20kHz (–0.3dB)		0.00068		%
	f_{IN} = 199kHz (–0.2dB)		0.0078		%
Spurious-Free Dynamic Range (SFDR)	f_{IN} = 20 kHz (–0.3dB)		107.1		dB
	f_{IN} = 199kHz (–12dB)		93.8		dB
Two-Tone Intermodulation Distortion (IMD)	f_1 = 195kHz (–6.5dB), f_2 = 200kHz (–6.5dB)		–81.4		dBC
	f_1 = 195kHz (–12.5dB), f_2 = 200kHz (–12.5dB)		–86.2		dBC
Signal-to-Noise-Ratio (SNR)	f_{IN} = 5kHz (–0.5dB)		93		dB
Total Power Dissipation	Operating		2.8	3.25	W

ADC701 MECHANICAL

H Package— Metal and Ceramic



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.075	2.115	52.71	53.72
B	1.080	1.100	27.43	27.94
C	.145	.175	3.68	4.45
D	.018 TYP		0.46 TYP	
F	.040 TYP		1.02 TYP	
G	.100 TYP		2.54 TYP	
H	.093	.103	2.36	2.62
J	.020 BASIC		0.51 BASIC	
K	.205 BASIC		5.21 BASIC	
L	.900 BASIC		22.86 BASIC	
N	.015	.035	0.38	0.89

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

ADC701 PIN ASSIGNMENTS

1	Bit 1/9 (Bit 1 = MSB)	40	$-V_{DD1}$ (–5V) Analog
2	Bit 2/10	39	Common (Analog)
3	Bit 3/11	38	$+V_{DD1}$ (+5V) Analog
4	Bit 4/12	37	Reference (Gain) Adjust
5	Bit 5/13	36	+10V Reference Output[2]
6	Bit 6/14	35	Common (Reference)
7	Bit 7/15	34	DNC
8	Bit 8/16	33	Common (Analog)
9	Clip Detect Output	32	+10V Reference Input[2]
10	$+V_{DD2}$ (+5V) Digital	31	Input D [1]
11	Common (Digital)	30	Input C [1]
12	Data Strobe	29	Common (Signal)
13	High/Low Byte Select	28	Input B [1]
14	Convert Command	27	Input A [1]
15	Sample/Hold Control[3]	26	$-V_{CC}$ (–15V) Analog
16	Common (Digital)	25	Common (Power)
17	Common (Digital)	24	$+V_{CC}$ (+15V) Analog
18	Clock Adjust	23	DNC[4]
19	Common (Digital)	22	Offset Adjust
20	$+V_{DD2}$ (+5V) Digital	21	Offset Adjust

NOTES: (1) Refer to Input Connection Table. (2) Reference Input is normally connected to Reference Output, unless an external 10V reference is used. (3) Sample/Hold Control goes high to activate Hold mode. (4) DNC = Do Not Connect.

ADC701 ORDERING INFORMATION

ADC701 ( ) H

Basic Model Number

Performance Grade Code
- K: 0°C to +70°C Ambient Temperature
- J: +15°C to +55°C Ambient Temperature

Package Code
- H: Metal and Ceramic

ADC701 ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	±18V
$\pm V_{DD1}$, $+V_{DD2}$	±7V, +7V
Analog Input	$\pm V_{CC}$
Logic Input	–0.5V to ($+V_{DD2}$ + 0.3V)
Logic Output	±25mA
Case Temperature	+150°C
Junction Temperature	+165°C
Storage Temperature	–65°C to +165°C
Power Dissipation	3W

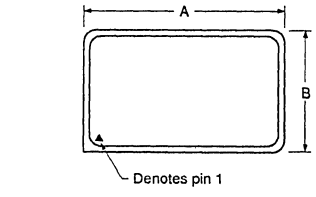
Stresses above these ratings may permanently damage the device.

ADC701 OUTPUT CODING

INPUT LEVEL (Exact Center of Code)	NOMINAL INPUT VOLTAGE TO ADC701 (Multiply by –1 for SHC702 Input Voltage) 0–10V RANGE (1LSB = 153µV)	±10V RANGE (1LSB = 305µV	±5V RANGE (1LSB = 153µV)	OUTPUT CODE (1 = Logic High) MSB LSB	CLIP DETECT
Underrange	< –76µV	< –10.000153V	< –5.000076V	0000 0000 0000 0000	1
–FS	0V	–10V	–5V	0000 0000 0000 0000	0
–FS + 1LSB	+153µV	–9.999695V	–4.999847V	0000 0000 0000 0001	0
–3/4FS	+1.25V	–7.5V	–3.75V	0010 0000 0000 0000	0
–1/2FS	+2.5V	–5V	–2.5V	0100 0000 0000 0000	0
–1/4FS	+3.75V	–2.5V	–1.25V	0110 0000 0000 0000	0
–1LSB	+4.999847V	–305µV	–153µV	0111 1111 1111 1111	0
Mid-Scale	+5V	0V	0V	1000 0000 0000 0000	0
+1LSB	+5.000153V	+305µV	+153µV	1000 0000 0000 0001	0
+1/4FS	+6.25V	+2.5V	+1.25V	1010 0000 0000 0000	0
+1/2FS	+7.5V	+5V	+2.5V	1100 0000 0000 0000	0
+3/4FS	+8.75V	+7.5V	+3.75V	1110 0000 0000 0000	0
+FS –2LSB	+9.999695V	+9.99939V	+4.999695V	1111 1111 1111 1110	0
+FS – 1LSB	+9.999847V	+9.999695V	+4.999847V	1111 1111 1111 1111	0
Overrange	> +9.999924V	> +9.999847V	> +4.999924V	1111 1111 1111 1111	1

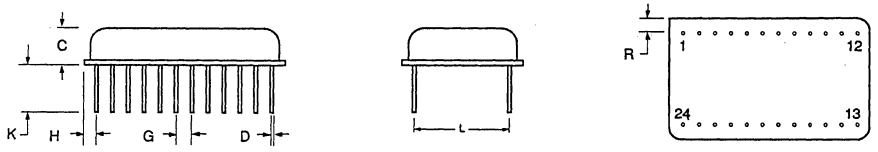
SHC702 MECHANICAL

M Package— Metal



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.365	1.385	34.67	35.18
B	.79	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin material and plating composition conform to method 2003 (solderability of MIL-STD-883 (except paragraph 3.2)



SHC702 PIN ASSIGNMENTS

1	Sample/Hold Output	24	$+V_{CC}$ (+15V) Analog
2	NC[3]	23	Common (Power)
3	NC	22	$-V_{CC}$ (–15V) Analog
4	NC	21	Common (Analog)
5	NC	20	NC
6	NC	19	NC
7	NC	18	NC
8	NC	17	Buffer Amp Input[2]
9	$+V_{DD1}$ (+5V) Analog	16	NC
10	Common (Digital)	15	Common (Signal)
11	Hold Input[1]	14	Buffer Amp Output
12	Hold Input[1]	13	Analog Input

NOTES: (1) Hold mode is activated only when pin 12 is low and pin 11 is high. For normal use with ADC701, pin 12 is grounded and pin 11 is connected to ADC701 Sample/Hold control (ADC701 pin 15). (2) If the buffer amp is not used, pin 17 should be grounded. (3) NC = No Internal Connection.

SHC702 ORDERING INFORMATION

SHC702 J M

Basic Model Number

Performance Grade Code
J: 0°C to +70°C Ambient Temperature

Package Code
M: Metal

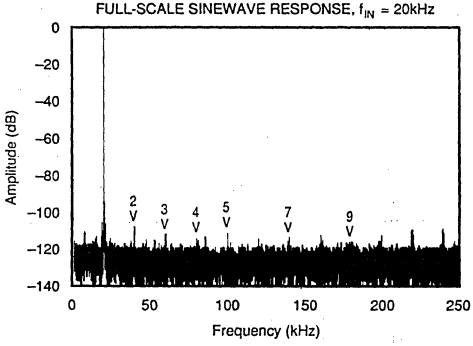
SHC702 ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	±18V
$+V_{DD1}$	+7V
Analog and Buffer Inputs	$\pm V_{CC}$
Outputs	Indefinite Short to Common
Logic Inputs	–0.5V to ($+V_{DD1}$ + 0.3V)
Case Temperature	+150°C
Junction Temperature	+165°C
Storage Temperature	–65°C to +165°C
Power Dissipation	1.5W

Stresses above these ratings may permanently damage the device.

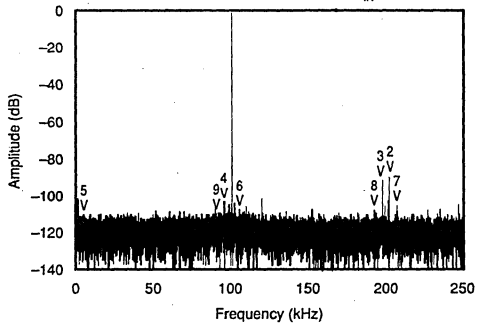
TYPICAL DYNAMIC PERFORMANCE (ADC701/SHC702)

FULL-SCALE SINEWAVE RESPONSE, f_{IN} = 20kHz



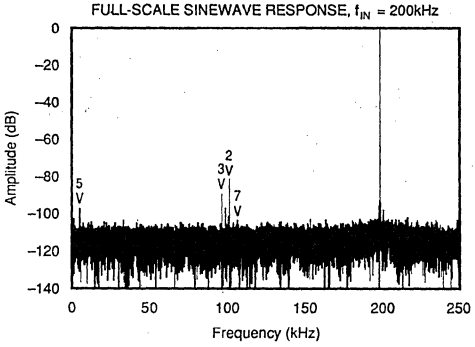
Input Frequency	19.9890136719 kHz		
Fundamental	–0.3 dB	4th Harmonic	–115.6 dB
2nd Harmonic	–107.5 dB	5th Harmonic	–111.2 dB
3rd Harmonic	–111.5 dB	6th Harmonic	–124.5 dB

FULL-SCALE SINEWAVE RESPONSE, f_{IN} = 100kHz



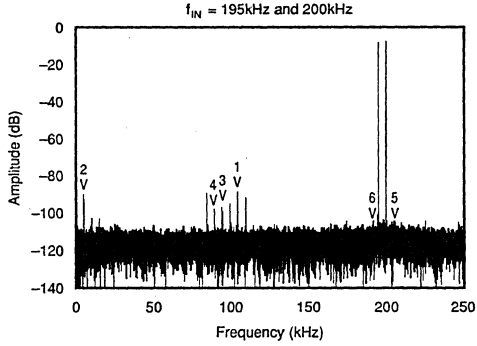
Input Frequency	199.005126953 kHz		
Fundamental	–0.7 dB	4th Harmonic	–111.5 dB
2nd Harmonic	–81.4 dB	5th Harmonic	–97.0 dB
3rd Harmonic	–89.4 dB	6th Harmonic	–112.5 dB

FULL-SCALE SINEWAVE RESPONSE, f_{IN} = 200kHz



Input Frequency	100.982666016 kHz		
Fundamental	–0.5 dB	4th Harmonic	–102.5 dB
2nd Harmonic	–89.1 dB	5th Harmonic	–110.2 dB
3rd Harmonic	–90.5 dB	6th Harmonic	–106.8 dB

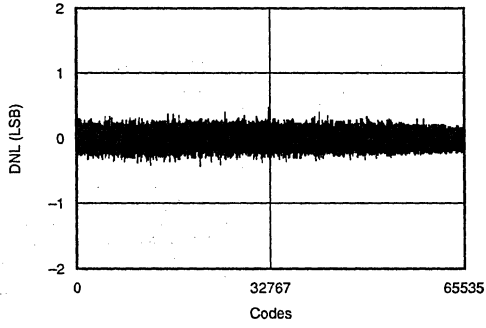
TWO-TONE INTERMODULATION RESPONSE, f_{IN} = 195kHz and 200kHz



	Frequency 1	194.976806641 kHz	
	Frequency 2	199.981689453 kHz	
f_1	–6.8 dB	3> f_1+2f_2	–96.0 dB
f_2	–6.3 dB	4> $2f_1+f_2$	–96.8 dB
1> f_1+f_2	–87.7 dB	5> f_1-2f_2	–104.9 dB
2> f_1-f_2	–88.8 dB	6> $2f_1-f_2$	–109.0 dB

NOTE: For figures above, sampling rate = 500.0000000000kHz. 16,384 point FFT, non-windowed. Noise floor limited by synthesized generators.

DIFFERENTIAL NONLINEARITY OF ALL CODES, 19.6 MILLION SAMPLES



THEORY OF OPERATION

The ADC701 uses a three-step subranging architecture, meaning that the analog-to-digital conversion is performed in three passes which constitute coarse, medium and fine approximations of the input signal. Refer to Figures 1 and 2 for simplified block diagrams of the system.

Before the input signal is presented to the ADC, it must be sampled with high linearity and low aperture error by the sample/hold amplifier.

In the SHC702, the sampling switch is placed at the summing junction (virtual ground) of a high speed FET amplifier (Figure 1). This arrangement maintains constant charge injection independent of the signal amplitude, which is critically important for good linearity performance. The sampling switch itself is a high speed DMOS FET whose gate is driven from a fast-slewing control signal, thus minimizing the time aperture between the fully closed (sample mode) and the fully open (hold mode) states of the switch. The signal voltage is held across the feedback capacitor, forcing the op-amp to maintain a constant output voltage for the duration of the A/D conversion. Feedthrough from the input, already low due to the MOSFET's low capacitance, is further reduced by clamping the summing point to ground with another FET.

The ADC701 input voltage is converted to a current through the input scaling resistors (Figure 2), and this current is applied to the summing junction (virtual ground) of error amplifier A_1. The current output of the DAC (0 to 2mA) is also applied to the summing point. If bipolar operation is selected, the 10V reference output is applied to input D, creating a 1mA offset current which sums with the input current.

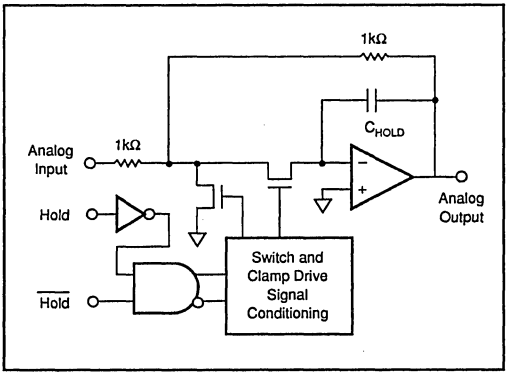


FIGURE 1. Simplified Block Diagram of the SHC702.

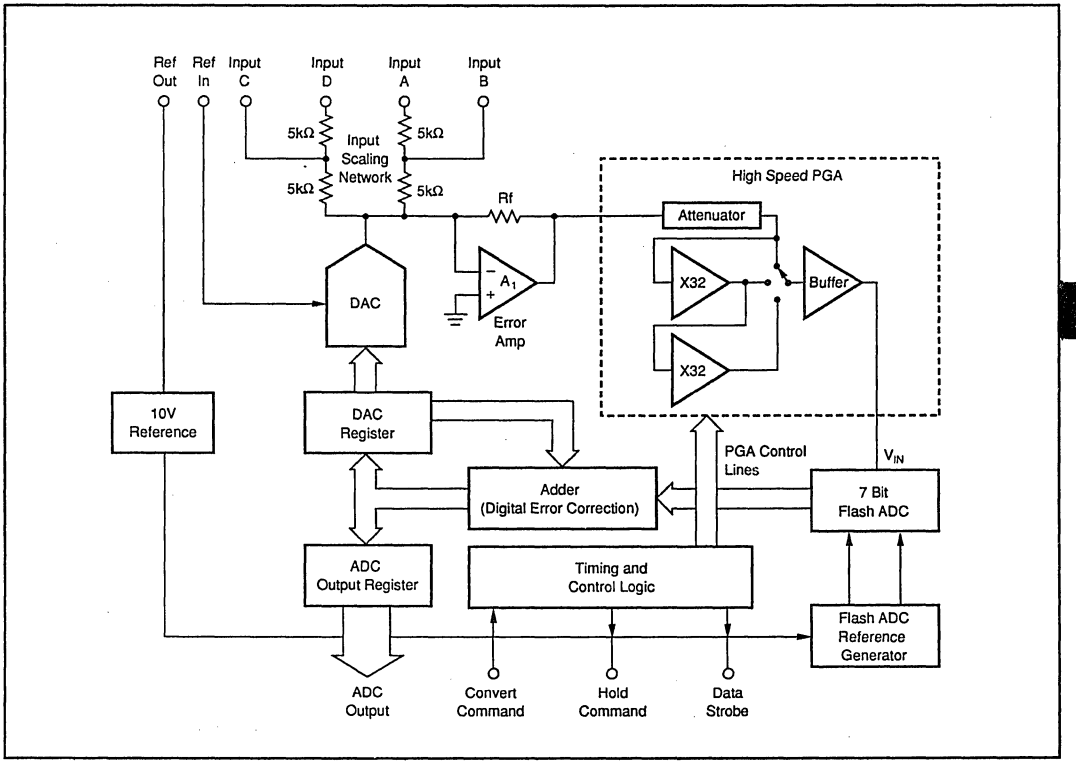


FIGURE 2. Simplified Block Diagram of the ADC701.

At the beginning of each conversion, the DAC is reset to mid-scale so that its output current is exactly 1mA. This 1mA is subtracted from the input signal current. The difference current flows through Rf and appears as an error voltage at the output of A_1.

During the first pass, the programmable gain amplifier (PGA) is set to unity gain, which matches the error voltage range to the input range of the flash ADC. The error signal is digitized to 7-bit resolution by the flash ADC, creating a coarse approximation of the digital output value, which is then applied to the DAC.

Since the DAC output is now approximately equal to the input signal current, the remaining difference current flowing through Rf is small—ideally less than 1/128 of full scale, which is due to the built-in quantizing uncertainty of the 7-bit flash ADC. However, other sources of error (e.g., integral and differential nonlinearity of the flash ADC, gain and offset of the PGA, settling and noise errors throughout the signal path) cause the possible error range to be significantly greater. In fact, the ADC701 is designed to handle remainder signals up to 1/32 of full scale, which is four times the "ideal" value.

Therefore, the PGA is set during the second pass to a gain of 32, allowing the small remainder signal to match the full range of the flash ADC. This is again digitized to 7-bit resolution and added to the previous result to create the "medium" approximation of the input signal. Because the full-scale range of the flash represents 1/32 of the input signal's full range, the 7-bit flash output is shifted right by 5 bits before being added to the original 7-bit "coarse" result, creating a 12-bit word. There is an overlap of two bits because the two least significant bits of the first-pass result correspond to the two most significant bits of the second-pass result. This overlap in the adder is called "digital error correction"—the mechanism that allows nonideal remainders from the first pass to be corrected in the second pass.

The 12-bit approximation is applied once again to the DAC, causing the remaining difference current to become yet smaller. For the third pass, the PGA's gain is increased by another factor of 32, and the remainder is again digitized by the flash ADC.

At this point in the conversion, all of the necessary data has been latched and it is no longer necessary to hold the analog signals from the sample/hold or the DAC. From a systems perspective, the conversion is now complete because the sample/hold is released to begin acquiring the next input sample and the DAC is reset to mid-scale for the next conversion. Meanwhile, the final result from the flash is added to the previous 12-bit result. Again there is a two-bit overlap to allow for error correction. The adder output is monitored to prevent a digital "rollover" condition, so that the ADC clips properly at the signal extremes. The upper sixteen bits of the final adder result are stored in the ADC's output register, ready to be presented in byte-sequential form at the eight output data lines. The overrange or "clip" condition can also be detected externally by monitoring pin 9. Refer to the section on ADC701 Digital I/O for further detail.

INSTALLATION AND OPERATING INSTRUCTIONS

The ADC701/SHC702 combination is designed to be easy to use in a wide variety of applications, without sacrificing flexibility of the analog and digital interface.

SHC702 INTERFACE

The connection diagram (Figure 3) shows the basic hookup. At the SHC702 input, the user may opt to connect the built-in FET buffer amplifier. The buffer is most useful in multi-channel applications where the signal bandwidth is less than 100kHz. In those applications, it serves to isolate the multiplexer output from the 1kΩ input impedance of the sample/hold. For higher frequency applications and for any system that does not require the very high impedance, the best results (lowest noise and distortion) will be achieved by driving the SHC702's analog input directly. If the buffer is not used, its input should be grounded to avoid random noise pickup and saturation of the buffer op-amp.

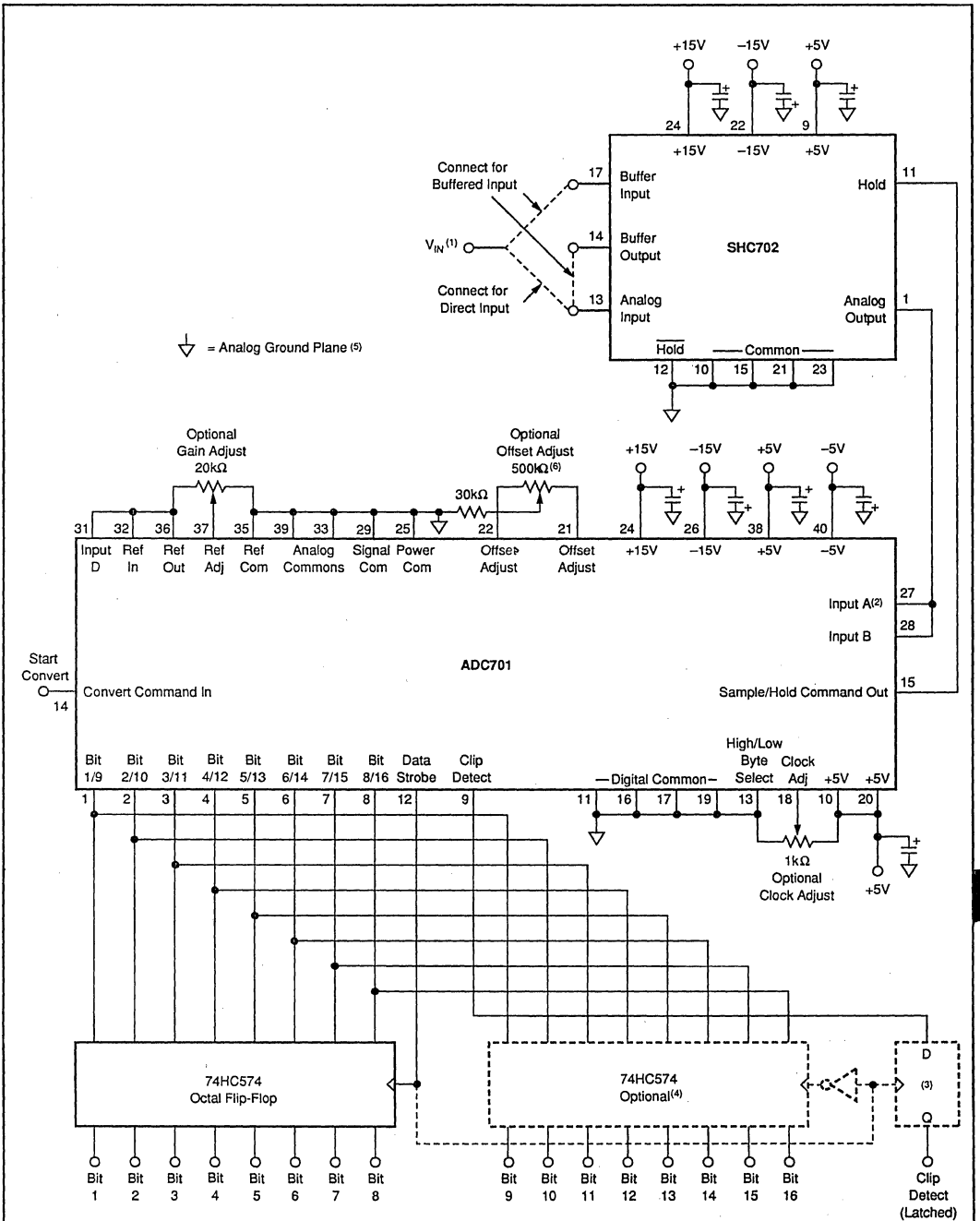
Only two connections are required between the SHC702 and the ADC701: SHC702 analog output to ADC701 input(s) and the digital Hold Command from the ADC701 to the SHC702. As always, it is best to avoid routing these analog and digital lines along parallel traces. Although the placement of the SHC702 relative to the ADC is not extremely critical, one good approach is to mount the SHC along one end of the ADC package as shown in Figure 4. This minimizes the length of the interconnections and keeps the digital lines well away from sensitive analog signals.

ADC701 INPUT CONNECTIONS

The ADC input network has four separate terminals, allowing many different input ranges. These should be connected as indicated in Table I. Most users will take advantage of the ADC701's built-in reference circuit, which has very low noise and excellent temperature stability. To use the internal reference, it is only necessary to connect pin 36 (Reference Output) to pin 32 (Reference Input). To use an external 10V reference (to cause the ADC gain to track a system reference, for example), pin 36 is left unconnected and the external reference is applied to pin 32. If required, the ADC701 will typically accommodate a five to ten percent variation in the 10V reference. External references should have very low noise to avoid degrading the excellent signal-to-noise ratio (SNR) of the ADC701.

INPUT RANGE	CONNECT V_{IN} TO	CONNECT Ref In TO
0 to +10V	Input A and Input D	—
±10V	Input A	Input D
±5V	Input A and Input B	Input D
−10V to 0	Input A and Input B	Input C and Input D
0 to +5V	Input B and Input C	—

TABLE I. ADC701 Input Connection Table.



NOTES: (1) For lowest distortion at high input frequencies the non-buffered option should be used. If the buffer is not used, its input should be grounded. (2) Shown connected for ±5V input range. Refer to Input Connection Table for other options. (3) If the Clip Detect feature is used, then the signal may be latched with a simple D type flip-flop as shown. See the section on ADC701 Digital I/O for additional applications information. (4) The second octal flip-flop is recommended but optional — it provides added digital signal isolation and buffering, and also permits three-state logic output compatibility. (5) All commons should be connected to the analog ground plane. Refer to the section on "Power and Ground Connections." (6) The Offset Adjust circuit shown provides an adjustment range of approximately ±0.25% FSR.

FIGURE 3. ADC701/SHC702 Connection Diagram.

OFFSET, GAIN AND CONVERSION SPEED ADJUSTMENTS (OPTIONAL)

Adjustment of the reference voltage is the most straightforward way to adjust the ADC gain. For the internal reference, this is accomplished by connecting a 20kΩ potentiometer as shown in Figure 3. This will provide a gain trim range of about ±3%. It is also possible to use external series or parallel resistance in the input network, but that is more cumbersome and usually will degrade the gain stability over temperature due to tempco (temperature coefficient) mismatches among the resistors.

ADC offset may be adjusted by connecting a 500kΩ potentiometer to pins 21 and 22, with the wiper connected through a series 30kΩ resistor to ground as shown in Figure 3. This will provide an offset trim range of approximately ±0.25% FSR. For a larger trim range of offset or gain, it is recommended that trims be accomplished elsewhere in the system.

The Clock Adjust input (pin 18) is intended primarily for small adjustments of the conversion time. However, this will rarely be necessary because the ADC701 is guaranteed to convert up to 512kHz over the specified temperature range without external clock adjustment.

POWER AND GROUND CONNECTIONS

Experience with testing and applying the ADC701 shows that it will perform well in most board layouts, provided that appropriate care is taken with grounding and bypassing.

Power supplies may be shared between the ADC701, SHC702 and other analog circuitry without difficulty. It is recommended that each power pin be locally bypassed to the ground plane with a high quality tantalum capacitor of at least 1µF. If at all possible, power should be derived from well-regulated linear supplies—switching power supplies will require much more effort for proper decoupling and are not recommended for this or any high performance wideband analog system.

The +5V Digital supply pins, though not as sensitive to noise as the +5V Analog pin, should nonetheless be kept as quiet as possible. If the system digital supply is noisy, then it is best to use the system +5V analog supply for all of the +5V connections on the ADC701 and SHC702 rather than trying to separate them. If only one +5V supply is available and it is shared with other system logic, then extra bypassing and/or supply filtering may be required.

The –5V supply will operate with any voltage between –4.75 and –6V. If –5V is not available from the system supplies, then an industry-standard 7905 regulator may be used to derive –5V from the –15V supply.

All ground pins on both the ADC701 and the SHC702 should be connected directly to a common ground plane. This is true for both analog and digital grounds. However, it is also helpful to recognize where the digital ground currents flow in the system, and to provide PC board return paths for potentially troublesome digital currents in addition to the ground plane connections. For example, the ADC701 output data lines will sink current (statically and/or dynamically) when in the low state. This current comes from the power supply that runs the interface logic, and so must return to that supply's ground. If the ground termination is placed such that this digital current will flow away from the ADC701, then the existing ground plane will suffice to carry the current. On the other hand, if the ground termination must be placed such that the digital current flows across the ADC or SHC layout, then it would be advisable to break the analog ground plane under the package (to stop the flow of current across the package) and to provide a separate trace (several centimeters wide) on another PC board layer to carry the digital return current from pins 11 and 19 to the termination point. If the ADC701 must interface into a fairly noisy digital environment, then another approach is to keep the first layer of latches and/or buffers connected to the ADC701 power and ground planes, so that the ADC itself is connected to "quiet" circuits with short return paths. This transfers the interface problem to the outputs of the latches, where it can be managed with less impact on the analog components.

PHYSICAL INSTALLATION

The packages may be soldered directly into a PC board or mounted in low-profile machined pin sockets with good results. Use of tall (long lead length) sockets, adapters or headers is not recommended unless a local ground plane and bypass capacitors can be mounted directly under the packages.

In a room-temperature environment or inside an enclosure with moderate airflow, the ADC701 and SHC702 normally do not require heat-sinking. However, to keep the devices running as cool as possible, it is helpful to install a thin heat-transfer plate under the packages to conduct heat into the ground plane. The plate may be made from metal (copper, aluminum or steel) or from a special heat-conductive material such as Sil-Pad(1). The Sil-Pad material has the advantage of being electrically insulating and somewhat pliable, so that it will tend to distribute pressure evenly and conform to the package—an advantage in systems where the board may be flexed or subjected to vibration.

PC BOARD LAYOUT EXAMPLE

Figure 4 is an example of a printed circuit layout that integrates the ADC701 and SHC702 into a four-layer PC board. The layout shown includes jumper options to set the ADC input range, and shows placement of the optional offset and gain adjust potentiometers. Note that the ground plane layer is on the component (top) side, which shields the components from digital signals on other layers and provides the possibility of using a simple heat sink plate as described above.

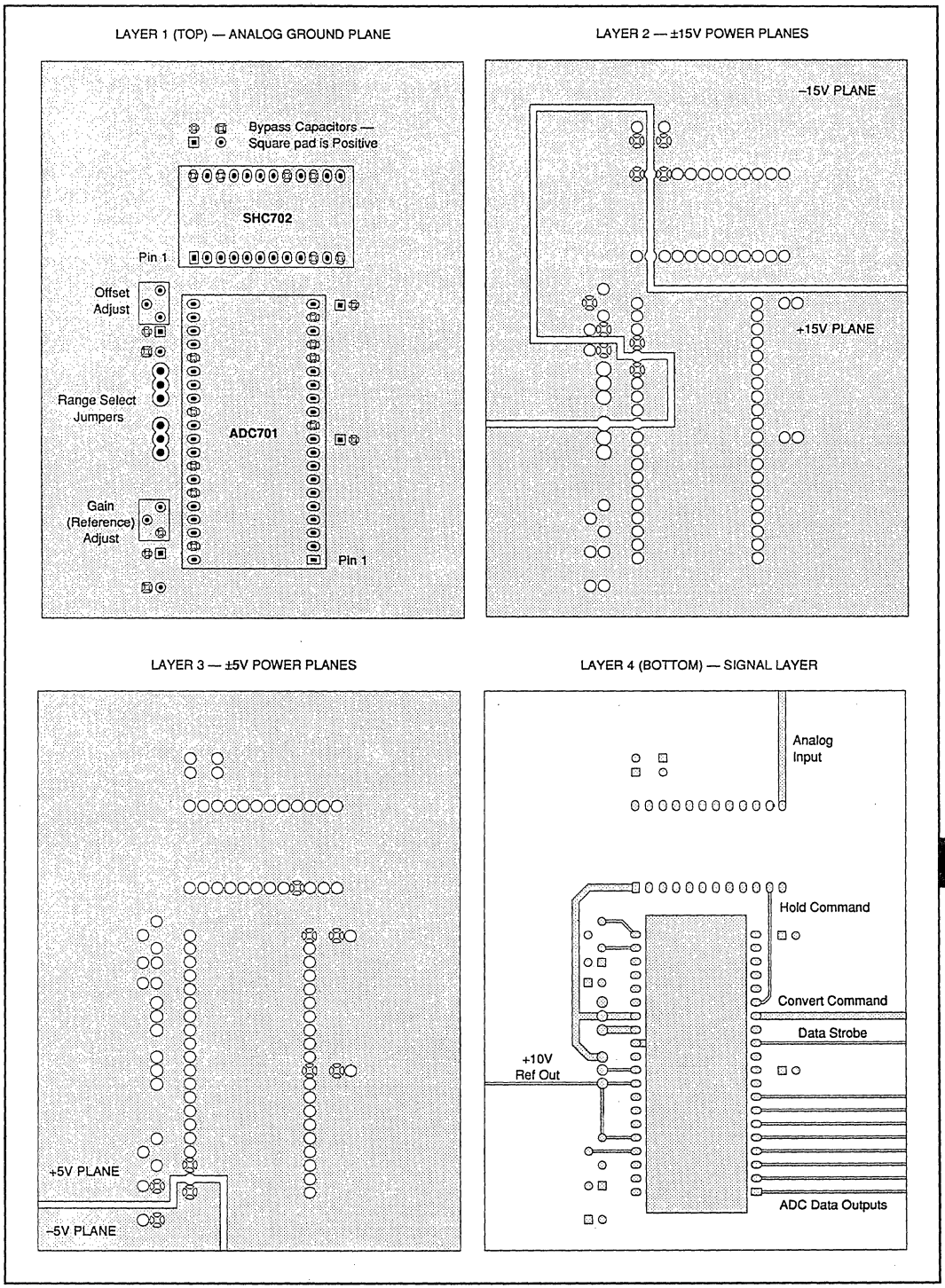


FIGURE 4. Example of Four-Layer PC Board Layout.

ADC701 DIGITAL I/O

Refer to the timing diagram, Figure 5. The conversion process is initiated by a rising edge on the Convert Command input. This will immediately bring the sample/hold command output to a logic high state (Hold mode).

After the ADC701 conversion is completed (approximately 1.5µs after the convert command edge), the Sample/Hold Command falls to a low state, enabling the sample/hold to begin acquisition of the next input sample. However, the ADC701 internal clock continues to run so that the output data may be processed.

There are two methods of reading data from the ADC:

1. Strobed Output—This will usually be the easiest and fastest method. The data are presented sequentially as high and low bytes of the total 16-bit word. The sequence High-Low or Low-High is controlled by the state of the High/Low Byte Select input. The first byte is valid on the rising edge of the Data Strobe output; the second byte is valid on the falling edge.
2. Polled output—With this method, data strobes will occur as described above, but they are ignored by the user. Instead, the user waits until the Data Strobe output falls, and then manually selects high and low output data by means of the High/Low Byte Select input. This polling procedure may be carried out during the subsequent ADC conversion cycle, but two precautions must be observed: First, the user should avoid switching the High/Low Byte Select immediately before or after the next convert command. This will prevent digital switching noise from coupling into the system at the instant of analog sampling. Second, the polling sequence must be completed before the ADC begins to strobe out data from the subsequent conversion.

OPTIONS FOR STROBED OUTPUT

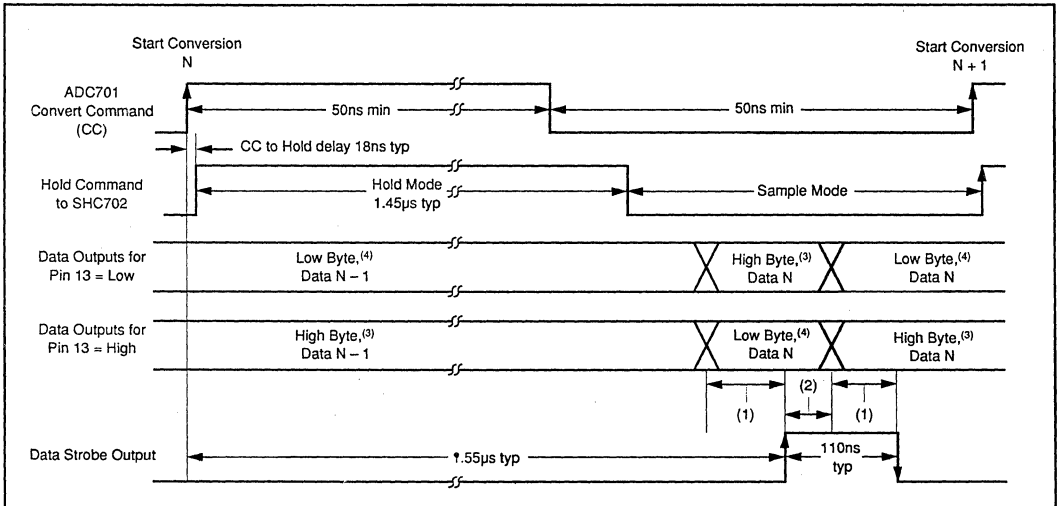
There are several ways in practice to implement the logic interface. Figure 3 shows the simplest configurations. In order to convert the ADC701's byte-sequential data into 16-bit parallel form, the minimum requirement is for one single octal flip-flop, such as a 74HC574 or equivalent. This will latch the first byte on the rising edge of the ADC701 Data Strobe. Then the second byte becomes valid, and all 16 bits may be strobed to the outside system on the falling edge of the Data Strobe.

For better noise isolation of the ADC701 from the digital system, or if full three-state capability is required for the 16 output lines, a second octal flip-flop can be added as shown in the dashed lines of Figure 3. This will also require an inverter to convert the falling Data Strobe edge into a rising clock edge for the second flip-flop IC.

If it is desirable to have all 16 output lines change simultaneously (for example when driving a D/A converter), then a third octal flip-flop (not shown in Figure 3) may be added to re-latch the output of the first byte. By driving that device's clock also from the inverted Data Strobe, fully synchronous switching of the 16 output bits will be achieved.

USING THE CLIP DETECT OUTPUT

The ADC701 provides a built-in Clip Detect signal on pin 9 which indicates an ADC overrange or underrange condition. The Clip Detect signal is only valid when the High Byte becomes valid as shown in Figure 5. Therefore, the simplest way to latch the Clip Detect signal is to provide an extra flip-flop which is clocked on the same strobe edge as the High Byte flip-flop. Such a setup is illustrated in Figure 3. The Clip Detect signal remains at logic 0 under normal conditions, and indicates a clip condition by rising to a logic 1.



NOTES: (1) Setup Time 28ns min, 37ns typ. (2) Hold Time 30ns min, 73ns typ. (3) High Byte refers to ADC bits 1–8, the most significant 8 bits. Also, the Clip Detect signal on pin 9 is valid simultaneously with High Byte. (4) Low Byte refers to ADC bits 9–16, the least significant bits.

FIGURE 5. ADC701 Interface Timing Diagram.

The latched version of Clip Detect may be used to generate an interrupt to the user's system computer, which would then launch a service routine to generate the appropriate alarms or corrective action. Another possible application would be to stretch the pulse using a monostable so that it would be easily visible when driving an LED warning lamp.

In some systems, it may be desirable to provide separate latched outputs for Underrange and Overrange. These conditions may be separately detected by using simple logic to implement the boolean equations:

$$\text{Underrange} = \text{Clip Detect AND } \overline{\text{Anybit}}$$

$$\text{Overrange} = \text{Clip Detect AND Anybit}$$

where "Anybit" is any one of the data output bits.

The Underrange and Overrange signals would then be latched into two separate flip-flops. A simple solution using a single '74 dual flip-flop and a single '00 quad NAND provides enough logic to implement the logic equations, with a spare NAND gate left over to use for creating the inverted Data Strobe signal.

USING THE ADC701 AT MAXIMUM CONVERSION RATES

The ADC701 is guaranteed to accept Convert commands at a rate of DC to 512kHz over the specified operating temperature range. At a conversion rate of 500kHz, the total throughput time of 2µs allows for the 1.5µs ADC conversion time plus 500ns for the digital output timing and sample/hold acquisition time.

If the user tries to exceed the maximum conversion rate by a large amount, the Convert Command of conversion N+1 will occur before the Data Strobe has fallen from conversion N. In such a situation, the ADC701 will simply ignore every other Convert command so the actual conversion rate will become half of the Convert command rate. Otherwise, the conversion will proceed normally. Note that the ADC timing slows down at high temperatures, so the frequency at which this occurs will vary with temperature—although it is still guaranteed to be greater than 512kHz over the specified temperature range.

Another consideration for operation at very high rates is that the sample/hold acquisition time becomes shorter as the conversion rate is increased. Users will note that the available acquisition time becomes less than 550ns at rates above 500kHz, which is less than the typical SHC702 acquisition time for a 10V step to 150µV accuracy. However, the signal degradation is gradual as the acquisition time is shortened—even at 512kHz, there is enough time to acquire a 5V step to better than 500µV. Also, most signal processing environments do not contain full-power signals at the Nyquist frequency, but rather show a rolloff of signal power at high frequencies. If the ability to acquire extremely large input changes at extremely high conversion rates is of paramount importance, the user may elect to use a Burr-Brown model SHC803 sample/hold instead—it is pin compatible with the SHC702 and provides much faster acquisition time at the expense of some extra noise and higher distortion at low input frequencies.

TESTING THE ADC701/SHC702

The ADC701 and SHC702 together form a very high performance converter system and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a Fast Fourier Transform (FFT) to the ADC digital output is the best method of examining total system performance. Attempts to evaluate the system by analog reconstruction through a D/A converter will usually prove unsatisfactory; assuming that the static and dynamic distortions of the D/A can be brought below the required level (–110dB), the performance will still be beyond the range of presently available spectrum analyzers.

Even when the analysis is done using FFT techniques, several key issues must be addressed. First, the parameters of the FFT need to be adequate to perform the analysis and extract meaningful data. Second, the proper selection of test frequencies is critical for good results. Third, the limitations of commercial signal generators must be considered. These three points are addressed in later sections. Finally, the test board layout must follow the recommendations discussed on pages 8 through 10.

DYNAMIC PERFORMANCE DEFINITIONS

1. Total Harmonic Distortion (THD):

$$10 \log \frac{\text{Harmonic Power (first 9 harmonics)}}{\text{Sinewave Signal Power}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

3. Intermodulation Distortion (IMD):

$$10 \log \frac{\text{IMD Product Power (RMS sum; to 3rd order)}}{\text{Sinewave Signal Power}}$$

4. Spurious-Free Dynamic Range (SFDR):

$$10 \log \frac{\text{Power of Peak Spurious Component}}{\text{Sinewave Signal Power}}$$

IMD is referred to the larger of the test signals f_1 or f_2—**not** to the total signal power, which would result in a number approximately 6dB "better." The zero frequency bin (DC) is not included in these calculations—it represents total offset of the ADC, SHC and test equipment and is of little importance in dynamic signal processing applications.

FFT Parameters

Accurate FFT analysis of 16-bit systems requires adequate computing hardware and software. The FFT length (number of points) should be relatively large—at least 4K and preferably 16K or larger. There are several reasons for this:

1. The converter itself has 64K codes. Ideally, the test would guarantee that all codes are tested at least once. Practically

speaking, however, that would require immensely long FFTs (>>64K points) or averaging of a large number of smaller FFTs. By using an FFT length of 4K or greater and proper selection of the test frequencies, a very good statistical picture of the ADC performance will be obtained which shows the effect of any defects in the transfer function.

2. The noise floor of the output spectrum is not low enough if less than 4K points are taken. Shorter FFTs have fewer bins to cover the output spectrum, so a larger fraction of the total system noise appears in each bin. Although the SNR of the ADC701/SCH702 system is in the range of –93dB, the noise level of the available generators may increase the total measured noise power to –80dB. Every doubling of the FFT length will spread the noise power among twice as many bins, resulting in a 3dB reduction of the spectral noise floor. In order to resolve spurious components that are at the level of –110dB, an average noise floor of less than –113dB would be barely adequate. This requires at least 2048 bins in the output half-spectrum, corresponding to a 4K-point FFT. Even at this level, it will be difficult or impossible to separate higher order harmonics in the ADC701 response from the average noise level, indicating that longer FFTs are desirable.
3. Following the guidelines for test frequency selection which are outlined in the next section, it becomes clear that longer FFTs allow a much wider choice of test frequencies without concern for sophisticated data windowing or code coverage problems.

Besides the consideration of FFT length, it is important to realize that the FFT calculations must be performed with high-precision arithmetic. The use of 32-bit fixed or floating point calculations will generally be inadequate because the noise floor due to calculation errors alone will interfere with the ADC performance data. Unfortunately, this consideration precludes the use of most DSP accelerator boards and similar hardware. In order to preserve the full dynamic range of the ADC output, it is best to use standard 64- or 80-bit arithmetic. To avoid excessively long calculation times, the FFT algorithm should be written in an efficiently compiled language and make use of techniques such as trigonometric look-up tables in software and dedicated floating-point coprocessors in hardware. There are several commercial software packages available from Burr-Brown and others that meet these requirements.

SELECTION OF TEST FREQUENCIES

The FFT (and any similar DSP operation) treats the total time-domain record length as one cycle of an infinitely long periodic signal. Therefore, if the end of the sampled record does not match up smoothly with the beginning, the output spectrum will contain serious errors known as leakage or truncation error[2]. This well-known problem is usually handled by applying a windowing function to the time-domain samples, suppressing the worst effects of the mismatch. However, the most often used windows such as Hanning, Hamming, raised cosine, etc., are completely inadequate for 16-bit ADC testing. More sophisticated functions such as the four-sample Blackman-Harris window[3] will provide much better results, although there still will be obvious spreading of the spectral lines.

The most successful approach is to eliminate the need for windowing by properly selecting the test signal frequency (or frequencies) in relation to the ADC sampling frequency[4]. If the time sample contains exactly an integer number of cycles, then there is no mismatch or truncation error. Another point to consider is that the sampling frequency should not be an exact integer multiple of the signal frequency, which would tend to reduce the number of different ADC codes that are tested and also tend to artificially concentrate quantization error in the harmonics of the test signal.

Both of these criteria are met by choosing an FFT length which is a power of two (the most standard and fastest to compute) and choosing a test frequency which causes an exact **odd** integer number of cycles to appear in the time record. In software, this selection can be accomplished very easily:

1. Determine the desired sampling frequency f_S.
2. Determine the desired input signal frequency f_{APPROX}.
3. Determine the FFT length N, which should be a power of 2 (e.g., 4096 or 16384).
4. Divide f_{APPROX} by f_S, multiply the quotient by N, and round the result to the nearest odd integer. This is M, the number of cycles in the time record.
5. Multiply M by f_S and divide by N to obtain the exact input signal frequency f_{ACTUAL}.

SIGNAL GENERATOR CONSIDERATIONS

To suppress leakage effects, the calculated ratio of f_S to f_{ACTUAL} must be precisely maintained during the test. This requirement is met easily by the use of synthesized signal generators whose reference oscillators can be locked together. Other possible approaches include external phase locking of non-synthesized generators and direct digital synthesis techniques. If it is not possible to use phase-locked signals, then a Blackman-Harris window may be used as mentioned previously.

Another key issue is the purity of both the signal and sampling frequency generators. The sampling clock's phase noise (jitter) will act as another source of SNR degradation. This is not serious as long as the jitter is random and the noise sidebands contain no sharp peaks. The HP3325 synthesizer is suitable for this purpose. The input signal generator will require more attention because its distortion will usually be greater than that of the ADC701/SHC702. Presently, the lowest distortion synthesized generator is the Brüel & Kjær Model 1051 (or 1049). This is suitable for testing the system in the audio range. The upper frequency limit of the B&K synthesizer is 200kHz. Above 20kHz, the distortion becomes a limiting factor, and low-pass filters must be inserted into the signal path to reduce the harmonic and spurious content.

As noted previously, the combined noise contributions of the signal generator and sampling clock generator far exceed the SNR of the ADC701/SHC702 itself. The SNR has been measured separately by applying a highly filtered sinewave to the input, resulting in typical SNR performance of –93dB. However, the filters employed to achieve this low-noise test stimulus are found to cause reactive loading of the signal source which results in increased distortion. Therefore it is best to separate the tests for SNR from those for THD and IMD, unless a suitably pure **and** low-noise signal can be generated.

Figures 6 and 7 show block diagrams of FFT test setups for the ADC701 and SHC702, summarizing the placement of the major components discussed above. The Typical Dynamic Performance section shows typical results obtained from testing the ADC701/SHC702 at a 500kHz conversion rate, using 16K samples for the FFT analysis.

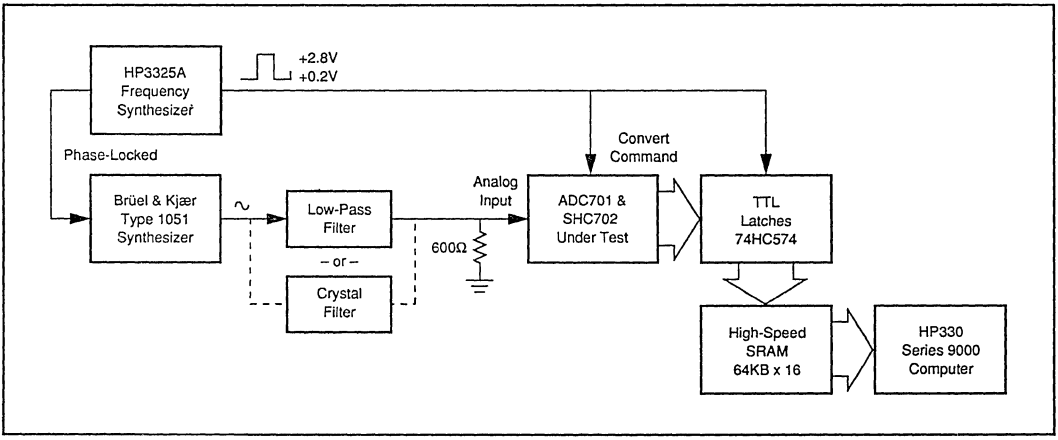


FIGURE 6. FFT Test Configuration for Single-Tone Testing.

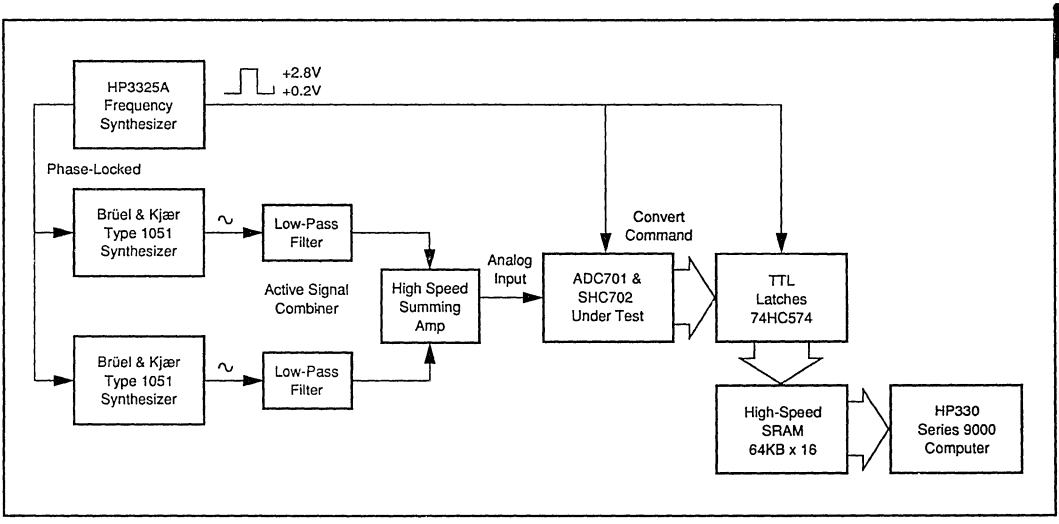


FIGURE 7. FFT Test Configuration for Two-Tone (Intermodulation) Testing.

HISTOGRAM TESTING

The FFT provides an excellent measure of harmonic and intermodulation distortion. Low-order spurious products are primarily caused by integral nonlinearity of the SHC and ADC. The influence of differential linearity errors is harder to distinguish in a spectral plot—it may show up as high-order harmonics or as very minor variations in the overall appearance of the noise floor.

A more direct method of examining the differential linearity (DL) performance is by using the popular histogram test method [5]. Application of the histogram test to the ADC701/SHC702 is relatively straightforward, though once again extra precision is required for a 16-bit system compared to 8- or 12-bit systems. Basically, this means that a very large number of samples are required to build an accurate statistical picture of each code width. If a histogram is taken using only one million points, then the average number of samples per code is less than fifteen. This is inadequate for good statistical confidence, and the resulting DL plot will look considerably worse than the actual performance of the converter. In practice 10 to 20 million samples will demonstrate good results for a 16-bit system and expose any serious flaws in the DL performance. If the memory incrementing hardware can keep pace with the ADC701, then 20 million samples can be accumulated in well under one minute. The last figure on page six shows the results of a 19.6 million point histogram taken at an input frequency of 1kHz.

NOTES:

1. Available from Bergquist, 5300 Edina Industrial Blvd., Minneapolis, MN 55435 (612) 835-2322.
2. Brigham, E. Oran, *The Fast Fourier Transform*, Englewood Cliffs, N.J.: Prentice-Hall, 1974.
3. Harris, Fredric J., "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform", *Proceedings of the IEEE*, Vol. 66, No. 1, January 1978, pp 51-83.
4. Halbert, Joel M. and Belcher, R. Allan, "Selection of Test Signals for DSP-Based Testing of Digital Audio Systems", Journal of the Audio Engineering Society, Vol. 34, No. 7/8, July/August, 1986, pp 546-555.
5. "Dynamic Tests for A/D Converter Performance", Application Note AN-133, Burr-Brown Corporation, Tucson, AZ, 1985.

BURR-BROWN®

ADC7802

Autocalibrating, 4-Channel, 12-Bit ANALOG-TO-DIGITAL CONVERTER

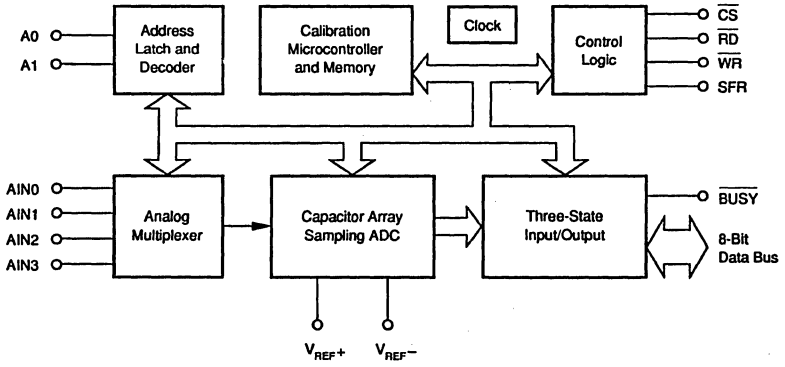
FEATURES

- TOTAL UNADJUSTED ERROR ≤1/2LSB OVER FULL TEMPERATURE RANGE
- FOUR-CHANNEL INPUT MULTIPLEXER
- LOW POWER: 10mW plus Power Down Mode
- SINGLE SUPPLY: +5V
- FAST CONVERSION TIME: 8.5µs Including Acquisition
- AUTOCAL: No Offset or Gain Adjust Required
- UNIPOLAR INPUTS: 0V to 5V
- MICROPROCESSOR-COMPATIBLE INTERFACE
- INTERNAL SAMPLE/HOLD

DESCRIPTION

The ADC7802 is a monolithic CMOS 12-bit A/D converter with internal sample/hold and four-channel multiplexer. An autocalibration cycle, occurring automatically at power on, guarantees a total unadjusted error within ±1/2LSB over the specified temperature range, eliminating the need for offset or gain adjustment. The 5V single-supply requirements and standard $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ control signals make the part very easy to use in microprocessor applications. Conversion results are available in two bytes through an 8-bit three-state output bus.

The ADC7802 is available in a 28-pin plastic DIP and 28-lead PLCC, fully specified for operation over the industrial –40°C to +85°C temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1050A

SPECIFICATIONS

ELECTRICAL

$V_A = V_D = V_{REF}+ = 5V \pm 5\%$; $V_A \geq V_D \geq V_{REF}+$; $V_{REF}- = AGND = DGND = 0V$; CLK = 2MHz external with 50% duty cycle, $T_A = -40°C$ to $+85°C$, after calibration cycle at any temperature; unless otherwise specified.

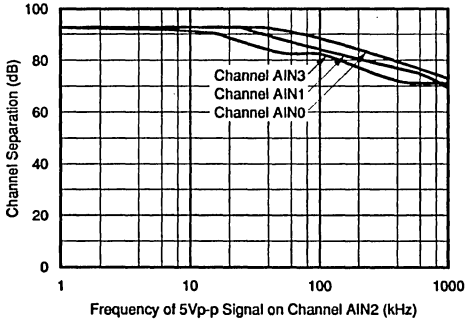
PARAMETER	CONDITIONS	ADC7802BP/ADC7802BN MIN	TYP	MAX	UNITS
RESOLUTION				12	Bits
ANALOG INPUT					
Voltage Input Range	$V_{REF}+ = 5V$, $V_{REF}- = 0V$	0		5	V
Input Capacitance			50		pF
On State Bias Current			100		nA
Off State Bias Current	$T_A = 25°C$			10	nA
	$T_A = -40°C$ to $+85°C$			100	nA
On Resistance Multiplexer			2		kΩ
Off Resistance Multiplexer			10		MΩ
Channel Separation	500Hz		92		dB
REFERENCE INPUT					
For Specified Performance: $V_{REF}+$	$V_{REF}+ \leq V_A$		5		V
$V_{REF}-$			0		V
For Derated Performance: [1] $V_{REF}+$		2.5		V_A	V
$V_{REF}-$		0		1	V
Input Reference Current	$V_{REF}+ = 5V$, $V_{REF}- = 0V$		10	100	µA
THROUGHPUT TIMING					
Conversion Time With External Clock (Including	CLK = 2MHz, 50% Duty Cycle			8.5	µs
Multiplexer Settling Time and Acquisition Time)	CLK = 1MHz, 50% Duty Cycle			17	µs
	CLK = 500kHz, 50% Duty Cycle			34	µs
With Internal Clock Using	$T_A = +25°C$			10	µs
Recommended Clock Components	$T_A = -40°C$ to $+85°C$		10		µs
Analog Signal Bandwidth [2]			500		Hz
Slew Rate [2]		8			mV/µs
Multiplexer Settling Time to 0.01%			460		ns
Multiplexer Access Time				20	ns
ACCURACY					
Total Adjusted Error,[3] All Channels				±1/2	LSB
Differential Nonlinearity				±1/2	LSB
No Missing Codes			Guaranteed		
Gain Error	All Channels			±1/4	LSB
Gain Error Drift	Between Calibration Cycles		±0.2		ppm/°C
Offset Error	All Channels			±1/4	LSB
Offset Error Drift	Between Calibration Cycles		±0.2		ppm/°C
Channel-to-Channel Mismatch				±1/4	LSB
Power Supply Sensitivity	$V_A = V_D = 4.75V$ to $5.25V$		±1/8		LSB
DIGITAL INPUTS					
All Pins Other Than CLK: V_{IL}				0.8	V
V_{IH}		2.4			V
Input Current	$T_A = +25°C$, $V_{IN} = 0$ to V_D			1	µA
	$T_A = -40°C$ to $+85°C$, $V_{IN} = 0$ to V_D			10	µA
CLK Input: V_{IL}				0.8	V
V_{IH}		3.5			V
I_{IL}				10	µA
I_{IH}				1.5	mA
I_{IH}	Power Down Mode (D3 in SFR HIGH)			100	nA
DIGITAL OUTPUTS					
V_{OL}	$I_{SINK} = 1.6mA$			0.4	V
V_{OH}	$I_{SOURCE} = 200µA$	4			V
Leakage Current	High-Z State, $V_{OUT} = 0V$ to V_D			±1	µA
Output Capacitance	High-Z State		4	15	pF
POWER SUPPLIES					
Supply Voltage for Specified Performance: V_A		4.75	5	5.25	V
V_D	$V_A \geq V_D$	4.75	5	5.25	V
Supply Current: I_A			1	2.5	mA
I_D	Logic Input Pins HIGH or LOW		1	2	mA
Power Dissipation	$\overline{WR} = \overline{RD} = \overline{CS} = \overline{BUSY}$ = HIGH		10		mW
Power Down Mode	See Table III, Page 9		50		µW
TEMPERATURE RANGE					
Specification		–40		+85	°C
Storage		–65		+150	°C

NOTES: (1) For $(V_{REF}+) - (V_{REF}-)$ as low as 2.5V, the total error will typically not exceed ±1LSB. (2) Faster signals can be accurately converted by using an external sample/hold in front of the ADC7802. (3) After calibration cycle, without external adjustment. Includes gain (full scale) error, offset error, integral nonlinearity, differential nonlinearity, and drift.

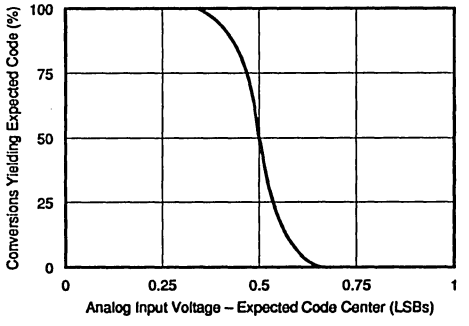
TYPICAL PERFORMANCE CURVES

$V_A = V_D = V_{REF}+ = 5V$, $V_{REF}- = AGND = 0V$, $T_A = +25°C$, unless otherwise specified.

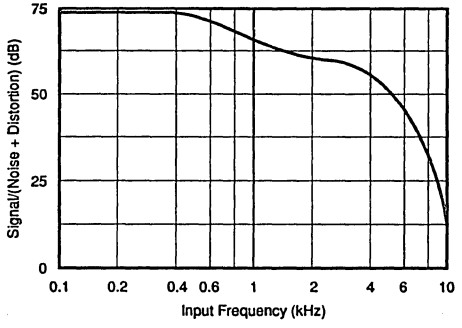
CHANNEL SEPARATION vs FREQUENCY



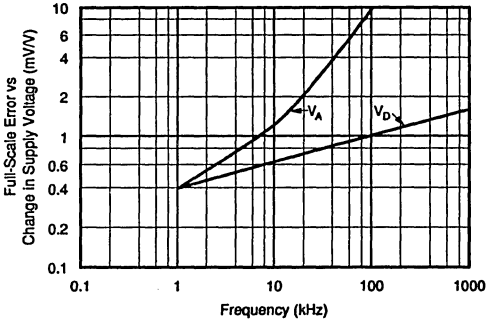
CODE TRANSITION NOISE



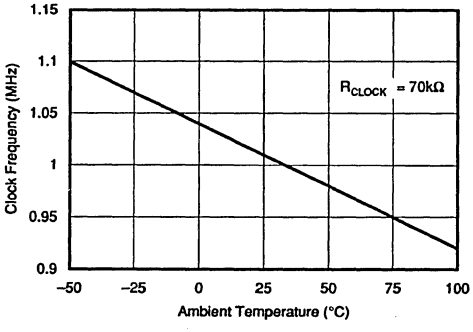
SIGNAL/(NOISE + DISTORTION) vs INPUT FREQUENCY



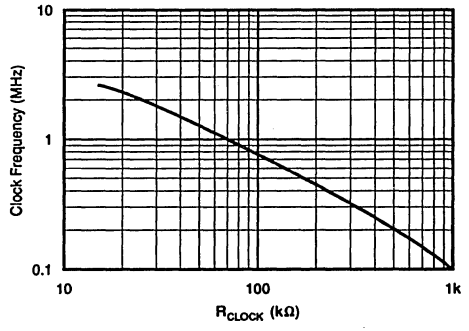
POWER SUPPLY REJECTION vs FREQUENCY



INTERNAL CLOCK FREQUENCY vs TEMPERATURE



INTERNAL CLOCK FREQUENCY vs R_{CLOCK}

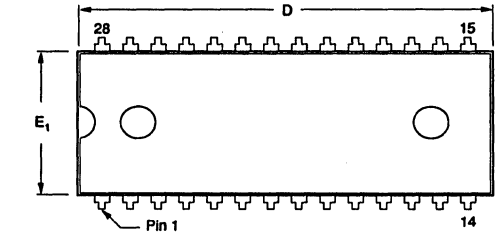


ORDERING INFORMATION

MODEL	MAXIMUM TOTAL ERROR, LSB	SPECIFICATION TEMPERATURE RANGE, °C	PACKAGE
ADC7802BN	±1/2	–40 to +85	PLCC
ADC7802BP	±1/2	–40 to +85	Plastic DIP

MECHANICAL

P Package — 28-Pin Plastic DIP

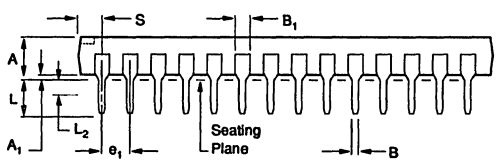


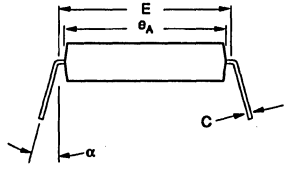
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A(1)	.169	.200	4.29	5.08
A1 (1)	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D(1)	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1 (1)	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
Q1	.020	.070	0.51	1.78
S1	.040	.080	1.02	2.03

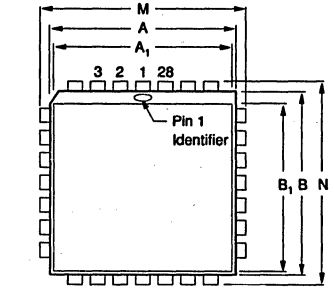
(1) Not JEDEC Standard.

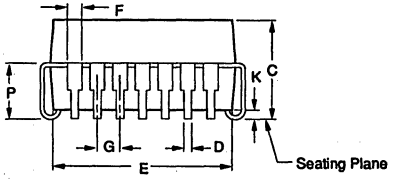
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.





N Package — 28-Pin Plastic LCC





DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.450	0.460	11.43	11.68
A1	0.450	0.460	11.43	11.68
B	0.450	0.460	11.43	11.68
B1	0.450	0.460	11.43	11.68
C	0.165	0.180	4.19	4.57
D	0.013	0.023	0.33	0.58
E	0.390	0.430	9.91	10.92
F	0.026	0.032	0.66	0.81
G	0.50 BASIC		1.27 BASIC	
K	0.015	0.025	0.38	0.64
M	0.485	0.495	12.32	12.57
N	0.485	0.495	12.32	12.57
P	0.100	0.110	2.54	2.79

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

ABSOLUTE MAXIMUM RATINGS

V_A to Analog Ground	6.5V
V_D to Digital Ground	6.5V
Pin V_A to Pin V_D	±0.3V
Analog Ground to Digital Ground	±1V
Control Inputs to Digital Ground	−0.3V to V_D + 0.3V
Analog Input Voltage to Analog Ground	−0.3V to V_D + 0.3V
Maximum Junction Temperature	150°C
Internal Power Dissipation	875mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}: Plastic DIP	75°C/W
PLCC	75°C/W

THEORY OF OPERATION

ADC7802 uses the advantages of advanced CMOS technology (logic density, stable capacitors, precision analog switches, and iow power consumption) to provide a precise 12-bit analog-to-digital converter with on-chip sampling and four-channel analog-input multiplexer.

The input stage consists of an analog multiplexer with an address latch to select from four input channels.

The converter stage consists of an advanced successive approximation architecture using charge redistribution on a capacitor network to digitize the input signal. A temperature-stabilized differential auto-zeroing circuit is used to minimize offset errors in the comparator. This allows offset errors to be corrected during the acquisition phase of each conversion cycle.

Linearity errors in the binary weighted main capacitor network are corrected using a capacitor trim network and correction factors stored in on-chip memory. The correction terms are calculated by a microcontroller during a calibration cycle, initiated either by power-up or by applying an external calibration signal at any time. During conversion, the correct trim capacitors are switched into the main capacitor array as needed to correct the conversion accuracy. This is faster than a complex digital error correction system, which could slow down the throughput rate. With all of the capacitors in both the main array and the trim array on the same chip, excellent stability is achieved, both over temperature and over time.

For flexibility, timing circuits include both an internal clock generator and an input for an external clock to synchronize with external systems. Standard control signals and three-state input/output registers simplify interfacing ADC7802 to most micro-controllers, microprocessors or digital storage systems.

Finally, this performance is matched with the low-power advantages of CMOS structures to allow a typical power consumption of 10mW.

OPERATION

BASIC OPERATION

Figure 1 shows the simple circuit required to operate ADC7802 in the Transparent Mode, converting a single input channel. A convert command on pin 20 ($\overline{WR}$) starts a conversion. Pin 22 ($\overline{BUSY}$) will output a LOW during the

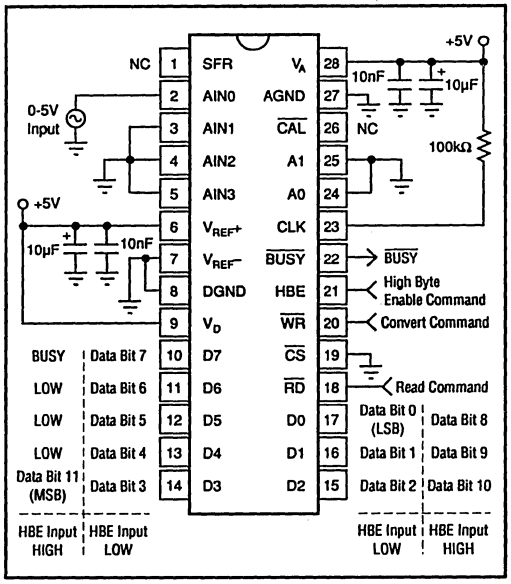
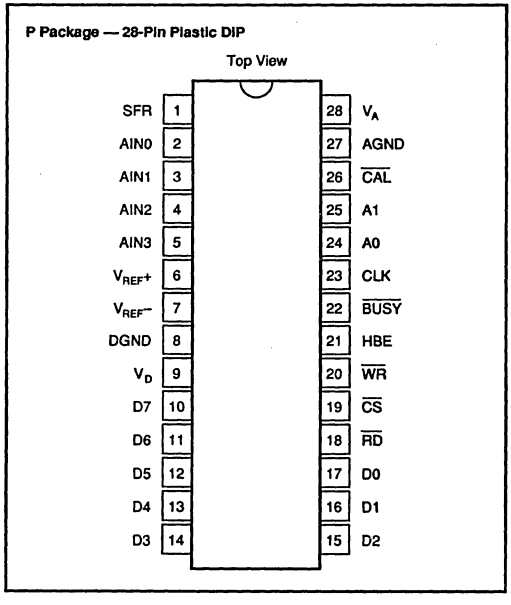
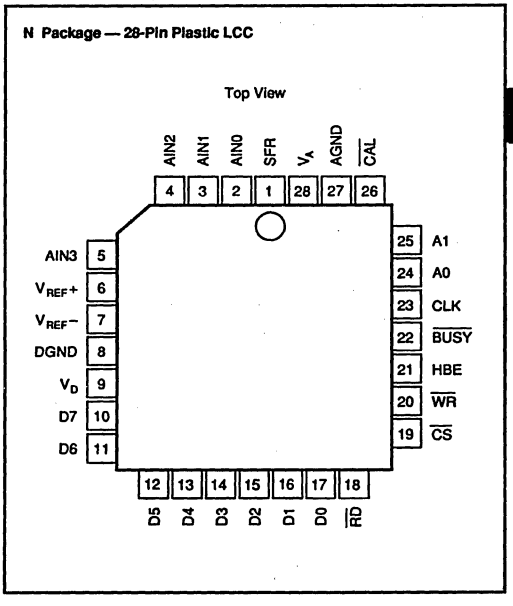


FIGURE 1. Basic Operation.

PIN CONFIGURATIONS





conversion process (including sample acquisition and conversion), and rises only after the conversion is completed. The two bytes of output data can then be read using pin 18 ($\overline{RD}$) and pin 21 (HBE).

STARTING A CONVERSION

A conversion is initiated on the rising edge of the $\overline{WR}$ input, with valid signals on A0, A1 and $\overline{CS}$. The selected input channel is sampled for five clock cycles, during which the comparator offset is also auto-zeroed to below 1/4LSB of error. The successive approximation conversion takes place during clock cycles 6 through 17.

Figures 2 and 3 show the full conversion sequence and the timing to initiate a conversion.

CALIBRATION

A calibration cycle is initiated automatically upon power-up (or after a power failure). Calibration can also be initiated by the user at any time by the rising edge of a minimum 100ns-wide LOW pulse on the $\overline{CAL}$ pin (pin 26), or by setting D1 HIGH in the Special Function Register (see SFR section). A calibration command will initiate a calibration cycle, regardless of whether a conversion is in process. During a calibration cycle, convert commands are ignored.

Calibration takes 168 clock cycles, and a normal conversion (17 clock cycles) is added automatically. For maximum accuracy, the supplies and reference need to be stable during the calibration procedure. To ensure that supply voltages and reference voltages have settled and are stable, an internal timer provides a waiting period of 42,425 clock cycles between power-up/power-failure and the start of the calibration cycle.

READING DATA

Data from the ADC7802 is read in two 8-bit bytes, with the Low byte containing the 8 LSBs of data, and the High byte containing the 4 MSBs of data. The outputs are coded in straight binary (with 0V = 000 hex, 5V = FFF hex), and the data is presented in a right-justified format (with the LSB as the most right bit in the 16-bit word). Two read operations are required to transfer the High byte and Low byte, and the bytes are presented according to the input level on the High Byte Enable pin (HBE).

PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	SFR	Special Function Register. When connected to a microprocessor address pin, allows access to special functions through D0 to D7. See the sections discussing the Special Function Register. If not used, connect to DGND. This pin has an internal pull-down.
2 to 5	AIN0 to AIN3	Analog inputs. Channel 0 to channel 3.
6	$V_{REF}+$	Positive voltage reference input. Normally +5V. Must be ≤ V_A.
7	$V_{REF}-$	Negative voltage reference input. Normally 0V.
8	DGND	Digital ground. DGND = 0V.
9	V_D	Logic supply voltage. V_D = +5V. Must be ≤ V_A and applied after V_A.
10 to 17	D0 to D7	Data Bus Input/Output Pins. Normally used to read output data. See section on SFR (Special Function Register) for other uses. When SFR is LOW, these function as follows:
10	D7	Data Bit 7 if HBE is LOW; if HBE is HIGH, acts as converter status pin and is HIGH during conversion or calibration, goes LOW after the conversion is completed. (Acts as an inverted $\overline{BUSY}$.)
11	D6	Data Bit 6 if HBE is LOW; LOW if HBE is HIGH.
12	D5	Data Bit 5 if HBE is LOW; LOW if HBE is HIGH.
13	D4	Data Bit 4 if HBE is LOW; LOW if HBE is HIGH.
14	D3	Data Bit 3 if HBE is LOW; Data Bit 11 (MSB) if HBE is HIGH.
15	D2	Data Bit 2 if HBE is LOW; Data Bit 10 if HBE is HIGH.
16	D1	Data Bit 1 if HBE is LOW; Data Bit 9 if HBE is HIGH.
17	D0	Data Bit 0 (LSB) if HBE is LOW; Data Bit 8 if HBE is HIGH.
18	$\overline{RD}$	Read Input. Active LOW; used to read the data outputs in combination with $\overline{CS}$ and HBE.
19	$\overline{CS}$	Chip Select Input. Active LOW.
20	$\overline{WR}$	Write Input. Active LOW; used to start a new conversion and to select an analog channel via address inputs A0 and A1 in combination with $\overline{CS}$. The minimum $\overline{WR}$ pulse LOW width is 100ns.
21	HBE	High Byte Enable. Used to select high or low data output byte in combination with $\overline{CS}$ and $\overline{RD}$, or to select SFR.
22	$\overline{BUSY}$	$\overline{BUSY}$ is LOW during conversion or calibration. $\overline{BUSY}$ goes HIGH after the conversion is completed.
23	CLK	Clock Input. For internal/external clock operation. For external clock operation, connect pin 23 to a 74 HC-compatible clock source. For internal clock operation, connect pin 23 per the clock operation description.
24 to 25	A0 to A1	Address Inputs. Used to select one of four analog input channels in combination with $\overline{CS}$ and $\overline{WR}$. The address inputs are latched on the rising edge of $\overline{WR}$ or $\overline{CS}$. A1 / A0 / Selected Channel LOW / LOW / AIN0 LOW / HIGH / AIN1 HIGH / LOW / AIN2 HIGH / HIGH / AIN3
26	$\overline{CAL}$	Calibration Input. A calibration cycle is initiated when $\overline{CAL}$ is LOW. The minimum pulse width of $\overline{CAL}$ is 100ns. If not used, connect to V_D. In this case calibration is only initiated at power on, or with SFR. This pin has an internal pull-up.
27	AGND	Analog Ground. AGND = 0V.
28	V_A	Analog Supply. V_A = +5V. Must be ≥ V_D and $V_{REF}+$.

The bytes can be read in either order, depending on the status of the HBE input. If HBE changes while $\overline{CS}$ and $\overline{RD}$ are LOW, the output data will change to correspond to the HBE input. Figure 4 shows the timing for reading first the Low byte and then the High byte.

ADC7802 provides two modes for reading the conversion results. At power-up, the converter is set in the Transparent Mode.

TRANSPARENT MODE

This is the default mode for ADC7802. In this mode, the conversion decisions from the successive approximation register are latched into the output register as they are made. Thus, the High byte (the 4 MSBs) can be read after the end of the ninth clock cycle (five clock cycles for the mux settling, sample acquisition and auto-zeroing of the comparator, followed by the four clock cycles for the 4MSB deci-

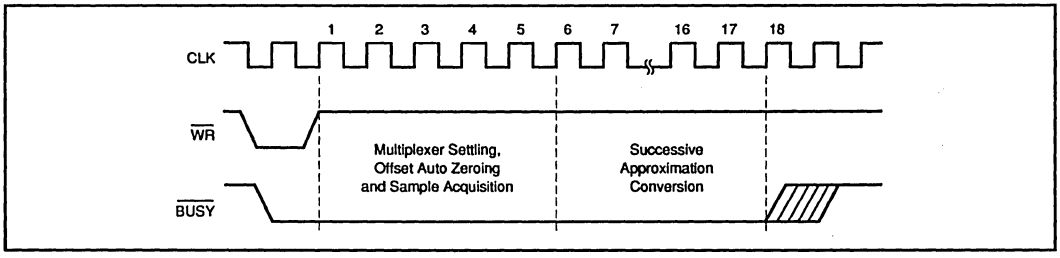


FIGURE 2. Converter Timing.

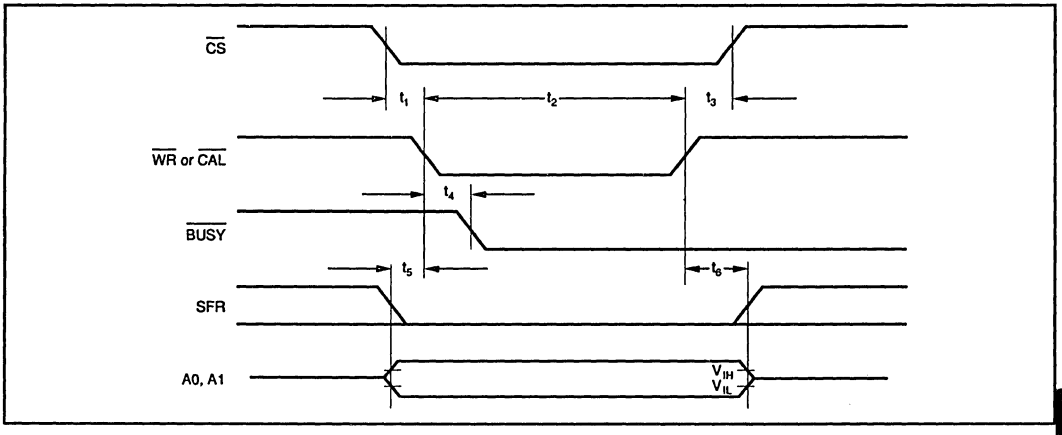


FIGURE 3. Write Cycle Timing (for initiating conversion or calibration).

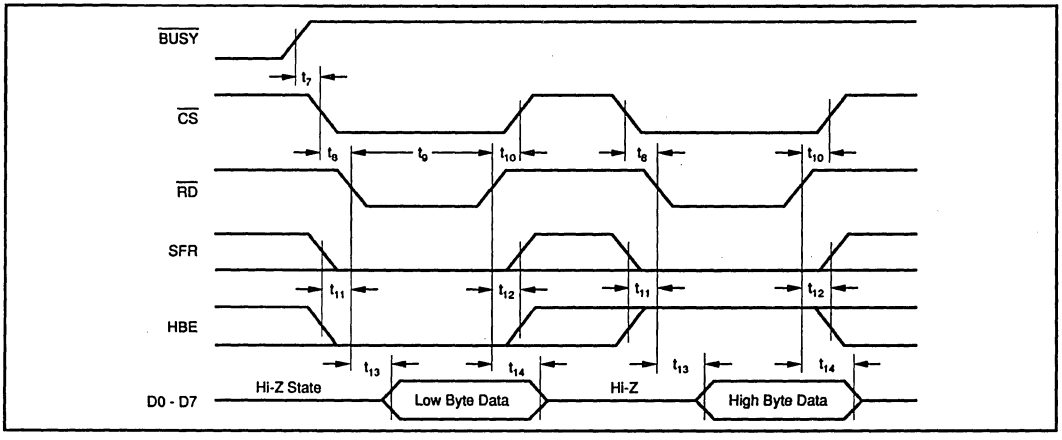


FIGURE 4. Read Cycle Timing.

sions.) The complete 12-bit data is available after $\overline{BUSY}$ has gone HIGH, or the internal status flag goes LOW (D7 when HBE is HIGH).

LATCHED OUTPUT MODE

This mode is activated by writing a HIGH to D0 and LOWs to D1 to D7 in the Special Function Register with $\overline{CS}$ and $\overline{WR}$ LOW and SFR and HBE HIGH. (See the discussion of the Special Function Register below.)

In this mode, the data from a conversion is latched into the output buffers only after a conversion is complete, and remains there until the next conversion is completed. The conversion result is valid during the next conversion. This allows the data to be read even after a new conversion is started, for faster system throughput.

TIMING CONSIDERATIONS

Table I and Figures 3 through 8 show the digital timing of ADC7802 under the various operating modes. All of the critical parameters are guaranteed over the full –40°C to +85°C operating range for ease of system design.

SPECIAL FUNCTION REGISTER (SFR)

An internal register is available, either to determine additional data concerning the ADC7802, or to write additional instructions to the converter. Access to the Special Function Register is made by driving SFR HIGH.

Table II shows the data in the Special Function Register that will be transferred to the output bus by driving HBE HIGH (with SFR HIGH) and initiating a read cycle (driving $\overline{RD}$ and $\overline{CS}$ LOW with $\overline{WR}$ HIGH as shown in Figure 4.) The Power Fail flag in the SFR is set when the power supply falls below about 3V. The flag also means that a new calibration has been started, and any data written to the SFR has been lost. Thus, the ADC7802 will again be in the Transparent Mode. Writing a LOW to D5 in the SFR resets the Power Fail flag. The Cal Error flag in the SFR is set when an overflow occurs during calibration, which may happen in very noisy systems. It is reset by starting a calibration, and remains low after a calibration without an overflow is completed.

SYMBOL	PARAMETER [1]	MIN	TYP	MAX	UNITS
t_1	$\overline{CS}$ to $\overline{WR}$ Setup Time [2]	0	0	0	ns
t_2	$\overline{WR}$ or $\overline{CAL}$ Pulse Width	100			ns
t_3	$\overline{CS}$ to $\overline{WR}$ Hold Time [2]	0	0	0	ns
t_4	$\overline{WR}$ to $\overline{BUSY}$ Propagation Delay	20	50	150	ns
t_5	A0, A1, HBE, SFR Valid to $\overline{WR}$ Setup Time	0			ns
t_6	A0, A1, HBE, SFR Valid to $\overline{WR}$ Hold Time	20			ns
t_7	$\overline{BUSY}$ to $\overline{CS}$ Setup Time	0			ns
t_8	$\overline{CS}$ to $\overline{RD}$ Setup Time [2]	0	0	0	ns
t_9	$\overline{RD}$ Pulse Width	100			ns
t_{10}	$\overline{CS}$ to $\overline{RD}$ Hold Time [2]	0	0	0	ns
t_{11}	HBE, SFR to $\overline{RD}$ Setup Time	50			ns
t_{12}	HBE, SFR to $\overline{RD}$ Hold Time	0			ns
t_{13}	$\overline{RD}$ to Valid Data (Bus Access Time) [3]		80	150	ns
t_{14}	$\overline{RD}$ to Hi-Z Delay (Bus Release Time) [3]		90	180	ns
t_{15}	$\overline{RD}$ to Hi-Z Delay For SFR [3]	20		60	ns
t_{16}	Data Valid to $\overline{WR}$ Setup Time	100			ns
t_{17}	Data Valid to $\overline{WR}$ Hold Time	20			ns

NOTES: (1) All input control signals are specified with $t_{RISE} = t_{FALL} = 20$ns (10% to 90% of 5V) and timed from a voltage level of 1.6V. Data is timed from V_{IH}, V_{IL}, V_{OH} or V_{OL}. (2) The internal RD pulse is performed by a NOR wiring of $\overline{CS}$ and $\overline{RD}$. The internal WR pulse is performed by a NOR wiring of $\overline{CS}$ and $\overline{WR}$. (3) Figures 7 and 8 show the measurement circuits and pulse diagrams for testing transitions to and from Hi-Z states.

TABLE I. Timing Specifications (CLK = 1MHz external, T_A = –40°C to +85°C).

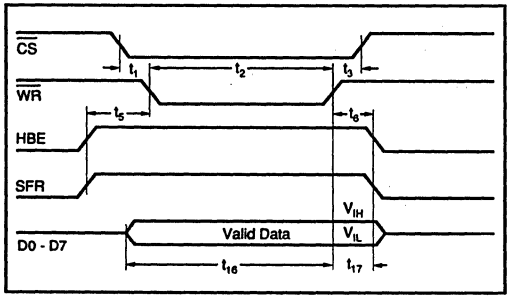


FIGURE 5. Writing to the SFR.

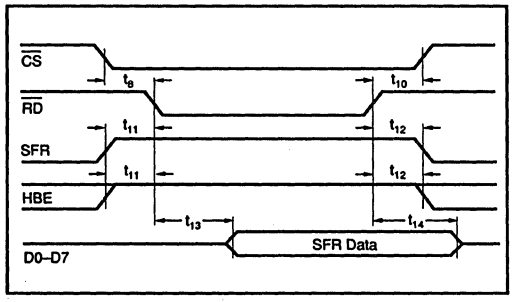


FIGURE 6. Reading the SFR.

Writing a HIGH to D3 in the FSR puts the ADC7802 in the Power Down Mode. Power consumption is reduced to 50µW and D3 remains HIGH. To exit Power Down Mode, either write a LOW to D3 in the SFR, or initiate a calibration by sending a LOW to the $\overline{CAL}$ pin or writing a HIGH to D1. During Power Down Mode, a pulse on $\overline{CS}$ and $\overline{WR}$ will initiate a single conversion, then the ADC7802 will revert to power down.

Table III shows how instructions can be transferred to the Special Function Register by driving HBE HIGH (with SFR HIGH) and initiating a write cycle (driving $\overline{WR}$ and $\overline{CS}$ LOW with $\overline{RD}$ HIGH.) The timing is shown in Figure 3. Note that writing to the SFR also initiates a new conversion.

CONTROL LINES

Table IV shows the functions of the various control lines on the ADC7802. The use of standard $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ control signals simplifies use with most microprocessors. At the same time, flexibility is assured by availability of status information and control functions, both through the SFR and directly on pins.

INSTALLATION

INPUT BANDWIDTH

From the typical performance curves, it is clear that ADC7802 can accurately digitize signals up to 500Hz, but distortion will increase beyond this point. Input signals slewing faster than 8mV/µs can degrade accuracy. This is a result of the high-precision auto-zeroing circuit used during the acquisition phase. For applications requiring higher signal bandwidth, any good external sample/hold, like the SHC5320, can be used.

INPUT IMPEDANCE

ADC7802 has a very high input impedance (input bias current over temperature is 100nA max), and a low 50pF

PIN	FUNCTION	DESCRIPTION
D0	Mode Status	If LOW, Transparent Mode enabled for data latches. If HIGH, Latched Output Mode enabled.
D1	CAL Flag	If HIGH, calibration cycle in progress.
D2		Reserved for factory use.
D3	Power Down Status	If HIGH, in Power Down Mode.
D4		Reserved for factory use.
D5	POWER FAIL Flag	If HIGH, a power supply failure has occurred. (Supply fell below 3V.)
D6	CAL ERROR Flag	If HIGH, an overflow occured during calibration.
D7	BUSY Flag	If HIGH, conversion or calibration in progress.

NOTE: These data are tranferred to the bus when a read cycle is initiated with SFR and HBE HIGH. Reading the SFR with SFR HIGH and HBE LOW is reserved for factory use at this time, and will yield unpredictable data.

TABLE II. Reading the Special Function Register.

	$\overline{CS}/\overline{WR}$	SFR/HBE	D0	D1	D3	D5	D7	D2/D4/D6
Enables Transparent Mode for Data Latches.	LOW	HIGH	LOW	X	LOW	X	LOW	LOW
Enables Latched Output Mode for Data Latches.	LOW	HIGH	HIGH	X	LOW	X	LOW	LOW
Initiates Calibration Cycle.	LOW	HIGH	X	HIGH	LOW	X	LOW	LOW
Resets Power Fail flag.	LOW	HIGH	X	X	LOW	LOW	LOW	LOW
Activates Power Down Mode	LOW	HIGH	X	X	HIGH	X	LOW	LOW

NOTES: (1) In Power Down Mode, a pulse on $\overline{CS}$ and $\overline{WR}$ will initiate a single conversion, then the ADC7802 will revert to power down. (2) X means it can be either HIGH or LOW without affecting this action. Writing HIGH to D2, D3, D4 or D6, or writing with SFR HIGH and HBE LOW, may result in unpredictable behavior. These modes are reserved for factory use at this time.

TABLE III. Writing to the Special Function Register.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	SFR	HBE	$\overline{CAL}$	$\overline{BUSY}$	OPERATION
X	X	X	X	X	0↑1	X	Initiates calibration cycle.
X	X	X	X	X	X	0	Conversion or calibration in process. Inhibits new conversion from starting.
1	X	X	X	X	1	X	None. Outputs in Hi-Z State.
0	1	0↑1	0	X	1	1	Initiates conversion.
0	0	1	0	0	1	X	Low byte conversion results output on data bus.
0	0	1	0	1	1	X	High byte conversion results output on data bus.
0	1	0	1	1	1	1	Write to SFR and rising edge on $\overline{WR}$ initiates conversion.
0	0	1	1	1	1	X	Contents of SFR output on data bus.
0	1	0	1	0	1	X	Reserved for factory use.
0	0	1	1	0	1	X	Reserved for factory use. (Unpredictable data on data bus.)

TABLE IV. Control Line Functions.

input capacitance. To ensure a conversion accurate to 12 bits, the analog source must be able to charge the 50pF and settle within the first five clock cycles after a conversion is initiated. During this time, the input is also very sensitive to noise at the analog input, since it could be injected into the capacitor array.

In many applications, a simple passive low-pass filter as shown in Figure 9a can be used to improve signal quality. In this case, the source impedance needs to be less than 5kΩ to keep the induced offset errors below 1/2LSB, and to meet the acquisition time of five clock cycles. The values in Figure 9a meet these requirements, and will maintain the full power bandwidth of the system. For higher source impedances, a buffer like the one in Figure 9b should be used.

INPUT PROTECTION

The input signal range must not exceed $\pm V_{REF}$ or V_A by more than 0.3V.

The analog inputs are internally clamped to V_A. To prevent damage to the ADC7802, the current that can flow into the inputs must be limited to 20mA. One approach is to use an external resistor in series with the input filter resistor. For example, a 1kΩ input resistor allows an overvoltage to 20V without damage.

REFERENCE INPUTS

A 10µF tantalum capacitor is recommended between $V_{REF}+$ and $V_{REF}-$ to insure low source impedance. These capacitors should be located as close as possible to the ADC7802 to reduce dynamic errors, since the reference provides packets of current as the successive approximation steps are carried out.

$V_{REF}+$ must not exceed V_A. Although the accuracy is specified with $V_{REF}+ = 5V$ and $V_{REF}- = 0V$, the converter can function with $V_{REF}+$ as low as 2.5V and $V_{REF}-$ as high as 1V. As long as there is at least a 2.5V difference between $V_{REF}+$ and $V_{REF}-$, the absolute value of errors does not change significantly, so that accuracy will typically be within ±1LSB. (1/2LSB for a 5V span is 610µV, which is 1LSB for a 2.5V span.)

The power supply to the reference source needs to be considered during system design to prevent $V_{REF}+$ from exceeding (or overshooting) V_A, particularly at power-on. Also, after power-on, if the reference is not stable within 42,425 clock cycles, an additional calibration cycle may be needed.

POWER SUPPLIES

The digital and analog power supply lines to the ADC7802 should be bypassed with 10µF tantalum capacitors as close

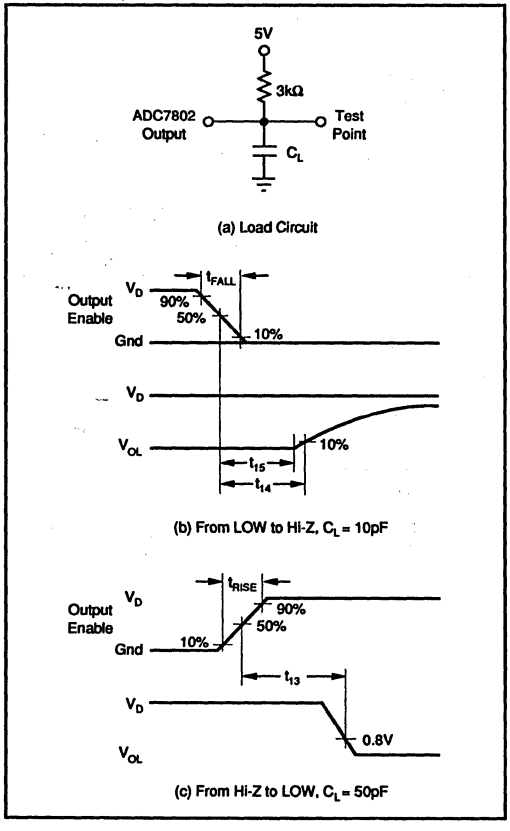


FIGURE 7. Measuring Active LOW to/from Hi-Z State.

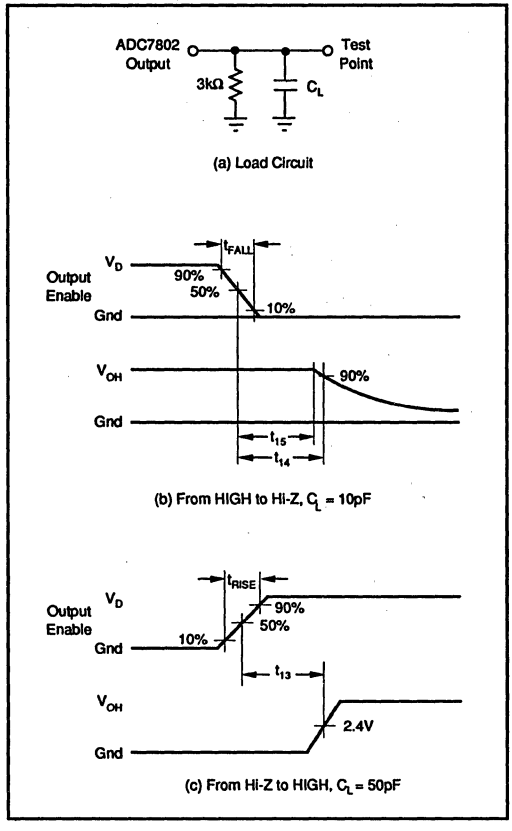


FIGURE 8. Measuring Active HIGH to/from Hi-Z State.

to the part as possible. Although ADC7802 has excellent power supply rejection, even for higher frequencies, linear regulated power supplies are recommended.

Care should be taken to insure that V_D does not come up before V_A, or permanent damage to the part may occur. Figure 10 shows a good supply approach, powering both V_A and V_D from a clean linear supply, with the 10Ω resistor between V_A and V_D insuring that V_D comes up after V_A. This is also a good method to further isolate the ADC7802 from digital supplies in a system with significant switching currents that could degrade the accuracy of conversions.

GROUNDING

To maximize accuracy of the ADC7802, the analog and digital grounds are not connected internally. These points should have very low impedance to avoid digital noise feeding back into the analog ground. The $V_{REF}-$ pin is used as the reference point for input signals, so it should be connected directly to AGND to reduce potential noise problems.

EXTERNAL CLOCK OPERATION

The circuitry required to drive the ADC7802 clock from an external source is shown in Figure 11a. The external clock must provide a 0.8V max for LOW and a 3.5V min for HIGH, with rise and fall times that do not exceed 200ns. The minimum pulse width of the external clock must be 300ns. Synchronizing the conversion clock to an external system clock is recommended in microprocessor applications to prevent beat-frequency problems.

Note that the electrical specification tables are based on using an external 2MHz clock. Typically, the specified accuracy is maintained for clock frequencies between 0.5 and 2.4MHz.

INTERNAL CLOCK OPERATION

Figure 11b shows how to use the internal clock generating circuitry. The clock frequency depends only on the value of the resistor, as shown in "Internal Clock Frequency vs R_{CLOCK}" in the Typical Performance Curves section.

The clock generator can operate between 100kHz and 2MHz. With R = 100kΩ, the clock frequency will nominally be 800kHz. The internal clock oscillators may vary by up to 20% from device to device, and will vary with temperature, as shown in the typical performance curves. Therefore, use of an external clock source is preferred in many applications where control of the conversion timing is critical, or where multiple converters need to be synchronized.

APPLICATIONS

BIPOLAR INPUT RANGES

Figure 12 shows a circuit to accurately and simply convert a bipolar ±5V input signal into a unipolar 0 to 5V signal for conversion by the ADC7802, using a precision, low-cost complete difference amplifier, INA105.

Figure 13 shows a circuit to convert a bipolar ±10V input signal into a unipolar 0 to 5V signal for conversion by the ADC7802. The precision of this circuit will depend on the matching and tracking of the three resistors used.

To trim this circuit for full 12-bit precision, R2 and R3 need to be adjustable over appropriate ranges. To trim, first have the ADC7802 converting continually and apply +9.9927V (+10V – 1.5LSB) at the input. Adjust R3 until the ADC7802 output toggles between the codes FFE hex and FFF hex. This makes R3 extremely close to R1. Then, apply –9.9976V (–10V + 0.5LSB) at the input, and adjust R2 until the ADC7802

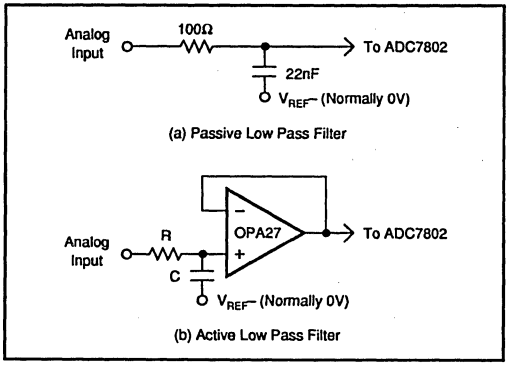


FIGURE 9. Input Signal Conditioning.

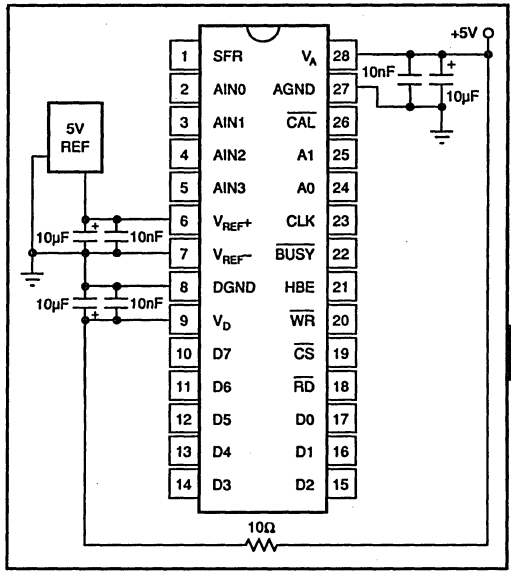


FIGURE 10. Power Supply and Reference Decoupling.

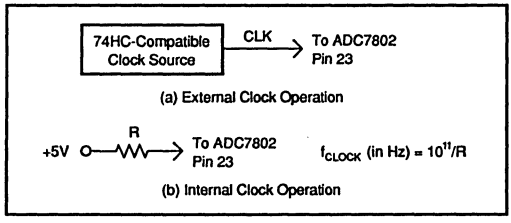


FIGURE 11. Internal Clock Operation.

output toggles between 000 hex and 001 hex. At each trim point, the current through the third resistor will be almost zero, so that one trim iteration will be enough in most cases. More iterations may be required if the op amp selected has large offset voltage or bias currents, or if the +5V reference is not precise.

This circuit can also be used to adjust gain and offset errors due to the components preceding the ADC7802, to match the performance of the self-calibration provided by the converter.

INTERFACING TO MOTOROLA MICROPROCESSORS

Figure 14 shows a typical interface to Motorola microprocessors, while Figure 15 shows how the result can be placed in register D0.

Conversion is initiated by a write instruction decoded by the address decoder logic, with the lower two bits of the address bus selecting an ADC input channel, as follows:

MOVE.W D0, ADC-ADDRESS

The result of the conversion is read from the data bus by a read instruction to ADC-ADDRESS as follows:

MOVEP.W $000 (ADC-ADDRESS), D0

This puts the 12-bit conversion result in the DO register, as shown in Figure 15. The address decoder must pull down $\overline{\text{ADC\_CS}}$ at ADC-ADDRESS to access the Low byte and ADC-ADDRESS +2 to access the High byte.

INTERFACING TO INTEL MICROPROCESSORS

Figure 16 shows a typical interface to Intel.

A conversion is initiated by a write instruction to address $\overline{\text{ADC\_CS}}$. Data pins DO0 and DO1 select the analog input channel. The $\overline{\text{BUSY}}$ signal can be used to generate a microprocessor interrupt (INT) when the conversion is completed.

A read instruction from the $\overline{\text{ADC\_CS}}$ address fetches the Low byte, and a read instruction from the $\overline{\text{ADC\_CS}}$ address +2 fetches the High byte.

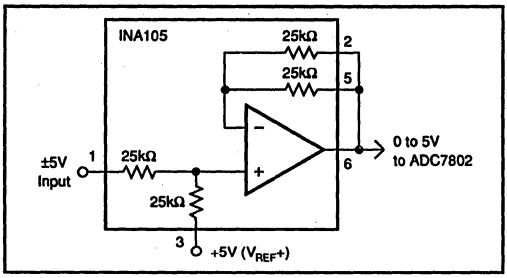


FIGURE 12. ±5V Input Range.

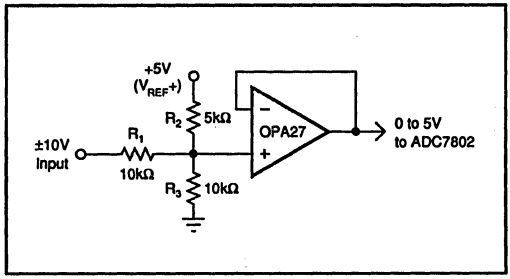


FIGURE 13. ±10V Input Range.

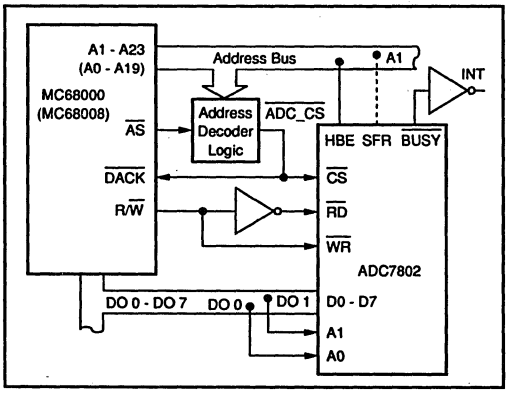


FIGURE 14. Interface to Motorola Microprocessors.

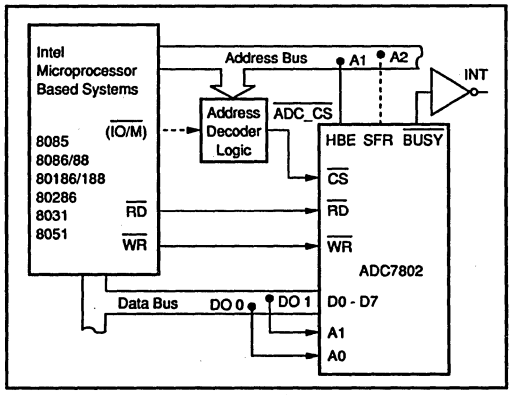


FIGURE 16. Interface to Intel Microprocessors.

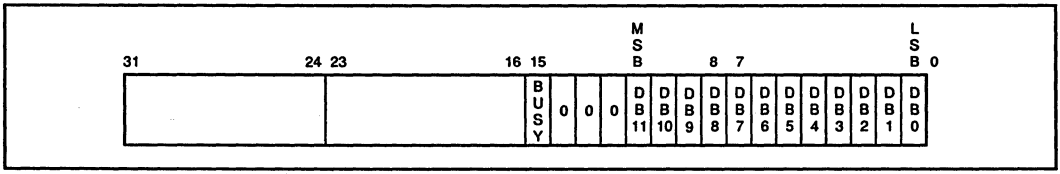
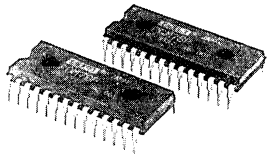


FIGURE 15. Conversion Results in Motorola Register D0.

BURR-BROWN®



PCM78P

16-Bit Audio ANALOG-TO-DIGITAL CONVERTER

FEATURES

- LOW COST/HIGH PERFORMANCE 16-BIT AUDIO A/D CONVERTER
- FAST 5µs MAX CONVERSION TIME (4µs TYP)
- VERY LOW THD+N (TYP –88dB AT FS; MAX –82dB)
- ±3V INPUT RANGE
- TWO SERIAL OUTPUT MODES PROVIDE VERSATILE INTERFACING
- COMPLETE WITH INTERNAL REFERENCE AND CLOCK IN 28-PIN PLASTIC DIP
- ±5V TO ±15V SUPPLY RANGE (600mW POWER DISSIPATION)

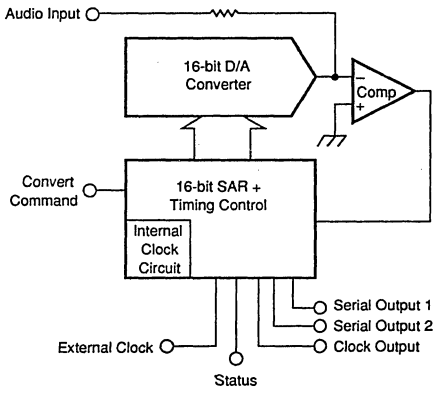
APPLICATIONS

- DSP DATA ACQUISTION
- TEST INSTRUMENTATION
- SAMPLING KEYBOARD SYNTHESIZERS
- DIGITAL AUDIO TAPE
- BROADCAST AUDIO PROCESSING
- TELECOMMUNICATIONS

DESCRIPTION

The PCM78P is a low-cost 16-bit A/D converter which is specifically designed and tested for dynamic applications. It features very fast, low distortion performance (4µs/–88dB THD+N typical) and is complete with internal clock and reference circuitry. The PCM78P is packaged in a reliable, low-cost 28-pin plastic DIP and data output is available in user-selectable serial output formats. The PCM78P is ideal for digital audio tape (DAT) recorders. Many similar applications such as digital signal processing and telecom applications are equally well served by the PCM78P.

The PCM78P uses a SAR technique. Analog and digital portions are efficiently partitioned into a high-speed, bipolar section and a low-power CMOS section. The PCM78P has been optimized for excellent dynamic performance and low cost.



SPECIFICATIONS

ELECTRICAL

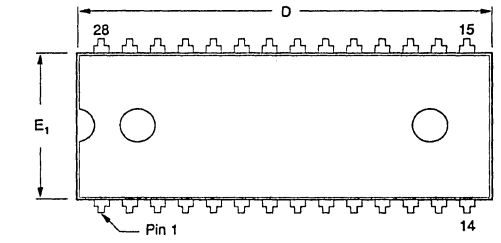
T_c = +25°C, $+V_{DD}$ = +5V, and $\pm V_{CC}$ = ±12V, and one minute warm-up in convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	PCM78P MIN	PCM78P TYP	PCM78P MAX	UNITS
RESOLUTION				16	Bits
INPUT/OUTPUT					
ANALOG INPUT					
Input Range		–3		+3	V
Input Impedance			1.5		kΩ
DIGITAL INPUT/OUTPUT					
Logic Family			TTL Compatible CMOS		
Logic Level: V_{IH}	I_{IH} = +40µA	+2		+5.5	V
V_{IL}	I_{IL} = –100µA	0		+0.8	V
V_{OH}	I_{OH} = 2TTL Loads	+2.4			V
V_{OL}	I_{OL} = 2TTL Loads			+0.4	V
Data Format			Serial BOB or BTC		
Convert Command			Negative Edge [1]		
Pulse Width		25	50		ns
CONVERSION TIME			4	5	µs
DYNAMIC CHARACTERISTICS					
SIGNAL-TO-NOISE RATIO (SNR)[2]	f_S = 200kHz/T_{CONV} = 4µs[3]				
f = 1kHz (0dB)	BW = 20kHz		90		dB[4]
f = 10kHz (0dB)	BW = 100kHz		80		dB
TOTAL HARMONIC DISTORTION[5]	f_S = 200kHz/T_{CONV} = 4µs				
f = 1kHz (0dB)	BW = 20kHz		–91		dB
f = 19kHz (0dB)	BW = 20kHz		–90		dB
f = 10kHz (0dB)	BW = 100kHz		–90		dB
f = 90kHz (0dB)	BW = 100kHz		–89		dB
TOTAL HARMONIC DISTORTION + NOISE[6]	f_S = 200kHz/T_{CONV} = 4µs				
f = 1kHz (0dB)	BW = 20kHz		–88	–82	dB
f = 1kHz (–20dB)	BW = 20kHz		–74	–68	dB
f = 1kHz (–60dB)	BW = 20kHz		–34		dB
f = 19kHz (0dB)	BW = 20kHz		–87		dB
f = 10kHz (0dB)	BW = 100kHz		–82		dB
f = 90kHz (0dB)	BW = 100kHz		–81		dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error			±2		%
Bipolar Zero Error			±20		mV
Differential Linearity Error			±0.002		% of FSR[7]
Integral Linearity Error			±0.003		% of FSR
Missing Codes			None		14 Bits[8]
DRIFT					
Gain	0°C to +70°C		±25		ppm/°C
Bipolar Zero	0°C to +70°C		±4		ppm of FSR/°C
POWER SUPPLY SENSITIVITY					
$+V_{CC}$			±0.008		%FSR/%V_{CC}
$-V_{CC}$			±0.003		%FSR/%V_{CC}
$+V_{DD}$			±0.003		%FSR/%V_{DD}
POWER SUPPLY REQUIREMENTS					
Voltage Range: $+V_{CC}$		+4.75		+15.6	V
$-V_{CC}$		–4.75		–15.6	V
$+V_{DD}$		+4.75		+5.25	V
Current: $+V_{CC}$	$+V_{CC}$ = +12V		+15		mA
$-V_{CC}$	$-V_{CC}$ = –12V		–21		mA
$+V_{DD}$	$+V_{DD}$ = +5V		+7		mA
Power Dissipation	$\pm V_{CC}$ = ±12V		575		mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Storage		–50		+100	°C
Operating		–25		+85	°C

NOTES: (1) When convert command is high, converter is in a halt/reset mode. Actual conversion begins on negative edge. See detailed text on timing for convert command description when using external clock. (2) Ratio of Noise rms/Signal rms. (3) f = input frequency; f_S = sample frequency (PCM78P and SHC702 in combination); BW = bandwidth of output (based on FFT or actual analog reconstruction using a 20kHz low-pass filter). (4) Referred to input signal level. (5) Ratio of Distortion rms/Signal rms. (6) Ratio of Distortion rms + Noise rms/Signal rms. (7) FSR: Full-Scale Range = 6Vp-p. (8) Typically no missing Codes at 14-bit resolution.

MECHANICAL

P Package — 28-Pin Plastic DIP

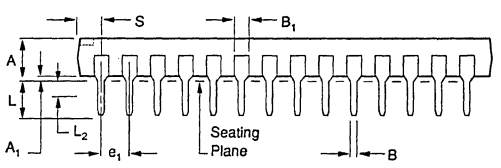


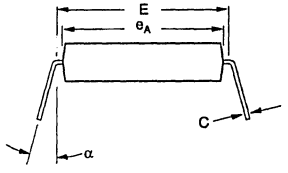
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A(1)	.169	.200	4.29	5.08
A1(1)	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D(1)	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1(1)	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
Q1	.020	.070	0.51	1.78
S1	.040	.080	1.02	2.03

(1) Not JEDEC Standard

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.





INPUT/OUTPUT RELATIONSHIPS

ANALOG INPUT	CONDITION	DIGITAL OUTPUT BTC	DIGITAL OUTPUT BOB
+2.999908V	+ Full Scale	7FFF Hex	FFFF Hex
–3.000000V	–Full Scale	8000 Hex	0000 Hex
0.000000V	Bipolar Zero	0000 Hex	8000 Hex
–0.000092V	Zero-1 LSB	FFFF Hex	7FFF Hex

ABSOLUTE MAXIMUM RATINGS

$+V_{cc}$ to Analog Common ..... 0 to +16.5V
$-V_{cc}$ to Analog Common ..... 0 to –16.5V
$-V_{DD}$ to Analog Common ..... 0 to +7V
Analog Common to Digital Common ..... ±0.5V
Logic Inputs to Digital Common ..... –0.3V to V_{DD} + 0.5V
Analog Inputs to Analog Common ..... ±16.5V
Lead Temperature (soldering, 10s) ..... +300°C
Stresses above these ratings may permanently damage the device.

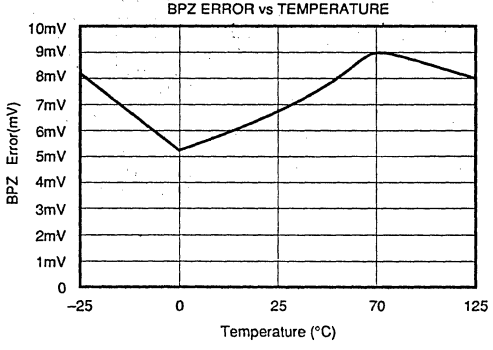
PIN ASSIGNMENTS

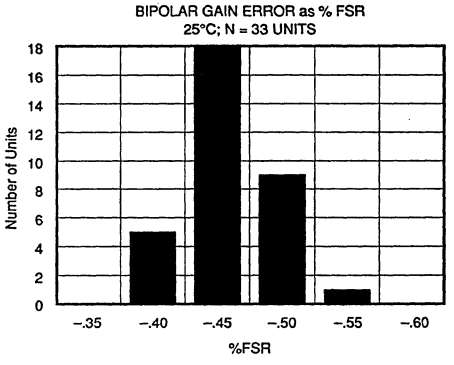
PIN	NAME	I/O	DESCRIPTIUON
1	Analog In	I	Analog Signal Input (1.5KΩ impedance).
2	$-V_{cc}$	I	Analog power supply (–5V to –15V).
3	MSB Adjust	I	Internal adjustment point to allow adjustment of MSB major carry.
4	$+V_{DD}$	I	Power connection for comparator (+5V).
5	No Connection	—	No internal connection.
6	Comparator Common	I	Comparator common connection. Connect to ground.
7	$\overline{MSB}$	O	Parallel output of bit 1 (MSB) inverted.
8	BTC/BOB Select	I	Two's complement (open) or straight binary (grounded) data output format selection.
9	Status	O	Output signal held high until conversion is complete.
10	Clock Out	O	Internal clock output generated from RC network on pins 11 and 12 (also present when external clock is used lagging external clock by ~24ns and same duty cycle).
11	R_1C_1	I	RC connection point used to generate internal clock. Sets clock high time. See text for details.
12	R_2C_2	I	RC connection point used to generate internal clock. Sets clock low time. See text for details.
13	S_{OUT2}	O	Internal shift register containing the previous conversion result. (Alternate latched data output mode).
14	$+V_{DD}$	I	Power connection for +5V logic supply.
15	S_{OUT1}	O	Primary real-time data output synchronized to clock out.
16	External Clock	I	External clock input point (internal clock must be disabled).
17	Int/Ext Clock Select	I	Selects either internal or external clock mode (low = internal; open = external).
18	Short Cycle	I	Terminates conversion at less than 16-bits (open for 16-bit mode). See text for details.
19	Convert Command	I	Starts conversion process (can optionally be generated internally).
20	S_{OUT2} Latch	I	Latches previous conversion result for readout (must be issued with the S_{OUT2} clock to initiate latch and an internal convert command).
21	S_{OUT2} Clock	I	Used to read out internally latched data from previous conversion.
22	Digital Common	I	Digital grounding pin.
23	$+V_{cc}$	I	Analog supply connection (+5V to +15V).
24	V_{POT}	O	Voltage output (~2.5V) for optional adjustment of MSB transition.
25	Reference Decouple	I	Reference decoupling point.
26	Analog Common	I	Analog grounding pin.
27	Reference Out	O	2V reference out. Should not be used except as shown in connection diagram.
28	Speed Up	I	Connection point for a capacitor to speed reference settling. See text for details.

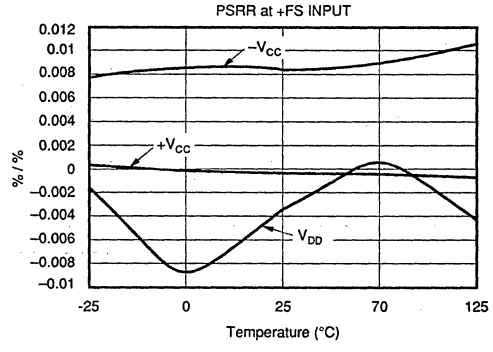
NOTE: Analog and digital commons are connected internally.

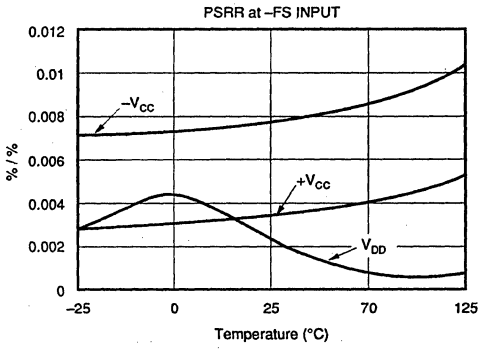
TYPICAL PERFORMANCE CURVES

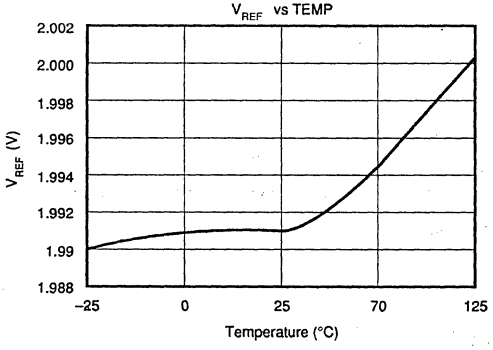
T_A = +25°C, V_{CC} = ±15V unless otherwise noted.

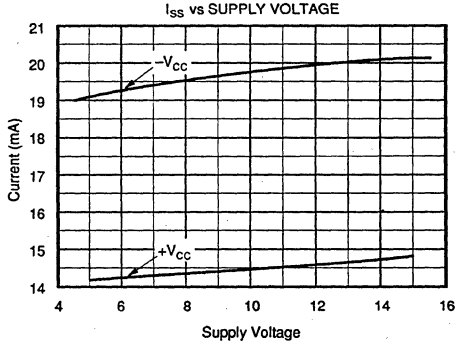








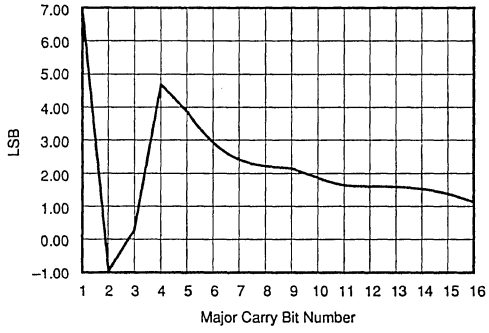




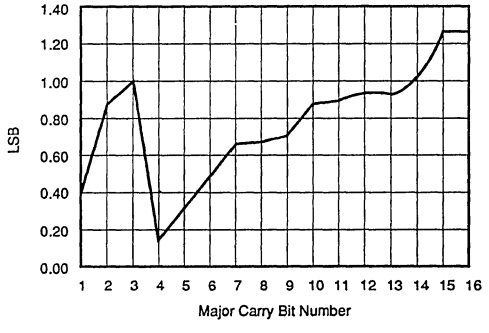
TYPICAL PERFORMANCE CURVES (cont)

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.

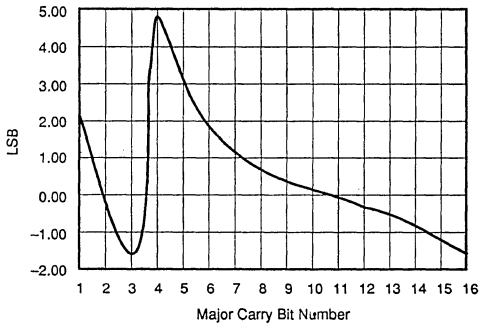
INTEGRAL NONLINEARITY
at –25°C



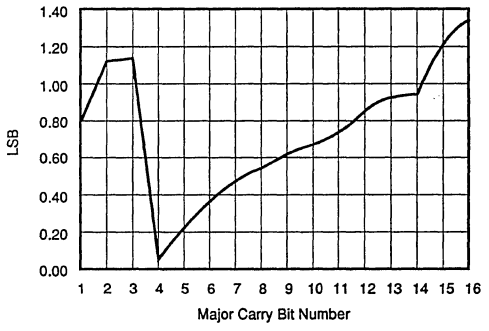
DIFFERENTIAL NONLINEARITY
at –25°C



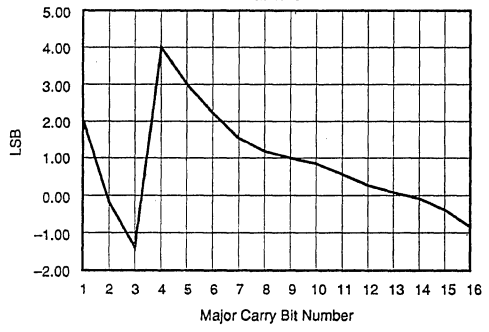
INTEGRAL NONLINEARITY
at 0°C



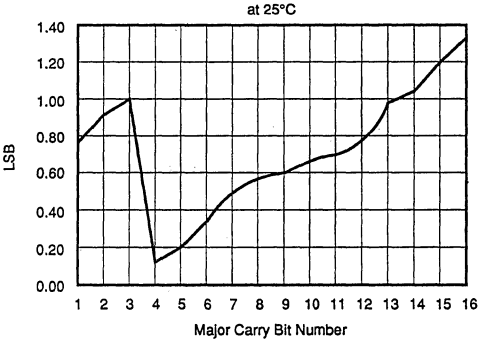
DIFFERENTIAL NONLINEARITY
at 0°C



INTEGRAL NONLINEARITY
at 25°C

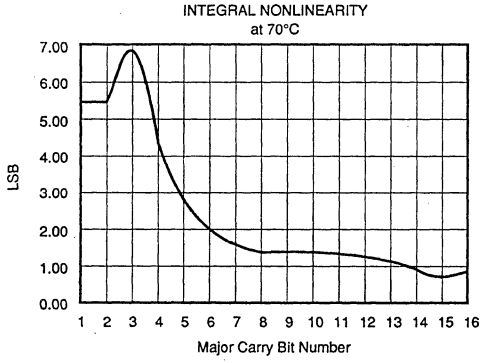


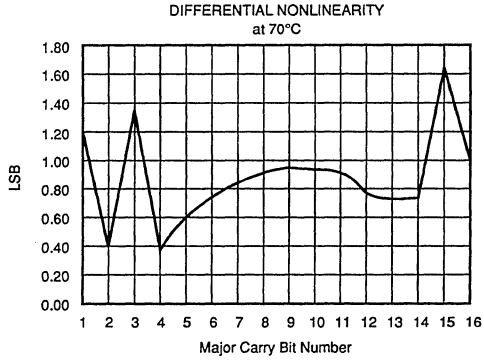
DIFFERENTIAL NONLINEARITY
at 25°C

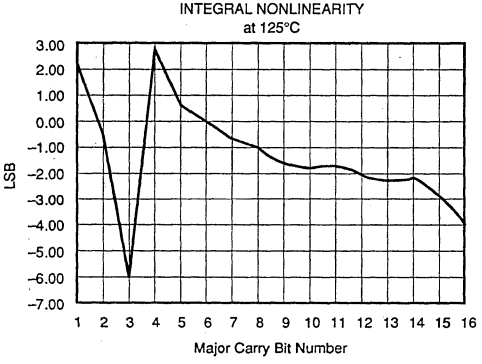


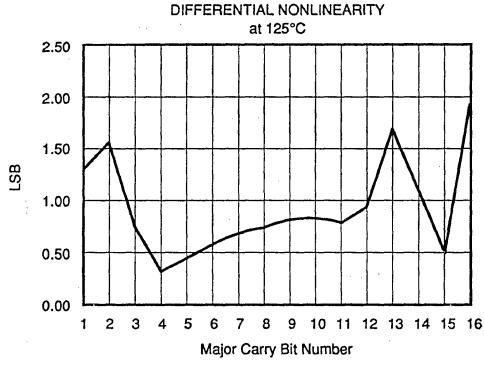
TYPICAL PERFORMANCE CURVES (cont)

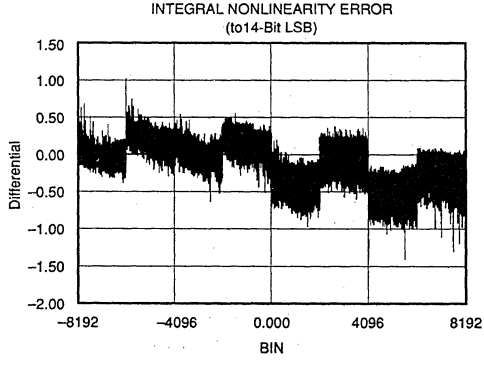
T_A = +25°C, V_{CC} = ±15V unless otherwise noted. Histograms done with conversion time = 8µs.

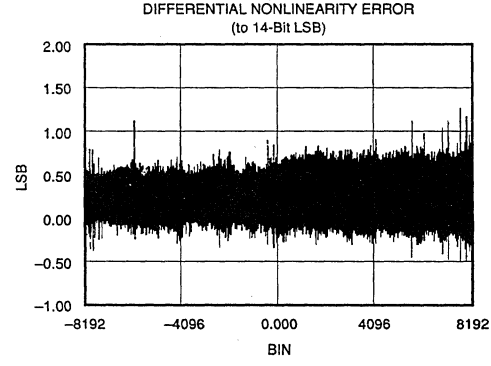








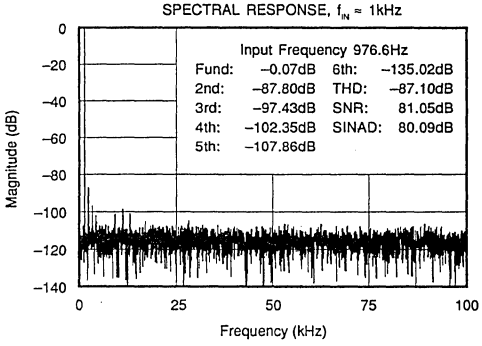




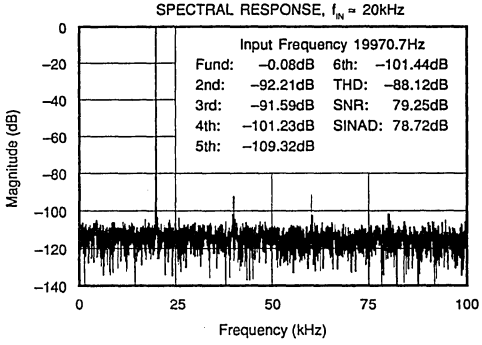
TYPICAL PERFORMANCE CURVES (cont)

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.

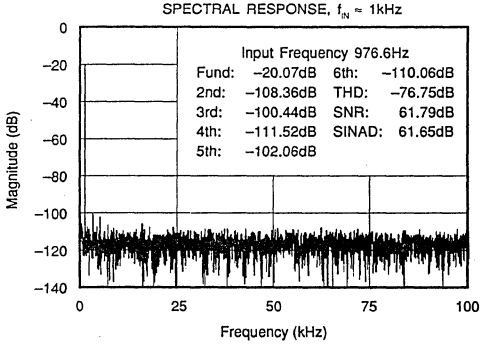
SPECTRAL RESPONSE, f_{IN} = 1kHz



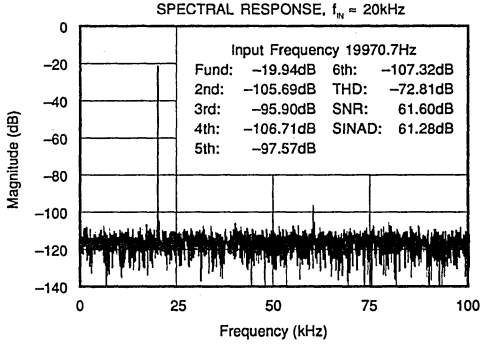
SPECTRAL RESPONSE, f_{IN} = 20kHz



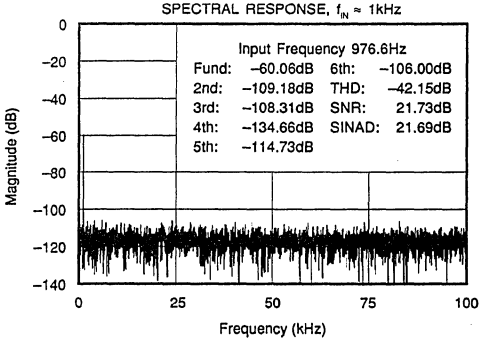
SPECTRAL RESPONSE, f_{IN} = 1kHz



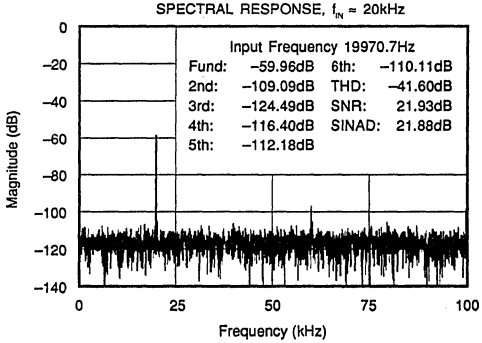
SPECTRAL RESPONSE, f_{IN} = 20kHz



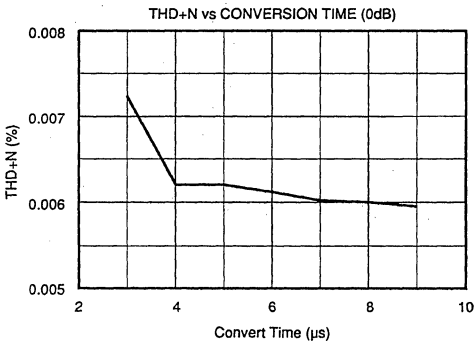
SPECTRAL RESPONSE, f_{IN} = 1kHz

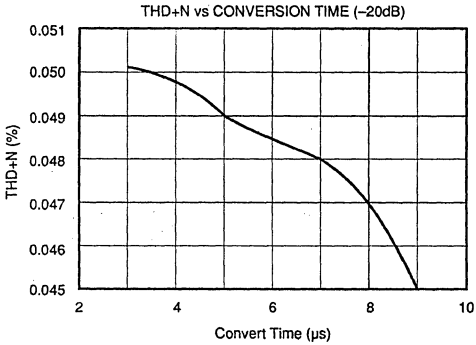


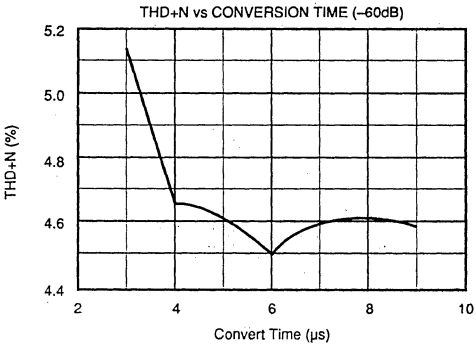
SPECTRAL RESPONSE, f_{IN} = 20kHz



TYPICAL PERFORMANCE CURVES (CONT)







THEORY OF OPERATION

The PCM78P is a successive approximation A/D converter; this type of converter is well suited to high speed and resolution. The accuracy of a successive approximation converter is described by the transfer function shown in Figure 1. All successive-approximation A/D converters have an inherent quantization error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Gain drift over temperature rotates the line (Figure 1) about zero, and Offset drift shifts the line left or right over the operating temperature range. Total Harmonic Distortion + Noise (THD + N) is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as quantization errors. The THD+N specification is most useful in audio or dynamic signal processing applications. To be useful, THD + N should be specified for both high level and low level input signals. This error is unadjustable and is the most meaningful indicator of A/D converter accuracy for dynamic applications.

DYNAMIC RANGE

Dynamic range is a measure of the ratio of the smallest signals the converter can resolve to the full scale range and is usually expressed in decibels. The theoretical dynamic range of a converter is approximately 6 x n, where n is the number of bits of resolution. A 16-bit converter would thus have a theoretical dynamic range of 96dB. The actual useful dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit.

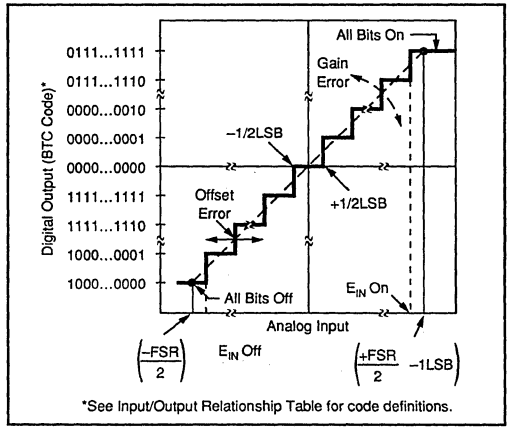


FIGURE 1. Input vs Output for Ideal Bipolar A/D Converter.

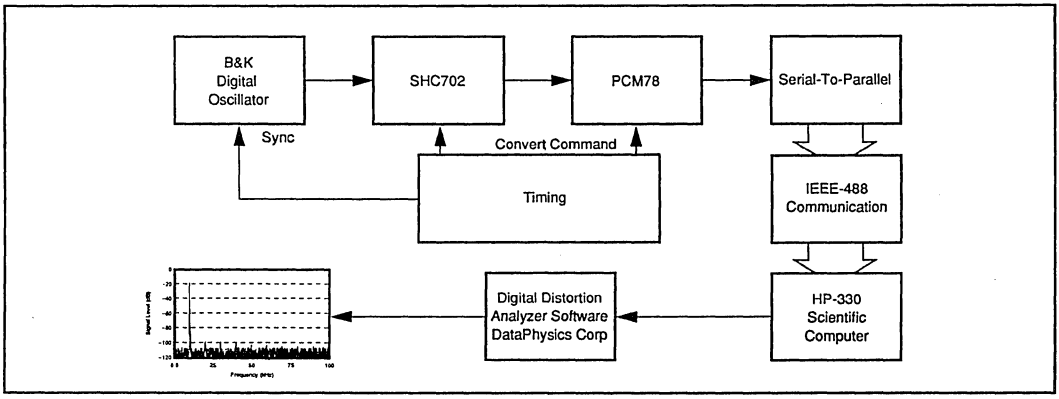


FIGURE 2. Block Diagram of Distortion Test Circuit.

DISCUSSION OF SPECIFICATIONS

TOTAL HARMONIC DISTORTION

Evaluating distortion specifications can be a difficult task, as distortion is often specified in different ways. Total Harmonic Distortion (THD) is defined as the ratio of the square root sum of the squares of the value of rms harmonics to the value of the rms fundamental and is expressed in percent or dB. Note that this measurement only includes energy present in those frequencies which would contain harmonics, and therefore is less than Total Harmonic Distortion plus Noise.

The Total Harmonic Distortion plus Noise (THD + N) is defined as the ratio of the square root of the sum of the squares of the value of the rms harmonics and rms noise to the value of the rms fundamental and is expressed in percent or dB. This is the most meaningful measurement of a dynamic converter's performance because it includes all energy present in the signal that is not fundamental. A block diagram of the test circuit used to measure the THD and THD + N of the PCM78 is shown in Figure 2. This digital system is capable of differentiating harmonic energy and noise; conventional distortion analyzers which operate on a tracking notch filter principle cannot distinguish this energy, and therefore only measure THD + N. Unfortunately, in the past, these systems were used for measuring distortion performance of converters, and the distortion was often simply specified as "THD", when in fact it was really THD + N. For this reason, it is often confusing to compare specifications of converters unless one knows exactly what was being measured.

If we assume that the error due to the test circuit of Figure 2 is negligible, then the rms value of the PCM78 error referred to the input can be shown to be

$$THD + N = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N}\left[E_L(i) + E_Q(i) + E_N(i)\right]^2}}{E_{rms}} X\ 100\,\%$$

where N is the number of samples, $E_L(i)$ is the linearity error at each sample, $E_Q(i)$ is the quantization error at each

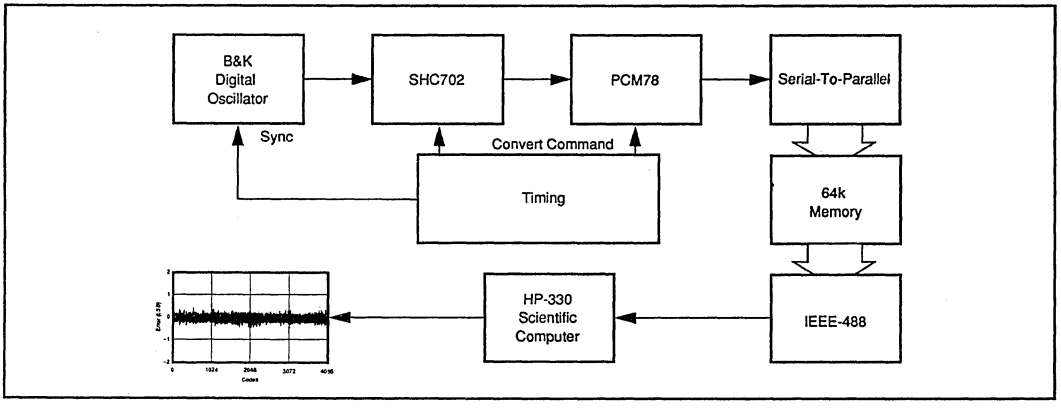


FIGURE 3. Block Diagram of Histogram Test .

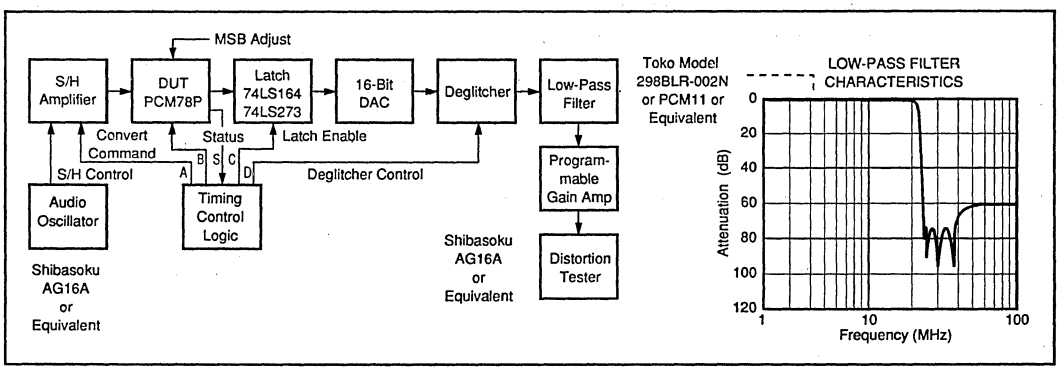


FIGURE 4. Production Distortion + Noise Test System Block Diagram.

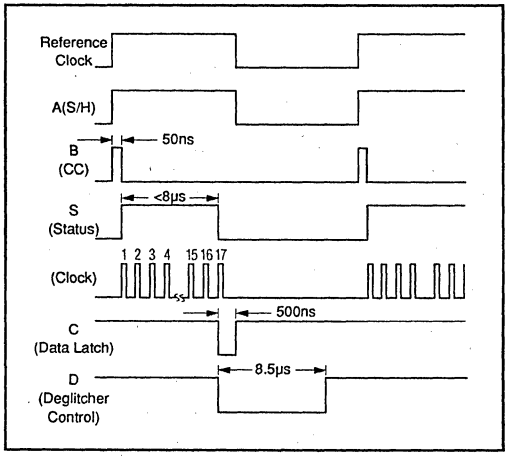


FIGURE 5. Timing Diagram for Figure 4.

sample, and $E_N(i)$ is the residual noise energy present at each sample. Similarly, THD alone can be expressed as

$$THD = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N}\left[E_L(i)\right]^2}}{E_{rms}} X\ 100\%$$

These expressions indicate that there is a correlation between THD + N and the square root of the sum of the squares of the linearity errors at each digital word of interest. In order to find this error at each code, a histogram test must be performed on the PCM78, as illustrated in Figure 3. The histogram for every converter is unique, as the linearity errors from converter to converter will vary in their placement along the transfer function. Typical histogram data is shown in the Typical Curves.

However, this expression for THD + N does not mean that the worst case linearity error of the A/D is directly correlated to the THD + N because the digital output words from the A/D vary according to the amplitude and frequency of the sine wave input as well as the sampling frequency.

For the PCM78 the test sampling frequency was chosen to be 200kHz, near the PCM78's fastest rate of conversion. The test frequencies used vary within the audio range, and are stepped in amplitude from 0dB, to –20dB, to –60dB.

In manufacturing the PCM78, the test system shown in Figure 4 is used to test for guaranteed THD + N.

ACCURACY VS CONVERSION TIME AND INPUT SIGNAL LEVEL

The relationship of THD vs input signal level and THD vs conversion time is shown is the typical curves. Slowing the conversion time to more than 8µs results in little added benefit in terms of THD + N.

For applications which are not as concerned with dynamic performance but require DC accuracy and linearity, it is best to use the PCM78 at the longest conversion time possible for the system requirements. Slowing the PCM78 to 8µs-10µs conversion time results in a substantial improvement in linearity. The typical curves show DNL and INL plots for a typical device, at an 8µs conversion time. Due to the segmented architecture of the internal DAC used in the successive approximation conversion technique, significant differential linearity errors occur near bits 3 and 4. Allowing more settling time for the DAC (by slowing the conversion speed) will improve this differential linearity error and give equivalent performance to more costly DC-specified 12-bit to 14-bit A/D converters.

SYSTEM DESIGN CONSIDERATIONS

DIGITAL CIRCUIT CONNECTIONS

The PCM78 comes complete with an internal clock circuit, or it may be clocked by an external clock. Choosing which mode to operate with depends upon the application for which the PCM78 will be used. In an application where the sample rate may not be fixed (transient recording, etc.), using the internal clock set to give a very fast conversion may be the best solution. In systems where the sample rate is fixed, an external clock is probably the better choice since it will allow the digital system design to be synchronous.

In either case, the PCM78 requires 17 clock cycles to complete a conversion. To calculate the clock frequency necessary for a given conversion time, the following equation may be used:

$$f_{CLOCK} = \frac{17}{\text{Conversion Time}}$$

The internal clock operates only during a conversion, and is gated on by the falling edge of the convert command. See Figure 6. The internal clock is available on pin 10, Clock Out. The high and low time of this clock is set by R_1C_1 and R_2C_2 respectively. The duty cycle of the clock should be between 20% to 80%, and may be set to 50% for simplicity.

$$\text{Clock High Time (in ns)} = 1.32R_1C_1$$
$$\text{Clock Low Time (in ns)} = 1.32R_2C_2$$
$$R \text{ in } k\Omega;\ C \text{ in } pF.$$

These equations are approximate (±5%); they should be used for determining an initial part value which will then need to be "tweaked" for accurate timing. If highly accurate time bases are required, use of an external clock is recommended.

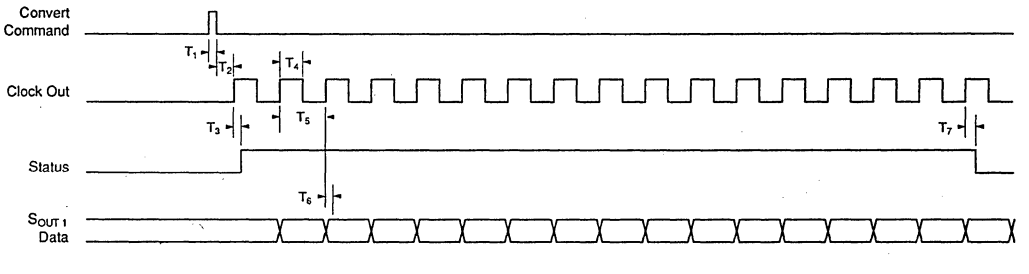
The external clock is applied at pin 16, and the Int/Ext Clock select (pin 17) should be left open (an internal pull-up resistor assures that the logical state of an open pin is "1"). Using the external clock requires careful placement in time of the convert command. Figure 7 diagrams the recommended timing with an external clock. A simple circuit which assures the proper timing of the convert command is shown in Figure 8.

Due to the design of the Clock/Logic chip in the PCM78, a conversion is begun inside the PCM78 by an asynchronous state machine. This places stringent requirements on the timing of the convert command, as improper timing can cause metastable states within this state machine. Using the circuitry shown in Figure 8, the user is assured of consistent operation, and these invalid states within the state machine are entirely avoided. (Note that this is not a consideration when using an internal clock, as nothing is being clocked when a convert command is presented to the PCM78).

The Clock Out function is a gated form of the external clock, i.e. the 17 clock cycles used in the conversion are present on this pin during conversion. This allows use of a continuous external clock, with Clock Out being the clock that the converter is actually using for conversion. Note that this is simply a delayed (~24ns) version of the external clock, and will have the same frequency and duty cycle.

The S_{OUT2} Latch enables the user to latch data from the previous conversion and read it out at a higher speed than the convert clock. This feature allows the converter to easily interface to digital filtering necessary for oversampling. See Figure 9 for timing information in this mode.

In this mode, the PCM78 generates its own internal convert command when the S_{OUT2} Clock goes high within ±50ns of S_{OUT2} Latch going low; the external convert command may not be used, and pin 19 must be grounded. The timing diagram shows the recommended timing for using this mode. After the S_{OUT2} Latch control signal goes low, data from the SAR is loaded into the S_{OUT2} latch on the next rising edge of the S_{OUT2} Clock. This clock edge should occur prior to the next rising edge of the conversion clock (internal or

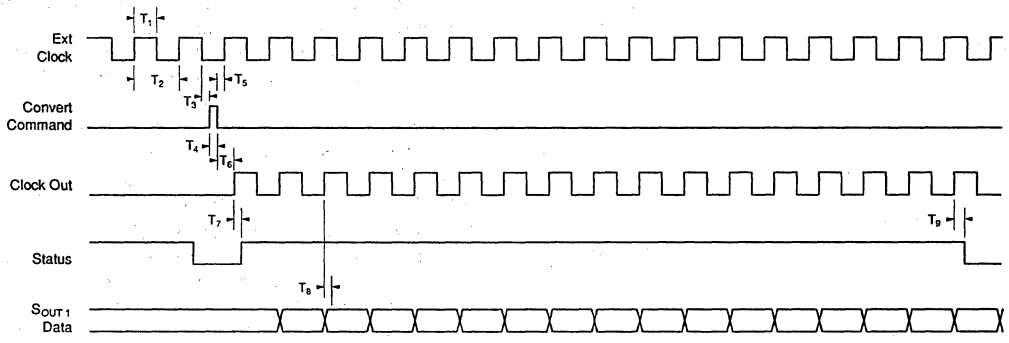


T_A = +25°C, V_{DD} = +5V, guaranteed by sample testing; these parameters are not 100% tested in production.

TIME	DESCRIPTION	TIME (ns) MIN	TYP	MAX
T_1	CONVERT COMMAND pulse width	25	50	(1)
T_2	Delay from falling edge of CONVERT COMMAND to rising edge of CLOCK OUT	60	70	85
T_3	Delay from rising edge of CLOCK OUT to rising edge of STATUS	8	10	30
T_4	INTERNAL CLOCK pulse width	50	125	450
T_5	INTERNAL CLOCK period	140	290	500
T_6	Delay from rising edge of CLOCK OUT to bit data valid	17	20	50
T_7	Delay from rising edge of 17th clock pulse to falling edge of STATUS	10	15	30

NOTE: (1) When using the internal clock, the clock does not operate until the Convert Command is low. It is therefore possible to keep the convert command high indefinitely, thereby keeping the PCM78 in a halt mode. The conversion cycle begins on the falling edge of convert command, and convert command must remain low during the entire conversion cycle in order to make the PCM78 operate properly.

FIGURE 6. Conversion Timing when using Internal Clock.



T_A = +25°C, V_{DD} = +5V, guaranteed by sample testing; these parameters are not 100% tested in production.

TIME	DESCRIPTION	TIME (ns) MIN	TYP	MAX
T_1	EXTERNAL CLOCK pulse width	50	125	(1)
T_2	EXTERNAL CLOCK period	140	290	(1)
T_3	Delay from falling edge of EXTERNAL CLOCK to rising edge of CONVERT COMMAND	–30	0	420
T_4	CONVERT COMMAND pulse width	10	50	200
T_5	Delay from falling edge of CONVERT COMMAND to rising edge of EXTERNAL CLOCK	20	50	430
T_6	Delay from falling edge of CONVERT COMMAND to rising edge of CLOCK OUT	40	75	460
T_7	Delay from rising edge of CLOCK OUT to rising edge of STATUS	6	10	30
T_8	Delay from rising edge of CLOCK OUT to bit data valid	15	17	20
T_9	Delay from rising edge of 17th clock pulse to falling edge of STATUS	8	10	30

NOTE: (1) The PCM78 does not contain dynamic digital circuitry, and can be clocked as slowly as the user wishes. In typical applications, the longest clock period may be as long as 1µs.

FIGURE 7. Conversion Timing when using External Clock.

external), since the SAR will reset itself prior to the latching if the convert clock rises before the S_{OUT2} Clock. This condition is avoided as long as the frequency of S_{OUT2} Clock is at least 1.5 times that of the conversion clock.

The internal convert command is generated upon S_{OUT2} Latch going low, and its falling edge occurs upon the first falling edge of S_{OUT2} Clock after S_{OUT2} Latch goes low. S_{OUT2} Latch should remain low for at least 2 cycles of S_{OUT2} Clock to insure proper latching. In many applications, the S_{OUT2} Latch can be the $2f_S$ signal present in many digital audio systems, typically known as WDCK. Figure 10 includes an example of this application.

The data read out on S_{OUT2} is from the conversion previously performed, while the data that is present on S_{OUT1} is the real time readout of the successive approximation as it occurs.

SHORT CYCLE

The PCM78 has the ability to be short cycled to a resolution less than 16 bits. This is accomplished by driving the Short Cycle pin (pin 18) low when the conversion is to be terminated, and holding it low until the next convert command is given. The circuit in Figure 11 will accomplish this function.

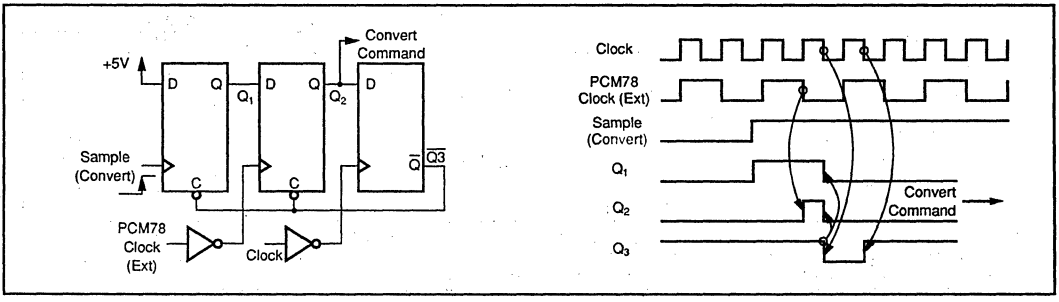
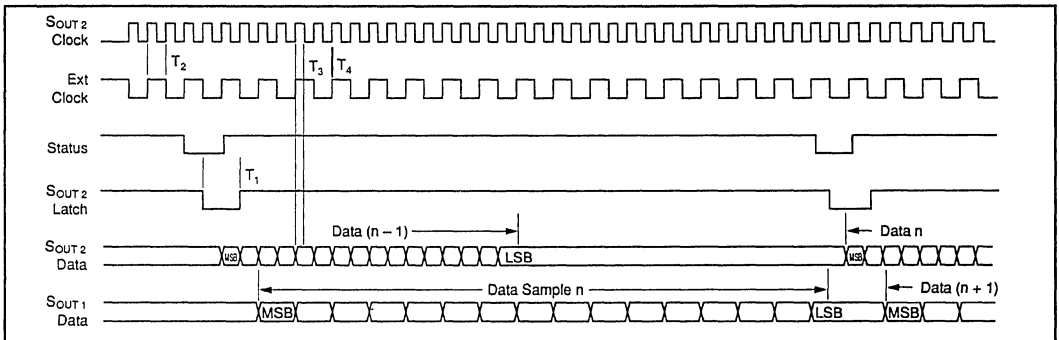


FIGURE 8. Convert Command Timing Circuit for Use with External Clock.



T_A = +25°C, V_{CC} = +5V, guaranteed by sample testing; these parameters are not 100% tested in production.

TIME	DESCRIPTION	TIME (ns) MIN	TYP	MAX
T_1	S_{OUT2} Latch pulse width	50	100	
T_2	S_{OUT2} Clock Cycle		24	
T_3	Delay from rising edge of CLOCK OUT to bit data valid		10	30
T_4	Delay from rising edge of S_{OUT2} Clock to rising edge of Ext Clock	50	125	

FIGURE 9. Timing when using S_{OUT2} Latch.

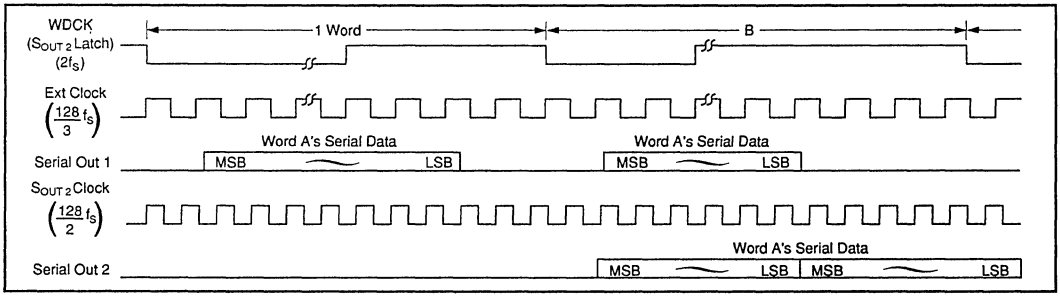
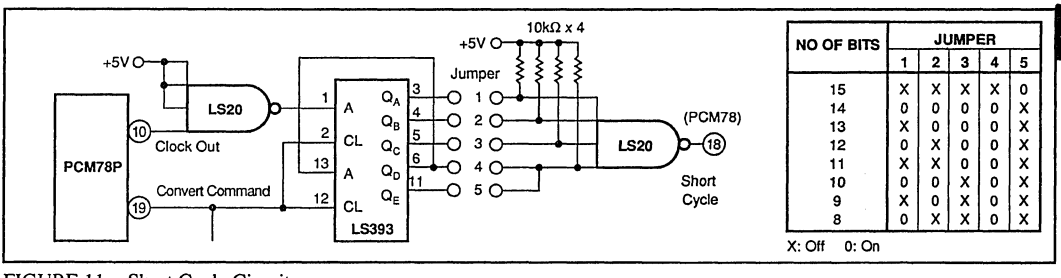


FIGURE 10. Application Example of S_{OUT2} Operation.



NO OF BITS	JUMPER 1	2	3	4	5
15	X	X	X	X	0
14	0	0	0	0	X
13	X	0	0	0	X
12	0	X	0	0	X
11	X	X	0	0	X
10	0	0	X	0	X
9	X	0	X	0	X
8	0	X	X	0	X

X: Off 0: On

FIGURE 11 . Short Cycle Circuit.

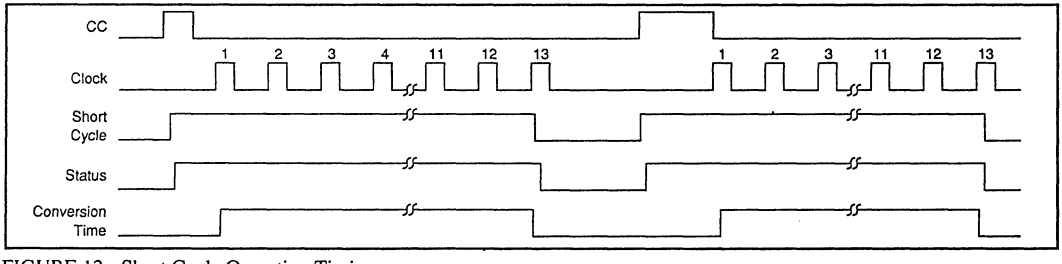


FIGURE 12. Short Cycle Operation Timing.

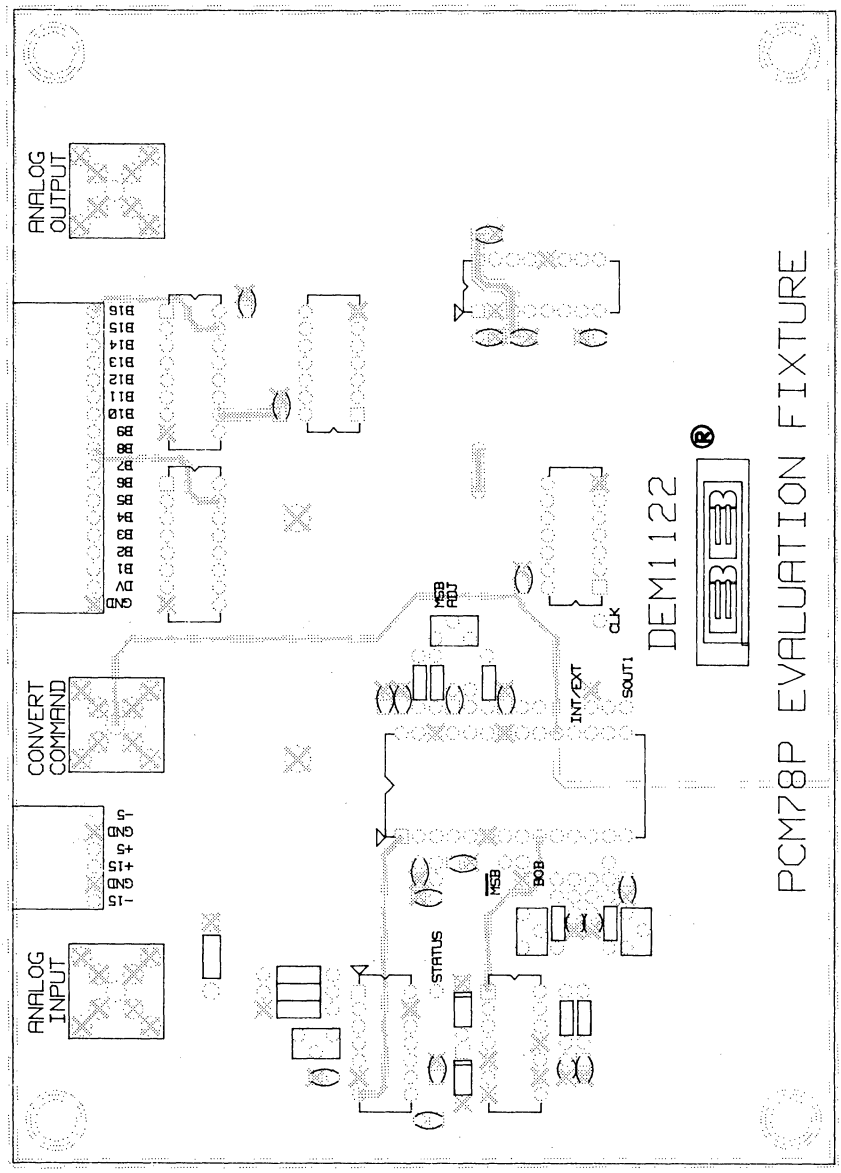


FIGURE 13a. Recommended PC Board Layout.

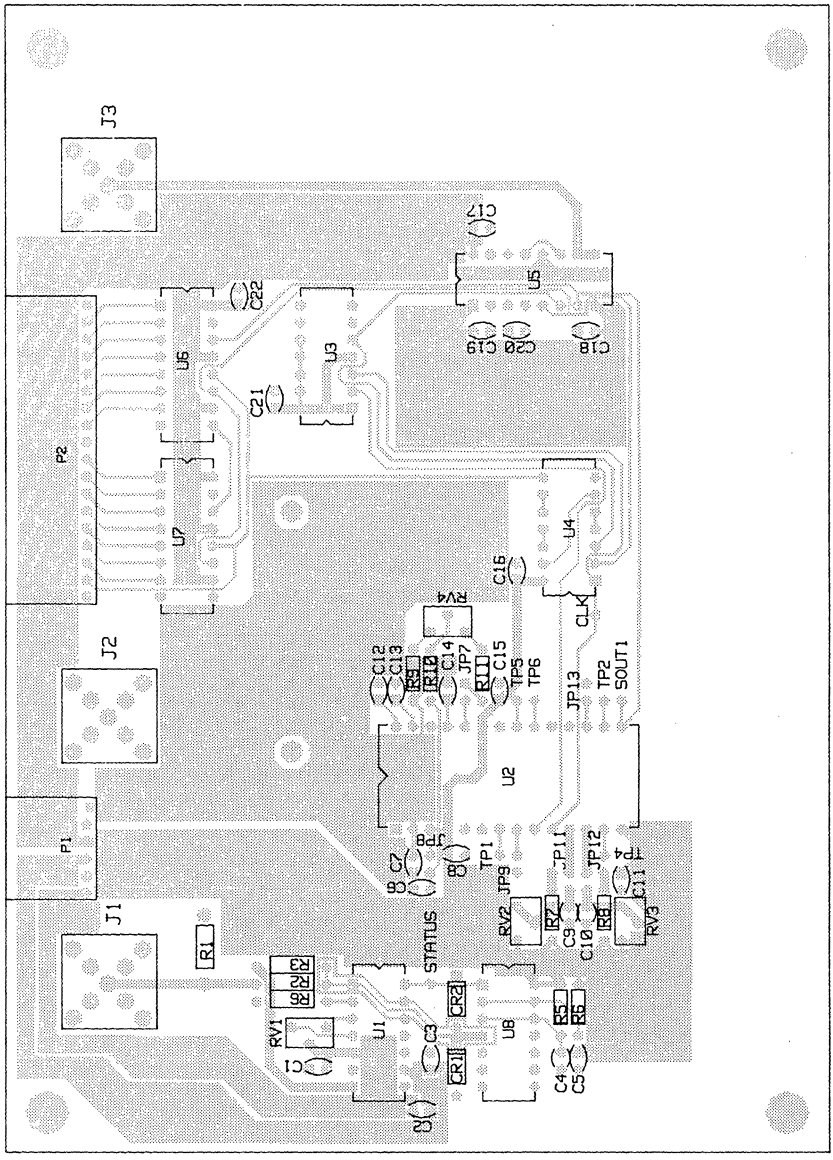


FIGURE 13b. Recommended PC Board Layout.

If Short Cycle is not held low until the next convert command is issued, the Status line will go high in synchronization with Short Cycle. This is because the operation of the Status line becomes invalid after Short Cycle is asserted. An example of the Short Cycle operation is shown in Figure 12.

In those systems where a user may not be using a continuous external clock, it is necessary to assure that a falling edge of external clock occurs after short cycle goes low. This is because conversion actually stops on the first falling edge of external clock after Short Cycle goes low.

ANALOG CIRCUIT CONSIDERATIONS

Layout Precautions

Analog and Digital Common are connected internally in the PCM78, and should be connected together as close to the unit as possible, preferably to a large ground plane under the ADC. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The input pin (pin 1) and the MSB adjust pin (pin 3) are both extremely sensitive to noise; digital lines should be kept away from these pins to avoid coupling digital noise into the sensitive analog circuitry.

Figure 13 shows a recommended PCB layout for the PCM78.

Power Supply Decoupling

The power supplies should be bypassed with tantalum or electrolytic capacitors as shown in Figure 14 to obtain noise free operation. These capacitors should be located as close to the ADC as possible. Bypass the 1µF electrolytic capacitors with 0.01µF ceramic or polystyrene capacitors for improved high frequency performance.

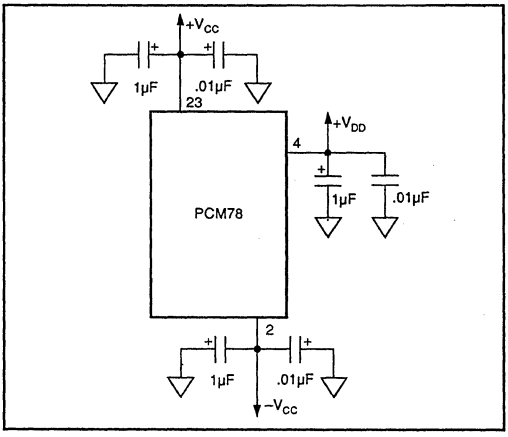


FIGURE 14. Recommended Power Supply Decoupling.

Reference Decoupling and Speed Up

In order to assure the lowest noise operation of the PCM78, the reference may be bypassed by three different capacitors. Pin 25 is a decoupling point for the reference to $-V_{CC}$. The decoupling capacitor should range from 0.1µF to 4.7µF; larger values can cause reference settling problems which may manifest themselves as missing codes. This capacitor should be as close to the PCM78 as possible, to minimize the potential for coupling noise into the device; with a good board layout it may be best to leave this capacitor out of the circuit altogether, as the extra lead length may only cause more noise in the reference.

Pin 27 is a decoupling point to ground, as well as the output of the 2V reference. This point should not be used to supply reference voltage to external circuitry unless it is buffered. A 2.2µF capacitor is recommended, and the capacitor used here should not exceed 4.7µF.

Pin 28, the Speed Up pin, allows a capacitor to be connected to ground to facilitate reference settling. This does not speed up the conversion time, but it does reduce odd order harmonic distortion. As with the decoupling capacitor on pin 25, this may also contribute to noise; if harmonic content is most important in an application, this capacitor (0.1µF - 10µF) should be connected. In all other cases, it is best to leave the capacitor out of the circuit.

Input Scaling

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. The DAC inside the PCM78 has a ±2mA range, and the nominal ±3V input is scaled by a 1.5kΩ resistor. In order to scale to other ranges, see Table I for recommended scaling resistor values, connected as shown in Figure 15.

INPUT RANGE	R
±10V	8.2kΩ
±5V	3.3kΩ
NOTE: R values shown assume use of 1k trim pot to adjust for scale accuracy.	

TABLE I. PCM78 Input Scaling Resistor Values.

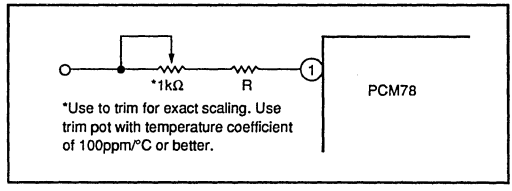


FIGURE 15. PCM78 Input Scaling Circuit.

INPUT IMPEDANCE

The input signal to the PCM78 should come from a low impedance source, such as the output of an op amp, to avoid any errors due to the dynamic input impedance that a successive-approximation converter presents to the the outside world because of the changing currents in this circuit during conversion as the converter steps through its approximations.

If the driving circuit output impedance is not low, a buffer amplifier should be added between the input signal and the direct input to the PCM78 as shown in Figure 16.

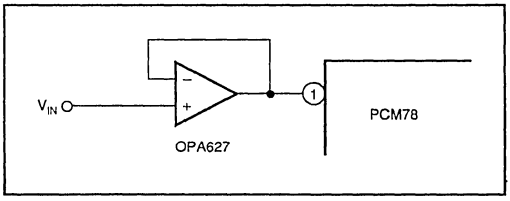


FIGURE 16. Buffer Amplifier for PCM78 Input.

MSB Adjustment

Differential Linearity errors at bipolar zero and THD are guaranteed to meet data sheet specifications without any external adjustment. However, a provision has been made for an optional adjustment of the MSB linearity point which makes it possible to eliminate DLE error at BPZ. This is important when the signal level is very low, because zero crossing noise (DLE at BPZ) becomes very significant when compared to the small codes changes occurring in the LSB portion of the converter.

The PCM78 is laser trimmed for best performance at the factory without the MSB adjust circuitry installed; if better performance can be obtained it would be by the addition of the MSB adjust circuitry shown in Figure 17.

The best method of adjusting the MSB is by using a real time FFT routine to monitor the levels of odd order harmonics when a sine-wave is being digitized by the PCM78. Adjusting the potentiometer in Figure 17 will allow the user to reduce the magnitude of odd-order harmonics.

An alternate method is to recontruct the data out of the PCM78 through a DAC, and measure THD+N on a conventional distortion analyzer. Adjust the potentiometer for minimum THD+N.

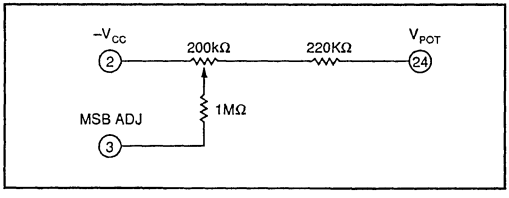


FIGURE 17. MSB Adjust Circuit.

APPLICATIONS INFORMATION

A typical digitization circuit, used on the demonstration board available for the PCM78, is shown in Figure 21. The connections and part values shown in this circuit have been optimized for the best THD+N performance at a 200kHz sample rate.

The PCM78 may be interfaced to many popular digital signal processors, such as the TMS320, DSP56001, and the DSP32. Suggested interface circuits for these processors are shown in Figures 18-20.

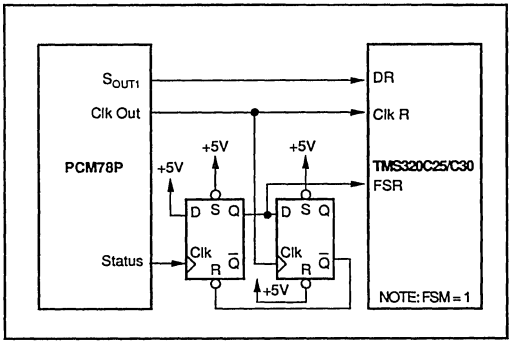


FIGURE 18. PCM78 Interface to TMS320C25/C30 DSP Processors.

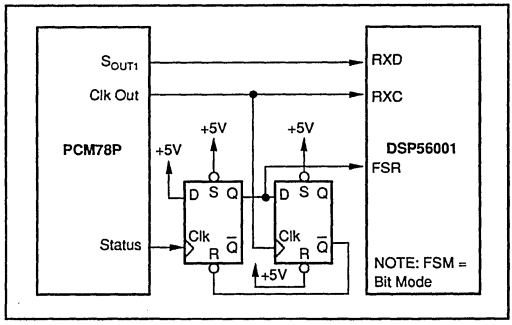


FIGURE 19. PCM78 Interface to Motorola DSP56001 DSP Processor.

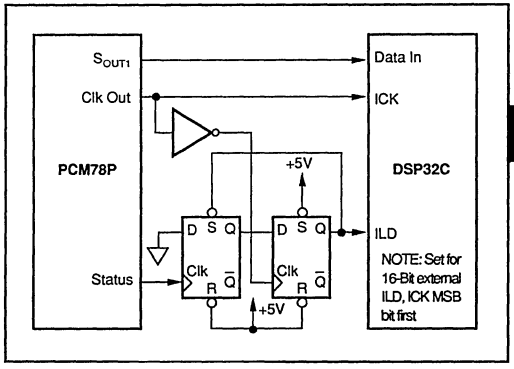


FIGURE 20. PCM78 Interface to AT&T DSP16 & DSP32C Processors.

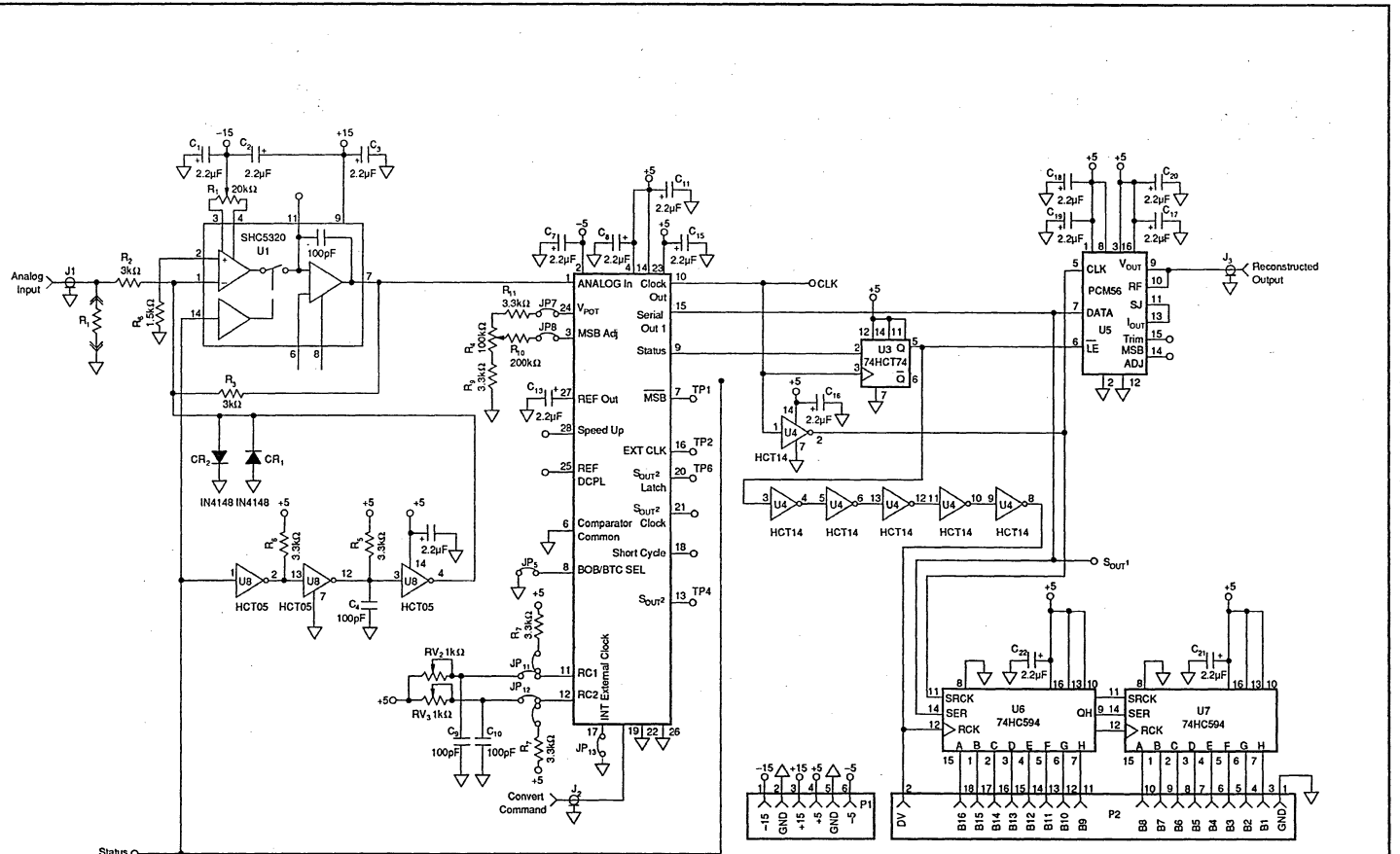


FIGURE 21. Schematic for Demonstration Board (DEM1122).

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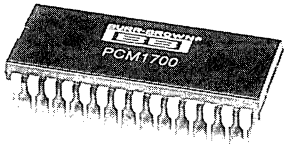


PCM1700P

ADVANCE INFORMATION
SUBJECT TO CHANGE

Dual 18-Bit Monolithic Audio DIGITAL-TO-ANALOG CONVERTER

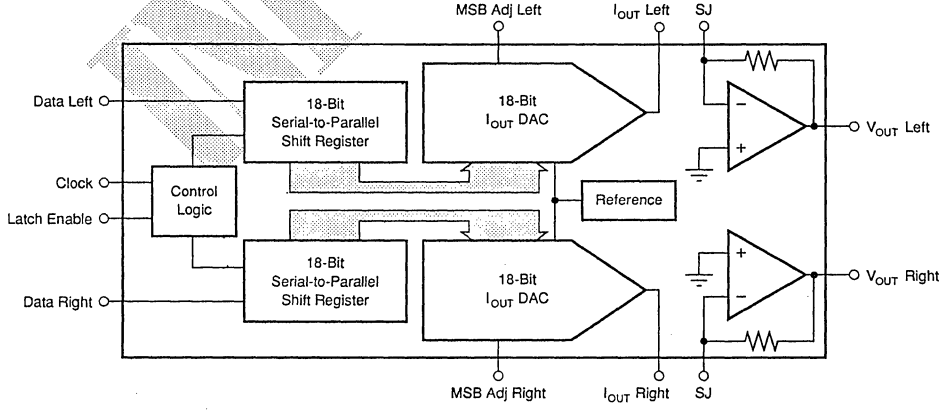
FEATURES

- DUAL 18-BIT LOW-POWER MONOLITHIC AUDIO D/A CONVERTER
- VERY LOW MAX THD+N: –92dB Without External Adjust
- CO-PHASE, GLITCH-FREE ±3V OR ±670µA AUDIO OUTPUTS
- CAPABLE OF 16X PER CHANNEL OVER-SAMPLING RATE
- COMPLETE WITH INTERNAL REFERENCE
- SERIAL INPUT FORMAT 100% COMPATIBLE WITH INDUSTRY STD PCM56P
- RUNS ON ±5V SUPPLIES AND DISSIPATES 300mW MAX
- COMPACT 28-PIN PLASTIC DIP

DESCRIPTION

The PCM1700P is a low cost, high-performance dual 18-bit digital-to-analog converter. The PCM1700P features true glitch-free, co-phase current and voltage outputs and only requires ±5V supplies. The PCM1700P comes complete with an internal reference and optional MSB adjustability for even greater THD performance. Total power dissipation is less than 400mW max. Low maximum Total Harmonic Distortion + Noise (–92dB max; PCM1700P-K) is 100% tested. The very fast PCM1700P is also capable of 16-times oversampling rates on both channels simultaneously, providing freedom in output filter selection.

The PCM1700P comes in space-saving 28-pin plastic DIP and SOIC packages. PCM1700P accepts a serial data input format that is compatible with other Burr-Brown PCM products such as the industry standard PCM56P.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1035

SPECIFICATIONS

ELECTRICAL

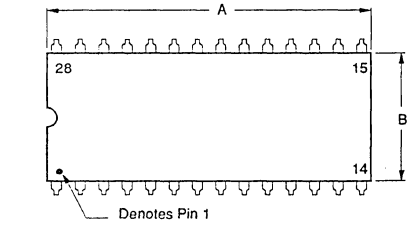
At 25°C, and $\pm V_{CC}$ = ±5.00V unless otherwise noted. Where relevant, specifications apply to both left and right input/output channels.

PARAMETER	CONDITIONS	PCM1750P/P-J/P-K MIN	TYP	MAX	UNITS
RESOLUTION		18			Bits
DYNAMIC RANGE			+108		dB
INPUT					
DIGITAL INPUT					
Logic Family			TTL Compatible		
Logic Level: V_{IH}		+2		$+V_{CC}$	V
V_{IL}		0		–0.8	V
I_{IH}	V_{IH} = +2.7V			+1	µA
I_{IL}	V_{IL} = +0.4V			–50	µA
Data Format			Serial BTC[1]		
Input Clock Frequency				16.9	ns
DYNAMIC CHARACTERISTICS					
TOTAL HARMONIC DISTORTION + N[6]					
PCM1700P:					
f = 991kHz (0dB)	f_S = 705.6kHz[4]		–88	–82	dB
f = 991kHz (–20dB)	f_S = 705.6kHz		–74	–68	dB
f_{IN} = 991kHz (–60dB)	f_S = 705.6kHz		–34	–28	dB
PCM1700P-J:					
f = 991kHz (0dB)	f_S = 705.6kHz		–94	–88	dB
f = 991kHz (–20dB)	f_S = 705.6kHz		–76	–74	dB
f = 991kHz (–60dB)	f_S = 705.6kHz		–36	–34	dB
PCM1700P-K:					
f = 991kHz (0dB)	f_S = 705.6kHz		–98	–92	dB
f = 991kHz (–20dB)	f_S = 705.6kHz		–80	–74	dB
f = 991kHz (–60dB)	f_S = 705.6kHz		–40	–34	dB
CHANNEL SEPARATION		+96	+108		dB
SIGNAL-TO NOISE RATIO[5]	20Hz to 20kHz at BPZ[6]		+108		dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error			±1	±3	%
Gain Mismatch	Channel to Channel		±1	±3	%
Bipolar Zero Error			10		mV
BPZ Error Mismatch	Channel to Channel		5		mV
BPZ Differential Linearity Error[7]			±1		LSB
Gain Drift			100		ppm/°C
Bipolar Zero Drift			20		ppm of FSR/°C
Warm-up Time		1			minute
POWER SUPPLY REJECTION	$\pm V_{CC}$ TO V_{OUT}		+86		dB
ANALOG OUTPUT					
Voltage: Output Range			±3		V
Output Impedance			0.1		Ω
Current Output			±8		mA
Capacitive Load Drive	R_{LOAD} = 1.5kΩ		TBD		pF
Short Circuit Duration			Indefinite		
Settling Time			Sufficient to Meet THD + N Specs		
Glitch Energ			Meets All THD + N Specs Without External Output Deglitching		
Current: Output Range	(±2%)		±670		µA
Output Impedance	(±2%)		1.67		kΩ
POWER SUPPLY REQUIREMENTS					
$\pm V_{CC}$ Supply Voltage		+4.75	+5.00	+5.25	V
Supply Current: $+I_{CC}$	$+V_{CC}$ = +5.0V		–40		mA
$-I_{CC}$	$-V_{CC}$ = –5.0V		+16		mA
Power Dissipation	$\pm V_{CC}$ = ±5.0V		280	380	mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–30		+70	°C
Storage		–60		+100	°C

NOTES: (1) Binary Two's Complement coding. (6) Ratio of (Distortion$_{RMS}$ + Noise$_{RMS}$) / Signal$_{RMS}$. (3) D/A converter input frequency/signal level on both left and right channels. (4) D/A converter sample frequency (16 X 44.1kHz; 16 times oversampling per channel). (5) Ratio of Noise$_{RMS}$/Signal$_{RMS}$. Measured using an A-weighted filter. (6) Bipolar zero. (7) Differential non-linearity at bipolar major carry input code. Measured in 16-bit LSB's. Adjustable to zero error.

MECHANICAL

P Package — 28-Pin Plastic DIP

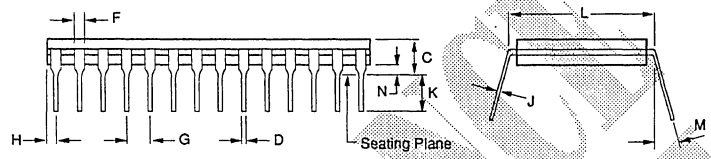


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.360	1.470	34.54	37.34
B	.500	.550	12.70	13.97
C	—	.200	—	5.08
D	.015	.021	0.38	0.53
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.007	.013	0.18	0.33
K	.100	—	2.54	—
L	.600 BASIC		15.24 BASIC	
M	—	15°	—	15°
N	.020	.090	0.51	2.29

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers are shown for reference only. Numbers may not be marked on package.

Case: Plastic

Weight: 4.3 grams (0.15oz.)



PIN ASSIGNMENTS

PIN	DESCRIPTION	MNEMONIC
1	–5V Analog Supply	$-V_{CC}$
2	Left Channel Servo-Amp Decoupling Point	CAP
3	Left Channel MSB Adjustment	MSB ADJ (L)
4	No Connect	NC
5	Left Channel Bipolar Offset Decoupling Point	CAP
6	Left Channel Current Output	IOUT (L)
7	Left Channel Analog Common	ACOM
8	Left Channel Summing Junction	SJ (L)
9	Left Channel Voltage Output	VOUT (L)
10	No Connect	NC
11	+5V Digital Supply	$+V_{DD}$
12	Left Channel Data Input	DATA
13	Clock Input	CLOCK
14	–5V Logic Supply	$-V_{DD}$
15	Latch Enable Input	LE
16	Right Channel Data Input	DATA (R)
17	Digital Common	DCOM
18	No Connect	NC
19	Right Channel Voltage Output	VOUT (R)
20	Right Channel Summing Junction	SJ (R)
21	Right Channel Analog Common	ACOM
22	Right Channel Current Output	IOUT (R)
23	Right Channel Bipolar Offset Decoupling Point	CAP
24	Right Channel MSB Adjustment	MSB ADJ (R)
25	Right Channel Servo-Amp Decoupling Point	CAP
26	MSB Adjustment Potentiometer Voltage Output	VPOT
27	+5V Analog Supply	$+V_{CC}$
28	Reference Decoupling Point	CAP

DIGITAL INPUT	ANALOG OUTPUT		
Binary Two's Complement (BTC)	DAC Output	Voltage (V) V_{OUT} Mode	Current (mA) I_{OUT} Mode
1FFFF Hex	+ FS	+2.99997711	–0.66999489
00000 Hex	BPZ	0.00000000	0.00000000
3FFFF Hex	BPZ – 1LSB	–0.00002289	+0.00000511
20000 Hex	– FS	–3.00000000	+0.67000000

TABLE I. PCM1700 Input/Output Relationships.

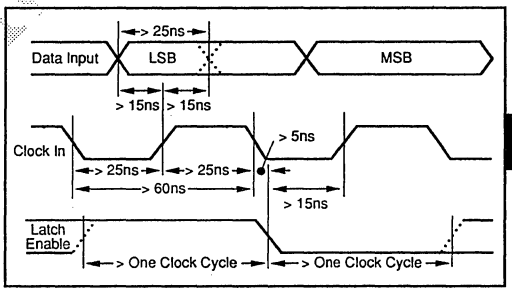


FIGURE 1. PCM1700P Setup and Hold Timing Diagram.

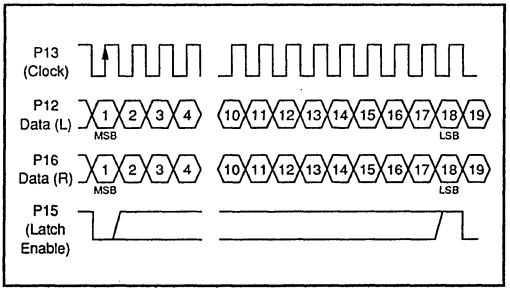


FIGURE 2. Timing Diagram.

ORDERING INFORMATION

PCM1700P ( )

Basic Model Number
P: Plastic
Performance Grade Code

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltages	±7.5VDC
Input Logic Voltage	–1V to $+V_{CC}$
Power Dissipation	500mW
Operating Temperature	–25°C to +70°C
Storage Temperature	–60°C to +100°C
Lead Temperature (soldering, 10s)	+300°C

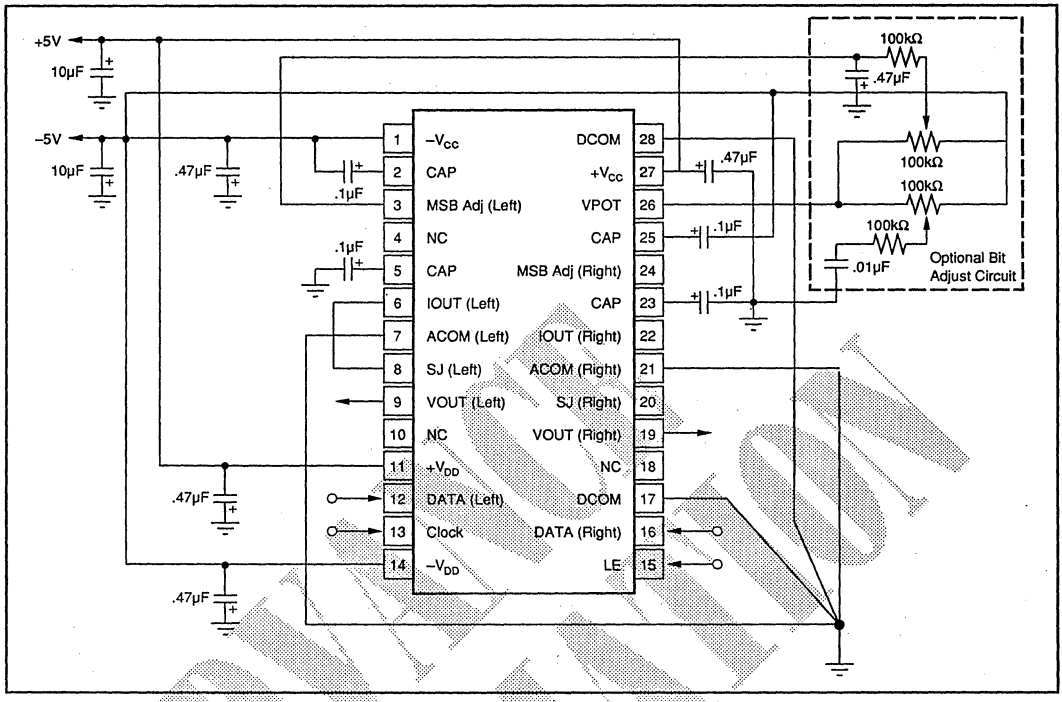


FIGURE 3. Voltage Output Connection Diagram.

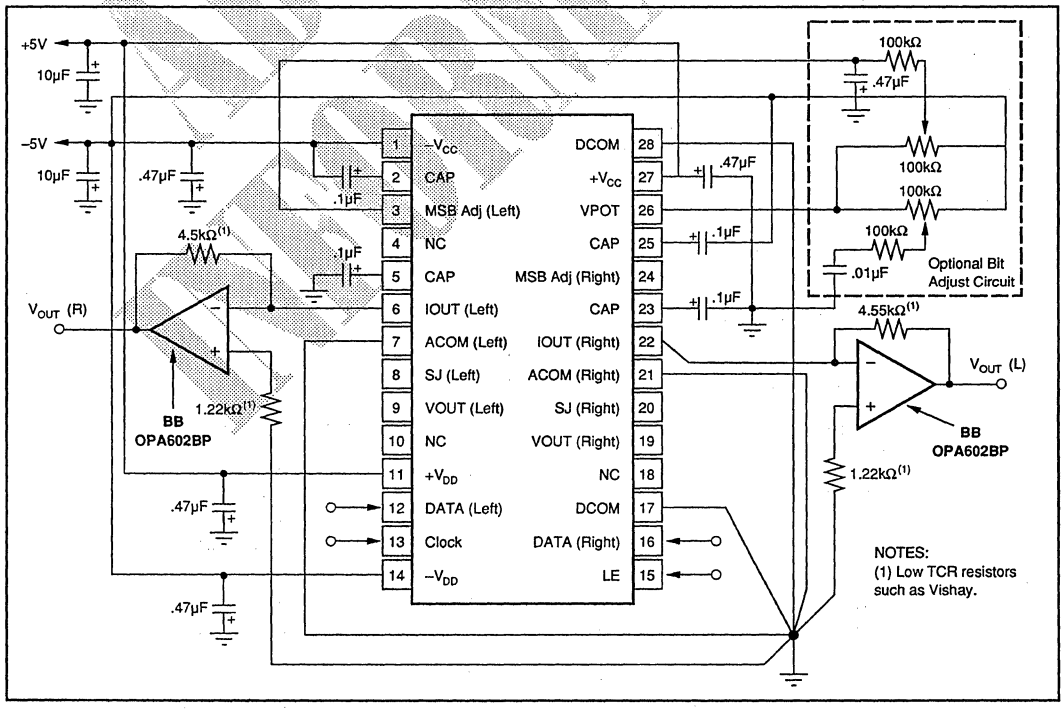


FIGURE 4. Current Output Connection Diagram.

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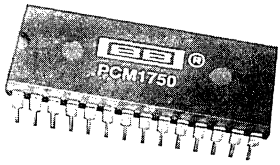


PCM1750P

ADVANCE INFORMATION
SUBJECT TO CHANGE

Dual CMOS 18-Bit Monolithic Audio ANALOG-TO-DIGITAL CONVERTER

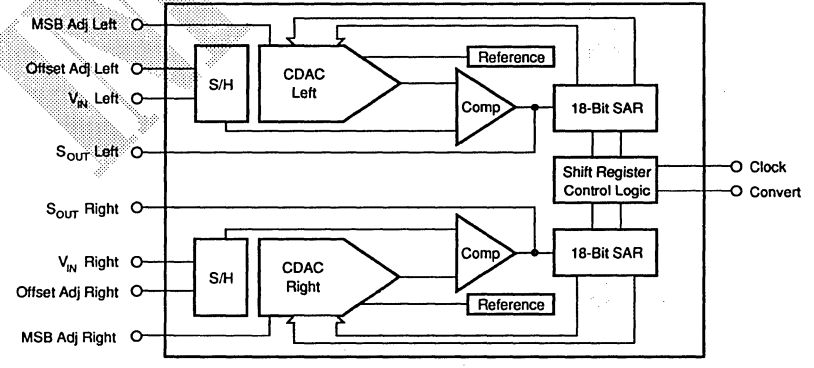
FEATURES

- DUAL18-BIT LOW-POWER CMOS AUDIO A/D CONVERTER
- FAST 4.5µs MIN CONVERSION TIME INCLUDING S/H
- VERY LOW MAX THD+N: –88dB Without External Adjust
- COMPLETE WITH INTERNAL REFERENCE AND DUAL S/H AMPLIFIERS
- TWO CO-PHASE SAMPLED, ±2.75V AUDIO INPUTS
- CAPABLE OF 4X PER CHANNEL OVERSAMPLING RATE
- RUNS ON ±5V SUPPLIES AND DISSIPATES 300mW MAX
- COMPACT 28-PIN PLASTIC DIP

DESCRIPTION

The PCM1750P is a low cost, dual 18-bit CMOS analog-to-digital converter optimized for dynamic signal applications. The PCM1750P features true co-phased inputs with internal sample/hold amplifiers for each channel. The PCM1750P also comes complete with an internal reference. Total power dissipation is less than 300mW max using ±5V voltage supplies. Low maximum Total Harmonic Distortion + Noise (–88dB max) is 100% tested. The very fast PCM1750P is capable of 4-times oversampling rates on both input channels simultaneously, providing greater freedom to designers in selecting input anti-aliasing filters.

PCM1750P outputs serial data in a format that is compatible with many digital filter chips and comes packaged in a space saving 28-pin plastic DIP.



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PDS-1084

SPECIFICATIONS

ELECTRICAL

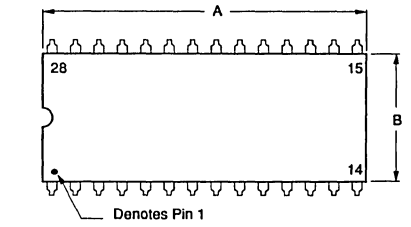
At 25°C, and $\pm V_{CC}$ = ±5.0V and $+V_{DD}$ = +5.0V unless otherwise noted. Where relevant, specifications apply to both left and right input/output channels.

PARAMETER	CONDITIONS	PCM1750P MIN	PCM1750P TYP	PCM1750P MAX	UNITS
RESOLUTION		18			Bits
INPUT/OUTPUT					
ANALOG INPUT					
Input Range		–2.75		+2.75	V
Input Capacitance			20		pF
Aperture Time			25		ns
Aperture Jitter			50		ps
Full Power Bandwidth			25		kHz
DIGITAL INPUT/OUTPUT					
Logic Family			Compatible CMOS		
Logic Level: V_{IH}	I_{IH} = +5 uA	+3.5			$+V_{DD}$
V					
V_{IL}	I_{IL} = +5 uA	0.0		+1.5	V
V_{OH}	I_{OH} = 2 TTL Loads	+2.7			V
V_{OL}	I_{OL} = 2 TTL Loads			+0.4	V
Data Format			Serial BTC(1)		
Convert Command			Positive edge		
Convert Command Pulse Width			81		ns
CONVERSION TIME	Throughput Including S/H	4.5	5.2	20.8	µs
DYNAMIC CHARACTERISTICS					
SIGNAL-TO NOISE RATIO[2]	f_S = 192kHz/channel[3] f_{IN} = 1kHz (0dB)[4]				
PCM1750P		+88	+90		dB[5]
TOTAL HARMONIC DISTORTION + N[6]					
PCM1750P:					
f_{IN} = 1kHz (0dB)	f_S = 192kHz		–90	–88	dB
f_{IN} = 1kHz (–20dB)	f_S = 192kHz		–70	–68	dB
f_{IN} = 1kHz (–60dB)	f_S = 192kHz		–30	–28	dB
CHANNEL SEPARATION	f_S = 192kHz/channel f_{IN} = 1kHz (0dB)	+96	+108		dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error			±2	±5	%
Gain Mismatch	Channel to Channel		±0.5	±1	%
Bipolar Zero Error[7]			±2		mV
BPZ Error Mismatch	Channel to Channel		±3		mV
BPZ Differential Linearity Error[8]			±0.002		% of FSR[9]
Linearity Error			±0.003		% of FSR
Warm-up Time		1			minute
DRIFT					
Gain	0°C to 70°C		100	250	ppm/°C
Bipolar Zero	0°C to 70°C		20		ppm of FSR/°C
POWER SUPPLY REJECTION	$\pm V_{CC}$ TO V_{IN}		TBD		dB
POWER SUPPLY REQUIREMENTS					
$\pm V_{CC}$ Supply Voltage		±4.75	±5.00	±5.25	V
Supply Current: $+I_{CC}$ and $+I_{DD}$	$+V_{CC}$ and $+V_{DD}$ = +5.0V		+28		mA
$-I_{CC}$	$-V_{CC}$ = –5.0V		–13		mA
Power Dissipation	$\pm V_{CC}$ = ±5.0V		210	300	mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–30		+70	°C
Storage		–60		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of $Signal_{RMS}$ / $Noise_{RMS}$ from20 Hz to 20kHz. (3) A/D converter sample frequency (4 X 48kHz; 4 times oversampling per channel). (4) A/D converter input frequency/signal level (on both left and right channels).(5) Refered to input signal level. (6) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$) / $Signal_{RMS}$. (7) Externally adjustable to zero error. (8) Differential non-linearity at bipolar major carry input code. Measured in 16-bit LSB's. Adjustable to zero error. (9) Full Scale Range.

MECHANICAL

P Package — 28-Pin Plastic DIP

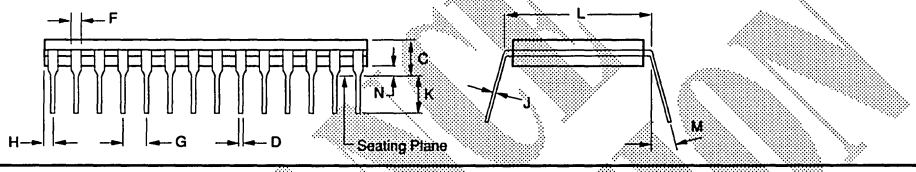


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.360	1.470	34.54	37.34
B	.500	.550	12.70	13.97
C	—	.200	—	5.08
D	.015	.021	0.38	0.53
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.007	.013	0.18	0.33
K	.100	—	2.54	—
L	.600 BASIC		15.24 BASIC	
M	—	15°	—	15°
N	.020	.090	0.51	2.29

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers are shown for reference only. Numbers may not be marked on package.

Case: Plastic

Weight: 4.3 grams (0.15oz.)



ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$ Supply Voltage	±7V
Input Logic Voltage	−0.5V to $+V_{CC}$
Storage Temperature	−65°C to +165°C
Lead Temperature (soldering, 10s)	+300°C

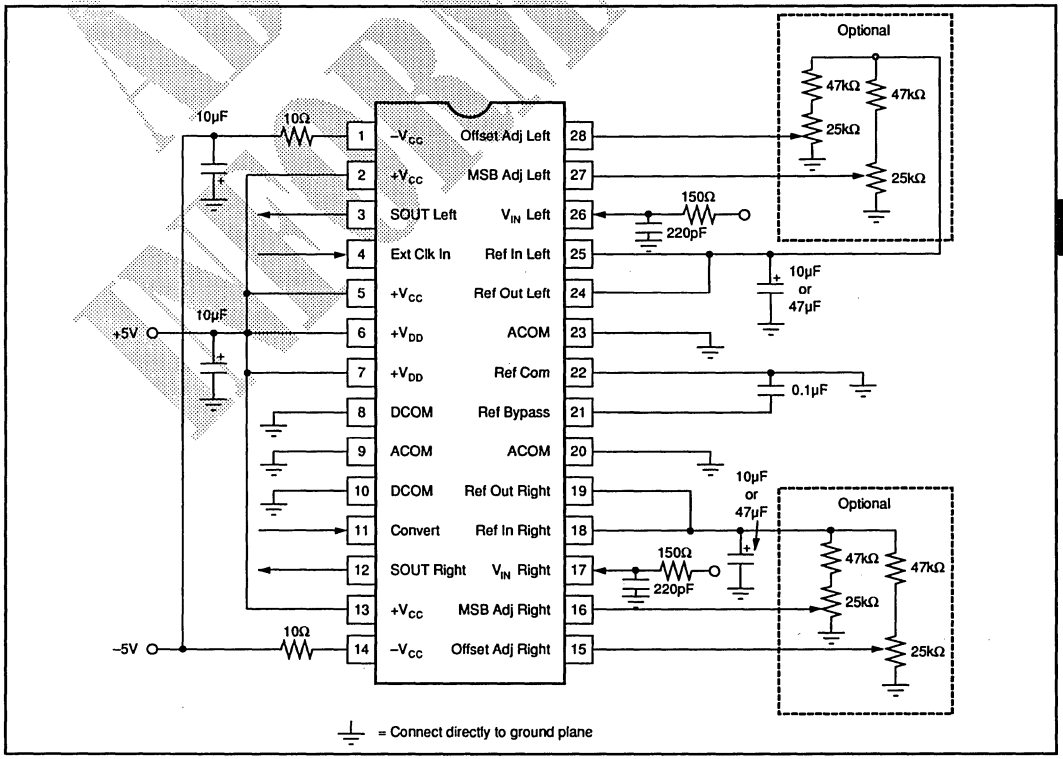
ORDERING INFORMATION

PCM1750 P

Basic Model Number

Package Code
P: Plastic

CONNECTION DIAGRAM



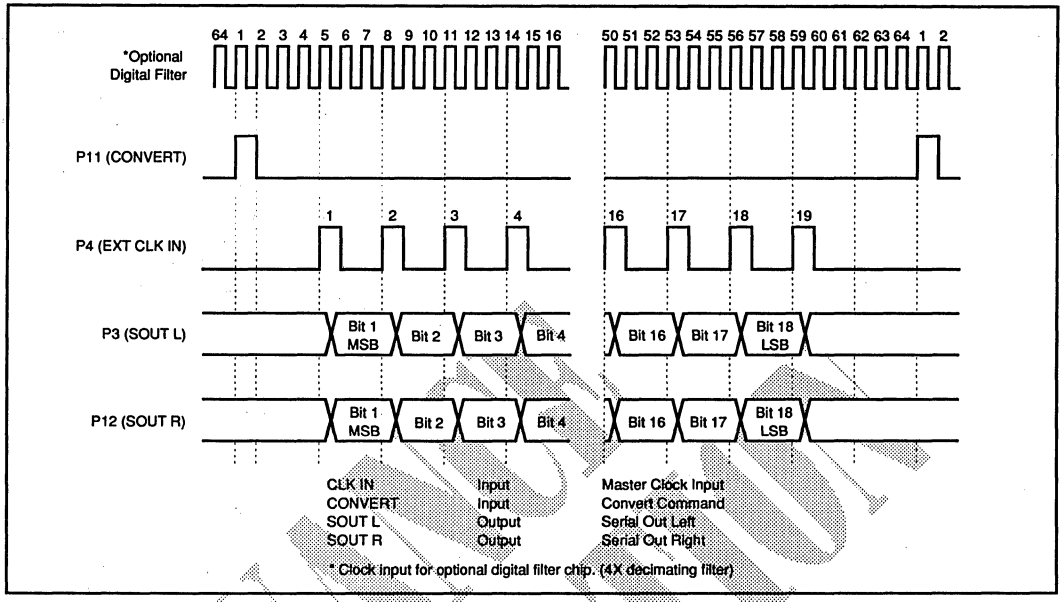
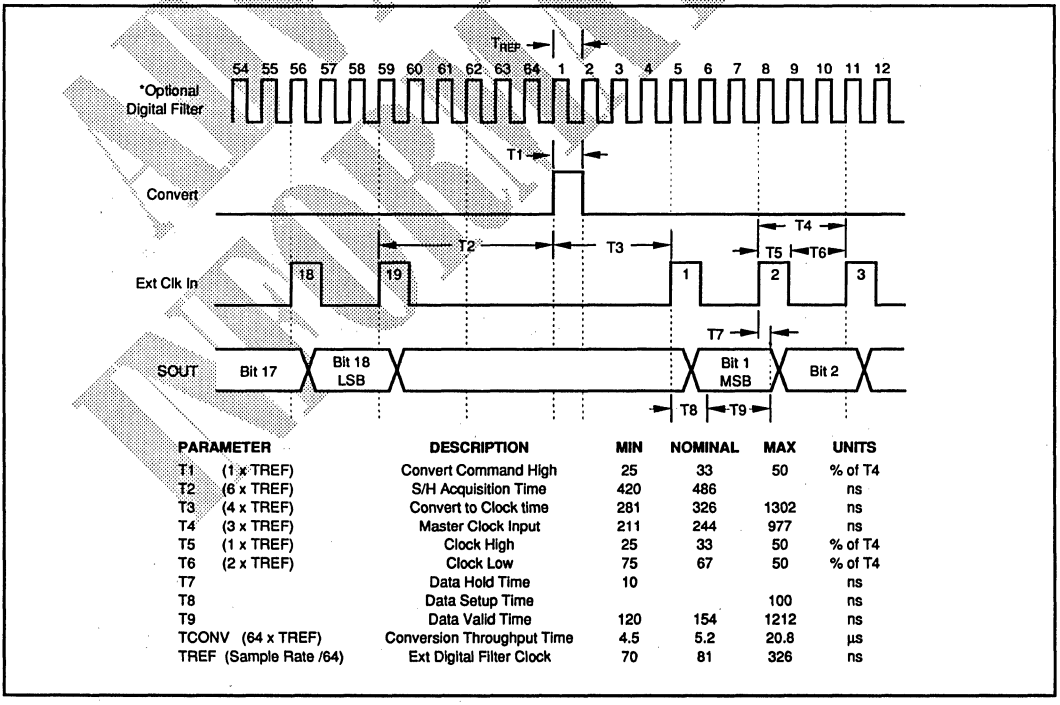


FIGURE 1. Input/Output Timing Diagram.



PARAMETER	DESCRIPTION	MIN	NOMINAL	MAX	UNITS
T1 (1 x TREF)	Convert Command High	25	33	50	% of T4
T2 (6 x TREF)	S/H Acquisition Time	420	486		ns
T3 (4 x TREF)	Convert to Clock time	281	326	1302	ns
T4 (3 x TREF)	Master Clock Input	211	244	977	ns
T5 (1 x TREF)	Clock High	25	33	50	% of T4
T6 (2 x TREF)	Clock Low	75	67	50	% of T4
T7	Data Hold Time	10			ns
T8	Data Setup Time			100	ns
T9	Data Valid Time	120	154	1212	ns
TCONV (64 x TREF)	Conversion Throughput Time	4.5	5.2	20.8	µs
TREF (Sample Rate /64)	Ext Digital Filter Clock	70	81	326	ns

FIGURE 2. Setup and Hold Timing Diagram.

VOLTAGE-TO-FREQUENCY CONVERTERS

Voltage-to-frequency converters provide a simple, low-cost way of converting analog signals into digital form. They provide an important alternative to other analog-to-digital conversion techniques. Their integrating input properties make them an appropriate choice when operating in noisy environments. The combination of high accuracy and linearity, low temperature drift, and monotonicity often provides performance characteristics unattainable with other techniques.

Since an analog quantity represented as a frequency is inherently serial data, it is easily handled in large multi-channel systems. Frequency information can be transmitted over long lines with excellent noise immunity using low cost digital line transmitters and receivers. Isolation can be accomplished with optical or transformer couplers without loss in accuracy. Outputs from multiple VFCs can be gated to common counter circuitry with simple digital logic. Low-cost isolation is obtained when a VFC is used together with a DC/DC converter and a single optical coupler.

Burr-Brown monolithic voltage-to-frequency converters provide industry-standard performance and reliability in such applications as precision test and measurement equipment, data acquisition systems, communications equipment, and process control.

VOLTAGE-TO-FREQUENCY CONVERTERS SELECTION GUIDE

The Selection Guide shows parameters for the high grade. Refer to the Product Data Sheet for a full selection of grades. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book.*

VOLTAGE-TO-FREQUENCY CONVERTERS — **Boldface = NEW**

Description	Model	Frequency Range (kHz)	V_{IN} Range (V)	Linearity, max (% of FSR)	Tempco, max (ppm of FSR/°C)	Temp Range[1]	Pkg	Page
Low-Cost Monolithic	VFC32P, U VFC32M, L	User-selected 500kHz, max	User-selected	±0.01 at 10kHz ±0.05 at 100kHz	75 typ ±100	Com Ind	DIP, SOIC TO-100, LCC	10-3 10-3
Low-Cost Complete	VFC42 VFC52	0 to 10 0 to 100	0 to +10 0 to +10	±0.01 ±0.05	±100 ±150	Ind Ind	DIP DIP	10-12 10-12
Precision Monolithic	VFC62 VFC320	User-selected	User-selected 1MHz max	±0.002 at 10kHz ±0.002 at 10kHz	±20 ±20	Ind Ind	DIP, TO-100 LCC	10-18 10-54
Synchronized Monolithic	VFC100G	Clock Programmed 2MHz max	0 to +10	0.1 at 1MHz	±50	Ind	DIP	10-26
	VFC101N	Clock Programmed, 2MHz max	0 to +10, 0 to +5, 0 to +8, –5 to +5	±0.02 at 100kHz	±40	Ind	PLCC	10-41
High-Performance	**VFC110**	**User-selected 4MHz max**	**0 to +10**	**±0.05 at 1MHz**	**±50**	**Ind**	**DIP, LCC**	**S10-3**
Single Supply, Low Power	**VFC121**	**User-selected 1.5MHz max**	**User-selected**	**±0.03 at 100kHz**	**±40**	**Ind**	**DIP**	**S10-11**

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C.

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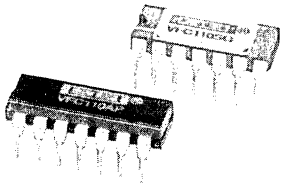


VFC110

High-Frequency VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

- HIGH-FREQUENCY OPERATION: 4MHz FS max
- EXCELLENT LINEARITY: ±0.02% typ at 2MHz
- PRECISION 5V REFERENCE
- DISABLE PIN
- LOW JITTER

APPLICATIONS

- INTEGRATING A/D CONVERSION
- PROCESS CONTROL
- VOLTAGE ISOLATION
- VOLTAGE-CONTROLLED OSCILLATOR
- FM TELEMETRY

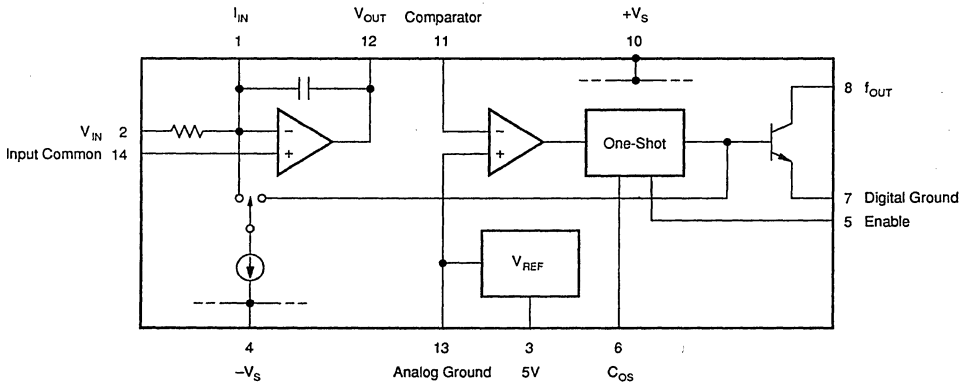
DESCRIPTION

The VFC110 voltage-to-frequency converter is a third-generation VFC offering improved features and performance. These include higher frequency operation, an on-board precision 5V reference and a Disable function.

The precision 5V reference can be used for offsetting the VFC transfer function, as well as exciting transducers or bridges. The Enable pin allows several VFCs' outputs to be paralleled, multiplexed, or simply to shut off the VFC. The open-collector frequency output is TTL/CMOS-compatible. The output may be isolated by using an opto-coupler or transformer.

Internal input resistor, one-shot and integrator capacitors simplify applications circuits. These components are trimmed for a full-scale output frequency of 4MHz at 10V input. No additional components are required for many applications.

The VFC110 is packaged in plastic and ceramic 14-pin DIPs. Industrial and military temperature range gradeouts are available.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-861A

SPECIFICATIONS

At T_A = +25°C and V_S = ±15V unless otherwise noted.

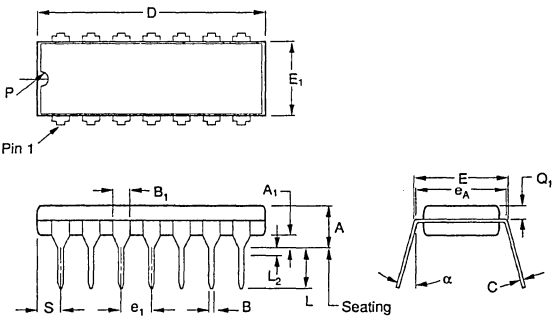
PARAMETER	CONDITIONS	VFC110BG			VFC110AG/SG/AP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
VOLTAGE-TO-FREQUENCY OPERATION								
Nonlinearity[1]: f_{FS} = 100kHz	C_{OS} = 2.2nF, R_{IN} = 44kΩ		0.005	0.01		0.01	0.05	%FS
f_{FS} = 1MHz	C_{OS} = 150pF, R_{IN} = 40kΩ		0.01	0.05			0.1	%FS
f_{FS} = 2MHz	C_{OS} = 56pF, R_{IN} = 34kΩ		0.02			*		%FS
f_{FS} = 4MHz	C_{OS} = (Int), R_{IN} = (Int)		1			*		%FS
Gain Error, f = 1MHz	C_{OS} = 150pF, R_{IN} = 40kΩ			5			*	%
Gain Drift, f = 1MHz	Specified Temp Range			50			100	ppm/°C
Relative to V_{REF}	Specified Temp Range		50			100		ppm/°C
PSRR	V_S = ±8V to ±18V			0.05			0.1	%/V
INPUT								
Full Scale Input Current			250	500		*	*	µA
I_B– (Inverting Input)			15	60		20	100	nA
I_B+ (Non-Inverting Input)			250			*		nA
V_{OS}				3			3	mV
V_{OS} Drift	Specified Temp Range		35			*		µV/°C
INTEGRATOR AMPLIFIER OUTPUT								
Output Voltage Range	R_L = 2kΩ	–0.2		$+V_S$ – 4	*		*	V
Output Current Drive		5	20		*	*		mA
Capacitive Load	No Oscillations		10			10		nF
COMPARATOR INPUT								
I_B (Input Bias Current)			–5			*		µA
Trigger Voltage			±50			*		mV
Input Voltage Range		–5		$+V_S$	*		*	V
OPEN COLLECTOR OUTPUT								
V_O Low				0.4			*	V
$I_{LEAKAGE}$			0.1	1		*	*	µA
Fall Time			25			*		ns
Delay to Rise			25			*		ns
Settling Time	To Specified Linearity for a Full-Scale Input Step		One Pulse of New Frequency Plus 1µs					
REFERENCE VOLTAGE								
Voltage		4.97	5	5.03	*	*	*	V
Voltage Drift				20			50	ppm/°C
Load Regulation	I_O = 0 to 10mA		2	10		*	*	mV
PSRR	V_S = ±8V to ±18V		5			*		mV/V
Current Limit	Short Circuit	15	20			*		mA
ENABLE INPUT								
V_{HIGH} (f_{OUT} Enabled)	Specified Temp Range	2			*			V
V_{LOW} (f_{OUT} Disabled)	Specified Temp Range			0.4			*	V
I_{HIGH}			0.1			*		µA
I_{LOW}			1			*		µA
POWER SUPPLY								
Voltage, $±V_S$		±8	±15	±18	*	*	*	V
Current			13	16		*	*	mA
TEMPERATURE RANGE								
Specified								
AG, BG, AP		–25		+85	*		*	°C
SG		–55		+125				°C
Storage								
AG, BG, SG		–65		+150	*		*	°C
AP		–40		+125	*		*	°C

* Same specifications as VFC110BG.

NOTE: (1) Nonlinearity measured from 1V to 10V input.

MECHANICAL

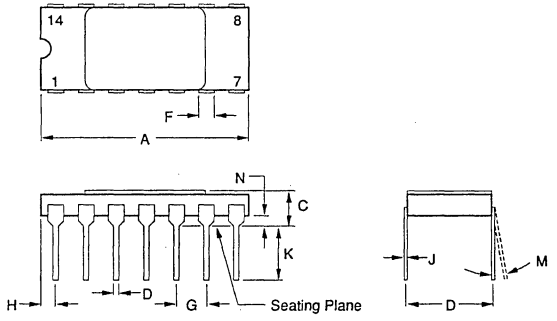
P Package — 14-Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.120	.160	3.048	4.064
A_1	.015	.065	.381	1.651
B	.014	.020	.355	.508
B_1	.050	.065	1.270	1.651
C	.008	.012	.203	.304
D	.745	.770	18.923	19.558
E	.300	.325	7.620	8.255
E_1	.240	.260	6.096	6.604
e_L	.100 BASIC		2.540 BASIC	
e_A	.300 BASIC		7.620 BASIC	
L	.125	.150	3.175	3.810
L_2[1]	0	.030	0	.762
α	0°	15°	0°	15
P	—	.050	—	1.270
Q_1	.050	.085	1.270	2.159
S[2]	.065	.090	1.651	2.286

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.
(1) e_1 and e_A apply in zone L_2 when unit is installed.
(2) Not per JEDEC.

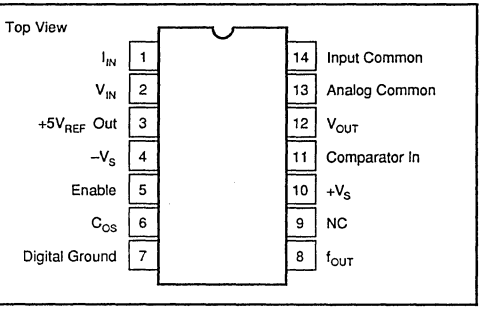
G Package — 14-Pin Hermetic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.009	.060	0.23	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages ($+V_S$ to $-V_S$) 40V
f_{OUT} Sink Current 50mA
Comparator In Voltage ..... $-5V$ to $+V_S$
Enable Input ..... $+V_S$ to $-V_S$
Integrator Common-Mode Voltage ..... −1.5V to +1.5V
Integrator Differential Input Voltage ..... +0.5V to −0.5V
Integrator Out (short-circuit) ..... Indefinite
V_{REF} Out (short-circuit) ..... Indefinite
Operating Temperature Range
G Package ..... −55°C to +125°C
P Package ..... −40°C to +85°C
Storage Temperature
G Package ..... −60°C to +150°C
P Package ..... −40°C to +125°C
Lead Temperature (soldering, 10s) ..... +300°C

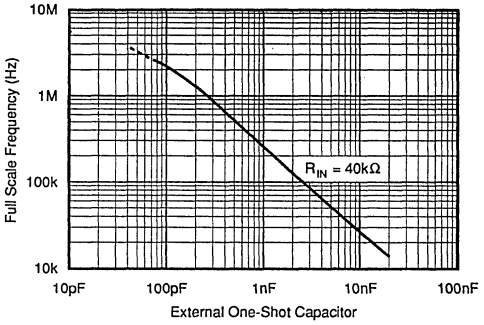
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
VFC110AG	Ceramic DIP	−25°C to +85°C
VFC110BG	Ceramic DIP	−25°C to +85°C
VFC110SG	Ceramic DIP	−55°C to +125°C
VFC110AP	Plastic DIP	−25°C to +85°C

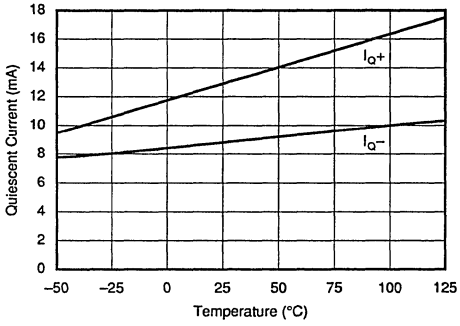
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±15V unless otherwise noted.

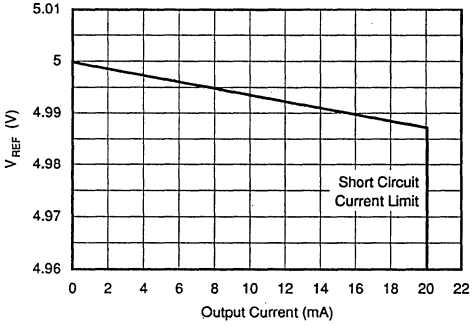
FULL-SCALE FREQUENCY vs EXTERNAL ONE-SHOT CAPACITOR



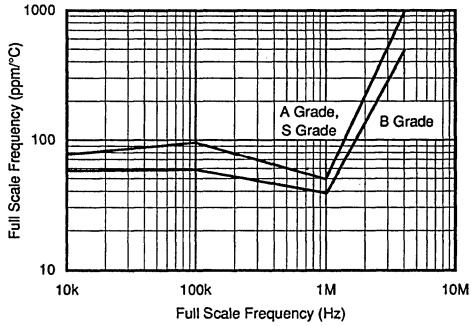
FULL-SCALE FREQUENCY vs EXTERNAL ONE-SHOT CAPACITOR



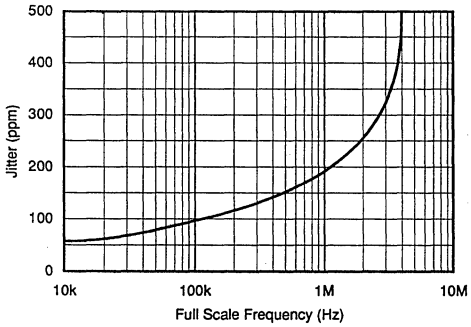
REFERENCE VOLTAGE vs REFERENCE LOAD CURRENT



TYPICAL FULL SCALE GAIN DRIFT vs FULL SCALE FREQUENCY

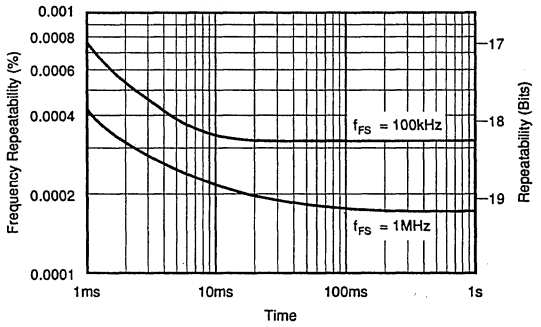


JITTER vs FULL SCALE FREQUENCY



Jitter is the ratio of the 1σ value of the distribution of the period ($1/f_{OUT}$, max) to the mean of the period.

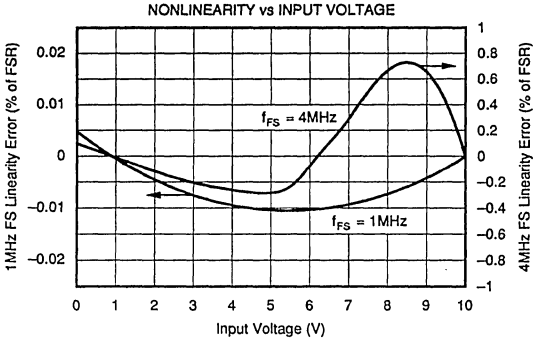
FREQUENCY COUNT REPEATABILITY vs COUNTER GATE TIME

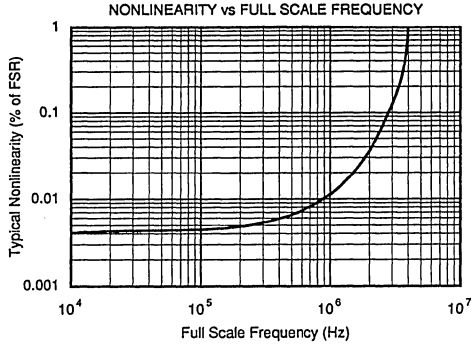


This graph describes the low frequency stability of the VFC110: the ratio of the 1σ point of the distribution of 100 runs (where each mean frequency came from 1000 readings for each gate time) to the overall mean frequency.

TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.





OPERATION

Figure 1 shows the connections required for operation at a full-scale output frequency of 4MHz. Only power supply bypass capacitors and an output pull-up resistor, R_{PU}, are required for this mode of operation. A 0V to 10V input voltage produces a 0Hz to 4MHz output frequency. The internal input resistor, one-shot and integrator capacitors set the full-scale output frequency. The input is applied to the summing junction of the integrator amplifier through the 25kΩ internal input resistor. Pin 14 (the non-inverting amplifier input) should be referred directly to the negative side of V_{IN}. The common-mode range of the integrating amplifier is limited to approximately −1V to +1V referred to analog ground. This allows the non-inverting input to Kelvin-sense the common connection of V_{IN}, easily accommodating any ground-drop errors. The input impedance loading V_{IN} is equal to the input resistor—approximately 25kΩ.

OPERATION AT LOWER FREQUENCIES

The VFC110 can be operated at lower frequencies simply by limiting the input voltage to less than the nominal 10V full-scale input. To maintain a 10V FS input and highest accuracy, however, external components are required (see Table I). Small adjustments may be required in the nominal values indicated. Integrator and one-shot capacitors are added in parallel to internal capacitors. Figure 2 shows the connections required for 100kHz full scale output. The one-shot capacitor, C_{OS}, should be connected to logic ground. The one-shot connection (pin 6) is not short-circuit protected. Short-circuits to ground may damage the device.

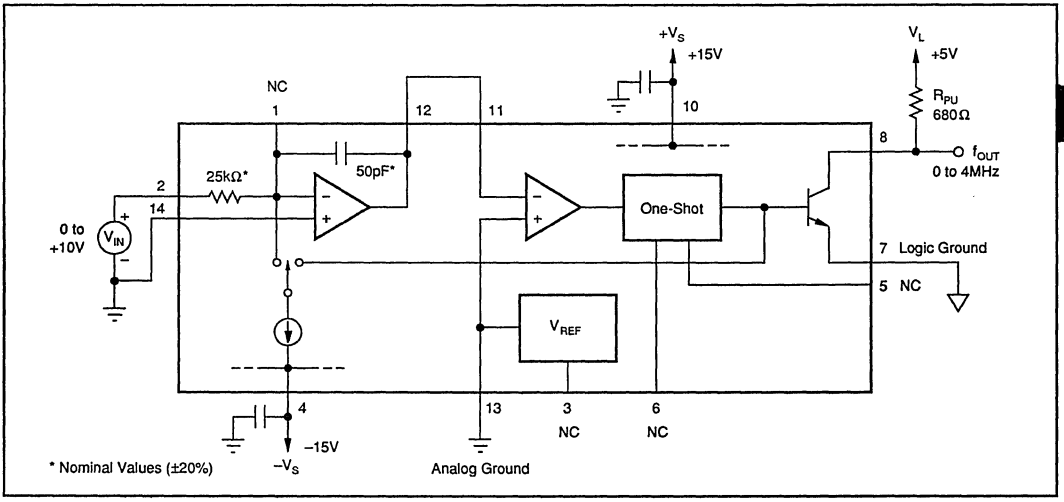


FIGURE 1. 4MHz Full-Scale Operation.

The integrator capacitor's value does not directly affect the output frequency, but determines the magnitude of the voltage swing on the integrator's output. Using a C_{INT} equal to C_{OS} provides an integrator output swing from 0V to approximately 1.5V.

COMPONENT SELECTION

Selection of the external resistor and capacitor type is important. Temperature drift of an external input resistor and one-shot capacitor will affect temperature stability of the output frequency. NPO ceramic capacitors will normally produce the best results. Silver-mica types will result in slightly higher drift, but may be adequate in many applications. A low temperature coefficient film resistor should be used for R_{IN}.

The integrator capacitor serves as a "charge bucket," where charge is accumulated from the input, V_{IN}, and that charge is drained during the one-shot period. While the size of the bucket (capacitor value) is not critical, it must not leak. Capacitor leakage or dielectric absorption can affect the linearity and offset of the transfer function. High-quality ceramic capacitors can be used for values less than 0.01µF. Use caution with higher value ceramic capacitors. High-k ceramic capacitors may have voltage nonlinearities which can degrade overall linearity. Polystyrene, polycarbonate, or mylar film capacitors are superior for high values.

FULL-SCALE FREQUENCY, f_{FS}	EXTERNAL COMPONENTS		
	R_{IN}	C_{OS}	C_{INT}
4MHz	*	*	*
2MHz	34kΩ	56pF	*
1MHz	40kΩ	150pF	*
500kHz	58kΩ	330pF	2nF
100kHz	44kΩ	2.2nF	10nF
50kHz	88kΩ	2.2nF	0.1µF
10kHz	44kΩ	22nF	0.1µF

* Use internal component only.
The values given were determined empirically to give the optimal performance, taking into consideration tradeoffs between linearity and jitter for each given full scale frequency of operation. The capacitors listed were chosen from standard values of NPO ceramic type capacitors while the resistor values were rounded off. Larger C_{INT} values may improve linearity, but may also increase frequency noise.

TABLE I. Component Selection Table.

PULL-UP RESISTOR

The VFC110's frequency output is an open-collector transistor. A pull-up resistor should be connected from f_{OUT} to the logic supply voltage, $+V_L$. The output transistor is On during the one-shot period, causing the output to be a logic Low. The current flowing in this resistor should be limited to 8mA to assure a 0.4V maximum logic Low. The value chosen for the pull-up resistor may depend on the full-scale frequency and capacitance on the output line. Excessive capacitance on f_{OUT} will cause a slow, rounded rising edge at the end of an output pulse. This effect can be minimized by using a pull-up resistor which sets the output current to its maximum of 8mA. The logic power supply can be any positive voltage up to $+V_S$.

ENABLE PIN

If left unconnected, the Enable input will assume a logic High level, enabling operation. Alternatively, the Enable input may be connected directly to $+V_S$. Since an internal pull-up current is included, the Enable input may be driven by an open-collector logic signal.

A logic Low at the Enable input causes output pulses to cease. This is accomplished by interrupting the signal path through the one-shot circuitry. While disabled, all circuitry remains active and quiescent current is unchanged. Since no reset current pulses can occur while disabled, any positive input voltage will cause the integrator op amp to ramp negatively and saturate at its most negative output swing of approximately –0.7V.

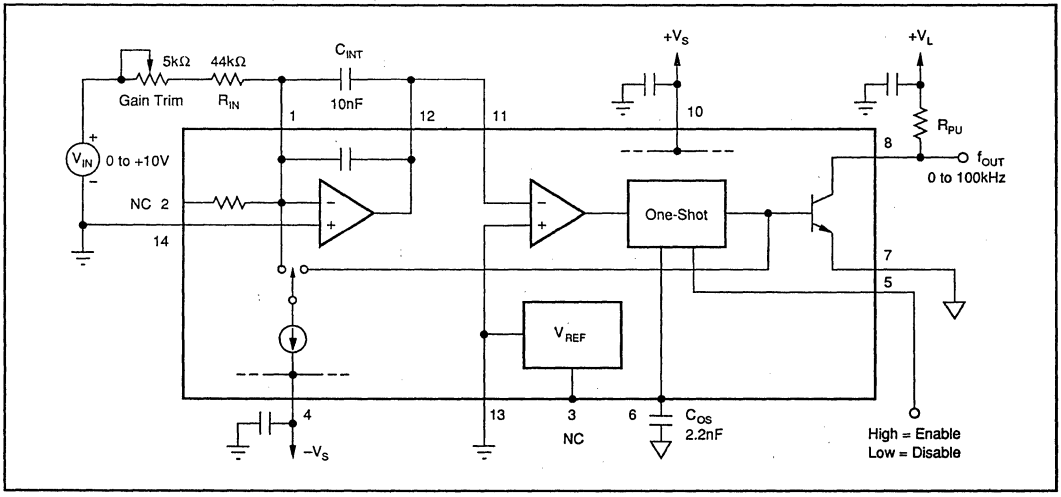


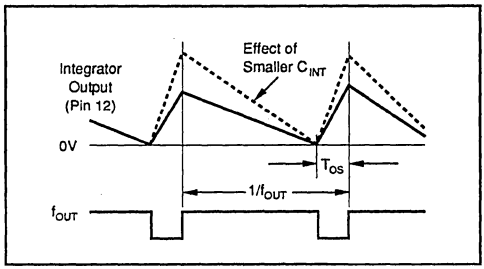
FIGURE 2. 100kHz Full-Scale Operation.

PRINCIPLE OF OPERATION

The VFC110 uses a charge-balance technique to achieve high accuracy. The heart of this technique is an analog integrator formed by the integrator op amp, feedback capacitor C_{INT}, and input resistor R_{IN}. The integrator's output voltage is proportional to the charge stored in C_{INT}. An input voltage develops an input current of V_{IN}/R_{IN}, which is forced to flow through C_{INT}. This current charges C_{INT}, causing the integrator output voltage to ramp negatively.

When the output of the integrator ramps to 0V, the comparator trips, triggering the one-shot. This connects the reference current, I_{REF}, to the integrator input during the one-shot period, T_{OS}. This switched current causes the integrator output to ramp positively until the one-shot period ends. Then the cycle starts again.

The oscillation is regulated by the balance of current (or charge) between the input current and the time-averaged



reset current. The equation of current balance is

$$I_{IN} = I_{REF} \cdot \text{Duty Cycle}$$

$$V_{IN}/R_{IN} = I_{REF} \cdot f_{OUT} \cdot T_O$$

where T_O is the one-shot period and f_{OUT} is the oscillation frequency.

When the Enable input receives a logic High (greater than +2V), a reset current cycle is initiated (causing f_{OUT} to go Low). The integrator ramps positively and normal operation is established. The time required for the output frequency to stabilize is equal to approximately one cycle of the final output frequency plus 1µs.

Using the Enable input, several VFCs' outputs can be connected to a single output line. All disabled VFCs will have a high output impedance; one active VFC can then transmit on the output line. Since the disabled VFCs are not oscillating, they cannot interfere or "lock" with the operating VFC. Locking can occur when one VFC operates at nearly the same frequency as—or a multiple of—a nearby VFC. Coupling between the two may cause them to lock to the same or exact multiple frequency. It then takes a small incremental input voltage change to unlock them. Locking cannot occur when unneeded VFCs are disabled.

REFERENCE VOLTAGE

The V_{REF} output is useful for offsetting the transfer function and exciting sensors. Figure 3 shows V_{REF} used to offset the transfer function of the VFC110 to achieve a bipolar input voltage range. Sub-surface zener reference circuitry is used for low noise and excellent temperature drift. Output current is specified to 10mA and current-limited to approximately 20mA. Excessive or variable loads on V_{REF} can decrease frequency stability due to internal heating.

MEASURING THE OUTPUT FREQUENCY

To complete an integrating A/D conversion, the output frequency of the VFC110 must be counted. Simple frequency counting is accomplished by counting output pulses for a reference time (usually derived from a crystal oscillator).

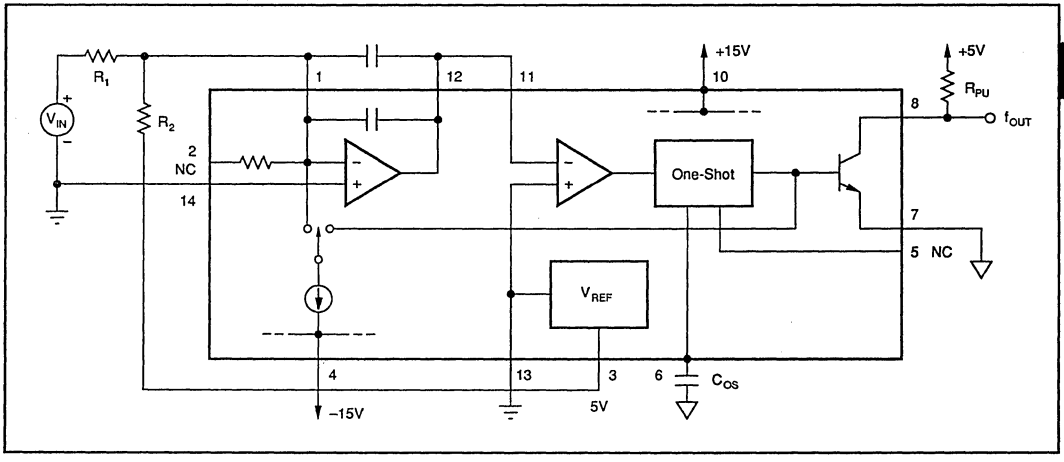


FIGURE 3. Offsetting the Frequency Output.

This can be implemented with counter/timer peripheral chips available for many popular microprocessor families. Many micro-controllers have counter inputs that can be programmed for frequency measurement.

Since f_{OUT} is an open-collector device, the negative-going edge provides the fastest logic transition. Clocking the counter on the falling edge will provide the best results in noisy environments.

Frequency can also be measured by accurately timing the period of one or more cycles of the VFC's output. Frequency must then be computed since it is inversely proportional to the measured period. This measurement technique can provide higher measurement resolution in short conversion times. It is the method used in most high-performance laboratory frequency counters. It is usually necessary to offset the transfer function so 0V input causes a finite frequency out. Otherwise the output period (and therefore the conversion time) approaches infinity.

FREQUENCY NOISE

Frequency noise (small random variation in the output frequency) limits the useful resolution of fast frequency measurement techniques. Long measurement time averages the affect of frequency noise and achieves the maximum useful resolution. The VFC110 is designed to minimize frequency noise and allows improved useful resolution with short measurement times. The typical curve "Frequency Count Repeatability vs Counter Gate Time" shows the effect of noise as the counter gate time is varied. It shows the one standard deviation (1σ) count variation (as a percentage of FS counts) versus counter gate time.

FREQUENCY-TO-VOLTAGE CONVERSION

The VFC110 can also be connected as a frequency-to-voltage converter (Figure 4). Input frequency pulses are applied to the comparator input. A negative-going pulse crossing 0V initiates a reference current pulse which is averaged by the integrator op amp. The values of the one-shot capacitor and feedback resistor (same as R_{IN}) are determined with Table I. The input frequency pulse must not remain negative for longer than the duration of the one-shot period. Figure 4 shows the required timing to assure this. If the negative-going input frequency pulses are longer in duration, the capacitive coupling circuit shown can be used. Level shift or capacitive coupling circuitry should not provide pulses which go lower than –5V or damage to the comparator input may occur.

This frequency-to-voltage converter operates by averaging (filtering) the reference current pulses triggered on every falling edge at the frequency input. Voltage ripple with a frequency equal to the input will be present in the output voltage. The magnitude of this ripple voltage is inversely proportional to the integrator capacitor. The ripple can be made arbitrarily small with a large capacitor, but at the sacrifice of settling time. The R-C time constant of C_{INT} and R_{IN} determine the settling behavior. A better compromise between output ripple and settling time can be achieved by adding a low-pass filter following the voltage output.

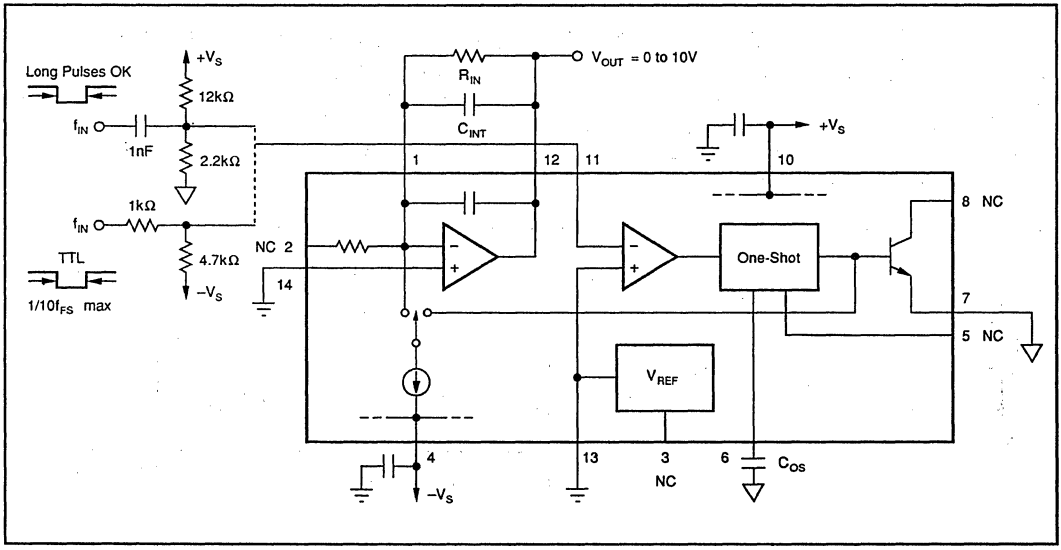
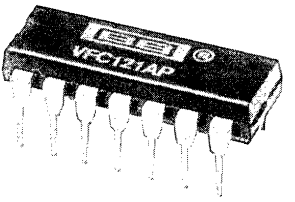


FIGURE 4. Frequency-to-Voltage Conversion.

BURR-BROWN®



VFC121

Precision Single Power Supply VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

- SINGLE SUPPLY OPERATION: +4.5V to +36V
- f_o = 1.5MHz max
- LOW NONLINEARITY: 0.03% max at 100kHz, 0.1% max at 1MHz
- HIGH INPUT IMPEDANCE
- VOLTAGE REFERENCE OUTPUT
- THERMOMETER OUTPUT: 1mV/°K

APPLICATIONS

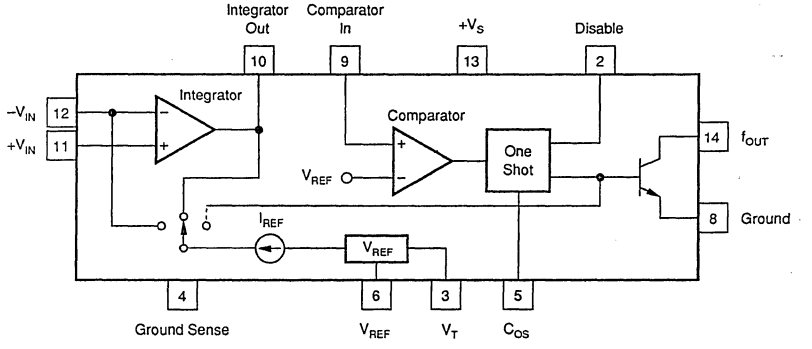
- INTEGRATING A/D CONVERSION
- ANALOG SIGNAL TRANSMISSION
- PHASE-LOCKED LOOP VCO
- GALVANICALLY ISOLATED SYSTEMS

DESCRIPTION

The VFC121 is a monolithic voltage-to-frequency converter consisting of an integrating amplifier, voltage reference, and one-shot charge pump circuitry. High-frequency complementary NPN/PNP circuitry is used to implement the charge-balance technique, achieving speed and accuracy far superior to previous single power supply VFCs.

The high-impedance input accepts signals from ground potential to V_S – 2.5V. Power supplies from 4.5V to 36V may be used. A 2.6V reference voltage output may be used to excite sensors or bias external circuitry. A thermometer output voltage proportional to absolute temperature (°K) may be used as a temperature sensor or for temperature compensation of applications circuits.

Frequency output is an open-collector transistor. A disable pin forces the output to the high impedance state, allowing multiple VFCs to share a common transmission path.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-971A

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_S = +5V, and R_{IN} = 8kΩ unless otherwise noted.

PARAMETER	CONDITIONS	VFC121AP MIN	VFC121AP TYP	VFC121AP MAX	VFC121BP MIN	VFC121BP TYP	VFC121BP MAX	UNITS
ACCURACY								
Nonlinearity: f_{FS} = 100kHz	C_{OS} 1200pF, C_{INT} = 2700pF			0.05			0.03	%FS
f_{FS} = 1MHz	C_{OS} 68pF, C_{INT} = 270pF		0.1				0.1	%FS
Gain Error: f_{FS} = 100kHz	C_{OS} 1200pF, C_{INT} = 2700pF			10			*	%FS
Gain Drift: f_{FS} = 100kHz	T_{MIN} to T_{MAX}			80			40	ppm/°C
Relative to V_{REF}	+V_S = +5V to +36V			100			40	ppm/°C
PSRR				0.025			*	%/V
INPUT								
Minimum Input Voltage				0			*	V
Maximum Input Voltage		V_S – 2.5	V_S – 2		*	*		V
Impedance		10	100		*	*		MΩ
I_{BIAS}			150	300		*	*	nA
V_{OS}			300	800		100	400	µV
V_{OS} Drift	T_{MIN} to T_{MAX}		10			*		µV/°C
OPEN COLLECTOR OUTPUT								
V_{SAT}	$I_{PULL\ UP}$ = 10mA			0.4			*	V
$I_{LEAKAGE}$	$V_{PULL\ UP}$ = 5V, $R_{PULL\ UP}$ = 470Ω			1			*	µA
Fall Time				100			*	ns
Delay to Rise				100			*	ns
Settling Time	To specified linearity for full scale input step	(1)						
REFERENCE VOLTAGE								
Voltage		2.59	2.6	2.61	*	*	*	V
Voltage Drift				100			50	ppm/°C
Load Regulation	I_O = 0 to 10mA			10			*	mV
PSRR	V_S = +5V to +36V			10			*	mV
Current Limit				Short Circuit Protected				
INTEGRATOR AMPLIFIER OUTPUT								
Output Voltage Range	R_L = 100kΩ	0.8		2.9	*		*	V
COMPARATOR INPUT								
I_{BIAS}			+1			*		µA
Trigger Voltage			2.6			*		V
Input Voltage Range		0		2.9	*		*	V
THERMOMETER								
V_T	T_A = +25°C		298			*		mV
V_T Slope	T_{MIN} to T_{MAX}		1			*		mV/°K
DISABLE INPUT								
V_{HIGH} (Disabled)		2			*			V
V_{LOW}				0.8			*	V
I_{HIGH} (Disabled)	V_{HIGH} = 2V		10			*		µA
I_{LOW}	V_{LOW} = 0.8V		10			*		µA
POWER SUPPLY								
Voltage		4.5	5	36	*	*	*	V
Current			7.5	10		*	*	mA
TEMPERATURE RANGE								
Specified		–25		+85	*		*	°C
Storage		–40		+125	*		*	°C

* Same specification as VFC121AP.

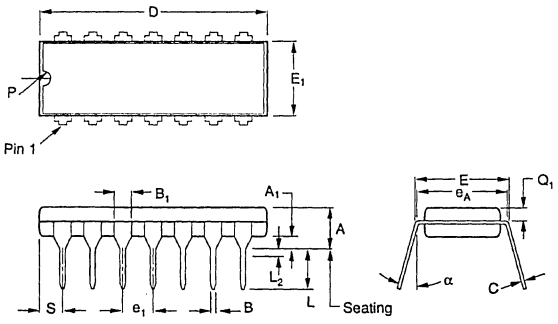
NOTE: (1) One pulse of new frequency plus 1µs.

ORDERING INFORMATION

MODEL	PACKAGE	LINEARITY ERROR, MAX (f_S = 100kHz)	TEMPERATURE RANGE
VFC121AP	Plastic DIP	0.05%	–25°C to +85°C
VFC121BP	Plastic DIP	0.03%	–25°C to +85°C

MECHANICAL

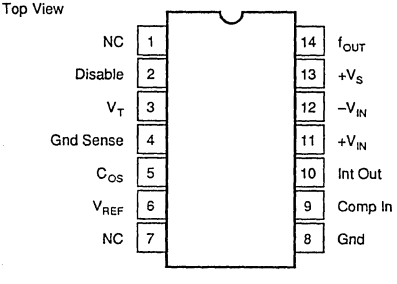
P Package — 14-Pin Plastic DIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.120	.160	3.048	4.064
A1	.015	.065	.381	1.651
B	.014	.020	.355	.508
B1	.050	.065	1.270	1.651
C	.008	.012	.203	.304
D	.745	.770	18.923	19.558
E	.300	.325	7.620	8.255
E1	.240	.260	6.096	6.604
e1	.100 BASIC		2.540 BASIC	
eA	.300 BASIC		7.620 BASIC	
L	.125	.150	3.175	3.810
L2(1)	0	.030	0	.762
α	0°	15°	0°	15
P	—	.050	—	1.270
Q1	.050	.085	1.270	2.159
S(2)	.065	.090	1.651	2.286

NOTES: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.
(1) e_1 and e_A apply in zone L_2 when unit is installed.
(2) Not per JEDEC.

PIN CONFIGURATION



PIN CONFIGURATION

PIN #	NAME	DESCRIPTION
1	NC	Not Connected
2	Disable	Input logic Low for normal operation. Input logic High to disable the VFC121. Has internal pull-down, for normal operation if not connected.
3	V_T	Temperature compensation voltage proportional to absolute temperature. Typically 298mV at room temperature (298°K), with a change of 1mV per °C (°K).
4	Gnd Sense	Defines ground for the internal voltage reference.
5	C_{OS}	One-shot capacitor is connected between here and ground to set full scale output frequency.
6	V_{REF}	Output from the internal band-gap voltage reference, typically 2.6V. Can be used externally to set levels or excite sensors.
7	NC	Not Connected
8	Gnd	Ground
9	Comp In	Comparator In
10	Int Out	Integrator Out
11	$+V_{IN}$	Non-inverting input of the integrating op amp. The input signal is applied here.
12	$-V_{IN}$	Inverting input of the integrating op amp. C_{INT} is connected between here and the integrator output (pin 10), and R_{IN} is connected between here and ground.
13	$+V_S$	Supply voltage connected here. Range is +4.5V to +36V.
14	f_{OUT}	Frequency output pin. This is the output of an open-collector transistor, and an external pull-up circuit should be used to generate the appropriate logic levels.

ABSOLUTE MAXIMUM RATINGS

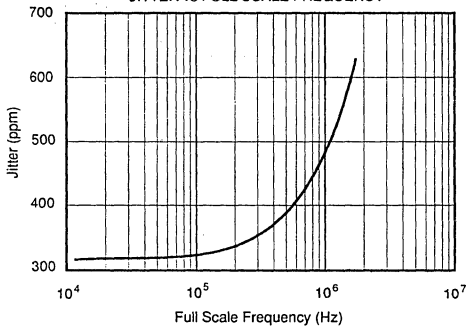
Power Supply Voltage ($+V_S$) 40V
f_{OUT} Sink Current 20mA
Comparator In Voltage ..... –0.5V to +3V
Enable Input ..... –0.3V to $+V_S$
Integrator Common-Mode Voltage ..... 0V to $+V_S$ – 2V
Integrator Differential Input Voltage ..... –0.3V to +0.3V
V_{REF} Out (short-circuit) ..... Indefinite
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature ..... –40°C to +125°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses above these ratings may permanently damage the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

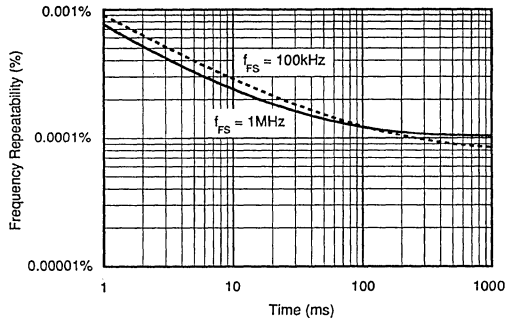
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = +5V, and R_{IN} = 8kΩ unless otherwise noted.

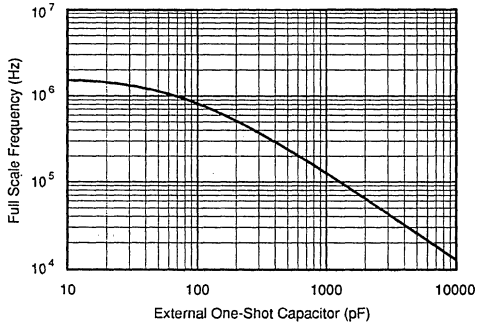
JITTER vs FULL SCALE FREQUENCY



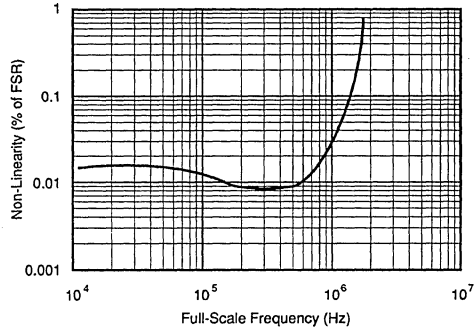
FREQUENCY COUNT REPEATABILITY vs COUNTER GATE TIME



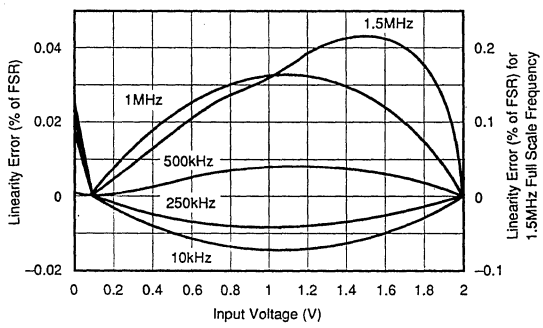
FULL SCALE FREQUENCY vs EXTERNAL ONE-SHOT CAPACITOR



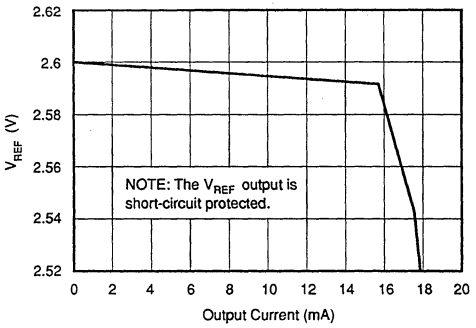
NON-LINEARITY vs FULL-SCALE FREQUENCY



NON-LINEARITY vs INPUT VOLTAGE

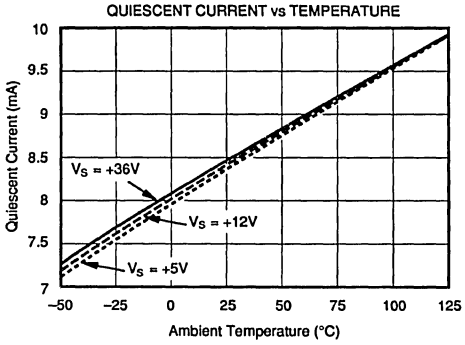


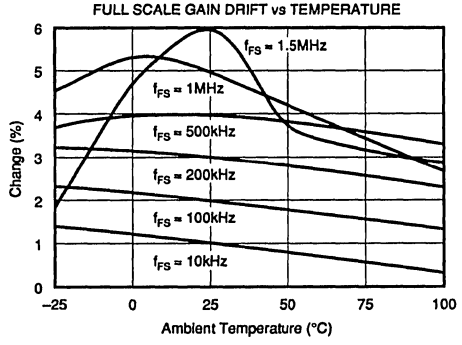
REFERENCE VOLTAGE vs REFERENCE LOAD CURRENT



TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = +5V, and R_{IN} = 8kΩ unless otherwise noted.





THEORY OF OPERATION

The VFC121 uses a charge-balance technique to achieve high accuracy. The basic architecture is shown in Figure 1. An analog integrator at the front end, consisting of a precision op amp and a feedback capacitor, C_{INT}, provides a true integrating approach for improved noise immunity. Use of the non-inverting input of the op amp for the analog input provides a high input impedance to the user.

The integrator's output is proportional to the charge stored on C_{INT} plus the analog input voltage. An input voltage, V_{IN}, forces a current through R_{IN} of V_{IN}/R_{IN}, which also flows through C_{INT}. This current through C_{INT} causes the integrator output to ramp positive. (Refer to the timing diagram in Figure 2.)

When the output of the integrator ramps to V_{REF}, the comparator trips, driving the output of the VFC121 Low, and triggering the one-shot. The tripping of the comparator also connects the reference current, I_{REF}, to the integrator input for the duration of the one-shot period, T_{OS}. This switched current causes the output of the integrator to ramp negative.

When the one-shot times out, the output of the VFC121 is reset High, the one-shot is reset, and I_{REF} is switched to the output of the integrating op amp. (This causes the output of

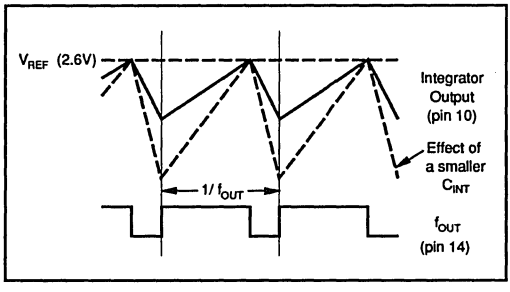


FIGURE 2. Timing Diagram.

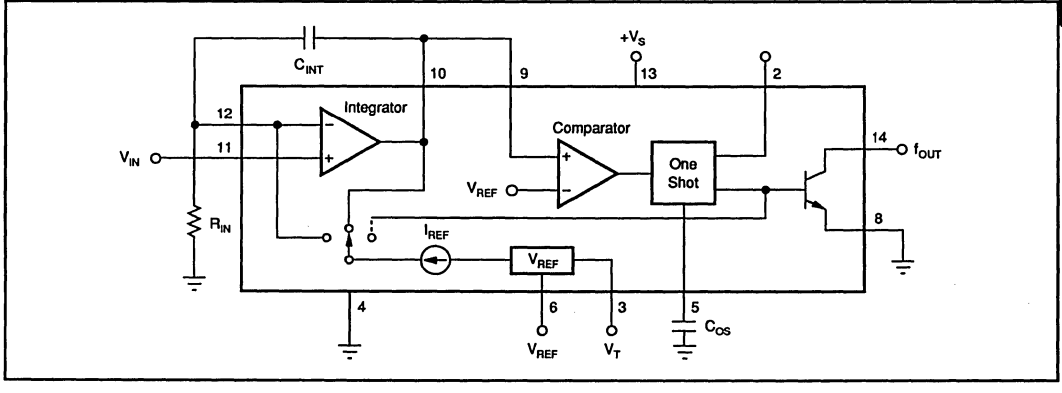


FIGURE 1. VFC121 Architecture.

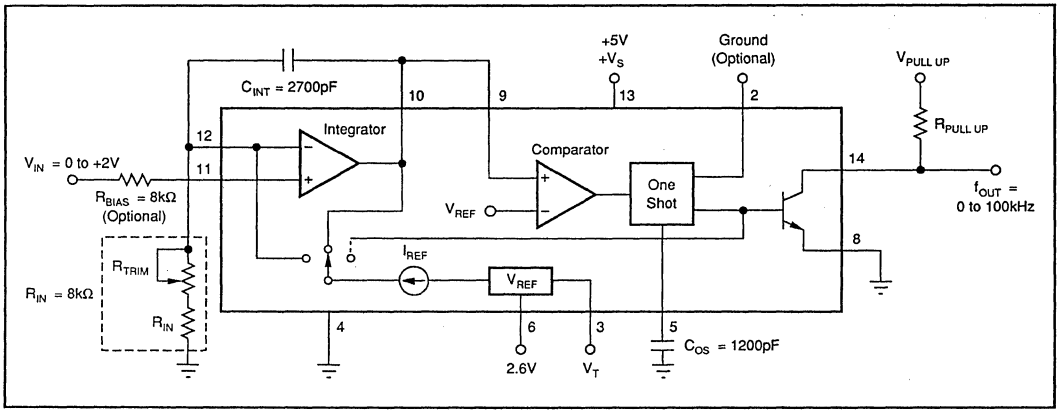


FIGURE 3. 2V Full Scale Input, 100kHz Full Scale Output.

the integrating op amp to see a constant current, reducing errors that might occur if the load were unbalanced.) In this state, the output of the integrator resumes a positive ramp, restarting the cycle.

The output frequency is regulated by the balance of current (or charge) between the current V_{IN}/R_{IN} and the time-averaged reset current. The size of the integrating capacitor, C_{INT}, determines the slew rate of the integrator, and thus how far down the integrator ramps during the one-shot period, but has no effect on the output frequency of the VFC121.

The reference voltage used internally is generated from a bandgap reference, which is actively trimmed to achieve the low drift characteristics of the VFC121. To maximize flexibility of designs using the VFC121, both the bandgap reference voltage and a thermometer voltage are available externally.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC OPERATION

The VFC121 allows users a wide range of input voltages and supply voltages, and easy control of the full scale output frequency. The basic connections are shown in Figure 3, with components that generate a 100kHz output with a 2V full scale input.

For other input and output ranges, the full scale input voltages and full scale output frequencies can be calculated as follows:

$$f_{FS} = \frac{V_{FS}}{2(R_{IN})(C_{OS} + 60)}$$

The full scale input current of 250µA was chosen to provide a 25% duty cycle in the output frequency. The VFC121 is designed to give optimum linearity under these conditions, but other current levels can be used without significantly degrading linearity. By reducing R_{IN}, the integrating current is increased, increasing the positive ramp rate of the integrator output. Since the one-shot period is unchanged, the duty cycle of the output increases.

Stray capacitance at the C_{OS} pin typically adds about 60pF to the capacitance of the external C_{OS}, which accounts for the adjustment in the above equation. This usually becomes negligible as the required output frequency is reduced, and C_{OS} is increased.

R_{BIAS} is included in the circuit in Figure 3 to compensate for the effects of bias currents at the input of the integrating op amp. It is optional in most applications, but when needed, R_{BIAS} should equal R_{IN}.

Table 1 indicates standard external component values for common input voltage ranges and output frequency ranges.

COMPONENT SELECTION

Selection of the external resistor and capacitor type is important. Temperature drift of the external input resistor and one-shot capacitor will affect temperature stability of the output frequency. NPO ceramic capacitors will normally produce the best results. Silver-mica types will result in slightly higher drift, but may be adequate in many applications. A low temperature coefficient film resistor should be used for R_{IN}.

The integrator capacitor, C_{INT}, serves as a "charge bucket," where charge accumulation is induced by the input, V_{IN}, and repeatedly reduced during the one-shot period. The size of

FULL SCALE INPUT RANGE (V)	$R_{IN} + R_{TRIM}$ (kΩ)	
2	8	
5	20	
10	40	
FULL SCALE OUTPUT FREQUENCY (kHz)	**C_{OS} (pF)**	**C_{INT} (pF)**
1500	22	150
1000	68	270
500	180	470
250	470	1000
125	1000	2200
25	4700	10,000
NOTE: Higher output frequencies can be achieved by reducing R_{IN}.		

TABLE 1. Standard External Component Values

the bucket (the capacitor value) is not critical, since it primarily determines how far below V_{REF} the output of the integrator ramps during the one-shot period. At the same time, the capacitor used must not leak since capacitor leakage or dielectric absorption can affect the linearity and offset of the transfer function. High-quality ceramic capacitors can be used for values less than 0.01µF, but caution should be used with higher value ceramic capacitors. High-k ceramic capacitors may have voltage non-linearities which can degrade overall linearity. Polystyrene, polycarbonate, or mylar film capacitors are superior for higher capacitance values.

During the one-shot period, the output of the integrator is ramping down. To prevent the integrating op amp from being saturated at its minimum output of 0.8V, C_{INT} should be kept at least 1.7 x C_{OS}.

OUTPUT FREQUENCY ADJUSTMENT

The full scale output frequency of the VFC121 can be adjusted using a trim-pot, R_{TRIM} in Figure 3, in series with R_{IN}. For optimum drift vs temperature, a low temperature coefficient fixed resistor of approximately 90% of the calculated R_{IN} requirement should be used in series with a trim-pot approximately 20% of the size of the calculated R_{IN}. The low-drift fixed resistor contributes most of the final R_{IN} resistance, so that the effect of higher drift from the trim-pot is attenuated in the total R_{IN}.

PULL-UP RESISTOR

The VFC121's frequency output is an open-collector transistor. A pull-up resistor should be connected from f_{OUT} to the logic supply, $+V_L$. The output transistor is On during the one-shot period, causing the output to be logic Low. The current flowing in this resistor should be limited to 10mA to assure a 0.4V maximum logic Low. The value chosen for the pull-up resistor may depend on the full-scale frequency and capacitance on the output line. Excessive capacitance on f_{OUT} will cause a slow, rounded rising edge at the end of an output pulse. This effect can be minimized by using a pull-up resistor which sets the output current to its maximum of 10mA. The logic power supply can be any positive voltage up to +36V.

ENABLE PIN

If left unconnected, the Enable input will assume a logic Low level, enabling the output stage, Alternatively, the Enable input may be connected directly to ground. This pin can also be driven by standard TTL or CMOS logic.

A logic High at the Enable input causes output pulses to cease. This is accomplished by interrupting the signal path through the one-shot circuitry. While disabled, all circuitry remains active and quiescent current is unchanged. Since no reset current pulses can occur while disabled, any positive input voltage will cause the integrator op amp to ramp positive and saturate at its most positive output swing of approximately V_{REF} + 0.7V.

When the Enable input receives a logic Low (less than 0.8V), a reset current cycle is initiated, (causing f_{OUT} to go Low). The integrator ramps negatively and normal operation is established. The time required for the output frequency to stabilize is equal to approximately one cycle of the final output frequency plus 1µs.

Using the Enable input, the outputs from several VFCs can be connected to a single line. All disabled VFCs will have a high output impedance; one active VFC can then transmit on the line. Since disabled VFCs are not oscillating, they cannot interfere or "lock" with the operating VFC. Locking can occur when one VFC operates at nearly the same frequency, or a multiple, as a nearby VFC. Coupling between the two may cause them to lock to the same frequency or an exact multiple. It then takes a small incremental input voltage change on one of the VFCs to unlock them. Locking cannot occur when unneeded VFCs are disabled.

APPLICATION INFORMATION

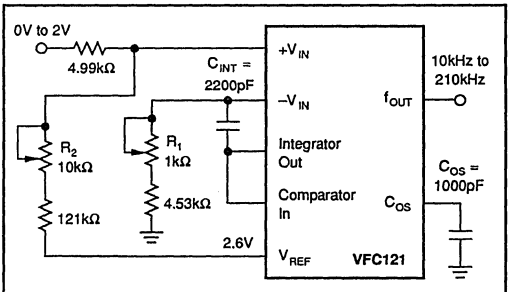
OPERATION FROM 10kHz TO 210kHz

The VFC121 is designed to provide an output frequency starting at 0Hz for a 0V input and increasing linearly to the full scale output frequency, f_{FS}, at the full scale input voltage, V_{FS}. For applications where low level inputs, near 0V, are critical, it may be inconvenient to have an output frequency approaching 0Hz. Figure 4 shows a circuit which transforms a 0V to 2V input level into output frequencies from 10kHz to 210kHz, by placing a resistor divider network between the input source and the V_{REF} output of the VFC121. This produces a positive voltage at $+V_{IN}$ when the input to the circuit is grounded. This circuit makes use of the high input impedance at $+V_{IN}$.

The transfer function of this circuit is:

$$V_{IN} = \frac{f_{OUT} - 10kHz}{100kHz} \text{ V}$$

To trim the circuit, first apply 2V to the analog input, and adjust R_1 to give a full scale output frequency of 210kHz. Then apply 0V to the analog input, and adjust R_2 until the output frequency is 10kHz. For absolute precision, it may be necessary to make several iterations trimming R_1 and R_2. In most cases, one iteration will be enough, since the effect of R_2 on full scale output frequency is attenuated by the divider net-



NOTE: Use 1% metal film fixed resistors, Cermet® trim pots, and NPO ceramic capacitors.

FIGURE 4. Offsetting the Output Frequency.

work, which sees only a 0.6V total delta at full scale (2.6V at V_{REF} minus 2V full scale input) as compared with a 2.6V delta at a 0V input level.

USING THE VFC121 THERMOMETER VOLTAGE

Because of the high input impedance of the VFC121 (which results from using the non-inverting input to the integrating op amp), it is relatively simple to use a standard multiplexer in front of the VFC121. One of the possible reason to multiplex the input to the VFC121 is to use it to track temperature changes in the operating environment of the electronics in a system, in addition to using the VFC121 in its normal mode to measure an analog signal.

Figure 5 shows a way to do this. In this circuit, the normal analog input signals to be multiplexed through the VFC121 have a full scale voltage of 2V, and generate a full scale output frequency of 100kHz. To measure the electronics system temperature, the user selects the multiplexer channel connected to the thermometer voltage on pin 3. A measured output frequency from the VFC121, with the multiplexer on channel 8, now corresponds to the temperature of the electronics as follows:

$$\text{Temp (°C)} = \frac{\text{Output Frequency} - 13{,}650}{50}$$

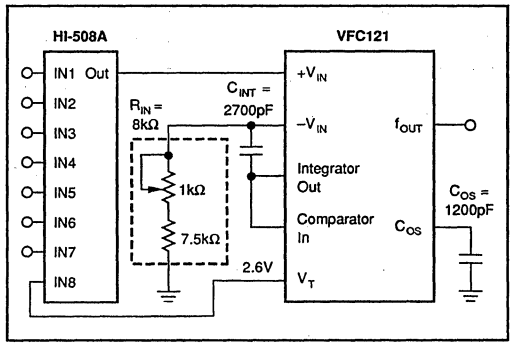
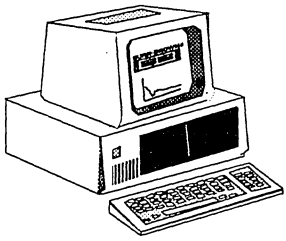


FIGURE 5. Measuring System Temperature.



DSP-RELATED AND OTHER BURR-BROWN PRODUCTS

Burr-Brown's world of digital signal processing solutions emphasizes ease of use and ranges from DIP-packaged analog input and analog output components all the way to complete DSP-based systems. The product line includes development and code generation software, dedicated processors, and analog I/O products. Easy-to-use and cost efficient, these products carry the user all the way from simulation to integration.

Other DSP design and integration tools are currently in development. If you need to find the shortest route from DSP development to integration, call a Burr-Brown applications engineer at 1-800-548-6132.

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ANALOG DSP COMPONENTS AND TEST SYSTEMS

Function	Model	Description	Sample Rate	Resolution	Package	Page
Analog-to-Digital Converters	DSP101	Low-cost, high resolution A-to-D with zero-chip interface to DSP IC's from ADI, AT&T, Motorola and TI	200kHz	16/18 bits	28-pin DIP	S14-4
	DSP102	Two channel, low-cost, high resolution A-to-D with zero-chip interface to DSP IC's from ADI, AT&T, Motorola and TI	200kHz	16/18 bits	28-pin DIP	S14-4
Digital-to-Analog Converters	DSP201	Low-cost, high resolution D-to-A with zero-chip interface to DSP IC's from ADI, AT&T, Motorola and TI	500kHz	16/18 bits	28-pin DIP	S14-15
	DSP202	Two channel, low-cost, high resolution D-to-A with zero-chip interface to DSP IC's from ADI, AT&T, Motorola and TI	200kHz	16/18 bits	28-pin DIP	S14-15
Analog Input DSP Test Systems	DSP-SYS603	Complete test system including A-to-D box, digital buffer, DSP processor, and software, designed to run on a PC	10MHz	12-bits	Hardware and Software	S14-27
	DSP-SYS701	Complete test system including A-to-D box, digital buffer, DSP processor, and software, designed to run on a PC	500kHz	16-bits	Hardware and Software	S14-31

DSP PROCESSOR BOARDS

Model	Processor	Quantity	Speed (ns)	SRAM (KB)	Board Form	1024 FFT Execution Time (ms)	FIR Filter Tap Execution Time (ns)	IIR Bi-Quad Filter Execution Time (µs)	Page
ZPB32	AT&T DSP32	1	250	64	PC	8.9	250	1.25	CALL
ZPB32-HS	AT&T DSP32	1	160	64	PC	5.7	160	0.8	1-800-
ZPB34-001	AT&T DSP32C	1	80	64	PC/AT	3.2	80	0.4	548-
ZPB34-002	AT&T DSP32C	1	80	192	PC/AT	3.2	80	0.4	6132
ZPB34-003	AT&T DSP32C	1	80	320	PC/AT	3.2	80	0.4	for
ZPB34-004	AT&T DSP32C	1	80	576	PC/AT	3.2	80	0.4	more
ZPB3201	AT&T DSP32	1	160	64	VME 6U	5.7	160	0.8	information
ZPB3202	AT&T DSP32	2	160	128	VME 6U	5.7	160	0.8	
ZPB3211	AT&T DSP32C	1	80	64	VME 6U	3.2	80	0.4	
ZPB3212	AT&T DSP32C	2	80	128	VME 6U	3.2	80	0.4	

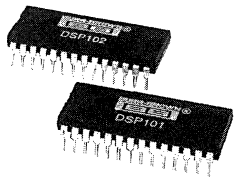
DSP ANALOG I/O SYSTEMS

Model	Form	Analog Input Channels	Analog Output Channels	Number of Bits	Max Conversion Rate (kHz)	Anti-Aliasing Filter	Smoothing Filter	On-Board Sample Rate Generator	Page
ZPB100	PC Board	1	1	16	8	300Hz-3kHz	0Hz-3kHz	8kHz	CALL
ZPB1100	PC Board	1		16	150	User Specified	—	75Hz-150kHz	1-800-
ZPB2100	PC Board		1	16	150	—	User Specified	—	548-
ZPD1001	External Box	1 or 2	1 or 2	16	150	—	—	4.8kHz-150kHz	6132
ZPD1002	External Box	1 or 2		12	10MHz	—	—	—	for more
ZPB1003	External Box	1		16	500kHz	—	—	—	information.

DOS-BASED DSP SOFTWARE

Model	Function	Page
ZPA1000	Emulates (3) test instruments for signal analysis: oscilloscope, spectrum and histogram analyzers	**CALL 1-800-548-6132 for more information**
ZPM50-001 (DSPlay)	DSP Algorithm development/simulation	
ZPM32 (DSPlay XL)	DSP Algorithm development/code generation for DSP32/DP32C	
ZPO32	AT&T DSP32/32C Assembler	
ZPO33	AT&T DSP32-CC "C"Compiler	
ZPOFDAS1/DAS2	Momentum Data's Filter Design	

BURR-BROWN®



DSP101
DSP102

ADVANCE INFORMATION
SUBJECT TO CHANGE

DSP-Compatible Sampling Single/Dual ANALOG-TO-DIGITAL CONVERTERS

FEATURES

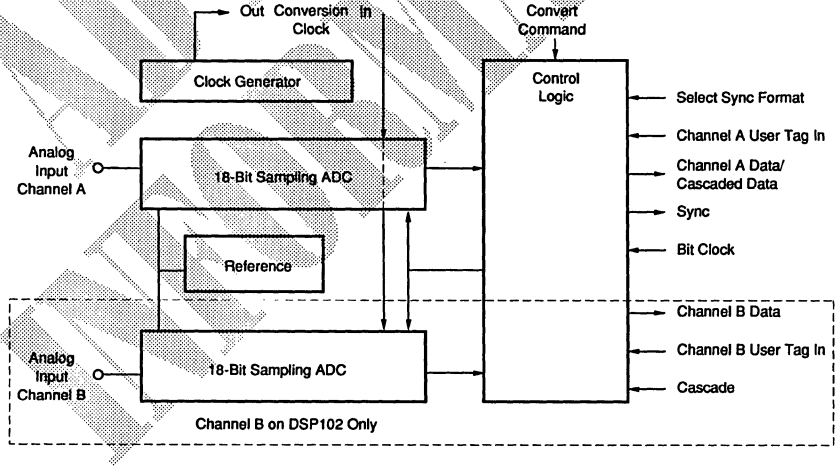
- **ZERO-CHIP INTERFACE TO STANDARD DSP ICs: AD, AT&T, MOTOROLA, TI**
- **SINGLE CHANNEL: DSP101**
- **DUAL CHANNEL: DSP102**
  Two Serial Outputs or Cascade to Single 32-Bit Word
- **SAMPLING RATE TO 200kHz**
- **DYNAMIC SPECIFICATIONS:**
  Signal/(Noise + Distortion) = 90dB;
  Spurious-Free Dynamic Range = 94dB;
  THD = –92dB
- **SERIAL OUTPUT DATA COMPATIBLE WITH 16-, 24-, AND 32-BIT DSP IC FORMATS**

DESCRIPTION

The DSP101 and DSP102 are high performance sampling analog-to-digital converters designed for simplicity of use with modern digital signal processing ICs. Both are complete with all interface logic for use directly with DSP ICs, and provide full sampling and conversion at rates up to 200kHz.

The DSP101 offers a single conversion channel, with 18 bits of serial data output, allowing the user to drive 16-bit, 24-bit, or 32-bit DSP ports. The DSP102 offers two complete conversion channels, with either two full 18-bit output ports, or a mode to cascade two 16-bit conversions into a 32-bit port as one word.

Both the DSP101 and DSP102 are packaged in standard, low-cost 28-pin plastic DIP packages. Each is offered in two performance grades to match application requirements.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1068

SPECIFICATIONS

ELECTRICAL

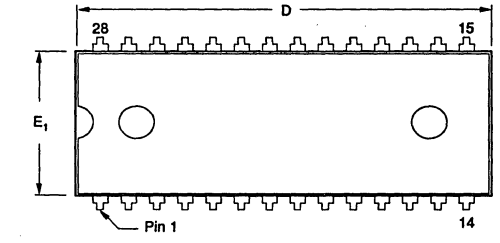
T_A = 0°C to 70°C, sampling frequency, f_S = 160kHz, $V_A+ = V_D$ = +5V, V_A- = –5V, 12.288MHz crystal oscillator, unless otherwise specified.

PARAMETER	CONDITIONS	DSP101JP DSP102JP MIN	DSP101JP DSP102JP TYP	DSP101JP DSP102JP MAX	DSP101KP DSP102KP MIN	DSP101KP DSP102KP TYP	DSP101KP DSP102KP MAX	UNITS
RESOLUTION				18			•	Bits
ANALOG INPUT								
Voltage Range			±2.75V			•		V
Impedance			1			•		kΩ
Capacitance			20			•		pF
THROUGHPUT SPEED								
Complete Cycle	Acquisition + Conversion			5			•	µs
Throughput Rate		200			•			kHz
AC ACCURACY [1]								
Signal to (Noise + Distortion) Ratio	f_{IN} = 1kHz		86			90		dB[2]
	f_{IN} = 1kHz (–60dB)		32			•		dB
	f_{IN} = 25kHz		82			•		dB
Total Harmonic Distortion	f_{IN} = 1kHz		–92			•		dB
Spurious-Free Dynamic Range	f_{IN} = 1kHz		94			•		dB
Signal to Noise Ratio (SNR)	f_{IN} = 1kHz		88			•		dB
DC ACCURACY								
Gain Error [3]				5			•	%
Gain Error Mismatch [3]	DSP102 Channels			1			•	%
Integral Linearity Error			±0.003			•		%
Differential Linearity Error			±0.002			•		%
No Missing Codes			14			•		Bits
Bipolar Zero Error [3]			±2					mV
Bipolar Zero Mismatch [3]	DSP102 Channels		±2			•		mV
Power Supply Sensitivity	–5.1 < V_A- < –4.9		–60			•		dB
	+4.9 < V_A+, V_D+ < +5.1		–60			•		dB
SAMPLING DYNAMICS								
Aperture Delay			30			•		ns
Aperture Jitter			300			•		ps,rms
Transient Response			1			•		µs
Overvoltage Recovery			5			•		µs
DIGITAL INPUTS								
Logic Levels (Except OSC1)								
V_{IL}	I_L = ±10µA	0		+0.8	•		•	V
V_{IH}	I_H = ±10µA	+2.4		+5	•		•	V
OSC1 Clock				74HC Compatible				
Data Transfer Clock								
Frequency		0.1		12	•		•	MHz
Duty Cycle		40	50	60	•		•	%
Conversion Clock (CLKIN)								
Frequency		0.5		5	•		•	MHz
Duty Cycle		25	33	40	•	•	•	%
DIGITAL OUTPUTS								
Format			Serial; MSB first; 16/18-bit and Cascaded 32-bit Mode					
Coding			Binary Two's Complement					
Logic Levels (Except OSC2)								
V_{OL}	I_{SINK} = 4mA	0		+0.4	•		•	V
V_{OH}	I_{SOURCE} = 4mA	+2.4		+5	•		•	V
OSC2			Can only be used to drive crystal oscillator.					
Conversion Clock (CLKOUT)								
Drive Capability		±2mA			•			mA
POWER SUPPLIES								
Rated Voltage								
V_A+		+4.75	+5	+5.25	•	•	•	V
V_A-		–5.25	–5	–4.75	•	•	•	V
V_D		+4.75	+5	+5.25	•	•	•	V
Power Consumption			250	400		•	•	mW
Supply Current								
I_A+			30			•		mA
I_A-			–13			•		mA
I_D			10			•		mA
TEMPERATURE RANGE								
Specification		0		+70	•		•	°C
Storage		–65		+125	•		•	°C

NOTES: (1) All dynamic specifications are based on 2048-point FFTs, using coherent sampling. (2) All specifications in dB are referred to a full-scale input, ±2.75Vp-p. (3) Adjustable to zero with external potentiometer.

MECHANICAL

P Package — 28-Pin Plastic DIP

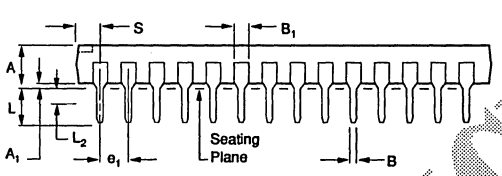


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A(1)	.169	.200	4.29	5.08
A1(1)	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D(1)	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1(1)	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
S1	.040	.080	1.02	2.03

(1) Not JEDEC Standard.

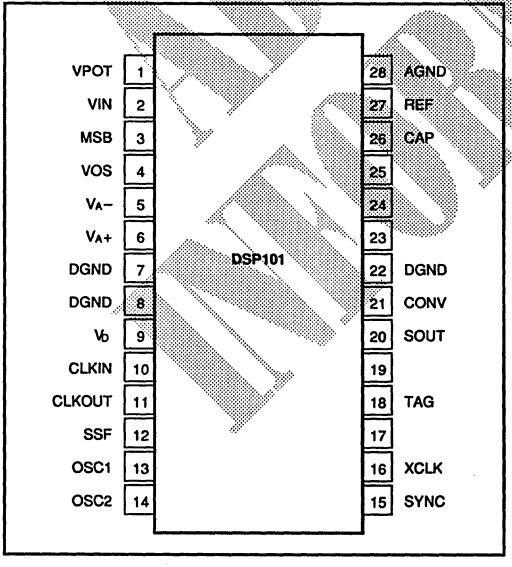
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.



ABSOLUTE MAXIMUM RATINGS

V_A+ to Analog Common	+7V
V_A– to Analog Common	–7V
V_D to Digital Common	+7V
Analog Common to Digital Common	±1V
Control Inputs to Digital Common	–0.5 to V_D + 0.5V
Analog Input Voltage	±5V
Maximum Junction Temperature	150°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}, Plastic DIP	50°C/W

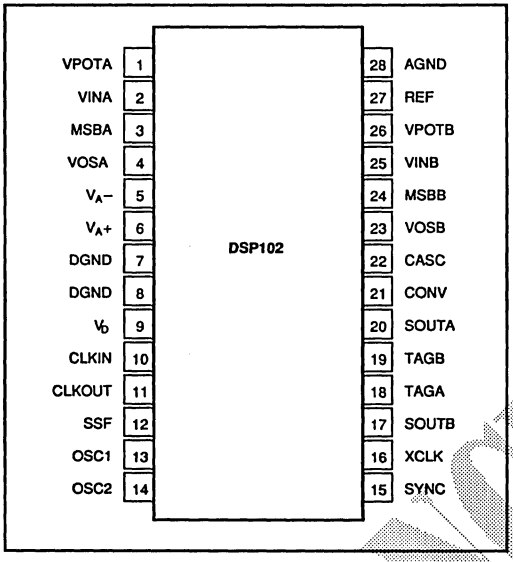
DSP101 PIN CONFIGURATION



DSP101 PIN ASSIGNMENTS

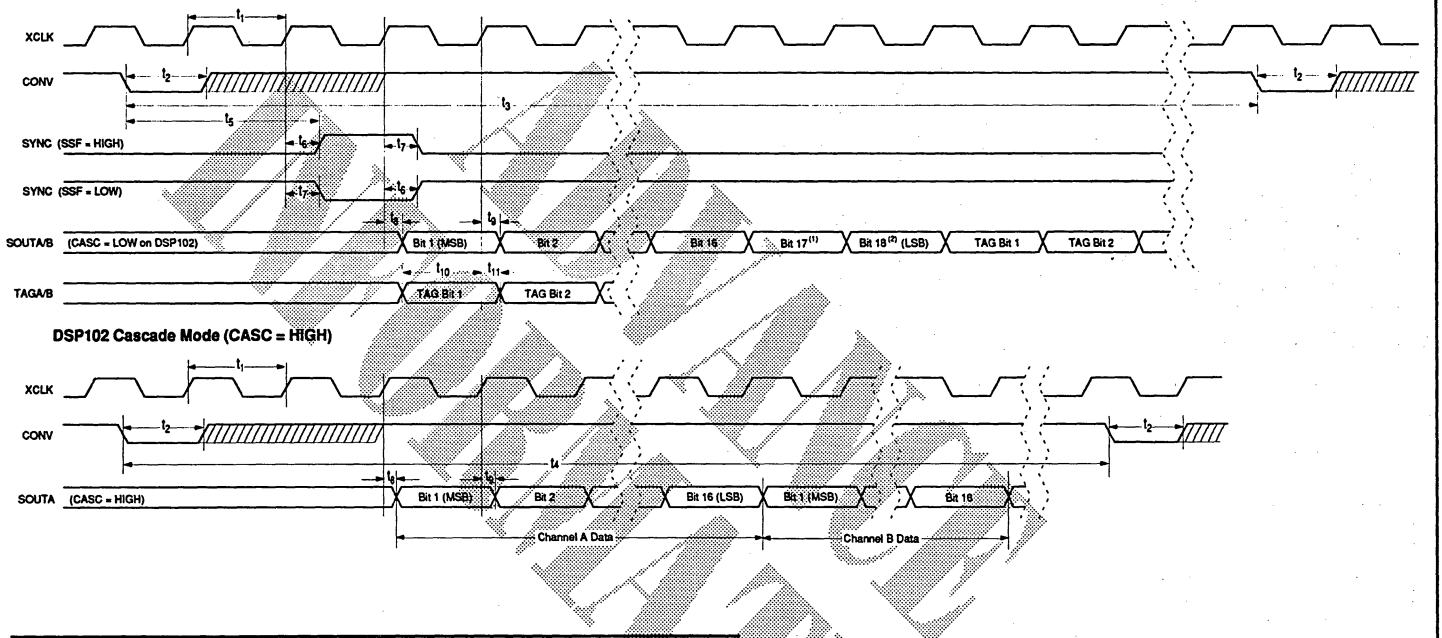
PIN #	NAME	DESCRIPTION
1	VPOT	Trim Reference Out.
2	VIN	Analog In.
3	MSB	MSB Adjust In.
4	VOS	VOS Adjust In.
5	V_A–	–5V Analog Power.
6	V_A+	+5V Analog Power.
7	DGND	Digital Ground.
8	DGND	Digital Ground.
9	V_D	+5V Digital Power.
10	CLKIN	Conversion Clock In.
11	CLKOUT	Conversion Clock Out. Can drive multiple DSP101/DSP102s to synchronize conversion.
12	SSF	Select Synch Format In. If HIGH, SYNC will be active High. If LOW, SYNC will be active Low. See timing diagram (Figure 1).
13	OSC1	Oscillator Point 1 In/External Clock In. If using external clock, drive with 74HC logic levels.
14	OSC2	Oscillator Point 2 Out. Provides drive for crystal oscillator. Make no electrical connection if using external clock.
15	SYNC	Data Synchronization Out. Active High when SSF is HIGH; active Low when SSF is LOW.
16	XCLK	Data Transfer Clock In.
17		No Connection.
18	TAG	User Tag In. Data clocked into this pin is appended to the conversion results on SOUT. See timing diagram (Figure 1).
19		No Connection.
20	SOUT	Serial Data Out. MSB first, Binary Two's Complement format.
21	CONV	Convert Command In. Falling edge puts converter into hold state, initiates conversion, and transmits previous conversion results to DSP IC with appropriate SYNC pulse.
22	DGND	Digital Ground.
23		No Connection.
24		No Connection.
25		No Connection.
26	CAP	Bypass Capacitor.
27	REF	Reference Bypass.
28	AGND	Analog Ground.

DSP102 PIN CONFIGURATION

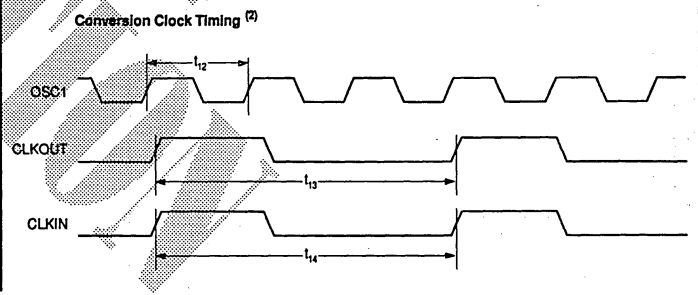


DSP102 PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	VPOTA	Channel A Trim Reference Out.
2	VINA	Channel A Analog In.
3	MSBA	Channel A MSB Adjust In.
4	VOSA	Channel A VOS Adjust In.
5	V_A-	–5V Analog Power.
6	V_A+	+5V Analog Power.
7	DGND	Digital Ground.
8	DGND	Digital Ground.
9	V_D	+5V Digital Power.
10	CLKIN	Conversion Clock In.
11	CLKOUT	Conversion Clock Out. Can drive multiple DSP101/DSP102s to synchronize conversion.
12	SSF	Select Synch Format In. If HIGH, SYNC will be active High. If LOW, SYNC will be active Low. See timing diagram (Figure 1).
13	OSC1	Oscillator Point 1 In / External Clock In. If using external clock, drive with 74HC logic levels.
14	OSC2	Oscillator Point 2 Out. Provides drive for crystal oscillator. Make no electrical connection if using external clock.
15	SYNC	Data Synchronization Out. Active High when SSF is HIGH; active Low when SSF is LOW.
16	XCLK	Data Transfer Clock In.
17	SOUTB	Channel B Serial Data Out. MSB first, Binary Two's Complement format.
18	TAGA	Channel A User Tag In. Data clocked into this pin is appended to the conversion results of SOUTA. See timing diagram (Figure 1).
19	TAGB	Channel B User Tag In. Data clocked into this pin is appended to the conversion results of SOUTB. See timing diagram (Figure 1).
20	SOUTA	Channel A Serial Data Out. MSB first, Binary Two's Complement format. If CASC is HIGH, 32 bits of data output, with first 16 bits being Channel A data.
21	CONV	Convert Command In. Falling edge puts converter into hold state, initiates conversion, and transmits previous conversion results to DSP IC with appropriate SYNC pulse.
22	CASC	Select Cascade Mode In. If HIGH, DSP102 transmits a 32-bit word on SOUTA, with the first 16 bits being data on Channel A. If LOW, DSP102 transmits data for both channels simultaneously.
23	VOSB	Channel B VOS Adjust In.
24	MSBB	Channel B MSB Adjust In.
25	VINB	Channel B Analog In.
26	VPOTB	Channel B Trim Reference Out.
27	REF	Reference Bypass.
28	AGND	Analog Ground.

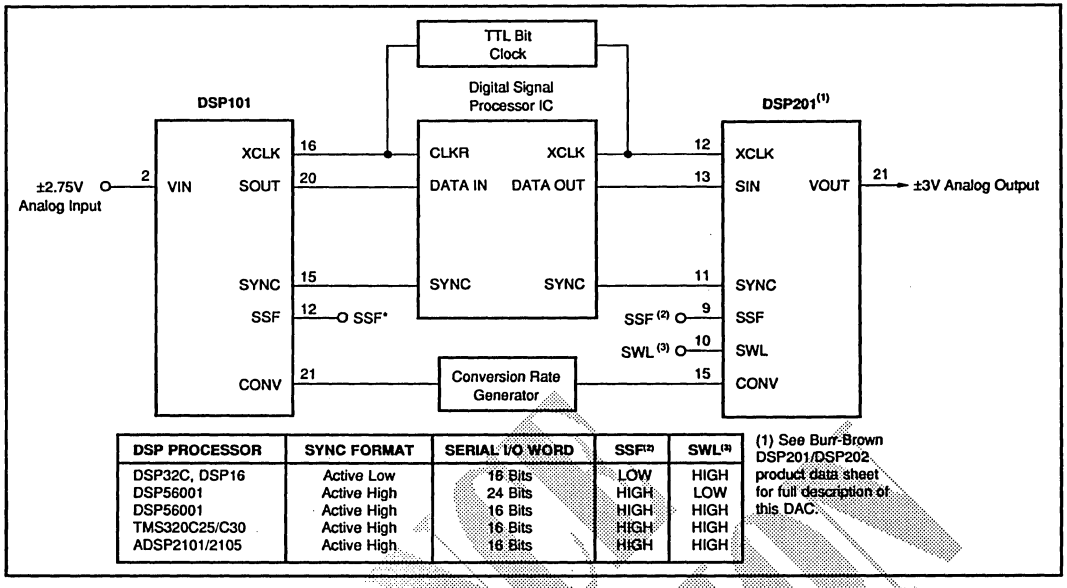


SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_1	XCLK period. Duty Cycle 50% ±10%	83		ns
t_2	Convert Command LOW Time	50		ns
t_3	Convert Period (CASC = LOW on DSP102)	24		t_1
t_4	Convert Period (CASC = HIGH on DSP102)	40		t_1
t_5	SYNC Active Delay after Convert Falling Edge	t_1 +40	2 t_1	ns
t_6	SYNC LOW to HIGH Delay from XCLK Rising; C_L = 50pF		15	ns
t_7	SYNC HIGH to LOW Delay from XCLK Rising; C_L = 50pF		15	ns
t_8	SOUTA/B Data Valid Delay from XCLK Rising; C_L = 50pF		15	ns
t_9	SOUTA/B Data Valid After from XCLK Rising; C_L = 50pF	10		ns
t_{10}	TAGA/B Data Setup before XCLK Rising	20		ns
t_{11}	TAGA/B Data Hold after XCLK Rising		0	ns
t_{12}	OSC1 Period.(2) Duty Cycle 50% ± 10%	67	667	ns
t_{13}	CLKOUT Period. Duty Cycle 33% ± 10%	3 t_{12}		ns
t_{14}	CLKIN Period. Duty Cycle 33% ± 20%	200	2000	ns



NOTES: (1)When using a DSP IC in a 16-bit mode, these data bits will be ignored by the processor. (2) f_{OSC1} must be at least 72 times faster than the conversion rate. (t_3, $t_4 \geq 72\ t_{12}$)

FIGURE 1. DSP101 and DSP102 Timing.



DSP PROCESSOR	SYNC FORMAT	SERIAL I/O WORD	SSF[2]	SWL[3]
DSP32C, DSP16	Active Low	16 Bits	LOW	HIGH
DSP56001	Active High	24 Bits	HIGH	LOW
DSP56001	Active High	16 Bits	HIGH	HIGH
TMS320C25/C30	Active High	16 Bits	HIGH	HIGH
ADSP2101/2105	Active High	16 Bits	HIGH	HIGH

(1) See Burr-Brown DSP201/DSP202 product data sheet for full description of this DAC.

FIGURE 2. Analog Input and Analog Output System.

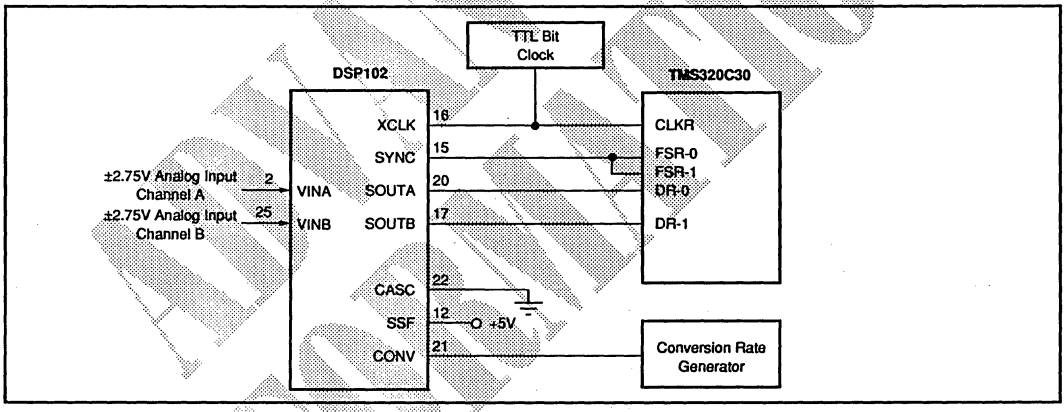


FIGURE 3. Using DSP102 with TMS320C30.

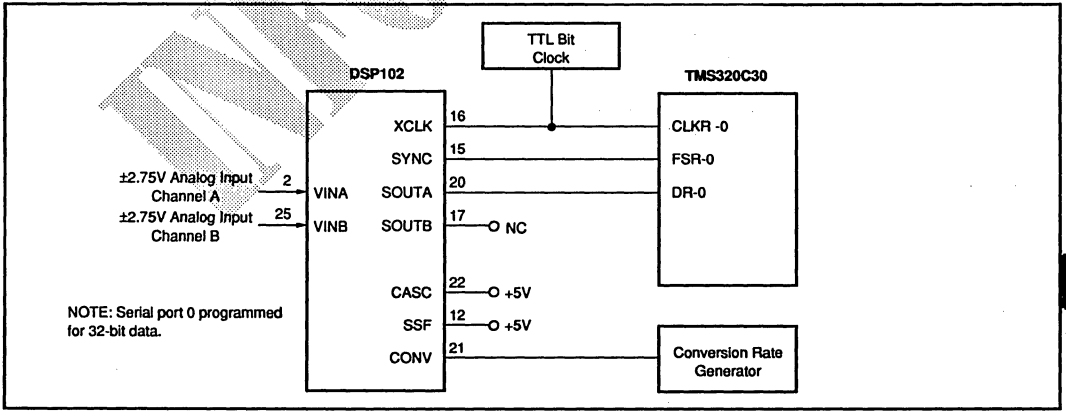


FIGURE 4. Using DSP102 with TMS320C30 in Cascade Mode.

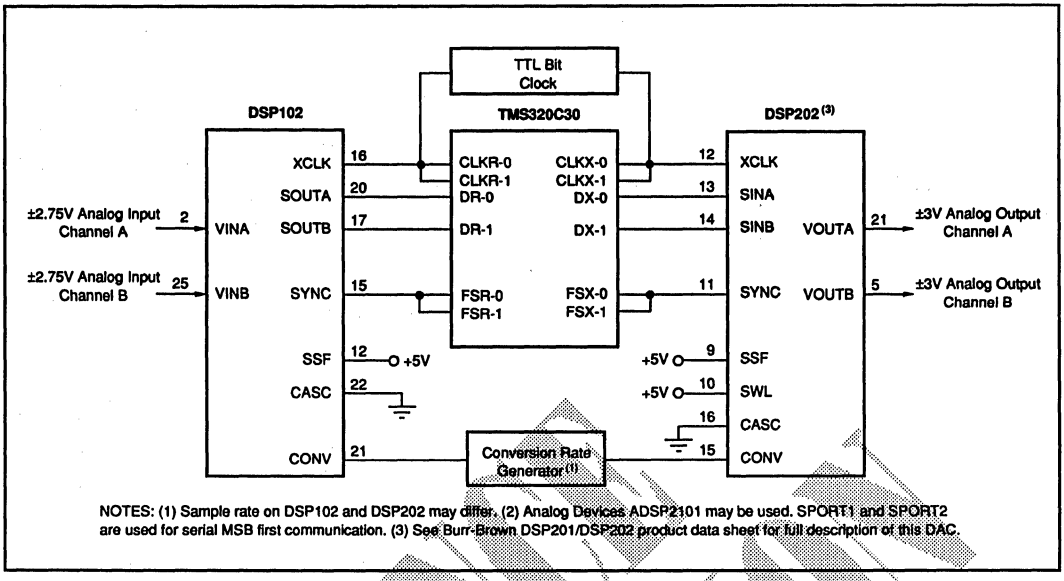


FIGURE 5. Two-Channel Analog Input and Output System with TMS320C30.

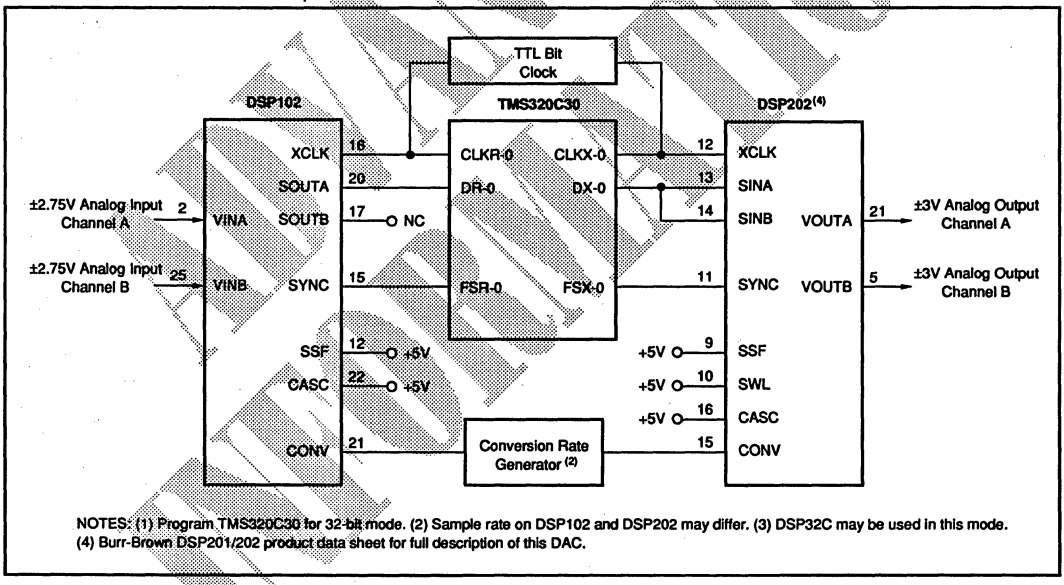


FIGURE 6. Two-Channel Analog Input and Output System with TMS320C30 in Cascade Mode.

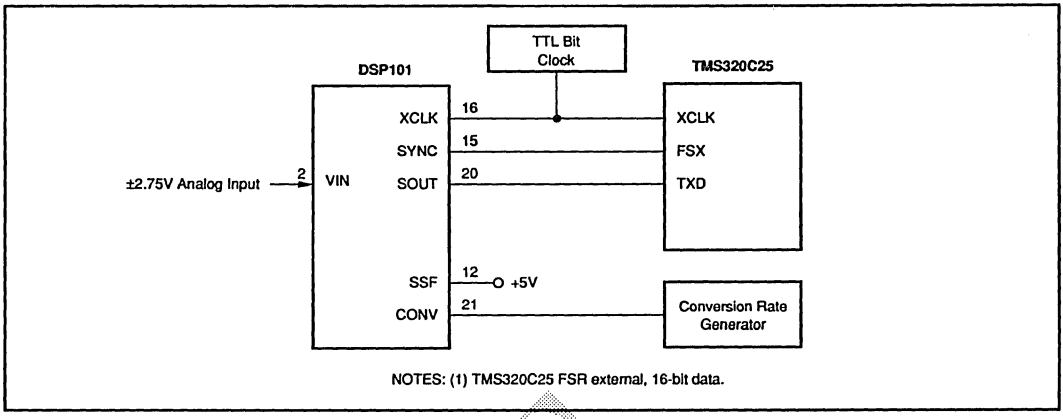


FIGURE 7. Using DSP101 with TMS320C25.

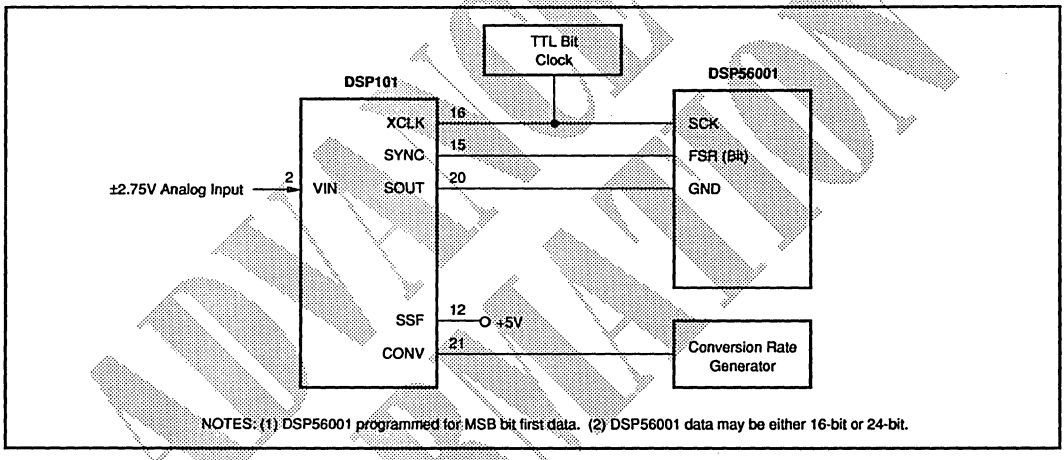


FIGURE 8. Using DSP101 with DSP56001.

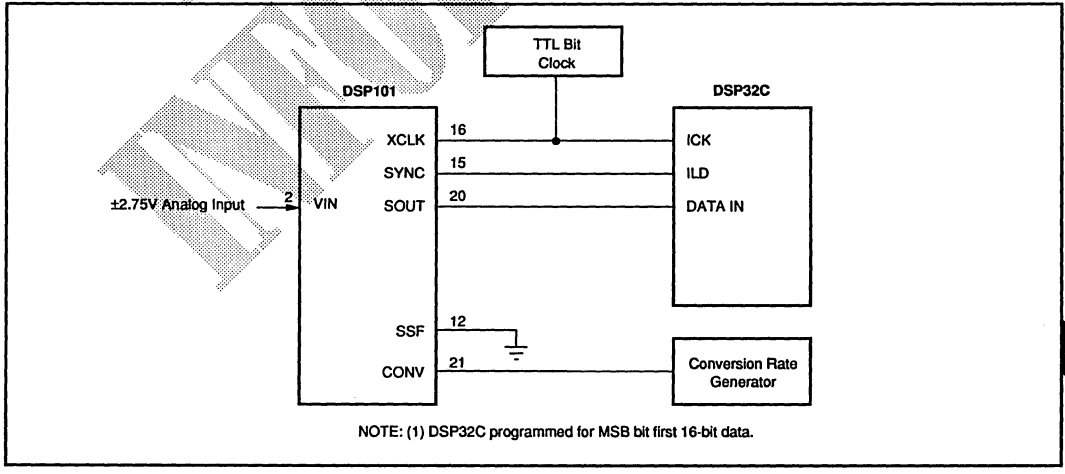


FIGURE 9. Using DSP101 with DSP32C.

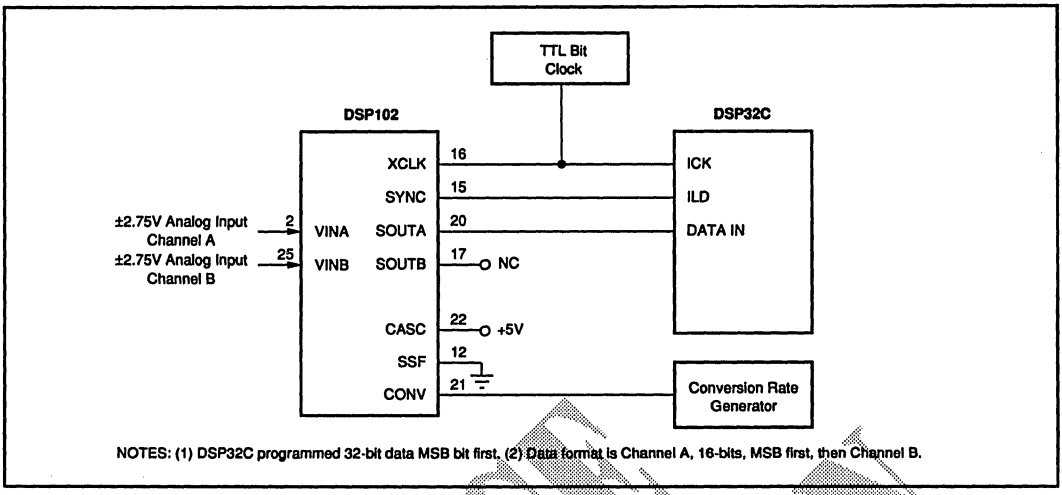


FIGURE 10. Using DSP202 with DSP32C in Cascade Mode.

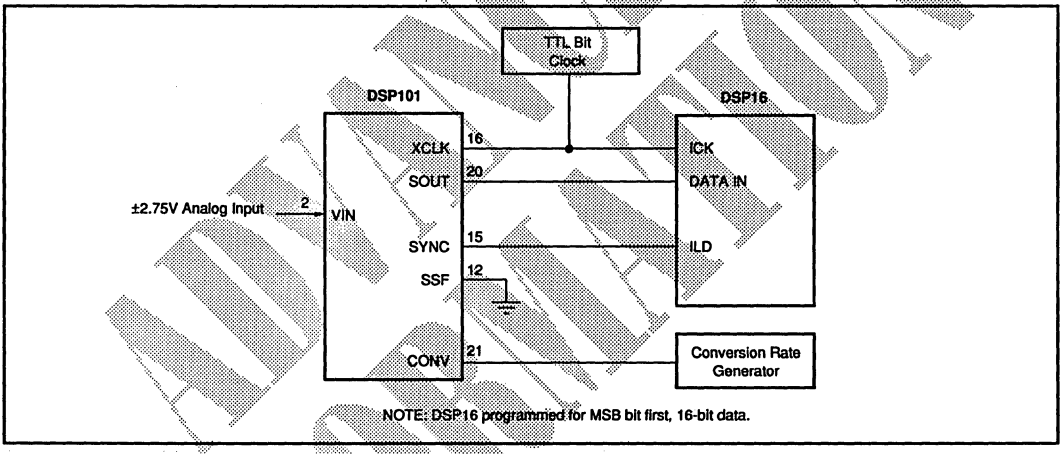


FIGURE 11. Using DSP101 with DSP16.

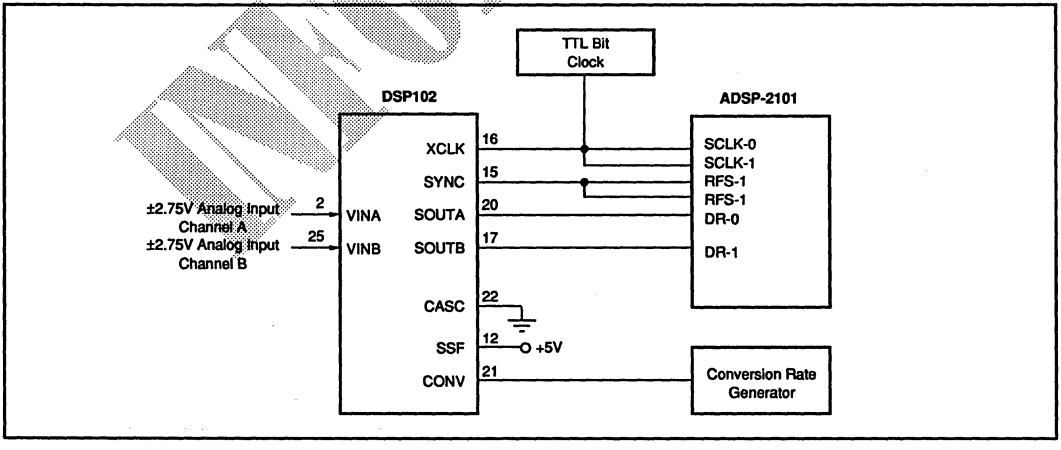


FIGURE 12. Using DSP102 with ADSP-2101.

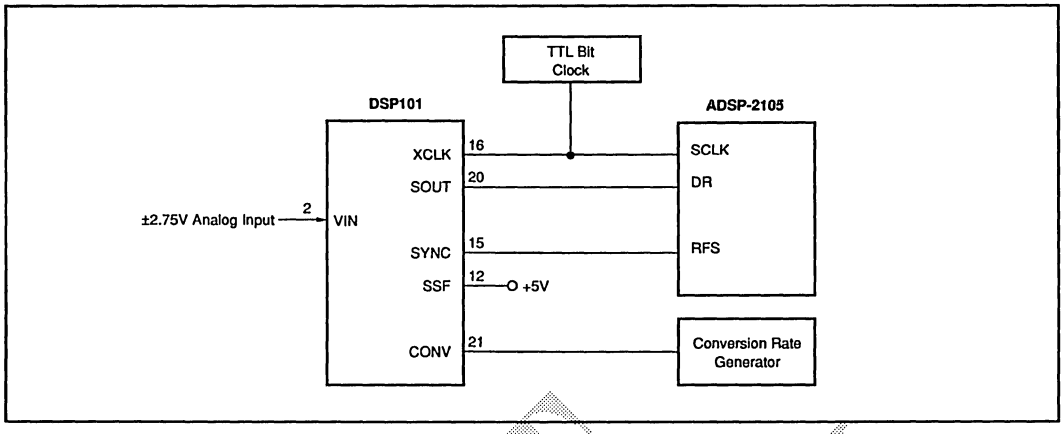


FIGURE 13. Using DSP101 with ADSP-2105.

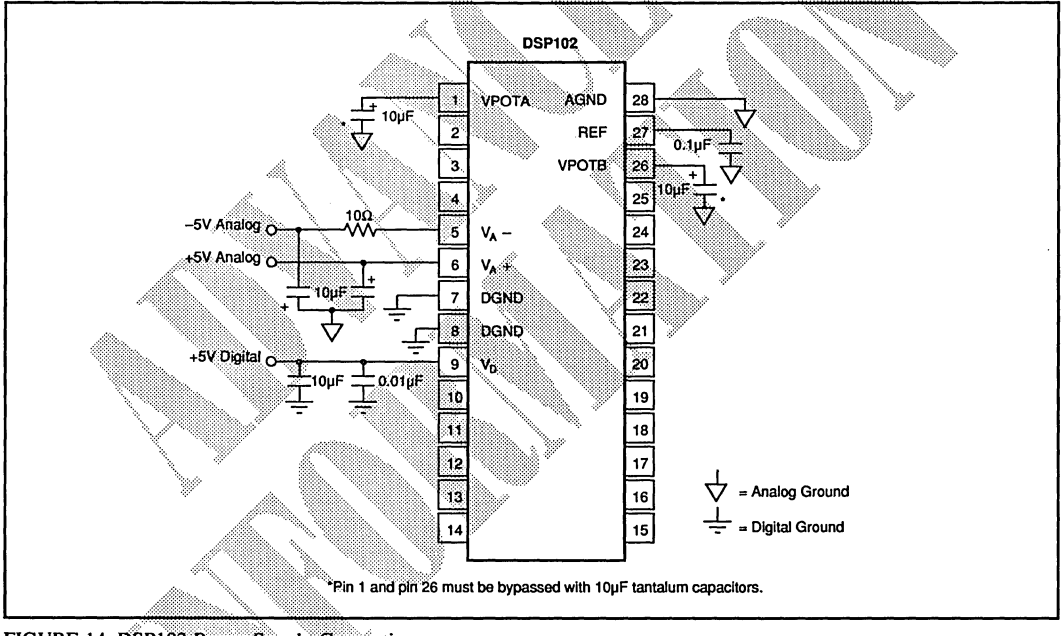


FIGURE 14. DSP102 Power Supply Connections.

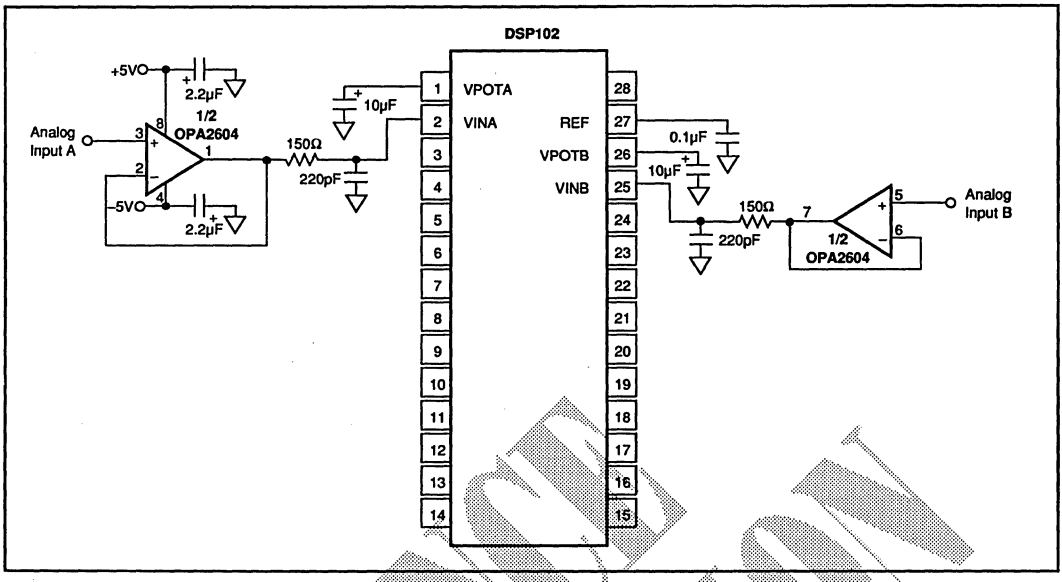


FIGURE 15. DSP102 Input Buffering.

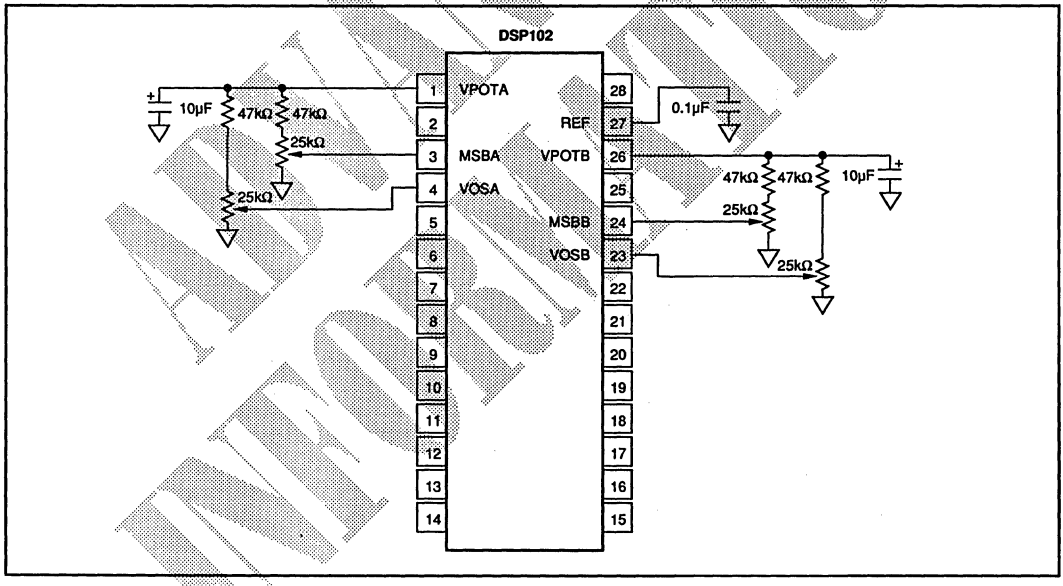


FIGURE 16. DSP102 Optional MSB and Offset Adjust.

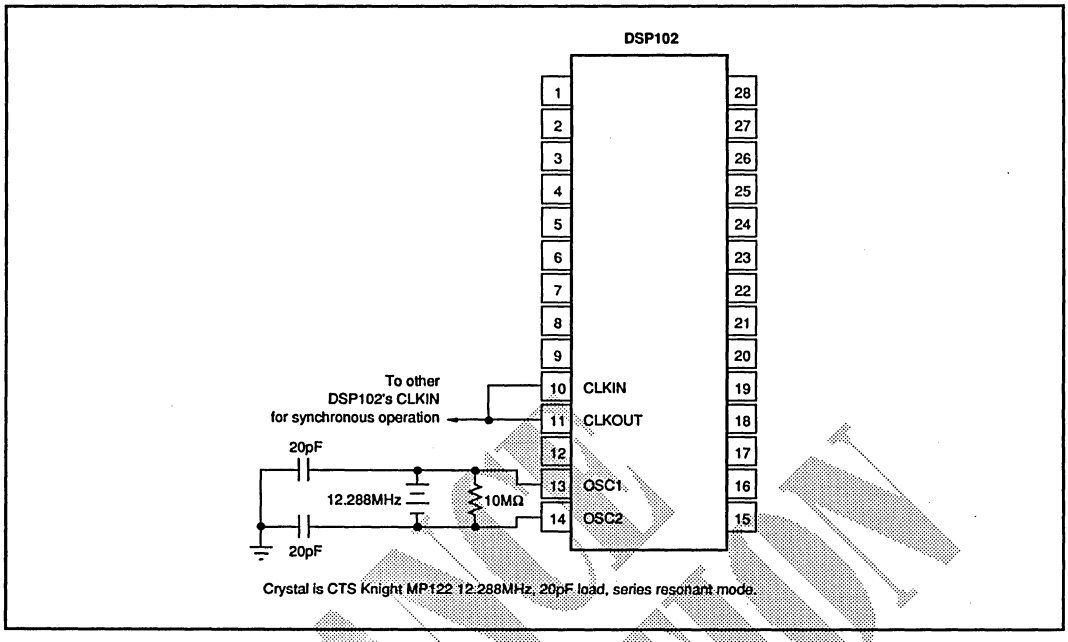


FIGURE 17. DSP102 Conversion Clock Circuit.

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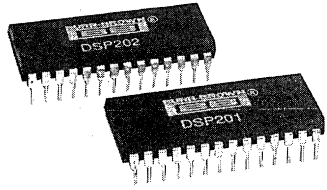


DSP201
DSP202

DSP-Compatible Single/Dual DIGITAL-TO-ANALOG CONVERTERS

FEATURES

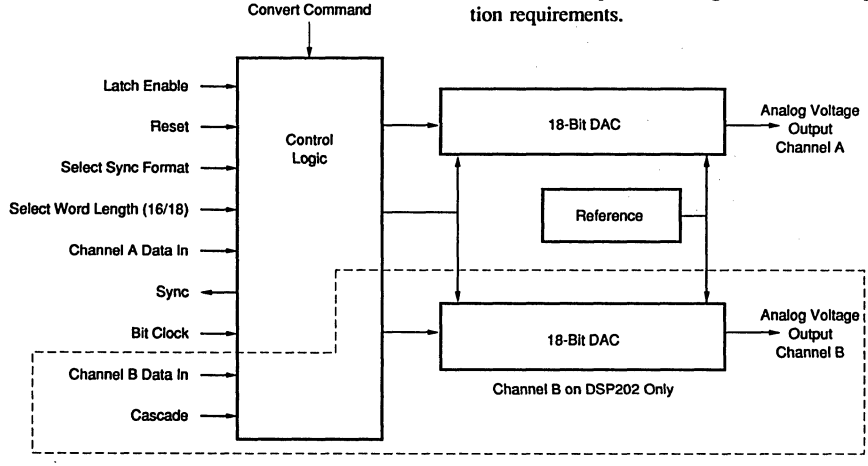
- **ZERO-CHIP INTERFACE TO STANDARD DSP ICs: AD, AT&T, MOTOROLA, TI**
- **SINGLE CHANNEL: DSP201**
- **DUAL CHANNEL: DSP202**
  Two Serial Inputs or Cascade from Single 32-Bit Word
- **SAMPLING RATE TO 500kHz**
- **DYNAMIC SPECIFICATIONS:**
  Signal/(Noise + Distortion) = 90dB;
  THD = –92dB
- **USER SELECTABLE 16-BIT OR 18-BIT DATA WORDS**

DESCRIPTION

The DSP201 and DSP202 are high performance digital-to-analog converters designed for simplicity of use with modern digital signal processing ICs. Both are complete with all interface logic for use directly with DSP ICs, and provide analog output voltages updated at up to 500kHz.

The DSP201 offers a single complete voltage output channel, accepting either 16 bits or 18 bits of input data, and can be driven by 16-bit, 24-bit, or 32-bit serial ports. The DSP202 offers two complete voltage output channels, with either two separate input ports, or a mode to drive both output channels from a single 32-bit word.

Both the DSP201 and DSP202 are packaged in standard, low-cost 28-pin plastic DIP packages. Each is offered in two performance grades to match application requirements.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1067

SPECIFICATIONS

ELECTRICAL

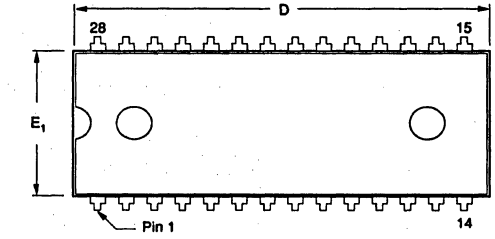
T_A = 0°C to 70°C, Output Update Frequency, f_S = 400kHz, $V_A+ = V_D+ = +5V$, $V_A- = V_D- = -5V$, unless otherwise specified.

PARAMETER	CONDITIONS	DSP201JP DSP202JP MIN	DSP201JP DSP202JP TYP	DSP201JP DSP202JP MAX	DSP201KP DSP202KP MIN	DSP201KP DSP202KP TYP	DSP201KP DSP202KP MAX	UNITS
RESOLUTION				18			•	Bits
DYNAMIC RANGE			108			•		dB
ANALOG OUTPUT								
Voltage Range	R_L = 375Ω		±3		•			V
Impedance			0.1			•		Ω
Current	R_L = 375Ω		±8		•			mA
THROUGHPUT SPEED (1)								
Update Rate	CASC = LOW on DSP202	500			•			kHz
DSP202 in Cascade Mode	CASC = HIGH	300						kHz
AC ACCURACY (2, 3)								
Signal to (Noise + Distortion) Ratio	f_{OUT} = 1kHz	82	86		88	90		dB(4)
	f_{OUT} = 1kHz (–60dB)		30			32		dB
	f_{OUT} = 10kHz	80	86		86	90		dB
Total Harmonic Distortion	f_{OUT} = 1kHz		–90	–85		–92	–88	dB
Channel Separation on DSP202	f_{OUT} = 1kHz to 100kHz		105			•		dB
DC ACCURACY								
Integral Nonlinearity Error			±0.006			±0.004		%
Differential Nonlinearity Error			±0.006			±0.004		%
Bipolar Zero Error (5)			±10					mV
Bipolar Zero Error Drift			20			•		ppm FSR/°C
Bipolar Zero Mismatch (5)	DSP202 Channels		5			•		mV
Gain Error (5)			1	3		•	•	%
Gain Error Drift			100			•		ppm/°C
Gain Error Mismatch (5)	DSP102 Channels		1	3		•	•	%
Digital Feedthrough	$\overline{ENABLE}$ = HIGH		–105					dB
Power Supply Sensitivity	$-5.1 < V_A-, V_D- < -4.9$		–60			•		dB
	$+4.9 < V_A+, V_D+ < +5.1$		–60			•		dB
DIGITAL INPUTS								
Format			Serial; MSB first; 16/18-bit and Cascaded					
Coding			Binary Twos Complement					
Logic Levels								
V_{IL}	I_{IL} = ±10µA	0		+0.8	•		•	V
V_{IH}	I_{IH} = ±10µA	+2.4		+5	•		•	V
Data Transfer Clock								
Frequency		0.1		12	•		•	MHz
Duty Cycle		40	50	60	•	•	•	%
DIGITAL OUTPUTS								
V_{OL}	I_{OL} = 4mA	0		+0.4	•		•	V
V_{OH}	I_{OH} = 4mA	+2.4		+5	•		•	V
POWER SUPPLIES								
Rated Voltage								
V_A+		+4.75	+5	+5.25	•	•	•	V
V_A-		–5.25	–5	–4.75	•	•	•	V
V_D+		+4.75	+5	+5.25	•	•	•	V
V_D-		–5.25	–5	–4.75	•	•	•	V
Current								
I_A+			18			•		mA
I_A-			17			•		mA
I_D+			13			•		mA
I_D-			25			•		mA
Power Consumption			365	450		•	•	mW
TEMPERATURE RANGE								
Specification		0		+70	•		•	°C
Storage		–65		+150	•		•	°C

NOTES: (1) The data transfer clock must be at least 24 times the update rate for the standard mode, and 40 times the update rate in the DSP202 cascade mode. (2) All dynamic specifications are based on 2048-point FFTs. (3) Data for the 1kHz test is bandlimited to 0 to 20kHz. Data for the 10kHz test is bandlimited to 0 to 40kHz. (4) All specifications in dB are referred to a full-scale output, ±3Vp-p. (5) Adjustable to zero with external potentiometer.

MECHANICAL

P Package — 28-Pin Plastic DIP

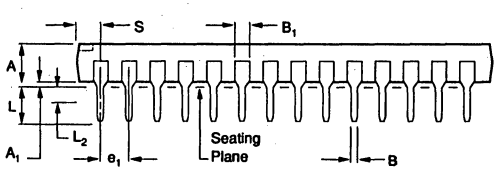


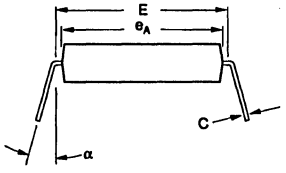
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A(1)	.169	.200	4.29	5.08
A1 (1)	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D(1)	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1 (1)	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
Q1	.020	.070	0.51	1.78
S1	.040	.080	1.02	2.03

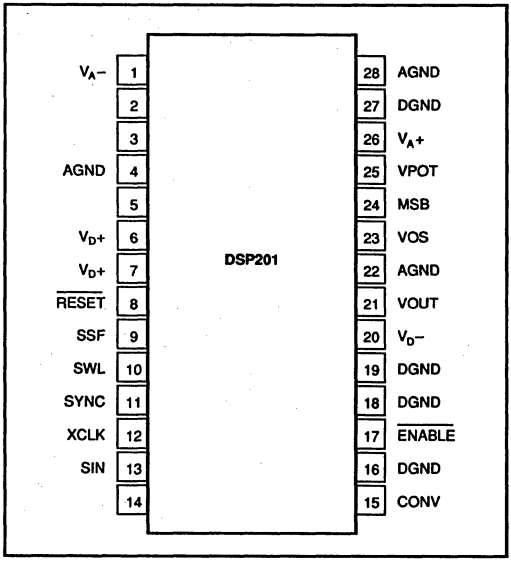
(1) Not JEDEC Standard.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.





DSP201 PIN CONFIGURATION



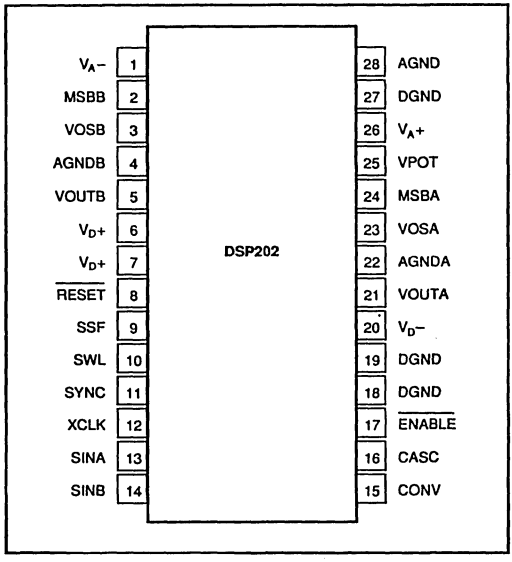
ABSOLUTE MAXIMUM RATINGS

V_A+ to Analog Common	+7V
V_A– to Analog Common	–7V
V_D+ to Digital Common	+7V
V_D– to Digital Common	–7V
Analog Common to Digital Common	±1V
Control Inputs to Digital Common	–0.5 to V_D + 0.5V
Analog Input Voltage	±5V
Maximum Junction Temperature	150°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}: Plastic DIP	50°C/W

DSP201 PIN ASSIGNMENTS

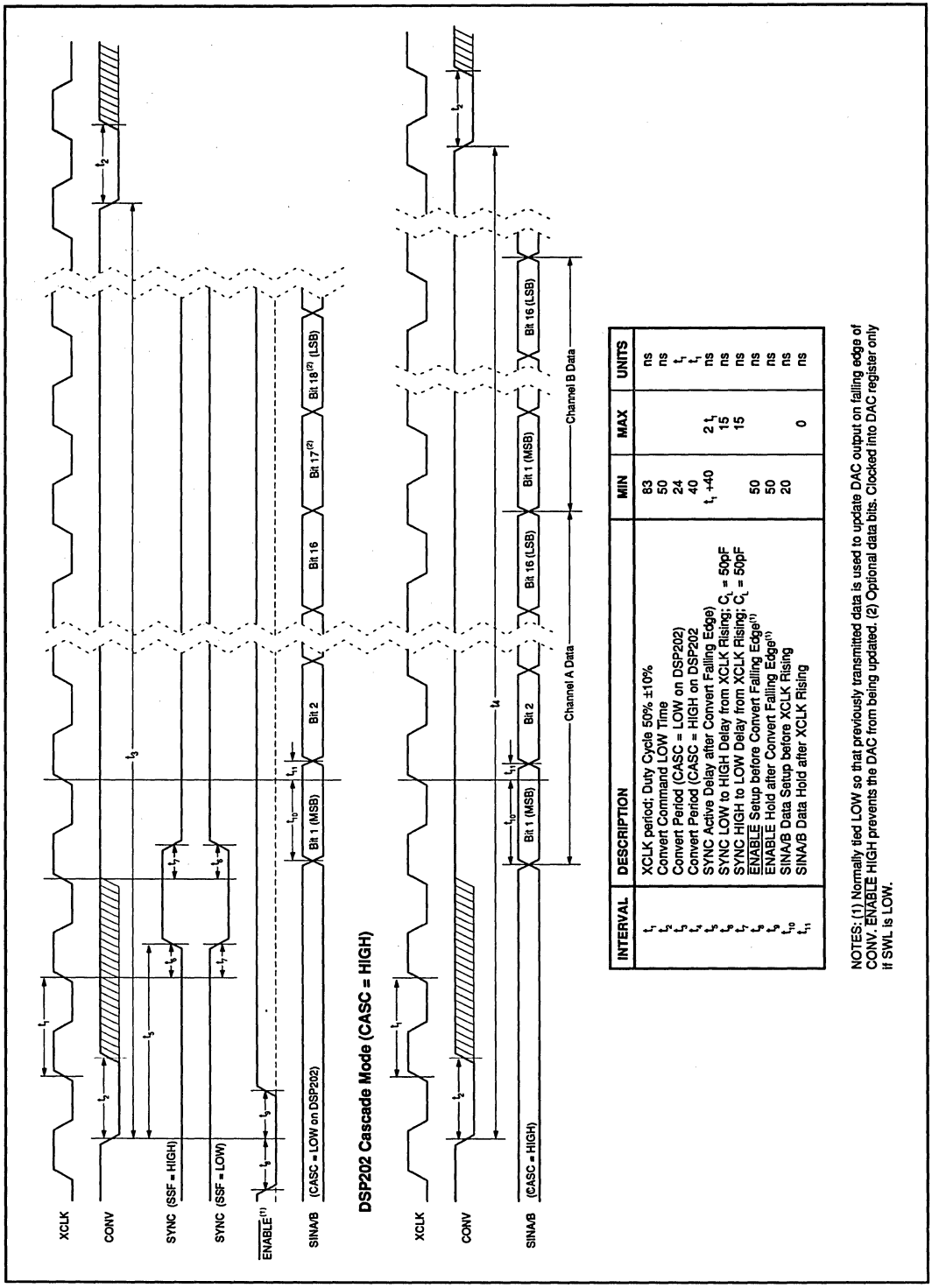
PIN #	NAME	DESCRIPTION
1	V_A–	–5V Analog Power.
2		No Connection.
3		No Connection.
4	AGND	Analog Ground.
5		No Connection.
6	V_D+	+5V Digital Power.
7	V_D+	+5V Digital Power.
8	$\overline{\text{RESET}}$	Reset. If LOW, DAC output will be 0V after two convert commands, and will remain there as long as the Reset input is LOW. If HIGH, normal operation proceeds. Two convert commands are required after Reset goes from LOW to HIGH before the output will relate to the input word.
9	SSF	Select Sync Format In. Tie HIGH for use with Motorola and TI DSP ICs. Tie LOW for use with AT&T DSP ICs.
10	SWL	Select Word Length In. If HIGH, DSP201 accepts first 16 bits of data. If LOW, DSP201 accepts first 18 bits of data.
11	SYNC	Data Synchronization Output. Active HIGH when SSF is HIGH, active LOW when SSF is LOW.
12	XCLK	Data Transfer Clock Input.
13	SIN	Serial Data In. MSB first, Binary Two's Complement format.
14		No Connection.
15	CONV	Convert Command In. DAC is updated on falling edge, and initiates clocking new data in.
16	DGND	Digital Ground.
17	$\overline{\text{ENABLE}}$	Latch Enable In. If LOW, DAC output will be latched with new data word on falling edge of Convert Command. If HIGH, Convert Commands will be ignored.
18	DGND	Digital Ground.
19	DGND	Digital Ground.
20	V_D–	–5V Digital Power.
21	VOUT	Voltage Out.
22	AGND	Analog Ground.
23	VOS	VOS Adjust In.
24	MSB	MSB Adjust In.
25	VPOT	Trim Reference Out for MSB adjustment.
26	V_A+	+5V Analog Power.
27	DGND	Digital Ground.
28	AGND	Analog Ground.

DSP202 PIN CONFIGURATION



DSP202 PIN ASSIGNMENTS

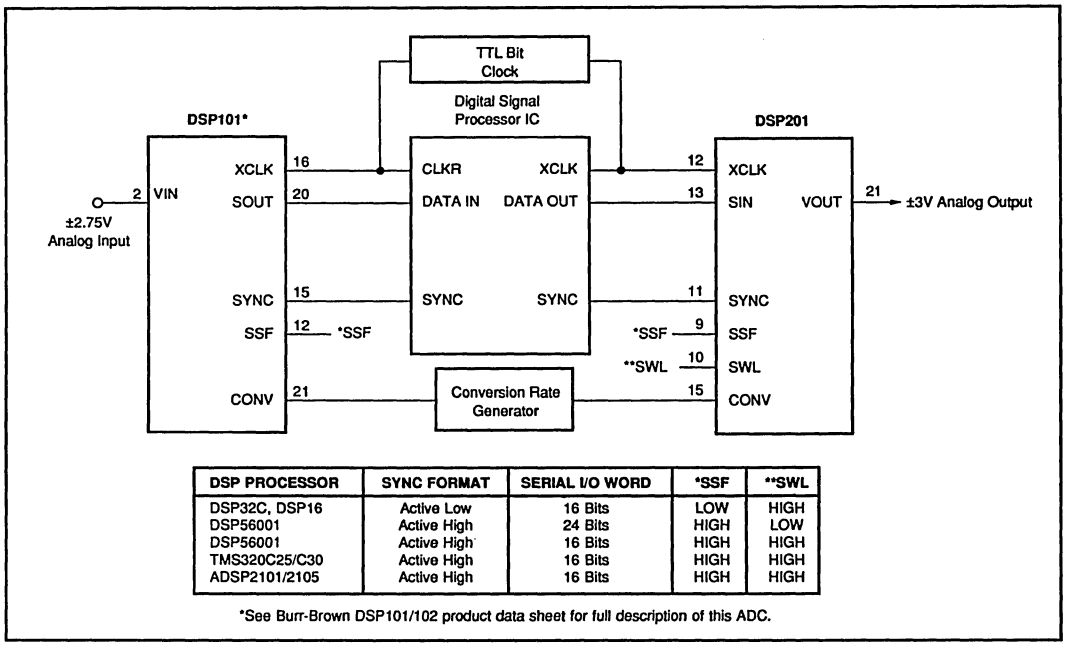
PIN #	NAME	DESCRIPTION
1	V_A-	–5V Analog Power.
2	MSBB	Channel B MSB Adjust In.
3	VOSB	Channel B VOS Adjust In.
4	AGNDB	Channel B Analog Ground.
5	VOUTB	Channel B Voltage Out.
6	V_D+	+5V Digital Power.
7	V_D+	+5V Digital Power.
8	$\overline{RESET}$	Reset. If LOW, DAC output will be 0V after two convert commands, and will remain there as long as the Reset input is LOW. If HIGH, normal operation proceeds. Two convert commands are required after Reset goes from LOW to HIGH before the output will relate to the input word.
9	SSF	Select Sync Format In. Tie HIGH for use with Motorola and TI DSP ICs. Tie LOW for use with AT&T DSP ICs.
10	SWL	Select Word Length In. If HIGH, DSP202 accepts first 16 bits of data. If LOW, DSP202 accepts first 18 bits of data.
11	SYNC	Data Synchronization Output. Active HIGH when SSF is HIGH, active LOW when SSF is LOW.
12	XCLK	Data Transfer Clock Input.
13	SINA	Channel A Serial Data In. MSB first, Binary Two's Complement format. In Cascade Mode, connect to SINB and to DSP IC output.
14	SINB	Channel B Serial Data In. MSB first, Binary Two's Complement format. In Cascade Mode, connect to SINA and to DSP IC output.
15	CONV	Convert Command In. DAC is updated on falling edge, and initiates clocking new data in.
16	CASC	Select Cascade Mode In. If HIGH, DSP202 accepts a 32-bit word, and uses the first 16 bits to update channel A, and the second 16 bits to update channel B. In Cascade Mode, SINA and SINB are connected together. If CASC is LOW, data is strobed into both channels on each clock cycle.
17	$\overline{ENABLE}$	Latch Enable In. If LOW, DAC output will be latched with new data word on falling edge of Convert Command. If HIGH, Convert Commands will be ignored.
18	DGND	Digital Ground.
19	DGND	Digital Ground.
20	V_D-	–5V Digital Power.
21	VOUTA	Channel A Voltage Out.
22	AGNDA	Channel A Analog Ground.
23	VOSA	Channel A VOS Adjust In.
24	MSBA	Channel A MSB Adjust In.
25	VPOT	Trim Reference Out for MSB adjustments.
26	V_A+	+5V Analog Power.
27	DGND	Digital Ground.
28	AGND	Analog Ground.



INTERVAL	DESCRIPTION	MIN	MAX	UNITS
t_1	XCLK period; Duty Cycle 50% ±10%	83		ns
t_2	Convert Command LOW Time	50		ns
t_3	Convert Period (CASC = LOW on DSP202)	24		t_1
t_4	Convert Period (CASC = HIGH on DSP202	40		t_1
t_5	SYNC Active Delay after Convert Falling Edge)	t_1 +40	2 t_1	ns
t_6	SYNC LOW to HIGH Delay from XCLK Rising; C_L = 50pF		15	ns
t_7	SYNC HIGH to LOW Delay from XCLK Rising; C_L = 50pF		15	ns
t_8	ENABLE Setup before Convert Falling Edge(1)	50		ns
t_9	ENABLE Hold after Convert Falling Edge(1)	50		ns
t_{10}	SINA/B Data Setup before XCLK Rising	20		ns
t_{11}	SINA/B Data Hold after XCLK Rising		0	ns

NOTES: (1) Normally tied LOW so that previously transmitted data is used to update DAC output on falling edge of CONV. ENABLE HIGH prevents the DAC from being updated. (2) Optional data bits. Clocked into DAC register only if SWL is LOW.

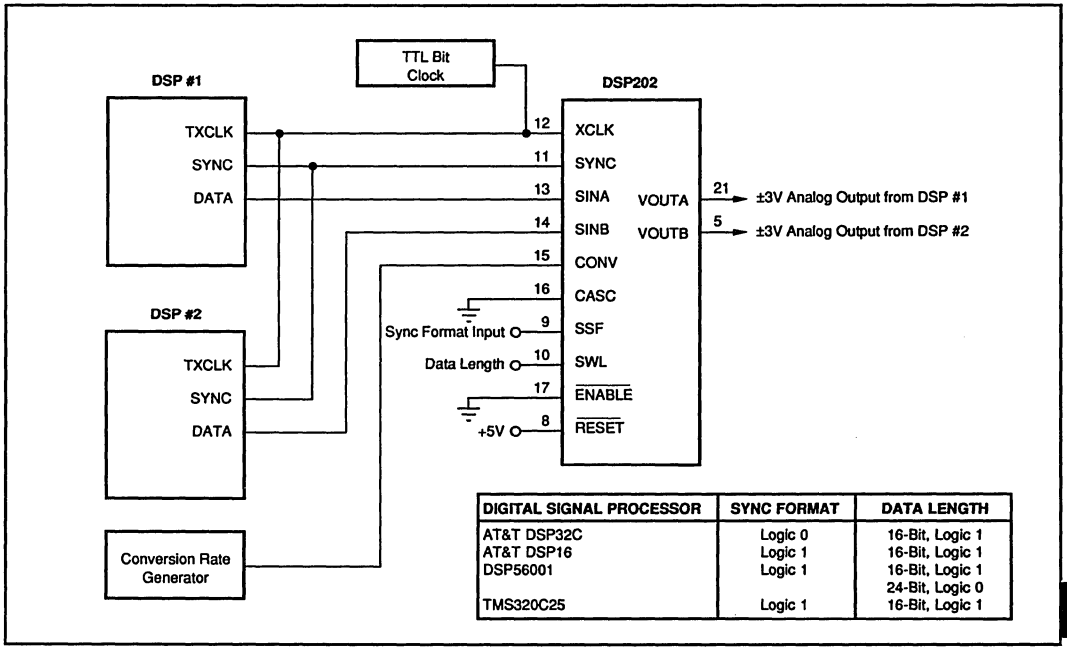
FIGURE 1. DSP201 and DSP202 Timing.



DSP PROCESSOR	SYNC FORMAT	SERIAL I/O WORD	*SSF	**SWL
DSP32C, DSP16	Active Low	16 Bits	LOW	HIGH
DSP56001	Active High	24 Bits	HIGH	LOW
DSP56001	Active High	16 Bits	HIGH	HIGH
TMS320C25/C30	Active High	16 Bits	HIGH	HIGH
ADSP2101/2105	Active High	16 Bits	HIGH	HIGH

*See Burr-Brown DSP101/102 product data sheet for full description of this ADC.

FIGURE 2. Analog Input and Analog Output System.



DIGITAL SIGNAL PROCESSOR	SYNC FORMAT	DATA LENGTH
AT&T DSP32C	Logic 0	16-Bit, Logic 1
AT&T DSP16	Logic 1	16-Bit, Logic 1
DSP56001	Logic 1	16-Bit, Logic 1 24-Bit, Logic 0
TMS320C25	Logic 1	16-Bit, Logic 1

FIGURE 3. DSP202 with Dual DSP ICs.

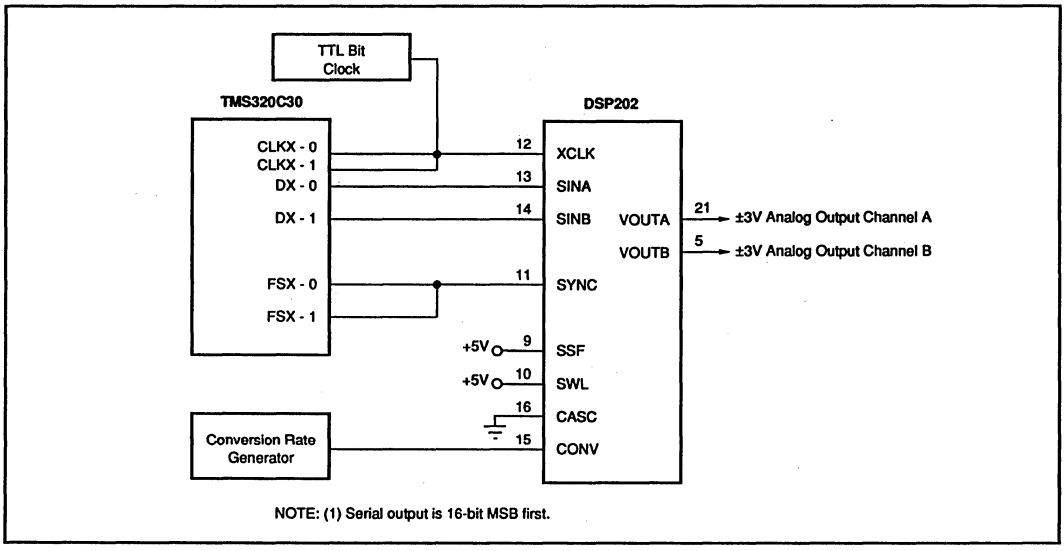


FIGURE 4. Using DSP202 with TMS320C30's Dual SIO.

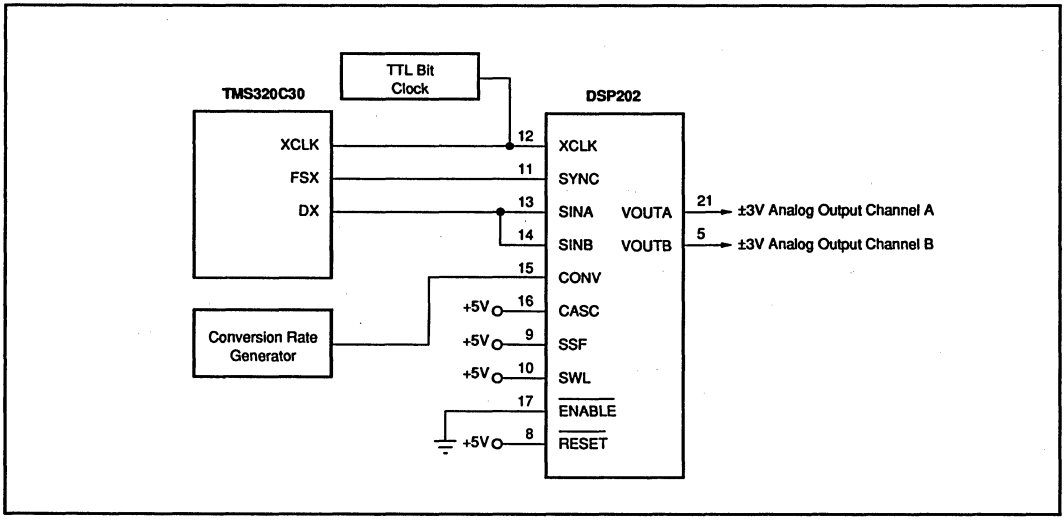
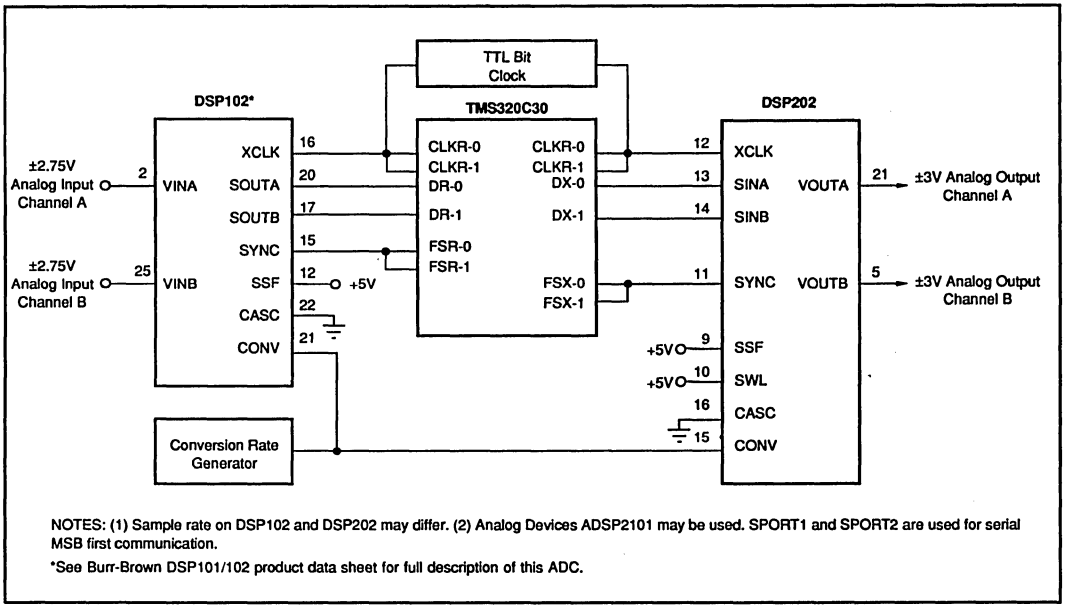


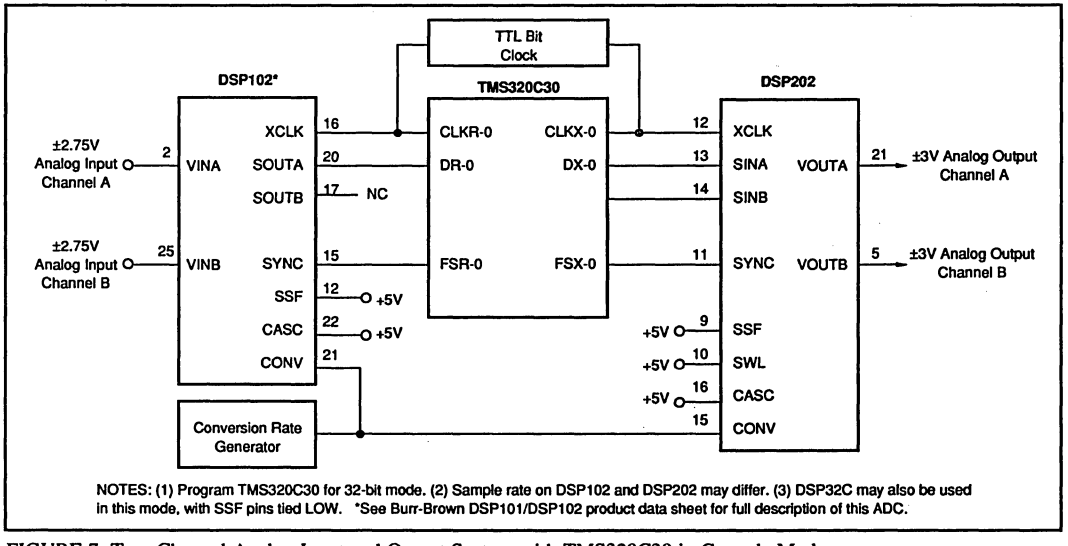
FIGURE 5. Using DSP202 with TMS320C30 in Cascade Mode.



NOTES: (1) Sample rate on DSP102 and DSP202 may differ. (2) Analog Devices ADSP2101 may be used. SPORT1 and SPORT2 are used for serial MSB first communication.

*See Burr-Brown DSP101/102 product data sheet for full description of this ADC.

FIGURE 6. Two-Channel Analog Input and Output System with TMS320C30.



NOTES: (1) Program TMS320C30 for 32-bit mode. (2) Sample rate on DSP102 and DSP202 may differ. (3) DSP32C may also be used in this mode, with SSF pins tied LOW. *See Burr-Brown DSP101/DSP102 product data sheet for full description of this ADC.

FIGURE 7. Two-Channel Analog Input and Output System with TMS320C30 in Cascade Mode.

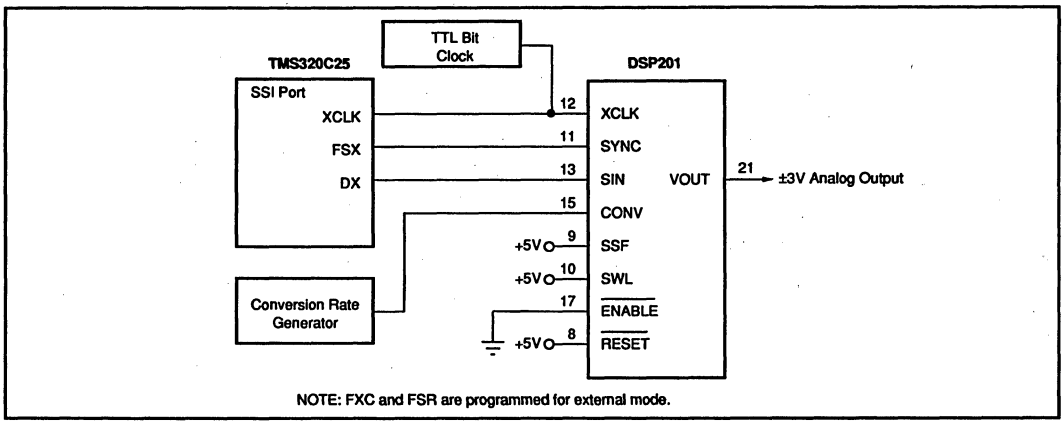


FIGURE 8. Using DSP201 with TMS320C25.

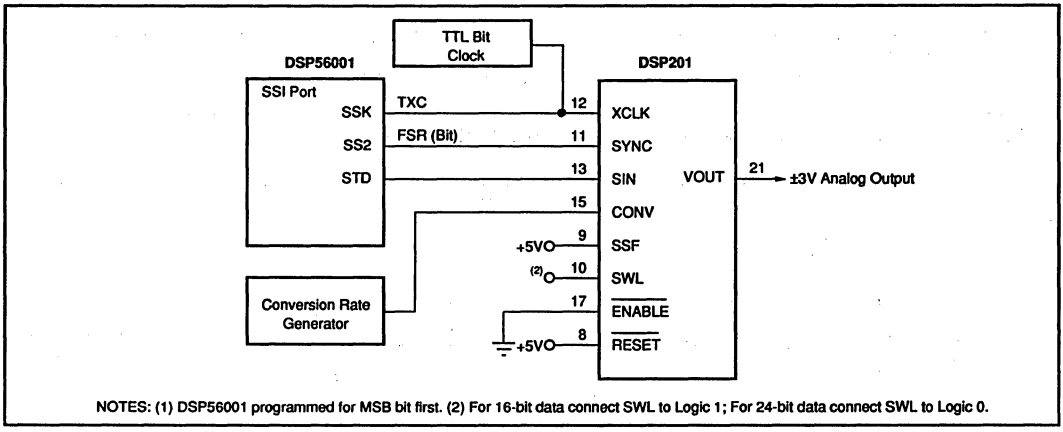


FIGURE 9. Using DSP201 with DSP56001.

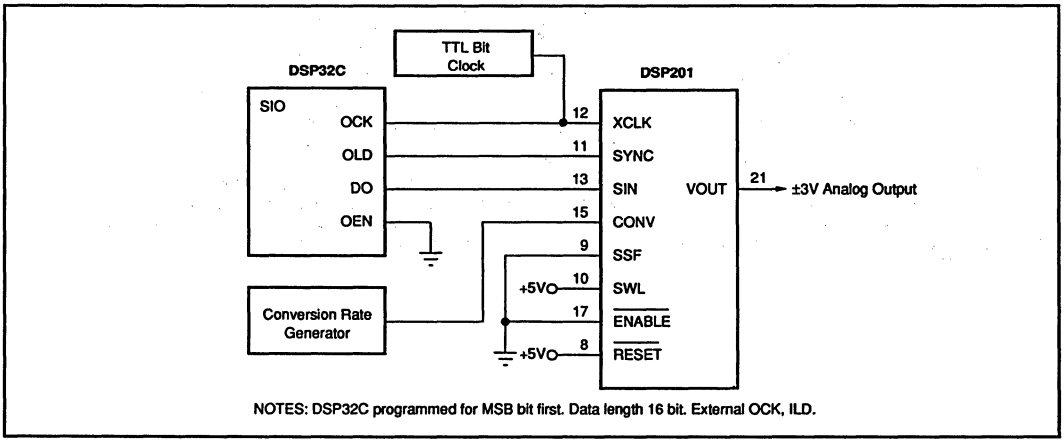


FIGURE 10. Using DSP201 with DSP32C with 16-Bit Data Words.

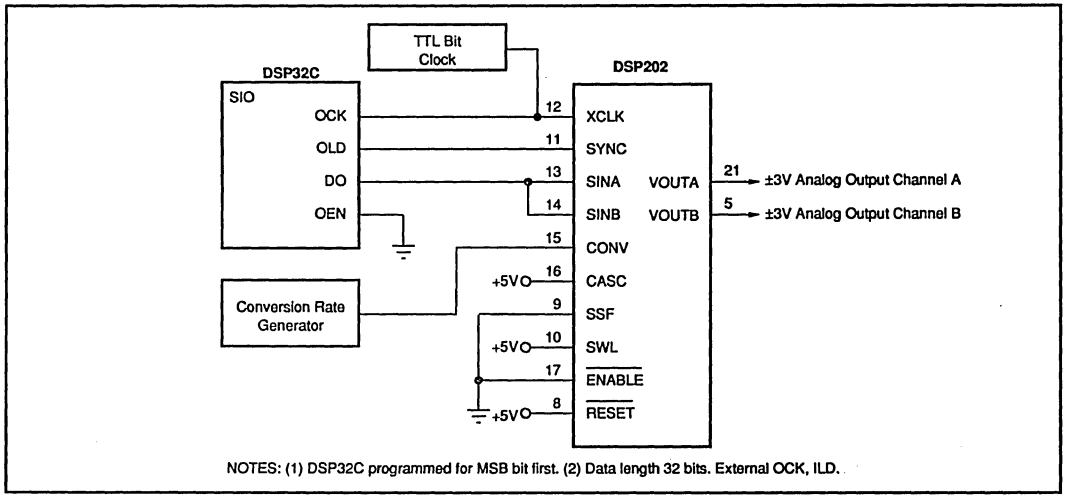


FIGURE 11. Using DSP202 with DSP32C in Cascade Mode.

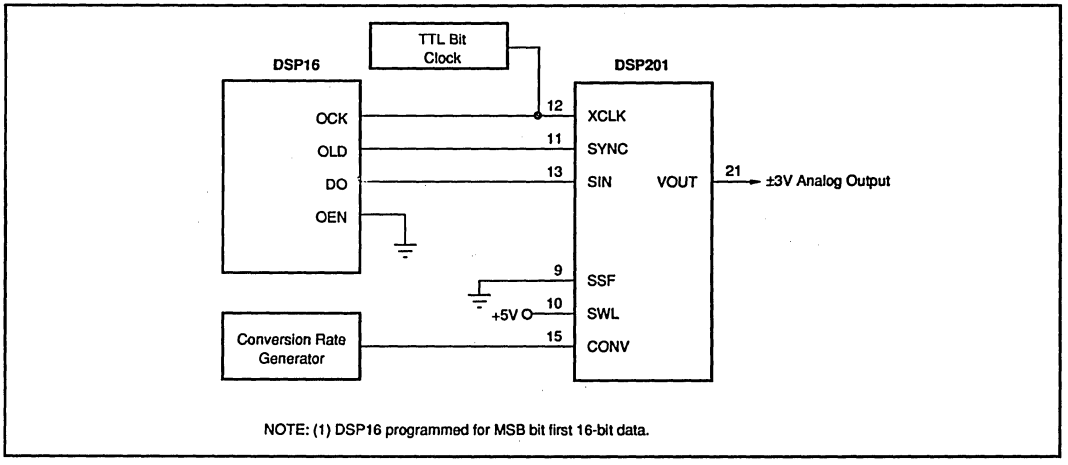


FIGURE 12. Using DSP201 with DSP16.

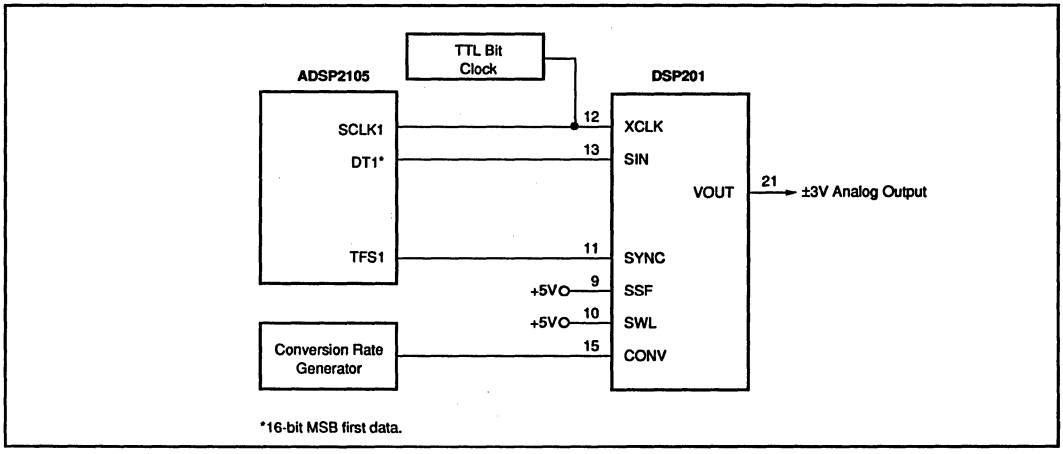


FIGURE 13. Using DSP201 with ADSP-2105.

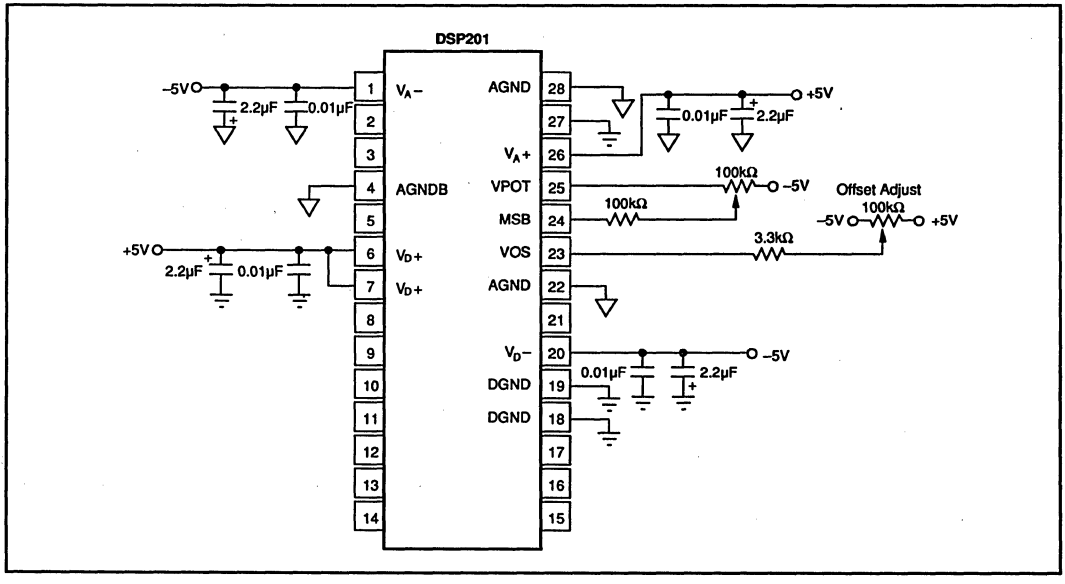


FIGURE 14. DSP201 Power Supply Connections and Adjust Circuits.

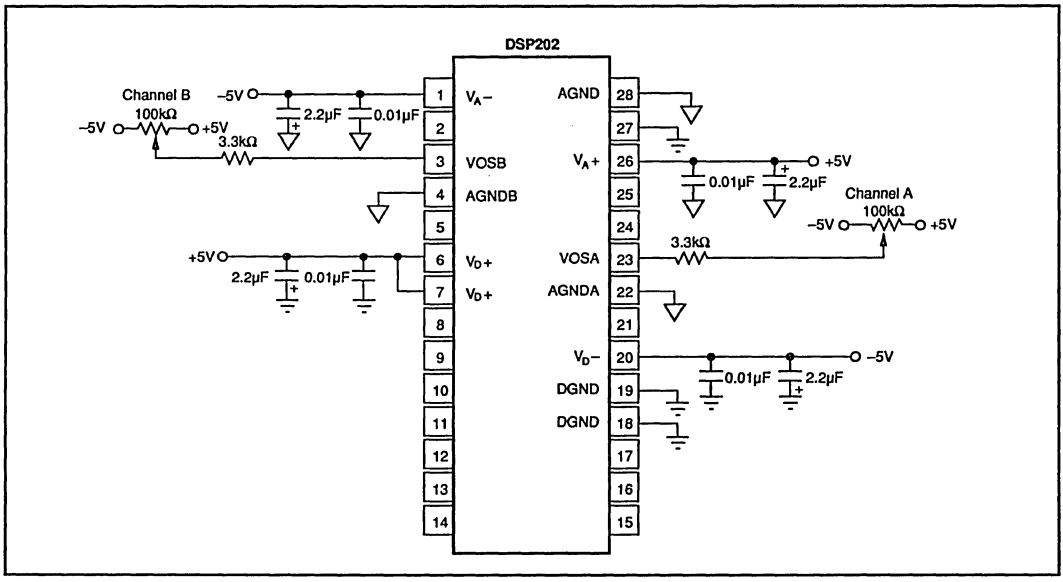


FIGURE 15. DSP202 Power Supply Connections and Optional Offset Voltage Adjustment.

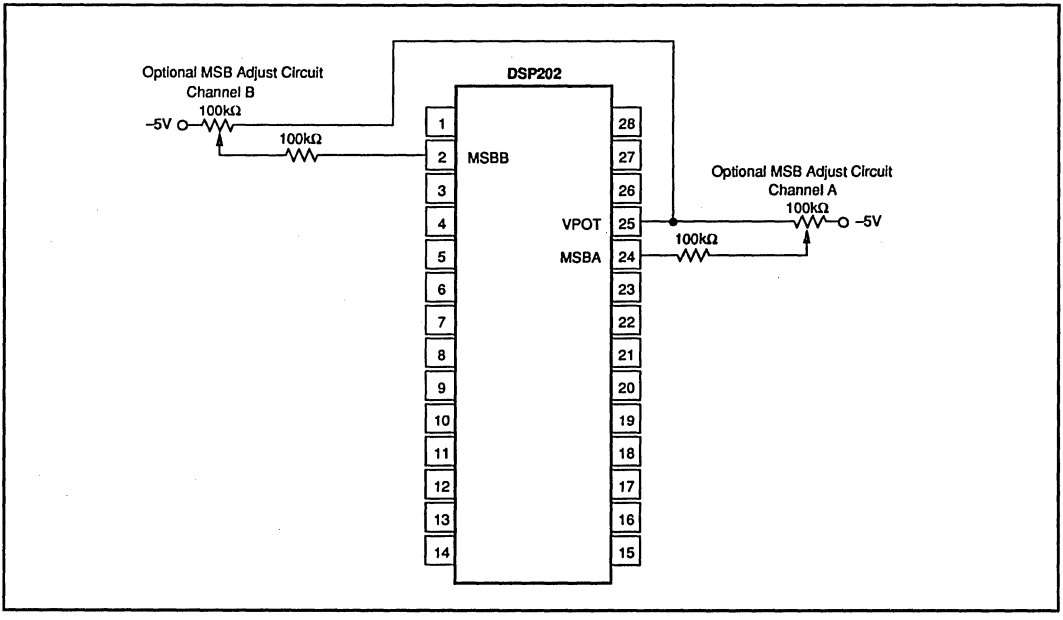


FIGURE 16. DSP202 Optional MSB Adjust Circuit.

BURR-BROWN®

DSP-SYS603
PC-Based Design/Test/ Evaluation System for the ADC603

BENEFITS/FEATURES

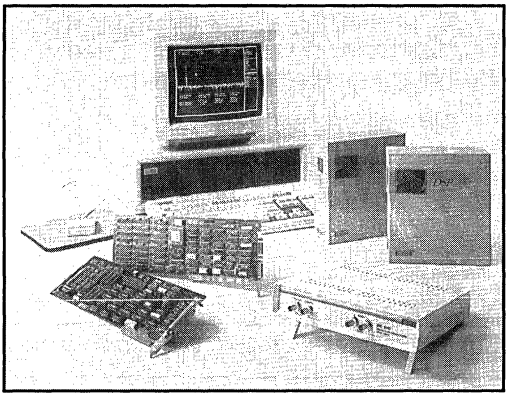
- COMPLETE SYSTEM "READY-TO-USE" WITH YOUR PC
- HIGH PERFORMANCE ADC603 ANALOG INPUTS (12-BIT ACCURACY 10MHz SAMPLING RATE)
- 64K WORD 10MHz DIGITAL BUFFER PC BOARD
- HIGH PERFORMANCE FLOATING POINT DSP PROCESSOR (AT&T WE® DSP32C)
- RUNS UNDER MS/DOS ON IBM® AT OR COMPATIBLE
- DSP DEVELOPMENT SOFTWARE INCLUDED (DSPLAY XL™)
- COMPLETE ADC TEST/EVALUATION SOFTWARE INCLUDED

APPLICATIONS

- DEVICE EVALUATION/CHARACTERIZATION
- SYSTEM DESIGN/DEVELOPMENT
- HIGH PERFORMANCE INSTRUMENTATION
- REAL-TIME SIGNAL PROCESSING ALGORITHM DEVELOPMENT
- MEDICAL IMAGING
- SONAR
- HIGH PERFORMANCE FFT SPECTRUM ANALYSIS
- HIGH SPEED DATA ACQUISITION
- ULTRASOUND SIGNAL PROCESSING
- I&Q PROCESSING
- ADC TESTING
- FATIGUE ANALYSIS
- NON-DESTRUCTIVE TESTING
- SCIENTIFIC RESEARCH

DESCRIPTION

The DSP-SYS603 Design System for the high performance ADC603 provides the user a ready-to-use solution for evaluation, test, and development purposes. As an evaluation tool,



the DSP-SYS603 can be used to analyze the performance of the ADC603 in specific applications. As a test instrument, it can be used to establish and measure specification profiles for certifying device system performance. As a development system, the DSP-SYS603 can receive direct analog signals and use them as inputs for the DSP processor.

Analog signals are converted at up to 10MHz with true 12-bit accuracy. The digital input is transferred to a DSP processor where, using DSPlay XL development software, signal processing algorithms may be easily designed and implemented.

Furthermore, using the Dynamic Signal Analysis software that is provided, the system may be used as a high performance digitizing scope, spectrum analyzer or histogram analyzer. Thus, the system can be used as a test instrument for assisting in the design of new products or the troubleshooting of circuitry. It may also be used as a receiving inspection station for testing hard-to-evaluate high performance analog-to-digital converters at time of receipt for manufacturing.

The DSP-SYS603 has two configuration options. Each system is made up of a combination of the following components best suited for specific applications:

- External Box with single or dual-channel ADC603 Converter(s)
- 64K Word Digital Input Buffer Board(s)
- AT&T DSP32C Processor Board with 576K SRAM
- DSPlay XL Real Time DSP Development Software
- Dynamic Signal Analysis Test Software

These system components are described below. More detailed descriptions can be provided upon request.

ANALOG SIGNAL INPUT BOX (ZPD1002)

The single or dual-channel external input box contains one or two ADC603s and drivers to provide high performance analog input into the system. The ADC603 is a 12-bit 10MHz sampling analog-to-digital converter.

COMPUTER PLATFORM

The system is designed to operate in an IBM PC/AT environment with an EGA or VGA monitor and Microsoft® Mouse. Although the standard system does not include the computer platform, a factory supplied computer (IBM AT-compatible) is available as an option. If the computer is purchased, all of the components are tested as a complete system, and shipped from the factory as a "ready-to-use" instrument. (Contact Customer Support at 1-800-548-6132 for price and delivery information for the complete system including the computer platform.)

DSP PROCESSOR BOARD (ZPB34-OO4)

The DSP processor board provided with the system (ZPB34-004) uses an AT&T DSP32C processor. This processor is capable of 25MFLOPS and is able to perform a 32-Bit multiply/accumulate instruction in 80ns. The board has 576KB of local SRAM and buffered high-speed (10MBits per second) serial I/O ports.

DIGITAL INPUT BUFFER (ZPB6064)

Due to the high speed sample rate of the ADC603, the system includes a digital input buffer board. This high speed card will capture, and subsequentially transfer, up to 65,536 words of data. Buffer size is set through the PC I/O port for 32 to 65,536 words with a word being 16 bits of digital information on either the ECL or TTL input signal at speeds from near DC to 10MHz.

Input data capture can be controlled by the Trigger function which can be either an external (ECL/TTL) signal or a PC I/O control byte. Post trigger data capture can be set for 1 to maximum buffer size minus one.

A second digital input buffer can be installed and slaved to the first card. The two boards can be triggered and clocked independently or simultaneously. When both buffers are full, the data can be serially transferred as 32-bit words (two concatenated 16-bit words). This feature can double the effective capture speed or allow two independent 16-bit input paths.

DYNAMIC SIGNAL ANALYSIS SOFTWARE (ZPA100)

At the heart of the system is the Dynamic Signal Analysis software which transforms the PC into a complete test and evaluation instrument, capable of analyzing data in time and frequency domain as well as producing linearity measurements. The software allows the PC to operate as any of three test instruments: digitizing scope, spectrum analyzer and histogram analyzer.

As a digitizing scope, the user may view, measure and analyze incoming data in the time domain.

Operating as a spectrum analyzer, FFTs are used for viewing, measuring or analyzing incoming data in the frequency domain. Direct readout of harmonic content, THD, SNR, THD + SNR, DC offset, and spurious-free dynamic range is possible through spectrum analysis.

Functioning as an histogram analyzer, the user may display histograms, differential non-linearity (DNL), and integral non-linearity (INL). For convenience, the software is completely mouse-driven allowing the user to zoom, pan, move markers, use display lines, or change parameters with simple mouse movements. Setup save and load features are also included.

DSP DEVELOPMENT SOFTWARE (ZPM32)

A second integral piece of software provided for real-time development is DSPlay XL. Supplied with over 100 block functions, DSPlay XL uses Flowgrams™ (block diagrams of an application) to develop algorithms which are executed on the system's DSP processor. Once designed and verified, the executable code can be saved and ported to any DSP system using the AT&T DSP32 or DSP32C processors.

HIGH PERFORMANCE WORKSTATION CONFIGURATIONS

As an integrated system, the state-of-the-art development and evaluation tools described above form a user-friendly, yet extremely powerful, workstation environment for real-time DSP applications. Since the applications for DSP are varied, two configurations for the high performance development system are offered.

Single Channel Analog Input System (DSP-SYS603-001)

Description

The DSP-SYS603-001 is the basic system for acquiring and working with single input analog signals at the 12-bit 10MHz sampling rate of the ADC603. For applications where it is necessary to evaluate the incorporation of an ADC603 into a current design or design under development, the -001 system allows the user to analyze the effects of the high performance of the ADC603. Furthermore, this analysis can be accomplished with little more effort than making the appropriate connections and establishing the proper system setup.

In addition to design support, the DSP-SYS603 may be used as the test software to characterize the performance of the user's system. A third application for the workstation is to take advantage of the development software in order to design DSP circuits that will enhance the performance of the user's system. DSP-SYS603 software will allow the user to not only develop the DSP algorithms, but will port the executable code to any DSP32C processors for continued use within the user's system.

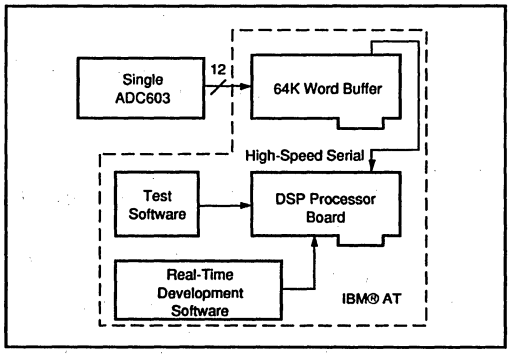


FIGURE 1. Single Channel Analog Input System.

Dual Channel Analog Input System (DSP-SYS603-002)

Description

The -002 system configuration is designed for applications where simultaneous sampling is required. Included in this system is an analog input box with dual ADC603s along with two digital input buffer boards. As a dual input system configuration, independent high resolution samples can be taken simultaneously, then passed to the respective buffer board, where the two inputs are concatenated to form one 32-bit word for transfer to the DSP board for analysis and processing.

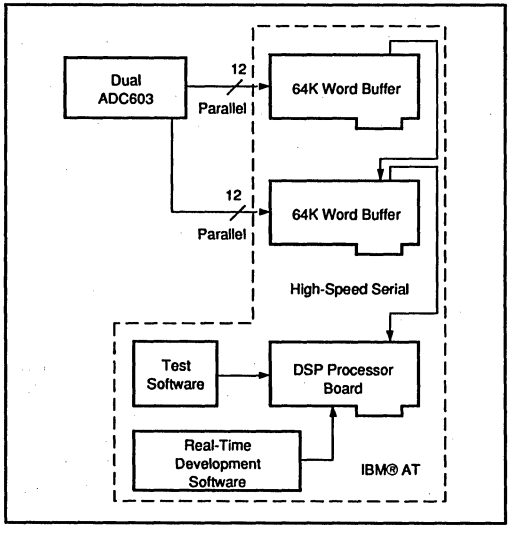


FIGURE 2. Dual Channel Analog Input System.

Digital Input Buffer

Sample Rate: ..... 10MHz max (externally supplied)
Data Format Out: ..... Buffered Differential line drivers
Base I/O Address: ..... I/O Port Address 0X0-0X3FF
I/O Mapped 4 Ports

DSP Processor Board

Memory: ..... 64KB 0 Wait State
512KB 1 Wait State
Clock Rate: 49.152MHz
Addressing: ..... I/O Port Address 0X0-0X3FF
I/O Mapped 16 Ports
Interrupts: ..... Selectable IRQ3-7,9-12,14,15
Serial I/O: ..... Buffered Differential Line Drivers and Receivers Terminated in 100Ω
Serial I/O- Internal: 6.1MBits/s

DSP Development Software

Over 100 DSP and related block functions in the following categories:

Arithmetic	Non_linear
Data	O_scope
Filter	Spectrum
Generator	Trigonometric
Input_Output	Window
fiLe	Measure
suBgram	

Execution times for several common functions:
1024 Point Complex FFT ..3.8ms
128 Tap FIR Filter .....80ns x 128
Second Order IIR Section ..80ns x 5

Dynamic Signal Analysis Software

Software performs instrumentation functions for:
Digitizing Scope
Spectrum Analyzer
Histogram Analyzer

Configuration

Hardware Requirements;
- IBM AT Compatible
- 640K memory
- Math Co-processor
- Mass Storage — Hard disk and one floppy drive
- Monitor — EGA or VGA
- Printer (optional) — IBM graphics printer, HP Laser jet printer or compatibles

Software Requirements

PC/MS-DOS Versions 3.0 or higher

SUPPLIED ACCESSORIES

Power Supply for the Analog Input Box
Power Connectors
Connection Cables
DSP Development Software Manual
Dynamic Signal Analysis Software Manual
DSP-SYS701 User's Manual

SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
INPUTS					
Analog					
Input Range		–1.25		+1.25	V
Input Impedance			50		Ω
Digital					
Logic Family	TTL				
Convert Command	Positive Edge				
Pulse Width		10		t-20	ns
Trigger	Positive Edge				
Pulse Width		20			ns
TRANSFER CHARACTERISTICS					
Accuracy					
Gain Error	f = 200Hz		±0.1	±1	%FSR
Conversion Characteristics					
Sample Rate		DC		10	MHz
Dynamic Characteristics					
Signal-to-Noise Ratio (SNR)	f = 100kHz				
	f_s = 9.99MHz	66	70.1		dB
OUTPUTS					
Logic Family - Differential ECL					
Logic coding - Two's Complement					
Logic Levels -	Logic "LO"	–1.95		–1.63	V
	Logic "HI"	–0.98		–0.81	V
Data Valid Pulse Width		20	45	60	ns

OPTIONAL CONFIGURED HARDWARE SYSTEM, INCLUDES HIGH PERFORMANCE 386PC

Burr-Brown will provide, as an option, an entire test/evaluation system including the required configuration hardware and software. With the purchase of this option, the system is configured and tested prior to shipment. Thus, the customer will receive a complete turn-key test/evaluation system for the ADC603.

The configuration hardware will be a high performance, 386 computer (without printer). For details of the exact computer specifications to be used at the time of shipment, contact your sales representative.

ORDERING INFORMATION

To order, please specify:

DSP-SYS603-001 .....Single Channel Analog Input System

DSP-SYS603-002 .....Dual Channel Analog Input System with Digital Input Buffers

DSP-SYS603-XXXA.....Analog Input System including Configured Hardware System

FOR MORE INFORMATION

For more information contact Applications Engineering at 1-800-548-6132.

FlowGram™ Burr-Brown Corp.
DSPlay XL™ Burr-Brown Corp.
Microsoft® Microsoft Corp.
WE® DSP32C AT&T Corp.
IBM® PC IBM Corp.

BURR-BROWN®

DSP-SYS701
PC-Based Design/Test/ Evaluation System for the ADC701

BENEFITS/FEATURES

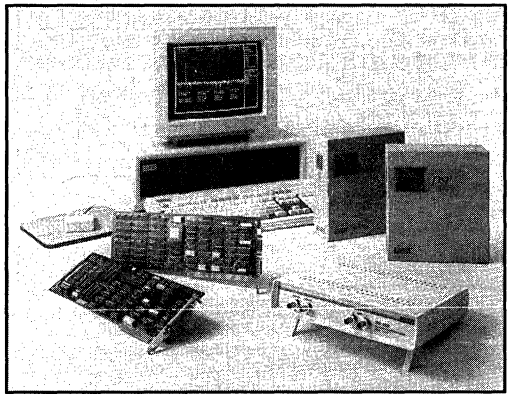
- COMPLETE SYSTEM "READY-TO-USE" WITH YOUR PC
- HIGH PERFORMANCE ADC701 ANALOG INPUTS (16-BIT ACCURACY 500kHz SAMPLING RATE)
- 64K WORD 10MHz DIGITAL BUFFER BOARD FOR THE PC
- HIGH PERFORMANCE FLOATING POINT DSP PROCESSOR (AT&T WE® DSP32C) FOR THE PC
- RUNS UNDER MS/DOS ON IBM® AT OR COMPATIBLE
- DSP DEVELOPMENT SOFTWARE INCLUDED (DSPLAY XL™)
- COMPLETE ADC TEST/EVALUATION SOFTWARE INCLUDED

APPLICATIONS

- ADC701 EVALUATION/CHARACTERIZATION
- SYSTEM DESIGN/DEVELOPMENT
- HIGH PERFORMANCE INSTRUMENTATION
- REAL-TIME SIGNAL PROCESSING ALGORITHM DEVELOPMENT
- MEDICAL IMAGING
- SONAR
- HIGH PERFORMANCE FFT SPECTRUM ANALYSIS
- HIGH SPEED DATA ACQUISITION
- ULTRASOUND SIGNAL PROCESSING
- I&Q PROCESSING
- ADC TESTING
- FATIGUE ANALYSIS
- NON-DESTRUCTIVE TESTING
- SCIENTIFIC RESEARCH

DESCRIPTION

The DSP-SYS701 Design System for the high performance ADC701 provides the user a ready-to-use solution for evaluation, test, and development purposes. As an evaluation tool, the DSP-SYS701 can be used to analyze the performance of the ADC701 in specific applications. As a test instrument, it can be used to establish and measure specification profiles for certifying device system performance. As a development system, the DSP-SYS701 can receive direct analog signals and use them as inputs for the DSP processor.



Analog signals are converted at up to 500kHz with true 16-bit accuracy. The digital input is transferred in real time to a DSP processor where, using DSPlay XL development software, signal processing algorithms may be easily designed and implemented.

Furthermore, using the Dynamic Signal Analysis software that is provided, the system may be used as a high performance digitizing scope, spectrum analyzer or histogram analyzer. Thus, the system can be used as a test instrument for assisting in the design of new products or the troubleshooting of circuitry. It may also be used as a receiving inspection station for testing hard-to-evaluate high performance analog-to-digital converters at time of receipt for manufacturing.

The DSP-SYS701 has three configuration options. Each system is made up of a combination of the following components best suited for specific applications:

- External Box(es) with ADC701 Converter
- 64K Word Digital Input Buffer Board(s)
- AT&T DSP32C Processor Board with 576K SRAM
- DSPlay XL Real Time DSP Development Software
- Dynamic Signal Analysis Test Software

PDS-1012

These system components are described below. More detailed descriptions can be provided upon request.

ANALOG SIGNAL INPUT BOX (ZPD1003)

This external input box contains an ADC701 and the necessary clock and drivers to provide high performance analog input. The ADC701 is a 16-bit 500kHz analog-to-digital converter. Included in the box is a companion sample/hold amplifier that provides outstanding dynamic performance.

COMPUTER PLATFORM

The system is designed to operate in an IBM PC/AT environment with an EGA or VGA monitor and Microsoft® Mouse. Although the standard system does not include the computer platform, a factory supplied computer (IBM AT-compatible) is available as an option. If the computer is purchased, all of the components are tested as a complete system, and shipped from the factory as a "ready-to-use" instrument. (Contact Customer Support at 1-800-548-6132 for price and delivery information for the complete system including the computer platform)

DSP PROCESSOR BOARD (ZPB34-004)

The DSP processor board provided with the system uses an AT&T DSP32C processor. This processor is capable of 25MFLOPS and is able to perform a 32-bit multiply/accumulate instruction in 80ns. The board has 576KB of local RAM and buffered high-speed (10MBits per second) serial I/O ports.

DIGITAL INPUT BUFFER (ZPB6064)

In the event that an application may require that the data be buffered, two configurations of the system include a digital input buffer board. This high speed card will capture, and subsequentially transfer, up to 65,536 words of data. Buffer size is set through the PC I/O port for 32 to 65,536 words with a word being 16 bits of digital information on either the ECL or TTL input signal at speeds from near DC to 10MHz.

Input data capture can be controlled by the Trigger function which can be either an external (ECL/TTL) signal or a PC I/O control byte. Post trigger data capture can be set for 1 to maximum buffer size minus one.

A second digital input buffer can be installed and slaved to the first card. The two boards can be triggered and clocked independently or simultaneously. When both buffers are full, the data can be serially transferred as 32-bit words (two concatenated 16-bit words). This feature can double the effective capture speed or allow two independent 16-bit input paths.

DYNAMIC SIGNAL ANALYSIS SOFTWARE

At the heart of the system is the Dynamic Signal Analysis software which transforms the PC into a complete test and evaluation instrument, capable of analyzing data in time and frequency domain as well as producing linearity measurements. The software allows the PC to operate as any of three test instruments: digitizing scope, spectrum analyzer and histogram analyzer.

As a digitizing scope, the user may view, measure and analyze incoming data in the time domain.

Operating as a spectrum analyzer, FFTs are used for viewing, measuring or analyzing incoming data in the frequency domain. Direct readout of harmonic content, THD, SNR, THD + SNR, DC offset and spurious-free dynamic range is possible.

Functioning as an histogram analyzer, the user may display histograms, dynamic linearity (DNL), and integral linearity (INL). For convenience, the software is completely mouse-driven, allowing the user to zoom, pan, move markers, use display lines, or change parameters with simple mouse movements. Setup save and load features are also included.

DSP DEVELOPMENT SOFTWARE (ZPM32)

A second integral piece of software provided for real-time development is DSPlay XL. Supplied with over 100 block functions, DSPlay XL uses Flowgrams™ (block diagrams of an application) to develop algorithms which are executed on the system's DSP processor. Once designed and verified, the executable code can be saved and ported to any DSP system using the AT&T DSP32 or DSP32C processors.

HIGH PERFORMANCE WORKSTATION CONFIGURATIONS

As an integrated system, the state-of-the-art development and evaluation tools described above form a user-friendly, yet extremely powerful, workstation environment for real-time DSP applications. Since the applications for DSP are varied, three configurations for the high performance development system are offered.

Single Channel Analog Input System (DSP-SYS701-001)

Description

The DSP-SYS701-001 is the basic system for acquiring and working with single input analog signals at the 16-bit 500kHz sampling rate of the ADC701. For applications where it is necessary to evaluate the incorporation of an ADC701 into a current design or design under development, the -001 system allows the user to analyze the effects of the high performance of the ADC701. Furthermore, this analysis can be accomplished with little more effort than making the appropriate connections and establishing the proper system setup.

In addition to design support, the DSP-SYS701 may be used as the test software to characterize the performance of the user's system. A third application for the workstation is to take advantage of the development software in order to design DSP circuits that will enhance the performance of the user's system. DSP-SYS701 software will allow the user to not only develop the DSP algorithms, but will port the executable code to any DSP32 or 32C processors for continued use in the user's system.

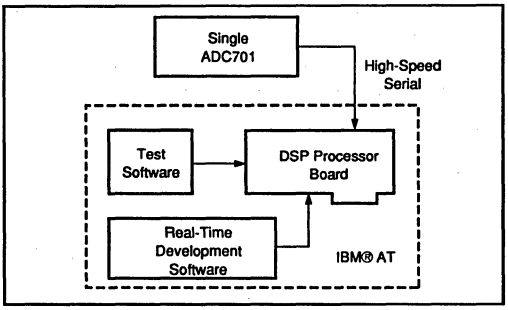


FIGURE 1. Single Channel Analog Input System.

Single Channel Analog Input System With Digital Input Buffer (DSP-SYS701-002)

Description

In certain applications that entail complicated post-processing, there may be a need for the capture of larger buffers. Simply stated, larger amounts of data can be captured in real-time, and stored, for post collection analysis. This configuration is designed for pre-trigger data analysis, such as that required in material testing, fatigue analysis, and scientific research.

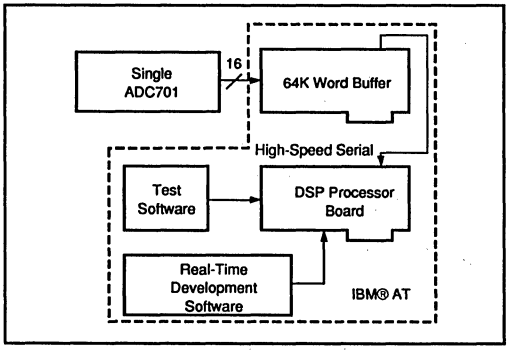


FIGURE 2. Single Channel Analog Input System with Digital Input Buffer.

Dual Channel Analog Input System (DSP-SYS701-003)

Description

The -003 system configuration is designed for applications where simultaneous sampling is required. Included in this system are two analog input boxes along with two digital input buffer boards. As a dual input system configuration, independent high resolution samples can be taken simultaneously, then passed to the respective buffer board, where the two inputs are concatenated to form one 32-bit word for transfer to the DSP board for analysis and processing.

Digital Input Buffer

Sample Rate: ..... 10MHz max (externally adjustable)

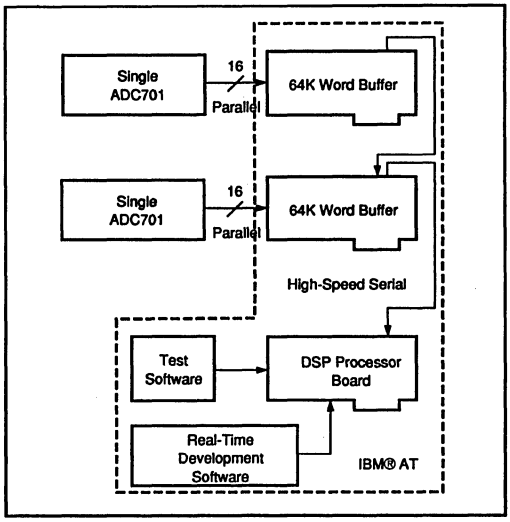


FIGURE 3. Dual Channel Analog Input System.

Data Format Out: ..... Differential line drivers, WE AT&T DSP32 serial format
Base I/O Address: ..... 4 locations 0x0 - 0x3FF

DSP Processor Board

Memory: ..... 64KB 0 Wait State
512K 1 Wait State
Clock Rate: 49.152MHz
Addressing: ..... I/O Mapped 16 Ports
Interrupts: ..... Selectable IRQ3-7,9-12,14,15
Serial I/O: ..... Buffered Differential Line Drivers and Receivers Terminated in 100Ω
Serial I/O- Internal: 6.1MBits/s

DSP Development Software

Over 100 functions in the following categories:

Arithmetic	suBgram
Data	Non-linear
Filter	O_scope
Generator	Spectrum
Input_Output	Trigonometric
fiLe	Window
Measure	

Execution times for several common functions:
1024 Point Complex FFT 3.8ns
128 Tap FIR Filter ..... 80ns x 128taps
Second Order IIR Section ..... 80ns x 5

Dynamic Signal Analysis Software

Software performs instrumentation functions for:
- Digitizing Scope
- Spectrum Analyzer
- Histogram Analyzer

Configuration

Hardware Requirements:
- IBM AT Compatible
- 640K memory

SPECIFICATIONS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS					
Sample Rate	Unadjusted	DC		500	kHz
Dynamic Nonlinearity			±0.002		%FSR
Total Harmonic Distortion (THD)	f_{IN} = 20kHz(–0.3dB)		0.00068		%
	f_{IN} = 199kHz(–0.2dB)		0.0078		%
Spurious-Free Dynamic Range	f_{IN} = 20kHz(–0.3dB)		107.1		dB
	f_{IN} = 199kHz(–12dB)		93.8		dB
Two-Tone Intermodulation Distortion	f_1 = 195kHz(–6.5dB)		–81.4		dBc
	f_2 = 200kHz(–6.5dB)				
	f_1 = 195kHz(–12.5dB)		–86.2		dBc
	f_2 = 200kHz(–12.5dB)				
Signal-to-Noise-Ratio (SNR)	f_{IN} = 5kHz (–0.5dB)		93		dB
INPUTS					
Analog					
Input Range	Jumper Selectable	0		10	V
		–10		10	V
		–5		5	V
		–10		0	V
		0		5	V
	Input Impedance			600	Ω
Digital					
Logic Family	TTL				
Convert Command	Positive Edge				
Pulse Width		50		t – 50	ns

Math Co-processor
Mass Storage — Hard disk and one floppy drive
Monitor — EGA or VGA
Printer (Optional) — IBM graphics printer, HP Laser jet printer or compatibles

Software Requirement
PC/MS-DOS Version 3.0 or higher.

Optional (Configured Hardware System), Includes High Performance 386 PC

Burr-Brown will provide, as an option, an entire test/evaluation system including the required configuration hardware and software. With the purchase of this option, the system is configured and tested prior to shipment. Thus, the customer will receive a complete turnkey test/evaluation system for the ADC701.

The configuration hardware will be a high performance, 386 computer (without printer). For details of the exact computer specifications to be used at the time of shipment, contact your sales representative.

SUPPLIED ACCESSORIES

Power Supply for the Analog Input Box
Power connectors
Connection Cables
DSP Development Software Manual
Dynamic Signal Analysis Software Manual
DSP-SYS701 User's Manual

ORDERING INFORMATION

To order, please specify:	
DSP-SYS701-001	Single Channel Analog Input System
DSP-SYS701-002	Single Channel Analog Input System with Digital Input Buffer
DSP-SYS701-003	Dual Channel Analog Input System with Digital Input Buffers
DSP-SYS701-XXXA	Analog Input System Including Configured Hardware System

FOR MORE INFORMATION

For more information contact Applications Engineering at 1-800-548-6132.

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DSPlay XL™ Burr-Brown Corp.
DSPeed™ Burr-Brown Corp.
WE® DSP32C AT&T Corp.
IBM® PC IBM Corp.

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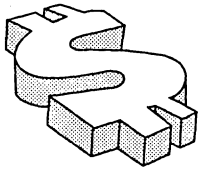
For Immediate Assistance, Contact Your Local Salesperson



USA PRICE LIST

ABOUT THIS SECTION

Prices listed here are effective until March 31, 1989 and unless otherwise noted apply only to domestic U.S.A. customers. All other customers should contact their local Burr-Brown salesperson or representative.

For U.S.A. customers all prices are FOB Tucson, Arizona. Applicable federal, state, and local taxes are extra. Terms are net 30 days. Prices and specifications are subject to change without notice.

Some of the models in this price list are not included in this book but are still available. For more information about them, contact your local Burr-Brown salesperson or representative.

QUOTATIONS

Price quotations made by Burr-Brown or its authorized field sales representatives are valid for 30 days. Delivery quotations are subject to reconfirmation at the time of order placement.

SALES & SERVICE

Burr-Brown also offers free technical assistance and literature, convenient methods for placing an order, and warranty service. Complete information can be found on page *xi* of this book.

MODEL	1-24	25-99	100
0100MS	17.15	14.30	11.35
0546	137.00	130.00	124.00
0700	63.00	61.00	59.00
M	68.00	66.00	64.00
U	58.00	56.00	54.00
UM	79.00	77.00	75.00
0722	60.65	45.80	39.55
BG	77.40	59.70	51.40
MG	69.70	52.85	44.45
0724	84.55	63.85	55.65
0729MC	102.00	102.00	102.00
2H946	3305.00	2809.00	2528.00
-1	2114.00	2000.00	1760.00
3507J	14.50	11.40	9.35
JQ	22.45	17.40	14.95
3527AM	20.25	15.00	12.35
BM	26.10	19.05	16.45
BMQ	34.60	27.50	23.30
CM	41.35	31.55	26.20
3528AM	25.25	18.70	14.60
BM	30.95	22.85	19.75
BMQ	42.70	32.40	28.60
CM	37.70	28.50	24.65
3550J	39.65	30.05	24.35
K	50.50	37.55	28.95
S	73.40	56.30	40.55
SQ	102.85	82.00	62.45
3551J	40.40	30.35	24.35
S	71.35	55.60	40.55
SQ	92.30	76.30	60.00
3553AM	45.75	34.75	25.50
AMQ	75.15	63.60	53.85
3554AM	85.85	70.70	58.15
AMQ	115.85	97.25	81.40
BM	98.05	82.15	66.30
BMQ	132.00	112.95	92.95
SM	115.55	95.70	79.55
SMQ	161.70	136.60	115.85
3571AM	85.20	61.25	49.00
3572AM	97.60	72.60	58.10
3573AM	42.70	29.75	26.80
3580J	69.65	51.40	43.10
JQ	103.80	79.55	66.85
3581J	105.00	75.55	64.10
3582J	114.05	82.70	74.60
JQ	157.30	136.15	117.85
3583AM	112.35	91.95	73.55
AMQ	163.25	135.05	116.70
JM	103.70	86.55	68.30
3584JM	106.00	78.40	68.80
JMQ	150.45	124.70	111.05
3606AG	133.40	114.20	99.70
BG	174.05	152.05	130.45
3627AM	15.90	11.85	10.50
AMQ	32.95	20.70	16.65
BM	21.25	15.15	12.90
BMQ	42.85	25.40	20.70
3650HG	71.45	51.45	37.95
JG	92.90	66.30	52.55
KG	112.95	90.60	73.10
MG	64.00	44.00	36.00
3652HG	92.90	68.95	52.55
JG	112.95	83.75	71.95
MG	72.70	56.80	48.15
3656AG	109.70	82.95	65.10
BG	135.65	102.60	87.55
HG	96.90	73.30	57.40
JG	103.30	78.10	61.30
KG	127.00	96.10	75.30
4127JG	65.10	47.80	39.80
KG	74.95	60.00	50.80
4204J	88.85	74.10	60.10
K	115.90	98.30	76.00
S	131.90	116.10	96.60
SQ	181.60	168.60	147.40
4206J	63.30	49.35	35.65
K	89.85	70.00	49.80
4213AM	35.35	27.15	21.25
BM	51.10	38.70	31.80
SM	66.15	54.30	42.45
UM	32.55	27.30	24.15
UM/883B	45.15	38.85	30.45

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MODEL	1-24	25-99	100
4213VM	47.25	40.95	32.55
VM/883B	63.50	39.90	36.75
WM	63.00	63.00	51.45
WM/883B	78.75	65.10	50.40
4214AP	32.05	25.55	19.25
BP	47.60	37.50	30.95
4302	68.65	49.05	37.20
4340	127.00	91.45	77.85
4341	38.10	29.70	20.75
4423	31.60	24.10	19.30
5962-88563013X	167.15	126.25	106.05
-8856301JX	119.70	89.90	75.75
AD515JH	27.55	19.75	12.75
KH	39.75	30.15	19.90
LH	50.35	36.15	23.95
AD532SD/883B	84.75	70.65	58.85
H/883B	68.40	57.00	47.50
AD534SD/883B	105.40	87.85	73.20
SH/883B	93.85	78.20	65.15
TD/883B	133.45	111.20	92.65
TH/883B	117.75	98.10	81.75
AD632AD	28.35	25.30	16.50
AH	19.95	17.80	11.65
BD	50.35	37.00	22.75
BH	38.05	28.05	18.85
SD	63.05	44.20	30.10
SD/883B	61.20	51.00	42.50
SH	47.15	37.45	25.50
SH/883B	54.60	45.50	37.90
TD	70.65	49.50	34.95
TD/883B	67.25	56.06	46.70
TH	52.95	42.05	29.60
TH/883B	57.25	47.70	39.75
ADC574AJH	35.20	27.40	22.20
AJH-BI	44.00	34.30	27.70
AJP	29.00	22.60	18.30
AJP-BI	33.40	28.30	22.80
AKH	46.10	36.00	29.00
AKH-BI	57.60	45.00	36.30
AKP	38.00	29.60	24.00
AKP-BI	43.70	37.00	29.90
ASH	94.40	78.40	68.00
ASH-BI	118.00	98.00	85.00
ATH	130.30	108.10	93.80
TH-BI	162.80	135.20	117.20

MODEL	1-24	25-99	100
ADC574KD			20.20
ADC600B	2560.00	2423.00	2132.00
K	1975.00	1728.00	1524.00
ADC601JG	124.00	98.00	86.00
KG	159.00	127.00	111.00
ADC603JH	710.00	645.00	590.00
KH	1099.00	1014.00	941.00
RH			
SH			
SH/MIL			
ADC604JH	1349.00	1226.00	1121.00
KH	2088.00	1865.00	1788.00
ADC674AJH	44.80	35.00	28.20
AJH-BI	56.00	43.70	35.30
AJP	37.20	29.00	23.40
AJP-BI	42.80	36.20	29.30
AKH	58.40	45.60	36.80
AKH-BI	73.00	57.00	46.00
AKP	48.80	38.10	30.80
AKP-BI	56.10	47.60	38.40
ASH	121.60	100.90	87.60
ASH-BI	152.00	126.20	109.40
ATH	166.40	138.10	119.80
ATH-BI	208.00	172.60	149.80
KD			25.25
ADC700AH	148.00	135.40	103.90
BH	178.00	162.80	124.90
JH	106.00	95.00	74.00
KH	127.00	114.00	89.00
RH	212.00	193.90	148.80
SH	255.00	233.30	179.00
ADC701JH	675.00	622.00	563.00
KH	783.00	722.00	653.00
ADC71AG	207.05	182.93	147.33
BG	235.10	207.05	168.65
JG	84.00	71.40	53.40
KG	106.10	90.80	67.70
ADC76AG	206.30	188.10	142.50
BG	237.90	213.90	173.00
JG	137.50	125.40	95.00
KG	158.60	142.60	115.30
ADC774JH	69.00	54.50	48.30
JH-BI	79.40	62.70	55.50
JP	55.20	43.60	38.60
JP-BI	61.90	50.20	44.40
KH	89.00	70.30	62.30

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MODEL	1-24	25-99	100
ADC774KH-BI	102.30	80.80	71.60
KP	71.20	56.20	49.80
KP-BI	79.80	64.60	57.30
SH	195.00	154.00	136.50
SH-BI	224.20	177.10	157.00
TH	265.00	209.35	185.50
TH-BI	304.80	240.80	213.30
ADC7802BN	36.70	28.70	22.95
BP	31.90	24.95	19.95
ADC803BM	255.78	219.40	203.00
BMQ	355.00	319.00	303.00
CM	297.00	249.00	235.00
CMQ	397.00	349.00	320.00
SM	389.00	327.00	290.00
SMQ	512.00	406.00	370.00
ADC804BH	67.47	48.20	41.77
BH-BI	76.10	54.30	47.10
BHQ	104.96	73.90	58.91
SH	127.45	88.89	70.69
SH-BI	143.70	100.20	79.70
SHQ	159.58	111.38	88.89
ADC80AG-10	86.70	76.50	48.96
AG-12	91.80	80.58	50.49
AG-12-BI	99.00	86.90	54.45
AGZ-12	91.80	80.58	50.49
H-AH-12	96.90	80.58	50.49
H-AH-12Q	125.97	105.57	66.15
KD			29.50
MAH-12	51.50	41.60	34.70
MAH-12-BI	59.20	47.80	39.90
ADC82AG	80.33	55.69	47.12
ADC84KG-10	88.23	78.54	63.19
KG-12	93.33	81.60	66.40
KG-12-BI	105.20	92.00	74.90
ADC85H-12	98.94	85.17	75.48
H-12-BI	111.50	96.00	85.10
ADC87	123.75	106.10	97.75
/883B	137.20	119.50	111.20
H-12	104.55	90.78	84.66
V	123.75	106.10	97.75
V/883B	135.20	117.50	109.20
ADS602JG	237.00	188.00	165.00
KG	294.00	234.00	205.00
ADS7800AH	49.85	38.90	31.15
BH	68.95	53.90	43.10
JD			22.75

MODEL	1-24	25-99	100
ADS7800JP	38.30	29.95	23.95
JU	42.15	32.95	26.35
KP	53.70	41.95	33.55
KU	57.55	44.95	35.95
ADS807JH	79.00	64.00	56.00
JH-BI	90.85	73.60	64.40
KH	102.00	81.00	72.00
KH-BI	117.30	93.15	82.80
RH	225.00	179.00	157.00
RH-BI	258.75	205.85	180.55
SH	305.00	241.00	213.00
SH-BI	350.75	277.15	244.95
ADS808JH	79.00	64.00	56.00
JH-BI	90.85	73.60	64.40
KH	102.00	81.00	72.00
KH-BI	117.30	93.15	82.80
RH	225.00	179.00	157.00
RH-BI	258.75	205.85	180.55
SH	305.00	241.00	213.00
SH-BI	350.75	277.15	244.95
BCS200-CTM	395.00	365.00	355.00
BCS220-CTM	425.00	395.00	385.00
BCS221-CTM	425.00	395.00	385.00
BCW210-CTM	225.00	200.00	195.00
BCW220-CTM	225.00	200.00	195.00
BCW221-CTM	225.00	200.00	195.00
BCW222-CTM	225.00	200.00	195.00
BOOK-1	63.05	61.90	60.70
-2	51.95	50.95	50.00
-3	45.60	44.70	43.85
-4	50.35	49.40	48.45
CMP100AP	29.00	26.10	23.20
AU	30.45	27.40	24.35
CTM150B-X	195.00	165.00	135.00
G-X	195.00	165.00	135.00
CTM170B-X	210.00	180.00	150.00
G-X	210.00	180.00	150.00
CTM200B-XY	235.00	195.00	165.00
G-XY	235.00	195.00	165.00
CTM220B-XY	235.00	195.00	165.00
G-XY	235.00	195.00	165.00

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MODEL	1-24	25-99	100
CTM250B-XY	295.00	245.00	195.00
G-XY	295.00	245.00	195.00
CTM270B-XY	295.00	245.00	195.00
G-XY	295.00	245.00	195.00
DAC1201KP-V	11.42	11.42	7.09
DAC1600JP-V	15.40	14.64	9.13
KP-V	17.85	17.03	10.61
DAC63BG	117.30	95.88	88.74
BM	117.30	95.88	88.74
CG	140.30	111.38	103.89
CM	163.86	133.88	119.95
DAC700BH	66.56	52.28	43.86
BH-BI	71.80	56.40	47.30
BH/QM	80.99	61.15	52.02
CH	100.78	85.68	72.32
CH-BI	108.70	92.40	78.00
KH	52.53	40.09	32.90
KH-BI	56.70	43.20	35.50
LH	81.60	69.67	58.96
LH-BI	88.00	75.10	63.60
SH	100.83	76.76	62.93
SH-BI	108.70	82.80	67.90
SH/883B	126.00	95.15	78.90
DAC701BH	66.56	52.28	43.86
BH-BI	71.80	56.40	47.30
BH/QM	80.99	61.15	52.02
CH	100.78	85.68	72.32
CH-BI	108.70	92.40	78.00
KH	52.53	40.09	32.90
KH-BI	56.70	43.20	35.50
LH	81.60	69.67	58.96
LH-BI	88.00	75.10	63.60
SH	100.83	76.76	62.93
SH-BI	108.70	82.80	67.90
SH/883B	126.00	95.15	78.90
DAC702BH	66.56	52.28	43.86
BH-BI	71.80	56.40	47.30
BH/QM	80.99	61.15	52.02
CH	100.78	85.68	72.32
CH-BI	108.70	92.40	78.00
JP	25.91	21.93	19.07
JP-BI	27.90	23.70	20.60
KH	52.53	40.09	32.90
KH-BI	56.70	43.20	35.50
KP	29.07	24.63	21.22
KP-BI	31.40	26.60	22.90
LH	81.60	69.67	58.96
LH-BI	88.00	75.10	63.60
SH	100.83	76.76	62.93

MODEL	1-24	25-99	100
DAC702SH-BI	108.70	82.80	67.90
SH/883B	126.00	95.15	78.90
DAC703AD			18.37
BH	66.56	52.28	43.86
BH-BI	71.80	56.40	47.30
BH/QM	80.99	61.15	52.02
CH	100.78	85.68	72.32
CH-BI	108.70	92.40	78.00
JP	25.91	21.93	19.07
JP-BI	27.90	23.70	20.60
JU	29.00	25.00	21.50
KH	52.53	40.09	32.90
KH-BI	56.70	43.20	35.50
KP	29.07	24.63	21.22
KP-BI	31.40	26.60	22.90
KU	33.00	28.00	24.00
LH	81.60	69.67	58.96
LH-BI	88.00	75.10	63.60
MD-B			33.95
SD			28.85
SH	100.83	76.76	62.93
SH-BI	108.70	82.80	67.90
VG	103.00	77.75	65.15
VG/883B	119.70	89.90	75.75
VL	144.95	109.10	90.90
VL/883B	167.15	126.25	106.05
DAC707BH	72.50	68.50	56.30
BH-BI	79.70	75.30	61.90
BH/QM	85.70	80.60	63.30
JP	28.70	24.30	20.95
JP-BI	31.60	26.70	23.00
KH	62.60	50.60	43.70
KH-BI	68.90	55.60	48.10
KP	31.80	27.05	23.05
KP-BI	35.00	29.80	25.40
SH	93.90	85.90	72.70
SH-BI	103.30	94.50	80.00
DAC708BH	70.80	67.00	52.40
BH-BI	78.00	73.70	57.60
BH/QM	83.80	78.80	61.90
KH	57.00	46.10	39.80
KH-BI	62.70	50.70	43.80
SH	90.70	83.00	70.20
SH-BI	99.80	91.30	77.30
DAC709BH	70.80	67.00	52.40
BH-BI	78.00	73.70	57.60
BH/QM	83.80	78.80	61.90
KH	57.00	46.10	39.80
KH-BI	62.70	50.70	43.80
SH	90.70	83.00	70.20
SH-BI	99.80	91.30	77.30

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MODEL	1-24	25-99	100
DAC70BH-COB-I	160.85	121.48	101.18
BH-COB-IBI	173.50	131.00	109.10
BH-CSB-I	160.85	121.48	101.18
BH-CSB-IBI	173.50	131.00	109.10
DAC71-CCD-V	76.50	65.26	57.19
-COB-I	57.99	49.47	43.35
-COB-I-BI	62.50	53.40	46.80
-COB-V	59.16	53.04	46.92
-COB-V-BI	63.80	57.20	50.60
-CSB-I	57.99	49.47	43.35
-CSB-I-BI	62.50	53.40	46.80
-CSB-V	59.16	53.04	46.92
-CSB-V-BI	63.80	57.20	50.60
DAC710KH	30.60	26.01	22.24
DAC711KH	30.60	26.01	22.24
DAC725AH	108.40	87.59	75.62
AH-BI	124.66	100.73	86.96
BH	134.52	127.30	99.56
BH-BI	154.70	146.40	114.49
JP	55.69	43.96	35.60
JP-BI	68.25	53.90	43.65
KP	66.40	52.53	44.98
KP-BI	81.40	64.40	55.10
SH	169.02	154.62	130.86
SH/QM	219.73	201.01	170.12
DAC729JH	179.00	157.00	141.00
JH-BI	196.90	172.70	155.10
KH	249.00	219.00	197.00
KH-BI	273.90	240.90	216.70
DAC72BH-COB-I	83.64	73.44	59.47
BH-COB-IBI	92.00	80.78	65.38
BH-COB-V	95.88	81.60	65.48
BH-COB-VBI	103.40	88.00	70.60
BH-CSB-I	83.64	73.44	59.47
BH-CSB-IBI	90.20	79.20	64.10
BH-CSB-V	95.88	81.60	65.48
BH-CSB-VBI	103.40	88.00	70.60
DAC7541AAH	11.09	9.09	6.73
AAH-BI	12.18	10.00	7.36
ABH	13.40	12.10	8.91
ABH-BI	14.80	13.31	9.79
AJP	9.40	7.80	5.70
AJP-BI	10.40	8.60	6.30
AJU	11.60	9.60	7.00
AKD			4.85
AKP	10.50	8.60	6.40
AKP-BI	11.50	9.40	7.00
AKU	12.90	10.60	7.80
ASH	29.64	24.18	18.00

MODEL	1-24	25-99	100
DAC7541ASH-BI	32.64	26.64	19.82
ATH	34.55	28.27	20.91
ATH-BI	38.00	31.18	23.00
DAC7545AH	14.60	11.90	8.80
AH-BI	16.10	13.10	9.80
BH	17.70	14.50	10.80
BH-BI	19.50	16.00	11.80
CH	19.20	15.80	11.70
CH-BI	21.20	17.40	12.80
GCH	28.50	17.30	14.30
GCH-BI	31.40	19.00	15.70
GLP	23.50	19.20	14.20
GLP-BI	25.80	21.20	15.60
GLU	26.20	22.10	16.40
GUH	80.80	66.10	49.00
GUH-BI	88.80	72.70	53.90
JP	11.20	9.20	6.80
JP-BI	12.30	10.10	7.50
JU	13.20	10.80	8.00
KP	14.70	12.00	8.90
KP-BI	16.20	13.20	9.80
KU	17.30	14.10	10.40
LP	16.10	13.10	9.70
LP-BI	17.70	14.50	10.70
LU	18.50	15.10	11.20
SH	41.40	33.90	20.60
SH-BI	45.60	37.30	22.70
TH	55.00	45.00	33.30
TH-BI	60.50	49.50	36.60
UH	59.60	48.80	36.10
UH-BI	65.60	53.70	39.70
DAC7700KD			18.37
DAC7701KD			18.37
DAC7802KP	15.95	14.05	12.35
LP	25.75	22.65	19.95
DAC80-CBI-I	27.40	17.60	14.30
-CBI-I-BI	30.20	19.40	15.70
-CBI-V	29.40	19.10	15.20
-CBI-V-BI	32.30	21.10	16.70
-CCD-V	43.35	38.76	26.52
DAC800-CBI-I	29.58	24.48	19.38
-CBI-V	31.62	26.52	21.42
DAC80KD-I			9.89
KD-V			9.89
MD-I			13.87
MD-V			14.96
P-CBI-V	22.80	16.60	14.00
P-CBI-V-BI	25.10	18.30	15.40
Z-CBI-I	28.56	23.63	15.30

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MODEL	1-24	25-99	100
DAC80Z-CBI-I-BI	30.80	25.50	16.50
Z-CBI-V	30.60	25.66	16.32
Z-CBI-V-BI	33.00	27.70	17.60
DAC811AH	24.60	16.00	14.80
AH-BI	27.00	17.70	16.30
BH	30.20	19.70	18.80
BH-BI	33.20	21.60	20.70
JD			10.12
JP	19.70	13.00	11.90
JP-BI	21.70	14.30	13.10
JU	21.20	14.30	13.50
KP	26.20	17.30	15.80
KP-BI	28.80	19.00	17.40
KU	28.00	18.50	17.20
RH	78.50	55.10	52.90
RH-BI	86.30	60.60	58.20
SH	129.20	92.70	85.80
SH-BI	142.00	102.10	94.30
DAC812BM	140.30	128.52	98.53
CM	187.43	142.44	129.59
DAC85H-CBI-I	41.97	30.09	25.45
H-CBI-I-BI	45.30	32.50	27.40
H-CBI-I/QM	52.17	37.59	31.82
H-CBI-V	44.52	32.39	27.18
H-CBI-V-BI	48.00	34.90	29.30
H-CBI-V/QM	56.00	40.49	34.12
DAC87-CBI-I	99.00	79.30	71.20
-CBI-I/B	106.05	85.85	75.50
-CBI-V	99.00	79.30	71.20
-CBI-V/B	106.05	85.85	77.25
DAC870V	80.80	75.75	67.70
V/883B	101.00	83.30	75.00
DAC87H-CBI-V	84.61	67.47	58.91
H-CBI-V-BI	91.20	72.80	63.50
H-CBI-V/QM	102.82	82.47	71.76
DIV100HP	38.80	29.45	20.80
JP	54.15	44.00	31.80
KP	77.40	63.00	45.65
HI-506KD			8.30
HI-507KD			8.30
HI-508KD			4.79
HI-509KD			4.79

MODEL	1-24	25-99	100
HI1-0506A-2	37.38	32.66	24.61
-2-BI	41.06	35.88	27.03
-5	19.32	16.91	12.77
-5-BI	21.16	18.52	14.03
HI1-0507A-2	37.38	32.66	24.61
-2-BI	41.06	35.88	27.03
-5	19.32	16.91	12.77
-5-BI	21.16	18.52	14.03
HI1-0508A-2	22.66	19.78	14.84
-2-BI	24.84	21.73	16.33
-5	10.81	9.43	7.59
-5-BI	11.85	10.35	8.28
HI1-0509A-2	22.66	19.78	14.84
-2-BI	24.84	21.73	16.33
-5	10.81	9.43	7.13
-5-BI	11.85	10.35	7.82
HI3-0506A-5	15.53	13.57	10.81
-5-BI	17.14	14.95	11.96
HI3-0507A-5	15.53	13.57	10.81
-5-BI	17.14	14.95	11.96
HI3-0508A-5	8.74	7.71	6.10
-5-BI	9.66	8.40	6.67
HI3-0509A-5	8.74	7.71	6.10
-5-BI	9.66	8.40	6.67
HPR1DD DUAL	12.00	10.70	8.25
SS SINGLE	12.00	10.70	8.25
INA101AD			5.05
AD/LAT			5.05
AG	20.00	14.75	11.80
AG-BI	25.95	19.20	15.30
AM	15.60	11.50	7.75
AM-BI	20.25	14.90	9.30
CG	25.60	18.80	17.50
CG-BI	33.30	24.50	22.75
CM	22.95	16.30	14.45
CM-BI	29.85	21.15	18.75
HP	8.20	6.20	5.45
HP-BI	9.80	7.75	7.00
KU	9.20	6.80	5.90
MD-B			10.40
SD			8.84
SG	30.85	21.85	19.85
SG-BI	40.10	28.40	25.80
SM	24.35	17.25	15.70
SM-BI	31.65	22.45	20.40
SMQ	36.25	26.20	24.25
VG	46.00	41.60	39.50

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MODEL	1-24	25-99	100
INA101VG/883B	49.50	44.75	42.50
VM	43.75	39.50	37.50
VM/883B	47.25	42.50	40.50
INA102AD			5.20
AG	15.55	12.15	8.50
AG-BI	20.20	15.80	10.05
AU	9.20	7.05	6.25
CG	22.95	18.70	12.75
CG-BI	29.85	24.35	16.60
INA102KP	8.50	6.50	5.75
KP-BI	10.05	8.05	7.30
INA103AG	22.25	16.20	12.15
BG	30.00	21.80	16.35
KP	12.70	9.25	6.90
INA104AM	31.70	23.75	20.75
BM	37.90	28.70	25.05
CM	48.90	36.85	32.25
SM	52.25	39.20	34.25
INA105AD			3.50
AM	10.60	7.80	6.15
AM-BI	13.80	9.35	7.70
BM	13.20	9.80	7.70
BM-BI	17.15	11.35	9.25
KP	6.95	5.10	3.75
KP-BI	8.55	6.65	5.30
KU	8.15	5.80	4.30
MD-B			7.86
SD			6.68
INA106AM	11.15	8.20	6.50
BM	13.85	10.25	8.10
KP	7.25	5.35	3.95
INA110AD			5.25
AD/LAT			5.25
AG	19.30	14.20	9.65
AG-BI	25.05	18.45	11.15
BG	30.25	21.55	14.20
BG-BI	39.35	28.00	18.40
KP	8.35	6.45	5.95
KP-BI	9.95	8.00	7.50
KU	10.00	7.40	6.65
MD-B			10.76
SD			9.15
SG	32.15	22.90	20.55
SG-BI	40.25	29.75	26.70
INA117AD			3.18
AD/LAT			3.18
AM	11.25	8.55	6.45
AM-BI	14.65	9.90	7.75

MODEL	1-24	25-99	100
INA117BM	15.60	11.85	8.90
BM-BI	20.30	15.30	10.50
KU	8.20	6.30	4.85
MD-B			8.50
P	7.10	5.45	4.20
P-BI	9.10	7.25	5.80
SD			7.22
SM	20.55	15.55	11.75
SM-BI	26.75	20.25	13.85
INA120AP	11.20	7.85	5.90
BG	17.40	12.15	9.15
BP	15.50	10.85	8.15
CG	28.10	19.70	14.80
SG	42.75	29.95	22.50
ISO100AP	40.50	33.90	28.65
BP	44.15	37.30	32.25
CP	49.25	42.80	37.80
ISO102	28.40	21.30	17.70
-BI	36.95	27.70	23.00
B	38.30	29.45	23.85
B-BI	47.90	38.25	31.00
ISO103	48.15	37.05	28.50
B	56.60	43.55	33.50
ISO106	37.85	29.05	23.55
-BI	47.35	37.80	30.65
B	51.10	39.25	31.90
-BI	63.85	49.10	39.85
ISO107	71.80	55.25	42.50
ISO108	27.45	21.15	16.25
ISO109	33.45	25.75	19.80
ISO113	48.15	37.05	28.50
B	56.60	43.55	33.50
ISO120BG	39.45	29.75	22.45
BG-BI	51.25	38.70	29.15
G	30.50	23.00	17.35
G-BI	39.65	29.90	22.55
ISO121BG	49.30	37.20	28.05
BG-BI	64.10	48.35	36.45
G	38.15	28.80	21.75
G-BI	49.60	37.45	28.25
ISO122P	18.30	13.80	10.45
ISO212JP	42.25	32.50	25.00
KP	49.00	37.70	29.00

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MODEL	1-24	25-99	100
LOG100JP	55.10	42.45	34.35
MC0068-1	14.00	14.00	14.00
MPC16S	24.84	21.47	18.21
MPC4D	13.87	12.04	10.15
MPC800KG	29.84	24.68	20.60
MPC801KG	15.56	12.85	10.71
MPC8D	24.35	21.05	17.85
S	13.60	11.75	9.95
MPY100AD			6.08
AG	17.30	15.25	13.10
AM	13.10	11.55	9.00
BG	28.00	24.15	18.45
BM	21.20	18.20	13.10
CG	42.05	36.55	29.55
CM	31.80	27.65	22.45
SG	63.00	54.85	36.00
SG/883B	97.00	80.85	67.35
SM	47.70	41.50	30.65
SM/883B	78.30	65.25	54.40
MPY534AD			9.38
AD/LAT			9.38
JD	37.10	30.10	21.40
JH	30.60	24.70	16.60
KD	50.00	41.55	30.10
KH	42.25	35.20	25.45
LD	79.50	65.00	47.70
LH	67.30	54.60	38.75
MD-B			19.20
SD	97.00	79.55	62.20
SD/883B	119.45	99.55	82.95
SH	86.90	70.20	54.55
SH/883B	106.40	88.65	73.85
TD	123.50	101.40	78.55
TD/883B	151.25	126.10	105.00
TH	113.95	90.50	70.90
TH/883B	133.45	111.15	92.65
MPY600AP	16.65	13.25	9.95
MPY634AM	22.75	17.90	12.25
BM	32.90	25.85	18.30
KP	16.80	13.15	9.40
KU	18.40	14.45	10.30
SD/883B	156.80	132.15	111.50
SH/883B	150.24	125.60	104.95
SM	81.45	64.40	46.60
SMQ	109.95	86.95	62.90

MODEL	1-24	25-99	100
OPA1013ACH	7.75	7.30	5.60
AMH	11.60	10.85	8.35
CH	4.60	4.35	3.35
CN8	4.00	3.65	2.80
DN8	3.15	3.00	2.30
MH	8.20	7.80	6.00
OPA101AM	48.95	38.25	28.70
BM	61.95	48.95	41.10
OPA102AM	51.80	40.65	29.95
BM	64.15	50.45	42.10
OPA103AM	13.45	10.45	7.85
BM	18.20	13.90	10.35
CM	23.85	18.00	13.35
DM	38.25	28.90	21.40
OPA104AM	22.40	16.95	11.85
BM	30.30	23.00	16.80
CM	37.85	28.50	22.00
OPA105UM	36.15	31.80	28.60
UM/883B	46.20	40.65	36.60
VM	56.20	49.45	44.50
VM/883B	66.15	58.20	52.40
WM	69.60	61.25	55.15
WM/883B	79.70	70.15	63.15
OPA106UM	48.45	42.65	38.40
UM/883B	56.20	49.45	44.50
VM	60.80	53.50	48.15
VM/883B	74.65	65.70	59.15
WM	80.85	71.15	64.05
WM/883B	94.75	83.40	75.05
OPA111AD			4.20
AD/LAT			4.20
AM	12.50	9.65	6.30
AM-BI	16.25	11.25	7.85
BM	21.60	16.35	12.65
BM-BI	28.10	21.20	16.40
MD-B			12.79
SD			9.21
SM	25.55	19.35	15.90
SM-BI	33.25	25.15	20.70
SMQ	33.05	26.45	21.25
VM	27.30	21.50	17.85
VM/883B	36.75	31.50	28.35
OPA121KM	7.80	5.00	3.70
KM-BI	9.40	6.55	5.25
KP	6.40	4.05	3.00
KP-BI	8.00	5.60	4.55
KU	8.80	4.75	3.45

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MODEL	1-24	25-99	100
OPA128JD			7.78
JD/LAT			7.78
JM	13.75	11.10	9.15
JM-BI	17.85	14.40	10.65
KM	19.25	15.50	12.75
KM-BI	25.00	20.10	16.60
LM	23.85	19.20	15.75
LM-BI	31.00	24.95	20.50
MD-B			15.95
SD			13.55
SM	50.00	40.20	33.15
SM-BI	62.50	50.25	41.45
SM/883B	65.25	57.10	51.40
OPA156AD			4.96
AM	14.30	10.75	7.75
OPA2107AD			6.84
AM	13.45	10.20	8.05
AM-BI	15.45	11.75	9.25
AP	10.80	7.50	5.70
AP-BI	12.40	8.65	6.55
AU	12.40	8.65	6.55
BM	19.20	13.95	10.90
BM-BI	22.10	16.05	12.55
SD			11.90
SM	34.65	25.95	19.80
SM-BI	39.85	29.85	22.75
OPA2111AD			7.59
AD/LAT			7.59
AM	18.60	13.95	11.55
AM-BI	24.15	18.10	15.00
BM	33.30	25.25	19.05
BM-BI	41.60	32.85	24.80
KM	11.25	8.80	5.70
KM-BI	14.65	10.35	7.25
KP	8.95	6.15	4.65
KP-BI	10.55	7.70	6.15
MD-B			15.56
SD			13.22
SM	33.95	25.75	19.40
SM-BI	42.45	33.50	25.20
SM/883B	49.60	42.50	38.25
OPA21GD			2.20
GD/LAT			2.20
MD-B			4.51
SD			3.83
OPA2541AM	53.80	38.25	29.55
AM-BI	64.55	47.85	38.40
BM	63.35	45.10	34.85
BM-BI	76.00	56.35	43.55
SM	90.95	64.95	50.20
SM-BI	109.15	77.95	62.75

MODEL	1-24	25-99	100
OPA27AJ	27.05	18.95	14.85
AZ	27.05	18.95	14.85
BJ	13.55	9.50	7.75
BZ	13.55	9.50	7.75
CD			4.05
CJ	10.70	7.45	5.95
CZ	10.70	7.45	5.95
EJ	11.80	8.25	6.75
EZ	11.80	8.25	6.75
FJ	8.50	5.95	4.75
FZ	8.50	5.95	4.75
GD			2.70
GJ	6.65	4.65	3.60
GP	2.80	1.95	1.55
GU	5.30	3.70	2.95
GZ	6.65	4.65	3.60
HT	71.15	57.65	45.00
MD-B			5.74
OPA356AM	9.20	7.20	5.15
OPA37AJ	27.05	18.95	14.85
AZ	27.05	18.95	14.85
CD			4.05
CJ	10.70	7.45	5.95
CZ	10.70	7.45	5.95
EJ	11.80	8.25	6.75
EZ	11.80	8.25	6.75
FJ	8.50	5.95	4.75
FZ	8.50	5.95	4.75
GD			2.70
GJ	6.65	4.65	3.60
GP	2.80	1.95	1.55
GU	5.30	3.70	2.95
GZ	6.65	4.65	3.60
MD-B			5.74
OPA404AD			6.44
AG	18.65	14.75	10.05
BG	24.65	18.55	14.45
KP	12.55	9.60	7.10
KU	14.45	11.10	8.10
SG	36.45	27.40	22.45
OPA445AD			3.44
AP	7.15	5.15	3.90
BM	7.35	5.40	4.05
SM	25.25	19.30	13.50
SM/883B	56.25	50.65	46.85
OPA501AM	66.55	47.15	36.55
BM	78.55	56.40	42.60
RM	85.40	58.10	47.80
SM	102.25	70.55	56.15
VM	100.80	88.70	79.80
VM/883B	105.00	92.40	82.95

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MODEL	1-24	25-99	100
OPA511AM	50.10	42.05	37.00
OPA512BM	70.70	58.90	51.95
SM	85.15	72.65	65.90
SMQ	123.00	106.90	98.90
OPA541AD			17.70
AD/LAT			17.70
AM	32.85	23.35	18.05
AM-BI	41.10	30.35	23.45
AP	16.40	12.90	9.95
AP-BI	21.25	16.75	12.90
BM	38.70	27.50	21.25
BM-BI	48.40	35.80	27.65
MD-B			29.65
SD			24.75
SM	56.60	40.40	31.20
SM-BI	67.95	50.50	39.00
SM/883B	115.30	100.90	90.80
OPA600BM	103.89	86.75	79.25
CM	127.45	108.17	103.89
VM	183.75	160.65	150.15
VM/BBC	204.75	184.80	171.15
OPA602AD			3.22
AD/LAT			3.22
AM	7.50	5.35	4.15
AM-BI	8.95	6.75	5.50
AP	4.60	2.95	2.40
AP-BI	6.20	4.50	3.95
AU	5.30	3.45	2.75
BM	11.70	8.30	6.45
BM-BI	15.20	9.90	7.95
BP	6.90	5.15	4.05
BP-BI	8.50	6.70	5.55
CM	17.05	12.15	9.40
CM-BI	22.20	15.80	10.90
MD-B			6.60
SD			5.61
SM	27.25	19.45	15.00
SM-BI	35.40	25.25	19.50
SM/883B	53.00	47.70	44.15
OPA605AM	87.15	67.85	57.65
CM	121.15	92.85	80.15
OPA606KD			2.54
KM	7.10	5.15	3.95
KP	4.65	3.40	2.80
LM	17.30	11.75	9.30
SM	17.75	12.05	9.60

MODEL	1-24	25-99	100
OPA620AD			14.00
AD/LAT			14.00
KG	20.20	16.75	14.75
KP	13.65	11.30	9.95
KU	13.85	11.50	10.15
LG	27.50	22.80	20.10
MD-B			28.70
SD			21.70
SG	43.80	36.35	32.00
OPA621AD			14.00
AD/LAT			14.00
KG	20.20	16.75	14.75
KP	13.65	11.30	9.95
KU	13.85	11.50	10.15
LG	27.50	22.80	20.10
MD-B			28.70
SD			21.70
SG	43.80	36.35	32.00
OPA627AD			14.45
AD/LAT			14.45
AM	14.80	10.75	8.45
AP	13.15	9.55	7.50
AU	15.10	11.00	8.65
BM	26.15	19.00	14.95
BP	22.60	16.45	12.95
SD			24.80
SM	49.90	37.00	29.15
OPA633AD			2.94
AD/LAT			2.94
KP	7.05	5.80	4.70
KP-BI	8.65	7.40	6.20
MD-B			9.25
SD			7.86
OPA637AD			14.45
AD/LAT			14.45
AM	14.80	10.75	8.45
AP	13.15	9.55	7.50
AU	15.10	11.00	8.65
BM	26.15	19.00	14.95
BP	22.60	16.45	12.95
SD			24.80
SM	49.90	37.00	29.15
OPA675JD			40.00
JD/LAT			40.00
JG	29.78	25.35	22.80
KG	40.55	34.48	31.01
SD			54.00
SG	64.57	54.88	49.42

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MODEL	1-24	25-99	100
OPA676JD			40.00
JD/LAT			40.00
JG	29.78	25.35	22.80
KG	40.55	34.48	31.01
SD			54.00
SG	64.57	54.88	49.42
PC862/863-1	16.00	16.00	16.00
-2	16.00	16.00	16.00
PCM1700P	27.05	23.80	0.00
-J	31.30	27.55	24.25
-K	42.00	36.95	32.50
U	27.05	23.80	20.95
U-J	31.30	27.55	24.25
-K	42.00	36.95	32.50
PCM53JP-I	21.50	18.90	16.65
JP-V	21.50	18.90	16.65
KP-I	28.50	25.10	22.10
KP-V	28.50	25.10	22.10
PCM54HP	17.10	15.05	13.25
JP	19.70	17.35	15.25
KP	25.75	22.65	19.95
PCM55HP	17.10	15.05	13.25
JP	19.70	17.35	15.25
PCM56P	17.10	15.05	13.25
-J	19.70	17.35	15.25
-K	25.75	22.65	19.95
PCM58P	26.60	23.40	20.60
-J	30.35	26.70	23.50
-K	36.95	32.50	28.60
PCM60P	22.65	19.95	17.55
-J	26.20	23.05	20.30
PCM61P	18.15	15.95	14.05
-J	20.95	18.45	16.25
-K	28.50	25.10	22.10
PCM64P	39.70	34.95	30.75
PCM66P	22.65	19.95	17.55
-J	26.20	23.05	20.30
PCM75JG	140.30	122.09	93.18
KG	159.58	138.16	106.03
PCM78P	42.00	36.95	32.50
PGA100AG	83.30	66.70	57.25
AG-BI	99.95	80.10	68.75

MODEL	1-24	25-99	100
PGA100BG	92.35	75.20	62.50
BG-BI	110.75	90.20	74.95
PGA102AD			3.57
AG	14.05	10.90	8.80
AG-BI	18.30	14.20	10.35
BG	25.60	19.70	15.90
BG-BI	33.30	25.65	20.70
KP	7.65	5.75	4.60
KP-BI	9.20	7.35	6.10
SG	31.30	24.20	19.40
SG-BI	40.70	31.45	25.20
PGA200AG	66.05	48.45	40.20
AG-BI	79.25	60.60	50.25
BG	74.15	56.75	47.45
BG-BI	89.00	68.05	59.30
PGA201AG	66.05	48.45	40.20
AG-BI	79.25	60.60	50.25
BG	74.15	56.75	47.45
BG-BI	89.00	68.05	59.30
PGA202AG	16.75	12.90	9.90
BG	21.90	16.85	12.95
KP	11.75	9.05	6.95
PGA203AG	16.75	12.90	9.90
BG	21.90	16.85	12.95
KP	11.75	9.05	6.95
PWS725A	40.05	30.25	22.80
PWS726A	49.60	37.45	28.25
PWS727	28.75	22.10	17.00
PWS728	28.75	22.10	17.00
PWS740-1	22.25	17.25	13.00
-2	4.45	3.40	2.55
-3	2.25	1.65	1.30
PWS750-1	5.90	4.55	3.50
-2	6.45	4.95	3.80
-3	2.30	1.75	1.35
-4	6.45	4.95	3.80
RCV420AG	12.50	9.45	7.15
BG	15.20	11.50	8.65
KP	8.05	6.10	4.60
REF101JM	39.25	33.40	25.80
KM	48.90	42.05	33.00
RM	42.90	36.90	28.85
SM	53.80	46.80	37.15

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MODEL	1-24	25-99	100
REF101SMQ	77.75	68.65	56.85
REF102AM	6.35	4.90	3.75
AP	4.65	3.60	2.75
AU	5.30	4.10	3.15
BM	9.00	6.90	5.30
BP	6.10	4.65	3.60
CM	12.00	9.25	7.10
RM	15.20	11.70	9.00
SM	23.65	18.20	14.00
REF10JM	22.10	18.80	15.30
KM	30.60	26.40	21.95
RM	25.35	21.60	17.60
SM	37.35	31.65	25.80
SMQ	54.05	46.40	39.40
REF200AM	5.65	4.35	3.45
AM-BI	7.25	5.95	5.00
AP	4.55	3.30	2.50
AP-BI	6.15	4.85	4.05
AU	5.25	3.80	2.85
SDM854AG	266.02	212.82	178.60
BG	295.19	236.90	197.63
SDM856JG	229.30	183.70	153.31
KG	277.44	221.70	186.20
SDM857JG	245.77	196.35	164.68
KG	293.91	235.62	196.35
SDM862AH	119.00	101.50	84.00
AL	119.00	101.50	84.00
BH	229.00	199.00	169.00
BL	229.00	199.00	169.00
JH	99.00	84.00	69.00
JL	99.00	84.00	69.00
KH	179.00	154.00	129.00
KL	179.00	154.00	129.00
RH	139.00	119.00	99.00
RH/QM	199.00	169.00	139.00
RL	139.00	119.00	99.00
RL/QM	199.00	169.00	139.00
SH	329.00	299.00	269.00
SH/QM	459.00	419.00	379.00
SL	329.00	299.00	269.00
SL/QM	459.00	419.00	379.00
SDM863AH	119.00	101.50	84.00
AL	119.00	101.50	84.00
BH	229.00	199.00	169.00
BL	229.00	199.00	169.00
JH	99.00	84.00	69.00
JL	99.00	84.00	69.00
KH	179.00	154.00	129.00
SDM863KL	179.00	154.00	129.00
RH	139.00	119.00	99.00
RH/QM	199.00	169.00	139.00
RL	139.00	119.00	99.00
RL/QM	199.00	169.00	139.00
SH	329.00	299.00	269.00
SH/QM	459.00	419.00	379.00
SL	329.00	299.00	269.00
SL/QM	459.00	419.00	379.00
SDM872AH	136.85	116.73	96.60
AL	136.85	116.73	96.60
BH	263.35	228.85	194.35
BL	263.35	228.85	194.35
JH	113.85	96.60	79.35
JL	113.85	96.60	79.35
KH	205.85	177.10	148.35
KL	205.85	177.10	148.35
RH	159.85	136.85	113.85
RH/QM	228.85	194.35	159.85
RL	159.85	136.85	113.85
RL/QM	228.85	194.35	159.85
SH	378.35	343.85	309.35
SH/QM	527.85	481.85	435.85
SL	378.35	343.85	309.35
SL/QM	527.85	481.85	435.85
SDM873AH	136.85	116.73	96.60
AL	136.85	116.73	96.60
BH	263.35	228.85	194.35
BL	263.35	228.85	194.35
JH	113.85	96.60	79.35
JL	113.85	96.60	79.35
KH	205.85	177.10	148.35
KL	205.85	177.10	148.35
RH	159.85	136.85	113.85
RH/QM	228.85	194.35	159.85
RL	159.85	136.85	113.85
RL/QM	228.85	194.35	159.85
SH	378.35	343.85	309.35
SH/QM	527.85	481.85	435.85
SL	378.35	343.85	309.35
SL/QM	527.85	481.85	435.85
SHC298AJP	6.30	5.25	4.25
AJP-BI	7.20	6.00	4.90
AM	8.35	5.80	4.75
AM-BI	9.60	6.70	5.50
JP	3.99	3.15	2.57
JP-BI	4.56	3.60	2.97
JU	4.33	3.61	2.98
SHC5320KD			11.70
KH	13.60	11.80	8.90
KP	12.70	11.00	8.30
SH	34.20	29.50	26.60

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MODEL	1-24	25-99	100
SHC600BH	270.00	256.00	235.00
BHQ	356.00	345.00	315.00
SHC601BH	218.00	207.00	190.00
SHC702JM	202.00	187.00	168.00
SHC76BM	106.03	80.33	67.47
BM-BI	119.50	90.60	76.10
KM	91.09	69.72	58.50
KM-BI	102.70	78.60	66.00
SHC803BM	186.35	144.59	131.73
CM	216.34	163.86	149.94
SHC804BM	171.36	129.59	117.81
BMQ	212.06	161.72	146.73
CM	187.43	141.37	129.59
CMQ	234.55	177.79	161.72
SHC85	124.13	86.14	72.22
ET	187.48	139.33	134.28
UAF21	117.45	98.95	64.65
41	26.70	17.10	13.30
VFC100AD			4.90
AG	11.60	9.50	7.45
BG	18.25	14.90	11.75
SG	21.10	17.40	14.65
VFC101AD			4.90
JN	14.80	11.35	8.75
KN	19.30	13.75	11.40
SD			8.54
VFC110AG	19.05	13.70	10.15
AP	14.50	10.30	8.10
BG	23.55	16.90	13.45
SG	26.90	19.35	16.10
VFC121AP	12.15	9.55	7.35
BP	16.40	12.95	9.95
VFC320AD			7.05
BG	17.75	12.85	9.60
BM	17.40	12.45	9.40
CG	23.05	16.10	12.95
CM	20.65	14.65	11.75
SD			12.28
SM	26.25	18.75	15.35
VFC32BD			5.55
BM	12.65	10.35	8.10
KP	9.50	7.75	6.05
KU	10.90	9.10	7.10
MD-B			11.38
SD			9.67
SM	19.40	15.60	12.10
SMQ	27.15	22.30	17.60
VM	24.25	19.70	18.70
VM/883B	36.35	29.05	27.52
WM	30.30	24.25	22.95
WM/883B	34.35	27.75	26.25
VFC42BM	37.70	30.20	25.15
SM	45.75	36.05	28.25
SMQ	68.80	55.30	44.20
VFC52BM	37.70	30.05	25.15
VFC62BG	19.90	13.85	10.05
CG	24.70	16.70	13.55
XTR101AD			5.61
AG	13.30	10.85	9.05
AG-BI	17.30	14.15	11.75
AP	9.65	7.85	6.50
AP-BI	11.25	9.40	8.00
AU	10.20	8.20	6.85
BG	19.65	16.05	13.35
BG-BI	25.55	20.90	17.40
XTR110AD			4.95
AG	12.30	9.70	8.10
AG-BI	16.00	11.30	9.65
BG	18.45	14.55	12.15
BG-BI	23.95	18.95	15.75
KP	8.45	6.60	5.40
KP-BI	10.00	8.15	6.95
KU	9.55	7.30	5.90

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